Integrated Device Technology, Inc.

HIGH PERFORMANCE CMOS DATA BOOK

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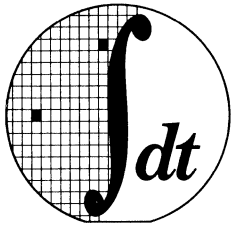

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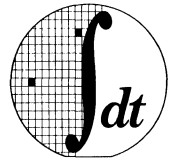

Integrated Device Technology, Inc.

HIGH-SPEED CMOS DATA BOOK

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CONTENTS OVERVIEW

This book has been organized into sections by product families, with additional sections providing numerous aids to assist in a better understanding of our high-performance CMOS devices. These include descriptions of IDT's commitment to providing the highest levels of technology, quality and service in the industry; our CEMOS™ and surface mount technologies; facilities and capabilities; product selector guides; article reprints; application and technical notes; quality flows and testing; package-related data and ordering information. Two separate indexes have also been provided to ensure ease of use of this data book. One is organized by product line and function within the product line; the other is a numerical index. As a further aid, industry cross reference guides are provided by product family.

Three different types of data sheets are contained in this book:

ADVANCE INFORMATION — Contain initial descriptions for products that are in development, including features, pinouts and block diagrams.

PRELIMINARY — Contain minimum and maximum limits, based upon initial device characterization, which are subject to change upon full characterization over the specified supply and temperature range.

FINAL — Contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative or call our factory at 1-800-IDT-CMOS to determine latest device specifications, package types and product availability.

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High-Speed CMOS MICROSLICE™ Products

- CMOS microprogrammable bit-slice microprocessor family
- Meets or exceeds bipolar speeds and output drive at a small fraction of the power consumption
- Sequential letter suffix designates 20%-40% speed upgrade
- Instruction set/operation codes functionally identical to 2900 family
- IDT39C000 products are pin-compatible, performance-enhanced 2900 family replacements
- IDT49C000 products offer dramatically improved system performance through new innovative architectures
- Available in military and commercial temperature ranges
- Produced with advanced CEMOS™ high-performance technology

	Part Number	Description	Replaces	Oper. Power (max) (mW) Com'l.	Mil.	Availability	Page No.
MICROPROCESSORS	IDT39C01C IDT39C01D IDT39C01E	4-Bit μP Slice	Am2901B,C; Am29C01C; IDM2901A,-2; SFC2901B,C; CY7C901	105	165	NOW	3-1
	IDT39C03A IDT39C03B	4-Bit μP Slice	Am2903, SFC2903	265	330	NOW	3-15
	IDT39C203 IDT39C203A	4-Bit μP Slice	Am29203	265	330	NOW	3-71
	IDT49C401 IDT49C401A	16-Bit μP Slice	IMI4X2901B	660	825	NOW	3-103
	IDT49C402 IDT49C402A	16-Bit μP Slice, Quad 2901 with 8 additional destination functions and a 64 × 16 dual-port memory capacity	UNIQUE	660	825	NOW	3-113
	IDT49C403 IDT49C403A	16-Bit μP Slice, Quad 2903/ 29203 with 64 × 16 register file, 4 Q-registers, word/BYTE control, BYTE swap, cascadeable	UNIQUE	660	825	NOW	3-124
	IDT49C404 IDT49C404A	32-Bit μP Slice, 3-port device with 32-Bit ALU, 64 × 32 register file, cascadeable funnel shifter, priority encoder, merge logic and mask generator	UNIQUE	3500	4000	Q4 '86	3-126
SEQUENCERS	IDT39C09A IDT39C09B	4-Bit Sequencer	Am2909A; CY7C909; SFC2909; LM2909	130	165	NOW	3-47
	IDT39C10B IDT39C10C	12-Bit Sequencer with 33-Deep Stack	Am2910A; CY7C910; SFC2910; IDM2910	395	495	NOW	3-61
	IDT39C11A IDT39C11B	4-Bit Sequencer	Am2911A; CY7C911; SFC2911A; IDM2911A	130	165	NOW	3-47
	IDT49C410 IDT49C410A	16-Bit Sequencer with 33-Deep Stack	UNIQUE	395	495	NOW	3-128
REGISTER FILES	IDT39C705A IDT39C705B	16 × 4 Register File Extension	Am29705A	105	165	NOW	3-99
	IDT39C707 IDT39C707A	16 × 4 Register File Extension	Am29707	105	165	NOW	3-99
	IDT49C470 IDT49C470A	64 × 16 Register File	UNIQUE	—	—	Q4 '86	*
EDC	IDT39C60 IDT39C60-1 IDT39C60A	16-Bit Cascadeable Error Detection Correction Unit	Am2960-1,A; N2960	450	550	NOW	3-73
	IDT49C460 IDT49C460A	32-Bit Cascadeable Error Detection Correction Unit	UNIQUE	500	690	NOW	3-138
OTHER	IDT39C02A	Carry Lookahead Generator	Am2902A	30	30	NOW	3-12
	IDT49C25	Clock Generator	Am2925	30	30	NOW	3-101

*Contact Factory

High-Speed CMOS Static RAMs

- Extremely fast access times
- Low power consumption
- 2V data retention battery backup on all low-power devices
- Three-state outputs
- 'M' type ceramic RAM modules are built with IDT monolithic RAMs in LCC packages surface mounted onto multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process
- 'MP' type commercial plastic modules are built using IDT monolithic RAMs in SMD plastic packages, surface mounted onto epoxy laminate (FR4) substrates

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)	Availability	Page No.
IDT6116A	16K (2K × 8)	35	30	250	30	NOW	2-1
IDT6120	16K (2K × 8) with high-speed chip select (chip select access time)	20	18	200	—	Q4 '86	*
IDT6167A	16K (16K × 1)	20	15	200	10	NOW	2-8
IDT6168A	16K (4K × 4)	25	20	225	10	NOW	2-15
IDT6169	16K (4K × 4) with high-speed chip select (chip select access time)	15	12	225	—	Q4 '86	
IDT71681A	16K (4K × 4) with separate data inputs and outputs; outputs track inputs during write mode	25	20	225	10	NOW	2-73
IDT71682A	16K (4K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode	25	20	225	10	NOW	2-73
IDT7164	64K (8K × 8)	45	30	300	30	NOW	2-59
IDT7165	64K (8K × 8) with asynchronous clear and high-speed chip select	45	30	300	30	NOW	2-67
IDT7174	64K (8K × 8) with cache address comparator, asynchronous clear and high-speed chip select	45	35	300	—	NOW	2-82
IDT7187	64K (64K × 1)	30	25	250	30	NOW	2-89
IDT7188	64K (16K × 4)	30	25	300	30	NOW	2-95
IDT7198	64K (16K × 4) output enable ($\overline{OE}$) and second chip select ($\overline{CS_2}$) for added system flexibility and memory control	30	25	300	30	NOW	2-101
IDT71981	64K (16K × 4) with separate data inputs and outputs; outputs track inputs during write mode	30	25	300	30	NOW	2-108
IDT71982	64K (16K × 4) with separate data inputs and outputs; outputs in high impedance state during write mode	30	25	300	30	NOW	2-108
IDT71256	256K (32K × 8)	55	45	350	100	Q4 '86	2-23
IDT71257	256K (256K × 1)	45	35	350	100	Q1 '87	2-25
IDT71258	256K (64K × 4)	45	35	350	100	Q1 '87	2-27
IDT7M864	64K (8K × 8) RAM module with static RAM pinout	75	65	325	80	NOW	7-55
IDT8M864	64K (8K × 8) RAM module with EPROM pinout	75	65	325	80	NOW	7-55
IDT8M628	128K (8K × 16) RAM module with monolithic pinout	60	50	750	750	Q4 '86	7-68
IDT8MP628	128K (8K × 16) plastic SIP RAM module	—	50	750	750	NOW	7-62
IDT7M656	256K (16K × 16, 32K × 8, 64K × 4) RAM module – customer configurable organization	35	25	2000	1500	NOW	7-35

*Contact Factory

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High-Speed CMOS Static RAMs (continued)

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)	Availability	Page No.
IDT7M856	256K (32K × 8) RAM module with monolithic pinout	55	50	950	1000	NOW	7-49
IDT8M856	256K (32K × 8) RAM module with monolithic pinout (low-power)	55	50	350	500	NOW	7-77
IDT8M656	256K (16K × 16) RAM module with monolithic pinout	60	50	1000	1000	Q4 '86	7-68
IDT8MP656	256K (16K × 16) plastic SIP RAM module	—	50	1000	1000	NOW	7-62
IDT7M812	512K (64K × 8) RAM module offering maximum addressable memory required by 8-bit MPs	55	45	1800	900	NOW	7-41
IDT7M912	512K (64K x 9) RAM module offering maximum addressable memory required by 8-bit MPs	55	45	1800	900	NOW	7-41
IDT8M612	512K (32K × 16) RAM module with monolithic pinout	75	60	1000	300	Q1 '87	7-66
IDT8MP612	512K (32K × 16) plastic SIP RAM module	—	60	1000	300	Q4 '86	7-60
IDT7M624	1 Megabit (64K × 16, 128K × 8, 256K × 4) RAM module – customer configurable organization	40	30	2000	1600	NOW	7-29
IDT7MP624	1 Megabit (64K × 16, 128K × 8, 256K × 4) plastic RAM module – customer configurable organization	—	30	2000	1600	Q4 '86	7-1
IDT8M824	1 Megabit (128K × 8) RAM module with monolithic pinout	75	60	500	150	Q1 '87	7-75
IDT8MP824	1 Megabit (128K × 8) plastic SIP RAM module	—	60	500	150	Q4 '86	7-64
IDT7M824	1 Megabit (128K × 8) RAM module with registered buffered/latched addresses and I/Os	75	65	950	1600	NOW	7-46
IDT8M624	1 Megabit (64K × 16) RAM module with monolithic pinout	75	60	1000	300	Q1 '87	7-66
IDT8MP624	1 Megabit (64K × 16) plastic SIP RAM module	—	60	1000	300	Q4 '86	7-66

High-Speed CMOS Dual-Port RAMs

- High-speed, low-power
- Independent read or write access to any memory location from either port
- Each port has separate controls, address and I/O
- On-chip port arbitration logic
- Fully asynchronous operation from either port
- $\overline{INT}$ and $\overline{BUSY}$ flags ($\overline{BUSY}$ only in IDT7132/7142)
- Automatic power-down feature controlled by $\overline{CE}$
- 2V data retention battery back-up on all low-power devices
- Dual-port RAM modules built with IDT monolithic dual-port RAMs in LCC packages, surface mounted to multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (mW)	Availability	Page No.
IDT7130	8K (1K × 8) replaces Synertek SY2130	70 55	55 45	325	1	NOW Q4 '86	2-29
IDT7132	16K (2K × 8) largest monolithic dual-port static RAM available in the industry	70 55	55 45	325	1	NOW Q4 '86	2-41
IDT7140	8K (1K × 8) functions as slave with IDT7130 to provide 16-bit words or wider; pin compatible with IDT7130	70 55	55 45	325	1	NOW Q4 '86	2-29
IDT7142	16K (2K × 8) functions as slave with IDT7132 to provide 16-bit words or wider; pin compatible with IDT7132	70 55	55 45	325	1	NOW Q4 '86	2-41
IDT71322	16K (2K × 8) with Semaphore	55	45	325	1	Q1 '87	2-51
IDT7133	32K (2K × 16)	90	70	325	1	Q4 '86	2-53
IDT7134	32K (4K × 8) high-speed operation in system where on-chip arbitration is not needed	55	45	325	1	Q1 '87	2-55
IDT71341	32K (4K × 8) with Semaphore	55	45	325	1	Q1 '87	2-57
IDT7143	32K (2K × 16) functions as slave with IDT7133 to provide 32-bit words or wider	90	70	325	1	Q4 '86	2-53
IDT7M134	64K (8K × 8) dual-port RAM module	90	70	950	20	NOW	7-3
IDT7M135	128K (16K × 8) dual-port RAM module	90	70	1600	50	NOW	7-3
IDT7M136	128K (16K × 8) functions in system where on-chip arbitration is not needed	80	60	1000	30	Q1'87	7-13
IDT7M137	256K (32K × 8) dual-port RAM module where on-chip arbitration is not needed	80	60	1800	60	Q1'87	7-13
IDT7M144	64K (8K × 8) functions as slave with IDT7M134 to provide 16-bit words or wider; pin compatible with IDT7M134	90	70	950	20	NOW	7-15
IDT7M145	128K (16K × 8) functions as slave with IDT7M135 to provide 16-bit words or wider; pin compatible with IDT7M135	90	70	1600	50	NOW	7-15

High-Speed CMOS FIFOs

- Extremely fast access and cycle times
- Low-power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Single read/write line operation
- Empty, full and half-full flags indicate status
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Auto retransmit capability
- FIFO modules are built with IDT monolithic FIFOs in LCC packages, surface mounted to multi-layered, co-fired ceramic substrates using IDT's high-reliability vapor phase reflow soldering process

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (mW)	Availability	Page No.
IDT7201	512 × 9 replaces Mostek MK4501	40	35	250	25	NOW	4-11
IDT7202	1024 × 9 largest monolithic FIFO available in the industry	40	35	250	25	NOW	4-11
IDT7201A	512 × 9 half-full flag	40	35	250	25	NOW	4-1
IDT7202A	1024 × 9 half-full flag	40	35	250	25	NOW	4-1
IDT7203	2K × 9 half-full flag	50	50	600	100	Q4 '86	4-21
IDT7204	4K × 9 half-full flag	50	50	600	100	Q4 '86	4-21
IDT72103	2K × 9 serial input. Half-full, almost-full, almost-empty flags	50	50	600	100	Q4 '86	4-50
IDT72104	4K × 9 serial input. Half-full, almost-full, almost-empty flags	50	50	600	100	Q4 '86	4-50
IDT72401	64 × 4 replace MMI 67401	60	50	200	20	Q1'87	4-75
IDT72402	64 × 5 replace MMI 67402	60	50	200	20	Q1'87	4-75
IDT72403	64 × 4 output enable	60	50	200	20	Q1'87	4-75
IDT72404	64 × 5 output enable	60	50	200	20	Q1'87	4-75
IDT72413	64 × 5 replace MMI 67413 output enable	50	30	200	20	Q1'87	4-77
IDT7M203	2K × 9 FIFO module using four IDT7201s	50	40	630	100	NOW	7-18
IDT7M204	4K × 9 FIFO module using four IDT7202s	50	40	630	100	NOW	7-18
IDT7M205	8K × 9 FIFO module using four IDT7203s	65	60	1400	400	Q4'86	7-28
IDT7M206	16K × 9 FIFO module using four IDT7204s	65	60	1400	400	Q4'86	7-28

High-Speed CMOS Parallel Multiplier-Accumulators

- High-speed, low-power
- Parallel multiplier-accumulators with selectable accumulation, rounding and preloading
- Extended product output for multiple accumulations
- Preload function allows output register to be preset
- All devices perform subtraction and double precision addition and multiplication
- Inputs and outputs directly TTL-compatible

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μmW)	Availability	Page No.
IDT7209	12 × 12-pin and functionally compatible with TRW TDC1009J	40	30	200	500	NOW	4-35
IDT7210	16 × 16-with 35-bit output; pin and functionally compatible with TRW TDC1010J	40	35	200	500	NOW	4-42
IDT7243	16 × 16-with 19-bit output; pin and functionally compatible with TRW TDC1043	40	35	200	500	NOW	4-42

High-Speed CMOS Parallel Multipliers

- High-speed, low-power
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Inputs and outputs directly TTL-compatible
- Three-state output controls and separate register enables

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)	Availability	Page No.
IDT7212	12 × 12-pin and functionally compatible with TRW MPY012H	40	30	150	500	NOW	4-52
IDT7213	12 × 12-with single clock architecture	40	30	150	500	NOW	4-52
IDT7216	16 × 16-pin and functionally compatible with TRW MPY016H/K and AMD Am29516	40	35	150	500	NOW	4-61
IDT7217	16 × 16-with single clock architecture; pin and functionally compatible with AMD Am29517	40	35	150	500	NOW	4-61

High-Speed CMOS Floating Point Products

- Advanced CEMOS technology
- Full IEEE standard 754 conformance
- Single 5V supply
- Full 32-bit and 64-bit multiply and ALU operations
- 144-Pin Grid Array
- Low-power – 750mW per device

Part Number	Description	Max. Speed (ns)	Power (typical) Oper. (mW)	Availability	Page No.
IDT72064	64-Bit Multiplier-pin and functionally compatible with Weitek WTL1064	Single precision 5 MFLOPS (200) Double precision 2.5 MFLOPS (400)	750	Q4 '86	4-31
IDT72065	64-Bit ALU-pin and functionally compatible with Weitek WTL1065	Single precision 10 MFLOPS (100) Double precision 10 MFLOPS (100)	750	Q4 '86	4-31
IDT72264	64-Bit Multiplier-pin and functionally compatible with Weitek WTL1264	Single precision 10 MFLOPS (100) Double precision 5 MFLOPS (200)	750	Q4 '86	4-71
IDT72265	64-Bit ALU-pin and functionally compatible with Weitek WTL1265	Single precision 10 MFLOPS (100) Double precision 10 MFLOPS (100)	750	Q4 '86	4-71

High-Speed CMOS Logic Products

- FCTXXXA devices 35%-50% faster than FAST™ with equivalent output drive but at dramatically lower CMOS power over full temperature and voltage supply extremes
- FCT devices same speed and output drive as FAST™, but at dramatically lower CMOS power
- AHCT devices same speed and output drive as ALS, but at dramatically lower CMOS power
- 39C8XX devices same speed and output drive as 29800, but at dramatically lower CMOS power
- 54/74 FCT8XXB devices 32%-38% faster than 29800 with equivalent output drive, but at dramatically lower CMOS power
- Both CMOS and TTL output compatible (eliminates need for pull-up resistors when driving CMOS static RAMs)
- Substantially lower input current levels than FAST™ or ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Pin-compatible with industry standard MSI logic

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)	Availability	Page No.
IDT54/74FCT138A	1-of-8 Decoder	7.8	5.8	10.0	5.0	NOW	5-98
IDT54/74FCT139A	Dual 1-of-4 Decoder	7.8	5.9	10.0	5.0	NOW	5-102
IDT54/74FCT161A	Synchronous Binary Counter	7.5	7.2	10.0	5.0	Q4 '86	5-105
IDT54/74FCT163A	Synchronous Binary Counter	7.5	7.2	10.0	5.0	Q4 '86	5-105
IDT54/74FCT182A	Carry Lookahead Generator	—	—	10.0	5.0	Q4 '86	5-109
IDT54/74FCT191A	Up/Down Binary Counter	10.5	7.8	10.0	5.0	Q4 '86	5-113
IDT54/74FCT193A	Up/Down Binary Counter	6.9	6.5	10.0	5.0	Q4 '86	5-117
IDT54/74FCT240A	Octal Buffer	5.1	4.8	10.0	5.0	NOW	5-121
IDT54/74FCT244A	Octal Buffer	4.6	4.3	10.0	5.0	NOW	5-125
IDT54/74FCT245A	Octal Bidirectional Transceiver	4.9	4.6	10.0	5.0	NOW	5-129
IDT54/74FCT273A	Octal D Flip-Flop	8.3	7.2	10.0	5.0	NOW	5-133
IDT54/74FCT299A	Octal Universal Shift Register	9.5	7.2	10.0	5.0	NOW	5-137
IDT54/74FCT373A	Octal Transparent Latch	5.6	5.2	10.0	5.0	NOW	5-141
IDT54/74FCT374A	Octal D Flip-Flop	7.2	6.5	10.0	5.0	NOW	5-145
IDT54/74FCT377A	Octal D Flip-Flop	8.3	7.2	10.0	5.0	NOW	5-149
IDT54/74FCT521A	8-Bit Comparator	9.5	7.2	10.0	5.0	NOW	5-153
IDT54/74FCT533A	Octal Transparent Latch	5.6	5.2	10.0	5.0	NOW	5-156
IDT54/74FCT534A	Octal D Flip-Flop	7.2	6.5	10.0	5.0	NOW	5-160
IDT54/74FCT573A	Octal Transparent Latch	5.6	5.2	10.0	5.0	NOW	5-164
IDT54/74FCT574A	Octal D Register	7.2	6.5	10.0	5.0	NOW	5-168
IDT54/74FCT640A	Octal Bidirectional Transceiver	5.3	5.0	10.0	5.0	NOW	5-172
IDT54/74FCT645A	Octal Bidirectional Transceiver	4.9	4.6	10.0	5.0	NOW	5-176
IDT54/74FCT138	1-of-8 Decoder	12.0	9.0	10.0	5.0	NOW	5-98
IDT54/74FCT139	Dual 1-of-4 Decoder	12.0	9.0	10.0	5.0	NOW	5-102
IDT54/74FCT161	Synchronous Binary Counter	11.5	11.0	10.0	5.0	Q4 '86	5-105
IDT54/74FCT163	Synchronous Binary Counter	11.5	11.0	10.0	5.0	Q4 '86	5-105
IDT54/74FCT182	Carry Lookahead Generator	11.5	9.0	10.0	5.0	NOW	5-109
IDT54/74FCT191	Up/Down Binary Counter	16.0	12.0	10.0	5.0	Q4 '86	5-113
IDT54/74FCT193	Up/Down Binary Counter	10.5	10.0	10.0	5.0	Q4 '86	5-117
IDT54/74FCT240	Octal Buffer	9.0	8.0	10.0	5.0	NOW	5-121
IDT54/74FCT244	Octal Buffer	7.0	6.5	10.0	5.0	NOW	5-125
IDT54/74FCT245	Octal Bidirectional Transceiver	7.5	7.0	10.0	5.0	NOW	5-129
IDT54/74FCT273	Octal D Flip-Flop	15.0	13.0	10.0	5.0	NOW	5-133
IDT54/74FCT299	Octal Universal Shift Register	16.0	10.0	10.0	5.0	NOW	5-137

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High-Speed CMOS Logic Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)	Availability	Page No.
IDT54/74FCT373	Octal Transparent Latch	8.5	8.0	10.0	5.0	NOW	5-141
IDT54/74FCT374	Octal D Flip-Flop	11.0	10.0	10.0	5.0	NOW	5-145
IDT54/74FCT377	Octal D Flip-Flop	15.0	13.0	10.0	5.0	NOW	5-149
IDT54/74FCT521	8-Bit Comparator	15.0	11.0	10.0	5.0	NOW	5-153
IDT54/74FCT533	Octal Transparent Latch	12.0	10.0	10.0	5.0	NOW	5-156
IDT54/74FCT534	Octal D Flip-Flop	11.0	10.0	10.0	5.0	NOW	5-160
IDT54/74FCT573	Octal Transparent Latch	8.5	8.0	10.0	5.0	NOW	5-164
IDT54/74FCT574	Octal D Register	11.0	10.0	10.0	5.0	NOW	5-168
IDT54/74FCT640	Octal Bidirectional Transceiver	8.0	7.0	10.0	5.0	NOW	5-172
IDT54/74FCT645	Octal Bidirectional Transceiver	11.0	9.5	10.0	5.0	NOW	5-176
IDT54/74AHCT138	1-of-8 Decoder	27.0	22.0	3.5	5.0	NOW	5-20
IDT54/74AHCT139	Dual 1-of-4 Decoder	25.0	20.0	3.5	5.0	NOW	5-24
IDT54/74AHCT161	Synchronous Binary Counter	20.0	17.0	3.5	5.0	Q4 '86	5-27
IDT54/74AHCT163	Synchronous Binary Counter	20.0	17.0	3.5	5.0	Q4 '86	5-27
IDT54/74AHCT182	Carry Lookahead Generator	15.0	12.0	3.5	5.0	NOW	5-31
IDT54/74AHCT191	Up/Down Binary Counter	22.0	18.0	3.5	5.0	Q4 '86	5-35
IDT54/74AHCT193	Up/Down Binary Counter	19.0	16.0	3.5	5.0	Q4 '86	5-39
IDT54/74AHCT240	Octal Buffer	12.0	9.0	3.5	5.0	NOW	5-43
IDT54/74AHCT244	Octal Buffer	13.0	10.0	3.5	5.0	NOW	5-47
IDT54/74AHCT245	Octal Bidirectional Transceiver	15.0	10.0	3.5	5.0	NOW	5-50
IDT54/74AHCT273	Octal D Flip-Flop	17.0	15.0	3.5	5.0	NOW	5-53
IDT54/74AHCT299	Universal Shift Register	20.0	14.0	3.5	5.0	NOW	5-57
IDT54/74AHCT373	Octal Transparent Latch	19.0	16.0	3.5	5.0	NOW	5-61
IDT54/74AHCT374	Octal D Flip-Flop	18.0	16.0	3.5	5.0	NOW	5-65
IDT54/74AHCT377	Octal D Flip-Flop	18.0	16.0	3.5	5.0	NOW	5-69
IDT54/74AHCT521	8-Bit Comparator	18.0	14.0	3.5	5.0	NOW	5-73
IDT54/74AHCT533	Octal Transparent Latch	24.0	19.0	3.5	5.0	NOW	5-76
IDT54/74AHCT534	Octal D Flip-Flop	18.0	16.0	3.5	5.0	NOW	5-80
IDT54/74AHCT573	Octal Transparent Latch	15.0	14.0	3.5	5.0	NOW	5-84
IDT54/74AHCT574	Octal D Register	15.0	14.0	3.5	5.0	NOW	5-88
IDT54/74AHCT640	Octal Bidirectional Transceiver	14.0	11.0	3.5	5.0	NOW	5-92
IDT54/74AHCT645	Octal Bidirectional Transceiver	15.0	10.0	3.5	5.0	NOW	5-95
IDT39C821	10-Bit Non-inverting Register	12.0	12.0	10.0	5.0	NOW	5-1
IDT39C822	10-Bit Inverting Register	12.0	12.0	10.0	5.0	Q4 '86	5-1
IDT39C823	9-Bit Non-inverting Register	12.0	12.0	10.0	5.0	NOW	5-1
IDT39C824	9-Bit Inverting Register	12.0	12.0	10.0	5.0	NOW	5-1
IDT39C825	8-Bit Non-inverting Register	12.0	12.0	10.0	5.0	NOW	5-1
IDT39C826	8-Bit Inverting Register	12.0	12.0	10.0	5.0	Q4 '86	5-1
IDT39C827	10-Bit Non-inverting Buffer	10.0	8.0	10.0	5.0	NOW	*
IDT39C828	10-Bit Inverting Buffer	10.0	8.0	10.0	5.0	NOW	*
IDT39C841	10-Bit Non-inverting Latch	11.0	9.5	10.0	5.0	NOW	5-7
IDT39C842	10-Bit Inverting Latch	11.0	9.5	10.0	5.0	Q4 '86	5-7
IDT39C843	9-Bit Non-inverting Latch	11.0	9.5	10.0	5.0	NOW	5-7
IDT39C844	9-Bit Inverting Latch	11.0	9.5	10.0	5.0	NOW	5-7

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CONTINUED

High-Speed CMOS Logic Products (continued)

Part Number	Description	Max. Speed (ns) Mil.	Max. Speed (ns) Com'l.	Power (typical) Oper. (mW)	Power (typical) Standby (μW)	Availability	Page No.
IDT39C845	8-Bit Non-inverting Latch	11.0	9.5	10.0	5.0	NOW	5-7
IDT39C846	8-Bit Inverting Latch	11.0	9.5	10.0	5.0	Q4 '86	5-7
IDT39C861	10-Bit Non-inverting Transceiver	10.0	8.0	10.0	5.0	NOW	5-13
IDT39C862	10-Bit Inverting Transceiver	10.0	8.0	10.0	5.0	Q4 '86	5-13
IDT39C863	9-Bit Non-inverting Transceiver	10.0	8.0	10.0	5.0	NOW	5-13
IDT39C864	9-Bit Inverting Transceiver	10.0	8.0	10.0	5.0	NOW	5-13
IDT54/74FCT821B	10-Bit Non-inverting Register	8.5	7.5	10.0	5.0	NOW	5-180
IDT54/74FCT822B	10-Bit Inverting Register	8.5	7.5	10.0	5.0	Q4 '86	5-180
IDT54/74FCT823B	9-Bit Non-inverting Register	8.5	7.5	10.0	5.0	NOW	5-180
IDT54/74FCT824B	9-Bit Inverting Register	8.5	7.5	10.0	5.0	NOW	5-180
IDT54/74FCT825B	8-Bit Non-inverting Register	8.5	7.5	10.0	5.0	NOW	5-180
IDT54/74FCT826B	8-Bit Inverting Register	8.5	7.5	10.0	5.0	Q4 '86	5-180
IDT54/74FCT827B	10-Bit Non-inverting Buffer	6.5	5.0	10.0	5.0	NOW	*
IDT54/74FCT828B	10-Bit Inverting Buffer	6.5	5.0	10.0	5.0	NOW	*
IDT54/74FCT841B	10-Bit Non-inverting Latch	7.5	6.5	10.0	5.0	NOW	5-186
IDT54/74FCT842B	10-Bit Inverting Latch	7.5	6.5	10.0	5.0	Q4 '86	5-186
IDT54/74FCT843B	9-Bit Non-inverting Latch	7.5	6.5	10.0	5.0	NOW	5-186
IDT54/74FCT844B	9-Bit Inverting Latch	7.5	6.5	10.0	5.0	NOW	5-186
IDT54/74FCT845B	8-Bit Non-inverting Latch	7.5	6.5	10.0	5.0	NOW	5-186
IDT54/74FCT846B	8-Bit Inverting Latch	7.5	6.5	10.0	5.0	Q4 '86	5-186
IDT54/74FCT861B	10-Bit Non-inverting Transceiver	6.5	5.0	10.0	5.0	NOW	5-192
IDT54/74FCT862B	10-Bit Inverting Transceiver	6.5	5.0	10.0	5.0	Q4 '86	5-192
IDT54/74FCT863B	9-Bit Non-inverting Transceiver	6.5	5.0	10.0	5.0	NOW	5-192
IDT54/74FCT864B	9-Bit Inverting Transceiver	6.5	5.0	10.0	5.0	NOW	5-192

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Integrated Device Technology, Inc

STATIC RAM CROSS REFERENCE

AMD	IDT
Am2167-35C	IDT6167-35
Am2167-45C	IDT6167-45
Am2167-55C	IDT6167-55
Am2167-55BRA	IDT6167-S55B
Am2167-70C	IDT6167-70
Am2167-70BRA	IDT6167-S70B
Am2168-35C	IDT6168-35
Am2168-45C	IDT6168-45
Am2168-55C	IDT6168-55
Am2168-55M	IDT6168-55B
Am2168-70C	IDT6168-70
Am2168-90M	IDT6168-70B
Am9128-70C	IDT6116-70
Am9128-70M	IDT6116-70B
Am9128-90M	IDT6116-90B
Am9128-100C	IDT6116-90
Am9128-100M	IDT6116-90B
Am9128-120M	IDT6116-120B
Am99C68-45C	IDT6168S-45
Am99C68-55C	IDT6168S-55
Am99C68-55M	IDT6168S-55B
Am99C68-70C	IDT6168S-70
Am99C68-70M	IDT6168S-70B
Am99C68L-45C	IDT6168L-45
Am99C68L-55C	IDT6168L-55
Am99C68L-55M	IDT6168L-55B
Am99C68L-70C	IDT6168L-70
Am99C68L-70M	IDT6168L-70B
Am99C88-70C	IDT7164S-70
Am99C88-100C	IDT7164S-70
Am99C88-100M	IDT7164S-85B
Am99C88-120C	IDT7164S-70
Am99C88-120M	IDT7164S-85B
Am99C88-150C	IDT7164S-70
Am99C88-150M	IDT7164S-85B
Am99C88L-70C	IDT7164L-70
Am99C88L-100C	IDT7164L-70
Am2130-70C	IDT7130-70
Am2130-90C	IDT7130-90
Am2130-90M	IDT7130-90B
Am2130-100C	IDT7130-100
Am2130-100M	IDT7130-100B

CYPRESS	IDT
CY7C128-35C	IDT6116-35
CY7C128-45C	IDT6116-45
CY7C128-45M	IDT6116-45B
CY7C128-55C	IDT6116-55
CY7C128-55M	IDT6116-55B
CY7C130-55C	IDT7130-55
CY7C130-70C	IDT7130-70
CY7C130-70M	IDT7130-70B
CY7C130-90C	IDT7130-90
CY7C130-90M	IDT7130-90B
CY7C161-25C	IDT71981-25
CY7C161-35C	IDT71981-35
CY7C161-35M	IDT71981-35B
CY7C161-45C	IDT71981-45
CY7C161-45M	IDT71981-45B
CY7C162-25C	IDT71982-25
CY7C162-35C	IDT71982-35
CY7C162-35M	IDT71982-35B
CY7C162-45C	IDT71982-45
CY7C162-45M	IDT71982-45B
CY7C164-25C	IDT7188-25
CY7C164-35C	IDT7188-35
CY7C164-35M	IDT7188-35B
CY7C164-45C	IDT7188-45
CY7C164-45M	IDT7188-45B
CY7C164-55C	IDT7188-55
CY7C164-55M	IDT7188-55B
CY7C166-25C	IDT7198-25
CY7C166-35C	IDT7198-35
CY7C166-35M	IDT7198-35B
CY7C166-45C	IDT7198-45
CY7C166-45M	IDT7198-45B
CY7C166-55C	IDT7198-55
CY7C166-55M	IDT7198-55B
CY7C167-25C	IDT6167-25
CY7C167-35C	IDT6167-35
CY7C167-35M	IDT6167-35B
CY7C167-45C	IDT6167-45
CY7C167-45M	IDT6167-45B
CY7C168-25C	IDT6168-25
CY7C168-35C	IDT6168-35
CY7C168-35M	IDT6168-35B
CY7C171-25C	IDT71681-25
CY7C171-35C	IDT71681-35
CY7C171-35M	IDT71681-35D
CY7C171-45C	IDT71681-45
CY7C171-45M	IDT71681-45D

CYPRESS	IDT
CY7C172-25C	IDT71682-25
CY7C172-35C	IDT71682-35
CY7C172-35M	IDT71682-35B
CY7C172-45C	IDT71682-45
CY7C172-45M	IDT71682-45B
CY7C185-35C	IDT7164-35
CY7C185-45C	IDT7164-45C
CY7C185-45M	IDT7164-45B
CY7C185-55C	IDT7164-55C
CY7C185-55M	IDT7164-55B
CY7C186-35C	IDT7164-35
CY7C186-45C	IDT7164-45
CY7C186-45M	IDT7164-45B
CY7C186-55C	IDT7164-55
CY7C186-55M	IDT7164-55B
CY7C187-25C	IDT7187-25
CY7C187-35C	IDT7187-35
CY7C187-35M	IDT7187-35B
CY7C187-45C	IDT7187-45
CY7C187-45M	IDT7187-45B
CY7C187-55C	IDT7187-55
CY7C187-55M	IDT7187-55B

FUJITSU	IDT
MB81C67-35	IDT6167-35
MB81C67-45	IDT6167-45
MB81C67-55	IDT6167-55
MB8416-120	IDT6116-120
MB8416-150	IDT6116-120
MB8416-200	IDT6116-120
MB81C68-35	IDT6168-35
MB81C68-45	IDT6168-45
MB81C68-55	IDT6168-55
MB81C75-35	IDT7198-35
MB81C75-45	IDT7198-45
MB81C75-55	IDT7198-55
MB81C71-35	IDT7187-35
MB81C71-45	IDT7187-45
MB81C71-55	IDT7187-55
MB81C78-45	IDT7164-45
MB81C78-55	IDT7164-55
MB81C78-70	IDT7164-70

FAIRCHILD	IDT
F1600-C45	IDT7187-45
F1600-C55	IDT7187-55
F1600-M55	IDT7187-55B
F1600-C70	IDT7187-70
F1600-M70	IDT7187-70B
F1601-C45	IDT7187-45
F1601-C55	IDT7187-55
F1601-M55	IDT7187-55B
F1601-C70	IDT7187-70
F1601-M70	IDT7187-70B

HARRIS	IDT
HM65262B-8	IDT6167-70B
HM65262S-9	IDT6167-55B
HM65262B-9	IDT6167-70B
HM65262-9	IDT6167-70B
HM65262-8	IDT6167-70B
HM65262C-9	IDT6167-70B
HM65162B-2	IDT6116-70B
HM65162-2	IDT6116-70B
HM65162C-2	IDT6116-70B
HM65162S-9	IDT6116-55B
HM65162B-9	IDT6116-70B
HM65162-9	IDT6116-70B
HM65162C-9	IDT6116-70B
HM65162S-5	IDT6116-55
HM65162B-5	IDT6116-70
HM65162-5	IDT6116-90

HITACHI	IDT
HM6267-35	IDT6167-35
HM6267-45	IDT6167-45
HM6116-120	IDT6116-55
HM6116-150	IDT6116-55
HM6116-200	IDT6116-55
HM6168-45	IDT6168-45
HM6168-55	IDT6168-55
HM6168-70	IDT6168-55
HM6287-45	IDT7187-45
HM6287-55	IDT7187-55
HM6287-70	IDT7187-55

HITACHI	IDT
HM6787-25	IDT7187-25
HM6264-100	IDT7164-70
HM6264-120	IDT7164-70
HM6264-150	IDT7164-70

INMOS	IDT
IMS1400-35	IDT6167-35
IMS1400-45	IDT6167-45
IMS1400-45M	IDT6167-45B
IMS1400-55	IDT6167-55
IMS1400-55M	IDT6167-55B
IMS1400L-70	IDT6167L-55
IMS1400L-100	IDT6167L-55
IMS1403-35	IDT6167-35
IMS1403-45	IDT6167-45
IMS1403-45M	IDT6167-45B
IMS1403-55	IDT6167-55
IMS1403-55M	IDT6167-55B
IMS1420-45	IDT6168-45
IMS1420-55	IDT6168-55
IMS1420-55M	IDT6168-55B
IMS1420-70	IDT6168-70
IMS1420-70M	IDT6168-70B
IMS1420L-70	IDT6168L-55
IMS1420L-100	IDT6168L-55
IMS1423-25	IDT6168-25
IMS1423-35	IDT6168-35
IMS1423-35M	IDT6168-35B
IMS1423-45	IDT6168-45
IMS1423-45M	IDT6168-45B
IMS1600-45	IDT7187-45
IMS1600-55	IDT7187-55
IMS1600-55M	IDT7187-55B
IMS1600-70	IDT7187-70
IMS1600-70M	IDT7187-70B

INMOS	IDT
IMS1620-45	IDT7188-45
IMS1620-55	IDT7188-55
IMS1620-55M	IDT7188-55B
IMS1620-70	IDT7188-70
IMS1620-70M	IDT7188-70B
IMS1624-45	IDT7198-45
IMS1624-55	IDT7198-55
IMS1624-55M	IDT7198-55B
IMS1624-70	IDT7198-70
IMS1624-70M	IDT7198-70B

MATRA-HARRIS	IDT
HM65263-45	IDT6167-45
HM65263-55	IDT6167-55
HM65163-45	IDT6116-45
HM65163-55	IDT6116-55
HM65682-45	IDT6168-45
HM65682-55	IDT6168-55
HM65682-70	IDT6168-70
HM62641-70	IDT7164-70
HM62641-90	IDT7164-70

LATTICE	IDT
SR16K8-35	IDT6116-35
SR16K8-45	IDT6116-45
SR16K8-45M	IDT6116-45B
SR16K8-55	IDT6116-55
SR16K8-55M	IDT6116-55B
SR16K4-35	IDT6168-35
SR16K4-45	IDT6168-45
SR16K4-45M	IDT6168-45B
SR16K4-55	IDT6168-55
SR16K4-55M	IDT6168-55B
SR64K4-35	IDT7188-35
SR64K4-45	IDT7188-45
SR64K4-45M	IDT7188-45B
SR64K4-55	IDT7188-55
SR64K4-55M	IDT7188-55B
SR64E4-35	IDT7198-35
SR64E4-45	IDT7198-45
SR64E4-45M	IDT7198-45B
SR64E4-55	IDT7198-55
SR64E4-55M	IDT7198-55B

LATTICE	IDT
SR64K1-35	IDT7187-35
SR64K1-45	IDT7187-45
SR64K1-45M	IDT7187-45B
SR64K1-55	IDT7187-55
SR64K1-55M	IDT7187-55B
SR64K8-35	IDT7164-35
SR64K8-45	IDT7164-45
SR64K8-45M	IDT7164-45B
SR64K8-55	IDT7164-55
SR64K8-55M	IDT7164-55B

MOTOROLA	IDT
MCM2167-45	IDT6167-45
MCM2167-55	IDT6167-55
MCM2167-70	IDT6167-70
MCM2016-45	IDT6116-45
MCM2016-55	IDT6116-55
MCM2016-70	IDT6116-70
MCM6168-35	IDT6168-35
MCM6168-45	IDT6168-45
MCM6168-55	IDT6168-55
MCM6168-70	IDT6168-70
MCM6268-35	IDT7188-35
MCM6268-45	IDT7188-45
MCM6268-55	IDT7188-55
MCM6287-35	IDT7187-35
MCM6287-45	IDT7187-45
MCM6287-55	IDT7187-55
MCM6164-45	IDT7164-45
MCM6164-55	IDT7164-55
MCM6164-70	IDT7164-70

NEC	IDT
μPD4311-35	IDT6167-35
μPD4311-45	IDT6167-45
μPD4311-55	IDT6167-55
μPD446	IDT6116-70
μPD4314-35	IDT6168-35
μPD4314-45	IDT6168-45
μPD4314-55	IDT6168-55

NEC	IDT
μPD4362-45	IDT7188-45
μPD4362-55	IDT7188-55
μPD4362-70	IDT7188-70
μPD4361-40	IDT7187-35
μPD4361-45	IDT7187-45
μPD4361-55	IDT7187-55
μPD4361-70	IDT7187-70
μPD4464-XXX	IDT7164-70

TOSHIBA	IDT
TC2018-35	IDT6116-35
TC2018-45	IDT6116-45
TC2018-55	IDT6116-55
TC2068-35	IDT6168-35
TC2068-45	IDT6168-45
TC2068-55	IDT6168-55
TC5562-35	IDT7187-35
TC5562-45	IDT7187-45
TC5562-55	IDT7187-55
TC2064-XXX	IDT7164-70

VITELIC	IDT
V61C67-35	IDT6167-35
V61C67-45	IDT6167-45
V61C67-55	IDT6167-55
V61C16-35	IDT6116-35
V61C16-45	IDT6116-45
V61C16-55	IDT6116-55
V61C68-35	IDT6168-35
V61C68-45	IDT6168-45
V61C68-55	IDT6168-55
V61C62-45	IDT6188-45
V61C62-55	IDT6188-55
V61C62-70	IDT6188-70
V61C64-45	IDT7165-45
VC1C64-55	IDT7165-55
VC1C64-70	IDT7165-70

VITELIC	IDT
V61C32-70	IDT7132-70
V61C32-90	IDT7132-90

VTI	IDT
VT64KS4-35	IDT7188-35
VT64KS4-45	IDT7188-45
VT64KS4-55	IDT7188-55
VT16H4-35	IDT71981-35
VT16H4-45	IDT71981-45
VT16H4-55	IDT71981-55

IDT39C000 SERIES

P/N	DESCRIPTION	COMPETITORS				IDT SPECIAL FEATURES
		AMD	NSC	THOMPSON CSF	CYPRESS	
IDT39C01C IDT39C01D IDT39C01E	4-Bit Slice	Am2901B Am2901C	IDM2901A IDM2901A-2	SFC2901B SFC2901C	CY7C901	• 1/5 The Bipolar Power • "D" Version 25% Faster Than "C" • "E" Version 25% Faster Than "D"
IDT39C02A	Carry Lookahead Generator	Am2902 Am2902A	IDM2902	SFC2902 SFC2902A		• High-Speed CMOS
IDT39C03A IDT39C03B	4-Bit Slice	Am2903 Am2903A	LM2903	SFC2903		• 1/4 The Bipolar Power • "B" Version 20% Faster Than "A"
IDT39C09A IDT39C09B	4-Bit Sequencer	Am2909 Am2909A	LM2909A	SFC2909 SFC2909A	CY7C909	• High-Speed CMOS • "B" Version 20% Faster than "A" • 1/3 The Bipolar Power
IDT39C10B IDT39C10C	12-Bit Sequencer	Am2910 Am2910A	IDM2910A	SFC2910	CY7C910	• 33-Deep Stack • "C" Version 20% Faster Than "B"
IDT39C11A IDT39C11B	4-Bit Sequencer	Am2911 Am2911A	IDM2911A	SFC2911A	CY7C911	• High-Speed CMOS • "B" Version 20% Faster Than "A"
IDT39C203 IDT39C203A	4-Bit Slice	Am29203				• 1/4 The Bipolar Power • "A" Version 20% Faster
IDT39C60 IDT39C60-1 IDT39C60A	16-Bit E.D.C.	Am2960 Am2960-1 Am2960A				• "A" Version World's Fastest 16-Bit E.D.C. • 1/4 The Bipolar Power
IDT39C705A IDT39C705B	16 X 4 Register File	Am29705 Am29705A	IDM29705 IDM29705A			• High-Speed CMOS • "B" Version 20% Faster than "A"
IDT39C707 IDT39C707A	16 X 4 Register File	Am29707				• High-Speed CMOS • "A" Version 20% Faster
IDT49C25	Clock Generator	Am2925				• 1/4 The Bipolar Power

IDT49C000 SERIES

P/N	DESCRIPTION	PACKAGE	IDT SPECIAL FEATURES
IDT49C401 IDT49C401A	16-Bit Slice	64-Pin Dip	• Speed Enhanced, Pin Compatible to IMI4X2901 • High-Speed CMOS • 2901 Instruction Set Compatible
IDT49C402 IDT49C402A	16-Bit Slice	68-Pin Dip, PGA, LCC	• Quad 2901 With 2902 • High-Speed CMOS ("A" Version 40% Faster than four 2901CS and 2902A) • 64 Registers • 8 Additional Destination Functions • 2901 Instruction Set Compatible
IDT49C403	16-Bit Slice	108-Pin PGA	• High-Speed CMOS • Quad 2903A/29203 With 2902A • Binary/BCD Arithmetic • 64 Registers • Four Q-Registers • Additional ALU Functions • Byte/Word Capability • 2903A/29203 Instruction Set Compatible
IDT49C410 IDT49C410A	16-Bit Sequencer	48-Pin Dip, LCC 52-Pin PLCC	• High-Speed CMOS • 33-Deep Stack • 2910 Instruction Set Compatible
IDT49C460 IDT49C460A	32-Bit E.D.C.	68-Pin Dip, PGA, LCC, PLCC	• Replaces Two Cascaded 16-Bit E.D.C. Chips • "A" Version World's Fastest 32-Bit E.D.C. • Compatible To IDT39C60s

Integrated Device Technology, Inc.

DIGITAL SIGNAL PROCESSING DIVISION CROSS REFERENCE GUIDE

IDT MULTIPLIER AND MULTIPLIER/ACCUMULATOR PRODUCTS

All IDT Fixed Point Multiplier/MACs feature:

- Low-power dissipation—less than 500mW typical
- Competitively priced
- Full conformance to MIL-STD-883, Class B
- Highest CMOS speeds in the industry
- Full complement of packages:
  - —Ceramic DIP
  - —SHRINKDIP
  - —Flatpack (Contact Factory)
  - —PLCC
  - —Pin Grid Array
  - —LCC

PART NUMBER	DESCRIPTION	CROSS REFERENCE				IDT SPECIAL FEATURES
		AMD	WEITEK	ANALOG DEVICES	TRW	
IDT7216	16 x 16 Multiplier	Am29516A	WTL1516	ADSP1016	MPY016	Speed to 35ns One-sixth bipolar power.
IDT7217	16x 16 Multiplier with Single Clock	Am29517A	WTL1517	—	—	Single clock option. Speed to 35ns.
IDT7212	12 x 12 Multiplier	—	—	ADSP1012	MPY012	Speeds to 30ns.
IDT7213	12 x 12 Multiplier with Single Clock	—	—	—	—	Single clock microprogrammed version.
IDT7210	16 x 16 Multiplier/Accumulator	Am29510	WTL1010	ADSP1010	TDC2010	One-sixth bipolar power. Speeds to 35ns.
IDT7243	16 x 16 Multiplier/Accumulator	—	WTL2044	—	TDC1043	One-sixth bipolar power. Speeds to 35ns.
IDT7209	12 x 12 Multiplier/Accumulator	Am29509	—	ADSP1009	TDC1009	Speeds to 30ns.

IDT FIFO PRODUCTS:

All IDT FIFOs feature:

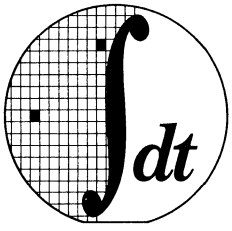
- Dual-ported RAM pointer architecture
- Advanced 1.2 micron CEMOS™ II technology
- Fully asynchronous and simultaneous read/write
- Fully expandable in word depth and/or width
- Auto retransmit capability zeros read pointer
- Zero fall-through time
- Full military temperature range operation
- Three-state buffered output
- Processed to MIL-STD-883, Class B

PART NUMBER	SPEED (ACCESS TIME) (ns)	SIZE DEPTH X WIDTH	PACKAGE	SPECIAL IDT FEATURES
IDT7201	35	512 x 9-Bit	• 28-Pin DIP • 32-Pin Ceramic Leaded Chip Carrier (LCC) • 28-Pin Plastic J-Bend Leaded Chip Carrier • 28-Pin Flatpack	Speeds to 35ns access time. Mostek MK4501 compatible
IDT7202	35	1024 x 9-Bit		
IDT7201A	35	512 x 9-Bit		Half-Full flag. Flow-through mode for first data byte.
IDT7202A	35	1024 x 9-Bit		
IDT7203	50	2048 x 9-Bit		Half-Full flag. Flow-through mode for first data byte.
IDT7204	50	4096 x 9-Bit		
IDT72103	50	2048 x 9-Bit	• 40-Pin DIP • 44-Pin Ceramic LCC • 44-Pin Plastic J-Bend Leaded Chip Carrier	Half-Full, Almost-Full and Almost-Empty flags. Serial input and output. Fully cascadable in word width and depth.
IDT72104	50	4096 x 9-Bit		

IDT FLOATING POINT PRODUCTS:

- Advanced CEMOS II 1.2 micron technology
- Full IEEE Standard 754 conformance
- Single 5 Volt supply operation
- Full 32-bit and 64-bit multiply and arithmetic operations
- 144-pin grid array
- Low-power (less than 750mW typical) per device

PART TYPE	SINGLE PRECISION OPERATIONS (32-BIT)	DOUBLE PRECISION OPERATIONS (64-BIT)	FEATURES
IDT72064 64-Bit Multiplier	5 megaflops (200ns pipelined)	2.5 megaflops (400ns pipelined)	• Weitek WTL1064 equivalent
IDT72065 64-Bit ALU	10 megaflops (100ns pipelined)	10 megaflops (100ns pipelined)	• Weitek WTL1065 equivalent
IDT72264 64-Bit Multiplier	10 megaflops (100ns pipelined)	5 megaflops (200ns pipelined)	• Weitek WTL1264 equivalent
IDT72265 64-Bit ALU	10 megaflops (100ns pipelined)	10 megaflops (100ns pipelined)	• Weitek WTL1265 equivalent



Integrated
Device
Technology

Technology/Capabilities

1

TECHNOLOGY/CAPABILITIES
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IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the 80's and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, our product strategy has been to apply the advantages of our extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight and size. Many of our innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, low-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance static RAMs, logic, DSP, MICROSLICE™ bit-slice microprocessor products, data conversion devices, and modular subsystem assemblies complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families and additional product lines will be introduced. Contact your IDT field representative or factory marketing at 1-800-IDT-CMOS to determine the latest product offerings. If you're building state-of-the-art equipment, IDT may be able to solve some of your design problems.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

CEMOS (the "E" stands for enhanced) is a state-of-the-art proprietary CMOS technology initially developed and continually refined by IDT to be at the leading-edge of new high-speed CMOS processes. It incorporates the best characteristics of traditional CMOS, including low-power, high-noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL.

The company has been producing CEMOS products in large volume for over five years. During this time, CEMOS technology has been re-engineered and refined from the original 2.5 micron CEMOS I to the present CEMOS III direct step-on-wafer, dry-etch process providing gate lengths as small as sub-micron. Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits.

CEMOS is a technology designed to optimize both speed and power capabilities of advanced architecture VLSI products. It achieves industry-leading speeds yet consumes very low operating power. Unlike many other competitive "CMOS" circuits, IDT products can power down to a full CMOS standby mode with extremely low micro-watt power levels or, in the case of memories, maintain memory contents in a battery backup data retention mode. Many competing "CMOS" technologies employ techniques aimed at obtaining fast performance, such as substrate bias generators or charge pumps, that consume higher levels of operating and standby power and preclude full CMOS level standby or battery backup operation.

DUAL-WELL STRUCTURES

CEMOS is constructed using an advanced dual-well, or twin-well process architecture to optimize the overall characteristics of a high-performance CMOS process. CMOS processes, using only "P-wells", resulted in inferior P (or N) channel transistors or compromised P/N channels. This compromise is largely eliminated by utilizing both a deep underlying main "well" (in this case a "P-well") and by altering the doping profile nearer the surface of the P-channel transistor regions. The latter region becomes the "N-well" of the dual- or twin-well process. This technique allows the fabrication of high-performance transistors in both polarities.

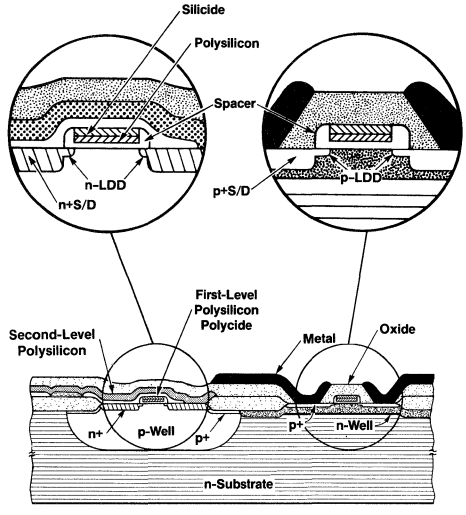
The industry now recognizes that the best combination of balanced capabilities is achieved using this "dual-well" approach. This construction technique suppresses punch-through, minimizes junction capacitance and transistor body effects, and allows extremely fast speeds. In addition, it virtually eliminates soft errors in fine line geometry memory products induced by high-energy alpha particles.

BUILT-IN ALPHA PARTICLE IMMUNITY

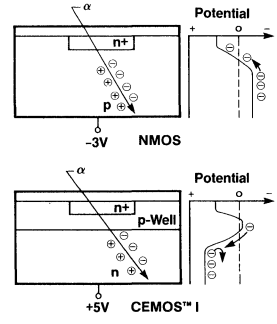
Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Travelling with high energy levels, alpha particles penetrate deep into an integrated circuit chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake. In typical NMOS or "N-well" CMOS processes, the free electrons are attracted by the N+ memory cells and cause soft errors by entering them.

To protect the cells from this hazardous occurrence, manufacturers using these technologies apply a liquid die coating of

IDT CEMOS
Device Cross Section



IDT CEMOS
Built-In High Alpha Particle Immunity



P-Well Barrier

- Deep burrowing alpha particles penetrate over 20μm beneath the surface
- Leaves trail of electron-hole pairs in its wake
- CEMOS™ I potential barrier repels electrons—then swept away to ground
- No need for protective surface coatings (i.e. organic polyimide)

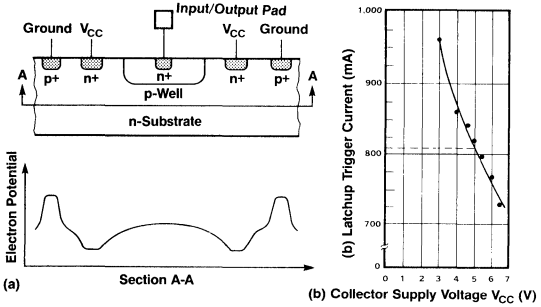
polyimide, an organic compound that becomes a jelly-like substance as a result of package sealing temperatures. These compounds may themselves have limitations. Often the sealing temperatures cause bubbles in the die coating which still allow alpha particles to reach the die. Also, the compounds are organic and may lead to future reliability problems (military standards preclude their use in package cavities unless a waiver is obtained).

In an IDT product, the P-well potential barrier of the dual-well structure repels the free electrons, preventing them from reaching the memory cells. Electrons then re-combine with the free holes or are swept away to the substrate contact. IDT dual-well memories are virtually immune to alpha particle soft errors and do not require organic die coatings with their related difficulties.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes. The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than 700mA.

IDT CEMOS
Latchup Suppression



- Double guard rings on I/O circuits
- npn and n-channel I/O devices eliminate hole injection latchup
- Latchup trigger current substantially greater than 500mA

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

Another traditional limitation associated with many MOS and bipolar products is electrostatic discharge induced failures. This problem has also been solved by a combination of IDT's CEMOS process and proper circuit design. All IDT products incorporate proprietary ESD protection circuitry on all inputs and outputs to ensure that they are insensitive to repeated applications of ESD stress and do not exhibit the degradation found in other other MOS or bipolar products which can eventually result in product failure.

CEMOS VARIATIONS

Variations of IDT CEMOS technology employ single- and dual-layer metalization as well as single and double poly layers to optimize memory or logic product performance. In addition, bipolar devices are utilized selectively, along with the N- and P-channel CMOS structures, to enhance performance and output drives.

MAINTAINING LEADING EDGE TECHNOLOGY

IDT maintains a constant research and development program to continue to enhance the capabilities of its CEMOS technology. CEMOS III, IDT's next generation process, is currently being refined to achieve aggressive submicron minimum feature size geometries to allow the implementation of significantly faster speeds as well as higher levels of integration.

These continued advancements in process development and manufacturing, coupled with customer-proven deliveries, quality and reliability, have established the company as a leader in high-speed CMOS integrated circuits. Committed to maintaining superior performance, IDT will continue to drive the technology to lead the CMOS future.

This chart — showing our evolution from the company's original CEMOS I technology to CEMOS II and CEMOS III — depicts the continuous research and development efforts that we expend to maintain our technological leadership in high-speed CMOS.

CEMOS TECHNOLOGY	MINIMUM[1] FEATURE SIZE (MICRONS)	FASTEST SPEED 16K x 1 RAM COM'L. ACCESS TIME (ns)	PRODUCT AVAILABILITY
I	2.5	45	Since 1982
IIA	2.0	35[2]	1983
IIB	1.5	30	1984
IIC	1.2	15	NOW
IIIA	1.0	SUB15	FUTURE
IIIB	SUBMICRON	T.B.D.	FUTURE

NOTES:

1. There are many claims and counter claims in this area of minimum feature size. We are using here a conservative approach, i.e. the gate length as physically measured on a scanning electron microscope.
2. Estimate — not manufactured in CEMOS IIA. Our 16K x 1 static RAM is used as a typical product to illustrate the figures of merit of this constant drive for ever higher performance standards.

RADIATION HARDENED TECHNOLOGY

IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built-in these to special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company concentrate on supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation handling capabilities (See "Improved Tolerance of Integrated Device Technology Products for High-Radiation Environments" in Section 8).

SURFACE MOUNT TECHNOLOGY

SUBSYSTEM MODULAR ASSEMBLIES

To take full advantage of the low-power aspect of CMOS, and obtain two to three times the space savings, CMOS products should be used as SMDs (surface mount devices). However, most integrated circuits sold today are still packaged in the traditional DIP (dual in-line package) configuration, and there is a tremendous support industry to handle thru-board assembly.

Determined to utilize CMOS advantages, IDT re-invented the DIP. This was accomplished by developing multilayered substrates (either co-fired ceramic or glass filled epoxy FR-4) with dual in-line (DIP) or single in-line (SIP) pins. An advanced vapor phase reflow surface mount technology was also developed after exhaustive evaluation proved vapor phase reflow to be the most efficient method of heat transfer and to produce the most reliable solder connections available.

Products that are to be interconnected to form larger electronic elements are electrically tested, environmentally screened, performance selected and then thermally matched to the appropriate ceramic or glass filled epoxy substrates. After modular assembly, the finished product is 100% re-tested to ensure that it completely performs to the specifications required.

As a result, IDT produces extraordinarily dense, high-speed combinations of monolithic ICs as complex subsystem modular assemblies. These modules convert SMDs to user-friendly DIPs/SIPs providing customers with the density advantages of surface mount in a format compatible with their extensive, thru-board, assembly expertise.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California — the heart of the "Silicon Valley." The company's operations are housed in five facilities totaling close to 300,000 square feet. These facilities incorporate all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test and administration. In-house capabilities incorporate scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), burn-in, life test and a full complement of environmental screening equipment.

IDT's 54,000 square foot Corporate Headquarters houses technology and product research and development. Teams equipped with state-of-the-art computerized design and analytical tools conduct the continuous R&D required to push CEMOS technology forward and to create future product lines. This facility contains a 10,000 square foot Class 10 (no more than 10 particles larger than 0.2 micron per cubic foot) wafer fabrication clean room used to produce the MICROSLICE, DSP and logic product families as well as support R&D.

Located adjacent to the headquarters facility, forming an IDT corporate campus, is a 100,000 square foot two-building complex that houses the DSP Division and MICROSLICE product line. Design and product teams, along with administrative functions, are situated in these buildings.

A second small wafer fabrication area, used for research and development, is also located at this site. This facility houses its own design tools, laboratories, test and burn-in facilities. Construction of an in-house plastic assembly area is also underway in this facility.

IDT's Subsystems Division is housed in a third Santa Clara location, only a few blocks away from the other sites. This 37,000 square foot facility contains the development and product teams that produce IDT's FCT, AHCT and IDT39C800 logic families and modular assemblies. Included at this facility are a quick turnaround hermetic package assembly line and an advanced vapor phase reflow surface mounting module assembly area.

IDT's largest facility is located in Salinas, California, about an hour away from Santa Clara. This is the Static RAM Division's headquarters, a 100,000 square foot facility located on a 14-acre site. Constructed in 1985, this facility houses an ultra-modern 25,000 square foot high-volume production wafer fabrication area measured at Class 2-to-Class 3 clean room conditions (a maximum of 2 to 3 particles per cubic foot of 0.2 micron or larger). Careful design and construction created a clean room environment far beyond the average of U.S. fab areas (Class 100), capable of producing large volumes of very high-density, submicron geometry, fast static RAMs. This facility also houses the product development areas, laboratories, test, burn-in and shipping areas for IDT's leadership family of CMOS static RAMs. This site has future expansion capabilities to accomodate a 250,000 square foot complex.

IDT's facilities now total nearly 300,000 square feet of floor space and house three wafer fabrication clean rooms, three domestic assembly lines, four test and three burn-in areas. All of these facilities are aimed at increasing our manufacturing productivity to supply ever larger volumes of high-performance, cost-effective leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing — as opposed to being "tested-in" later — in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials and chemicals are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT's commercial grade products are required to meet stringent criteria.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510. As per MIL-HDBK-217, products screened to Class B requirements result in failure rates thirty (30) times better than those not subjected to stress screening. Parts processed to these reliability levels are generally used in applications where product reliability is vital.

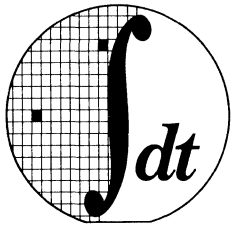
For module assemblies, additional screening of the fully assembled substrates is performed to assure package integrity and mechanical reliability. Finally, 100% electrical tests are performed on the finished module to ensure compliance with the defined "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial, and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.



Integrated
Device
Technology

Static RAM

2

STATIC RAM PRODUCTS
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Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (2K x 8-BIT)

IDT6116SA
IDT6116LA

FEATURES:

- High-speed
  - —Military — 35/45/55/70/90/120/150ns (max.)
  - —Commercial — 30/35/45/55/70/90ns (max.)
- Low-power operation
  - —IDT6116SA
    - Active: 180mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6116LA
    - Active: 160mW (typ.)
    - Standby: 20μW (typ.)
- Battery backup operation — 2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Standard 24-pin DIP, 24-pin THINDIP or plastic DIP, 28- and 32-pin LCC, or 24-Lead Flatpack
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Access times as fast as 30ns are available with maximum power consumption of only 495mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20μW typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW to 4μW operating off of a 2V battery.

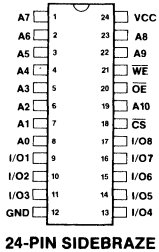
All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in either a 24-pin, 600 and 300 mil DIPs or 32- and 28-pin leadless chip carriers, providing high board-level packing densities.

The IDT6116SA/LA Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

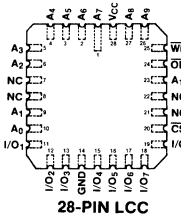
2

PIN CONFIGURATIONS



24-PIN SIDEBRAZE
TOP VIEW

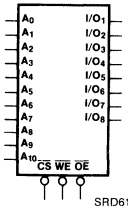
SRD6116SA/LA-001



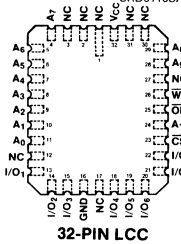
28-PIN LCC
TOP VIEW

SRD6116SA/LA-002

LOGIC SYMBOL



SRD6116SA/LA-003

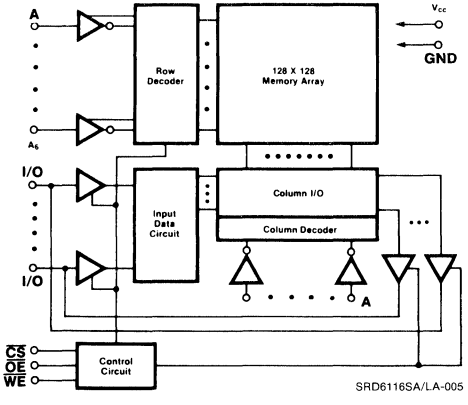


32-PIN LCC
TOP VIEW

SRD6116SA/LA-004

A_0-A_{10}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O1-I/O8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}$	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

FUNCTIONAL BLOCK DIAGRAM



SRD6116SA/LA-005

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING		VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND		-0.5 to +7.0	V
T_A	Operating Temperature	MIL. COM'L.	-55 to +125 0 to +70	°C
T_{BIAS}	Temperature Under Bias	MIL. COM'L.	-65 to +135 -10 to +85	°C
T_{STG}	Storage Temperature	MIL. COM'L.	-65 to +150 -55 to +125	°C
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-1.0(1)	—	0.8	V
C_L	Output Load	—	—	30	pF

NOTE:

1. V_{IL} = -3.0V for pulse widths less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116SA MIN.	IDT6116SA TYP.(1)	IDT6116SA MAX.	IDT6116LA MIN.	IDT6116LA TYP.(1)	IDT6116LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	30ns COM'L.	30ns MIL.	35ns(2) COM'L.	35ns(2) MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	70ns COM'L.	70ns MIL.	90ns COM'L.	90ns MIL.	120ns(3) COM'L.	120ns(3) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	SA	80	—	80	90	80	90	80	90	80	90	80	90	—	90	mA
		LA	75	—	75	85	75	85	75	85	75	85	75	85	—	85	
I_{CC2}	Dyn. Op. Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	SA	110	—	100	115	100	100	100	100	100	100	90	100	—	100	mA
		LA	105	—	95	105	90	95	80	90	80	90	75	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	SA	35	—	25	35	25	25	25	25	25	25	20	25	—	25	mA
		LA	30	—	25	30	20	20	20	20	15	20	15	15	—	15	
I_{SB1}	Full Stdby. Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	SA	2	—	2	10	2	10	2	10	2	10	2	10	—	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	0.1	0.9	0.1	0.9	—	0.9	

NOTE:

1. All values are maximum guaranteed values.
2. Data is preliminary for Military devices.
3. Also available: 150ns Military device.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

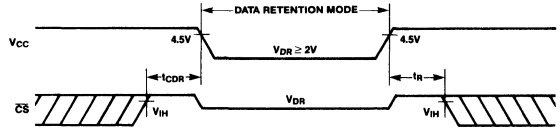
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

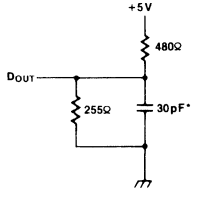
LOW V_{CC} DATA RETENTION WAVEFORM



SRD6116SA/LA-006

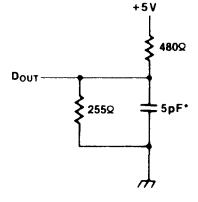
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2



SRD6167-006

Figure 1. Output Load



SRD6167-007

Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, and t_{OW})

***Including scope and jig.**

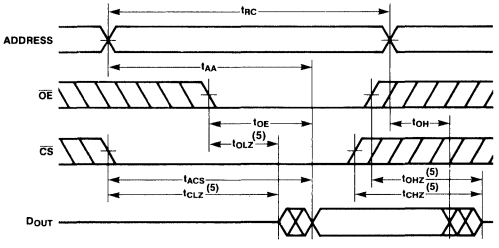
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	6116SA30[1] 6116LA30[1] MIN.	MAX.	6116SA35/45[4] 6116LA35/45[4] MIN.	MAX.	6116SA55 6116LA55 MIN.	MAX.	6116SA70 6116LA70 MIN.	MAX.	6116SA90 6116LA90 MIN.	MAX.	6116SA120[2] 6116LA120[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	30	—	35/45	—	55	—	70	—	90	—	120	—	ns
t_{AA}	Address Access Time	—	30	—	35/45	—	55	—	70	—	90	—	120	ns
t_{ACS}	Chip Select Access Time	—	30	—	35/45	—	50	—	65	—	90	—	120	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	20/25	—	40	—	50	—	65	—	80	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselect to Output in High Z[3]	—	18	—	20/25	—	30	—	35	—	40	—	40	ns
t_{OHZ}	Output Disable to Output in High Z[3]	—	18	—	20/25	—	30	—	35	—	40	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	30	—	35/45	—	55	—	70	—	90	—	120	—	ns
t_{CW}	Chip Select to End of Write	20	—	25/30	—	40	—	40	—	55	—	70	—	ns
t_{AW}	Address Valid to End of Write	20	—	25/30	—	45	—	65	—	80	—	105	—	ns
t_{AS}	Address Setup Time	0	—	0	—	5	—	15	—	15	—	20	—	ns
t_{WP}	Write Pulse Width	15	—	20/25	—	40	—	40	—	55	—	70	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	5	—	5	—	5	—	5	—	ns
t_{OHZ}	Output Disable to Output in High Z[3]	—	18	—	20/25	—	30	—	35	—	40	—	40	ns
t_{WHZ}	Write to Output in High Z[3]	—	18	—	20/25	—	30	—	35	—	40	—	40	ns
t_{DW}	Data to Write Time Overlap	15	—	15/20	—	25	—	30	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

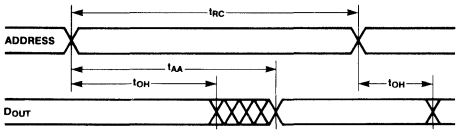
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Data is preliminary for military devices only.

TIMING WAVEFORMS OF READ CYCLE NO. 1(1)



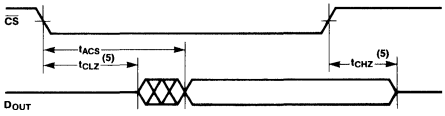
SRD6116SA/LA-007

READ CYCLE 2(1,2,4)



SRD6116SA/LA-008

READ CYCLE 3(1,3,4)

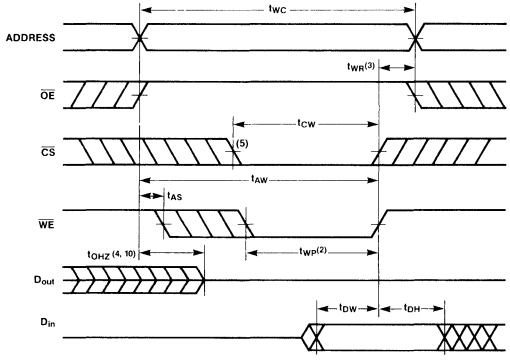


SRD6116SA/LA-009

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

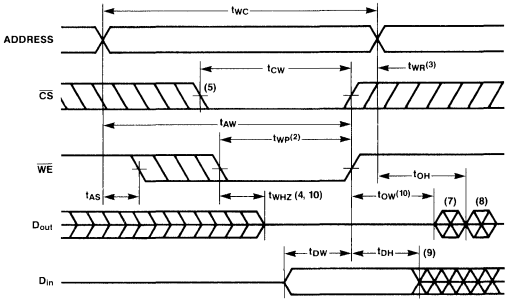
2

TIMING WAVEFORMS OF WRITE CYCLE 1(1) ($\overline{WE}$ CONTROLLED)



SRD6116SA/LA-010

TIMING WAVEFORMS OF WRITE CYCLE 2(1) ($\overline{CS}$ CONTROLLED)

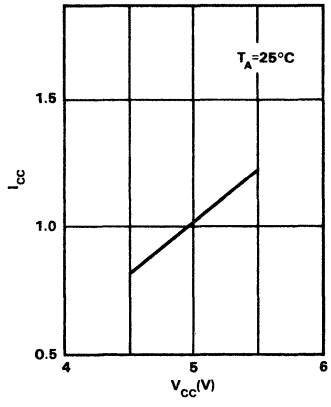


SRD6116SA/LA-011

NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

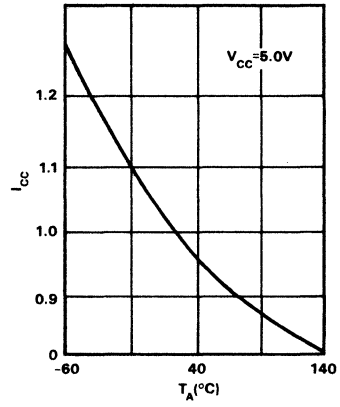
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

I_{CC} vs. Supply Voltage



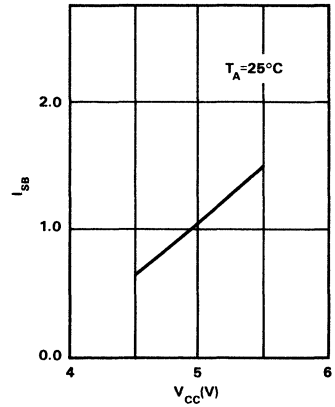
SRD6116SA/LA-012

I_{CC} vs. Temperature



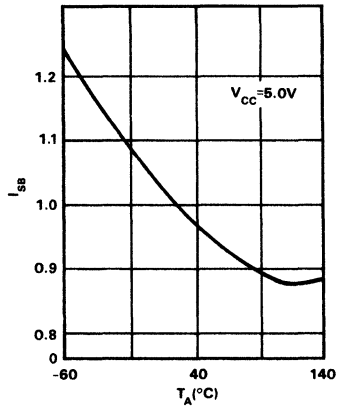
SRD6116SA/LA-013

I_{SB} vs. Supply Voltage



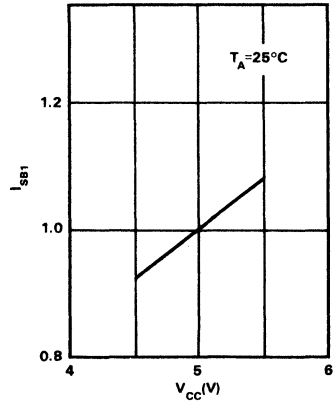
SRD6116SA/LA-014

I_{SB} vs. Temperature



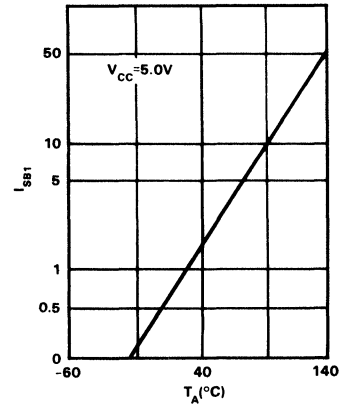
SRD6116SA/LA-015

I_{SB1} vs. Supply Voltage



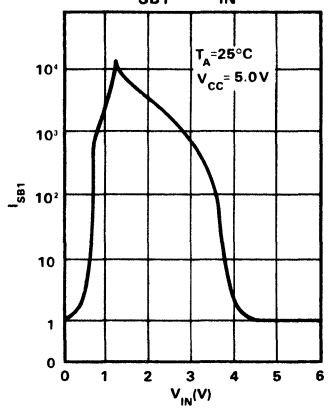
SRD6116SA/LA-016

I_{SB1} vs. Temperature



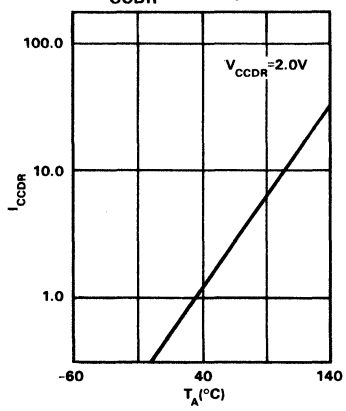
SRD6116SA/LA-017

I_{SB1} vs. V_{IN}



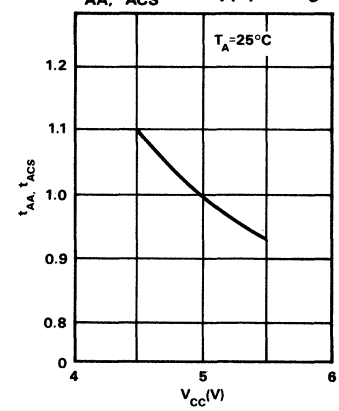
SRD6116SA/LA-018

I_{CCDR} vs. Temperature



SRD6116SA/LA-019

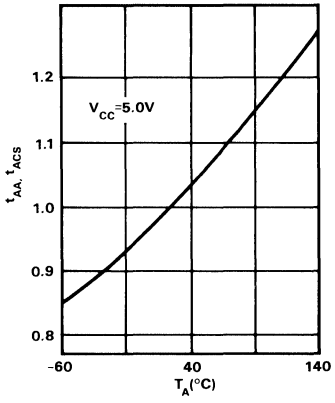
t_{AA}, t_{ACS} vs. Supply Voltage



SRD6116SA/LA-020

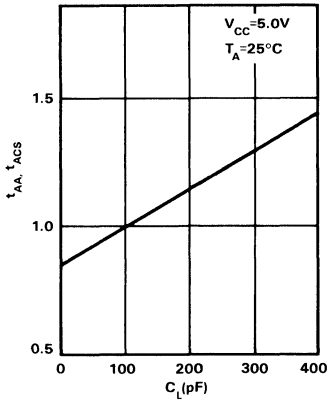
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

t_{AA}, t_{ACS} vs. Temperature



SRD6116SA/LA-021

t_{AA}, t_{ACS} vs. Output Loading



SRD6116SA/LA-022

2

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

PINOUT CONFIGURATION

16K CMOS SRAM

IDT6116 (2K x 8)

FUNCTION	LOGIC SYMBOL	PIN NUMBER 24 DIP	28 LCC	32 LCC
Address Line	A_7	1	1	4
Address Line	A_6	2	2	5
Address Line	A_5	3	3	6
Address Line	A_4	4	4	7
Address Line	A_3	5	5	8
Address Line	A_2	6	6	9
Address Line	A_1	7	9	10
Address Line	A_0	8	10	11
Input/Output	I/O 1	9	11	13
Input/Output	I/O 2	10	12	14
Input/Output	I/O 3	11	13	15
Power Ground	GND	12	14	16
Input/Output	I/O 4	13	15	18
Input/Output	I/O 5	14	16	19
Input/Output	I/O 6	15	17	20
Input/Output	I/O 7	16	18	21
Input/Output	I/O 8	17	19	22
Chip Select/ Data Retention	$\overline{CS}$	18	20	23
Address Line	A_{10}	19	23	24
Output Enable	$\overline{OE}$	20	24	25
Write Enable	$\overline{WE}$	21	25	26
Address Line	A_9	22	26	28
Address Line	A_8	23	27	29
Power Supply	V_{CC}	24	28	32

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - —Military — 25/35/45/55/70/85/100ns (max.)
  - —Commercial — 15/20/25/35/45/55ns (max.)
- Low-power consumption
  - —IDT6167SA
    - Active: 200mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6167LA
    - Active: 150mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6167LA only)
- High-density 20-pin DIP, 20-pin plastic DIP and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

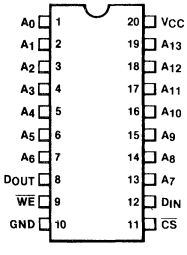
Access times as fast as 15ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

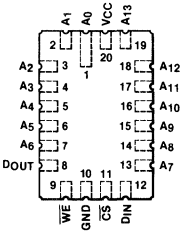
The IDT6167 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



DIP
TOP VIEW

SRD6167-001



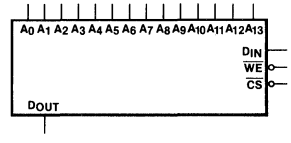
LCC
TOP VIEW

SRD6167-002

PIN NAMES

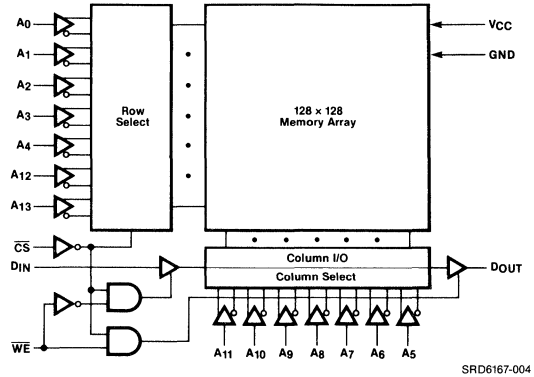
A_0-A_{13}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

LOGIC SYMBOL



SRD6167-003

FUNCTIONAL BLOCK DIAGRAM



SRD6167-004

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6167SA MIN.	IDT6167SA TYP.(1)	IDT6167SA MAX.	IDT6167LA MIN.	IDT6167LA TYP.(1)	IDT6167LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 12mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	15ns COM'L.	15ns MIL.	20ns COM'L.	20ns MIL.	25ns COM'L.	25ns MIL.	35ns COM'L.	35ns MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	70ns(2) COM'L.	70ns(2) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	SA	90	—	90	—	90	90	90	90	90	90	90	90	—	90	mA
		LA	—	—	55	—	55	60	55	60	55	60	55	60	—	60	
I_{CC2}	Dyn. Op. Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	SA	100	—	100	—	100	100	100	100	100	100	100	100	—	100	mA
		LA	—	—	80	—	70	75	65	70	60	65	55	60	—	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	SA	35	—	35	—	35	35	35	35	35	35	35	35	—	35	mA
		LA	—	—	30	—	25	25	20	20	15	20	15	20	—	15	
I_{SB1}	Full Stdby. Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	SA	5	—	5	—	5	10	5	10	5	10	5	10	—	10	mA
		LA	—	—	0.05	—	0.05	0.9	0.05	0.9	0.05	0.9	0.05	0.9	—	0.9	

NOTE:

1. All values are maximum guaranteed values.
2. Also available: 85 and 100ns Military devices.

DATA RETENTION CHARACTERISTICS

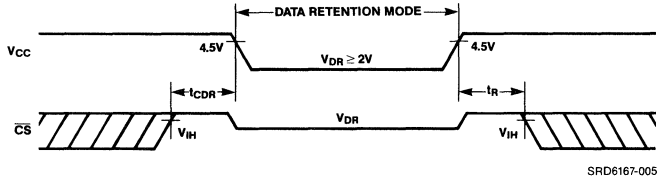
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1)		MAX.		UNIT
					V_{CC} @ 2.0V	V_{CC} @ 3.0V	V_{CC} @ 2.0V	V_{CC} @ 3.0V	
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL. COM'L.	— —	0.5 0.5	1.0 1.0	200 20	300 30	μA
t_{CDR}	Chip Deselect to Data Retention Time			0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		μA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

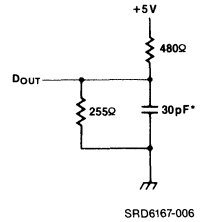
LOW V_{CC} DATA RETENTION WAVEFORM



SRD6167-005

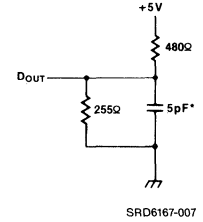
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1 and 2



SRD6167-006

Figure 1. Output Load



SRD6167-007

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

AC ELECTRICAL CHARACTERISICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

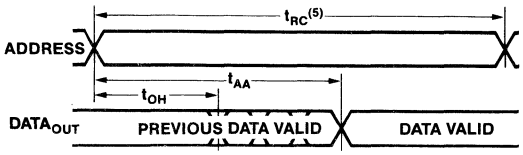
SYMBOL	PARAMETER	6167SA15[3] 6167LA15[3] MIN.	MAX.	6167SA20[3] 6167LA20[3] MIN.	MAX.	6167SA25 6167LA25 MIN.	MAX.	6167SA35 6167LA35 MIN.	MAX.	6167SA45 6167LA45 MIN.	MAX.	6167SA55 6167LA55 MIN.	MAX.	6167SA70[1] 6167LA70[1] MIN.	MAX.	UNITS
READ CYCLE																
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	3	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}[2]	Chip Select to Output in Low Z	3	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}[2]	Chip Deselect to Output in High Z	—	10	—	10	—	10	—	15	—	30	—	40	—	40	ns
t_{PU}[2]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[2]	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	35	—	35	—	55	—	70	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	15	—	20	—	20	—	30	—	45	—	55	—	70	—	ns
t_{CW}	Chip Select to End of Write	15	—	15	—	20	—	30	—	40	—	45	—	55	—	ns
t_{AW}	Address Valid to End of Write	15	—	15	—	20	—	30	—	40	—	45	—	55	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	13	—	15	—	20	—	30	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	12	—	13	—	15	—	20	—	25	—	25	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}[2]	Write Enable to Output in High Z	—	10	—	10	—	10	—	15	—	30	—	40	—	40	ns
t_{OW}[2]	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

1. Available over -55°C to +125°C temperature range only. Also available: 85 and 100ns Military devices.
2. This parameter guaranteed but not tested.
3. Available over 0°C to +70°C temperature range only.

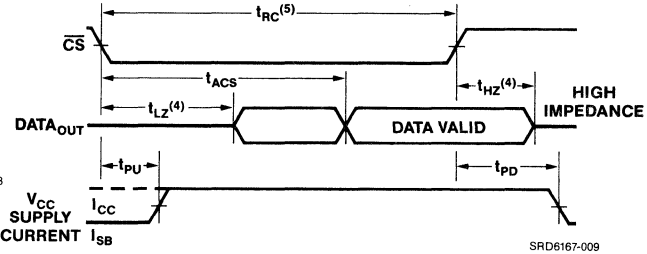
2

TIMING WAVEFORM OF READ CYCLE NO.1(1, 2)



SRD6167-008

TIMING WAVEFORM OF READ CYCLE NO.2(1, 3)

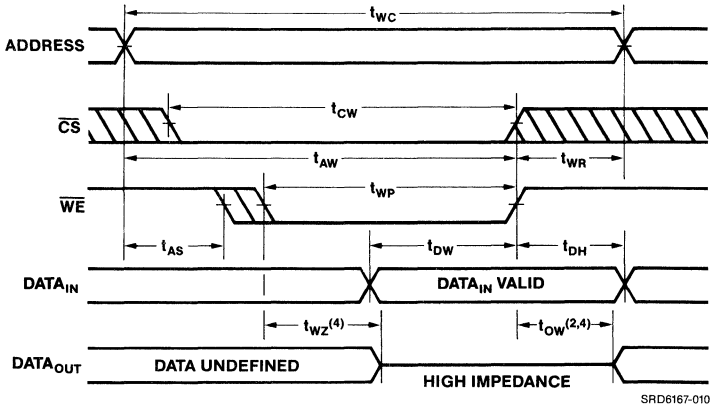


SRD6167-009

NOTES:

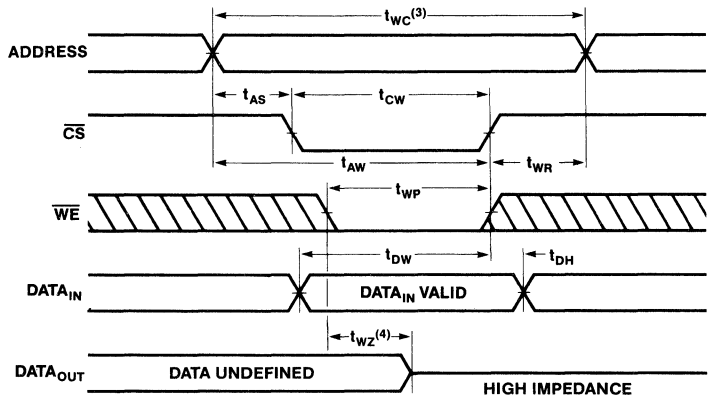
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED)(1)



SRD6167-010

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED)(1)



SRD6167-011

NOTES:

1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

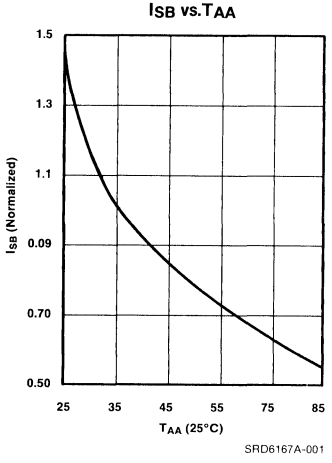
MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

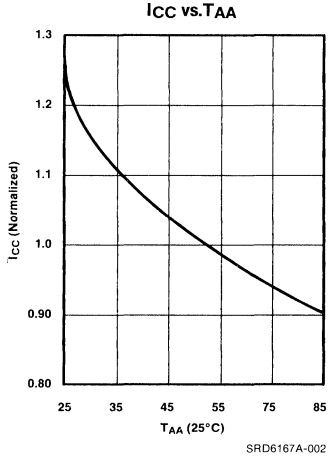
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

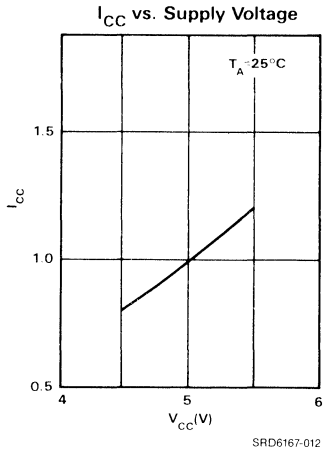
SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

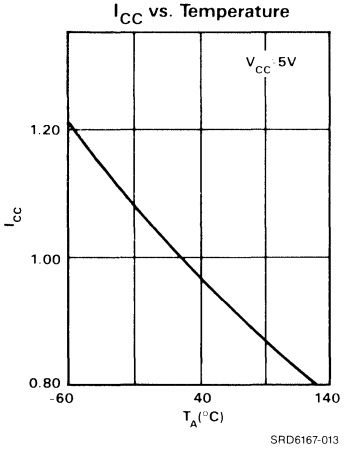
NOTE:
1. This parameter is sampled and not 100% tested.

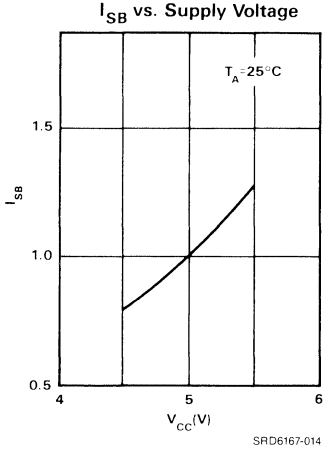
NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

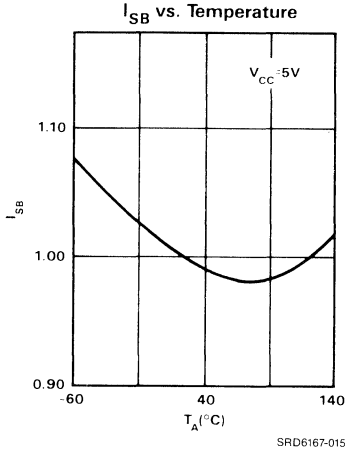






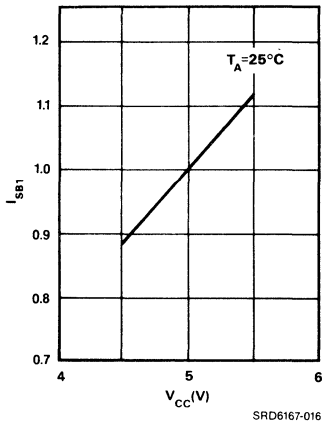






NORMALIZED TYPICAL DC AND AC CHARACTERISTICS (CONTINUED)

I_{SB1} vs. Supply Voltage



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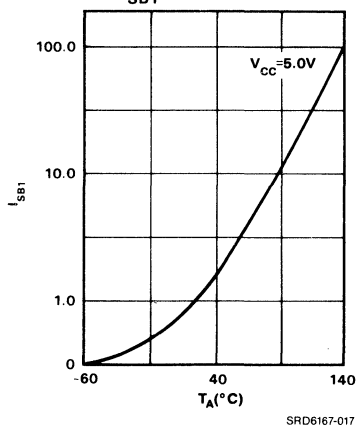
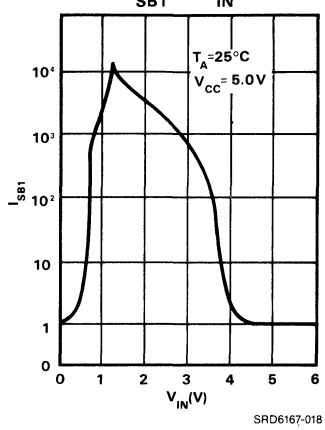
I_{SB1} vs. Temperature



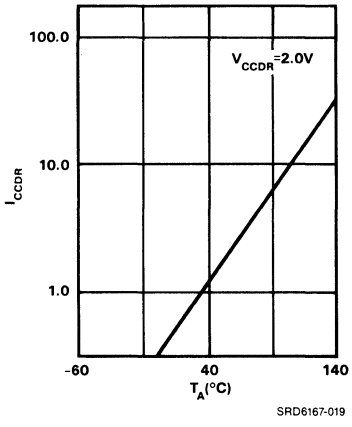
SRD6167-017

I_{SB1} vs. V_{IN}



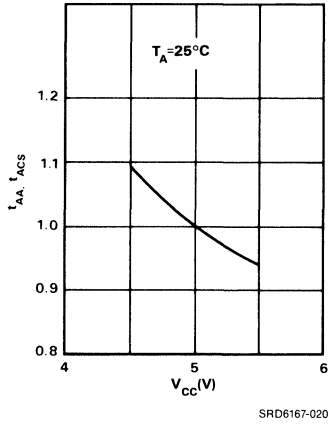
SRD6167-018

I_{CCDR} vs. Temperature



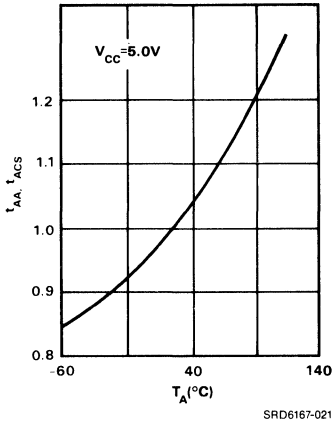
SRD6167-019

t_{AA}, t_{ACS} vs. Supply Voltage



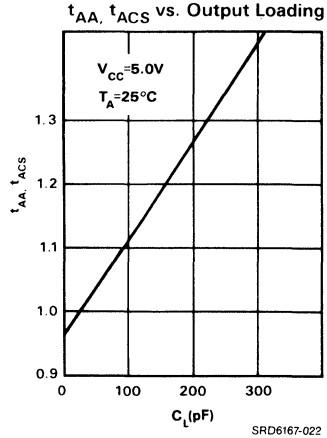
SRD6167-020

t_{AA}, t_{ACS} vs. Temperature



SRD6167-021

t_{AA}, t_{ACS} vs. Output Loading



SRD6167-022

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K × 4 BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - —Military: 25/35/45/55/70/85/100ns (max.)
  - —Commercial: 20/25/35/45/55ns (max.)
- Low-power consumption
  - —IDT6168SA
    - Active: 225mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT6168LA
    - Active: 225mW (typ.)
    - Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin DIP, 20-pin plastic DIP and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 20ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

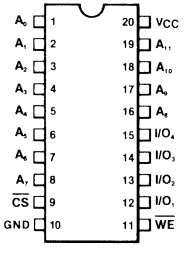
All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6168 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

The IDT6168 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

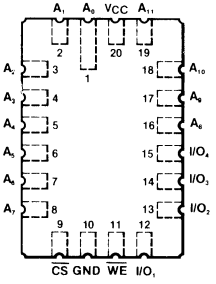
2

PIN CONFIGURATIONS



SSD6168-001

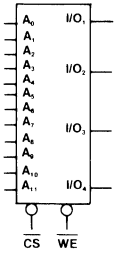
DIP
TOP VIEW



SSD6168-002

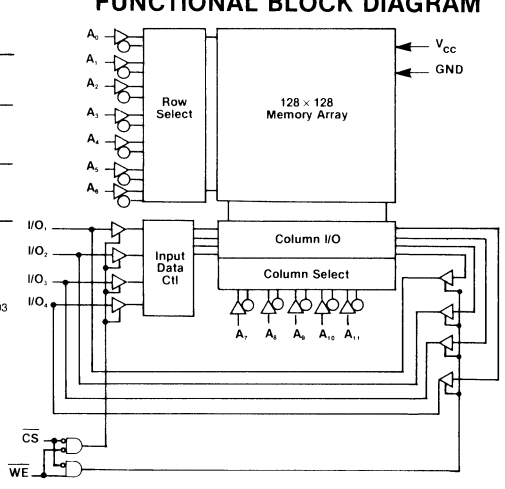
LCC
TOP VIEW

LOGIC SYMBOL



SSD6168-003

FUNCTIONAL BLOCK DIAGRAM



SSD6168-004

PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	I/O_1–I/O_4	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6168SA MIN.	IDT6168SA TYP.(1)	IDT6168SA MAX.	IDT6168LA MIN.	IDT6168LA TYP.(1)	IDT6168LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	2	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	2	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	20ns COM'L.	20ns MIL.	25ns COM'L.	25ns MIL.	35ns COM'L.	35ns MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	70ns(2) COM'L.	70ns(2) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	SA	90	—	90	100	90	100	90	100	90	100	—	100	mA
		LA	70	—	70	80	70	80	70	80	70	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	SA	120	—	110	120	100	110	100	110	100	110	—	110	mA
		LA	100	—	90	100	80	90	70	80	70	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	SA	45	—	35	45	30	35	30	35	30	35	—	35	mA
		LA	30	—	25	30	20	25	20	25	20	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	SA	20	—	2	10	2	10	2	10	2	10	—	10	mA
		LA	2	—	0.05	0.3	0.05	0.3	0.05	0.3	0.05	0.3	—	0.3	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85 and 100ns military devices.

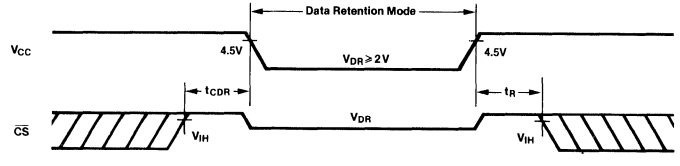
DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT76168SA/LA MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(4)			ns

NOTES:

1. T_A = 25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time
5. This parameter is guaranteed but not tested.

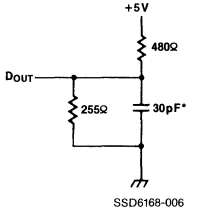
LOW V_{CC} DATA RETENTION WAVEFORM



SSD6168-005

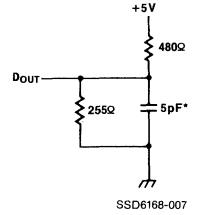
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SSD6168-006

Figure 1. Output Load



SSD6168-007

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

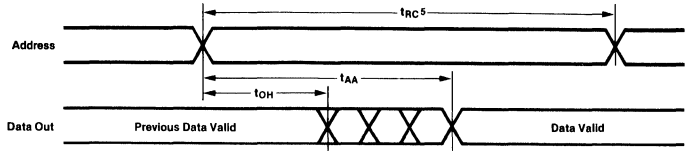
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	6168SA20[1] 6168LA20[1]		6168SA25 6168LA25		6168SA35 6168LA35		6168SA45 6168LA45		6168SA55 6168LA55		6168SA70[2] 6168LA70[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	—	10	—	10	—	15	—	15	—	25	—	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time[3]	—	20	—	25	—	35	—	40	—	50	—	60	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Select to End of Write	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	13	—	13	—	17	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{WZ}	Write Enable to Output in High Z[3]	—	7	—	7	—	13	—	20	—	25	—	30	ns
t_{OW}	Output Active from End of Write[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns

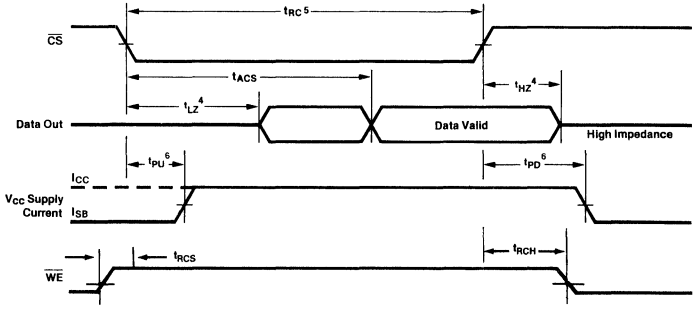
NOTES:

1. Available over 0°C to +70°C temperature range only.
2. Available over -55°C to +125°C temperature range only. Also available: 85 and 100ns military devices.
3. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

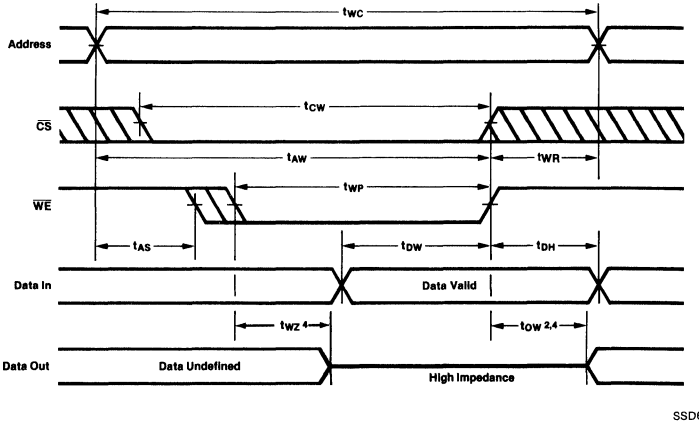


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

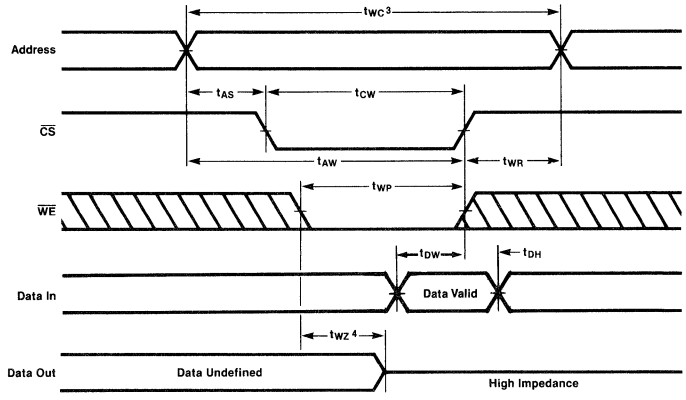


NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced the last valid address to the first transitioning address.
6. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



SSD6168-011

NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

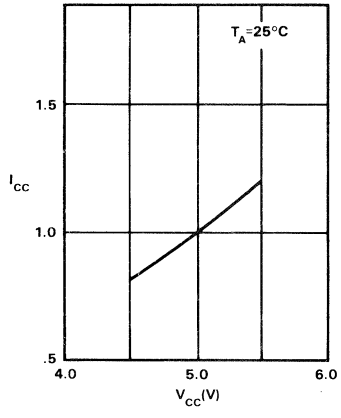
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

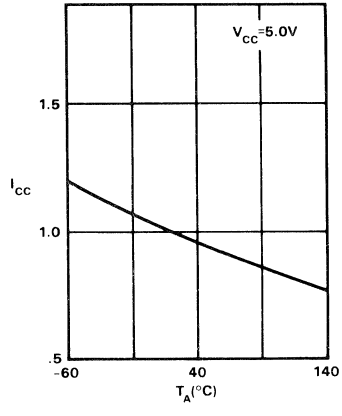
NOTE:
1. This parameter is sampled and not 100% tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

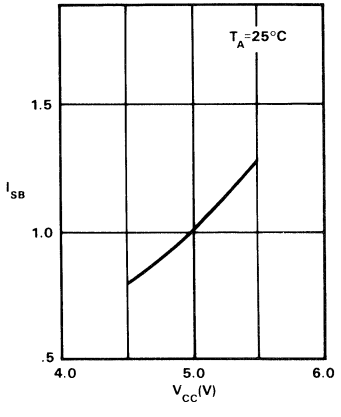
I_{CC} vs. Supply Voltage



I_{CC} vs. Temperature

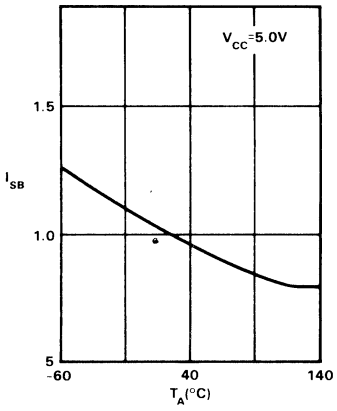


I_{SB} vs. Supply Voltage

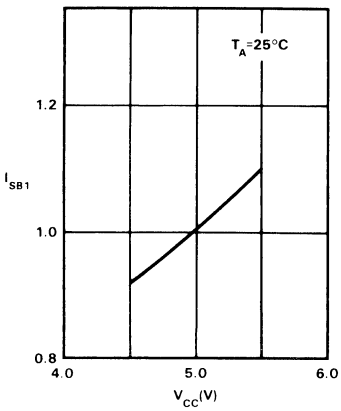


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

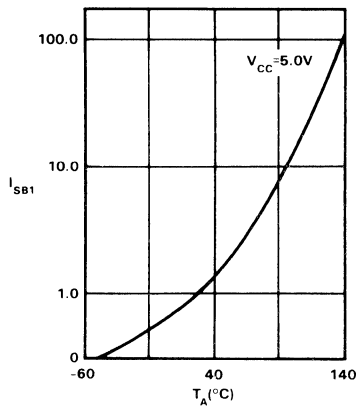
I_{SB} vs. Temperature



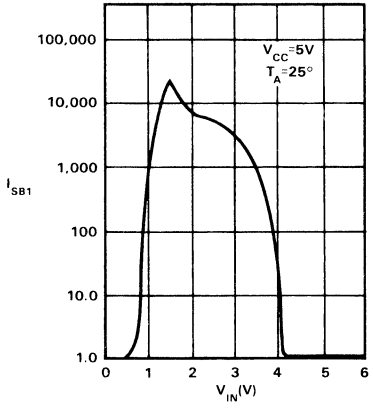
I_{SB1} vs. Supply Voltage



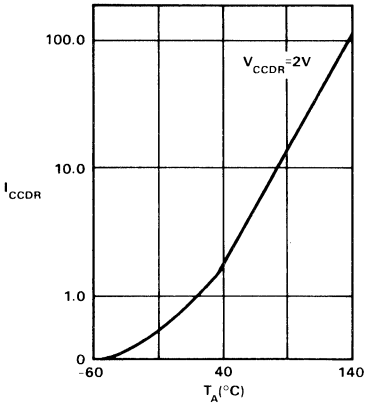
I_{SB1} vs. Temperature



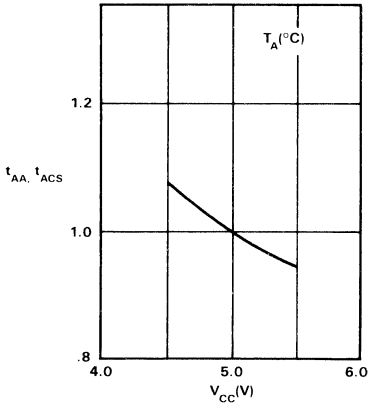
I_{SB1} vs. V_{IN}



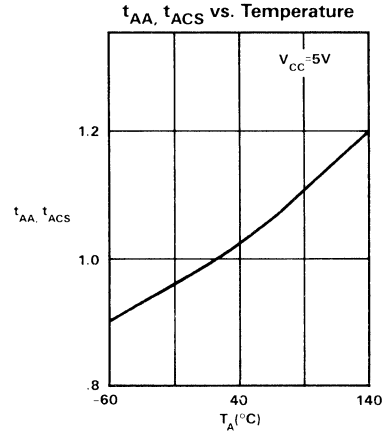
I_{CCDR} vs. Temperature



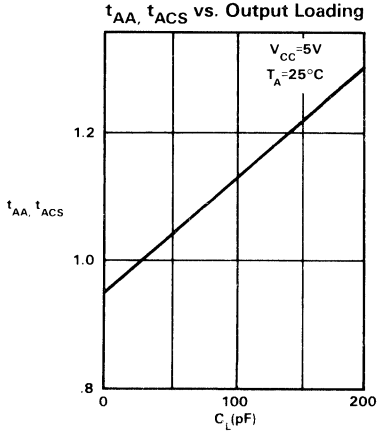
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

ADVANCE INFORMATION
IDT71256S
IDT71256L

FEATURES:

- High-speed address/chip select access time
  - —Military: 55/70/85ns (max.)
  - —Commercial: 45/55/70ns (max.)
- Low-power operation
  - —IDT71256S
    - Active: 300mW (typ.)
    - Standby: 200μW (typ.))
  - —IDT71256L
    - Active: 250mW (typ.)
    - Standby: 50μW (typ.)
- Battery backup operation — 2V data retention
- Produced with advanced high-performance CEMOS™ technology
- Single 5V (±10%) power supply
- Input and output directly TTL compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 mil), 28-pin THINDIP (400 mil) and 32-pin LCC
- Pin compatible with standard 256K static RAM and EPROM
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology.

Address access times as fast as 45ns are available with typical power consumption of only 300mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode. In the full standby mode, the low-power device consumes less than 50μW, typically. The low-power version (L) offers a battery backup data retention capability where the circuit typically consumes only 20μW operating off a 2V battery.

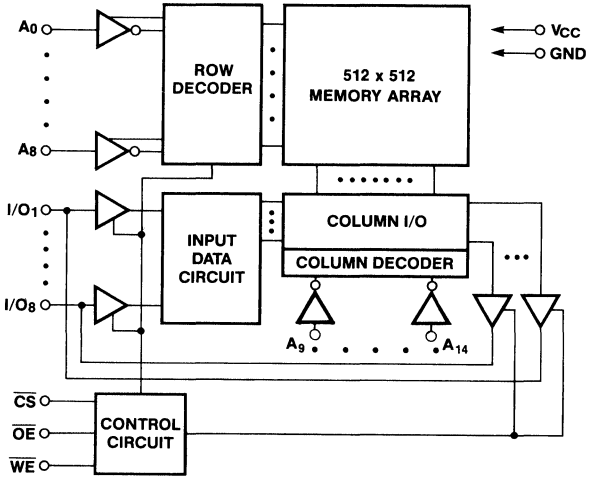
All inputs and outputs of the IDT71256 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT71256 is packaged in either a 28-pin 400 mil THINDIP, a 28-pin 600 mil DIP or 32-pin leadless chip carrier, providing high board-level packing densities.

The IDT71256 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performances and reliability.

2

FUNCTIONAL BLOCK DIAGRAM



SRD71256-001

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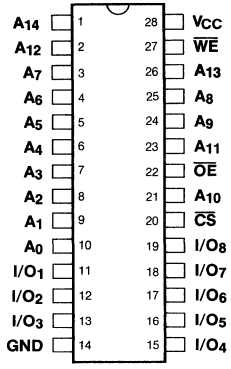
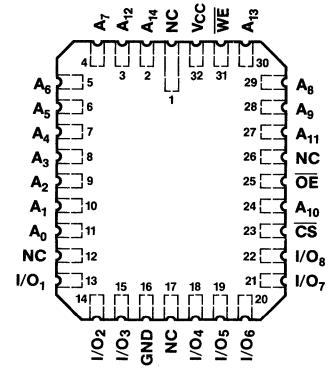
PIN CONFIGURATIONS



DIP
TOP VIEW

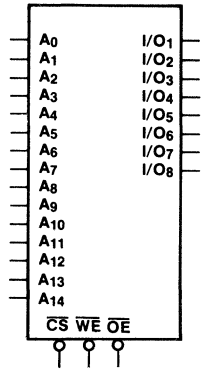
SRD71256-002



LCC
TOP VIEW

SRD71256-003

LOGIC SYMBOL



SRD71256-004

PIN NAMES

A_{0-14}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (256K x 1-BIT)

ADVANCE INFORMATION
IDT71257S
IDT71257L

FEATURES:

- High-speed (equal access and cycle times)
  - —Military — 45/55/70/85ns max.
  - —Commercial — 35/45/55/70ns max.
- Low-power operation
  - —IDT 71257S
    Active: 400mW (typ.)
    Standby: 400μW (typ.)
  - —IDT 71257L
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density industry standard 24-pin, 300 mil DIP
- Produced with advanced CEMOS™ technology
- Separate data input and output
- Single 5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three state outputs
- Static operation — no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71257, a 262,144-bit high-speed static RAM organized as 256K x 1, is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 45ns are available, with typical power consumption of only 400mW. The IDT71257 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 80μW when operating from a 2V battery.

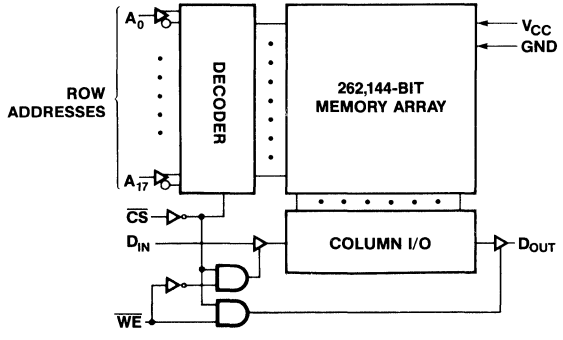
All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT71257 is packaged in a 24-pin, 300 mil DIP providing excellent board-level packing densities.

The IDT71257 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

2

FUNCTIONAL BLOCK DIAGRAM

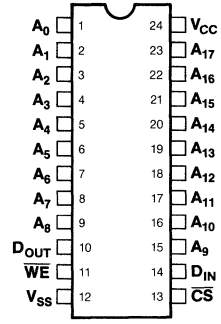


SRD71257-001

CEMOS is a trademark of Integrated Device Technology, Inc.

Printed in U.S.A.

PIN CONFIGURATION



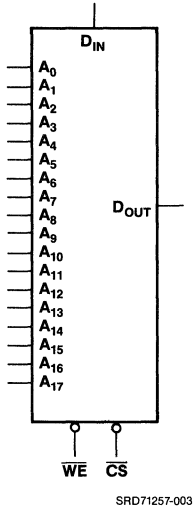
DIP
TOP VIEW

SRD71257-002

PIN NAMES

A_{0-17}	Address Inputs
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

LOGIC SYMBOL



SRD71257-003

Integrated Device Technology, Inc.

CMOS STATIC RAMS 256K (64K x 4-BIT)

ADVANCE INFORMATION
IDT71258S
IDT71258L

FEATURES:

- High-speed (equal access and cycle times)
  - —Military — 45/55/70/85ns max.
  - —Commercial — 35/45/55/70ns max.
- Low-power operation
  - —IDT71258S
    Active: 400mW (typ.)
    Standby: 400μW (typ.)
  - —IDT71258L
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density industry standard 24-pin, 300 mil DIP
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Single 5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three state outputs
- Static operation — no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71258, a 262,144-bit high-speed static RAM organized as 64K x 4, is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 35ns are available, with typical power consumption of only 400mW. The IDT71258 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 80μW when operating from a 2V battery.

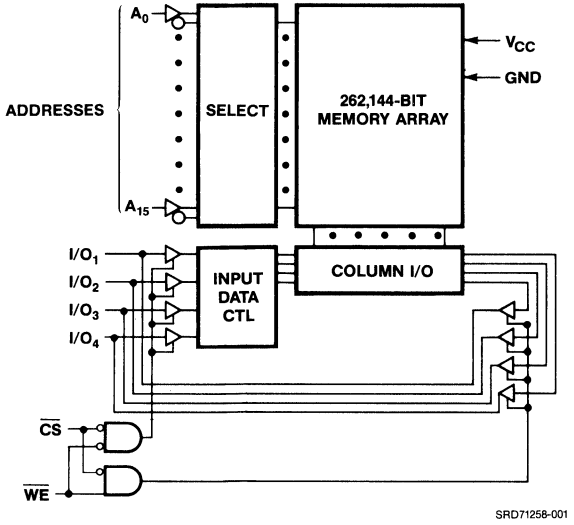
All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT71258 is packaged in a 24-pin, 300 mil DIP providing excellent board-level packing densities.

The IDT71258 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

2

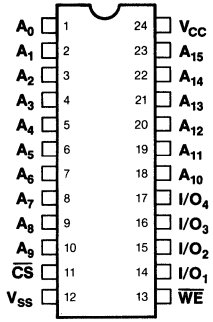
FUNCTIONAL BLOCK DIAGRAM



SRD71258-001

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



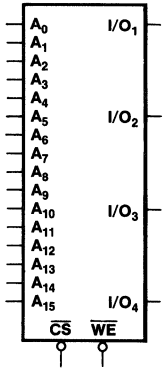
DIP
TOP VIEW

SRD71258-002

PIN NAMES

A_{0-15}	Address Inputs
I/O_{1-4}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

LOGIC SYMBOL



SRD71258-003

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 8K (1K x 8-BIT)

IDT7130S/L
IDT7140S/L

FEATURES:

- High-speed access
  - —Military: 70/90/100/120ns (max.)
  - —Commercial: 55/70/90/100ns (max.)
- Low-power operation
  - —IDT7130/40S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT7130/40L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation — 2V data retention
- TTL compatible, single 5V ± 10% power supply
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

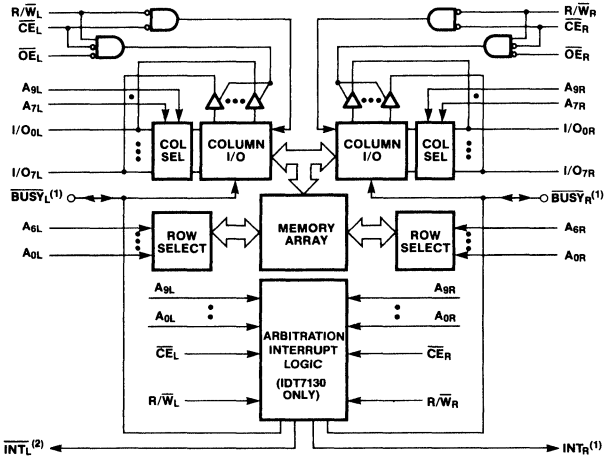
The IDT7130/IDT7140 are high-speed 1K x 8 dual-port static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7140 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 55ns. Low-power (L) versions offer battery backup data retention capability, with each dual-port typically consuming 200μW from a 2V battery.

The IDT7130/7140 devices are packaged in 48-pin sidebraze, plastic DIP, 48- or 52-pin LCC and 52-pin PLCC, with the military devices available 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

2



SRD7130-002

NOTES:

1. IDT7130 (master): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (slave): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

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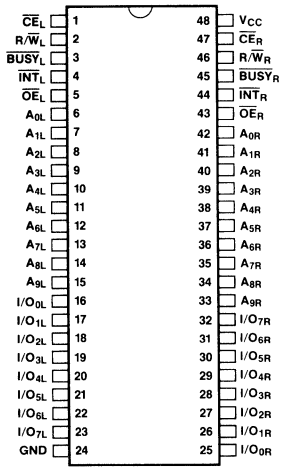
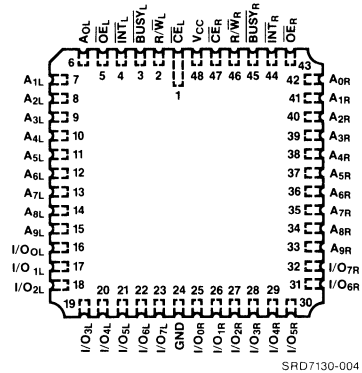
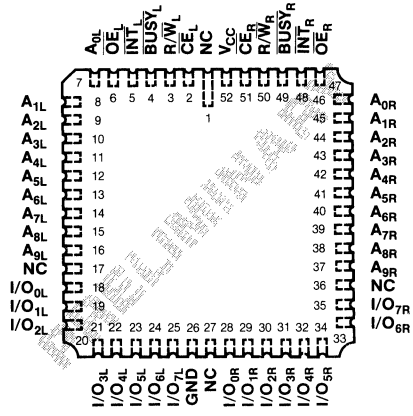
PIN CONFIGURATIONS



DIP
TOP VIEW



48-PIN LCC
TOP VIEW



52-PIN LCC & PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7130S IDT7140S MIN.	IDT7130S IDT7140S MAX.	IDT7130L IDT7140L MIN.	IDT7130L IDT7140L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{IH}	Input High Voltage		2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage		-1.0(1)	0.8	-1.0(1)	0.8	V
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 4.0mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:

1. V_{IL} min. = -3.5V for pulse width less than 30ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		VERSION	7130x55(2) 7140x55 TYP(4)	7130x55(2) 7140x55 MAX	7130x70 7140x70 TYP(4)	7130x70 7140x70 MAX	7130x90/100 7140x90/100 TYP(4)	7130x90/100 7140x90/100 MAX	7130x120(3) 7140x120 TYP(4)	7130x120(3) 7140x120 MAX	UNITS
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open	MIL.	S	—	—	65	225	65	185	65	185	mA
				L	—	—	65	180	65	150	65	150	
			COM'L.	S	65	170	65	170	65	170	—	—	
				L	65	120	65	120	65	120	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	MIL.	S	—	—	25	65	25	65	25	65	mA
				L	—	—	25	55	25	45	25	45	
			COM'L.	S	25	65	25	60	25	50	—	—	
				L	25	45	25	40	25	30	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	MIL.	S	—	—	40	135	40	125	40	125	mA
				L	—	—	40	110	40	100	40	100	
			COM'L.	S	40	115	40	110	40	110	—	—	
				L	40	85	40	85	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	MIL.	S	—	—	1	30	1	30	1	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1	15	1	15	—	—	
				L	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open	MIL.	S	—	—	40	110	40	110	40	110	mA
				L	—	—	35	80	35	80	35	80	
			COM'L.	S	40	90	40	90	40	90	—	—	
				L	35	70	35	70	35	65	—	—	

NOTES:

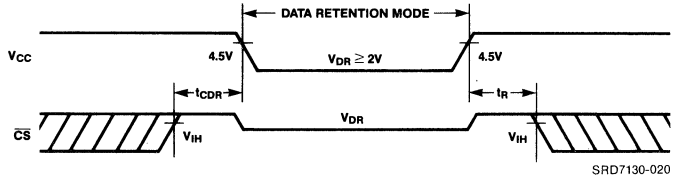
1. X in part numbers represents versions (S or L).
2. Available in Commercial 0°C to +70°C temperature range only.
3. Available in Military -55°C to +125°C temperature range only.
4. V_{CC} = 5V, T_A = +25°C.

DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7130L/IDT7140L MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

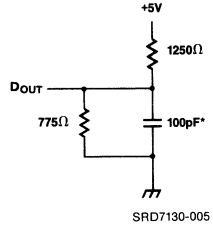


Figure 1.
Output Load

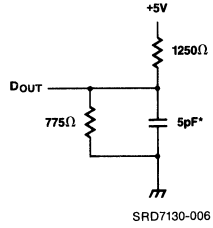


Figure 2.
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

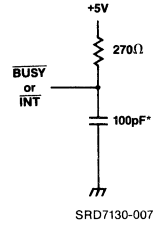


Figure 3.
$\overline{BUSY}$ and $\overline{INT}$
Output Load
(IDT7130 only)

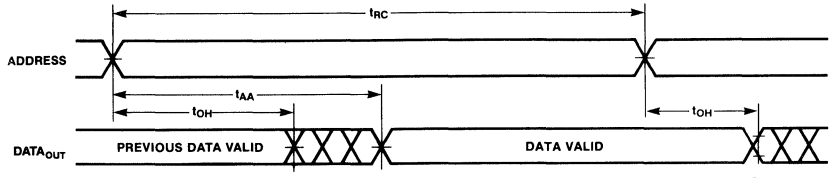
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	IDT7130S/L55[2] IDT7140S/L55[2] MIN.	MAX.	IDT7130S/L70 IDT7140S/L70 MIN.	MAX.	IDT7130S/L90 IDT7140S/L90 MIN.	MAX.	IDT7130S/L100 IDT7140S/L100 MIN.	MAX.	IDT7130S/L120[3] IDT7140S/L120[3] MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
t_{ACE}	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
t_{AOE}	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
t_{LZ}	Output Low Z Time[1,4]	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
t_{PU}	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time[10]	55	—	70	—	90	—	100	—	120	—	ns
t_{EW}	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	60	—	70	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
t_{HZ}	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z[1,4]	—	30	—	35	0	40	0	40	0	50	ns
t_{OW}	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns
BUSY TIMING												
t_{WB}	Write to $\overline{BUSY}$[5,8]	-10	—	-10	—	-10	—	-10	—	-10	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[9]	20	—	20	—	20	—	20	—	20	—	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
t_{BDC}	$\overline{BUSY}$ Disable time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
t_{WDD}	Write Pulse to Data Delay[6]	—	80	—	90	—	100	—	120	—	140	ns
t_{DDD}	Write Data Valid to Read Data Delay[6]	—	55	—	70	—	90	—	100	—	120	ns
t_{APS}	Arbitration Priority Set Up Time	5	—	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[7]	—	Note 7	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns
INTERRUPT TIMING												
t_{AS}	Address Set Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	45	—	50	—	55	—	60	—	70	ns
t_{INR}	Interrupt Reset Time	—	45	—	50	—	55	—	60	—	70	ns

NOTES:

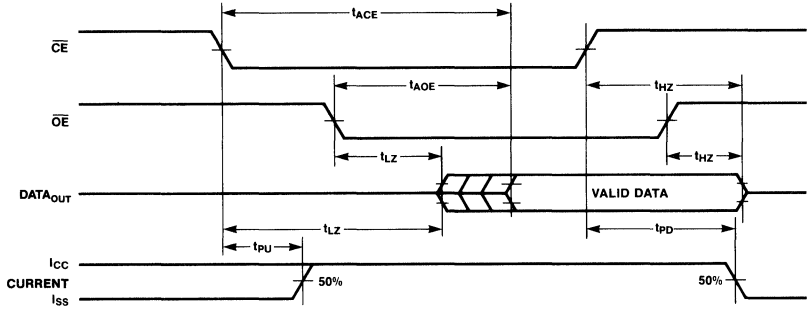
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 & 3).
2. Available over 0°C to +70°C temperature range only.
3. Available over -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For Slave part (IDT7140) only.
6. Port to port delay through RAM cells from writing port to reading port.
7. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
8. To ensure that the write cycle is inhibited during contention.
9. To ensure that a write cycle is completed after contention.
10. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$.

TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE(1,2,6)



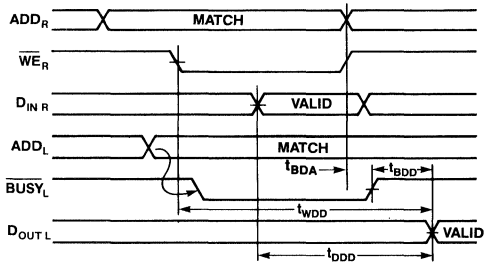
SRD7130-008

TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE(1,3)



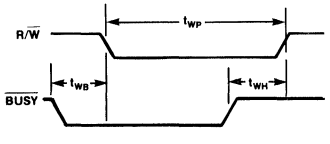
SRD7130-009

TIMING WAVEFORM OF READ WITH BUSY



SRD7130-023

TIMING WAVEFORM OF WRITE WITH BUSY



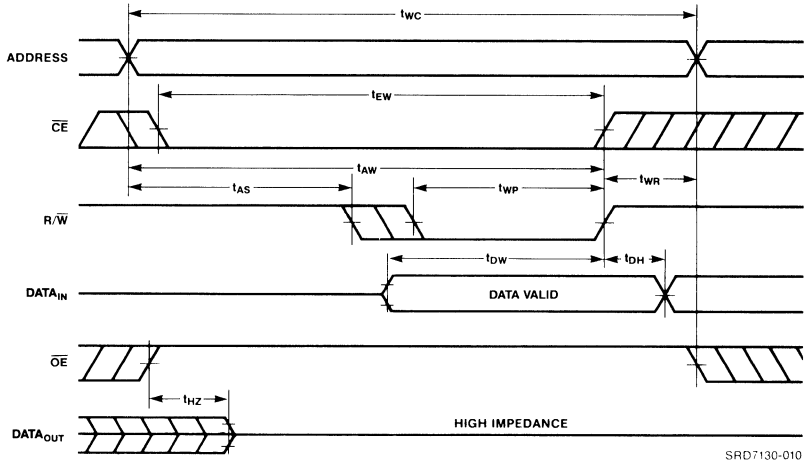
SRD7130-024

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

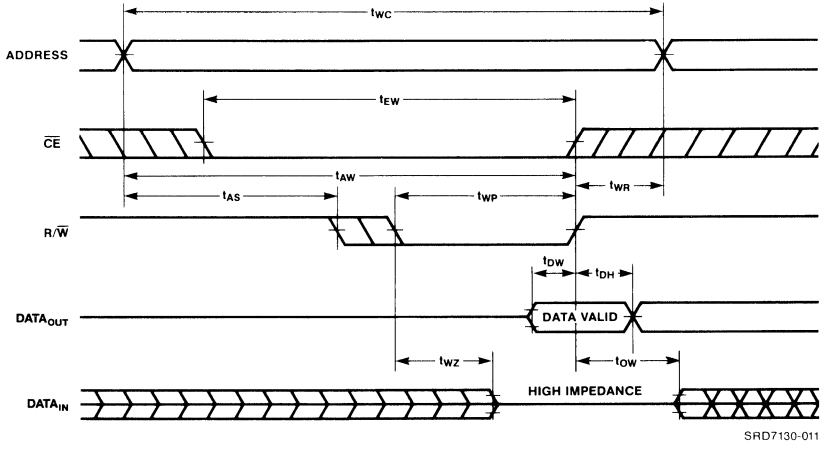
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 EITHER SIDE[4,7]



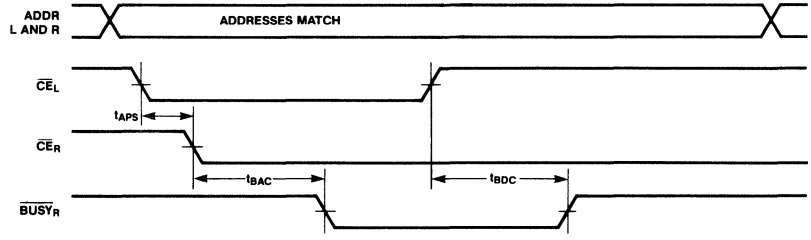
2

TIMING WAVEFORM OF WRITE CYCLE NO. 2 EITHER SIDE[4,7]



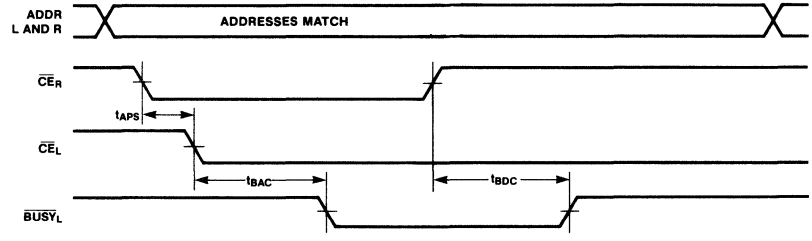
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



SRD7130-013

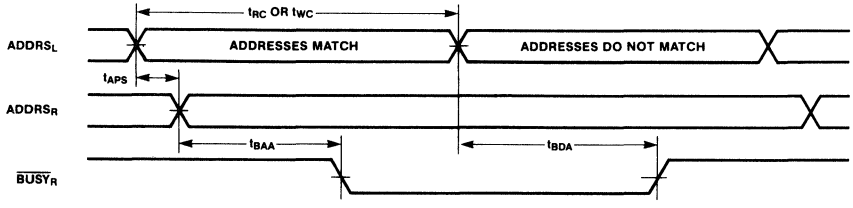
$\overline{CE}_R$ VALID FIRST



SRD7130-012

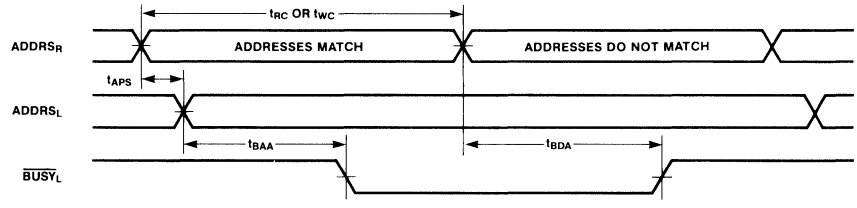
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST:



SRD7130-014

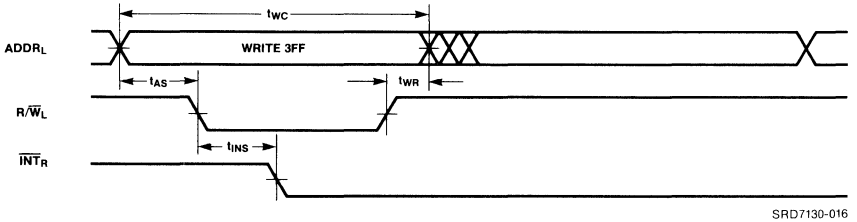
RIGHT ADDRESS VALID FIRST:



SRD7130-015

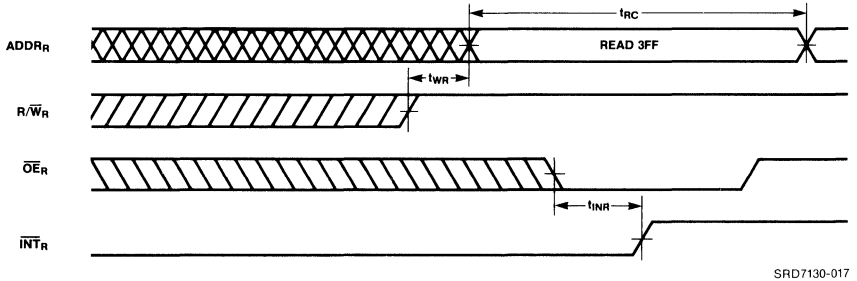
TIMING WAVEFORM OF INTERRUPT MODE(5,8)

LEFT SIDE SETS $\overline{INT}_R$:



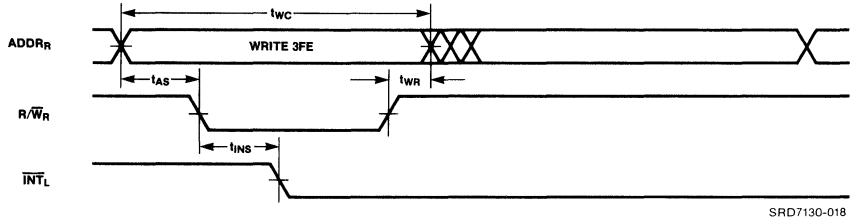
SRD7130-016

RIGHT SIDE CLEARS $\overline{INT}_R$:



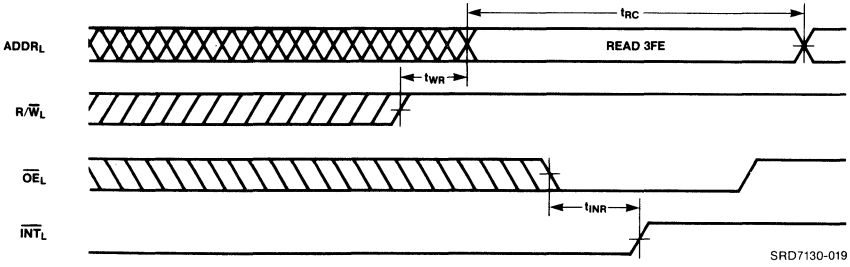
SRD7130-017

RIGHT SIDE SETS $\overline{INT}_L$:



SRD7130-018

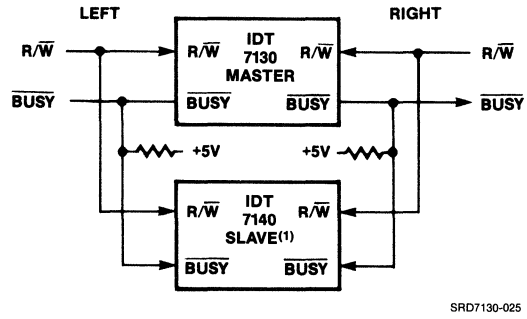
LEFT SIDE CLEARS $\overline{INT}_L$:



SRD7130-019

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
6. $\overline{OE} = V_{IL}$.
7. R/$\overline{W} = V_{IH}$ during address transition.
8. $\overline{INT}_R$ and $\overline{INT}_L$ are reset (high) during power up.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEM



SRD7130-025

NOTE:
1. No arbitration in IDT7140 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7140 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7130/40 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/40 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 3FE (HEX). The left port clears the interrupt by reading address location 3FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FF. The message (8-bits) at 3FE or 3FF is user-defined. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its L $\overline{BUSY}$ while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT[1]				FUNCTION
$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB1} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs
—	—	—	—	Data in Memory Output on Right Port

NOTES:

1. $A_{0L} - A_{9L} \neq A_{0R} - A_{9R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.

H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

TABLE II — INTERRUPT FLAG[1]

LEFT PORT					RIGHT PORT					FUNCTION
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{9L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0L}-A_R	$\overline{INT}_R$	
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.

H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS[1]		FUNCTION
$\overline{CE}_L$	A_{0L}-A_{9L}	$\overline{CE}_R$	A_{0R}-A_{9R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{9R}	L	$\neq A_{0L}$-A_{9L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	LV5R	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R} - A_{9R}$	LL5R	$= A_{0L} - A_{9L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{9R}$	RL5R	$= A_{0L} - A_{9L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{9R}$	LW5R	$= A_{0L} - A_{9L}$	L	H	Arbitration Resolved

NOTE:

1. INT Flags Don't Care.

X = DON'T CARE, L = LOW, H = HIGH

LV5R = Left Address Valid ≥ 5ns before right address.

RV5R = Right Address Valid ≥ 5ns before left address.

Same = Left and Right Addresses match within 5ns of each other.

LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.

RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.

LW5R = Left and Right $\overline{CE}$ = LOW within 5ns of each other.

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT7132S/L
IDT7142S/L

FEATURES:

- High-speed access
  - —Military: 70/90/100/120ns (max.)
  - —Commercial: 55/70/90/100ns (max.)
- Low-power operation
  - —IDT7132/42S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT7132/42L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Fully asynchronous operation from either port
- Battery backup operation — 2V data retention
- TTL compatible, single 5V ± 10% power supply
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 dual-port static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7142 "SLAVE" dual-port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

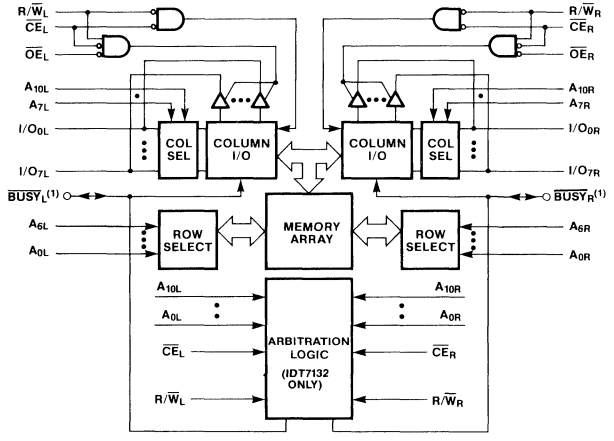
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by CE permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 55ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT7132/7142 devices are packaged in either a 48-pin sidebraze or plastic DIP, or 48- or 52-pin LCC and 52-pin PLCC, with the military devices available 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

2

FUNCTIONAL BLOCK DIAGRAM

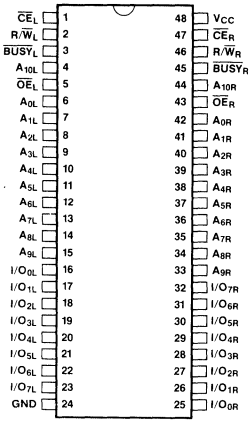


SRD7132-001

NOTE:
1. IDT7132 (master): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7142 (slave): $\overline{BUSY}$ is input.

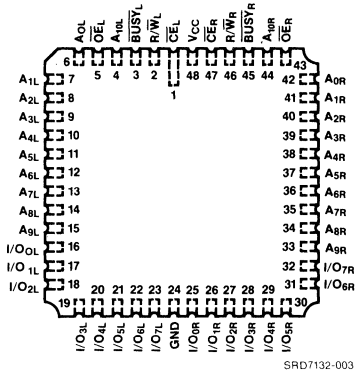
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



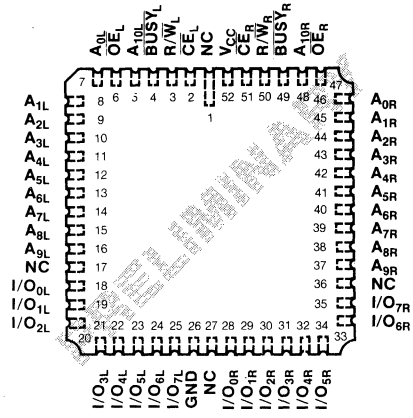
SRD7132-002

DIP
TOP VIEW



SRD7132-003

48-PIN LCC
TOP VIEW



52-PIN LCC & PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7132S IDT7142S MIN.	IDT7132S IDT7142S MAX.	IDT7132L IDT7142L MIN.	IDT7132L IDT7142L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{IH}	Input High Voltage		2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage		-1.0(1)	0.8	-1.0(1)	0.8	V
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$, INT)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:

1. V_{IL} min. = -3.5V for pulse width less than 30ns.

2

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		VERSION	7132x55(2) 7142x55 TYP(4)	7132x55(2) 7142x55 MAX	7132x70 7142x70 TYP(4)	7132x70 7142x70 MAX	7132x90/100 7142x90/100 TYP(4)	7132x90/100 7142x90/100 MAX	7132x120(3) 7142x120 TYP(4)	7132x120(3) 7142x120 MAX	UNITS
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open	MIL.	S	—	—	65	225	65	185	65	185	mA
				L	—	—	65	180	65	150	65	150	
			COM'L.	S	65	170	65	170	65	170	—	—	
				L	65	120	65	120	65	120	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	MIL.	S	—	—	25	65	25	65	25	65	mA
				L	—	—	25	55	25	45	25	45	
			COM'L.	S	25	65	25	60	25	50	—	—	
				L	25	45	25	40	25	30	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	MIL.	S	—	—	40	135	40	125	40	125	mA
				L	—	—	40	110	40	100	40	100	
			COM'L.	S	40	115	40	110	40	110	—	—	
				L	40	85	40	85	40	75	—	—	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	MIL.	S	—	—	1	30	1	30	1	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1	15	1	15	1	15	—	—	
				L	0.2	4	0.2	4	0.2	4	—	—	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open	MIL.	S	—	—	40	110	40	110	40	110	mA
				L	—	—	35	80	35	80	35	80	
			COM'L.	S	40	90	40	90	40	90	—	—	
				L	35	70	35	70	35	65	—	—	

NOTES:

1. X in part numbers represents versions (S or L).
2. Available in Commercial 0°C to +70°C temperature range only.
3. Available in Military -55°C to +125°C temperature range only.
4. V_{CC} = 5V, T_A = +25°C.

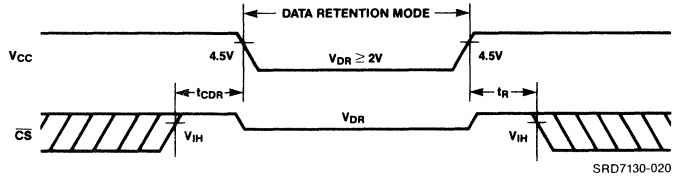
DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7130L/IDT7140L MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, CE ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL	—	100	4000	µA
			COM'L.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:

1. V_{CC} = 2V, T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

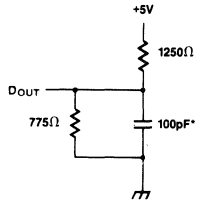


Figure 1.
Output Load

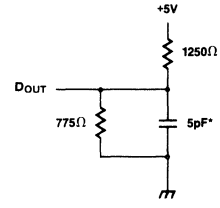


Figure 2.
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

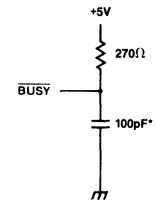


Figure 3.
$\overline{BUSY}$ Output Load
(IDT7132 only)

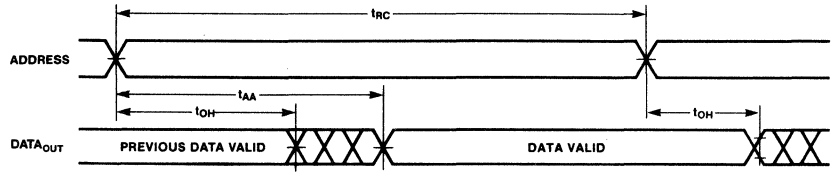
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

SYMBOL	PARAMETER	IDT7132S/L55[2] IDT7142S/L55[2]		IDT7132S/L70 IDT7142S/L70		IDT7132S/L90 IDT7142S/L90		IDT7132S/L100 IDT7142S/L100		IDT7132S/L120[3] IDT7142S/L120[3]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	70	—	90	—	100	—	120	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	90	—	100	—	120	ns
t_{ACE}	Chip Enable Access Time	—	55	—	70	—	90	—	100	—	120	ns
t_{AOE}	Output Enable Access Time	—	35	—	40	—	40	—	40	—	60	ns
t_{OH}	Output Hold From Address Change	0	—	0	—	10	—	10	—	10	—	ns
t_{LZ}	Output Low Z Time[1,4]	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
t_{PU}	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time[10]	55	—	70	—	90	—	100	—	120	—	ns
t_{EW}	Chip Enable to End of Write	40	—	50	—	85	—	90	—	100	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	85	—	90	—	100	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	55	—	55	—	65	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	30	—	40	—	40	—	40	—	ns
t_{HZ}	Output High Z Time[1,4]	—	30	—	35	—	40	—	40	—	40	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enabled to Output in High Z[1,4]	—	30	—	35	0	40	0	40	0	50	ns
t_{OW}	Output Active From End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns
BUSY TIMING												
t_{WB}	Write to $\overline{BUSY}$[5,8]	-10	—	-10	—	-10	—	-10	—	-10	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[9]	20	—	20	—	20	—	20	—	20	—	ns
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	45	—	50	—	60	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	40	—	40	—	45	—	50	—	60	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	35	—	35	—	45	—	50	—	60	ns
t_{BDC}	$\overline{BUSY}$ Disable time to Chip Enable	—	30	—	30	—	45	—	50	—	60	ns
t_{WDD}	Write Pulse to Data Delay[6]	—	80	—	90	—	100	—	120	—	140	ns
t_{DDD}	Write Data Valid to Read Data Delay[6]	—	55	—	70	—	90	—	100	—	120	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[7]	—	Note 7	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns
t_{APS}	Arbitration Priority Set Up Time	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

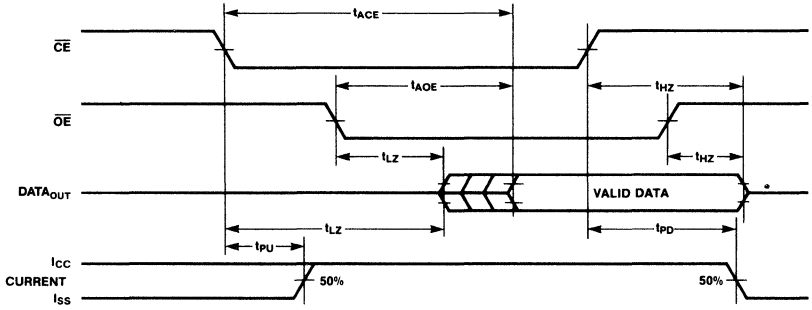
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 & 3).
2. Available over 0°C to +70°C temperature range only.
3. Available over -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For Slave part (IDT7142) only.
6. Port to port delay through RAM cells from writing port to reading port.
7. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
8. To ensure that the write cycle is inhibited during contention.
9. To ensure that a write cycle is completed after contention.
10. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$.

TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE(1,2,6)



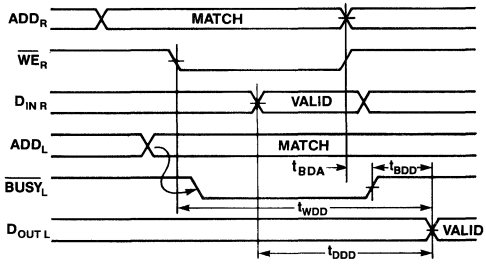
SRD7130-008

TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE(1,3)

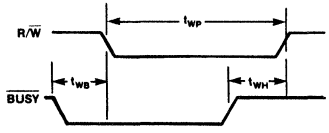


SRD7130-009

TIMING WAVEFORM OF READ WITH BUSY

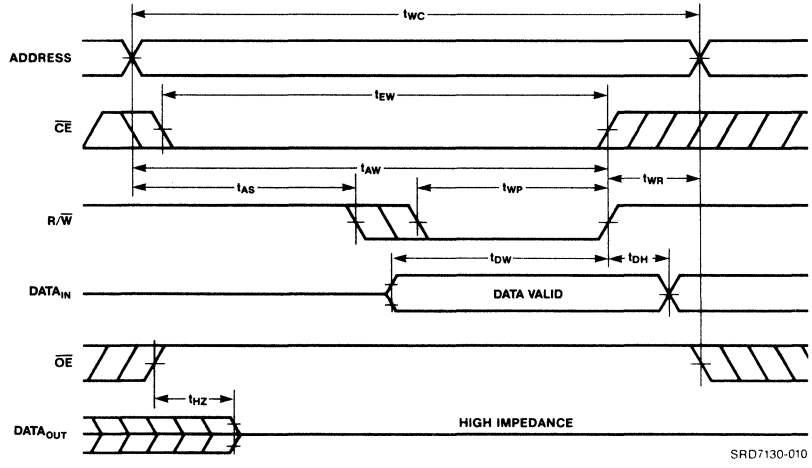


TIMING WAVEFORM OF WRITE WITH BUSY



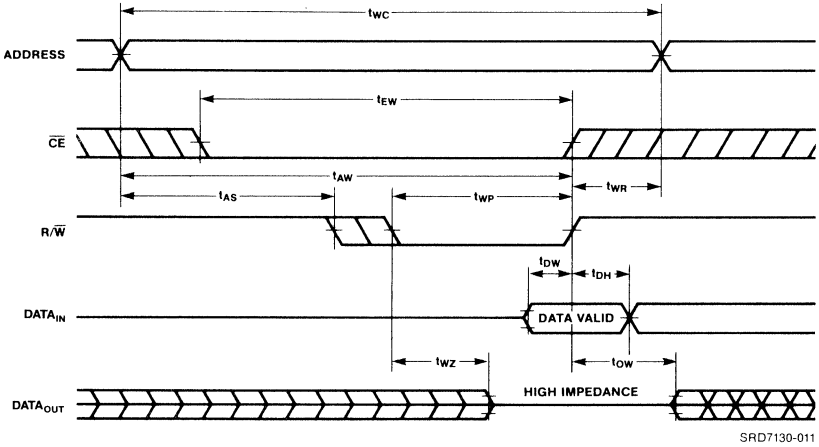
SRD7130-024

TIMING WAVEFORM OF WRITE CYCLE NO. 1 EITHER SIDE(4,7)



SRD7130-010

TIMING WAVEFORM OF WRITE CYCLE NO. 2 EITHER SIDE[4,7]

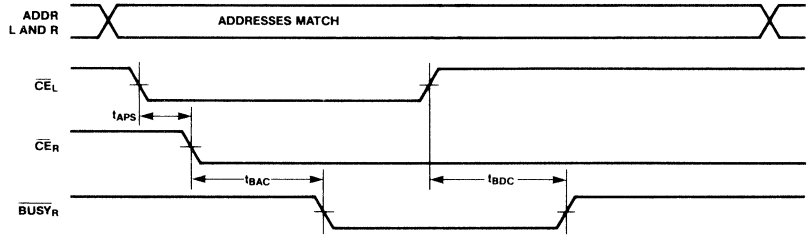


SRD7130-011

2

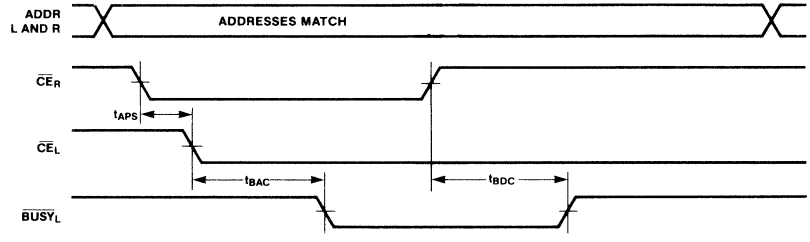
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



SRD7130-013

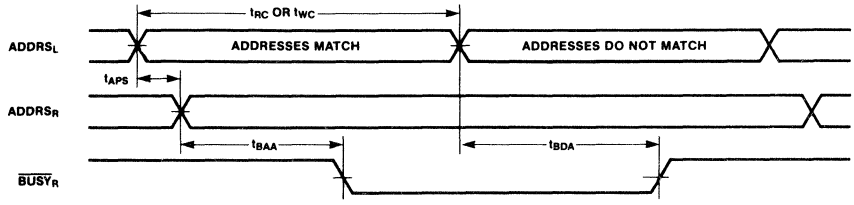
$\overline{CE}_R$ VALID FIRST



SRD7130-012

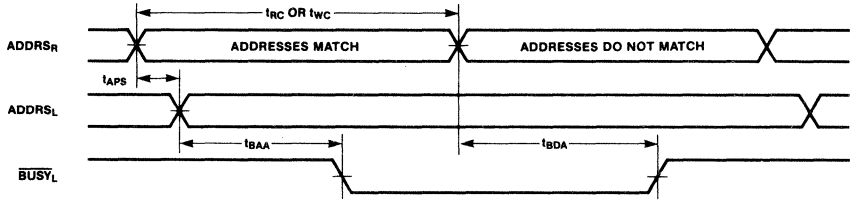
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION[5]

LEFT ADDRESS VALID FIRST:



SRD7130-014

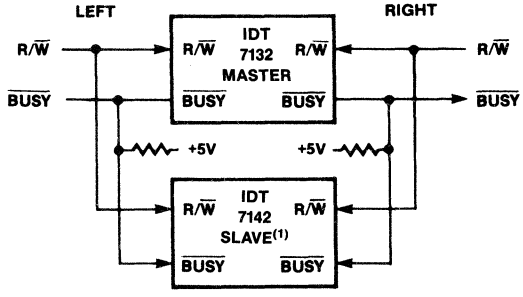
RIGHT ADDRESS VALID FIRST:



SRD7130-015

NOTES:
1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during address transition.

16-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEM



SRD7130-025

NOTE:
1. No arbitration in IDT7142 (SLAVE). $\overline{BUSY}$-IN inhibits write in IDT7142 (SLAVE).

FUNCTIONAL DESCRIPTION:

The IDT7132/42 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table II). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its L $\overline{BUSY}$ while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

2

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL

LEFT OR RIGHT PORT[1]				FUNCTION
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB1} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs
—	—	—	—	Data in Memory Output on Right Port

NOTES:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.

H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:

1. This parameter is sampled and not 100% tested.

TABLE II — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS[1]		FUNCTION
$\overline{CE}_L$	A_{0L}-A_{10L}	$\overline{CE}_R$	A_{0R}-A_{10R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{10R}	L	$\neq A_{0L}$-A_{10L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	LV5R	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL5R	$= A_{0R} - A_{10R}$	LL5R	$= A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	$= A_{0R} - A_{10R}$	RL5L	$= A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	$= A_{0R} - A_{10R}$	LW5R	$= A_{0L} - A_{10L}$	L	H	Arbitration Resolved

NOTE:

1. INT Flags Don't Care
   X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$=LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$=LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and Right $\overline{CE}$=LOW within 5ns of each other.

Integrated Device Technology, Inc

CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH SEMAPHORE

ADVANCE INFORMATION
IDT71322S
IDT71322L

FEATURES:

- High-speed access
  - —Military: 55/70/90/100ns (max.)
  - —Commercial: 45/55/70/90ns (max.)
- Low-power operation
  - —IDT71322S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT71322L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation — 2V data retention
- TTL compatible, single 5V ± 10% power supply
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71322 is an extremely high-speed 2K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

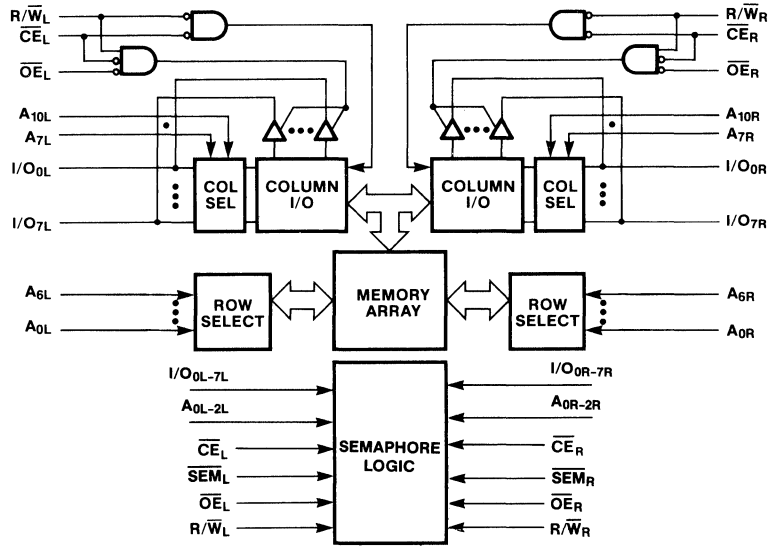
the IDT71322 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. An automatic power down feature controlled by $\overline{CE}$ and $\overline{SEM}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 325mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT71322 is packaged in either a 48-pin sidebraze or plastic DIP or 52-pin LCC, with the military devices available 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

2

FUNCTIONAL BLOCK DIAGRAM



SRD71322-001

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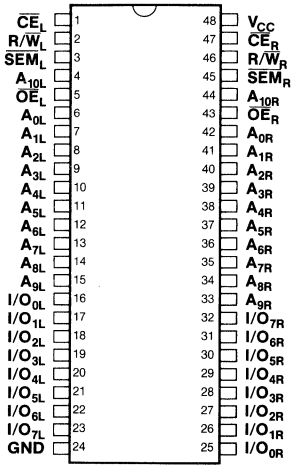
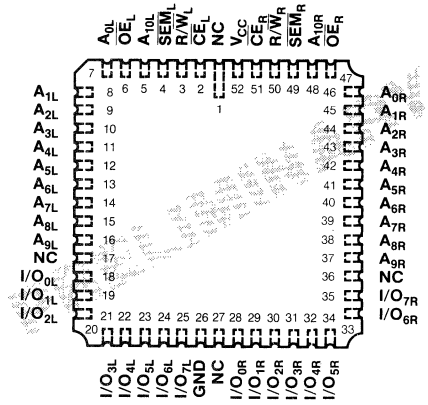
PIN CONFIGURATIONS



SRD71322-002

DIP
TOP VIEW



LCC
TOP VIEW

Integrated Device Technology Inc

CMOS DUAL-PORT RAM 32K (2K x 16-BIT)

ADVANCE INFORMATION
IDT7133S/L
IDT7143S/L

FEATURES:

- High-speed access
  - —Military: 90/100/120ns (max.)
  - —Commercial: 70/90/100ns (max.)
- Low-power operation
  - —IDT7133/43S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT7133/43L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32-or-more bits using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation — 2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, DIP (600 mil, 70 mil centers), LCC
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7133/IDT7143 are high-speed 2K x 16 dual-port static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT7143 "SLAVE" dual-port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

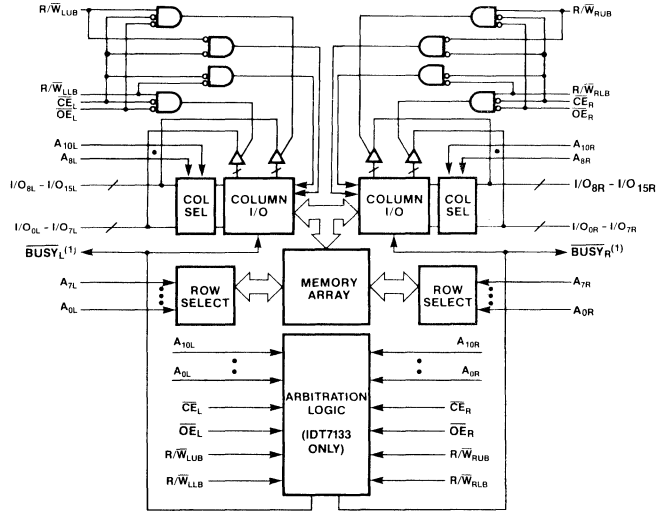
Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 325mW of power at maximum access times as fast as 70ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

Both the IDT7133/7143 2K x 16 devices have identical pinouts. Each are packaged in either a 68-pin PGA, sidebraze or plastic DIP or LCC, with the military devices available 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

2

FUNCTIONAL BLOCK DIAGRAM



SRD7133-002

NOTE:

1. IDT7133 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7143 (SLAVE): $\overline{BUSY}$ is input.
2. LB = LOWER BYTE
   UB = UPPER BYTE

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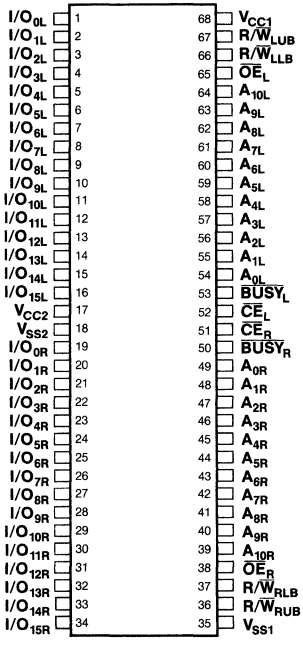
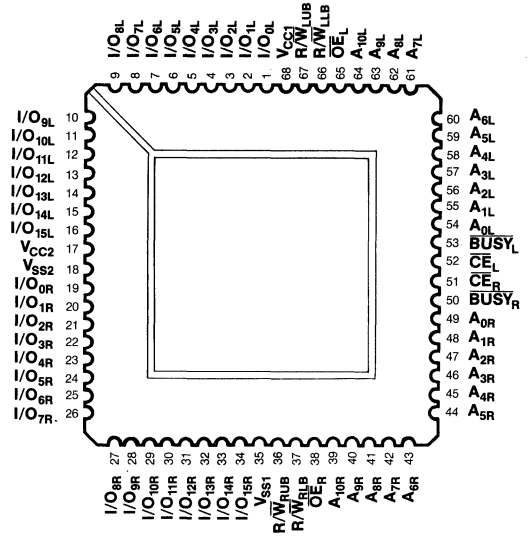
PIN CONFIGURATIONS



SRD7133-003

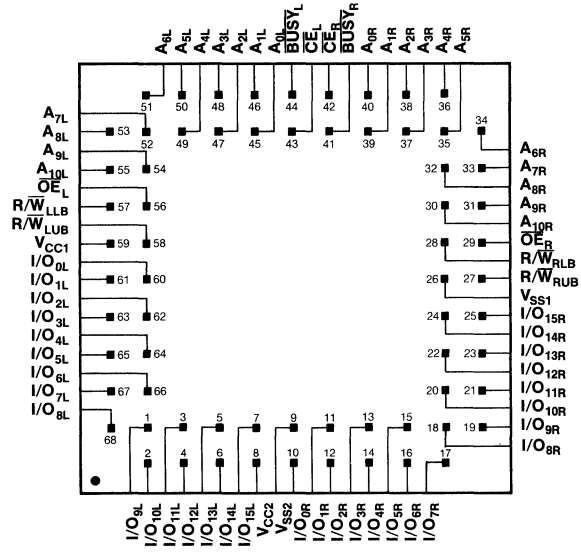
DIP
TOP VIEW

UB = UPPER BYTE
LB = LOWER BYTE



LCC
TOP VIEW

SRD7133-004



PGA
TOP VIEW

SRD7133-005

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

ADVANCE INFORMATION
IDT7134S
IDT7134L

FEATURES:

- High-speed access
  - —Military: 55/70/90/100ns (max.)
  - —Commercial: 45/55/70/90ns (max.)
- Low-power operation
  - —IDT7134S
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT7134L
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation — 2V data retention
- TTL compatible, single +5V (±10%) power supply
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7134 is an extremely high-speed 4K x 8 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed.

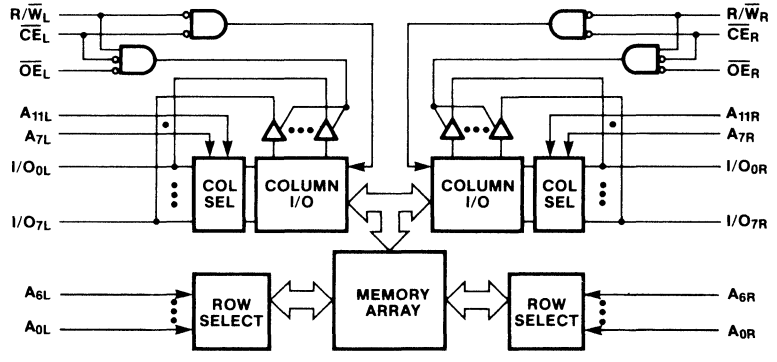
The IDT7134 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these dual ports typically operate on only 325mW of power at maximum access times as fast as 45ns. Low power (L) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT7134 is packaged in either a 48-pin sidebraze or plastic DIP or LCC, with the military devices available 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

2

FUNCTIONAL BLOCK DIAGRAM



SDR7134-001

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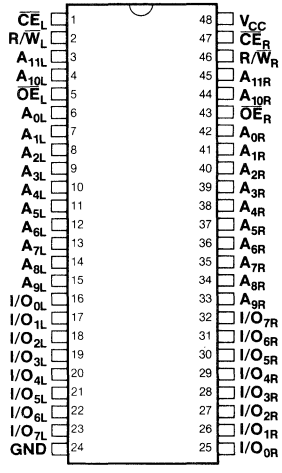
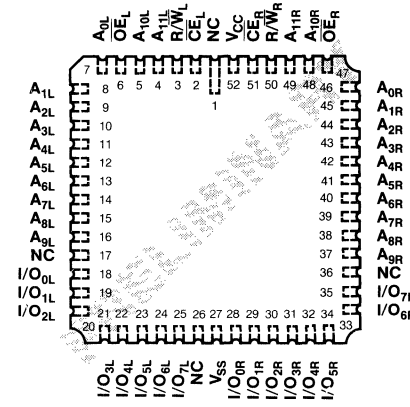
PIN CONFIGURATIONS



DIP
TOP VIEW

SDR7134-002



SDR7134-003

LCC
TOP VIEW

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

ADVANCE INFORMATION
IDT71341S
IDT71341L

FEATURES:

- High-speed access
  - —Military: 55/70/90/100ns (max.)
  - —Commercial: 45/55/70/90ns (max.)
- Low-power operation
  - —IDT71341S
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - —IDT71341L
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation — 2V data retention
- TTL compatible, single 5V (±10%) power supply
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71341 is an extremely high-speed 4K x 8 dual-port static RAM with full on-chip hardware support of semaphore signalling between the two ports.

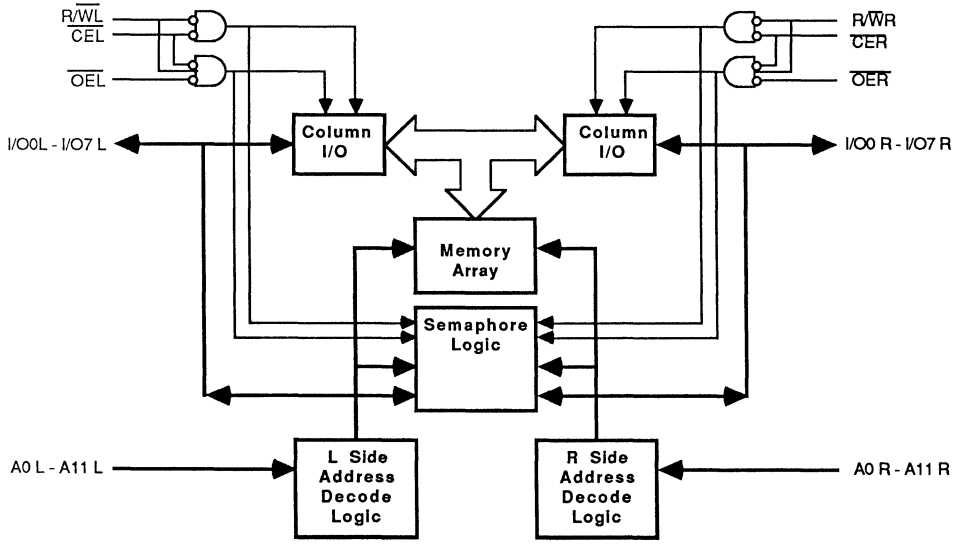
The IDT71341 provides two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

Fabricated using IDT's CEMOS™ high-performance technology, this device typically operates on only 325mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200μW from a 2V battery.

The IDT71341 military devices are available 100% processed in compliance to the test methods of MIL-STD-883, Class B, Method 5004.

2

FUNCTIONAL BLOCK DIAGRAM



SRD71341-001

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CMOS STATIC RAMS 64K (8K x 8-BIT)

IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
  Military — 35/45/55/70/85/100/120/150/200ns (max.)
  Commercial — 30/35/45/55/70ns (max.)
- Low-power operation
  —IDT7164S
  Active: 300mW (typ.)
  Standby: 100μW (typ.)
  —IDT7164L
  Active: 250mW (typ.)
  Standby: 30μW (typ.)
- Battery Backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 mil), 28-pin THINDIP (400 mil) and 32-pin LCC
- Pin compatible with standard 64K static RAM and EPROM
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology.

Address access times as fast as 30ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When $\overline{CS_1}$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low power standby mode. In the full standby mode, the low power device consumes less than 30μW typically. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW operating off a 2V battery.

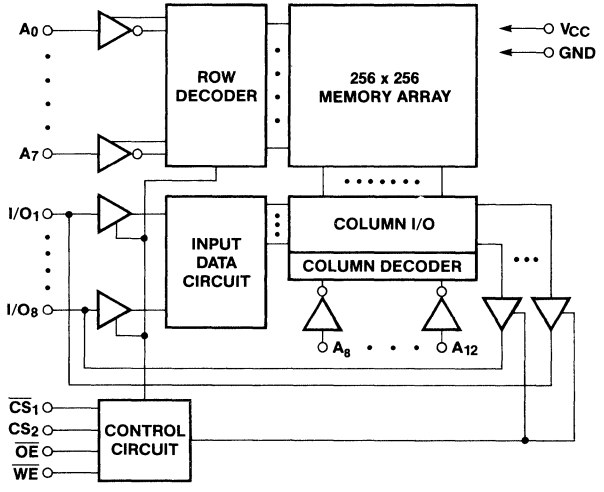
All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in either a 28-pin, 400 mil THINDIP; a 28-pin, 600 mil DIP or 32-pin leadless chip carrier, providing high board-level packing densities.

The IDT7164 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

2

FUNCTIONAL BLOCK DIAGRAM



SRD7164-001

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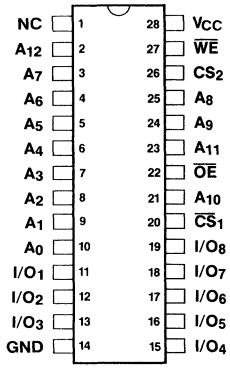
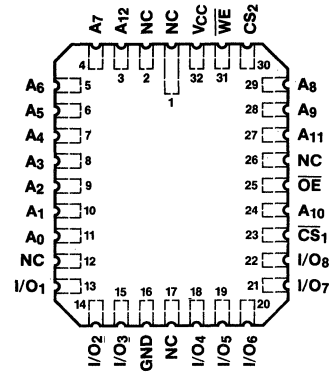
PIN CONFIGURATIONS



SDR7164-002

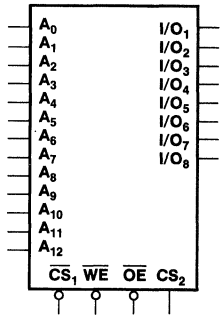
DIP
TOP VIEW



SDR7164-003

LCC
TOP VIEW

LOGIC SYMBOL



SDR7164-004

PIN NAMES

A_0–A_{12}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1–I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}_1$	CHIP SELECT	GND	GROUND
CS_2	CHIP SELECT	V_{CC}	POWER

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7164S MIN.	IDT7164S TYP.(1)	IDT7164S MAX.	IDT7164L MIN.	IDT7164L TYP.(1)	IDT7164L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	30ns COM'L.	30ns MIL.	35ns COM'L.	35ns MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	70ns COM'L.	70ns MIL.	85ns(2) COM'L.	85ns(2) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, Output Open, CS_2 = V_{IH} V_{CC} = Max., f = 0	S	90	—	90	100	90	100	90	100	90	100	—	100	mA
		L	80	—	80	90	80	90	80	90	80	90	—	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, Output Open, CS_2 = V_{IH} V_{CC} = Max., f = f Max.	S	160	—	150	160	150	160	150	160	150	160	—	160	mA
		L	140	—	130	140	120	130	115	125	110	120	—	120	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$ V_{CC} = Max., Output Open	S	20	—	20	20	20	20	20	20	20	20	—	20	mA
		L	3	—	3	5	3	5	3	5	3	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) 1. $\overline{CS_1} \geq V_{HC}$ and $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$, V_{CC} = Max.	S	15	—	15	20	15	20	15	20	15	20	—	20	mA
		L	0.2	—	0.2	1.0	0.2	1.0	0.2	1.0	0.2	1.0	—	1.0	

NOTES:
1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

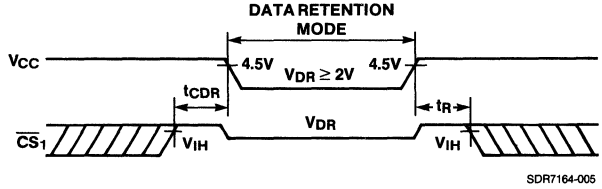
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	1. $\overline{CS_1} \geq V_{HC}$, & $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$	MIL.	—	10	15	200	300	µA
			COM'L.	—	10	15	60	90	
t_{CDR}	Chip Deselect to Data Retention Time			0	—		—		ns
t_R	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1 and 2

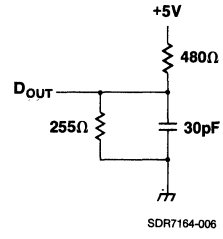


Figure 1. Output Load

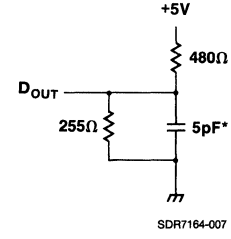


Figure 2. Output Load (for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW}, t_{WHZ})

***Including scope and jig**

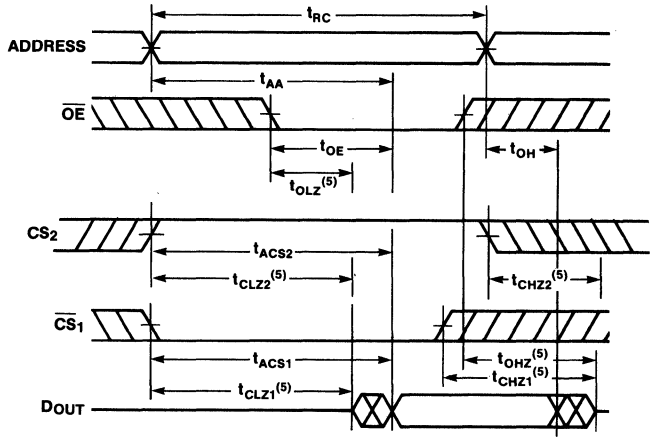
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	7164S30[1,7] 7164L30[1,7] MIN.	MAX.	7164S35[5] 7164L35[5] MIN.	MAX.	7164S45 7164L45 MIN.	MAX.	7164S55 7164L55 MIN.	MAX.	7164S70 7164L70 MIN.	MAX.	7164S85[2] 7164L85[2] MIN.	MAX.	UNITS
READ CYCLE														
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1,2 Access Time[3]	—	35[7]	—	40[5]	—	45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$	Chip Select-1,2 to Output in Low Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	20	—	25	—	30	—	35	—	40	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
$t_{CHZ1,2}$	Chip Select-1,2 to Output in High Z[4]	—	15	—	15	—	20	—	25	—	30	—	35	ns
t_{OHZ}	Chip Select-1,2 to Output in High Z[4]	—	15	—	15	—	20	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time[4]	—	30	—	35	—	45	—	55	—	70	—	85	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	30	—	35	—	45	—	55	—	70	—	85	—	ns
$t_{CW1,2}$	Chip Select to End of Write	25	—	30	—	40	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	50	—	60	—	75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write Enable to Output High Z[4]	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold from Write Time[6]	3/5	—	3/5	—	3/5	—	3/5	—	3/5	—	3/5	—	ns
t_{OW}	Output Active from End of Write[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

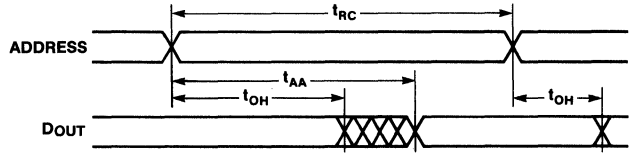
1. 0°C to 70°C product only.
2. -55°C to +125°C product only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter guaranteed but not tested.
5. t_{ACS1} = 35ns, t_{ACS2} = 40ns.
6. With respect to $\overline{CS_1}$ = 30ns, CS_2 = 5ns.
7. t_{ACS1} = 30ns, t_{ACS2} = 35ns.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



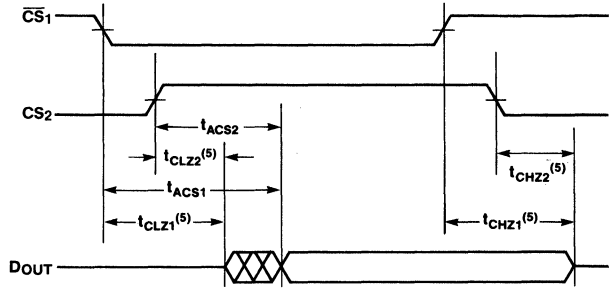
SDR7164-008

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SDR7164-009

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

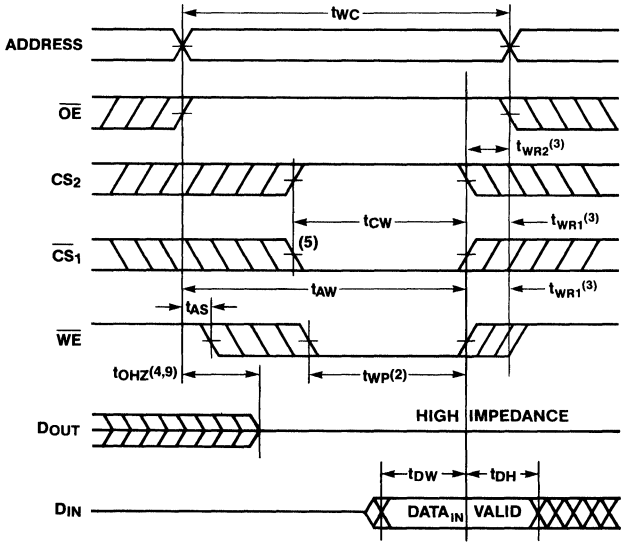


SDR7164-010

NOTES:

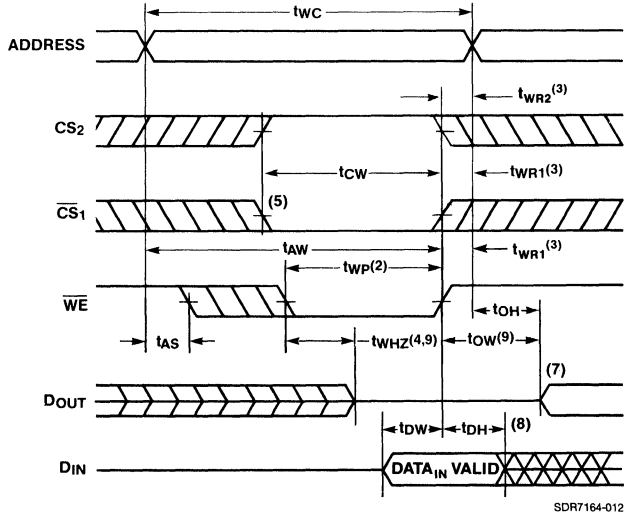
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



SDR7164-011

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



SDR7164-012

NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTES:
1. This parameter is sampled and not 100% tested.

TRUTH TABLE (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O	MODE
X	H	X	X	HIGH Z	Standby (I_{SB})
X	X	L	X	HIGH Z	Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	HIGH Z	Standby (I_{SB1})
X	X	V_{LC}	X	HIGH Z	Standby (I_{SB1})
H	L	H	H	HIGH Z	Output disable
H	L	H	L	D_{OUT}	Read
L	L	H	X	D_{IN}	Write

NOTE:
1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2.

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (8K x 8-BIT) RESETTABLE RAM

PRELIMINARY
IDT7165S
IDT7165L

FEATURES:

- High-speed address access time
  - —Military: 35/45/55ns (max.)
  - —Commercial: 30/35/45/55ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
  - —Military: 20/25/30/35ns (max.)
  - —Commercial: 15/20/25/30ns (max.)
- Low-power operation
  - —IDT7165S
    Active: 300mW (typ.)
    Standby: 100μW (typ.)
  - —IDT7165L
    Active: 250mW (typ.)
    Standby: 30μW (typ.)
- Battery backup operation — 2V data retention voltage (IDT7165L only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 and 400 mil) and 32-pin LCC
- Asynchronous clear on Pin 1
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION

The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. It also provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset.

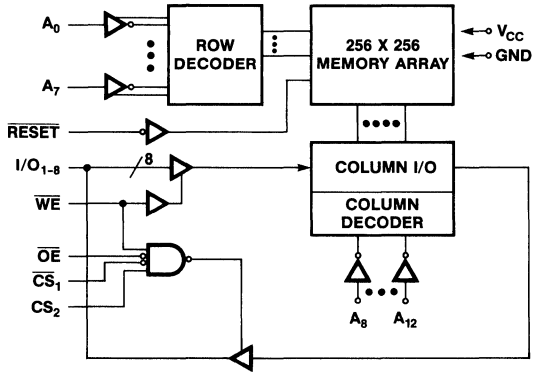
This product is fabricated using IDT's high-performance, high-reliability CEMOS™ technology. Address access time of 30ns and chip select ($\overline{CS}_1$) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When CS_2 goes low, the circuit will automatically go to and remain in low-power standby mode. In the full standby mode, the low-power device consumes less than 30μW typically. The low-power (L) version offers a battery backup data retention capability where the circuit typically consumes only 10μW operating off a 2V battery.

All inputs and outputs of the IDT7165 are TTL-compatible and the device operates from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used so no clocks or refreshing for operation is required.

The IDT7165 is packaged in a 28-pin 600 mil or 400 mil DIP or 32-pin leadless chip carrier, providing high board level densities.

This resettable military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004 making it ideally suited to the military temperature applications demanding the highest level of performance and reliability.

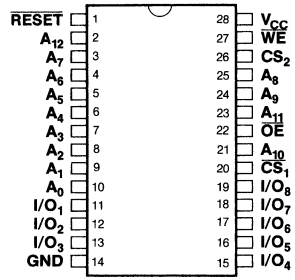
2



SRD7165-001

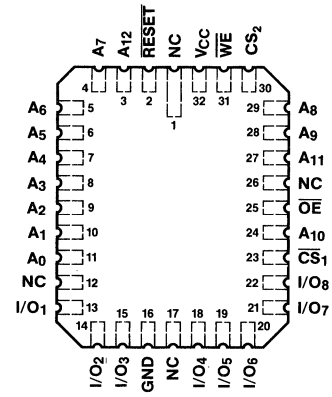
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW

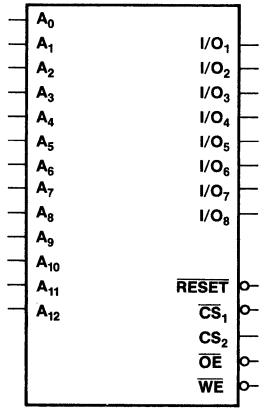
SRD7165-002



LCC
TOP VIEW

SRD7165-003

LOGIC SYMBOL



SRD7165-004

PIN NAMES

A_{0-12}	Address	$\overline{WE}$	Write Enable
I/O_{1-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS_1}$, CS_2	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7165S MIN.	IDT7165S TYP.(1)	IDT7165S MAX.	IDT7165L MIN.	IDT7165L TYP.(1)	IDT7165L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	30ns COM'L.	30ns MIL.	35ns COM'L.	35ns MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	UNIT
I_{CC1}(2)	Operating Power Supply Current Output Open, V_{CC} = Max., f = 0	S	90	—	90	100	90	100	90	100	mA
		L	80	—	80	90	80	90	80	90	
I_{CC2}(2)	Dynamic Operating Current Output Open, V_{CC} = Max., f = f Max.	S	160	—	150	160	150	160	150	160	mA
		L	140	—	130	140	120	130	115	125	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1} \geq V_{IH}$, $CS_2 \leq V_{IL}$, and $\overline{RESET} \geq V_{IH}$ V_{CC} = Max., Output Open	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $CS_2 \leq V_{LC}$ and $\overline{RESET} \geq V_{HC}$, V_{CC} = Max.	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

NOTES:
1. All values are maximum guaranteed values.
2. CS_2 = V_{IH}

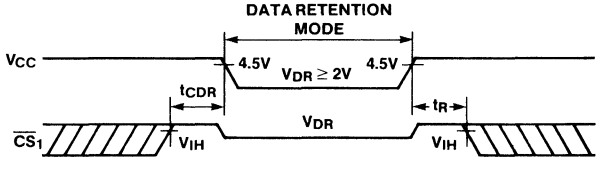
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$CS_2 \leq V_{LC}$ and $\overline{RESET} \geq V_{HC}$	MIL.	—	10	15	200	300	µA
			COM'L.	—	10	15	60	90	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



SRD7165-005

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1 and 2

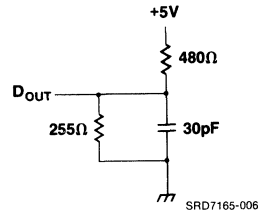


Figure 1. Output Load

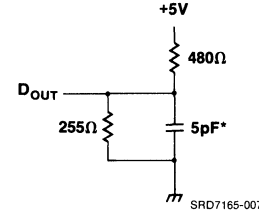


Figure 2. Output Load (for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

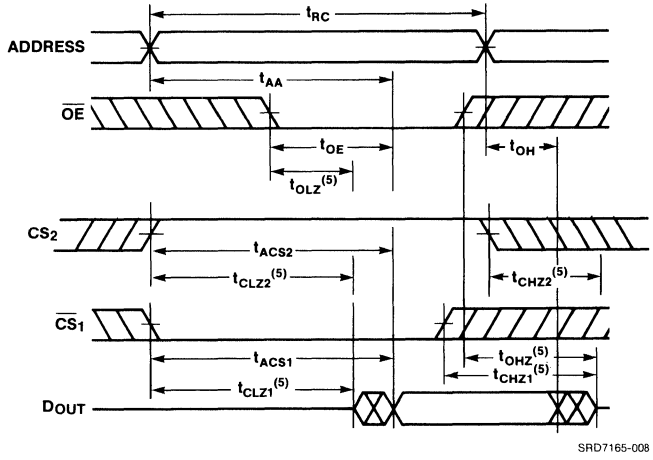
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7165S30[1] IDT7165L30[1] MIN.	MAX.	IDT7165S35[5] IDT7165L35[5] MIN.	MAX.	IDT7165S45 IDT7165L45 MIN.	MAX.	IDT7165S55 IDT7165L55 MIN.	MAX.	UNITS
READ CYCLE										
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	ns
t_{ACS1}	Chip Select-1 Access Time[2]	—	15	—	20	—	25	—	30	ns
t_{ACS2}	Chip Select-2 Access Time[2]	—	35	—	40	—	45	—	55	ns
t_{CLZ1}	Chip Select-1 to Output in Low Z[3]	0	—	0	—	0	—	0	—	ns
t_{CLZ2}	Chip Select-2 to Output in Low Z[3]	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	20	—	25	—	30	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	0	—	0	—	0	—	0	—	ns
t_{CHZ1}	Chip Select-1 to Output in High Z[3]	—	15	—	15	—	20	—	25	ns
t_{CHZ2}	Chip Select-2 to Output in High Z[3]	—	15	—	15	—	20	—	25	ns
t_{OHZ}	Output Disable to Output in High Z[3]	—	15	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	30	—	35	—	45	—	55	—	ns
t_{CW1}	Chip Select-1 to End of Write	20	—	20	—	25	—	30	—	ns
t_{CW2}	Chip Select-2 to End of Write	25	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	25	—	30	—	40	—	50	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	40	—	50	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write Enable to Output in High Z[3]	—	12	—	15	—	20	—	25	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t_{DH1}	Data Hold From Write Time ($\overline{CS_1}$)	3	—	3	—	3	—	3	—	ns
t_{DH2}	Data Hold From Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	ns
RESET[4]										
t_{RSPW}	Reset Pulse Width	55	—	65	—	80	—	100	—	ns
t_{RSR}	Reset High to $\overline{WE}$ Low	5	—	5	—	10	—	10	—	ns

NOTES:

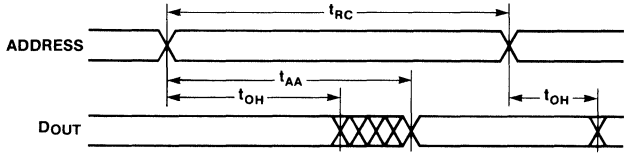
1. 0°C to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. This parameter guaranteed but not tested.
4. Maximum 10% duty cycle applies.
5. Data is preliminary for military devices only.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



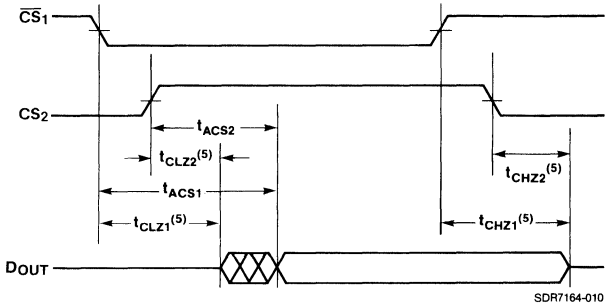
SRD7165-008

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



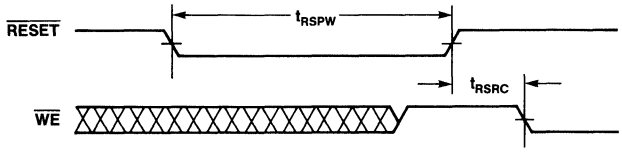
SRD7165-009

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SDR7164-010

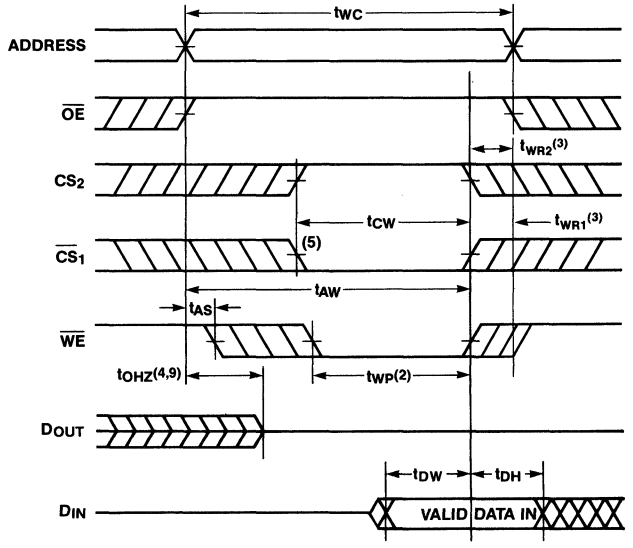
RESET TIMING



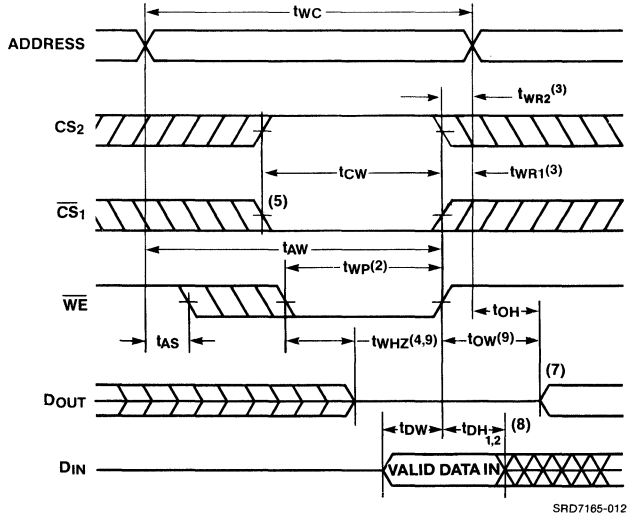
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1} = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTES:
1. This parameter is sampled and not 100% tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{RESET}$	I/O	FUNCTION
X	X	X	X	L	—	Resets all bits to low
X	H	X	X	H	Z	Deselect chip
X	X	L	X	H	Z	Deselect power down
X	V_{HC}	X	X	H	Z	Deselect chip
X	X	V_{LC}	X	V_{HC}	Z	CMOS deselect power down
H	L	H	H	H	Z	Output disable
H L	L L	H H	L X	H H	D_{OUT} D_{IN}	Read Write

NOTE:
1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2.

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4-BIT) SEPARATE DATA INPUTS AND OUTPUTS

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high impedance outputs during write mode
- High-speed (equal access and cycle time)
  - —Military — 25/35/45/55/70/85/100ns (max.)
  - —Commercial — 20/25/35/45/55ns (max.)
- Low-power consumption
  - —IDT71681/2SA
    Active: 225mW (typ.)
    Standby: 100μW (typ.)
  - —IDT71681/2LA
    Active: 225mW (typ.)
    Standby: 10μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density 24-pin 300-mil DIPs and 28-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories

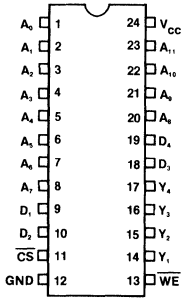
Access times as fast as 20ns are available with maximum power consumption of only 550mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains high. In the ultra low power standby mode (I_{SB1}), the devices consume less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

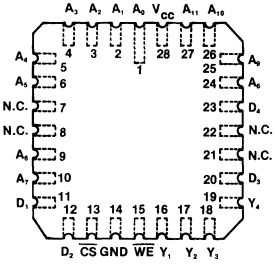
The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300 mil DIPs or 28-pin leadless chip carriers, providing high board-level packing densities.

The IDT71681/IDT71682 Military RAMs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

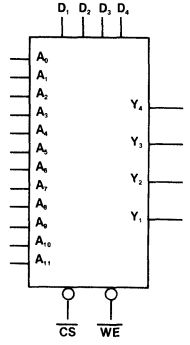


DIP
TOP VIEW

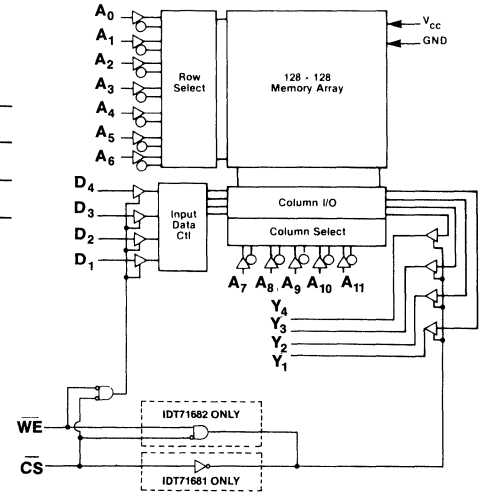


LCC
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	D_1–D_4	DATA IN
$\overline{CS}$	CHIP SELECT	Y_1–Y_4	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71681SA IDT71682SA MIN.	TYP.(1)	MAX.	IDT71681LA IDT71682LA MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	20ns		25ns		35ns		45ns		55ns		70ns(2)		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	SA	90	—	90	100	90	100	90	100	90	100	—	100	mA
		LA	70	—	70	80	70	80	70	80	70	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	SA	120	—	110	120	100	110	100	110	100	110	—	110	mA
		LA	100	—	90	100	80	90	70	80	70	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	SA	45	—	35	45	30	35	30	35	30	35	—	35	mA
		LA	30	—	25	30	20	25	20	25	20	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	SA	20	—	2	10	2	10	2	10	2	10	—	10	mA
		LA	2	—	0.05	0.3	0.05	0.3	0.05	0.3	0.05	0.3	—	0.3	

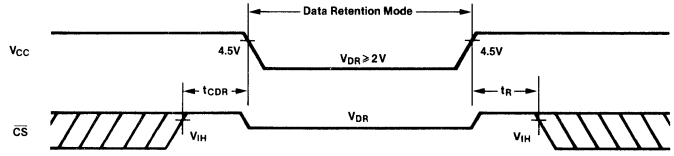
NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices.

DATA RETENTION CHARACTERISTICS (L Version Only)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71681SA/LA - IDT71682SA/LA MIN.	TYP.	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	µA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(6)	Operation Recovery Time			t_{RC}(4)			ns

NOTES:
1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time
5. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

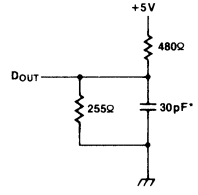


Figure 1. Output Load

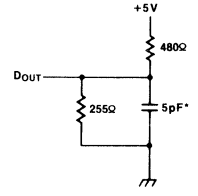


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

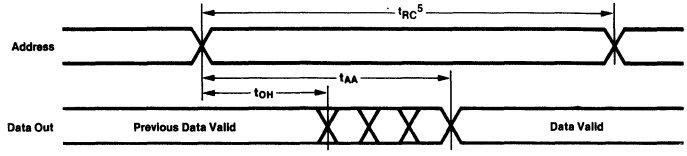
AC ELECTRICAL CHARACTERISTICS[4] (V_{CC} = 5V ± 10%, All Temperature Ranges.)

SYMBOL	PARAMETER	71681X20[1] 71682X20[1] MIN.	MAX.	71681X25[5] 71682X25[5] MIN.	MAX.	71681X35 71682X35 MIN.	MAX.	71681X45 71682X45 MIN.	MAX.	71681X55 71682X55 MIN.	MAX.	71681X70[2] 71682X70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	—	10	—	10	—	15	—	20	—	25	—	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time[3]	—	20	—	25	—	35	—	40	—	50	—	60	ns
t_{RCS}	Read Command Set-Up Time	-5	—	-5	—	-5	—	-5	—	-5	—	-5	—	ns
t_{RCH}	Read Command Hold Time	-5	—	-5	—	-5	—	-5	—	-5	—	-5	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Select to End of Write	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	20	—	20	—	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	20	—	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	13	—	13	—	17	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{IY}	Data Valid to Output Valid (71681 only)[3]	—	20	—	25	—	30	—	35	—	35	—	40	ns
t_{WY}	Write Enable to Output Valid (71681 only)[3]	—	20	—	25	—	30	—	35	—	35	—	40	ns
t_{WZ}	Write Enable to Output in High Z (71682 only)[3]	—	7	—	7	—	13	—	20	—	25	—	30	ns
t_{OW}	Output Active from End of Write (71682 only)[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns

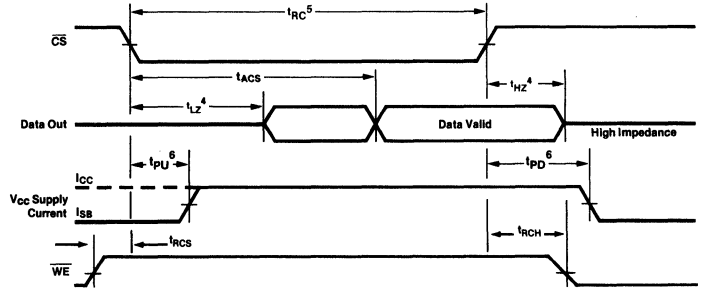
NOTES:

1. 0°C to +70°C temperature range and standard power only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. X in part numbers represents SA or LA.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)

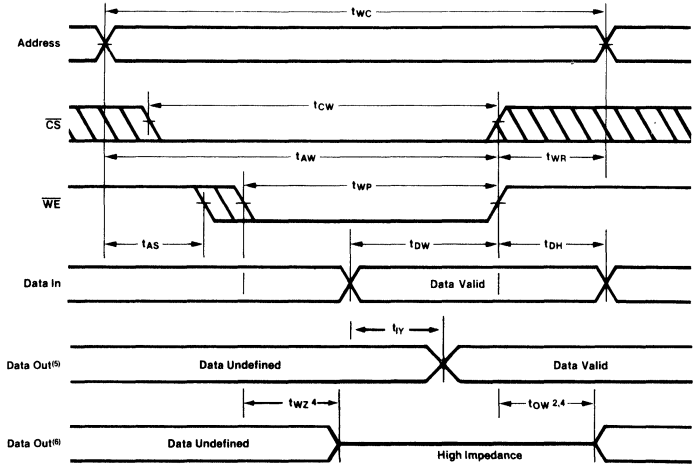


TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)

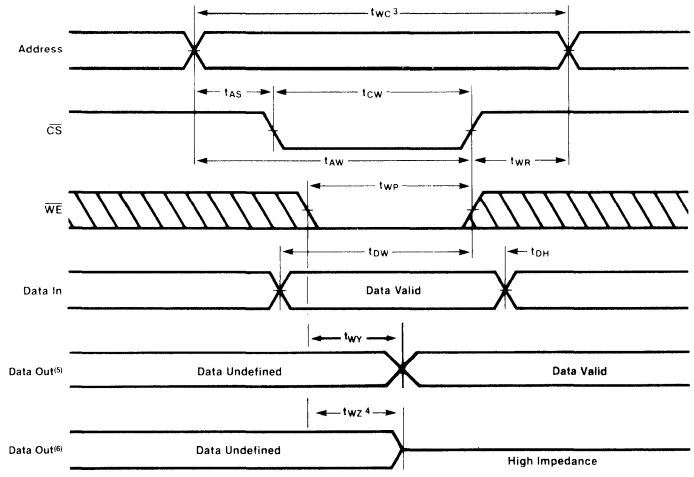


NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. For IDT71681 only.
6. For IDT71682 only.

2

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write(1)	L	L	D_{IN}	Active
Write(2)	L	L	High Z	Active

NOTES:
1. For IDT71681 only.
2. For IDT71682 only.

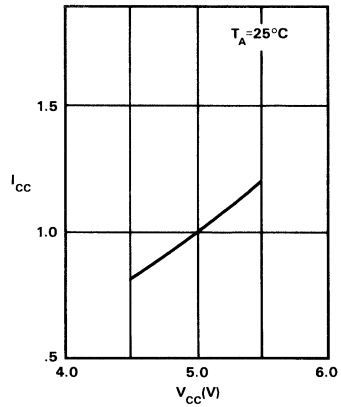
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

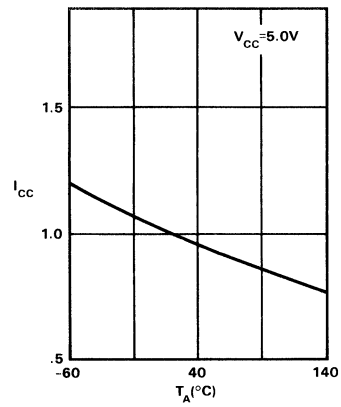
NOTE:
1. This parameter is sampled and not 100% tested.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

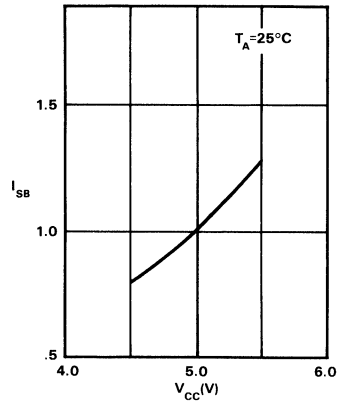
I_{CC} vs. Supply Voltage



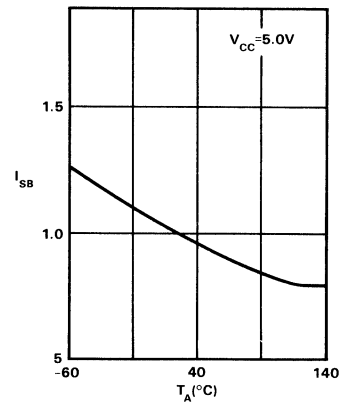
I_{CC} vs. Temperature



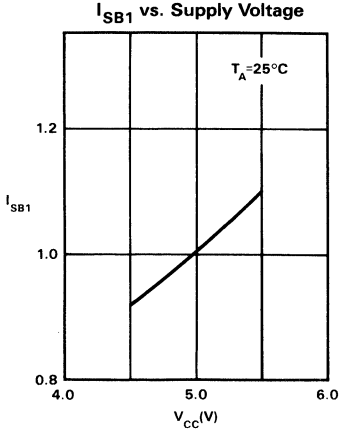
I_{SB} vs. Supply Voltage



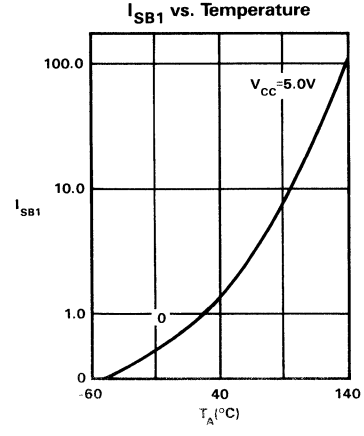
I_{SB} vs. Temperature



I_{SB1} vs. Supply Voltage

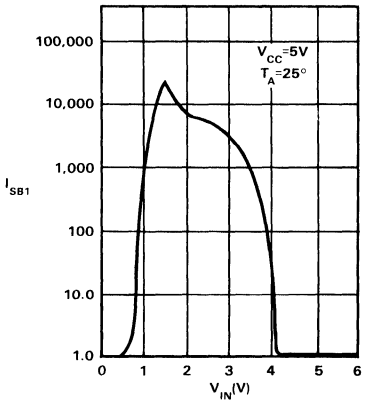


I_{SB1} vs. Temperature

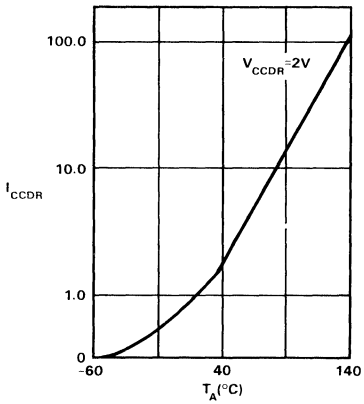


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

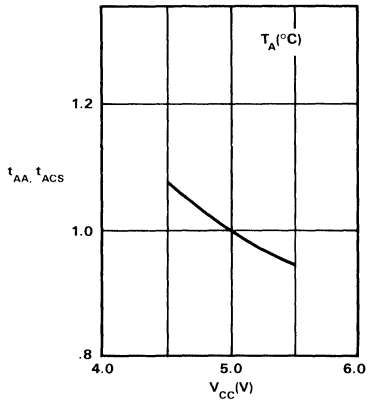
I_{SB1} vs. V_{IN}



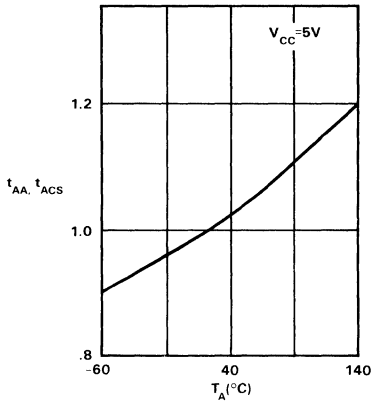
I_{CCDR} vs. Temperature



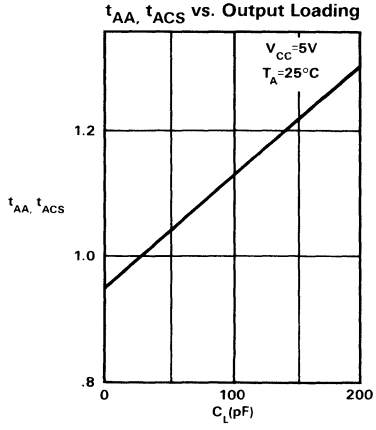
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



2

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (8K x 8-BIT) CACHE-TAG RAM

PRELIMINARY IDT7174S

FEATURES:

- High-speed address/access time
  - —Military: 45/55ns (max.)
  - —Commercial: 35/45ns (max.)
- High-speed chip select access time
  - —Military: 25/30ns (max.)
  - —Commercial: 20/25ns (max.)
- High-speed comparison time
  - —Military: 45/55ns (max.)
  - —Commercial: 37/45ns (max.)
- Low-power operation
  - —IDT7174S
    Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 mil), 28-pin THINDIP (400 mil) and 32-pin LCC
- High-speed asynchronous RAM Clear on Pin 1
  (Reset Cycle Time = 2 x T_{AA})
  (Note: Some duty cycle limitations may apply)
- Match Output on Pin 26
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7174 is a high-speed cache address comparator subsystem consisting of a 65,536 bit static RAM organized as 8K x 8 and an 8-bit comparator. The IDT7174 can also be used as an 8K x 8 high-speed static RAM. A single IDT7174 can provide address comparison for 8K cache words as 21 bits of address organized as 13 word cache address bits and 8 upper address bits. Two IDT7174s can be combined to provide 29 bits of address comparison, etc. The IDT7174 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system reset, a requirement for cache comparator systems.

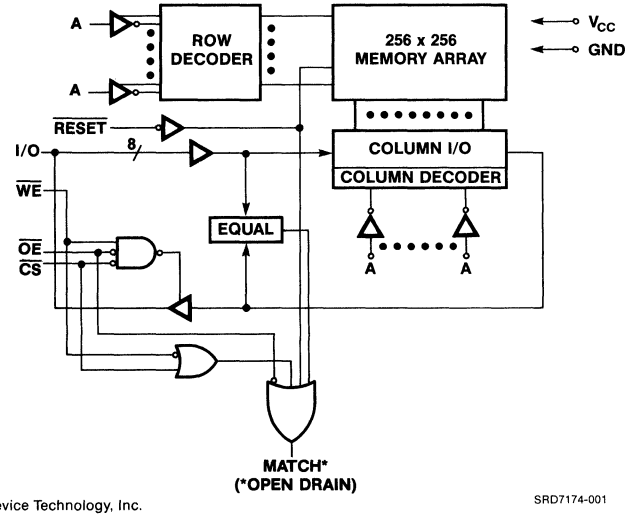
The IDT7174 is fabricated using IDT's high-performance, high-reliability technology — CEMOS. Address access times as fast as 35ns, chip select times of 20ns and comparison times of 37ns are available with maximum power consumption of 825mW.

All inputs and outputs of the IDT7174 are TTL-compatible and the device operates from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7174 is packaged in either a 28-pin, 600 mil DIP; a 28-pin, 400 mil THINDIP, or a 32-pin leadless chip carrier, providing high board level packing densities.

The IDT7174 Military grade Cache Comparator is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

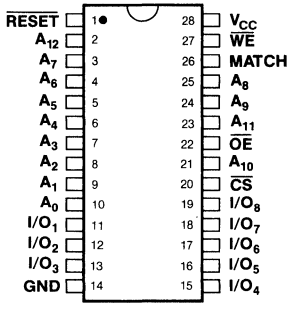
FUNCTIONAL BLOCK DIAGRAM



SRD7174-001

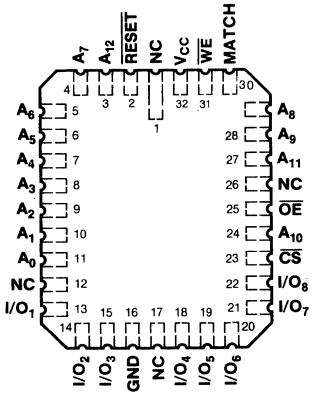
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SRD7174-002

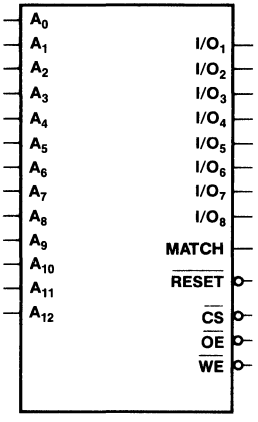
DIP
TOP VIEW



SRD7174-003

LCC
TOP VIEW

LOGIC SYMBOL



SRD7174-004

PIN NAMES

A_{0-12}	Address	$\overline{WE}$	Write Enable
I/O_{1-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power
MATCH	Data/Memory Match (Open Drain)		

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7174S MIN.	IDT7174S TYP.(1)	IDT7174S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	µA
$\|I_{LO}\|$	Output Leakage Current(2)	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	µA
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH	MIL.	—	—	0.5	V
		I_{OL} = 22mA MATCH	COM'L.	—	—	0.5	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min. (Except Match)		2.4	—	—	V

NOTES:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. Data and match.

DC ELECTRICAL CHARACTERISTICS(1,2)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	35ns		45ns		55ns		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current Output Open, V_{CC} = Max., f = 0	S	110	—	110	125	—	125	mA
I_{CC2}	Dynamic Operating Current Output Open, V_{CC} = Max., f = f Max.	S	150	—	140	150	—	145	mA

NOTES:

1. All values are maximum guaranteed values.
2. This device has no power down mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1, 2, and 3

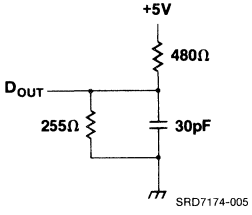


Figure 1. Output Load

***Including scope and jig**

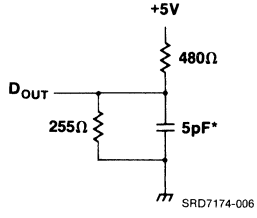
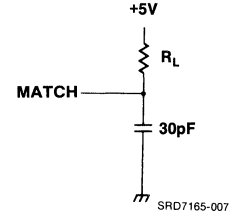


Figure 2. Output Load (for t_{CLZ} t_{OLZ}, t_{CHZ} t_{OHZ}, t_{OW}, t_{WHZ})



R_L = 200Ω (COM'L.)
= 270Ω (MIL.)

Figure 3. Output Load for Match

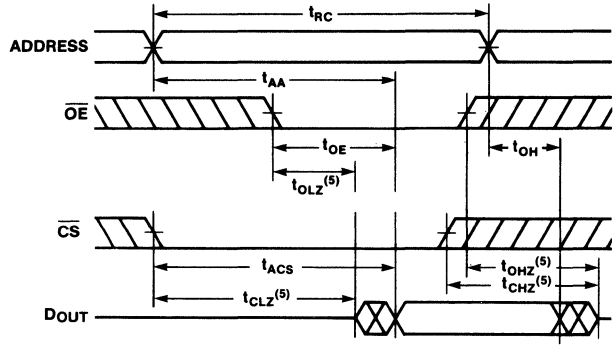
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S35[1] MIN.	IDT7174S35[1] MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55[4] MIN.	IDT7174S55[4] MAX.	UNITS
READ CYCLE								
t_{RC}	Read Cycle Time	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	ns
t_{CLZ}	Chip Select to Output in Low Z	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	—	20	—	25	—	30	ns
t_{OLZ}	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	ns
t_{CHZ}	Chip Select to Output in High Z[2]	—	15	—	20	—	25	ns
t_{OHZ}	Output Disable to Output in High Z[2]	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[2]	—	35	—	45	—	55	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	—	45	—	55	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	ns
t_{AW}	Address Valid to End of Write	30	—	40	—	50	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	40	—	50	—	ns
t_{WR}	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z[2]	—	15	—	20	—	25	ns
t_{DW}	Data to Write Time Overlap	15	—	20	—	25	—	ns
t_{DH}	Data Hold From Write Time	2	—	2	—	2	—	ns
t_{OW}	Output Active from End of Write[2]	5	—	5	—	5	—	ns
MATCH								
t_{ADM}	Addresss to Match Valid	—	37	—	45	—	55	ns
t_{CSM}	Chip Select to Match Valid	—	20	—	25	—	30	ns
t_{CSMHI}	Chip Deselect to Match High	—	20	—	25	—	30	ns
t_{DAM}	Data Input to Match Valid	—	28	—	35	—	45	ns
t_{OEMHI}	$\overline{OE}$ Low to Match High	—	25	—	35	—	45	ns
t_{OEM}	$\overline{OE}$ High to Match Valid	—	25	—	35	—	45	ns
t_{WEMHI}	$\overline{WE}$ Low to Match High	—	25	—	35	—	45	ns
t_{WEM}	$\overline{WE}$ High to Match Valid	—	25	—	35	—	45	ns
t_{RSMHI}	$\overline{RESET}$ Low to Match High	—	25	—	35	—	45	
t_{MHA}	Match Valid Hold From Address	5	—	5	—	5	—	ns
t_{MHD}	Match Valid Hold From Data	5	—	5	—	5	—	ns
RESET								
t_{RSPW}	$\overline{RESET}$ Pulse Width[3]	65	—	80	—	100	—	ns
t_{RSRC}	$\overline{RESET}$ High to $\overline{WE}$ Low	5	—	10	—	10	—	ns

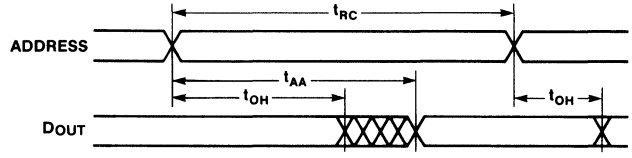
NOTES:

1. 0°C to +70°C temperature range only.
2. This parameter guaranteed but not tested.
3. Recommended duty cycle 10% maximum.
4. -55°C to +125°C temperature range only.

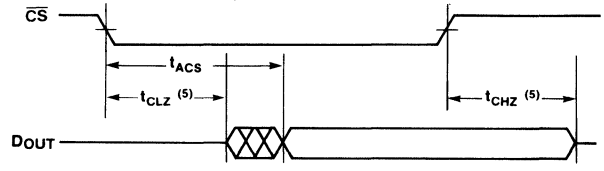
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



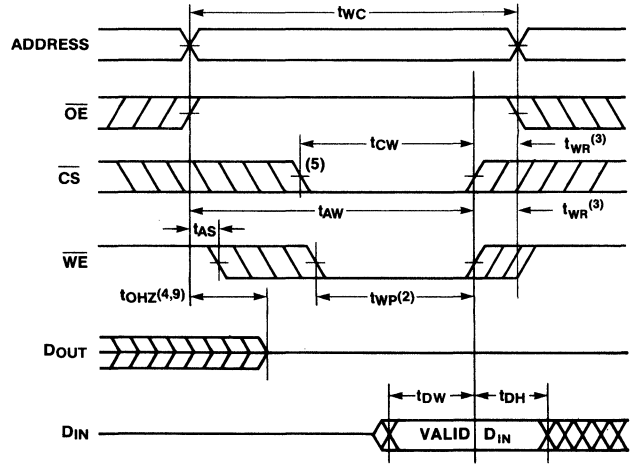
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



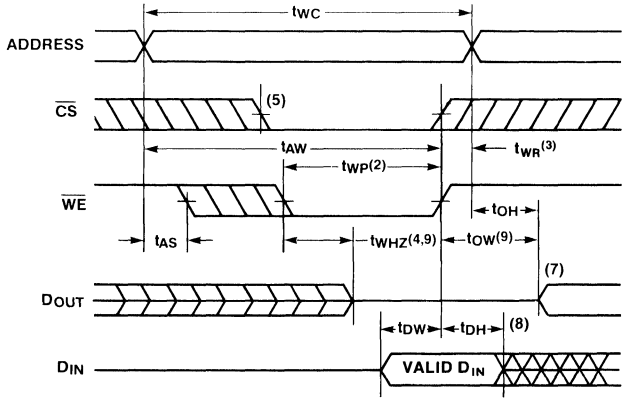
NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

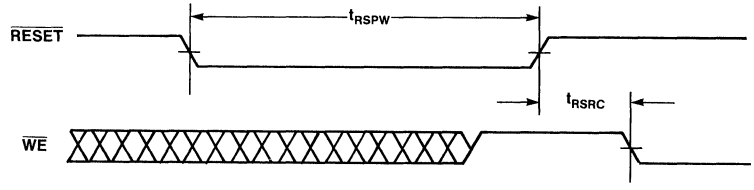
TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



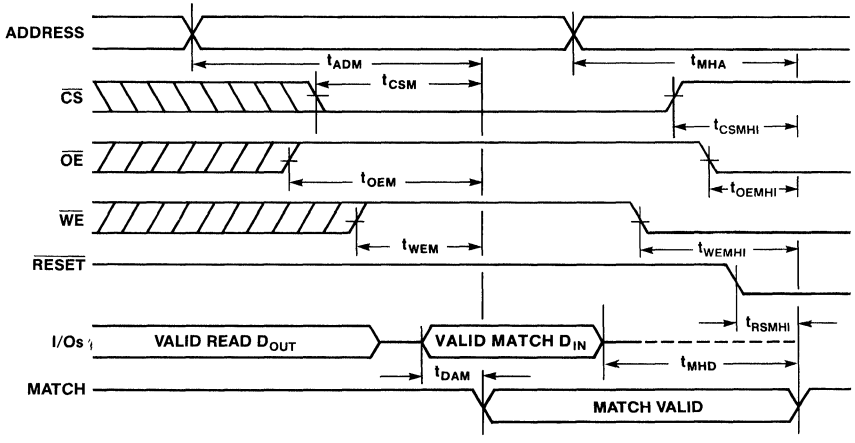
TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



RESET TIMING



MATCH TIMING



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) or a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	$\overline{RESET}$	MATCH	I/O	FUNCTION
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	High Z	Deselect chip
H	L	H	H	L	D_{IN}	No Match
H	L	H	H	H	D_{IN}	Match
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (64K x 1-BIT)

IDT7187S
IDT7187L

FEATURES:

- High-speed (equal access and cycle time)
  - —Military: 25/30/35/45/55/70/85ns (max.)
  - —Commercial: 25/30/35/45/55/70ns (max.)
- Low-power consumption
  - —IDT7187S
    - Active: 300mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT7187L
    - Active: 250mW (typ.)
    - Standby: 30μW (typ.)
- Battery backup operation — 2V data retention (IDT7187L version only)
- JEDEC standard high-density 22-pin DIP, 22-pin plastic DIP, 22-pin and 28-pin leadless chip carrier
- Produced with advanced CEMOS ™ high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7187 is a 64K x 1-bit high-speed static RAM fabricated using IDT's high-performance, high-reliability technology, CEMOS. Access times as fast as 25ns are available with maximum power consumption of 550mW.

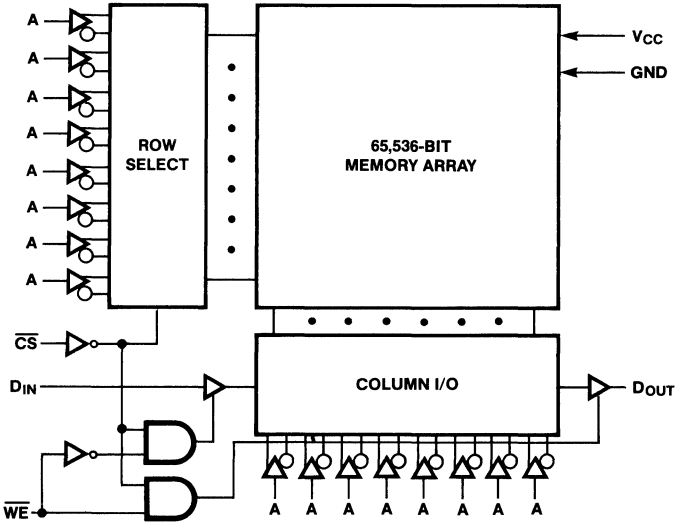
Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes — I_{SB} and I_{SB1}. I_{SB} provides ultra low-power operation (192.5mW max.); I_{SB1} provides low-power operation (5mW max.). The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 20μW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil DIP or 22- and 28-pin leadless chip carriers.

The IDT7187 Military RAM version is 100% processed to the test methods of MIL-STD-883, Class B, Methods 5004 and 5005, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

2

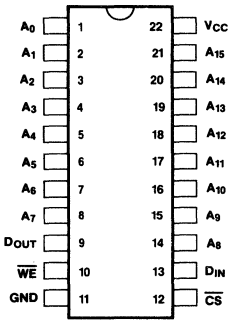
FUNCTIONAL BLOCK DIAGRAM



SRD7187-004

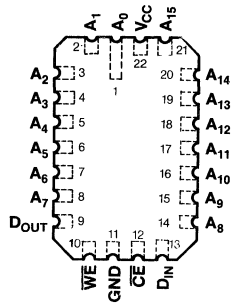
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

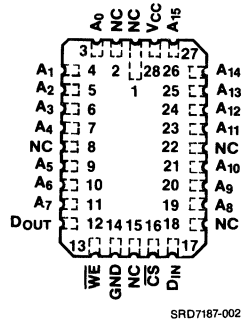


SRD7187-001

DIP
TOP VIEW



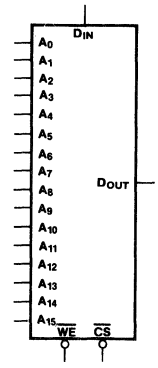
22-PIN LCC
TOP VIEW



SRD7187-002

28-PIN LCC
TOP VIEW

LOGIC SYMBOL



SRD7187-003

PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7187S MIN.	IDT7187S TYP.(1)	IDT7187S MAX.	IDT7187L MIN.	IDT7187L TYP.(1)	IDT7187L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS (for each speed)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	25ns		30ns		35ns		45ns		55ns		70ns		85ns		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	S	90	105	90	105	90	105	90	105	90	105	90	105	90	105	mA
		L	70	85	70	85	70	85	70	85	70	85	70	85	70	85	
I_{CC2}	Dyn. Op. Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	S	120	130	110	120	110	120	110	120	110	120	110	120	110	120	mA
		L	100	110	95	110	90	100	85	95	85	95	80	90	80	90	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	S	55	55	45	50	45	50	45	50	45	50	45	50	45	50	mA
		L	45	50	40	45	35	40	30	35	25	30	25	28	25	28	
I_{SB1}	Full Stdby. Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	S	15	20	15	20	15	20	15	20	15	20	15	20	15	20	mA
		L	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	0.3	1.5	

NOTE:
1. All values are maximum guaranteed values.

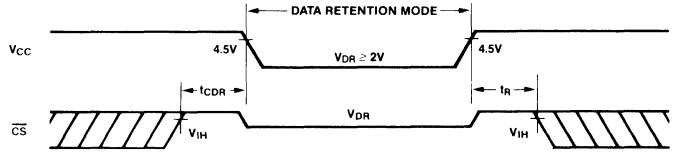
DATA RETENTION CHARACTERISTICS

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1)		MAX.		UNIT
					V_{CC} @ 2.0V	V_{CC} @ 3.0V	V_{CC} @ 2.0V	V_{CC} @ 3.0V	
V_{DR}	Operation Recovery Time	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



SRD7187-005

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

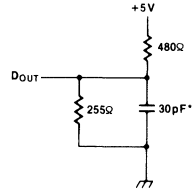


Figure 1. Output Load

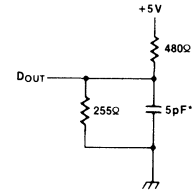


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

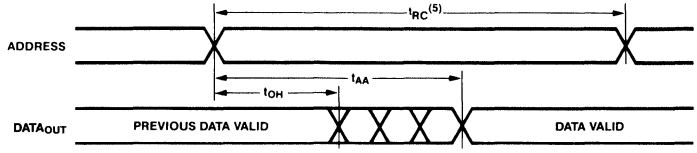
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	7187S25 7187L25 MIN.	MAX.	7187S30 7187L30 MIN.	MAX.	7187S35 7187L35 MIN.	MAX.	7187S45 7187L45 MIN.	MAX.	7187S55 7187L55 MIN.	MAX.	7187S70 7187L70 MIN.	MAX.	7187S85(2) 7187L85(2) MIN.	MAX.	UNITS
READ CYCLE																
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z(3)	—	20	—	25	—	25	—	30	—	30	—	30	—	40	ns
t_{PU}	Chip Select to Power Up Time(3)	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time(3)	—	20	—	30	—	30	—	35	—	35	—	35	—	40	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	25	—	30	—	35	—	45	—	55	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	40	—	50	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	30	—	40	—	50	—	55	—	65	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	20	—	25	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z(3)	0	20	0	25	0	25	0	30	0	30	0	30	0	40	ns
t_{OW}	Output Active from End of Write(3)	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

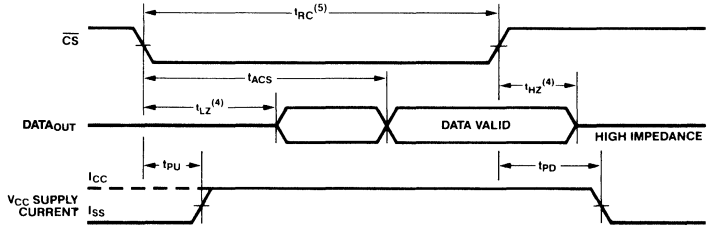
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



SRD7187-008

TIMING WAVEFORM OF READ CYCLE NO. (1, 3)

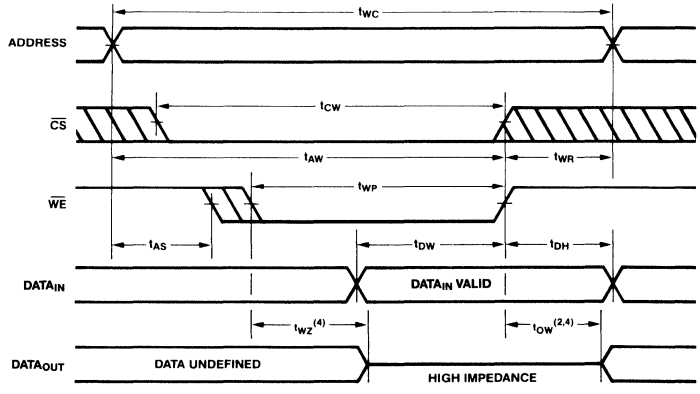


SRD7187-009

NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)

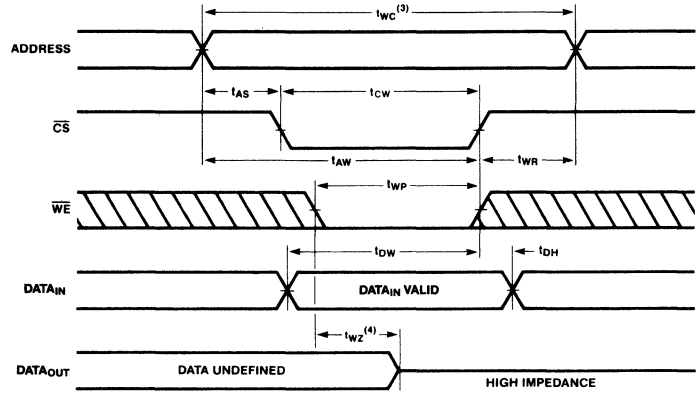


SRD7187-010

NOTES:

1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



SRD7187-011

NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

CMOS STATIC RAMS 64K (16K x 4-BIT)

IDT7188S
IDT7188L

Integrated Device Technology, Inc.

FEATURES:

- High-speed (equal access and cycle times)
  - —Military — 30/35/45/55/70/85ns (max.)
  - —Commercial — 25/30/35/45/55/70ns (max.)
- Low-power operation
  - —IDT7188S
    - Active: 350mW (typ.)
    - Standby: 100μW (typ.)
  - —IDT7188L
    - Active: 300mW (typ.)
    - Standby: 30μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIPs
- Produced with advanced CEMOS™ technology
- Single +5V (±10%) power supply
- Inputs/outputs TTL-compatible
- Three state outputs
- Static operation - no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 25ns are available, with maximum power consumption of only 740mW. The IDT7188 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 20μW when operating from a 2V battery.

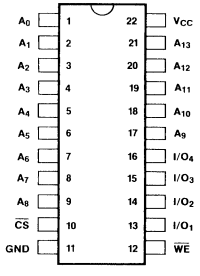
All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT7188 is packaged in a 22-pin, 300 mil DIP providing excellent board-level packing densities.

The IDT7188 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

2

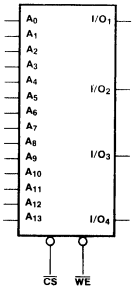
PIN CONFIGURATION



SSD7188-001

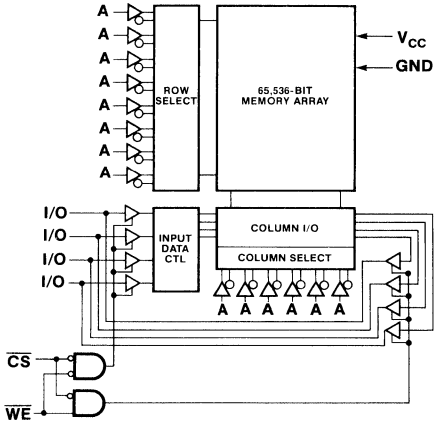
DIP
TOP VIEW

LOGIC SYMBOL



SSD7188-002

FUNCTIONAL BLOCK DIAGRAM



SSD7188-003

PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	I/O_1-I/O_4	DATA I/O
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7188S MIN.	IDT7188S TYP.(1)	IDT7188S MAX.	IDT7188L MIN.	IDT7188L TYP.(1)	IDT7188L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	25ns COM'L.	25ns MIL.	30ns COM'L.	30ns MIL.	35ns COM'L.	35ns MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	70ns COM'L.	70ns MIL.	85ns COM'L.	85ns MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	S	100	—	100	110	100	110	100	110	100	110	100	110	—	110	mA
		L	85	—	85	95	85	95	85	95	85	95	85	95	—	95	
I_{CC2}	Dyn. Op. Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	S	135	—	125	140	125	140	125	140	125	140	125	140	—	140	mA
		L	125	—	115	125	105	115	100	110	100	110	95	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	S	55	—	50	55	45	50	45	50	45	50	45	50	—	50	mA
		L	45	—	40	45	35	40	30	35	30	35	30	35	—	35	
I_{SB1}	Full Stdby. Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	S	15	—	15	20	15	20	15	20	15	20	15	20	—	20	mA
		L	0.5	—	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	

NOTE:

1. All values are maximum guaranteed values.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

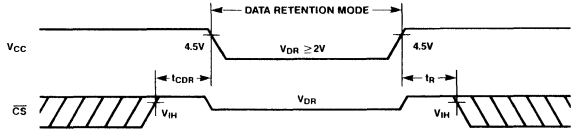
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	μA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		μA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

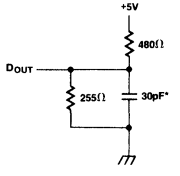
LOW V_{CC} DATA RETENTION WAVEFORM



SSD7188-004

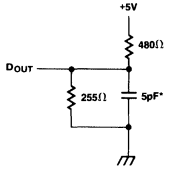
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



SSD7188-005

Figure 1. Output Load



SSD7188-006

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

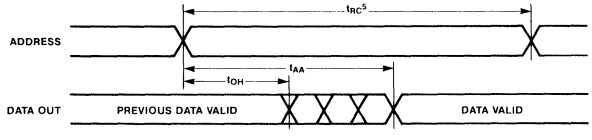
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	7188S25[1] 7188L25[1] MIN.	MAX.	7188S30[4] 7188L30 MIN.	MAX.	7188S35 7188L35 MIN.	MAX.	7188S45 7188L45 MIN.	MAX.	7188S55 7188L55 MIN.	MAX.	7188S70 7188L70 MIN.	MAX.	7188S85[2] 7188L85[2] MIN.	MAX.	UNITS
READ CYCLE																
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z[3]	—	10	—	13	—	15	—	15	—	20	—	25	—	30	ns
t_{PU}	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[3]	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	20	—	25	—	30	—	40	—	50	—	60	—	75	—	ns
t_{CW}	Chip Select to End of Write	20	—	25	—	30	—	35	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	25	—	35	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	25	—	35	—	50	—	60	—	75	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	13	—	15	—	15	—	20	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z[3]	—	7	—	10	—	10	—	15	—	25	—	30	—	40	ns
t_{OW}	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

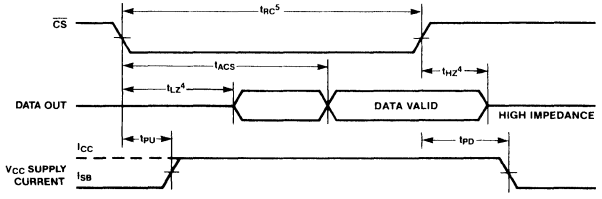
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data only for military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



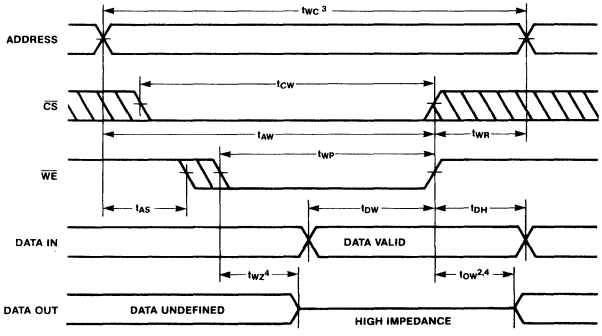
SSD7188-007

TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

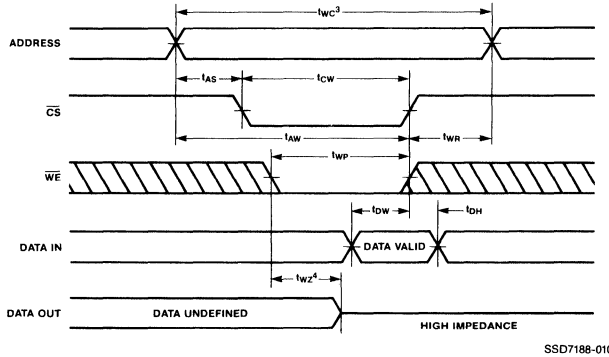


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	I/O	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)

Added chip select and output enable controls

IDT7198S
IDT7198L

FEATURES:

- Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS_1}$, $\overline{CS_2}$) simplify system design and operation
- High-speed (equal access and cycle times)
  - —Military: 30/35/45/55/70/85ns (max.)
  - —Commercial: 25/30/35/45/55/70ns (max.)
- Low-power operation
  - — IDT7198S
    - Active: 350mW (typ.)
    - Standby: 100μW (typ.)
  - — IDT7198L
    - Active: 300mW (typ.)
    - Standby: 30μW (typ.)
- Battery back-up operation — 2V data retention (L version only)
- 24-pin THINDIP, 24-pin plastic DIP and high-density 28-pin leadless chip carrier
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three state outputs
- Military product 100% screened to MIL-STD-883, Class B

MEMORY CONTROL:

The IDT7198 64K high-speed CEMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

The dual chip select feature ($\overline{CS_1}$, $\overline{CS_2}$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding. Since external decoding logic is reduced, board space is saved, system speed is enhanced by approximately 10-20ns and system reliability improves as a result of lower part count.

Both chip selects, chip select 1 ($\overline{CS_1}$) and chip select 2 ($\overline{CS_2}$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

The output enable function ($\overline{OE}$) is also a highly desirable feature of the IDT7198 high-speed common I/O static RAM. This function is designed to eliminate problems associated with data bus contention by allowing the data outputs to be controlled independent of either chip select.

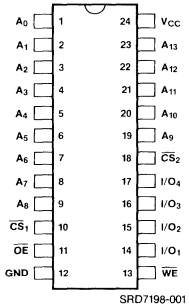
These added memory control features provide improved system design flexibility, along with overall system speed performance enhancements.

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

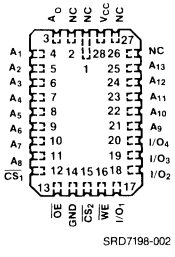
The IDT7198 features three memory control functions: chip select 1 ($\overline{CS_1}$), chip select 2 ($\overline{CS_2}$) and output enable ($\overline{OE}$). These three functions greatly enhance the IDT7198's overall flexibility in high-speed memory applications. **(Con't on next page)**

PIN CONFIGURATION



SRD7198-001

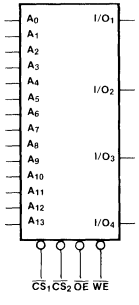
DIP
TOP VIEW



SRD7198-002

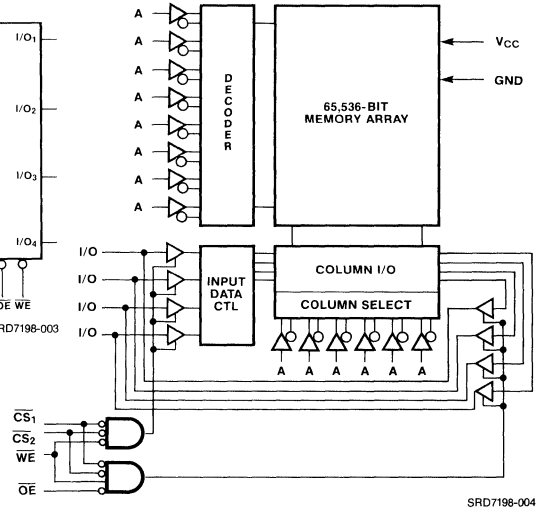
LCC
TOP VIEW

LOGIC SYMBOL



SRD7198-003

FUNCTIONAL BLOCK DIAGRAM



SRD7198-004

PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS_1}$	CHIP SELECT 1	I/O_1-I/O_4	DATA I/O
$\overline{CS_2}$	CHIP SELECT 2	V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

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MILITARY AND COMMERCIAL TEMPERATURE RANGES **JULY 1986**

Printed in U.S.A.

DESCRIPTION (Con't)

Access times as fast as 25ns are available, with maximum power consumption of only 740mW. The IDT7198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 20μW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT7198 is packaged in either a 24-pin DIP, 24-pin plastic DIP or 28-pin leadless chip carrier, providing improved board-level packing densities.

The IDT7198 military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7198S MIN.	IDT7198S TYP.(1)	IDT7198S MAX.	IDT7198L MIN.	IDT7198L TYP.(1)	IDT7198L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	25ns		30ns		35ns		45ns		55ns		70ns		85ns		UNIT
			COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	S	100	—	100	110	100	110	100	110	100	110	100	110	—	110	mA
		L	85	—	85	95	85	95	85	95	85	95	85	95	—	95	
I_{CC2}	Dyn. Op. Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	S	135	—	125	140	125	140	125	140	125	140	125	140	—	140	mA
		L	125	—	115	125	105	115	100	110	100	110	95	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	S	55	—	50	55	45	50	45	50	45	50	45	50	—	50	mA
		L	45	—	40	45	35	40	30	35	30	35	30	35	—	35	
I_{SB1}	Full Stdby. Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	S	15	—	15	20	15	20	15	20	15	20	15	20	—	20	mA
		L	0.5	—	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	

NOTE:
1. All values are maximum guaranteed values.

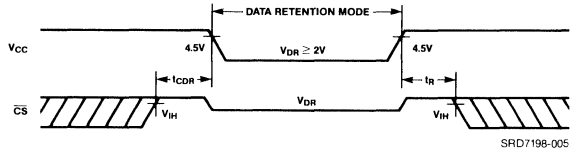
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1)		MAX.		UNIT
					V_{CC} @ 2.0V	3.0V	V_{CC} @ 2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

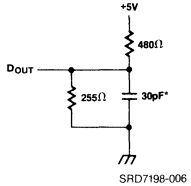


Figure 1. Output Load
***Including scope and jig**

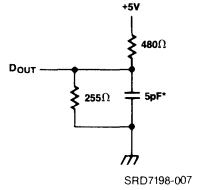


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

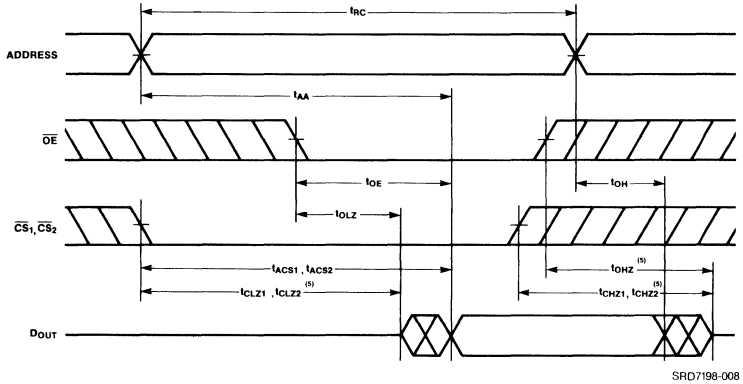
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	7198S25[1] 7198L25[1] MIN.	MAX.	7198S30[5] 7198L30[5] MIN.	MAX.	7198S35 7198L35 MIN.	MAX.	7198S45 7198L45 MIN.	MAX.	7198S55 7198L55 MIN.	MAX.	7198S70 7198L70 MIN.	MAX.	7198S85[2] 7198L85[2] MIN.	MAX.	UNITS
READ CYCLE																
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
$t_{ACS1, 2}$	Chip Select-1, 2 Access Time[3]	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
$t_{CLZ1, 2}$[4]	Chip Select-1, 2 to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	20	—	25	—	30	—	35	—	45	—	55	ns
t_{OLZ}[4]	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1, 2}$[4]	Chip Select-1, 2 to Output in High Z	—	10	—	13	—	15	—	15	—	20	—	25	—	30	ns
t_{OHZ}[4]	Output Disable to Output in High Z	—	15	—	15	—	15	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}[4]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}[4]	Chip Deselect to Power Down Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	20	—	25	—	30	—	40	—	50	—	60	—	75	—	ns
$t_{CW1, 2}$	Chip Select to End of Write[3]	20	—	25	—	30	—	35	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	25	—	35	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	25	—	35	—	50	—	60	—	75	—	ns
$t_{WR1, 2}$	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}[4]	Write Enable to Output in High Z	—	7	—	10	—	10	—	15	—	25	—	30	—	40	ns
t_{DW}	Data Valid to End of Write	13	—	15	—	15	—	20	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}[4]	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

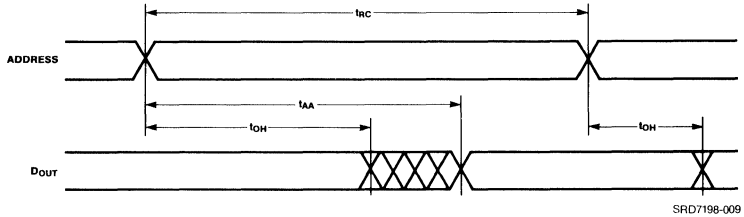
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data only for military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



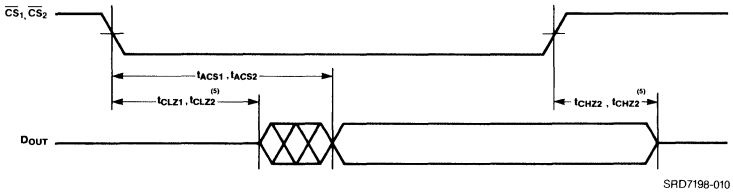
SRD7198-008

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD7198-009

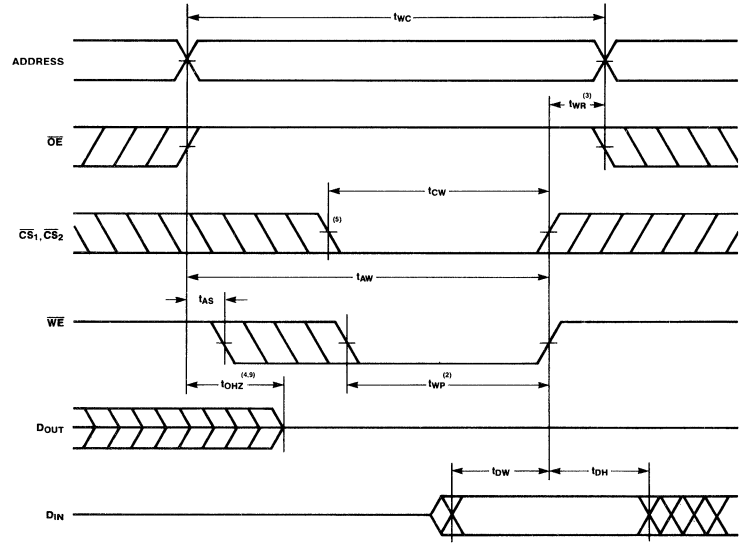
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SRD7198-010

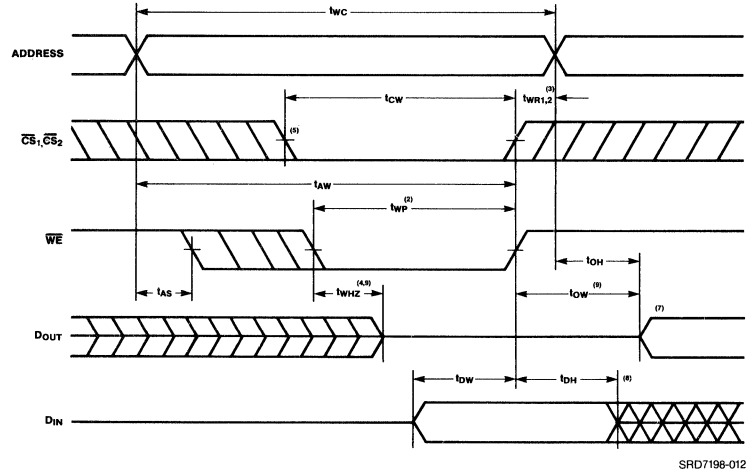
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, $\overline{CS_2}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS_1}$ and or $\overline{CS_2}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



SRD7198-011

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



SRD7198-012

NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$ and a low $\overline{CS_2}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{CS_2}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ and or $\overline{CS_2}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS_1}$ and $\overline{CS_2}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write	L	L	L	X	D_{IN}	Active
Read	L	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

2

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)

Separate data inputs and outputs

IDT71981S/L
IDT71982S/L

FEATURES:

- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - —Commercial — 25/30/35/45/55/70ns (max.)
  - —Military — 30/35/45/55/70/85ns (max.)
- Low-power consumption
  - —IDT71981/2S
    - Active: 300mW (Typ.)
    - Standby: 100μW (Typ.)
  - —IDT71981/2L
    - Active: 300mW (Typ.)
    - Standby: 30μW (Typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin 400 mil DIP and 28-pin leadless chip carriers
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (± 10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

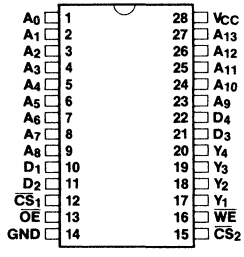
Access times as fast as 25ns are available with maximum power consumption of only 740mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}_1$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra low-power standby mode (I_{SB1}), the devices consume less than 30μW, typically. This capability provides significant system-level power and cooling savings. The low-power(L) versions also offer a battery backup data retention capability where the circuit typically consumes only 20μW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71981/IDT71982 are packaged in either space-saving 28-pin, 400 mil DIPs or 28-pin leadless chip carriers, providing high board-level packing densities.

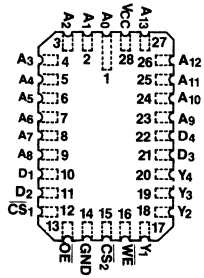
The IDT71981/IDT71982 military RAMs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



DIP
TOP VIEW

SRD71981-002



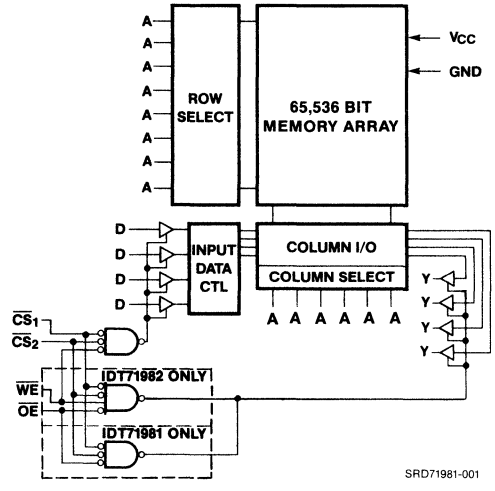
LCC
TOP VIEW

SRD71981-003

PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	D_1-D_4	DATA IN
$\overline{CS}_1$, $\overline{CS}_2$	CHIP SELECTS	Y_1-Y_4	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{OE}$	OUTPUT ENABLE	V_{CC}	POWER

FUNCTIONAL BLOCK DIAGRAM



SRD71981-001

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MILITARY AND COMMERCIAL TEMPERATURE RANGES **JULY 1986**

Printed in U.S.A.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} min = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS (for all speeds)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71981/2S MIN.	IDT71981/2S TYP.(1)	IDT71981/2S MAX.	IDT71981/2L MIN.	IDT71981/2L TYP.(1)	IDT71981/2L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	25ns COM'L.	25ns MIL.	30ns COM'L.	30ns MIL.	35ns COM'L.	35ns MIL.	45ns COM'L.	45ns MIL.	55ns COM'L.	55ns MIL.	70ns COM'L.	70ns MIL.	85ns COM'L.	85ns MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = 0	S	100	—	100	110	100	110	100	110	100	110	100	110	—	110	mA
		L	85	—	85	95	85	95	85	95	85	95	85	95	—	95	
I_{CC2}	Dyn. Op. Current $\overline{CS}$ = V_{IL}, Output Open, V_{CC} = Max., f = f Max.	S	135	—	125	140	125	140	125	140	125	140	125	140	—	140	mA
		L	125	—	115	125	105	115	100	110	100	110	95	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open	S	55	—	50	55	45	50	45	50	45	50	45	50	—	50	mA
		L	45	—	40	45	35	40	30	35	30	35	30	35	—	35	
I_{SB1}	Full Stdby. Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	S	15	—	15	20	15	20	15	20	15	20	15	20	—	20	mA
		L	0.5	—	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	

NOTE:

1. All values are maximum guaranteed values.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

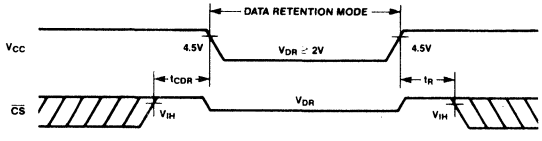
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—		—		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—		—		ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—		2		µA

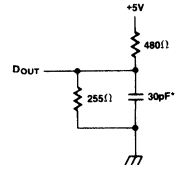
NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM

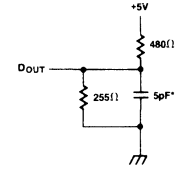


SRD7198-005



SRD7198-006

Figure 1. Output Load



SRD7198-007

Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

***Including scope and jig**

AC TEST CONDITIONS

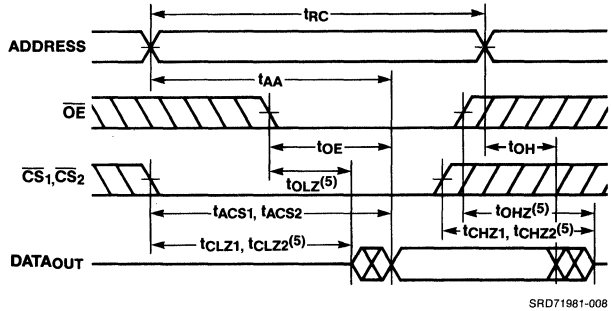
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1 and 2

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

SYMBOL	PARAMETER	71981/2S25[6] 71981/2L25[6] MIN.	MAX.	71981/2S30 71981/2L30 MIN.	MAX.	71981/2S35 71981/2L35 MIN.	MAX.	71981/2S45 71981/2L45 MIN.	MAX.	71981/2S55 71981/2L55 MIN.	MAX.	71981/2S70 71981/2L70 MIN.	MAX.	71981/2S85[1] 71981/2L85[1] MIN.	MAX.	UNITS
READ CYCLE																
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1, 2 Access Time[2]	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	20	—	25	—	30	—	35	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z[3]	—	10	—	13	—	15	—	15	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z[3]	—	15	—	15	—	15	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[3]	—	25	—	30	—	35	—	45	—	55	—	70	—	85	ns
WRITE CYCLE																
t_{WC}	Write Cycle Time	20	—	25	—	30	—	40	—	50	—	60	—	75	—	ns
$t_{CW1,2}$	Chip Select to End of Write	20	—	25	—	30	—	35	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	20	—	25	—	25	—	35	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	25	—	35	—	50	—	60	—	75	—	ns
$t_{WR1,2}$	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z[3,5]	—	7	—	10	—	10	—	15	—	25	—	30	—	40	ns
t_{DW}	Data Valid to End of Write	13	—	15	—	15	—	20	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write[3,5]	5	—	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{IY}	Data Valid to Output Valid[4]	—	20	—	30	—	30	—	35	—	40	—	45	—	50	ns
t_{WY}	Write Enable to Output Valid[4]	—	20	—	30	—	30	—	35	—	40	—	45	—	50	ns

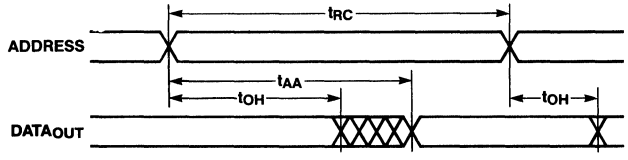
NOTES:
1. -55°C to +125°C temperature range only.
2. Both chip selects must be active low for the device to be selected.
3. This parameter guaranteed but not tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.
6. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



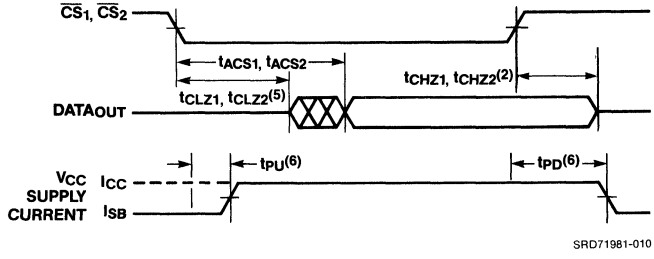
SRD71981-008

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD71981-009

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

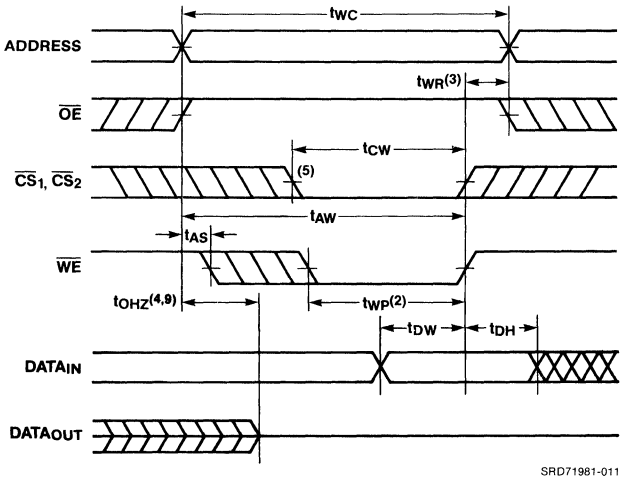


SRD71981-010

NOTES:

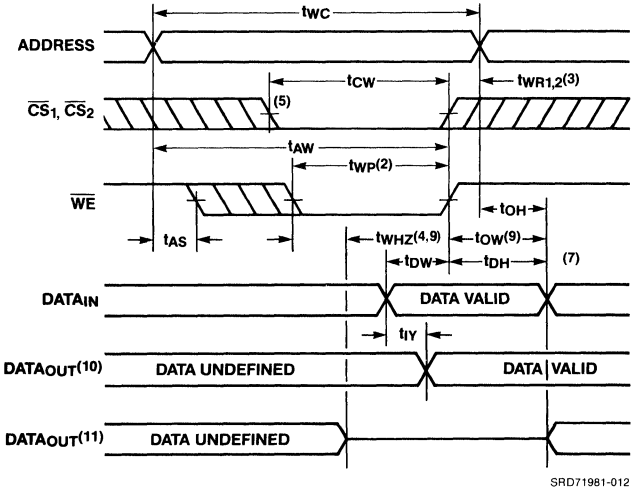
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$, and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.
6. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1[1]

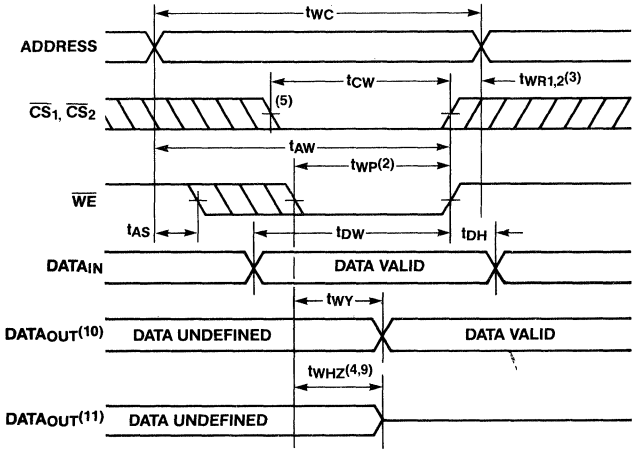


2

TIMING WAVEFORM OF WRITE CYCLE NO. 2[1,6]



TIMING WAVEFORM OF WRITE CYCLE NO. 3(1,6)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a low $\overline{CS}_2$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$ or $\overline{CS}_2$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ and or $\overline{CS}_2$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ and $\overline{CS}_2$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.
10. For IDT71981 only.
11. For IDT71982 only.

TRUTH TABLE

MODE	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	OUTPUT	POWER
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write(1)	L	L	L	L	D_{IN}	Active
Write(1)	L	L	L	H	High Z	Active
Write(2)	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

NOTES:

1. For IDT71981 only.
2. For IDT71982 only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

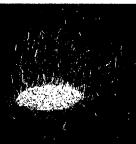
SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTES:

1. This parameter is sampled and not 100% tested.

Integrated Device Technology, Inc

Static RAM Ordering Information



ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6116LA30P	30	75	P24-1, P24-2	Com'l.
IDT6116LA30D			D24-1	
IDT6116LA30T			D24-2	
IDT6116LA30L			L28-1, L32	
IDT6116LA30F			F24	
IDT6116SA30P		80	P24-1, P24-2	
IDT6116SA30D			D24-1	
IDT6116SA30T			D24-2	
IDT6116SA30L			L28-1, L32	
IDT6116SA30F			F24	
IDT6116LA35P	35	75	P24-1, P24-2	Com'l.
IDT6116LA35D			D24-1	
IDT6116LA35T			D24-2	
IDT6116LA35L			L28-1, L32	
IDT6116LA35F			F24	
IDT6116LA35DB		85	D24-1	Mil.
IDT6116LA35TB			D24-2	
IDT6116LA35LB			L28-1, L32	
IDT6116LA35FB			F24	
IDT6116SA35P		80	P24-1, P24-2	Com'l.
IDT6116SA35D			D24-1	
IDT6116SA35T			D24-2	
IDT6116SA35L			L28-1, L32	
IDT6116SA35F			F24	
IDT6116SA35DB		90	D24-1	Mil.
IDT6116SA35TB			D24-2	
IDT6116SA35LB			L28-1, L32	
IDT6116SA35FB			F24	
IDT6116LA45P	45	75	P24-1, P24-2	Com'l.
IDT6116LA45D			D24-1	
IDT6116LA45T			D24-2	
IDT6116LA45L			L28-1, L32	
IDT6116LA45F			F24	
IDT6116LA45DB		85	D24-1	Mil.
IDT6116LA45TB			D24-2	
IDT6116LA45LB			L28-1, L32	
IDT6116LA45FB			F24	
IDT6116SA45P		80	P24-1, P24-2	Com'l.
IDT6116SA45D			D24-1	
IDT6116SA45T			D24-2	
IDT6116SA45L			L28-1, L32	
IDT6116SA45F			F24	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6116SA45DB	45	90	D24-1	Mil.
IDT6116SA45TB			D24-2	
IDT6116SA45LB			L28-1, L32	
IDT6116SA45FB			F24	
IDT6116LA55P	55	75	P24-1, P24-2	Com'l.
IDT6116LA55D			D24-1	
IDT6116LA55T			D24-2	
IDT6116LA55L			L28-1, L32	
IDT6116LA55F			F24	
IDT6116LA55DB		85	D24-1	Mil.
IDT6116LA55TB			D24-2	
IDT6116LA55LB			L28-1, L32	
IDT6116LA55FB			F24	
IDT6116SA55P		80	P24-1, P24-2	Com'l.
IDT6116SA55D			D24-1	
IDT6116SA55T			D24-2	
IDT6116SA55L			L28-1, L32	
IDT6116SA55F			F24	
IDT6116SA55DB		90	D24-1	Mil.
IDT6116SA55TB			D24-2	
IDT6116SA55LB			L28-1, L32	
IDT6116SA55FB			F24	
IDT6116LA70P	70	75	P24-1, P24-2	Com'l.
IDT6116LA70D			D24-1	
IDT6116LA70T			D24-2	
IDT6116LA70L			L28-1, L32	
IDT6116LA70F			F24	
IDT6116LA70DB		85	D24-1	Mil.
IDT6116LA70TB			D24-2	
IDT6116LA70LB			L28-1, L32	
IDT6116LA70FB			F24	
IDT6116SA70P		80	P24-1, P24-2	Com'l.
IDT6116SA70D			D24-1	
IDT6116SA70T			D24-2	
IDT6116SA70L			L28-1, L32	
IDT6116SA70F			F24	
IDT6116SA70DB		90	D24-1	Mil.
IDT6116SA70TB			D24-2	
IDT6116SA70LB			L28-1, L32	
IDT6116SA70FB			F24	
IDT6116LA90P	90	75	P24-1, P24-2	Com'l.
IDT6116LA90D			D24-1	
IDT6116LA90T			D24-2	
IDT6116LA90L			L28-1, L32	
IDT6116LA90F			F24	

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ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6116LA90DB	90	85	D24-1	Mil.
IDT6116LA90TB			D24-2	
IDT6116LA90LB			L28-1, L32	
IDT6116LA90FB			F24	
IDT6116SA90P		80	P24-1, P24-2	Com'l.
IDT6116SA90D			D24-1	
IDT6116SA90T			D24-2	
IDT6116SA90L			L28-1, L32	
IDT6116SA90F			F24	
IDT6116SA90DB		90	D24-1	Mil.
IDT6116SA90TB			D24-2	
IDT6116SA90LB			L28-1, L32	
IDT6116SA90FB			F24	
IDT6116LA120DB	120	85	D24-1	Mil.
IDT6116LA120TB			D24-2	
IDT6116LA120LB			L28-1, L32	
IDT6116LA120FB			F24	
IDT6116SA120DB		90	D24-1	
IDT6116SA120TB			D24-2	
IDT6116SA120LB			L28-1, L32	
IDT6116SA120FB			F24	
IDT6116LA150DB	150	85	D24-1	Mil.
IDT6116LA150TB			D24-2	
IDT6116LA150LB			L28-1, L32	
IDT6116LA150FB			F24	
IDT6116SA150DB		90	D24-1	Mil.
IDT6116SA150TB			D24-2	
IDT6116SA150LB			L28-1, L32	
IDT6116SA150FB			F24	
IDT6167SA15P	15	90	P20	Com'l.
IDT6167SA15D			D20	
IDT6167SA15L			L20-1	
IDT6167SA15F			F20	
IDT6167LA20P	20	55	P20	Com'l.
IDT6167LA20D			D20	
IDT6167LA20L			L20-1	
IDT6167LA20F			F20	
IDT6167SA20P		90	P20	
IDT6167SA20D			D20	
IDT6167SA20L			L20-1	
IDT6167SA20F			F20	
IDT6167LA25P	25	55	P20	Com'l.
IDT6167LA25D			D20	
IDT6167LA25L			L20-1	
IDT6167LA25F			F20	
IDT6167LA25DB		60	D20	Mil.
IDT6167LA25LB			L20-1	
IDT6167LA25FB			F20	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6167SA25P	25	90	P20	Com'l.
IDT6167SA25D			D20	
IDT6167SA25L			L20-1	
IDT6167SA25F			F20	
IDT6167SA25DB			D20	Mil.
IDT6167SA25LB			L20-1	
IDT6167SA25FB			F20	
IDT6167LA35P	35	55	P20	Com'l.
IDT6167LA35D			D20	
IDT6167LA35L			L20-1	
IDT6167LA35F			F20	
IDT6167LA35DB		60	D20	Mil.
IDT6167LA35LB			L20-1	
IDT6167LA35FB			F20	
IDT6167SA35P		90	P20	Com'l.
IDT6167SA35D			D20	
IDT6167SA35L			L20-1	
IDT6167SA35F			F20	
IDT6167SA35DB			D20	Mil.
IDT6167SA35LB			L20-1	
IDT6167SA35FB			F20	
IDT6167LA45P	45	55	P20	Com'l.
IDT6167LA45D			D20	
IDT6167LA45L			L20-1	
IDT6167LA45F			F20	
IDT6167LA45DB		60	D20	Mil.
IDT6167LA45LB			L20-1	
IDT6167LA45FB			F20	
IDT6167SA45P		90	P20	Com'l.
IDT6167SA45D			D20	
IDT6167SA45L			L20-1	
IDT6167SA45F			F20	
IDT6167SA45DB			D20	Mil.
IDT6167SA45LB			L20-1	
IDT6167SA45FB			F20	
IDT6167LA55P	55	55	P20	Com'l.
IDT6167LA55D			D20	
IDT6167LA55L			L20-1	
IDT6167LA55F			F20	
IDT6167LA55DB		60	D20	Mil.
IDT6167LA55LB			L20-1	
IDT6167LA55FB			F20	
IDT6167SA55P		90	P20	Com'l.
IDT6167SA55D			D20	
IDT6167SA55L			L20-1	
IDT6167SA55F			F20	
IDT6167SA55DB			D20	Mil.
IDT6167SA55LB			L20-1	
IDT6167SA55FB			F20	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6167LA70DB	70	60	D20	Mil.
IDT6167LA70LB			L20-1	
IDT6167LA70FB			F20	
IDT6167SA70DB		90	D20	Mil.
IDT6167SA70LB			L20-1	
IDT6167SA70FB			F20	
IDT6167LA85DB	85	60	D20	Mil.
IDT6167LA85LB			L20-1	
IDT6167LA85FB			F20	
IDT6167SA85DB		90	D20	
IDT6167SA85LB			L20-1	
IDT6167SA85FB			F20	
IDT6167LA100DB	100	60	D20	Mil.
IDT6167LA100LB			L20-1	
IDT6167LA100FB			F20	
IDT6167SA100DB		90	D20	
IDT6167SA100LB			L20-1	
IDT6167SA100FB			F20	
IDT6168LA20P	20	70	P20	Com'l.
IDT6168LA20D			D20	
IDT6168LA20L			L20-1	
IDT6168LA20F			F20	
IDT6168SA20P		90	P20	
IDT6168SA20D			D20	
IDT6168SA20L			L20-1	
IDT6168SA20F			F20	
IDT6168LA25P	25	70	P20	Com'l.
IDT6168LA25D			D20	
IDT6168LA25L			L20-1	
IDT6168LA25F			F20	
IDT6168LA25DB		80	D20	Mil.
IDT6168LA25LB			L20-1	
IDT6168LA25FB			F20	
IDT6168SA25P		90	P20	Com'l.
IDT6168SA25D			D20	
IDT6168SA25L			L20-1	
IDT6168SA25F			F20	
IDT6168SA25DB		100	D20	Mil.
IDT6168SA25LB			L20-1	
IDT6168SA25FB			F20	
IDT6168LA35P	35	70	P20	Com'l.
IDT6168LA35D			D20	
IDT6168LA35L			L20-1	
IDT6168LA35F			F20	
IDT6168LA35DB		80	D20	Mil.
IDT6168LA35LB			L20-1	
IDT6168LA35FB			F20	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6168SA35P	35	90	P20	Com'l.
IDT6168SA35D			D20	
IDT6168SA35L			L20-1	
IDT6168SA35F			F20	
IDT6168SA35DB		100	D20	Mil.
IDT6168SA35LB			L20-1	
IDT6168SA35FB			F20	
IDT6168LA45P	45	70	P20	Com'l.
IDT6168LA45D			D20	
IDT6168LA45L			L20-1	
IDT6168LA45F			F20	
IDT6168LA45DB		80	D20	Mil.
IDT6168LA45LB			L20-1	
IDT6168LA45FB			F20	
IDT6168SA45P		90	P20	Com'l.
IDT6168SA45D			D20	
IDT6168SA45L			L20-1	
IDT6168SA45F			F20	
IDT6168SA45DB		100	D20	Mil.
IDT6168SA45LB			L20-1	
IDT6168SA45FB			F20	
IDT6168LA55P	55	70	P20	Com'l.
IDT6168LA55D			D20	
IDT6168LA55L			L20-1	
IDT6168LA55F			F20	
IDT6168LA55DB		80	D20	Mil.
IDT6168LA55LB			L20-1	
IDT6168LA55FB			F20	
IDT6168SA55P		90	P20	Com'l.
IDT6168SA55D			D20	
IDT6168SA55L			L20-1	
IDT6168SA55F			F20	
IDT6168SA55DB		100	D20	Mil.
IDT6168SA55LB			L20-1	
IDT6168SA55FB			F20	
IDT6168LA70DB	70	80	D20	Mil.
IDT6168LA70LB			L20-1	
IDT6168LA70FB			F20	
IDT6168SA70DB		100	D20	
IDT6168SA70LB			L20-1	
IDT6168SA70FB			F20	
IDT6168LA85DB	85	80	D20	Mil.
IDT6168LA85LB			L20-1	
IDT6168LA85FB			F20	
IDT6168SA85DB		100	D20	
IDT6168SA85LB			L20-1	
IDT6168SA85FB			F20	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT6168LA100DB	100	80	D20	Mil.
IDT6168LA100LB			L20-1	
IDT6168LA100FB			F20	
IDT6168SA100DB		100	D20	
IDT6168SA100LB			L20-1	
IDT6168SA100FB			F20	
IDT71256L45D	45	—	D28-1	Com'l.
IDT71256L45T			D28-2	
IDT71256L45L			L32	
IDT71256S45D			D28-1	
IDT71256S45T			D28-2	
IDT71256S45L			L32	
IDT71256L55D	55	—	D28-1	Com'l.
IDT71256L55T			D28-2	
IDT71256L55L			L32	
IDT71256L55DB			D28-1	Mil.
IDT71256L55TB			D28-2	
IDT71256L55LB			L32	
IDT71256S55D			D28-1	Com'l.
IDT71256S55T			D28-2	
IDT71256S55L			L32	
IDT71256S55DB			D28-1	Mil.
IDT71256S55TB			D28-2	
IDT71256S55LB			L32	
IDT71256L70D	70	—	D28-1	Com'l.
IDT71256L70T			D28-2	
IDT71256L70L			L32	
IDT71256L70DB			D28-1	Mil.
IDT71256L70TB			D28-2	
IDT71256L70LB			L32	
IDT71256S70D			D28-1	Com'l.
IDT71256S70T			D28-2	
IDT71256S70L			L32	
IDT71256S70DB			D28-1	Mil.
IDT71256S70TB			D28-2	
IDT71256S70LB			L32	
IDT71256L85DB	85	—	D28-1	Mil.
IDT71256L85TB			D28-2	
IDT71256L85LB			L32	
IDT71256S85DB			D28-1	
IDT71256S85TB			D28-2	
IDT71256S85LB			L32	
IDT71257L35T	35	—	D24-2	Com'l.
IDT71257S35T				
IDT71257L45T	45	—	D24-2	Com'l.
IDT71257L45TB				Mil.
IDT71257S45T				Com'l.
IDT71257S45TB				Mil.

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT71257L55T	55	—	D24-2	Com'l.
IDT71257L55TB				Mil.
IDT71257S55T				Com'l.
IDT71257S55TB				Mil.
IDT71257L70T	70	—	D24-2	Com'l.
IDT71257L70TB				Mil.
IDT71257S70T				Com'l.
IDT71257S70TB				Mil.
IDT71257L85TB	85	—	D24-2	Mil.
IDT71257S85TB				
IDT71258L35T	35	—	D24-2	Com'l.
IDT71258S35T				
IDT71258L45T	45	—	D24-2	Com'l.
IDT71258L45TB				Mil.
IDT71258S45T				Com'l.
IDT71258S45TB				Mil.
IDT71258L55T	55	—	D24-2	Com'l.
IDT71258L55TB				Mil.
IDT71258S55T				Com'l.
IDT71258S55TB				Mil.
IDT71258L70T	70	—	D24-2	Com'l.
IDT71258L70TB				Mil.
IDT71258S70T				Com'l.
IDT71258S70TB				Mil.
IDT71258L85TB	85	—	D24-2	Mil.
IDT71258S85TB				
IDT7130L55P	55	120	P48	Com'l.
IDT7130L55J			J52	
IDT7130L55C			D48-1	
IDT7130L55L			L48, L52	
IDT7130S55P		170	P48	
IDT7130S55J			J52	
IDT7130S55C			D48-1	
IDT7130S55L			L48, L52	
IDT7130L70P	70	120	P48	Com'l.
IDT7130L70J			J52	
IDT7130L70C			D48-1	
IDT7130L70L			L48, L52	
IDT7130L70CB		180	D48-1	Mil.
IDT7130L70LB			L48, L52	
IDT7130S70P		170	P48	Com'l.
IDT7130S70J			J52	
IDT7130S70C			D48-1	
IDT7130S70L			L48, L52	
IDT7130S70CB		225	D48-1	Mil.
IDT7130S70LB			L48, L52	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7130L90P	90	120	P48	Com'l.
IDT7130L90J			J52	
IDT7130L90C			D48-1	
IDT7130L90L			L48, L52	
IDT7130L90CB		150	D48-1	Mil.
IDT7130L90LB			L48, L52	
IDT7130S90P		170	P48	Com'l.
IDT7130S90J			J52	
IDT7130S90C			D48-1	
IDT7130S90L			L48, L52	
IDT7130S90CB		185	D48-1	Mil.
IDT7130S90LB			L48, L52	
IDT7130L100P	100	120	P48	Com'l.
IDT7130L100J			J52	
IDT7130L100C			D48-1	
IDT7130L100L			L48, L52	
IDT7130L100CB		150	D48-1	Mil.
IDT7130L100LB			L48, L52	
IDT7130S100P		170	P48	Com'l.
IDT7130S100J			J52	
IDT7130S100C			D48-1	
IDT7130S100L			L48, L52	
IDT7130S100CB		185	D48-1	Mil.
IDT7130S100LB			L48, L52	
IDT7130L120CB	120	150	D48-1	Mil.
IDT7130L120LB			L48, L52	
IDT7130S120CB		185	D48-1	
IDT7130S120LB			L48, L52	
IDT7132L55P	55	120	P48	Com'l.
IDT7132L55J			J52	
IDT7132L55C			D48-1	
IDT7132L55L			L48, L52	
IDT7132S55P		170	P48	
IDT7132S55J			J52	
IDT7132S55C			D48-1	
IDT7132S55L			L48, L52	
IDT7132L70P	70	120	P48	Com'l.
IDT7132L70J			J52	
IDT7132L70C			D48-1	
IDT7132L70L			L48, L52	
IDT7132L70CB		180	D48-1	Mil.
IDT7132L70LB			L48, L52	
IDT7132S70P		170	P48	Com'l.
IDT7132S70J			J52	
IDT7132S70C			D48-1	
IDT7132S70L			L48, L52	
IDT7132S70CB		225	D48-1	Mil.
IDT7132S70LB			L48, L52	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7132L90P	90	120	P48	Com'l.
IDT7132L90J			J52	
IDT7132L90C			D48-1	
IDT7132L90L			L48, L52	
IDT7132L90CB		150	D48-1	Mil.
IDT7132L90LB			L48, L52	
IDT7132S90P		170	P48	Com'l.
IDT7132S90J			J52	
IDT7132S90C			D48-1	
IDT7132S90L			L48, L52	
IDT7132S90CB		185	D48-1	Mil.
IDT7132S90LB			L48, L52	
IDT7132L100P	100	120	P48	Com'l.
IDT7132L100J			J52	
IDT7132L100C			D48-1	
IDT7132L100L			L48, L52	
IDT7132L100CB		150	D48-1	Mil.
IDT7132L100LB			L48, L52	
IDT7132S100P		170	P48	Com'l.
IDT7132S100J			J52	
IDT7132S100C			D48-1	
IDT7132S100L			L48, L52	
IDT7132S100CB		185	D48-1	Mil.
IDT7132S100LB			L48, L52	
IDT7132L120CB	120	150	D48-1	Mil.
IDT7132L120LB			L48, L52	
IDT7132S120CB		185	D48-1	
IDT7132S120LB			L48, L52	
IDT71322L45P	45	—	P48	Com'l.
IDT71322L45C			D48-1	
IDT71322L45L			L52	
IDT71322S45P			P48	
IDT71322S45C			D48-1	
IDT71322S45L			L52	
IDT71322L55P	55	—	P48	Com'l.
IDT71322L55C			D48-1	
IDT71322L55L			L52	
IDT71322L55CB			D48-1	Mil.
IDT71322L55LB			L52	
IDT71322S55P			P48	Com'l.
IDT71322S55C			D48-1	
IDT71322S55L			L52	
IDT71322S55CB			D48-1	Mil.
IDT71322S55LB			L52	
IDT71322L70P	70	—	P48	Com'l.
IDT71322L70C			D48-1	
IDT71322L70L			L52	
IDT71322L70CB			D48-1	Mil.
IDT71322L70LB			L52	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT71322S70P	70	—	P48	Com'l.
IDT71322S70C			D48-1	
IDT71322S70L			L52	
IDT71322S70CB			D48-1	Mil.
IDT71322S70LB			L52	
IDT71322L90P	90	—	P48	Com'l.
IDT71322L90C			D48-1	
IDT71322L90L			L52	
IDT71322L90CB			D48-1	Mil.
IDT71322L90LB			L52	
IDT71322S90P			P48	Com'l.
IDT71322S90C			D48-1	
IDT71322S90L			L52	
IDT71322S90CB			D48-1	Mil.
IDT71322S90LB			L52	
IDT71322L100CB	100	—	D48-1	Mil.
IDT71322L100LB			L52	
IDT71322S100CB			D48-1	
IDT71322S100LB			L52	
IDT7133L70P	70	—	P68	Com'l.
IDT7133L70XC			D68	
IDT7133L70L			L68	
IDT7133S70P			P68	
IDT7133S70XC			D68	
IDT7133S70L			L68	
IDT7133L90P	90	—	P68	Com'l.
IDT7133L90XC			D68	
IDT7133L90L			L68	
IDT7133L90XCB			D68	Mil.
IDT7133L90LB			L68	
IDT7133S90P			P68	Com'l.
IDT7133S90XC			D68	
IDT7133S90L			L68	
IDT7133S90XCB			D68	Mil.
IDT7133S90LB			L68	
IDT7133L100P	100	—	P68	Com'l.
IDT7133L100XC			D68	
IDT7133L100L			L68	
IDT7133L100XCB			D68	Mil.
IDT7133L100LB			L68	
IDT7133S100P			P68	Com'l.
IDT7133S100XC			D68	
IDT7133S100L			L68	
IDT7133S100XCB			D68	Mil.
IDT7133S100LB			L68	
IDT7133L120XCB	120	—	D68	Mil.
IDT7133L120LB			L68	
IDT7133S120XCB			D68	
IDT7133S120LB			L68	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7134L45P	45	—	P48	Com'l.
IDT7134L45C			D48-1	
IDT7134L45L			L48	
IDT7134S45P			P48	
IDT7134S45C			D48-1	
IDT7134S45L			L48	
IDT7134L55P	55	—	P48	Com'l.
IDT7134L55C			D48-1	
IDT7134L55L			L48	
IDT7134L55CB			D48-1	Mil.
IDT7134L55LB			L48	
IDT7134S55P			P48	Com'l.
IDT7134S55C			D48-1	
IDT7134S55L			L48	
IDT7134S55CB			D48-1	Mil.
IDT7134S55LB			L48	
IDT7134L70P	70	—	P48	Com'l.
IDT7134L70C			D48-1	
IDT7134L70L			L48	
IDT7134L70CB			D48-1	Mil.
IDT7134L70LB			L48	
IDT7134S70P			P48	Com'l.
IDT7134S70C			D48-1	
IDT7134S70L			L48	
IDT7134S70CB			D48-1	Mil.
IDT7134S70LB			L48	
IDT7134L90P	90	—	P48	Com'l.
IDT7134L90C			D48-1	
IDT7134L90L			L48	
IDT7134L90CB			D48-1	Mil.
IDT7134L90LB			L48	
IDT7134S90P			P48	Com'l.
IDT7134S90C			D48-1	
IDT7134S90L			L48	
IDT7134S90CB			D48-1	Mil.
IDT7134S90LB			L48	
IDT7134L100CB	100	—	D48-1	Mil.
IDT7134L100LB			L48	
IDT7134S100CB			D48-1	
IDT7134S100LB			L48	
IDT71341	Consult Factory			
IDT7140L55P	55	120	P48	Com'l.
IDT7140L55J			J52	
IDT7140L55C			D48-1	
IDT7140L55L			L48, L52	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7140S55P	55	170	P48	Com'l.
IDT7140S55J			J52	
IDT7140S55C			D48-1	
IDT7140S55L			L48, L52	
IDT7140L70P	70	120	P48	Com'l.
IDT7140L70J			J52	
IDT7140L70C			D48-1	
IDT7140L70L			L48, L52	
IDT7140L70CB		180	D48-1	Mil.
IDT7140L70LB			L48, L52	
IDT7140S70P		170	P48	Com'l.
IDT7140S70J			J52	
IDT7140S70C			D48-1	
IDT7140S70L			L48, L52	
IDT7140S70CB		225	D48-1	Mil.
IDT7140S70LB			L48, L52	
IDT7140L90P	90	120	P48	Com'l.
IDT7140L90J			J52	
IDT7140L90C			D48-1	
IDT7140L90L			L48, L52	
IDT7140L90CB		150	D48-1	Mil.
IDT7140L90LB			L48, L52	
IDT7140S90P		170	P48	Com'l.
IDT7140S90J			J52	
IDT7140S90C			D48-1	
IDT7140S90L			L48, L52	
IDT7140S90CB		185	D48-1	Mil.
IDT7140S90LB			L48, L52	
IDT7140L100P	100	120	P48	Com'l.
IDT7140L100J			J52	
IDT7140L100C			D48-1	
IDT7140L100L			L48, L52	
IDT7140L100CB		150	D48-1	Mil.
IDT7140L100LB			L48, L52	
IDT7140S100P		170	P48	Com'l.
IDT7140S100J			J52	
IDT7140S100C			D48-1	
IDT7140S100L			L48, L52	
IDT7140S100CB		185	D48-1	Mil.
IDT7140S100LB			L48, L52	
IDT7140L120CB	120	150	D48-1	Mil.
IDT7140L120LB			L48, L52	
IDT7140S120CB		185	D48-1	
IDT7140S120LB			L48, L52	
IDT7142L55P	55	120	P48	Com'l.
IDT7142L55J			J52	
IDT7142L55C			D48-1	
IDT7142L55L			L48, L52	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7142S55P	55	170	P48	Com'l.
IDT7142S55J			J52	
IDT7142S55C			D48-1	
IDT7142S55L			L48, L52	
IDT7142L70P	70	120	P48	Com'l.
IDT7142L70J			J52	
IDT7142L70C			D48-1	
IDT7142L70L			L48, L52	
IDT7142L70CB		180	D48-1	Mil.
IDT7142L70LB			L48, L52	
IDT7142S70P		170	P48	Com'l.
IDT7142S70J			J52	
IDT7142S70C			D48-1	
IDT7142S70L			L48, L52	
IDT7142S70CB		225	D48-1	Mil.
IDT7142S70LB			L48, L52	
IDT7142L90P	90	120	P48	Com'l.
IDT7142L90J			J52	
IDT7142L90C			D48-1	
IDT7142L90L			L48, L52	
IDT7142L90CB		150	D48-1	Mil.
IDT7142L90LB			L48, L52	
IDT7142S90P		170	P48	Com'l.
IDT7142S90J			J52	
IDT7142S90C			D48-1	
IDT7142S90L			L48, L52	
IDT7142S90CB		185	D48-1	Mil.
IDT7142S90LB			L48, L52	
IDT7142L100P	100	120	P48	Com'l.
IDT7142L100J			J52	
IDT7142L100C			D48-1	
IDT7142L100L			L48, L52	
IDT7142L100CB		150	D48-1	Mil.
IDT7142L100LB			L48, L52	
IDT7142S100P		170	P48	Com'l.
IDT7142S100J			J52	
IDT7142S100C			D48-1	
IDT7142S100L			L48, L52	
IDT7142S100CB		185	D48-1	Mil.
IDT7142S100LB			L48, L52	
IDT7142L120CB	120	150	D48-1	Mil.
IDT7142L120LB			L48, L52	
IDT7142S120CB		185	D48-1	
IDT7142S120LB			L48, L52	
IDT7143L70P	70	—	P68	Com'l.
IDT7143L70XC			D68	
IDT7143L70L			L68	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7143S70P	70	—	P68	Com'l.
IDT7143S70XC			D68	
IDT7143S70L			L68	
IDT7143L90P	90	—	P68	Com'l.
IDT7143L90XC			D68	
IDT7143L90L			L68	
IDT7143L90XCB			D68	Mil.
IDT7143L90LB			L68	
IDT7143S90P			P68	Com'l.
IDT7143S90XC			D68	
IDT7143S90L			L68	
IDT7143S90XCB			D68	Mil.
IDT7143S90LB			L68	
IDT7143L100P	100	—	P68	Com'l.
IDT7143L100XC			D68	
IDT7143L100L			L68	
IDT7143L100XCB			D68	Mil.
IDT7143L100LB			L68	
IDT7143S100P			P68	Com'l.
IDT7143S100XC			D68	
IDT7143S100L			L68	
IDT7143S100XCB			D68	Mil.
IDT7143S100LB			L68	
IDT7143L120XCB	120	—	D68	Mil.
IDT7143L120LB			L68	
IDT7143S120XCB			D68	
IDT7143S120LB			L68	
IDT7164L30P	30	80	P28	Com'l.
IDT7164L30D			D28-1	
IDT7164L30T			D28-2	
IDT7164L30L			L32	
IDT7164S30P		90	P28	
IDT7164S30D			D28-1	
IDT7164S30T			D28-2	
IDT7164S30L			L32	
IDT7164L35P	35	80	P28	Com'l.
IDT7164L35D			D28-1	
IDT7164L35T			D28-2	
IDT7164L35L			L32	
IDT7164L35DB		90	D28-1	Mil.
IDT7164L35TB			D28-2	
IDT7164L35LB			L32	
IDT7164S35P			P28	Com'l.
IDT7164S35D			D28-1	
IDT7164S35T			D28-2	
IDT7164S35L			L32	
IDT7164S35DB		100	D28-1	Mil.
IDT7164S35TB			D28-2	
IDT7164S35LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7164L45P	45	80	P28	Com'l.
IDT7164L45D			D28-1	
IDT7164L45T			D28-2	
IDT7164L45L			L32	
IDT7164L45DB		90	D28-1	Mil.
IDT7164L45TB			D28-2	
IDT7164L45LB			L32	
IDT7164S45P			P28	Com'l.
IDT7164S45D			D28-1	
IDT7164S45T			D28-2	
IDT7164S45L			L32	
IDT7164S45DB		100	D28-1	Mil.
IDT7164S45TB			D28-2	
IDT7164S45LB			L32	
IDT7164L55P	55	80	P28	Com'l.
IDT7164L55D			D28-1	
IDT7164L55T			D28-2	
IDT7164L55L			L32	
IDT7164L55DB		90	D28-1	Mil.
IDT7164L55TB			D28-2	
IDT7164L55LB			L32	
IDT7164S55P			P28	Com'l.
IDT7164S55D			D28-1	
IDT7164S55T			D28-2	
IDT7164S55L			L32	
IDT7164S55DB		100	D28-1	Mil.
IDT7164S55TB			D28-2	
IDT7164S55LB			L32	
IDT7164L70P	70	80	P28	Com'l.
IDT7164L70D			D28-1	
IDT7164L70T			D28-2	
IDT7164L70L			L32	
IDT7164L70DB		90	D28-1	Mil.
IDT7164L70TB			D28-2	
IDT7164L70LB			L32	
IDT7164S70P			P28	Com'l.
IDT7164S70D			D28-1	
IDT7164S70T			D28-2	
IDT7164S70L			L32	
IDT7164S70DB		100	D28-1	Mil.
IDT7164S70TB			D28-2	
IDT7164S70LB			L32	
IDT7164L85DB	85	90	D28-1	Mil.
IDT7164L85TB			D28-2	
IDT7164L85LB			L32	
IDT7164S85DB		100	D28-1	
IDT7164S85TB			D28-2	
IDT7164S85LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7164L100DB	100	90	D28-1	Mil.
IDT7164L100TB			D28-2	
IDT7164L100LB			L32	
IDT7164S100DB		100	D28-1	
IDT7164S100TB			D28-2	
IDT7164S100LB			L32	
IDT7164L120DB	120	90	D28-1	Mil.
IDT7164L120TB			D28-2	
IDT7164L120LB			L32	
IDT7164S120DB		100	D28-1	
IDT7164S120TB			D28-2	
IDT7164S120LB			L32	
IDT7164L150DB	150	90	D28-1	Mil.
IDT7164L150TB			D28-2	
IDT7164L150LB			L32	
IDT7164S150DB		100	D28-1	
IDT7164S150TB			D28-2	
IDT7164S150LB			L32	
IDT7164L200DB	200	90	D28-1	Mil.
IDT7164L200TB			D28-2	
IDT7164L200LB			L32	
IDT7164S200DB		100	D28-1	
IDT7164S200TB			D28-2	
IDT7164S200LB			L32	
IDT7165L30P	30	80	P28	Com'l.
IDT7165L30D			D28-1	
IDT7165L30T			D28-2	
IDT7165L30L			L32	
IDT7165S30P		90	P28	
IDT7165S30D			D28-1	
IDT7165S30T			D28-2	
IDT7165S30L			L32	
IDT7165L35P	35	80	P28	Com'l.
IDT7165L35D			D28-1	
IDT7165L35T			D28-2	
IDT7165L35L			L32	
IDT7165L35DB		90	D28-1	Mil.
IDT7165L35TB			D28-2	
IDT7165L35LB			L32	
IDT7165S35P			P28	Com'l.
IDT7165S35D			D28-1	
IDT7165S35T			D28-2	
IDT7165S35L			L32	
IDT7165S35DB		100	D28-1	Mil.
IDT7165S35TB			D28-2	
IDT7165S35LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7165L45P	45	80	P28	Com'l.
IDT7165L45D			D28-1	
IDT7165L45T			D28-2	
IDT7165L45L			L32	
IDT7165L45DB		90	D28-1	Mil.
IDT7165L45TB			D28-2	
IDT7165L45LB			L32	
IDT7165S45P			P28	Com'l.
IDT7165S45D			D28-1	
IDT7165S45T			D28-2	
IDT7165S45L			L32	
IDT7165S45DB		100	D28-1	Mil.
IDT7165S45TB			D28-2	
IDT7165S45LB			L32	
IDT7165L55P	55	80	P28	Com'l.
IDT7165L55D			D28-1	
IDT7165L55T			D28-2	
IDT7165L55L			L32	
IDT7165L55DB		90	D28-1	Mil.
IDT7165L55TB			D28-2	
IDT7165L55LB			L32	
IDT7165S55P			P28	Com'l.
IDT7165S55D			D28-1	
IDT7165S55T			D28-2	
IDT7165S55L			L32	
IDT7165S55DB		100	D28-1	Mil.
IDT7165S55TB			D28-2	
IDT7165S55LB			L32	
IDT71681LA20P	20	70	P20	Com'l.
IDT71681LA20C			D24-2	
IDT71681LA20L			L28-1	
IDT71681SA20P		90	P20	
IDT71681SA20C			D24-2	
IDT71681SA20L			L28-1	
IDT71681LA25P	25	70	P20	Com'l.
IDT71681LA25C			D24-2	
IDT71681LA25L			L28-1	
IDT71681LA25CB		80	D24-2	Mil.
IDT71681LA25LB			L28-1	
IDT71681SA25P		90	P20	Com'l.
IDT71681SA25C			D24-2	
IDT71681SA25L			L28-1	
IDT71681SA25CB		100	D24-2	Mil.
IDT71681SA25LB			L28-1	
IDT71681LA35P	35	70	P20	Com'l.
IDT71681LA35C			D24-2	
IDT71681LA35L			L28-1	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT71681LA35CB	35	80	D24-2	Mil.
IDT71681LA35LB			L28-1	
IDT71681SA35P		90	P20	Com'l.
IDT71681SA35C			D24-2	
IDT71681SA35L			L28-1	
IDT71681SA35CB		100	D24-2	Mil.
IDT71681SA35LB			L28-1	
IDT71681LA45P	45	70	P20	Com'l.
IDT71681LA45C			D24-2	
IDT71681LA45L			L28-1	
IDT71681LA45CB		80	D24-2	Mil.
IDT71681LA45LB			L28-1	
IDT71681SA45P		90	P20	Com'l.
IDT71681SA45C			D24-2	
IDT71681SA45L			L28-1	
IDT71681SA45CB		100	D24-2	Mil.
IDT71681SA45LB			L28-1	
IDT71681LA55P	55	70	P20	Com'l.
IDT71681LA55C			D24-2	
IDT71681LA55L			L28-1	
IDT71681LA55CB		80	D24-2	Mil.
IDT71681LA55LB			L28-1	
IDT71681SA55P		90	P20	Com'l.
IDT71681SA55C			D24-2	
IDT71681SA55L			L28-1	
IDT71681SA55CB		100	D24-2	Mil.
IDT71681SA55LB			L28-1	
IDT71681LA70CB	70	80	D24-2	Mil.
IDT71681LA70LB			L28-1	
IDT71681SA70CB		100	D24-2	
IDT71681SA70LB			L28-1	
IDT71681LA85CB	85	80	D24-2	Mil.
IDT71681LA85LB			L28-1	
IDT71681SA85CB		100	D24-2	
IDT71681SA85LB			L28-1	
IDT71681LA100CB	100	80	D24-2	Mil.
IDT71681LA100LB			L28-1	
IDT71681SA100CB		100	D24-2	
IDT71681SA100LB			L28-1	
IDT71682LA20P	20	70	P20	Com'l.
IDT71682LA20C			D24-2	
IDT71682LA20L			L28-1	
IDT71682SA20P		90	P20	
IDT71682SA20C			D24-2	
IDT71682SA20L			L28-1	
IDT71682LA25P	25	70	P20	Com'l.
IDT71682LA25C			D24-2	
IDT71682LA25L			L28-1	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT71682LA25CB	25	80	D24-2	Mil.
IDT71682LA25LB			L28-1	
IDT71682SA25P		90	P20	Com'l.
IDT71682SA25C			D24-2	
IDT71682SA25L			L28-1	
IDT71682SA25CB		100	D24-2	Mil.
IDT71682SA25LB			L28-1	
IDT71682LA35P	35	70	P20	Com'l.
IDT71682LA35C			D24-2	
IDT71682LA35L			L28-1	
IDT71682LA35CB		80	D24-2	Mil.
IDT71682LA35LB			L28-1	
IDT71682SA35P		90	P20	Com'l.
IDT71682SA35C			D24-2	
IDT71682SA35L			L28-1	
IDT71682SA35CB		100	D24-2	Mil.
IDT71682SA35LB			L28-1	
IDT71682LA45P	45	70	P20	Com'l.
IDT71682LA45C			D24-2	
IDT71682LA45L			L28-1	
IDT71682LA45CB		80	D24-2	Mil.
IDT71682LA45LB			L28-1	
IDT71682SA45P		90	P20	Com'l.
IDT71682SA45C			D24-2	
IDT71682SA45L			L28-1	
IDT71682SA45CB		100	D24-2	Mil.
IDT71682SA45LB			L28-1	
IDT71682LA55P	55	70	P20	Com'l.
IDT71682LA55C			D24-2	
IDT71682LA55L			L28-1	
IDT71682LA55CB		80	D24-2	Mil.
IDT71682LA55LB			L28-1	
IDT71682SA55P		90	P20	Com'l.
IDT71682SA55C			D24-2	
IDT71682SA55L			L28-1	
IDT71682SA55CB		100	D24-2	Mil.
IDT71682SA55LB			L28-1	
IDT71682LA70CB	70	80	D24-2	Mil.
IDT71682LA70LB			L28-1	
IDT71682SA70CB		100	D24-2	
IDT71682SA70LB			L28-1	
IDT71682LA85CB	85	80	D24-2	Mil.
IDT71682LA85LB			L28-1	
IDT71682SA85CB		100	D24-2	
IDT71682SA85LB			L28-1	
IDT71682LA100CB	100	80	D24-2	Mil.
IDT71682LA100LB			L28-1	
IDT71682SA100CB		100	D24-2	
IDT71682SA100LB			L28-1	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7174L35P	35	100	P28	Com'l.
IDT7174L35D			D28-1	
IDT7174L35T			D28-2	
IDT7174L35L			L32	
IDT7174L35DB		115	D28-1	Mil.
IDT7174L35TB			D28-2	
IDT7174L35LB			L32	
IDT7174S35P		110	P28	Com'l.
IDT7174S35D			D28-1	
IDT7174S35T			D28-2	
IDT7174S35L			L32	
IDT7174S35DB		125	D28-1	Mil.
IDT7174S35TB			D28-2	
IDT7174S35LB			L32	
IDT7174L45P	45	100	P28	Com'l.
IDT7174L45D			D28-1	
IDT7174L45T			D28-2	
IDT7174L45L			L32	
IDT7174L45DB		115	D28-1	Mil.
IDT7174L45TB			D28-2	
IDT7174L45LB			L32	
IDT7174S45P		110	P28	Com'l.
IDT7174S45D			D28-1	
IDT7174S45T			D28-2	
IDT7174S45L			L32	
IDT7174S45DB		125	D28-1	Mil.
IDT7174S45TB			D28-2	
IDT7174S45LB			L32	
IDT7174L55DB	55	115	D28-1	Mil.
IDT7174L55TB			D28-2	
IDT7174L55LB			L32	
IDT7174S55DB		125	D28-1	
IDT7174S55TB			D28-2	
IDT7174S55LB			L32	
IDT7187L25P	25	70	P22	Com'l.
IDT7187L25C			D22	
IDT7187L25L			L22, L28-2	
IDT7187L25CB		85	D22	Mil.
IDT7187L25LB			L22, L28-2	
IDT7187S25P		90	P22	Com'l.
IDT7187S25C			D22	
IDT7187S25L			L22, L28-2	
IDT7187S25CB		105	D22	Mil.
IDT7187S25LB			L22, L28-2	
IDT7187L30P	30	70	P22	Com'l.
IDT7187L30C			D22	
IDT7187L30L			L22, L28-2	
IDT7187L30CB		85	D22	Mil.
IDT7187L30LB			L22, L28-2	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7187S30P	30	90	P22	Com'l.
IDT7187S30C			D22	
IDT7187S30L			L22, L28-2	
IDT7187S30CB		105	D22	Mil.
IDT7187S30LB			L22, L28-2	
IDT7187L35P	35	70	P22	Com'l.
IDT7187L35C			D22	
IDT7187L35L			L22, L28-2	
IDT7187L35CB		85	D22	Mil.
IDT7187L35LB			L22, L28-2	
IDT7187S35P		90	P22	Com'l.
IDT7187S35C			D22	
IDT7187S35L			L22, L28-2	
IDT7187S35CB		105	D22	Mil.
IDT7187S35LB			L22, L28-2	
IDT7187L45P	45	70	P22	Com'l.
IDT7187L45C			D22	
IDT7187L45L			L22, L28-2	
IDT7187L45CB		85	D22	Mil.
IDT7187L45LB			L22, L28-2	
IDT7187S45P		90	P22	Com'l.
IDT7187S45C			D22	
IDT7187S45L			L22, L28-2	
IDT7187S45CB		105	D22	Mil.
IDT7187S45LB			L22, L28-2	
IDT7187L55P	55	70	P22	Com'l.
IDT7187L55C			D22	
IDT7187L55L			L22, L28-2	
IDT7187L55CB		85	D22	Mil.
IDT7187L55LB			L22, L28-2	
IDT7187S55P		90	P22	Com'l.
IDT7187S55C			D22	
IDT7187S55L			L22, L28-2	
IDT7187S55CB		105	D22	Mil.
IDT7187S55LB			L22, L28-2	
IDT7187L70P	70	70	P22	Com'l.
IDT7187L70C			D22	
IDT7187L70L			L22, L28-2	
IDT7187L70CB		85	D22	Mil.
IDT7187L70LB			L22, L28-2	
IDT7187S70P		90	P22	Com'l.
IDT7187S70C			D22	
IDT7187S70L			L22, L28-2	
IDT7187S70CB		105	D22	Mil.
IDT7187S70LB			L22, L28-2	
IDT7187L85P	85	70	P22	Com'l.
IDT7187L85C			D22	
IDT7187L85L			L22, L28-2	
IDT7187L85CB		85	D22	Mil.
IDT7187L85LB			L22, L28-2	

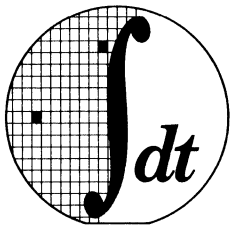
ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7187S85P	85	90	P22	Com'l.
IDT7187S85C			D22	
IDT7187S85L			L22, L28-2	
IDT7187S85CB		105	D22	Mil.
IDT7187S85LB			L22, L28-2	
IDT7188L25P	25	85	P22	Com'l.
IDT7188L25C			D22	
IDT7188S25P		100	P22	
IDT7188S25C			D22	
IDT7188L30P	30	85	P22	Com'l.
IDT7188L30C			D22	
IDT7188L30CB		95	D22	Mil.
IDT7188S30P		100	P22	Com'l.
IDT7188S30C			D22	
IDT7188S30CB		110	D22	Mil.
IDT7188L35P	35	85	P22	Com'l.
IDT7188L35C			D22	
IDT7188L35CB		95	D22	Mil.
IDT7188S35P		100	P22	Com'l.
IDT7188S35C			D22	
IDT7188S35CB		110	D22	Mil.
IDT7188L45P	45	85	P22	Com'l.
IDT7188L45C			D22	
IDT7188L45CB		95	D22	Mil.
IDT7188S45P		100	P22	Com'l.
IDT7188S45C			D22	
IDT7188S45CB		110	D22	Mil.
IDT7188L55P	55	85	P22	Com'l.
IDT7188L55C			D22	
IDT7188L55CB		95	D22	Mil.
IDT7188S55P		100	P22	Com'l.
IDT7188S55C			D22	
IDT7188S55CB		110	D22	Mil.
IDT7188L70P	70	85	P22	Com'l.
IDT7188L70C			D22	
IDT7188L70CB		95	D22	Mil.
IDT7188S70P		100	P22	Com'l.
IDT7188S70C			D22	
IDT7188S70CB		110	D22	Mil.
IDT7188L85CB	85	95	D22	Mil.
IDT7188S85CB		110	D22	
IDT7198L25P	25	85	P24-2	Com'l.
IDT7198L25C			D24-2	
IDT7198L25L			L28-2	
IDT7198S25P		100	P24-2	
IDT7198S25C			D24-2	
IDT7198S25L			L28-2	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7198L30P	30	85	P24-2	Com'l.
IDT7198L30C			D24-2	
IDT7198L30L			L28-2	
IDT7198L30CB		95	D24-2	Mil.
IDT7198L30LB			L28-2	
IDT7198S30P		100	P24-2	Com'l.
IDT7198S30C			D24-2	
IDT7198S30L			L28-2	
IDT7198S30CB		110	D24-2	Mil.
IDT7198S30LB			L28-2	
IDT7198L35P	35	85	P24-2	Com'l.
IDT7198L35C			D24-2	
IDT7198L35L			L28-2	
IDT7198L35CB		95	D24-2	Mil.
IDT7198L35LB			L28-2	
IDT7198S35P		100	P24-2	Com'l.
IDT7198S35C			D24-2	
IDT7198S35L			L28-2	
IDT7198S35CB		110	D24-2	Mil.
IDT7198S35LB			L28-2	
IDT7198L45P	45	85	P24-2	Com'l.
IDT7198L45C			D24-2	
IDT7198L45L			L28-2	
IDT7198L45CB		95	D24-2	Mil.
IDT7198L45LB			L28-2	
IDT7198S45P		100	P24-2	Com'l.
IDT7198S45C			D24-2	
IDT7198S45L			L28-2	
IDT7198S45CB		110	D24-2	Mil.
IDT7198S45LB			L28-2	
IDT7198L55P	55	85	P24-2	Com'l.
IDT7198L55C			D24-2	
IDT7198L55L			L28-2	
IDT7198L55CB		95	D24-2	Mil.
IDT7198L55LB			L28-2	
IDT7198S55P		100	P24-2	Com'l.
IDT7198S55C			D24-2	
IDT7198S55L			L28-2	
IDT7198S55CB		110	D24-2	Mil.
IDT7198S55LB			L28-2	
IDT7198L70P	70	85	P24-2	Com'l.
IDT7198L70C			D24-2	
IDT7198L70L			L28-2	
IDT7198L70CB		95	D24-2	Mil.
IDT7198L70LB			L28-2	
IDT7198S70P		100	P24-2	Com'l.
IDT7198S70C			D24-2	
IDT7198S70L			L28-2	
IDT7198S70CB		110	D24-2	Mil.
IDT7198S70LB			L28-2	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7198L85CB	85	95	D24-2	Mil.
IDT7198L85LB			L28-2	
IDT7198S85CB		110	D24-2	
IDT7198S85LB			L28-2	
IDT71981L25C	25	85	D28-2	Com'l.
IDT71981L25L			L28-2	
IDT71981S25C		100	D28-2	
IDT71981S25L			L28-2	
IDT71981L30C	30	85	D28-2	Com'l.
IDT71981L30L			L28-2	
IDT71981L30CB		95	D28-2	Mil.
IDT71981L30LB			L28-2	
IDT71981S30C		100	D28-2	Com'l.
IDT71981S30L			L28-2	
IDT71981S30CB		110	D28-2	Mil.
IDT71981S30LB			L28-2	
IDT71981L35C	35	85	D28-2	Com'l.
IDT71981L35L			L28-2	
IDT71981L35CB		95	D28-2	Mil.
IDT71981L35LB			L28-2	
IDT71981S35C		100	D28-2	Com'l.
IDT71981S35L			L28-2	
IDT71981S35CB		110	D28-2	Mil.
IDT71981S35LB			L28-2	
IDT71981L45C	45	85	D28-2	Com'l.
IDT71981L45L			L28-2	
IDT71981L45CB		95	D28-2	Mil.
IDT71981L45LB			L28-2	
IDT71981S45C		100	D28-2	Com'l.
IDT71981S45L			L28-2	
IDT71981S45CB		110	D28-2	Mil.
IDT71981S45LB			L28-2	
IDT71981L55C	55	85	D28-2	Com'l.
IDT71981L55L			L28-2	
IDT71981L55CB		95	D28-2	Mil.
IDT71981L55LB			L28-2	
IDT71981S55C		100	D28-2	Com'l.
IDT71981S55L			L28-2	
IDT71981S55CB		110	D28-2	Mil.
IDT71981S55LB			L28-2	
IDT71981L70C	70	85	D28-2	Com'l.
IDT71981L70L			L28-2	
IDT71981L70CB		95	D28-2	Mil.
IDT71981L70LB			L28-2	
IDT71981S70C		100	D28-2	Com'l.
IDT71981S70L			L28-2	
IDT71981S70CB		110	D28-2	Mil.
IDT71981S70LB			L28-2	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT71981L85CB	85	95	D28-2	Mil.
IDT71981L85LB			L28-2	
IDT71981S85CB		110	D28-2	
IDT71981S85LB			L28-2	
IDT71982L25C	25	85	D28-2	Com'l.
IDT71982L25L			L28-2	
IDT71982S25C		100	D28-2	
IDT71982S25L			L28-2	
IDT71982L30C	30	85	D28-2	Com'l.
IDT71982L30L			L28-2	
IDT71982L30CB		95	D28-2	Mil.
IDT71982L30LB			L28-2	
IDT71982S30C		100	D28-2	Com'l.
IDT71982S30L			L28-2	
IDT71982S30CB		110	D28-2	Mil.
IDT71982S30LB			L28-2	
IDT71982L35C	35	85	D28-2	Com'l.
IDT71982L35L			L28-2	
IDT71982L35CB		95	D28-2	Mil.
IDT71982L35LB			L28-2	
IDT71982S35C		100	D28-2	Com'l.
IDT71982S35L			L28-2	
IDT71982S35CB		110	D28-2	Mil.
IDT71982S35LB			L28-2	
IDT71982L45C	45	85	D28-2	Com'l.
IDT71982L45L			L28-2	
IDT71982L45CB		95	D28-2	Mil.
IDT71982L45LB			L28-2	
IDT71982S45C		100	D28-2	Com'l.
IDT71982S45L			L28-2	
IDT71982S45CB		110	D28-2	Mil.
IDT71982S45LB			L28-2	
IDT71982L55C	55	85	D28-2	Com'l.
IDT71982L55L			L28-2	
IDT71982L55CB		95	D28-2	Mil.
IDT71982L55LB			L28-2	
IDT71982S55C		100	D28-2	Com'l.
IDT71982S55L			L28-2	
IDT71982S55CB		110	D28-2	Mil.
IDT71982S55LB			L28-2	
IDT71982L70C	70	85	D28-2	Com'l.
IDT71982L70L			L28-2	
IDT71982L70CB		95	D28-2	Mil.
IDT71982L70LB			L28-2	
IDT71982S70C		100	D28-2	Com'l.
IDT71982S70L			L28-2	
IDT71982S70CB		110	D28-2	Mil.
IDT71982S70LB			L28-2	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT71982L85CB	85	95	D28-2	Mil.
IDT71982L85LB			L28-2	
IDT71982S85CB		110	D28-2	
IDT71982S85LB			L28-2	



Integrated
Device
Technology

Technology/Capabilities

Static RAM

MICROSLICE™

3

Digital Signal Processing (DSP)

Logic

Data Conversion

Subsystems Modules

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Integrated Device Technology, Inc.

FOUR-BIT CMOS MICROPROCESSOR SLICE

IDT39C01C
IDT39C01D
IDT39C01E

MICROSLICE™ PRODUCT

FEATURES:

- Low-power
  - —I_{CC} (max.)
    - Military — 35mA
    - Commercial — 30mA
- Fast
  - —IDT39C01C — meets 2901C speeds
  - —IDT39C01D — 20% speed upgrade
  - —IDT39C01E — 40% speed upgrade
- Eight-function ALU
  - —Performs addition, two subtraction operations and five logic functions on two source operands
- Expandable
  - —Longer word lengths achieved through cascading any number of IDT39C01s
- Four status flags
  - —Carry, overflow, negative and zero
- Pin compatible and functionally equivalent to the 2901A,B,C
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C01Cs are high-speed, cascadable ALUs which can be used to implement CPUs, peripheral controllers and programmable microprocessors. The IDT39C01's microinstruction flexibility allows for easy emulation of most digital computers.

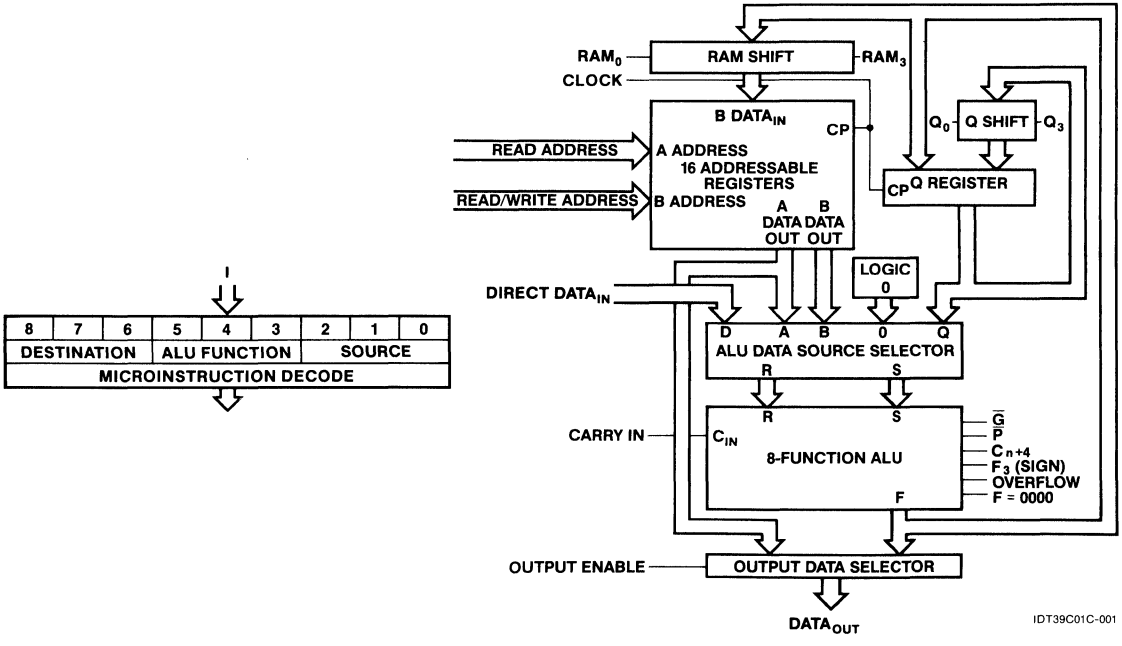
This extremely low-power yet high-speed ALU consists of a 16-word by 4-bit dual-port RAM, a high-speed ALU, and the required shifting, decoding and multiplexing logic. It is expandable in 4-bit increments, contains a flag output along with three-state data outputs, and can easily use either a ripple carry or full lookahead carry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU destination register, ALU source operands and the ALU function.

The IDT39C01C is fabricated using CEMOS™, a single poly, double metal CMOS technology designed for high-performance and high-reliability.

The IDT39C01C is a pin-compatible, performance-enhanced, functional replacement for all versions of the 2901.

3

FUNCTIONAL BLOCK DIAGRAM



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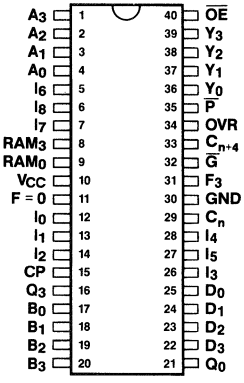
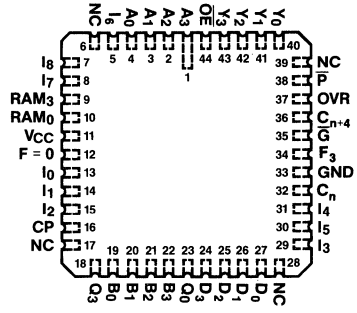


DIP
TOP VIEW

IDT39C01C-002



LCC
TOP VIEW

IDT39C01C-003

FLATPACK
(Consult Factory)

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs to the register file which selects one register and displays its contents through the A-port.
B_0-B_3	I	Four address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B-port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_8	I	Nine instruction control lines which determine what data source will be applied to the ALU $I_{0, 1, 2}$, what function the ALU will perform $I_{3, 4, 5}$, and what data is to be deposited in the Q Register or the register file $I_{6, 7, 8}$.
D_0-D_3	I	Four-bit direct data inputs which are the ALU data source for entering external data into the device. D_0 is the LSB.
Y_0-Y_3	O	Four three-state output lines which, when enabled, display either the four outputs of the ALU or the data on the A-port of the register stack. This is determined by the destination code $I_{6, 7, 8}$.
F_3	O	Most significant ALU output bit (sign-bit).
F=0	O	Open drain output which goes HIGH if the F_0-F_3 ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+4}	O	Carry-out of the internal ALU.
Q_3 RAM_3	I/O	Bidirectional lines controlled by $I_{6, 7, 8}$. Both are three-state output drivers connected to the TTL-compatible CMOS inputs. When the destination code on $I_{6, 7, 8}$ indicates an up shift, the three-state outputs are enabled and the MSB of the Q Register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_3 and RAM_3 lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable which, when pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{G}$,$\overline{P}$	O	Carry generate and carry propagate output of the ALU. These are used to perform a carry-lookahead operation.
OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
CP	I	Clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 16x4 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.

DEVICE ARCHITECTURE:

The IDT39C01 CMOS bit-slice microprocessor is configured four bits wide and is cascadable to any number of bits (4,8,12,16, etc.). Key elements which make up this four-bit-slice microprocessor are: (1) the register file (16x4 dual-port RAM) with shifter, (2) ALU, and (3) Q Register and shifter.

REGISTER FILE—RAM data is read from the A-port as controlled by the 4-bit A address field input. Data, as defined by the B address field input, can be simultaneously read from the B-port of the RAM. This same code can be applied to the A select and B select field with the identical data appearing at both the RAM A-port and B-port outputs simultaneously. New data is written into the file (word) defined by the B address field of the RAM when activated by the RAM write enable. The RAM data input field is driven by a 3-input multiplexer that is used to shift the ALU output data (F). It is capable of shifting the data up one position, down one position, or no shift at all. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins. For a shift up operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. During a shift down operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled. Four-bit latches hold the RAM data while the clock is LOW with the A-port output and B-port output each driving separate latches. The data to be written into the RAM is applied from the ALU F output.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer with both having an inhibit capability. Both multiplexers are controlled by the I_0, I_1, I_2 inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q, and "0" inputs as source operands to the ALU. Microinstruction inputs (I_3, I_4, I_5) are used to select the ALU function. This high-speed ALU also incorporates a carry-in (C_n) input, carry propagate ($\overline{P}$) output, carry generate ($\overline{G}$) output and carry-out (C_{n+4}) all aimed at accelerating arithmetic operations by the use of carry-lookahead logic. The overflow output pin (OVR) will be HIGH when arithmetic operations exceed the two's complement number range. The ALU data outputs (F_0, F_1, F_2, F_3) are routed to the RAM Q Register inputs and the Y outputs under control of the I_6, I_7, I_8 control signal inputs. The MSB of the ALU is output as F_3 so the user can examine the sign-bit without enabling the three-state outputs. An open drain output, F=0, is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so that the user can determine when the ALU output is zero by wire-ORing these outputs together.

Q REGISTER—The Q Register is a separate 4-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_3, which operate comparably to the RAM shifter. They are controlled by the I_6, I_7, I_8 inputs.

The clock input of the IDT39C01 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and RAM EN is enabled, new data will be written into the RAM file defined by the B address field.

3

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R $\vee$ S
AND	H	L	L	4	R AND S	R $\wedge$ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	R $\triangledown$ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

ALU DESTINATION CONTROL

MNEMONIC	MICROCODE				RAM FUNCTION		Q REGISTER FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.

B = Register Addressed by B inputs.

UP is toward MSB; DOWN is toward LSB.

SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL							
		0	1	2	3	4	5	6	7
		ALU SOURCE							
		A,Q	A,B	0,Q	0,B	O,A	D,A	D,Q	D,0
0	C_n = L **R Plus S**	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L **S Minus R**	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	C_n = L **R Minus S**	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	**R OR S**	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	**R AND S**	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ **AND S**	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	**R EX-OR S**	A ∇ Q	A ∇ B	Q	B	A	D ∇ A	D ∇ Q	D
7	**R EX-NOR S**	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	Q	B	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

+ = PLUS; - = MINUS; ∧ = AND; ∇ = EX-OR; ∨ = OR

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$, $I_{2,1,0}$	GROUP	FUNCTION
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \triangledown Q$
6 1		$A \triangledown B$
6 5		$D \triangledown A$
6 6		$D \triangledown Q$
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL	C_n = L		C_n = H	
$I_{5,4,3}$, $I_{2,1,0}$	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

DEFINITIONS

$P_0 = R_0 + S_0$
$P_1 = R_1 + S_1$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$
$G_0 = R_0 S_0$
$G_1 = R_1 S_1$
$G_2 = R_2 S_2$
$G_3 = R_3 S_3$
$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n$
$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$

+ = OR

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, AND OVR

$I_{5,4,3}$	FUNCTION	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3 P_2 P_1 P_0}$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$	C_4	$C_3 \triangledown C_4$
1	S - R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R - S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3 P_2 P_1 P_0$	$\overline{P_3 P_2 P_1 P_0} + C_n$	$\overline{P_3 P_2 P_1 P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ▽ S	← Same as $R \triangledown S$ equations, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \triangledown S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0 (G_0 + C_n)}$	See Note 2

NOTES:
1. + = OR
2. $[\overline{P}_2 + \overline{G}_2 \overline{P}_1 + \overline{G}_2 \overline{G}_1 \overline{P}_0 + \overline{G}_2 \overline{G}_1 \overline{G}_0 C_n] \triangledown [\overline{P}_3 + \overline{G}_3 \overline{P}_2 + \overline{G}_3 \overline{G}_2 \overline{P}_1 + \overline{G}_3 \overline{G}_2 \overline{G}_1 \overline{P}_0 + \overline{G}_3 \overline{G}_2 \overline{G}_1 \overline{G}_0 C_n]$

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(3)	MAX.	UNITS
I_{IH}	Output Short Circuit Current (All Inputs)	V_{CC} = Max. V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input Low Current (All Inputs)	V_{CC} = Max. V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} = or V_{IL}	I_{OH} = -1.0mA (MIL.)	2.4	4.3	—	V
			I_{OH} = -1.6mA (COM'L.)	2.4	4.3	—	
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} = or V_{IL}	I_{OL} = 16mA (MIL.)	—	0.3	0.5	V
			I_{OL} = 20mA (COM'L.)	—	0.3	0.5	
V_{IH}	Input High Voltage	(1)		2.0	—	—	V
V_{IL}	Input Low Voltage	(1)		—	—	0.8	V
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = HIGH Z		-40	—	40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0V(2)		-30	—	-130	mA

NOTES:

1. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test shall not exceed one second.
3. V_{CC} = +5.0V @ T_A +25°C.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.(3)	MAX.	UNITS
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H			—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L			—	—	—	mA
I_{CCT}	Quiescent Input Power Supply(4) Current (per Input @ TTL High)	V_{CC} = Max., V_{IN} = 3.4V, f_{CP} = 0			—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L		MIL.	—	—	—	mA/ MHz
				COM'L.	—	—	—	
I_{CC}	Total Power Supply Current(5)	V_{CC} = Max., Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	IDT39C01C f_{CP} = 10MHz	MIL.	—	—	—	mA
				COM'L.	—	—	—	
			IDT39C01D f_{CP} = 15MHz	MIL	—	—	—	
				COM'L.	—	—	—	
			IDT39C01E f_{CP} = 17.5MHz	MIL.	—	—	—	
				COM'L.	—	—	—	
		V_{CC} = Max., Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IN} = 3.4V, V_{IN} = 0	IDT39C01C f_{CP} = 10MHz	MIL.	—	—	35	
				COM'L.	—	—	30	
			IDT39C01D f_{CP} = 15MHz	MIL.	—	—	40	
				COM'L.	—	—	35	
			IDT39C01E f_{CP} = 17.5MHz	MIL.	—	—	45	
				COM'L.	—	—	40	

NOTES:

4. I_{CCQT} is derived by measuring the total current with all the inputs tied togetherat 3.4V, subtracting I_{CCQH}, then dividing by the total number of inputs.
5. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input Frequency.

3

IDT39C01C
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01C over the -55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10%. All times are in nanoseconds and are measured between the 1.5V signal level. The input switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

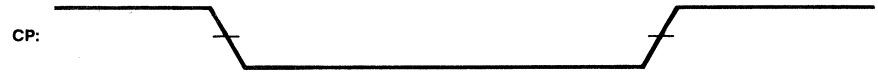
CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	32	31	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=432 or 632)	31	32	MHz
Minimum Clock LOW Time	15	15	ns
Minimum Clock HIGH Time	15	15	ns
Minimum Clock Period	32	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		F_3		C_{n+4}		$\overline{G},\overline{P}$		F=0		OVR		RAM_0 RAM_3		Q_0 Q_3		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Address	48	40	48	40	48	40	44	37	48	40	48	40	48	40	—	—	ns
D	37	30	37	30	37	30	34	30	40	38	37	30	37	30	—	—	ns
C_n	25	22	25	22	21	20	—	—	28	25	25	22	28	25	—	—	ns
$I_{0,1,2}$	40	35	40	35	40	35	44	37	44	37	40	35	40	35	—	—	ns
$I_{3,4,5}$	40	35	40	35	40	35	40	35	40	38	40	35	40	35	—	—	ns
$I_{6,7,8}$	29	25	—	—	—	—	—	—	—	—	—		29	26	29	26	ns
A Bypass ALU (I=2XX)	40	35	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock ⎍	40	35	40	35	40	35	40	35	40	35	40	35	40	35	33	28	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	15	15	2	1[3]	30, 15+TPWL[4]		2	1	ns
B Destination Address	15	15	Do not change[2]				2	1	ns
D	—[1]	—	—	—	25	25	0	0	ns
C_n	—	—	—	—	20	20	0	0	ns
$I_{0,1,2}$	—	—	—	—	30	30	0	0	ns
$I_{3,4,5}$	—	—	—	—	30	30	0	0	ns
$I_{6,7,8}$	10	10	Do not change[2]				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	—	—	—	—	12	12	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L
$\overline{OE}$	Y	25	23	25	23

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.

IDT39C01D
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01D over the -55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10%. All times are in nanoseconds and are measured between the 1.5V signal level. The input switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

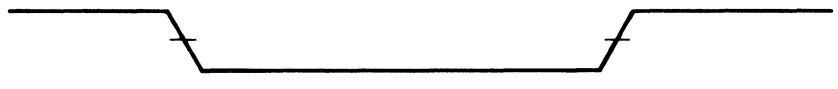
CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	27	23	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=432 or 632)	37	43	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	27	23	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																
	Y		F_3		C_{n+4}		$\overline{G}$,$\overline{P}$		F=0		OVR		RAM_0 RAM_3		Q_0 Q_3		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Address	33	30	33	30	33	30	33	28	33	30	33	30	33	30	—	—	ns
D	24	21	23	20	23	20	21	20	25	24	24	21	25	22	—	—	ns
C_n	18	17	17	16	14	14	—	—	19	18	17	16	19	18	—	—	ns
$I_{0,1,2}$	28	26	27	25	26	24	28	24	29	25	27	24	27	25	—	—	ns
$I_{3,4,5}$	27	26	27	24	26	24	26	24	27	26	26	24	27	26	—	—	ns
$I_{6,7,8}$	18	16	—	—	—	—	—	—	—	—	—		21	21	21	21	ns
A Bypass ALU (I=2XX)	26	24	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock ⎍	27	24	26	23	26	23	25	23	27	24	26	24	27	24	20	19	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	11	10	0	0[3]	24, 11+TPWL[4]	21, 10+TPWL[4]	2	1	ns
B Destination Address	11	10	Do not change[2]				2	1	ns
D	—[1]	—	—	—	16	16	0	0	ns
C_n	—	—	—	—	13	13	0	0	ns
$I_{0,1,2}$	—	—	—	—	19	19	0	0	ns
$I_{3,4,5}$	—	—	—	—	19	19	0	0	ns
$I_{6,7,8}$	7	7	Do not change[2]				0	0	ns
$RAM_{0,3}$,$Q_{0,3}$	—	—	—	—	9	9	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L=5pF, measured to 0.5V change of V_{OUT})

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L
$\overline{OE}$	Y	16	14	18	16

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.

IDT39C01E
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01E over the -55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10%. All times are in nanoseconds and are measured between the 1.5V signal level. The input switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

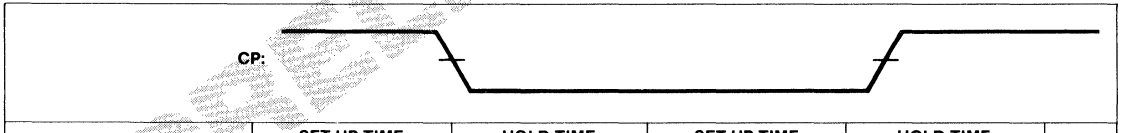
CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	21	20	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=432 or 632)	46	50	MHz
Minimum Clock LOW Time	10	8	ns
Minimum Clock HIGH Time	10	8	ns
Minimum Clock Period	21	20	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		F_3		C_{n+4}		$\overline{G},\overline{P}$		F=0		OVR		RAM_0 RAM_3		Q_0 Q_3		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Address	26	22	26	22	26	22	26	21	26	22	26	22	26	22	—	—	ns
D	18	16	17	15	17	15	16	15	19	18	18	16	19	16	—	—	ns
C_n	13	13	13	12	10	10	—	—	14	13	13	12	14	13	—	—	ns
$I_{0,1,2}$	21	20	20	19	19	18	21	18	22	19	20	18	20	19	—	—	ns
$I_{3,4,5}$	20	20	20	18	19	18	19	18	20	20	19	18	20	20	—	—	ns
$I_{6,7,8}$	13	12	—	—	—	—	—	—	—	—	—		16	16	16	16	ns
A Bypass ALU (I=2XX)	19	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock ⎍	20	18	19	17	19	17	19	17	20	18	19	18	20	18	15	15	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	8	7	0	0[3]	18,8 +TPWL[4]	15, 7 + TPWL[4]	2	1	ns
B Destination Address	8	7	Do not change[2]				2	1	ns
D	—[1]	—	—	—	12	12	0	0	ns
C_n	—	—	—	—	10	10	0	0	ns
$I_{0,1,2}$	—	—	—	—	14	14	0	0	ns
$I_{3,4,5}$	—	—	—	—	14	14	0	0	ns
$I_{6,7,8}$	5	5	Do not change[2]				0	0	ns
$RAM_{0,3}$,$Q_{0,3}$	—	—	—	—	7	7	0	0	ns

OUTPUT ENABLE/DISABLE TIMES
(C_L=5pF, measured to 0.5V change of V_{OUT})

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L
$\overline{OE}$	Y	14	10	12	12

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the H→L transition occurs.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1, 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

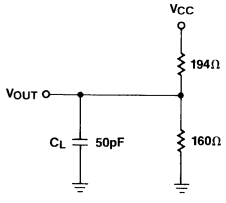


Figure 1. All Outputs (Except f = 0)

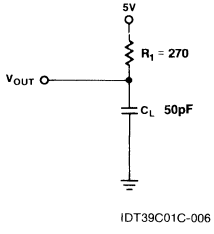


Figure 2. Open Drain Output (f = 0)

INPUT/OUTPUT INTERFACE CIRCUITRY

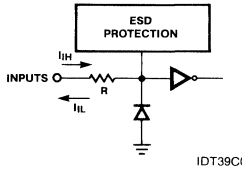


Figure 1. Input Structure (All Inputs)

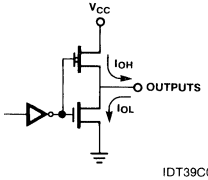


Figure 2. Output Structure (All Outputs Except F = 0)

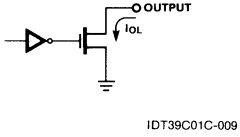


Figure 3. Output Structure (F = 0 Only)

3

Integrated Device Technology, Inc.

CMOS CARRY LOOKAHEAD GENERATOR

IDT39C02A

MICROSLICE™ PRODUCT

FEATURES:

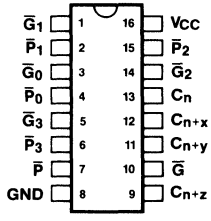
- Provides lookahead carries across any number of 4-bit microprocessor ALUs
- Very high-speed and output drive over full temperature and voltage supply extremes
- 6ns typical propagation delay
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than bipolar (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT39C02A is a high-speed carry lookahead generator built using advanced CEMOS™ II, a dual metal 1.5μm CMOS technology. The IDT39C02A is generally used with an arithmetic logic unit to provide high-speed lookahead over larger word lengths.

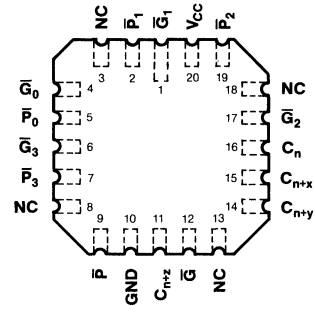
The IDT39C02A is a pin-compatible, performance enhanced, functional replacement for all versions of the 2902.

PIN CONFIGURATIONS



SSDFCT182-001

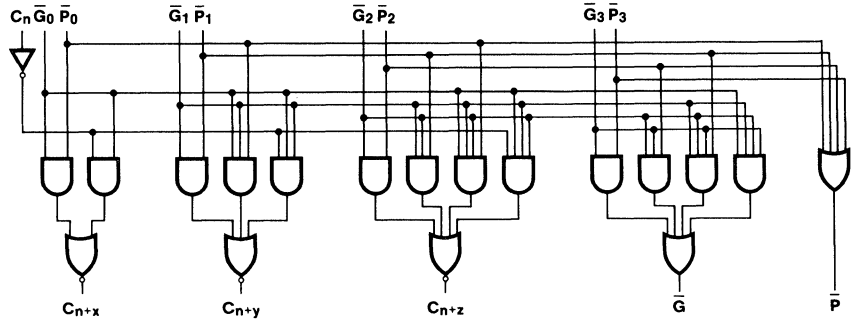
DIP
TOP VIEW



SSDFCT182-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT182-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{CCQC}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN} \leq V_{LC}$ f = 0		—	0.001	2.0	mA
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)	V_{CC} = Max. V_{IN} = 3.4V(4)		—	0.5	2.5	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	0.15	—	mA/ MHz
I_{CC}	Total Power Supply(5) Current	V_{CC} = Max. f = 10 MHz Outputs Open 50% Duty Cycle One Input Toggling	$V_{HC} \leq V_{IN} \leq V_{LC}$	—	1.5	—	mA
			V_{IN} = 3.4V(4)	—	2.0	—	
		All Inputs	V_{IN} = 3.4V(4)	—	16.0	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{CCQC} + (I_{CCQT} \times N_T) + (I_{CCD} \times f \times N) + (I_{CCQT} \times D \times N_D)$
   N = Total number of inputs toggling.
   f = Frequency in MHz.
   D = Percent high duty cycle.
   N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
   N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G_0}$, $\overline{G_1}$, $\overline{G_2}$, $\overline{G_3}$	Carry Generate Inputs (Active LOW)
$\overline{P_0}$, $\overline{P_1}$, $\overline{P_2}$, $\overline{P_3}$	Carry Propagate Inputs (Active LOW)
C_{n+x}–C_{n+z}	Carry Outputs
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+x}	C_{n+y}	C_{n+z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_N to C_{N+X}, C_{N+Y}, C_{N+Z}	C_L = 50 pf R_L = 500Ω	6.0	3.0	14.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_0, P_1, or P_2, to C_{N+X}, C_{N+Y}, C_{N+Z}		6.0	2.0	9.0	2.0	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay G_0, G_1, or G_2, to C_{N+X}, C_{N+Y}, C_{N+Z}		6.0	2.0	9.5	2.0	11.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_1, P_2, or P_3, to G		7.0	3.0	12.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay G_N to G		7.5	3.0	12.0	3.0	16.5	ns
t_{PLH} t_{PHL}	Propagation Delay P_N to P		6.0	2.5	11.0	2.5	12.5	ns

Integrated Device Technology, Inc.

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C03A
IDT39C03B

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - —IDT39C03A matches 2903A speeds
  - —IDT39C03B 20% speed upgrade
- Low-power CMOS
  - —50mA commercial (max.)
  - —60mA (military) (max.)
- Pin-compatible, performance-enhanced functional replacement for the 2903A
- Cascadable to 8, 12, 16, etc. bits
- Expandable Register File
- On-chip Parity Generation and Sign Extension Logic
  - —Provides parity across the entire ALU output and sign extension at any slice boundary
- On-chip Normalization Logic
  - —Floating point mantissa and exponent easily developed using single microcycle per shift
- On-chip Multiplication and Division Logic
  - —Executes unsigned and two's complement multiplication along with last cycle of two's complement multiplication
- Packaged in 48-pin plastic and ceramic DIPs and 52-pin LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C03s are four-bit expandable CMOS microprocessor slices. While executing the identical functions associated with the high-speed IDT39C01 series of 4-bit slices, the IDT39C03s also provide additional enhancements for use in arithmetic-oriented processors.

This extremely low-power yet high-speed microprocessor consists of a 16-word-by-4-bit dual-port RAM, a multidirectional three-port architecture, 16 logic operation ALU and the necessary shifting, decoding and multiplexing logic. Compatible 2903A arithmetic and logic instructions, including the special multiplication, division and normalization instructions, are available on the IDT39C03s. Both are easily expandable in 4-bit increments.

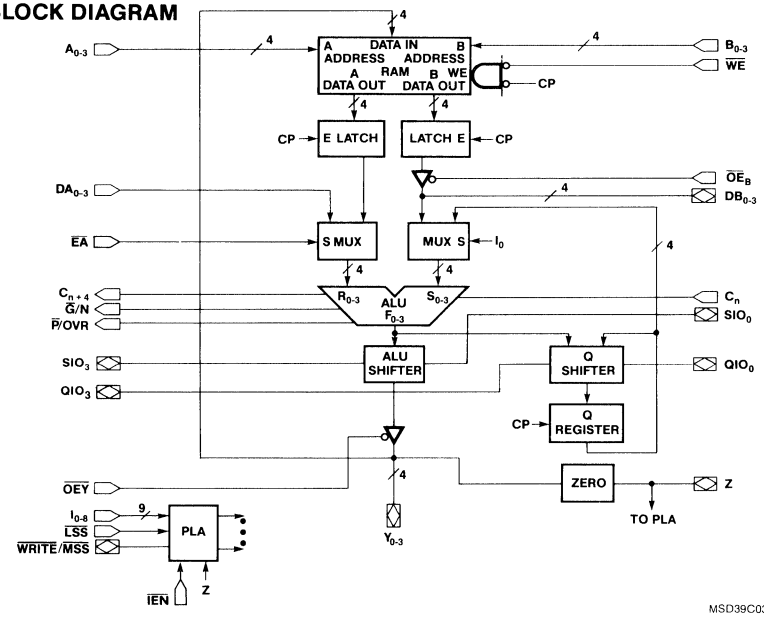
Both devices are pin-compatible, functional-replacements for the 2903A. The fastest version, the IDT39C03B, is a 20% speed upgrade from the normal 2903A device. The IDT39C03A meets the 2903A speeds.

The IDT39C03s are fabricated using CEMOS™, a single poly double metal CMOS technology designed for high-performance and high-reliability.

Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications.

3

FUNCTIONAL BLOCK DIAGRAM



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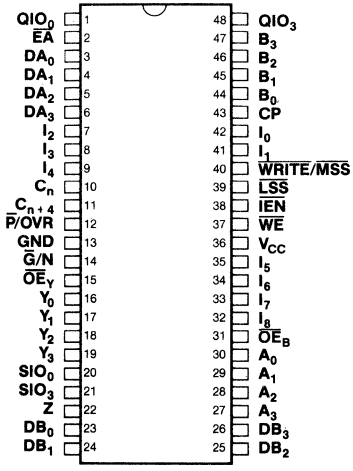
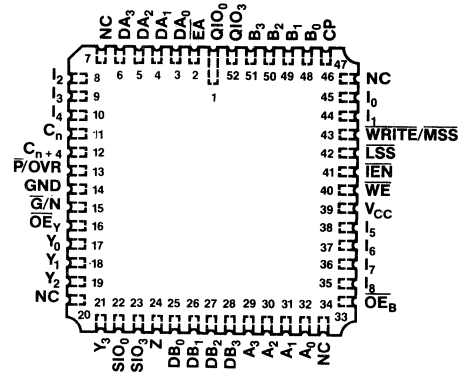
PIN CONFIGURATIONS



MSD39C03-002

DIP
TOP VIEW



MSD39C03-003

LCC
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_{0-3}	I	RAM A Address Inputs (TTL Input) — Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.
B_{0-3}	I	RAM B Address Inputs (TTL Input) — Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.
$\overline{WE}$	I	Write Enable Input (TTL Input) — The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
DA_{0-3}	I	External Data Inputs (TTL Input) — A four-bit external data input which can be selected as one of the IDT39C03 ALU operand sources; DA_0 is the least significant bit.
$\overline{EA}$	I	Control Input (TTL Input) — A control input which, when HIGH, selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
DB_{0-3}	I/O	External Data Inputs/Outputs (Three-State Input/Output) — A four-bit external data input/output. Under control of the $\overline{OE}_B$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.
$\overline{OE}_B$	I	Control Input (TTL Input) — A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.
C_n	I	Carry-In Input (TTL Input) — The carry-in input to the IDT39C03 ALU.
I_{0-8}	I	Instruction Inputs (TTL Input) — The nine instruction inputs used to select the IDT39C03 operation to be performed.
$\overline{IEN}$	I	Instruction Enable Input (TTL Input) — The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the IDT39C03, $\overline{IEN}$ also controls $\overline{WRITE}$.
C_{n+4}	O	Carry-Out Output (TTL Output) — This output generally indicates the carry-out of the IDT39C03 ALU. Refer to Table 5 for an exact definition of this pin.
$\overline{G}/N$	O	Carry-Generate Output (TTL Output) — A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.
$\overline{P}$/OVR	O	Carry-Propagate Output (TTL Output) — A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.
Z	I/O	Open-Drain I/O Pin (Open-Drain Input/Output) — An open-drain input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.
SIO_0, SIO_3	I/O	Bidirectional Serial Shift I/Os for the ALU (Three-State Input/Output) — Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.
QIO_0, QIO_3	I/O	Bidirectional Serial Shift I/Os for the Q Shifter (Three-State Input/Output) — Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of thise pins.
$\overline{LSS}$	I	Control Input (TTL Input) — An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an IDT39C03 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.
$\overline{WRITE}/\overline{MSS}$	I/O	Control Input (Three-State Input/Output) — When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).
Y_{0-3}	I/O	Data Inputs/Outputs (Three-State Input/Output) — Four data inputs/outputs of the IDT39C03. Under control of the $\overline{OE}_Y$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
$\overline{OE}_Y$	I	Control Input (TTL Input) — A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.
CP	I	Clock Input (TTL Input) — The clock input to the IDT39C03. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

ARCHITECTURE OF THE IDT39C03

The IDT39C03s are high-performance, cascadable, 4-bit microprocessor slices used in CPUs, peripheral controllers, microprogrammable machines and in a number of other applications. The functional blocks consist of the following:

—16-word-by-4-bit dual-port RAM
—high-speed ALU and shifter
—Q register with shifter input
—9-bit instruction decoder

DUAL-PORT RAM

Both the A and B ports of the Dual-Port RAM can be addressed and read simultaneously at the respective RAM A and B output ports. If both ports address the same memory location, identical data will be read from both the A and B port. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and holds the RAM output data when CP is LOW. RAM data is read at the DB (I/O) port under control of the $\overline{OE}_B$ three-state output enable.

External data can be written directly into the RAM from the Y I/O port, or the ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

ALU

The IDT39C03s perform seven arithmetic operations and nine logic operations on two 4-bit operands. Various pairs of ALU source operands are easily selected via the ALU multiplexer inputs. The $\overline{EA}$ input selects either the DA external data input or RAM output port A for use as one ALU operand. The $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q register content for use as the second ALU source operand. During certain ALU operations, zeroes are forced at the ALU operand inputs. Thus, the IDT39C03s are capable of operating on data from two external sources, from an internal and external source, or from two internal sources. Table 1 indicates all the possible pairs of ALU source operands as a function of the $\overline{EA}$ $\overline{OE}_B$ and I_0 inputs.

With instruction bits I_4, I_3, I_2, I_1 and I_0 LOW, the IDT39C03s execute special functions which have been defined in Table 4. When the IDT39C03s execute instructions other than the nine special instructions, the ALU operation is defined by instruction bits I_4, I_3, I_2 and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Cascading the IDT39C03s, in either the carry lookahead or ripple carry approach, is very simple. In a cascaded configuration, each slice must be properly programmed to most significant slice (MSS), intermediate slice (IS) or least significant slice (LSS). The IDT39C03s incorporate the carry generate ($\overline{G}$), and carry propagate ($\overline{P}$) signals necessary for cascading.

TABLE 1.
ALU OPERAND SOURCES

$\overline{EA}$	I_0	$\overline{OE}_B$	ALU OPERAND R	ALU OPERAND S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2.
IDT39C03 ALU FUNCTIONS

I_4	I_3	I_2	I_1	HEX CODE	ALU FUNCTIONS
L	L	L	L	0	I_0 = L: Special Functions; I_0 = H: F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n
L	L	H	H	3	F = R Plus S Plus C_n
L	H	L	L	4	F = S Plus C_n
L	H	L	H	5	F = $\overline{S}$ Plus C_n
L	H	H	L	6	F = R Plus C_n
L	H	H	H	7	F = $\overline{R}$ Plus C_n
H	L	L	L	8	F_i = LOW
H	L	L	H	9	F_i = $\overline{R}_i$ AND S_i
H	L	H	L	A	F_i = R_i EXCLUSIVE NOR S_i
H	L	H	H	B	F_i = R_i EXCLUSIVE OR S_i
H	H	L	L	C	F_i = R_i AND S_i
H	H	L	H	D	F_i = R_i NOR S_i
H	H	H	L	E	F_i = R_i NAND S_i
H	H	H	H	F	F_i = R_i OR S_i

L = LOW H = HIGH i = 0 to 3

Also generated is a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. Refer to Table 5 for the exact definition of these four signals.

ALU SHIFTER

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. The arithmetic shift operation shifts data around the most significant (sign) bit position of the MSS and a logical shift operation shifts data through this bit position (see Figure 1). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation SIO_3 is generally a serial shift input and SIO_0 a serial shift output. For exact definition of the SIO_0 and SIO_3 operation, refer to Table 3 and 4.

Also provided in the ALU shifter is sign extension at the slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

Providing ALU error detection, the IDT39C03s ALU shifter contains a cascadable, five-bit parity generator/checker. Parity for the F_0, F_1, F_2, F_3, ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output.

The operation of the ALU shifter is defined by the instruction inputs. Specified in Table 4 are the special functions and the operations the ALU shifter performs. When the IDT39C03s execute instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6 and I_5. How these four bits operate with the ALU shifter is defined in Table 3.

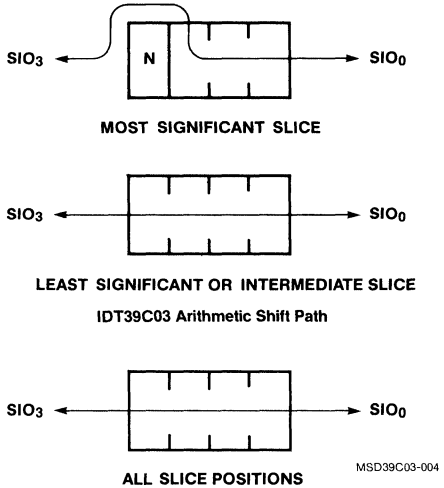


Figure 1.

Q REGISTER

The Q register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The F output of the ALU can be loaded into the Q register and/or the Q register can be selected as the source for the ALU S operand. The shifter at the input to the Q register can shift the Q register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. Both QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

The IDT39C03s provide the capability of double-length arithmetic and logical shifting. To perform the double-length shift, QIO_3 of the MSS is connected to SIO_0 of the LSS, and executing an instruction which shifts both the ALU output and the Q register.

The instruction inputs also control the Q register and shifter, as shown in Table 4. When executing instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5, as shown in Table 3.

OUTPUT BUFFERS

Both the DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE}_Y$ input is LOW and are in the high Z state when $\overline{OE}_Y$ is HIGH. The DB output buffers are enabled when the $\overline{OE}_B$ input is LOW. The zero, Z pin is an open drain I/O that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. Table 5 defines the exact signal functions.

INSTRUCTION DECODER

The Instruction Decoder generates the required internal control signals relative to the nine instruction inputs, I_{0-8}, the instruction Enable input, $\overline{IEN}$, the $\overline{LSS}$ input, and the $\overline{WRITE}$/$\overline{MSS}$ input/output.

When an instruction which writes data into the RAM is being performed, the $\overline{WRITE}$ output is LOW. Reference Table 3 and 4 for proper pin operation. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q register and Sign Compare Flip-Flop can be written according to the IDT39C03s instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation. See Figure 2.

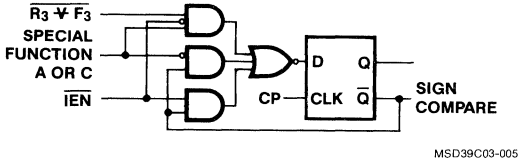


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

When the $\overline{LSS}$ input is LOW, the device becomes the least significant slice and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When the $\overline{LSS}$ input is HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input which when HIGH programs the slice to operate as an intermediate slice (IS). Connecting it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{WRITE}/\overline{MSS}$ pin must be tied HIGH via a pull-up resistor. $\overline{WRITE}/\overline{MSS}$ and $\overline{LSS}$ should not be connected together.

SPECIAL FUNCTIONS

Nine special functions are provided on the IDT39C03s which make possible the implementation of the following operations:

- Single and Double Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Adjusting a single-precision or double-precision floating point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations. Three special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient).

The unsigned multiply special function and the two two's

complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude-two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special function.

TABLE 3.
ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	HEX CODE	ALU SHIFTER FUNCTION	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{WRITE}$	Q REG & SHIFTER FUNCTION	QIO_3	QIO_0
			MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES							
L L L L	0	Arith. F/2 → Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L L L H	1	Log. F/2 → Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L L H L	2	Arith. F/2 → Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/ 2 → Q	Input	Q_0
L L H H	3	Log. F/2 → Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/ 2 → Q	Input	Q_0
L H L L	4	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Z	Z
L H L H	5	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/ 2 → Q	Input	Q_0
L H H L	6	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F → Q	Z	Z
L H H H	7	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F → Q	Z	Z
H L L L	8	Arith. 2F → Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H L L H	9	Log. 2F → Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H L H L	A	Arith. 2F → Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q → Q	Q_3	Input
H L H H	B	Log. 2F → Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q → Q	Q_3	Input
H H L L	C	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Hold	Z	Z
H H L H	D	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Log. 2Q → Q	Q_3	Input
H H H L	E	SIO_0 → Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Z	Z
H H H H	F	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	L	Hold	Z	Z

Parity = $F_3 \nabla F_2 \nabla F_1 \nabla F_0 \nabla SIO_3$ L = LOW Z = High-Impedance
∇ = Exclusive OR H = HIGH

TABLE 4.
SPECIAL FUNCTIONS FOR $I_4 = I_3 = I_2 = I_1 = I_0$ = LOW (Note 4)

(HEX) $I_{8,7,6,5}$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_3		SIO_0	Q REG & SHIFTER FUNCTION	QIO_3	QIO_0	$\overline{WRITE}$
				MOST SIG. SLICE	OTHER SLICES					
0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log F/2 → Y (Note 1)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	(Note 5)									
2	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
3	(Note 5)									
4	Increment by One or Two	$F = S + 1 + C_n$	F → Y	Input	Input	Parity	Hold	Z	Z	L
5	Sign/Magnitude Two's Complement	$F = \overline{S} + C_n$ if $Z = L$ $F = \overline{S} + C_n$ if $Z = H$	F → Y (Note 3)	Input	Input	Parity	Hold	Z	Z	L
6	Two's Complement Multiply. Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
7	(Note 5)									
8	Single Length Normalize	$F = S + C_n$	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
9	(Note 5)									
A	Double Length Normalize and First Divide Op	$F = S + C_n$	Log 2F → Y	$R_3 \nabla F_3$	F_3	Input	Log 2Q → Q	Q_3	Input	L
B	(Note 5)									
C	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log 2F → Y	$\overline{R_3 \nabla F_3}$	F_3	Input	Log 2Q → Q	Q_3	Input	L
D	(Note 5)									
E	Two's Complement Divide Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
F	(Note 5)									

NOTES:

1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \nabla$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \nabla F_3$ is generated at the Y_3 output.
4. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
5. Not valid.

L = LOW
H = HIGH
X = Don't Care
Z = High-Impedance
∇ = Exclusive OR
Parity = $SIO_3 \nabla F_3 \nabla F_2 \nabla F_1 \nabla F_0$

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TABLE 5. IDT39C03A STATUS OUTPUTS

						$\overline{P}$/OVR		$\overline{G}$/N		Z($\overline{OE}_Y$ = LOW)		
(HEX) I_{8-5}	(HEX) I_{4-1}	I_0	G_i (i = 0 to 3)	P_i (i = 0 to 3)	C_{n+4}	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	INTER-MEDIATE SLICE	LEAST SIG. SLICE
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$R_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	(Note 6)	—	—	—	—	—	—	—	—	—
1	8	L	(Note 6)	—	—	—	—	—	—	—	—	—
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)	—	—	—	—	—	—	—	—	—
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z = L $\overline{S}_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \nabla S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R}_i \wedge S_i$ if Z = H	S_i if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	(Note 6)									
8	0	L	0	S_i	(Note 3)	$Q_2 \nabla Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	(Note 6)	—	—	—	—	—	—	—	—	—
9	8	L	(Note 6)	—	—	—	—	—	—	—	—	—
A	0	L	0	S_i	(Note 4)	$F_2 \nabla F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	(Note 6)	—	—	—	—	—	—	—	—	—
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	(Note 6)	—	—	—	—	—	—	—	—	—
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	(Note 6)	—	—	—	—	—	—	—	—	—

NOTES:

1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q_3 \nabla Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \nabla F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$.
6. Not valid.

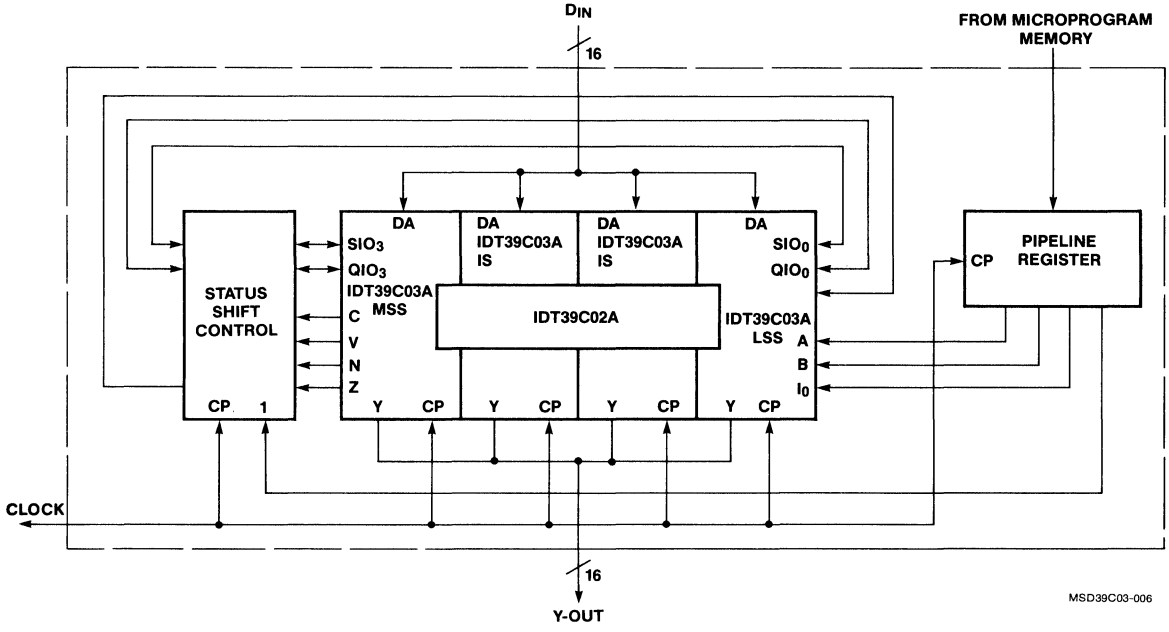
L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
∇ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

Shown below is a circuit diagram for a 16-bit application using four IDT39C03s, one IDT39C02 and a status shift control device. This application has four key speed paths which are defined below:

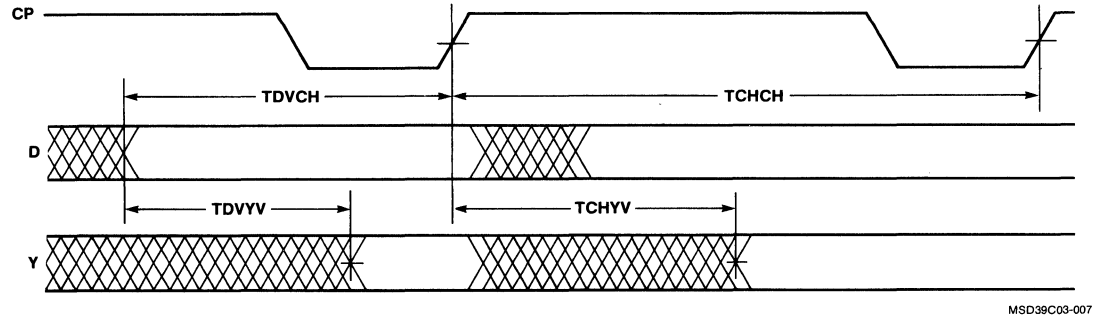
1. **Microcycle Time (TCHCH)**
   Minimum elapsed time between a LOW-to-HIGH clock transition and the next LOW-to-HIGH clock transition.
2. **Data Setup Time (TDVCH)**
   Minimum allowable time between valid data on the D inputs and the clock LOW-to-HIGH transition.
3. **D to Y (TDVYV)**
   Maximum time needed to receive valid Y output data after the D inputs are valid.
4. **CP to Y (TCHYV)**
   Maximum time required to obtain valid Y outputs after a clock LOW-to-HIGH transition.

TIME IN NANOSECONDS OVER COMMERCIAL OPERATING RANGE

CYCLE	TCHCH		TDVCH		TDVYV		TCHYV	
	A	B	A	B	A	B	A	B
Logic	99	—	79	—	59	—	81	—
Logic Rotate	118	—	99	—	79	—	98	—
Arithmetic	130	—	109	—	91	—	112	—
Multiply	152	—	113	—	95	—	135	—
Divide	139	—	113	—	95	—	121	—



TIMING WAVEFORM FOR $DATA_{IN}$, CLOCK AND Y OUTPUT



ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25° C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-130	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0	MIL.	—	25	60	
			COM'L.	—	25	50	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input frequency.

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IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 6. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	15ns

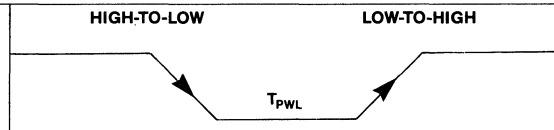
TABLE 7. ENABLE/DISABLE TIMES ALL FUNCTIONS

FROM	TO	ENABLE	DISABLE
$\overline{OE_Y}$	Y	25	21
$\overline{OE_B}$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	38
$\overline{LSS}$	$\overline{WR}$	25	21

NOTE:

C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 8. SETUP AND HOLD TIMES ALL FUNCTIONS



From	With Respect To	Setup	Hold	Setup	Hold	Comments
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	—	20	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	24			0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	—	32	0	Write into Q(2)

NOTES:

1. The internal Y-bus to RAM setup condition will be met 5ns after valid Y output ($\overline{OE_Y}$ = 0).
2. The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.
3. For all other setup conditions not specified in this table, the setup time should be the delay to stable Y output plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this setup condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{WE}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The setup time prior to the clock LOW-TO-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual setup time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the setup time prior to clock L → H and (2) the sum of the setup time prior to clock H → L and the clock LOW time.

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

FROM	TO											
	Y	C_{n+4}	G, P	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	67	55	52	74	61	67	28	—	—	41	62	78
DA, DB	58	50	40	65	54	58	—	—	—	35	59	65
Cn	33	18	—	35	28	26	—	—	—	23	30	38
I_{8-0}	64	64	50	72	61	62	—	34	26*	50*	62*	74*
CP	58	42	43	61	54	58	22	—	22	37	54	60
SIO_0, SIO_3	23	—	—	29	—	—	—	—	—	—	29	19
$\overline{MSS}$	44	—	44	44	44	44	—	—	—	44	44	44
Y	—	—	—	17	—	—	—	—	—	—	—	—
$\overline{IEN}$	—	—	—	—	—	—	—	20	—	—	—	—
$\overline{EA}$	58	50	40	65	54	58	—	—	—	35	59	65

NOTES:

1. A "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

Standard Functions: See Table 2 Increment SF 4: F = S + 1 + Cn

MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\bar{G}, \bar{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	67	@	—	—	@	@	@	—	—	@
	IS	@	@	@	—	—	—	@	—	—	@
	LSS	@	@	@	—	—	—	@	—	—	@
DA, DB	MSS	58	@	—	—	@	@	—	—	—	@
	IS	@	@	@	—	—	—	—	—	—	@
	LSS	@	@	@	—	—	—	—	—	—	@
C_n	MSS	35	@	—	—	@	@	—	—	—	@
	IS	@	@	—	—	—	—	—	—	—	@
	LSS	@	@	—	—	—	—	—	—	—	@
I_{8-0}	MSS	94	75	—	—	88	88	—	—	@	73*
	IS	94	75	71	—	—	—	—	—	@	73*
	LSS	94	75	71	30	—	—	—	@	@	73*
CP	MSS	58	@	—	—	@	@	@	—	@	@
	IS	@	@	@	—	—	—	@	—	@	@
	LSS	90	71	67	26	—	—	@	—	@	69
Z	MSS	64	45	—	—	58	58	—	—	—	43
	IS	64	45	41	—	—	—	—	—	—	43
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

Unsigned Multiply
SF 0: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply
SF 2: F = S + Cn if Z = 0
F = R + S + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle
SF 6: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = OVR \oplus$ (MSS)
$Z = Q_0$ (LSS)

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SF A/SF C, SF E)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	@	72/@	—	78/—	68	67	@	—	—	71
	IS	@	@	@	@/—	—	—	@	—	—	@
	LSS	@	@	@	@/—	—	—	@	—	—	@
DA, DB	MSS	@	66/@	—	66/—	55	58	—	—	—	61
	IS	@	@	@	@/—	—	—	—	—	—	@
	LSS	@	@	@	@/—	—	—	—	—	—	@
C_n	MSS	@	37/@	—	41/—	31	29	—	—	—	36
	IS	@	@	—	@/—	—	—	—	—	—	@
	LSS	@	@	—	@/—	—	—	—	—	—	@
I_{8-0}	MSS	72/96	89/79	—	80/33	71/91	69/91	—	—	@	76/98*
	IS	72/96	69/79	56/79	80/—	—	—	—	—	@	75/98*
	LSS	72/96	69/79	56/79	80/—	—	—	—	@	@	75/98*
CP	MSS	@/91	51/74	—	67/28	55/74	58/74	@	—	@	61/93
	IS	@	@	@	@/—	—	—	@	—	@	@
	LSS	@	@	@	@/—	—	—	@	—	@	@
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—/63	—/46	—/46	—	—	—	—	—	—	—/65
	LSS	—/63	—/46	—/46	—	—	—	—	—	—	—/65
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op
SF A: F = S + Cn
Y = Log. 2F
Q = Log. 2Q
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = \overline{F_2} \oplus F_1$ (MSS)
$Z = \overline{Q_0}\overline{Q_1}\overline{Q_2}\overline{Q_3}\overline{F_0}\overline{F_1}\overline{F_2}\overline{F_3}$

Two's Complement Divide
SF C: F = R + S + Cn if Z = 0
F = S - R -1 + Cn if Z = 1
Y = Log. 2F
Q = $\underline{\text{Log. 2Q}}$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder
SF E: F = R + S + Cn if Z = 0
F = S - R - 1 + Cn if Z = 1
Y = F
Q = $\underline{\text{Log. 2Q}}$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	97	81	—	42	89	89	@	—	—	102
	IS	@	@	@	—	—	—	@	—	—	@
	LSS	@	@	@	—	—	—	@	—	—	@
DA, DB	MSS	94	76	—	37	84	84	—	—	—	97
	IS	@	@	@	—	—	—	—	—	—	@
	LSS	@	@	@	—	—	—	—	—	—	@
C_n	MSS	33	@	—	—	32	27	—	—	—	@
	IS	@	@	—	—	—	—	—	—	—	@
	LSS	@	@	—	—	—	—	—	—	—	@
I_{8-0}	MSS	85	67	—	28	82	73	—	—	@	88*
	IS	85	67	63	—	—	—	—	—	@	88*
	LSS	85	67	63	—	—	—	—	@	@	88*
CP	MSS	94	76	—	37	84	84	@	—	@	97
	IS	@	@	@	—	—	—	@	—	@	@
	LSS	@	@	@	—	—	—	@	—	@	@
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	57	39	35	—	—	—	—	—	—	60
	LSS	57	39	35	—	—	—	—	—	—	60
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 5: F = S + Cn if Z = 0
F = $\overline{S}$ + Cn if Z = 1

$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)

Q = Q
$N = F_3$ if Z = 0
$N = F_3 \oplus S_3$ if Z = 1

3

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF 8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	@	—	—	—	—	—	@	—	—	@
	IS	@	@	@	—	—	—	@	—	—	@
	LSS	@	@	@	—	—	—	@	—	—	@
DA, DB	MSS	@	—	—	—	—	—	—	—	—	@
	IS	@	@	@	—	—	—	—	—	—	@
	LSS	@	@	@	—	—	—	—	—	—	@
C_n	MSS	@	—	—	—	—	—	—	—	—	@
	IS	@	@	—	—	—	—	—	—	—	@
	LSS	@	@	—	—	—	—	—	—	—	@
I_{8-0}	MSS	64	37	—	29	24	24	—	—	@	62*
	IS	64	64	50	29	—	—	—	—	@	62*
	LSS	64	64	50	29	—	—	—	@	@	62*
CK	MSS	@	29	—	26	26	29	@	—	@	@
	IS	@	@	@	26	—	—	@	—	@	@
	LSS	@	@	@	26	—	—	@	—	@	@
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 8: $F = S + Cn$
$N = Q_3$ (MSS)
$Y = F$
Q = LOG. $2Q$

$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$

$OVR = Q_2 \oplus Q_1$ (MSS)

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the military operating range of -55°C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 9. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

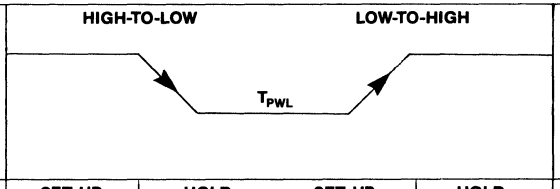
Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	30ns

TABLE 10. ENABLE/DISABLE TIMES ALL FUNCTIONS

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WR}$	30	25

NOTE:
C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 11. SETUP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	—	20	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	24			0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	—	32	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM setup condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0).
2. The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.
3. For all other setup conditions not specified in this table, the setup time should be the delay to stable Y output plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this setup condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the WRITE/MSS output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The setup time prior to the clock LOW-TO-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual setup time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the setup time prior to clock L → H and (2) the sum of the setup time prior to clock H → L and the clock LOW time.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	70	58	52	78	68	67	28	—	—	47	71	84
DA, DB	60	52	40	66	55	58	—	—	—	35	61	74
Cn	35	19	—	41	31	29	—	—	—	23	33	40
I_{8-0}	72	69	56	80	71	69	—	36	26*	58*	75*	89*
CP	60	42	43	67	55	58	22	—	25	41	61	66
SIO_0, SIO_3	26	—	—	29	—	—	—	—	—	—	29	19
$\overline{MSS}$	44	—	44	44	44	44	—	—	—	44	44	44
Y	—	—	—	17	—	—	—	—	—	—	—	—
$\overline{IEN}$	—	—	—	—	—	—	—	20	—	—	—	—
$\overline{EA}$	60	52	40	66	55	58	—	—	—	35	61	74

NOTES:

1. A "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

Standard Functions: See Table 2 Increment SF 4: F = S + 1 + Cn

MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	72	@	—	—	@	@	@	—	—	@
	IS	@	@	@	—	—	—	@	—	—	@
	LSS	@	@	@	—	—	—	@	—	—	@
DA, DB	MSS	62	@	—	—	@	@	—	—	—	@
	IS	@	@	@	—	—	—	—	—	—	@
	LSS	@	@	@	—	—	—	—	—	—	@
C_n	MSS	40	@	—	—	@	@	—	—	—	@
	IS	@	@	—	—	—	—	—	—	—	@
	LSS	@	@	—	—	—	—	—	—	—	@
I_{8-0}	MSS	108	84	—	—	98	98	—	—	@	81*
	IS	108	84	80	—	—	—	—	—	@	81*
	LSS	108	84	80	33	—	—	—	@	@	81*
CP	MSS	62	@	—	—	@	@	@	—	@	@
	IS	@	@	@	—	—	—	@	—	@	@
	LSS	104	80	74	29	—	—	@	—	@	77
Z	MSS	75	51	—	—	65	65	—	—	—	48
	IS	75	51	47	—	—	—	—	—	—	48
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

Unsigned Multiply
SF 0: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply
SF 2: F = S + Cn if Z = 0
F = R + S + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle
SF 6: F = S + Cn if Z = 0
F = S - R - 1 + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = OVR \oplus F_3$ (MSS)
$Z = Q_0$ (LSS)

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SF A/SF C, SF E)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	@	72/@	—	78/—	68	67	@	—	—	71
	IS	@	@	@	@/—	—	—	@	—	—	@
	LSS	@	@	@	@/—	—	—	@	—	—	@
DA, DB	MSS	@	66/@	—	66/—	55	58	—	—	—	61
	IS	@	@	@	@/—	—	—	—	—	—	@
	LSS	@	@	@	@/—	—	—	—	—	—	@
C_n	MSS	@	37/@	—	41/—	31	29	—	—	—	36
	IS	@	@	—	@/—	—	—	—	—	—	@
	LSS	@	@	—	@/—	—	—	—	—	—	@
I_{8-0}	MSS	72/96	89/79	—	80/33	71/91	69/91	—	—	@	76/98*
	IS	72/96	69/79	56/79	80/—	—	—	—	—	@	75/98*
	LSS	72/96	69/79	56/79	80/—	—	—	—	@	@	75/98*
CP	MSS	@/91	51/74	—	67/28	55/74	58/74	@	—	@	61/93
	IS	@	@	@	@/—	—	—	@	—	@	@
	LSS	@	@	@	@/—	—	—	@	—	@	@
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—/63	—/46	—/46	—	—	—	—	—	—	—/65
	LSS	—/63	—/46	—/46	—	—	—	—	—	—	—/65
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op
SF A: F = S + Cn
Y = Log. 2F
Q = Log. 2Q
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

Two's Complement Divide
SF C: F = R + S + Cn if Z = 0
F = S − R −1 + Cn if Z = 1
Y = Log. 2F
Q = Log. 2Q
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder
SF E: F = R + S + Cn if Z = 0
F = S − R − 1 + Cn if Z = 1
Y = F
Q = Log. 2Q
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	114	95	-	49	106	106	@	—	—	125
	IS	@	@	@	—	—	—	@	—	—	@
	LSS	@	@	@	—	—	—	@	—	—	@
DA, DB	MSS	108	89	—	43	101	101	—	—	—	119
	IS	@	@	@	—	—	—	—	—	—	@
	LSS	@	@	@	—	—	—	—	—	—	@
C_n	MSS	36	@	—	—	35	29	—	—	—	@
	IS	@	@	—	—	—	—	—	—	—	@
	LSS	@	@	—	—	—	—	—	—	—	@
I_{8-0}	MSS	98	79	—	33	97	88	—	—	@	109*
	IS	98	79	73	—	—	—	—	—	@	109*
	LSS	98	79	73	—	—	—	—	@	@	109*
CP	MSS	108	89	—	43	101	101	@	—	@	119
	IS	@	@	@	—	—	—	@	—	@	@
	LSS	@	@	@	—	—	—	@	—	@	@
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	65	46	40	—	—	—	—	—	—	76
	LSS	65	46	40	—	—	—	—	—	—	76
EN											
SIO_0, SIO_3	Any	-	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 5: F = S + Cn if Z = 0
F = S + Cn if Z = 1

$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)
Y = F

Q = Q
$N = F_3$ if Z = 0
$N = F_3 \oplus S_3$ if Z = 1

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF 8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\bar{G}, \bar{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	@	—	—	—	—	—	@	—	—	@
	IS	@	@	@	—	—	—	@	—	—	@
	LSS	@	@	@	—	—	—	@	—	—	@
DA, DB	MSS	@	—	—	—	—	—	—	—	—	@
	IS	@	@	@	—	—	—	—	—	—	@
	LSS	@	@	@	—	—	—	—	—	—	@
C_n	MSS	@	—	—	—	—	—	—	—	—	@
	IS	@	@	—	—	—	—	—	—	—	@
	LSS	@	@	—	—	—	—	—	—	—	@
I_{8-0}	MSS	72	47	—	33	27	27	—	—	@	75*
	IS	72	69	56	33	—	—	—	—	@	75*
	LSS	72	69	56	33	—	—	—	@	@	75*
CK	MSS	@	31	—	28	26	31	@	—	@	@
	IS	@	@	@	28	—	—	@	—	@	@
	LSS	@	@	@	28	—	—	@	—	@	@
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	@	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 8: $F = S + Cn$
$N = Q_3$ (MSS)
$Y = F$
$Q = LOG.\ 2Q$

$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$Z = \bar{Q}_0\bar{Q}_1\bar{Q}_2\bar{Q}_3$

$OVR = Q_2 \oplus Q_1$ (MSS)

3

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 12. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	—
Minimum Clock High Time	—
Minimum Time CP and $\overline{WE}$ both Low to Write	—

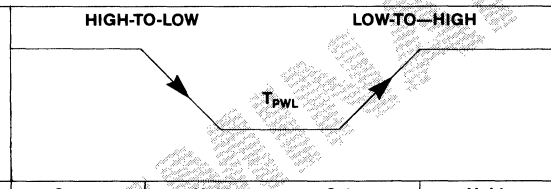
TABLE 13. ENABLE/DISABLE TIMES ALL FUNCTIONS

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	—	—
$\overline{OE}_B$	DB	—	—
$\overline{EA}$	DA	—	—
I_8	SIO	—	—
I_8	QIO	—	—
$I_{8,7,6,5}$	QIO	—	—
$I_{4,3,2,1,0}$	QIO	—	—
$\overline{LSS}$	$\overline{WR}$	—	—

NOTE:

C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 14. SETUP AND HOLD TIMES ALL FUNCTIONS



From	With Respect To	Setup	Hold	Setup	Hold	Comments
Y	CP	—	—	—	—	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	—	—		—	Prevent Writing
$\overline{WE}$ LOW	CP	—	—	—	—	Write into RAM
A, B Source	CP	—	—	—	—	Latch Data from RAM Out
B Destination	CP	—	—		—	Write Data into B Address
$QIO_{0,3}$	CP	—	—	—	—	Shift Q
$I_{8,7,6,5}$	CP	—	—	—	—	Write into Q(2)
$\overline{IEN}$ HIGH	CP	—	—	—	—	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	—	—	—	—	Write into Q
$I_{4,3,2,1,0}$	CP	—	—	—	—	Write into Q(2)

NOTES:

1. The internal Y-bus to RAM setup condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0).
2. The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.
3. For all other setup conditions not specified in this table, the setup time should be the delay to stable Y output plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this setup condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{WE}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The setup time prior to the clock LOW-TO-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual setup time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the setup time prior to clock L → H and (2) the sum of the setup time prior to clock H → L and the clock LOW time.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

FROM	TO											
	Y	C_{n+4}	G, P	Z	N	OVR	DB	$\overline{WRITE}$/ $\overline{MSS}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	—	—	—	—	—	—	—	—	—	—	—	—
DA, DB	—	—	—	—	—	—	—	—	—	—	—	—
Cn	—	—	—	—	—	—	—	—	—	—	—	—
I_{8-0}	—	—	—	—	—	—	—	—	—	—	—	—
CP	—	—	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	—	—	—	—	—	—	—	—	—	—	—	—
$\overline{MSS}$	—	—	—	—	—	—	—	—	—	—	—	—
Y	—	—	—	—	—	—	—	—	—	—	—	—
$\overline{IEN}$	—	—	—	—	—	—	—	—	—	—	—	—
$\overline{EA}$	—	—	—	—	—	—	—	—	—	—	—	—

NOTES:

1. A "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

Standard Functions: See Table 2 Increment SF 4: F = S + 1 + Cn

MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$/ $\overline{MSS}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Cn	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CP	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

Unsigned Multiply
SF 0: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = C_{n+4}$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply
SF 2: F = S + Cn if Z = 0
F = R + S + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle
SF 6: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
Y_3 = OVR ⊕ (MSS)
$Z = Q_0$ (LSS)

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SF A/SF C, SF E)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CP	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op
SF A: $F = S + Cn$
$Y = \text{Log. } 2F$
$Q = \text{Log. } 2Q$
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$

Two's Complement Divide
SF C: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
$Y = \text{Log. } 2F$
$Q = \underline{\text{Log. } 2Q}$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder
SF E: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 - Cn$ if $Z = 1$
$Y = F$
$Q = \underline{\text{Log. } 2Q}$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CP	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 5: F = S + Cn if Z = 0
F = $\overline{S}$ + Cn if Z = 1

$Y_3 = S_3 \oplus F_3$ (MSS)
$\overline{Z} = S_3$ (MSS)

Q = Q
N = F_3 if Z = 0
N = $F_3 \oplus S_3$ if Z = 1

3

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF 8)

FROM	TO										
	SLICE	Y	C_{n+4}	G, P	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CK	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 8: F = S + Cn
N = Q_3 (MSS)
Y = F
Q = LOG. 2Q

$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$Z = \bar{Q}_0\bar{Q}_1\bar{Q}_2\bar{Q}_3$

$OVR = Q_2 \oplus Q_1$ (MSS)

IDT3903B GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03B over the military operating range of -55°C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 15. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	—
Minimum Clock High Time	—
Minimum Time CP and $\overline{WE}$ both Low to Write	—

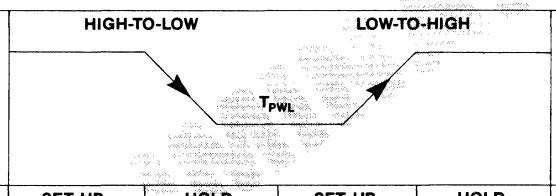
TABLE 16. ENABLE/DISABLE TIMES ALL FUNCTIONS

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	—	—
$\overline{OE}_B$	DB	—	—
$\overline{EA}$	DA	—	—
I_8	SIO	—	—
I_8	QIO	—	—
$I_{8,7,6,5}$	QIO	—	—
$I_{4,3,2,1,0}$	QIO	—	—
$\overline{LSS}$	$\overline{WR}$	—	—

NOTE:

C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 17. SETUP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	—	—	—	—	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	—	—	—	—	Prevent Writing
$\overline{WE}$ LOW	CP	—	—	—	—	Write into RAM
A, B Source	CP	—	—	—	—	Latch Data from RAM Out
B Destination	CP	—	—	—	—	Write Data into B Address
$QIO_{0,3}$	CP	—	—	—	—	Shift Q
$I_{8,7,6,5}$	CP	—	—	—	—	Write into Q(2)
$\overline{IEN}$ HIGH	CP	—	—	—	—	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	—	—	—	—	Write into Q
$I_{4,3,2,1,0}$	CP	—	—	—	—	Write into Q(2)

NOTES:

1. The internal Y-bus to RAM setup condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0).
2. The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.
3. For all other setup conditions not specified in this table, the setup time should be the delay to stable Y output plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this setup condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the WRITE/MSS output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The setup time prior to the clock LOW-TO-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual setup time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the setup time prior to clock L→ H and (2) the sum of the setup time prior to clock H→ L and the clock LOW time.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	—	—	—	—	—	—	—	—	—	—	—	—
DA, DB	—	—	—	—	—	—	—	—	—	—	—	—
Cn	—	—	—	—	—	—	—	—	—	—	—	—
I_{8-0}	—	—	—	—	—	—	—	—	—	—	—	—
CP	—	—	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	—	—	—	—	—	—	—	—	—	—	—	—
$\overline{MSS}$	—	—	—	—	—	—	—	—	—	—	—	—
Y	—	—	—	—	—	—	—	—	—	—	—	—
$\overline{IEN}$	—	—	—	—	—	—	—	—	—	—	—	—
$\overline{EA}$	—	—	—	—	—	—	—	—	—	—	—	—

NOTES:

1. A "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.

Standard Functions: See Table 2 Increment SF 4: F = S + 1 + Cn

MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CP	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

Unsigned Multiply
SF 0: F = S + Cn if Z = 0
F = S + R + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = C_{n+4}$ (MSS)
$\overline{Z} = Q_0$ (LSS)

Two's Complement Multiply
SF 2: F = S + Cn if Z = 0
F = R + S + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = F_3 \oplus OVR$ (MSS)
$Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle
SF 6: F = S + Cn if Z = 0
F = S - R - 1 + Cn if Z = 1
Y = Log. F/2
Q = Log. Q/2
$Y_3 = OVR \oplus F_3$ (MSS)
$\overline{Z} = Q_0$ (LSS)

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SF A/SF C, SF E)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WR}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CP	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op
SF A: $F = S + Cn$
$Y = \text{Log. } 2F$
$Q = \text{Log. } 2Q$
$SIO_3 = F_3 \oplus R_3$ (MSS)
$C_{n+4} = F_3 \oplus F_2$ (MSS)
$OVR = F_2 \oplus F_1$ (MSS)
$Z = \overline{Q_0 Q_1 Q_2 Q_3 F_0 F_1 F_2 F_3}$

Two's Complement Divide
SF C: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
$Y = \text{Log. } 2F$
$Q = \text{Log. } 2Q$
$SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
$Z = F_3 \oplus R_3$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder
SF E: $F = R + S + Cn$ if $Z = 0$
$F = S - R - 1 + Cn$ if $Z = 1$
$Y = F$
$Q = \text{Log. } 2Q$
$Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

3

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CP	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
EN											
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

SF 5: F = S + Cn if Z = 0
F = S + Cn if Z = 1

$Y_3 = S_3 \oplus F_3$ (MSS)
$Z = S_3$ (MSS)
Y = F

Q = Q
$N = F_3$ if Z = 0
$N = F_3 \oplus S_3$ if Z = 1

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF 8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\bar{G}, \bar{P}$	Z	N	OVR	DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
DA, DB	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
C_n	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
I_{8-0}	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
CK	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO_0, SIO_3	Any	—	—	—	—	—	—	—	—	—	—

NOTES:

1. An "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. An "@" means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.

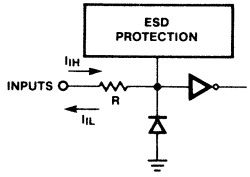
SF 8: F = S + Cn
N = Q_3 (MSS)
Y = F
Q = LOG. 2Q

$C_{n+4} = Q_3 \oplus Q_2$ (MSS)
$Z = Q_0Q_1Q_2Q_3$

OVR = $Q_2 \oplus Q_1$ (MSS)

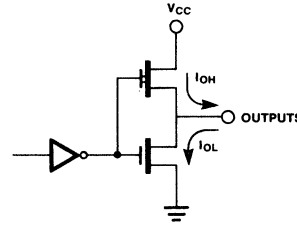
3

IDT39C03 INPUT/OUTPUT INTERFACE CIRCUITRY



IDT49C410-007

Figure 1. Input Structure (All Inputs)

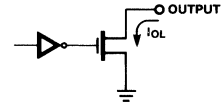


IDT49C410-008

Figure 2. Output Structure (All Outputs)

AC TEST CONDITIONS

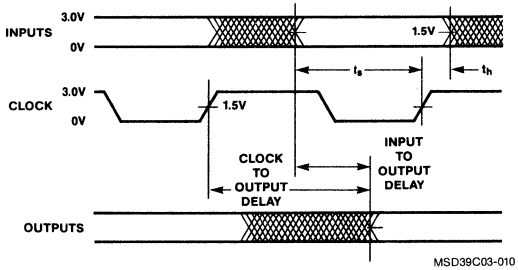
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 4



MSD39C03-008

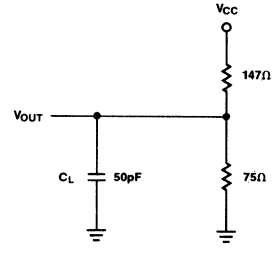
Figure 3. Open Drain Structure

SWITCHING WAVEFORMS



MSD39C03-010

TEST LOAD CIRCUITS



MSD39C03-009

Figure 4. Switching Test Circuit (all outputs)

Integrated Device Technology, Inc.

4-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C09A/B
IDT39C11A/B

MICROSLICE™ PRODUCT

FEATURES:

- Low-power CMOS
  - —Commercial — 45mA (max.)
  - —Military — 55mA (max.)
- Fast
  - —A versions meet standard speeds
  - —B versions are 20% speed upgrades
- 9-Deep stack
  - —Accommodates nested loops and subroutines
- Cascadable
  - —Infinitely expandable in 4-bit increments
- Available in 28-pin DIP/LCC (IDT39C09) and 20-pin DIP/LCC (IDT39C11)
- Pin-compatible, functional enhancement for all versions of the 2909/2911
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

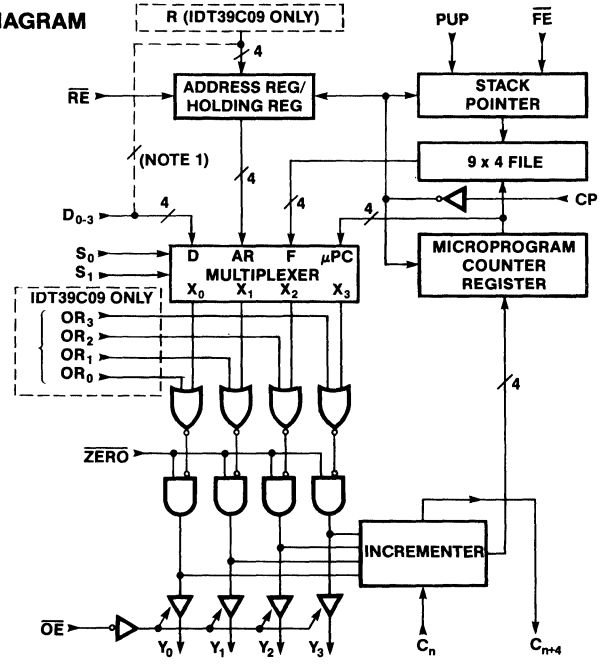
The IDT39C09/11 devices are high-speed, 4-bit address sequencers intended for controlling the sequence of micro-instructions located in the microprogram memory. They are fully cascadable and can be expanded to any increment of 4 bits.

The IDT39C09s can select an address from any four sources: 1) external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a 9-word deep push-pop stack; or 4) a program counter register. Also included in the stack are additional control functions which efficiently execute nested subroutine linkage. Each output can be ORed with an external input for conditional skip or branch instructions. A $\overline{ZERO}$ input line forces the outputs to all zeroes. All outputs are three-state and are controlled by the $\overline{OE}$ (Output Enable) pin.

The IDT39C11s operate identically to the IDT39C09s except the four OR outputs are removed and the D and R inputs are tied together. They are fabricated using CEMOS™, a single poly, double metal CMOS technology designed for high-performance and high-reliability. Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

3

FUNCTIONAL BLOCK DIAGRAM



Note 1: D and R connected on IDT39C11 only.

MSD39C09-001

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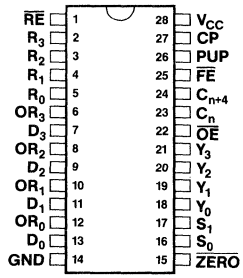
PIN CONFIGURATIONS

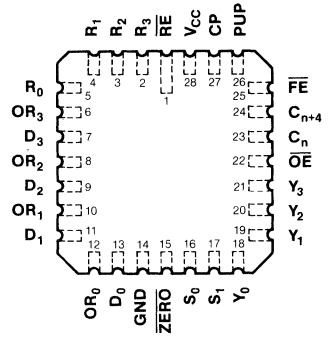
IDT39C09



DIP
TOP VIEW

MSD39C09-002

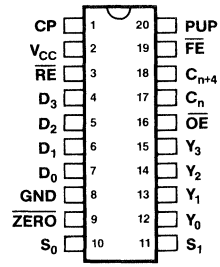
IDT39C09



LCC
TOP VIEW

MSD39C09-003

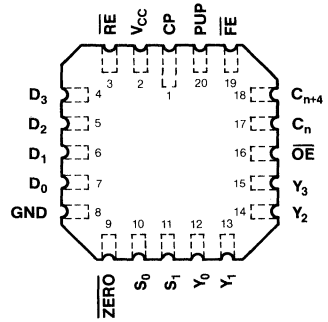
IDT39C11



DIP
TOP VIEW

MSD39C09-004

IDT39C11



LCC
TOP VIEW

MSD39C09-005

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
S_1, S_0	I	Control lines for address source selection.
$\overline{FE}$, PUP	I	Control lines for push/pop stack.
$\overline{RE}$	I	Enable line for internal address register.
OR_i	I	Logic OR inputs on each address output line. (IDT39C09 ONLY)
$\overline{ZERO}$	I	Logic AND input on the output lines.
$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance).
C_n	I	Carry-in to the incrementer.
R_i	I	Inputs to the internal address register. (IDT39C09 ONLY)
D_I	I	Direct inputs to the multiplexer.
CP	I	Clock input to the AR and μPC register and Push-Pop stack.
Y_i	O	Address outputs from IDT39C09/11. (Address inputs to control memory.)
C_{n+4}	O	Carry out from the incrementer

MICROPROGRAM SEQUENCER ARCHITECTURE

The IDT39C09/11's architecture consists of the following segments:

- —Multiplexer
- —Direct Inputs
- —Address Register
- —Microprogram Counter
- —Stack

MULTIPLEXER

The multiplexer is controlled by the S_0 and S_1 inputs to select the address source. The two inputs control the selection of the address register, direct inputs, microprogram counter or stack as the source of the next microinstruction address.

DIRECT INPUTS

This 4-bit field of inputs (D_i) allows addresses from an external source to be output on the Y outputs. On the IDT39C11s, these inputs are also used as inputs to the register.

ADDRESS REGISTER

The Address Register (AR) consists of 4 D-type, edge-triggered flip-flops which are controlled by the Register Enable ($\overline{RE}$) input. With the address register enable LOW, new data will be entered into the register on the clock LOW-to-HIGH transition. The address register is also available as the next microinstruction address to the multiplexer.

MICROPROGRAM COUNTER

Both devices contain a microprogram counter (μPC), which consists of a 4-bit incrementer followed by a 4-bit register. The incrementer has Carry-In (C_n) and Carry-Out (C_{n+4}) for easy and simple cascading.

When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 → μPC). If the least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y → μPC).

STACK

The 9-deep stack, which stores return addresses when executing microinstructions, is an input to the multiplexer. It contains a stack pointer which always points to the last word written. The added stack depth of 9 on the IDT39C09/11 allows for additional microinstruction nesting.

The stack pointer is an up/down counter controlled by File Enable ($\overline{FE}$) and Push/Pop (PUP) inputs. When the $\overline{FE}$ input is LOW and the PUP input is HIGH, the PUSH operation is enabled. The stack pointer will then increment and the memory array is written with the microinstruction address following the subroutine jump that initiated the PUSH. A POP operation is initiated at the end of a microsubroutine to obtain the return address. A POP will occur when $\overline{FE}$ and PUP are both LOW, implying a return from a subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the $\overline{FE}$ input is HIGH, no action is taken by the stack pointer regardless of any other input.

The $\overline{ZERO}$ is used to force the four outputs to the binary zero state. When LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output (IDT39C09 only). This allows jumping to different microinstructions on programmed conditions.

The Output Enable ($\overline{OE}$) input controls the Y outputs. When HIGH, the outputs are programmed to a high impedance condition.

OPERATION OF THE IDT39C09/11

Figure 1 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Also in Figure 1 is the truth table for the output control and the push/pop stack control. S_0, S_1, $\overline{FE}$ and PUP operation is explained in Figure 2. All four define the address appearing on the Y outputs and the state of the internal registers following a clock LOW-to-HIGH transition.

The columns on the left explain the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A". At the time T2, this instruction is in the μWR and the IDT39C09 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A) is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution and the return address J + 3 is pushed onto the stack. The return instruction is executed at T5. Figure 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

Figures 3 and 4 are examples of subroutine execution. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls the four signals S_0, S_1, $\overline{FE}$ and PUP. The starting address of the subroutine is applied to the D inputs of the IDT39C09 at the correct time.

3

ADDRESS SELECTION

S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
L	L	Microprogram Counter	μPC
L	H	Address/Holding Register	AR
H	L	Push-Pop stack	STK0
H	H	Direct inputs	D_i

OUTPUT CONTROL

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

SYNCHRONOUS STACK CONTROL

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 1.

CYCLE	S_0, S_1, $\overline{FE}$, PUP	μPC	REG	Y_{OUT}	COMMENT	PRINCIPAL USE
N N + 1	L L L L —	J J + 1	K K	J —	Pop Stack	End Loop
N N + 1	L L L H —	J J + 1	K K	J —	Push μPC	Set-up Loop
N N + 1	L L H X —	J J + 1	K K	J —	Continue	Continue
N N + 1	L H L L —	J K + 1	K K	K —	Pop Stack; Use AR for Address	End Loop
N N + 1	L H L H —	J K + 1	K K	K —	Push μPC; Jump to Address in AR	JSR AR
N N + 1	L H H X —	J K + 1	K K	K —	Jump to Address in AR	JMP AR
N N + 1	H L L L —	J Ra + 1	K K	Ra —	Jump to Address in STK0; Pop Stack	RTS
N N + 1	H L L H —	J Ra + 1	K K	Ra —	Jump to Address in STK0; Push μPC	
N N + 1	H L H X —	J Ra + 1	K K	Ra —	Jump to Address in STK0	Stack Ref (Loop)
N N + 1	H H L L —	J D + 1	K K	D —	Pop Stack; Jump to Address on D	End Loop
N N + 1	H H L H —	J D + 1	K K	D —	Jump to Address on D; Push μPC	JSR D
N N + 1	H H H X —	J D + 1	K K	D —	Jump to Address on D	JMP D

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_N = HIGH

Figure 2. Output and Internal Next-Cycle Register States for IDT39C09/11

CONTROL MEMORY

EXECUTE CYCLE	MICROPROGRAM ADDRESS	MICROPROGRAM SEQUENCER INSTRUCTION
	J - 1	—
T_0	J	—
T_1	J + 1	—
T_2	J + 2	JSR A
T_6	J + 3	—
T_7	J + 4	—
	—	—
	—	—
	—	—
	—	—
	—	—
T_3	A	I(A)
T_4	A + 1	—
T_5	A + 2	RTS
	—	—
	—	—
	—	—
	—	—
	—	—
	—	—
	—	—

In the columns on pages 5 and 6, the sequence of microinstructions to be executed are shown. At address J+2, the command "Jump to Subroutine at A" is contained in the sequence control portion of the microinstruction. At time T_2, this instruction is in the μWR, and the IDT39C09 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 4 shows a similar timing chart of one subroutine linking to a second, the latter consisting of only one microinstruction.

EXECUTIVE CYCLE		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
CLOCK SIGNALS											
IDT39C09/11 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	—	—	—	J + 3	J + 3	J + 3	—	—		
	STK1	—	—	—	—	—	—	—	—		
	STK2	—	—	—	—	—	—	—	—		
	STK3	—	—	—	—	—	—	—	—		
IDT39C09/11 Output	Y	J + 1	J + 2	A	A + 1	A + 2	$\bar{J}$ + 3	J + 4	J + 5		
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)	I(J + 5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)		

C_n = High

Figure 3. Subroutine Execution.

CONTROL MEMORY

EXECUTE CYCLE	MICROPROGRAM	
	ADDRESS	SEQUENCER INSTRUCTION
	J - 1	—
T_0	J	—
T_1	J + 1	—
T_2	J + 2	JSR A
T_9	J + 3	—
	—	—
	—	—
	—	—
	—	—
T_3	A	—
T_4	A + 1	—
T_5	A + 2	JSR B
T_7	A + 3	—
T_8	A + 4	RTS
	—	—
	—	—
	—	—
	—	—
T_6	B	RTS
	—	—
	—	—

EXECUTIVE CYCLE		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
CLOCK SIGNALS											
IDT39C09/11 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	—	—	—	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	—
	STK1	—	—	—	—	—	—	J + 3	—	—	—
	STK2	—	—	—	—	—	—	—	—	—	—
	STK3	—	—	—	—	—	—	—	—	—	—
IDT39C09/11 Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A + 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)	I(J + 4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)

C_n = High

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction.

IDT39C09/11 APPLICATIONS

The IDT39C09 and IDT39C11 are four-bit-slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the IDT39C09 and IDT39C11 apart from the IDT39C10, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The IDT39C09 or IDT39C11 should be selected instead of the IDT39C10 under the following conditions: (1) address less than 8 bits and not likely to be expanded; (2) address longer than 12 bits; (3) more complex instruction set needed than is available on IDT39C10.

CONTROL UNIT ARCHITECTURE

The recommended architecture using the IDT39C09 or IDT39C11 is shown in Figure 5. The path from the pipeline register output through the next address logic, multiplexer and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return from subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the IDT39C09 or IDT39C11.

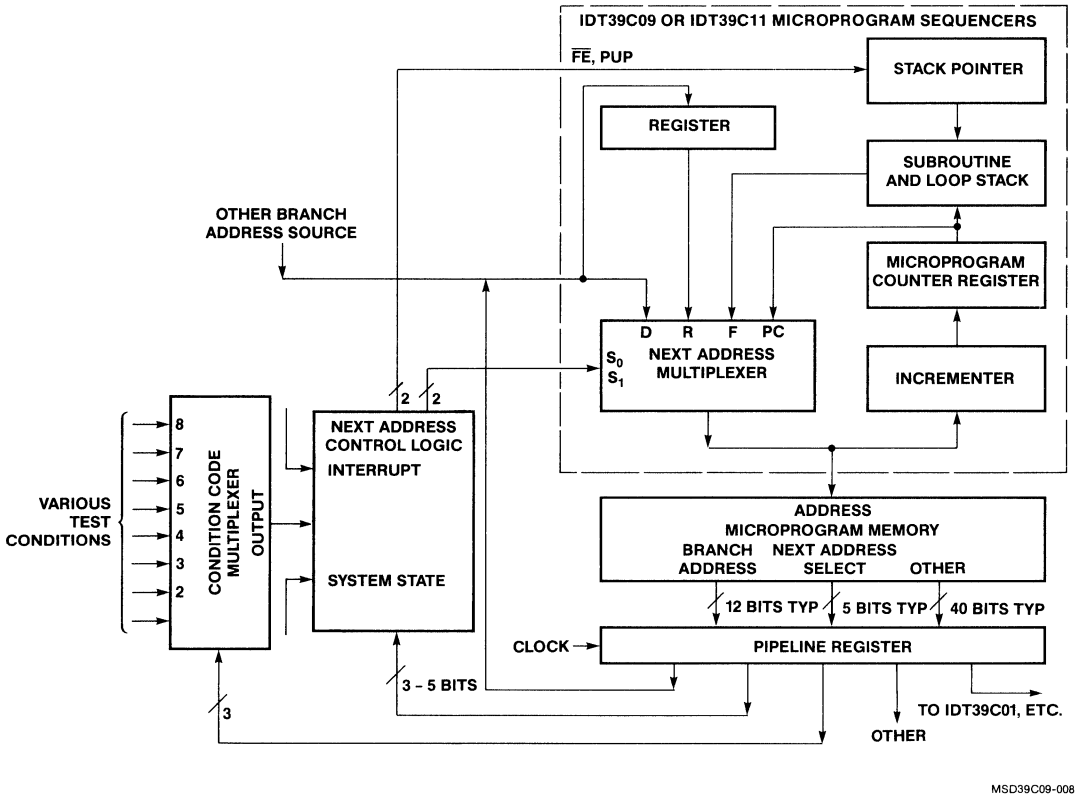


Figure 5. Recommended Computer Control Unit Architecture Using the IDT39C09A/B and IDT39C11A/B.

IDT39C09/11 EXPANSION

Figure 6 shows the interconnection of three IDT39C11s to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the IDT39C11 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a microaddress register is placed at the IDT39C11 output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a setup time prior to the clock.

SELECTING BETWEEN THE IDT39C09 AND IDT39C11

The difference between the IDT39C09 and the IDT39C11 involves two signals: the data inputs to the holding register and the OR inputs. In the IDT39C09, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the IDT39C11, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 7. Using the IDT39C09, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the IDT39C11, it is more common to connect the IDT39C11's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 7 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

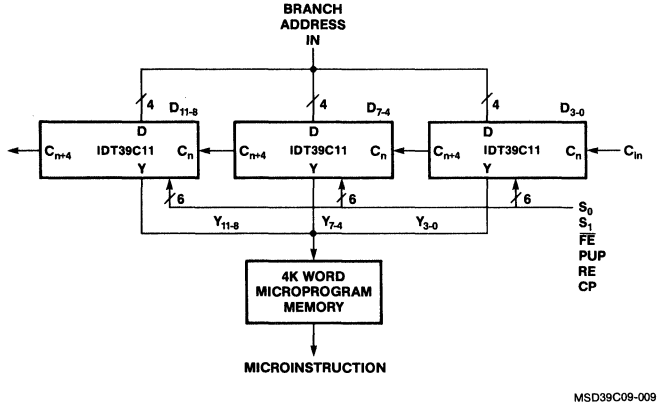


Figure 6. Twelve Bit Sequencer.

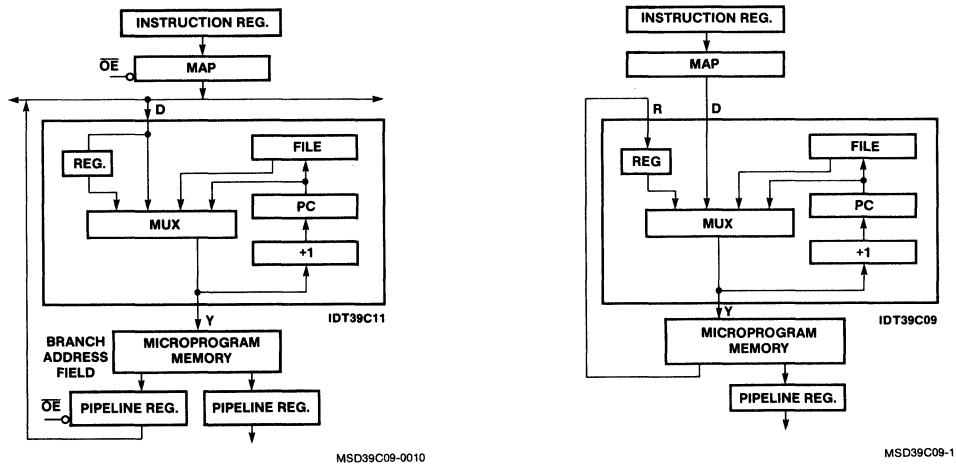


Figure 7. Branch Address Structures.

The second difference between the IDT39C09 and IDT39C11 is that the IDT39C09 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply typing several test conditions into the OR lines (see Figure 8). Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1s or 0s by test conditions applied to the OR lines. In Figure 8, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110 or 1111.

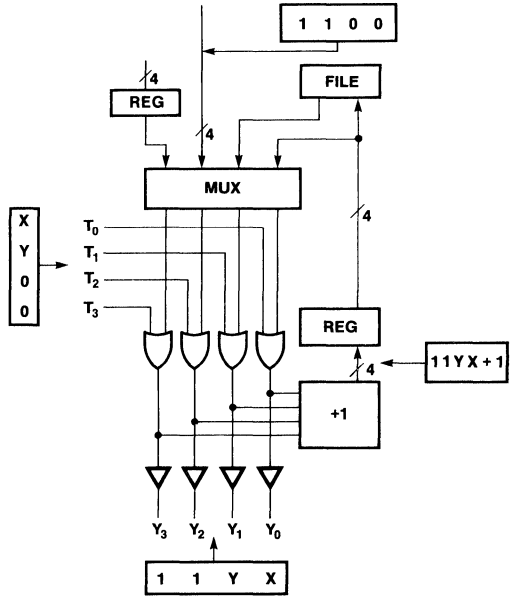


Figure 8. Use of OR Inputs to Obtain 4-Way Branch.

How to Perform Common Functions with the IDT39C09/11

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	H	L	L	H	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	H	H	H	H	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP TO SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	H	H	H	L	H

Subroutine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN FROM SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	H	H	L	L	L

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

3

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-130	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (CONT'D)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	—	55	
			COM'L.	—	—	45	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input frequency.

3

IDT39C09A/IDT39C11A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Table I, II and III below define the timing characteristics of the IDT39C09A/11A over the operating voltage and temperature range. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF (except output disable test)

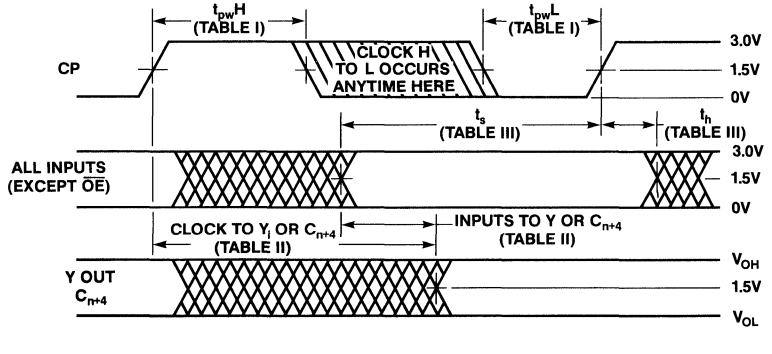
FROM INPUT	COMMERCIAL		MILITARY		UNITS
	Y	C_{n+4}	Y	C_{n+4}	
D_i	17	22	20	25	ns
S_0, S_1	29	34	29	34	ns
OR_i	17	22	20	25	ns
C_n	—	14	—	16	ns
$\overline{ZERO}$	29	34	30	35	ns
$\overline{OE}$ LOW (enable)	25	—	25	—	ns
$\overline{OE}$ HIGH (disable)(1)	25	—	25	—	ns
Clock ↑ S_1S_0 = LH	39	44	45	50	ns
Clock ↑ S_1S_0 = LL	39	44	45	50	ns
Clock ↑ S_1S_0 = HL	44	49	53	58	ns

NOTE:
1. C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES(1)

FROM INPUT	COMMERCIAL		MILITARY		UNITS
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
$\overline{RE}$	19	4	19	5	ns
R_i(2)	10	4	12	5	ns
PUP	25	4	27	5	ns
$\overline{FE}$	25	4	27	5	ns
C_n	18	4	18	5	ns
D_i	25	0	25	0	ns
OR_i	25	0	25	0	ns
S_0, S_1	25	0	29	0	ns
$\overline{ZERO}$	25	0	29	0	ns

NOTES
1. All times relative to clock LOW-to-HIGH transition.
2. On IDT39C11, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



MSD39C09-007

IDT39C09B/IDT39C11B SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Table I, II and III below define the timing characteristics of the IDT39C09B/11B over the operating voltage and temperature range. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	—	—
Minimum Clock HIGH Time	—	—

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF (except output disable test)

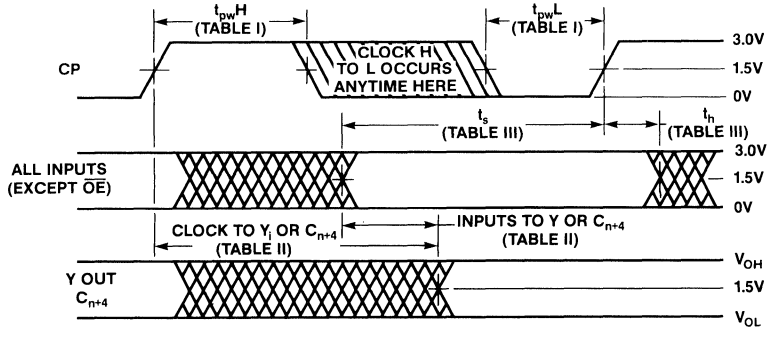
FROM INPUT	COMMERCIAL		MILITARY		UNITS
	Y	C_{n+4}	Y	C_{n+4}	
D_i	—	—	—	—	ns
S_0, S_1	—	—	—	—	ns
OR_i	—	—	—	—	ns
C_n	—	—	—	—	ns
$\overline{ZERO}$	—	—	—	—	ns
$\overline{OE}$ LOW (enable)	—	—	—	—	ns
$\overline{OE}$ HIGH (disable)[1]	—	—	—	—	ns
Clock ↑ S_1S_0 = LH	—	—	—	—	ns
Clock ↑ S_1S_0 = LL	—	—	—	—	ns
Clock ↑ S_1S_0 = HL	—	—	—	—	ns

NOTE:
1. C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES[1]

FROM INPUT	COMMERCIAL		MILITARY		UNITS
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
$\overline{RE}$	—	—	—	—	ns
R_i[2]	—	—	—	—	ns
PUP	—	—	—	—	ns
$\overline{FE}$	—	—	—	—	ns
C_n	—	—	—	—	ns
D_i	—	—	—	—	ns
OR_i	—	—	—	—	ns
S_0, S_1	—	—	—	—	ns
$\overline{ZERO}$	—	—	—	—	ns

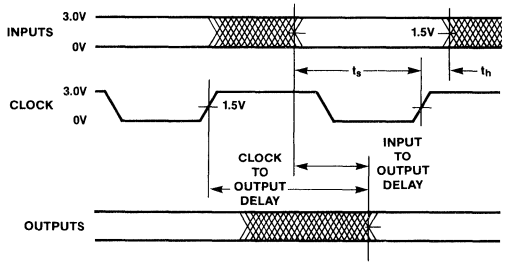
NOTES:
1. All times relative to clock LOW-to-HIGH transition.
2. On IDT39C11, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

SWITCHING WAVEFORMS



TEST LOAD CIRCUIT

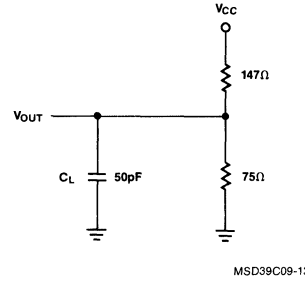


Figure 1. Switching Test Circuit (all outputs)

INPUT/OUTPUT INTERFACE CIRCUITRY

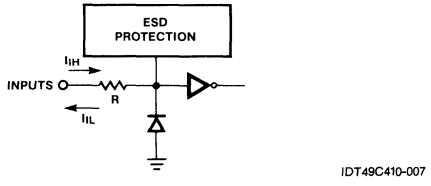


Figure 1. Input Structure (All Inputs)

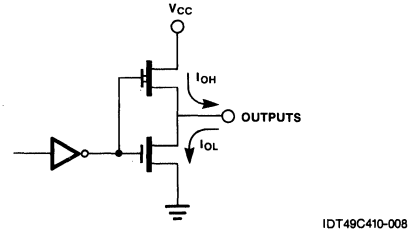


Figure 2. Output Structure (All Outputs)

Integrated Device Technology, Inc.

12-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C10B
IDT39C10C

MICROSLICE™ PRODUCT

FEATURES:

- Low-power CEMOS™
  - I_{CC} (max.)
    Military — 90mA
    Commercial — 75mA
- Fast
  - IDT39C10B matches 2910A speeds
  - IDT39C10C 30% speed upgrade
- 33-Deep stack
  - Accommodates highly nested loops and subroutines microcode
- 12-bit address width
- 12-bit internal loop counter
- 16 powerful microinstructions
- 3 enables control branch address sources
- Available in 40-pin DIP and 44-pin LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

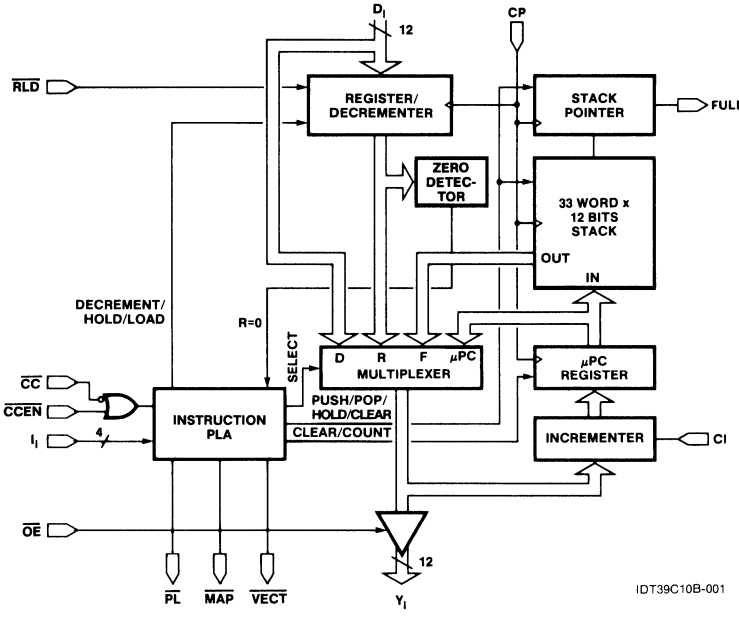
The IDT39C10 microprogram sequencers are designed for use in high-performance microprogram state machines. These microprogram sequencers are intended for use in controlling the sequence of microinstructions executed in the microprogram memory. The IDT39C10s provide several conditional branch instructions that allow branching to any microinstruction within the 4K microword address space. A 33-deep last-in, first-out stack provides for a very powerful microprogram subroutine return linkage and looping capability. With this depth of a microprogram return stack, the microprogrammer has maximum flexibility in nesting subroutines and loops. The counter contained in the IDT39C10s provides for microinstruction loop counts of up to 4096, in terms of total count length.

The IDT39C10s provide a 12-bit address to the microprogram memory. This microprogram sequencer selects one of four sources for the address: these are (1) the microprogram address register, (2) external direct input, (3) internal register counter, and (4) the 33-deep LIFO stack. The microprogram counter usually contains an address that is one greater than the microinstruction currently being executed in the microprogram pipeline register.

The IDT39C10s are fabricated using CEMOS, a single-poly double metal CMOS technology designed for high-performance and high-reliability. The devices are pin-compatible, performance-enhanced, functional replacements for the 2910A.

3

FUNCTIONAL BLOCK DIAGRAM



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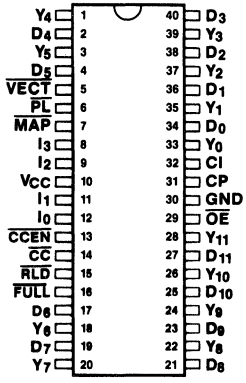
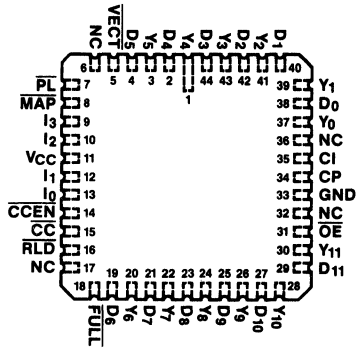
PIN CONFIGURATIONS



DIP
TOP VIEW

IDT39C10B-002



LCC
TOP VIEW

IDT39C10B-003

PIN FUNCTIONS

PIN NAME	DESCRIPTION	FUNCTION
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer D_0 is LSB.
I_i	Instruction Bit i	Selects one-of-sixteen instructions.
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs.
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge.
V_{CC}	5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB.
$\overline{FULL}$	Full	Indicates that 33 items are on the stack.
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

PRODUCT DESCRIPTION

The IDT39C10s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 4K words of microprogram.

The heart of the microprogram sequencers is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter or the stack as the source for the address of the next microinstruction.

The register/counter consists of twelve D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable as well as the four microinstruction control inputs. When the load control (RLD) is LOW, the data at the D-inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as a condition code input for some of the microinstructions. The IDT39C10s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 12-bit incrementer followed by a 12-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry-in input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are twelve D-inputs on the IDT39C10s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 12-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT39C10s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT39C10s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

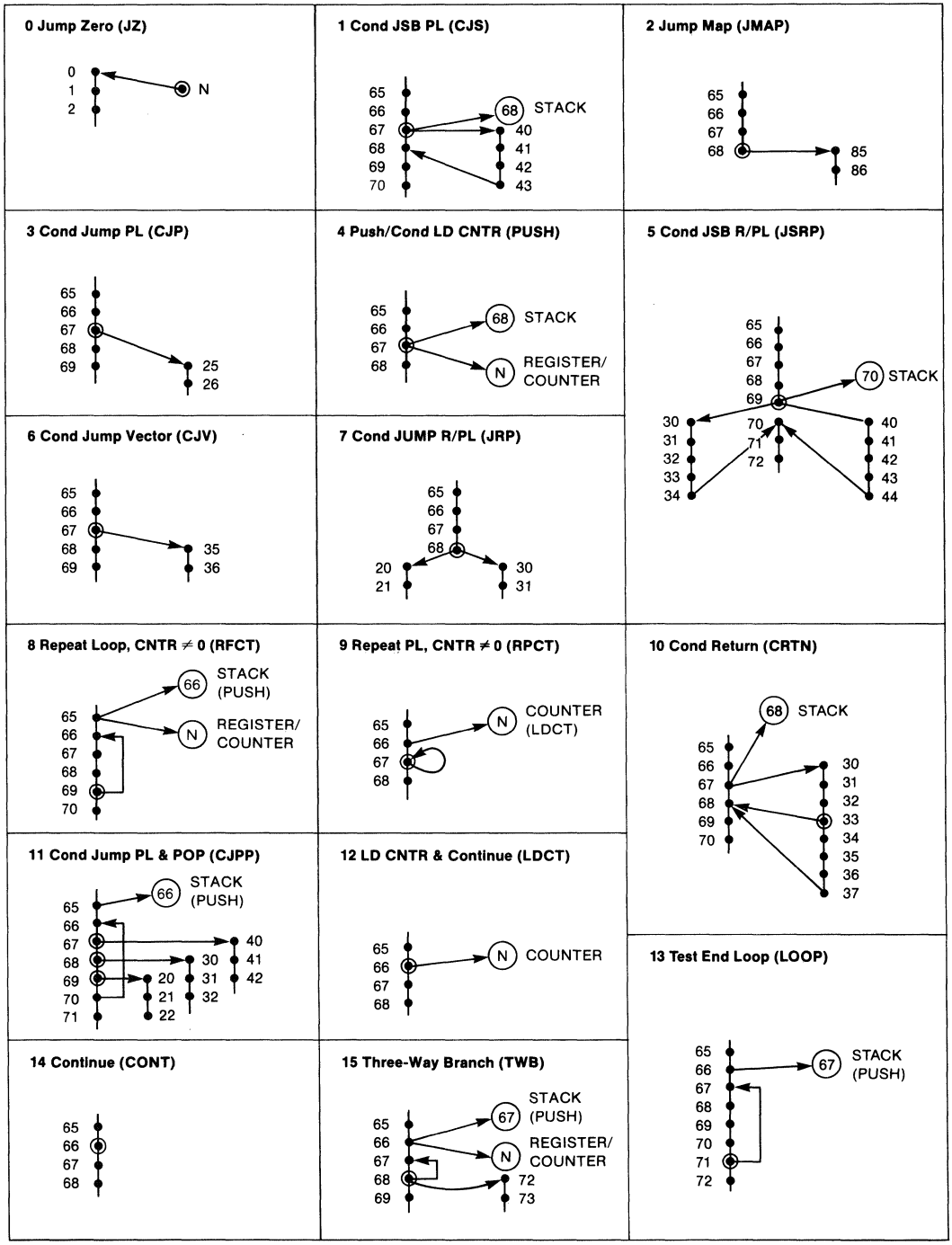
The IDT39C10s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{\text{FULL}}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (Instruction 0). This sets the stack pointer to the stack empty position—the equivalent depth of 0. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed so as not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

The IDT39C10s' internal 12-bit register/counter is used during microinstructions eight, nine and fifteen. During these instructions, the 12-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that if it is preloaded with a number N, and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, Instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next address coming from the D inputs, the stack or the microprogram counter.

The IDT39C10s provide a 12-bit address at the Y outputs that are under control of the $\overline{\text{OE}}$ input. Thus, the outputs can be put in the three-state mode, allowing the writeable control store to be loaded or certain types of external diagnostics to be executed.

In summary, the IDT39C10s are the most powerful microprogram sequencers currently available. They provide the deepest stack, the highest performance, and the lowest power dissipation for today's microprogrammed machine design.

FIGURE 1. IDT39C10B FLOW DIAGRAMS



IDT39C10 OPERATION

The IDT39C10s are CMOS pin-compatible implementations of the Am2910 & 2910A microprogram sequencers. The IDT39C10s' microprogram is functionally identical except that it provides a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry input. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$ or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT39C10s is a last-in, first-out memory that is 12-bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way; however, it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more PUSHes than pops have occurred since the stack was last empty. When this happens, the FULL flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT39C10 INSTRUCTION SET

This data sheet contains a block diagram of the IDT39C10 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3-I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 4K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT39C10s can be from one of four sources. These include the internal microprogram counter, the last-in first-out stack, the register/ counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT39C10s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and currently being executed.

INSTRUCTION 0— JUMP 0 (JZ)

This instruction is used at power-up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1— CONDITIONAL JUMP TO SUBROUTINE (CJS)

The conditional jump to subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT39C10s shown in Figure 1, we see that the contents of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, then this conditional jump to subroutine instruction behaves as a simple continue. That is, the contents of microinstruction address 68 is executed next.

INSTRUCTION 2— JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be to the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3— CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT39C10 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken while, if the test fails, this instruction executes as a simple continue. In the example shown in the flow diagrams of Figure 1, we see that if the test is passed, the next microinstruction to be executed is the contents of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

IDT39C10 INSTRUCTION OPERATIONAL SUMMARY

I_3-I_0	MNEMONIC	CC	COUNTER TEST	STACK	ADDRESS SOURCE	REGISTER/ COUNTER	ENABLE SELECT
0	JZ	X	X	CLEAR	0	NC	PL
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	PL PL
2	JMAP	X	X	NC	D	NC	MAP
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	PL PL
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	PL PL
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	PL PL
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	VECT VECT
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	PL PL
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	PL PL
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	PL PL
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	PL PL
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	PL PL
12	LDCT	X	X	NC	PC	LOAD	PL
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	PL PL
14	CONT	X	X	NC	PC	NC	PL
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	PL PL PL PL

NC = no change; DEC = decrement

INSTRUCTION 4— PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/conditional load counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5— CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a conditional jump subroutine from the internal register or from the external pipeline register. In this instruction the contents of the microprogram counter are pushed on the stack and the branch adddress for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6— CONDITIONAL JUMP VECTOR (CJV)

The conditional jump vector instruction is similar to the jump map instruction in that it allows a branch operation to a microinstruction as defined from some external source. This instruction is similar to the jump map instruction except that it is conditional. The jump map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{\text{VECT}}$ output is LOW unconditionally. Thus, an external 12-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7— CONDITIONAL JUMP R/PL (JRP)

The conditional jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8— REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/conditional load counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9— REPEAT PIPELINE COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10— CONDITIONAL RETURN (CRTN)

The conditional return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11— CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The conditional jump pipeline and pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagrams for the IDT39C10s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and since the loop is being terminated, the stack will be popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12— LOAD COUNTER AND CONTINUE (LDCT)

The load counter and continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13— TEST END OF LOOP (LOOP)

The test end of loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14— CONTINUE (CONT)

The continue instruction is a simple instruction whereby the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15— THREE WAY BRANCH (TWB)

The three-way branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, then a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT39C10s' flow diagrams and is also described in full detail in the IDT39C10s' instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, then the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT39C10s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, then this instruction "times out." The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT39C10 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

IDT39C10 INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	Cond JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	Jump Map	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	Cond Jump PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/Cond Ld Cntr	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	Cond JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	Cond Jump Vector	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	Cond Jump R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	Cond RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	Cond Jump PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD Contr & Continue	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	Test End Loop	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	Continue	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	Three Way Branch	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

NOTE: 1. If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level[4]		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level[4]		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V[3]		-30	—	-130	mA
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		—	—	—	mA
I_{CCQT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power[6] Supply Current	V_{CC} = Max., F_C = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., F_C = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	55	90	
			COM'L.	—	55	75	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. I_{CCQT} is derived by measuring the total current with all the inputs tied together @ 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

   $I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$

   CD_H = Clock duty cycle high period.
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
   N_T = Number of dynamic inputs driven at TTL levels.
   f_{CP} = Clock Input frequency.

IDT39C10B AC ELECTRICAL CHARACTERISTICS

C_L = 50pF, T_A = -55°C to +125°C (Military), 0°C to +70°C (Commercial)

I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	
$D_i \rightarrow R$	16	16	0	0	ns
$D_i \rightarrow PC$	30	30	0	0	ns
I_{0-3}	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	20	25	—	—	—	—	ns
I_{0-3}	35	40	30	35	—	—	ns
$\overline{CC}$	30	36	—	—	—	—	ns
$\overline{CCEN}$	30	36	—	—	—	—	ns
CP	40	46	—	—	31	35	ns
$\overline{OE}$(1)	25/27	25/30	—	—	—	—	ns

NOTE:

1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNITS
Minimum clock LOW time	20	25	ns
Minimum clock HIGH time	20	25	ns
Minimum clock period	50	51	ns

IDT39C10C AC ELECTRICAL CHARACTERISTICS

C_L = 50pF, T_A = -55°C to +125°C (Military), 0°C to +70°C (Commercial)

I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	
$D_i \rightarrow R$	6	7	0	0	ns
$D_i \rightarrow PC$	13	15	0	0	ns
I_{0-3}	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	12	15	—	—	—	—	ns
I_{0-3}	20	25	13	15	—	—	ns
$\overline{CC}$	16	20	—	—	—	—	ns
$\overline{CCEN}$	16	20	—	—	—	—	ns
CP	28	33	—	—	22	25	ns
$\overline{OE}$(1)	10/10	13/13	—	—	—	—	ns

NOTE:

1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

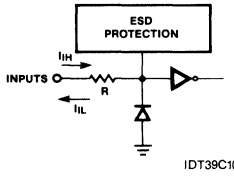
III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNITS
Minimum clock LOW time	18	20	ns
Minimum clock HIGH time	17	20	ns
Minimum clock period	35	40	ns

AC TEST CONDITIONS

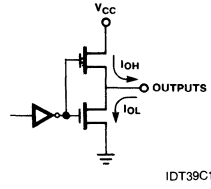
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 3

IDT39C10B INPUT/OUTPUT INTERFACE CIRCUITRY



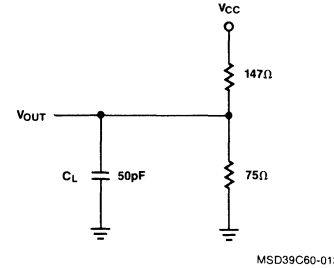
IDT39C10B-007

Figure 1. Input Structure (All Inputs)



IDT39C10B-008

Figure 2. Output Structure (All Outputs)



MSD39C60-013

Figure 3. Output Load Circuit

Integrated Device Technology, Inc

4-BIT CMOS MICROPROCESSOR SLICE

ADVANCE INFORMATION
IDT39C203
IDT39C203A

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - —IDT39C203 matches 29203 speeds
  - —IDT39C203A 20% speed upgrade
- Low-power CMOS
  - —Commercial — 60mA (max.)
  - —Military — 70mA (max.)
- Pin-compatible, performance-enhanced functional replacement for the 29203
- Cascadable to 8, 12, 16, etc. bits
- Infinitely expandable register file
- Improved I/O capability
  - —DA, DB and Y ports are bidirectional
- Performs BCD arithmetic
  - —Features automatic BCD add, subtract and conversion between binary and BCD
- On-chip parity generation and sign extension logic
  - —Provides parity across the entire ALU output and sign extension at any slice boundary
- On-chip normalization logic
  - —Floating point mantissa and exponent easily developed using single microcycle per shift
- On-chip multiplication and division logic
- Two bidirectional data lines
- Packaged in 48-pin DIP and 52-pin LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C203s are four-bit expandable, high-performance CMOS microprocessor slices. Along with the standard features associated with the IDT39C01s and IDT39C03s, the IDT39C203s also incorporate additional enhancements for arithmetic-oriented processors.

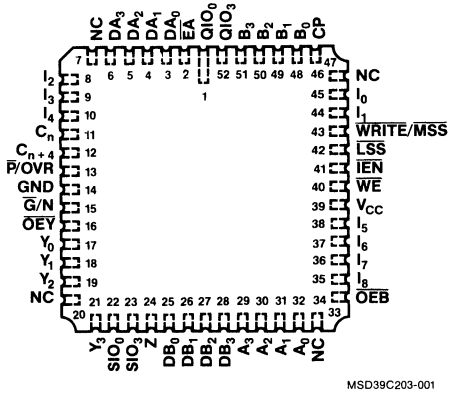
These extremely low-power yet high-speed three-port three-address architectured microprocessors consist of a 16-word by 4-bit dual-port RAM with latches on both outputs, high-performance ALU and shifter, a flexible Q Register with shifter input, and nine-bit instruction decoder. Additionally, special instructions which allow the easy implementation of multiplication, division, normalization, BCD arithmetic and conversion are standard on the IDT39C203s. Both devices are easily expandable in 4-bit increments.

They are pin-compatible, functional replacements for all versions of the 29203. The fastest version, the IDT39C203A, is a 20% speed upgrade from the normal 29203 device. The IDT39C203 meets the 29203 speeds.

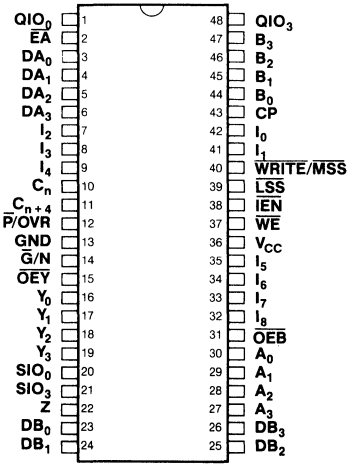
The IDT39C203s are fabricated using CEMOS™, a single-poly, double metal CMOS technology designed for high-performance and high-reliability.
Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications.

3

PIN CONFIGURATIONS



LCC
TOP VIEW



DIP
TOP VIEW

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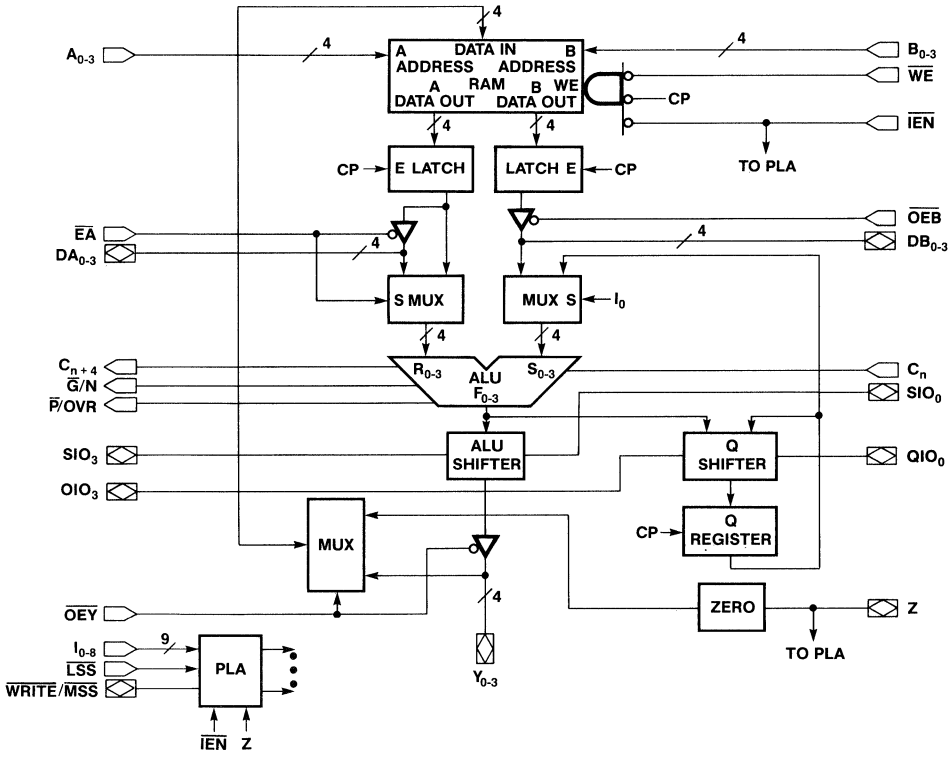
FUNCTIONAL BLOCK DIAGRAM



16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60A
IDT39C60-1
IDT39C60

MICROSLICE™ PRODUCT

FEATURES:

- Low Power CEMOS
  - — Military — 100mA (max.)
  - — Commercial — 85mA (max.)
- Fast
  - — Data in to error detect
    IDT39C60A — 20ns (max.), IDT39C60-1 — 25ns (max.)
    IDT39C60 — 32ns (max.)
  - — Data in to corrected data out
    IDT39C60A — 30ns (max.), IDT39C60-1 — 52ns (max.)
    IDT39C60 — 65ns (max.)
- Improves system memory reliability
  - — Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64-bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 52-pin LCC, as well as space-efficient 48-pin SHRINK-DIP (70 mil pin centers) and 48-pin LCC
- Pin-compatible, functional equivalent to all versions of the 2960
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate check bits on a 16-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

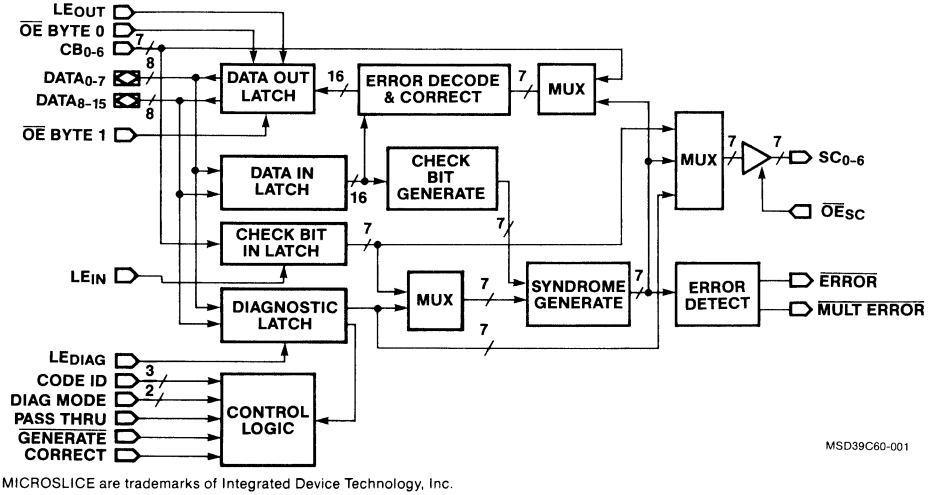
The IDT39C60s are easily cascadable from 16 bits up to 64 bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

All incorporate 2 built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the 2960. They are fabricated using CEMOS™, a single poly, double metal CMOS technology designed for high-performance and high-reliability. The devices are packaged in either 48-pin DIPs or 48-pin and 52-pin LCCs. Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

3

FUNCTIONAL BLOCK DIAGRAM



MSD39C60-001

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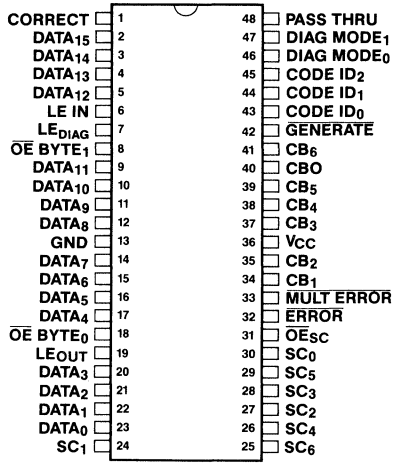
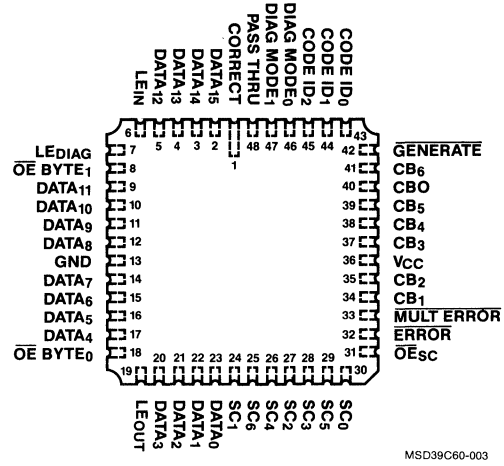
PIN CONFIGURATIONS



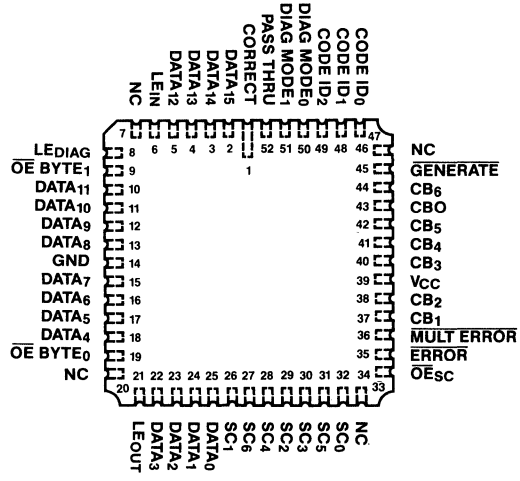
MSD39C60-002

DIP
TOP VIEW
(600 mil x 100 mil CENTERS)
(400 mil x 70 mil CENTERS)



MSD39C60-003

LCC
TOP VIEW
(560 mil x 650 mil)



MSD39C60-004

LCC
TOP VIEW
(750 mil x 750 mil)

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-15}$	I/O	16 bidirectional data lines. They provide input to the Data Input Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.
CB_{0-6}	I	Seven check bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.
LE_{IN}	I	Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.
$\overline{GENERATE}$	I	Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected —corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error.
SC_{0-6}	O	Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.
$\overline{ERROR}$	O	Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, $\overline{ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{ERROR}$ must be implemented externally.)
$\overline{MULT\ ERROR}$	O	Multiple Errors Detected output. When the EDC is in Detect or Correct mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, $\overline{MULT\ ERROR}$ is forced HIGH. (In a 64-bit configuration, $\overline{MULT\ ERROR}$ must be implemented externally.)
CORRECT	I	Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.
LE_{OUT}	I	Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.
$\overline{OE}\ BYTE_0$ $\overline{OE}\ BYTE_1$	I	Output Enable — Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch, and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.
PASS THRU	I	Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.
DIAG $MODE_{0-1}$	I	Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.
CODE ID_{0-2}	I	Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16-, 32- and 64-bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the diagnostic latch rather than the control lines.
LE DIAG	I	Latch Enable — Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- Data Input Latch
- Data Output Latch
- Diagnostic Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Control Logic

DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LE_{IN}, Latch Enable input, controls the Data Input Latch which can load 16-bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostic modes.

The Data Output Latch is split into 2 bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LE_{OUT}). The PASS THRU control input determines which data is loaded.

CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming code from the 16 bits of data input from the Data Input Latch.

SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs. If one or more errors are detected, $\overline{\text{ERROR}}$ goes low. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LE_{OUT} control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC Unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming code. The EDC can compare internally generated check bits against those read with the 16-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits), or 64-bit data words.

CODE AND BYTE SELECTION

The 3 code identification pins, ID_{2-0}, are used to determine the data word size from 16-, 32- or 64-bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.
Code 32/39 refers to a 32-bit data field with 7 check bits.
Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID_{2-0} of 001 is used to place the device in the Internal Control Mode as described later in this section.

Table 1 defines all possible identification codes.

CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three state output pins SC_{0-6}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double error was detected. Some triple-bit errors are also detected. The check bits are labeled:

CX, C0, C1, C2, C4 for the 8-bit configuration
CX, C0, C1, C2, C4, C8 for the 16-bit configuration
CX, C0, C1, C2, C4, C8, C16 for the 32-bit configuration
CX, C0, C1, C2, C4, C8, C16, C32 for the 64-bit configuration

Syndrome bits are similarly labeled SX through S32.

CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG $MODE_{1-0}$, define 4 basic areas of operation, with $\overline{\text{GENERATE}}$, CORRECT, and PASS THRU further dividing operation into 8 functions with the ID_{2-0} defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC_{0-6}. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-6}. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero, and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG $MODE_{1-0}$, CORRECT, PASS THRU and CODE ID to be defined by the Diagnostic Latch. When in the internal mode, the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

TABLE 1.
HAMMING CODE AND SLICE IDENTIFICATION

CODE ID_2	CODE ID_1	CODE ID_0	HAMMING CODE AND SLICE SELECTED
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE 2.
DIAGNOSTIC MODE CONTROL

DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.

TABLE 3. IDT39C60 OPERATING MODES

OPERATING MODE	DM1	DM0	$\overline{\text{GENERATE}}$	CORRECT	PASS THRU	DATA OUT LATCH (LE_{OUT} = HIGH)	SC_{0-6} ($\overline{OE}_{SC}$ = LOW)	$\overline{\text{ERROR}}$ $\overline{\text{MULT ERROR}}$
Generate	0 1	0 0	0	X	0	—	Check Bits Generated from Data In Latch	—
Detect	0 0	0 1	1	0	0	Data In Latch	Syndrome Bits Data In/Check Bit Latch	Error(1) Dep
Correct	0 0	0 1	1	1	0	Data In Latch with Single Bit Correction	Syndrome Bits Data In/Check Bit Latch	Error Dep
Pass Thru	0 0 1	0 1 0	X	X	1	Data In Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	0	—	Check Bits from Diagnostic Latch	—
Diagnostic Detect	1	0	1	0	0	Data In Latch	Syndrome Bits Data In/Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	0	Data In Latch with Single Bit Correction	Syndrome Bits Data In/Diagnostic Latch	Error Dep
Initialization Mode	1	1	X	X	X	Data In Latch Set to 0000	Check Bits Generated from Data In Latch (0000)	—
Internal Mode	ID_{2-0} = 001 Control Signals ID_{2-0}, DIAG $MODE_{1-0}$, CORRECT, and PASS THRU are taken from the Diagnostic Latch							

NOTE:
1. ERROR DEP (Error Dependent): $\overline{\text{ERROR}}$ will be low for single or multiple errors, with $\overline{\text{MULT ERROR}}$ low for double or multiple errors. Both signals are high for no errors.

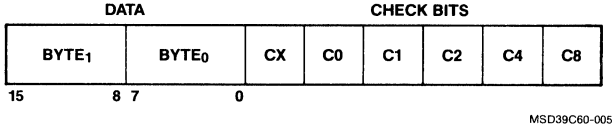
16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC Unit, connected as shown in Figure 2, provides all logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicated 6 check bits are required. The CB_6 pin is therefore a "Don't Care" and ID_2, ID_1, ID_0 = 000.

Table 3 describes the operating modes available. The output pin SC_6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function or the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. Check bits are passed as stored in the Pass Thru or Diagnostic Generate mode.



USES MODIFIED HAMMING CODE 16/22
16 DATA BITS WITH 6 CHECK BITS

Figure 1. 16-Bit Data Format

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six syndrome bits to indicate the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-5} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

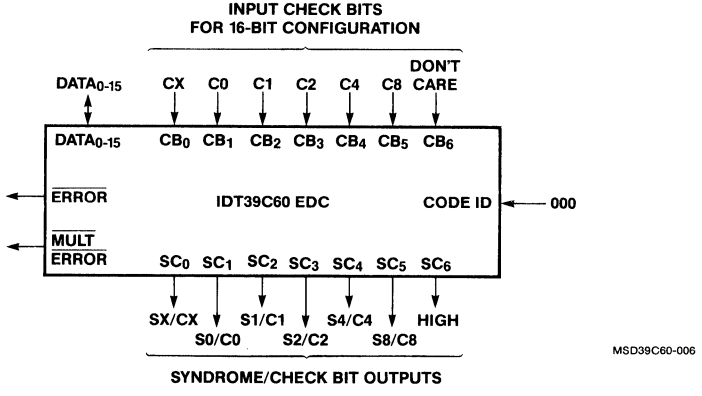


Figure 2. 16-Bit Configuration

TABLE 4. 16-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

TABLE 5. SYNDROME DECODE TO BIT-IN-ERROR

SYNDROME BITS			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 6. DIAGNOSTIC LATCH LOADING — 16-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID_0
9	CODE ID_1
10	CODE ID_2
11	DIAG $MODE_0$
12	DIAG $MODE_1$
13	CORRECT
14	PASS THRU
15	Don't Care

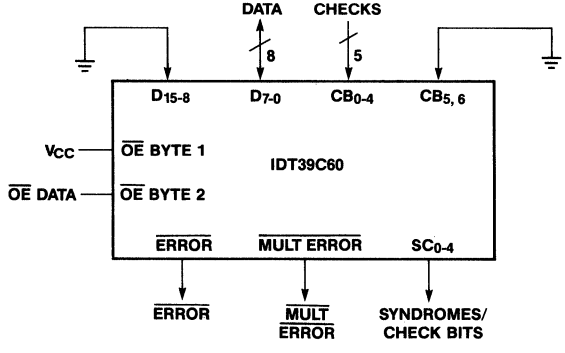


Figure 3. 8-Bit Configuration

32-BIT DATA WORD CONFIGURATION

Two IDT39C60 EDC Units, connected as shown in Figure 5, provide all logic needed for single bit error correction and double bit error detection of a 32-bit data field. The Identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID_2, ID_1, ID_0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The $\overline{OE}_{SC}$ always enables the SC_{0-6} outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format of 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of syndrome bits from byte 2/3 into the byte 1/0 unit. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 7 indicates the decoding of the 7 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the Data Bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. Check bits are passed as stored in the Pass Thru or Diagnostic Generate mode.

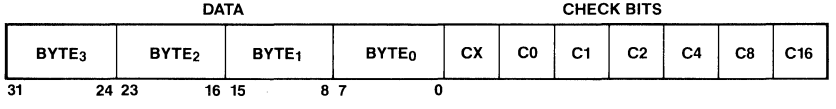
TABLE 7. SYNDROME DECODE TO BIT-IN-ERROR FOR 32 BITS

SYNDROME BITS				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

NOTES:
* = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 8. KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-BIT PROPAGATION DELAY		COMPONENT DELAY FROM IDT39C60 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	Corrected DATA Out	(DATA to SC) + (CB to SC, Code ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)



MSD39C60-007

USES MODIFIED HAMMING CODE 32/39
32 DATA BITS WITH 7 CHECK BITS

Figure 4. 32-Bit Data Format

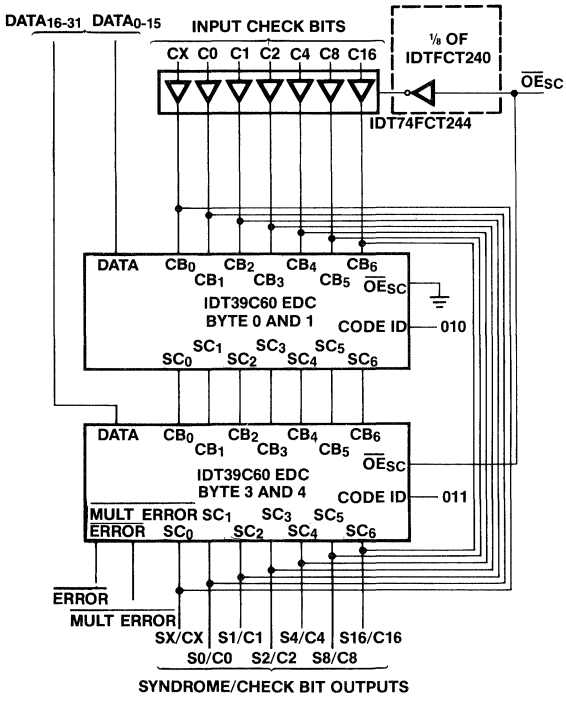


Figure 5. 32-Bit Configuration

TABLE 9.
DIAGNOSTIC LATCH LOADING — 32-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1—CODE ID_0
9	Slice 0/1—CODE ID_1
10	Slice 0/1—CODE ID_2
11	Slice 0/1—DIAG $MODE_0$
12	Slice 0/1—DIAG $MODE_1$
13	Slice 0/1—CORRECT
14	Slice 0/1—PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3—CODE ID_0
25	Slice 2/3—CODE ID_1
26	Slice 2/3—CODE ID_2
27	Slice 2/3—DIAG $MODE_0$
28	Slice 2/3—DIAG $MODE_1$
29	Slice 2/3—CORRECT
30	Slice 2/3—PASS THRU
31	Don't Care

TABLE 10. 32-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC Units connected with the MSI gates, as shown in Figure 6, provide the logic needed for single bit error correction and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed back to the CB_{0-6} inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The $\overline{\text{ERROR}}$ signal is low for one or more errors detected. From any of the 4 devices, $\overline{\text{MULT ERROR}}$ is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of eight bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CB_{0-6} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 decribes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 in relating a single IDT39C60 EDC with the four units of Figure 7. Delay through the exclusive, or MSI, gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function or the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the Pass Thru mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs labeled CX to C32.

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-6} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

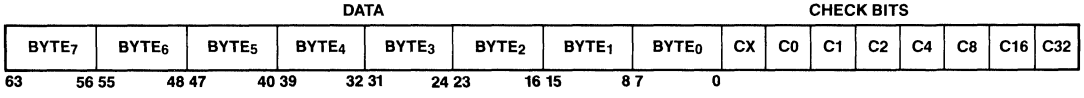
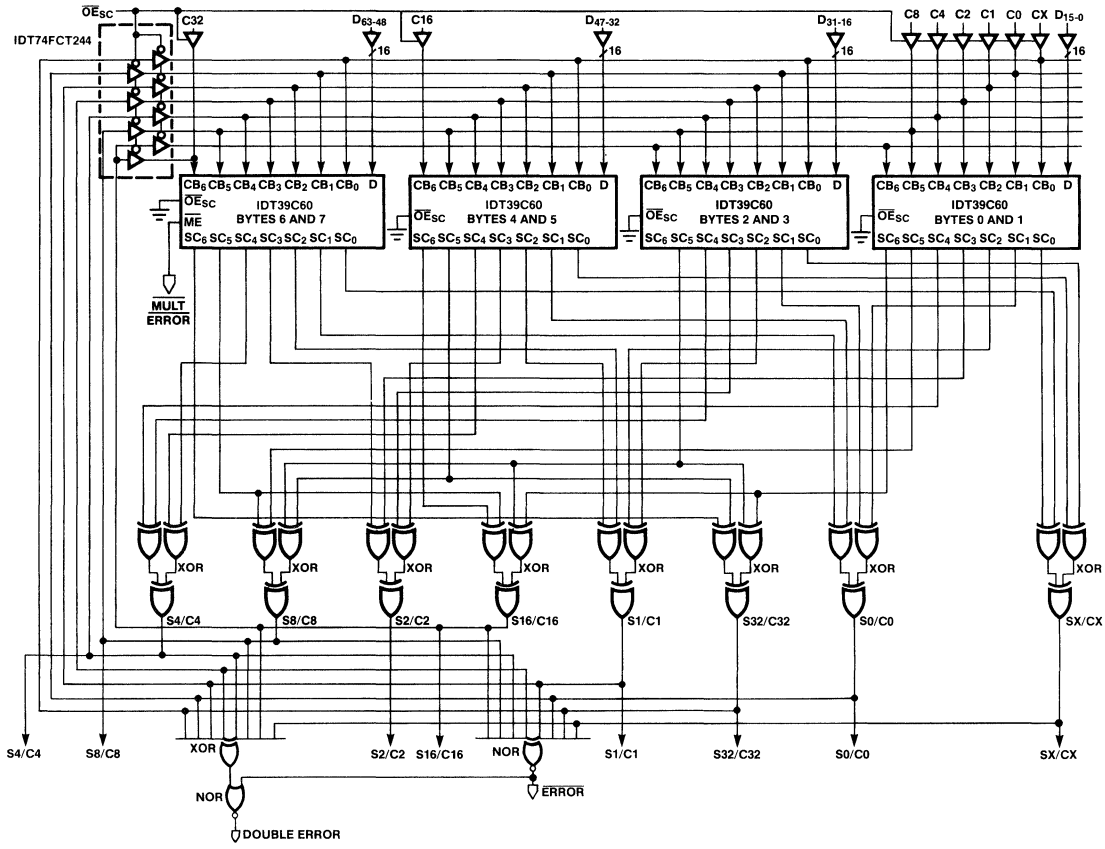


Figure 6. 64-Bit Data Format

TABLE 11. SYNDROME DECODE TO BIT-IN-ERROR

SYNDROME BITS																		
				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	35	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = More than two errors detected



NOTES: 1. In Pass Thru mode the contents of the Check Latch appear on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

TABLE 12. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FROM IDT39C60 AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer DELAY) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64-Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64-Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64-Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

TABLE 13. 64-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE: The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

TABLE 14.
DIAGNOSTIC LATCH LOADING — 64-BIT FORMAT

DATA BIT	INTERNAL FUNCTION
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1—CODE ID_0
9	Slice 0/1—CODE ID_1
10	Slice 0/1—CODE ID_2
11	Slice 0/1—DIAG $MODE_0$
12	Slice 0/1—DIAG $MODE_1$
13	Slice 0/1—CORRECT
14	Slice 0/1—PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3—CODE ID_0
25	Slice 2/3—CODE ID_1
26	Slice 2/3—CODE ID_2
27	Slice 2/3—DIAG $MODE_0$
28	Slice 2/3—DIAG $MODE_1$
29	Slice 2/3—CORRECT
30	Slice 2/3—PASS THRU

DATA BIT	INTERNAL FUNCTION
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5—CODE ID_0
41	Slice 4/5—CODE ID_1
42	Slice 4/5—CODE ID_2
43	Slice 4/5—DIAG $MODE_0$
44	Slice 4/5—DIAG $MODE_1$
45	Slice 4/5—CORRECT
46	Slice 4/5—PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7—CODE ID_0
57	Slice 6/7—CODE ID_1
58	Slice 6/7—CODE ID_2
59	Slice 6/7—DIAG $MODE_0$
60	Slice 6/7—DIAG $MODE_1$
61	Slice 6/7—CORRECT
62	Slice 6/7—PASS THRU
63	Don't Care

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 1111000 (SC, S0, S1, S2, S4, S8) is produced. The bit-in-error decoder receives the syndrome 11100 (S0, S1, S2, S4, S8) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibition correction when a multiple error occurs.

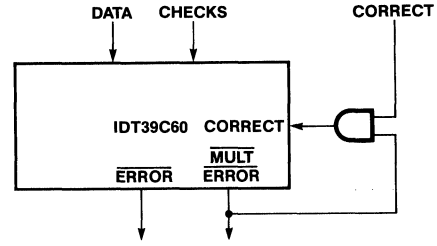


Figure 8. Inhibition of Data Modification

TOME (Three or More Errors)(1)

			S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			(2)S6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			S5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			S4	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S1	S2	S3																	
0	0	0		0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0
0	0	1		0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0		0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1		1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0		0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	1		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	1	0		1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	1	1		0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

NOTES:

1. (S6, S5, . . . S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes, the syndromes are input over the check bit lines. S6 ← C6, S5 ← C6, . . . S1 ← C1, S0 ← C0.
2. The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC Outputs

Tables 15, 16, 17, 18, 19 show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE 15.

GENERATE MODE (CHECK BITS)	CODE ID_{2-0}						
	000	010	011	100	101	110	111
SC_0←	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1←	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
SC_2←	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
SC_3←	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
SC_4←	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
SC_5←	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
SC_6←	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

Definitions

D_i ←(DATA$_i$ if LE_{IN} is HIGH or the output of bit i of the Data Input Latch if LE_{IN} is LOW)

C_i ←(CB_i if LE_{IN} is HIGH or the output of bit i of the Check Bit Latch if LE_{IN} is LOW)

DL_i ←Output of bit i of the Diagnostic Latch

S_i ←Internally generated syndromes (same as outputs of SC_i if outputs enabled)

PA ←$D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$

PB ←$D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$

PC ←$D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14}$

PD ←$D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$

PE ←$D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$

PF ←$D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15}$

PG_1←$D_1 \oplus D_4 \oplus D_6 \oplus D_7$

PG_2←$D_1 \oplus D_2 \oplus D_3 \oplus D_5$

PG_3←$D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$

PG_4←$D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

Error Signals

$\overline{ERROR}$: ← $\overline{(S6 \cdot (ID_1 + ID_2))} \cdot \overline{S5} \cdot \overline{S4} \cdot \overline{S3} \cdot \overline{S2} \cdot \overline{S1} \cdot \overline{S0}$ + GENERATE + INITIALIZE + PASSTHRU

$\overline{MULT\ ERROR}$:

(16 and 32-Bit Modes) ← $\overline{((S6 \cdot ID_1) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\ (\overline{ERROR})} + \overline{TOME}$ + GENERATE + PASSTHRU + INITIALIZE

$\overline{MULT\ ERROR}$: (64-Bit Modes) ← $\overline{TOME}$ + GENERATE + PASSTHRU + INITIALIZE

TABLE 16.

DETECT AND CORRECT MODES (SYNDROMES)	CODE ID_{2-0}						
	000	010	011[1]	100	101	110	111
SC_0←	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1←	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
SC_2←	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
SC_3←	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
SC_4←	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
SC_5←	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
SC_6←	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

NOTE:
1. In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 17.

DIAGNOSTIC READ MODE	CODE ID_{2-0}						
	000	010	011[1]	100	101	110	111
SC_0←	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
SC_1←	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_2$	PA	PA	PA
SC_2←	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
SC_3←	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
SC_4←	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
SC_5←	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
SC_6←	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

NOTE:
In Code ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Latch operates normally.

TABLE 18.

DIAGNOSTIC WRITE MODE	CODE ID_{2-0}						
	000	010	011[1]	100	101	110	111
SC_0←	DL_0	DL_0	CB_0	DL_0	1	1	1
SC_1←	DL_1	DL_1	CB_1	DL_1	1	1	1
SC_2←	DL_2	DL_2	CB_2	DL_2	1	1	1
SC_3←	DL_3	DL_3	CB_3	DL_3	1	1	1
SC_4←	DL_4	DL_4	CB_4	DL_4	1	1	1
SC_5←	DL_5	DL_5	CB_5	DL_5	1	1	1
SC_6←	1	DL_6	CB_6	1	1	DL_6	DL_7

NOTE:
In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Input Latch operates normally.

TABLE 19.

PASS THRU MODE	CODE ID_{2-0}						
	000	010	011[1]	100	101	110	111
SC_0←	C_0	C_0	CB_0	C_0	1	1	1
SC_1←	C_1	C_1	CB_1	C_1	1	1	1
SC_2←	C_2	C_2	CB_2	C_2	1	1	1
SC_3←	C_3	C_3	CB_3	C_3	1	1	1
SC_4←	C_4	C_4	CB_4	C_4	1	1	1
SC_5←	C_5	C_5	CB_5	C_5	1	1	1
SC_6←	1	C_6	CB_6	1	1	C_6	C_6

NOTE:
In CODE ID_{2-0} 011 the Check Bit Latch is forced transparent; the Data Input Latch operates normally.

TABLE 20. CODE ID_{2-0} = 000(1)

		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted S combinations are no correction.

TABLE 21. CODE ID_{2-0} = 010(1)

		CB6	0	0	0	0	1	1	1	1
		CB5	1	1	1	1	0	0	0	0
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 22. CODE ID_{2-0} = 011(1)

		S6	0	0	0	0	1	1	1	1
		S5	0	0	0	0	1	1	1	1
		S4	0	0	1	1	0	0	1	1
S2	S1	S3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted S combinations are no correction.

TABLE 23. CODE ID_{2-0} = 100(1)

		CB0	0	0	0	0	1	1	1	1
		CB6	0	0	0	0	1	1	1	1
		CB5	1	1	1	1	0	0	0	0
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 24. CODE ID_{2-0} = 101(1)

		CB0	0	0	0	0	1	1	1	1
		CB6	0	0	0	0	1	1	1	1
		CB5	0	0	0	0	1	1	1	1
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 25. CODE ID_{2-0} = 110(1)

		CB0	0	0	0	0	1	1	1	1
		CB6	1	1	1	1	0	0	0	0
		CB5	0	0	0	0	1	1	1	1
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		—	—	—	5	—	11	14	—
0	1		—	1	2	6	8	12	—	—
1	0		—	—	3	7	9	13	15	—
1	1		—	0	4	—	10	—	—	—

NOTE:
1. Unlisted CB combinations are no correction.

TABLE 26. CODE ID_{2-0} = 111(1)

		CB0	0	0	0	0	1	1	1	1
		CB6	1	1	1	1	0	0	0	0
		CB5	1	1	1	1	0	0	0	0
		CB4	0	0	1	1	0	0	1	1
CB2	CB1	CB3	0	1	0	1	0	1	0	1
0	0		—	11	14	—	—	—	—	5
0	1		8	12	—	—	—	1	2	6
1	0		9	13	15	—	—	—	3	7
1	1		10	—	—	—	—	0	4	—

NOTE:
1. Unlisted CB combinations are no correction.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTES:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_I or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-130	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{OP} = 0		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{OP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty Cycle V_{IN} = 3.4V, V_{IN} = 0	MIL.	—	60	100	
			COM'L.	—	60	85	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Clock Input frequency.

3

IDT39C60 INPUT/OUTPUT INTERFACE CIRCUITRY

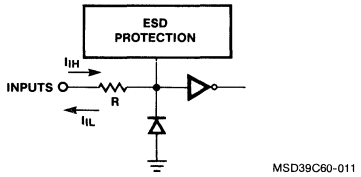


Figure 9. Input Structure (All Inputs)

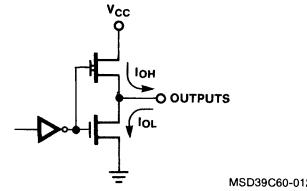


Figure 10. Output Structure

TEST LOAD CIRCUITS

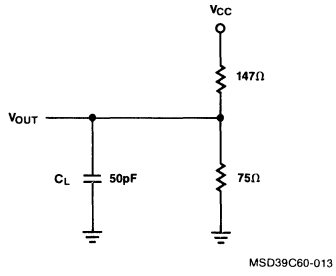


Figure 11. Output Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 11

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	20	30	20	23
CB_{0-6} (CODE ID_{2-0} 000,011)	14	25	20	23
CB_{0-6} (CODE ID_{2-0} 010,100, 101,110,111)	14	18	20	23
$\overline{GENERATE}$	15	25	14	17
CORRECT (Not Internal Control Mode)	—	20	—	—
DIAG MODE (Not Internal Control Mode)	22	25	18	21
PASS THRU (Not Internal Control Mode)	22	25	18	21
$CODE\ ID_{2-0}$	23	28	25	28
LE_{IN} (From latched to transparent)	22	32[1]	22	25
LE_{OUT} (From latched to transparent)	—	13	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	22	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	28	38	28	31
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	28	38	28	31

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 12 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	24	2
CB_{0-6} (CODE ID) 000, 011)	LE_{OUT}	21	0
CB_{0-6} (CODE ID 100, 101, 110, 111)	LE_{OUT}	21	0
$\overline{GENERATE}$	LE_{OUT}	26	0
CORRECT	LE_{OUT}	22	0
DIAG MODE	LE_{OUT}	22	0
PASS THRU	LE_{OUT}	22	0
$CODE\ ID_{2-0}$	LE_{OUT}	25	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-15}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	24	21
$\overline{OE}_{SC}$	SC_{0-6}	24	21

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

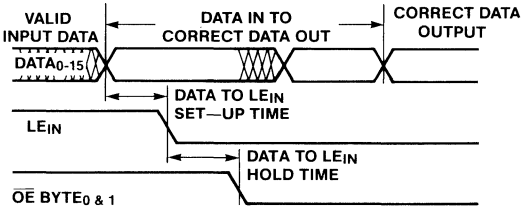


Figure 12. MSD39C60-014

IDT39C60A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60A over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	22	35	24	27
CB_{0-6} (CODE ID_{2-0} 000,011)	17	28	24	27
CB_{0-6} (CODE ID_{2-0} 010,100, 101,110,111)	17	20	24	27
$\overline{GENERATE}$	20	28	18	21
CORRECT (Not Internal Control Mode)	—	25	—	—
DIAG MODE (Not Internal Control Mode)	25	28	21	24
PASS THRU (Not Internal Control Mode)	25	28	21	24
CODE ID_{2-0}	26	31	28	31
LE_{IN} (From latched to transparent)	24	37(1)	26	29
LE_{OUT} (From latched to transparent)	—	16	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	37	26	29
Internal Control Mode: LE_{DIAG} (From latched to transparent)	30	43	32	35
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	30	43	32	35

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 13 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	5	3
CB_{0-6}	LE_{IN}	5	3
$DATA_{0-15}$	LE_{OUT}	27	2
CB_{0-6} (CODE ID) 000, 011)	LE_{OUT}	24	0
CB_{0-6} (CODE ID 100, 101, 110, 111)	LE_{OUT}	24	0
$\overline{GENERATE}$	LE_{OUT}	29	0
CORRECT	LE_{OUT}	25	0
DIAG MODE	LE_{OUT}	25	0
PASS THRU	LE_{OUT}	25	0
CODE ID_{2-0}	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	30	0
$DATA_{0-15}$	LE_{DIAG}	5	3

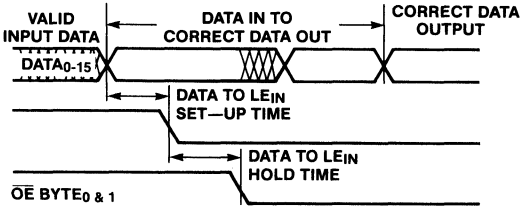
OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	28	25
$\overline{OE}_{SC}$	SC_{0-6}	28	25

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12



MSD39C60-014

Figure 13.

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	28	52	25	50
CB_{0-6} ($CODE\ ID_{2-0}$ 000,011)	23	50	23	47
CB_{0-6} ($CODE\ ID_{2-0}$ 010,100, 101,110,111)	28	34	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	—	45	—	—
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
$CODE\ ID_{2-0}$	61	90	60	80
LE_{IN} (From latched to transparent)	39	72[1]	39	59
LE_{OUT} (From latched to transparent)	—	31	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 14 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	34	5
CB_{0-6} (CODE ID) 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 100, 101, 110, 111)	LE_{OUT}	27	0
$\overline{GENERATE}$	LE_{OUT}	42	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASS THRU	LE_{OUT}	26	0
$CODE\ ID_{2-0}$	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

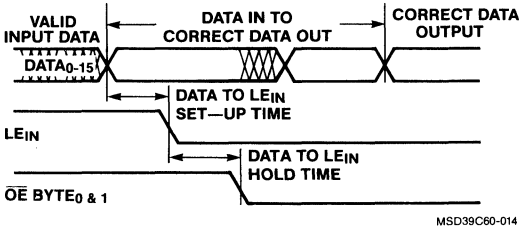


Figure 14.

IDT39C60-1 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60-1 over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	31	59	28	56
CB_{0-6} ($CODE\ ID_{2-0}$ 000,011)	25	55	25	50
CB_{0-6} ($CODE\ ID_{2-0}$ 010,100, 101,110,111)	30	38	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	—	49	—	—
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASS THRU (Not Internal Control Mode)	39	51	34	54
$CODE\ ID_{2-0}$	69	100	68	90
LE_{IN} (From latched to transparent)	39	82(1)	43	66
LE_{OUT} (From latched to transparent)	—	33	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 15 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	39	5
CB_{0-6} (CODE ID) 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 100, 101, 110, 111)	LE_{OUT}	30	0
$\overline{GENERATE}$	LE_{OUT}	46	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASS THRU	LE_{OUT}	30	0
$CODE\ ID_{2-0}$	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}\ BYTE_0$, $\overline{OE}\ BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

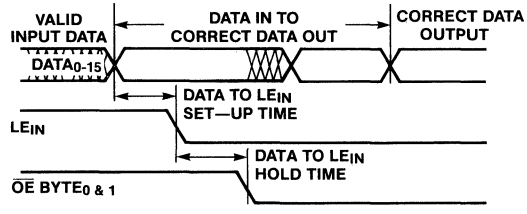


Figure 15.

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65(1)	32	50
CB_{0-6} (CODE ID_{2-0} 000,011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010,100, 101,110,111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	—	45	—	—
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE_{IN} (From latched to transparent)	39	72(1)	39	59
LE_{OUT} (From latched to transparent)	—	31	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE_{DIAG} (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 16 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	6	7
CB_{0-6}	LE_{IN}	5	6
$DATA_{0-15}$	LE_{OUT}	44	5
CB_{0-6} (CODE ID) 000, 011)	LE_{OUT}	35	0
CB_{0-6} (CODE ID 100, 101, 110, 111)	LE_{OUT}	27	0
$\overline{GENERATE}$	LE_{OUT}	42	0
CORRECT	LE_{OUT}	26	1
DIAG MODE	LE_{OUT}	69	0
PASS THRU	LE_{OUT}	26	0
CODE ID_{2-0}	LE_{OUT}	81	0
LE_{IN}	LE_{OUT}	51	5
$DATA_{0-15}$	LE_{DIAG}	6	8

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	30	30
$\overline{OE}_{SC}$	SC_{0-6}	30	30

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

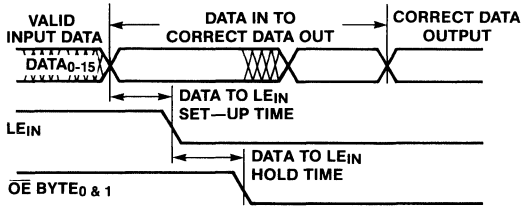


Figure 16.

IDT39C60 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT39C60 over the military operating range of -55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in nanoseconds, with inputs switching between 0V and 3V at 1V per nanosecond and measurements made at 1.5V. All outputs have maximum DC load. V_{CC} equal to 5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73(1)	36	56
CB_{0-6} (CODE ID_{2-0} 000,011)	30	61	31	50
CB_{0-6} (CODE ID_{2-0} 010,100, 101,110,111)	30	50	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	—	49	—	—
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASS THRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE_{IN} (From latched to transparent)	44	82(1)	43	66
LE_{OUT} (From latched to transparent)	—	33	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE_{DIAG} (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 17 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-15}$	LE_{IN}	7	7
CB_{0-6}	LE_{IN}	5	7
$DATA_{0-15}$	LE_{OUT}	50	5
CB_{0-6} (CODE ID) 000, 011)	LE_{OUT}	38	0
CB_{0-6} (CODE ID 100, 101, 110, 111)	LE_{OUT}	30	0
$\overline{GENERATE}$	LE_{OUT}	46	0
CORRECT	LE_{OUT}	28	1
DIAG MODE	LE_{OUT}	84	0
PASS THRU	LE_{OUT}	30	0
CODE ID_{2-0}	LE_{OUT}	89	0
LE_{IN}	LE_{OUT}	59	5
$DATA_{0-15}$	LE_{DIAG}	7	9

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE	DISABLE
$\overline{OE}$ $BYTE_0$, $\overline{OE}$ $BYTE_1$	$DATA_{0-15}$	35	35
$\overline{OE}_{SC}$	SC_{0-6}	35	35

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

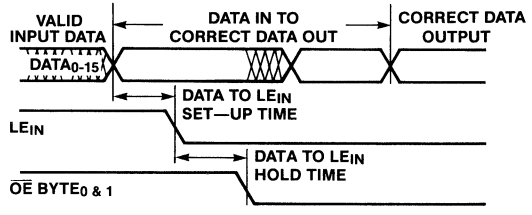


Figure 17.

Integrated Device Technology, Inc.

16-WORD BY 4-BIT DUAL-PORT RAM

ADVANCE INFORMATION
IDT39C705A/B
IDT39C707/A

FEATURES:

- Fast
  - —Available in either industry-standard speed or 20% speed upgraded versions
- Low-power CEMOS™
  - —Military — 50mA (max.)
  - —Commercial — 40mA (max.)
- 16-word x 4-bit, dual-port CMOS RAM
- Non-inverting data output with respect to data input
- Easily cascadable with separate Chip Select and Write Enable
- Separate 4-bit latches with enables for each output port (IDT39C707/A has separate output control)
- IDT39C705A/B pin-compatible to all versions of the 29705
- IDT39C707/A pin-compatible to all versions of the 29707
- Available in 28-pin DIP and LCC
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C705s are high-performance 16-word by 4-bit, dual-port RAMs. Addressing any of the 16-words is performed via the 4-bit A address field with the data appearing on the A output port. The same respective operation holds true for the B address input/output port and can happen simultaneously with the A-port operation. New incoming data is written into the 4-bit RAM word selected by the B address. The D inputs are used to load new data into the device.

Featured are two separate output ports which allow any two 4-bit words to be read from these outputs simultaneously. Also featured is a 4-bit latch for each of the two output ports with a common Latch Enable (LE) input being used to control all eight latches. Two Write Enable ($\overline{WE}$) inputs are designed such that Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be connected to the RAM to operate in an edge-triggered mode. The Write Enable inputs control the writing of new data into the RAM. Data is written into the B address field when both Write Enables are LOW. If either of the Write Enables are HIGH, no data is written into the RAM.

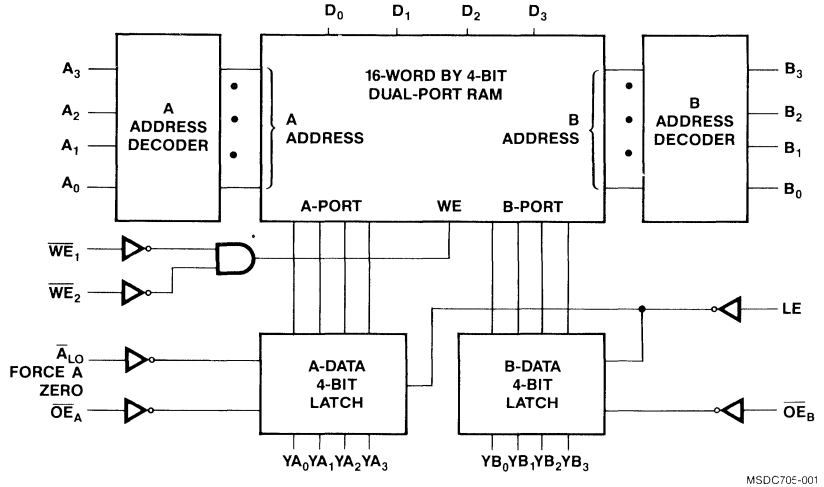
Three-state outputs allow several devices to be easily cascaded for increased memory size. When $\overline{OE}_A$ input is HIGH, the A output port is in the high impedance mode. The same respective operation occurs for the $\overline{OE}_B$ input.

The IDT39C707s function identically to the IDT39C705s, except each output port has a separate Latch Enable (LE) input. Also, an extra Write Enable ($\overline{WE}$) may be connected directly to the IEN of the IDT39C203/A for improved cycle times when compared to the IDT39C705s. The $\overline{WE}$/BLE input can then be connected directly to the system clock.

These performance-enhanced, pin-compatible replacements for all respective versions of the 29705s and 29707s are fabricated using IDTs high-speed, high-reliability CEMOS technology. Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications.

3

FUNCTIONAL BLOCK DIAGRAM
IDT39C705A/B



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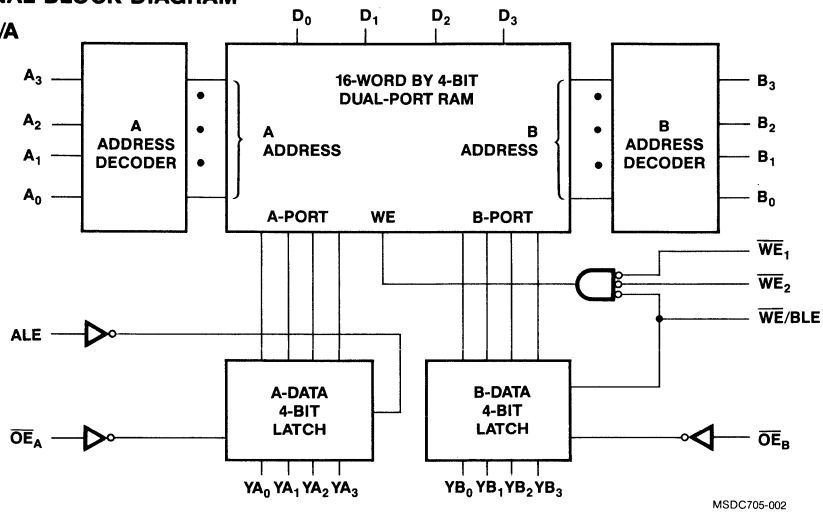
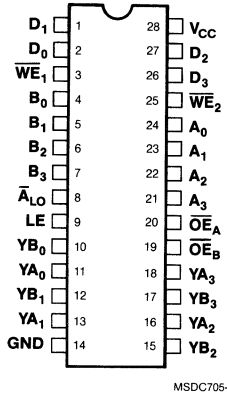
FUNCTIONAL BLOCK DIAGRAM

IDT39C707/A



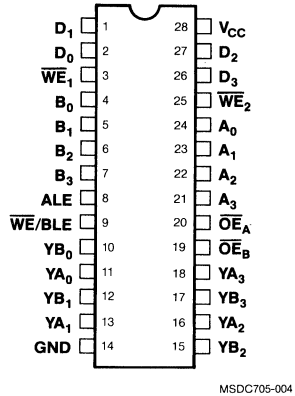
PIN CONFIGURATIONS

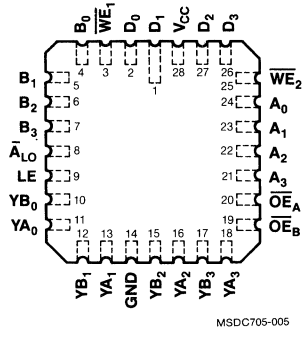
IDT39C705A/B



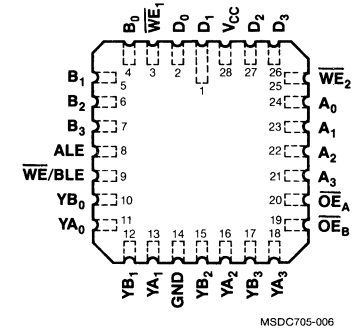
DIP
TOP VIEW

IDT39C707/A





LCC
TOP VIEW



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS MICROCYCLE LENGTH CONTROLLER

ADVANCE INFORMATION
IDT49C25

MICROSLICE™ PRODUCT

FEATURES:

- Similar function to AMD's Am2925 bipolar controller with improved speeds and output drive over full temperature and voltage supply extremes
- Four microcode-controlled clock outputs allow clock cycle length control for 15 to 30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- System controls for $\overline{RUN}/\overline{HALT}$ and Single Step
  —Switch-debounced inputs provide flexible halt controls
- Low input/output capacitance
  —6pF inputs (typ.)
  —8pF outputs (typ.)
- CMOS power levels
- Available in 300 mil 24-pin THINDIP package
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar Am2900 series (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available

DESCRIPTION:

The IDT49C25 is a single-chip general purpose clock generator/driver built using advanced CEMOS™, a dual metal CMOS technology. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meets a variety of system speed requirements.

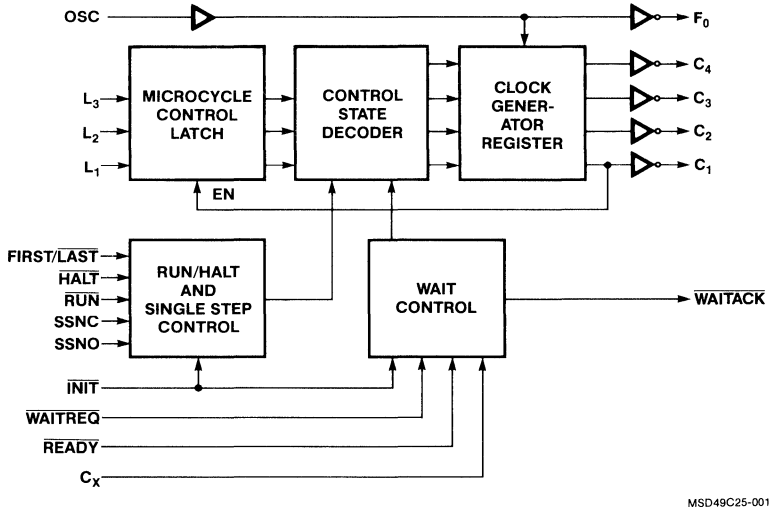
The IDT49C25 generates four different simultaneous clock output waveforms tailored to meet the needs of the IDT39C000 CMOS family and other MOS and bipolar microprocessor-based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1, L_2 and L_3.

A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs C_1, C_2, C_3 and C_4.

System control functions include $\overline{RUN}$, $\overline{HALT}$, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/$\overline{LAST}$ input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. $\overline{WAITACK}$ indicates that the IDT49C25 is in a wait state.

3

FUNCTIONAL BLOCK DIAGRAM



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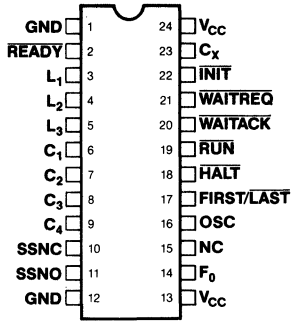
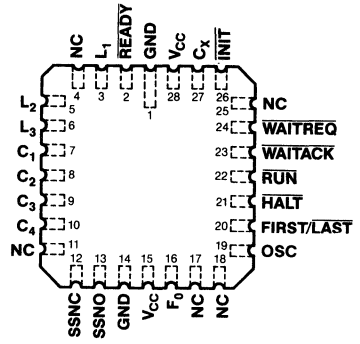
PIN CONFIGURATIONS



DIP
TOP VIEW

MSD49C25-002



LCC
TOP VIEW

MSD49C25-003

Integrated Device Technology, Inc

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C401
IDT49C401A

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - —30% faster than four 2901Cs and one 2902A
- Low-power CEMOS™
  - —Military — 150mA (max.)
  - —Commercial — 125mA (max.)
- Functionally equivalent to four 2901s and on 2902
- Pin-compatible, performance-enhanced replacement for IMI4X2901B
- Independent, simultaneous access to two 16-word x 16-bit register files
- Expanded destination functions with eight new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Cascadable
- Available in a 64-pin DIP
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

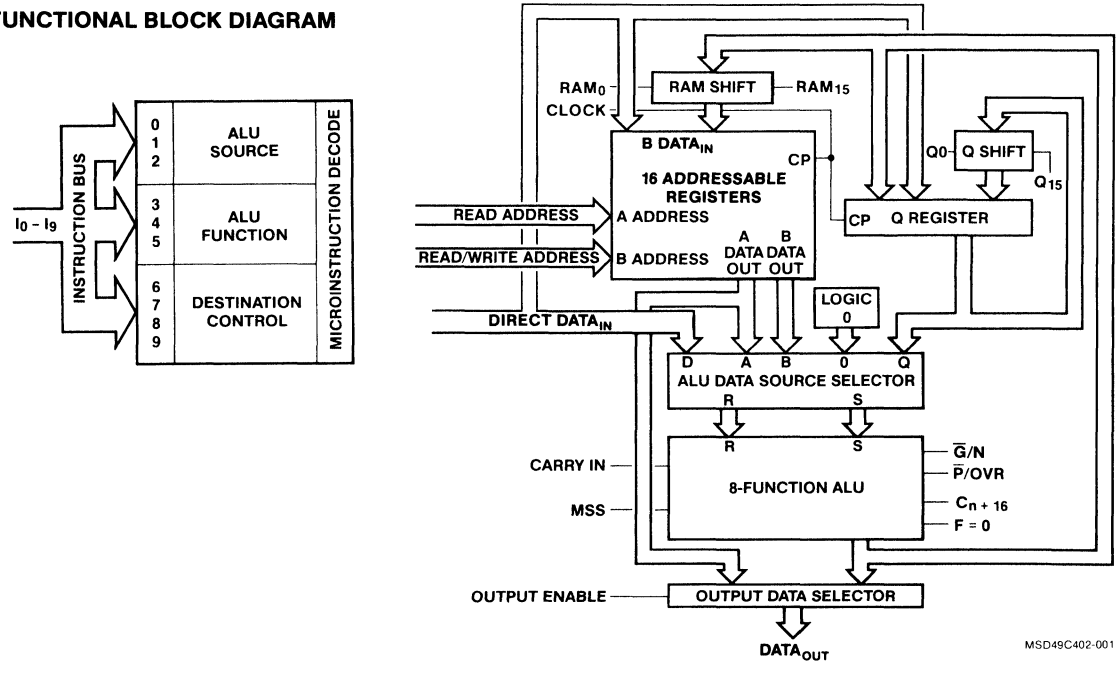
The IDT49C401s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902, with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

The IDT49C401s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0,I_1,I_2) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field (I_3,I_4,I_5) used to control the eight possible functions of the ALU, and; (c) sixteen destination control functions which are selected by the microcode inputs (I_6,I_7,I_8,I_9). Eight of the sixteen destination control functions reflect the standard 2901 operation, while the other eight additional destination control functions allow for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and new combinations of destination functions with the RAM A-port output available at the Y output pins of the device. Also featured is an on-chip dual-port RAM that contains 16 words by 16 bits.

The IDT49C401s are fabricated using CEMOS, a single poly, double metal CMOS technology designed for high-performance and high-reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

3

FUNCTIONAL BLOCK DIAGRAM



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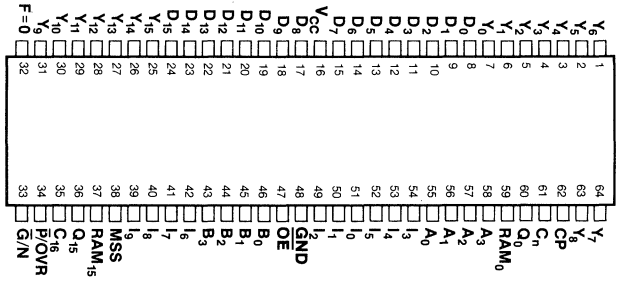
PIN CONFIGURATION



DIP
TOP VIEW

DEVICE ARCHITECTURE

The IDT49C401 CMOS Bit-Slice Microprocessors are configured sixteen bits wide and are cascadable to any number of bits (16, 32, 48, 64). Key elements which make up these sixteen-bit slice microprocessors are the (1) register file (16 x 16 dual-port RAM) with shifter, (2) ALU, and (3) Q Register and shifter.

REGISTER FILE—A 16-bit data word from one of the 16 RAM registers can be read from the A-port as selected by the 4-bit A address field. Simultaneously, the same data word or any other word from the 16 RAM registers can be read from the B-port as selected by the 4-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A-port and B-port data during the clock (CP) LOW time, eliminating any data races. During clock HIGH these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involve the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output while the RAM_{15} I/O input is selected as the input to the MSB.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0,1,2)}$ inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3,4,5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least-significant slices, the MSS pin is programmed LOW selecting the carry-generate ($\overline{G}$) and carry-propagate ($\overline{P}$) output functions to be used by carry-lookahead logic. For the most-significant slice, MSS is programmed high, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign-bit (F_{15}) allows the ALU sign-bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign-bit, as logically determined from the Exclusive-OR of the carry-in and carry-out of the most-significant bit of the ALU. For all 16-bit applications, the MSS pin on the IDT49C401s is tied high or not connected since only one device is needed. With MSS open or tied high, internal circuitry will direct pins 33 and 34 to function as F_{15} and OVR, respectively. It is in this 16-bit operating mode that the IDT49C401s function identically to the IMI4X2901B. The ALU data outputs are available at the three-state outputs $Y_{(0-15)}$, or as inputs to the RAM register file and Q Register under control of the $I_{(6,7,8,9)}$ instruction inputs.

Q REGISTER—The Q Register is a separate 16-bit register intended for multiplication and division routines, and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6,7,8,9)}$ inputs.

The clock input of the IDT49C401 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6,7,8,9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs to the register file which selects one register and displays its contents through the A-port.
B_0-B_3	I	Four address inputs to the register file which selects one of the registers in the file, the contents of which are displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0,1,2)}$, what function the ALU will perform $I_{(3,4,5)}$, and what data is to be deposited in the Q Register or the register file $I_{(6,7,8,9)}$. Original 2901 destinations are selected if I_9 is disconnected. In this mode, proper I_9 bias is controlled by an internal pullup resistor to V_{CC}.
D_0-D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0-Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A-port of the register stack. This is determined by the destination code $I_{(6,7,8,9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F=0	O	Open drain output which goes HIGH if the F_0-F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the internal ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6,7,8,9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6,7,8,9)}$ indicates an up shift, the three-state outputs are enabled and the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry-lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64x16 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice and will define pins as OVR and F_{15}.

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R $\vee$ S
AND	H	L	L	4	R AND S	R $\wedge$ S
NOTRS	H	L	H	5	R AND S	$\overline{R}$ $\wedge$ S
EXOR	H	H	L	6	R EX-OR S	$\overline{R \vee S}$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \vee S}$

ALU ARITHMETIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$ $I_{2,1,0}$	C_n = L		C_n = H	
	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	A + Q	ADD Plus One	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$ $I_{2,1,0}$	GROUP	FUNCTION
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \triangledown Q$
6 1		$A \triangledown B$
6 5		$D \triangledown A$
6 6		$D \triangledown Q$
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	Q
7 3		B
7 4		A
7 7		D
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL 0	1	2	3	4	5	6	7
		ALU SOURCE							
		A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C_n = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C_n = L S Minus R	Q - A - 1	B - A - 1	Q - 1	B - 1	A - 1	A - D - 1	Q - D - 1	-D - 1
	C_n = H	Q - A	B - A	Q	B	A	A - D	Q - D	-D
2	C_n = L R Minus S	A - Q - 1	A - B - 1	-Q - 1	-B - 1	-A - 1	D - A - 1	D - Q - 1	D - 1
	C_n = H	A - Q	A - B	-Q	-B	-A	D - A	D - Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ▽ Q	A ▽ B	Q	B	A	D ▽ A	D ▽ Q	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; - = Minus; ∧ = AND; ▽ = EX-OR; ∨ = OR

ALU DESTINATION CONTROL

MNE-MONIC	MICROCODE I_9	I_8	I_7	I_6	HEX CODE	RAM FUNCTION SHIFT	RAM FUNCTION LOAD	Q REGISTER FUNCTION SHIFT	Q REGISTER FUNCTION LOAD	Y OUTPUT	RAM SHIFTER RAM_0	RAM SHIFTER RAM_{15}	Q SHIFTER Q_0	Q SHIFTER Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	Existing 2901 Functions
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D→B	NONE	F→Q	F	X	X	X	X	
DFA	L	L	L	H	1	NONE	D→B	NONE	F→Q	A	X	X	X	X	
FDF	L	L	H	L	2	NONE	F→B	NONE	D→Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F→B	NONE	D→Q	A	X	X	X	X	New Added IDT49C401 Functions
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2→Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D→B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q→Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D→Q	F	X	X	X	Q_{15}	

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB; DOWN is toward LSB.

3

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	1.0	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-1.0	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-135	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	70	150	
			COM'L.	—	70	125	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input frequency.

IDT49C401A AC ELECTRICAL CHARACTERISTICS

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C401A over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

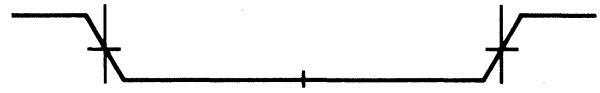
CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	28	24	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=C32 or E32)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	36	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) G, P		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	—	—	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	—	—	ns
C_n	29	26	—	—	26	24	25	23	20	18	29	26	23	21	—	—	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	—	—	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	—	—	ns
$I_{6,7,8,9}$	25	23	—	—	—	—	—	—	—	—	—	—	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock —	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	11	10	0[3]	0[3]	24[4]	21[4]	0	0	ns
B Destination Address	11	10	Do not change[2]				0	0	ns
D	—[1]	—	—	—	12/22[5]	10/20[5]	0	0	ns
C_n	—	—	—	—	17	15	0	0	ns
$I_{0,1,2}$	—	—	—	—	28	25	0	0	ns
$I_{3,4,5}$	—	—	—	—	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change[2]				0	0	ns
$RAM_{0,15}$,$Q_{0,15}$	—	—	—	—	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C401 AC ELECTRICAL CHARACTERISTICS

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C401 over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

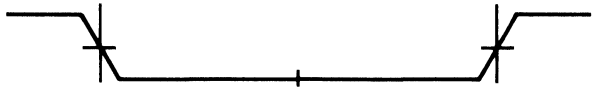
	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) G, P		(MSS = H) F_{i5}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	—	—	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	—	—	ns
C_n	29	26	—	—	29	26	27	25	20	18	29	26	23	21	—	—	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	—	—	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	—	—	ns
$I_{6,7,8,9}$	26	24	—	—	—	—	—	—	—	—	—	—	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock —	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	20	18	0[3]	0[3]	50[4]	48[4]	0	0	ns
B Destination Address	20	18	Do not change[2]				0	0	ns
D	—[1]	—	—	—	30/40[5]	26/36[5]	0	0	ns
C_n	—	—	—	—	35	32	0	0	ns
$I_{0,1,2}$	—	—	—	—	45	41	0	0	ns
$I_{3,4,5}$	—	—	—	—	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change[2]				0	0	ns
$RAM_{0,15}, Q_{0,15}$	—	—	—	—	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q REGISTER). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q REGISTER).

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IDT49C401
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	25	23	25	23

IDT49C401A
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
$\overline{OE}$	Y	22	20	20	18

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 1

TEST LOAD CIRCUITS

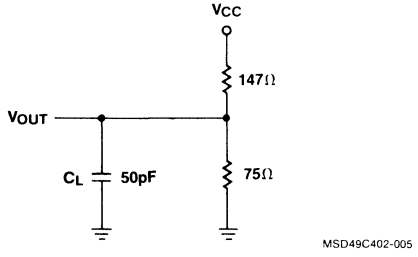


Figure 1. Switching Test Circuit (all outputs)

INPUT/OUTPUT INTERFACE CIRCUITRY

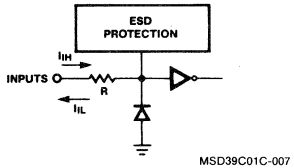


Figure 2. Input Structure (All Inputs)

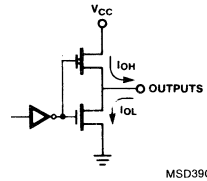


Figure 3. Output Structure (All Outputs Except F = 0)

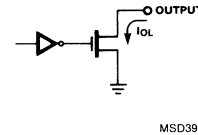


Figure 4. Output Structure (F = Only)

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A

MICROSLICE™ PRODUCT

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402A 45% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- High-performance, low-power CEMOS™ II
- Fully cascadable
- 68-pin PGA, DIP (600 mil, 70 mil centers), LCC (25 and 50 mil centers)
- Military product 100% screened to MIL-STD-833, Class B

DESCRIPTION:

The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902, with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

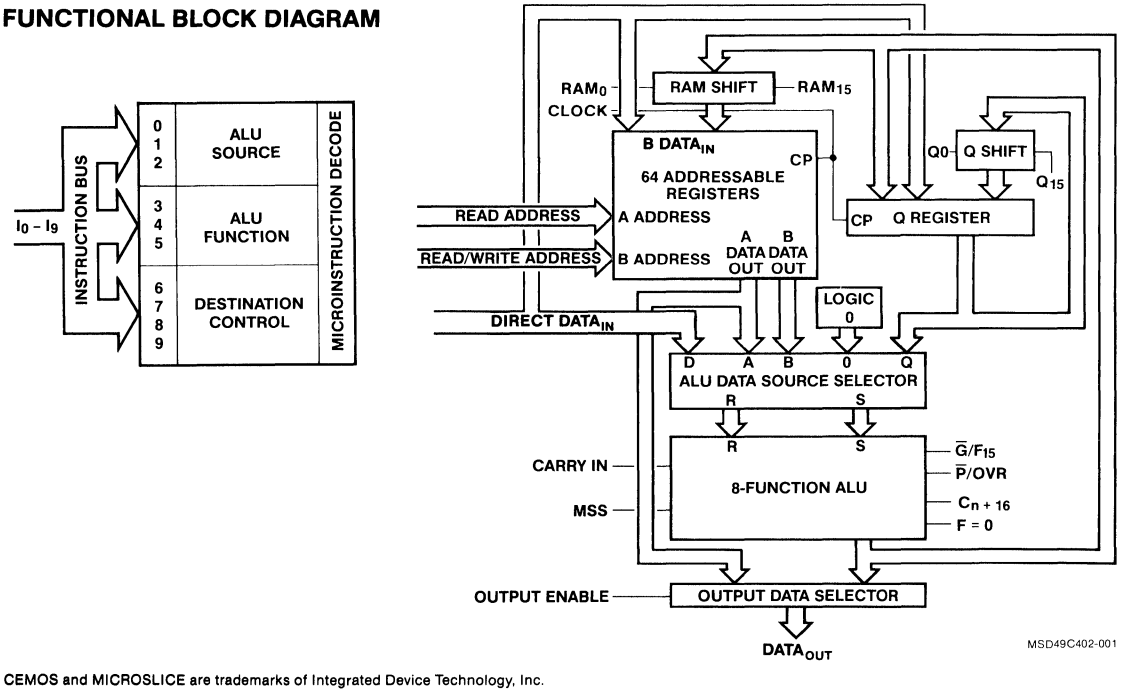
The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: (a) a 3-bit instruction field (I_0,I_1,I_2) which controls the source operand selection for the ALU; (b) a 3-bit microinstruction field (I_3,I_4,I_5) used to control the eight possible functions of the ALU; (c) eight destination control functions which are selected by the microcode inputs (I_6,I_7,I_8); and (d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7, and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and new combinations of destination functions with the RAM A-port output available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64 words by 16 bits, which is four times the number of working registers in a 2901.

The IDT49C402s are fabricated using CEMOS II, a single poly, double metal CMOS technology designed for high-performance and high-reliability. These performance enhanced devices feature both bipolar speed and bipolar output drive capabilities while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

3

FUNCTIONAL BLOCK DIAGRAM



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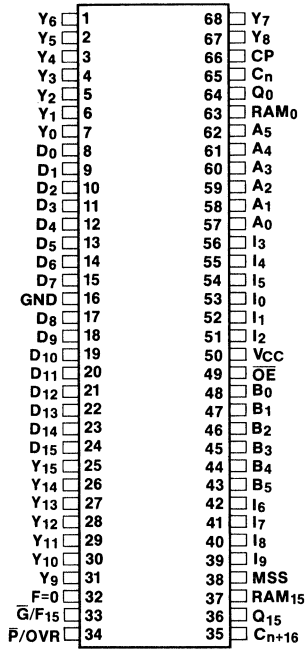
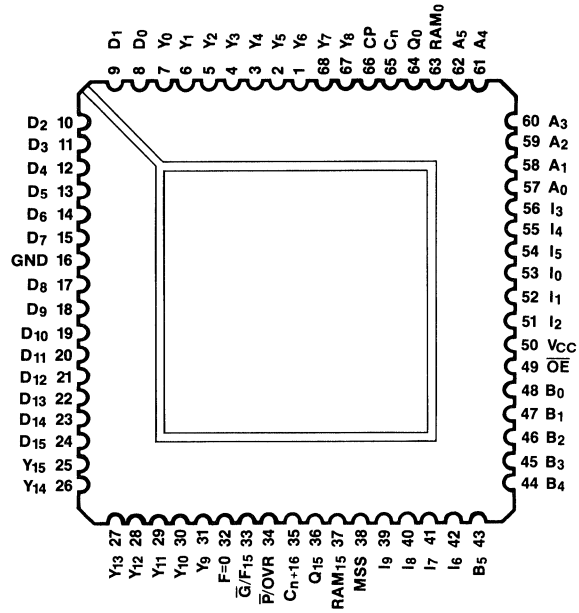
PIN CONFIGURATIONS



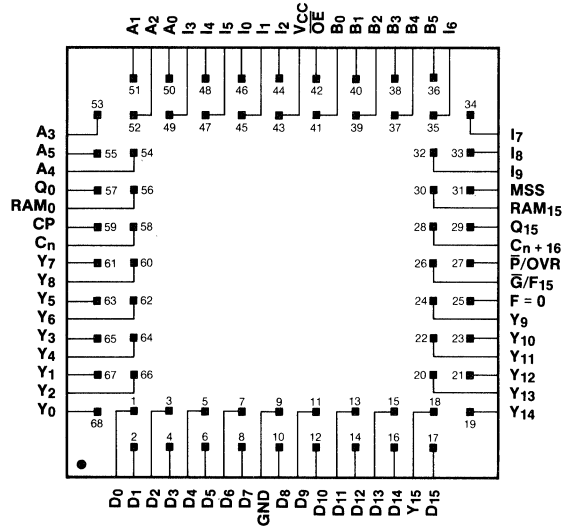
MSD49C402-002

DIP
TOP VIEW



MSD49C402-003

LCC
TOP VIEW



MSD49C402-004

PGA
TOP VIEW

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_5	I	Six address inputs to the register file which selects one register and displays its contents through the A-port.
B_0-B_5	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which are displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0-I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0,1,2)}$; what function the ALU will perform $I_{(3,4,5)}$; and what data is to be deposited in the Q Register or the register file $I_{(6,7,8,9)}$. Original 2901 destinations are selected if I_9 is disconnected. In this mode, proper I_9 bias is controlled by an internal pullup resistor to V_{CC}.
D_0-D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0-Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A-port of the register stack. This is determined by the destination code $I_{(6,7,8,9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F=0	O	Open drain output which goes HIGH if the F_0-F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the internal ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6,7,8,9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6,7,8,9)}$ indicates an up shift, the three-state outputs are enabled and the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry-lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64x16 RAM which compromises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice.

DEVICE ARCHITECTURE

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this sixteen-bit-slice microprocessor are the (1) register file (64 x 16 dual-port RAM) with shifter; (2) ALU; and (3) Q Register and shifter.

REGISTER FILE—A 16-bit data word from one of the 64 RAM registers can be read from the A-port as selected by the 6-bit A address field. Simultaneously, the same data word or any other word from the 64 RAM registers can be read from the B-port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A-port and B-port data during the clock (CP) LOW time, eliminating any data races. During clock HIGH these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involve the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output while the RAM_{15} I/O input is selected as the input to the MSB.

ALU—The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0,1,2)}$ inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3,4,5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least-significant slices, the MSS pin is programmed LOW selecting the carry-generate ($\overline{G}$) and carry-propagate ($\overline{P}$) output functions to be used by carry-

DEVICE ARCHITECTURE (CONT'D)

lookahead logic. For the most-significant slice, MSS is programmed high, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign-bit (F_{15}) allows the ALU sign-bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign-bit, as logically determined from the Exclusive-OR of the carry-in and carry-out of the most-significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0-15)}$, or as inputs to the RAM register file and Q Register under control of the $I_{(6,7,8,9)}$ instruction inputs.

Q REGISTER—The Q Register is a separate 16-bit file intended for multiplication and division routines, and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6,7,8,9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6,7,8,9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

ALU ARITHMETIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$, $I_{2,1,0}$	C_n = L		C_n = H	
	GROUP	FUNCTION	GROUP	FUNCTION
0 0	ADD	A + Q	ADD Plus One	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICROCODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICROCODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ▽ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

ALU LOGIC MODE FUNCTIONS

OCTAL $I_{5,4,3}$, $I_{2,1,0}$	GROUP	FUNCTION
4 0	AND	A ∧ Q
4 1		A ∧ B
4 5		D ∧ A
4 6		D ∧ Q
3 0	OR	A ∨ Q
3 1		A ∨ B
3 5		D ∨ A
3 6		D ∨ Q
6 0	EX-OR	A ▽ Q
6 1		A ▽ B
6 5		D ▽ A
6 6		D ▽ Q
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$ ∧ Q
5 1		$\overline{A}$ ∧ B
5 5		$\overline{D}$ ∧ A
5 6		$\overline{D}$ ∧ Q

SOURCE OPERAND AND ALU FUNCTION MATRIX

OCTAL $I_{5,4,3}$	ALU FUNCTION	$I_{2,1,0}$ OCTAL							
		0	1	2	3	4	5	6	7
		ALU SOURCE							
		A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q - A - 1 Q - A	B - A - 1 B - A	Q - 1 Q	B - 1 B	A - 1 A	A - D - 1 A - D	Q - D - 1 Q - D	-D - 1 -D
2	C_n = L R Minus S C_n = H	A - Q - 1 A - Q	A - B - 1 A - B	-Q - 1 -Q	-B - 1 -B	-A - 1 -A	D - A - 1 D - A	D - Q - 1 D - Q	D - 1 D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \triangledown Q$	$A \triangledown B$	Q	B	A	$D \triangledown A$	$D \triangledown Q$	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; - = Minus; $\wedge$ = AND; $\triangledown$ = EX-OR; $\vee$ = OR

ALU DESTINATION CONTROL

MNE-MONIC	MICROCODE					RAM FUNCTION		Q REGISTER FUNCTION		Y OUT-PUT	RAM SHIFTER		Q SHIFTER		
	I_9	I_8	I_7	I_6	HEX CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	Existing 2901 Functions
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D→B	NONE	F→Q	F	X	X	X	X	
DFA	L	L	L	H	1	NONE	D→B	NONE	F→Q	A	X	X	X	X	
FDF	L	L	H	L	2	NONE	F→B	NONE	D→Q	F	X	X	X	X	
FDA	L	L	H	H	3	NONE	F→B	NONE	D→Q	A	X	X	X	X	New Added IDT49C402 Functions
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2→Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D→B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q→Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D→Q	F	X	X	X	Q_{15}	

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB; DOWN is toward LSB.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		—	-30	-130	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	80	150	
			COM'L.	—	80	125	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(\ _{CP})$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input frequency.

3

IDT49C402A AC ELECTRICAL CHARACTERISTICS

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

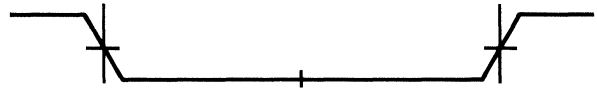
	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	28	24	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=C32 or E32)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	36	31	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	—	—	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	—	—	ns
C_n	29	26	—	—	26	24	25	23	20	18	29	26	23	21	—	—	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	—	—	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	—	—	ns
$I_{6,7,8,9}$	25	23	—	—	—	—	—	—	—	—	—	—	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock ⎍	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP:



INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	11	10	0[3]	0[3]	21, 10 + TPWL[4]		0	0	ns
B Destination Address	11	10	Do not change[2]				0	0	ns
D	—[1]	—	—	—	12/22[5]	10/20[5]	0	0	ns
C_n	—	—	—	—	17	15	0	0	ns
$I_{0,1,2}$	—	—	—	—	28	25	0	0	ns
$I_{3,4,5}$	—	—	—	—	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change[2]				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	—	—	—	—	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).

IDT49C402
AC ELECTRICAL CHARACTERISTICS
(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the -55°C to +125°C and 0°C to +70°C temperature ranges. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

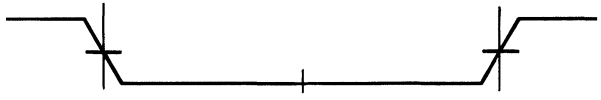
CYCLE TIME AND CLOCK CHARACTERISTICS

	MIL.	COM'L.	UNITS
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I=C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	30	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

COMBINATIONAL PROPAGATION DELAYS[1] (C_L = 50pF)

FROM INPUT	TO OUTPUT																UNIT
	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	—	—	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	—	—	ns
C_n	29	26	—	—	29	26	27	25	20	18	29	26	23	21	—	—	ns
$I_{0,1,2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	—	—	ns
$I_{3,4,5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	—	—	ns
$I_{6,7,8,9}$	26	24	—	—	—	—	—	—	—	—	—	—	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ns
Clock ⎍	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

INPUT	SET-UP TIME BEFORE H→L		HOLD TIME AFTER H→L		SET-UP TIME BEFORE L→H		HOLD TIME AFTER L→H		UNIT
	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	
A,B Source Address	20	18	0[3]	0[3]	50, 20 + TPWL[4]		0	0	ns
B Destination Address	20	18	Do not change[2]				0	0	ns
D	—[1]	—	—	—	30/40[5]	26/36[5]	0	0	ns
C_n	—	—	—	—	35	32	0	0	ns
$I_{0,1,2}$	—	—	—	—	45	41	0	0	ns
$I_{3,4,5}$	—	—	—	—	45	41	0	0	ns
$I_{6,7,8,9}$	12	11	Do not change[2]				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	—	—	—	—	12	11	0	0	ns

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q REGISTER).

IDT49C402A
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
OE	Y	22	20	20	18

IDT49C402
OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

INPUT	OUTPUT	ENABLE		DISABLE	
		MIL.	COM'L.	MIL.	COM'L.
OE	Y	25	23	25	23

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 1

TEST LOAD CIRCUITS

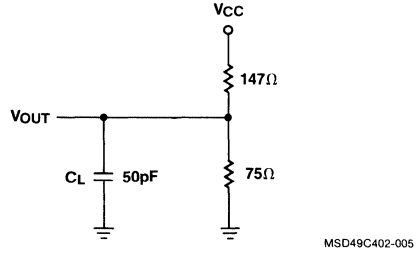


Figure 1. Switching Test Circuit (all outputs)

INPUT/OUTPUT INTERFACE CIRCUITRY

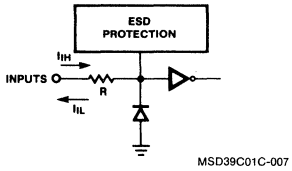


Figure 2. Input Structure (All Inputs)

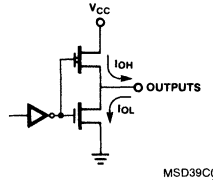


Figure 3. Output Structure (All Outputs Except F = 0)

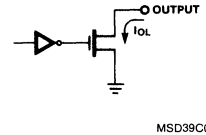


Figure 4. Output Structure (F = Only)

CRITICAL SPEED PATH ANALYSIS

Critical speed paths for the IDT49C402A vs the equivalent bipolar circuit implementation using four 2901Cs and one 2902A is shown below.

The IDT49C402A operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

TIMING COMPARISON IDT49C402A vs 2901C w/2902A

16-BIT μP SYSTEM	DATA PATH (COM'L.)		DATA PATH (MIL.)		UNITS
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	37	36	41	40	ns
Speed Savings	34	35	42.5	43.5	ns

TIMING COMPARISON IDT49C402 vs 2901C w/2902A

16-BIT μP SYSTEM	DATA PATH (COM'L.)		DATA PATH (MIL.)		UNITS
	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0,15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

ADVANCE INFORMATION
IDT49C403
IDT49C403A

MICROSLICE™ PRODUCT

FEATURES:

- Monolithic 16-bit CMOS μP slice
- Replaces four 2903As/29203s and a 2902A
- Fast
  —20% faster than four 2903As/29203s and a 2902A
- Low-power CMOS
  —Commercial — 150mA (max.)
  —Military — 200mA (max.)
- Performs binary and BCD arithmetic
- Expandable two-address architecture with independent, simultaneous access to internal 64 x 16 register file
- Word/BYTE control
- Expanded 4 word x 16-bit Q Register
- Performs BYTE swap operation
- Fully cascadable without the need for additional carry-lookahead
- Incorporates three 16-bit bidirectional buses
- High output drive
  —Commercial — 24mA (max.)
  —Military — 20mA (max.)
- Available in 108-pin grid array and 144-pin leaded chip carrier
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C403/A are high-speed, fully cascadable 16-bit CEMOS™ microprocessor slices. They combine the standard functions of four 2903s/29203s and one 2902, with additional control features aimed at enhancing the performance of all bit-slice microprocessor designs.

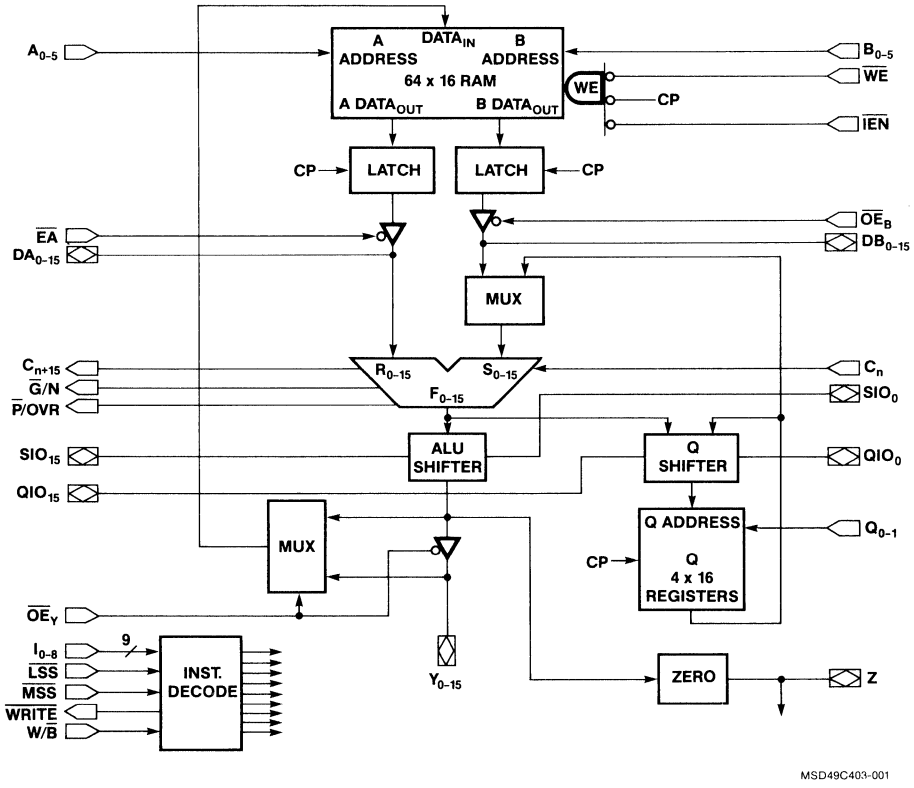
Included in these extremely low-power, yet fast, IDT49C403 devices are: 3 bidirectional data buses, 64 word x 16-bit dual-port expandable RAM, 4 word x 16-bit Q Register file, parity generation, sign extension, multiplication/division and normalization logic. Additionally, the IDT49C403s offer the special feature of enhanced byte support through both Word/BYTE control and BYTE swap control.

The IDT49C403s easily support fast 100ns microcycles and will enhance the speed of all existing quad 2903A/29203 systems by 20%. Being specified at an extremely low 150mA maximum (commercial), the IDT devices offer an immediate system power savings and improved reliability.

The devices are packaged in either 108-pin PGAs or 144-pin leaded chip carriers. Military product is 100% screened to MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Printed in U.S.A.

FUNCTIONAL BLOCK DIAGRAM



Integrated Device Technology, Inc.

32-BIT CMOS MICROPROCESSOR SYSTEM-SLICE™

ADVANCE INFORMATION
IDT49C404

MICROSLICE™ PRODUCT

FEATURES:

- High-speed
  - —Supports 80-100ns microcycles
- Low-power CMOS
  - —700mA typ. (dynamic)
  - —450mA typ. (quiescent)
- 32-bit ALU cascadable to 64 bits
- 64-word x 32-bit RAM
  - —Easily expandable
- Three bidirectional 32-bit data I/O ports
  - —DA, DB, Y
- Powerful, yet simple, instruction set
- Cascadable funnel shifter
- Powerful mask generator
- Versatile merge logic
- Built-In multiplication/division
- Counter function
- Priority encoder
- Single 5V supply
- Available in 196-pin PGA and surface mount package

DESCRIPTION

The IDT49C404 "SYSTEM-SLICE" is an expandable, microprogrammable, high-speed microprocessor slice. This monolithic three-port device consists of a powerful 32-bit ALU, 64-word x 32-bit RAM, cascadable funnel shifter, priority encoder, merge logic and mask generator.

This monolithic device has been optimized, both architecturally and instruction set-wise, for use in ultra-high-speed controllers, high-speed graphic engines, as well as high-speed communication disk controllers and special purpose mini-computers.

The IDT49C404 is fabricated using CEMOS™, IDT's advanced CMOS technology designed for high-performance and high-reliability. It will be packaged in a 196-pin PGA and a 1XX-pin surface mount package.

Printed in U.S.A.

Integrated Device Technology Inc

16-BIT CMOS MICROPROGRAM SEQUENCER

IDT49C410
IDT49C410A

MICROSLICE™ PRODUCT

FEATURES:

- 16-bit wide address path
  —Address up to 65,536 words of micro-program memory
- 16-bit loop counter
  —Pre-settable down-counter for counting loop iterations and repeating instructions
- Low-power CEMOS™
  —I_{CC} (max.)
  Military — 90mA
  Commercial — 75mA
- Fast
  —IDT49C410 meets 2910A speeds
  —IDT49C410A 30% speed upgrade
- 33-deep stack
  —Accomodates highly nested microcode
- 16 powerful microinstructions
  —Executes 16 sequence control instructions
- Available in 48-pin DIP (600 mil), (400 mil x 70 mil centers), 48-pin LCC and 52-pin PLCC
- Three enables control branch address sources
- Four address sources
- 2910A instruction compatiblity
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C410s are architecture and function code compatible to the 2910A with an expanded 16-bit address path, thus allowing for programs up to 65,536 words in length. They are microprogram address sequencers intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, they provide conditional branching to any microinstruction within their 65,536 microword range.

The 33-deep stack provides microsubroutine return linkage and looping capability. The deep stack can be used for highly nested microcode applications. Microinstruction loop count control is provided with a count capacity of 65,536.

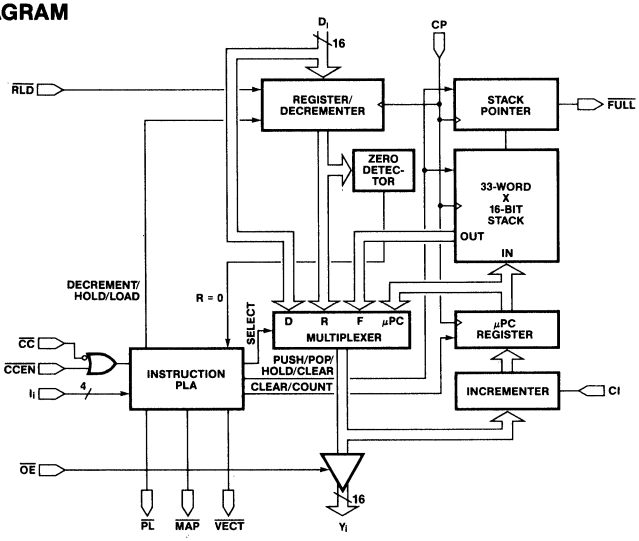
During each microinstruction, the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in, first-out stack (F).

The IDT49C410s are fabricated using CEMOS, a single-poly double-metal CMOS technology designed for high-performance and high-reliability.

The IDT49C410s are pin-compatible, performance-enhanced, easily upgradable versions of the 2910A.

The IDT49C410s are available in 48-pin DIPs (600 mil x 100 mil centers or space-saving 400 mil x 70 mil centers), 48-pin LCCs and 52-pin PLCCs.

FUNCTIONAL BLOCK DIAGRAM



MSD49C410-001

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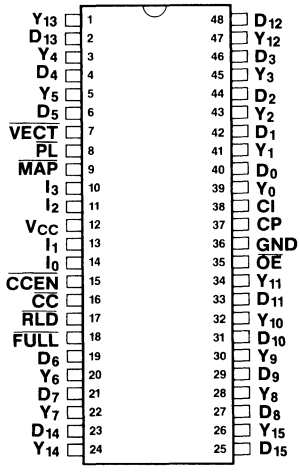
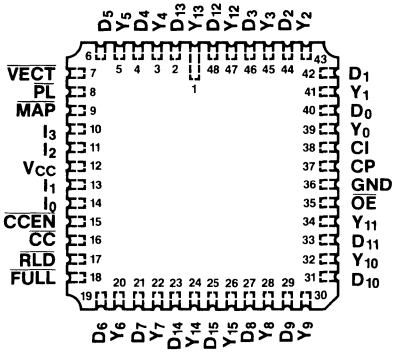
PIN CONFIGURATIONS



DIP MSD49C410-002
TOP VIEW
(600 mil x 100 mil centers)
(400 mil x 70 mil centers)



MSD49C410-003

LCC
TOP VIEW
(560 mil x 560 mil)

IDT49C410 PIN FUNCTIONS

PIN NAME	DESCRIPTION	FUNCTION
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer, D_0 is LSB.
I_i	Instruction Bit i	Selects one-of-sixteen instructions.
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on CC.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, CC is ignored and the part operates as though CC were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter.
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition.
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs.
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge.
V_{CC}	5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{15} is MSB.
$\overline{FULL}$	Full	Indicates that 33 items are on the stack.
PL	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source.
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source.
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source.

3

PRODUCT DESCRIPTION

The IDT49C410s are high-performance CMOS microprogram sequencers that are intended for use in very high-speed microprogrammable microprocessor applications. The sequencers allow for direct control of up to 64K-words of microprogram.

The heart of the microprogram sequencer is a 4-input multiplexer that is used to select one of four address sources to select the next microprogram address. These address sources include the register/counter, the direct input, the microprogram counter, or the stack as the source for the address of the next microinstruction.

The register/counter consists of sixteen D-type flip-flops which can contain either an address or a count. These edge-triggered flip-flops are under the control of a common clock enable as well as the four microinstruction control inputs. When the load control ($\overline{RLD}$) is LOW, the data at the D-inputs is loaded into this register on the LOW-to-HIGH transition of the clock. The output of the register/counter is available at the multiplexer as a possible next address source for the microcode. Also, the terminal count output associated with the register/counter is available at the internal instruction PLA to be used as a condition code input for some of the microinstructions. The IDT49C410s contain a microprogram counter that usually contains the address of the next microinstruction compared to that currently being executed. The microprogram counter actually consists of a 16-bit incrementer followed by a 16-bit register. The microprogram counter will increment the address coming out of the sequencer going to the microprogram memory if the carry-in input to this counter is HIGH; otherwise, this address will be loaded into the microprogram counter. Normally, this carry-in input is set to the logic HIGH state so that the incrementer will be active. Should the carry input be set LOW, the same address is loaded into the microprogram counter. This is a technique that can be used to allow execution of the same microinstruction several times.

There are sixteen D-inputs on the IDT49C410s that go directly to the address multiplexer. These inputs are used to provide a branch address that can come directly from the microcode or some other external source. The fourth input available to the multiplexer for next address control is the 33-deep, 16-bit wide LIFO stack. The LIFO stack provides return address linkage for subroutines and loops. The IDT49C410s contain a built-in stack pointer that always points to the last stack location written. This allows for stack reference operations, usually called loops, to be performed without popping the stack.

The stack pointer internal to the IDT49C410s is actually an up/down counter. During the execution of microinstructions one, four and five, the PUSH operation may occur depending on the state of the condition code input. This causes the stack pointer to be incremented by one and the stack to be written with the required return linkage (the value contained in the microprogram counter). On the microprogram cycle following the PUSH, this new return linkage data that was in the microprogram counter is now at the new location pointed to by the stack pointer. Thus, any time the multiplexer looks at the stack, it will see this data on the top of the stack.

During five different microinstructions, a pop operation associated with the stack may occur. If the pop occurs, the stack pointer is decremented at the next LOW-to-HIGH transition of the clock. A pop decrements the stack pointer which is the equivalent of removing the old information from the top of the stack.

The IDT49C410s are designed so that the stack pointer linkage allows any sequence of pushes, pops or stack references to be used. The depth of the stack can grow to a full 33 locations. After a depth of 33 is reached, the $\overline{FULL}$ output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack will be destroyed but the stack pointer will not end around. It is necessary to initialize the stack pointer when power is first turned on. This is performed by executing a RESET instruction (instruction 0). This sets the stack pointer to the stack empty position—the equivalent depth of 0. Similarly, a pop from an empty stack may place unknown data on the Y outputs, but the stack pointer is designed so as not to end around. Thus, the stack pointer will remain at the 0 or stack empty location if a pop is executed while the stack is already empty.

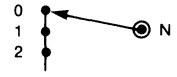
The IDT49C410s' internal 16-bit register/counter is used during microinstructions eight, nine, and fifteen. During these instructions, the 16-bit counter acts as a down counter and the terminal count (count = 0) is used by the internal instruction PLA as an input to control the microinstruction branch test capability. The design of the internal counter is such that, if it is preloaded with a number N and then this counter is used in a microprogram loop, the actual sequence in the loop will be executed N + 1 times. Thus, it is possible to load the counter with a count of 0 and this will result in the microcode being executed one time. The 3-way branch microinstruction, instruction 15, uses both the loop counter and the external condition code input to control the final source address from the Y outputs of the microprogram sequencer. This 3-way branch may result in the next adresss coming from the D inputs, the stack or the microprogram counter.

The IDT49C410s provide a 16-bit address at the Y outputs that are under control of the $\overline{OE}$ input. Thus, the outputs can be put in the three-state mode, allowing the writeable control store to be loaded or certain types of external diagnostics to be executed.

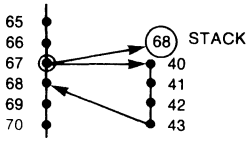
In summary, the IDT49C410s are the most powerful microprogram sequencers currently available. They provides the deepest stack, the highest performance, and the lowest power dissipation for today's microprogrammed machine design.

FIGURE 1. IDT49C410 FLOW DIAGRAMS

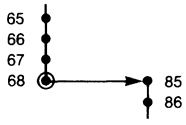
0 Jump Zero (JZ)



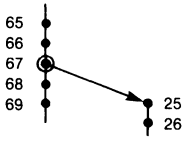
1 Cond JSB PL (CJS)



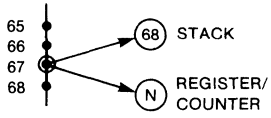
2 Jump Map (JMAP)



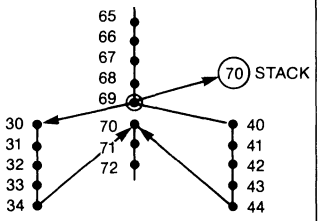
3 Cond Jump PL (CJP)



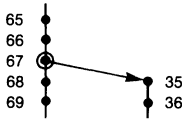
4 Push/Cond LD CNTR (PUSH)



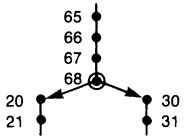
5 Cond JSB R/PL (JSRP)



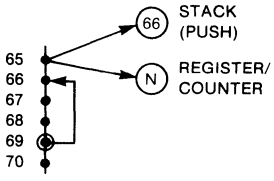
6 Cond Jump Vector (CJV)



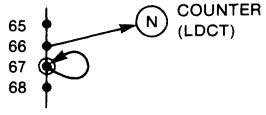
7 Cond JUMP R/PL (JRP)



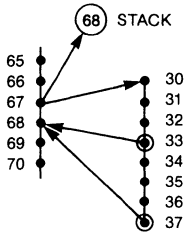
8 Repeat Loop, CNTR ≠ 0 (RFCT)



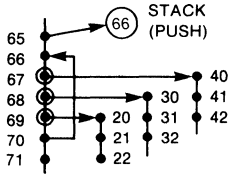
9 Repeat PL, CNTR ≠ 0 (RPCT)



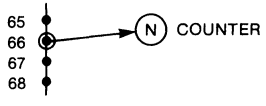
10 Cond Return (CRTN)



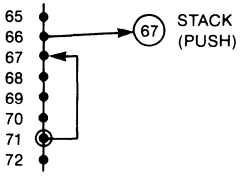
11 Cond Jump PL & POP (CJPP)



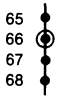
12 LD CNTR & Continue (LDCT)



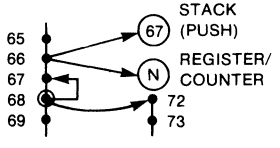
13 Test End Loop (LOOP)



14 Continue (CONT)



15 Three-Way Branch (TWB)



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IDT49C410 OPERATION

The IDT49C410s are CMOS pin-compatible implementations of the Am2910 & 2910A microprogram sequencers. The IDT49C410 sequencers are functionally identical except that they are 16 bits wide and provide a 33-deep stack to give the microprogrammer more capability in terms of microprogram subroutines and microprogram loops. The definition of each microprogram instruction is shown in the table of instructions. This table shows the results of each instruction in terms of controlling the multiplexer which determines the Y outputs, and in controlling the signals that can be used to enable various branch address sources ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$). The operation of the register/counter and the 33-deep stack after the next LOW-to-HIGH transition of the clock are also shown. The internal multiplexer is used to select which of the internal sources is used to drive the Y outputs. The actual value loaded into the microprogram counter is either identical to the Y output or the Y output value is incremented by 1 and placed in the microprogram counter. This function is under the control of the carry input. For each of the microinstruction inputs, only one of the three outputs ($\overline{PL}$, $\overline{MAP}$ or $\overline{VECT}$) will be LOW. Note that this function is not determined by any of the possible condition code inputs. These outputs can be used to control the three-state selection of one of the sources for the microprogram branches.

Two inputs, $\overline{CC}$ and $\overline{CCEN}$, can be used to control the conditional instructions. These are fully defined in the table of instructions. The $\overline{RLD}$ input can be used to load the internal register/counter at any time. When this input is LOW, the data at the D inputs will be loaded into this register/counter on the LOW-to-HIGH transition of the clock. Thus, the $\overline{RLD}$ input overrides the internal hold or decrement operations specified by the various microinstructions. The $\overline{OE}$ input is normally LOW and is used as the three-state enable for the Y outputs. The internal stack in the IDT49C410s is a last-in, first-out memory that is 16 bits in width and 33 words deep. It has a stack pointer that addresses the stack and always points to the value currently on the top of the stack. When instruction 0 (RESET) is executed, the stack pointer is initialized to the top of the stack which is, by definition, the stack empty condition. Thus, the contents of the top of the stack are undefined until the forced PUSH occurs. A pop performed while the stack is empty will not change the stack pointer in any way, however it will result in unknown data at the Y outputs.

By definition, the stack is full any time 33 more PUSHes than pops have occurred since the stack was last empty. When this happens, the $\overline{FULL}$ flag will go LOW. This signal first goes LOW on the microcycle after the 33 pushes occur. When this signal is LOW, no additional pushes should be attempted or the information on the top of the stack will be lost.

THE IDT49C410 INSTRUCTION SET

This data sheet contains a block diagram of the IDT49C410 microprogram sequencers. As can be seen, the devices are controlled by a 4-bit microinstruction word (I_3–I_0). Normally, this word is supplied from one 4-bit field of the microinstruction word associated with the entire state machine system. These four bits provide for the selection of one of the sixteen powerful instructions associated with selecting the address of the next microinstruction. Unused Y outputs can be left open; however, the corresponding most significant D inputs should be tied to ground for smaller microwords. This is necessary to make sure the internal operation of the counter is proper should less than 64K of microcode be implemented. As shown in the block diagram, the internal instruction PLA uses the four instruction inputs as well as the $\overline{CC}$, $\overline{CCEN}$ and the internal counter = 0 line for controlling the sequencer. This internal instruction PLA provides all of the necessary internal control signals to control each particular part of the microprogram sequencer. The next address at the Y outputs of the IDT49C410s can be from one of four sources. These include the internal microprogram counter; the last-in, first-out stack; the register/counter and the direct inputs.

The following paragraphs will describe each instruction associated with the IDT49C410s. As a part of the discussion, an example of each instruction is shown in Figure 1. The purpose of the examples is to show microprogram flow. Thus, in each example the microinstruction currently being executed has a circle around it. That is, this microinstruction is assumed to be the contents of the pipeline register at the output of the microprogram memory. In these drawings, each of the dots refers to the time that the contents of the microprogram memory word would be in the pipeline register and currently being executed.

INSTRUCTION 0— JUMP 0 (JZ)

This instruction is used at power-up time or at any restart sequence when the need is to reset the stack pointer and jump to the very first address in microprogram memory. The jump 0 instruction does not change the contents of the register/counter.

INSTRUCTION 1— CONDITIONAL JUMP TO SUBROUTINE (CJS)

The conditional jump to subroutine instruction is the one used to call microprogram subroutines. The subroutine address will be contained in the pipeline register and presented at the D inputs. If the condition code test is passed, a branch is taken to the subroutine. Referring to the flow diagram for the IDT49C410s shown in Figure 1, we see that the content of the microprogram counter is 68. This value is pushed onto the stack and the top of stack pointer is incremented. If the test is failed, then this conditional jump to subroutine instruction behaves as a simple continue. That is, the contents of microinstruction address 68 is executed next.

INSTRUCTION 2— JUMP MAP (JMAP)

This sequencer instruction can be used to start different microprogram routines based on the machine instruction opcode. This is typically accomplished by using a mapping PROM as an input to the D inputs on the microprogram sequencer. The JMAP instruction branches to the address appearing on the D inputs. In the flow diagram shown in Figure 1, we see that the branch actually will be to the contents of microinstruction 85 and this instruction will be executed next.

INSTRUCTION 3— CONDITIONAL JUMP PIPELINE (CJP)

The simplest branching control available in the IDT49C410 microprogram sequencers is that of conditional jump to address. In this instruction, the jump address is usually contained in the microinstruction pipeline register and presented to the D inputs. If the test is passed, the jump is taken while, if the test fails, this instruction executes as a simple continue. In the example shown in the flow diagrams of Figure 1, we see that if the test is passed the next microinstruction to be executed is the contents of address 25. If the test is failed, the microcode simply continues to the contents of the next instruction.

INSTRUCTION 4— PUSH/CONDITIONAL LOAD COUNTER (PUSH)

With this instruction, the counter can be conditionally loaded during the same instruction that pushes the current value of the microprogram counter on to the stack. Under any condition independent of the conditional testing, the microprogram counter

IDT49C410 INSTRUCTION OPERATIONAL SUMMARY

I_3-I_0	MNEMONIC	CC	COUNTER TEST	STACK	ADDRESS SOURCE	REGISTER/ COUNTER	ENABLE SELECT
0	JZ	X	X	CLEAR	0	NC	PL
1	CJS	PASS FAIL	X X	PUSH NC	D PC	NC NC	PL PL
2	JMAP	X	X	NC	D	NC	MAP
3	CJP	PASS FAIL	X X	NC NC	D PC	NC NC	PL PL
4	PUSH	PASS FAIL	X X	PUSH PUSH	PC PC	LOAD NC	PL PL
5	JSRP	PASS FAIL	X X	PUSH PUSH	D R	NC NC	PL PL
6	CJV	PASS FAIL	X X	NC NC	D PC	NC NC	VECT VECT
7	JRP	PASS FAIL	X X	NC NC	D R	NC NC	PL PL
8	RFCT	X X	= 0 NOT = 0	POP NC	PC STACK	NC DEC	PL PL
9	RPCT	X X	= 0 NOT = 0	NC NC	PC D	NC DEC	PL PL
10	CRTN	PASS FAIL	X X	POP NC	STACK PC	NC NC	PL PL
11	CJPP	PASS FAIL	X X	POP NC	D PC	NC NC	PL PL
12	LDCT	X	X	NC	PC	LOAD	PL
13	LOOP	PASS FAIL	X X	POP NC	PC STACK	NC NC	PL PL
14	CONT	X	X	NC	PC	NC	PL
15	TWB	PASS PASS FAIL FAIL	= 0 NOT = 0 = 0 NOT = 0	POP POP POP NC	PC PC D STACK	NC DEC NC DEC	PL PL PL PL

NC = no change; DEC = decrement

is pushed on to the stack. If the conditional test is passed, the counter will be loaded with the value on the D inputs to the sequencer. If the test fails, the contents of the counter will not change. The PUSH/conditional load counter instruction is used in conjunction with the loop instruction (Instruction 13), the repeat file based on the counter instruction (Instruction 9) or the 3-way branch instruction (Instruction 15).

INSTRUCTION 5— CONDITIONAL JUMP TO SUBROUTINE R/PL (JSRP)

Subroutines may be called by a conditional jump subroutine from the internal register or from the external pipeline register. In this instruction, the contents of the microprogram counter are pushed on the stack and the branch adddress for the subroutine call will be taken from either the internal register/counter or the external pipeline register presented to the D inputs. If the conditional test is passed, the subroutine address will be taken from the pipeline register. If the conditional test fails, the branch address is taken from the internal register/counter. An example of this is shown in the flow diagram of Figure 1.

INSTRUCTION 6— CONDITIONAL JUMP VECTOR (CJV)

The conditional jump vector instruction is similar to the jump map instruction in that it allows a branch operation to a microinstruction as defined from some external source. This instruction is similar to the jump map instruction except that it is conditional. The jump map instruction is unconditional. If the conditional test is passed, the branch is taken to the new address on the D inputs. If the conditional test is failed, no branch is taken but rather the microcode simply continues to the next sequential microinstruction. When this instruction is executed, the $\overline{VECT}$ output is LOW unconditionally. Thus, an external 16-bit field can be enabled on to the D inputs of the microprogram sequencer.

INSTRUCTION 7— CONDITIONAL JUMP R/PL (JRP)

The conditional jump register/counter or external pipeline register always causes a branch in microcode. This jump will be to one of two different locations in the microcode address space. If the test is passed, the jump will be to the address presented on the D inputs to the microprogram sequencer. If the conditional test fails, the branch will be to the address contained in the internal register/counter.

INSTRUCTION 8— REPEAT LOOP COUNTER NOT EQUAL TO 0 (RFCT)

This instruction utilizes the loop counter and the stack to implement microprogrammed loops. The start address for the loop would be initialized by using the PUSH/conditional load counter instruction. Then, when the repeat loop instruction is executed, if the counter is not equal to 0, the next microword address will be taken from the stack. This will cause a loop to be executed as shown in the Figure 1 flow diagram. Each time the microcode sequence goes around the loop, the counter is decremented. When the counter reaches 0, the stack will be popped and the microinstruction address will be taken from the

microprogram counter. This instruction performs a timed wait or allows a single sequence to be executed the desired number of times. Remember, the actual number of loops performed is equal to the value in the counter plus 1.

INSTRUCTION 9— REPEAT PIPELINE, COUNTER NOT EQUAL TO 0 (RPCT)

This instruction is another technique for implementing a loop using the counter. Here, the branch address for the loop is contained in the pipeline register. This instruction does not use the stack in any way as a part of its implementation. As long as the counter is not equal to 0, the next microword address will be taken from the D inputs of the microprogram sequencer. When the counter reaches 0, the internal multiplexer will select the address source from the microprogram counter, thus causing the microcode to continue on and leave the loop.

INSTRUCTION 10— CONDITIONAL RETURN (CRTN)

The conditional return instruction is used for terminating subroutines. The fact that it is conditional allows the subroutine either to be ended or to continue. If the conditional test is passed, the address of the next microinstruction will be taken from the stack and it will be popped. If the conditional test fails, the next microinstruction address will come from the internal microprogram counter. This is depicted in the flow diagram of Figure 1. It is important to remember that every subroutine call must somewhere be followed by a return from subroutine call in order to have an equal number of pushes and pops on the stack.

INSTRUCTION 11— CONDITIONAL JUMP PIPELINE AND POP (CJPP)

The conditional jump pipeline and pop instruction is a technique for exiting a loop from within the middle of the loop. This is depicted fully in the flow diagrams for the IDT49C410s as shown in Figure 1. The conditional test input for this instruction results in a branch being taken if the test is passed. The address selected will be that on the D inputs to the microprogram sequencer and since the loop is being terminated, the stack will be popped. Should the test be failed on the conditional test inputs, the microprogram will simply continue to the next address as taken from the microprogram counter. The stack will not be affected if the conditional test input is failed.

INSTRUCTION 12— LOAD COUNTER AND CONTINUE (LDCT)

The load counter and continue instruction is used to place a value on the D inputs in the register/counter and continue to the next microinstruction.

INSTRUCTION 13— TEST END OF LOOP (LOOP)

The test end of loop instruction is used as a last instruction in a loop associated with the stack. During this instruction, if the conditional test input is failed, the loop branch address will be that on the stack. Since we may go around the loop a number of times, the stack is not popped. If the conditional test input is passed, then the loop is terminated and the stack is popped. Notice that the loop instruction requires a PUSH to be performed at the instruction immediately prior to the loop return address. This is necessary so as to have the correct address on the stack before the loop operation. It is for this reason that the stack pointer always points to the last thing written on the stack.

INSTRUCTION 14— CONTINUE (CONT)

The continue instruction is a simple instruction whereby the address for the microinstruction is taken from the microprogram counter. This instruction simply causes sequential program flow to the next microinstruction in microcode memory.

INSTRUCTION 15— THREE WAY BRANCH (TWB)

The three way branch instruction is used for looping while waiting for a conditional event to come true. If the event does not come true after some number of microinstructions, then a branch is taken to another microprogram sequence. This is depicted in Figure 1 showing the IDT49C410 flow diagrams and is also described in full detail in the IDT49C410s' instruction operational summary. Operation of the instruction is such that any time the external conditional test input is passed, the next microinstruction will be that associated with the program counter and the loop will be left. The stack is also popped. Thus, the external test input overrides the other possibilities. Should the external conditional test input not be true, then the rest of the operation is controlled by the internal counter. If the counter is not equal to 0, the loop is taken by selecting the address on the top of the stack as the address out of the Y outputs of the IDT49C410s. In addition, the counter is decremented. Should the external conditional test input be failed and the counter also have counted to 0, then this instruction "times out." The result is that the stack is popped and a branch is taken to the address presented to the D inputs of the IDT49C410 microprogram sequencers. This address is usually provided by the external pipeline register.

CONDITIONAL TEST

Throughout this discussion we have talked about microcode passing the conditional test. There are actually two inputs associated with the conditional test input. These include the $\overline{CCEN}$ and the $\overline{CC}$ inputs. The $\overline{CCEN}$ input is a condition code enable. Whenever the $\overline{CCEN}$ input is HIGH, the $\overline{CC}$ input is ignored and the device operates as though the $\overline{CC}$ input were true (LOW). Thus, a fail of the external test condition can be defined as $\overline{CCEN}$ equals LOW and $\overline{CC}$ equals HIGH. A pass condition is defined as a $\overline{CCEN}$ equal to HIGH or a $\overline{CC}$ equal to LOW. It is important to recognize the full function of the condition code enable and the condition code inputs in order to understand when the test is passed or failed.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM'L	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL	—	0.3	0.5	
			I_{OL} = 24mA COM'L	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-130	mA

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

3

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = +5.0V ± 5% Min. = +4.75V Max. = +5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% Min. = +4.50V Max. = +5.50V (Military)
V_{LC} = +0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ F_C = 0, CP = H		—	—	—	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ F_C = 0, CP = L		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High)[5]	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	50	90	
			COM'L.	—	50	75	

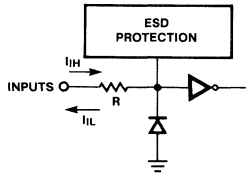
NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

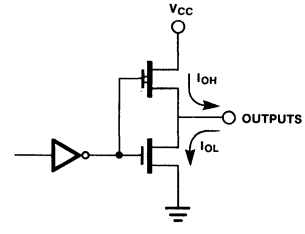
CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock Input frequency.

IDT49C410 INPUT/OUTPUT INTERFACE CIRCUITRY



IDT49C410-007

Figure 1. Input Structure (All Inputs)



IDT49C410-008

Figure 2. Output Structure (All Outputs)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 3

IDT49C410A
AC ELECTRICAL CHARACTERISTICS

Commercial: 5.0V ± 5%, T_A = 0°C to +70°C
Military: 5.0V ± 10%, T_A = -55°C to +125°C
C_L = 50pF

I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	
D_i→R	6	7	0	0	ns
D_i→PC	13	15	0	0	ns
I_{0-3}	23	25	0	0	ns
$\overline{CC}$	15	18	0	0	ns
$\overline{CCEN}$	15	18	0	0	ns
CI	6	7	0	0	ns
$\overline{RLD}$	11	12	0	0	ns

II. COMBINATIONAL DELAYS

INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	12	15	—	—	—	—	ns
I_{0-3}	20	25	13	15	—	—	ns
$\overline{CC}$	16	20	—	—	—	—	ns
$\overline{CCEN}$	16	20	—	—	—	—	ns
CP	28	33	—	—	22	25	ns
$\overline{OE}$(1)	10/10	13/13	—	—	—	—	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNITS
Minimum Clock LOW Time	18	20	ns
Minimum Clock HIGH Time	17	20	ns
Minimum Clock Period	35	40	ns

IDT49C410
AC ELECTRICAL CHARACTERISTICS

Commercial: 5.0V ± 5%, T_A = 0°C to +70°C
Military: 5.0V ± 10%, T_A = -55°C to +125°C
C_L = 50pF

I. SET-UP AND HOLD TIMES

INPUTS	$t_{(s)}$		$t_{(h)}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	
D_i→R	16	16	0	0	ns
D_i→PC	30	30	0	0	ns
I_{0-3}	35	38	0	0	ns
$\overline{CC}$	24	35	0	0	ns
$\overline{CCEN}$	24	35	0	0	ns
CI	18	18	0	0	ns
$\overline{RLD}$	19	20	0	0	ns

II. COMBINATIONAL DELAYS

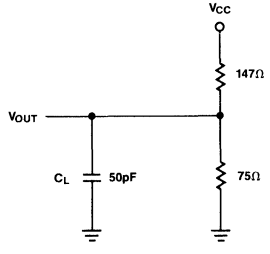
INPUTS	Y		$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$		$\overline{FULL}$		UNITS
	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
D_{0-11}	20	25	—	—	—	—	ns
I_{0-3}	35	40	30	35	—	—	ns
$\overline{CC}$	30	36	—	—	—	—	ns
$\overline{CCEN}$	30	36	—	—	—	—	ns
CP	40	46	—	—	31	35	ns
$\overline{OE}$(1)	25/27	25/30	—	—	—	—	ns

NOTE:
1. Enable/Disable. Disable times measure to 0.5V change on output voltage level with C_L = 5pF.

III. CLOCK REQUIREMENTS

	COM'L.	MIL.	UNITS
Minimum Clock LOW Time	20	25	ns
Minimum Clock HIGH Time	20	25	ns
Minimum Clock Period	50	51	ns

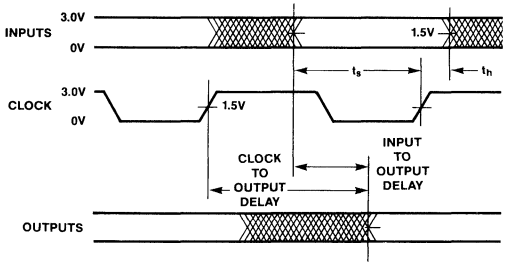
TEST LOAD CIRCUITS



MSD49C410-004

Figure 3. Switching Test Circuit (all outputs)

SWITCHING WAVEFORMS



MSD49C410-005

Integrated Device Technology, Inc.

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

PRELIMINARY
IDT49C460
IDT49C460A

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - — Error detect
    IDT49C460A — 30ns (max.), IDT49C460 — 40ns (max.)
  - — Error correct
    IDT49C460A — 36ns (max.), IDT49C460 — 49ns (max.)
- Low-Power CMOS
  - — Commercial — 95mA (max.)
  - — Military — 125mA (max.)
- Improves system memory reliability
  - — Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64-bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the 2960
- Available in 68-pin PGA, DIP (600 mil, 70 mil centers), LCC (25 and 50 mil centers)
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

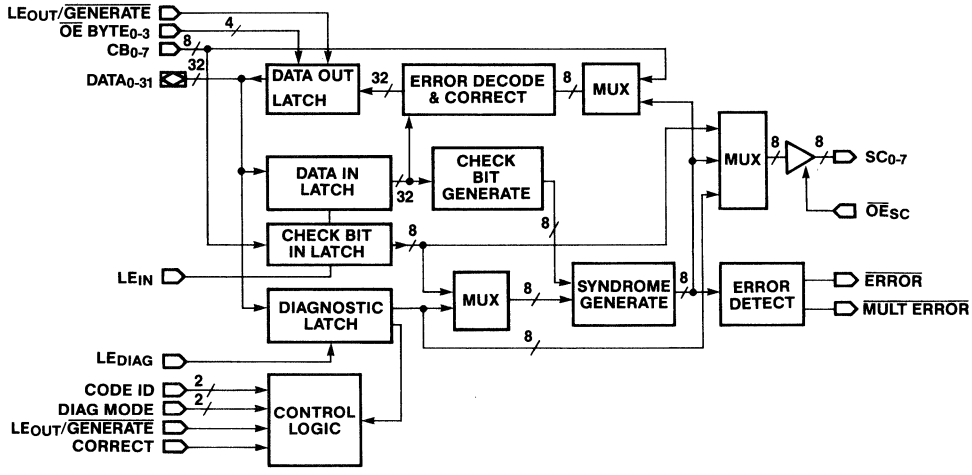
The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors, will detect all double bit errors and some triple bit errors.

The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostic functions.

They are fabricated using CEMOS™, a single poly, double metal CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin PGA, DIP (600 mil centers) and LCC (25 mil and 50 mil centers). Military product is 100% screened to MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



MSD49C460-001

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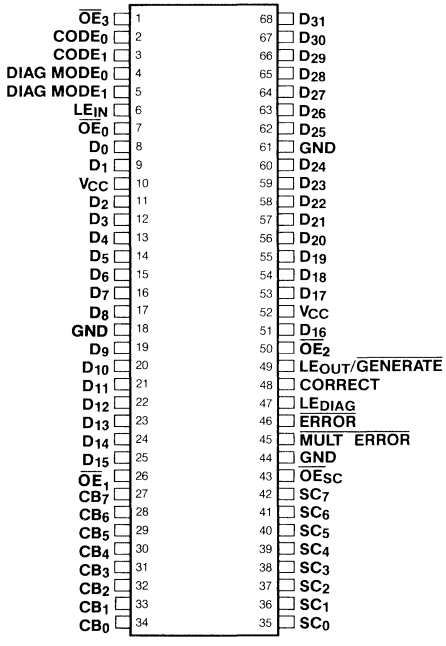
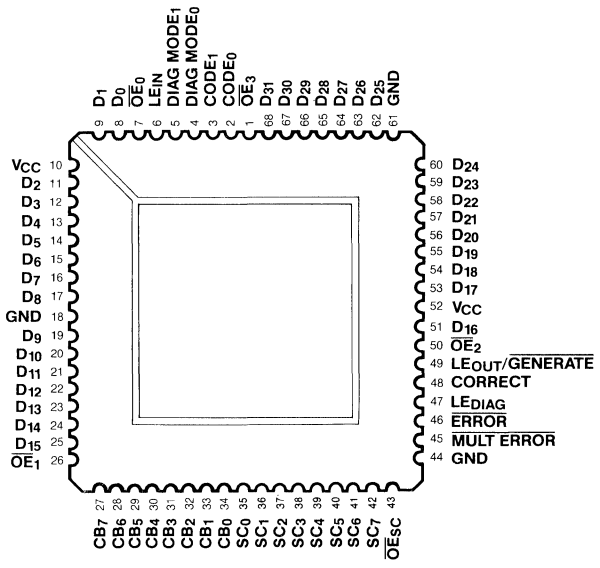
PIN CONFIGURATION



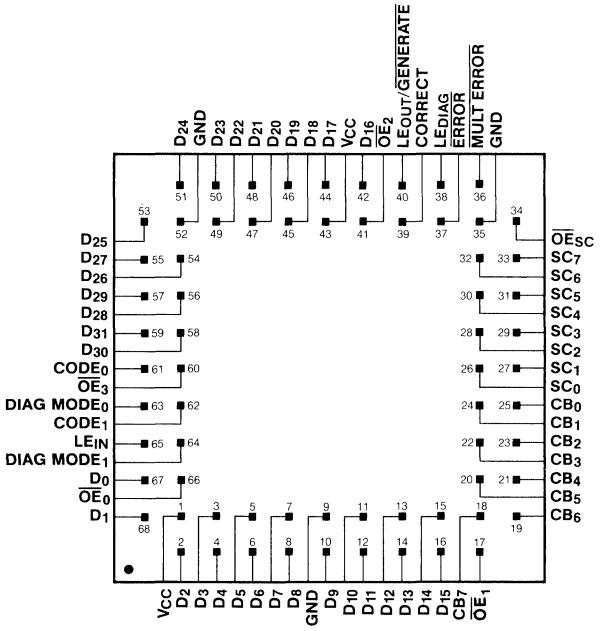
DIP
TOP VIEW

MSD49C460-002



LCC
TOP VIEW

MSD49C460-003



PGA
TOP VIEW

MSD49C460-004

3

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
$DATA_{0-31}$	I/O	32 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines. Used to input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
LE_{OUT}/ $\overline{GENERATE}$	I	A multifunction pin which, when LOW, is in the Check Bit Generate mode. In this mode, the device generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated Check Bits are placed on the SC outputs. Also when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected, with the corrected data placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable — Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT\ ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}\ BYTE_{0-3}$	I	Output Enable — Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
$DIAG\ MODE_{0,1}$	I	Selects the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
$CODE\ ID_{0,1}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32- and 64-bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special CODE ID input 01 is also used to instruct the EDC that the signals $CODE\ ID_{0,1}$, $DIAG\ MODE_{0,1}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for $CODE\ ID_{0,1}$, $DIAG\ MODE_{0,1}$ and CORRECT.

EDC ARCHITECTURE SUMMARY

The IDT49C460A/460 are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostics Latch
- Control Logic

DATA INPUT/OUTPUT LATCH:

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The 32 bits of data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used in the Internal Control mode or in one of the Diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT INPUT LATCH:

Eight check bits are loaded under control of LE_{IN}. Check bits are used in the Error Detection and Error Correction modes.

CHECK BIT GENERATION LOGIC:

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC:

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits means no error was detected. If there is a mismatch, then one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits means the syndrome bits will be all zeroes. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC:

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs are HIGH. $\overline{\text{ERROR}}$ will go low if one error is detected. $\overline{\text{MULT ERROR}}$ and $\overline{\text{ERROR}}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC:

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS:

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch under control of the PASS THRU control input. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0\text{-}3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH:

A 32-bit latch is loadable, under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

CONTROL LOGIC:

Specifies what mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since the LE_{OUT} and $\overline{\text{GENERATE}}$ are controlled by the same pin, the latching action, LE_{OUT} from high to low, of the data output latch causes the EDC to go into the generate mode.

DETAILED PRODUCT DESCRIPTION

The IDT49C460/A EDC unit contains the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double and some triple bit errors. The IDT49C460/A can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

CODE AND BYTE SELECTION

The 2 code identification pins, $ID_{0,1}$ are used to determine the data word size that is 32- or 64-bits. Table 4 defines all possible slice identification codes.

CHECK AND SYNDROME BITS

The IDT49C460/A provides either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bit sorted with the data. Syndrome bits can be decoded to determine the single bit in error, or that a double (some triple) error was detected. The check bits are labeled:

CX, C0, C1, C2, C4, C8, C16 for the 32-bit configuration
CX, C0, C1, C2, C4, C8, C16, C32 for the 64-bit configuration

Syndrome bits are similarly labeled SX through S32.

TABLE 2. DIAGNOSTIC MODE CONTROL

CORRECT	DIAG $MODE_1$	DIAG $MODE_0$	DIAGNOSTIC MODE SELECTED
X	0	0	**Non-diagnostic mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct Modes.
X	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeroes (and latched upon removal of Initialize Mode) and the check bits generated corresponding to the all zero data.
0	1	1	**Pass Thru.**

TABLE 3. IDT49C460 OPERATING MODES

OPERATING MODE	DM_1	DM_0	$\overline{GENERATE}$	CORRECT	DATA OUT LATCH	SC_{0-7} ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW(1)	Check Bits Generated from Data In Latch	—
Detect	0 0	0 1	1	0	Data In Latch	Syndrome Bits Data In/ Check Bit Latch	Error Dep(2)
Correct	0 0	0 1	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Check Bit Latch	Error Dep
Pass Thru	1	1	1	0	Data In Latch	Check Bit Latch	HIGH
Diagnostic Generate	0	1	0	X	—	Check Bits from Diagnostic Latch	—
Diagnostic Detect	1	0	1	0	Data In Latch	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	Data In Latch w/ Single Bit Correction	Syndrome Bits Data In/ Diagnostic Latch	Error Dep
Initialization Mode	1	1	1	1	Data In Latch set to 0000	Check Bit Data generated from Data In Latch	—
Internal Mode	CODE $ID_{0,1}$ = 01 Control Signals $ID_{0,1}$, DIAG $MODE_{0,1}$, and CORRECT are taken from Diagnostic Latch.						

NOTES:

1. In Generate Mode, data is read in to the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the Data Out Latch is not used in the Generate Mode, LE_{OUT}, being LOW (since it is tied to Generate), does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.

CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT49C460/A. The Diagnostic Mode pins, DIAG $MODE_{0,1}$, define four basic areas of operation, with $\overline{GENERATE}$ and CORRECT further dividing operation into 8 functions with the $ID_{0,1}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC_{0-7}. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs $\overline{ERROR}$ and $\overline{MULT\ ERROR}$. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC_{0-7}. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set and latched to a logic zero, and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG $MODE_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even $ID_{1,0}$ although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

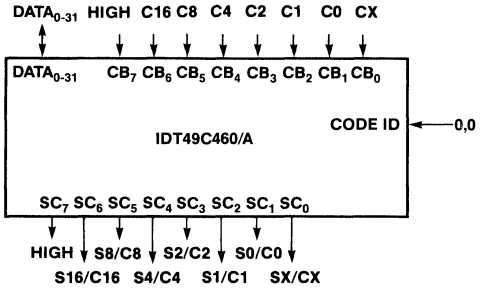


Figure 1. 32-Bit Configuration

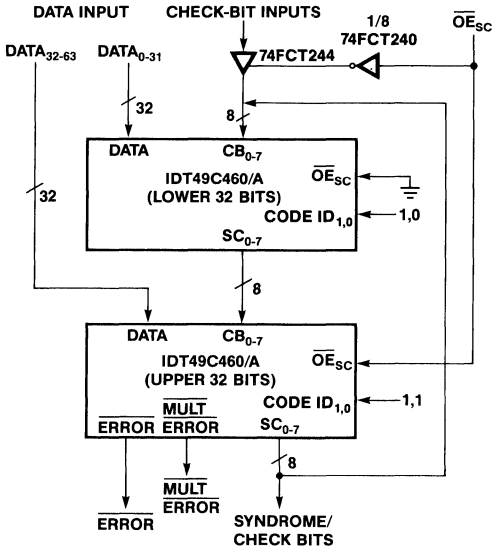


Figure 2. 64-Bit Configuration

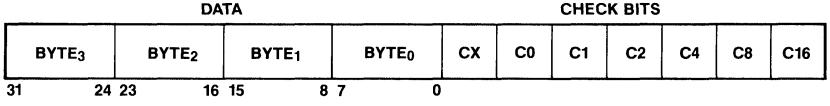


Figure 3. 32-Bit Data Format

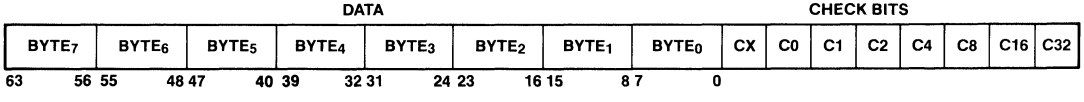


Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION

A single IDT49C460/A EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB_7 pin is therefore a "Don't Care" and $ID_{1,0} = 00$.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available. The output pin, SC_7, is forced HIGH for either syndrome or check bits since only 7 check bits are used for the 32-bit mode.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the Pass Thru or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 4 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal mode substitutes the indicated bit position for the external control signals.

TABLE 4. 32-BIT DIAGNOSTIC LATCH CODING FORMAT

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13-31	DON'T CARE

TABLE 5. SLICE IDENTIFICATION

CODE ID_1	CODE ID_0	SLICE SELECTED
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32-Bit (0-31)
1	1	64-Bit, Upper 32-Bit (32-63)

TABLE 6. 32-BIT MODIFIDED HAMMING CODE—CHECK BIT ENCODE CHART

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X			X	
C4	Even (XOR)			X	X	X	X	X	X						X	X	
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X			X	
C4	Even (XOR)			X	X	X	X	X	X						X	X	
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

TABLE 7.
SYNDROME DECODE TO BIT-IN-ERROR

SYNDROME BITS				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

NOTES:
* — no errors detected
Number — number of the single bit-in-error
T — two errors detected
M — three or more errors detected

TABLE 8.
64-BIT DIAGNOSTIC LATCH — CODING FORMAT

BIT	INTERNAL FUNCTION
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	$CODE_0$ LOWER 32-BIT
9	$CODE_1$ LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13-31	DON'T CARE
32-39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45-63	DON'T CARE

64-BIT DATA WORD CONFIGURATION

Two IDT49C460/A EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error correction and double bit error detection of a 64-bit data field. Table 5 gives the $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals come from the IC with the CODE ID = 11. Control signals not indicated are connected to both units in parallel. The EDC with the CODE ID = 10 has the $\overline{OE}_{SC}$ grounded. The $\overline{OE}_{SC}$ selects the syndrome bits from the EDC with CODE ID = 11 and also controls the check bit buffers from memory.

Data In bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE ID = 10 while Data In bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE ID = 11.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE ID = 10 through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the lower EDC unit to the upper EDC units. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating mode available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit C0 is the exclusive-OR function or the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the Pass Thru or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 9 indicates the decoding of the 7 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 8 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10 in relating a single IDT49C460/A EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

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TABLE 9. SYNDROME DECODE TO BIT-IN-ERROR

SYNDROME BITS				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 10.
KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-BIT PROPAGATION DELAY		COMPONENT DELAY FOR IDT49C460/A AC SPECIFICATIONS
FROM	TO	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected DATA Out	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{\text{ERROR}}$ for 32-Bits	(DATA TO SC) + (CB TO $\overline{\text{ERROR}}$, CODE ID 11)
DATA	$\overline{\text{MULT ERROR}}$ for 32-Bits	(DATA TO SC) + (CB TO $\overline{\text{MULT ERROR}}$, CODE ID 11)

TABLE 11. 64-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODING

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE: The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

SC OUTPUTS

The tables below indicate how the SC_{0-7} outputs are generated in each control mode for various CODE IDs (internal control mode not applicable).

GENERATE	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	PH0	PH1	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA	PA	PA ⊕ CB_1
$SC_2 \leftarrow$	PB	PB	PB ⊕ CB_2
$SC_3 \leftarrow$	PC	PC	PC ⊕ CB_3
$SC_4 \leftarrow$	PD	PD	PD ⊕ CB_4
$SC_5 \leftarrow$	PE	PE	PE ⊕ CB_5
$SC_6 \leftarrow$	PF	PF	PF ⊕ CB_6
$SC_7 \leftarrow$	1	PF	PG ⊕ CB_7

CORRECT/ DETECT	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	PH0 ⊕ C0	PH1 ⊕ C0	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA ⊕ C1	PA ⊕ C1	PA ⊕ CB_1
$SC_2 \leftarrow$	PB ⊕ C2	PB ⊕ C2	PB ⊕ CB_2
$SC_3 \leftarrow$	PC ⊕ C3	PC ⊕ C3	PC ⊕ CB_3
$SC_4 \leftarrow$	PD ⊕ C4	PD ⊕ C4	PC ⊕ CB_4
$SC_5 \leftarrow$	PE ⊕ C5	PE ⊕ C5	PE ⊕ CB_5
$SC_6 \leftarrow$	PF ⊕ C6	PF ⊕ C6	PF ⊕ CB_6
$SC_7 \leftarrow$	1	PF ⊕ C7	PG ⊕ CB_7

DIAGNOSTIC READ	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	PH0 ⊕ DL0	PH1 ⊕ DL0	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA ⊕ DL1	PA ⊕ DL1	PA ⊕ CB_1
$SC_2 \leftarrow$	PB ⊕ DL2	PB ⊕ DL2	PB ⊕ CB_2
$SC_3 \leftarrow$	PC ⊕ DL3	PC ⊕ DL3	PC ⊕ CB_3
$SC_4 \leftarrow$	PD ⊕ DL4	PD ⊕ DL4	PD ⊕ CB_4
$SC_5 \leftarrow$	PE ⊕ DL5	PE ⊕ DL5	PE ⊕ CB_5
$SC_6 \leftarrow$	PF ⊕ DL6	PF ⊕ DL6	PF ⊕ CB_6
$SC_7 \leftarrow$	1	PF ⊕ DL7	PG ⊕ CB_7

DIAGNOSTIC WRITE	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	DL0	DL0	CB_0
$SC_1 \leftarrow$	DL1	DL1	CB_1
$SC_2 \leftarrow$	DL2	DL2	CB_2
$SC_3 \leftarrow$	DL3	DL3	CB_3
$SC_4 \leftarrow$	DL4	DL4	CB_4
$SC_5 \leftarrow$	DL5	DL5	CB_5
$SC_6 \leftarrow$	DL6	DL6	CB_6
$SC_7 \leftarrow$	1	DL7	CB_7

PASS THRU	CODE ID_{1-0}		
	00	10	11
$SC_0 \leftarrow$	C0	C0	CB_0
$SC_1 \leftarrow$	C1	C1	CB_1
$SC_2 \leftarrow$	C2	C2	CB_2
$SC_3 \leftarrow$	C3	C3	CB_3
$SC_4 \leftarrow$	C4	C4	CB_4
$SC_5 \leftarrow$	C5	C5	CB_5
$SC_6 \leftarrow$	C6	C6	CB_6
$SC_7 \leftarrow$	1	C7	CB_7

DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE ID position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

32-BIT CONFIGURATION CODE $ID_{1,0}$ = 00

SYNDROME BITS				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	1	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		—	—	—	—	—	—	—	30
0	0	0	1		—	—	—	27	—	5	—	—
0	0	1	0		—	—	—	25	—	3	15	—
0	0	1	1		—	—	13	—	23	—	—	—
0	1	0	0		—	—	—	24	—	2	—	—
0	1	0	1		—	1	12	—	22	—	—	—
0	1	1	0		—	—	10	—	20	—	—	—
0	1	1	1		16	—	—	—	—	—	—	—
1	0	0	1		—	—	—	—	—	—	14	—
1	0	0	1		—	—	11	—	21	—	—	—
1	0	1	0		—	—	9	—	19	—	—	31
1	0	1	1		—	—	—	29	—	7	—	—
1	1	0	0		—	—	8	—	18	—	—	—
1	1	0	1		17	—	—	28	—	6	—	—
1	1	1	0		—	—	26	—	4	—	—	—
1	1	1	1		—	9	—	—	—	—	—	—

64-BIT (LOWER 32-BIT) CONFIGURATION CODE ID_{1-0} = 10

SYNDROME BITS				CB32	0	1	0	1	0	1	0	1
				CB16	0	0	1	1	0	0	1	1
				CB8	0	0	0	0	1	1	1	1
				CB4	0	0	0	0	0	0	0	0
CBX	CB0	CB1	CB2									
0	0	0	0		—	—	—	—	—	—	—	—
0	0	0	1		—	—	—	—	—	—	—	
0	0	1	0		—	—	—	—	—	—	15	31
0	0	1	1		—	—	13	29	23	7	—	—
0	1	0	0		—	—	—	—	—	—	—	—
0	1	0	1		—	—	12	28	22	6	—	—
0	1	1	0		—	—	10	26	20	4	—	—
0	1	1	1		16	0	—	—	—	—	—	—
1	0	0	0		—	—	—	—	—	—	14	30
1	0	0	1		—	—	11	27	21	5	—	—
1	0	1	0		—	—	9	25	19	3	—	—
1	0	1	1		—	—	—	—	—	—	—	—
1	1	0	0		—	—	8	24	18	2	—	—
1	1	0	1		17	1	—	—	—	—	—	—
1	1	1	1		—	—	—	—	—	—	—	—

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS[1]

PA = D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D20 ⊕ D22 ⊕ D24 ⊕ D26 ⊕ D28

PB = D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D19 ⊕ D20 ⊕ D23 ⊕ D25 ⊕ D26 ⊕ D29 ⊕ D31

PC = D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D16 ⊕ D17 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D27 ⊕ D28 ⊕ D29

PD = D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23 ⊕ D30 ⊕ D31

PE = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PF = D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D24 ⊕ D25 ⊕ D26 ⊕ D27 ⊕ D28 ⊕ D29 ⊕ D30 ⊕ D31

PG = D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15 ⊕ D16 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D20 ⊕ D21 ⊕ D22 ⊕ D23

PH0 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

PH1 = D1 ⊕ D2 ⊕ D3 ⊕ D5 ⊕ D8 ⊕ D9 ⊕ D11 ⊕ D14 ⊕ D17 ⊕ D18 ⊕ D19 ⊕ D21 ⊕ D24 ⊕ D25 ⊕ D27 ⊕ D30

PH2 = D0 ⊕ D4 ⊕ D6 ⊕ D7 ⊕ D10 ⊕ D12 ⊕ D13 ⊕ D15 ⊕ D16 ⊕ D20 ⊕ D22 ⊕ D23 ⊕ D26 ⊕ D28 ⊕ D29 ⊕ D31

NOTE:

1. S32 = 1 in $CODE_{1,0}$ = 00

64-BIT (UPPER-BIT) CONFIGURATION CODE ID_{1-0} = 11[1]

SYNDROME BITS				S32	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0
SX	S0	S1	S2									
0	0	0	0		—	—	—	—	—	—	46	62
0	0	0	1		—	—	43	59	53	37	—	—
0	0	1	0		—	—	41	57	51	35	—	—
0	0	1	1		—	—	—	—	—	—	—	—
0	1	0	0		—	—	40	56	50	34	—	—
0	1	0	1		49	33	—	—	—	—	—	—
0	1	1	0		—	—	—	—	—	—	—	—
0	1	1	1		—	—	—	—	—	—	—	—
1	0	0	1		—	—	—	—	—	—	—	—
1	0	0	1		—	—	—	—	—	—	—	—
1	0	1	0		—	—	—	—	—	—	47	63
1	0	1	1		—	—	45	61	55	39		
1	1	0	0		—	—	—	—	—	—	—	—
1	1	0	1		—	—	44	60	54	38	—	—
1	1	1	0		—	—	42	58	52	36	—	—
1	1	1	1		48	32	—	—	—	—	—	—

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(3) to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation(2)	1.0	W
I_{OUT}	DC Output Current into Outputs	30	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. P_T maximum can only be achieved by excessive I_{OL} or I_{OH}.
3. V_{IL} Min. = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level(4)		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level(4)		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	V
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	—	0.3	0.5	
			I_{OL} = 24mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	—	—	-40	µA
			V_O = V_{CC}	—	—	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V(3)		-30	—	-130	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{OP} = 0		—	—	—	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{OP} = 0		—	—	—	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	—	—	—	mA/ MHz
			COM'L.	—	—	—	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	—	—	—	mA
			COM'L.	—	—	—	
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	70	125	
			COM'L.	—	70	95	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{OP})$$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Operating frequency.

3

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to +5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-31}$	27	36	30	33
CB_{0-7} (CODE ID 00, 11)	16	34	19	23
CB_{0-7} (CODE ID 10)	16	20	19	21
$\overline{GENERATE}$	21	23	15	15
CORRECT (Not Internal Control Mode)	—	23	—	—
DIAG MODE (Not Internal Control Mode)	17	26	20	24
CODE $ID_{0,1}$	18	26	21	26
LE_{IN} (From latched to transparent)	27	38(1)	30	33
LE_{OUT} (From latched to transparent)	—	12	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	15	29	19	22
Internal Control Mode: LE_{DIAG} (From latched to transparent)	16	32	19	24
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	16	32	20	25

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 5 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	5	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	23	0
CB_{0-7} (CODE ID) 00, 11)	LE_{OUT}	15	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	15	0
CORRECT	LE_{OUT}	11	0
DIAG MODE	LE_{OUT}	17	0
CODE $ID_{0,1}$	LE_{OUT}	17	0
LE_{IN}	LE_{OUT}	25	0
$DATA_{0-31}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}$ $BYTE_{0-3}$	$DATA_{0-31}$	10	23	10	19
$\overline{OE}_{SC}$	SC_{0-7}	10	24	10	20

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	9

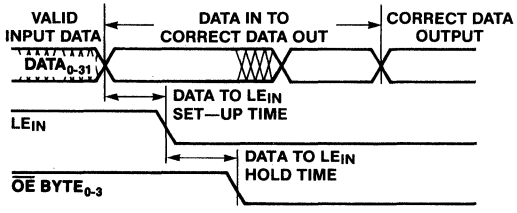


Figure 5.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460A over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to +5.0V ±10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	MULT ERROR
$DATA_{0-31}$	30	39	33	36
CB_{0-7} (CODE ID 00, 11)	19	37	22	26
CB_{0-7} (CODE ID 10)	19	23	22	24
$\overline{GENERATE}$	24	26	18	18
CORRECT (Not Internal Control Mode)	—	26	—	—
DIAG MODE (Not Internal Control Mode)	20	29	23	27
$CODE\ ID_{0,1}$	21	29	24	29
LE_{IN} (From latched to transparent)	30	41	33	36
LE_{OUT} (From latched to transparent)	—	15	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	18	32	22	25
Internal Control Mode: LE_{DIAG} (From latched to transparent)	19	35	22	27
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	19	35	23	28

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 6 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	5	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	27	0
CB_{0-7} (CODE ID 00, 11)	LE_{OUT}	18	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	18	0
CORRECT	LE_{OUT}	14	0
DIAG MODE	LE_{OUT}	20	0
$CODE\ ID_{0,1}$	LE_{OUT}	20	0
LE_{IN}	LE_{OUT}	28	0
$DATA_{0-31}$	LE_{DIAG}	5	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}\ BYTE_{0-3}$	$DATA_{0-31}$	10	25	10	21
$\overline{OE}_{SC}$	SC_{0-7}	10	27	10	22

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

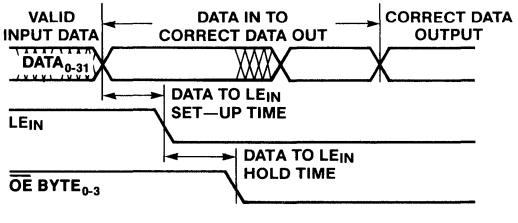


Figure 6.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the 0°C to +70°C commercial temperature range. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to +5.0V ± 5%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-31}$	37	49	40	45
CB_{0-7} (CODE ID 00, 11)	22	46	26	31
CB_{0-7} (CODE ID 10)	22	30	26	29
$\overline{GENERATE}$	29	31	21	21
CORRECT (Not Internal Control Mode)	—	31	—	—
DIAG MODE (Not Internal Control Mode)	23	35	27	33
$CODE\ ID_{0,1}$	25	35	29	35
LE_{IN} (From latched to transparent)	37	51	41	45
LE_{OUT} (From latched to transparent)	—	17	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	21	38	26	30
Internal Control Mode: LE_{DIAG} (From latched to transparent)	22	42	26	33
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	22	42	27	34

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 7 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	6	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	30	0
CB_{0-7} (CODE ID) 00, 11)	LE_{OUT}	20	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	20	0
CORRECT	LE_{OUT}	16	0
DIAG MODE	LE_{OUT}	23	0
$CODE\ ID_{0,1}$	LE_{OUT}	23	0
LE_{IN}	LE_{OUT}	31	0
$DATA_{0-31}$	LE_{DIAG}	6	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}\ BYTE_{0-3}$	$DATA_{0-31}$	10	27	10	23
$\overline{OE}_{SC}$	SC_{0-7}	10	28	10	24

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	12

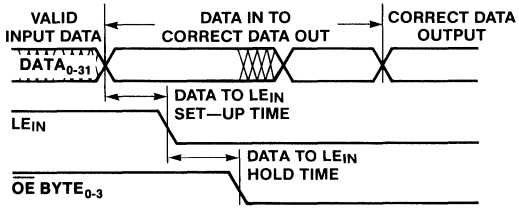


Figure 7.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance)

The tables below specify the guaranteed performance of the IDT49C460 over the -55°C to +125°C military temperature range. All times are in nanoseconds and are measured between the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC load. V_{CC} equal to +5.0V ± 10%.

COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF

FROM INPUT	TO OUTPUT			
	SC_{0-7}	$DATA_{0-31}$	ERROR	MULT ERROR
$DATA_{0-31}$	40	52	44	48
CB_{0-7} (CODE ID 00, 11)	25	49	29	34
CB_{0-7} (CODE ID 10)	25	33	29	32
$\overline{GENERATE}$	32	34	24	24
CORRECT (Not Internal Control Mode)	—	34	—	—
DIAG MODE (Not Internal Control Mode)	26	38	30	36
$CODE\ ID_{0,1}$	28	38	32	38
LE_{IN} (From latched to transparent)	40	54	44	48
LE_{OUT} (From latched to transparent)	—	20	—	—
LE_{DIAG} (From latched to transparent; Not Internal Control Mode)	24	42	29	33
Internal Control Mode: LE_{DIAG} (From latched to transparent)	25	47	29	36
Internal Control Mode: $DATA_{0-31}$ (Via Diagnostic Latch)	25	47	30	37

NOTE:

1. $DATA_{IN}$ (or LE_{IN}) to Correct Data Out measurement requires timing as shown in Figure 8 below.

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

FROM INPUT	TO (LATCHING UP DATA)	SET-UP TIME	HOLD TIME
$DATA_{0-31}$	LE_{IN}	6	4
CB_{0-7}	LE_{IN}	5	4
$DATA_{0-31}$	LE_{OUT}	36	0
CB_{0-7} (CODE ID) 00, 11)	LE_{OUT}	24	0
CB_{0-7} (CODE ID 10)	LE_{OUT}	24	0
CORRECT	LE_{OUT}	20	0
DIAG MODE	LE_{OUT}	28	0
$CODE\ ID_{0,1}$	LE_{OUT}	28	0
LE_{IN}	LE_{OUT}	37	0
$DATA_{0-31}$	LE_{DIAG}	6	3

OUTPUT ENABLE/DISABLE TIMES

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

INPUT	OUTPUT	ENABLE		DISABLE	
		MIN.	MAX.	MIN.	MAX.
$\overline{OE}\ BYTE_{0-3}$	$DATA_{0-31}$	10	29	10	25
$\overline{OE}_{SC}$	SC_{0-7}	10	30	10	26

MINIMUM PULSE WIDTHS

LE_{IN}, LE_{OUT}, LE_{DIAG}	15

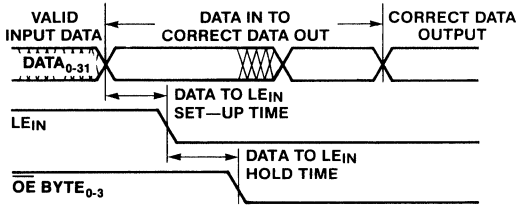


Figure 8.

INPUT/OUTPUT INTERFACE CIRCUIT

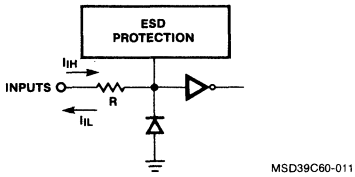


Figure 9. Input Structure (All Inputs)

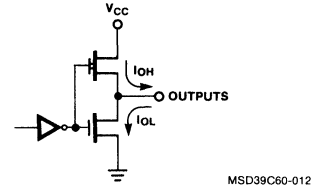


Figure 10. Output Structure

TEST LOAD CIRCUITS

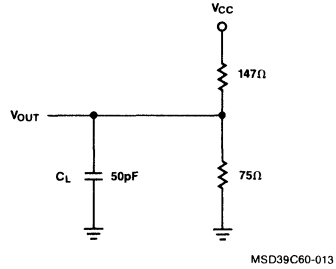


Figure 11. Output Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Fig. 11

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

Integrated Device Technology, Inc.

MICROSLICE™ Ordering Information

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT39C01CP	C	P40	Com'l.
IDT39C01CD		D40-2	
IDT39C01CC		D40-1	
IDT39C01CL		L44	
IDT39C01CF		F42	
IDT39C01CDB		D40-2	Mil.
IDT39C01CCB		D40-1	
IDT39C01CLB		L44	
IDT39C01CFB		F42	
IDT39C01DP	D	P40	Com'l.
IDT39C01DD		D40-2	
IDT39C01DC		D40-1	
IDT39C01DL		L44	
IDT39C01DF		F42	
IDT39C01DDB		D40-2	Mil.
IDT39C01DCB		D40-1	
IDT39C01DLB		L44	
IDT39C01DFB		F42	
IDT39C01EP	E	P40	Com'l.
IDT39C01ED		D40-2	
IDT39C01EC		D40-1	
IDT39C01EL		L44	
IDT39C01EF		F42	
IDT39C01EDB		D40-2	Mil.
IDT39C01ECB		D40-1	
IDT39C01ELB		L44	
IDT39C01EFB		F42	
IDT39C02AD	A	D16	Com'l.
IDT39C02AL		L20-2	
IDT39C02ADB		D16	Mil.
IDT39C02ALB		L20-2	
IDT39C03AP	A	P48	Com'l.
IDT39C03AC		D48	
IDT39C03AL		L52	
IDT39C03ACB		D48	Mil.
IDT39C03ALB		L52	
IDT39C03BP	B	P48	Com'l.
IDT39C03BC		D48	
IDT39C03BL		L52	
IDT39C03BCB		D48	Mil.
IDT39C03BLB		L52	

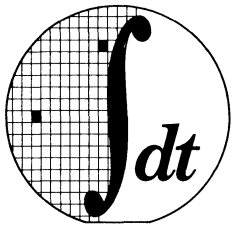
ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT39C09AP	A	P28	Com'l.
IDT39C09AD		D28-1	
IDT39C09AL		L28-3	
IDT39C09ADB		D28-1	Mil.
IDT39C09ALB		L28-3	
IDT39C09BP	A	P28	Com'l.
IDT39C09BD		D28-1	
IDT39C09BL		L28-3	
IDT39C09BDB		D28-1	Mil.
IDT39C09BLB		L28-3	
IDT39C10BP	B	P40	Com'l.
IDT39C10BD		D40-1	
IDT39C10BC		D40-2	
IDT39C10BL		L44	
IDT39C10BF		F42	
IDT39C10BDB		D40-1	Mil.
IDT39C10BCB		D40-2	
IDT39C10BLB		L44	
IDT39C10BFB		F42	
IDT39C10CP	B	P40	Com'l.
IDT39C10CD		D40-1	
IDT39C10CC		D40-2	
IDT39C10CL		L44	
IDT39C10CF		F42	
IDT39C10CDB		D40-1	Mil.
IDT39C10CCB		D40-2	
IDT39C10CLB		L44	
IDT39C10CFB		F42	
IDT39C11AP	A	P20	Com'l.
IDT39C11AD		D20	
IDT39C11AL		L20-2	
IDT39C11ADB		D20	Mil.
IDT39C11ALB		L20-2	
IDT39C11BP	B	P20	Com'l.
IDT39C11BD		D20	
IDT39C11BL		L20-2	
IDT39C11BDB		D20	Mil.
IDT39C11BLB		L20-2	
IDT39C203C	—	D48-1	Com'l.
IDT39C203L		L52	
IDT39C203CB		D48-1	Mil.
IDT39C203LB		L52	

3

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT39C203AC	A	D48-1	Com'l.
IDT39C203AL		L52	
IDT39C203ACB		D48-1	Mil.
IDT39C203ALB		L52	
IDT39C60P	—	P48	Com'l.
IDT39C60C		D48-1	
IDT39C60XC		D48-2	
IDT39C60L		L48, L52	
IDT39C60CB		D48-1	Mil.
IDT39C60XCB		D48-2	
IDT39C60LB		L48, L52	
IDT39C60AP	A	P48	Com'l.
IDT39C60AC		D48-1	
IDT39C60AXC		D48-2	
IDT39C60AL		L48, L52	
IDT39C60ACB		D48-1	Mil.
IDT39C60AXCB		D48-2	
IDT39C60ALB		L48, L52	
IDT39C60-1P	-1	P48	Com'l.
IDT39C60-1C		D48-1	
IDT39C60-1XC		D48-2	
IDT39C60-1L		L48, L52	
IDT39C60-1CB		D48-1	Mil.
IDT39C60-1XCB		D48-2	
IDT39C60-1LB		L48, L52	
IDT39C705AD	A	D28-1	Com'l.
IDT39C705AC		D28-3	
IDT39C705AL		L28-1	
IDT39C705ADB		D28-1	Mil.
IDT39C705ACB		D28-3	
IDT39C705ALB		L28-1	
IDT39C705BD	B	D28-1	Com'l.
IDT39C705BC		D28-3	
IDT39C705BL		L28-1	
IDT39C705BDB		D28-1	Mil.
IDT39C705BCB		D28-3	
IDT39C705BLB		L28-1	
IDT39C707D	—	D28-1	Com'l.
IDT39C707C		D28-3	
IDT39C707L		L28-1	
IDT39C707DB		D28-1	Mil.
IDT39C707CB		D28-3	
IDT39C707LB		L28-1	
IDT39C707AD	A	D28-1	Com'l.
IDT39C707AC		D28-3	
IDT39C707AL		L28-1	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT39C707ADB	A	D28-1	Mil.
IDT39C707ACB		D28-3	
IDT39C707ALB		L28-1	
IDT49C25	Consult Factory		
IDT49C401C	—	D64	Com'l
IDT49C401CB			Mil.
IDT49C401AC	A		Com'l.
IDT49C401ACB			Mil.
IDT49C402XC	—	D68	Com'l.
IDT49C402G		G68	
IDT49C402L		L68-1	
IDT49C402XL		L68-2	
IDT49C402XCB		D68	Mil.
IDT49C402GB		G68	
IDT49C402LB		L68-1	
IDT49C402XLB		L68-2	
IDT49C402AXC	A	D68	Com'l.
IDT49C402AG		G68	
IDT49C402AL		L68-1	
IDT49C402AXL		L68-2	
IDT49C402AXCB		D68	Mil.
IDT49C402AGB		G68	
IDT49C402ALB		L68-1	
IDT49C402AXLB		L68-2	
IDT49C403/A	Consult Factory		
IDT49C404	Consult Factory		
IDT49C410J	—	J52	Com'l.
IDT49C410C		D48-1	
IDT49C410XC		D48-2	
IDT49C410L		L48	
IDT49C410CB		D48-1	Mil.
IDT49C410XCB		D48-2	
IDT49C410LB		L48	
IDT49C410AJ	A	J52	Com'l.
IDT49C410AC		D48-1	
IDT49C410AXC		D48-2	
IDT49C410AL		L48	
IDT49C410ACB		D48-1	Mil.
IDT49C410AXCB		D48-2	
IDT49C410ALB		L48	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT49C460XC	—	D68	Com'l.
IDT49C460G		G68	
IDT49C460L		L68-1	
IDT49C460XL		L68-2	
IDT49C460XCB		D68	Mil.
IDT49C460GB		G68	
IDT49C460LB		L68-1	
IDT49C460XLB		L68-2	
IDT49C460AXC	A	D68	Com'l.
IDT49C460AG		G68	
IDT49C460AL		L68-1	
IDT49C460AXL		L68-2	
IDT49C460AXCB		D68	Mil.
IDT49C460AGB		G68	
IDT49C460ALB		L68-1	
IDT49C460AXLB		L68-2	



Integrated
Device
Technology

Digital Signal Processing (DSP)

4

DIGITAL SIGNAL PROCESSING PRODUCTS
TABLE OF CONTENTS

CONTENTS **PAGE**

Integrated Device Technology, Inc

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 512 x 9-BIT & 1024 x 9-BIT

IDT7201SA/LA
IDT7202SA/LA

FEATURES:

- First-In, First-Out dual port memory
- 512 x 9 organization (IDT7201A)
- 1024 x 9 organization (IDT7202A)
- Low power consumption
- Ultra high speed — 45ns cycle time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7201A pin and functionally compatible with Mostek MK4501 but with half-full flag capability
- IDT7202A allows for deep word structure (1024) without expansion
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance 1.2 micron CEMOS™ II technology
- Available in Plastic DIP, CERDIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7201A/7202A is a dual port memory that utilizes a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

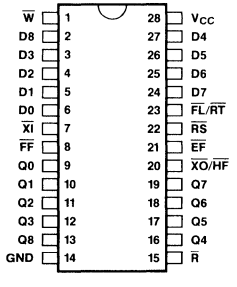
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 45ns (22MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also featues a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A half-full flag is available in the single device mode and width expansion modes.

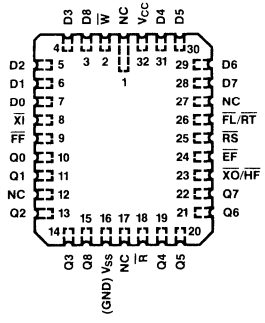
The IDT7201A/7202A is fabricated using the high speed CEMOS II, 1.2 micron technology and is available in DIPs and LCCs screened to MIL-STD-883, Method 5004. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202A allows a 1024 deep word structure without the need for expansion.

4

PIN CONFIGURATIONS

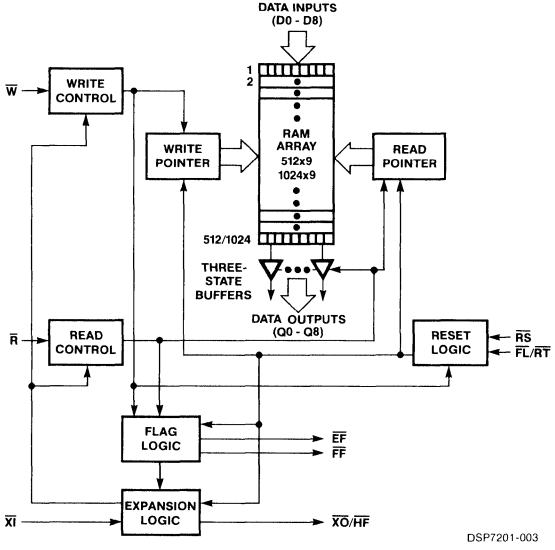


DIP
TOP VIEW



PLCC & LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V	—
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V	—
GND	Supply Voltage	0	0	0	V	—
V_{IH}	Input High Voltage Commercial	2.0	—	—	V	—
V_{IH}	Input High Voltage Military	2.2	—	—	V	—
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V	1

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7201SA/LA IDT7202SA/LA COMMERCIAL T_A = 35ns			IDT7201SA/LA IDT7202SA/LA MILITARY T_A = 40ns			IDT7201SA/LA IDT7202SA/LA COMMERCIAL T_A = 50, 65, 80, 120ns			IDT7201SA/LA IDT7202SA/LA MILITARY T_A = 50, 65, 80, 120ns			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{LI}	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	-1	—	1	-10	—	10	µA	1
I_{LO}	Output Leakage Current	-10	—	10	-10	—	10	-10	—	10	-10	—	10	µA	2
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	—	100	—	—	120	—	50	80	—	70	100	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	—	15	—	—	20	—	5	8	—	8	15	mA	3
$I_{CC3}(L)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	500	—	—	900	—	—	500	—	—	900	µA	3
$I_{CC3}(S)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	5	—	—	9	—	—	5	—	—	9	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

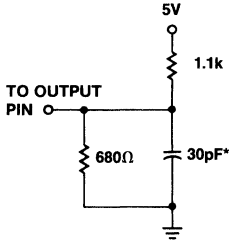
(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	COM'L		MILITARY		MILITARY AND COMMERCIAL								UNITS
		7201A/2A-35		7201A/2A-40		7201A/2A-50		7201A/2A-65		7201A/2A-80		7201A/2A-120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	35	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3, 4]	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	20	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Setup Time	18	—	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
$t_{HFH,FFH}$	Reset to Half & Full Flag High	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WEF}	Write High to Empty Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	45	—	50	—	65	—	80	—	100	—	140	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



DSP7201-004

*Includes jig and scope capacitances.

Figure 1. Output Load.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

NOTE:

Generating $\overline{R}/\overline{W}$ Signals — When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important to not have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 5ns can affect the read or write pointer and cause it to increment.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0-D8)
Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2; i.e., t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change until t_{RSR} after the rising edge of $\overline{RS}$. HALF-FULL FLAG ($\overline{HF}$) will be reset to high after master RESET ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF-FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF-FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$, so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)
This is a dual purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The IDT7201A/2A can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF-FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)
This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

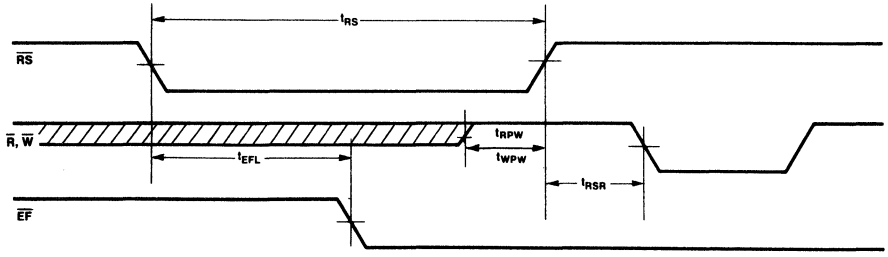
OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAT ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. if the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 512 writes for the IDT7201A and 1024 writes for the IDT7202A.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)
This is a dual purpose output. In the single device mode, when EXPANSION IN ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF-FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF-FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. W and R = V_{IH} around the rising edge of RS.

Figure 2. Reset

DSP7201-005

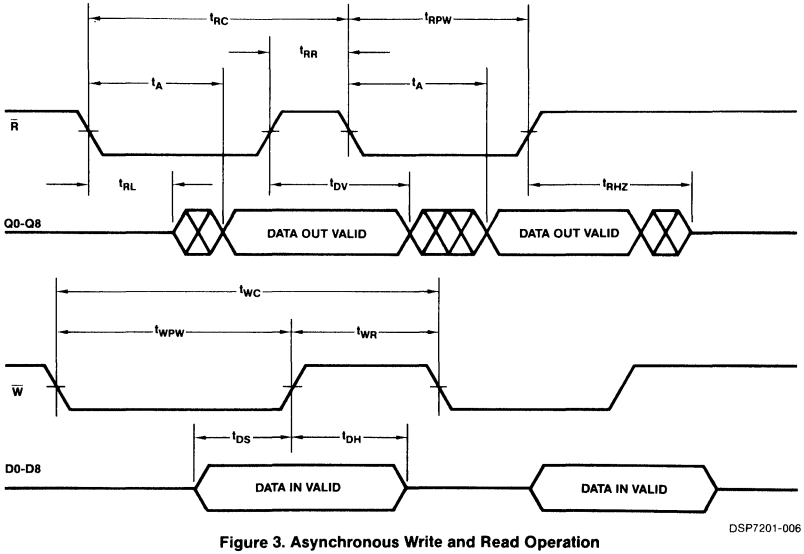


Figure 3. Asynchronous Write and Read Operation

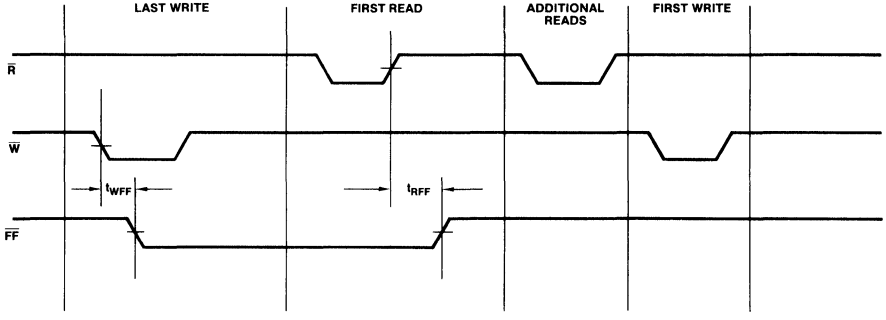


Figure 4. Full Flag From Last Write to First Read

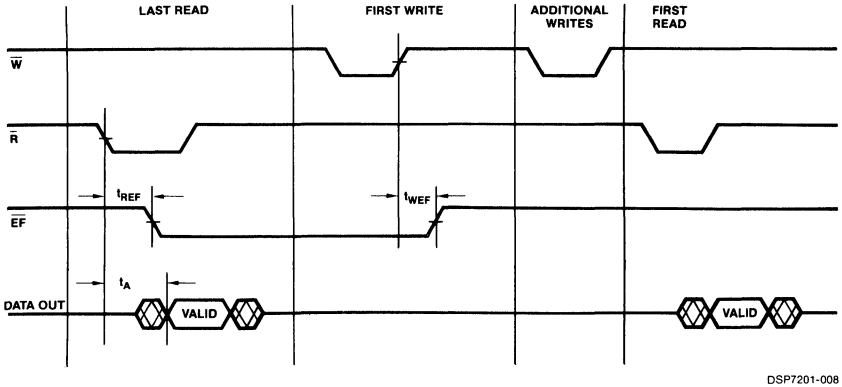
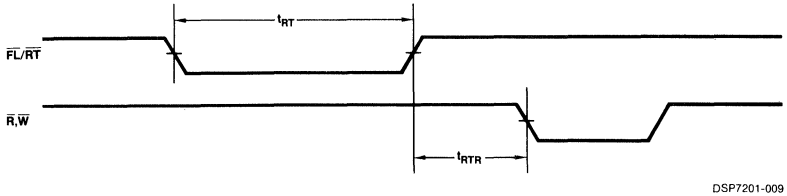


Figure 5. Empty Flag From Last Read to First Write

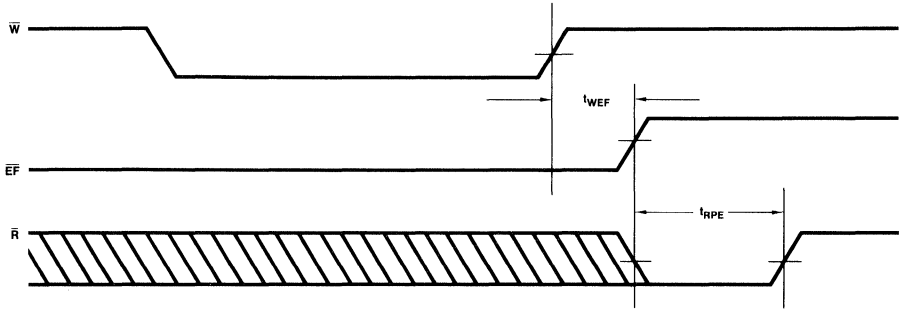


NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

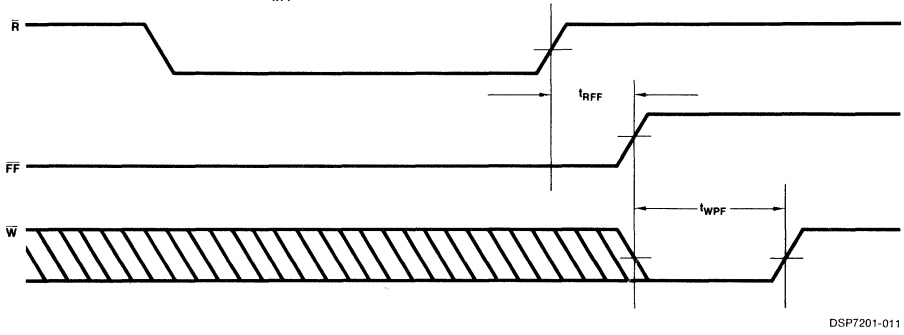


NOTE:

1. ($t_{RPE} = t_{RPW}$).

Figure 7. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:

1. ($t_{WPF} = t_{WPW}$).

Figure 8. Full Flag Timing

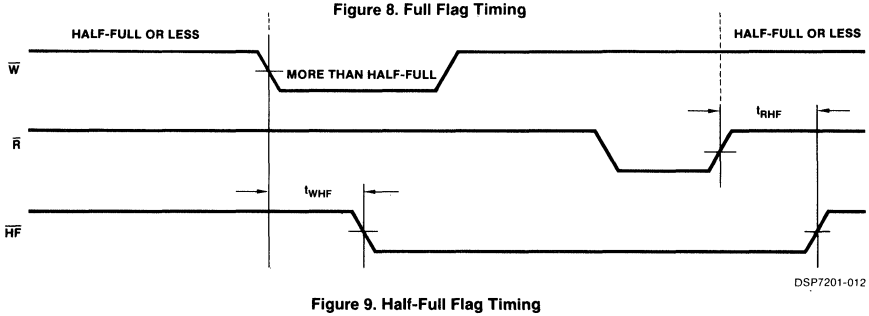


Figure 9. Half-Full Flag Timing

DATA OUTPUTS (Q0-Q8)
Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

OPERATING MODES:

SINGLE DEVICE MODE
A single IDT7201A/2A may be used when the application requirements are for 512/1024 words or less. The IDT7201A/2A is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded. (See Figure 10.) In this mode the HALF-FULL FLAG ($\overline{HF}$), which is an active low output, is shared with EXPANSION OUT ($\overline{XO}$).

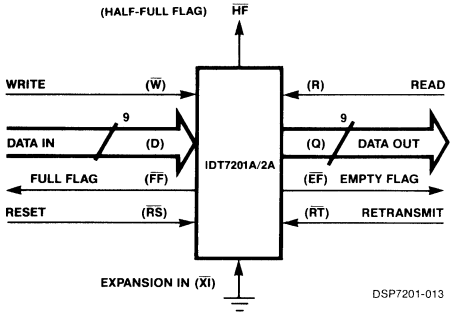
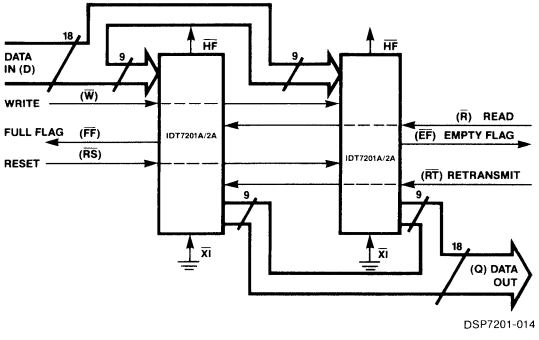


Figure 10. Block Diagram of Single 512x9/1024x9 FIFO



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 11. Block Diagram of 512x18/1024x18 FIFO Memory Used in Width Expansion Mode

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 11 demonstrates an 18-bit word width by using two IDT7201A/2As. Any word width can be attained by adding additional IDT7201A/2As.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7201A/2A can easily be adapted to applications when the requirements are for greater than 512/1024 words. Figure 12 demonstrates Depth Expansion using three IDT7201A/2As. Any depth can be attained by adding additional IDT7201A/2As. The IDT7201A/2A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 12.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 12.
5. The RETRANSMIT ($\overline{RT}$) function and HALF-FULL FLAG ($\overline{HF}$) are not available in the Depth Expansion Mode.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 13.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7201A/2As as is shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 15), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would de-assert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 16), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

4

TRUTH TABLES

TABLE I — RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

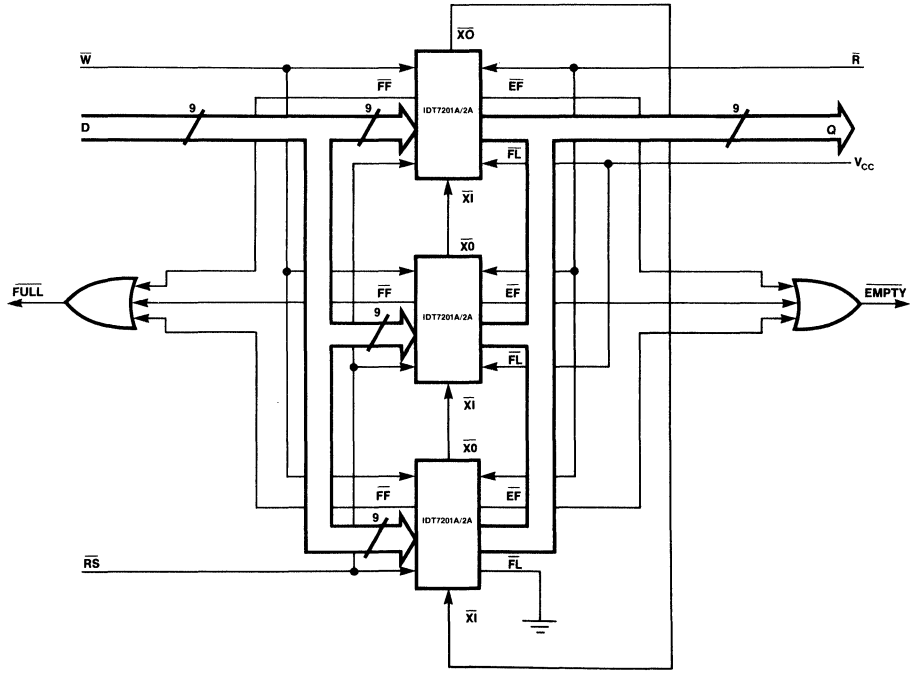
MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

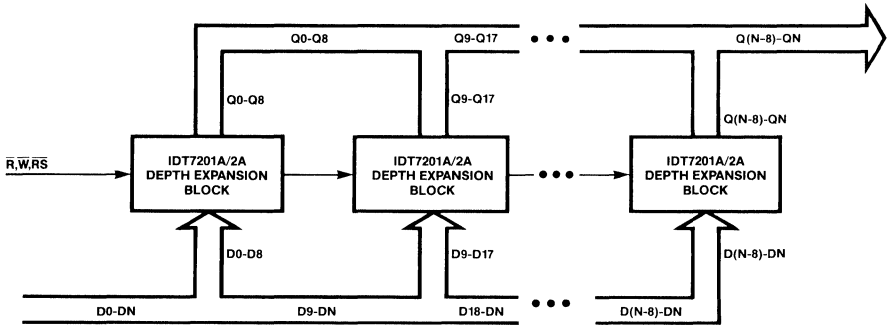
MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output.



DSP7201-015

Figure 12. Block Diagram of 1536x9/3072x9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag detection see WIDTH EXPANSION Section and Figure 11.

Figure 13. Compound FIFO Expansion

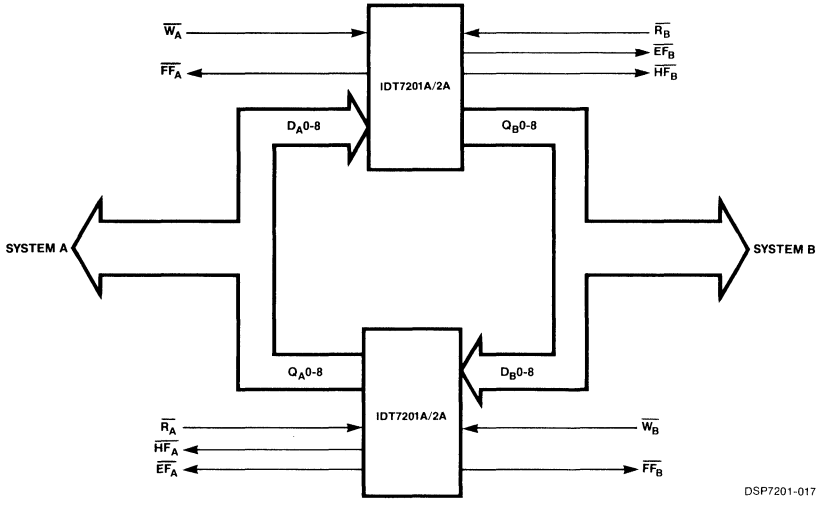
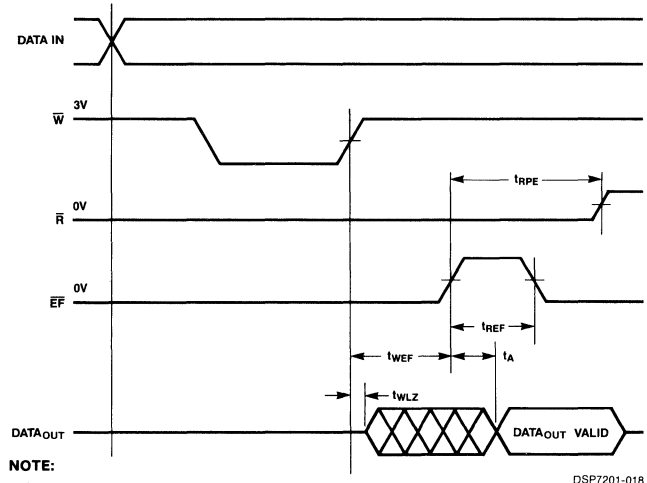


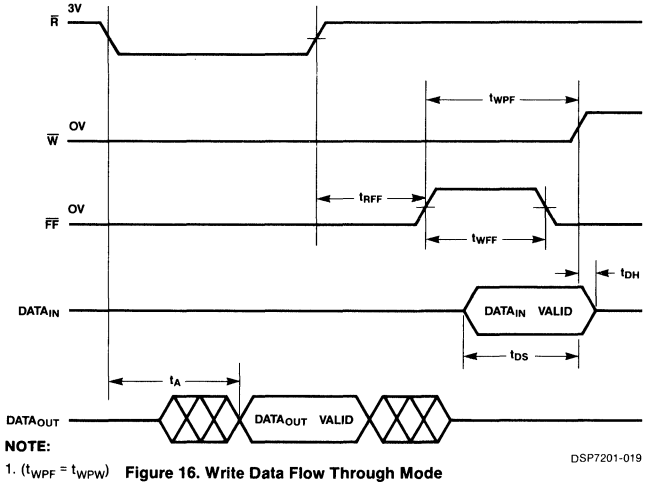
Figure 14. Bidirectional FIFO Mode

4



NOTE:
1. ($t_{RPE} = t_{RPW}$)

Figure 15. Read Data Flow Through Mode



NOTE:
1. ($t_{WPF} = t_{WPW}$)

Figure 16. Write Data Flow Through Mode

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 512 x 9-BIT & 1024 x 9-BIT

IDT7201S/L
IDT7202S/L

FEATURES:

- First-In, First-Out dual port memory
- 512 x 9 organization (IDT7201)
- 1024 x 9 organization (IDT7202)
- Low power consumption
- Ultra high speed — 45ns cycle time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7201 pin and functionally compatible with Mostek MK4501
- IDT7202 allows for deep word structure (1024) without expansion
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in Plastic DIP, CERDIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

NOTE: No Half-Full Flag on these devices. For Half-Full Flag see IDT7201SA/LA and IDT7202SA/LA data sheet.

DESCRIPTION:

The IDT7201/7202 is a dual port memory that utilizes a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

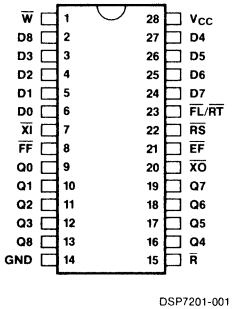
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 45ns (22MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also featues a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data.

The IDT7201/7202 is fabricated using IDT's high-speed CEMOS technology and is available in DIPs and LCCs screened to MIL-STD-883, Method 5004. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 1024 x 9 organization of the IDT7202 allows a 1024 deep word structure without the need for expansion.

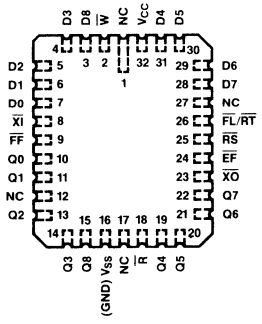
4

PIN CONFIGURATIONS



DSP7201-001

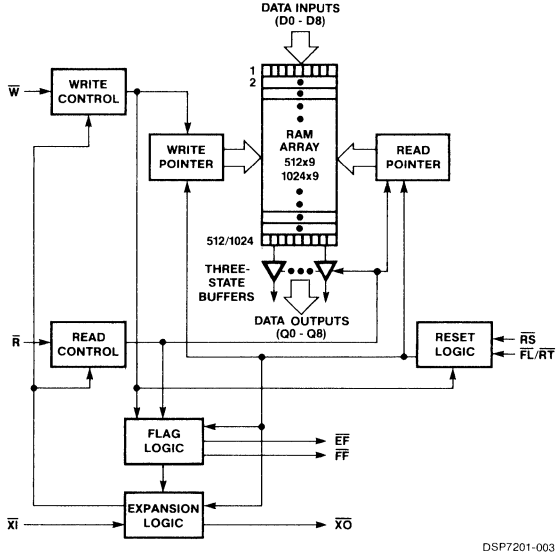
DIP
TOP VIEW



DSP7201-002

PLCC & LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



DSP7201-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V	—
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V	—
GND	Supply Voltage	0	0	0	V	—
V_{IH}	Input High Voltage Commercial	2.0	—	—	V	—
V_{IH}	Input High Voltage Military	2.2	—	—	V	—
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V	1

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7201S/L IDT7202S/L COMMERCIAL T_A = 35ns			IDT7201S/L IDT7202S/L MILITARY T_A = 40ns			IDT7201S/L IDT7202S/L COMMERCIAL T_A = 50, 65, 80, 120ns			IDT7201S/L IDT7202S/L MILITARY T_A = 50, 65, 80, 120ns			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{LI}	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	-1	—	1	-10	—	10	µA	1
I_{LO}	Output Leakage Current	-10	—	10	-10	—	10	-10	—	10	-10	—	10	µA	2
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	—	100	—	—	120	—	50	80	—	70	100	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	15	—	—	20	—	5	8	—	8	15	mA	3
$I_{CC3}(L)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	500	—	—	900	—	—	500	—	—	900	µA	3
$I_{CC3}(S)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	5	—	—	9	—	—	5	—	—	9	mA	3

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS

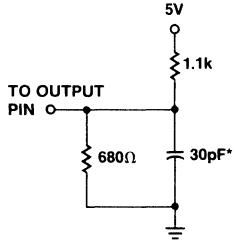
(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MILITARY		MILITARY AND COMMERCIAL								UNITS
		7201/2-35		7201/2-40		7201/2-50		7201/2-65		7201/2-80		7201/2-120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	35	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3, 4]	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	20	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Setup Time	18	—	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[2]	35	—	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WEF}	Write High to Empty Flag High	—	30	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	30	—	35	—	45	—	60	—	60	—	60	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



*Includes jig and scope capacitances.

Figure 1. Output Load.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

NOTE:

Generating $\overline{R}/\overline{W}$ signals — When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important to not have glitches, spikes or ringing on the $\overline{R}$ $\overline{W}$ (that violate the V_{IL}, V_{IH} requirements), although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 5ns can affect the read or write pointer and cause it to increment.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0-D8)
Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2; i.e., t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and should not change until t_{RSR} after the rising edge of $\overline{RS}$.

WRITE ENABLE ($\overline{W}$)
A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)
A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$, so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)
This is a dual purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The IDT7201/IDT7202 can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets.

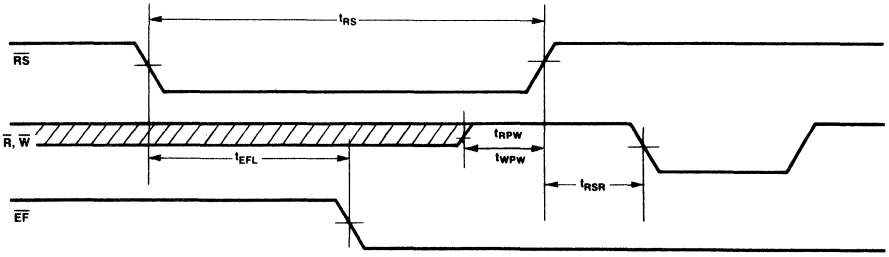
EXPANSION IN ($\overline{XI}$)
This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)
The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 512 writes for the IDT7201 and 1024 writes for the IDT7202.

EXPANSION OUT ($\overline{XO}$)
In the Depth Expansion Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q0-Q8)
Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. W and R = V_{IH} around the rising edge of RS.

Figure 2. Reset

DSP7201-005

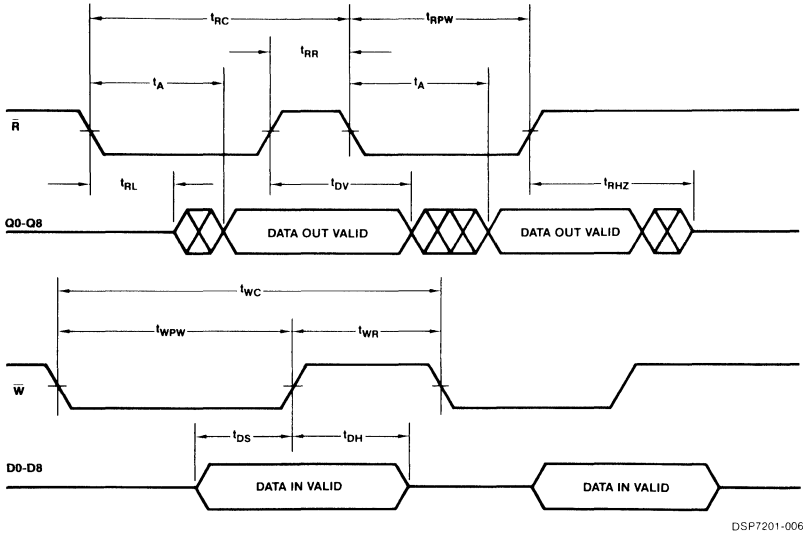


Figure 3. Asynchronous Write and Read Operation

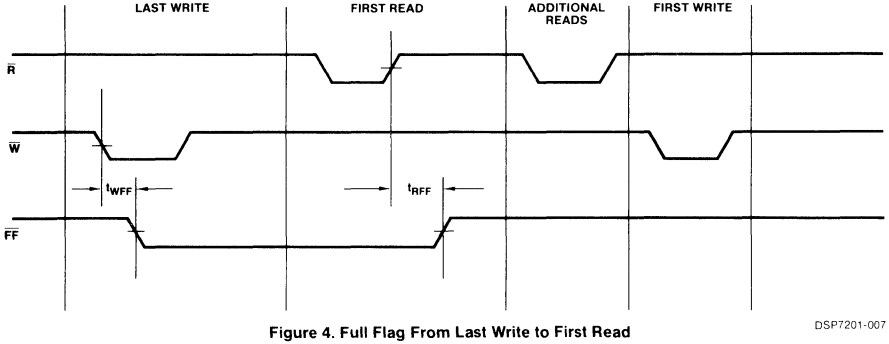


Figure 4. Full Flag From Last Write to First Read

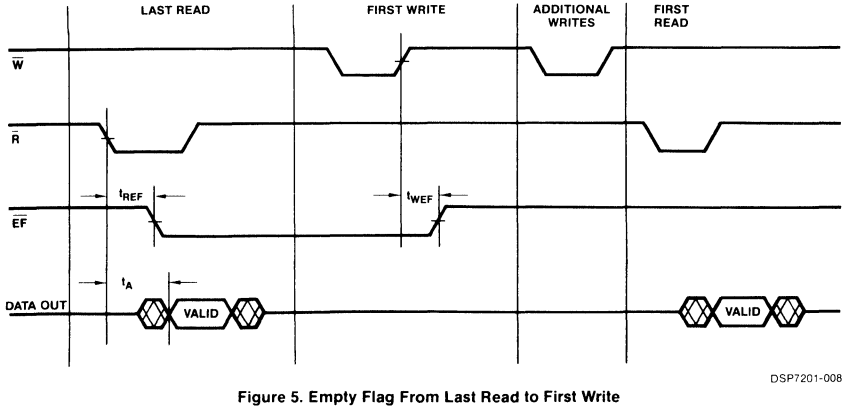
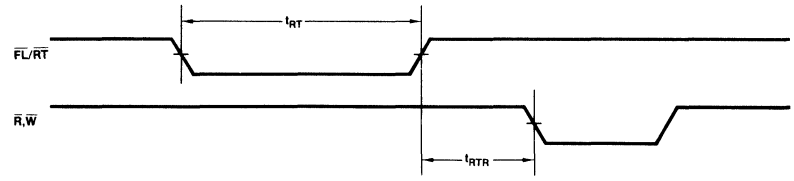


Figure 5. Empty Flag From Last Read to First Write

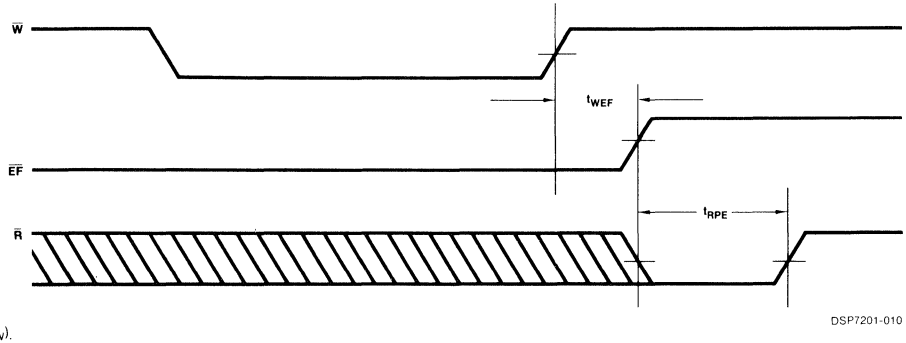


NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

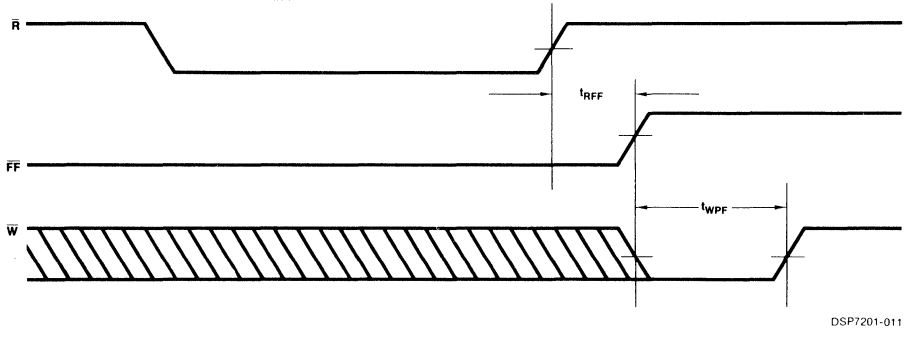


NOTE:

1. ($t_{RPE} = t_{RPW}$).

Figure 7. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:

1. ($t_{WPF} = t_{WPW}$).

Figure 8. Full Flag Timing

OPERATING MODES: SINGLE DEVICE MODE

A single IDT7201/IDT7202 may be used when the application requirements are for 512/1024 words or less. The IDT7201/IDT7202 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded. (See Figure 9).

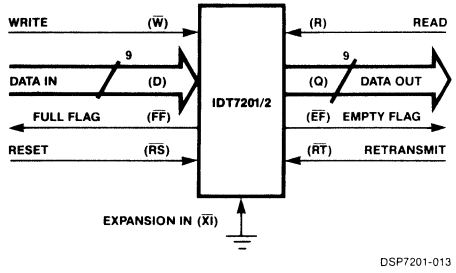
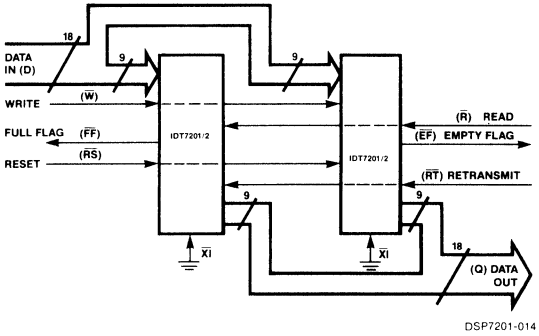


Figure 9. Block Diagram of Single 512x9/1024x9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 10 demonstrates an 18-bit word width by using two IDT7201/IDT7202s. Any word width can be attained by adding additional IDT7201/IDT7202s.



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$, signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 10. Block Diagram of 512x18/1024x18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7201/IDT7202 can easily be adapted to applications when the requirements are for greater than 512/1024 words. Figure 11 demonstrates Depth Expansion using three IDT7201/IDT7202s. Any depth can be attained by adding additional IDT7201/IDT7202s. The IDT7201/IDT7202 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 11.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 11.
5. The RETRANSMIT ($\overline{RT}$) function is not available in the Depth Expansion Mode.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 12.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7201/IDT7202s as is shown in Figure 13. Care must be taken to assure that the appropriate flag is monitored by each system; (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted — a read flow-through and a write flow-through mode. For the read flow-through mode (Figure 14), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The EF line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would de-assert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In a write flow-through mode (Figure 15), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted, but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, a new word is loaded into the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data into the FIFO and increment the write pointer.

4

TRUTH TABLES

TABLE I — RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset	0	X	0	Location Zero	Location Zero	0	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 11.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

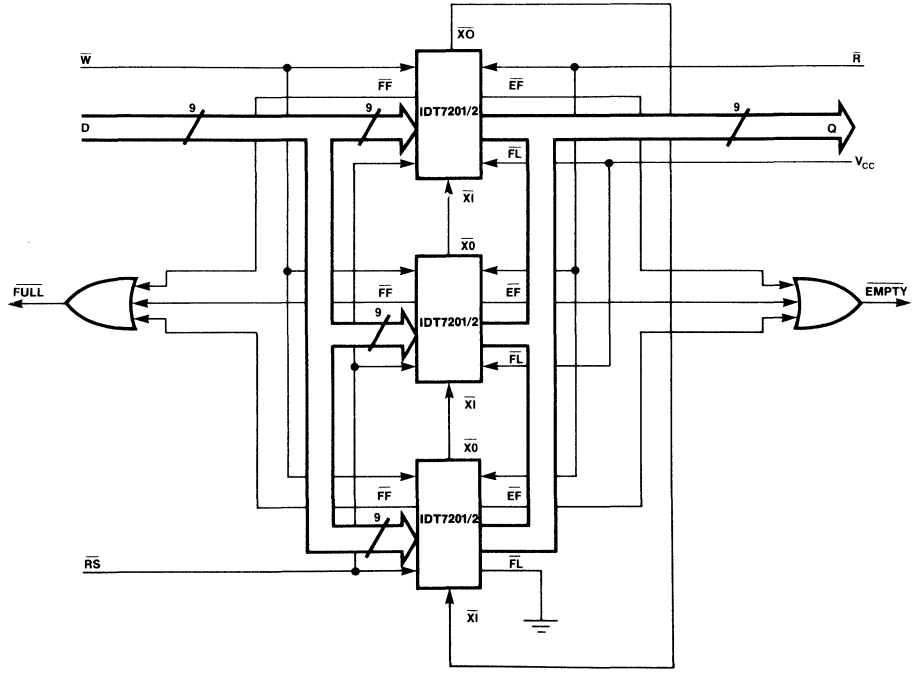


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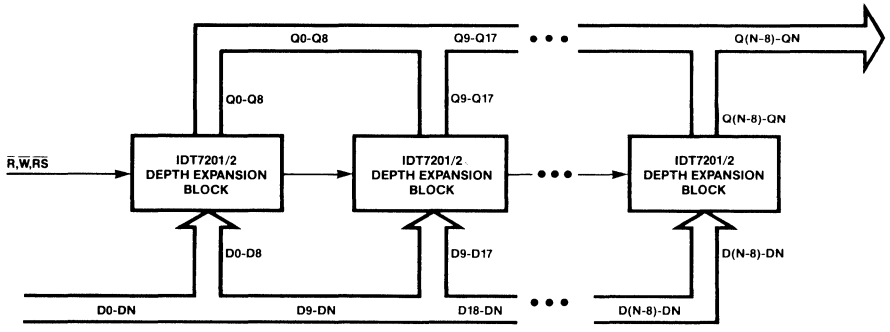
Figure 11. Block Diagram of 1536x9/3072x9 FIFO Memory (Depth Expansion)



NOTES:

1. For depth expansion block see DEPTH EXPANSION Section and Figure 11.
2. For detection see WIDTH EXPANSION Section and Figure 10.

Figure 12. Compound FIFO Expansion

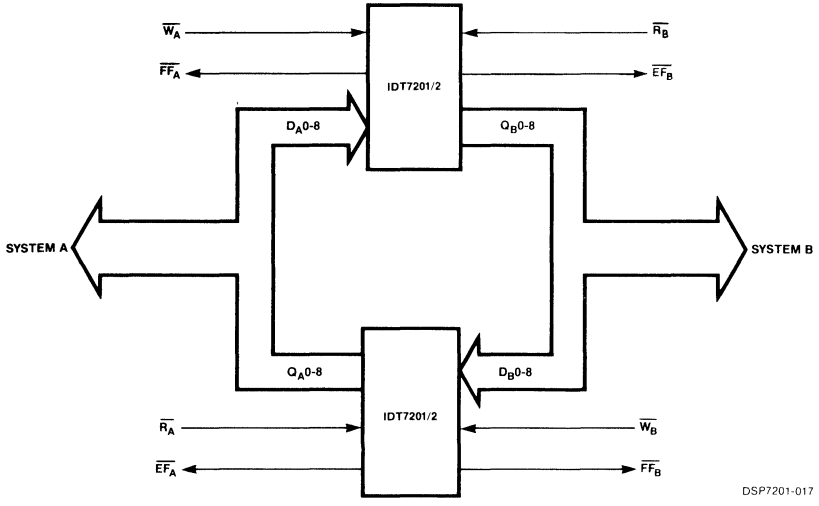


Figure 13. Bidirectional FIFO Mode

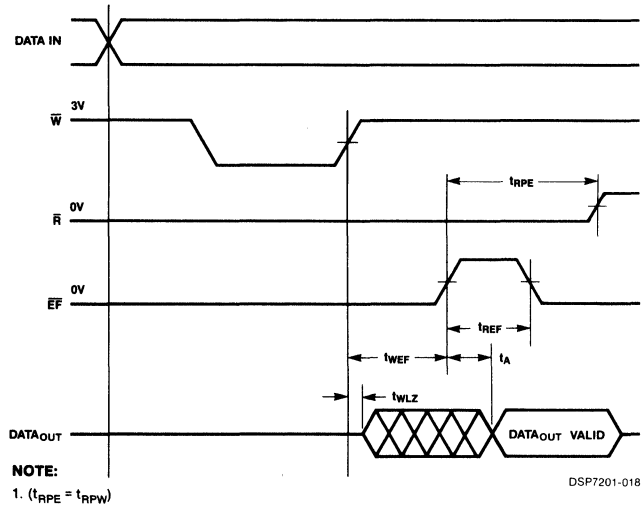


Figure 14. Read Data Flow Through Mode

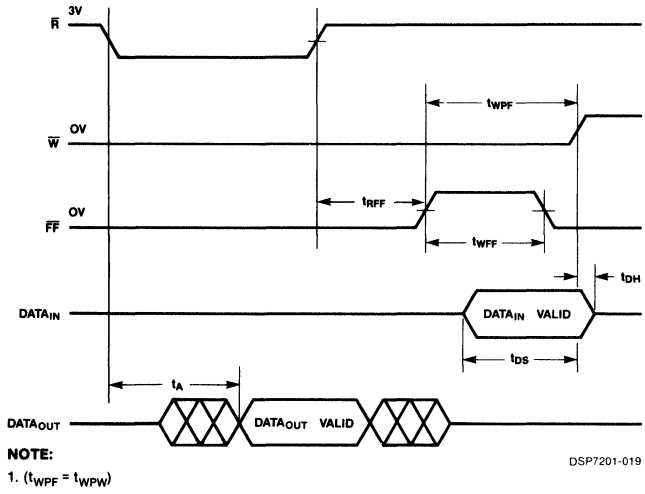


Figure 15. Write Data Flow Through Mode

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 2048 x 9-BIT & 4096 x 9-BIT

PRELIMINARY
IDT7203S/L
IDT7204S/L

FEATURES:

- First-In, First-Out dual port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- Low power consumption
  —Active: 660mW (max.)
  —Power down: 66mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with IDT7201/02
- IDT7204 allows 4096 word structure without expansion
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Auto retransmit capability
- High-performance CEMOS™ II technology
- Available in DIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7203/7204 is a dual port memory that utilizes a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

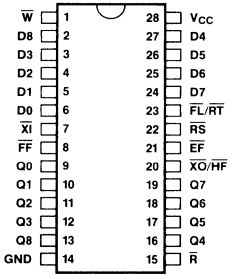
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz).

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A half-full flag is available in the single device mode and width expansion modes.

The IDT7203/7204 is fabricated using the high-speed CEMOS™ II, 1.5 micron technology and is available in DIP and LCC screened to MIL-STD-883, Method 5004. It is designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. The 4096 x 9 organization for the IDT7204 allows a 4096 deep word structure without the need for expansion.

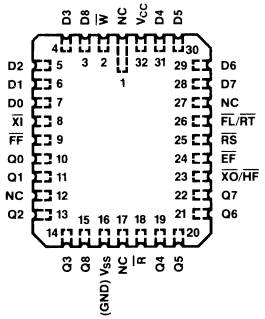
4

PIN CONFIGURATIONS



DSP7201-001

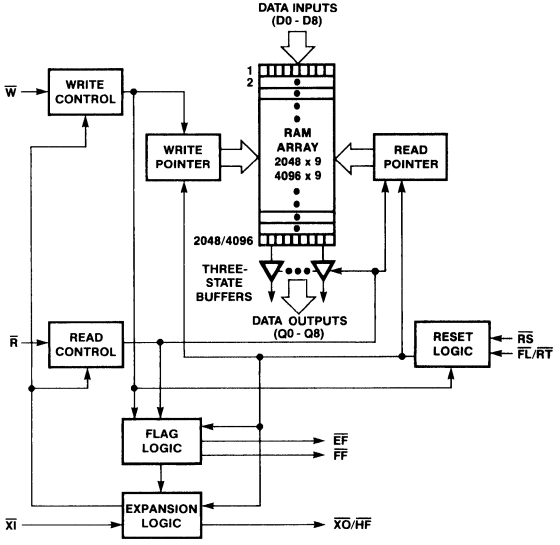
DIP
TOP VIEW



DSP7201-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



DSP7203-001

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V	—
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V	—
GND	Supply Voltage	0	0	0	V	—
V_{IH}	Input High Voltage Commercial	2.0	—	—	V	—
V_{IH}	Input High Voltage Military	2.2	—	—	V	—
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V	1

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7203S/L IDT7204S/L COMMERCIAL			IDT7203S/L IDT7204S/L MILITARY			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{IL}	Input Leakage Current (Any Input)	-1	—	1	-10	—	10	μA	1
I_{OL}	Output Leakage Current	-10	—	10	-10	—	10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	75	120	—	100	150	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	—	8	12	—	12	25	mA	3
$I_{CC3}(L)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	2	—	—	4	mA	3
$I_{CC3}(S)$	Power Down Current (All Input = V_{CC} -0.2V)	—	—	8	—	—	12	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{OUT}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.

AC ELECTRICAL CHARACTERISTICS[1] (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

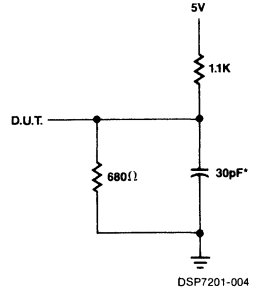
SYMBOL	PARAMETERS	IDT7203/4-50		IDT7203/4-65		IDT7203/4-80		IDT7203/4-120		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Read Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_A	Access Time	—	50	—	65	—	80	—	120	ns	—
t_{RR}	Read Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{RPW}	Read Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{RLZ}	Read Pulse Low to Data Bus at Low Z	10	—	10	—	10	—	10	—	ns	3
t_{WLZ}	Write Pulse High to Data Bus at Low Z	15	—	15	—	20	—	20	—	ns	3
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns	—
t_{RHZ}	Read Pulse High to Data Bus at High Z	—	30	—	30	—	30	—	35	ns	3
t_{WC}	Write Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_{WPW}	Write Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{WR}	Write Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{DS}	Data Setup Time	30	—	30	—	40	—	40	—	ns	—
t_{DH}	Data Hold Time	5	—	10	—	10	—	10	—	ns	—
t_{RSC}	Reset Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_{RS}	Reset Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{RSR}	Reset Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{RTC}	Retransmit Cycle Time	65	—	80	—	100	—	140	—	ns	—
t_{RT}	Retransmit Pulse Width	50	—	65	—	80	—	120	—	ns	2
t_{RTR}	Retransmit Recovery Time	15	—	15	—	20	—	20	—	ns	—
t_{EFL}	Reset to Empty Flag Low	—	65	—	80	—	100	—	140	ns	—
t_{REF}	Read Low to Empty Flag Low	—	45	—	60	—	70	—	110	ns	—
t_{RFF}	Read High to Full Flag High	—	45	—	60	—	70	—	110	ns	—
t_{WEF}	Write High to Empty Flag High	—	45	—	60	—	70	—	110	ns	—
t_{WFF}	Write Low to Full Flag Low	—	45	—	60	—	70	—	110	ns	—
t_{WHF}	Write Low to Half Full Flag Low	—	65	—	80	—	100	—	140	ns	—
t_{RHF}	Read High to Half Full Flag High	—	65	—	80	—	100	—	140	ns	—

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



***Includes jig and scope capacitances.**

Figure 1. Output Load.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)[1]

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT	NOTES
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF	3
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF	2,3

NOTES:

1. This parameter is sampled and not 100% tested.
2. With output deselected.
3. Characterized values, not currently tested.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0 - D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset. HALF FULL FLAG ($\overline{HF}$) will be reset to high after master RESET ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual purpose output. In the Multiple Device Mode, this pin is grounded to indicate that it is the first device loaded. (See Operating Modes.) In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the EXPANSION IN ($\overline{XI}$).

The IDT7203/4 can be made to retransmit data when the RETRANSMIT ENABLE CONTROL ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual purpose pin. EXPANSION IN ($\overline{XI}$) is grounded to indicate an operation in the single device mode. EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 2048 writes for the IDT7203 and 4096 writes for the IDT7204.

EXPANSION OUT/HALF FULL FLAG ($\overline{XO}/\overline{HF}$)

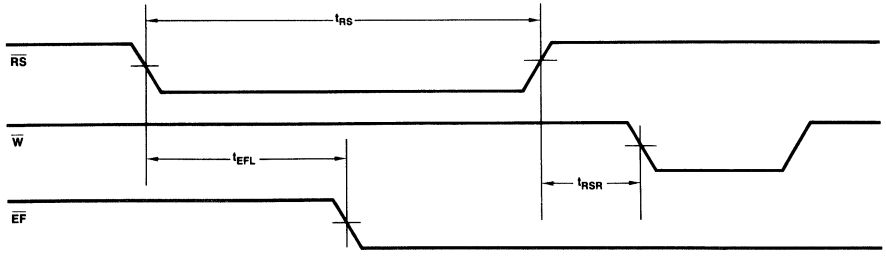
This is a dual purpose output. In the single device mode, when EXPANSION IN ($\overline{XI}$) is grounded, this output acts as an indication of a half full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the HALF FULL FLAG ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The HALF FULL FLAG ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Multiple Device Mode, EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q0 - Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

Figure 2. Reset

DSP7201-005

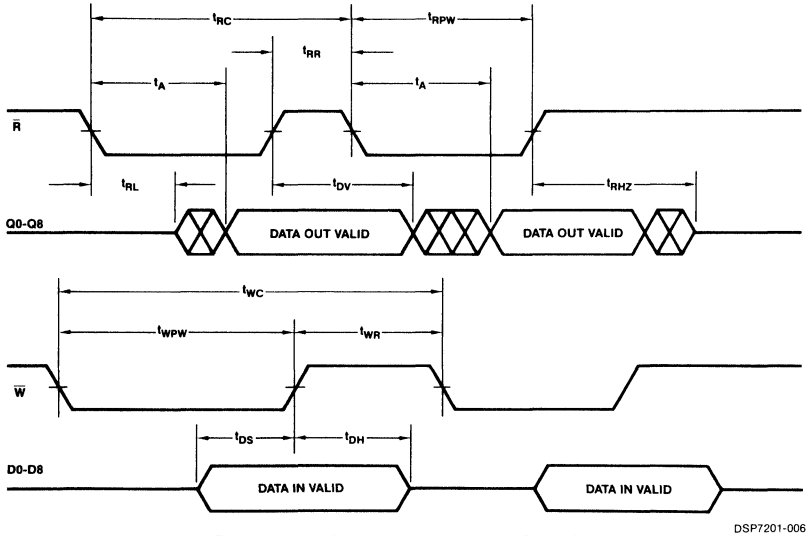


Figure 3. Asynchronous Write and Read Operation

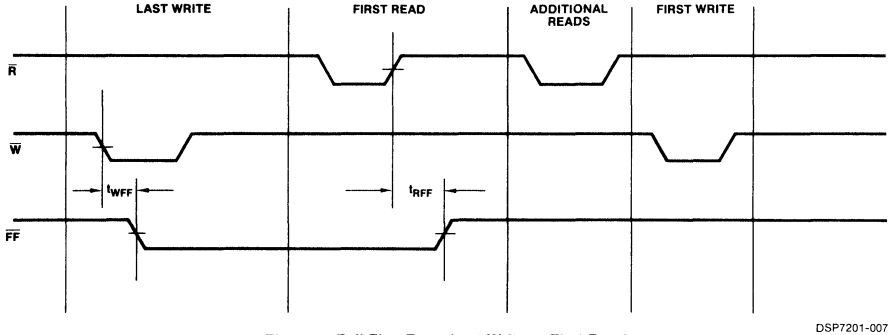


Figure 4. Full Flag From Last Write to First Read

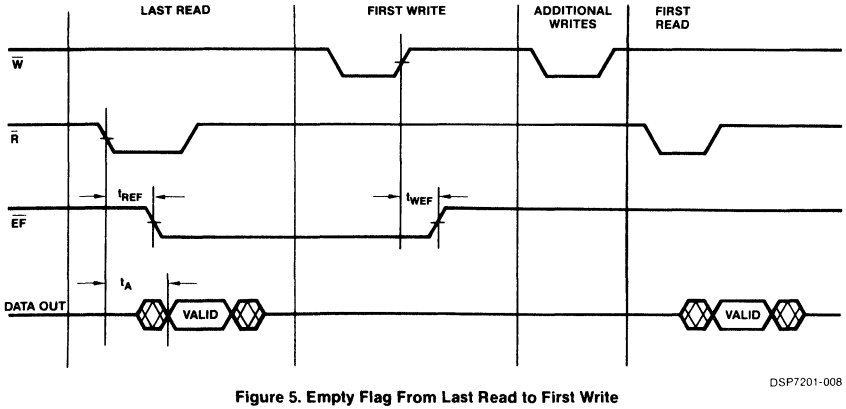
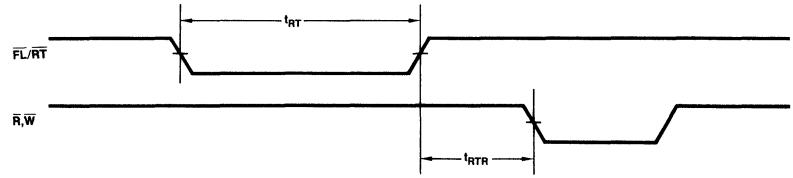


Figure 5. Empty Flag From Last Read to First Write

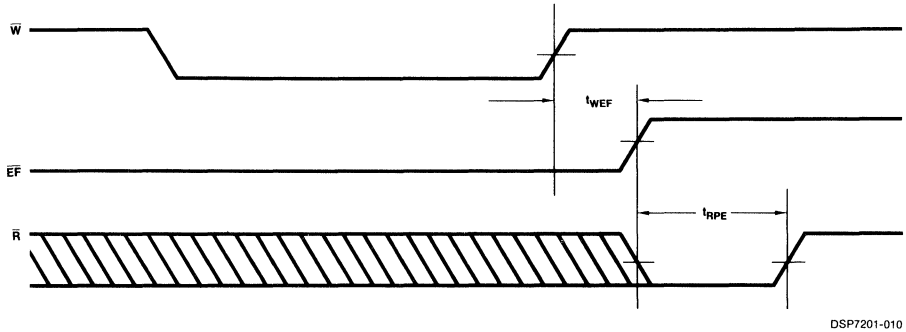


NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

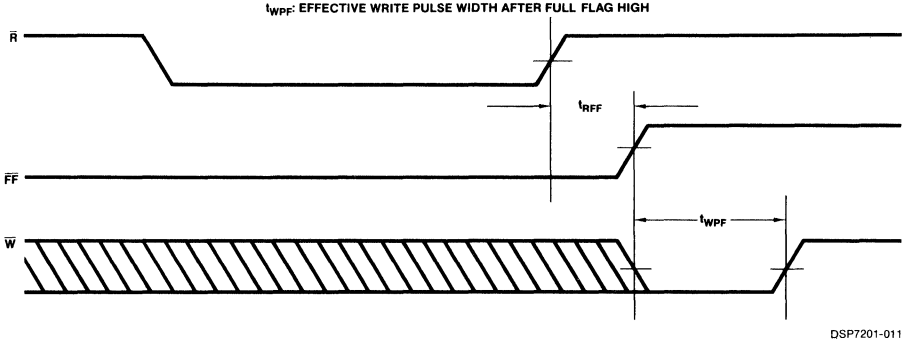


NOTE:

1. ($t_{RPE} = t_{RPW}$).

Figure 7. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:

1. ($t_{WPF} = t_{WPW}$).

Figure 8. Full Flag Timing

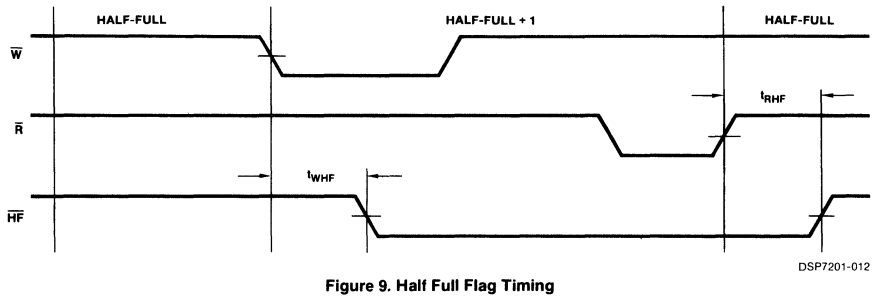


Figure 9. Half Full Flag Timing

OPERATING MODES:
SINGLE DEVICE MODE

A single IDT7203/4 may be used when the application requirements are for 2048/4096 words or less. The IDT7203/4 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is grounded. (See Figure 10.) In this mode the HALF FULL FLAG ($\overline{HF}$), which is an active low output, is shared with EXPANSION OUT ($\overline{XO}$).

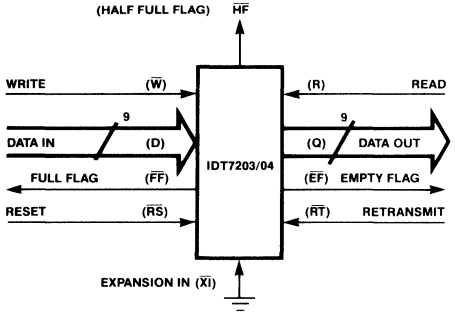
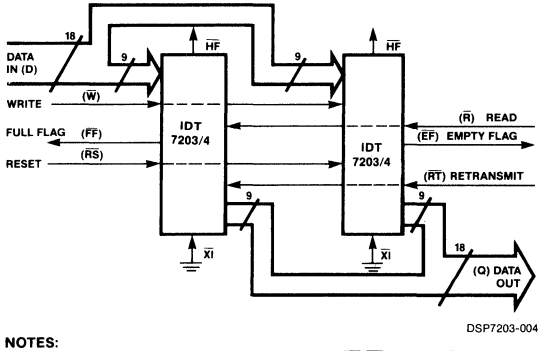


Figure 10. Block Diagram of Single 2048 x 9/4096 x 9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 11 demonstrates an 18-bit word width by using two IDT7203/4s. Any word width can be attained by adding additional IDT7203/4s.



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 11. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7203/4 can easily be adapted to applications when the requirements are for greater than 2048/4906 words. Figure 12 demonstrates Depth Expansion using three IDT7203/4s. Any depth can be attained by adding additional IDT7203/4s. The IDT7203/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other device must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 12.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s. (I.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 12.
5. The RETRANSMIT ($\overline{RT}$) function and HALF FULL FLAG ($\overline{HF}$) are not available in the Depth Expansion Mode.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 13.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7203/4s as is shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system. (I.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW THRU MODES

Two types of flow through modes are permitted with the IDT7203/7204. A read flow through and write flow through mode. For the read flow through mode (Figure 15), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow through mode (Figure 16), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

4

TRUTH TABLES

TABLE I — RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

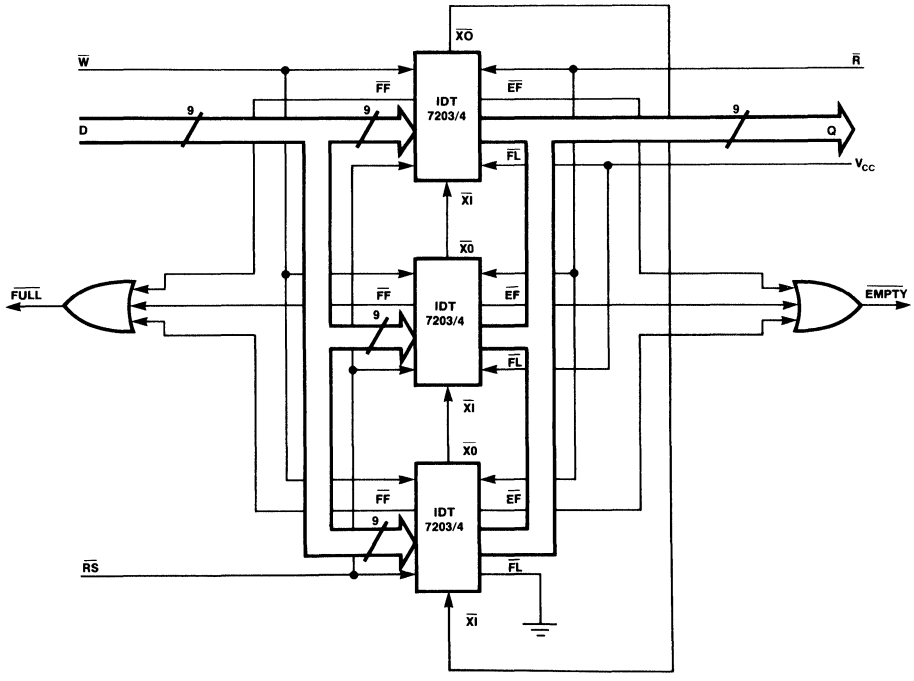
MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

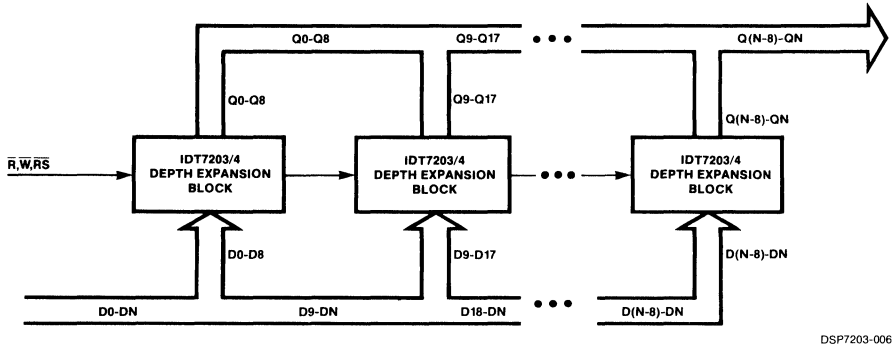
MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half Full Flag Output.



DSP7203-005

Figure 12. Block Diagram of 6,144 x 9/12,288 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 12.
2. For Flag detection see WIDTH EXPANSION Section and Figure 11.

Figure 13. Compound FIFO Expansion

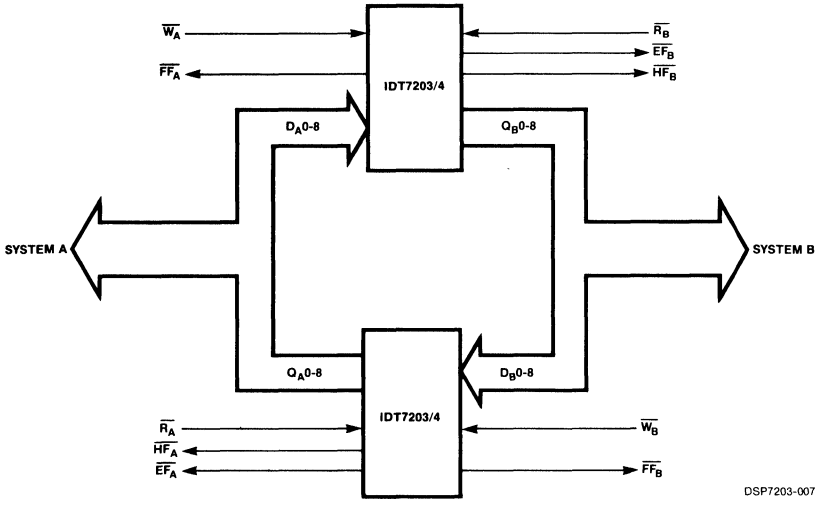


Figure 14. Bidirectional FIFO Mode

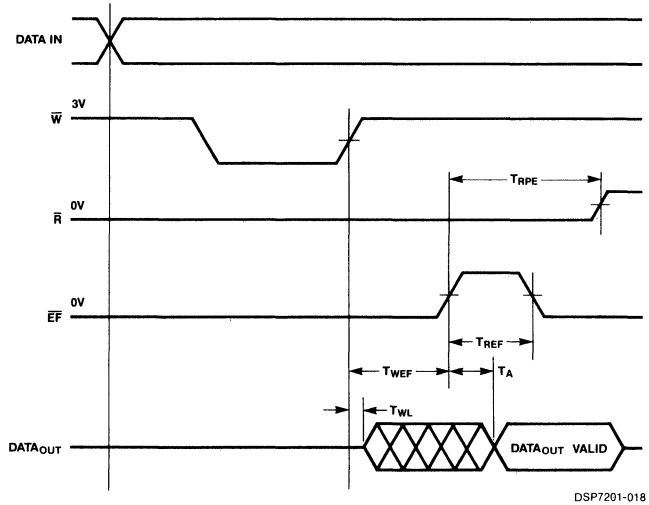


Figure 15. Read Data Flow-Through Mode

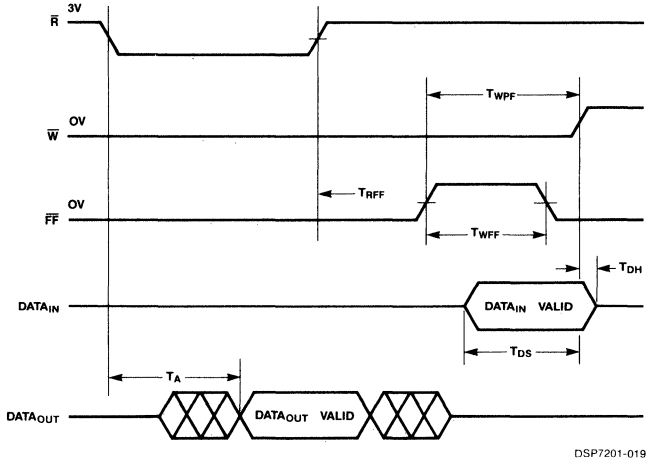


Figure 16. Write Data Flow-Through Mode

Integrated Device Technology, Inc.

64-BIT IEEE FLOATING POINT MULTIPLIER AND ALU

ADVANCE INFORMATION
IDT72064
IDT72065

FEATURES:

- Pin and functionally compatible with Weitek 1064/1065
- Low-power (750mW typical per device) operation
- Single 5 volt supply — no need for two supplies
- Advanced CEMOS™ II 1.5 micron technology
- Fully conforms to the requirements of IEEE Standard 754, version 10.0 for full 32-bit and 64-bit multiply and arithmetic operations.
- Very high-speed operation
  - —10 megaflops (100ns) pipelined ALU operation (add/subtract/convert/compare)
  - —5 megaflops (200ns) pipelined 32-bit (single precision) multiplications
  - —2.5 megaflops (400ns) pipelined 64-bit (double precision) multiplications
- Full floating point function arithmetic logic unit including:
  - —Add
  - —Subtract
  - —Absolute Value
  - —Compare
  - —Conversion to and from two's complement integer
- Flexible system design
  - —Three 32-bit ports allow two data inputs and one result output every 50ns
  - —One, two, or three port architectures supported
  - —Single phase, edge-triggered clock interface, with fully registered TTL or CMOS compatible inputs and outputs
- Standard 144-pin grid array package

DESCRIPTION:

The IDT72064 floating-point multiplier and the IDT72065 floating-point ALU provide high-speed 32-bit and 64-bit floating-point processing capability.

The IDT72064/065 are fabricated using IDT's advanced CEMOS II 1.5 micron technology and are capable of a total multiply latency (time required from the input of the operand until the result can be used by another device) of 500ns for single precision and 700ns for double precision multiplications. This ultra-high speed performance is achieved by combining both state-of-the-art CEMOS technology and advanced circuit design techniques.

For signal processing applications, where higher throughput speeds are required, operations including the function specification can be pipelined. For single precision multiplications, new operands can be loaded and a product unloaded every 200ns while double precision multiplies can be accomplished at a 400ns rate. The IDT72065 ALU executes all operations at a 100ns pipelined throughput. All operations including the function specification are pipelined so there is no penalty for interleaving various functions. The on-chip pipeline is automatically advanced using internal timers, so explicit pipeline flushing is not required.

This flexible two-chip set operates in full conformance with the requirements of IEEE standard 754 revision 10.0. It performs operations on single (32-bit) and double (64-bit) precision operands as well as conversion to 32-bit two's complement integers. The IDT72064/065 accommodates all rounding modes, infinity and reserved operand representations, and the treatment of exceptions, such as overflow, underflow, invalid and inexact operations. Exact conformance to the standards ensures complete software portability between prototype development and final application. A "FAST" mode eliminates the time penalty for denormalized numbers by substituting zero for a denormalized number.

The flexible input/output architecture of these devices allows them to be used in systems with one, two, or three 32-bit buses, or one 64-bit bus. Fully registered inputs and outputs, separately controlled, are loaded on each positive-going transition of the clock.

A 6-bit function control determines the arithmetic function to be performed while a 4-bit status output flags arithmetic exceptions and conditions. Both the function inputs and status outputs propagate along with the data to ease system design timing.

4

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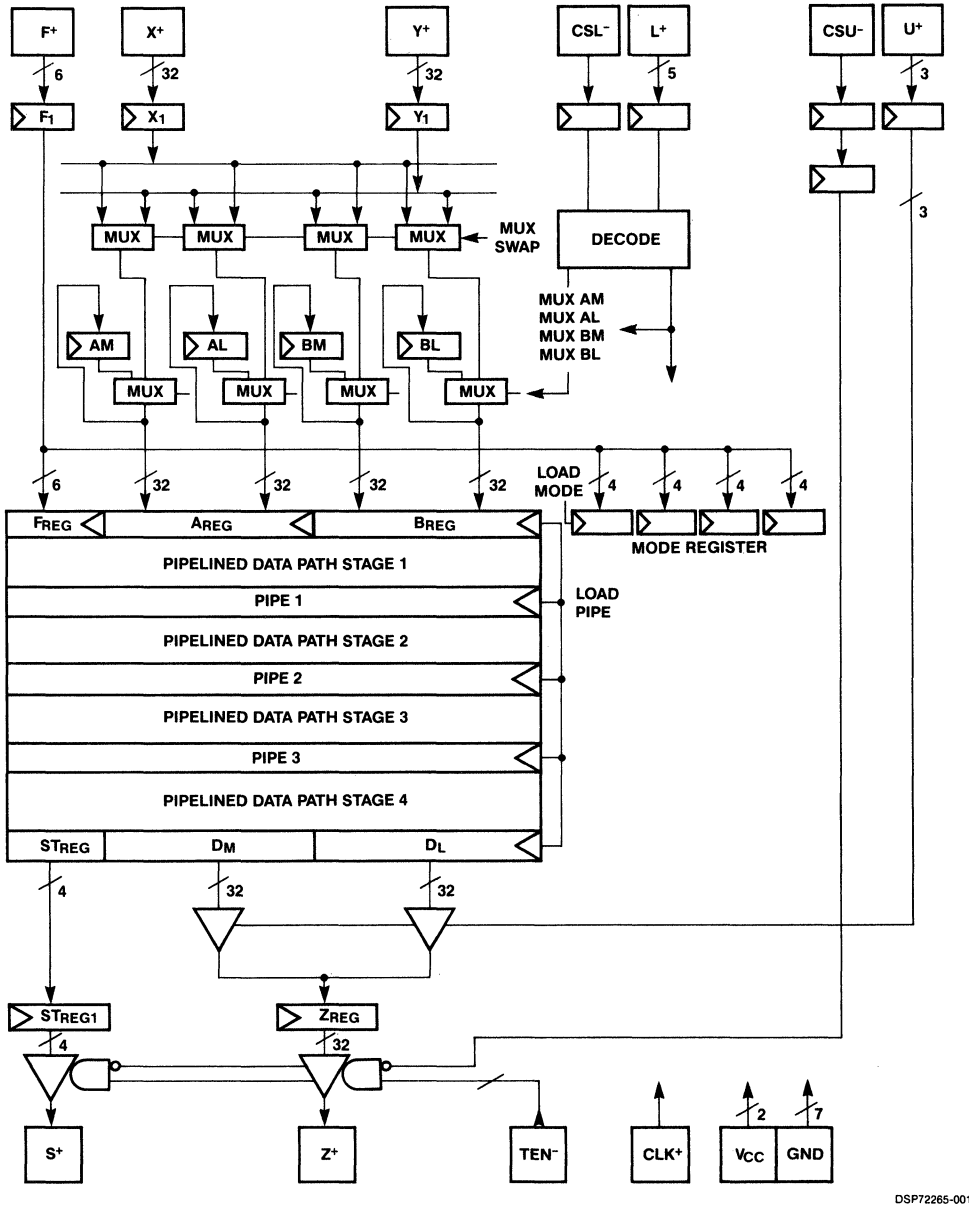
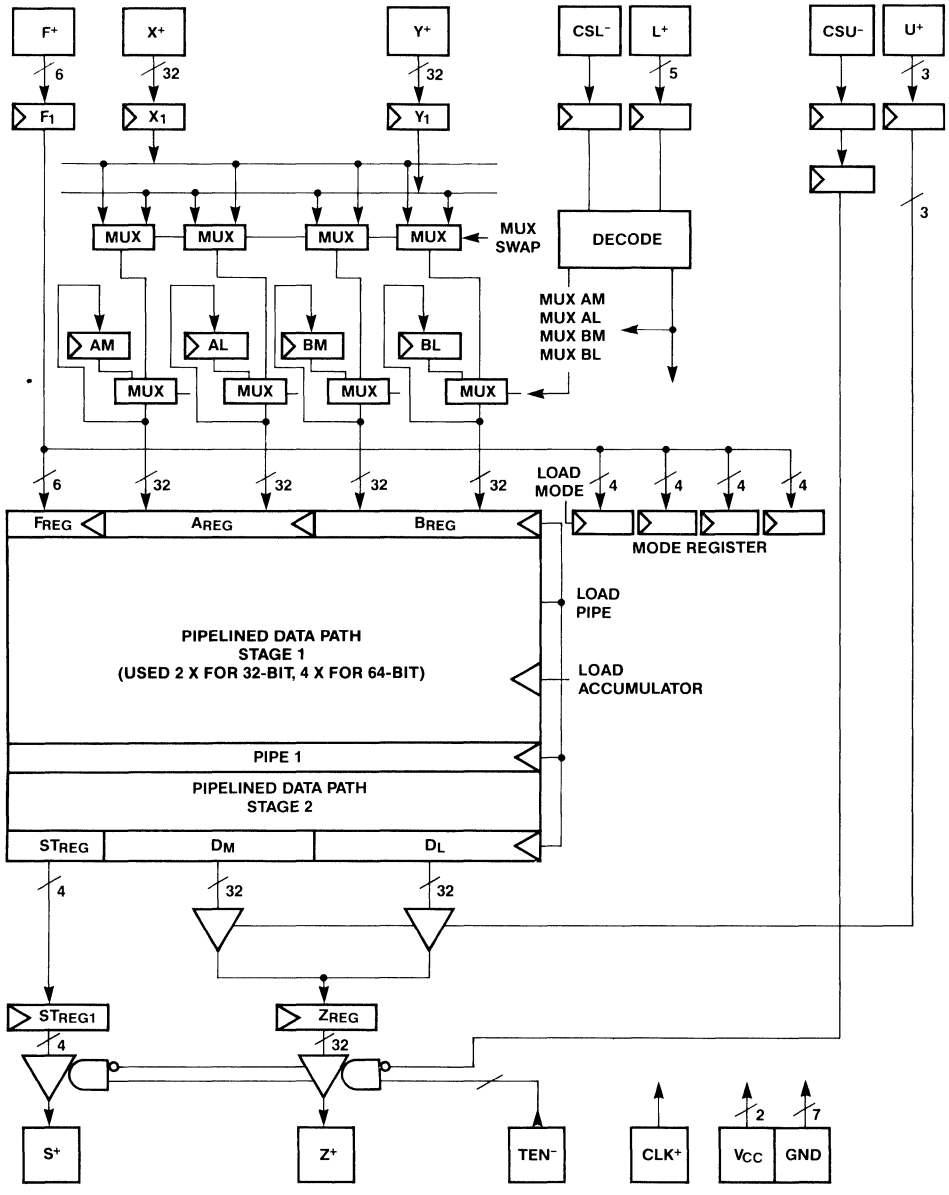
FUNCTIONAL BLOCK DIAGRAM
IDT72065 FLOATING POINT ALU



DSP72265-001

FUNCTIONAL BLOCK DIAGRAM
IDT72065 FLOATING POINT MULTIPLIER



DSP72265-002

PIN CONFIGURATION

GND	Z_{31}	Z_{14}	Z_{13}	Z_{27}	Z_{10}	Z_{25}	Z_{24}	Z_7	Z_{22}	Z_{20}	Z_{19}	Z_3	Z_1	GND
S_3	NC	V_{CC}	Z_{15}	Z_{29}	Z_{12}	Z_{11}	Z_9	Z_6	Z_{21}	Z_4	Z_{18}	Z_{17}	V_{CC}	Y_0
GND	S_2	NC	NC	Z_{30}	Z_{28}	Z_{26}	Z_8	Z_{23}	Z_5	Z_2	Z_{16}	Z_0	GND	Y_{17}
TEN	S_0	NC										NC	Y_{16}	Y_{18}
U_2	CSU	S_1										Y_1	Y_2	Y_4
NC	U_0	U_1										Y_3	Y_{19}	Y_{21}
NC	CLK	NC										Y_5	Y_{20}	Y_6
F_5	F_4	V_{SS}										Y_{23}	Y_{22}	Y_7
F_3	F_0	F_1										Y_8	Y_{25}	Y_{24}
F_2	NC	L_4										Y_{26}	Y_{10}	Y_9
NC	L_2	L_0										Y_{29}	Y_{27}	Y_{11}
L_3	NC	NC										Y_{15}	Y_{13}	Y_{12}
L_1	GND	X_{31}	X_{15}	X_{29}	X_{26}	X_8	X_{23}	X_5	X_3	X_1	NC	Y_{31}	Y_{14}	Y_{28}
CSL	NC	X_{14}	X_{13}	X_{27}	X_{10}	X_{25}	X_{22}	X_{20}	X_{19}	X_2	X_{16}	NC	NC	Y_{30}
GND	X_{30}	X_{28}	X_{12}	X_{11}	X_9	X_{24}	X_7	X_6	X_{21}	X_4	X_{18}	X_{17}	X_0	V_{SS}

144-PIN PGA
(PIN GRID ARRAY)
TOP VIEW

DSP72265-003

Integrated Device Technology, Inc.

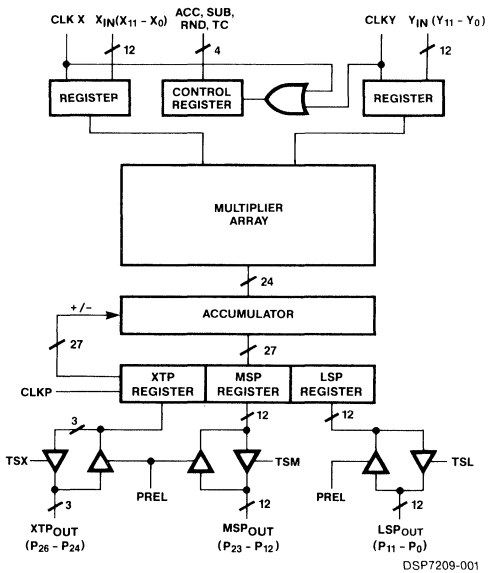
12 x 12 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7209L

FEATURES:

- 12 x 12 parallel multiplier/accumulator with selectable accumulation and subtraction
- High-speed — 30ns maximum multiply/accumulate time
- Selectable accumulation, subtraction, rounding and preloading with 27-bit result
- Pin and functionally compatible with the TRW TDC1009J
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- Low-power consumption (less than 150mW typical) — less than 1/10 the power of compatible bipolar
- Inputs and outputs directly TTL-compatible
- Single 5V supply
- Available in DIP, SHRINK-DIP, plastic DIP or LCC
- Military product available 100% screened to MIL-STD-883, Class B

FUNCTIONAL BLOCK DIAGRAM



IDT7209

DESCRIPTION:

The IDT7209 is a high-speed, low-power 12 x 12 parallel multiplier/accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using IDT's CEMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/10 the power dissipation and exceptional speed (30ns maximum) performance.

A pin and functional replacement for TRW's TDC1009J, the IDT7209 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7209 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flops, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the extended product (XTP) and most significant product (MSP), and a least significant product (LSP) output.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the two's complement input (TC) as either two's complement or an unsigned magnitude, yielding a full-precision 24-bit result that may be accumulated to a full 27-bit result. The three output registers—extended product (XTP), most significant product (MSP) and least significant product (LSP)—are controlled by the respective TSX, TSM and TSL input lines.

The accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the extended product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The ROUND (RND) control rounds up the most significant product (MSP) and the 3-bit extended product (XTP) outputs. When preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see PRELOAD truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

4

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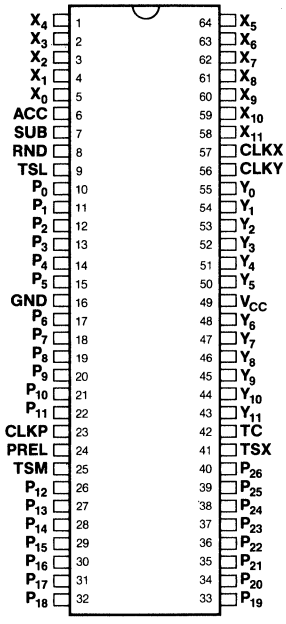
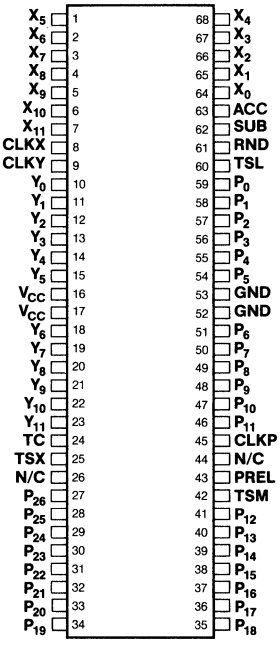
PIN CONFIGURATIONS



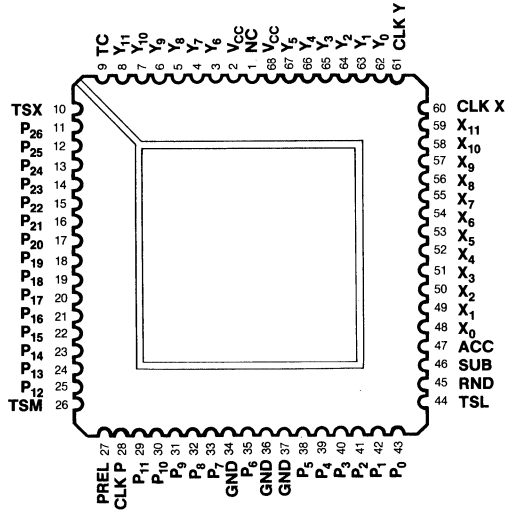
DSP7209-002

DIP
TOP VIEW



DSP7209-015

SHRINK-DIP
TOP VIEW



DSP7209-003

LCC
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.6	1.6	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 30,45,55,65ns or Military, 40,55,65,75ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$	—	4	20	—	4	25	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	6	—	—	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80 + 6(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 100 + 8(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 100,135ns or Military, 120,170ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	30	60	—	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$	—	0.1	1.0	—	0.1	2.0	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	5	—	—	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 60 + 5(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 80 + 7(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled and not 100% tested.

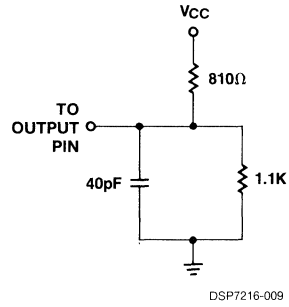


Figure 1. AC Output Test Load

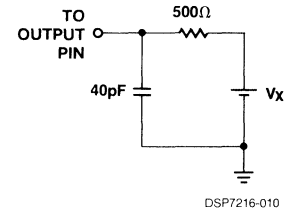


Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7209L-30 MIN.	IDT7209L-30 MAX.	IDT7209L-45 MIN.	IDT7209L-45 MAX.	IDT7209L-65 MIN.	IDT7209L-65 MAX.	IDT7209L-100 MIN.	IDT7209L-100 MAX.	IDT7209L-135 MIN.	IDT7209L-135 MAX.	UNITS	TEST LOAD FIG.
t_{MA}	Multiply-Accumulate Time	—	30	—	45	—	65	—	100	—	135	ns	1
t_D	Output Delay	—	25	—	25	—	35	—	35	—	40	ns	1
t_{ENA}	3-State Output Enable Delay(1)	—	25	—	25	—	30	—	35	—	40	ns	2
t_{DIS}	3-State Output Disable Delay(1)	—	25	—	25	—	30	—	35	—	40	ns	2
t_S	Input Register Setup Time	12	—	15	—	25	—	25	—	25	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	10	—	15	—	25	—	25	—	25	—	ns	—

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = 0°C to +125°C)

SYMBOL	PARAMETER	IDT7209L-40 MIN.	IDT7209L-40 MAX.	IDT7209L-55 MIN.	IDT7209L-55 MAX.	IDT7209L-75 MIN.	IDT7209L-75 MAX.	IDT7209L-120 MIN.	IDT7209L-120 MAX.	IDT7209L-170 MIN.	IDT7209L-170 MAX.	UNITS	TEST LOAD FIG.
t_{MA}	Multiply-Accumulate Time	—	40	—	55	—	75	—	120	—	170	ns	1
t_D	Output Delay	—	25	—	30	—	35	—	40	—	45	ns	1
t_{ENA}	3-State Output Enable Delay(1)	—	25	—	30	—	35	—	40	—	45	ns	2
t_{DIS}	3-State Output Disable Delay(1)	—	25	—	30	—	35	—	40	—	45	ns	2
t_S	Input Register Setup Time	15	—	20	—	25	—	30	—	30	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	15	—	20	—	30	—	30	—	30	—	ns	—

NOTE:

1. Transition is measured ±500mV from steady state with loading specified in Fig. 2.

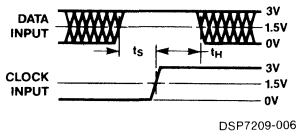


Figure 3. Set Up and Hold Time

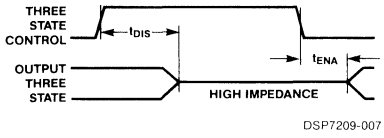


Figure 4. Three State Control Timing Diagram

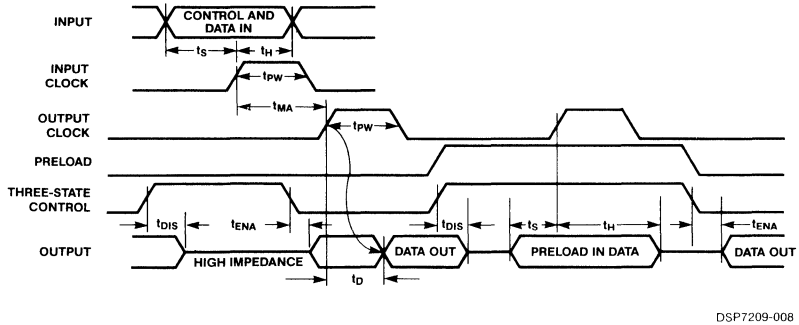


Figure 5. Timing Diagram

4

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11}-X_0)
Multiplicand Data Inputs

Y_{IN} (Y_{11}-Y_0)
Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY
Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)
When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)
When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

TC (Two's Complement)
When the TC Control is HIGH, it makes both the X and Y input, two's complement inputs. When the TC Control is LOW, it makes both inputs, X and Y, unsigned magnitude inputs.

RND (Round)
A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)
When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM TSL and TSX inputs must all be valid over the same period that the preload input is valid.

TSX, TSL, TSM (Three State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP

Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{26}-P_{24})

Extended Product Output (3-bits)

MSP (P_{23}-P_{12})

Most Significant Product

LSP (P_{11}-P_0)

Least Significant Product

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

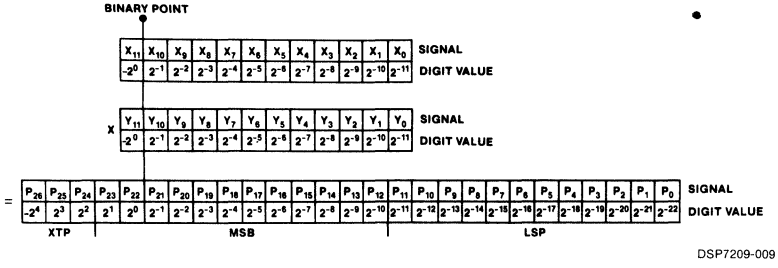
2. When in the non-accumulating mode, the first four bits (P_{26} through P_{23}) will all indicate the sign of the product. Additionally, the P_{22} term will also indicate the sign except for one exceptional case when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is valid operation that yields a +1 product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 27-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:
Hi Z = Output buffers at high impedance (output disabled).
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.



DSP7209-009

Figure 6. Fractional Two's Complement Notation

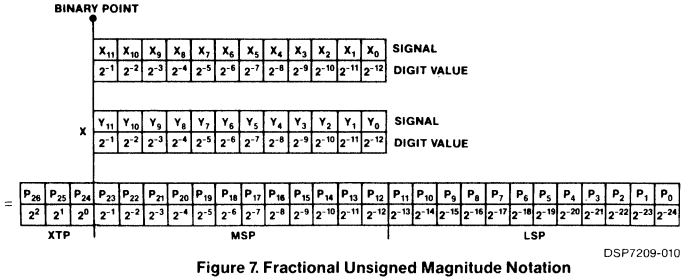


Figure 7. Fractional Unsigned Magnitude Notation

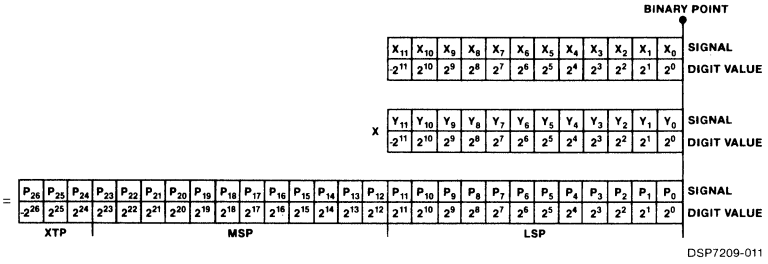


Figure 8. Integer Two's Complement Notation

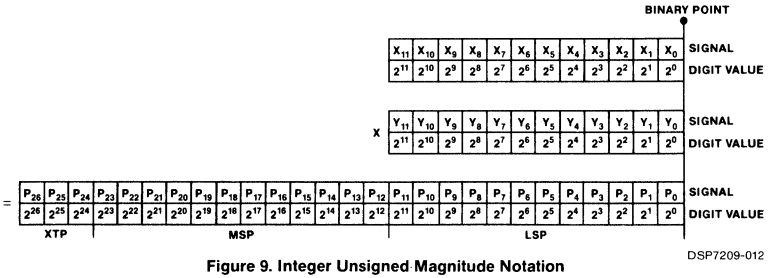


Figure 9. Integer Unsigned Magnitude Notation

4

16 x 16 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7210L
IDT7243L

Integrated Device Technology, Inc.

FEATURES:

- 16 x 16 parallel multiplier/accumulator with selectable accumulation and subtraction
- High-speed — 35ns multiply/accumulate time
- IDT7210 features selectable accumulation, subtraction and rounding and preloading with 35-bit result
- IDT7243 features selectable accumulation, subtraction and rounding with 19-bit result
- IDT7210 is pin and functionally compatible with the TRW TDC1010J
- IDT7243 is pin and functionally compatible with the TRW TDC1043
- Both devices perform subtraction and double precision addition and multiplication
- Produced using advanced CEMOS™ high-performance technology
- Low-power consumption (less than 250mW typical) — less than 1/10 the power of compatible bipolar and 1/7 the power of NMOS designs
- Input and output directly TTL-compatible
- Single 5V supply
- Available in topbraze DIP, SHRINK-DIP, plastic DIP, LCC, Fine-Pitch LCC, PLCC and Flatpack
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

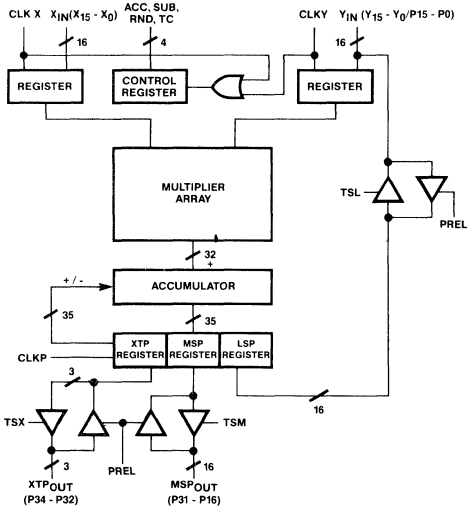
The IDT7210/IDT7243 are high-speed, low-power 16 x 16 parallel multiplier/accumulators that are ideally suited for real-time digital signal processing applications. Fabricated using CEMOS silicon gate technology, these devices offer a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (35ns maximum) performance.

Pin and functional replacements for TRW's TDC1010J/TDC-1043, the IDT7210/7243 operate from a single 5 volt supply and are compatible with standard TTL logic levels. The architecture of the IDT7210/7243 is farily straightforward, featuring individual input and output registers with clocked D-type flip-flops, a pre-load capability (IDT7210 only) which enables input data to be preloaded into the output registers, individual three-state output ports for the extended product (XTP) and most significant product (MSP), and a least significant product output (LSP) which is multiplexed with the Y input. Unlike the IDT7210, the IDT7243 does not have either a preload capability or a least significant product (LSP) output accessible externally.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the two's complement input (TC) as either two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The

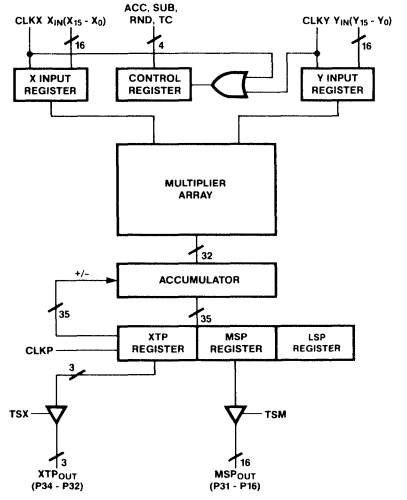
Continued on Page 2

FUNCTIONAL BLOCK DIAGRAMS



DSP7210-001

IDT7210



DSP7210-002

IDT7243

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Printed in U.S.A.

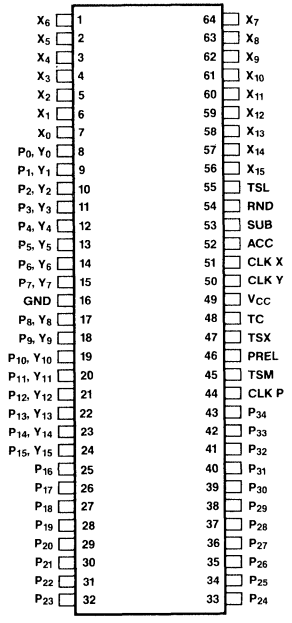
DESCRIPTION (CONT'D)

three output registers—extended product (XTP), most significant product (MSP) and least significant product (LSP)—are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through Y_{IN} ports in the IDT7210.

The accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from subsequent results. When the subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the extended product output (XTP) is sign extended in the two's complement mode, or set to zero in the unsigned mode. The ROUND (RND) control rounds up the most significant product (MSP) and the 3-bit extended product (XTP) outputs. When pre-load input (PREL) is active, all the output buffers are forced into a high-impedance state (see PRELOAD truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

PIN CONFIGURATIONS

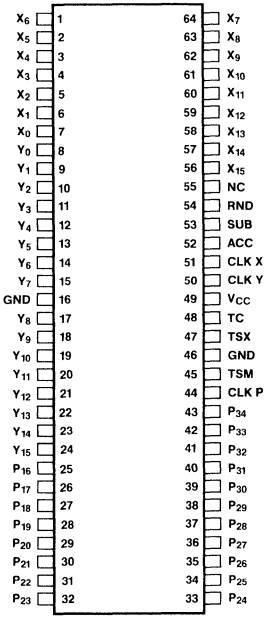
IDT7210



DSP7210-003

DIP
TOP VIEW

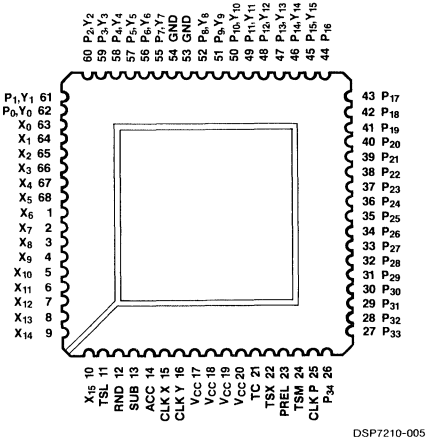
IDT7243



DSP7210-004

DIP
TOP VIEW

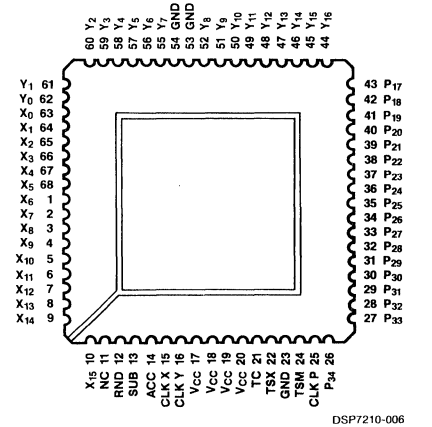
IDT7210



DSP7210-005

LCC, PLCC & FINE-PITCH LCC
TOP VIEW

IDT7243



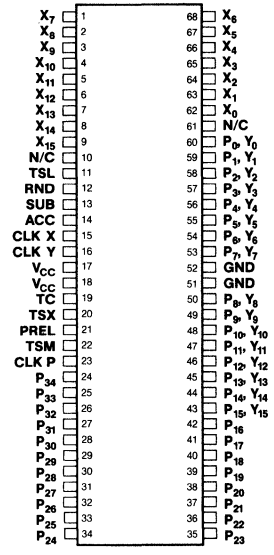
DSP7210-006

LCC, PLCC & FINE-PITCH LCC
TOP VIEW

4

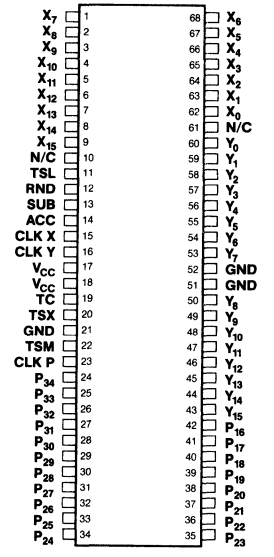
PIN CONFIGURATIONS (Cont'd)

IDT7210



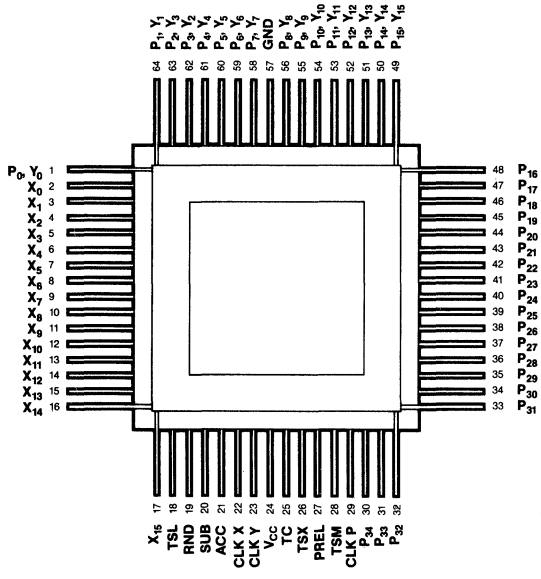
SHRINK-DIP
TOP VIEW

IDT7243



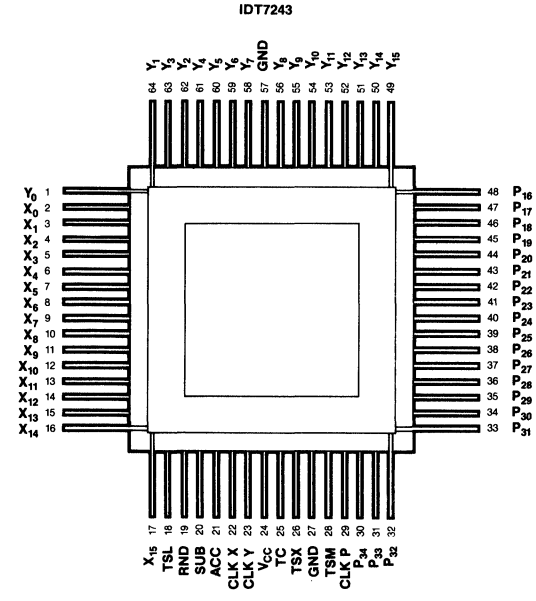
SHRINK-DIP
TOP VIEW

IDT7210



FLATPACK
TOP VIEW

IDT7243



FLATPACK
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.6	1.6	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C for Commercial clocked multiply times of 35,45,55,65ns or Military 40,55,65,75ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	45	90	—	45	110	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$	—	4	20	—	4	25	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	6	—	—	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 90 + 8(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 110 + 8(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 10V ± 10%, T_A = 0°C to +70°C, Military V_{CC} = 10V ± 10%, T_A = -55°C to +125°C for Commercial clocked multiply times of 100,165ns or Military 120/200ns.

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	35	70	—	35	90	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$	—	0.1	1.0	—	0.1	2.0	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	5	—	—	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 70 + 5(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 90 + 7(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

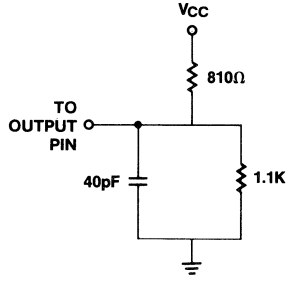
AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	7210L35 7243L35 MIN.	MAX.	7210L45 7243L45 MIN.	MAX.	7210L55 7243L55 MIN.	MAX.	7210L65 7243L65 MIN.	MAX.	7210L75 7243L75 MIN.	MAX.	7210L100 7243L100 MIN.	MAX.	7210L165 7243L165 MIN.	MAX.	UNITS	TEST LOAD FIG.
t_{MA}	Multiply - Accumulate Time	—	35	—	45	—	55	—	65	—	75	—	100	—	165	ns	1
t_D	Output Delay	—	25	—	25	—	30	—	35	—	35	—	35	—	40	ns	1
t_{ENA}	Three-State Output Enable Delay[1]	—	25	—	25	—	30	—	30	—	35	—	35	—	40	ns	2
t_{DIS}	Three-State Output Disable Delay[1]	—	25	—	25	—	30	—	30	—	35	—	35	—	40	ns	2
t_S	Input Register Setup Time	12	—	15	—	20	—	25	—	25	—	25	—	30	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	3	—	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	10	—	15	—	20	—	25	—	25	—	25	—	25	—	ns	—

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

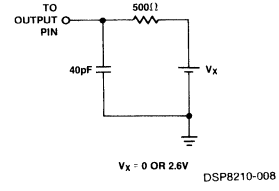
SYMBOL	PARAMETER	7210L40 7243L40 MIN.	MAX.	7210L55 7243L55 MIN.	MAX.	7210L65 7243L65 MIN.	MAX.	7210L75 7243L75 MIN.	MAX.	7210L85 7243L85 MIN.	MAX.	7210L120 7243L120 MIN.	MAX.	7210L200 7243L200 MIN.	MAX.	UNITS	TEST LOAD FIG.
t_{MA}	Multiply - Accumulate Time	—	40	—	55	—	65	—	75	—	85	—	120	—	200	ns	1
t_D	Output Delay	—	25	—	30	—	35	—	35	—	35	—	40	—	45	ns	1
t_{ENA}	Three-State Output Enable Delay[1]	—	25	—	30	—	30	—	35	—	35	—	40	—	45	ns	2
t_{DIS}	Three-State Output Disable Delay[1]	—	25	—	30	—	30	—	30	—	35	—	40	—	45	ns	2
t_S	Input Register Setup Time	15	—	20	—	25	—	25	—	25	—	30	—	30	—	ns	—
t_H	Input Register Hold Time	3	—	3	—	3	—	3	—	3	—	0	—	0	—	ns	—
t_{PW}	Clock Pulse Width	15	—	20	—	25	—	25	—	30	—	30	—	30	—	ns	—

NOTE:
1. Transition is measured ±500mV from steady state with loading specified in Fig. 2.



DSP7216-009

Figure 1. AC Output Test Load



DSP8210-008

Figure 2. Output Three State Delay Load

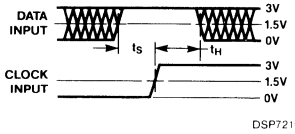


Figure 3. Set Up and Hold Time

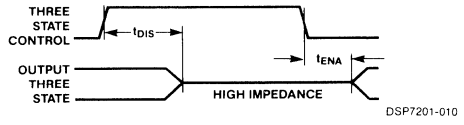


Figure 4. Three State Control Timing Diagram

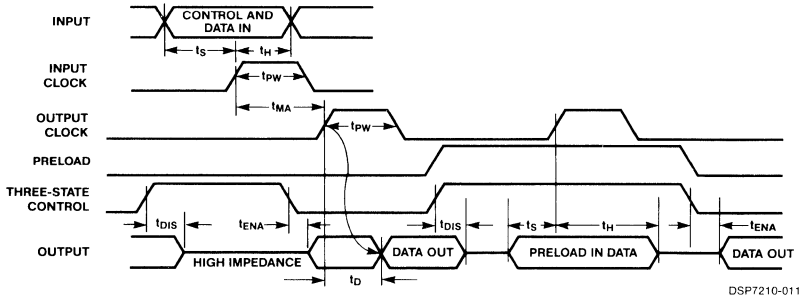


Figure 5. Timing Diagram

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{15}-X_0)
Multiplicand Data Inputs

Y_{IN} (Y_{15}-Y_0)
Multiplier Data Inputs

INPUT CLOCKS:

CLKX, CLKY
Input data is loaded on the rising edge of these clocks.

CONTROLS:

ACC (Accumulate)
When ACC is high, the contents of the XTP, MSP and LSP registers are added to or subtracted from the multiplier output. When ACC is low, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)
When the ACC and SUB signals are both high, the contents of the output register are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is high and SUB is low, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is low, SUB acts as a "don't care" input.

TC (Two's Complement)
When the TC Control is HIGH, it makes both the X and Y inputs, two's complement inputs. When the TC control is LOW, it makes both inputs, X and Y, unsigned magnitude inputs.

RND (Round)
A high level at this input adds a "1" to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload) (IDT7210 only)
When the PREL input is high, the output is driven to a high impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM, TSL and TSX inputs must all be valid over the same period that the preload input is valid.

Y_{IN}/LSP Output — (LSP output, IDT7210 only)
Shares functions between 16-bit data input (Y_{IN}) and the least significant product output (LSP).

TSX, TSL, TSM (Three State Output Controls)
The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are high and are enabled when TSX, TSM and TSL are low.

OUTPUT CLOCK:

CLKP
Output data is loaded into the output register on the rising edge of this clock.

OUTPUTS:

XTP (P_{34}-P_{32})
Extended Product Output (3-bits)

MSP (P_{31}-P_{16})
Most Significant Product

LSP (P_{15}-P_0)
Least Significant Product (IDT7210 only), shared with Y_{IN} input.

4

NOTES ON TWO'S COMPLEMENT FORMATS:

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the 2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.
2. When in the non-accumulating mode, the first four bits (P34 to P31) will all indicate the sign of the product. Additionally, the P30 term will also indicate the sign except for one exceptional case when multiplying -1×-1. With the additional bits that are available in this multiplier, the -1×-1 is a valid operation that yields a +1 product.
3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

PRELOAD TRUTH TABLE (IDT7210 only)

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES:
Hi Z = Output buffers at high impedance (output disabled).
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

Figure 6. Fractional Two's Complement Notation

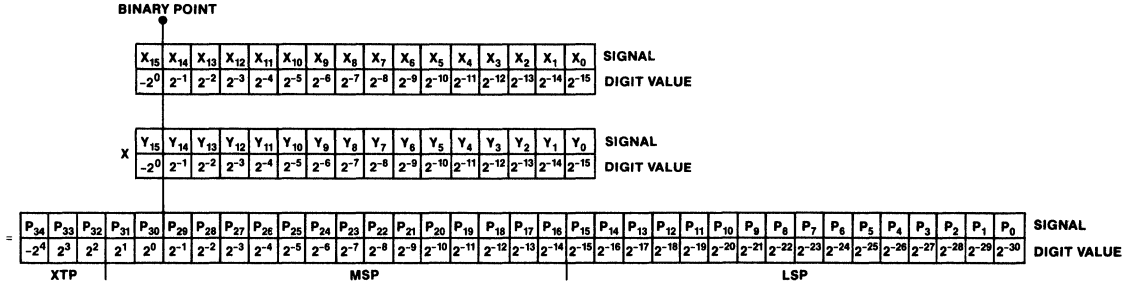


Figure 7. Fractional Unsigned Magnitude Notation

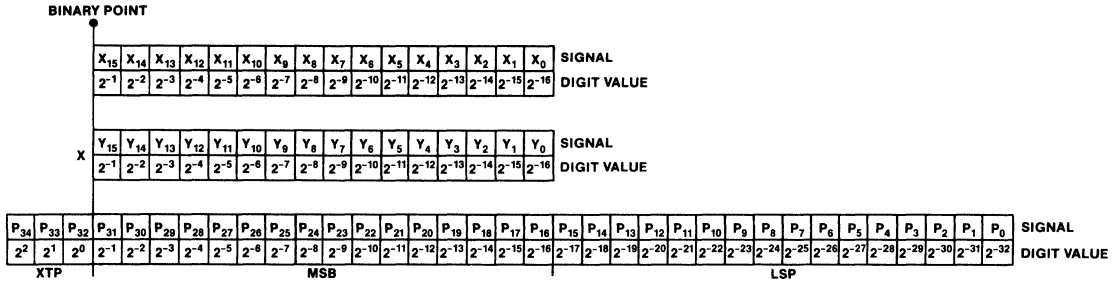


Figure 8. Integer Two's Complement Notation

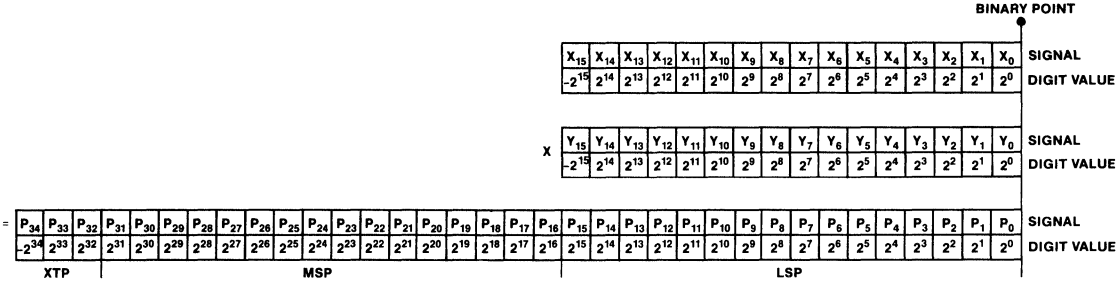
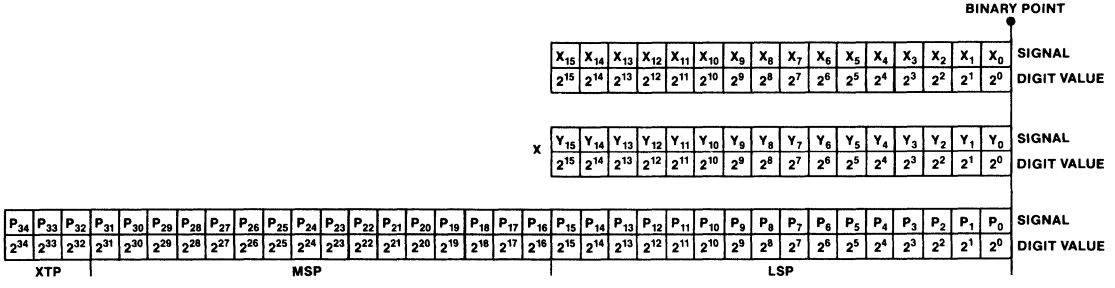


Figure 9. Integer Unsigned Magnitude Notation



Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

ADVANCE INFORMATION
IDT72103
IDT72104

FEATURES:

- 20MHz parallel port access time
- 40MHz serial input/output port clock cycle
- Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial and Parallel-to-Parallel operations
- Easily expandable in depth and width
- Programmable wordlengths from 3-bits to any bit width using Flexishift™ without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Full-Minus-One, Empty, Almost-Empty (1/8 from empty), Empty-Plus-One, and Half-Full
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture with 50ns access time
- Output enable control provided for parallel port
- Retransmit capability in single device mode
- High-performance CEMOS™ technology
- Available in DIP, LCC, and J-Leaded PLCC
- Military product available 100% screened to MIL-STD-883, Class B

APPLICATIONS:

- High-Speed Data Acquisition Systems
- Local Area Network Buffers
- Remote Telemetry Buffers
- Serial Link Buffers
- High-Speed Parallel Bus-to-Bus Serial Communications
- Magnetic Media Controllers
- Single Chip Video Frame Buffers
- FAX/Printer Buffers

DESCRIPTION:

The IDT72103/IDT72104 are high-speed Parallel Serial FIFOs that are ideally suited for serial communications, high-density media storage and local area networks.

The devices have four ports: Two of these are 9-bit parallel ports and the other two are for serial input and serial output. A variety of operations can be performed: Serial-to-Parallel, Parallel-to-Serial, Serial-to-Serial, and Parallel-to-Parallel. The Parallel-Serial FIFOs can expand in depth or width for any of these modes.

A unique feature that enhances the bandwidth is the handling of serial wordlengths that are not a multiple of 9. The IDT72103/IDT72104 can be configured to handle serial wordlengths of 3 to 9 bits, up to words of any length, using multiple devices. This feature is provided without using any additional ICs. For example, a user can configure a 4K x 24 FIFO by using three devices to generate internal increments to the read/write pointers every 24 cycles rather than every 27 cycles, thereby maintaining a high bandwidth.

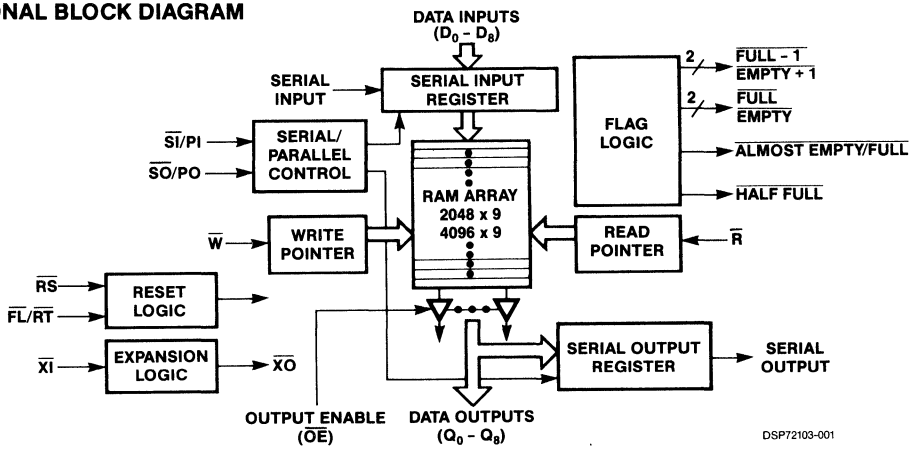
A number of flags are provided to monitor the status of the FIFO. These include Full, Almost-Full (when the FIFO is more than 7/8 full), Full-Minus-One (when the FIFO has one or zero locations left), Empty, Almost-Empty (when the FIFO is less than 1/8 full), Empty-Plus-One (when there is only one or zero samples left in the FIFO), and a Half-Full Flag.

Read and Write controls are provided to permit asynchronous and simultaneous operations. An Output Enable control is provided on the parallel port, and this is an additional control to the Read input that also controls the parallel port.

Expansion controls $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

The IDT72103/IDT72104 are manufactured in advanced CEMOS technology and fully conform to the requirements of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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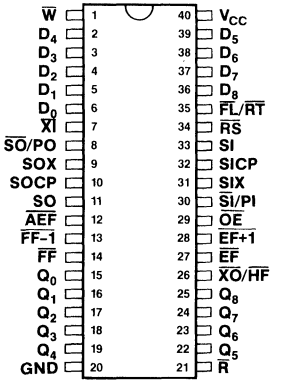
PIN CONFIGURATION



DSP72103-002

DIP
TOP VIEW

4

Integrated Device Technology, Inc.

12 x 12 BIT PARALLEL CMOS MULTIPLIER

IDT7212L
IDT7213L

FEATURES:

- 12 x 12 parallel multiplier with double precision product
- High-speed — 30ns maximum clock to multiply time
- Low-power consumption — 150mW typical, less than 1/10th the power of compatible bipolar parts
- Produced with advanced CEMOS™ high-performance technology
- IDT7212L is pin and functionally compatible with TRW MPY012H
- IDT7213L requires only a single clock with register enables
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in DIP, SHRINK-DIP, plastic DIP, LCC or Flatpack
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7212/IDT7213 are high-speed, low power 12 x 12 multipliers ideal for fast, real-time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high-reliability technology, CEMOS, has achieved speeds (30ns max.) exceeding bipolar at 1/10th the power consumption.

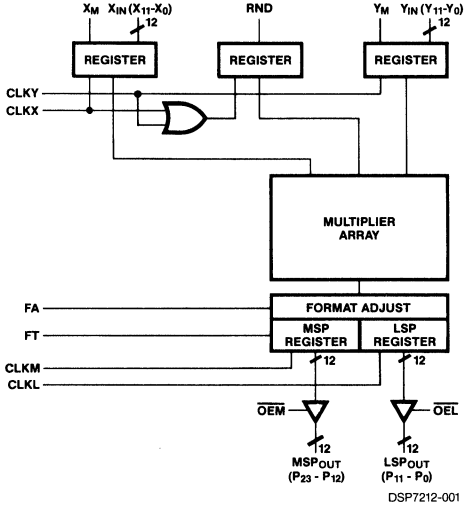
The IDT7212/IDT7213 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. With the IDT7212, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7213 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

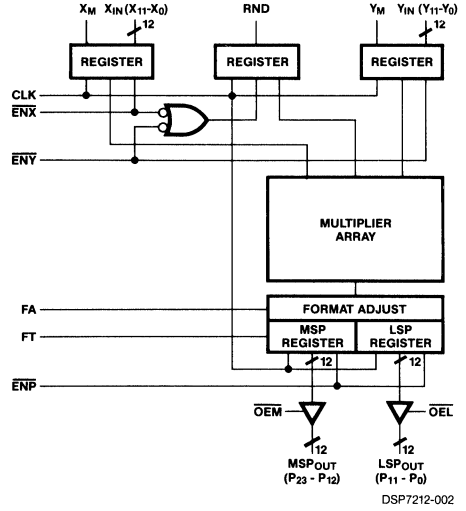
The IDT7212/IDT7213 offer additional flexibility with the FA control. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP.

The IDT7212/IDT7213 Multipliers are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS



IDT7212



IDT7213

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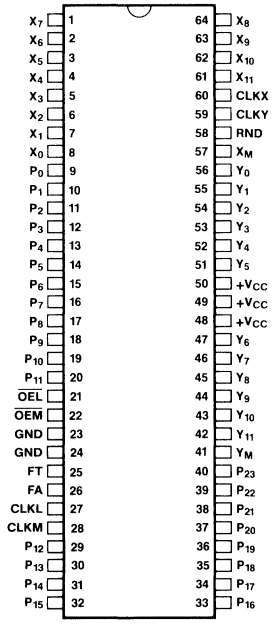
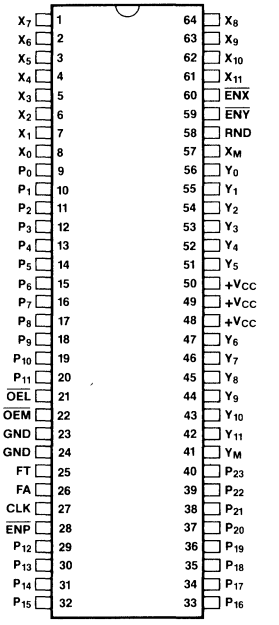
PIN CONFIGURATIONS

IDT7212
64-PIN DIP



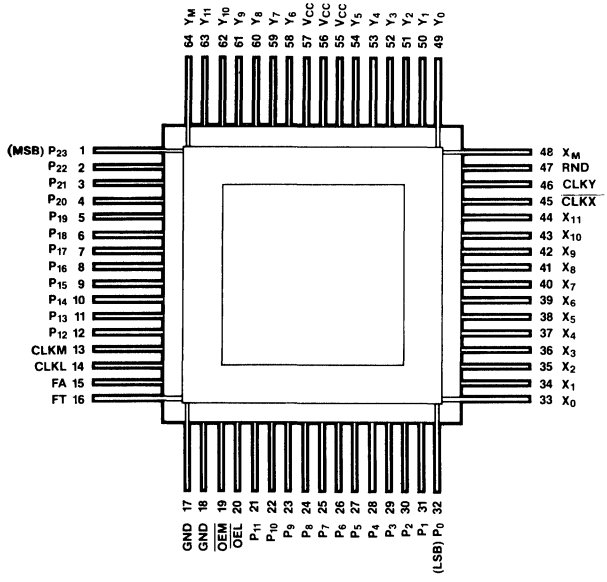
TOP VIEW DSP7212-003

IDT7213
64-PIN DIP



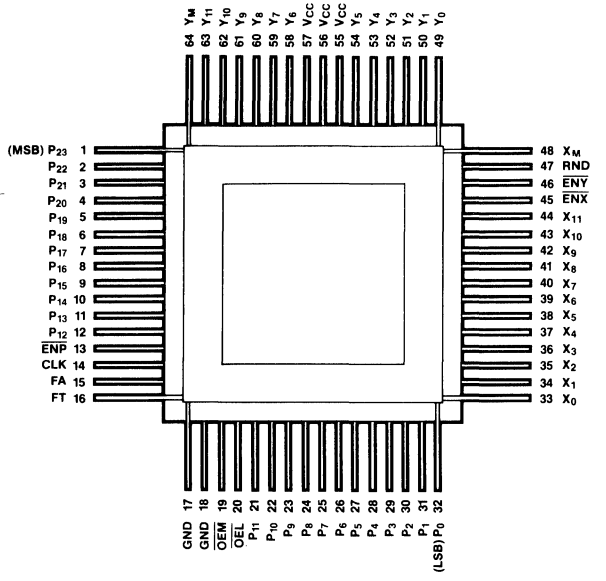
TOP VIEW DSP7212-004

IDT7212
64-LEAD FLATPACK



TOP VIEW DSP7212-005

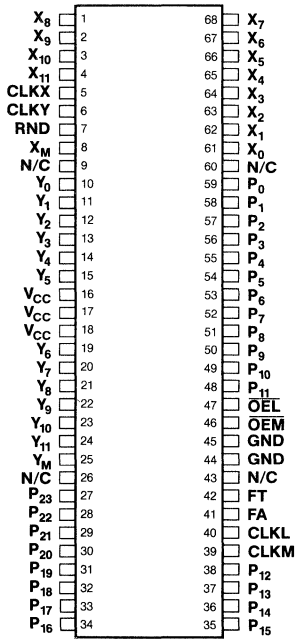
IDT7213
64-LEAD FLATPACK



TOP VIEW DSP7212-007

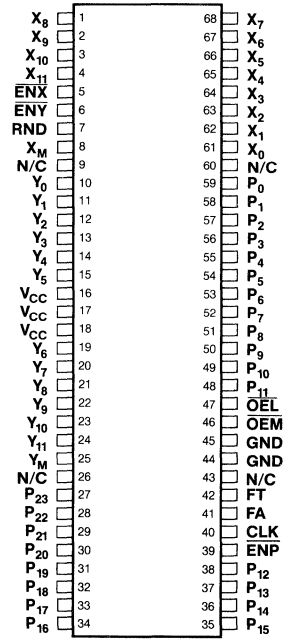
4

IDT7212
68-PIN SHRINK-DIP



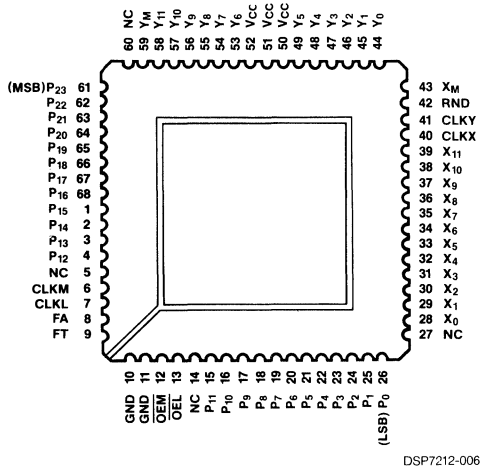
TOP VIEW

IDT7213
68-PIN SHRINK-DIP



TOP VIEW

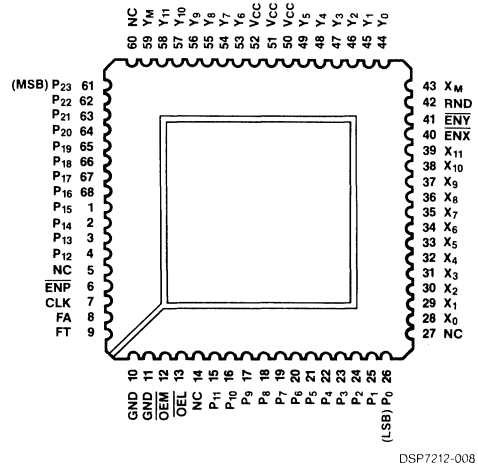
IDT7212
68-PIN LCC



DSP7212-006

TOP VIEW

IDT7213
68-PIN LCC



DSP7212-008

TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.4	1.4	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C , Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 30,45,70ns or Military, 40,55,90ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	30	65	—	30	85	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	50	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	—	4	25	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	6	—	—	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 65 + 6(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 85 + 8(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to +70°C , Military V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)
for Commercial clocked multiply times of 115ns or Military, 140ns

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	25	55	—	25	75	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq$ 0.2V	—	0.1	1.0	—	0.1	2.0	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	5	—	—	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 55 + 5(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 75 + 7(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7212L30 IDT7213L30 MIN.	MAX.	IDT7212L45 IDT7213L45 MIN.	MAX.	IDT7212L70 IDT7213L70 MIN.	MAX.	IDT7212L115 IDT7213L115 MIN.	MAX.	UNITS	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	50	—	65	—	105	—	155	ns	1
t_{MC}	Clocked Multiply Time	—	30	—	45	—	70	—	115	ns	1
t_S	X, Y, RND Set-Up Time	15	—	20	—	20	—	25	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	2	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	15	—	20	—	20	—	25	—	ns	1
t_{PWL}	Clock Pulse Width Low	15	—	20	—	20	—	25	—	ns	1
t_{PDP}	Output Clock to P	—	25	—	25	—	30	—	40	ns	1
t_{ENA}	3 State Enable Time(2)	—	25	—	30	—	35	—	40	ns	2
t_{DIS}	3 State Disable Time(2)	—	25	—	25	—	30	—	35	ns	2
t_S	Clock Enable Setput Time (IDT7213 only)	15	—	20	—	25	—	25	—	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	—	3	—	3	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	—	0	—	0	—	0	—	ns	1

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7212L40 IDT7213L40 MIN.	MAX.	IDT7212L55 IDT7213L55 MIN.	MAX.	IDT7212L90 IDT7213L90 MIN.	MAX.	IDT7212L140 IDT7213L140 MIN.	MAX.	UNITS	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	60	—	75	—	130	—	185	ns	1
t_{MC}	Clocked Multiply Time	—	40	—	55	—	90	—	140	ns	1
t_S	X, Y, RND Set-Up Time	20	—	20	—	25	—	30	—	ns	1
t_H	X, Y, RND Hold Time	3	—	3	—	2	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	20	—	25	—	30	—	30	—	ns	1
t_{PWL}	Clock Pulse Width Low	20	—	25	—	30	—	30	—	ns	1
t_{PDP}	Output Clock to P	—	25	—	30	—	35	—	45	ns	1
t_{ENA}	3 State Enable Time(2)	—	25	—	30	—	40	—	45	ns	2
t_{DIS}	3 State Disable Time(2)	—	25	—	25	—	40	—	45	ns	2
t_S	Clock Enable Setput Time (IDT7213 only)	20	—	25	—	30	—	30	—	ns	1
t_H	Clock Enable Hold Time (IDT7213 only)	3	—	3	—	2	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML(1) (IDT7212 only)	0	—	0	—	0	—	0	—	ns	1

NOTES:

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is sampled and not 100% tested.

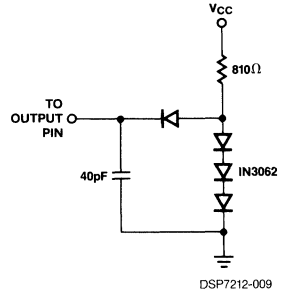


Figure 1. AC Output Test Load

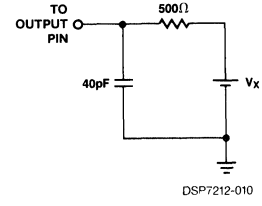
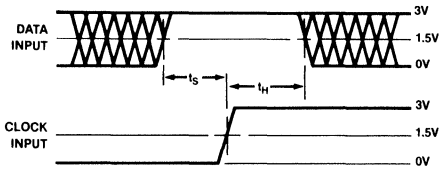


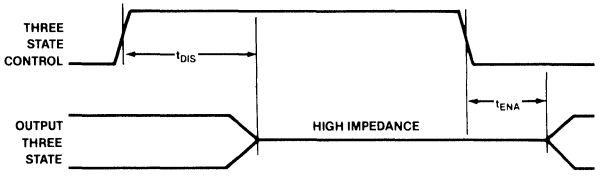
Figure 2. Output Three State Delay Load (V_X = 0V or 2.6V)



NOTE:
Diagram shown for HIGH data only. Output transition may be opposite sense.

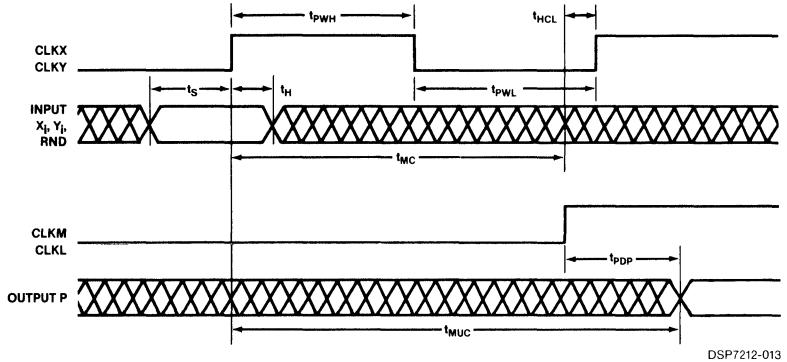
DSP7212-011

Figure 3. Set-Up And Hold Time



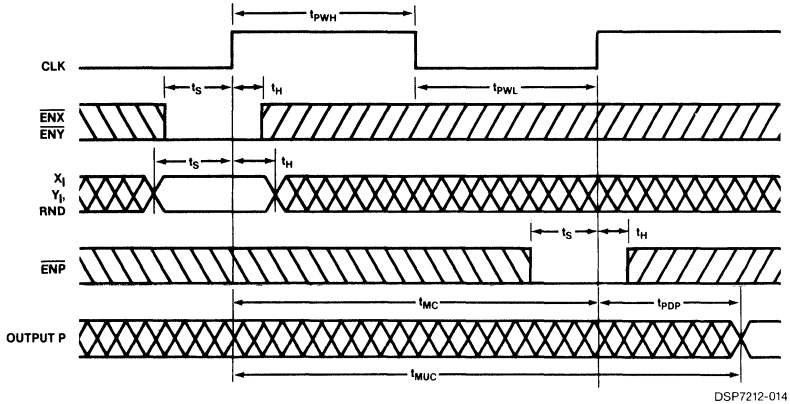
DSP7212-012

Figure 4. Three-State Control Timing Diagram



DSP7212-013

Figure 5. IDT7212 Timing Diagram



DSP7212-014

Figure 6. IDT7213 Timing Diagram

4

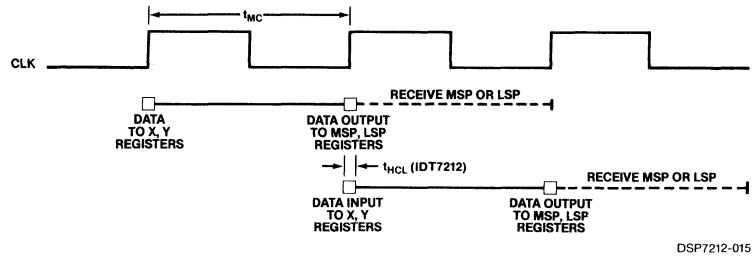


Figure 7. Simplified Timing Diagram-Typical Application

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{11} through X_0)
Twelve Multiplicand Data Inputs

Y_{IN} (Y_{11} through Y_0)
Twelve Multiplier Data Inputs

INPUT CLOCKS (IDT7212 ONLY):

CLKX
The rising edge of this clock loads the X_{11} - X_0 data input register along with the two's complement and round registers.

CLKY
The rising edge of this clock loads the Y_{11} - Y_0 data input register along with the two's complement and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7213 ONLY):

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{11} - X_0 data input register along with the two's complement and round registers.

$\overline{ENY}$
Register enable for the Y_{11} - Y_0 data input register along with the two's complement and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS:

X_M, Y_M (TCX, TCY)[1]
Mode control inputs for each data word. A low input designates unsigned data input with a high input used for two's complement.

NOTE:
1. TRW MPY012H/K pin designation

FA (RS)[1]
When the format adjust control is HIGH, a full 24-bit product is selected. When this control is LOW, a left-shifted 23-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications. (See Multiplier Input/Output Formats.)

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are bypassed.

$\overline{OEL}$
Three-state enable for LSP output.

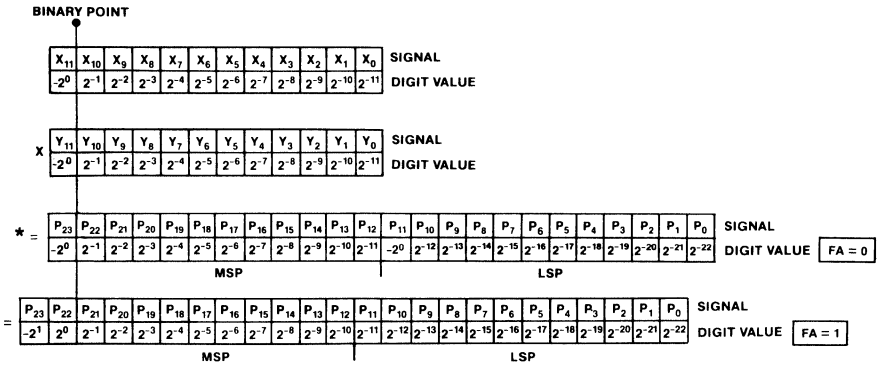
$\overline{OEP}$
Three-state enable for MSP output.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the Format Adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the P_{10}. If FA is HIGH when RND is HIGH, a one will be added to the P_{11}. In either case, the LSP output will reflect this addition when RND is HIGH. Note also the rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

OUTPUTS:

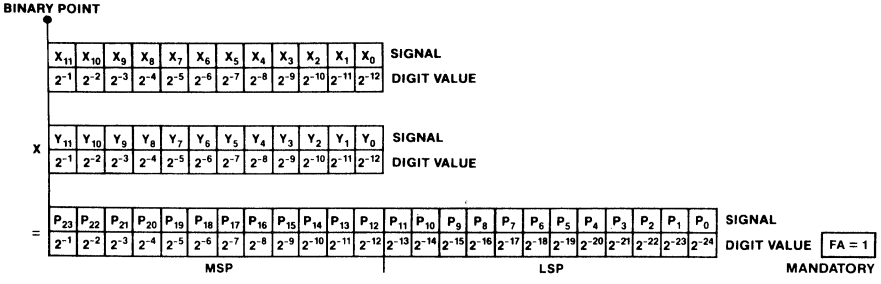
MSP (P_{23} through P_{12})
Most Significant Product Output

LSP (P_{11} through P_0)
Least Significant Product Output



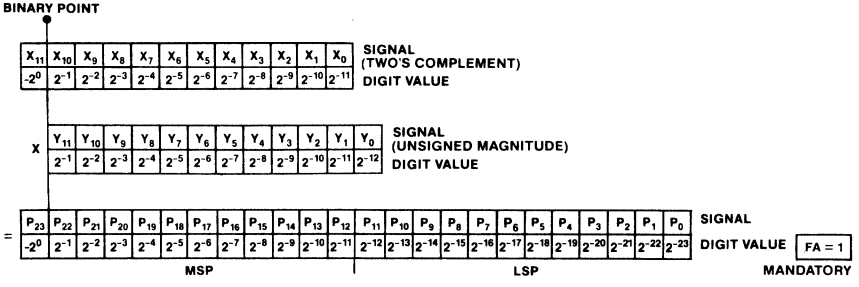
DSP7212-016

Figure 8. Fractional Two's Complement Notation



DSP7212-017

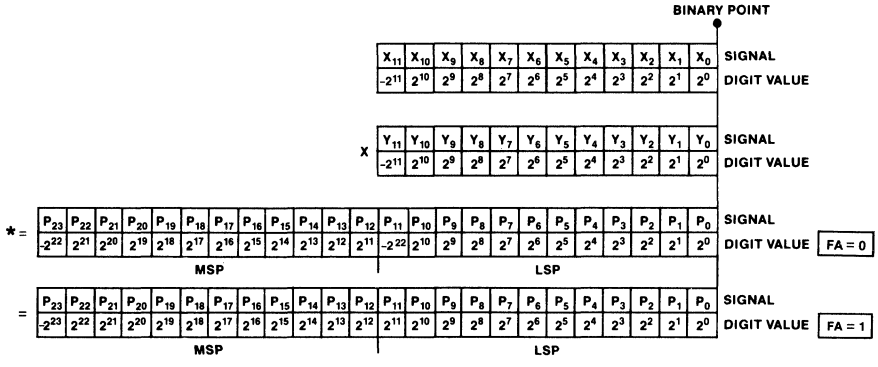
Figure 9. Fractional Unsigned Magnitude Notation



DSP7212-018

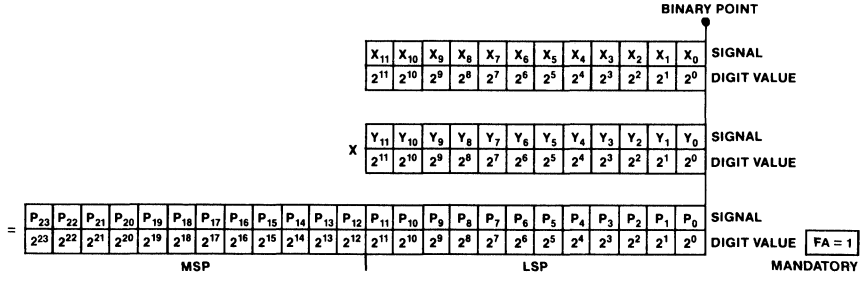
Figure 10. Fractional Mixed Mode Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 10000 . . . 0 with 1000 . . . 00 yielding an erroneous product of -1 in the fraction case and -2^{22} in the integer case.



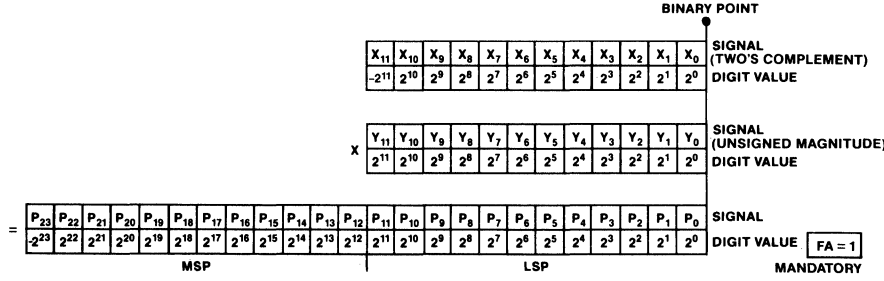
DSP7212-019

Figure 11. Integer Two's Complement Notation



DSP7212-020

Figure 12. Integer Unsigned Magnitude Notation



DSP7212-021

Figure 13. Integer Mixed Mode Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 10000 . . . 0 with 1000 . . . 00 yielding an erroneous product of -1 in the fraction case and -2^{22} in the integer case.

Integrated Device Technology, Inc.

16x16 BIT PARALLEL CMOS MULTIPLIER

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- High-speed 35ns clocked multiply time
- Low-power consumption — 200mW typical, less than 1/10th the power of compatible bipolar parts
- Produced with advanced CEMOS™ high-performance technology
- IDT7216L is pin and functionally compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires only single clock with register enables making it pin and functionally compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL compatible
- Three-state output
- Available in SHRINK-DIP, Plastic DIP, LCC, Flatpack, Fine-Pitch LCC, Pin Grid Array and Plastic LCC
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16 x 16 multipliers, ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high-reliability technology, CEMOS, has achieved speeds comparable to bipolar, (35ns max.) at 1/10th the power consumption.

The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

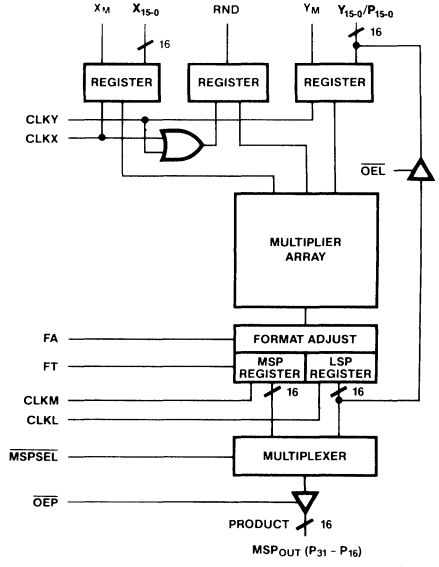
All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The $\overline{MSPSEL}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 Multipliers are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

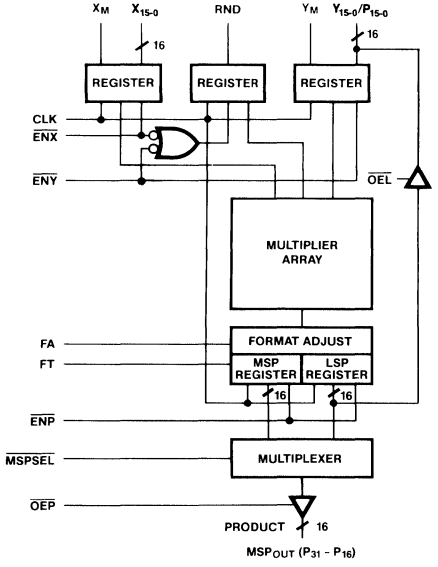
4

FUNCTIONAL BLOCK DIAGRAMS



IDT7216

DSP7216-001



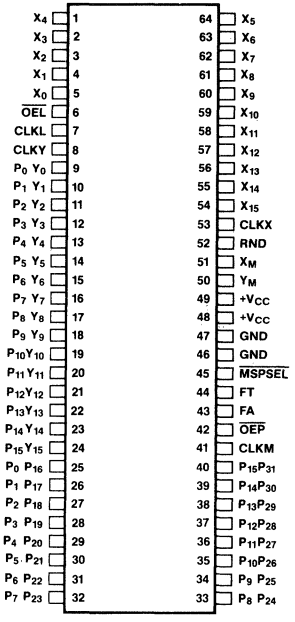
IDT7217

DSP7216-002

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

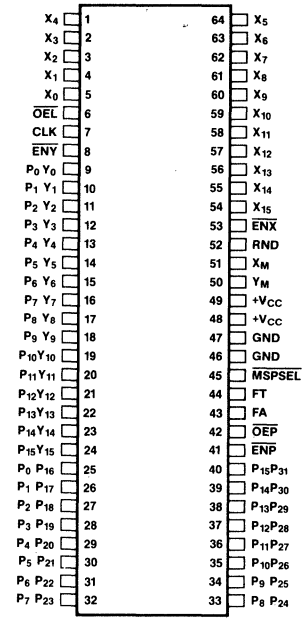
IDT7216
64-PIN DIP



DSP7216-003

TOP VIEW

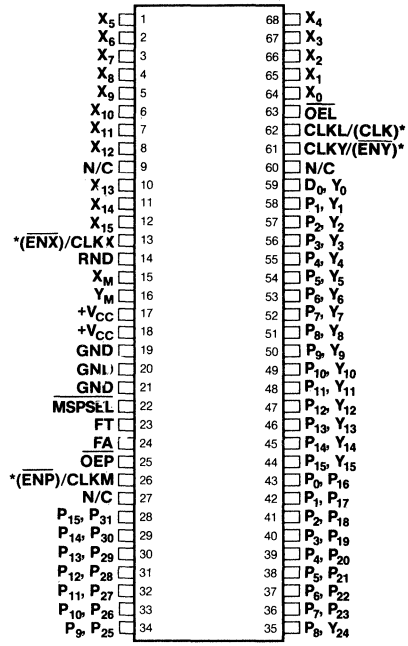
IDT7217
64-PIN DIP



DSP7216-004

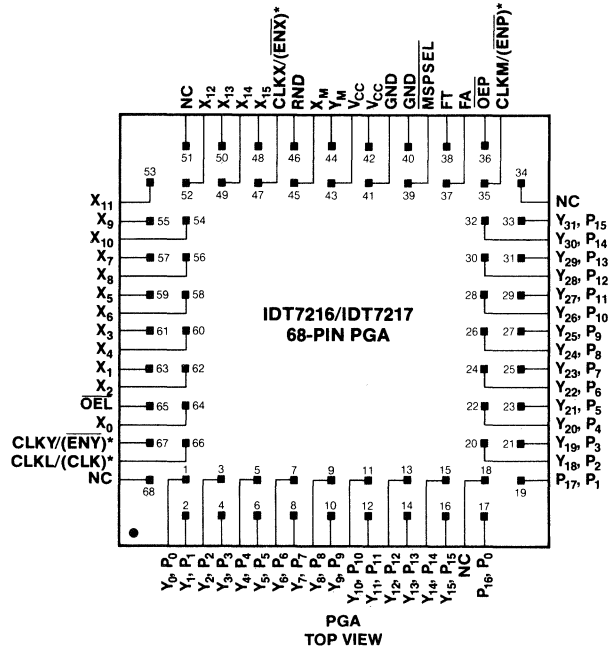
TOP VIEW

IDT7216/IDT7217
68-PIN SHRINKDIP



DSP7216-026

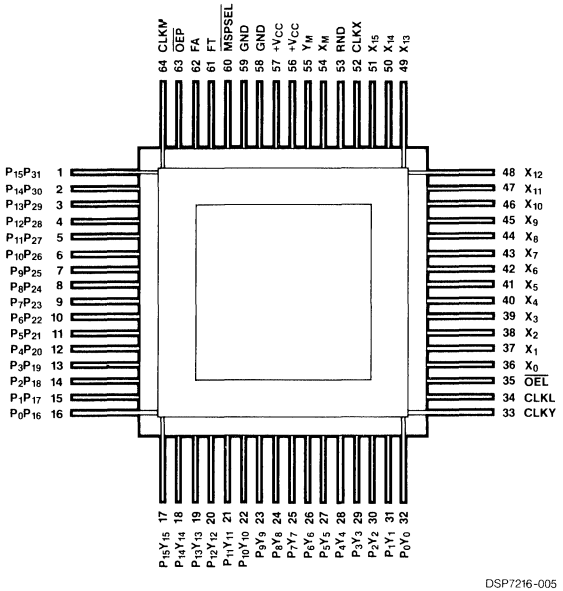
TOP VIEW



PGA
TOP VIEW

*PIN DESIGNATION IN PARENTHESES INDICATES IDT7217 PIN NAME

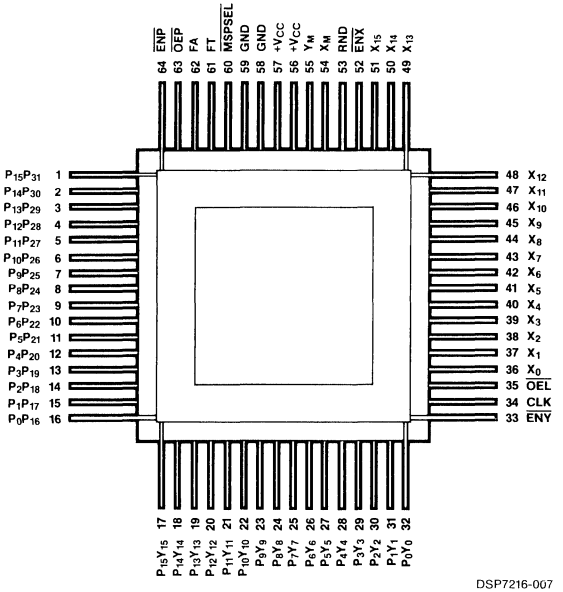
IDT7216
64-LEAD FLATPACK



DSP7216-005

TOP VIEW

IDT7217
64-LEAD FLATPACK

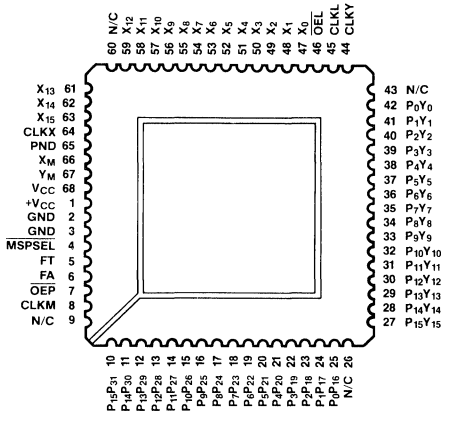


DSP7216-007

TOP VIEW

4

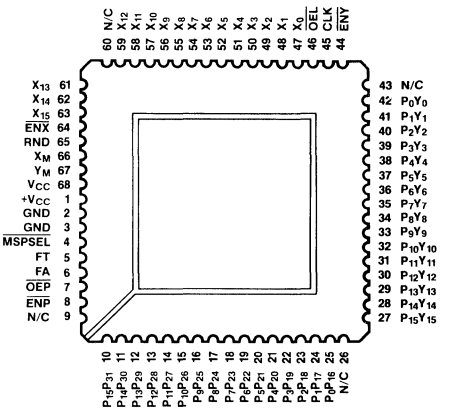
IDT7216
LCC, PLCC
FINE-PITCH LCC



DSP7216-006

TOP VIEW

IDT7217
LCC, PLCC
FINE-PITCH LCC



DSP7216-008

TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.2	1.2	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to 125°C)
for Commercial clocked multiply times of 35,45,55,65ns or Military, 40,55,65,75ns.

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	10	—	—	20	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$	—	4	20	—	4	25	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	6	—	—	8	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80 + 6(f - 10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 100 + 8(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

DC ELECTRICAL CHARACTERISTICS

(Commercial V_{CC} = 5V ± 10%, T_A = 0°C to 70°C, Military V_{CC} = 5V ± 10%, T_A = -55°C to 125°C)
for Commercial clocked multiply times of 75,95,140ns or Military, 90,120,185ns.

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL MIN.	COMMERCIAL TYP.(1)	COMMERCIAL MAX.	MILITARY MIN.	MILITARY TYP.(1)	MILITARY MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	Hi Z, V_{CC} = Max., V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	µA
I_{CC}(2)	Operating Power Supply Current	Outputs Open Measured at 10MHz(2)	—	30	60	—	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ - 0.2V, $V_{IN} \leq 0.2V$	—	0.1	1.0	—	0.1	2.0	mA
I_{CC}/f(2,3)	Increase in Power Supply Current/MHz	V_{CC} = Max., f > 10MHz	—	—	5	—	—	7	mA/MHz
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = TTL voltages. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 60 + 5(f - 10) mA, where f = operating frequency in MHz. For the military range, I_{CC} = 80 + 7(f - 10) where f = operating frequency in MHz.
3. For frequencies greater than 10MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

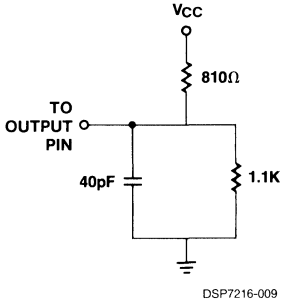


Figure 1. AC Output Test Load

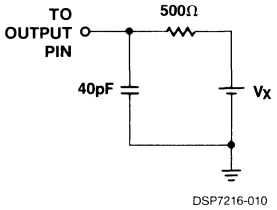
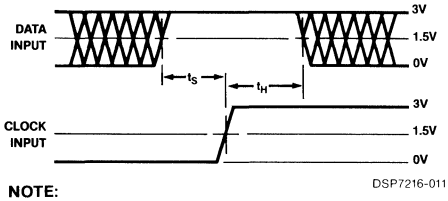


Figure 2. Output Three State Delay Load (V_x = 0V or 2.6V)



NOTE:
Diagram shown for HIGH data only. Output transition may be opposite sense.

Figure 3. Set-Up And Hold Time

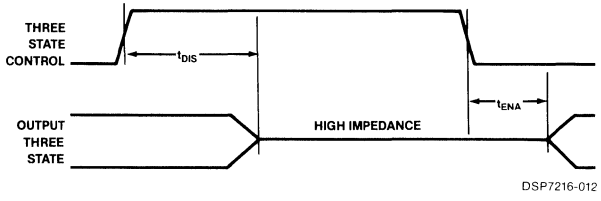


Figure 4. Three-State Control Timing Diagram

AC ELECTRICAL CHARACTERISTICS MILITARY[3] (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7216L-40 IDT7217L-40 MIN.	MAX.	IDT7216L-55 IDT7217L-55 MIN.	MAX.	IDT7216L-65 IDT7217L-65 MIN.	MAX.	IDT7216L-75 IDT7217L-75 MIN.	MAX.	IDT7216L-90 IDT7217L-90 MIN.	MAX.	IDT7216L-120 IDT7217L-120 MIN.	MAX.	IDT7216L-185 IDT7217L-185 MIN.	MAX.	UNITS
t_{MUC}	Unclocked Multiply Time	—	60	—	75	—	85	—	95	—	125	—	160	—	230	ns
t_{MC}	Clocked Multiply Time	—	40	—	55	—	65	—	75	—	90	—	120	—	185	ns
t_S	X, Y, RND Setup Time	15	—	20	—	25	—	25	—	30	—	30	—	30	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	3	—	2	—	0	—	0	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	15	—	25	—	30	—	30	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	15	—	15	—	15	—	25	—	30	—	30	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	—	25	—	30	—	35	—	35	—	40	—	40	—	45	ns
t_{PDP}	Output Clock to P	—	25	—	30	—	30	—	35	—	40	—	40	—	45	ns
t_{PDY}	Output Clock to Y	—	25	—	30	—	30	—	35	—	40	—	40	—	45	ns
t_{ENA}	3 State Enable Time[2]	—	25	—	25	—	35	—	40	—	40	—	40	—	45	ns
t_{DIS}	3 State Disable Time[2]	—	25	—	25	—	25	—	25	—	40	—	40	—	45	ns
t_S	Clock Enable Setup Time (IDT7217 only)	12	—	15	—	15	—	15	—	30	—	30	—	30	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML[1] (IDT7216 only)	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV form steady state voltage with loading specified in Figure 2.
3. For Test Load, see Figure 1.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL[1] (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7216L-35 IDT7217L-35 MIN.	MAX.	IDT7216L-45 IDT7217L-45 MIN.	MAX.	IDT7216L-55 IDT7217L-55 MIN.	MAX.	IDT7216L-65 IDT7217L-65 MIN.	MAX.	IDT7216-75 IDT7217L-75 MIN.	MAX.	IDT7216L-90 IDT7217L-90 MIN.	MAX.	IDT7216L-140 IDT7217L-140 MIN.	MAX.	UNITS
t_{MUC}	Unclocked Multiply Time	—	55	—	65	—	75	—	85	—	100	—	125	—	180	ns
t_{MC}	Clocked Multiply Time	—	35	—	45	—	55	—	65	—	75	—	90	—	140	ns
t_S	X, Y, RND Setup Time	12	—	15	—	20	—	20	—	25	—	25	—	25	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	3	—	2	—	0	—	0	—	ns
t_{PWH}	Clock Pulse Width High	10	—	15	—	15	—	15	—	20	—	20	—	25	—	ns
t_{PWL}	Clock Pulse Width Low	10	—	15	—	20	—	20	—	20	—	20	—	25	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	—	25	—	25	—	25	—	30	—	30	—	35	—	40	ns
t_{PDP}	Output Clock to P	—	25	—	25	—	30	—	30	—	35	—	35	—	40	ns
t_{PDY}	Output Clock to Y	—	25	—	25	—	30	—	30	—	35	—	35	—	40	ns
t_{ENA}	3 State Enable Time[2]	—	25	—	25	—	30	—	35	—	35	—	35	—	40	ns
t_{DIS}	3 State Disable Time[2]	—	22	—	22	—	25	—	25	—	30	—	30	—	40	ns
t_S	Clock Enable Setup Time (IDT7217 Only)	10	—	10	—	10	—	10	—	25	—	25	—	25	—	ns
t_H	Clock Enable Hold Time (IDT7217 Only)	3	—	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML[1] (IDT7216 Only)	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. For Test Load, see Figure 1.

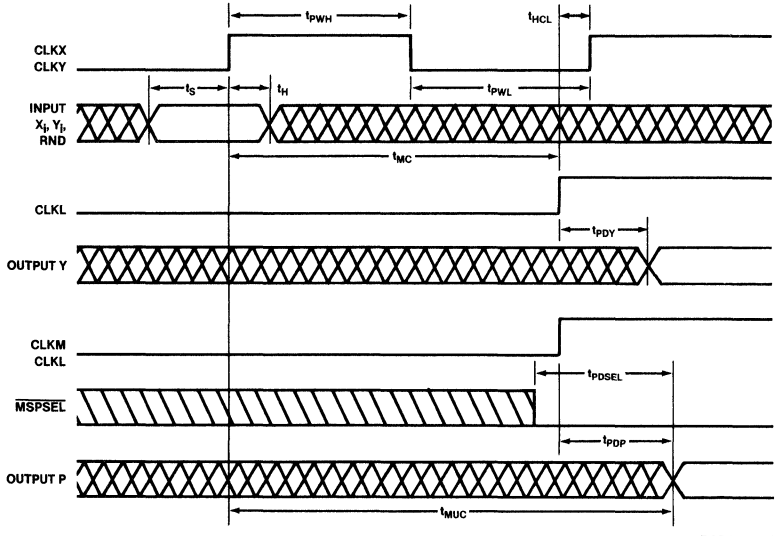
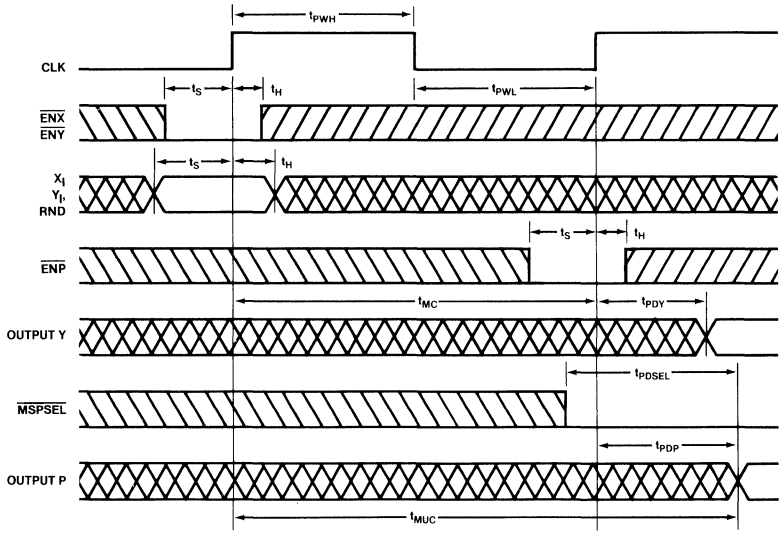


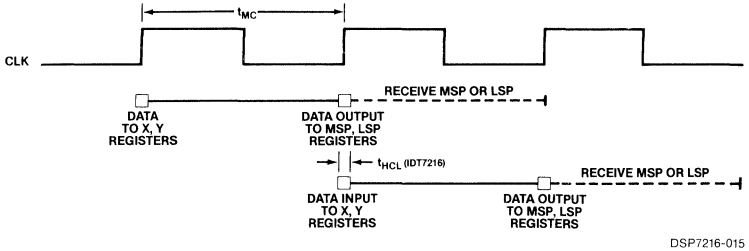
Figure 5. IDT7216 Timing Diagram

DSP7216-013



DSP7216-014

Figure 6. IDT7217 Timing Diagram



DSP7216-015

Figure 7. Simplified Timing Diagram - Typical Application

4

SIGNAL DESCRIPTIONS:

INPUTS:

X_{IN} (X_{15} through X_0)
Sixteen Multiplicand Data Inputs.

Y_{IN} (Y_{15} through Y_0)
Sixteen Multiplier Data Inputs. (This is also an output port for P_{15-0}.)

INPUT CLOCKS (IDT7216 ONLY):

CLKX
The rising edge of this clock loads the X_{15-0} data input register along with the X mode and round registers.

CLKY
The rising edge of this clock loads the Y_{15-0} data input register along with the Y mode and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

INPUT CLOCKS (IDT7217 ONLY):

CLK
The rising edge of this clock loads all registers.

$\overline{ENX}$
Register enable for the X_{15-0} data input register along with the X mode and round registers.

$\overline{ENY}$
Register enable for the Y_{15-0} data input register along with the Y mode and round registers.

$\overline{ENP}$
Register enable for the Most Significant Product (MSP) and Least Significant Product (LSP).

CONTROLS:

X_M, Y_M (TCX, TCY)[1]
Mode control inputs for each data word. A LOW input designates unsigned data input and a HIGH input designates two's complement.

NOTE:
1. TRW MPY016H/K pin designation.

FA (RS)[1]
When the format adjust control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional two's complement applications. (See Multiplier Input/Output Formats.)

FT
When this control is HIGH, both the Most Significant Product (MSP) and Least Significant Product (LSP) registers are transparent.

$\overline{OEL}$
Three-state enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$
Three-state enable for the product output port.

RND
Round control for the rounding of the Most Significant Product (MSP). When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the Least Significant Product (LSP). Note that this bit depends on the state of the format adjust (FA) control. If FA is LOW when RND is HIGH, a one will be added to the 2^{-16}-bit (P_{14}). If FA is HIGH when RND is HIGH, a one will be added to the 2^{-15}-bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH. Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MSPSEL}$
When the $\overline{MSPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

OUTPUTS:

MSP (P_{31} through P_{16})
Most Significant Product Output.

LSP (P_{15} through P_0)
Least Significant Product Output.

Y_{15-0}/LSP_{OUT} (Y_{15} through Y_0 or P_{15} through P_0)
Least Significant Product (LSP) Output available when $\overline{OEL}$ is LOW. This is also an output port for Y_{15-0}.

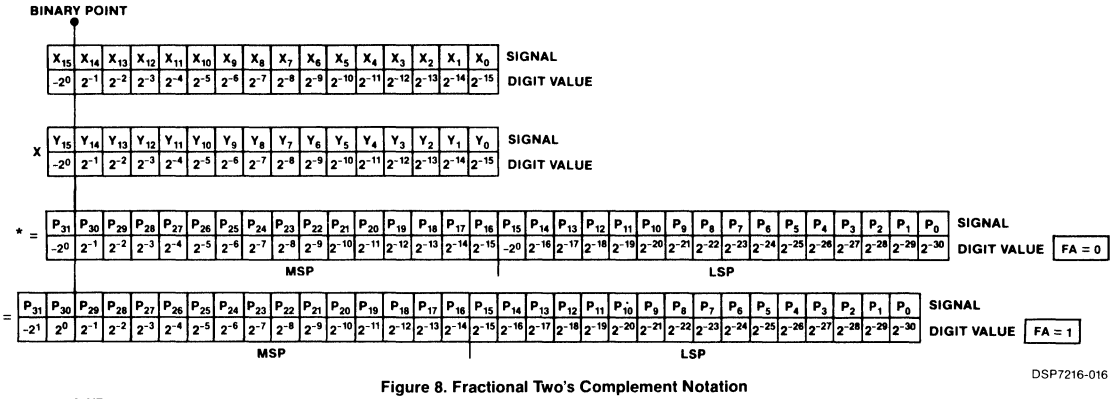


Figure 8. Fractional Two's Complement Notation

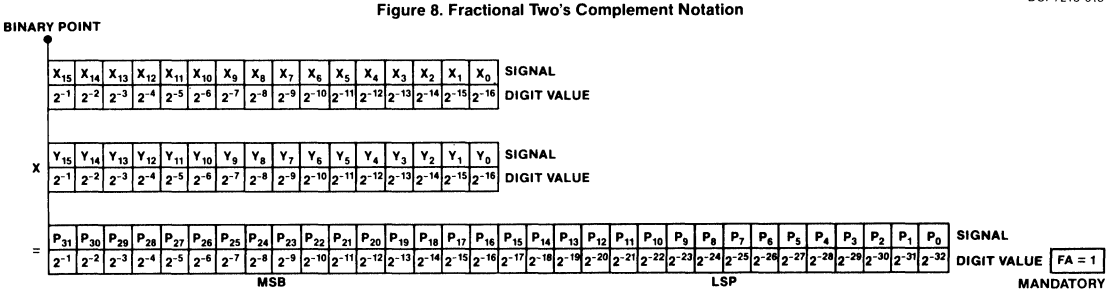


Figure 9. Fractional Unsigned Magnitude Notation

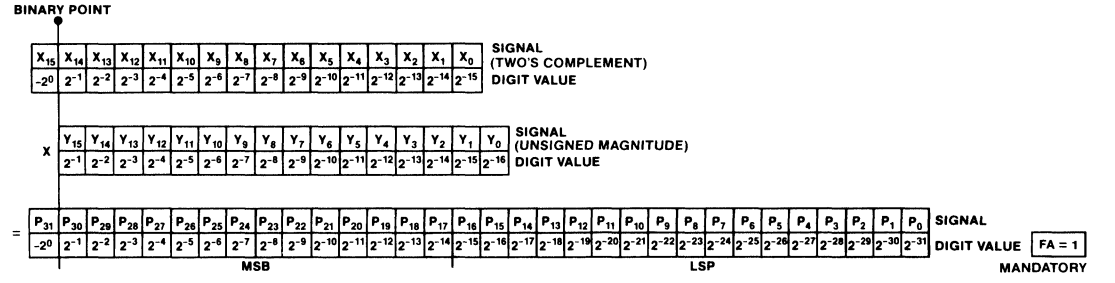


Figure 10. Fractional Mixed Mode Notation

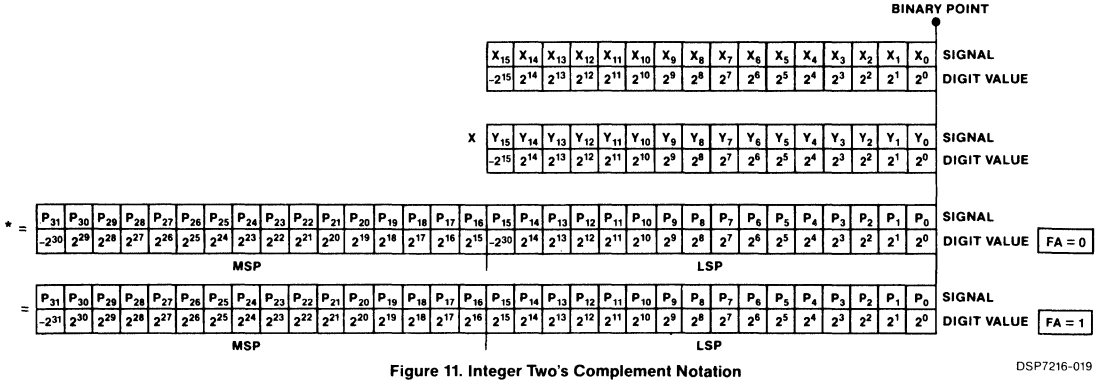


Figure 11. Integer Two's Complement Notation

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1000 . . . 0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

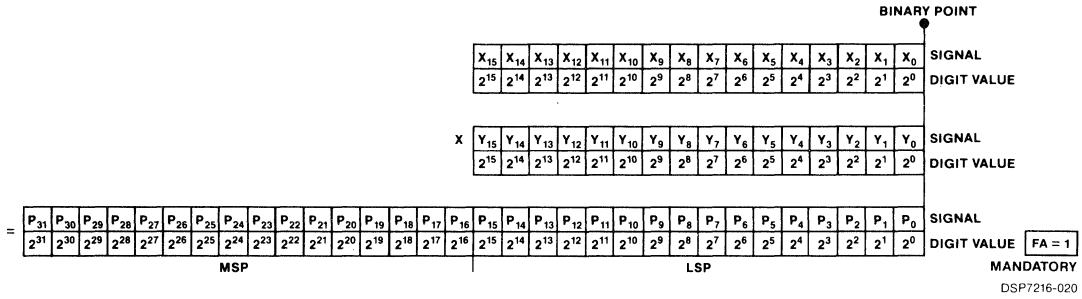


Figure 12. Integer Unsigned Magnitude Notation

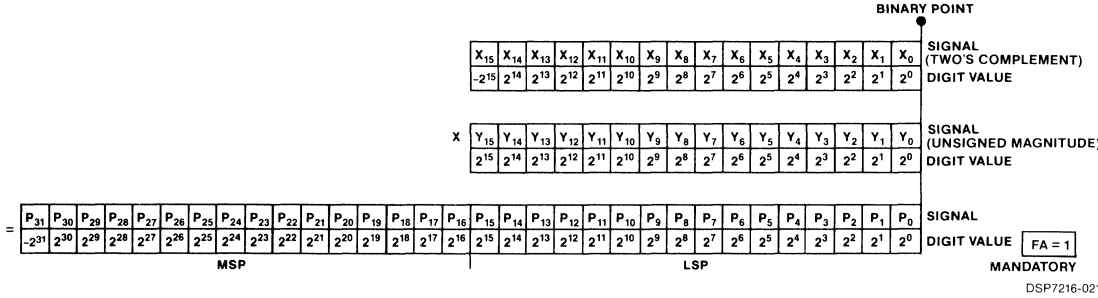


Figure 13. Integer Mixed Mode Notation

Integrated Device Technology, Inc.

64-BIT IEEE FLOATING POINT MULTIPLIER AND ALU

ADVANCE INFORMATION
IDT72264
IDT72265

FEATURES:

- Pin and functionally compatible with Weitek 1264/1265
- Low-power (750mW typical per device) operation
- Single 5 volt supply — no need for two supplies
- Advanced CEMOS™ II 1.5 micron technology
- Fully conforms to the requirements of IEEE Standard 754, version 10.0 for full 32-bit and 64-bit multiply and arithmetic operations.
- Very high-speed operation
  - —10 megaflops (100ns) pipelined ALU operation (add/subtract/convert/compare)
  - —10 megaflops (100ns) pipelined 32-bit (single precision) multiplications
  - —5 megaflops (200ns) pipelined 64-bit (double precision) multiplications
- Full floating point function arithmetic logic unit including:
  - —Add
  - —Subtract
  - —Absolute Value
  - —Compare
  - —Conversion to and from two's complement integer
- Flexible system design
  - —Three 32-bit ports allow two data inputs and one result output every 50ns
  - —One, two, or three port architectures supported
  - —Single phase, edge-triggered clock interface, with fully registered TTL compatible inputs and outputs
- Standard 144-pin grid array package

DESCRIPTION:

The IDT72264 floating-point multiplier and the IDT72265 floating-point ALU provide high-speed 32-bit and 64-bit floating-point processing capability.

The IDT72264/265 are fabricated using IDT's advanced CEMOS II 1.5 micron technology and are capable of a total multiply latency (time required from the input of the operand until the result can be used by another device) of 400ns for single precision and 500ns for double precision multiplications. This ultra-high speed performance is achieved by combining both state-of-the-art CEMOS technology and advanced circuit design techniques.

For signal processing applications, where higher throughput speeds are required, operations including the function specification can be pipelined. For single precision multiplications, new operands can be loaded and a product unloaded every 100ns while double precision multiplies can be accomplished at a 200ns rate. The IDT72265 ALU executes all operations at a 100ns pipelined throughput. All operations including the function specification are pipelined so there is no penalty for interleaving various functions. The on-chip pipeline is automatically advanced using internal timers, so explicit pipeline flushing is not required.

This flexible two-chip set operates in full conformance with the requirements of IEEE standard 754 revision 10.0. It performs operations on single (32-bit) and double (64-bit) precision operands as well as conversion to 32-bit two's complement integers (IDT72265 only). The IDT72264/265 accommodates all rounding modes, infinity and reserved operand representations, and the treatment of exceptions, such as overflow, underflow, invalid and inexact operations. Exact conformance to the standards ensures complete software portability between prototype development and final application. A "FAST" mode eliminates the time penalty for denormalized numbers by substituting zero for a denormalized number.

The flexible input/output architecture of these devices allows them to be used in systems with one, two, or three 32-bit buses, or one 64-bit bus. Fully registered inputs and outputs, separately controlled, are loaded on each positive-going transition of the clock.

A 6-bit function control determines the arithmetic function to be performed while a 4-bit status output flags arithmetic exceptions and conditions. Both the function inputs and status outputs propagate along with the data to ease system design timing.

4

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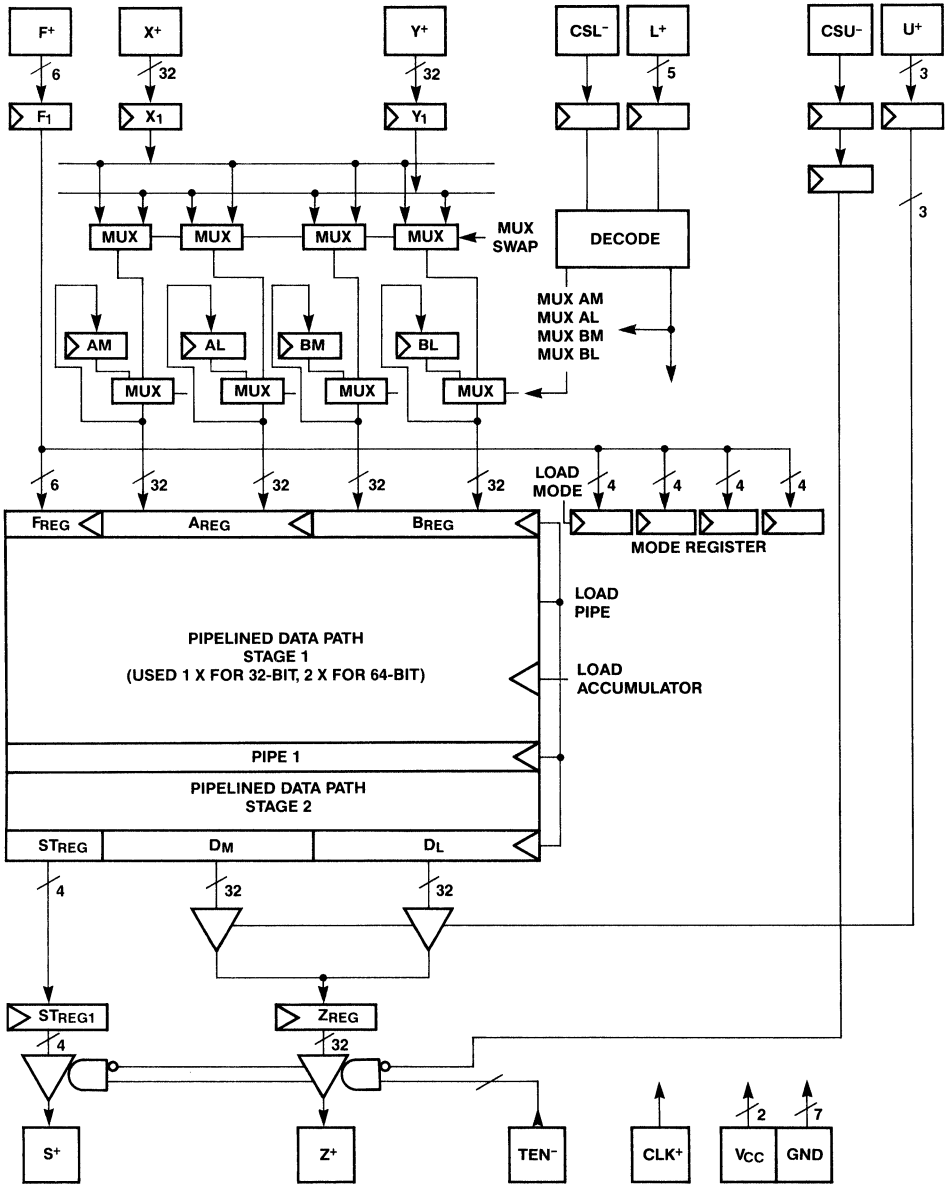
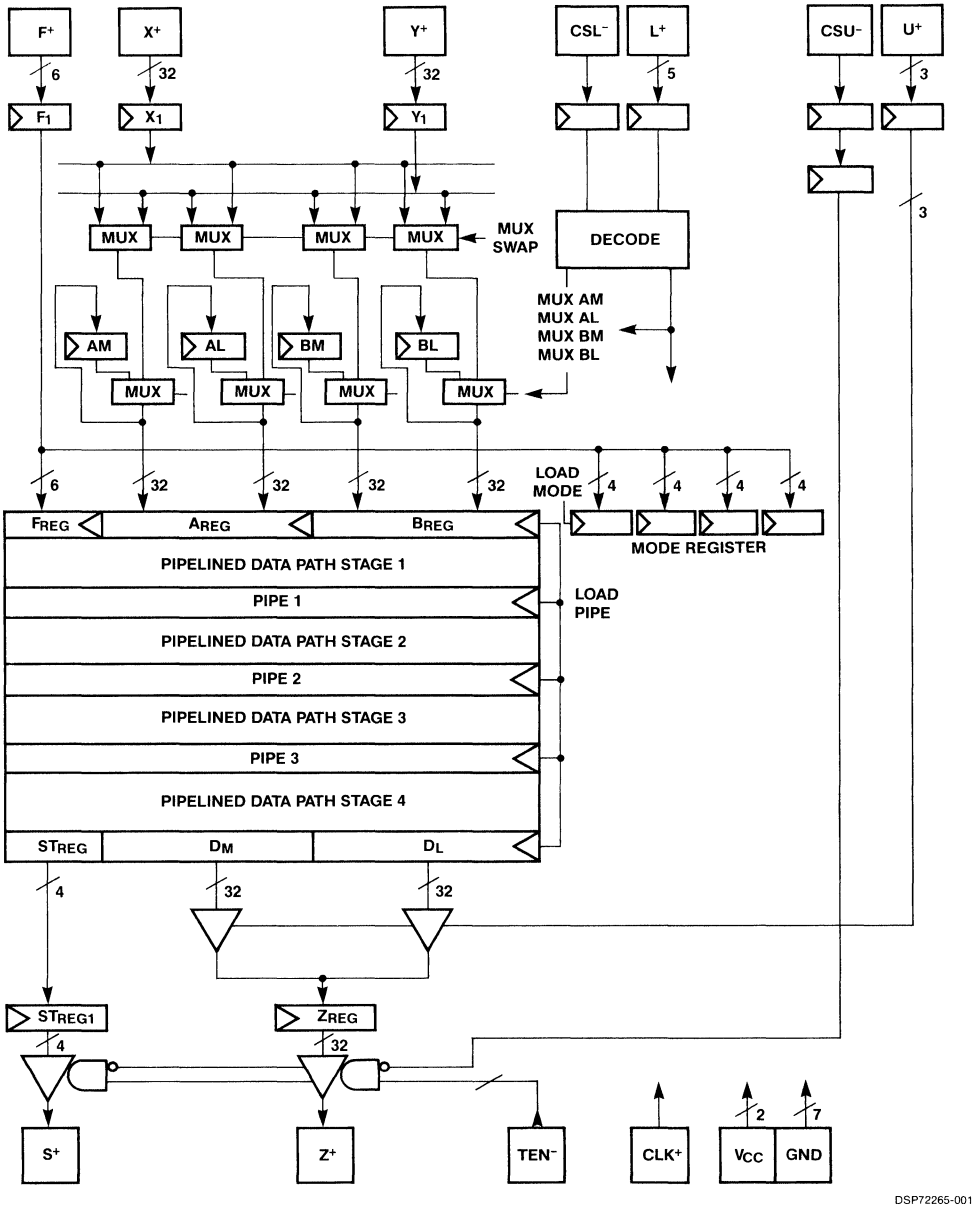
FUNCTIONAL BLOCK DIAGRAM
IDT72264 FLOATING POINT MULTIPLIER



DSP72265-002

FUNCTIONAL BLOCK DIAGRAM
IDT72265 FLOATING POINT ALU



4

PIN CONFIGURATION

GND	Z_{31}	Z_{14}	Z_{13}	Z_{27}	Z_{10}	Z_{25}	Z_{24}	Z_7	Z_{22}	Z_{20}	Z_{19}	Z_3	Z_1	GND
S_3	NC	V_{CC}	Z_{15}	Z_{29}	Z_{12}	Z_{11}	Z_9	Z_6	Z_{21}	Z_4	Z_{18}	Z_{17}	V_{CC}	Y_0
GND	S_2	NC	NC	Z_{30}	Z_{28}	Z_{26}	Z_8	Z_{23}	Z_5	Z_2	Z_{16}	Z_0	GND	Y_{17}
TEN	S_0	NC										NC	Y_{16}	Y_{18}
U_2	CSU	S_1										Y_1	Y_2	Y_4
NC	U_0	U_1										Y_3	Y_{19}	Y_{21}
NC	CLK	NC										Y_5	Y_{20}	Y_6
F_5	F_4	V_{SS}										Y_{23}	Y_{22}	Y_7
F_3	F_0	F_1										Y_8	Y_{25}	Y_{24}
F_2	NC	L_4										Y_{26}	Y_{10}	Y_9
NC	L_2	L_0										Y_{29}	Y_{27}	Y_{11}
L_3	NC	NC										Y_{15}	Y_{13}	Y_{12}
L_1	GND	X_{31}	X_{15}	X_{29}	X_{26}	X_8	X_{23}	X_5	X_3	X_1	NC	Y_{31}	Y_{14}	Y_{28}
CSL	NC	X_{14}	X_{13}	X_{27}	X_{10}	X_{25}	X_{22}	X_{20}	X_{19}	X_2	X_{16}	NC	NC	Y_{30}
GND	X_{30}	X_{28}	X_{12}	X_{11}	X_9	X_{24}	X_7	X_6	X_{21}	X_4	X_{18}	X_{17}	X_0	V_{SS}

144-PIN PGA
(PIN GRID ARRAY)
TOP VIEW

DSP72265-003

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 64 x 4-BIT AND 64 x 5-BIT

ADVANCE INFORMATION
IDT72401/02/03/04

FEATURES:

- First-In, First-Out dual-port memory
- 64 x 4 organization (IDT72401/IDT72403)
  64 x 5 organization (IDT72402/IDT72404)
- Low-power consumption
  —Commercial — Active: 375mW
  —Military — Active: 450mW
- Maximum shift rate
  —15MHz (IDT72401/IDT72402)
  —25MHz (IDT72403/IDT72404)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT72401/02 pin and functionally compatible with MMI67401/02
- IDT72403/04 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CEMOS™ technology
- Available in DIP and LCC
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous, high-performance First-In, First-Out memories organized 64 words by 4 bits. The IDT72402 and IDT72404 are asynchronous, high-performance First-In, First-Out memories organized 64 words by 5 bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input (D_0-$D_{3,4}$). The stored data stack up on a first-in, first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to shift to the output and all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH), or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output contains valid data (OR = HIGH), or to indicate that the FIFO is empty (OR = LOW). The Output Ready signal can also be used to cascade multiple devices together.

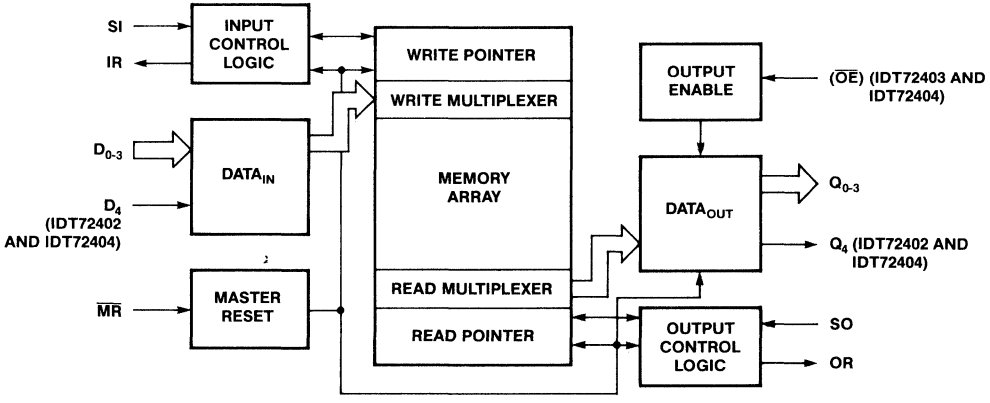
Width expansion is accomplished by logically AND-ing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device, and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 25MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

4

FUNCTIONAL BLOCK DIAGRAM



DSP72401-001

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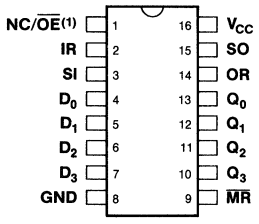
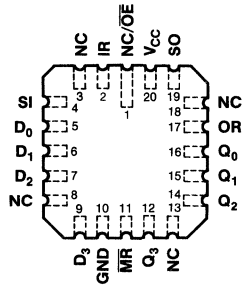
PIN CONFIGURATIONS

IDT72401
IDT72403



DSP72401-002

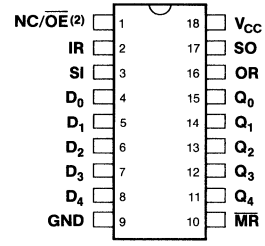
DIP
TOP VIEW



DSP72401-004

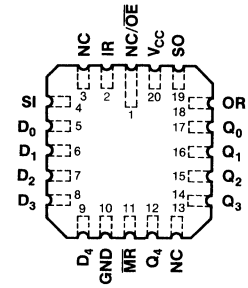
LCC
TOP VIEW

IDT72402
IDT72404



DSP72401-003

DIP
TOP VIEW



DSP72401-005

LCC
TOP VIEW

NOTE:

1. Pin 1: NC — No Connection IDT72401
   $\overline{OE}$ — IDT72403

2. Pin 1: NC — No Connection IDT72402
   $\overline{OE}$ — IDT72404

Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO

ADVANCE INFORMATION
IDT72413

FEATURES:

- First-In, First-Out dual-port memory
- 64 x 5 organization
- Low-power consumption
  — Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time — 35MHz
- Asynchronous and simultaneous read and write
- Cascadable by both word depth and/or bit width
- Half-full and Almost-full/Empty status flags
- IDT72413 is pin and functionally compatible with MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CEMOS™ technology
- Available in DIP and LCC
- Military product available, 100% screened to MIL-STD-883, Class B

DESCRIPTION:

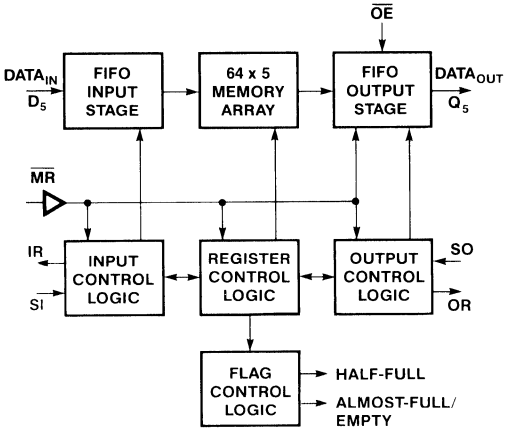
The IDT72413 is a 64 x 5, high-speed First-In, First-Out (FIFO) that loads and empties data on a first-in, first-out basis. It is cascadable in both word depth and/or bit width.

The FIFO has a Half-full flag, which signals when it has 32 or more words in memory. The Almost Full/Empty flag is active when there are 56 or more words in memory, or when there are 8 or less words in memory.

The IDT72413 is pin and functionally compatible to the MMI 67413. It operates at a shift rate of 35MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers.

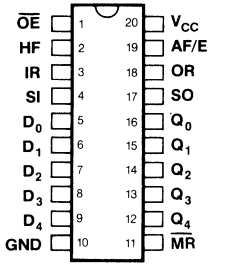
The IDT72413 is fabricated using IDT's high-performance CEMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

FUNCTIONAL BLOCK DIAGRAM



DSP72413-001

PIN CONFIGURATION



DSP72413-002

DIP
TOP VIEW

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Integrated Device Technology, Inc.

Digital Signal Processing Ordering Information

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7201LA35P	35	100	P28	Com'l.
IDT7201LA35J			J32	
IDT7201LA35D			D28-1	
IDT7201LA35L			L32	
IDT7201LA40DB	40	120	D28-1	Mil.
IDT7201LA40LB			L32	
IDT7201LA50P	50	80	P28	Com'l.
IDT7201LA50J			J32	
IDT7201LA50D			D28-1	
IDT7201LA50L			L32	
IDT7201LA50DB		100	D28-1	Mil.
IDT7201LA50LB			L32	
IDT7201LA65P	65	80	P28	Com'l.
IDT7201LA65J			J32	
IDT7201LA65D			D28-1	
IDT7201LA65L			L32	
IDT7201LA65DB		100	D28-1	Mil.
IDT7201LA65LB			L32	
IDT7201LA80P	80	80	P28	Com'l.
IDT7201LA80J			J32	
IDT7201LA80D			D28-1	
IDT7201LA80L			L32	
IDT7201LA80DB		100	D28-1	Mil.
IDT7201LA80LB			L32	
IDT7201LA120P	120	80	P28	Com'l.
IDT7201LA120J			J32	
IDT7201LA120D			D28-1	
IDT7201LA120L			L32	
IDT7201LA120DB		100	D28-1	Mil.
IDT7201LA120LB			L32	
IDT7201SA35P	35	100	P28	Com'l.
IDT7201SA35J			J32	
IDT7201SA35D			D28-1	
IDT7201SA35L			L32	
IDT7201SA40DB	40	120	D28-1	Mil.
IDT7201SA40LB			L32	
IDT7201SA50P	50	80	P28	Com'l.
IDT7201SA50J			J32	
IDT7201SA50D			D28-1	
IDT7201SA50L			L32	
IDT7201SA50DB		100	D28-1	Mil.
IDT7201SA50LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7201SA65P	65	80	P28	Com'l.
IDT7201SA65J			J32	
IDT7201SA65D			D28-1	
IDT7201SA65L			L32	
IDT7201SA65DB		100	D28-1	Mil.
IDT7201SA56LB			L32	
IDT7201SA80P	80	80	P28	Com'l.
IDT7201SA80J			J32	
IDT7201SA80D			D28-1	
IDT7201SA80L			L32	
IDT7201SA80DB		100	D28-1	Mil.
IDT7201SA80LB			L32	
IDT7201SA120P	120	80	P28	Com'l.
IDT7201SA120J			J32	
IDT7201SA120D			D28-1	
IDT7201SA120L			L32	
IDT7201SA120DB		100	D28-1	Mil.
IDT7201SA120LB			L32	
IDT7201L35P	35	100	P28	Com'l.
IDT7201L35J			J32	
IDT7201L35D			D28-1	
IDT7201L35L			L32	
IDT7201L40DB	40	120	D28-1	Mil.
IDT7201L40LB			L32	
IDT7201L50P	50	80	P28	Com'l.
IDT7201L50J			J32	
IDT7201L50D			D28-1	
IDT7201L50L			L32	
IDT7201L50DB		100	D28-1	Mil.
IDT7201L50LB			L32	
IDT7201L65P	65	80	P28	Com'l.
IDT7201L65J			J32	
IDT7201L65D			D28-1	
IDT7201L65L			L32	
IDT7201L65DB		100	D28-1	Mil.
IDT7201L65LB			L32	
IDT7201L80P	80	80	P28	Com'l.
IDT7201L80J			J32	
IDT7201L80D			D28-1	
IDT7201L80L			L32	
IDT7201L80DB		100	D28-1	Mil.
IDT7201L80LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7201L120P	120	80	P28	Com'l.
IDT7201L120J			J32	
IDT7201L120D			D28-1	
IDT7201L120L			L32	
IDT7201L120DB		100	D28-1	Mil.
IDT7201L120LB			L32	
IDT7201S35P	35	100	P28	Com'l.
IDT7201S35J			J32	
IDT7201S35D			D28-1	
IDT7201S35L			L32	
IDT7201S40DB	40	120	D28-1	Mil.
IDT7201S40LB			L32	
IDT7201S50P	50	80	P28	Com'l.
IDT7201S50J			J32	
IDT7201S50D			D28-1	
IDT7201S50L			L32	
IDT7201S50DB		100	D28-1	Mil.
IDT7201S50LB			L32	
IDT7201S65P	65	80	P28	Com'l.
IDT7201S65J			J32	
IDT7201S65D			D28-1	
IDT7201S65L			L32	
IDT7201S65DB		100	D28-1	Mil.
IDT7201S65LB			L32	
IDT7201S80P	80	80	P28	Com'l.
IDT7201S80J			J32	
IDT7201S80D			D28-1	
IDT7201S80L			L32	
IDT7201S80DB		100	D28-1	Mil.
IDT7201S80LB			L32	
IDT7201S120P	120	80	P28	Com'l.
IDT7201S120J			J32	
IDT7201S120D			D28-1	
IDT7201S120L			L32	
IDT7201S120DB		100	D28-1	Mil.
IDT7201S120LB			L32	
IDT7202LA35P	35	100	P28	Com'l.
IDT7202LA35J			J32	
IDT7202LA35D			D28-1	
IDT7202LA35L			L32	
IDT7202LA40DB	40	120	D28-1	Mil.
IDT7202LA40LB			L32	
IDT7202LA50P	50	80	P28	Com'l.
IDT7202LA50J			J32	
IDT7202LA50D			D28-1	
IDT7202LA50L			L32	
IDT7202LA50DB		100	D28-1	Mil.
IDT7202LA50LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7202LA65P	65	80	P28	Com'l.
IDT7202LA65J			J32	
IDT7202LA65D			D28-1	
IDT7202LA65L			L32	
IDT7202LA65DB		100	D28-1	Mil.
IDT7202LA65LB			L32	
IDT7202LA80P	80	80	P28	Com'l.
IDT7202LA80J			J32	
IDT7202LA80D			D28-1	
IDT7202LA80L			L32	
IDT7202LA80DB		100	D28-1	Mil.
IDT7202LA80LB			L32	
IDT7202LA120P	120	80	P28	Com'l.
IDT7202LA120J			J32	
IDT7202LA120D			D28-1	
IDT7202LA120L			L32	
IDT7202LA120DB		100	D28-1	Mil.
IDT7202LA120LB			L32	
IDT7202SA35P	35	100	P28	Com'l.
IDT7202SA35J			J32	
IDT7202SA35D			D28-1	
IDT7202SA35L			L32	
IDT7202SA40DB	40	120	D28-1	Mil.
IDT7202SA40LB			L32	
IDT7202SA50P	50	80	P28	Com'l.
IDT7202SA50J			J32	
IDT7202SA50D			D28-1	
IDT7202SA50L			L32	
IDT7202SA50DB		100	D28-1	Mil.
IDT7202SA50LB			L32	
IDT7202SA65P	65	80	P28	Com'l.
IDT7202SA65J			J32	
IDT7202SA65D			D28-1	
IDT7202SA65L			L32	
IDT7202SA65DB		100	D28-1	Mil.
IDT7202SA65LB			L32	
IDT7202SA80P	80	80	P28	Com'l.
IDT7202SA80J			J32	
IDT7202SA80D			D28-1	
IDT7202SA80L			L32	
IDT7202SA80DB		100	D28-1	Mil.
IDT7202SA80LB			L32	
IDT7202SA120P	120	80	P28	Com'l.
IDT7202SA120J			J32	
IDT7202SA120D			D28-1	
IDT7202SA120L			L32	
IDT7202SA120DB		100	D28-1	Mil.
IDT7202SA120LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7202L35P	35	100	P28	Com'l.
IDT7202L35J			J32	
IDT7202L35D			D28-1	
IDT7202L35L			L32	
IDT7202L40DB	40	120	D28-1	Mil.
IDT7202L40LB			L32	
IDT7202L50P	50	80	P28	Com'l.
IDT7202L50J			J32	
IDT7202L50D			D28-1	
IDT7202L50L			L32	
IDT7202L50DB		100	D28-1	Mil.
IDT7202L50LB			L32	
IDT7202L65P	65	80	P28	Com'l.
IDT7202L65J			J32	
IDT7202L65D			D28-1	
IDT7202L65L			L32	
IDT7202L65DB		100	D28-1	Mil.
IDT7202L65LB			L32	
IDT7202L80P	80	80	P28	Com'l.
IDT7202L80J			J32	
IDT7202L80D			D28-1	
IDT7202L80L			L32	
IDT7202L80DB		100	D28-1	Mil.
IDT7202L80LB			L32	
IDT7202L120P	120	80	P28	Com'l.
IDT7202L120J			J32	
IDT7202L120D			D28-1	
IDT7202L120L			L32	
IDT7202L120DB		100	D28-1	Mil.
IDT7202L120LB			L32	
IDT7202S35P	35	100	P28	Com'l.
IDT7202S35J			J32	
IDT7202S35D			D28-1	
IDT7202S35L			L32	
IDT7202S40DB	40	120	D28-1	Mil.
IDT7202S40LB			L32	
IDT7202S50P	50	80	P28	Com'l.
IDT7202S50J			J32	
IDT7202S50D			D28-1	
IDT7202S50L			L32	
IDT7202S50DB		100	D28-1	Mil.
IDT7202S50LB			L32	
IDT7202S65P	65	80	P28	Com'l.
IDT7202S65J			J32	
IDT7202S65D			D28-1	
IDT7202S65L			L32	
IDT7202S65DB		100	D28-1	Mil.
IDT7202S65LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7202S80P	80	80	P28	Com'l.
IDT7202S80J			J32	
IDT7202S80D			D28-1	
IDT7202S80L			L32	
IDT7202S80DB		100	D28-1	Mil.
IDT7202S80LB			L32	
IDT7202S120P	120	80	P28	Com'l.
IDT7202S120J			J32	
IDT7202S120D			D28-1	
IDT7202S120L			L32	
IDT7202S120DB		100	D28-1	Mil.
IDT7202S120LB			L32	
IDT7203L50P	50	120	P28	Com'l.
IDT7203L50D			D28-1	
IDT7203L50C			D28-3	
IDT7203L50L			L32	
IDT7203L50DB		150	D28-1	Mil.
IDT7203L50CB			D28-3	
IDT7203L50LB			L32	
IDT7203L65P	65	120	P28	Com'l.
IDT7203L65D			D28-1	
IDT7203L65C			D28-3	
IDT7203L65L			L32	
IDT7203L65DB		150	D28-1	Mil.
IDT7203L65CB			D28-3	
IDT7203L65LB			L32	
IDT7203L80P	80	120	P28	Com'l.
IDT7203L80D			D28-1	
IDT7203L80C			D28-3	
IDT7203L80L			L32	
IDT7203L80DB		150	D28-1	Mil.
IDT7203L80CB			D28-3	
IDT7203L80LB			L32	
IDT7203L120P	120	120	P28	Com'l.
IDT7203L120D			D28-1	
IDT7203L120C			D28-3	
IDT7203L120L			L32	
IDT7203L120DB		150	D28-1	Mil.
IDT7203L120CB			D28-3	
IDT7203L120LB			L32	
IDT7203S50P	50	120	P28	Com'l.
IDT7203S50D			D28-1	
IDT7203S50C			D28-3	
IDT7203S50L			L32	
IDT7203S50DB		150	D28-1	Mil.
IDT7203S50CB			D28-3	
IDT7203S50LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7203S65P	65	120	P28	Com'l.
IDT7203S65D			D28-1	
IDT7203S65C			D28-3	
IDT7203S65L			L32	
IDT7203S65DB		150	D28-1	Mil.
IDT7203S65CB			D28-3	
IDT7203S65LB			L32	
IDT7203S80P	80	120	P28	Com'l.
IDT7203S80D			D28-1	
IDT7203S80C			D28-3	
IDT7203S80L			L32	
IDT7203S80DB		150	D28-1	Mil.
IDT7203S80CB			D28-3	
IDT7203S80LB			L32	
IDT7203S120P	120	120	P28	Com'l.
IDT7203S120D			D28-1	
IDT7203S120C			D28-3	
IDT7203S120L			L32	
IDT7203S120DB		150	D28-1	Mil.
IDT7203S12CB			D28-3	
IDT7203S120LB			L32	
IDT7204L50P	50	120	P28	Com'l.
IDT7204L50D			D28-1	
IDT7204L50C			D28-3	
IDT7204L50L			L32	
IDT7204L50DB		150	D28-1	Mil.
IDT7204L50CB			D28-3	
IDT7204L50LB			L32	
IDT7204L65P	65	120	P28	Com'l.
IDT7204L65D			D28-1	
IDT7204L65C			D28-3	
IDT7204L65L			L32	
IDT7204L65DB		150	D28-1	Mil.
IDT7204L65CB			D28-3	
IDT7204L65LB			L32	
IDT7204L80P	80	120	P28	Com'l.
IDT7204L80D			D28-1	
IDT7204L80C			D28-3	
IDT7204L80L			L32	
IDT7204L80DB		150	D28-1	Mil.
IDT7204L80CB			D28-3	
IDT7204L80LB			L32	
IDT7204L120P	120	120	P28	Com'l.
IDT7204L120D			D28-1	
IDT7204L120C			D28-3	
IDT7204L120L			L32	
IDT7204L120DB		150	D28-1	Mil.
IDT7204L120CB			D28-3	
IDT7204L120LB			L32	

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7204S50P	50	120	P28	Com'l.
IDT7204S50D			D28-1	
IDT7204S50C			D28-3	
IDT7204S50L			L32	
IDT7204S50DB		150	D28-1	Mil.
IDT7204S50CB			D28-3	
IDT7204S50LB			L32	
IDT7204S65P	65	120	P28	Com'l.
IDT7204S65D			D28-1	
IDT7204S65C			D28-3	
IDT7204S65L			L32	
IDT7204S65DB		150	D28-1	Mil.
IDT7204S65CB			D28-3	
IDT7204S65LB			L32	
IDT7204S80P	80	120	P28	Com'l.
IDT7204S80D			D28-1	
IDT7204S80C			D28-3	
IDT7204S80L			L32	
IDT7204S80DB		150	D28-1	Mil.
IDT7204S80CB			D28-3	
IDT7204S80LB			L32	
IDT7204S120P	120	120	P28	Com'l.
IDT7204S120D			D28-1	
IDT7204S120C			D28-3	
IDT7204S120L			L32	
IDT7204S120DB		150	D28-1	Mil.
IDT7204S120CB			D28-3	
IDT7204S120LB			L32	
IDT72064	Consult Factory			
IDT72065	Consult Factory			

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7209L30P	30	P64	Com'l
IDT7209L30C		D64	
IDT7209L30XC		D68	
IDT7209L30L		L68-1	
IDT7209L40CB	40	D64	Mil.
IDT7209L40XCB		D68	
IDT7209L40LB		L68-1	
IDT7209L45P	45	P64	Com'l.
IDT7209L45C		D64	
IDT7209L45XC		D68	
IDT7209L45L		L68-2	
IDT7209L55CB	55	D64	Mil.
IDT7209L55XCB		D68	
IDT7209L55LB		L68-2	

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ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7209L65P	45	P64	Com'l.
IDT7209L65C		D64	
IDT7209L65XC		D68	
IDT7209L65L		L68-2	
IDT7209L75CB	75	D64	Mil.
IDT7209L75XCB		D68	
IDT7209L75LB		L68-2	
IDT7209L100P	100	P64	Com'l.
IDT7209L100C		D64	
IDT7209L100XC		D68	
IDT7209L100L		L68-2	
IDT7209L120CB	120	D64	Mil.
IDT7209L120XCB		D68	
IDT7209L120LB		L68-2	
IDT7209L135P	135	P64	Com'l.
IDT7209L135C		D64	
IDT7209L135XC		D68	
IDT7209L135L		L68-2	
IDT7209L170CB	170	D64	Mil.
IDT7209L170XCB		D68	
IDT7209L170LB		L68-2	
IDT7210L35P	35	P64	Com'l.
IDT7210L35J		J68	
IDT7210L35C		D64	
IDT7210L35XC		D68	
IDT7210L35L		L68-1	
IDT7210L35XL		L68-2	
IDT7210L35F		F64	
IDT7210L40CB	40	D64	Mil.
IDT7210L40XCB		D68	
IDT7210L40LB		L68-1	
IDT7210L40XLB		L68-2	
IDT7210L40FB		F64	
IDT7210L45P	45	P64	Com'l.
IDT7210L45J		J68	
IDT7210L45C		D64	
IDT7210L45XC		D68	
IDT7210L45L		L68-1	
IDT7210L45XL		L68-2	
IDT7210L45F		F64	
IDT7210L55P	55	P64	Com'l.
IDT7210L55J		J68	
IDT7210L55C		D64	
IDT7210L55XC		D68	
IDT7210L55L		L68-1	
IDT7210L55XL		L68-2	
IDT7210L55F		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7210L55CB	55	D64	Mil.
IDT7210L55XCB		D68	
IDT7210L55LB		L68-1	
IDT7210L55XLB		L68-2	
IDT7210L55FB		F64	
IDT7210L65P	65	P64	Com'l.
IDT7210L65J		J68	
IDT7210L65C		D64	
IDT7210L65XC		D68	
IDT7210L65L		L68-1	
IDT7210L65XL		L68-2	
IDT7210L65F		F64	
IDT7210L65CB		D64	Mil.
IDT7210L65XCB		D68	
IDT7210L65LB		L68-1	
IDT7210L65XLB		L68-2	
IDT7210L65FB		F64	
IDT7210L75P	75	P64	Com'l.
IDT7210L75J		J68	
IDT7210L75C		D64	
IDT7210L75XC		D68	
IDT7210L75L		L68-1	
IDT7210L75XL		L68-2	
IDT7210L75F		F64	
IDT7210L75CB		D64	Mil.
IDT7210L75XCB		D68	
IDT7210L75LB		L68-1	
IDT7210L75XLB		L68-2	
IDT7210L75FB		F64	
IDT7210L85CB	85	D64	Mil.
IDT7210L85XCB		D68	
IDT7210L85LB		L68-1	
IDT7210L85XLB		L68-2	
IDT7210L85FB		F64	
IDT7210L100P	100	P64	Com'l.
IDT7210L100J		J68	
IDT7210L100C		D64	
IDT7210L100XC		D68	
IDT7210L100L		L68-1	
IDT7210L100XL		L68-2	
IDT7210L100F		F64	
IDT7210L120CB	120	D64	Mil.
IDT7210L120XCB		D68	
IDT7210L120LB		L68-1	
IDT7210L120XLB		L68-2	
IDT7210L120FB		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7210L165P	165	P64	Com'l.
IDT7210L165J		J68	
IDT7210L165C		D64	
IDT7210L165XC		D68	
IDT7210L165L		L68-1	
IDT7210L165XL		L68-2	
IDT7210L165F		F64	
IDT7210L200CB	200	D64	Mil.
IDT7210L200XCB		D68	
IDT7210L200LB		L68-1	
IDT7210L200XLB		L68-2	
IDT7210L200FB		F64	
IDT72103	Consult Factory		
IDT72104	Consult Factory		
IDT7212L30P	30	P64	Com'l.
IDT7212L30C		D64	
IDT7212L30XC		D68	
IDT7212L30L		L68-1	
IDT7212L30F		F64	
IDT7212L40CB	40	D64	Mil.
IDT7212L40XCB		D68	
IDT7212L40LB		L68-1	
IDT7212L40FB		F64	
IDT7212L45P	45	P64	Com'l.
IDT7212L45C		D64	
IDT7212L45XC		D68	
IDT7212L45L		L68-1	
IDT7212L45F		F64	
IDT7212L55CB	55	D64	Mil.
IDT7212L55XCB		D68	
IDT7212L55LB		L68-1	
IDT7212L55FB		F64	
IDT7212L70P	70	P64	Com'l.
IDT7212L70C		D64	
IDT7212L70XC		D68	
IDT7212L70L		L68-1	
IDT7212L70F		F64	
IDT7212L90CB	90	D64	Mil.
IDT7212L90XCB		D68	
IDT7212L90LB		L68-1	
IDT7212L90FB		F64	
IDT7212L115P	115	P64	Com'l.
IDT7212L115C		D64	
IDT7212L115XC		D68	
IDT7212L115L		L68-1	
IDT7212L115F		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7212L140CB	140	D64	Mil.
IDT7212L140XCB		D68	
IDT7212L140LB		L68-1	
IDT7212L140FB		F64	
IDT7213L30P	30	P64	Com'l.
IDT7213L30C		D64	
IDT7213L30XC		D68	
IDT7213L30L		L68-1	
IDT7213L30F		F64	
IDT7213L40CB	40	D64	Mil.
IDT7213L40XCB		D68	
IDT7213L40LB		L68-1	
IDT7213L40FB		F64	
IDT7213L45P	45	P64	Com'l.
IDT7213L45C		D64	
IDT7213L45XC		D68	
IDT7213L45L		L68-1	
IDT7213L45F		F64	
IDT7213L55CB	55	D64	Mil.
IDT7213L55XCB		D68	
IDT7213L55LB		L68-1	
IDT7213L55FB		F64	
IDT7213L70P	70	P64	Com'l.
IDT7213L70C		D64	
IDT7213L70XC		D68	
IDT7213L70L		L68-1	
IDT7213L70F		F64	
IDT7213L90CB	90	D64	Mil.
IDT7213L90XCB		D68	
IDT7213L90LB		L68-1	
IDT7213L90FB		F64	
IDT7213L115P	115	P64	Com'l.
IDT7213L115C		D64	
IDT7213L115XC		D68	
IDT7213L115L		L68-1	
IDT7213L115F		F64	
IDT7213L140CB	140	D64	Mil.
IDT7213L140XCB		D68	
IDT7213L140LB		L68-1	
IDT7213L140FB		F64	
IDT7216L35P	35	P64	Com'l.
IDT7216L35J		J68	
IDT7216L35C		D64	
IDT7216L35XC		D68	
IDT7216L35G		G68	
IDT7216L35L		L68-1	
IDT7216L35XL		L68-2	
IDT7216L35F		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7216L40CB	40	D64	Mil.
IDT7216L40XCB		D68	
IDT7216L40GB		G68	
IDT7216L40LB		L68-1	
IDT7216L40XLB		L68-2	
IDT7216L40FB		F64	
IDT7216L45P	45	P64	Com'l.
IDT7216L45J		J68	
IDT7216L45C		D64	
IDT7216L45XC		D68	
IDT7216L45G		G68	
IDT7216L45L		L68-1	
IDT7216L45XL		L68-2	
IDT7216L45F		F64	
IDT7216L55P	55	P64	Com'l.
IDT7216L55J		J68	
IDT7216L55C		D64	
IDT7216L55XC		D68	
IDT7216L55G		G68	
IDT7216L55L		L68-1	
IDT7216L55XL		L68-2	
IDT7216L55F		F64	
IDT7216L55CB		D64	Mil.
IDT7216L55XCB		D68	
IDT7216L55GB		G68	
IDT7216L55LB		L68-1	
IDT7216L55XLB		L68-2	
IDT7216L55FB		F64	
IDT7216L65P	65	P64	Com'l.
IDT7216L65J		J68	
IDT7216L65C		D64	
IDT7216L65XC		D68	
IDT7216L65G		G68	
IDT7216L65L		L68-1	
IDT7216L65XL		L68-2	
IDT7216L65F		F64	
IDT7216L65CB		D64	Mil.
IDT7216L65XCB		D68	
IDT7216L65GB		G68	
IDT7216L65LB		L68-1	
IDT7216L65XLB		L68-2	
IDT7216L65FB		F64	
IDT7216L75P	75	P64	Com'l.
IDT7216L75J		J68	
IDT7216L75C		D64	
IDT7216L75XC		D68	
IDT7216L75G		G68	
IDT7216L75L		L68-1	
IDT7216L75XL		L68-2	
IDT7216L75F		F64	

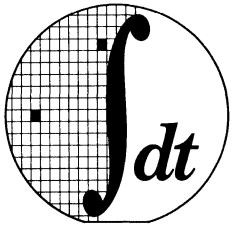
ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7216L75CB	75	D64	Mil.
IDT7216L75XCB		D68	
IDT7216L75GB		G68	
IDT7216L75LB		L68-1	
IDT7216L75XLB		L68-2	
IDT7216L75FB		F64	
IDT7216L90P	90	P64	Com'l.
IDT7216L90J		J68	
IDT7216L90C		D64	
IDT7216L90XC		D68	
IDT7216L90G		G68	
IDT7216L90L		L68-1	
IDT7216L90XL		L68-2	
IDT7216L90F		F64	
IDT7216L90CB		D64	Mil.
IDT7216L90XCB		D68	
IDT7216L90GB		G68	
IDT7216L90LB		L68-1	
IDT7216L90XLB		L68-2	
IDT7216L90FB		F64	
IDT7216L120CB	120	D64	Mil.
IDT7216L120XCB		D68	
IDT7216L120GB		G68	
IDT7216L120LB		L68-1	
IDT7216L120XLB		L68-2	
IDT7216L120FB		F64	
IDT7216L140P	140	P64	Com'l.
IDT7216L140J		J68	
IDT7216L140C		D64	
IDT7216L140XC		D68	
IDT7216L140G		G68	
IDT7216L140L		L68-1	
IDT7216L140XL		L68-2	
IDT7216L140F		F64	
IDT7216L185CB	185	D64	Mil.
IDT7216L185XCB		D68	
IDT7216L185GB		G68	
IDT7216L185LB		L68-1	
IDT7216L185XLB		L68-2	
IDT7216L185FB		F64	
IDT7217L35P	35	P64	Com'l.
IDT7217L35J		J68	
IDT7217L35C		D64	
IDT7217L35XC		D68	
IDT7217L35G		G68	
IDT7217L35L		L68-1	
IDT7217L35XL		L68-2	
IDT7217L35F		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7217L40CB	40	D64	Mil.
IDT7217L40XCB		D68	
IDT7217L40GB		G68	
IDT7217L40LB		L68-1	
IDT7217L40XLB		L68-2	
IDT7217L40FB		F64	
IDT7217L45P	45	P64	Com'l.
IDT7217L45J		J68	
IDT7217L45C		D64	
IDT7217L45XC		D68	
IDT7217L45G		G68	
IDT7217L45L		L68-1	
IDT7217L45XL		L68-2	
IDT7217L45F		F64	
IDT7217L55P	55	P64	Com'l.
IDT7217L55J		J68	
IDT7217L55C		D64	
IDT7217L55XC		D68	
IDT7217L55G		G68	
IDT7217L55L		L68-1	
IDT7217L55XL		L68-2	
IDT7217L55F		F64	
IDT7217L55CB		D64	Mil.
IDT7217L55XCB		D68	
IDT7217L55GB		G68	
IDT7217L55LB		L68-1	
IDT7217L55XLB		L68-2	
IDT7217L55FB		F64	
IDT7217L65P	65	P64	Com'l.
IDT7217L65J		J68	
IDT7217L65C		D64	
IDT7217L65XC		D68	
IDT7217L65G		G68	
IDT7217L65L		L68-1	
IDT7217L65XL		L68-2	
IDT7217L65F		F64	
IDT7217L65CB		D64	Mil.
IDT7217L65XCB		D68	
IDT7217L65GB		G68	
IDT7217L65LB		L68-1	
IDT7217L65XLB		L68-2	
IDT7217L65FB		F64	
IDT7217L75P	75	P64	Com'l.
IDT7217L75J		J68	
IDT7217L75C		D64	
IDT7217L75XC		D68	
IDT7217L75G		G68	
IDT7217L75L		L68-1	
IDT7217L75XL		L68-2	
IDT7217L75F		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7217L75CB		D64	Mil.
IDT7217L75XCB		D68	
IDT7217L75GB		G68	
IDT7217L75LB		L68-1	
IDT7217L75XLB		L68-2	
IDT7217L75FB		F64	
IDT7217L90P	90	P64	Com'l.
IDT7217L90J		J68	
IDT7217L90C		D64	
IDT7217L90XC		D68	
IDT7217L90G		G68	
IDT7217L90L		L68-1	
IDT7217L90XL		L68-2	
IDT7217L90F		F64	
IDT7217L90CB		D64	Mil.
IDT7217L90XCB		D68	
IDT7217L90GB		G68	
IDT7217L90LB		L68-1	
IDT7217L90XLB		L68-2	
IDT7217L90FB		F64	
IDT7217L120CB	120	D64	Mil.
IDT7217L120XCB		D68	
IDT7217L120GB		G68	
IDT7217L120LB		L68-1	
IDT7217L120XLB		L68-2	
IDT7217L120FB		F64	
IDT7217L140P	140	P64	Com'l.
IDT7217L140J		J68	
IDT7217L140C		D64	
IDT7217L140XC		D68	
IDT7217L140G		G68	
IDT7217L140L		L68-1	
IDT7217L140XL		L68-2	
IDT7217L140F		F64	
IDT7217L185CB	185	D64	Mil.
IDT7217L185XCB		D68	
IDT7217L185GB		G68	
IDT7217L185LB		L68-1	
IDT7217L185XLB		L68-2	
IDT7217L185FB		F64	
IDT72264	Consult Factory		
IDT72265	Consult Factory		
IDT72401	Consult Factory		
IDT72402	Consult Factory		
IDT72403	Consult Factory		

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT72404	Consult Factory		
IDT72413	Consult Factory		
IDT7243L35P	35	P64	Com'l.
IDT7243L35J		J68	
IDT7243L35C		D64	
IDT7243L35XC		D68	
IDT7243L35L		L68-1	
IDT7243L35XL		L68-2	
IDT7243L35F		F64	
IDT7243L40CB	40	D64	Mil.
IDT7243L40XCB		D68	
IDT7243L40LB		L68-1	
IDT7243L40XLB		L68-2	
IDT7243L40FB		F64	
IDT7243L45P	45	P64	Com'l.
IDT7243L45J		J68	
IDT7243L45C		D64	
IDT7243L45XC		D68	
IDT7243L45L		L68-1	
IDT7243L45XL		L68-2	
IDT7243L45F		F64	
IDT7243L55P	55	P64	Com'l.
IDT7243L55J		J68	
IDT7243L55C		D64	
IDT7243L55XC		D68	
IDT7243L55L		L68-1	
IDT7243L55XL		L68-2	
IDT7243L55F		F64	
IDT7243L55CB	55	D64	Mil.
IDT7243L55XCB		D68	
IDT7243L55LB		L68-1	
IDT7243L55XLB		L68-2	
IDT7243L55FB		F64	
IDT7243L65P	65	P64	Com'l.
IDT7243L65J		J68	
IDT7243L65C		D64	
IDT7243L65XC		D68	
IDT7243L65L		L68-1	
IDT7243L65XL		L68-2	
IDT7243L65F		F64	
IDT7243L65CB		D64	Mil.
IDT7243L65XCB		D68	
IDT7243L65LB		L68-1	
IDT7243L65XLB		L68-2	
IDT7243L65FB		F64	

ORDER PART NUMBER	SPEED	PACKAGE TYPE	OPER. TEMP.
IDT7243L75P	75	P64	Com'l.
IDT7243L75J		J68	
IDT7243L75C		D64	
IDT7243L75XC		D68	
IDT7243L75L		L68-1	
IDT7243L75XL		L68-2	
IDT7243L75F		F64	
IDT7243L75CB		D64	Mil.
IDT7243L75XCB		D68	
IDT7243L75LB		L68-1	
IDT7243L75XLB		L68-2	
IDT7243L75FB		F64	
IDT7243L85CB	85	D64	Mil.
IDT7243L85XCB		D68	
IDT7243L85LB		L68-1	
IDT7243L85XLB		L68-2	
IDT7243L85FB		F64	
IDT7243L100P	100	P64	Com'l.
IDT7243L100J		J68	
IDT7243L100C		D64	
IDT7243L100XC		D68	
IDT7243L100L		L68-1	
IDT7243L100XL		L68-2	
IDT7243L100F		F64	
IDT7243L120CB	120	D64	Mil.
IDT7243L120XCB		D68	
IDT7243L120LB		L68-1	
IDT7243L120XLB		L68-2	
IDT7243L120FB		F64	
IDT7243L165P	165	P64	Com'l.
IDT7243L165J		J68	
IDT7243L165C		D64	
IDT7243L165XC		D68	
IDT7243L165L		L68-1	
IDT7243L165XL		L68-2	
IDT7243L165F		F64	
IDT7243L200CB	200	D64	Mil.
IDT7243L200XCB		D68	
IDT7243L200LB		L68-1	
IDT7243L200XLB		L68-2	
IDT7243L200FB		F64	



Integrated
Device
Technology

Technology Capabilities

FIFO/ RAM

Microprocessor

Digital Signal Processing (DSP)

Logic

5

Data Conversion

Subsystems Modules

Support Product Information

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Logic (CONT'D.)

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT39C821-26

FEATURES:

- Equivalent to AMD's Am29821-26 Bipolar Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  —Non-inverting CP-Y t_{PD} = 7.5ns typ.
  —Inverting CP-Y t_{PD} = 7.5ns typ.
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on clock INPUT
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
  —6pF inputs (typ.)
  —8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's Bipolar Am29800 series (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available.

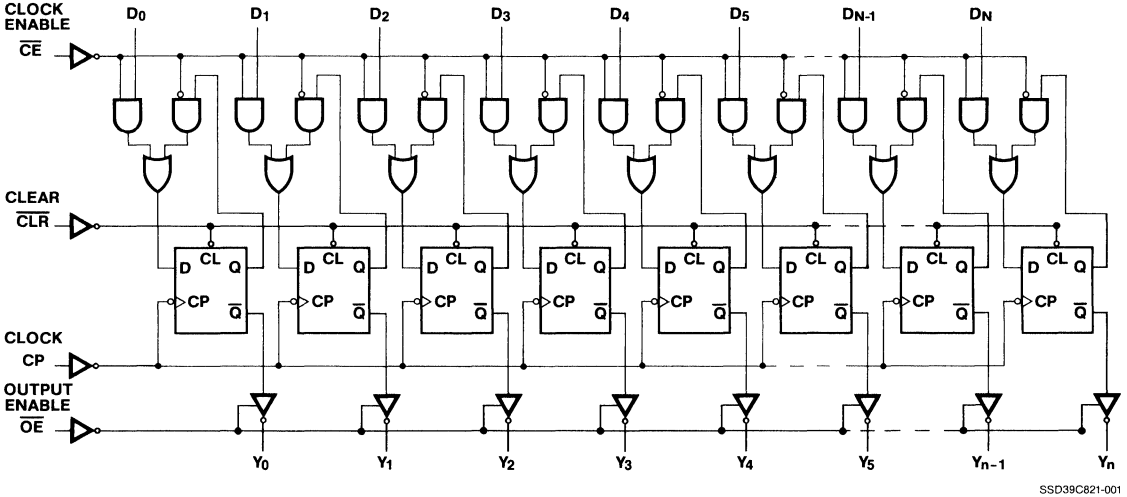
DESCRIPTION:

The IDT39C800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT39C820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT39C821 and IDT39C822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The IDT39C823 and IDT39C824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT39C825 and IDT39C826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

cAll of the IDT39C800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



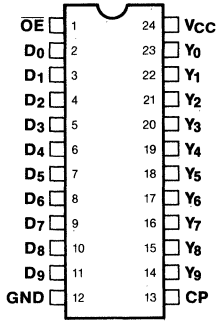
SSD39C821-001

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

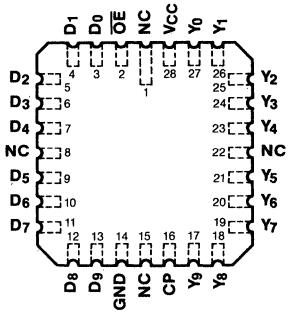
LOGIC SYMBOLS

IDT39C821/IDT39C822 10-BIT REGISTERS



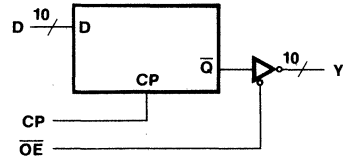
DIP
TOP VIEW

SSD39C821-005



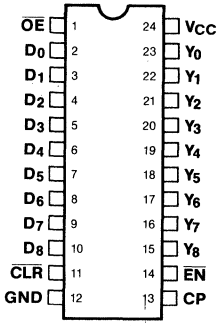
LCC
TOP VIEW

SSD39C821-006



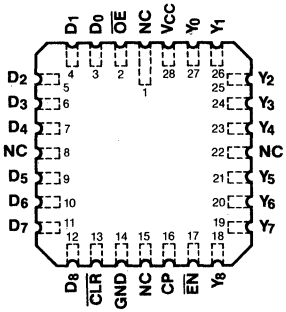
SSD39C821-002

IDT39C823/IDT39C824 9-BIT REGISTERS



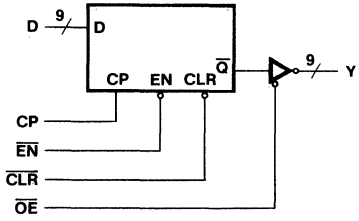
DIP
TOP VIEW

SSD39C821-007



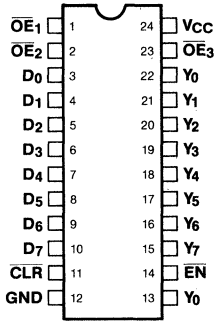
LCC
TOP VIEW

SSD39C821-008



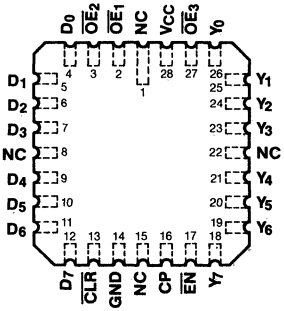
SSD39C821-003

IDT39C825/IDT39C826 8-BIT REGISTERS



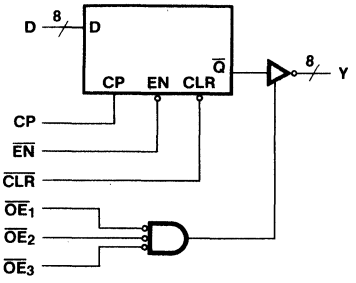
DIP
TOP VIEW

SSD39C821-009



LCC
TOP VIEW

SSD39C821-010



SSD39C821-004

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D_i	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and noninverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_i, $\overline{Y}_i$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

PRODUCT SELECTOR GUIDE

	DEVICE		
	10-BIT	9-BIT	8-BIT
Noninverting	IDT39C821	IDT39C823	IDT39C825
Inverting	IDT39C822	IDT39C824	IDT39C826

FUNCTION TABLES

IDT39C821/23/25

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i	
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

IDT39C822/24/26

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	$\overline{Y}_i$	
H	X	L	L	↑	H	Z	Hi-Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

5

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)

T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on Clock Only	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50pF R_L = 500Ω	—	12	—	12	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	20	—	20	ns
t_S	Data to CP Setup Time		C_L = 50pF R_L = 500Ω	4		4		ns
t_H	Data to CP Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			4		4		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			4		4		ns
t_H	Enable ($\overline{EN}$) Hold Time			2		2		ns
t_{PHL}	Propagation Delay, Clear to Y_i				20		20	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time			7		7		ns
t_{PWH}	Clock Pulse Width	HIGH		7		7		ns
t_{PWL}		LOW		7		7		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			7		7		ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300pF R_L = 500Ω		23		25	ns
t_{ZH} t_{ZL}			C_L = 50pF R_L = 500Ω		14		15	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50pF R_L = 500Ω		16		18	ns
t_{HZ}[2] t_{LZ}			C_L = 5pF R_L = 500Ω		9		10	ns

NOTE:
1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT39C841-46

FEATURES:

- Equivalent to AMD's Am29841-46 Bipolar Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  —Noninverting transparent t_{PD} = 5.5ns typ.
  —Inverting transparent t_{PD} = 6.0ns typ.
- Buffered common latch enable, clear and preset input
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on latch enable input
- Clamp diodes on all inputs for ringing supression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
  —6pF inputs (typ.)
  —8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's Bipolar Am29800 Series (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available

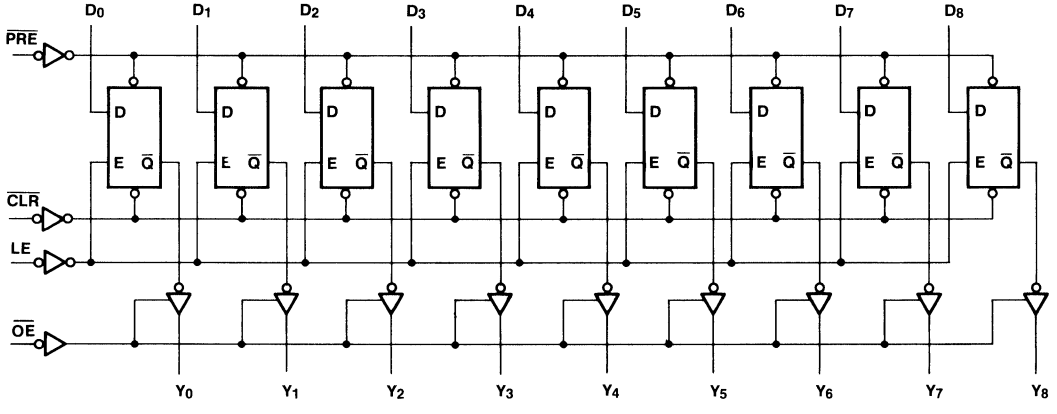
DESCRIPTION:

The IDT39C800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT39C840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT39C841 and IDT39C842 are buffered, 10-bit wide versions of the popular '373 function. The IDT39C843 and IDT39C844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance systems. The IDT39C845 and IDT39C846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT39C800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



DSR39C841-001

PRODUCT SELECTOR GUIDE

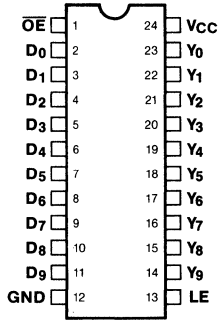
	DEVICE		
	10-BIT	**9-BIT**	**8-BIT**
Noninverting	IDT39C841	IDT39C843	IDT39C845
Inverting	IDT39C842	IDT39C844	IDT39C846

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

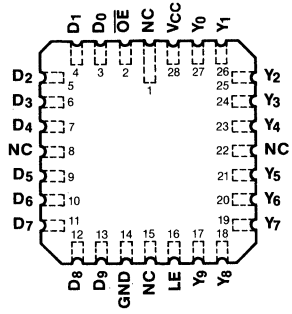
LOGIC SYMBOLS

IDT39C841/IDT39C842 10-BIT LATCHES



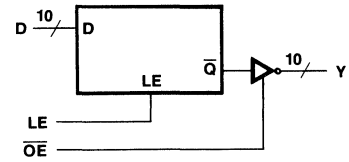
DIP
TOP VIEW

DSR39C841-005



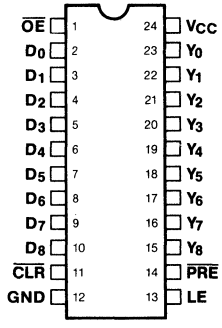
LCC
TOP VIEW

DSR39C841-006



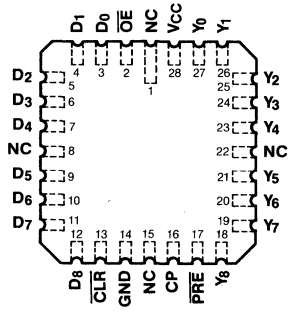
DSR39C841-002

IDT39C843/IDT39C844 9-BIT LATCHES



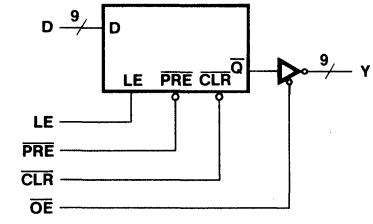
DIP
TOP VIEW

DSR39C841-007



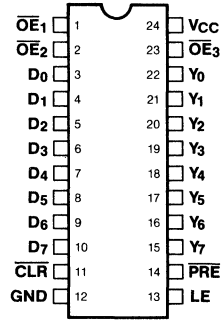
LCC
TOP VIEW

DSR39C841-008



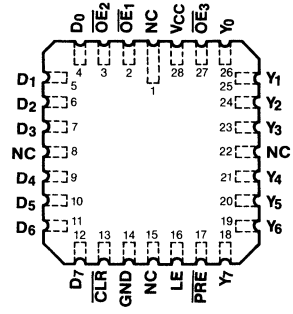
DSR39C841-003

IDT39C845/IDT39C846 8-BIT LATCHES



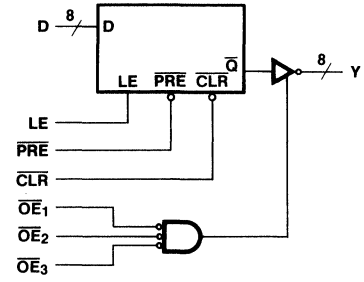
DIP
TOP VIEW

DSR39C841-009



LCC
TOP VIEW

DSR39C841-010



DSR39C841-004

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT39C841/43/45 (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_i	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
IDT39C842/44/46 (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_i	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

IDT39C841/43/45

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

IDT39C842/44/46

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

5

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS *may cause permanent damage to the device.* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)

T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA	2.4	4.0	—	
			I_{OH} = -24mA COM'L.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM'L.	—	—	0.5	
V_H	Input Hysteresis on LE	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} (IDT39C841, 43, 45) t_{PHL}	Data (D_i) to Output (Y_i) (LE = HIGH)		C_L = 50pF R_L = 500Ω	—	9.5	—	11	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	13	—	15	ns
t_S	Data to LE Setup Time		C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time			2.5	—	3	—	ns
t_{PLH} (IDT39C842, 44, 46) t_{PHL}	Data (D_i) to Output (Y_i) (LE = HIGH)		C_L = 50pF R_L = 500Ω	—	10	—	12	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	13	—	15	ns
t_S	Data to LE Setup Time		C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time			2.5	—	3	—	ns
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_i		C_L = 50pF R_L = 500Ω	—	12	—	16	ns
t_{PLH} t_{PHL}			C_L = 300 pF R_L = 500Ω	—	16	—	20	ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50pF R_L = 500Ω	—	12	—	14	ns
t_S	Preset Recovery ($\overline{PRE}$ ⎍) Time			—	14	—	17	ns
t_{PHL}	Propagation Delay, Clear to Y_i			—	13	—	15	ns
t_S	Clear Recovery ($\overline{CLR}$ ⎍) Time			—	14	—	17	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF R_L = 500Ω	6	—	6	—	ns
t_{PWL}	Preset Pulse Width	LOW		8	—	9	—	ns
t_{PWL}	Clear Pulse Width	LOW		8	—	9	—	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ ⎍ to Y_i		C_L = 300pF R_L = 500Ω	—	23	—	25	ns
t_{ZH} t_{ZL}			C_L = 50pF R_L = 500Ω	—	14	—	15	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ ⎍ to Y_i		C_L = 50pF R_L = 500Ω	—	12	—	12	ns
t_{HZ}[2] t_{LZ}			C_L = 5pF R_L = 500Ω	—	9	—	10	ns

NOTE:
1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT39C861-64

FEATURES:

- Equivalent to AMD's Am29861-64 Bipolar Registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed symmetrical bidirectional transceivers
  —Noninverting t_{PD} = 5.5ns typ.
  —Inverting t_{PD} = 6.0ns typ.
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on T and R buses
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's Bipolar Am29800 series (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available.

DESCRIPTION:

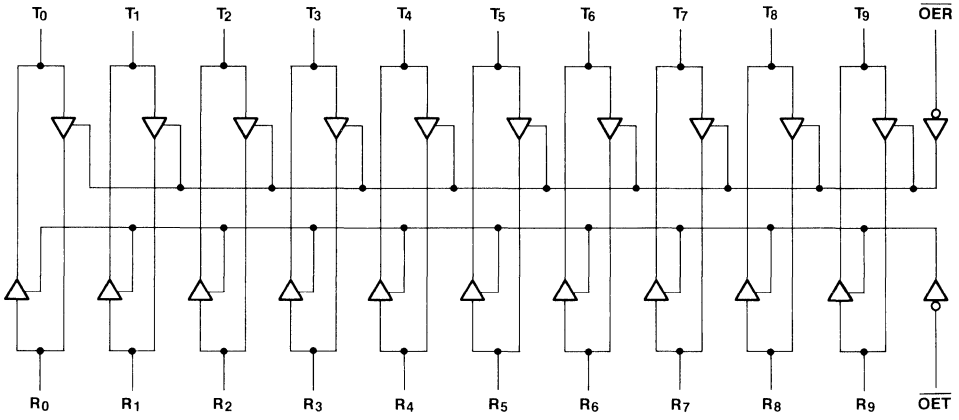
The IDT39C800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT39C860 Series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT39C863/64 9-bit transceivers have NOR-ed output enables for maximum control flexibility.

All of the IDT39C800 high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT39C861/IDT39C862 10-BIT TRANSCEIVERS



SSD39C861-001

PRODUCT SELECTOR GUIDE

	DEVICE	
	10-BIT	**9-BIT**
Noninverting	IDT39C861	IDT39C863
Inverting	IDT39C862	IDT39C864

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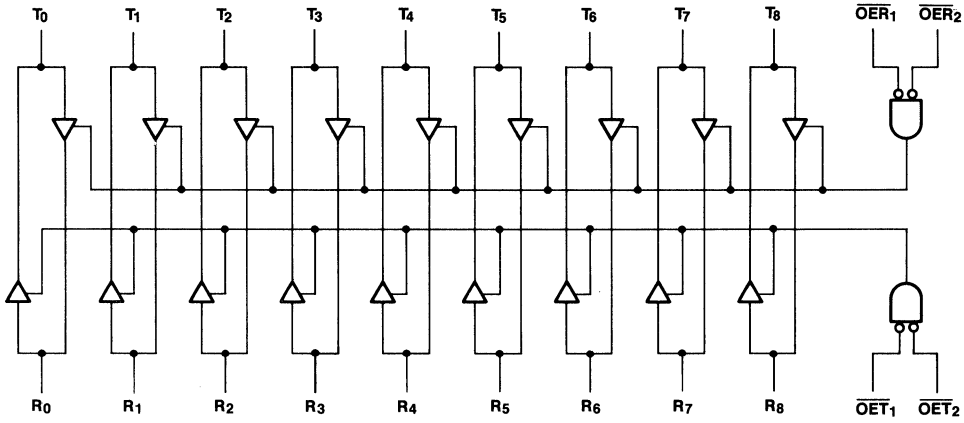
Printed in U.S.A.

FUNCTIONAL BLOCK DIAGRAM

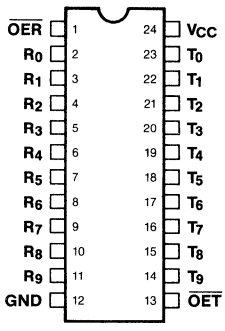
IDT39C863/IDT39C864 9-BIT TRANSCEIVERS



SSD39C861-004

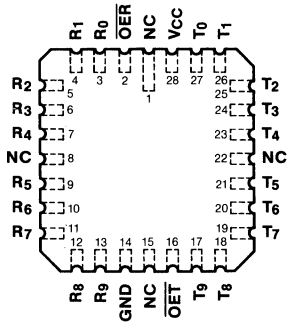
PIN CONFIGURATIONS

IDT39C861/IDT39C862 10-BIT TRANSCEIVERS



DIP
TOP VIEW

SSD39C861-005

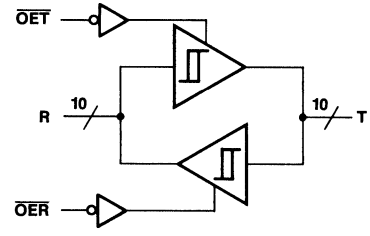


LCC
TOP VIEW

SSD39C861-006

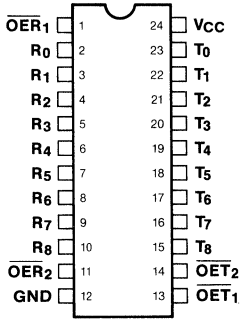
LOGIC SYMBOLS

IDT39C861



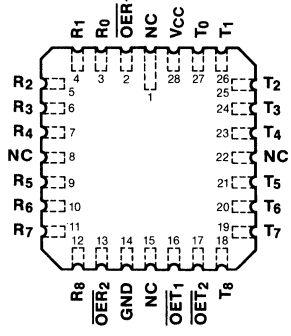
SSD39C8610-002

IDT39C863/IDT39C864 9-BIT TRANSCEIVERS



DIP
TOP VIEW

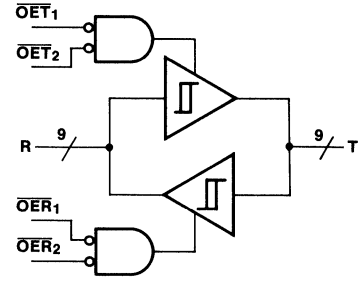
SSD39C861-007



LCC
TOP VIEW

SSD39C861-008

IDT39C863



SSD39C861-003

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT39C861/62		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
R_i	I/O	10-bit RECEIVE input/output.
T_i	I/O	10-bit TRANSMIT input/output.
IDT39C863/64		
$\overline{OER}_i$	I	When LOW in conjunction with $\overline{OET}_i$ HIGH activates the RECEIVE mode.
$\overline{OET}_i$	I	When LOW in conjunction with $\overline{OER}_i$ HIGH activates the TRANSMIT mode.
R_i	I/O	9-bit RECEIVE input/output.
T_i	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLES

IDT39C861/IDT39C863 (Noninverting)

INPUTS				OUTPUTS		FUNCTION
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

IDT39C862/IDT39C864 (Inverting)

INPUTS				OUTPUTS		FUNCTION
$\overline{OET}$	$\overline{OER}$	R_i	$\overline{T}_i$	R_i	$\overline{T}_i$	
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

5

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)

T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on R_i and T_i	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION	TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from R_i to T_i or T_i to R_i IDT39C861/IDT39C863 (Noninverting)	C_L = 50pF R_L = 500Ω	—	8	—	10	ns
t_{PLH} t_{PHL}		C_L = 300pF R_L = 500Ω	—	15	—	17	ns
t_{PLH} t_{PHL}	Propagation Delay from R_i to T_i or T_i to R_i IDT39C862/IDT39C864 (Inverting)	C_L = 50pF R_L = 500Ω	—	7.5	—	9.5	ns
t_{PLH} t_{PHL}		C_L = 300pF R_L = 500Ω	—	14	—	16	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 50pF R_L = 500Ω	—	15	—	17	ns
t_{ZH} t_{ZL}		C_L = 300pF R_L = 500Ω	—	20	—	22	ns
t_{ZH}[2] t_{ZL}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 5pF R_L = 500Ω	—	9	—	10	ns
t_{ZH} t_{ZL}		C_L = 50pF R_L = 500Ω	—	17	—	19	ns

NOTE:

1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTER WITH SPC™
(Serial Protocol Channel)

ADVANCE INFORMATION
IDT49C818

FEATURES:

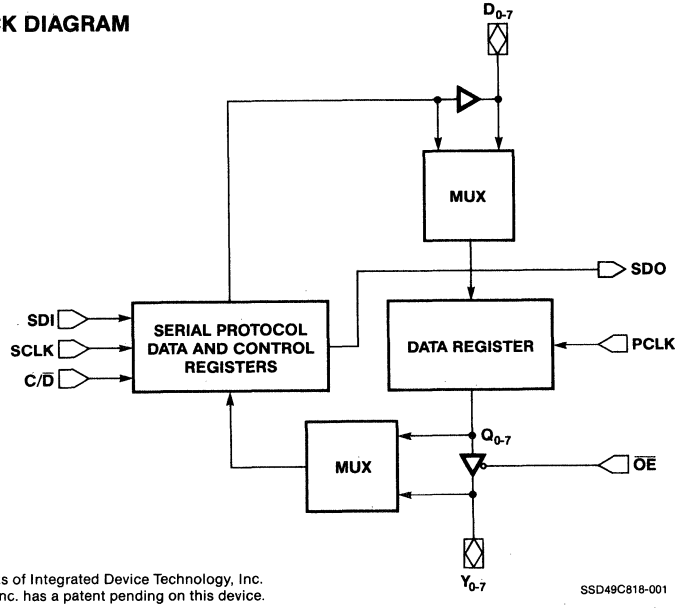
- High-speed non-inverting 8-bit parallel register for any data path, control path or pipelining application
- Pin-out similar to the Am29818 and 54/74S818, but uses an improved protocol for the serial interface
- New, unique command capability which allows for multiplicity of diagnostic functions
- High-speed Serial Protocol Channel (SPC) which provides access to octal data register using four pins
- Controllability
  - —Serial scan of new machine state
  - —Form temporary connections between D and Y buses
  - —Load new machine state "on the fly" synchronous with PCLK
  - —Temporarily force Y output bus
  - —Temporarily force data out the D input bus (as in loading Writeable Control Store — WCS)
- Observability
  - —Directly observe D and Y buses
  - —Serial scan out current machine state
  - —Capture machine state "on the fly" synchronous with PCLK
  - —WCS pipeline register
  - —Load WCS from serial input
  - —Read WCS via serial scan
- Ideal for diagnostic scan testing

DESCRIPTION:

The IDT49C818 is a high-speed, general-purpose octal register with a Serial Protocol Channel (SPC). The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required. The IDT49C818 is pin-out similar to the 29818 and 54/74S818, but uses the serial data, clock and mode pins as SPC to communicate with the serial command and data registers.

The command and data registers are used to observe and control the operation of the octal data registers. The serial command and data registers can be accessed while the system is performing normal system function. Diagnostic operations then can be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in (SDI) and data out (SDO) pins which can participate in a serial scan loop throughout the system where normal data, address, status and control registers are replaced with the IDT49C818. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results. An "oscilloscope mode" can be achieved by loading data from the SPC serial data register into the octal data register synchronous to the system clock (PCLK) using a diagnostic command which transfers data synchronously. When repeated every Nth clock, the repeating states of the system can be observed on an oscilloscope. When used as a pipeline register, WCS loading can be accomplished by scanning in data through the SPC port and enabling the data onto the D bus pins.

FUNCTIONAL BLOCK DIAGRAM

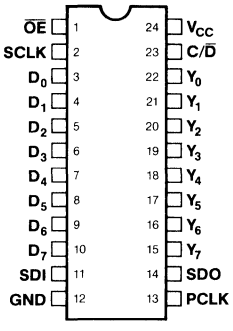


SSD49C818-001

CEMOS and SPC are trademarks of Integrated Device Technology, Inc.
Integrated Device Technology, Inc. has a patent pending on this device.

Printed in U.S.A.

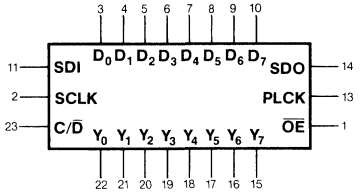
PIN CONFIGURATION



DIP
TOP VIEW

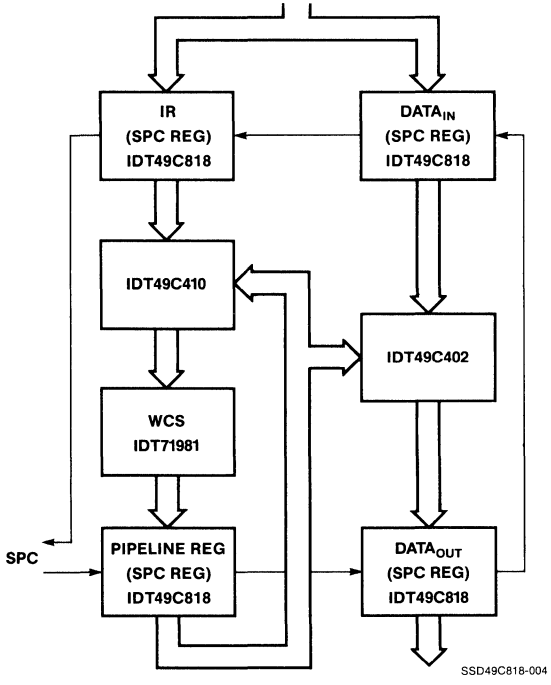
SSD49C818-002

LOGIC SYMBOL



SSD49C818-003

TYPICAL MICROPROGRAM APPLICATION



SSD49C818-004

5

Integrated Device Technology, Inc.

HIGH-SPEED CMOS 1-of-8 DECODER

IDT54/74AHCT138

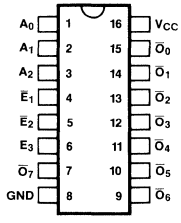
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 1-of-8 decoder with enables
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

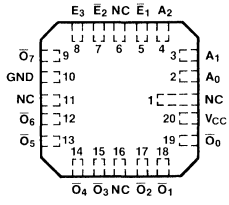
The IDT54/74AHCT138 are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT138 accepts three binary weighed inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74AHCT138 features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outpus will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74AHCT138 devices and one inverter.

PIN CONFIGURATIONS



SSD54/74AHCT138-001

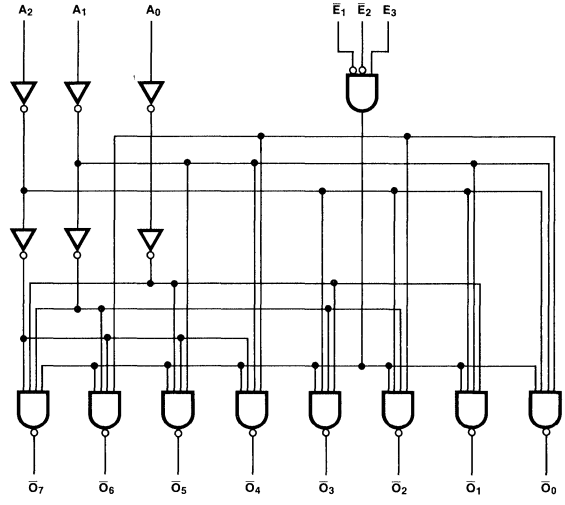
DIP
TOP VIEW



SSD54/74AHCT138-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT138-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.04	1.6	
			V_{IN} = 3.4V or V_{IN} = GND	—	0.3	2.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	O_0	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N to $\overline{O}_N$	C_L = 50 pf R_L = 500 Ω	11.0	6.0	22.0	6.0	27.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_N$		13.0	4.0	17.0	4.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_N$		13.0	4.0	17.0	4.0	20.0	ns

5

Integrated Device Technology, Inc.

HIGH-SPEED CMOS DUAL 1-OF-4 DECODER

IDT54/74AHCT139

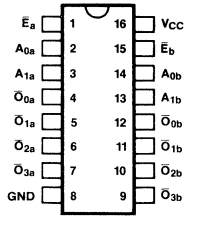
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Dual 1-of-4 decoder with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

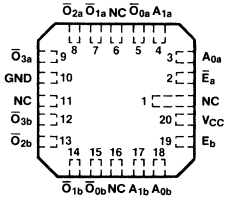
The IDT54/74AHCT139 are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. The device has two independent decoders, each of which accept two binary weighed inputs (A_0-A_1) and provides four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS



SSD54/74AHCT139-001

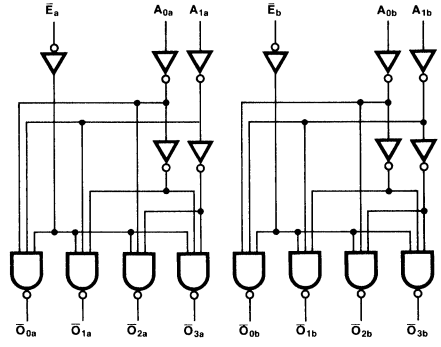
DIP
TOP VIEW



SSD54/74AHCT139-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT139-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Input Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle One Input Toggling on Each Decoder	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.1	
			V_{IN} = 3.4V V_{IN} = GND	—	0.8	3.7	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_N$	C_L = 50 pf R_L = 500 Ω	9.0	5.0	20.0	5.0	25.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_N$		11.0	5.0	15.0	5.0	18.0	ns

Integrated Device Technology, Inc

HIGH-SPEED CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74AHCT161/163

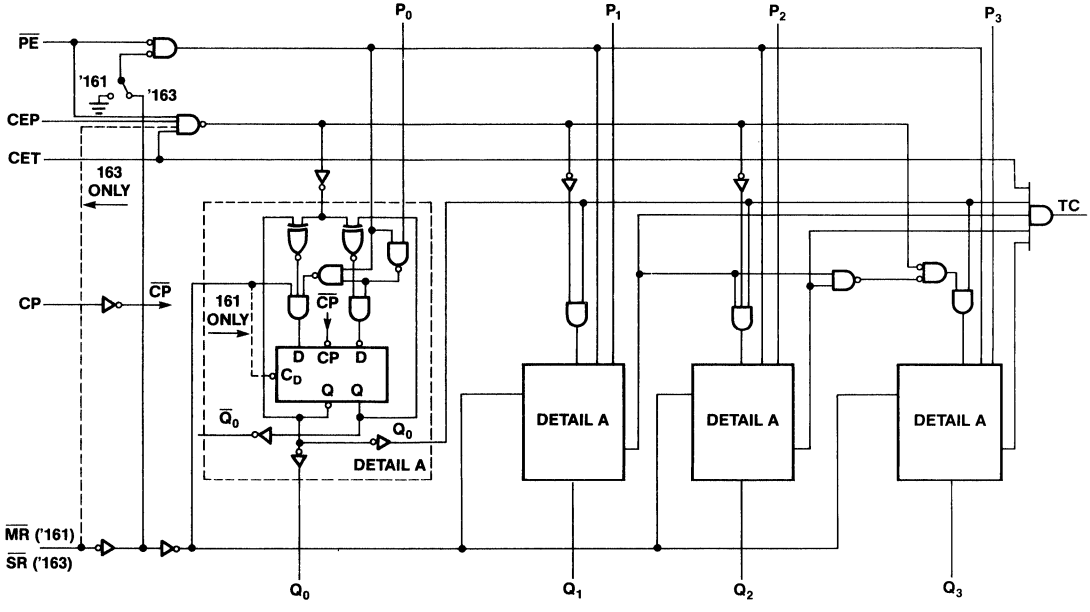
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μ max)
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT161/163 are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The IDT54/74AHCT161/163 have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74AHCT161/163 have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



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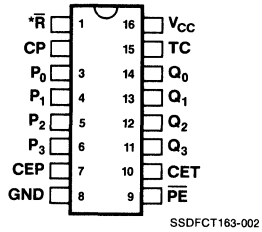
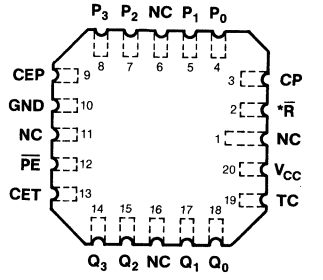
PIN CONFIGURATIONS



SSDFCT163-002

DIP
TOP VIEW



SSDFCT163-003

LCC
TOP VIEW

***MR FOR '161**
***SR FOR '163**

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150μA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25° C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS (IDT54/74AHCT161)

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Mode $\overline{CEP} = CET = \overline{MR} = \overline{PE} = V_{HC}$ $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle Count Mode $\overline{CEP} = CET = \overline{MR} = \overline{PE} = V_{HC}$ $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA
			CP V_{IN} = 3.4V or V_{IN} = GND	—	1.1	—	

POWER SUPPLY CHARACTERISTICS (IDT54/74AHCT163)

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Mode $\overline{CEP} = CET = \overline{SR} = \overline{PE} = V_{HC}$ $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle Count Mode $\overline{CEP} = CET = \overline{SR} = \overline{PE} = V_{HC}$ $P_{0-3} = V_{LC}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.1	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP} + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   f_i = P_{0-3} Input Frequency (Load)
   N_i = Number of P_{0-3} Inputs at f_i (Load)
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

TRUTH TABLE

$\overline{SR}$(1)	$\overline{PE}$	CET	CEP	ACTION ON THE RISING CLOCK EDGE (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:

1. For AHCT163 only

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	MILITARY		COMMERCIAL		UNITS
				MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n($\overline{PE}$ Input HIGH)	C_L = 50pF R_L = 500Ω	12.0	4.0	20.0	3.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)		12.0	4.0	20.0	3.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		18.0	5.0	30.0	5.0	26.0	ns
t_{PHL} t_{PHL}	Propagation Delay CET to TC		10.0	3.0	16.0	3.0	13.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (161)		10.0	6.0	27.0	6.0	24.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC		10.0	6.0	31.0	6.0	28.0	ns
t_S(H) t_S(L)	Setup Time, HIGH or LOW P_n to CP		—	20.0	—	15.0	—	ns
t_H(H) t_H(L)	Hold Time, HIGH or LOW P_n to CP		—	0	—	0	—	ns
t_S(H) t_S(L)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		—	20.0	—	15.0	—	ns
t_H(H) t_H(L)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		—	0	—	0	—	ns
t_S(H) t_S(L)	Setup Time, HIGH or LOW CEP or CET to CP		—	25.0	—	20.0	—	ns
t_H(H) t_H(L)	Setup Time, HIGH or LOW CEP to CET to CP		—	0	—	0	—	ns
t_W(H) t_W(L)	Clock Pulse Width (Load) HIGH or LOW		—	20.0	—	15.0	—	ns
t_W(H) t_W(L)	Clock Pulse Width (Count) HIGH or LOW		—	20.0	—	15.0	—	ns
t_W(L)	$\overline{MR}$ Pulse Width, LOW (161)		—	20.0	—	15.0	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP (161)		—	20.0	—	15.0	—	ns

HIGH-SPEED CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74AHCT182

Integrated Device Technology, Inc.

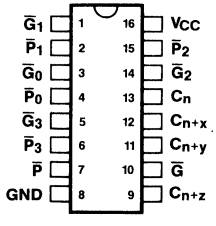
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Carry lookahead generator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

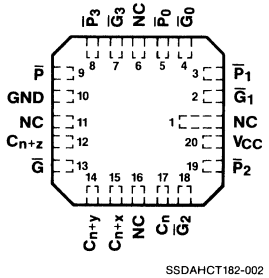
The IDT54/74AHCT182 is a carry lookahead generator built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT182 is generally used with a 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

PIN CONFIGURATIONS



SSDAHCT182-001

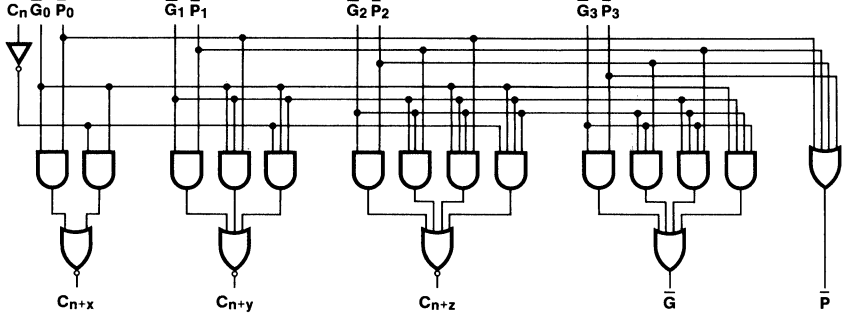
DIP
TOP VIEW



SSDAHCT182-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT182-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)
$\overline{G}_1$	Carry Generate Input (Active LOW)
$\overline{G}_3$	Carry Generate Input (Active LOW)
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)
$\overline{P}_2$	Carry Propagate Input (Active LOW)
$\overline{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x}–C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	H	H	H	H					L		
X	X	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	L	H	L					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	X		L	X	L	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_N to C_{N+X}, C_{N+Y}, C_{N+Z}	C_L = 50 pf R_L = 500Ω	8.0	—	18.0	—	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		8.0	—	13.0	—	15.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, or $\overline{G}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		8.0	—	13.5	—	15.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, or $\overline{P}_3$, to $\overline{G}$		9.0	—	16.0	—	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_N$ to $\overline{G}$		9.5	—	16.0	—	20.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_N$ to $\overline{P}$		8.0	—	15.0	—	16.5	ns

Integrated Device Technology, Inc

HIGH-SPEED CMOS UP/DOWN BINARY COUNTER

IDT54/74AHCT191

FEATURES:

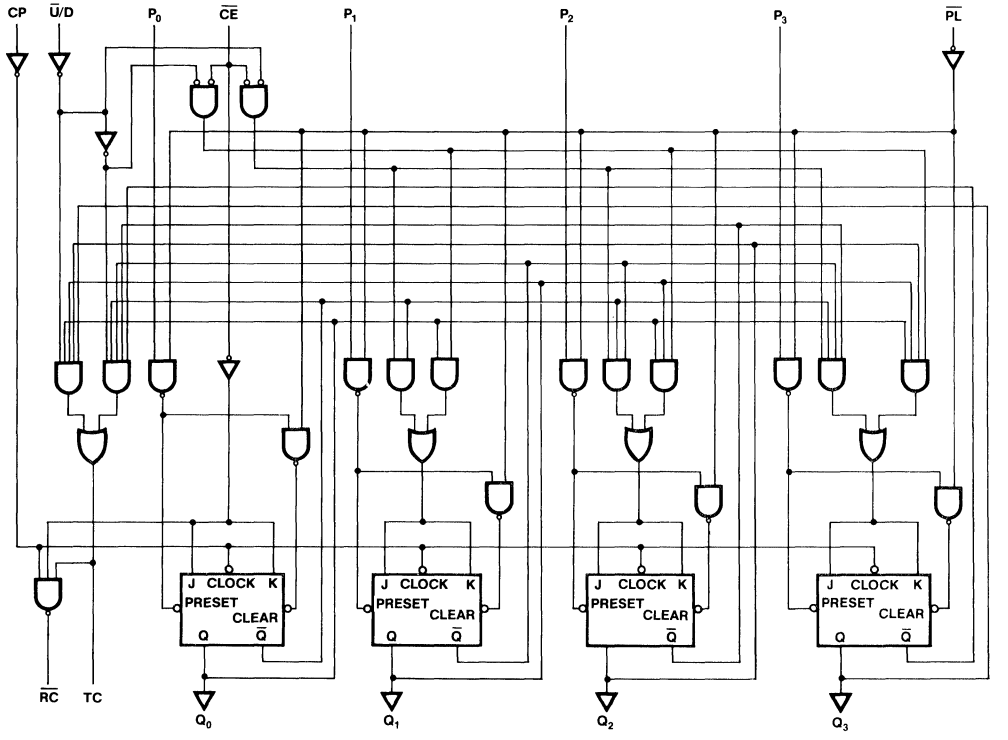
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μ max.)
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT191 is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting, built using advanced CEMOS™, a dual metal CMOS technology.

The preset feature allows the IDT54/74AHCT191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



SSDFCT191-001

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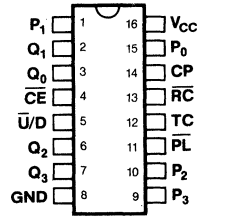
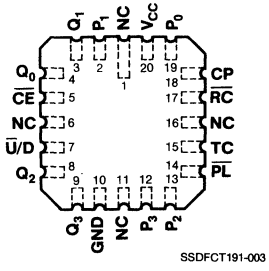
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Up or Down $\overline{CE} = V_{LC}$ $\overline{PL} = P_0 - P_3 = V_{HC}$ $\overline{U}/D = V_{HC}$ or V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle Count Up or Down $\overline{CE} = V_{LC}$ $\overline{PL} = P_0 - P_3 = V_{HC}$ $\overline{U}/D = V_{HC}$ or V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.1	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output shold be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP} + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   $f_i = P_{0-3}$ Input Frequency (Load)
   N_i = Number of P_{0-3} Inputs at f_i (Load)
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Count Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Clock Output (Active HIGH)

RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC(1)	CP	$\overline{RC}$
L	H		
H	X	X	H
X	L	X	H

NOTES:

1. TC is generated internally.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

TRUTH TABLES
MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Preset (Asynch.)
H	H	X	X	No Change (Hold)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN..	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	—	3.0	18.0	3.0	22.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		—	6.0	31.0	6.0	34.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		—	5.0	20.0	4.0	24.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		—	4.0	18.0	4.0	21.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$		—	6.0	25.0	6.0	30.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}/D$ to TC		—	6.0	25.0	6.0	30.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		—	4.0	21.0	4.0	25.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		—	6.0	30.0	6.0	34.0	ns
$t_S(H)$ $t_S(L)$	Setup Time HIGH or LOW P_n to $\overline{PL}$		—	20.0	—	25.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW P_n to $\overline{PL}$		—	5.0	—	5.0	—	ns
$t_S(L)$	Setup Time LOW $\overline{CE}$ to CP		—	20.0	—	25.0	—	
$t_H(L)$	Hold Time LOW $\overline{CE}$ to CP		—	0	—	0	—	
$t_S(H)$ $t_S(L)$	Setup Time HIGH or LOW $\overline{U}/D$ to CP		—	20.0	—	20.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW $\overline{U}/D$ to CP		—	0	—	0	—	ns
$t_W(L)$	$\overline{PL}$ Pulse Width LOW		—	20.0	—	25.0	—	ns
$t_W(L)$	CP Pulse Width LOW		—	15.0	—	20.0	—	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP		—	15.0	—	20.0	—	ns

Integrated Device Technology Inc

HIGH-SPEED CMOS UP/DOWN BINARY COUNTER

IDT54/74AHCT193

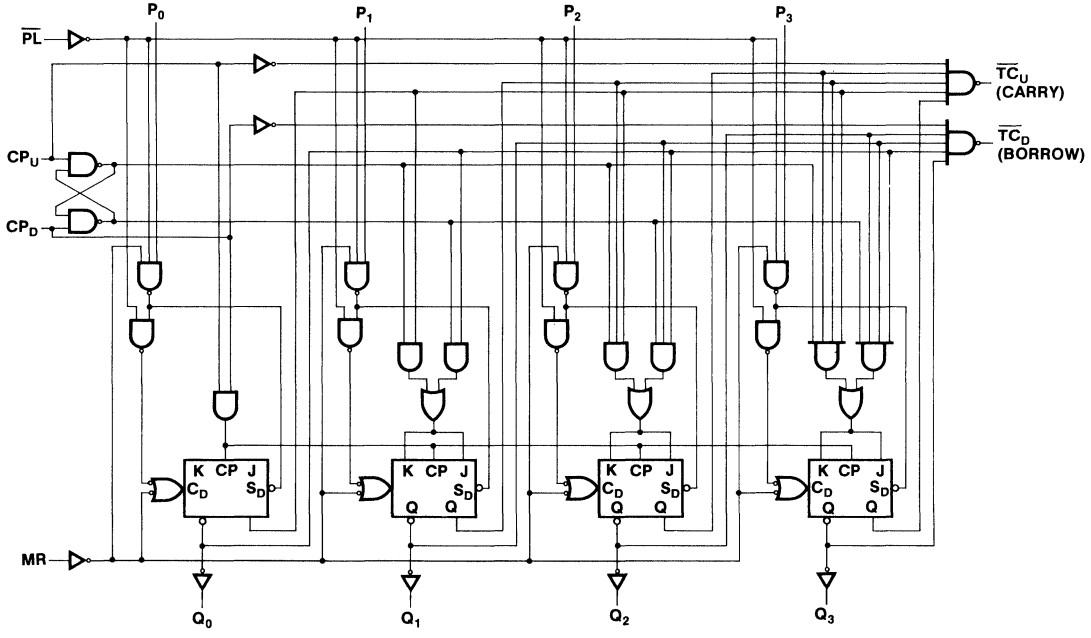
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μ max.)
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT193 is an up/down modulo-16 binary counter built using advanced CEMOS™, a dual metal CMOS technology. Separate Count-up and Count-down Clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count-up and Terminal Count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset ($\overline{MR}$) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM



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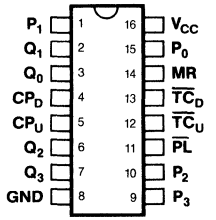
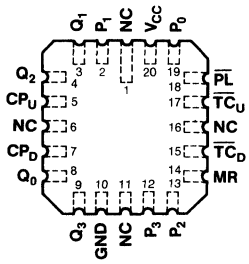
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = –55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	–5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		–60	–100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –150µA	V_{HC}	V_{CC}	—	
			I_{OH} = –1.0mA MIL.	2.4	4.3	—	
			I_{OH} = –2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP_U} = f_{CP_D} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ MR = V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ MR = V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	—	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.1	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP} + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   f_i = P_{0-3} Input Frequency (Load)
   N_i = Number of P_{0-3} Inputs at f_i (Load)
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P_{0-3}	Parallel Data Inputs
Q_{0-3}	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↓	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN..	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	C_L = 50pF R_L = 500Ω	—	4.0	16.0	4.0	19.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		—	4.0	17.0	4.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		—	4.0	17.0	4.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		—	6.0	28.0	6.0	31.0	ns
t_{PHL}	Propagation Delay MR to Q_n		—	6.0	28.0	6.0	31.0	ns
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		—	6.0	28.0	6.0	31.0	ns
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		—	6.0	28.0	6.0	31.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$		—	6.0	28.0	6.0	31.0	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		—	4.0	17.0	4.0	20.0	ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$		—	20.0	—	25.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$		—	5.0	—	5.0	—	ns
$t_W(L)$	$\overline{PL}$ Pulse Width, LOW		—	20.0	—	25.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW		—	15.0	—	20.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)		—	15.0	—	20.0	—	ns
$t_W(H)$	MR Pulse Width, HIGH		—	10.0	—	10.0	—	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP_U or CP_D		—	15.0	—	20.0	—	ns
t_{REC}	Recovery Time MR to CP_U or CP_D		—	15.0	—	20.0	—	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74AHCT240

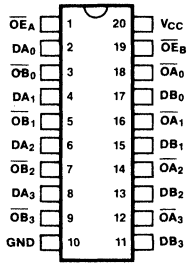
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 7ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT240 is an octal buffer/line driver built using advanced CEMOS™, a dual metal CMOS technology. The device is designed to be employed as a memory and address driver, clock driver and bus-oriented transmitter/receiver which provides improved board density.

PIN CONFIGURATION



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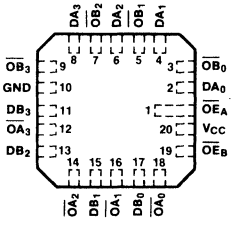
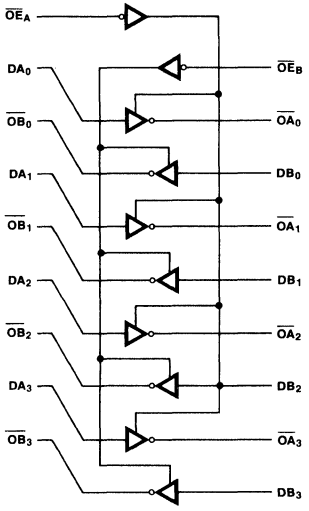
DIP
TOP VIEW



SSDAHCT240-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT240-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250KHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	7.0	2.0	9.0	2.0	12.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	18.0	5.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		10.0	2.0	12.0	2.0	18.0	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74AHCT244

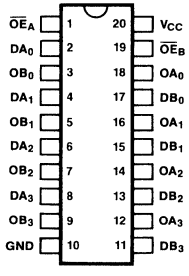
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 7ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

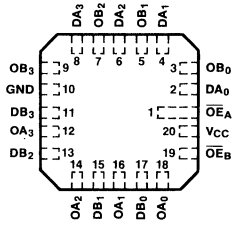
The IDT54/74AHCT244 are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved board density.

PIN CONFIGURATIONS



SSD54/74AHCT244-001

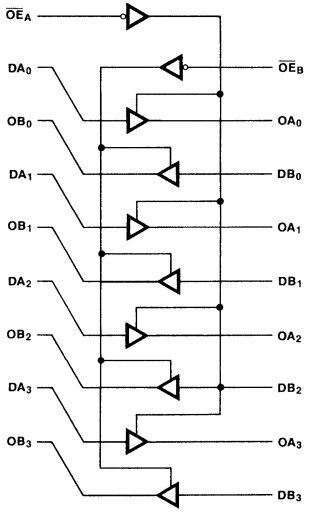
DIP
TOP VIEW



SSD54/74AHCT244-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT244-003

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CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pf R_L = 500Ω	7.0	3.0	10.0	3.0	13.0	ns
t_{ZH} t_{ZL}	Output Enable Time		16.0	7.0	20.0	7.0	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		10.0	2.0	13.0	2.0	18.0	ns

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Integrated Device Technology, Inc.

HIGH-SPEED CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74AHCT245

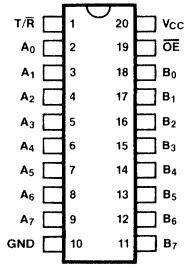
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical data to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

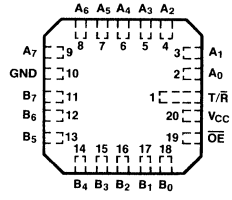
The IDT54/74AHCT245 are 8-bit non-inverting, bidirectional buffers built using advanced CEMOS™, a dual metal CMOS technology. This bidirectional buffer has 3-state outputs and is intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in High Z condition.

PIN CONFIGURATIONS



SSD54/74AHCT245-001

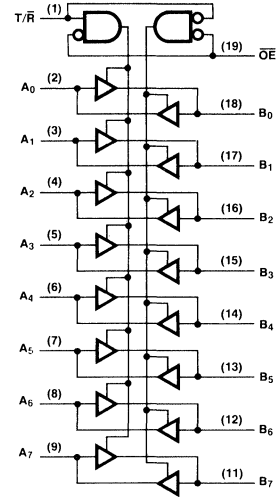
DIP
TOP VIEW



SSD54/74AHCT245-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT245-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage Port A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage Port A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B B to B	C_L = 50 pf R_L = 500Ω	8.0	3.0	10.0	3.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	15.0	2.0	18.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		14.0	—	—	—	—	ns

*Guaranteed by Design

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT54/74AHCT273

FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with clear
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

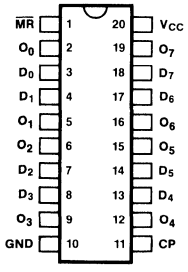
DESCRIPTION:

The IDT54/74AHCT273 are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT273 has eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

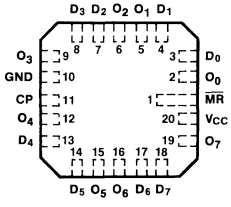
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS



SSD54/74AHCT273-001

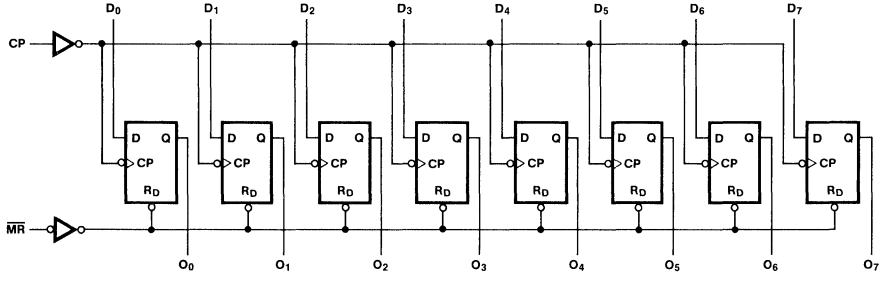
DIP
TOP VIEW



SSD54/74AHCT273-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT273-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{MR} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{MR} = V_{CC}$ One Bit Toggling at f_i = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{MR} = V_{CC}$ Eight Bits Toggling f_i = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_0-O_7	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load '1'	H	↑	h	H
Load '0'	H	↑	l	L

H = HIGH Voltage steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
X = Don't Care
↑ = LOW-to-HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500Ω	10.0	3.0	15.0	3.0	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output		12.0	4.0	18.0	4.0	21.0	ns
t_S	Set Up Time High or Low Data to CP		3.0	10.0	—	10.0	—	ns
t_H	Hold Time High or Low Data to CP		0.6	1.0	—	1.0	—	ns
t_W	Clock Pulse Width High or Low		10.0	16.0	—	16.0	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		5.0	15.0	—	15.0	—	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74AHCT299

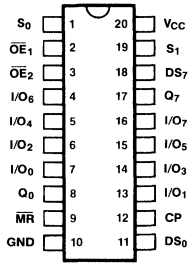
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-input universal shift register
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

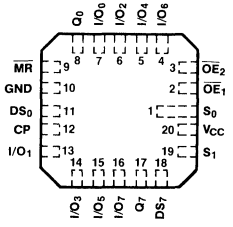
The IDT54/74AHCT299 is an 8-bit universal shift register built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0-Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS



SSDFCT299-001

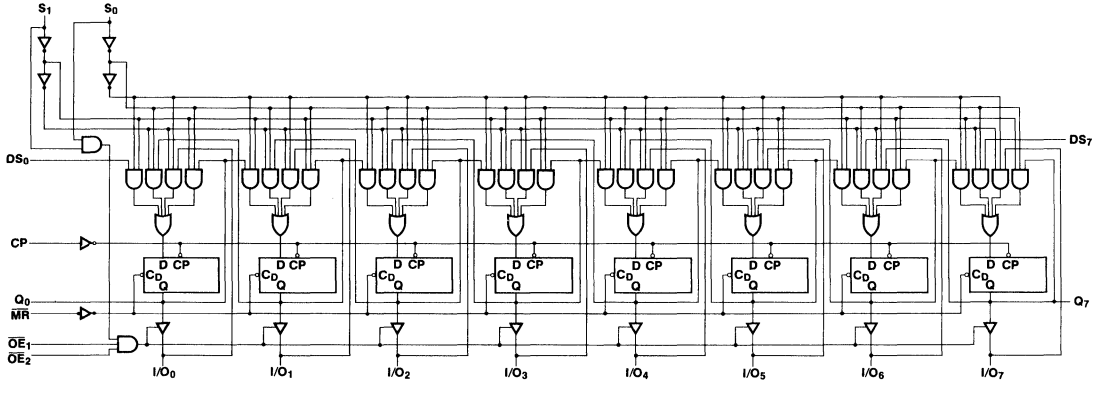
DIP
TOP VIEW



SSDFCT299-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT299-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -200µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND One Bit Toggling at f_i = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND Eight Bits Toggling at f_i = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Rising Edge)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌠	Parallel Load; $I/O_N \rightarrow Q_N$
H	L	H	⌠	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌠	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50 pf R_L = 500 Ω	9.0	3.5	13.0	—	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_N		8.0	4.0	15.0	—	15.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		9.0	4.5	13.0	—	15.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_N		9.0	6.5	15.0	—	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ to I/O_N		10.0	3.5	14.0	—	18.0	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ to I/O_N		7.5	2.0	10.0	—	12.0	ns
t_S	Setup Time HIGH or LOW S_0 or S_1 to CP		4.0	8.5	—	8.5	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	1.0	—	1.0	—	ns
t_S	Setup Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		1.5	5.5	—	5.5	—	ns
t_H	Hold Time HIGH or LOW I/O_N, DS_0 or DS_7 to CP		0	3.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		8.0	8.0	—	8.0	—	ns
t_W	$\overline{MR}$ Pulse Width Low		8.0	8.0	—	8.0	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		8.0	8.0	—	8.0	—	ns

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH

IDT54/74AHCT373

Integrated Device Technology, Inc.

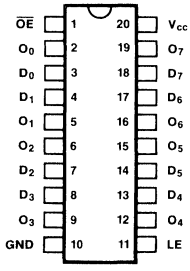
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

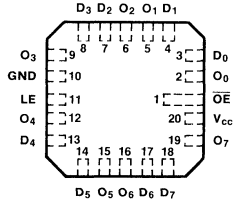
The IDT54/74AHCT373 are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. This octal latch has 3-state output and is intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSD54/74AHCT373-001

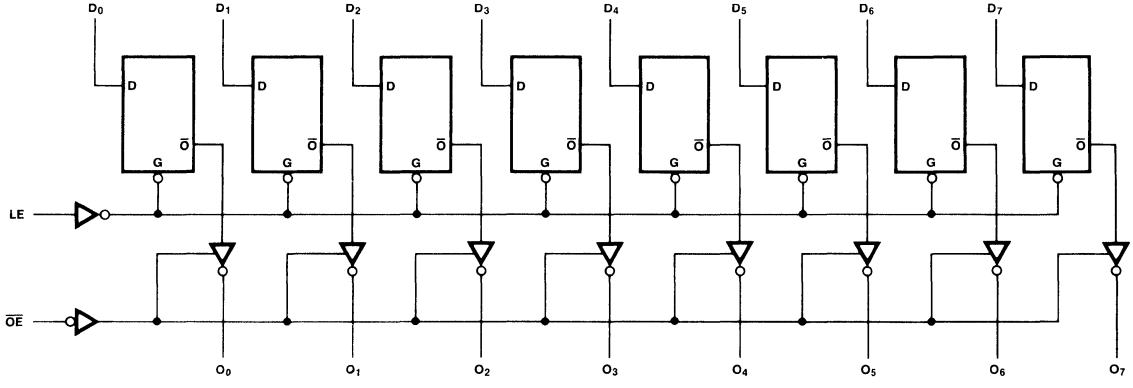
DIP
TOP VIEW



SSD54/74AHCT373-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT373-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{LE}$	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50 pf R_L = 500Ω	10.0	2.0	16.0	2.0	19.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	24.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	12.0	2.0	16.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		20.0	6.0	23.0	6.0	27.0	ns
t_S	Set-up Time HIGH or LOW D_N to LE		4.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		3.0	7.0	—	7.0	—	ns
t_W	LE Pulse Width HIGH or LOW		7.0	10.0	—	10.0	—	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D REGISTER (3-STATE)

IDT54/74AHCT374

FEATURES:

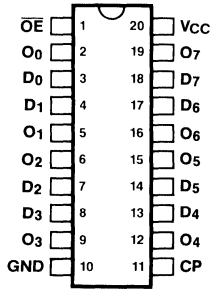
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D register (3-state)
- 100% product assurance screening to MIL-STD-833, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT374 are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. This register consists of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

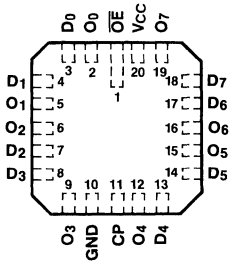
Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS



SSD54/74AHCT374-001

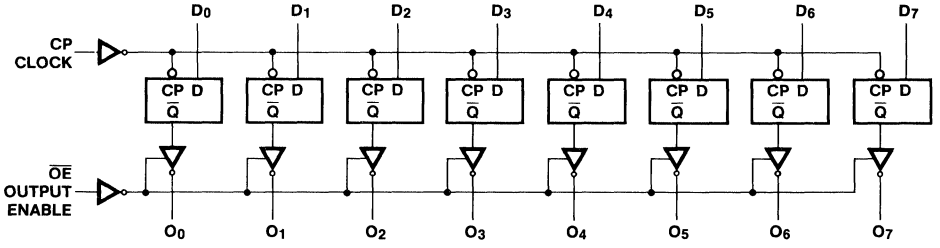
DIP
TOP VIEW



SSD54/74AHCT374-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT374-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↗	L	L	L
	L	↗	H	H	H
	H	↗	L	Z	L
	H	↗	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↗ = LOW-to-HIGH transition
NO = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500 Ω	10.0	3.0	16.0	3.0	18.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	5.0	18.0	5.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	18.0	2.0	24.0	ns
t_S	Setup Time HIGH or LOW D_N to CP		2.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	3.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		10.0	14.0	—	16.5	—	ns

HIGH-SPEED CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74AHCT377

Integrated Device Technology, Inc.

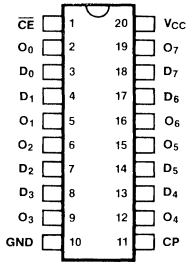
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with clock enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74AHCT377 is an octal D flip-flop built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS



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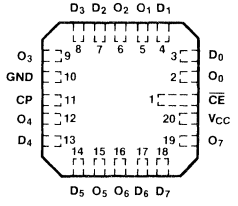
DIP
TOP VIEW

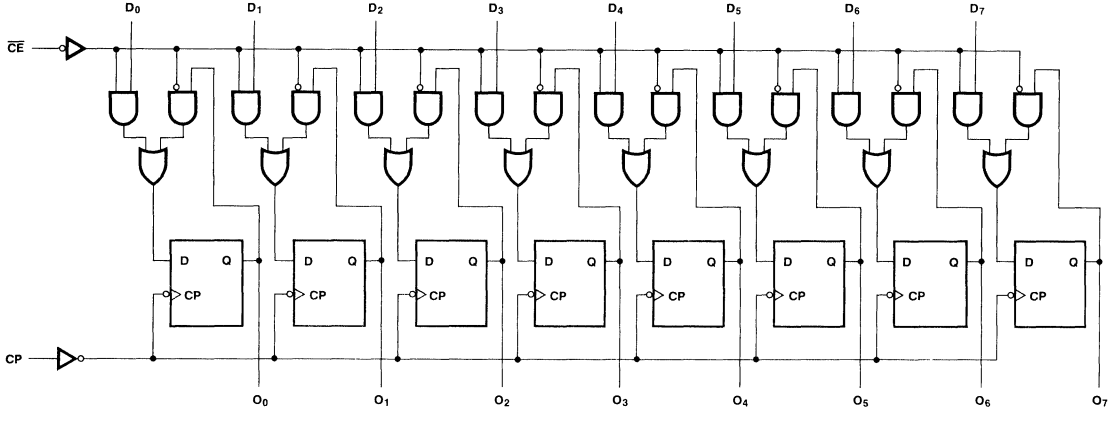


SSD54/74FCT377-002

LCC
TOP VIEW

5

FUNCTIONAL BLOCK DIAGRAM



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SSD54/74FCT377-003

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_i = 500KHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open F_{CP} = 1.0MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_i = 250KHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_N	O_N
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↑ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pf R_L = 500Ω	10.0	4.0	18.0	4.0	20.0	ns
t_S	Set Up Time HIGH or LOW D_N to CP		5.0	6.0	—	6.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		2.0	3.0	—	4.0	—	ns
t_S	Set Up Time HIGH or LOW $\overline{CE}$ to CP		3.0	5.0	—	5.0	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		2.0	6.0	—	8.0	—	ns
t_W	Clock Pulse Width, LOW		7.0	10.0	—	10.0	—	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74AHCT521

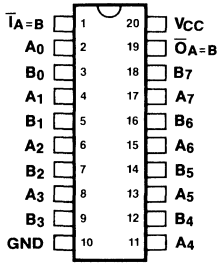
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 9ns typical propagation delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- 8-bit identity comparator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

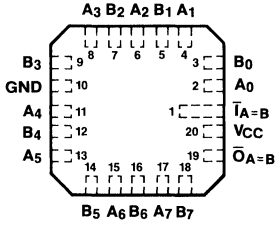
The IDT54/74AHCT521 is an 8-bit identity comparator built using advanced CEMOS™, a dual metal CMOS technology. The device compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS



SSDAHCT521-001

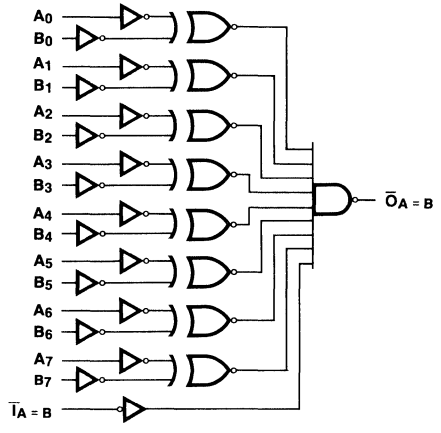
DIP
TOP VIEW



SSDAHCT521-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT521-003

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CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_7	Word A inputs
B_0-B_7	Word B inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active Low)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	C_L = 50 pf R_L = 500 Ω	9.0	—	13.0	—	17.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	—	12.0	—	11.0	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54/74AHCT533

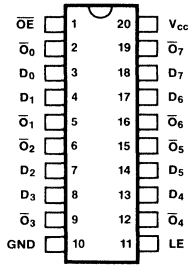
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 11ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μ max.)
- Octal transparent latch with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

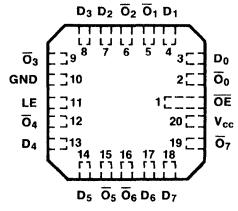
The IDT54/74AHCT533 are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74AHCT533 consist of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSD54/74FCT533-001

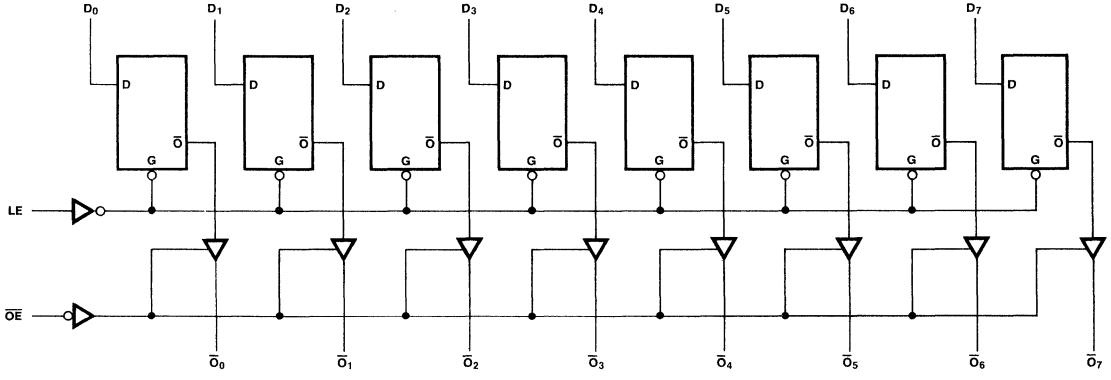
DIP
TOP VIEW



SSD54/74FCT533-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT533-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250KHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	11.0	4.0	19.0	4.0	24.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	4.0	18.0	4.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	16.0	2.0	22.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_N$		15.0	4.0	23.0	4.0	28.0	ns
t_S	Set Up Time HIGH or LOW D_N to LE		7.0	15.0	—	15.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		5.0	7.0	—	7.0	—	ns
t_W	LE Pulse Width HIGH or LOW		7.0	15.0	—	15.0	—	ns

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Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54/74AHCT534

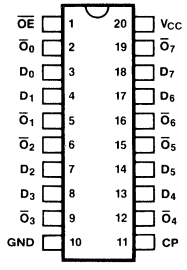
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D flip-flop with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

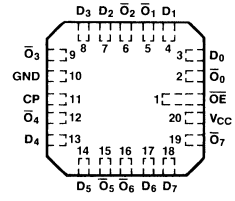
The IDT54/74AHCT534 are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT534 are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN CONFIGURATIONS



SSD54/74FCT534-001

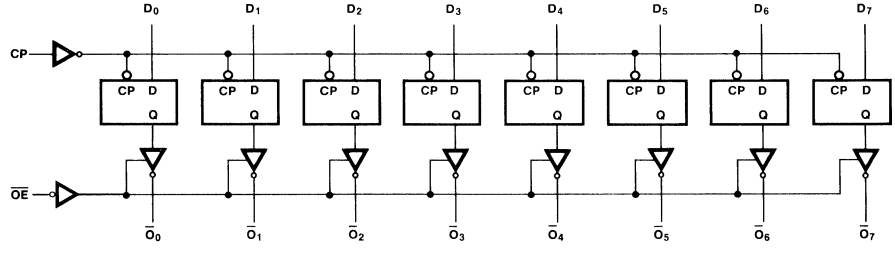
DIP
TOP VIEW



SSD54/74FCT534-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT534-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 500KHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 250KHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	$\overline{O_N}$	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	H
	L	↑	H	L	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_N$	C_L = 50 pf R_L = 500Ω	10.0	3.0	16.0	3.0	18.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	5.0	18.0	5.0	20.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	14.0	2.0	16.0	ns
t_S	Set Up Time HIGH or LOW D_N to CP		2.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	3.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	14.0	—	16.0	—	ns

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Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL TRANSPARENT LATCH

IDT54/74AHCT573

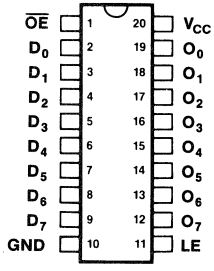
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

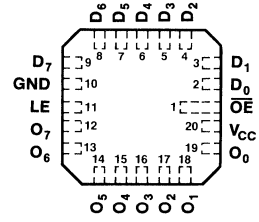
DESCRIPTION:

The IDT54/74AHCT573 are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. This octal latch has 3-state outputs and is intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

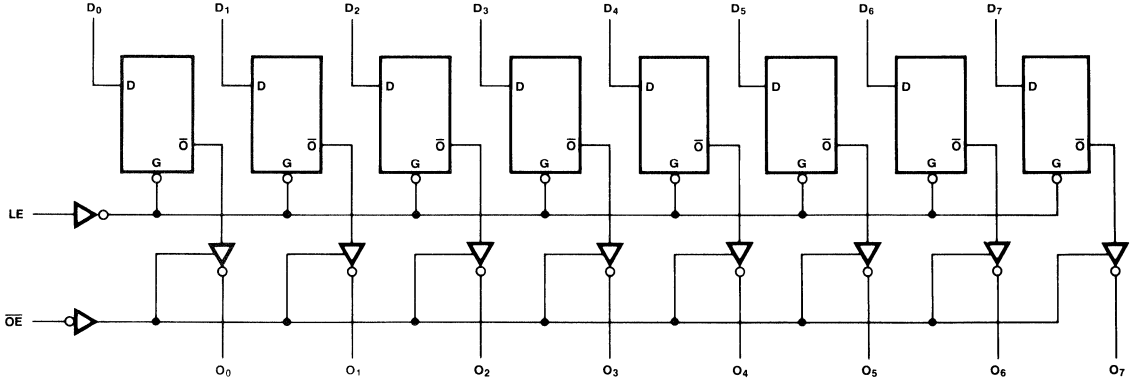


DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT373-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL	2.4	4.3	—	
			I_{OH} = -2.6mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250KHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{LE}$	Latch Enables Input (Active HIGH)
$\overline{OE}$	Output Enables Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50 pf R_L = 500Ω	10.0	2.0	14.0	2.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	4.0	18.0	4.0	21.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	13.0	2.0	15.0	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		20.0	8.0	20.0	8.0	27.0	ns
t_S	Set-up Time HIGH or LOW D_N to LE		4.0	10.0	—	10.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		3.0	7.0	—	7.0	—	ns
t_W	LE Pulse Width HIGH or LOW		7.0	10.0	—	10.0	—	ns

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Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D REGISTER (3-STATE)

IDT54/74AHCT574

FEATURES:

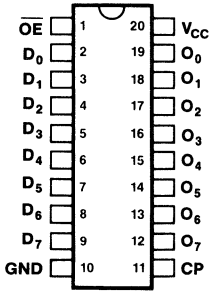
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical address to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Octal D register (3-state)
- 100% product assurance screening to MIL-STD-833, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

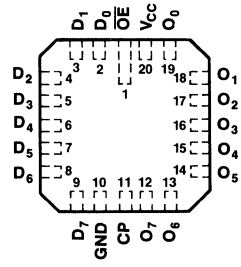
The IDT54/74AHCT574 are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. This register consists of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

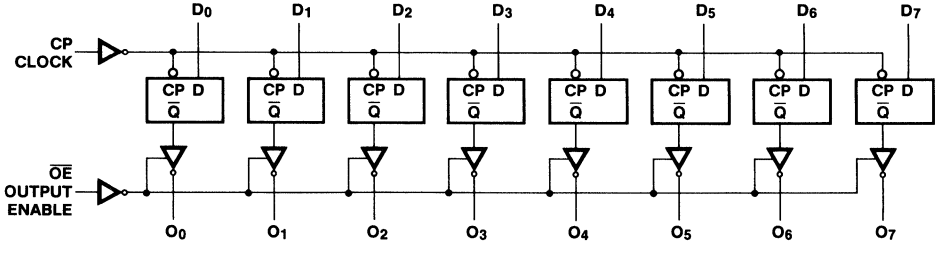


DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT374-003

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -1.0mA MIL.	2.4	4.3	—	
			I_{OH} = -2.6mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL.	—	—	0.4	
			I_{OL} = 24mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 500kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.65	3.4	
		V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 250kHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.63	2.2	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.88	9.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$

   I_{CCQ} = Quiescent Current

   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

   D_H = Duty Cycle for TTL Inputs High

   N_T = Number of TTL Inputs at D_H

   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)

   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

   f_i = Input Frequency

   N_i = Number of Inputs at f_i

   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_I	The D flip-flop data inputs.
CP	Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.
O_I	The register three-state outputs.
$\overline{OE}$	Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CLOCK	D_I	O_I	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↗	L	L	L
	L	↗	H	H	H
	H	↗	L	Z	L
	H	↗	H	Z	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↗ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50 pf R_L = 500 Ω	10.0	4.0	14.0	4.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		11.0	4.0	18.0	4.0	21.0	ns
t_{HZ} t_{LZ}	Output Disable Time		9.0	2.0	12.0	2.0	15.0	ns
t_S	Setup Time HIGH or LOW D_N to CP		2.0	15.0	—	15.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	4.0	—	4.0	—	ns
t_W	CP Pulse Width HIGH or LOW		10.0	14.0	—	16.5	—	ns

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HIGH-SPEED CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT54/74AHCT640

Integrated Device Technology, Inc.

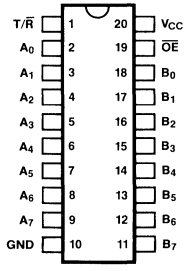
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns data to output
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

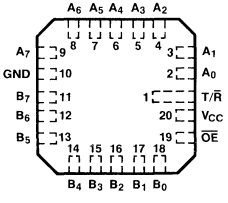
The IDT54/74AHCT640 are 8-bit inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control ($T/\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



SSD54/74AHCT640-001

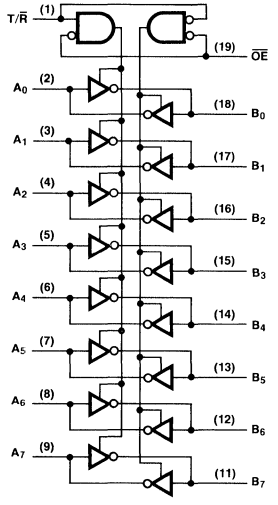
DIP
TOP VIEW



SSD54/74AHCT640-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT640-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50 pf R_L = 500 Ω	10.0	2.0	11.0	2.0	14.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	24.0	5.0	27.0	ns
t_{HZ} t_{LZ}	Output Disable Time		12.0	2.0	15.0	2.0	20.0	ns

Integrated Device Technology, Inc.

HIGH-SPEED CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74AHCT645

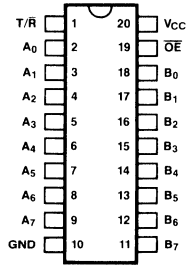
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 8ns typical data to output delay
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

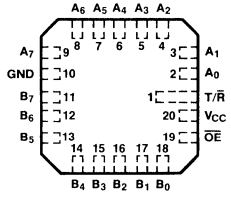
DESCRIPTION:

The IDT54/74AHCT645 are 8-bit non-inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These non-inverting buffer transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control ($T/\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



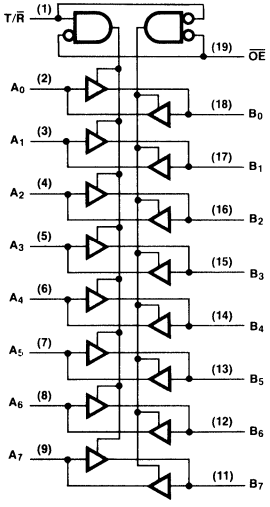
SSD54/74AHCT645-001



SSD54/74AHCT645-002

LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74AHCT645-003

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CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 14mA MIL	—	—	0.4	
			I_{OL} = 24mA COM	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 1.0MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.15	1.8	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	0.4	2.6	
		V_{CC} = Max. Outputs Open f_i = 250kHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	—	0.3	2.0	
			V_{IN} = 3.4V or V_{IN} = GND	—	2.3	8.4	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	TYPICAL	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B B to A	C_L = 50 pf R_L = 500Ω	8.0	3.0	10.0	3.0	15.0	ns
t_{ZH} t_{ZL}	Output Enable Time		15.0	5.0	20.0	5.0	25.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	15.0	2.0	18.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B*		15.0	—	—	—	—	ns

*Guaranteed by Design

Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER

IDT54/74FCT138
IDT54/74FCT138A

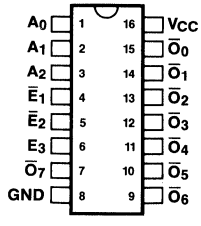
FEATURES:

- IDT54/74FCT138 equivalent to FAST™ speed; **IDT54/74FCT138A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 1-of-8 decoder with enables
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

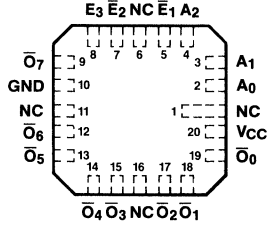
The IDT54/74FCT138 and IDT54/74FCT138A are 1-of-8 decoders built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT138 and IDT54/74FCT138A accept three binary weighed inputs (A_0, A_1, A_2) and, when enabled, provide eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138 and IDT54/74FCT138A feature three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outpus will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138 or IDT54/74FCT138A devices and one inverter.

PIN CONFIGURATIONS



SSD54/74FCT138-001

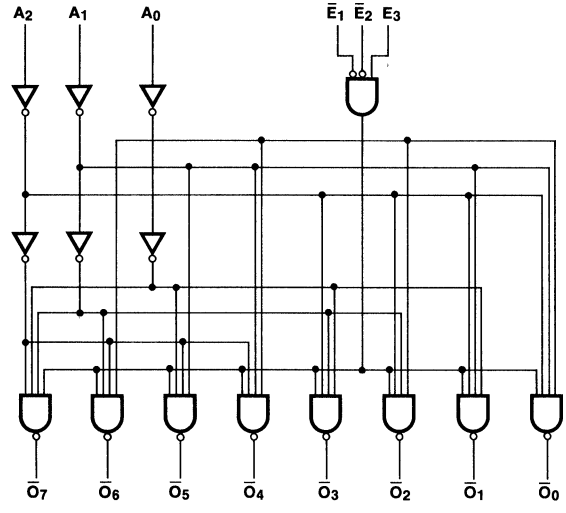
DIP/SOIC TOP VIEW



SSD54/74FCT138-002

LCC/PLCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT138-003

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FAST is a trademark of Fairchild Semiconductor Co.

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.38	2.3	
			V_{IN} = 3.4V V_{IN} = GND	—	0.63	3.1	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT138					IDT54/74FCT138A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 to $\overline{O}_N$	C_L = 50pF R_L = 500Ω	7.0	3.5	9.0	3.5	12.0	4.5	1.5	5.8	1.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_N$		6.0	3.0	9.0	3.0	12.5	4.5	1.5	5.9	1.5	8.0	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_N$		6.0	3.5	9.0	3.5	12.5	4.5	1.5	5.9	1.5	8.0	ns

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Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER

IDT54/74FCT139
IDT54/74FCT139A

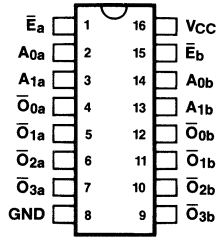
FEATURES:

- IDT54/74FCT139 equivalent to FAST™ speed; **IDT54/74FCT139A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Dual 1-of-4 decoder with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

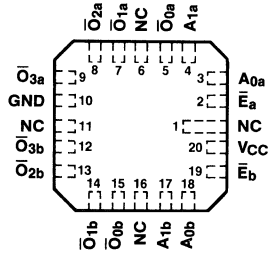
The IDT54/74FCT139 and IDT54/74FCT139A are dual 1-of-4 decoders built using advanced CEMOS™, a dual metal CMOS technology. The devices have two independent decoders, each of which accept two binary weighed inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

PIN CONFIGURATIONS



SSD54/74FCT139-001

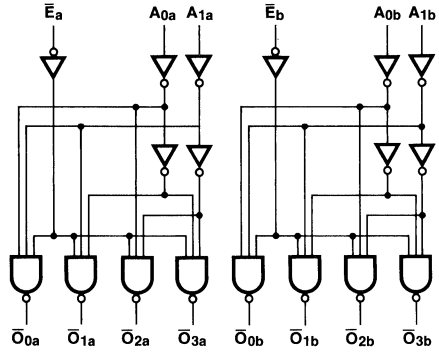
DIP/SOIC
TOP VIEW



SSD54/74FCT139-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT139-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V

V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.3	
		V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Input Toggling on Each Decoder	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	7.5	
			V_{IN} = 3.4V V_{IN} = GND	—	3.5	9.1	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT139					IDT54/74FCT139A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50pf R_L = 500Ω	6.0	3.0	9.0	2.5	12.0	4.5	1.5	5.9	1.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		5.5	3.0	8.0	2.5	9.0	4.0	1.5	5.5	1.5	7.2	ns

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161/A
IDT54/74FCT163/A

Integrated Device Technology, Inc

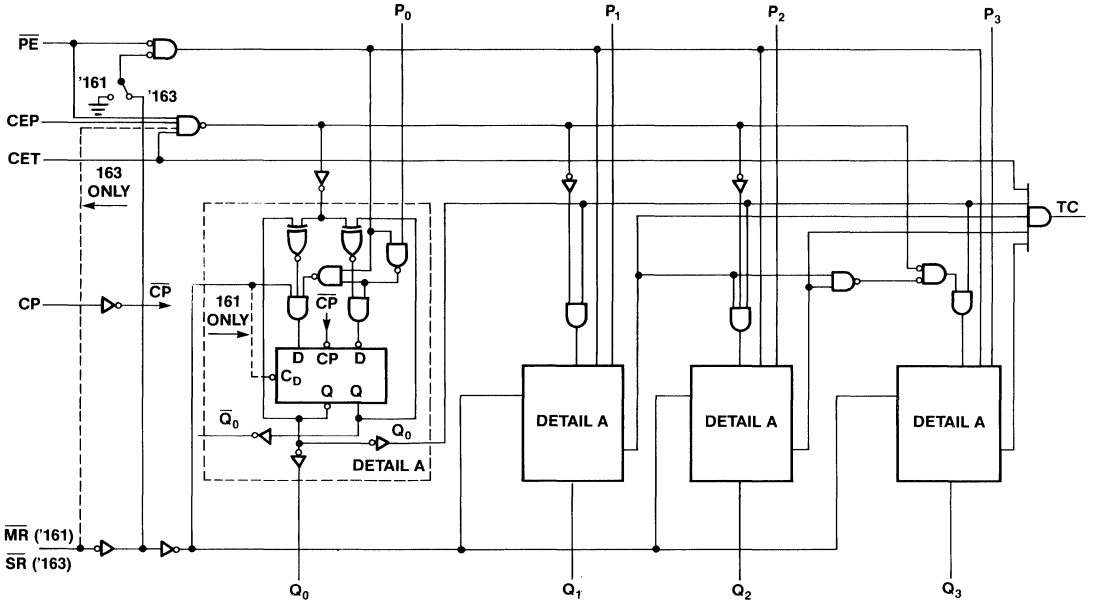
FEATURES:

- IDT54/74FCT161/163 equivalent to FAST™ speed; **IDT54/74FCT161A/163A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT161/163 and IDT54/74FCT161A/163A are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The IDT54/74FCT161/163 and IDT54/74FCT161A/163A have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT161/163 and IDT54/74FCT161A/163A have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



SSDFCT163-001

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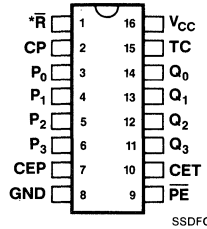
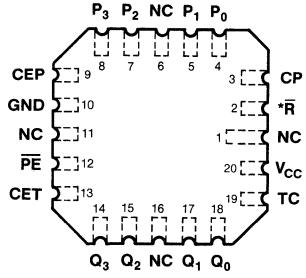
PIN CONFIGURATIONS



SSDFCT163-002

DIP/SOIC
TOP VIEW



SSDFCT163-003

LCC/PLCC
TOP VIEW

***MR FOR '161**
***SR FOR '163**

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA COM'L.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS (IDT54/74FCT161/A)

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Mode $P_{0-3} = V_{LC}$ $\overline{CEP} = CET = \overline{MR} = \overline{PE} = V_{HC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle Count Mode $P_{0-3} = V_{LC}$ $\overline{CEP} = CET = \overline{MR} = \overline{PE} = V_{HC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	—	mA
			CP V_{IN} = 3.4V or V_{IN} = GND	—	3.8	—	

POWER SUPPLY CHARACTERISTICS (IDT54/74FCT163/A)

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Mode $P_{0-3} = V_{LC}$ $\overline{CEP} = CET = \overline{SR} = \overline{PE} = V_{HC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle Count Mode $P_{0-3} = V_{LC}$ $\overline{CEP} = CET = \overline{SR} = \overline{PE} = V_{HC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	—	mA
			CP V_{IN} = 3.4V or V_{IN} = GND	—	3.8	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP} + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   $f_i = P_{0-3}$ Input Frequency (Load)
   $N_i = P_{0-3}$ Inputs at f_i (Load)

All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

TRUTH TABLE

$\overline{SR}$(1)	$\overline{PE}$	CET	CEP	ACTION ON THE RISING CLOCK EDGE (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:
1. For FCT163/163A ONLY
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT161 IDT54/74FCT163					IDT54/74FCT161A IDT54/74FCT163A					UNITS
			TYP.	MIL.		COM'L.		TYP.	MIL.		COM'L.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n ($\overline{PE}$ Input HIGH)	C_L = 50pf R_L = 500Ω	7.0	3.5	11.5	3.5	11.0	4.5	2.0	7.5	2.0	7.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n ($\overline{PE}$ Input LOW)		7.0	4.0	10.0	4.0	9.5	4.5	2.0	6.5	2.0	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		10.0	5.0	16.5	5.0	15.0	6.5	2.0	10.8	2.0	9.8	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		4.5	2.5	9.0	2.5	8.5	3.0	1.5	5.9	1.5	5.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F161A)		9.0	5.5	14.0	5.5	13.0	5.9	2.0	9.1	2.0	8.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC		8.0	4.5	12.5	4.5	11.5	5.2	2.0	8.2	2.0	7.5	ns
$t_{S}(H)$ $t_{S}(L)$	Setup Time, HIGH or LOW P_n to CP		5.0	5.5	—	5.0	—	4.0	4.5	—	4.0	—	ns
$t_{N}(H)$ $t_{N}(L)$	Hold Time, HIGH or LOW P_n to CP		2.0	2.5	—	2.0	—	1.5	2.0	—	1.5	—	ns
$t_{S}(H)$ $t_{S}(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.0	13.5	—	11.5	—	9.0	11.5	—	9.5	—	ns
$t_{N}(H)$ $t_{N}(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		2.0	2.0	—	2.0	—	1.5	1.5	—	1.5	—	ns
$t_{S}(H)$ $t_{S}(L)$	Setup Time, HIGH or LOW CEP or CET to CP		11.0	13.0	—	11.5	—	9.0	11.0	—	9.5	—	ns
$t_{N}(H)$ $t_{N}(L)$	Hold Time, HIGH or LOW CEP or CET to CP		0	0	—	0	—	0	0	—	0	—	ns
$t_{W}(H)$ $t_{W}(L)$	Clock Pulse Width (Load) HIGH or LOW		5.0	5.0	—	5.0	—	4.0	4.0	—	4.0	—	ns
$t_{W}(H)$ $t_{W}(L)$	Clock Pulse Width (Count) HIGH or LOW		6.0	8.0	—	7.0	—	5.0	7.0	—	6.0	—	ns
$t_{W}(L)$	$\overline{MR}$ Pulse Width, LOW ('F161A)		5.0	5.0	—	5.0	—	4.0	4.0	—	4.0	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP ('F161A)		6.0	6.0	—	6.0	—	5.0	5.0	—	5.0	—	ns

Integrated Device Technology, Inc.

FAST CMOS CARRY LOOKAHEAD GENERATOR

IDT54/74FCT182
IDT54/74FCT182A

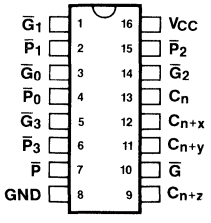
FEATURES:

- IDT54/74FCT182 equivalent to FAST™ specs
  IDT54/74FCT182A 35% faster than FAST
- Equivalent to FAST™ speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Carry lookahead generator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT182 and IDT54/74FCT182A are high-speed carry lookahead generators built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT182 and IDT54/74FCT182A are generally used with a 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

PIN CONFIGURATIONS



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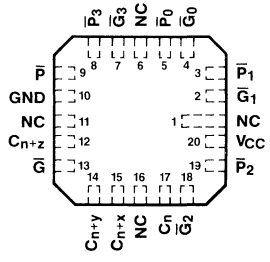
DIP/SOIC
TOP VIEW



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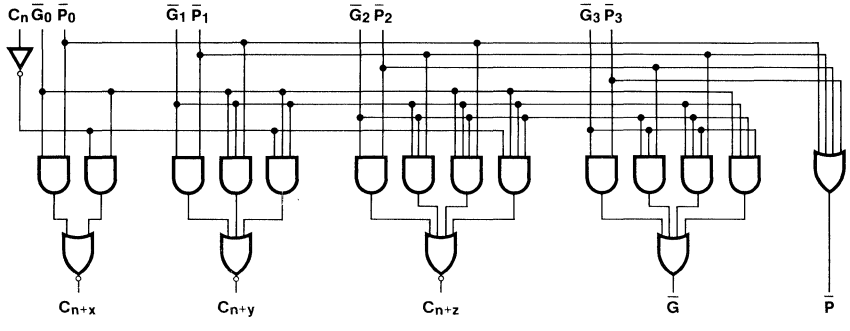
LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.3	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle One Input Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.3	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)
$\overline{G}_1$	Carry Generate Input (Active LOW)
$\overline{G}_3$	Carry Generate Input (Active LOW)
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)
$\overline{P}_2$	Carry Propagate Input (Active LOW)
$\overline{P}_3$	Carry Propagate Input (Active LOW)
C_{n+x}-C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

5

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	X	H	H	H	X					L		
X	H	X	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT182					IDT54/74FCT182A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay C_N to C_{N+X}, C_{N+Y}, C_{N+Z}	C_L = 50 pf R_L = 500Ω	6.0	3.0	10.0	3.0	16.5	4.0	2.0	6.5	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		6.0	2.0	9.0	2.0	11.5	4.0	1.5	5.8	1.5	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, to C_{N+X}, C_{N+Y}, C_{N+Z}		6.0	2.0	9.5	2.0	11.5	4.0	1.5	6.0	1.5	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$ to $\overline{G}$		7.0	3.0	11.0	3.0	16.5	4.8	2.0	7.0	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_N$ to $\overline{G}$		7.5	3.0	11.5	3.0	16.5	5.0	2.0	7.4	2.0	10.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_N$ to $\overline{P}$		6.0	2.5	8.5	2.5	12.5	4.0	1.5	5.5	1.5	7.4	ns

Integrated Device Technology, Inc.

FAST CMOS UP/DOWN BINARY COUNTER

IDT54/74FCT191
IDT54/74FCT191/A

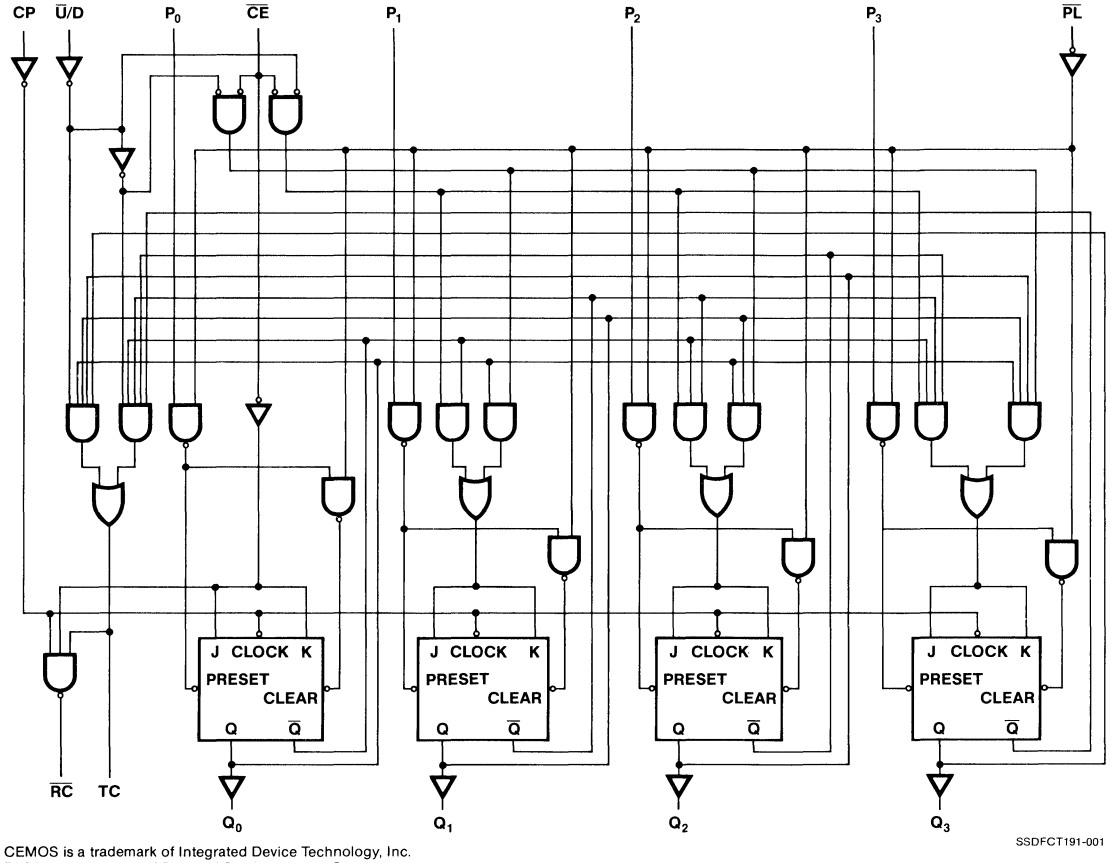
FEATURES:

- IDT54/74FCT191 equivalent to FAST™ speed; **IDT54/74FCT191A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT191 and IDT54/74FCT191A are reversible modulo-16 binary counters, featuring synchronous counting and asynchronous presetting, and built using advanced CEMOS™, a dual metal CMOS technology. The preset feature allows the IDT54/74FCT191 and IDT54/74FCT191A to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



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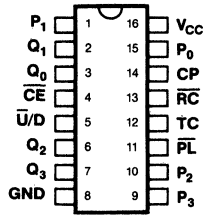
PIN CONFIGURATIONS



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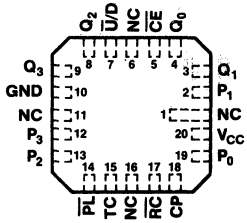
DIP/SOIC
TOP VIEW



SSDFCT191-003

LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Up or Down Mode $\overline{CE} = V_{LC}$ $\overline{PL} = P_0 - P_3 = V_{HC}$ $\overline{U}/D = V_{HC}$ or V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle Count Up or Down Mode $\overline{PL} = P_0 - P_3 = V_{HC}$ $\overline{CE} = V_{LC}$ $\overline{U}/D = V_{HC}$ or V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	—	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	3.8	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP} + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   f_i = P_{0-3} Input Frequency (Load)
   N_i = Number of P_{0-3} Inputs at f_i (Load)

All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Count Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Clock Output (Active HIGH)

TRUTH TABLES
MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asynch.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC[1]	CP	$\overline{RC}$
L	H	⎍	⎍
H	X	X	H
X	L	X	H

NOTES:

1. TC is generated internally.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT191					IDT54/74FCT191A					UNITS
			TYP.	MIL.		COM'L.		TYP.	MIL.		COM'L.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	8.5	1.5	16.0	3.0	12.0	5.5	1.5	10.5	2.5	7.8	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		10.0	4.5	16.0	5.0	14.0	6.5	2.0	10.5	3.0	9.1	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		5.5	1.5	12.5	3.0	8.5	3.6	1.5	8.2	2.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		5.5	3.0	8.5	3.0	8.0	3.6	2.0	5.6	2.0	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay U/D to $\overline{RC}$		11.0	5.5	22.5	5.5	20.0	7.2	4.0	14.7	4.0	13.0	ns
t_{PLH} t_{PHL}	Propagation Delay U/D to TC		7.0	4.0	13.0	4.0	11.0	4.6	3.0	8.5	3.0	7.2	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		10.0	1.5	16.0	3.0	14.0	6.5	1.5	10.4	2.0	9.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		9.0	5.0	14.0	5.0	13.0	5.9	3.0	9.1	3.0	8.5	ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$		4.5	6.0	—	5.0	—	4.0	5.0	—	4.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$		2.0	2.0	—	2.0	—	1.5	1.5	—	1.5	—	ns
$t_S(L)$	Setup Time LOW $\overline{CE}$ to CP		10.0	10.5	—	10.0	—	9.0	9.5	—	9.0	—	ns
$t_H(L)$	Hold Time LOW $\overline{CE}$ to CP		0	0	—	0	—	0	0	—	0	—	ns
$t_S(H)$ $t_s(L)$	Setup Time, HIGH or LOW U/D to CP		12.0	12.0	—	12.0	—	10.0	10.0	—	10.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW U/D to CP		0	0	—	0	—	0	0	—	0	—	ns
$t_W(L)$	$\overline{PL}$ Pulse Width, LOW		6.0	8.5	—	6.0	—	5.5	8.0	—	5.5	—	ns
$t_W(L)$	CP Pulse Width, LOW		5.0	7.0	—	5.0	—	4.0	6.0	—	4.0	—	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP		6.0	7.5	—	6.0	—	5.0	6.5	—	5.0	—	ns

Integrated Device Technology, Inc

FAST CMOS UP/DOWN BINARY COUNTERS

IDT54/74FCT193
IDT54/74FCT193A

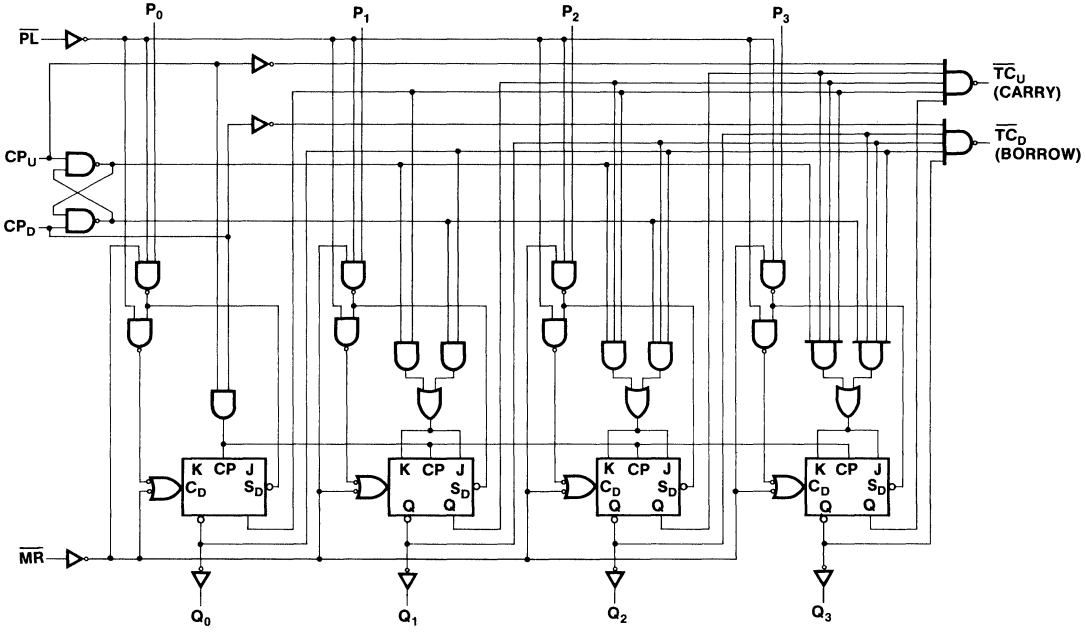
FEATURES:

- IDT54/74FCT193 equivalent to FAST™ speed; **IDT54/74FCT193A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 100% product assurance screening to MIL-STD-883, Class B is available

DESCRIPTION:

The IDT54/74FCT193 and IDT54/74FCT193A are up/down modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. Separate Count-up and Count-down Clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count-up and Terminal Count-down outputs are provided that are used as the clocks for subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel ($\overline{PL}$) and the Master Reset ($\overline{MR}$) inputs asynchronously override the clocks.

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

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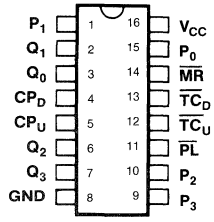
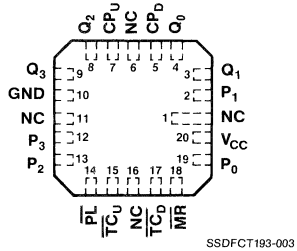
PIN CONFIGURATIONS



SSDFCT193-002

DIP/SOIC
TOP VIEW



SSDFCT193-003

LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operation Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP_U} = f_{CP_D} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ MR = V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.3	—	mA/ MHz
I_{CC}	Total Power Supply Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle Count Up or Down $\overline{PL} = P_0 - P_3 = V_{HC}$ MR = V_{LC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	—	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	3.8	—	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output shold be shorted at one time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP} + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Input High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Count Clock or Load Clock Frequency
   f_i = P_{0-3} Input Frequency (Load)
   N_i = Number of P_{0-3} Inputs at f_i (Load)

All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P_0-P_3	Parallel Data Inputs
Q_0-Q_3	Flip-flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

TRUTH TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT193					IDT54/74FCT193A					UNITS
			TYP.	MIL.		COM'L.		TYP.	MIL.		COM'L.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	C_L = 50pF R_L = 500Ω	7.0	3.5	10.5	3.5	10.5	4.6	2.0	6.9	2.0	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		9.5	4.0	14.0	4.0	13.5	6.2	2.0	9.1	2.0	8.8	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		11.0	3.0	16.5	3.0	15.5	7.2	2.0	10.8	2.0	10.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		10.0	5.0	13.5	5.0	14.0	6.5	2.0	9.1	2.0	8.8	ns
t_{PHL}	Propagation Delay MR to Q_n		11.0	6.5	16.0	6.5	15.5	7.0	3.0	10.4	3.0	10.1	ns
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		10.5	6.0	15.0	6.0	14.5	6.5	3.0	9.8	3.0	9.4	ns
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		11.5	7.0	16.0	7.0	15.5	7.5	3.0	10.4	3.0	10.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$		12.0	7.0	18.5	7.0	16.5	8.0	3.0	12.0	3.0	10.8	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		11.5	6.5	16.5	6.5	15.5	7.5	3.0	10.8	3.0	10.1	ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW P_n to $\overline{PL}$		4.5	6.0	—	5.0	—	4.0	5.0	—	4.0	—	ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW P_n to $\overline{PL}$		2.0	2.0	—	2.0	—	1.5	1.5	—	1.5	—	ns
$t_W(L)$	$\overline{PL}$ Pulse Width, LOW		6.0	7.5	—	6.0	—	5.0	6.5	—	5.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW		5.0	7.0	—	5.0	—	4.0	6.0	—	4.0	—	ns
$t_W(L)$	CP_U or CP_D Pulse Width, LOW (Change of Direction)		10.0	12.0	—	10.0	—	8.0	10.0	—	8.0	—	ns
$t_W(H)$	MR Pulse Width, HIGH		6.0	6.0	—	6.0	—	5.0	5.0	—	5.0	—	ns
t_{REC}	Recovery Time $\overline{PL}$ to CP_U or CP_D		6.0	8.0	—	6.0	—	5.0	7.0	—	5.0	—	ns
t_{REC}	Recovery Time MR to CP_U or CP_D		4.0	4.5	—	4.0	—	3.0	3.5	—	3.0	—	ns

Integrated Device Technology, Inc

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT240
IDT54/74FCT240A

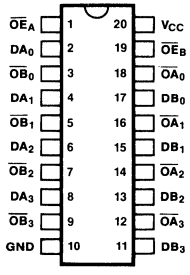
FEATURES:

- IDT54/74FCT240 equivalent to FAST™ speed; **IDT54/74FCT240A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT240 and IDT54/74FCT240A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved board density.

PIN CONFIGURATIONS



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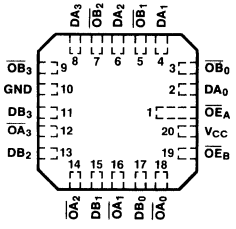
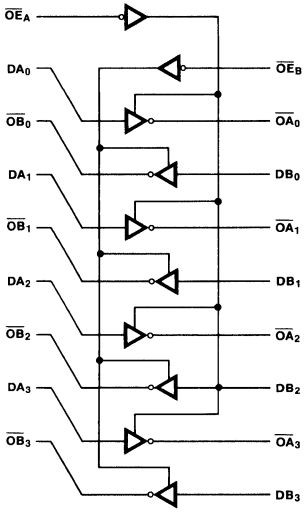
DIP/SOIC
TOP VIEW



SSDFCT240-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
$\overline{O}$xx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT240					IDT54/74FCT240A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	5.0	2.0	8.0	2.0	9.0	3.5	1.5	4.8	1.5	5.1	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	10.0	2.0	10.5	4.8	1.5	6.2	1.5	6.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	9.5	2.0	12.5	4.3	1.5	5.6	1.5	5.9	ns

Integrated Device Technology, Inc

FAST CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT244
IDT54/74FCT244A

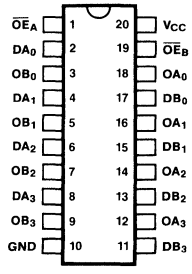
FEATURES:

- IDT54/74FCT244 equivalent to FAST™ speed; **IDT54/74FCT244A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal buffer/line driver with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

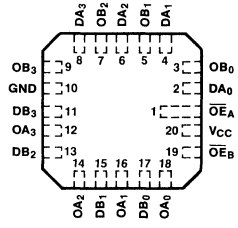
The IDT54/74FCT244 and IDT54/74FCT244A are octal buffer/line drivers built using advanced CEMOS™, a dual metal CMOS technology. The devices are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

PIN CONFIGURATIONS



SSD54/74FCT244-001

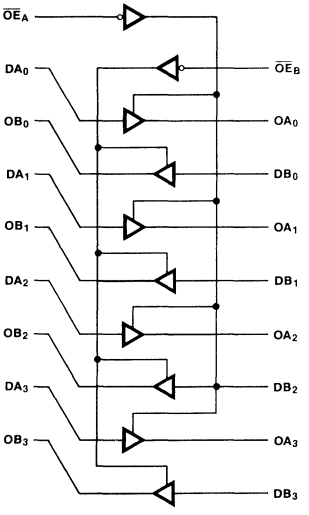
DIP/SOIC TOP VIEW



SSD54/74FCT244-002

LCC/PLCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT244-003

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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	
$V^+ - V^-$	Hysteresis	On Data Inputs		—	0.4	—	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Input (Active LOW)
Dxx	Inputs
Oxx	Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}_A$, $\overline{OE}_B$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT244					IDT54/74FCT244A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pf R_L = 500Ω	4.5	2.5	6.5	2.0	7.0	3.1	1.5	4.3	1.5	4.6	ns
t_{ZH} t_{ZL}	Output Enable Time		6.0	2.0	8.0	2.0	8.5	3.8	1.5	5.2	1.5	5.5	ns
t_{HZ} t_{LZ}	Output Disable Time		5.0	2.0	7.0	2.0	7.5	3.3	1.5	4.6	1.5	4.9	ns

Integrated Device Technology, Inc.

FAST CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74FCT245
IDT54/74FCT245A

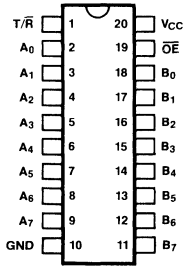
FEATURES:

- IDT54/74FCT245 equivalent to FAST™ speed; **IDT54/74FCT245A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA port A, 48mA port B over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

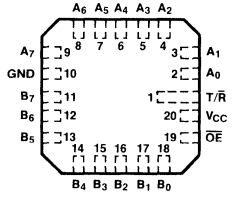
The IDT54/74FCT245 and IDT54/74FCT245A are 8-bit non-inverting, bidirectional buffers built using advanced CEMOS™, a dual metal CMOS technology. These bidirectional buffers have 3-state outputs and are intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in High Z condition.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

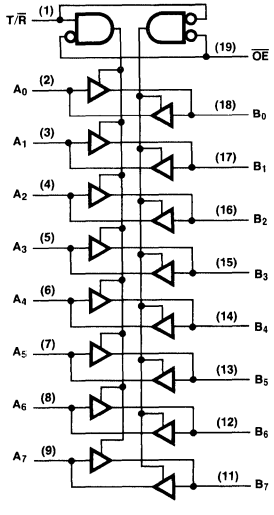
SSD54/74FCT245-001



LCC/PLCC
TOP VIEW

SSD54/74FCT245-002

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT245-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage Ports A and B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage Port A	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	
V_{OL}	Output LOW Voltage Port B	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	
$V^+ - V^-$	Hysteresis	On A_i and B_i		—	0.4	—	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \leq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{LC}$ $V_{CC} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V or V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_0	Side B Inputs or 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUT
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT245					IDT54/74FCT245A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B B to A	C_L =50 pF R_L = 500Ω	5.0	2.5	7.0	2.0	7.5	3.3	1.5	4.6	1.5	4.9	ns
t_{ZH} t_{ZL}	Output Enable Time		6.0	3.0	9.5	3.0	10.0	4.8	1.5	6.2	1.5	6.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.5	2.5	10.0	4.5	1.5	5.0	1.5	6.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B[1]		6.0	—	—	—	—	5.0	—	—	—	—	ns

NOTE:

1. Guaranteed by design.

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLEAR

IDT54/74FCT273
IDT54/74FCT273A

FEATURES:

- IDT54/74FCT273 equivalent to FAST™ speed; **IDT54/74FCT273A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clear
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

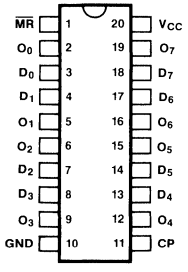
DESCRIPTION:

The IDT54/74FCT273 and IDT54/74FCT273A are octal flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT273 and IDT54/74FCT273A have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

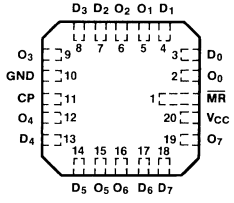
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

PIN CONFIGURATIONS



SSDAHCT273-001

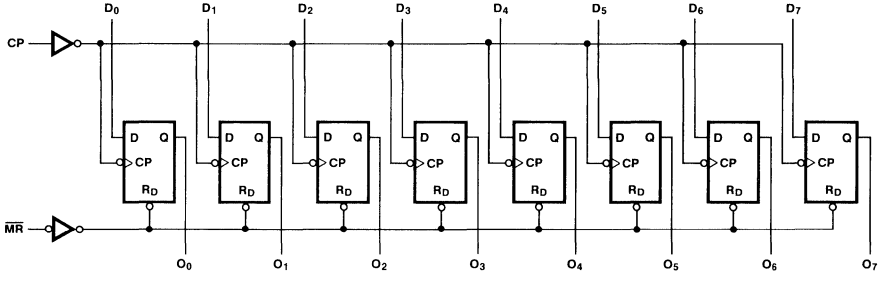
DIP/SOIC
TOP VIEW



SSDAHCT273-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT273-003

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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.4	
			I_{OL} = 48mA COM'L.	—	—	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{MR} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{MR} = V_{CC}$ One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open F_{CP} = 10MHz 50% Duty Cycle $\overline{MR} = V_{CC}$ Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_0-O_7	Data Outputs

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUT
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = DON'T CARE
↑ = LOW to HIGH clock transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT273					IDT54/74FCT273A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	C_L = 50 pf R_L = 500Ω	7.0	3.0	13.0	3.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_{PLH} t_{PHL}	Propagation Delay MR to Output		8.0	2.0	13.0	2.0	15.0	5.0	2.0	7.2	2.5	8.3	ns
t_S	Set Up time HIGH or LOW Data to CP		3.0	3.0	—	3.5	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Data to CP		1.0	2.5	—	2.5	—	1.0	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		4.0	7.0	—	7.0	—	—	—	—	6.0	—	ns
t_{REC}	Recovery Time MR to CP		3.0	4.0	—	5.0	—	1.5	2.5	—	3.0	—	ns

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299
IDT54/74FCT299A

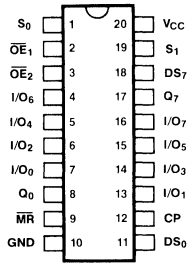
FEATURES:

- IDT54/74FCT299 equivalent to FAST™ speed; **IDT54/74FCT299A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-input universal shift register
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

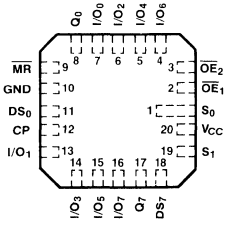
The IDT54/74FCT299 and IDT54/74FCT299A are 8-bit universal shift registers built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT299 and IDT54/74FCT299A are 8-bit universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0–Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

PIN CONFIGURATIONS



SSD54/74FCT299-001

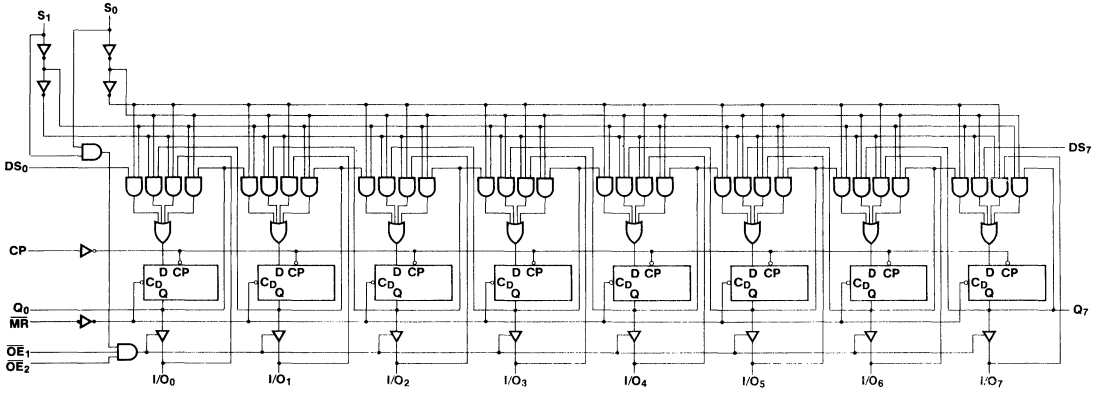
DIP/SOIC
TOP VIEW



SSD54/74FCT299-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT299-003

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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_7$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND $\overline{MR}$ = V_{CC} $S_0 = S_1 = V_{CC}$ $DS_0 = DS_1$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

5

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CP	Clock Pulse Input (Active Rising Edge)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs (Active LOW)
I/O_0-I/O_7	Parallel Data Inputs or 3-State Parallel Inputs
Q_0, Q_7	Serial Outputs

TRUTH TABLE

INPUTS				RESPONSE
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0-Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_N \rightarrow Q_N$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT299					IDT54/74FCT299A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	7.0	3.5	10.0	4.0	14.0	5.0	2.5	7.2	2.5	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_N		6.0	4.0	12.0	3.5	12.0	5.0	2.5	7.2	2.5	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		7.0	4.5	10.0	4.0	12.0	5.0	2.5	7.2	2.5	9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_N		7.0	6.5	15.0	7.0	15.0	6.0	2.5	8.7	2.5	11.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_N		8.0	3.5	11.0	4.0	15.0	5.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_N		5.5	2.0	7.0	3.0	9.0	4.0	1.5	5.5	1.5	6.5	ns
t_S	Setup Time HIGH or LOW S_0 or S_1 to CP		2.0	8.5	—	8.5	—	2.5	4.0	—	5.0	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		0	0	—	0	—	-1.5	0	—	0	—	ns
t_S	Setup Time HIGH or LOW, I/O_N, DS_0 or DS_7 to CP		0.5	5.5	—	5.5	—	2.5	4.0	—	5.0	—	ns
t_S	Hold Time HIGH or LOW, I/O_N, DS_0 or DS_7 to CP		0	2.0	—	2.0	—	1.0	2.0	—	2.0	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	7.0	—	7.0	—	4.0	5.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	7.0	—	7.0	—	4.0	5.0	—	6.0	—	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP		7.0	7.0	—	7.0	—	4.0	5.0	—	6.0	—	ns

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT373
IDT54/74FCT373A

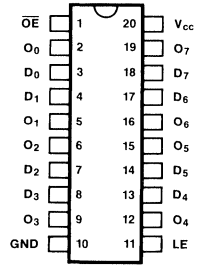
FEATURES:

- IDT54/74FCT373 equivalent to FAST™ speed; **IDT54/74FCT373A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes.
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

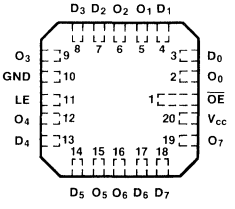
The IDT54/74FCT373 and IDT54/74FCT373A are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSD54/74FCT373-001

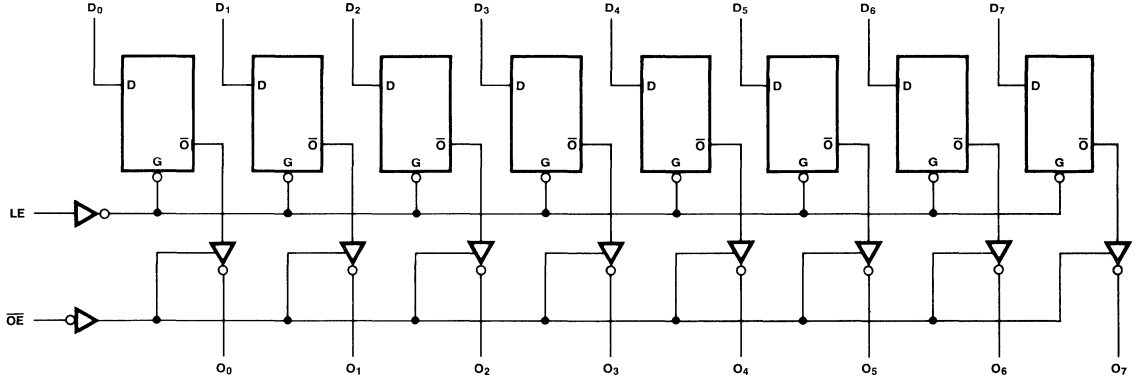
DIP/SOIC
TOP VIEW



SSD54/74FCT373-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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SSD54/74FCT373-003

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5

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.6	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0-O_7	3-State Latch Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT373					IDT54/74FCT373A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pf R_L = 500Ω	5.0	2.0	8.0	2.0	8.5	4.0	1.5	5.2	1.5	5.6	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	12.0	2.0	13.5	5.5	1.5	6.5	1.5	7.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.5	2.0	10.0	4.0	1.5	5.5	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		9.0	3.0	13.0	3.0	15.0	7.0	2.0	8.5	2.0	9.8	ns
t_S	Set up Time HIGH or LOW D_n to LE		1.0	2.0	—	2.0	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.0	3.0	—	3.0	—	1.0	1.8	—	1.8	—	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	—	6.0	—	4.0	6.0	—	5.0	—	ns

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTER (3-STATE)

IDT54/74FCT374
IDT54/74FCT374A

FEATURES:

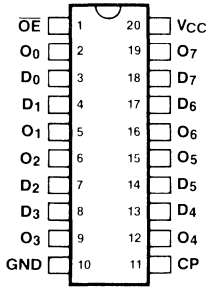
- IDT54/74FCT374 equivalent to FAST™ speed; **IDT54/74FCT374A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Positive, edge-triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/75FCT374 and IDT54/74FCT374A are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the setup and hold time requirements of the D inputs is transferred the the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS



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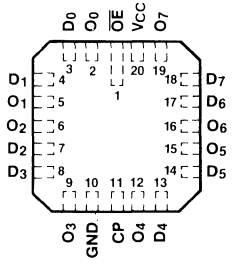
DIP/SOIC TOP VIEW



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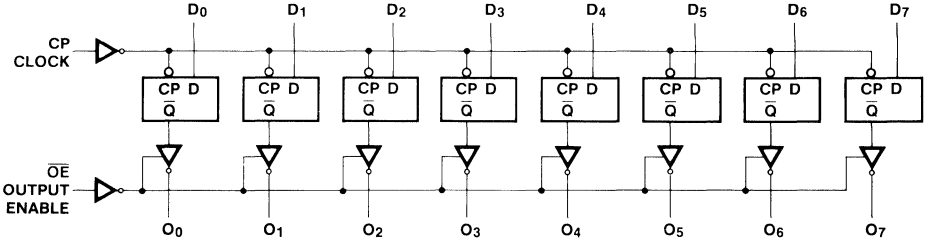
LCC/PLCC TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT374-003

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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
O_0-O_7	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	O_N	O_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	H
	L	↑	H	L	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT374					IDT54/74FCT374A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pf R_L = 500Ω	6.6	4.0	10.0	4.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	12.5	2.0	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	8.0	2.0	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_S	Set Up Time HIGH or LOW D_N to CP		1.0	2.0	—	2.5	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	2.0	—	2.5	—	0.5	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	—	7.0	—	4.0	5.0	—	6.0	—	ns

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377
IDT54/74FCT377A

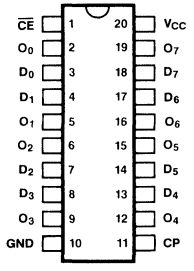
FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed; **IDT54/74FCT377A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with clock enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

The IDT54/74FCT377 and IDT54/74FCT377A are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT377 and IDT54/74FCT377A have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

PIN CONFIGURATIONS



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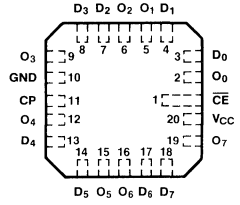
DIP/SOIC
TOP VIEW



SSD54/74FCT377-002

LCC/PLCC
TOP VIEW

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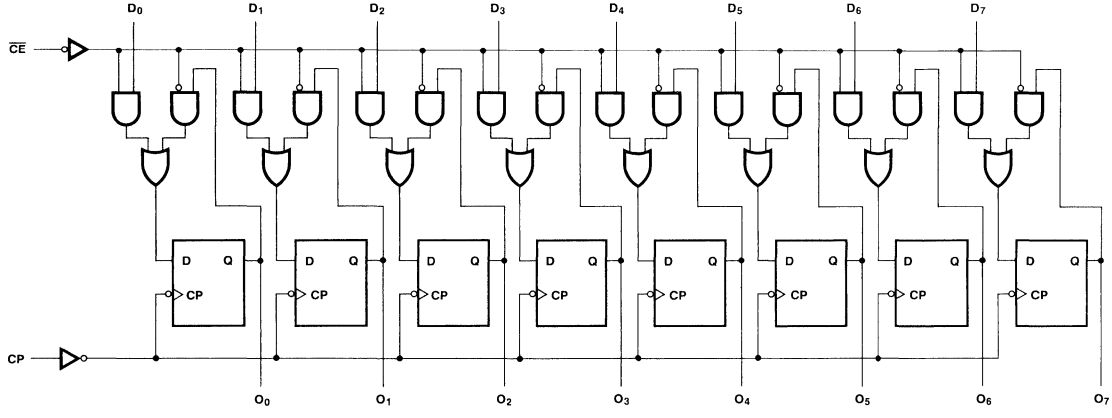
FUNCTIONAL BLOCK DIAGRAM



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CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	3.0	0.5	
			I_{OL} = 48mA COM'L.	—	3.0	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{CE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O_0-O_7	Data Outputs
CP	Clock Pulse Input

TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_N	O_N
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't care
↑ = LOW-to-HIGH Clock Transition

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT377					IDT54/74FCT377A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_N	C_L = 50pf R_L = 500Ω	7.0	3.0	13.0	3.0	15.0	5.0	2.0	7.2	2.0	8.3	ns
t_S	Set Up Time HIGH or LOW D_N to CP		1.0	2.5	—	3.0	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		1.0	2.0	—	2.5	—	1.0	1.5	—	1.5	—	ns
t_S	Set Up Time HIGH or LOW $\overline{CE}$ to CP		1.5	3.0	—	3.0	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		3.0	4.0	—	5.0	—	1.0	2.0	—	2.0	—	ns
t_W	Clock Pulse Width, LOW		4.0	7.0	—	7.0	—	4.0	—	—	—	—	ns

Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521
IDT54/74FCT521A

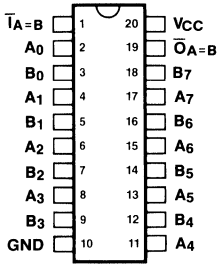
FEATURES:

- IDT54/74FCT521 7.0ns typical propagation delay; **IDT54/74FCT521A 5.5ns typical propagation delay**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- 8-bit identity comparator
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

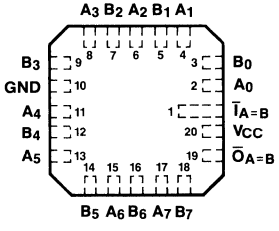
The IDT54/74FCT521 and IDT54/74FCT521A are 8-bit identity comparators built using advanced CEMOS™, a dual metal CMOS technology. The devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

PIN CONFIGURATIONS



SSDFCT521-001

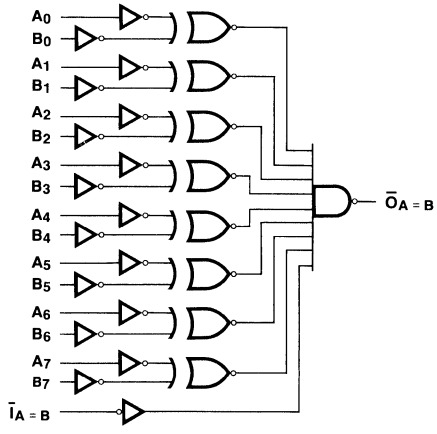
DIP/SOIC
TOP VIEW



SSDFCT521-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT521-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
A_0-A_7	Word A inputs
B_0-B_7	Word B inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active Low)

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT521					IDT54/74FCT521A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	C_L = 50pf R_L = 500Ω	7.0	3.5	11.0	3.5	15.0	5.5	1.5	7.2	1.5	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		5.0	3.0	10.0	3.0	9.0	4.4	1.5	6.0	1.5	7.8	ns

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCH (3-STATE)

IDT54/74FCT533
IDT54/74FCT533A

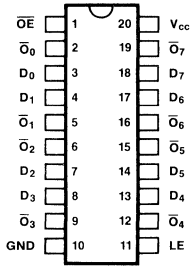
FEATURES:

- IDT54/74FCT533 6.0ns typical clock to output; **IDT54/74FCT533A 4.0ns typical clock to output**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

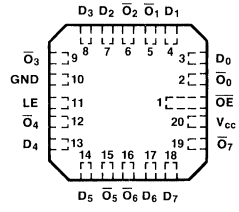
The IDT54/74FCT533 and IDT54/74FCT533A are octal transparent latches built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT533 and IDT54/74FCT533A consist of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS



SSD54/74FCT533-001

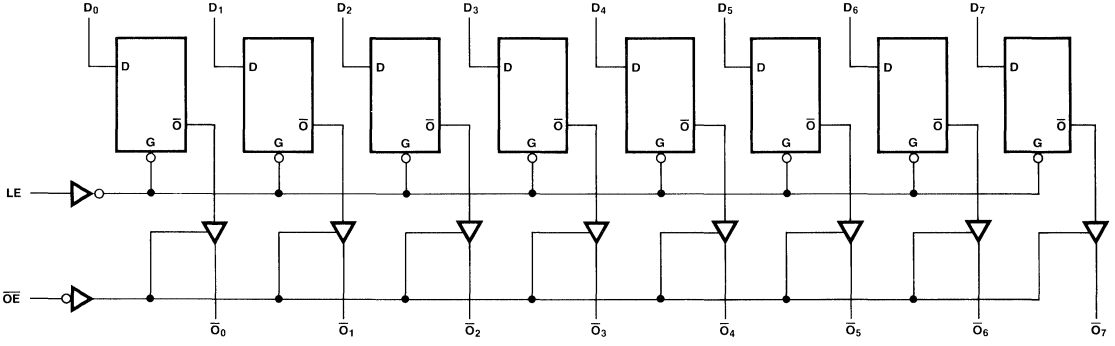
DIP/SOIC
TOP VIEW



SSD54/74FCT533-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT533-003

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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.6	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
$\overline{LE}$	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

INPUTS		OUTPUTS	
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT533					IDT54/74FCT533A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	6.0	3.0	10.0	3.0	12.0	4.0	1.5	5.2	1.5	5.6	ns
t_{ZH} t_{ZL}	Output Enable Time		8.0	2.0	11.0	2.0	12.5	5.5	1.5	6.5	1.5	7.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.0	2.0	8.5	4.0	1.5	5.5	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_N$		9.0	3.0	13.0	3.0	14.0	7.0	2.0	8.5	2.0	9.8	ns
t_S	Set Up Time HIGH or LOW D_N to LE		1.0	2.0	—	2.0	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to LE		1.0	3.0	—	3.0	—	1.0	1.8	—	1.8	—	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	—	6.0	—	4.0	5.0	—	6.0	—	ns

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Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54/74FCT534
IDT54/74FCT534A

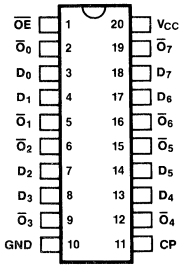
FEATURES:

- IDT54/74FCT534 6.5ns typical clock to output; **IDT54/74FCT534A 4.5ns typical clock to output**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal D flip-flop with 3-state output
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

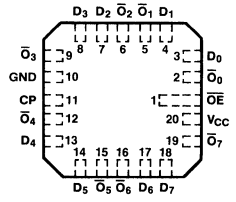
The IDT54/74FCT534 and IDT54/74FCT534A are octal D flip-flops built using advanced CEMOS™, a dual metal CMOS technology. The IDT54/74FCT534 and IDT54/74FCT534A are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

PIN CONFIGURATIONS



SSDFCT534-001

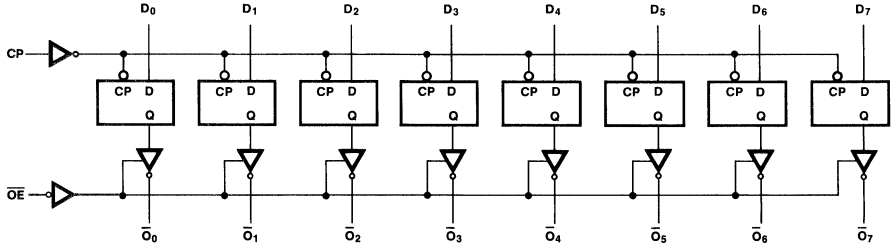
DIP/SOIC
TOP VIEW



SSDFCT534-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDFCT534-003

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	0.3	0.5	
			I_{OL} = 48mA COM'L.	—	0.3	0.5	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} = \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_7$	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	$\overline{O}_N$	Q_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	H	H
	L	↑	H	L	L
	H	↑	L	Z	H
	H	↑	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT534					IDT54/74FCT534A					UNITS
			TYPICAL	COMMERCIAL		MILITARY		TYPICAL	COMMERCIAL		MILITARY		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_N$	C_L = 50pf R_L = 500Ω	6.5	4.0	10.0	4.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	12.5	2.0	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	8.0	2.0	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_S	Set Up Time HIGH or LOW D_N to CP		1.0	2.0	—	2.5	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	2.0	—	2.5	—	1.0	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	—	7.0	—	4.0	5.0	—	6.0	—	ns

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Integrated Device Technology, Inc.

FAST™ CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT573
IDT54/74FCT573A

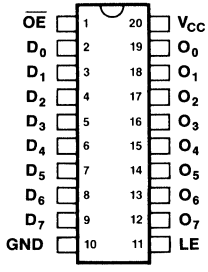
FEATURES:

- IDT54/74FCT573 equivalent to FAST™ speed; **IDT54/74FCT573A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes.
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Octal transparent latch with enable
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

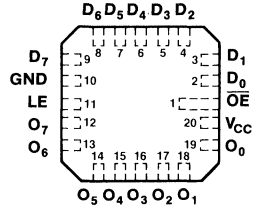
DESCRIPTION:

The IDT54/74FCT573 and IDT54/74FCT573A are 8-bit latches built using advanced CEMOS™, a dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus-oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

PIN CONFIGURATIONS

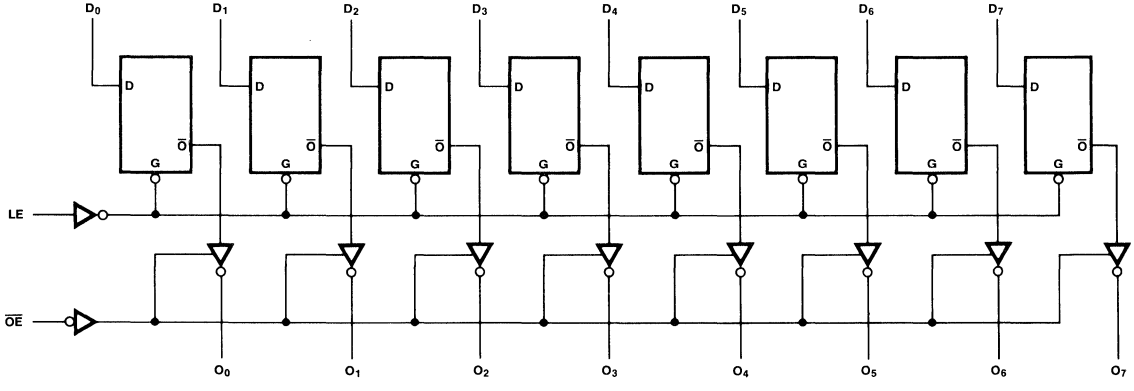


DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Input Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V or V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25° C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0-O_7	3-State Latch Outputs

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT573					IDT54/74FCT573A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	C_L = 50pf R_L = 500Ω	5.0	2.0	8.0	2.0	8.5	4.0	1.5	5.2	1.5	5.6	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	12.0	2.0	13.5	5.5	1.5	6.5	1.5	7.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	7.5	2.0	10.0	4.0	1.5	5.5	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_n		9.0	3.0	13.0	3.0	15.0	7.0	2.0	8.5	2.0	9.8	ns
t_S	Set up Time HIGH or LOW D_n to LE		1.0	2.0	—	2.0	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_n to LE		1.0	3.0	—	3.0	—	1.0	1.8	—	1.8	—	ns
t_W	LE Pulse Width HIGH or LOW		5.0	6.0	—	6.0	—	4.0	6.0	—	5.0	—	ns

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Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTER (3-STATE)

IDT54/74FCT574
IDT54/74FCT574A

FEATURES:

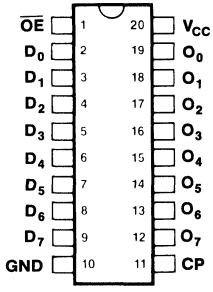
- IDT54/74FCT574 equivalent to FAST™ speed; **IDT54/74FCT574A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 32mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Positive, edge-triggered master/slave, D-type flip-flops
- Buffered common clock and buffered common three-state control
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

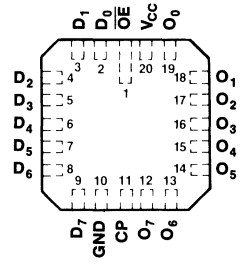
The IDT54/74FCT574 and IDT54/74FCT574A are 8-bit registers built using advanced CEMOS™, a dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state conditions.

Input data meeting the setup and hold time requirements of the D inputs is transferred the the O outputs on the LOW-to-HIGH transition of the clock input.

PIN CONFIGURATIONS

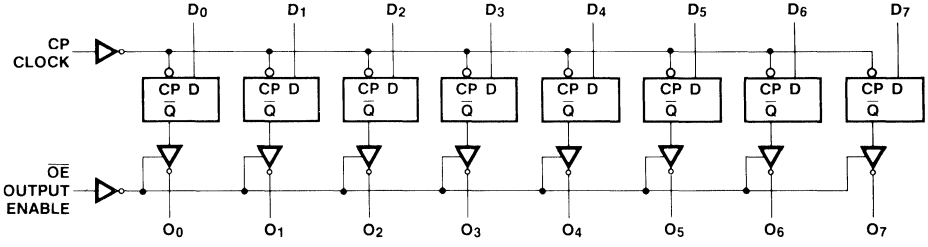


DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSDAHCT374-003

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial) V_{LC} = 0.2V
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military) V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL	2.4	4.3	—	
			I_{OH} = -15mA COM	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL	—	0.3	0.5	
			I_{OL} = 48mA COM	—	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.4V	—	—	-40	µA
			V_O = 2.4V	—	—	40	

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D_0-D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	3-State Output Enable Input (Active LOW)
O_0-O_7	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_I	O_N	O_I
Hi-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↓	L	H	H
	L	↓	H	L	L
	H	↓	L	Z	H
	H	↓	H	Z	L

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
↓ = LOW-to-HIGH transition
NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT574					IDT54/74FCT574A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pf R_L = 500Ω	6.6	4.0	10.0	4.0	11.0	4.5	2.0	6.5	2.0	7.2	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	12.5	2.0	14.0	5.5	1.5	6.5	1.5	7.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	8.0	2.0	8.0	4.0	1.5	5.5	1.5	6.5	ns
t_S	Set Up Time HIGH or LOW D_N to CP		1.0	2.0	—	2.5	—	1.0	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		0.5	2.0	—	2.5	—	0.5	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		4.0	7.0	—	7.0	—	4.0	5.0	—	6.0	—	ns

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Integrated Device Technology, Inc.

FAST CMOS OCTAL INVERTING BUFFER TRANSCEIVER

IDT54/74FCT640
IDT54/74FCT640A

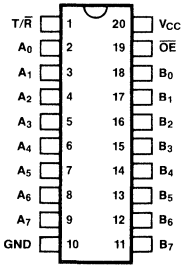
FEATURES:

- IDT54/74FCT640 6.0ns typical data to output; **IDT54/74FCT640A 3.5ns typical data to output**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes.
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than FAST™ (5μA max.)
- Inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

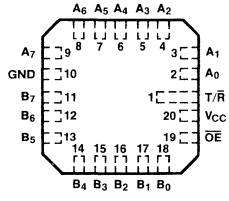
The IDT54/74FCT640 and IDT54/74FCT640A are 8-bit inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These octal bus transceivers are designed for asynchronous two-way communication between data busses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control (T/$\overline{R}$) input. The enable input ($\overline{OE}$) can be used to disable the device so the busses are effectively isolated.

PIN CONFIGURATIONS



SSD54/74FCT640-001

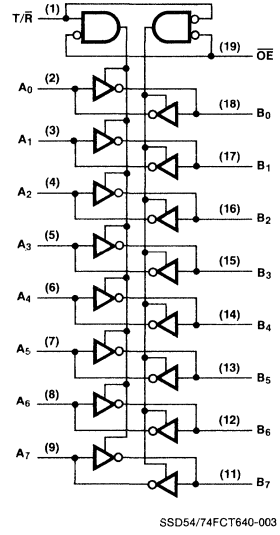
DIP/SOIC
TOP VIEW



SSD54/74FCT640-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT640-003

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FAST is a trademark of Fairchild Semiconductor Co.

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
$V_{HC} = V_{CC}$ - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	μA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32μA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300μA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300μA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300μA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	
$V^+ - V^-$	Hysteresis	On A_i and B_i		—	0.4	—	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V or V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT640					IDT54/74FCT640A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50pF R_L = 500Ω	6.0	2.0	7.0	2.0	8.0	3.5	1.5	5.0	1.5	5.3	ns
t_{ZH} t_{ZL}	Output Enable Time		7.0	2.0	10.0	2.0	12.0	4.5	1.5	5.0	1.5	6.0	ns
t_{HZ} t_{LZ}	Output Disable Time		11.0	2.0	13.0	2.0	16.0	4.8	1.5	6.2	1.5	6.5	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B[1]		7.0	—	—	—	—	5.0	—	—	—	—	ns

NOTE:

1. Guaranteed by design.

5

Integrated Device Technology, Inc.

FAST CMOS NON-INVERTING BUFFER TRANSCEIVER

IDT54/74FCT645
IDT54/74FCT645A

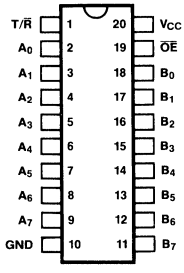
FEATURES:

- IDT54/74FCT645 equivalent to FAST™ speed; **IDT54/74FCT645A 35% faster than FAST™**
- Equivalent to FAST™ output drive over full temperature and voltage supply extremes
- I_{OL} = 48mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Substantially lower input current levels than FAST™ (5μA max.)
- Non-inverting buffer transceiver
- 100% product assurance screening to MIL-STD-883, Class B is available
- JEDEC standard pinout for DIP and LCC

DESCRIPTION:

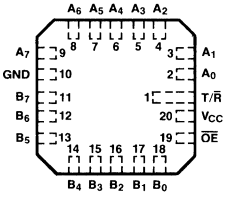
The IDT54/74FCT645 and IDT54/74FCT645A are 8-bit non-inverting buffer transceivers built using advanced CEMOS™, a dual metal CMOS technology. These non-inverting buffer transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending upon the level at the direction control ($\overline{T}/R$) input. The enable input ($\overline{OE}$) can be used to disable the device so the buses are effectively isolated.

PIN CONFIGURATIONS



SSD54/74FCT645-001

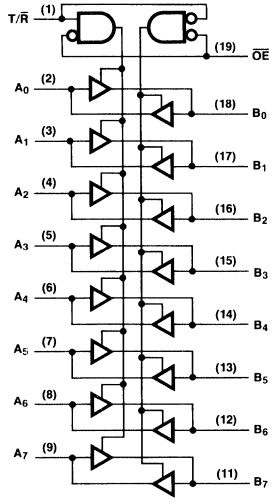
DIP/SOIC
TOP VIEW



SSD54/74FCT645-002

LCC/PLCC
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



SSD54/74FCT645-003

CEMOS is a trademark of Integrated Device Technology, Inc.
FAST is a trademark of Fairchild Semiconductor Co.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level (Except I/O Pins)	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	—	
			I_{OH} = -12mA MIL.	2.4	4.3	—	
			I_{OH} = -15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 48mA MIL.	—	0.3	0.55	
			I_{OL} = 64mA COM'L.	—	0.3	0.55	
$V^+ - V^-$	Hysteresis	On A_i and B_i		—	0.4	—	V

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

FUNCTION TABLE

INPUTS		OPERATIONS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION	IDT54/74FCT645					IDT54/74FCT645A					UNITS
			TYP.	COM'L.		MIL.		TYP.	COM'L.		MIL.		
				MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay A to B or B to A	C_L = 50pF R_L = 500Ω	6.0	2.0	9.5	2.0	11.0	3.3	1.5	4.6	1.5	4.9	ns
t_{ZH} t_{ZL}	Output Enable Time		9.0	2.0	11.0	2.0	12.0	4.8	1.5	6.2	1.5	6.5	ns
t_{HZ} t_{LZ}	Output Disable Time		6.0	2.0	12.0	2.0	13.0	4.5	1.5	5.0	1.5	6.0	ns
t_{DLH} t_{DHL}	Propagation Delay T/$\overline{R}$ to A or B[1]		6.0	—	—	—	—	5.0	—	—	—	—	ns

NOTE:

1. Guaranteed by design.

5

Integrated Device Technology, Inc.

HIGH-PERFORMANCE BUS INTERFACE REGISTERS

IDT54/74FCT821-26B

FEATURES:

- **35% faster than AMD's Am29821-26 series**
- Equivalent to AMD's Am29821-26 bipolar registers in pinout/function and output drive over full temperature and voltage supply extremes
- High-speed parallel registers with positive edge-triggered D-type flip-flops
  — Non-inverting CP-Y t_{PD} = 5.0ns typ.
  — Inverting CP-Y t_{PD} = 5.0ns typ.
- Buffered common Clock Enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on clock INPUT
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
  — 6pF inputs (typ.)
  — 8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Military product available 100% screened to MIL-STD-883, Class B

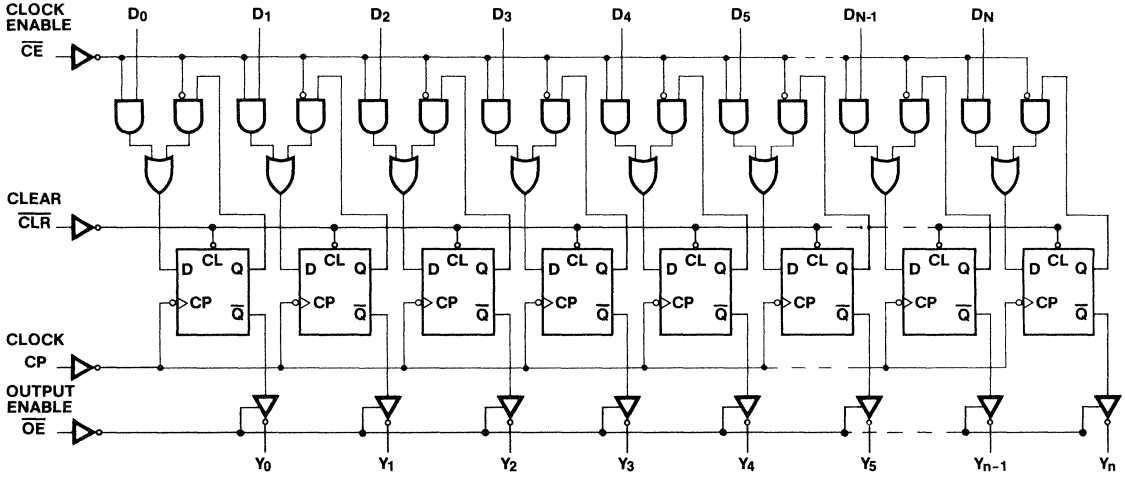
DESCRIPTION:

The IDT54/74FCT800B Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT800B Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or busses carrying parity. The IDT54/74FCT821B and IDT54/74FCT822B are buffered, 10-bit wide versions of the popular '374/'534 functions. The IDT54/74FCT823B and IDT54/74FCT824B are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$—ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825B and IDT54/74FCT826B are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800B high-performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



SSD39C821-001

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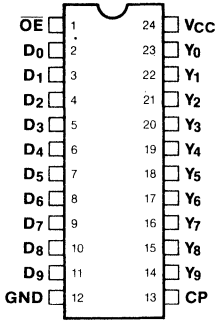
Printed in the U.S.A.

PIN CONFIGURATIONS

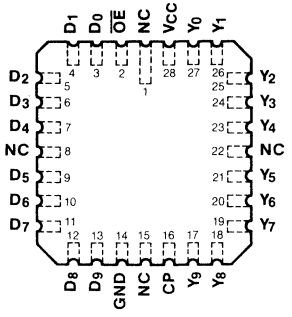
LOGIC SYMBOLS

IDT54/74FCT821B/IDT54/74FCT822B 10-BIT REGISTERS



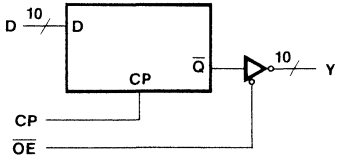
DIP
TOP VIEW

SSD39C821-005



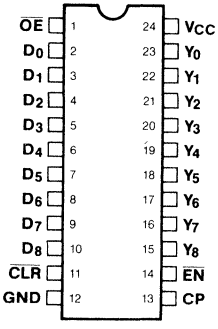
LCC
TOP VIEW

SSD39C821-006



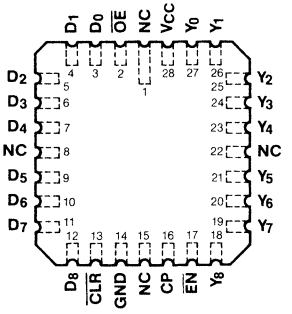
SSD39C821-002

IDT54/74FCT823B/IDT54/74FCT824B 9-BIT REGISTERS



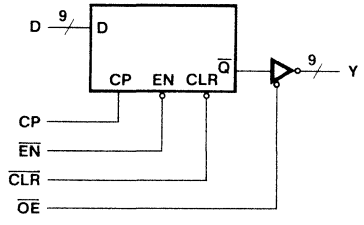
DIP
TOP VIEW

SSD39C821-007



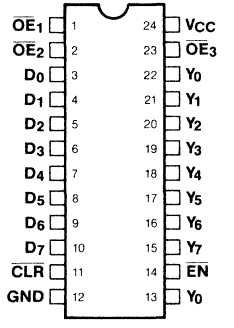
LCC
TOP VIEW

SSD39C821-008



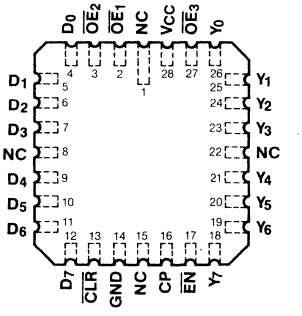
SSD39C821-003

IDT54/74FCT825B/IDT54/74FCT826B 8-BIT REGISTERS



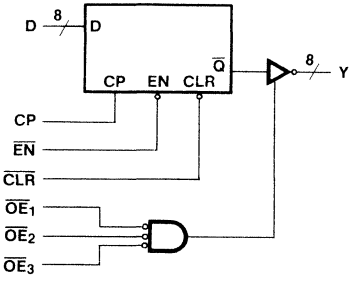
DIP
TOP VIEW

SSD39C821-009



LCC
TOP VIEW

SSD39C821-010



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5

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D_i	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and noninverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_i, $\overline{Y_i}$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

PRODUCT SELECTOR GUIDE

	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	IDT54/74 FCT821B	IDT54/74 FCT823B	IDT54/74 FCT825B
Inverting	IDT54/74 FCT822B	IDT54/74 FCT824B	IDT54/74 FCT826B

FUNCTION TABLES

IDT54/74FCT821/23/25B

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i	
H	X	L	L	↑	L	Z	Hi-Z
H	X	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

IDT54/74FCT822/24/26B

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	$\overline{Y_i}$	
H	X	L	L	↑	H	Z	Hi-Z
H	X	L	H	↑	L	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	H	Z	Load
H	H	L	H	↑	L	Z	
L	H	L	L	↑	H	H	
L	H	L	H	↑	L	L	

H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	Min. = 4.75V	Max. = 5.25V (Commercial)
T_A = -55°C to +125°C	V_{CC} = 5.0V ± 10%	Min. = 4.50V	Max. = 5.50V (Military)

V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on Clock Only	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	—	2.0	5.6	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.75	7.8	
			V_{IN} = 3.4V or V_{IN} = GND	—	6.0	15.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
				MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay Clock to Y_i (OE = LOW)		C_L = 50pF R_L = 500Ω	—	7.5	3.5	8.5	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	7.5	3.5	8.5	ns
t_S	Data to CP Setup Time		C_L = 50pF R_L = 500Ω	3.0	—	3.0	—	ns
t_H	Data to CP Hold Time			1.5	—	1.5	—	ns
t_S	Enable ($\overline{EN}$ ⌐⌐) to CP Setup Time			3.0	—	3.0	—	ns
t_S	Enable ($\overline{EN}$ ⌐⌐) to CP Setup Time			3.0	—	3.0	—	ns
t_H	Enable ($\overline{EN}$) Hold Time			0	—	0	—	ns
t_{PHL}	Propagation Delay, Clear to Y_i			—	9.0	—	9.5	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐⌐) Time			6.0	—	6.0	—	ns
t_{PWH}	Clock Pulse Width	HIGH		6.0	—	6.0	—	ns
t_{PWL}		LOW		6.0	—	6.0	—	ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			6.0	—	6.0	—	ns
t_{ZH} t_{ZL}	Output Enable Time $\overline{OE}$ ⌐⌐ to Y_i		C_L = 300pF R_L = 500Ω	—	8.0	—	8.0	ns
t_{ZH} t_{ZL}			C_L = 50pF R_L = 500Ω	—	8.0	—	8.0	ns
t_{HZ} t_{LZ}	Output Disable Time $\overline{OE}$ ⌐⌐ to Y_i		C_L = 50pF R_L = 500Ω	—	6.5	—	7.0	ns
t_{HZ}[2] t_{LZ}			C_L = 5pF[2] R_L = 500Ω	—	6.5	—	7.0	ns

NOTES:
1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

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Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

IDT54/74FCT841-46B

FEATURES:

- **35% faster than AMD's Am29841-46 series**
- Equivalent to AMD's Am29841-46 Bipolar Registers in pinout/function, and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  —Non-inverting transparent t_{PD} = 4.0ns typ.
  —Inverting transparent t_{PD} = 4.5ns typ.
- Buffered common latch enable, clear and preset input
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on latch enable input
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
  —6pF inputs (typ.)
  —8pF outputs (typ.)
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar AM29800 Series (5μA max.)
- Military product available 100% screened to MIL-STD-883, Class B

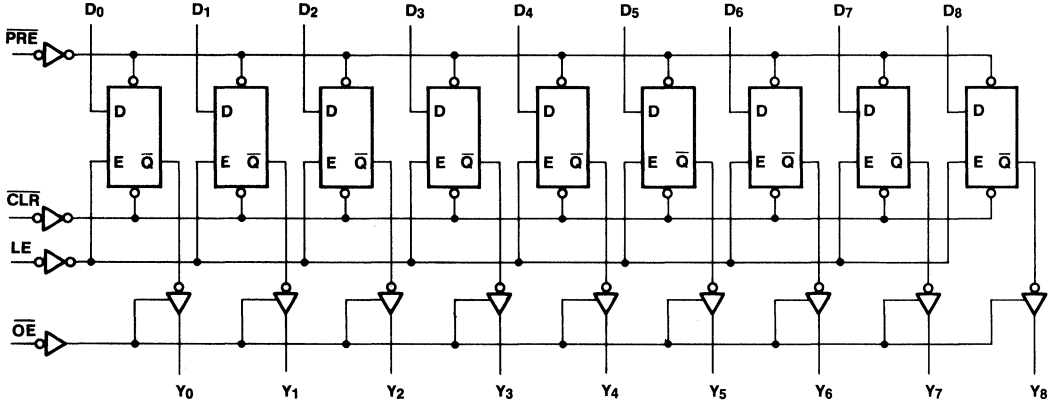
DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT840B Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841B and IDT54/74FCT842B are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843B and IDT54/74FCT844B are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$)—ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845B and IDT54/74FCT846B are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g. $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the IDT54/74FCT800B high-performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



DSR39C841-001

PRODUCT SELECTOR GUIDE

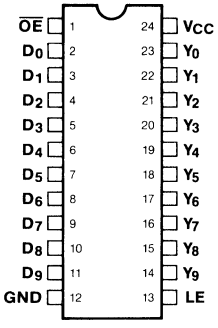
	DEVICE		
	10-BIT	**9-BIT**	**8-BIT**
Non-inverting	IDT54/74 FCT841B	IDT54/74 FCT843B	IDT54/74 FCT845B
Inverting	IDT54/74 FCT842B	IDT54/74 FCT844B	IDT54/74 FCT846B

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

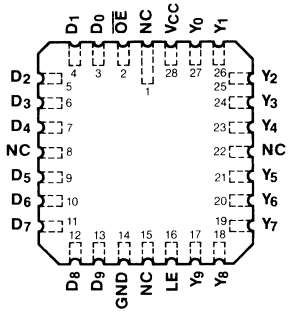
LOGIC SYMBOLS

IDT54/74FCT841B/IDT54/74FCT842B 10-BIT LATCHES



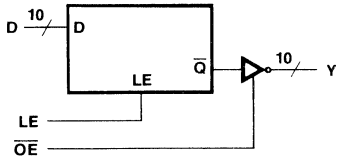
DIP
TOP VIEW

DSR39C841-005



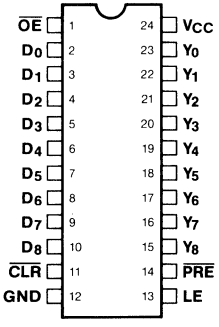
LCC
TOP VIEW

DSR39C841-006



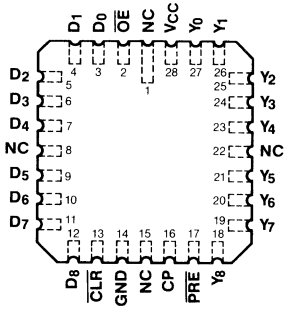
DSR39C841-002

IDT54/74FCT843B/IDT54/74FCT844B 9-BIT LATCHES



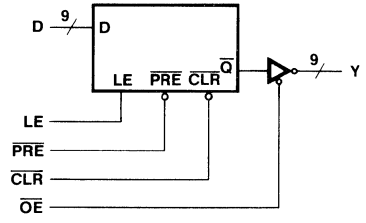
DIP
TOP VIEW

DSR39C841-007



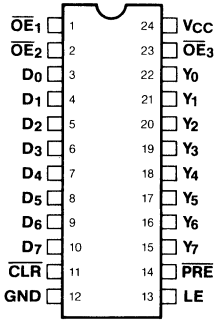
LCC
TOP VIEW

DSR39C841-008



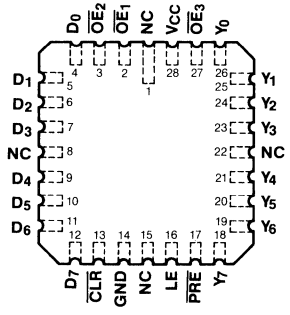
DSR39C841-003

IDT54/74FCT845B/IDT54/74FCT846B 8-BIT LATCHES



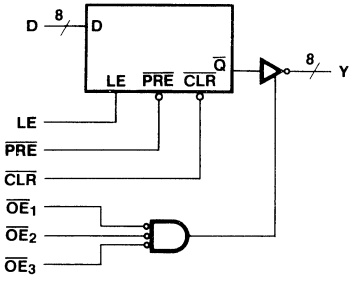
DIP
TOP VIEW

DSR39C841-009



LCC
TOP VIEW

DSR39C841-010



DSR39C841-004

5

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT841/43/45B (Non-inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_i	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.
IDT54/74FCT842/44/46B (Inverting)		
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_i	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_i	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLES

IDT54/74FCT841/43/45B

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

IDT54/74FCT842/44/46B

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on Latch Enable Only	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

5

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC} \leq$; $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETERS	DESCRIPTION		TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{PLH} (IDT54/74FCT41B,43B,45B) t_{PHL}	Data (D_i) to Output (Y_i) (LE = HIGH)		C_L = 50pF R_L = 500Ω	—	6.5	—	7.5	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	6.5	—	7.5	ns
t_S	Data to LE Setup Time		C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time			2.5	—	2.5	—	ns
t_{PLH} (IDT54/74FCT42B,44B,46B) t_{PHL}	Data (D_i) to Output (Y_i) (LE = HIGH)		C_L = 50pF R_L = 500Ω	—	8.0	—	9.0	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	8.0	—	9.0	ns
t_S	Data to LE Setup Time		C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time			2.5	—	2.5	—	ns
t_{PLH} t_{PHL}	Latch Enable (LE) to Y_i		C_L = 50pF R_L = 500Ω	—	8.0	—	10.5	ns
t_{PLH} t_{PHL}			C_L = 300pF R_L = 500Ω	—	8.0	—	9.0	ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50pF R_L = 500Ω	—	8.0	—	10.0	ns
t_S	Preset recovery ($\overline{PRE}$ ⌐) Time			—	10.0	—	13.0	ns
t_{PHL}	Propagation$_i$Delay, Clear to Y			—	10.0	—	11.0	ns
t_S	Clear Recovery ($\overline{CLR}$ ⌐) Time			10.0	—	10.0	—	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF R_L = 500Ω	4.0	—	4.0	—	ns
t_{PWL}	Preset Pulse Width	LOW		4.0	—	4.0	—	ns
t_{PWL}	Clear Pulse Width	LOW		4.0	—	4.0	—	ns
t_{ZH} t_{ZL}	Output Enable Time ($\overline{OE}$ ⌐) Time		C_L = 300pF R_L = 500Ω	—	8.0	—	8.5	ns
t_{ZH} t_{ZL}			C_L = 50pF R_L = 500Ω	—	8.0	—	8.5	ns
t_{HZ} t_{LZ}	Output Disable Time ($\overline{OE}$ ⌐) Time		C_L = 50pF R_L = 500Ω	—	7.0	—	7.5	ns
t_{HZ}[2] t_{LZ}			C_L = 5pF R_L = 500Ω	—	7.0	—	7.5	ns

NOTES:

1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

5

Integrated Device Technology, Inc

HIGH-PERFORMANCE CMOS BUS TRANSCEIVERS

IDT54/74FCT861-64B

FEATURES:

- **35% faster than AMD's Am29861-64 series**
- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function and output drive over full temperature and voltage supply extremes
- High-speed symmetrical bidirectional transceivers
  —Non-inverting t_{PD} = 3.5ns typ.
  —Inverting t_{PD} = 4.0ns typ.
- 48mA commercial I_{OL}, 32mA military I_{OL}
- 200mV (typ.) hysteresis on T and R buses
- Clamp diodes on all inputs for ringing suppression
- ESD protection 5000V (typ.) — MIL-STD-883 Category B
- Low input/output capacitance
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series (5μA max.)
- Military product available 100% screened to MIL-STD-883, Class B

DESCRIPTION:

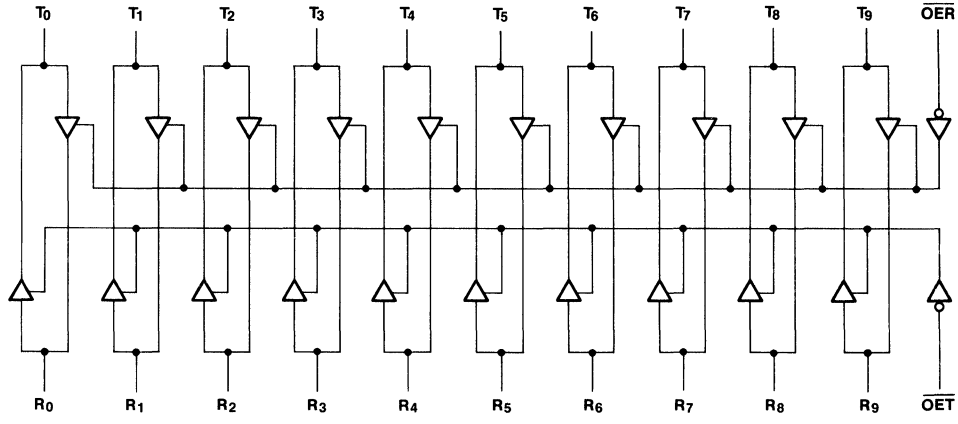
The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT860 Series bus transceivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The IDT54/74FCT863B and IDT54/74FCT864B 9-bit transceivers have NORed output enables for maximum control flexibility.

All of the IDT54/74FCT800B high-performance interface family are designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes, and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT861B/IDT54/74FCT862B 10-BIT TRANSCEIVERS



SSD39C861-001

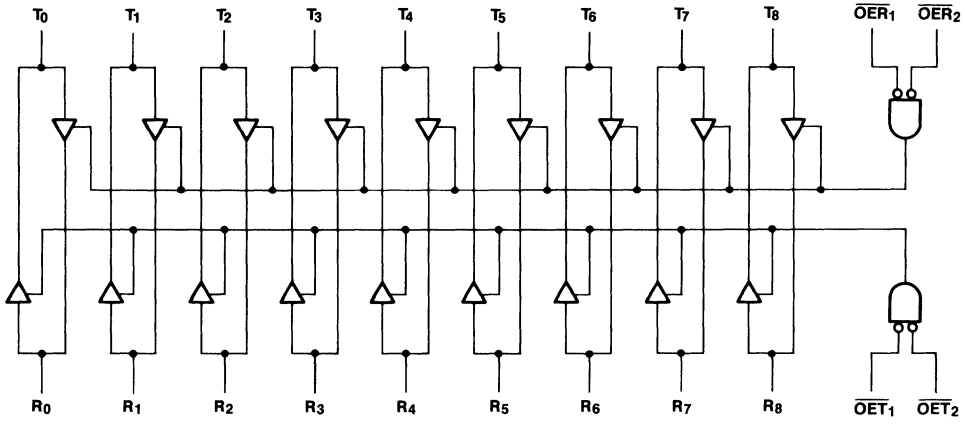
PRODUCT SELECTOR GUIDE

	DEVICE	
	10-BIT	**9-BIT**
Non-inverting	IDT54/74FCT861B	IDT54/74FCT863B
Inverting	IDT54/74FCT862B	IDT54/74FCT864B

CEMOS is a trademark of Integrated Device Technology, Inc.

FUNCTIONAL BLOCK DIAGRAM

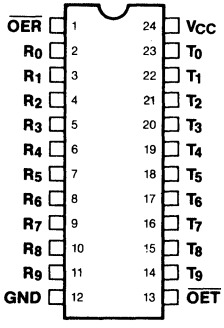
IDT54/74FCT863B/IDT54/74FCT864B 9-BIT TRANSCEIVERS



SSD39C861-004

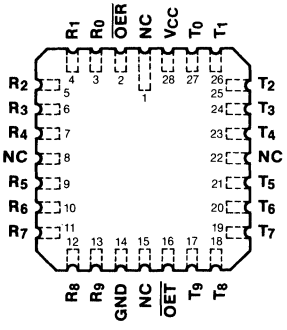
PIN CONFIGURATIONS

IDT54/74FCT861B/IDT54/74FCT862B 10-BIT TRANSCEIVERS



DIP
TOP VIEW

SSD39C861-005

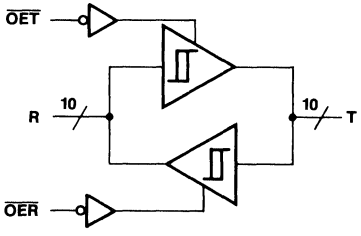


LCC
TOP VIEW

SSD39C861-006

LOGIC SYMBOLS

IDT54/74FCT861B



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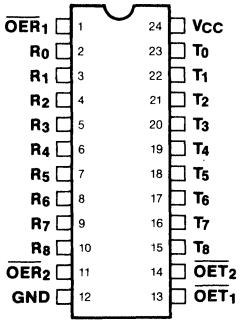
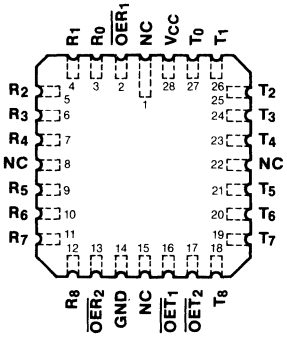
IDT54/74FCT863B/IDT54/74FCT864B 9-BIT TRANSCEIVERS



DIP
TOP VIEW

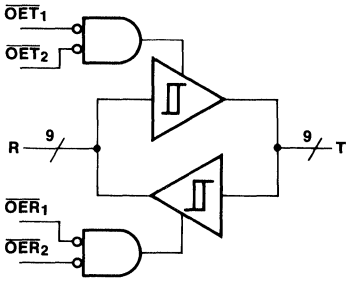
SSD39C861-007



LCC
TOP VIEW

SSD39C861-008

IDT54/74FCT863B



SSD39C861-003

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
IDT54/74FCT861/62B		
$\overline{OER}$	I	When LOW in conjunction with $\overline{OET}$ HIGH activates the RECEIVE mode.
$\overline{OET}$	I	When LOW in conjunction with $\overline{OER}$ HIGH activates the TRANSMIT mode.
R_i	I/O	10-bit RECEIVE input/output.
T_i	I/O	10-bit TRANSMIT input/output.
IDT54/74FCT863/64B		
$\overline{OER}_i$	I	When LOW in conjunction with $\overline{OET}_i$ HIGH activates the RECEIVE mode.
$\overline{OET}_i$	I	When LOW in conjunction with $\overline{OER}_i$ HIGH activates the TRANSMIT mode.
R_i	I/O	9-bit RECEIVE input/output.
T_i	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLES

IDT54/74FCT861B/IDT54/74FCT863B (Non-inverting)

INPUTS				OUTPUTS		FUNCTION
OER	OER	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

IDT54/74FCT862B/IDT54/74FCT864B (Inverting)

INPUTS				OUTPUTS		FUNCTION
OER	OER	R_i	T_i	R_i	T_i	
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min. = 4.75V Max. = 5.25V (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		—	—	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		—	—	-5	µA
V_I	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V	—	—	-10	µA
			V_O = 2.4V	—	—	10	
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -250µA	V_{HC}	V_{CC}	—	
			I_{OH} = -15mA MIL.	2.4	4.0	—	
			I_{OH} = -24mA COM.	2.0	3.5	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}	
			I_{OL} = 32mA MIL.	—	—	0.5	
			I_{OL} = 48mA COM.	—	—	0.5	
V_H	Input Hysteresis on R_i and T_i	—		—	200	—	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ f_i = 0		—	0.001	1.5	mA
I_{CCT}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.6	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND T/$\overline{R}$ = GND or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_{CC}	Total Power Supply[4] Current	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.8	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.9	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT}D_HN_T + I_{CCD}(f_{CP}/2 + f_iN_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

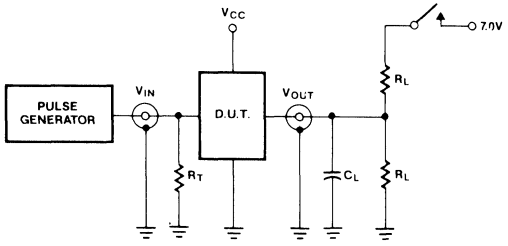
PARAMETERS	DESCRIPTION	TEST CONDITIONS[1]	COMMERCIAL		MILITARY		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from R_i to T_i or T_i to R_i IDT54/74FCT861B/IDT54/74FCT863B (Non-inverting)	C_L = 50pF R_L = 500Ω	—	5.0	—	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF R_L = 500Ω	—	5.0	—	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay from R_i to T_i or T_i to R_i IDT54/74FCT862B/IDT54/74FCT863B (Inverting)	C_L = 50pF R_L = 500Ω	—	5.5	—	6.5	ns
t_{PLH} t_{PHL}		C_L = 300pF R_L = 500Ω	—	5.5	—	6.5	ns
t_{ZH} t_{ZL}	Output Enable Time OET to T_i or OER to R_i	C_L = 50pF R_L = 500Ω	—	8.0	—	9.0	ns
t_{ZH} t_{ZL}		C_L = 300pF R_L = 500Ω	—	8.0	—	9.0	ns
t_{ZH}[2] t_{ZL}	Output Enable Time OET to T_i or OER to R_i	C_L = 5pF R_L = 500Ω	—	7.0	—	8.0	ns
t_{ZH} t_{ZL}		C_L = 50pF R_L = 500Ω	—	7.0	—	8.0	ns

NOTE:

1. See test circuit and waveforms.
2. This parameter guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR THREE-STATE OUTPUTS



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SWITCH POSITION

TEST	SWITCH
t_{LZ}	Closed
t_{ZL}	Closed
All Other	Open

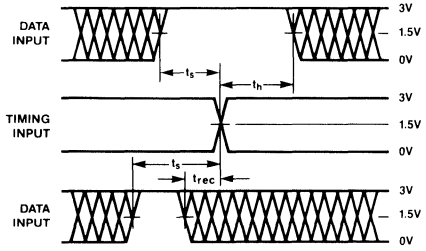
DEFINITIONS

R_L = Load resistor: see AC CHARACTERSICS for value.

C_L = Load capacitance includes jig and probe capacitance: see AC CHARACTERISTICS for value.

R_T = Termination should be equal to Z_{OUT} of pulse generators.

SET-UP, HOLD, AND RELEASE TIMES



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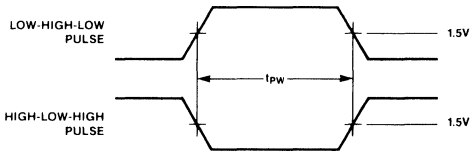
PULSE WIDTH



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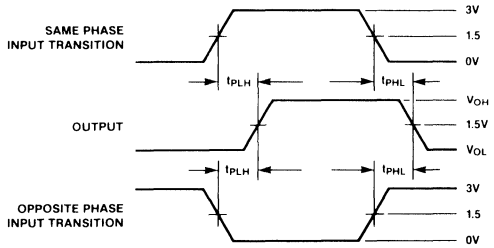
PROPAGATION DELAY



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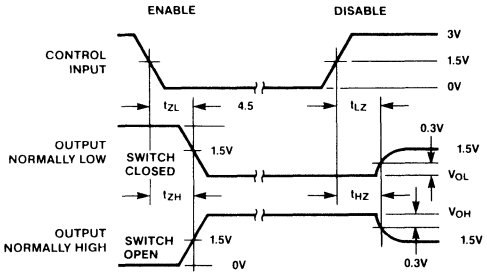
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. Pulse Generator for ALl Pulses: $t_f \leq 2.5$ns; $t_r \leq 2.5$ns.

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ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT39C821P	12.0	P24-2	Com'l.
IDT39C821J		J28	
IDT39C821D		D24-2	
IDT39C821L		L28-1	
IDT39C821DB		D24-2	Mil.
IDT39C821LB		L28-1	
IDT39C822P	12.0	P24-2	Com'l.
IDT39C822J		J28	
IDT39C822D		D24-2	
IDT39C822L		L28-1	
IDT39C822DB		D24-2	Mil.
IDT39C822LB		L28-1	
IDT39C823P	12.0	P24-2	Com'l.
IDT39C823J		J28	
IDT39C823D		D24-2	
IDT39C823L		L28-1	
IDT39C823DB		D24-2	Mil.
IDT39C823LB		L28-1	
IDT39C824P	12.0	P24-2	Com'l.
IDT39C824J		J28	
IDT39C824D		D24-2	
IDT39C824L		L28-1	
IDT39C824DB		D24-2	Mil.
IDT39C824LB		L28-1	
IDT39C825P	12.0	P24-2	Com'l.
IDT39C825J		J28	
IDT39C825D		D24-2	
IDT39C825L		L28-1	
IDT39C825DB		D24-2	Mil.
IDT39C825LB		L28-1	
IDT39C826P	12.0	P24-2	Com'l.
IDT39C826J		J28	
IDT39C826D		D24-2	
IDT39C826L		L28-1	
IDT39C826DB		D24-2	Mil.
IDT39C826LB		L28-1	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT39C841P	9.5	P24-2	Com'l.
IDT39C841J		J28	
IDT39C841D		D24-2	
IDT39C841L		L28-1	
IDT39C841DB	11.0	D24-2	Mil.
IDT39C841LB		L28-1	
IDT39C842P	9.5	P24-2	Com'l.
IDT39C842J		J28	
IDT39C842D		D24-2	
IDT39C842L		L28-1	
IDT39C842DB	11.0	D24-2	Mil.
IDT39C842LB		L28-1	
IDT39C843P	9.5	P24-2	Com'l.
IDT39C843J		J28	
IDT39C843D		D24-2	
IDT39C843L		L28-1	
IDT39C843DB	11.0	D24-2	Mil.
IDT39C843LB		L28-1	
IDT39C844P	9.5	P24-2	Com'l.
IDT39C844J		J28	
IDT39C844D		D24-2	
IDT39C844L		L28-1	
IDT39C844DB	11.0	D24-2	Mil.
IDT39C844LB		L28-1	
IDT39C845P	9.5	P24-2	Com'l.
IDT39C845J		J28	
IDT39C845D		D24-2	
IDT39C845L		L28-1	
IDT39C845DB	11.0	D24-2	Mil.
IDT39C845LB		L28-1	
IDT39C846P	9.5	P24-2	Com'l.
IDT39C846J		J28	
IDT39C846D		D24-2	
IDT39C846L		L28-1	
IDT39C846DB	11.0	D24-2	Mil.
IDT39C846LB		L28-1	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT39C861P	8.0	P24-2	Com'l.
IDT39C861J		J28	
IDT39C861D		D24-2	
IDT39C861L		L28-1	
IDT39C861DB	10.0	D24-2	Mil.
IDT39C861LB		L28-1	
IDT39C862P	8.0	P24-2	Com'l.
IDT39C862J		J28	
IDT39C862D		D24-2	
IDT39C862L		L28-1	
IDT39C862DB	10.0	D24-2	Mil.
IDT39C862LB		L28-1	
IDT39C863P	8.0	P24-2	Com'l.
IDT39C863J		J28	
IDT39C863D		D24-2	
IDT39C863L		L28-1	
IDT39C863DB	10.0	D24-2	Mil.
IDT39C863LB		L28-1	
IDT39C864P	8.0	P24-2	Com'l.
IDT39C864J		J28	
IDT39C864D		D24-2	
IDT39C864L		L28-1	
IDT39C864DB	10.0	D24-2	Mil.
IDT39C864LB		L28-1	
IDT49C818	Consult Factory		
IDT54AHCT138DB	27.0	D16	Mil.
IDT54AHCT138LB		L20-2	
IDT54AHCT138EB		E20	
IDT54AHCT139DB	25.0	D16	Mil.
IDT54AHCT139LB		L20-2	
IDT54AHCT139EB		E20	
IDT54AHCT161DB	20.0	D16	Mil.
IDT54AHCT161LB		L20-2	
IDT54AHCT161EB		E20	
IDT54AHCT163DB	20.0	D16	Mil.
IDT54AHCT163LB		L20-2	
IDT54AHCT163EB		E20	
IDT54AHCT182DB	15.0	D20	Mil.
IDT54AHCT182LB		L20-2	
IDT54AHCT182EB		E20	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT54AHCT191DB	22.0	D16	Mil.
IDT54AHCT191LB		L20-2	
IDT54AHCT191EB		E20	
IDT54AHCT193DB	19.0	D16	Mil.
IDT54AHCT193LB		L20-2	
IDT54AHCT193EB		E20	
IDT54AHCT240DB	12.0	D20	Mil.
IDT54AHCT240LB		L20-2	
IDT54AHCT240EB		E20	
IDT54AHCT244DB	13.0	D20	Mil.
IDT54AHCT244LB		L20-2	
IDT54AHCT244EB		E20	
IDT54AHCT245DB	15.0	D20	Mil.
IDT54AHCT245LB		L20-2	
IDT54AHCT245EB		E20	
IDT54AHCT273DB	17.0	D20	Mil.
IDT54AHCT273LB		L20-2	
IDT54AHCT273EB		E20	
IDT54AHCT299DB	20.0	D20	Mil.
IDT54AHCT299LB		L20-2	
IDT54AHCT299EB		E20	
IDT54AHCT373DB	19.0	D20	Mil.
IDT54AHCT373LB		L20-2	
IDT54AHCT373EB		E20	
IDT54AHCT374DB	18.0	D20	Mil.
IDT54AHCT374LB		L20-2	
IDT54AHCT374EB		E20	
IDT54AHCT377DB	18.0	D20	Mil.
IDT54AHCT377LB		L20-2	
IDT54AHCT377EB		E20	
IDT54AHCT521DB	18.0	D20	Mil.
IDT54AHCT521LB		L20-2	
IDT54AHCT521EB		E20	
IDT54AHCT533DB	24.0	D20	Mil.
IDT54AHCT533LB		L20-2	
IDT54AHCT533EB		E20	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT54AHCT534DB	18.0	D20	Mil.
IDT54AHCT534LB		L20-2	
IDT54AHCT534EB		E20	
IDT54AHCT573DB	15.0	D20	Mil.
IDT54AHCT573LB		L20-2	
IDT54AHCT573EB		E20	
IDT54AHCT574DB	15.0	D20	Mil.
IDT54AHCT574LB		L20-2	
IDT54AHCT574EB		E20	
IDT54AHCT640DB	14.0	D20	Mil.
IDT54AHCT640LB		L20-2	
IDT54AHCT640EB		E20	
IDT54AHCT645DB	15.0	D20	Mil.
IDT54AHCT645LB		L20-2	
IDT54AHCT645EB		E20	
IDT54FCT138ADB	7.8	D16	Mil.
IDT54FCT138ALB		L20-2	
IDT54FCT138AEB		E20	
IDT54FCT138DB	12.0	D16	
IDT54FCT138LB		L20-2	
IDT54FCT138EB		E20	
IDT54FCT139ADB	7.8	D16	Mil.
IDT54FCT139ALB		L20-2	
IDT54FCT139AEB		E20	
IDT54FCT139DB	12.0	D16	
IDT54FCT139LB		L20-2	
IDT54FCT139EB		E20	
IDT54FCT161ADB	7.5	D16	Mil.
IDT54FCT161ALB		L20-2	
IDT54FCT161AEB		E20	
IDT54FCT161DB	11.5	D16	
IDT54FCT161LB		L20-2	
IDT54FCT161EB		E20	
IDT54FCT163ADB	7.5	D16	Mil.
IDT54FCT163ALB		L20-2	
IDT54FCT163AEB		E20	
IDT54FCT163DB	11.5	D16	
IDT54FCT163LB		L20-2	
IDT54FCT163EB		E20	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT54FCT182ADB	—	D20	Mil.
IDT54FCT182ALB		L20-2	
IDT54FCT182AEB		E20	
IDT54FCT182DB	11.5	D20	
IDT54FCT182LB		L20-2	
IDT54FCT182EB		E20	
IDT54FCT191ADB	10.5	D16	Mil.
IDT54FCT191ALB		L20-2	
IDT54FCT191AEB		E20	
IDT54FCT191DB	16.0	D16	
IDT54FCT191LB		L20-2	
IDT54FCT191EB		E20	
IDT54FCT193ADB	6.9	D16	Mil.
IDT54FCT193ALB		L20-2	
IDT54FCT193AEB		E20	
IDT54FCT193DB	10.5	D16	
IDT54FCT193LB		L20-2	
IDT54FCT193EB		E20	
IDT54FCT240ADB	5.1	D20	Mil.
IDT54FCT240ALB		L20-2	
IDT54FCT240AEB		E20	
IDT54FCT240DB	9.0	D20	
IDT54FCT240LB		L20-2	
IDT54FCT240EB		E20	
IDT54FCT244ADB	4.6	D20	Mil.
IDT54FCT244ALB		L20-2	
IDT54FCT244AEB		E20	
IDT54FCT244DB	7.0	D20	
IDT54FCT244LB		L20-2	
IDT54FCT244EB		E20	
IDT54FCT245ADB	4.9	D20	Mil.
IDT54FCT245ALB		L20-2	
IDT54FCT245AEB		E20	
IDT54FCT245DB	7.5	D20	
IDT54FCT245LB		L20-2	
IDT54FCT245EB		E20	
IDT54FCT273ADB	8.3	D20	Mil.
IDT54FCT273ALB		L20-2	
IDT54FCT273AEB		E20	
IDT54FCT273DB	15.0	D20	
IDT54FCT273LB		L20-2	
IDT54FCT273EB		E20	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT54FCT299ADB	9.5	D20	Mil.
IDT54FCT299ALB		L20-2	
IDT54FCT299AEB		E20	
IDT54FCT299DB	16.0	D20	
IDT54FCT299LB		L20-2	
IDT54FCT299EB		E20	
IDT54FCT373ADB	5.6	D20	Mil.
IDT54FCT373ALB		L20-2	
IDT54FCT373AEB		E20	
IDT54FCT373DB	8.5	D20	
IDT54FCT373LB		L20-2	
IDT54FCT373EB		E20	
IDT54FCT374ADB	7.2	D20	Mil.
IDT54FCT374ALB		L20-2	
IDT54FCT374AEB		E20	
IDT54FCT374DB	11.0	D20	
IDT54FCT374LB		L20-2	
IDT54FCT374EB		E20	
IDT54FCT377ADB	8.3	D20	Mil.
IDT54FCT377ALB		L20-2	
IDT54FCT377AEB		E20	
IDT54FCT377DB	15.0	D20	
IDT54FCT377LB		L20-2	
IDT54FCT377EB		E20	
IDT54FCT521ADB	9.5	D20	Mil.
IDT54FCT521ALB		L20-2	
IDT54FCT521AEB		E20	
IDT54FCT521DB	15.0	D20	
IDT54FCT521LB		L20-2	
IDT54FCT521EB		E20	
IDT54FCT533ADB	5.6	D20	Mil.
IDT54FCT533ALB		L20-2	
IDT54FCT533AEB		E20	
IDT54FCT533DB	12.0	D20	
IDT54FCT533LB		L20-2	
IDT54FCT533EB		E20	
IDT54FCT534ADB	7.2	D20	Mil.
IDT54FCT534ALB		L20-2	
IDT54FCT534AEB		E20	
IDT54FCT534DB	11.0	D20	
IDT54FCT534LB		L20-2	
IDT54FCT534EB		E20	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT54FCT573ADB	5.6	D20	Mil.
IDT54FCT573ALB		L20-2	
IDT54FCT573AEB		E20	
IDT54FCT573DB	8.5	D20	
IDT54FCT573LB		L20-2	
IDT54FCT573EB		E20	
IDT54FCT574ADB	7.2	D20	Mil.
IDT54FCT574ALB		L20-2	
IDT54FCT574AEB		E20	
IDT54FCT574DB	11.0	D20	
IDT54FCT574LB		L20-2	
IDT54FCT574EB		E20	
IDT54FCT640ADB	5.3	D20	Mil.
IDT54FCT640ALB		L20-2	
IDT54FCT640AEB		E20	
IDT54FCT640DB	8.0	D20	
IDT54FCT640LB		L20-2	
IDT54FCT640EB		E20	
IDT54FCT645ADB	4.9	D20	Mil.
IDT54FCT645ALB		L20-2	
IDT54FCT645AEB		E20	
IDT54FCT645DB	11.0	D20	
IDT54FCT645LB		L20-2	
IDT54FCT645EB		E20	
IDT54FCT821BDB	8.5	D24-2	Mil.
IDT54FCT821BLB		L28-1	
IDT54FCT822BDB	8.5	D24-2	Mil.
IDT54FCT822BLB		L28-1	
IDT54FCT823BDB	8.5	D24-2	Mil.
IDT54FCT823BLB		L28-1	
IDT54FCT824BDB	8.5	D24-2	Mil.
IDT54FCT824BLB		L28-1	
IDT54FCT825BDB	8.5	D24-2	Mil.
IDT54FCT825BLB		L28-1	
IDT54FCT826BDB	8.5	D24-2	Mil.
IDT54FCT826BLB		L28-1	
IDT54FCT841BDB	7.5	D24-2	Mil.
IDT54FCT841BLB		L28-1	

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ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT54FCT842BDB	7.5	D24-2	Mil.
IDT54FCT842BLB		L28-1	
IDT54FCT843BDB	7.5	D24-2	Mil.
IDT54FCT843BLB		L28-1	
IDT54FCT844BDB	7.5	D24-2	Mil.
IDT54FCT844BLB		L28-1	
IDT54FCT845BDB	7.5	D24-2	Mil.
IDT54FCT845BLB		L28-1	
IDT54FCT846BDB	7.5	D24-2	Mil.
IDT54FCT846BLB		L28-1	
IDT54FCT861BDB	6.5	D24-2	Mil.
IDT54FCT861BLB		L28-1	
IDT54FCT862BDB	6.5	D24-2	Mil.
IDT54FCT862BLB		L28-1	
IDT54FCT863BDB	6.5	D24-2	Mil.
IDT54FCT863BLB		L28-1	
IDT54FCT864BDB	6.5	D24-2	Mil.
IDT54FCT864BLB		L28-1	
IDT74AHCT138P	22.0	Consult Factory	Com'l.
IDT74AHCT138SO		Consult Factory	
IDT74AHCT138D		D16	
IDT74AHCT138L		L20-2	
IDT74AHCT139P	20.0	Consult Factory	Com'l.
IDT74AHCT139SO		Consult Factory	
IDT74AHCT139D		D16	
IDT74AHCT139L		L20-2	
IDT74AHCT161P	17.0	Consult Factory	Com'l.
IDT74AHCT161SO		Consult Factory	
IDT74AHCT161D		D16	
IDT74AHCT161L		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74AHCT163P	17.0	Consult Factory	Com'l.
IDT74AHCT163SO		Consult Factory	
IDT74AHCT163D		D16	
IDT74AHCT163L		L20-2	
IDT74AHCT182P	12.0	P20	Com'l.
IDT74AHCT182J		J20	
IDT74AHCT182SO		S20	
IDT74AHCT182D		D20	
IDT74AHCT182L		L20-2	
IDT74AHCT191P	18.0	Consult Factory	Com'l.
IDT74AHCT191SO		Consult Factory	
IDT74AHCT191D		D16	
IDT74AHCT191L		L20-2	
IDT74AHCT193P	16.0	Consult Factory	Com'l.
IDT74AHCT193SO		Consult Factory	
IDT74AHCT193D		D16	
IDT74AHCT193L		L20-2	
IDT74AHCT240P	9.0	P20	Com'l.
IDT74AHCT240J		J20	
IDT74AHCT240SO		S20	
IDT74AHCT240D		D20	
IDT74AHCT240L		L20-2	
IDT74AHCT244P	10.0	P20	Com'l.
IDT74AHCT244J		J20	
IDT74AHCT244SO		S20	
IDT74AHCT244D		D20	
IDT74AHCT244L		L20-2	
IDT74AHCT245P	10.0	P20	Com'l.
IDT74AHCT245J		J20	
IDT74AHCT245SO		S20	
IDT74AHCT245D		D20	
IDT74AHCT245L		L20-2	
IDT74AHCT273P	15.0	P20	Com'l.
IDT74AHCT273J		J20	
IDT74AHCT273SO		S20	
IDT74AHCT273D		D20	
IDT74AHCT273L		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74AHCT299P	14.0	P20	Com'l.
IDT74AHCT299J		J20	
IDT74AHCT299SO		S20	
IDT74AHCT299D		D20	
IDT74AHCT299L		L20-2	
IDT74AHCT373P	16.0	P20	Com'l.
IDT74AHCT373J		J20	
IDT74AHCT373SO		S20	
IDT74AHCT373D		D20	
IDT74AHCT373L		L20-2	
IDT74AHCT374P	16.0	P20	Com'l.
IDT74AHCT374J		J20	
IDT74AHCT374SO		S20	
IDT74AHCT374D		D20	
IDT74AHCT374L		L20-2	
IDT74AHCT521P	16.0	P20	Com'l.
IDT74AHCT521J		J20	
IDT74AHCT521SO		S20	
IDT74AHCT521D		D20	
IDT74AHCT521L		L20-2	
IDT74AHCT533P	14.0	P20	Com'l.
IDT74AHCT533J		J20	
IDT74AHCT533SO		S20	
IDT74AHCT533D		D20	
IDT74AHCT533L		L20-2	
IDT74AHCT534P	19.0	P20	Com'l.
IDT74AHCT534J		J20	
IDT74AHCT534SO		S20	
IDT74AHCT534D		D20	
IDT74AHCT534L		L20-2	
IDT74AHCT573P	14.0	P20	Com'l.
IDT74AHCT573J		J20	
IDT74AHCT573SO		S20	
IDT74AHCT573D		D20	
IDT74AHCT573L		L20-2	
IDT74AHCT574P	14.0	P20	Com'l.
IDT74AHCT574J		J20	
IDT74AHCT574SO		S20	
IDT74AHCT574D		D20	
IDT74AHCT574L		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74AHCT640P	11.0	P20	Com'l.
IDT74AHCT640J		J20	
IDT74AHCT640SO		S20	
IDT74AHCT640D		D20	
IDT74AHCT640L		L20-2	
IDT74AHCT645P	10.0	P20	Com'l.
IDT74AHCT645J		J20	
IDT74AHCT645SO		S20	
IDT74AHCT645D		D20	
IDT74AHCT645L		L20-2	
IDT74FCT138AP	5.8	Consult Factory	Com'l.
IDT74FCT138ASO		Consult Factory	
IDT74FCT138AD		D16	
IDT74FCT138AL		L20-2	
IDT74FCT138P	9.0	Consult Factory	
IDT74FCT138SO		Consult Factory	
IDT74FCT138D		D16	
IDT74FCT138L		L20-2	
IDT74FCT139AP	5.9	Consult Factory	Com'l.
IDT74FCT139ASO		Consult Factory	
IDT74FCT139AD		D16	
IDT74FCT139AL		L20-2	
IDT74FCT139P	9.0	Consult Factory	
IDT74FCT139SO		Consult Factory	
IDT74FCT139D		D16	
IDT74FCT139L		L20-2	
IDT74FCT161AP	7.2	Consult Factory	Com'l.
IDT74FCT161ASO		Consult Factory	
IDT74FCT161AD		D16	
IDT74FCT161AL		L20-2	
IDT74FCT161P	11.0	Consult Factory	
IDT74FCT161SO		Consult Factory	
IDT74FCT161D		D16	
IDT74FCT161L		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT161P	11.0	Consult Factory	Com'l.
IDT74FCT161SO		Consult Factory	
IDT74FCT161D		D16	
IDT74FCT161L		L20-2	
IDT74FCT163AP	7.2	Consult Factory	Com'l.
IDT74FCT163ASO		Consult Factory	
IDT74FCT163AD		D16	
IDT74FCT163AL		L20-2	
IDT74FCT163P	11.0	Consult Factory	
IDT74FCT163SO		Consult Factory	
IDT74FCT163D		D16	
IDT74FCT163L		L20-2	
IDT74FCT182AP	—	P20	Com'l.
IDT74FCT182AJ		J20	
IDT74FCT182ASO		S20	
IDT74FCT182AD		D20	
IDT74FCT182AL		L20-2	
IDT74FCT182P	9.0	P20	
IDT74FCT182J		J20	
IDT74FCT182SO		S20	
IDT74FCT182D		D20	
IDT74FCT182L		L20-2	
IDT74FCT191AP	7.8	Consult Factory	Com'l.
IDT74FCT191ASO		Consult Factory	
IDT74FCT191AD		D16	
IDT74FCT191AL		L20-2	
IDT74FCT191P	12.0	Consult Factory	
IDT74FCT191SO		Consult Factory	
IDT74FCT191D		D16	
IDT74FCT191L		L20-2	
IDT74FCT193AP	6.5	Consult Factory	Com'l.
IDT74FCT193ASO		Consult Factory	
IDT74FCT193AD		D16	
IDT74FCT193AL		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT193P	10.0	Consult Factory	Com'l
IDT74FCT193SO		Consult Factory	
IDT74FCT193D		D16	
IDT74FCT193L		L20-2	
IDT74FCT240AP	4.8	P20	Com'l.
IDT74FCT240AJ		J20	
IDT74FCT240ASO		S20	
IDT74FCT240AD		D20	
IDT74FCT240AL		L20-2	
IDT74FCT240P	8.0	P20	
IDT74FCT240J		J20	
IDT74FCT240SO		S20	
IDT74FCT240D		D20	
IDT74FCT240L		L20-2	
IDT74FCT244AP	4.3	P20	Com'l.
IDT74FCT244AJ		J20	
IDT74FCT244ASO		S20	
IDT74FCT244AD		D20	
IDT74FCT244AL		L20-2	
IDT74FCT244P	6.5	P20	
IDT74FCT244J		J20	
IDT74FCT244SO		S20	
IDT74FCT244D		D20	
IDT74FCT244L		L20-2	
IDT74FCT245AP	4.6	P20	Com'l.
IDT74FCT245AJ		J20	
IDT74FCT245ASO		S20	
IDT74FCT245AD		D20	
IDT74FCT245AL		L20-2	
IDT74FCT245P	7.0	P20	
IDT74FCT245J		J20	
IDT74FCT245SO		S20	
IDT74FCT245D		D20	
IDT74FCT245L		L20-2	
IDT74FCT273AP	7.2	P20	Com'l.
IDT74FCT273AJ		J20	
IDT74FCT273ASO		S20	
IDT74FCT273AD		D20	
IDT74FCT273AL		L20-2	
IDT74FCT273P	13.0	P20	
IDT74FCT273J		J20	
IDT74FCT273SO		S20	
IDT74FCT273D		D20	
IDT74FCT273L		L20-2	

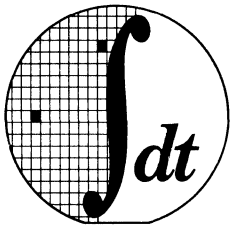
ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT299AP	7.2	P20	Com'l.
IDT74FCT299AJ		J20	
IDT74FCT299ASO		S20	
IDT74FCT299AD		D20	
IDT74FCT299AL		L20-2	
IDT74FCT299P	10.0	P20	
IDT74FCT299J		J20	
IDT74FCT299SO		S20	
IDT74FCT299D		D20	
IDT74FCT299L		L20-2	
IDT74FCT373AP	5.2	P20	Com'l.
IDT74FCT373AJ		J20	
IDT74FCT373ASO		S20	
IDT74FCT373AD		D20	
IDT74FCT373AL		L20-2	
IDT74FCT373P	8.0	P20	
IDT74FCT373J		J20	
IDT74FCT373SO		S20	
IDT74FCT373D		D20	
IDT74FCT373L		L20-2	
IDT74FCT374AP	6.5	P20	Com'l.
IDT74FCT374AJ		J20	
IDT74FCT374ASO		S20	
IDT74FCT374AD		D20	
IDT74FCT374AL		L20-2	
IDT74FCT374P	10.0	P20	
IDT74FCT374J		J20	
IDT74FCT374SO		S20	
IDT74FCT374D		D20	
IDT74FCT374L		L20-2	
IDT74FCT377AP	7.2	P20	Com'l.
IDT74FCT377AJ		J20	
IDT74FCT377ASO		S20	
IDT74FCT377AD		D20	
IDT74FCT377AL		L20-2	
IDT74FCT377P	13.0	P20	
IDT74FCT377J		J20	
IDT74FCT377SO		S20	
IDT74FCT377D		D20	
IDT74FCT377L		L20-2	
IDT74FCT521AP	7.2	P20	Com'l.
IDT74FCT521AJ		J20	
IDT74FCT521ASO		S20	
IDT74FCT521AD		D20	
IDT74FCT521AL		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT521P	11.0	P20	Com'l
IDT74FCT521J		J20	
IDT74FCT521SO		S20	
IDT74FCT521D		D20	
IDT74FCT521L		L20-2	
IDT74FCT533AP	5.2	P20	Com'l.
IDT74FCT533AJ		J20	
IDT74FCT533ASO		S20	
IDT74FCT533AD		D20	
IDT74FCT533AL		L20-2	
IDT74FCT533P	10.0	P20	
IDT74FCT533J		J20	
IDT74FCT533SO		S20	
IDT74FCT533D		D20	
IDT74FCT533L		L20-2	
IDT74FCT534AP	6.5	P20	Com'l.
IDT74FCT534AJ		J20	
IDT74FCT534ASO		S20	
IDT74FCT534AD		D20	
IDT74FCT534AL		L20-2	
IDT74FCT534P	10.0	P20	
IDT74FCT534J		J20	
IDT74FCT534SO		S20	
IDT74FCT534D		D20	
IDT74FCT534L		L20-2	
IDT74FCT573AP	5.2	P20	Com'l.
IDT74FCT573AJ		J20	
IDT74FCT573ASO		S20	
IDT74FCT573AD		D20	
IDT74FCT573AL		L20-2	
IDT74FCT573P	8.0	P20	
IDT74FCT573J		J20	
IDT74FCT573SO		S20	
IDT74FCT573D		D20	
IDT74FCT573L		L20-2	
IDT74FCT574AP	6.5	P20	Com'l.
IDT74FCT574AJ		J20	
IDT74FCT574ASO		S20	
IDT74FCT574AD		D20	
IDT74FCT574AL		L20-2	
IDT74FCT574P	10.0	P20	
IDT74FCT574J		J20	
IDT74FCT574SO		S20	
IDT74FCT574D		D20	
IDT74FCT574L		L20-2	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT640AP	5.0	P20	Com'l.
IDT74FCT640AJ		J20	
IDT74FCT640ASO		S20	
IDT74FCT640AD		D20	
IDT74FCT640AL		L20-2	
IDT74FCT640P	7.0	P20	
IDT74FCT640J		J20	
IDT74FCT640SO		S20	
IDT74FCT640D		D20	
IDT74FCT640L		L20-2	
IDT74FCT645AP	4.6	P20	Com'l.
IDT74FCT645AJ		J20	
IDT74FCT645ASO		S20	
IDT74FCT645AD		D20	
IDT74FCT645AL		L20-2	
IDT74FCT645P	9.5	P20	
IDT74FCT645J		J20	
IDT74FCT645SO		S20	
IDT74FCT645D		D20	
IDT74FCT645L		L20-2	
IDT74FCT821BP	7.5	P24-2	Com'l.
IDT74FCT821BJ		J28	
IDT74FCT821BD		D24-2	
IDT74FCT821BL		L28-1	
IDT74FCT822BP	7.5	P24-2	Com'l.
IDT74FCT822BJ		J28	
IDT74FCT822BD		D24-2	
IDT74FCT822BL		L28-1	
IDT74FCT823BP	7.5	P24-2	Com'l.
IDT74FCT823BJ		J28	
IDT74FCT823BD		D24-2	
IDT74FCT823BL		L28-1	
IDT74FCT824BP	7.5	P24-2	Com'l.
IDT74FCT824BJ		J28	
IDT74FCT824BD		D24-2	
IDT74FCT824BL		L28-1	
IDT74FCT825BP	7.5	P24-2	Com'l.
IDT74FCT825BJ		J28	
IDT74FCT825BD		D24-2	
IDT74FCT825BL		L28-1	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT826BP	7.5	P24-2	Com'l.
IDT74FCT826BJ		J28	
IDT74FCT826BD		D24-2	
IDT74FCT826BL		L28-1	
IDT74FCT841BP	6.5	P24-2	Com'l.
IDT74FCT841BJ		J28	
IDT74FCT841BD		D24-2	
IDT74FCT841BL		L28-1	
IDT74FCT842BP	6.5	P24-2	Com'l.
IDT74FCT842BJ		J28	
IDT74FCT842BD		D24-2	
IDT74FCT842BL		L28-1	
IDT74FCT843BP	6.5	P24-2	Com'l.
IDT74FCT843BJ		J28	
IDT74FCT843BD		D24-2	
IDT74FCT843BL		L28-1	
IDT74FCT844BP	6.5	P24-2	Com'l.
IDT74FCT844BJ		J28	
IDT74FCT844BD		D24-2	
IDT74FCT844BL		L28-1	
IDT74FCT845BP	6.5	P24-2	Com'l.
IDT74FCT845BJ		J28	
IDT74FCT845BD		D24-2	
IDT74FCT845BL		L28-1	
IDT74FCT846BP	6.5	P24-2	Com'l.
IDT74FCT846BJ		J28	
IDT74FCT846BD		D24-2	
IDT74FCT846BL		L28-1	
IDT74FCT861BP	5.0	P24-2	Com'l.
IDT74FCT861BJ		J28	
IDT74FCT861BD		D24-2	
IDT74FCT861BL		L28-1	
IDT74FCT862BP	5.0	P24-2	Com'l.
IDT74FCT862BJ		J28	
IDT74FCT862BD		D24-2	
IDT74FCT862BL		L28-1	
IDT74FCT863BP	5.0	P24-2	Com'l.
IDT74FCT863BJ		J28	
IDT74FCT863BD		D24-2	
IDT74FCT863BL		L28-1	

ORDER PART NUMBER	SPEED (ns)	PACKAGE TYPE	OPER. TEMP.
IDT74FCT864BP	5.0	P24-2	Com'l.
IDT74FCT864BJ		J28	
IDT74FCT864BD		D24-2	
IDT74FCT864BL		L28-1	



Integrated
Device
Technology

Technology/Capabilities

Static RAM

MICROSLICE™

Digital Signal Processing (DSP)

Logic

Data Conversion

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Subsystems Modules

General Product Information

DATA CONVERSION PRODUCT
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Integrated Device Technology, Inc.

8-BIT CMOS 125MHz VIDEO DAC

ADVANCE INFORMATION IDT75C18/28

FEATURES:

- Graphics-ready
- Pin-compatible with TRW TDC1018
- 8 bits, 1/2 LSB linearity
- 70, 100, 125MHz models available
- ECL-compatible inputs — IDT75C18
- TTL-compatible inputs — IDT75C28
- Ultra-low power dissipation < 400mW
- Power supply noise rejection > 50dB
- Registered data and video controls
- Differential current outputs
- Flexible video controls
- Inherently low glitch energy
- Multiplying mode capability
- Single 5V power supply
- Available in 24-pin hermetic DIP, 24-pin plastic DIP and 28-pin LCC
- Military product is 100% screened to MIL-STD-883, Class B

DESCRIPTION

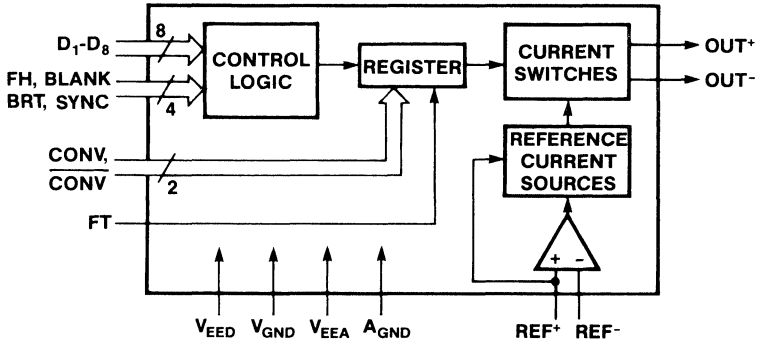
The IDT75C18/28 are 70/100/125 MegaSample per Second (MSPS), 8-bit Digital to Analog Converters, capable of directly driving a 75Ω load to standard video levels. Most applications require no extra registering, buffering or deglitching. Four special level controls simplify the interface for video applications. The IDT75C18 has ECL-compatible inputs while the IDT75C28 is TTL-compatible.

The IDT75C18/28 are built using IDT's high-performance CEMOS™ process. On chip data registers and precise matching of propagation delays, as well as an improved segmenting/decoding architecture, significantly reduce glitch energy. The IDT75C18/28 offer high-performance and ultra-low-power in a 24-pin hermetic DIP, 24-pin plastic DIP or 28-pin LCC.

The IDT75C18 is pin and functionally compatible with the TRW TDC1018, with the advantage of low power due to CMOS processing. Besides providing higher reliability by running cooler, power supply requirements are reduced. Another advantage of the lower power dissipation is that this part may be packaged in a space-saving, cost-effective, 0.3 inch plastic package.

The IDT75C18/28 Military DACs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

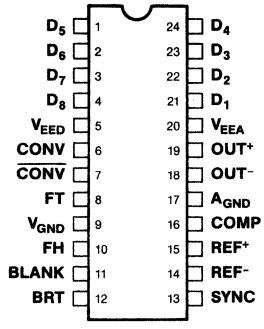


SSD75C18-001

6

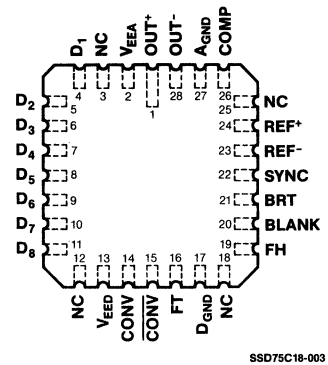
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SSD75C18-002

DIP
TOP VIEW



SSD75C18-003

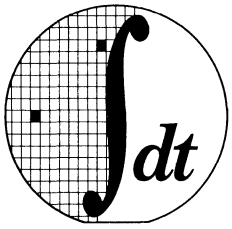
LCC
TOP VIEW

Integrated Device Technology, Inc.

Data Conversion Ordering Information

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT75C18	Consult Factory			
IDT75C28	Consult Factory			

6



Integrated
Device
Technology

Subsystems Modules

7

SUBSYSTEMS MODULES
TABLE OF CONTENTS

Integrated Device Technology, Inc

1 MEGABIT CMOS STATIC RAM PLASTIC MODULE

ADVANCE INFORMATION IDT7MP624S

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  —30ns (max.) over commercial temperature range
- Low-power consumption
  —Active: 4.8W (typ. in 64K x 16 organization)
  —Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in 40-pin, 900 mil center plastic DIP, achieving very high memory density
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate

DESCRIPTION:

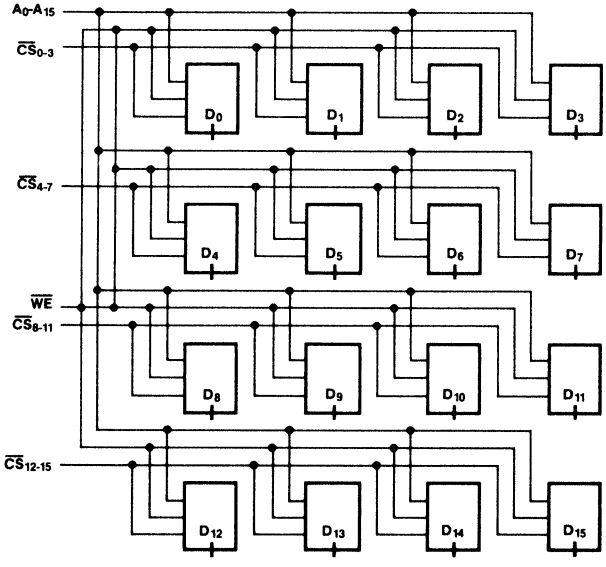
The IDT7MP624 is a 1024K-bit high-speed CMOS static RAM constructed on an epoxy laminate substrate using 16 IDT7187 (64K x 1) static RAMs in plastic surface mount packages. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7MP624 is available with access times as fast as 30ns commercial temperature range, with maximum operating power consumption of only 10.5W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.4W (max.) and a full standby mode of 1.7W (max.).

The IDT7MP624 is offered in a high-density 40-pin, 900 mil center plastic DIP to take full advantage of the compact IDT7187s in plastic surface mount packages.

All inputs and outputs of the IDT7MP624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



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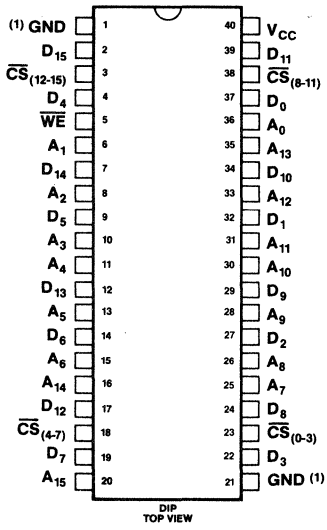
PIN CONFIGURATION



DIP
TOP VIEW

PIN NAMES

A_0 - A_{15}	ADDRESSES
D_0 - D_{15}	DATA INPUT/OUTPUT
$\overline{CS}_{XX}$	CHIP SELECTS
$\overline{WE}$	WRITE ENABLE
V_{CC}	POWER
GND	GROUND

NOTE:
1. Both GND pins need to be grounded for proper operation.

Integrated Device Technology, Inc.

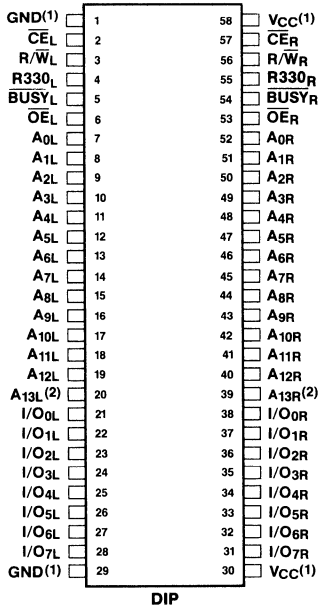
CMOS DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

PRELIMINARY
IDT7M134S
IDT7M135S

FEATURES:

- High-density 64K/128K-bit CMOS dual-port RAM module
- 16K x 8 organization (IDT7M135) with 8K x 8 option (IDT7M134)
- Low-power consumption
- CEMOS™ process virtually eliminates alpha particle soft errors rates (with no organic die coating)
- On-chip port arbitration logic
- $\overline{BUSY}$ flags
- Fully asynchronous operation from either port
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{BUSY}$ flag option
- Inputs and output directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirement

PIN CONFIGURATION



DIP
TOP VIEW

NOTES

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On 8Kx8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.

CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION:

The IDT7M134/135 are 64K/128K-bit high-speed CMOS dual-port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port RAMs (IDT7M134) or eight IDT7132 dual-port RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M134 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.) Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{BUSY}$ flag of the delayed port. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive).

The IDT7M134/135 are available with access times as fast as 70ns commercial and 90ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{BUSY}$ FLAG (OPEN DRAIN)
$R330_L$	$R330_R$	PULL-UP RESISTORS for Open-drain $\overline{BUSY}$ FLAG option
A_{0L}-A_{13L}	A_{0R}-A_{13R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

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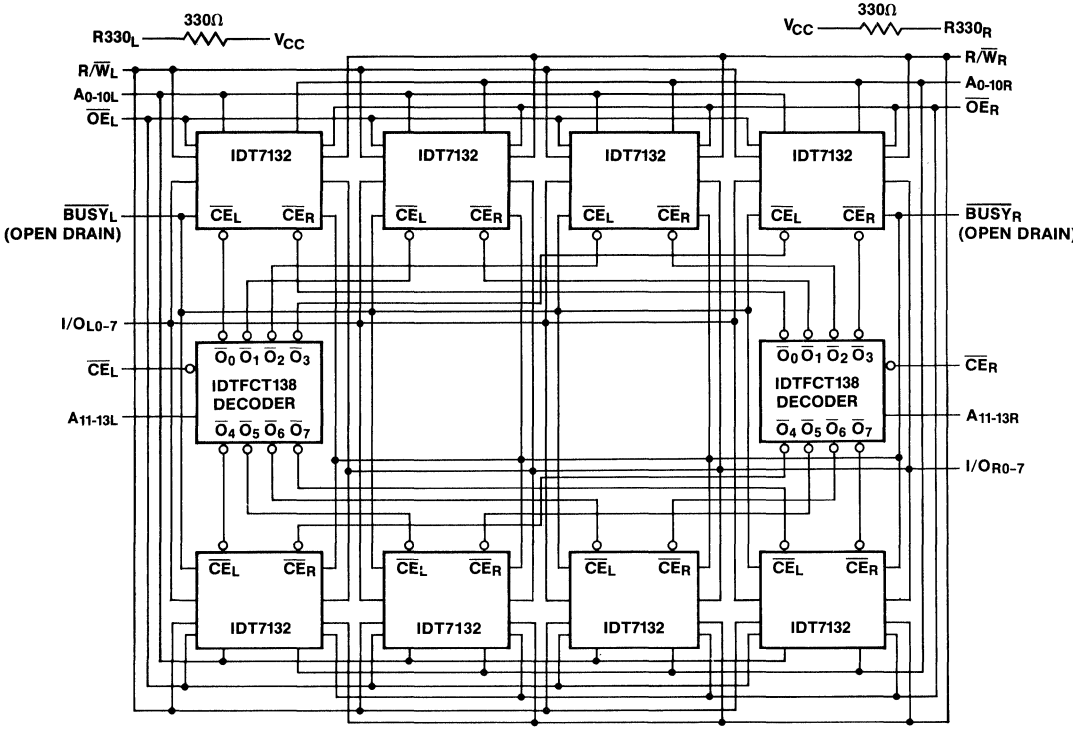
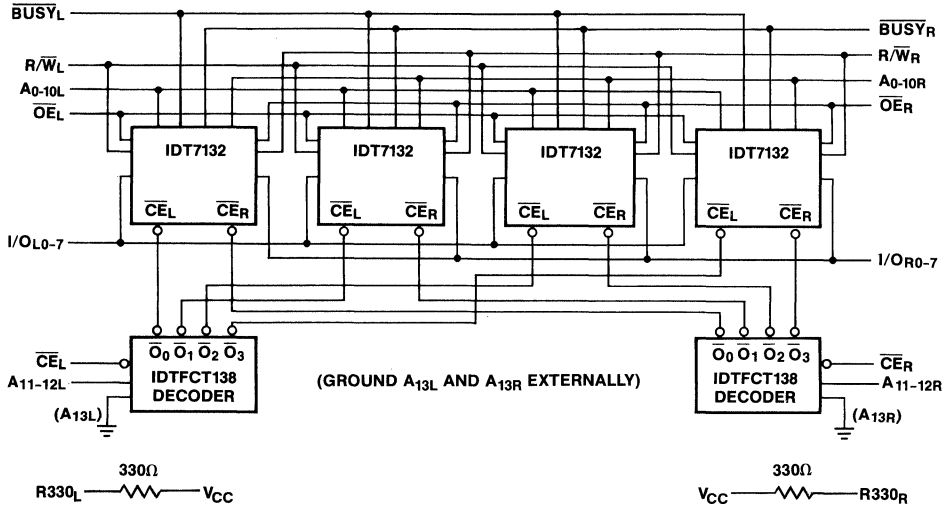
Printed in U.S.A.

FUNCTIONAL BLOCK DIAGRAMS

(A) IDT7M135 (16K x 8-BIT)



(B) IDT7M134 (8K x 8-BIT)



ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	8.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} = -3.5V for pulse width less than 30ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M134S MIN.	IDT7M134S TYP.(1)	IDT7M134S MAX.	IDT7M135S MIN.	IDT7M135S TYP.(1)	IDT7M135S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	—	—	20	µA
V_{IH}	Input High Voltage		2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage		-1.0(2)	—	0.8	-1.0(2)	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	—	190	380	—	320	640	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	—	130	260	—	260	520	mA
I_{SB_1}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	—	160	320	—	290	580	mA
I_{SB_2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	—	4	120(3)	—	10	240(3)	mA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 3.5mA, V_{CC} = 4.5V	—	—	0.4	—	—	0.4	V
		I_{OL} = 8mA, V_{CC} = 4.5V	—	—	0.5	—	—	0.5	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA, V_{CC} = 4.5V	—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = 4.5V	2.4	—	—	2.4	—	—	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C.
2. V_{IL} min. = -3.5V for pulse width less than 30ns.
3. I_{SB_2} max. of IDT7M134/IDT7M135 at commercial temperature = 80mA/150mA.

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AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M134S70 IDT7M135S70 COM'L. ONLY		IDT7M134S90 IDT7M135S90		IDT7M134S100 IDT7M135S100		IDT7M134S120 IDT7M135S120		IDT7M134S140 IDT7M135S140 MIL. ONLY		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	70	—	90	—	100	—	120	—	140	—	ns
t_{AA}	Address Access Time	—	70	—	90	—	100	—	120	—	140	ns
t_{ACE}	Chip Enable Access Time	—	70	—	90	—	100	—	120	—	140	ns
t_{AOE}	Output Enable Access Time	—	40	—	45	—	50	—	60	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	10	—	10	—	10	—	10	—	ns
t_{CLZ}	Chip Select to Output in Low Z	10	—	15	—	15	—	15	—	15	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	35	—	45	—	50	—	50	—	60	ns
t_{OHZ}	Output Enable to Output in High Z	—	30	—	40	—	40	—	40	—	50	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	70	—	90	—	100	—	120	—	140	—	ns
t_{CW}	Chip Selection to End of Write	60	—	80	—	95	—	110	—	120	—	ns
t_{AW}	Address Valid to End of Write	60	—	80	—	95	—	110	—	120	—	ns
t_{AS}	Address Setup Time	10	—	10	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	55	—	65	—	75	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{DW}	Data Valid to End of Write	30	—	40	—	40	—	40	—	50	—	ns
t_{DH}	Data Hold Time	10	—	10	—	10	—	10	—	10	—	ns
t_{OHZ}	Output Enable to Output in High Z	—	35	—	40	—	40	—	40	—	40	ns
t_{WZ}	Write Enabled to Output in High Z	—	35	—	40	—	40	—	50	—	60	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
BUSY TIMING												
t_{RC}	Read Cycle Time	70	—	90	—	100	—	120	—	140	—	
t_{WC}	Write Cycle Time	70	—	90	—	100	—	120	—	140	—	
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	50	—	60	—	70	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	45	—	45	—	50	—	60	—	70	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	40	—	40	—	50	—	60	—	70	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	—	35	—	35	—	50	—	60	—	70	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data	—	50	—	50	—	60	—	80	—	90	ns
t_{WDD}	Write Pulse to Data Delay	—	90	—	100	—	120	—	140	—	160	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	70	—	80	—	100	—	120	—	140	ns
t_{APS}	Arbitration Priority Set Up Time	10	—	10	—	10	—	10	—	10	—	ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1, 2, and 3

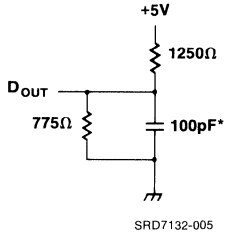


Figure 1.
Output Load

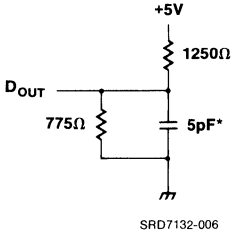


Figure 2.
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

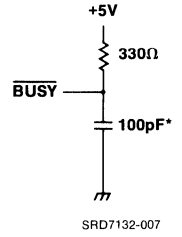


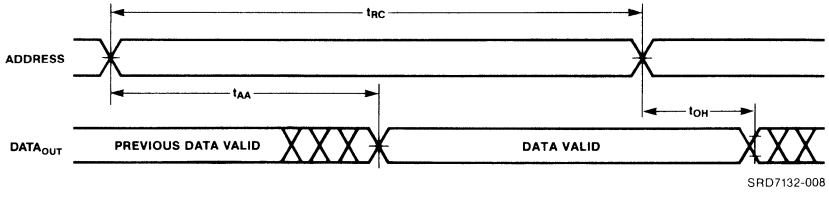
Figure 3.
$\overline{BUSY}$ Output Load

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	7M134S	7M135S	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	150	180	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	70	pF

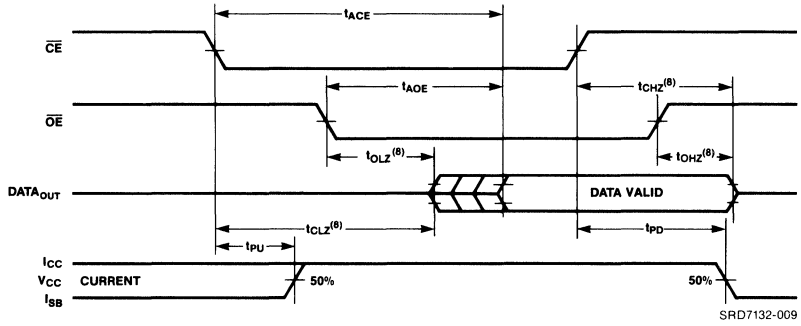
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE(1,2,6)

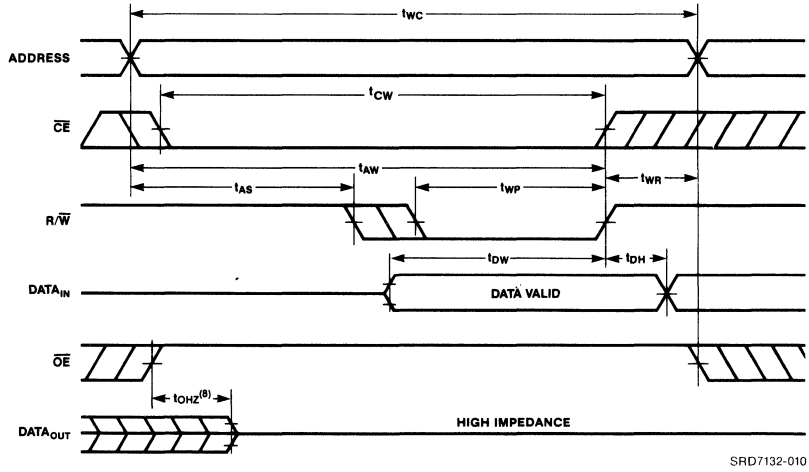


7

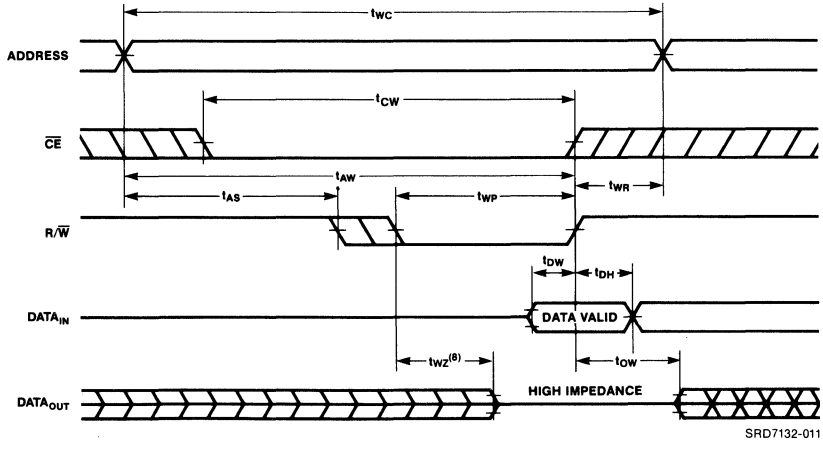
TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE[1,3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 EITHER SIDE[4,7]

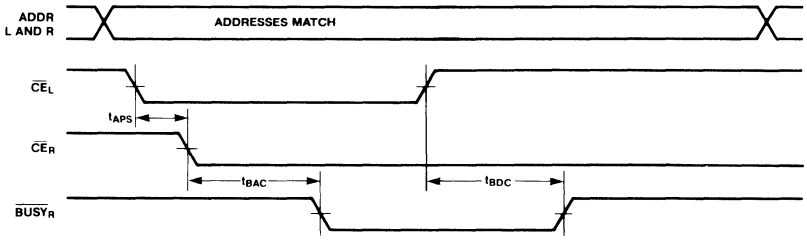


TIMING WAVEFORM OF WRITE CYCLE NO. 1 EITHER SIDE[4,7]



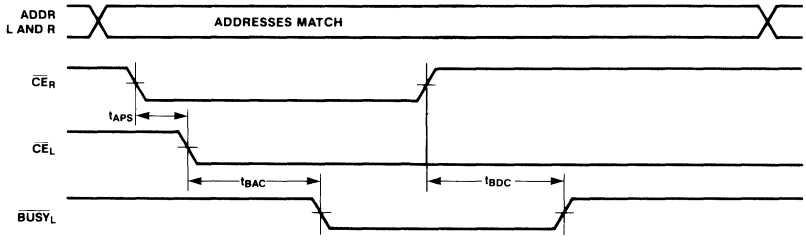
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



SRD7132-012

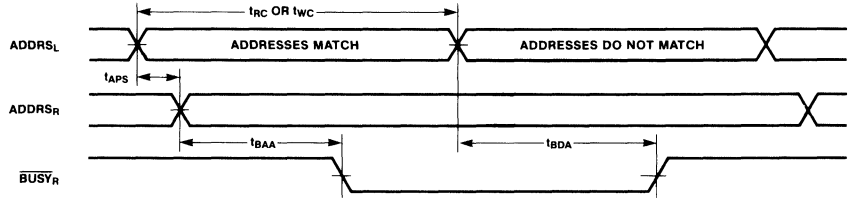
$\overline{CE}_R$ VALID FIRST:



SRD7132-013

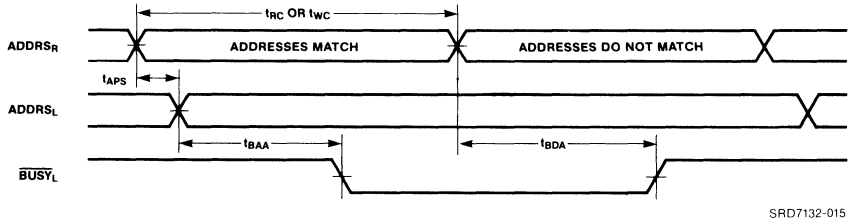
TIMING WAVEFORM OF CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST



SRD7132-014

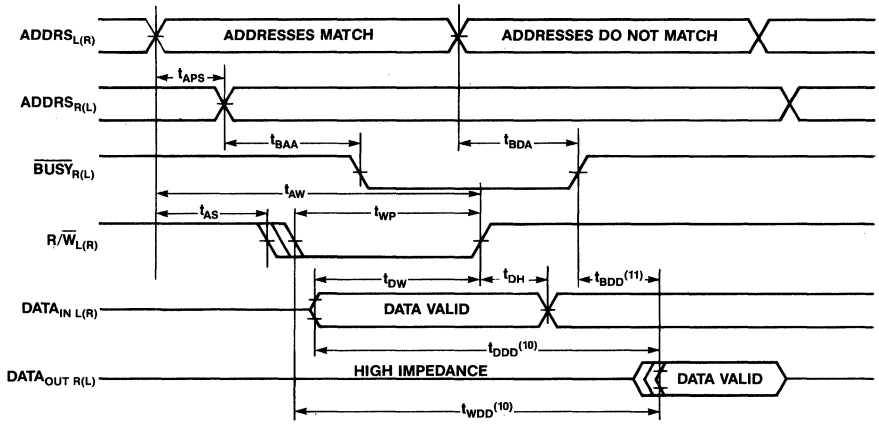
RIGHT ADDRESS VALID FIRST



SRD7132-015

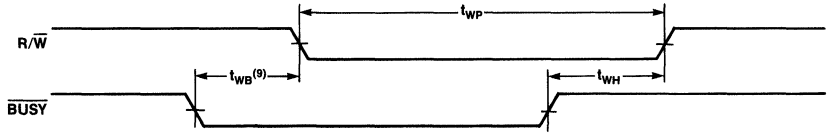
7

TIMING WAVEFORM OF READ WITH BUSY(5)



SRD7134-001

TIMING WAVEFORM OF WRITE WITH BUSY(5)



SRD7134-002

NOTES:

1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during address transition.
8. Transition is measured at ±500mV from low or high impedance voltage with load (Figures 1, 2 & 3). This parameter is guaranteed by design, but not tested.
9. For slave port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

FUNCTIONAL DESCRIPTION:

The IDT7M134/IDT7M135 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M134/IDT7M135 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 10ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and set the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) If the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its L $\overline{BUSY}$ while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL, LEFT OR RIGHT PORT[1]

$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	FUNCTION
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = H$, Power Down Mode, I_{SB} or I_{SB2}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES:

1. $A_{0L} - A_{13L} \neq A_{0R} - A_{13R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.

H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

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TABLE II — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS		FUNCTION
$\overline{CE}_L$	A_{0L}-A_{13L}	$\overline{CE}_R$	A_{0R}-A_{13R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{13R}	L	$\neq A_{0L}$-A_{13L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV10R	L	LV10R	H	L	Left-Port Wins
L	RV10L	L	LV10R	L	H	Right-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL10R	= A_{0R} - A_{13R}	LL10R	= A_{0L} - A_{13L}	H	L	Left-Port Wins
RL10L	= A_{0R} - A_{13R}	RL10R	= A_{0L} - A_{13L}	L	H	Right-Port Wins
LW10R	= A_{0R} - A_{13R}	LW10R	= A_{0L} - A_{13L}	H	L	Arbitration Resolved
LW10R	= A_{0R} - A_{13R}	LW10R	= A_{0L} - A_{13L}	L	H	Arbitration Resolved

NOTE:

X = DON'T CARE, L = LOW, H = HIGH, Same = Left and Right Addresses match within 10ns of each other.

LV10R = Left Address Valid ≥ 10ns before Right Address.

RV10L = Right Address Valid ≥ 10ns before Left Address.

LL10R = Left $\overline{CE}$ = LOW ≥ 10ns before Right $\overline{CE}$.

RL10L = Right $\overline{CE}$ = LOW ≥ 10ns before Left $\overline{CE}$.

LW10R = Left and Right $\overline{CE}$ = LOW within 10ns of each other.

Integrated Device Technology, Inc.

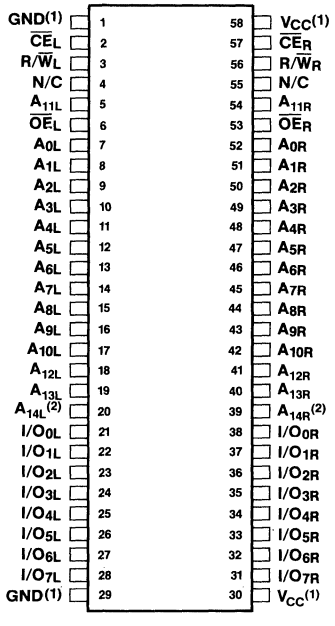
CMOS DUAL-PORT RAM MODULE 128K (16K x 8-BIT) & 256K (32K x 8-BIT)

ADVANCE INFORMATION
IDT7M136
IDT7M137

FEATURES:

- High-density 128K/256K-bit CMOS dual-port RAM module
- 32K x 8 organization (IDT7M137) or 16K x 8 option (IDT7M136)
- Low-power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Battery backup operation — 2V data retention
- Fully asynchronous operation from either port
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirement

PIN CONFIGURATION



DIP
TOP VIEW

DESCRIPTION

The IDT7M136/137 are 128K/256K-bit high-speed CMOS dual-port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7134 4K x 8 dual-port RAMs (IDT7M136) or eight IDT7134 dual-port RAMs (IDT7M137) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L12-14} and A_{R12-14} to select one of the eight 4K x 8 dual-port RAMs. (On the IDT7M136 16K x 8 option, the A_{L14} and A_{R14} need to be externally grounded and the selection becomes one of the four 4K x 8 dual-port RAMs.) Extremely high speeds are achieved in this fashion due to the use of the IDT7134 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M136/137s provides two ports with separate control, address and I/O pins that permit independent, asynchronous access for reads or writes to any location in the memory. The IDT7M136/137s are designed to be used in systems where on-chip hardware port arbitration is not needed. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M136/136s are available with access times as fast as 60ns commercial and 80ns military temperature ranges, with operating power consumption of only 2.1W/3.5W (max.). The modules also offer a standby power mode of 1.4W/2.8W (max.) and full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
A_{0L-14L}	A_{0R-14R}	ADDRESS
I/O_{0L-7L}	I/O_{0R-7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On 16K x 8 IDT7M136 option, A_{14L} and A_{14R} need to be externally connected to ground for proper operation.

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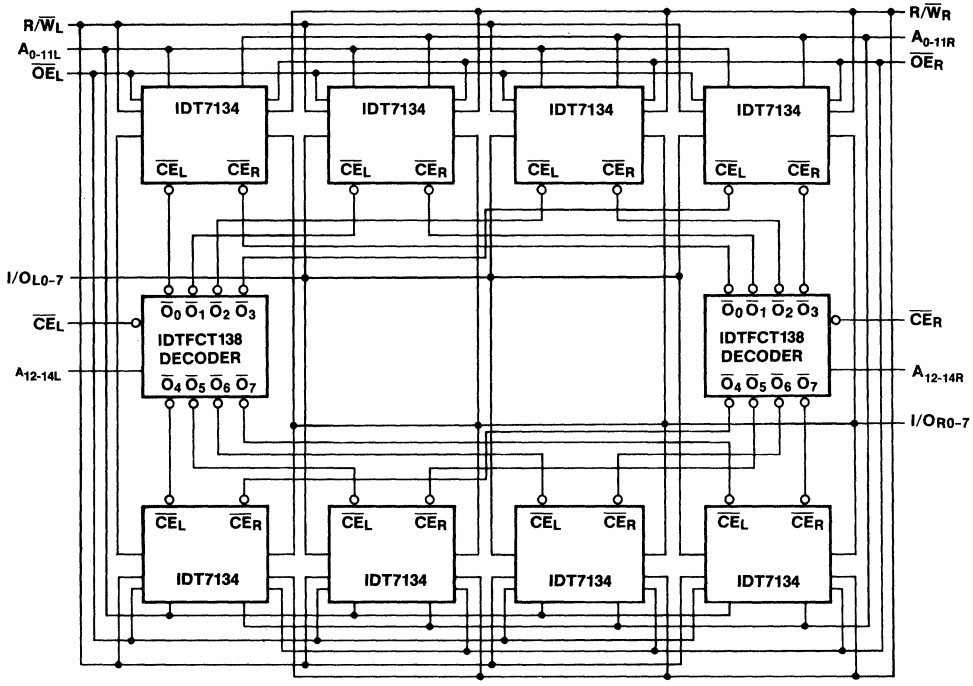
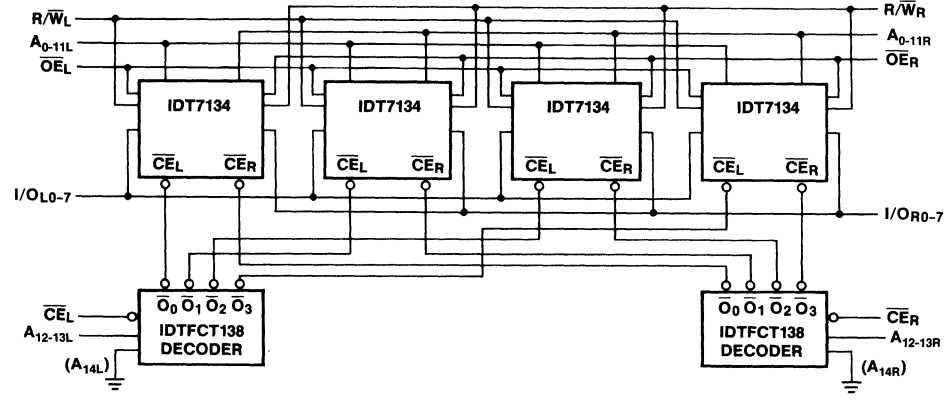
FUNCTIONAL BLOCK DIAGRAM

(A) IDT7M137 (32K x 8-BIT)



(B) IDT7M136 (16K x 8-BIT)



CMOS SLAVE DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

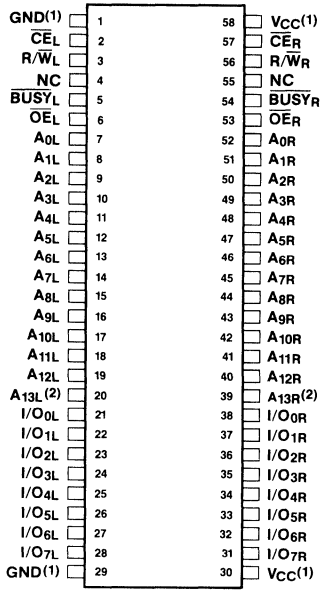
PRELIMINARY
IDT7M144S
IDT7M145S

Integrated Device Technology, Inc.

FEATURES:

- High-density 64K/128K-bit CMOS slave dual-port RAM module
- Easily expands data bus width to 16-or-more-bits when used with master IDT7M134 or IDT7M135
- 16K x 8 organization (IDT7M145) or 8K x 8 option (IDT7M144)
- High-speed access
  - —Military: 90/100/120/140ns (max.)
  - —Commercial: 70/90/100/120ns (max.)
- Low-power operation
  - —Active: 950mW (typ.) (IDT7M144)
  - —Standby: 20mW (typ.) (IDT7M144)
- $\overline{BUSY}$ input flags
- Fully asynchronous operation from either port
- Fully static operation
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B

PIN CONFIGURATION



DIP
TOP VIEW

DESCRIPTION:

The IDT7M144/145 are 64K/128K-bit high-speed CEMOS™ SLAVE dual-port static RAM modules constructed on a multi-layered, co-fired, ceramic substrate using four IDT7142 2K x 8 slave dual-port RAMs (IDT7M144) or eight IDT7142 slave dual-port RAMs (IDT7M145) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M144 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.)

The IDT7M144/145 are designed as "SLAVE" dual-port RAM modules to be used together with the IDT7M134/135 "MASTER" dual-port RAM modules in 16-or-more-bit systems; whereas, the IDT7M134/135 are designed to be used as stand-alone 8-bit dual-port RAM modules. Using the IDT MASTER/SLAVE dual-port RAM module approach in 16-or-more-bit memory system applications results in full speed operation without the need for additional discrete logic.

Both SLAVE IDT7M144/145 and MASTER IDT7M134/135 modules provide two ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive). The $\overline{BUSY}$ pins are outputs on the MASTER and inputs on the SLAVE.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
R/$\overline{W}_L$	R/$\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	BUSY FLAG
A_{0L}-A_{13L}	A_{0R}-A_{13R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On 8K x 8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
3. IDT7M134/135 (MASTER): $\overline{BUSY}$ is open drain output and requires pull up resistor. IDT7M144/145 (SLAVE): $\overline{BUSY}$ is input.

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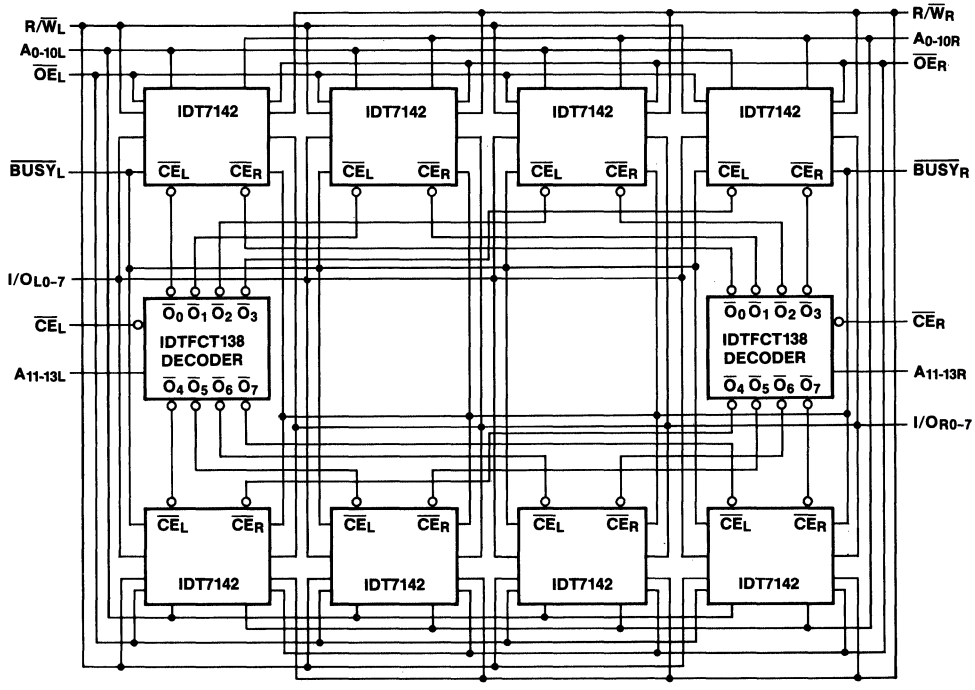
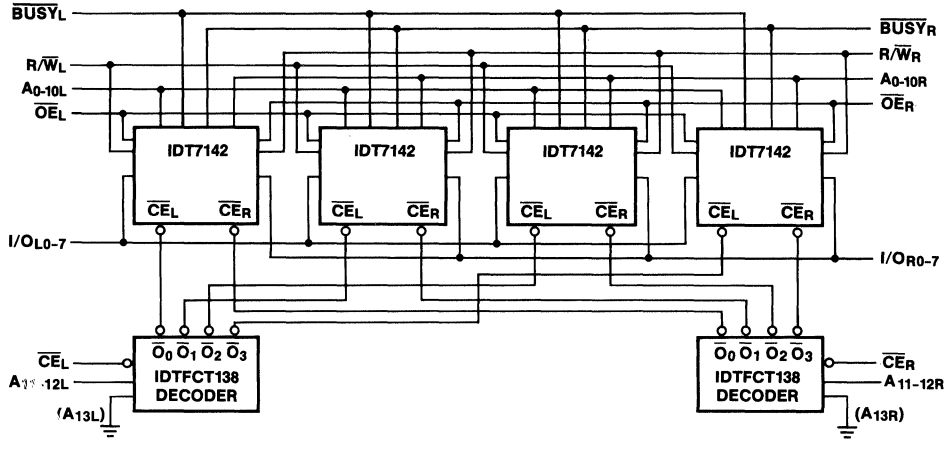
FUNCTIONAL BLOCK DIAGRAMS

(A) IDT7M145 (16K x 8-BIT)



(B) IDT7M144 (8K x 8-BIT)



(GROUND A_{13L} AND A_{13R} EXTERNALLY)

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

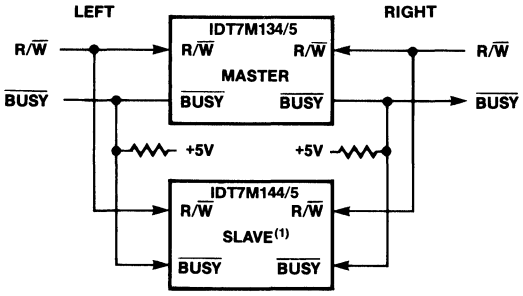
(DC electricals for the IDT7M144/IDT7M145 SLAVE Dual-Port are identical to the IDT7M134/IDT7M135 MASTER Dual-Port. Reference the IDT7M134/IDT7M135 CMOS Dual-Port RAM data sheet.)

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(AC electricals for the IDT7M144/IDT7M145 SLAVE Dual-Port are identical to the IDT7M134/IDT7M135 MASTER Dual-Port *except* where noted below.)

SYMBOL	PARAMETER	IDT7M144S70 IDT7M145S70 COM'L. ONLY		IDT7M144S90 IDT7M145S90		IDT7M144S100 IDT7M145S100		IDT7M144S120 IDT7M145S120		IDT7M144S140 IDT7M145S140 MIL. ONLY		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WP}	Write Pulse Width	40	—	50	—	60	—	70	—	80	—	ns
t_{WB}	Write to $\overline{BUSY}$	-10	—	-10	—	-10	—	-10	—	-10	—	ns
t_{WH}	Write Hold after $\overline{BUSY}$	20	—	20	—	20	—	20	—	20	—	ns

16-BIT MASTER/SLAVE DUAL PORT MEMORY SYSTEM



NOTE:

1. No arbitration in IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ IN inhibits write in IDT7M144/IDT7M145.

7

CMOS PARALLEL IN-OUT FIFO MODULE 2K x 9-BIT & 4K x 9-BIT

IDT7M203S
IDT7M204S

Integrated Device Technology, Inc.

FEATURES:

- First-In, First-Out memory module
- 2K x 9 organization (IDT7M203S)
- 4K x 9 organization (IDT7M204S)
- Low-power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™ technology
- Pin compatible with IDT7201 and Mostek MK4501, but with four times word depth (IDT7M203S) or eight times (IDT7M204S)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M203/204 are FIFO memory modules that utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

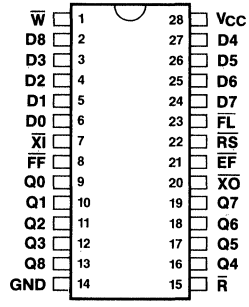
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz) for commercial and 70ns (14MHz) for military temperature ranges.

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

The IDT7M203/204 are constructed on a multi-layered ceramic substrate using four IDT7201 (512x9) or four IDT7202 (1Kx9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7201s and IDT7202s fabricated in IDT's high-performance CEMOS technology.

IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



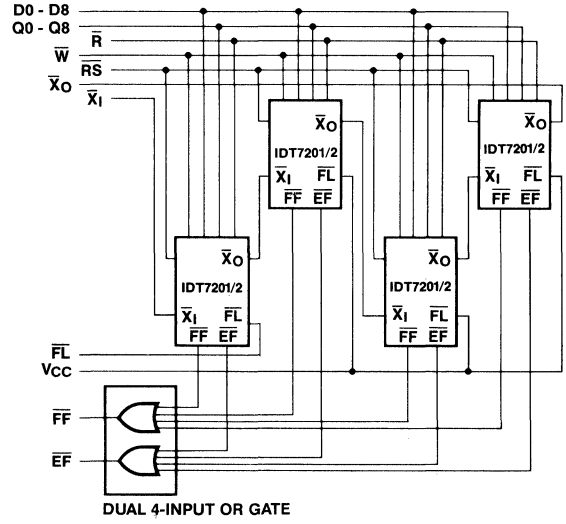
DIP
TOP VIEW

SSD7M203-001

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85°	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M203S IDT7M204S COMMERCIAL			IDT7M203S IDT7M204S MILITARY			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{IL}	Input Leakage Current (Any Input)	-5	—	5	-10	—	10	μA	1
I_{OL}	Output Leakage Current	-10	—	10	-10	—	10	μA	2
V_{OH}	Output Logic "1" Voltage I_H = -2mA	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_L = 8mA	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	110	176	—	155	230	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ = V_{IH})	—	20	33	—	30	60	mA	3
I_{CC3}	Power Down Current (All Input = V_{CC} -0.2V)	—	—	20	—	—	36	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

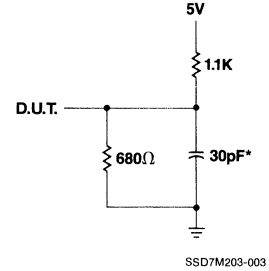
SYMBOL	PARAMETER	7M203/4S40 COM'L. ONLY		7M203/4S50		7M203/4S55		7M203/4S65		7M203/4S100		7M203/4S140		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_A	Access Time	—	40	—	50	—	55	—	65	—	100	—	140	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	30	—	35	—	40	—	50	ns
t_{WC}	Write Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{DS}	Data Setup Time	20	—	25	—	30	—	40	—	50	—	50	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	65	—	70	—	85	—	125	—	165	ns
t_{REF}	Read Low to Empty Flag Low	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{RFF}	Read High to Full Flag High	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{WEF}	Write High to Empty Flag High	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{WFF}	Write Low to Full Flag Low	—	45	—	50	—	55	—	60	—	95	—	135	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

NOTE:
Generating $\overline{R}/\overline{W}$ Signals — When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important to not have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ lines (violates the V_{IH}, V_{IL} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 5ns can affect the read or write pointer and cause it to increment.



SSD7M203-003

*Includes jig and scope capacitances.

Figure 1. Output Load.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0-D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2: i.e., t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and $\overline{W}$ should not change until t_{RSR} after the rising edge of $\overline{RS}$.

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the data outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$; so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD ($\overline{FL}$)

This pin is grounded to indicate that it is the first device. In the multiple mode (depth expansion mode) application, this pin on the rest of the devices should connect to V_{CC} for proper operation.

EXPANSION IN ($\overline{XI}$)

EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper application.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

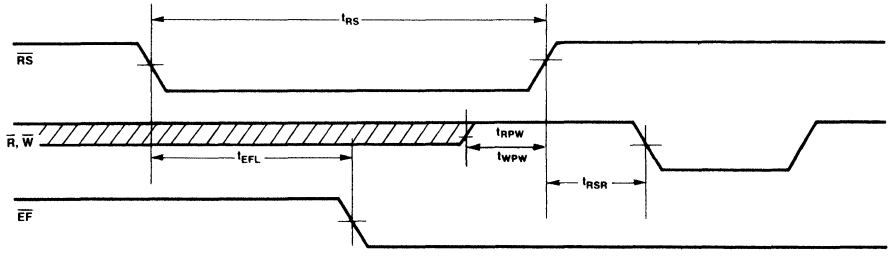
The FULL FLAT ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indiciating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 2048 writes for the IDT7M203 and 4096 writes for the IDT7M204.

EXPANSION OUT ($\overline{XO}$)

EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expanion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q0-Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



DSP7201-005

NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

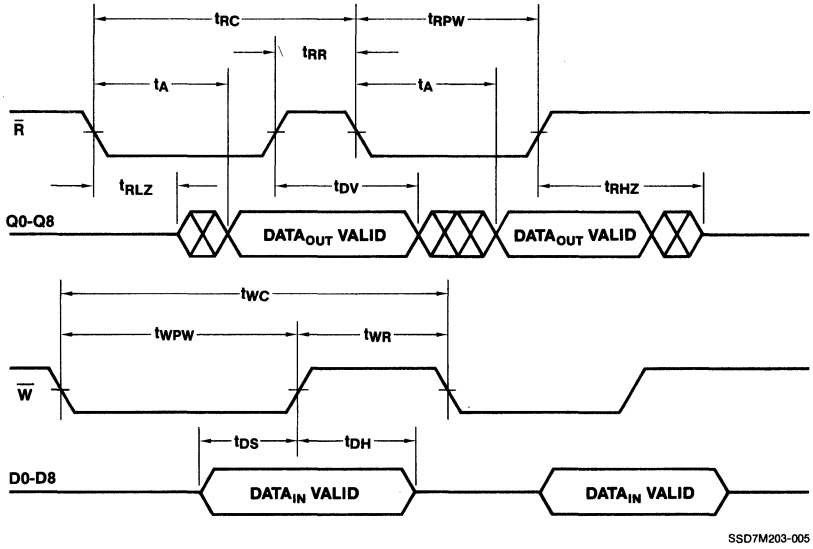


Figure 3. Asynchronous Write and Read Operation

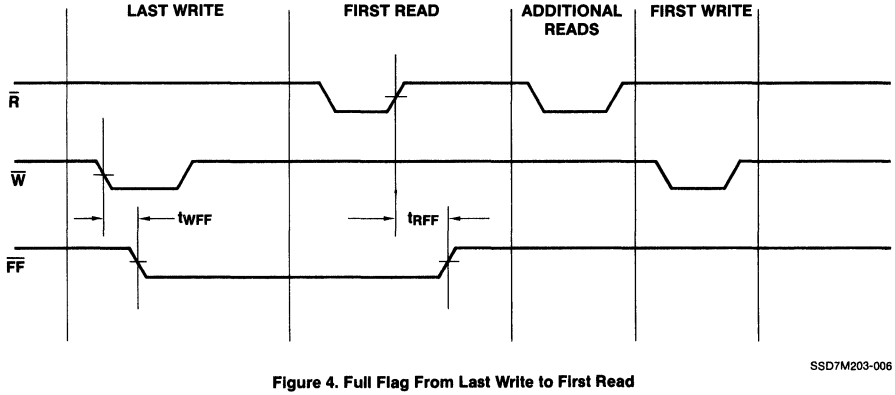


Figure 4. Full Flag From Last Write to First Read

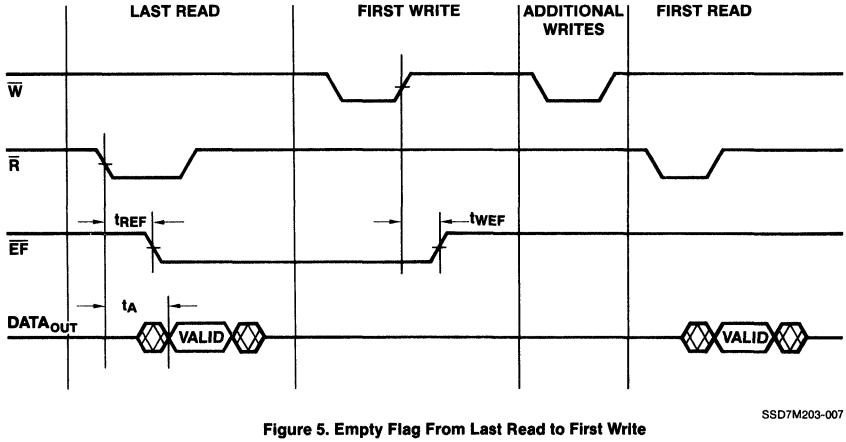
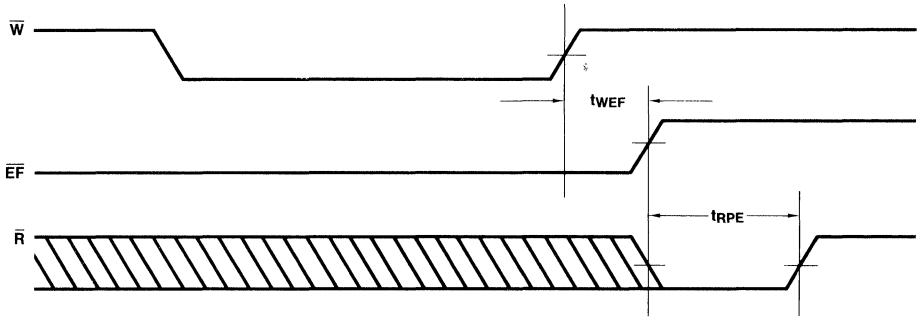


Figure 5. Empty Flag From Last Read to First Write

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

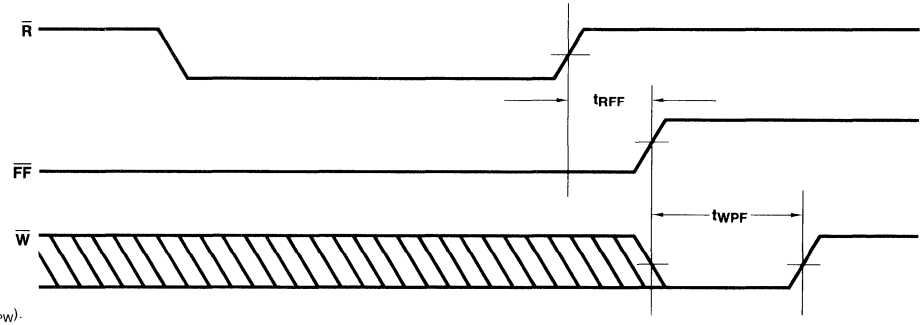


NOTE:
1. ($t_{RPE} = t_{RPW}$)

SSD7M203-008

Figure 6. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:
1. ($t_{WPF} = t_{WPW}$).

SSD7M203-009

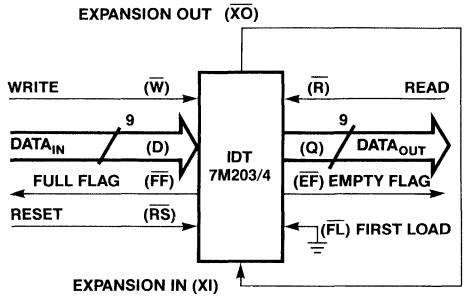
Figure 7. Full Flag Timing

OPERATING MODES:
SINGLE DEVICE MODE

A single IDT7M203/IDT7M204 may be used when the application requirements are for 2048/4096 words or less. The IDT7M203/IDT7M204 is a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M203/ IDT7M204s. Any word width can be attained by adding additional IDT7M203/IDT7M204s.



SSD7M203-010

Figure 8. Block Diagram of Single IDT7M203/IDT7M204 FIFO

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M203/IDT7M204 can easily be adapted to applications when the requirements are for greater than 2048/4096 words. Figure 10 demonstrates Depth Expansion using three IDT7M203/IDT7M204s. Any depth can be attained by adding additional IDT7M203/IDT7M204s. The IDT7M203/IDT7M204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 10.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 10.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 11.)

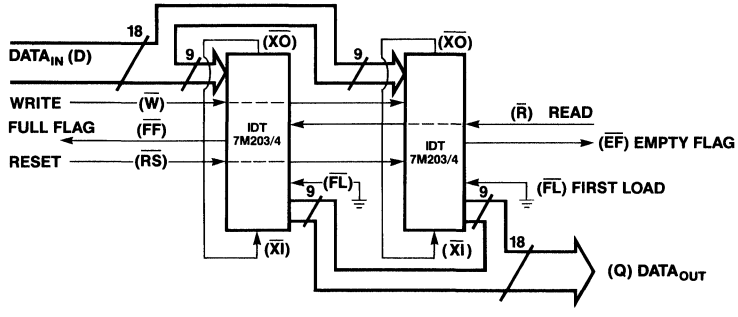
BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7M203/IDT7M204s as is shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7M203/IDT7M204: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the empty flag); however, the same word (written on the first edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In a write flow-through mode (Figure 14), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted, but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, a new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and increment the write pointer.



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 2048x18/4096x18 FIFO Memory Used in Width Expansion Mode

TABLE I — RESET — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUT	INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	Location Zero	Location Zero	0	1
Read/Write	1	Increment(1)	Increment(1)	X	X

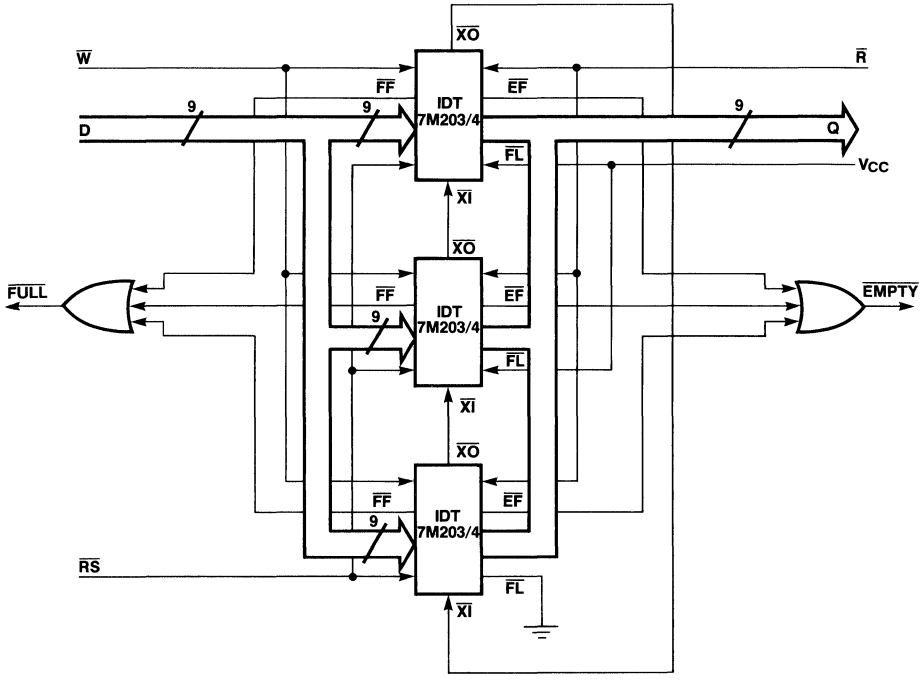
NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

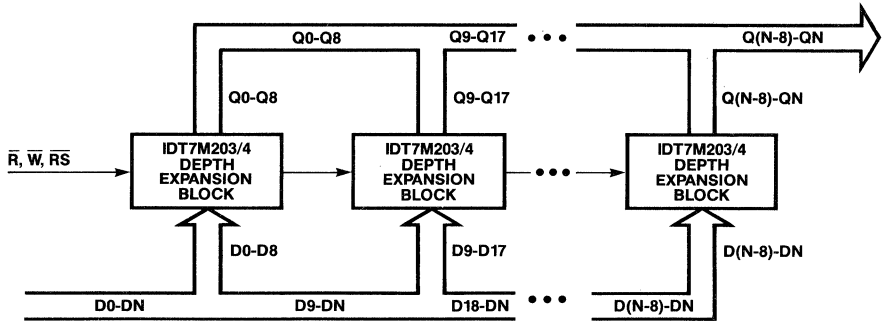
NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 10.

$\overline{RS}$ = Reset Input, $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.



SSD7M203-012

Figure 10. Block Diagram of 6144x9/12288x9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For flag detection see WIDTH expansion Section and Figure 9.

Figure 11. Compound FIFO Expansion

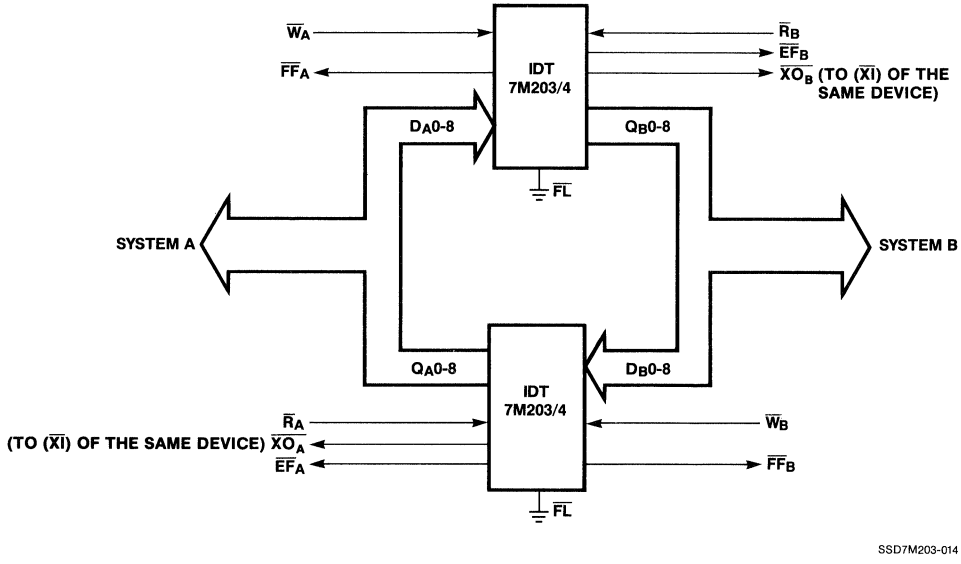
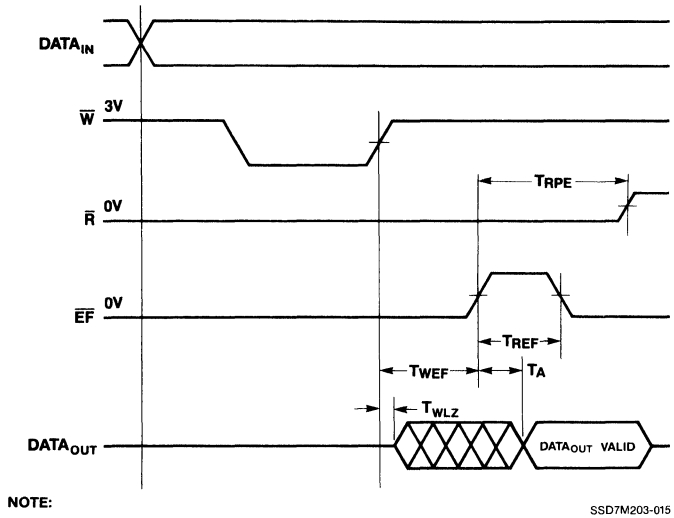
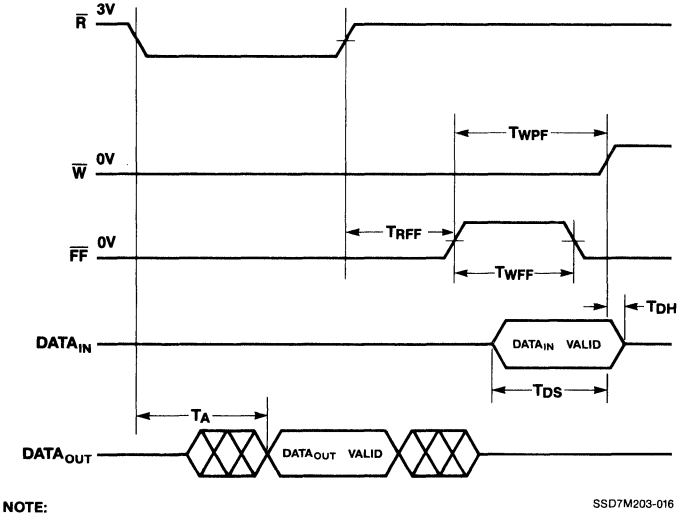


Figure 12. Bidirectional FIFO Mode



NOTE:
($T_{RPE} = T_{RPW}$)

Figure 13. Read Data Flow-Through Mode



NOTE:
($T_{WPF} = T_{WPW}$)

Figure 14. Write Data Flow-Through Mode

7

CMOS PARALLEL IN-OUT FIFO MODULE 8K x 9-BIT & 16K x 9-BIT

ADVANCE INFORMATION
IDT7M205
IDT7M206

Integrated Device Technology, Inc.

FEATURES:

- First-In, First-Out memory module
- 8K x 9 organization (IDT7M205)
- 16K x 9 organization (IDT7M206)
- Low power consumption
  - —Active: 900mW (typ.)
  - —Power Down: 50mW (typ.)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™ technology
- Pin compatible with IDT7201 and Mostek MK4501, but with 16 times word depth (IDT7M205) or 32 times (IDT7M206)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

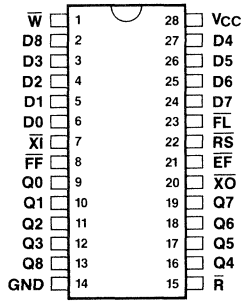
The IDT7M205/206 are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7203 (2K x 9) or four IDT7204 (4K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high-performance CEMOS technology. These devices utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 75ns (13MHz) for commercial and 80ns (12.5MHz) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



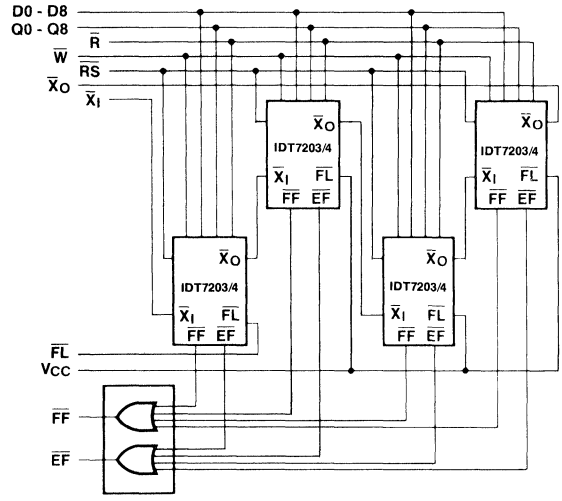
SSD7M203-001

DIP
TOP VIEW

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

CEMOS is a trademark of Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM MODULE

IDT7M624S

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - —Military: 45ns (max.)
  - —Commercial: 30ns (max.)
- Low power consumption
  - — Active 4.8W (typ. in 64K x 16 organization)
  - — Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin compatible with IDT7M656 (256K RAM module)
- Single 5V (±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 (64K x 1) static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

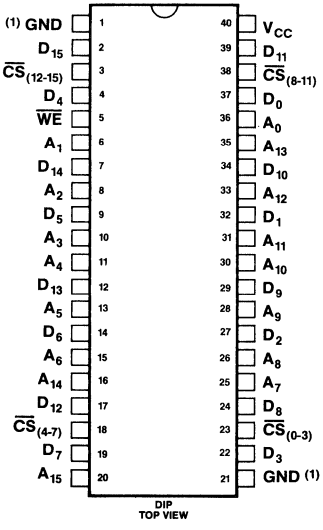
The IDT7M624 is available with access times as fast as 30ns commercial and 45ns military temperature range, with maximum operating power consumption of only 10.7W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.5W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP to take advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



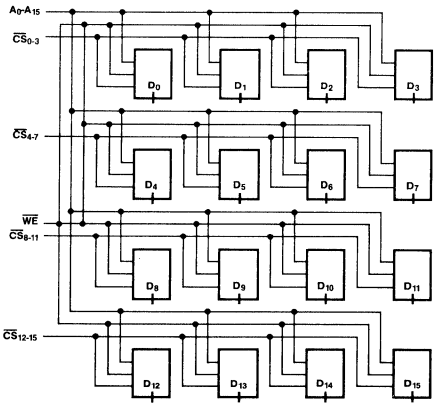
DIP
TOP VIEW

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

NOTE:
1. Both GND pins need to be grounded for proper operation.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	8	8	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M624S			UNIT
			MIN.	TYP.(1)	MAX.	
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	20	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}_{XX}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = fMax.	—	960	1950	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	720	1380	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	600	1100	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX} \geq V_{IH}$, (TTL Level), V_{CC} = 5.5V, Output Open	—	480	820	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V (CMOS Level)	—	0.32	320(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = 4.5V	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = 4.5V	2.4	—	—	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. I_{SB1} max. at commercial temperature = 240 mA.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

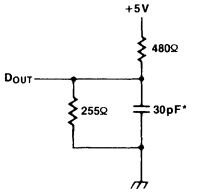


Figure 1. Output Load

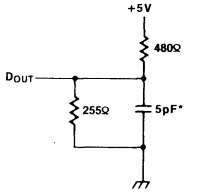


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

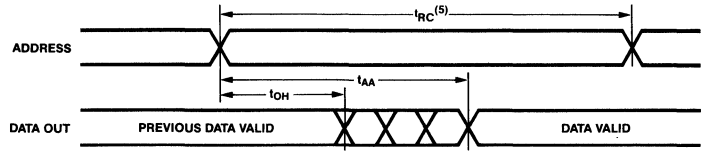
*Including scope and jig.

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

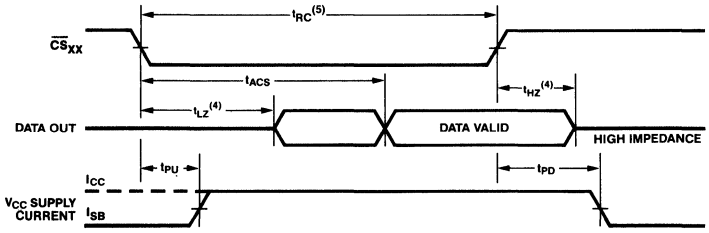
SYMBOL	PARAMETER	IDT7M624S30 COM'L ONLY MIN.	MAX.	IDT7M624S45 MIN.	MAX.	IDT7M624S55 MIN.	MAX.	IDT7M624S65 MIN.	MAX.	IDT7M624S85 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	30	—	45	—	55	—	65	—	85	—	ns
t_{AA}	Address Access Time	—	30	—	45	—	55	—	65	—	85	ns
t_{ACS}	Chip Select Access Time	—	30	—	45	—	55	—	65	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	—	25	—	30	—	30	—	30	—	4υ	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Selection to Power Down Time	—	30	—	35	—	35	—	35	—	40	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	30	—	45	—	55	—	65	—	85	—	ns
t_{CW}	Chip Selection to End of Write	25	—	40	—	50	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	25	—	40	—	50	—	55	—	65	—	ns
t_{AS}	Address Setup Time	3	—	5	—	5	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	35	—	40	—	45	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	0	25	0	30	0	30	0	35	0	40	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

7

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



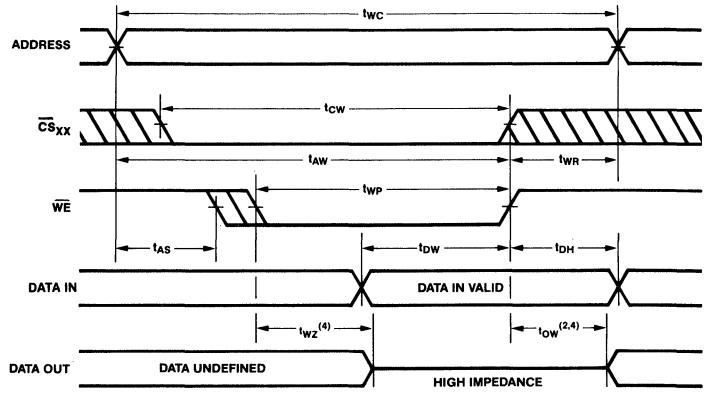
TIMING WAVEFORM OF READ CYCLE NO.2(1,3)



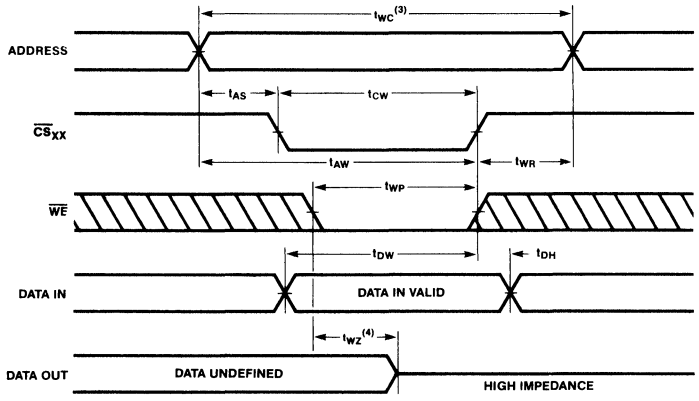
NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transititioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



NOTES:

1. $\overline{CS}_{XX}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}_{XX}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}_{XX}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	130	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE:

1. This parameter is sampled and not 100% tested.

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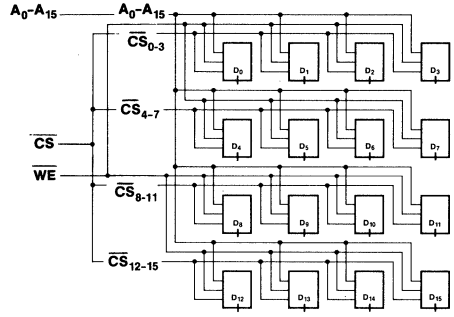
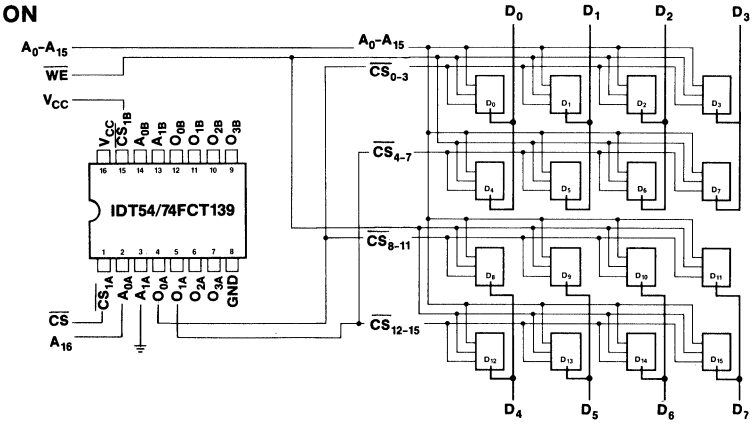
IDT7M624
64K x 16 CONFIGURATION



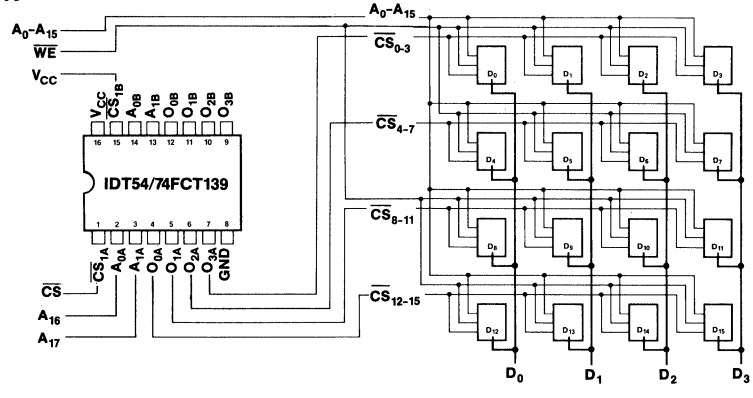
NOTE:
All chips selects tied together since, in a by 16 configuration, all chips are either on or off.

IDT7M624
128K x 8 CONFIGURATION



NOTE:
The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{16}) to determine which of the two banks of memory are enabled.

IDT7M624
256K x 4 CONFIGURATION



NOTE:
Each chip select is now controlled by the two higher order address pins A_{16} and A_{17}.

Integrated Device Technology, Inc.

256K CMOS STATIC RAM MODULE

IDT7M656L

FEATURES:

- High-density 256K-bit CMOS static RAM Module
- Customer-configured to 16Kx16, 32Kx8 or 64Kx4
- Fast access times
  - —Commercial — 25ns
  - —Military — 35ns
- Low-power consumption
  - —Active: 3.2W (typ.) (in 16K x 16 organization)
  - —Standby: 0.16mW (typ.)
- Utilizes 16 IDT6167s — high-performance 16K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Module available with components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M656 is a 256K-bit high-speed CMOS static RAM constructed on a multilayered ceramic substrate using 16 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Making 4 chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 16Kx16, 32Kx8 or 64Kx4 organization. In addition, extremely high speeds are achievable by the use of IDT6167s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides some of the fastest 16K static RAMs available.

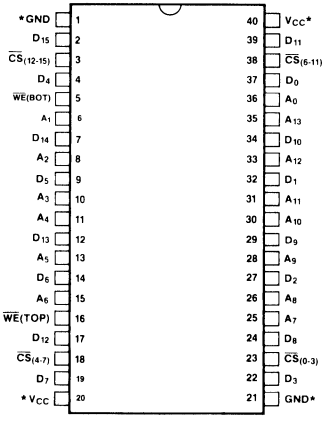
The IDT7M656 is available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 7.0W (significantly less if organized 32K x 8 or 64K x 4). The RAM Module also offers a maximum standby power mode of 2.2W and a maximum full standby mode of 82.5mW.

The IDT7M656 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT6167s in leadless chip carriers.

All inputs and outputs of the IDT7M656 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Full asyncronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

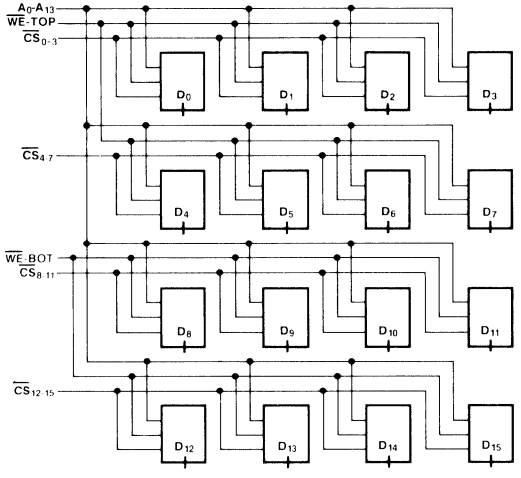
SRD7M656-001

* Both V_{CC} pins need to be connected to the 5V Supply, and both GND pins need to be grounded for proper operation.

PIN NAMES

A_{XX}	ADDRESSES	D_{XX}	DATA IN/OUT
$\overline{CS}_{XX}$	CHIP SELECTS	V_{CC}	POWER
$\overline{WE}_{XX}$	WRITE ENABLES	GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



SRD7M656-002

CEMOS is a trademark of Integrated Device Technology, Incorporated.

7

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	8.0	8.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} min = -1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M656L MIN.	TYP.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	640	1280	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	420	840	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	310	620	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	200	400	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{CC} - 0.2V (CMOS Level) V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.032	15(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V

NOTES

1. V_{CC} = 5V, T_A = +25°C
2. I_{SB1} max. at commercial temperature = 5.0mA

TRUTH TABLE

MODE	$\overline{CS}_{XX}$	$\overline{WE}_{XX}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	200	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	60	pF

NOTES:

1. This parameter is sampled and not 100% tested.
2. For each output, 16K x 16 mode.

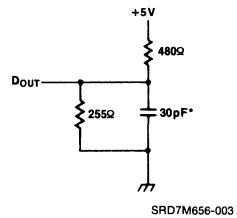


Figure 1. Output Load

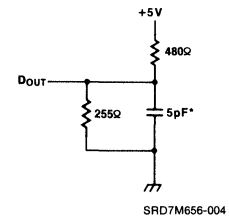


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

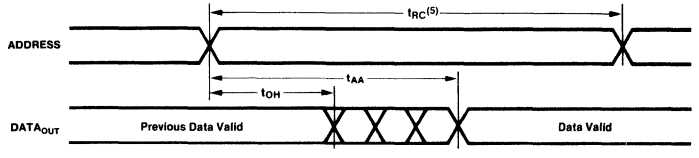
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7M656L25[1] COM'L. ONLY MIN.	MAX.	IDT7M656L35 MIN.	MAX.	IDT7M656L55 MIN.	MAX.	IDT7M656L65 MIN.	MAX.	IDT7M656L85 MIN.	MAX.	IDT7M656L100 MIL. ONLY MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	25	—	35	—	55	—	65	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	55	—	65	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	—	55	—	65	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z	—	15	—	20	—	40	—	40	—	50	—	50	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time	—	25	—	35	—	55	—	65	—	85	—	100	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	—	35	—	55	—	65	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	20	—	30	—	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	25	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Setup Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	—	10	—	15	—	40	—	40	—	50	—	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

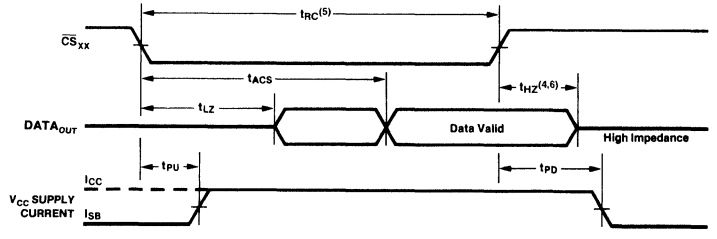
1. IDT7M656L25 will not have low V_{CC} data retention characteristics.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



SRD7M656-005

TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

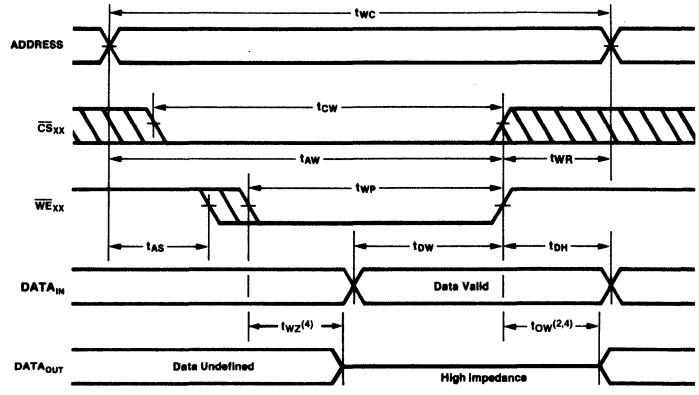


SRD7M656-006

NOTES:

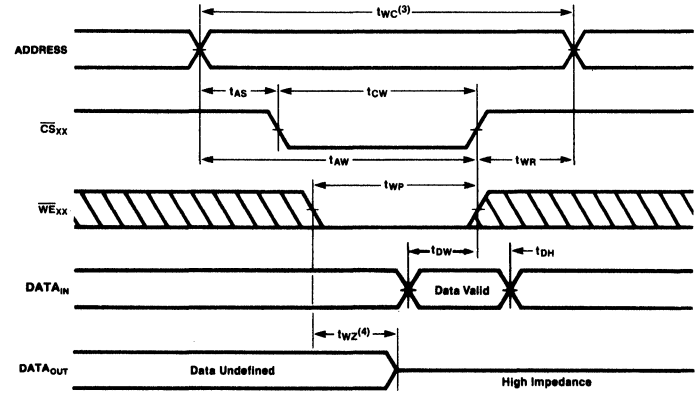
1. $\overline{WE}_{XX}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



SRD7M656-007

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



SRD7M656-008

NOTES:

1. $\overline{CS}_{XX}$ or $\overline{WE}_{XX}$ must be high during address transitions.
2. If $\overline{CS}_{XX}$ goes high simultaneously with $\overline{WE}_{XX}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.

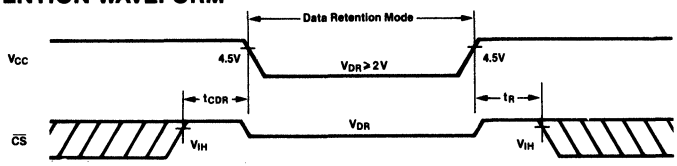
LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C and 0°C to +70°C) (Except IDT7M656L25)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX. COM'L.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_{XX} \geq V_{CC} - 0.2V$	—	.01(2)	2.0(2)	6.0	mA
		$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	.02(3)	3.0(3)	9.0	
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES:

1. T_A = +25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

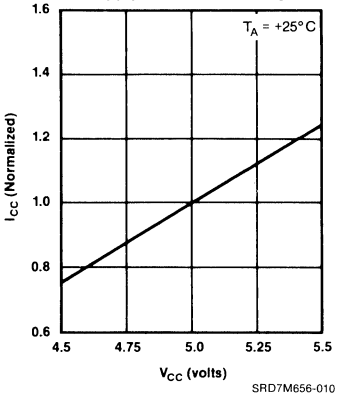
LOW V_{CC} DATA RETENTION WAVEFORM



SRD7M656-009

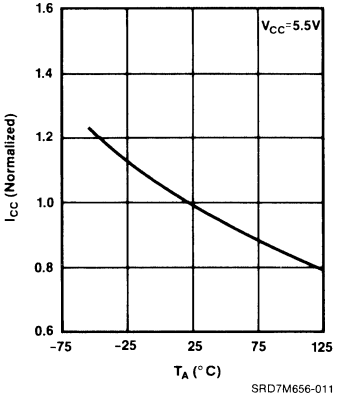
NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs. Voltage



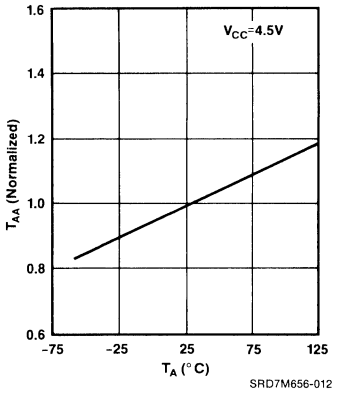
SRD7M656-010

Supply Current vs. Ambient Temperature



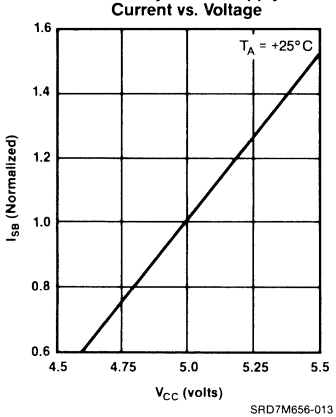
SRD7M656-011

Address Access Time vs. Ambient Temperature



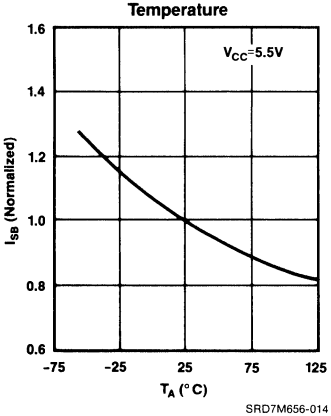
SRD7M656-012

Stand-by Power Supply Current vs. Voltage



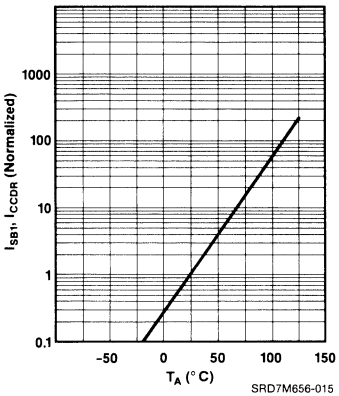
SRD7M656-013

Stand-by-Power Supply Current vs. Ambient Temperature



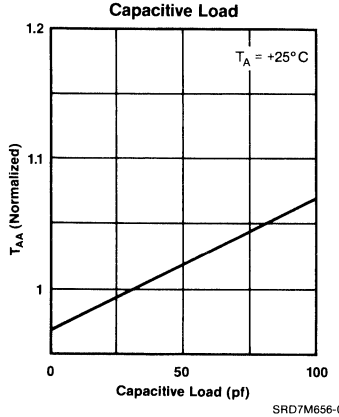
SRD7M656-014

Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



SRD7M656-015

Address Access Time vs. Capacitive Load

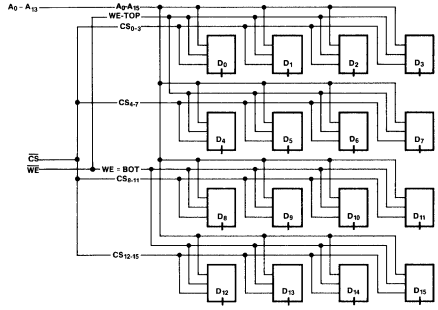


SRD7M656-016

7

IDT7M656

16K x 16 CONFIGURATION

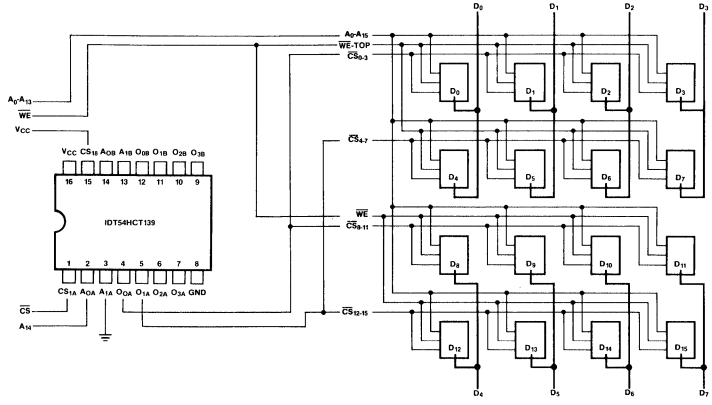


SRD7M656-017

NOTES:

1. All chip selects tied together since, in a by 16 configuration, all chips are either on or off.
2. The two write enables are tied together allowing control of the write enable for entire memory at one time (necessary) in a by 16 organization since all chips are either writing or reading at any given time.

32K x 8 CONFIGURATION

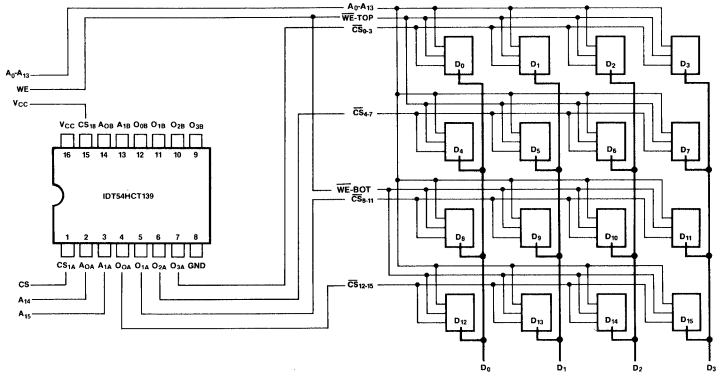


SRD7M656-018

NOTES:

1. The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{14}) to determine which of the two banks of memory are enabled.
2. The two write enables are tied together for ease of layout. They could be controlled by the decoder similar to the chip selects but would save only a minimal amount of power and add complexity to the layout.

64K x 4 CONFIGURATION



SRD7M656-019

NOTES:

1. Each chip select is now controlled by the two higher order address pins A_{14} (necessary in 64K deep memory).
2. Again the two write enables are tied together for ease of layout (the megabit part will only have one write enable pin).

Integrated Device Technology, Inc.

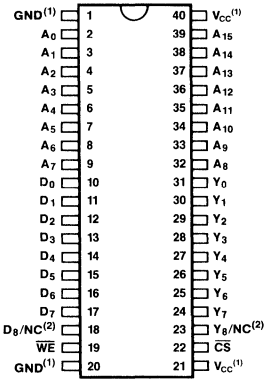
512K (64K x 8-BIT or 64K x 9-BIT) CMOS STATIC RAM MODULE

IDT7M812
IDT7M912

FEATURES

- High-density 512K-bit CMOS static RAM module
- 64Kx8 (IDT7M812) or 64Kx9 (IDT7M912) configuration
- Fast access times
  - — Military: 55ns (max.)
  - — Commercial: 45ns (max.)
- Low power consumption
  - —Active 2.4W (typ. in 64K x 8 organization)
  - —Standby: 240μW (typ. in 64Kx8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT7187 high-performance 64Kx1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

PIN CONFIGURATION



SSD7M812-001

DIP
TOP VIEW

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. Pin 18 is D_8 and pin 23 is Y_8 in 64K x 9 (IDT7M912) option, and both 18 and 23 are NC in 64K x 8 (IDT7M812) option.

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64Kx1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7M812/IDT7M912 are available with access times as fast as 45ns commercial and 55ns military temperature range, with maximum operating power consumption of only 5.9W (IDT7M912, 64Kx9 option). The module also offers a standby power mode of less than 2.5W (max.) and a full standby mode of 1W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

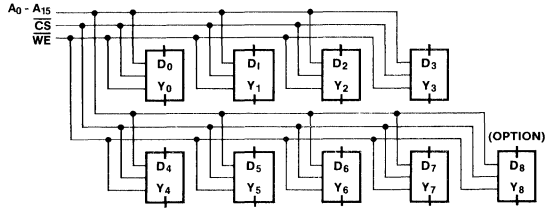
All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

A_0 - A_{15}	ADDRESS
D_0 - D_8	DATA INPUT
Y_0 - Y_8	DATA OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
V_{CC}	POWER
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



SSD7M812-002

CEMOS is a trademark of Integrated Device Technology, Incorporated.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	8	8	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M912 MIN.	IDT7M912 TYP.(1)	IDT7M912 MAX.	IDT7M812 MIN.	IDT7M812 TYP.(1)	IDT7M812 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V; V_{IN} = GND to V_{CC}	—	—	20	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	—	—	20	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open Min. Duty Cycle = 100%	—	540	1080	—	480	960	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% Output Open	—	540	1080	—	480	960	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ Min. Duty Cycle = 100%	—	270	450	—	240	400	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $\leq$ 0.2V	—	0.2	180(2)	—	0.05	160(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C.
2. I_{SB1} (max.) of IDT7M812/912 at commercial temperature = 80mA/90mA.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

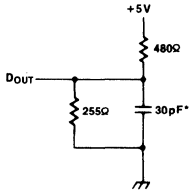


Figure 1. Output Load

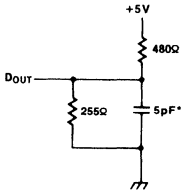


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

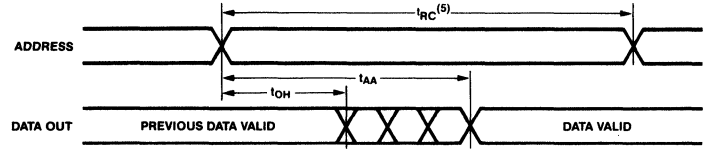
*Including scope and jig.

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

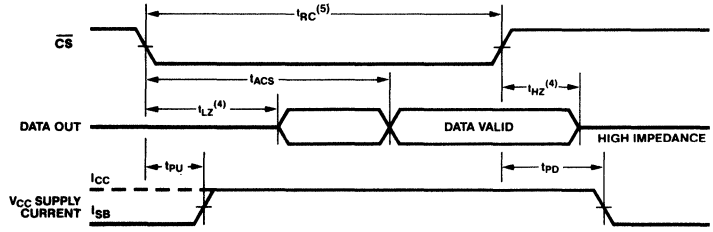
SYMBOL	PARAMETER	IDT7M912S45 IDT7M812S45 COM'L ONLY		IDT7M912S55 IDT7M812S55		IDT7M912S65 IDT7M812S65		IDT7M912S85 IDT7M812S85		IDT7M912S100 IDT7M812S100 MIL. ONLY		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	45	—	55	—	65	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	65	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	45	—	55	—	65	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	—	30	—	30	—	30	—	40	—	50	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Selection to Power Down Time	—	35	—	35	—	35	—	40	—	50	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	45	—	55	—	65	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	40	—	50	—	55	—	65	—	75	—	ns
t_{AW}	Address Valid to End of Write	40	—	50	—	55	—	65	—	75	—	ns
t_{AS}	Address Setup Time	5	—	5	—	5	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	25	—	30	—	35	—	45	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	0	30	0	30	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns

7

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



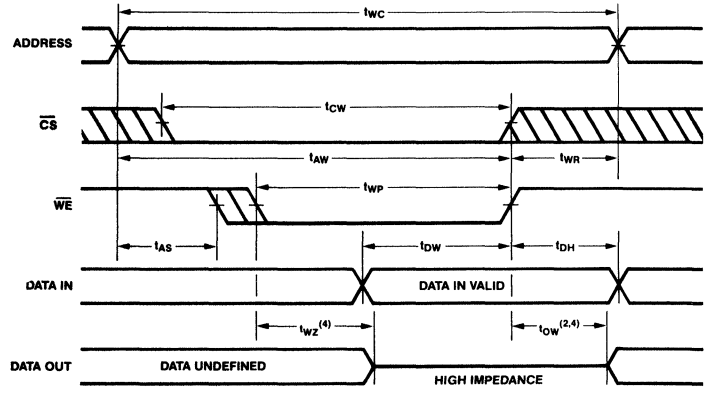
TIMING WAVEFORM OF READ CYCLE NO.2(1,3)



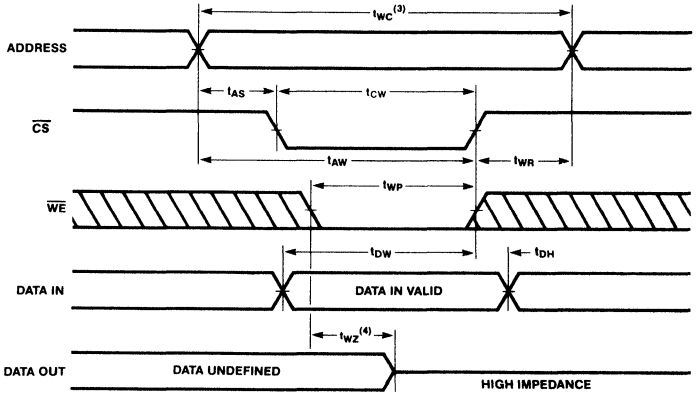
NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage specified loading in Figure 2. This parameter is sampled, not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

SYMBOL	ITEM	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:
This parameter is sampled and not 100% tested.

7

Integrated Device Technology, Inc.

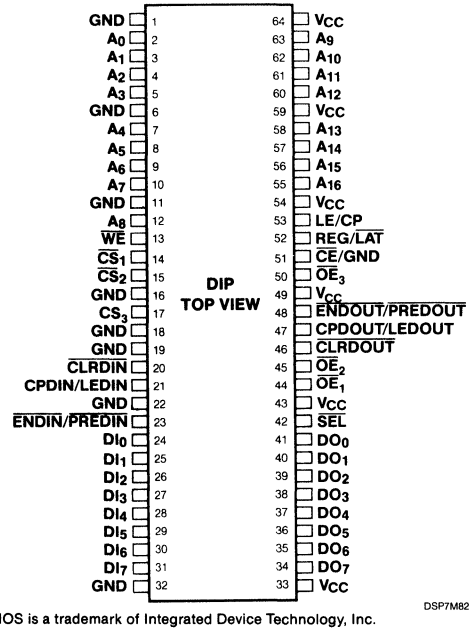
1 MEGABIT REGISTERED/ BUFFERED/LATCHED CMOS STATIC RAM MODULES

ADVANCE INFORMATION IDT7M824S FAMILY

FEATURES:

- High-density 1024K-bit (128K x 8-bit) CMOS static RAM modules with registered/buffered/latched addresses and I/Os
- Fast access times: 75ns max. commercial and military
- Low-power consumption (typ.): active 980mW; standby 150mW; full-standby 1.6mW
- Low input capacitance (typ.): input 20pF; output 25pF
- High output drive (min.): I_{OL} = 32mA; I_{OH} = −15mA
- 64-pin, 900 mil center sidebraze DIP with LCCs on both sides, achieving very high memory density
- Module select output
- Separate inputs and outputs
- Clear data and clock enables on all registers
- Addresses, inputs and outputs on separate clocks or latch enables
- Registered write enable
- Internal bypass capacitors for minimizing power supply noise
- TTL compatible; single 5V (±10%) power supply
- Five GND pins for maximum noise immunity, 5 V_{CC} pins
- Military grade module available with semiconductor components 100% manufactured and screened to MIL-STD-883, Class B

PIN CONFIGURATION



DSP7M824S-002

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DESCRIPTION:

The IDT7M824 family is a set of 1024K-bit (128K x 8-bit) high-speed CMOS static RAM modules with registered/buffered/latched addresses and I/Os. They are constructed on co-fired, multi-layered ceramic substrates with sidebrazed leads using 16 IDT71981 (16K x 4) static RAMs, IDT logic devices, and decoupling capacitors. Devices in leadless chip carriers are mounted top and bottom for maximum density.

Extremely high speeds are achievable by the use of IDT71981s and logic devices fabricated in IDT's high-performance, high-reliability technology, CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest circuits possible. The IDT7M824 has access times of 75ns (max.) over commercial and military temperature ranges, but it can be operated with cycle times as fast as 50ns if skewed clocks are used.

Designing with this device can be very flexible because of such features as module select output and clock enables on all registers, registered write enable and 8-bit separate inputs and outputs. Because of the proprietary IDT49C801, the modules are cascadable in terms of depth. The write enable can be turned off when the module is de-selected. Immunity to noise has been extended with such features as 8-bit separate inputs and outputs; addresses, inputs, and outputs on separate clocks; internal decoupling capacitors; five ground pins; and five V_{CC} pins.

The semiconductor components used on all IDT military modules are 100% processed to the test methods of MIL-STD-883, Class B. In addition IDT military modules are qualified to requirements patterned after MIL-STD-883, Method 5005 making them ideally suited to applications demanding the highest level of performance and reliability.

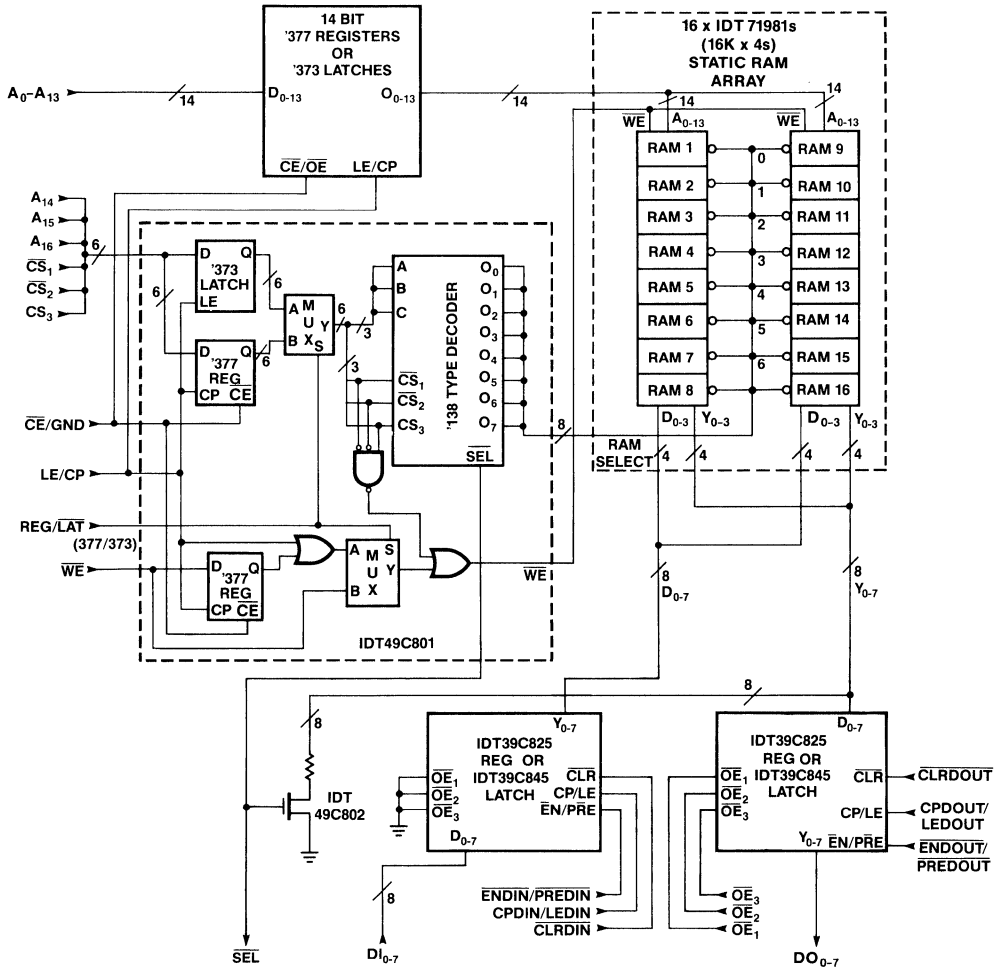
PRODUCT SELECTOR GUIDE

DATA INPUT & OUTPUT FEATURE	ADDRESS	
	REGISTERED	LATCHED
Input — Registered Output — Registered	IDT7M824SA	IDT7M824SE
Input — Registered Output — Latched	IDT7M824SB	IDT7M824SF
Input — Latched Output — Registered	IDT7M824SC	IDT7M824SG
Input — Latched Output — Latched	IDT7M824SD	IDT7M824SH

NOTE:

All V_{CC} pins (33, 43, 49, 54, 59 and 64) need to be connected to the 5V supply. and all GND pins (1, 6, 11, 16, 18, 19, 22, and 32) need to be grounded for proper operation.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{16}$	Addresses
$DI_0 - DI_7$	Data input
$DO_0 - DO_7$	Data output
$\overline{CLRDIN}$	Data input latch/register clear
CPDIN/LEDIN	Data input register clock/latch enable
$\overline{ENDIN}/\overline{PREDIN}$	Data input register clock enable/ latch preset
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output enable
CPDOUT/LEDOUT	Data output register clock/latch enable
$\overline{ENDOUT}/\overline{PREDOUT}$	Data output register clock enable/ latch preset
$\overline{CS}_1$, $\overline{CS}_2$ & CS_3	Chip select
$\overline{WE}$	Write enable
$\overline{SEL}$	Select output
LE/CP	Latch enable/clock pulse control input
$\overline{CE}$/GND	Clock enable/ground
REG/$\overline{LAT}$	Register/latch (low active) input control
V_{CC}	Power
GND	Ground

Integrated Device Technology, Inc.

256K (32K x 8-BIT) CMOS STATIC RAM MODULE

IDT7M856S

FEATURES:

- High-density 256K (32K x 8-bit) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed — 40ns (max.) commercial; 55ns (max.) military
- Low-power consumption; typically less than 1W operating, less than 1mW in standby
- Utilizes IDT7198s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7198 (16,384 x 4) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder, used as an inverter, that interprets the higher order address A_{14} to select two of the four 16K x 4 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

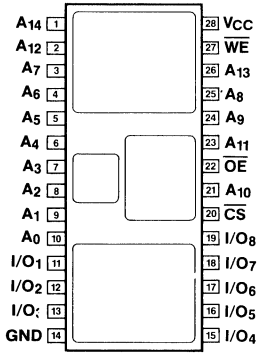
The IDT8M856 is available with maximum access times as fast as 40ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 2 watts. The circuit also offers a reduced power standby mode. When CS goes high, the circuit will automatically go to a standby mode with power consumption of only 1.1mW (max.). Substantially lower power levels can be achieved in a full standby mode (440mW max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT7M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

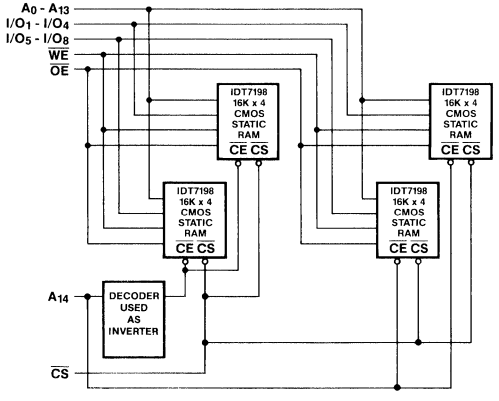


DIP
TOP VIEW

PIN NAMES

A_0 - A_{14}	ADDRESSES
I/O_1 - I/O_8	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = 0	—	190	380	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	190	380	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	90	200	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V (CMOS Level) V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.2	80(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V I_{OL} = 8mA, V_{CC} = 4.5V	— —	— —	0.5 0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = 4.5V	2.4	—	—	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB1} at commercial temperature = 60mA.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

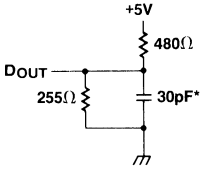


Figure 1. Output Load

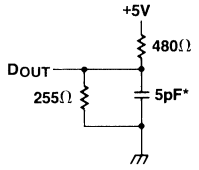


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M856S40 MIN.	IDT7M856S40 MAX.	IDT7M856S50 MIN.	IDT7M856S50 MAX.	IDT7M856S60 MIN.	IDT7M856S60 MAX.	IDT7M856S70 MIN.	IDT7M856S70 MAX.	IDT7M856S85 MIN.	IDT7M856S85 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	40	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	40	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	40	—	50	—	55	—	65	—	80	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	15	—	15	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z	—	15	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	40	—	50	—	60	—	70	—	85	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	40	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	35	—	45	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End or Write	35	—	45	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	5	—	5	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	20	—	20	—	25	—	30	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

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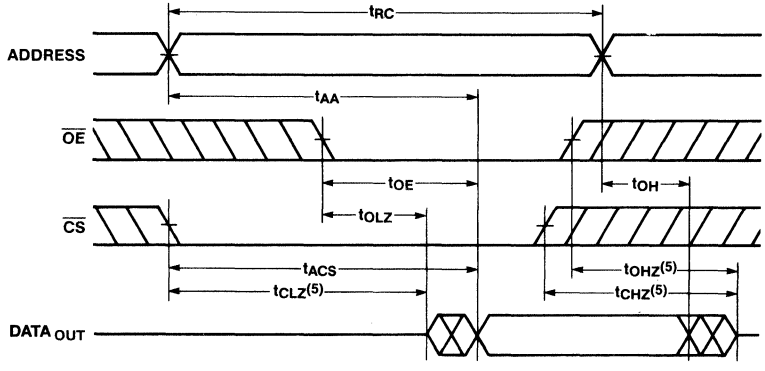
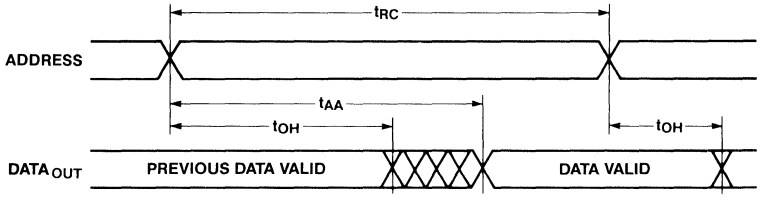
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M856S55 MIN.	IDT7M856S55 MAX.	IDT7M856S65 MIN.	IDT7M856S65 MAX.	IDT7M856S75 MIN.	IDT7M856S75 MAX.	IDT7M856S90 MIN.	IDT7M856S90 MAX.	IDT7M856S100 MIN.	IDT7M856S100 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	75	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	55	—	65	—	80	—	90	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	50	—	60	—	65	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	55	—	65	—	75	—	90	—	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AW}	Address Valid to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AS}	Address Setup Time	5	—	10	—	10	—	15	—	15	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	25	—	30	—	40	—	50	—	50	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	35	—	45	—	45	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

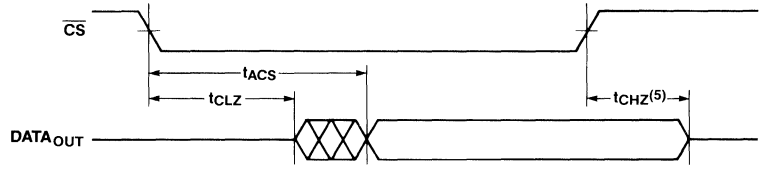


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD7198S/L-008

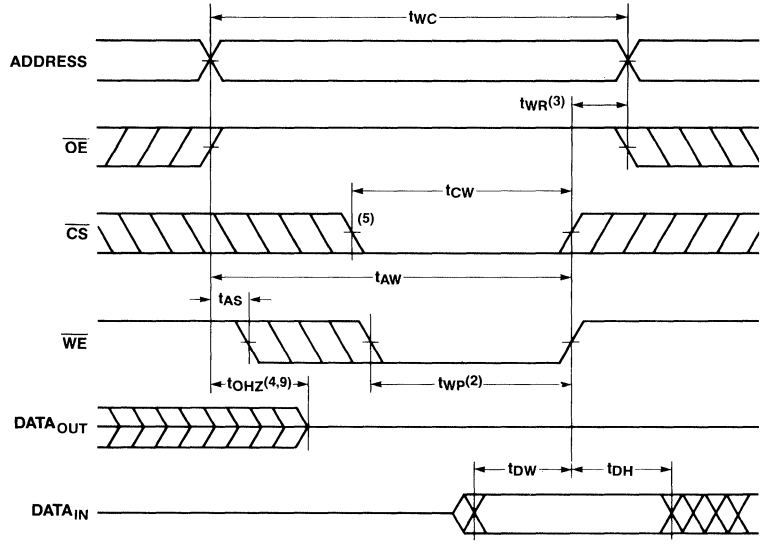
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SRD7198S/L-009

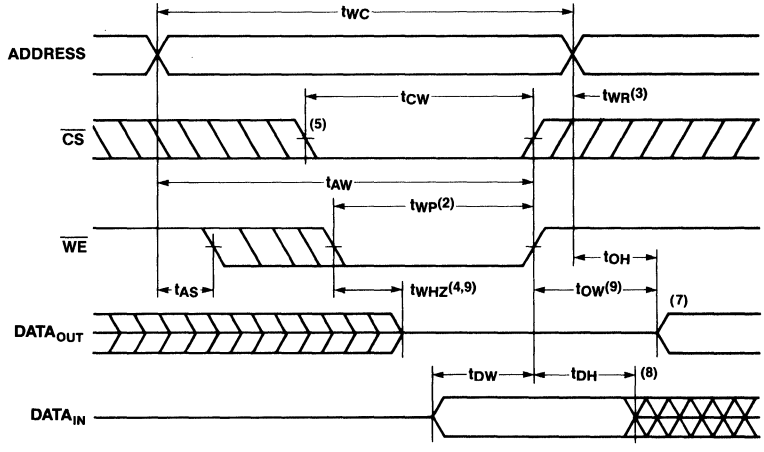
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



SRD7198S/L-010

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,6)



SRD7198S/L-011

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. DATA OUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

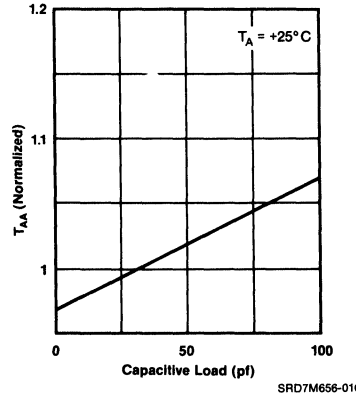
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	26	pF

NOTE:
1. This parameter is sampled and not 100% tested.

Address Access Time vs. Capacitive Load



SRD7M656-016

Integrated Device Technology, Inc.

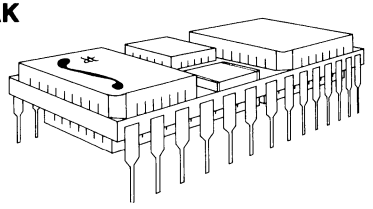
64K (8K x 8) CMOS STATIC RAMPAK

IDT7M864 IDT8M864

FEATURES:

- Equivalent to JEDEC standard 8K x 8 monolithic RAM
- 8,192 x 8 CMOS static RAM module complete with decoder and decoupling capacitor
- High-speed 65 (commercial only) 75/85/120/150/200ns (equal access and cycle times)
- Low power consumption, less than 1 watt maximum
- Two pinout options (64K EPROM & 64K static RAM)
- Utilizes IDT6116s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Military modules available with semiconductor components 100% screened to MIL-STD-883 Class B

64K RAMPAK



The IDT7M864/IDT8M864 are available with access times as fast as 65ns for commercial and 75ns for military temperature ranges, with maximum power consumption of only 990mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ high and/or CS_2 (7M864) goes low, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In the standby mode, the module consumes less than 440mW. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 20mW max.) and 2V data retention mode (less than 3mW max.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

Pinout of the IDT8M864 is equivalent to the 64K EPROMs (no connect on pin 26), ideal for applications requiring easy micro-code changes during prototyping. The IDT7M864's pinout is compatible with monolithic 64K static RAMs (CS_2 on pin 26).

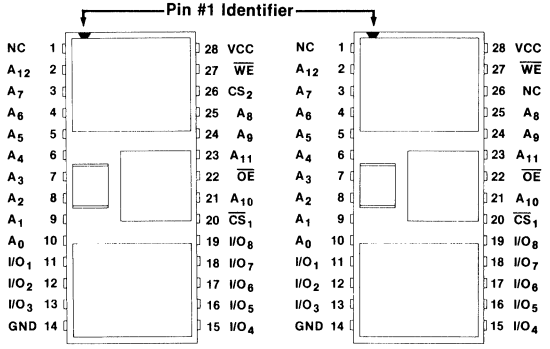
All inputs and outputs of the IDT7M864/IDT8M864 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT module semiconductor components are processed in compliance to the test methods of MIL-STD-883, as shown on back of data sheet, making them ideally, suited for applications demanding the highest level of performance and reliability.

DESCRIPTION:

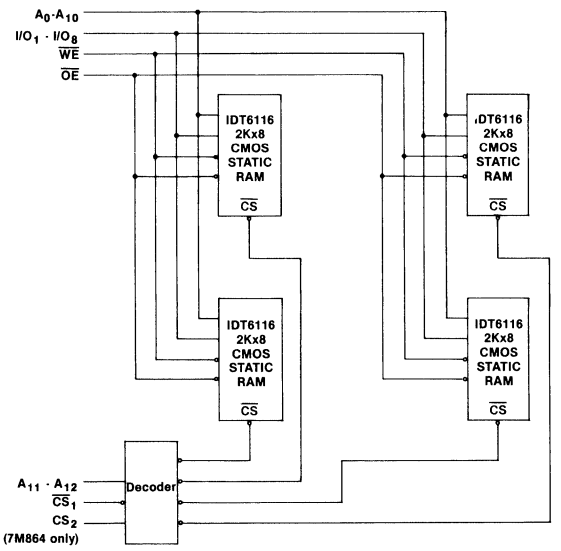
The IDT7M864/IDT8M864 are 64K (8,192 x 8 bit) high speed static RAMs constructed on a ceramic substrate using 4 IDT6116 (2,048 x 8) static RAMs in leadless chip carriers. Functional equivalence to a monolithic 64K static RAM is achieved by utilization of an on-board decoder circuit that interprets the higher order addresses A_{11} and A_{12} to select one of the four 2Kx8 RAMs. Extremely fast speeds can be achieved with this technique due to use of the IDT6116 fabricated in IDT's high performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

PIN CONFIGURATIONS



7M864 8M864

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1-I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

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TRUTH TABLE

MODE	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Read	L	H	L	H	D_{OUT}
Read	L	H	H	H	High Z
Write	L	H	X	L	D_{IN}

RECOMMENDED DC OPERATING CONDITIONS

(T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	.65	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

*V_{IL} min = −1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M864/8M864 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ or $\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC}	Operating Power Supply Current	$\overline{CS_1} \leq V_{IL}$, $CS_2 \geq V_{IH}$, Output Open	—	65	180	mA
I_{CC1}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	65	180	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$	—	20	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS_1} \geq V_{CC}-0.2V$, and/or $CS_2 \leq 0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $\leq 0.2V$	—	.016	3.6(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1mA	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{SB1} max at commercial temperature = 1.0 mA

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF (including scope and jig)

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

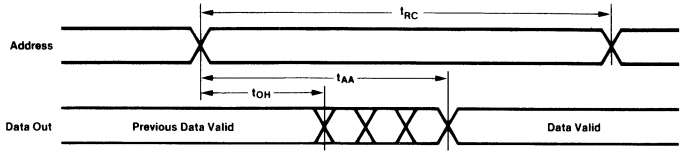
SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	28	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	33	pF

NOTE: This parameter is sampled and not 100% tested.

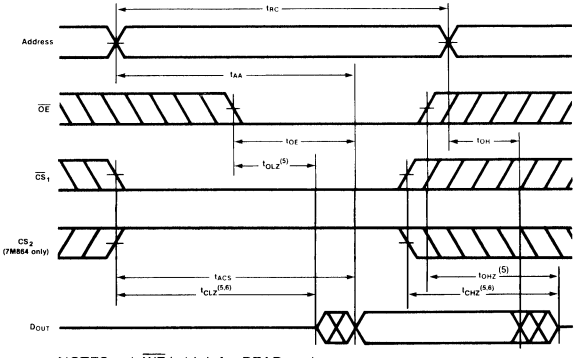
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M/8M864L65 COMMERCIAL ONLY		IDT7M/8M864L75		IDT7M/8M864L85		IDT7M/8M864L120		IDT7M/8M864L150		IDT7M/8M864L200		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	65	—	75	—	85	—	120	—	150	—	200	—	ns
t_{AA}	Address Access Time	—	65	—	75	—	85	—	120	—	150	—	200	ns
t_{ACS}	Chip Select Access Time	—	65	—	75	—	85	—	120	—	150	—	200	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	50	—	55	—	65	—	65	—	80	—	100	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CHZ}	Output Deselection to Output in High Z	—	40	—	50	—	55	—	70	—	70	—	80	ns
t_{OHZ}	Chip Disable to Output in High Z	—	30	—	35	—	40	—	40	—	40	—	50	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	0	—	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	65	—	75	—	85	—	120	—	150	—	200	—	ns
t_{CW}	Chip Selection to End of Write	55	—	65	—	65	—	80	—	100	—	120	—	ns
t_{AW}	Address Valid to End of Write	60	—	70	—	70	—	85	—	100	—	120	—	ns
t_{AS}	Address Setup Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	55	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	10	—	10	—	10	—	10	—	ns
t_{OHZ}	Output Disable to Output in High Z	—	30	—	35	—	40	—	40	—	40	—	50	ns
t_{WHZ}	Write to Output in High Z	0	35	0	40	0	50	0	50	0	60	0	60	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	5	—	ns

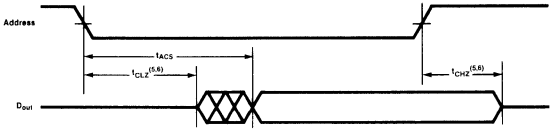
TIMING WAVEFORM OF READ CYCLE NO. 1 (1,2,4)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1,3)

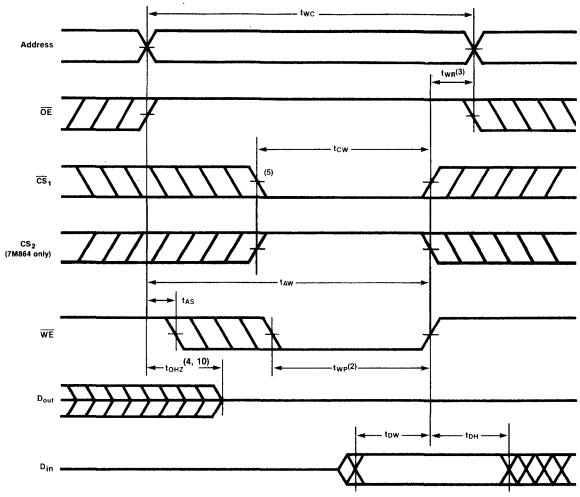


TIMING WAVEFORM OF READ CYCLE NO. 3 (1,3,4)

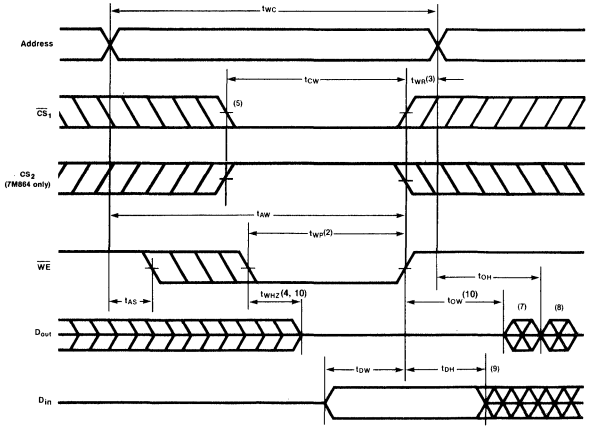


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected, $\overline{CS}_1$ = V_{IL}, CS_2 = V_{IH} (7M864 only).
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high (7M864 only).
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. For any given speed grade, operating voltage, and temperature, t_{CHZ} will be less than or equal to t_{CLZ}.

TIMING WAVEFORMS OF WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



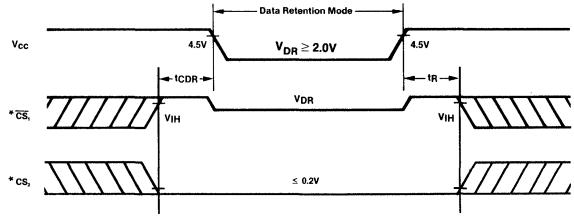
NOTES: 1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, or high CS_2 (7M864 only) and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low or CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.[1]	MAX. COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \leq 0.2V$	—	2.0[2]	350[2]	1200[2]	µA
		$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	4.0[3]	500[3]	1800[3]	
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}[4]	—	—	—	ns

NOTES: 1. T_A = 25°C 3. at V_{CC} = 3V
2. at V_{CC} = 2.0V 4. t_{RC} = Read Cycle Time

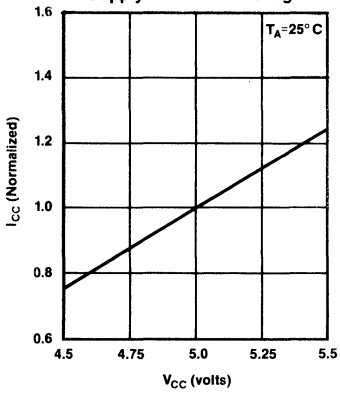
LOW V_{CC} DATA RETENTION WAVEFORM



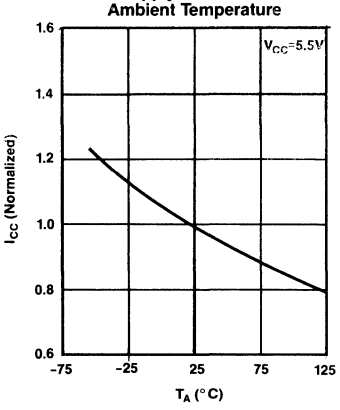
*Low V_{CC} data retention achieved by the indicated $\overline{CS_1}$ waveform or CS_2 waveform.

NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

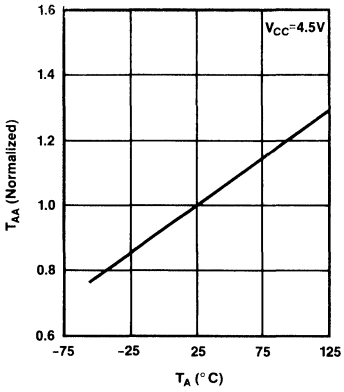
Supply Current vs. Voltage



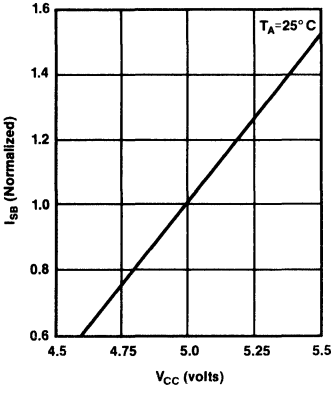
Supply Current vs. Ambient Temperature



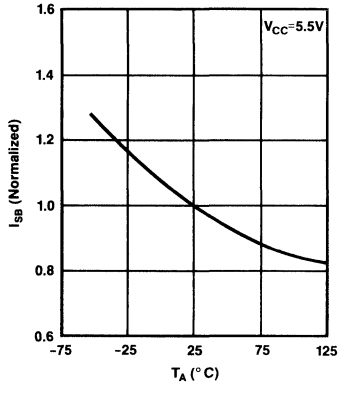
Address Access Time vs. Ambient Temperature



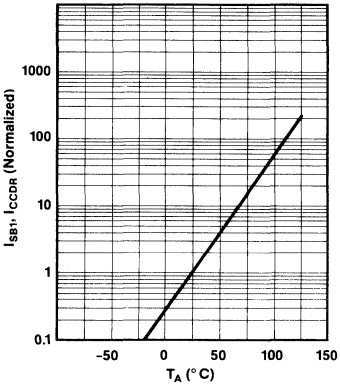
Stand-by Power Supply Current vs. Voltage



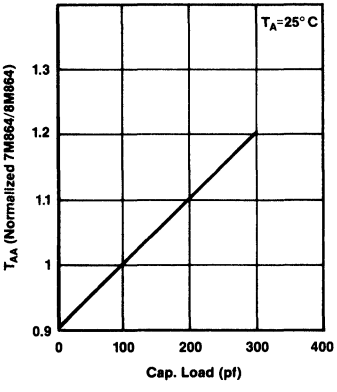
Stand-by Power Supply Current vs. Ambient Temperature



Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



Address Access Time vs. Capacitive Load



7

Integrated Device Technology, Inc.

CMOS STATIC RAM PLASTIC MODULE 1 MEGABIT (64K x 16-BIT) AND 512K (32K x 16-BIT)

ADVANCE INFORMATION
IDT8MP624S
IDT8MP612S

FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8MP624) with 32K x 16 option (IDT8MP612)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  —Allows flexibility in application
- Equivalent to JEDEC standard for future monolithic 64K x 8/32K x 16 static RAMs
- Fast access times
  —60ns (max.) over commercial temperature range
- Low-power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in both DIP and SIP (single in-line) packages for maximum space-saving flexibility
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

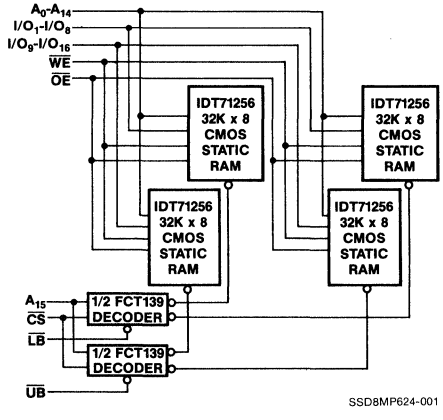
The IDT8MP624/IDT8MP612 are 1024K/512K high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs (IDT8MP624) or two IDT71256 static RAMs (IDT8MP612) in plastic surface-mount packages. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8MP612 32K x 16 option, A_{15} needs to be externally grounded for proper operation.) Extremely high speeds are achieved by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

The IDT8MP624/IDT8MP612 are available with access times as fast as 60ns over commercial temperature range, with maximum operating power consumption of only 1.7W (64K x 16 option). The module also offers a full standby mode of 110mW (max.).

The IDT8MP624/IDT8MP612 are offered in a 40-pin plastic SIP package, as well as a 40-pin DIP which conform to JEDEC standard pinouts.

All inputs and outputs of the IDT8MP824/IDT8MP612 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



SSD8MP624-001

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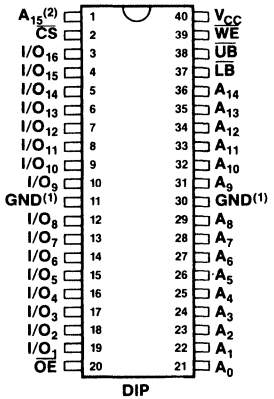
COMMERCIAL TEMPERATURE RANGE **JULY 1986**

Printed in U.S.A.

PIN CONFIGURATIONS

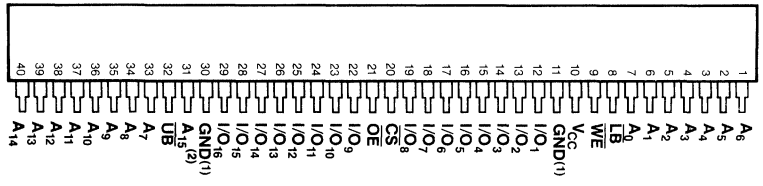


DIP
TOP VIEW

SSD8MP624-002

PIN NAMES

A_{0-15}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control



SIP
SIDE VIEW

SSD8MP624-003

NOTES:

1. Both GND pins need to be grounded for proper operation.
2. On IDT8MP612, 512K (32K x 16-bit) option, A_{15} (pin 1 — DIP; Pin 31 — SIP) requires external grounding for proper operation.

7

Integrated Device Technology, Inc.

CMOS STATIC RAM PLASTIC MODULES 256K (16K x 16-BIT) & 128K (8K x 16-BIT)

ADVANCE INFORMATION
IDT8MP656S
IDT8MP628S

FEATURES:

- High-density 256K/128K CMOS static RAM modules
- 16K x 16 organization (IDT8MP656) with 8K x 16 option (IDT8MP628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  —Flexibility in application
- Equivalent to JEDEC standard for future monolithic 16K x 16/8K x 16 static RAMs
- Fast access times
  —50ns (max.) over commercial temperature range
- Low-power consumption
  —Active: less than 1W (typ. in 16K x 16 organization)
  —Standby: less than 1mW (typ.)
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in both DIP and SIP (single in-line) packages for maximum space-saving flexibility
- Utilizes IDT7164s — high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

DESCRIPTION:

The IDT8MP656/IDT8MP628 are 265K/128K-bit high-speed CMOS static RAMs constructed on an epoxy laminate substrate using four IDT7164 8K x 8 static RAMs (IDT8MP656) or two IDT7164 static RAMs (IDT8MP628) in plastic surface mount packages.

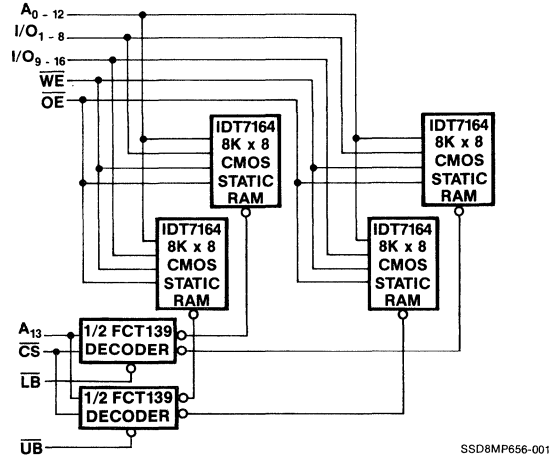
Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On IDT8MP628 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s, fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

The IDT8MP656/IDT8MP628 are available with access times as fast as 50ns over the commercial temperature range, with maximum operating power consumption of only 1.8W (IDT8MP656 16K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8MP656/IDT8MP628 are offered in both a 40-pin plastic SIP, as well as a 40-pin plastic DIP which conform to JEDEC standard pinouts for future monolithic devices.

All inputs and outputs of the IDT8MP656/IDT8MP628 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous ciruitry is used requiring no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



SSD8MP656-001

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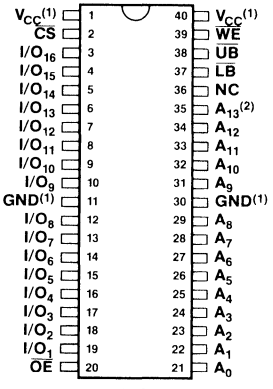
PIN CONFIGURATIONS

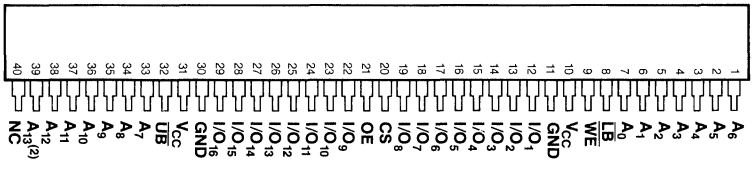


DIP
TOP VIEW

SSD8MP656-002

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground



SIP
SIDE VIEW

SSD8MP656-003

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. A_{13} (pin 39 - SIP; pin 35 - DIP) requires external grounding for IDT8MP628 128K (8K x 16-Bit) option.

7

Integrated Device Technology, Inc.

1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM PLASTIC MODULE

ADVANCE INFORMATION
IDT8MP824S

FEATURES:

- High-density 1024K (128K x 8) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 128K x 8 static RAMs
- Fast access times
  —60ns (max.) over commercial temperature range
- Low-power consumption
  —Active: less than 500mW (typ.)
  —Standby: less than 150μW (typ.)
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Cost-effective plastic surface-mounted RAM packages on an epoxy laminate (FR4) substrate
- Offered in both DIP and SIP (single in-line) packages for maximum space-saving flexibility
- Utilizes IDT71256s — high-performance 256K static RAMs produced with advanced CEMOS technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible

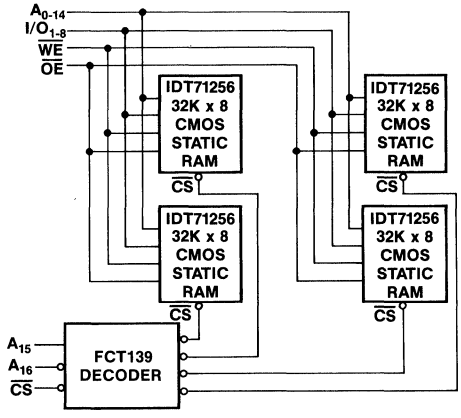
DESCRIPTION:

The IDT8MP824 is a 1024K (131,072 x 8-bit) high-speed static RAM constructed on an epoxy laminate substrate using four IDT71256 32K x 8 static RAMs in plastic surface mount packages. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order addresses A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability technology, CEMOS.

The IDT8MP824 is available with maximum access times as fast as 60ns for commercial range, with maximum power consumption of 1.0 watts. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode with maximum power consumption of only 85mW.

The IDT8MP824 is offered in a 30-pin SIP (single in-line) package, as well as a 32-pin DIP which conform to JEDEC standard pinouts for future monolithic devices.

All inputs and outputs of the IDT8MP824 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.



SSD8MP824-001

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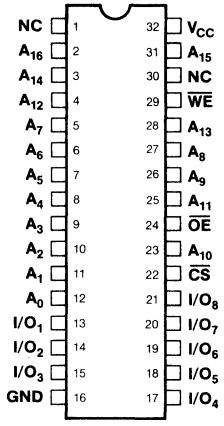
PIN CONFIGURATIONS

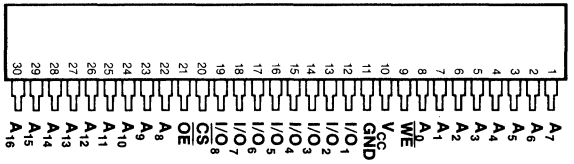


DIP
TOP VIEW

SSD8MP824-002

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground



SIP SIDE VIEW

SSD8MP824-003

7

Integrated Device Technology, Inc.

1 MEGABIT (64K x 16-BIT) & 512K (32K x 16-BIT) CMOS STATIC RAM MODULE

ADVANCE INFORMATION
IDT8M624
IDT8M612

FEATURES:

- High-density 1024K/512K-bit CMOS static RAM module
- 64K x 16 organization (IDT8M624) with 32K x 16 option (IDT8M612)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  —allows flexibility in application
- Equivalent to JEDEC standard for future monolithic 64K x 16/ 32K x 16 static RAMs
- High-speed — 60ns (max.) commercial; 75ns (max.) military
- Low-power consumption
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT8M624/IDT8M612 are 1024K/512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four IDT71256 32K x 8 static RAMs (IDT8M624) or two IDT71256 static RAMs (IDT8M612) in leadless chip carriers. Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{15} to select one of the two 32K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On the IDT8M612 32K x 16 option, A_{15} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT71256s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 1024K/512K static RAMs available.

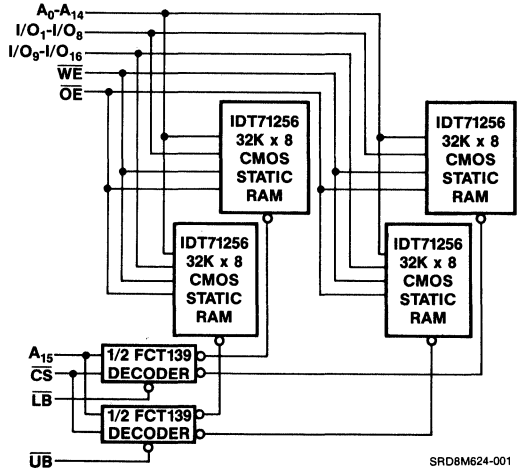
The IDT8M624/IDT8M612 are available with access times as fast as 60ns commercial and 75ns military temperature range, with maximum operating power consumption of only 1.7W (max. —IDT8M624 64K x 16 option). The module also offers a full standby mode of 110mW (max.).

The IDT8M624/IDT8M612 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT71256s in leadless chip carriers.

All inputs and outputs of the IDT8M624/IDT8M612 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, as well as being qualified to requirements patterned after Methods 5004 and 5005, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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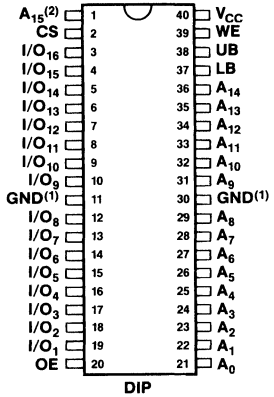
PIN CONFIGURATION



DIP
TOP VIEW

SRD8M624-002

PIN NAMES

A_{0-15}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground
$\overline{OE}$	Output Enable
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:

1. Both GND pins need to be grounded for proper operation.
2. On IDT8M612, 512K (32K x 16-bit) option, A_{15} (pin 1) requires external grounding for proper operation.

7

Integrated Device Technology, Inc.

CMOS STATIC RAM MODULE 256K (16K x 16-BIT) & 128K (8K x 16-BIT)

PRELIMINARY
IDT8M656S
IDT8M628S

FEATURES:

- High-density 256K/128K-bit CMOS static RAM modules
- 16K x 16 organization (IDT8M656) with 8K x 16 option (IDT8M628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  — Flexibility in application
- Equivalent to JEDEC standard for future monolithic 16K x 16/8K x 16 static RAMs
- High-speed
  — Military — 60ns (max.)
  — Commercial — 50ns (max.)
- Low-power consumption: typically less than 1W operating (IDT8M656), less than 1mW in standby
- Utilizes IDT7164s — high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT8M656/IDT8M628 are 265K/128K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four IDT7164 8K x 8 static RAMs (IDT8M656) or two IDT7164 static RAMs (IDT8M628) in leadless chip carriers.

Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On IDT8M628 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

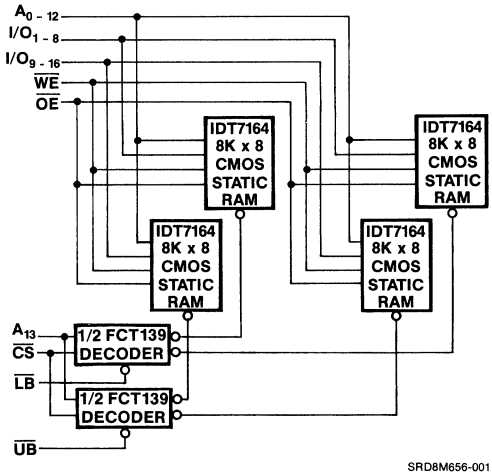
The IDT8M656/IDT8M628 are available with access times as fast as 50ns commercial and 60ns military temperature range, with maximum operating power consumption of only 1.8W (IDT8M656, 16K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8M656/IDT8M628 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7164s in leadless chip carriers.

All inputs and outputs of the IDT8M656/IDT8M628 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous ciruitry is used requiring no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



SRD8M656-001

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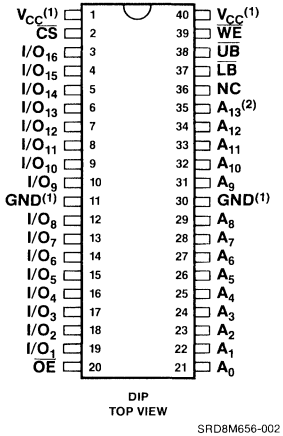
PIN CONFIGURATION



DIP
TOP VIEW

SRD8M656-002

PIN NAMES

A_{0-13}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On IDT8M628, 128K (8K x 16-Bit) option, A_{13} (Pin 35) is required external grounding for proper operation.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +155	°C
P_T	Power Dissipation	4.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} (min) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} = -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8M656S			IDT8M628S			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current in X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f Max.	—	165	330	—	150	300	mA
I_{CCX8}	Operating Current in X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f Max.	—	100	200	—	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	4	80(2)	—	2	40(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

NOTE:

1. V_{CC} = 5V, T_A = +25°C
2. I_{SB} and I_{SB1} of IDT8M656/IDT8M628 at commercial temperature = 60mA/30mA.

7

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1 & 2

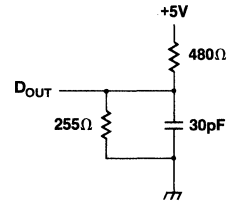


Figure 1. Output Load

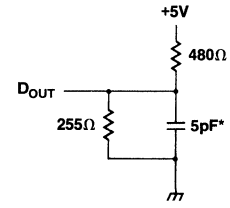


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

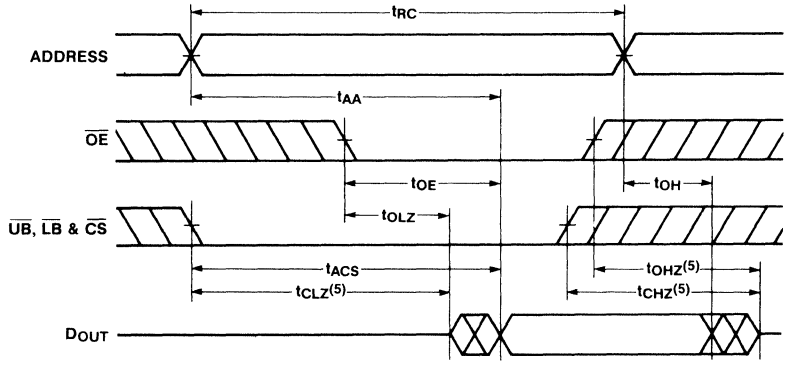
SRD8M656-003

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT8M656S50 IDT8M729S50 COM'L. ONLY		IDT8M656S60 IDT8M628S60		IDT8M656S70 IDT8M628S70		IDT8M656S85 IDT8M628S85		IDT8M656S100 IDT8M628S100 MIL. ONLY		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	50	—	60	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	50	—	60	—	70	—	85	—	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Setup Time	5	—	10	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	55	—	65	—	80	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

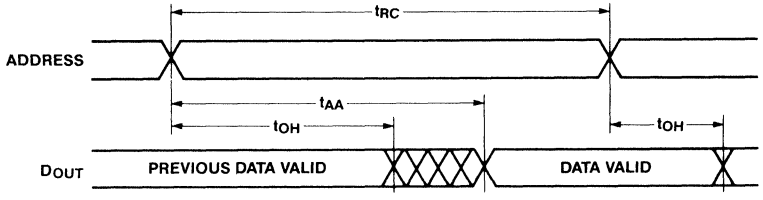
NOTES:
1. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



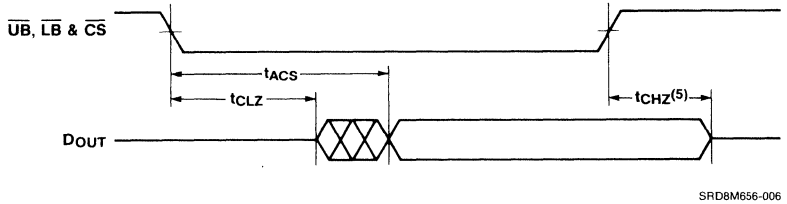
SRD8M656-004

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD8M656-005

TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

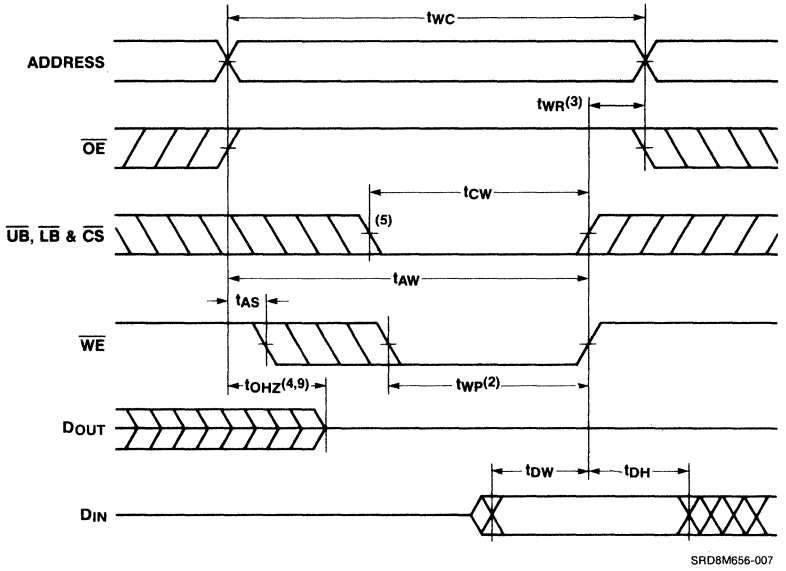


SRD8M656-006

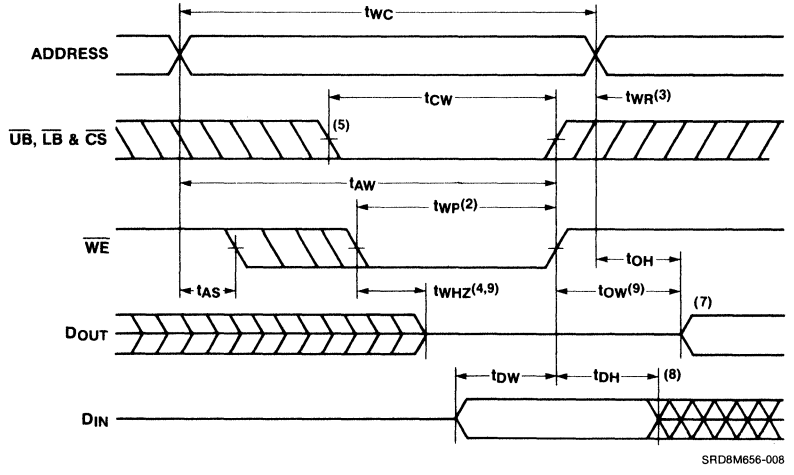
NOTES:

1. WE is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ or $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

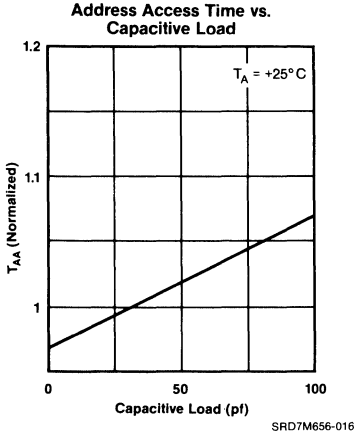
TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	TBD	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	TBD	pF

NOTE:
1. This parameter is sampled and not 100% tested.



Integrated Device Technology, Inc.

1 MEGABIT (128K x 8-BIT) CMOS STATIC RAM MODULE

ADVANCE INFORMATION
IDT8M824

FEATURES:

- High-density 1024K-bit (128K x 8) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 128K x 8 static RAMs
- High-speed — 60ns (max.) commercial; 75ns (max.) military
- Low-power consumption; typically less than 500mW operating, less than 150μW in standby
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 32-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT8M824 is a 1024K (131,072 x 8) bit high-speed static RAM constructed on a co-fired ceramic substrate using four IDT71256 32K x 8 static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic one megabit static RAMs is achieved by utilization of an on-board decoder that interprets the higher order addresses A_{15} and A_{16} to select one of the four 32K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 256K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability technology, CEMOS.

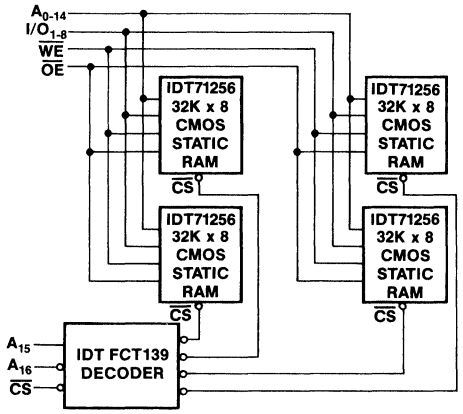
The IDT8M824 is available with maximum access times as fast as 60ns for commercial and 75ns for military temperature ranges, with maximum power consumption of 1.0 watts. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to a substantially lower power mode with maximum power consumption of only 85mW.

The IDT8M824 is offered in a 32-pin, 600 mil center sidebraze DIP, adhering to JEDEC standards for one megabit monolithic pinouts, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT8M824 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, as well as being qualified to requirements patterned after Methods 5004 and 5005, making them ideally suited to applications demanding the highest level of performance and reliability.

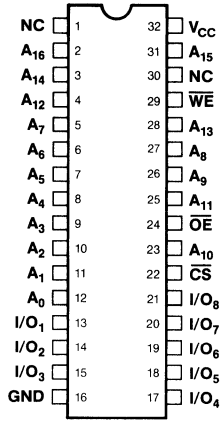
FUNCTIONAL BLOCK DIAGRAM



SRD8M824-001

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP
TOP VIEW

SRD8M824-002

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground

Integrated Device Technology, Inc.

256K (32K x 8-BIT) CMOS STATIC RAM MODULE (Low-Power Version)

PRELIMINARY IDT8M856L

FEATURES:

- High-density 256K (32K x 8) bit CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed — 45ns (max.) commercial; 55ns (max.) military
- Low-power consumption; typically less than 400mW operating, less than 500μW in full standby
- Utilizes IDT7164s — high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT8M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7164 (8192 x 8) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address A_{13} and A_{14} to select one of the four 8K x 8 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

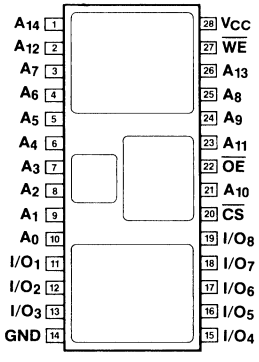
The IDT8M856 is available with maximum access times as fast as 45ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 880mW. The circuit also offers a substantially low-power standby mode. When $\overline{CS}$ goes high, the ciruit will automatically go to a standby mode with power consumption of only 83mW (max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT8M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



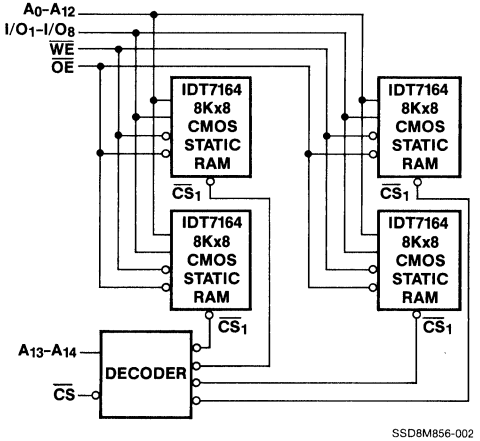
DIP
TOP VIEW

SSD8M856-001

PIN NAMES

A_0 - A_{14}	ADDRESSES
I/O_1 - I/O_8	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



SSD8M856-002

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Printed in U.S.A.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IL}, Output Open, f = 0	—	80	160	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IL}, Output Open, f = f Max.	—	80	160	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	8	15	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V (CMOS Level) V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.1	12.0(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V I_{OL} = 8mA, V_{CC} = 4.5V	— —	— —	0.5 0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = 4.5V	2.4	—	—	V

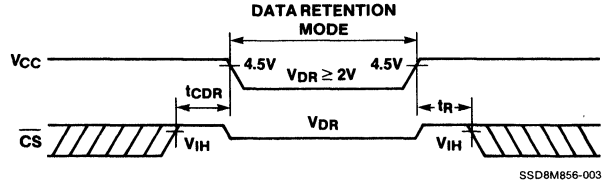
NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB1} at commercial temperature = 5mA.

DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	COM'L MAX.	MIL MAX.	UNIT
V_{DR}	V_{CC} for Retention Data		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≤ V_{CC} - 0.2V or ≥ 0.2V	— —	6.0(2) 12.0(3)	1000(2) 1500(3)	4000(2) 6000(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES:
1. T_A =25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



SSD8M856-003

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

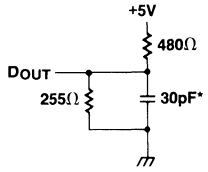


Figure 1. Output Load

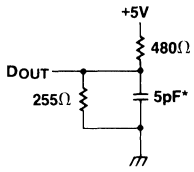


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

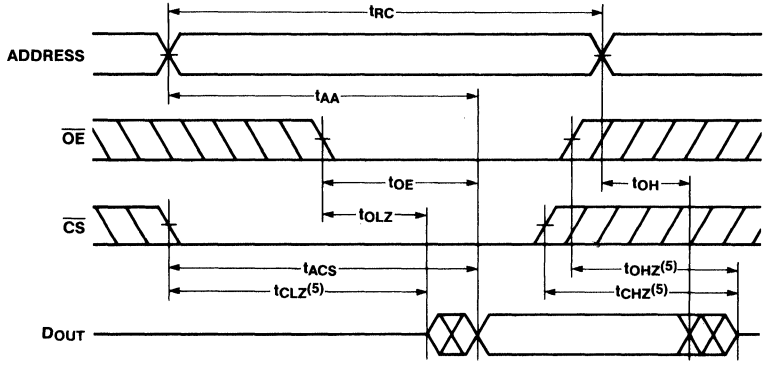
SYMBOL	PARAMETER	IDT8M856L45 MIN.	IDT8M856L45 MAX.	IDT8M856L50 MIN.	IDT8M856L50 MAX.	IDT8M856L60 MIN.	IDT8M856L60 MAX.	IDT8M856L70 MIN.	IDT8M856L70 MAX.	IDT8M856L85 MIN.	IDT8M856L85 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	45	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	45	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	45	—	50	—	55	—	65	—	85	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	35	—	40	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	20	—	20	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	20	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	45	—	50	—	60	—	70	—	85	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	45	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	40	—	45	—	50	—	60	—	70	—	ns
t_{AW}	Address Valid to End or Write	40	—	45	—	50	—	60	—	70	—	ns
t_{AS}	Address Setup Time	5	—	5	—	10	—	10	—	15	—	ns
t_{WP}	Write Pulse Width	35	—	35	—	40	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	20	—	20	—	25	—	30	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

7

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

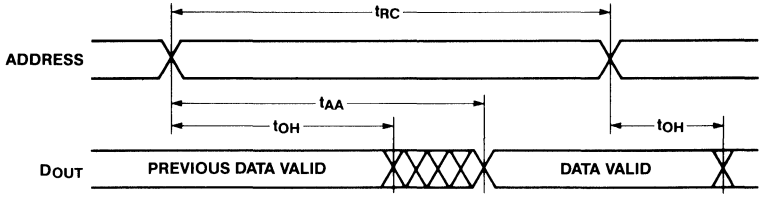
SYMBOL	PARAMETER	IDT8M856L55 MIN.	IDT8M856L55 MAX.	IDT8M856L65 MIN.	IDT8M856L65 MAX.	IDT8M856L75 MIN.	IDT8M856L75 MAX.	IDT8M856L90 MIN.	IDT8M856L90 MAX.	IDT8M856L100 MIN.	IDT8M856L100 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	75	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	55	—	65	—	80	—	90	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	50	—	60	—	65	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	55	—	65	—	75	—	90	—	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AW}	Address Valid to End or Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AS}	Address Setup Time	5	—	10	—	10	—	15	—	15	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	25	—	30	—	40	—	50	—	50	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	35	—	45	—	45	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



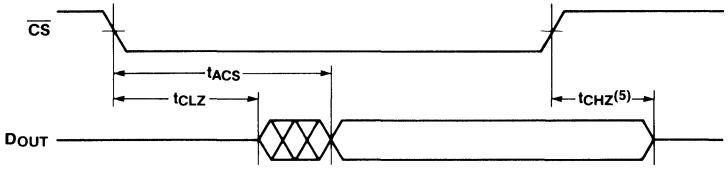
SSD8M856-004

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD7198S/L-008

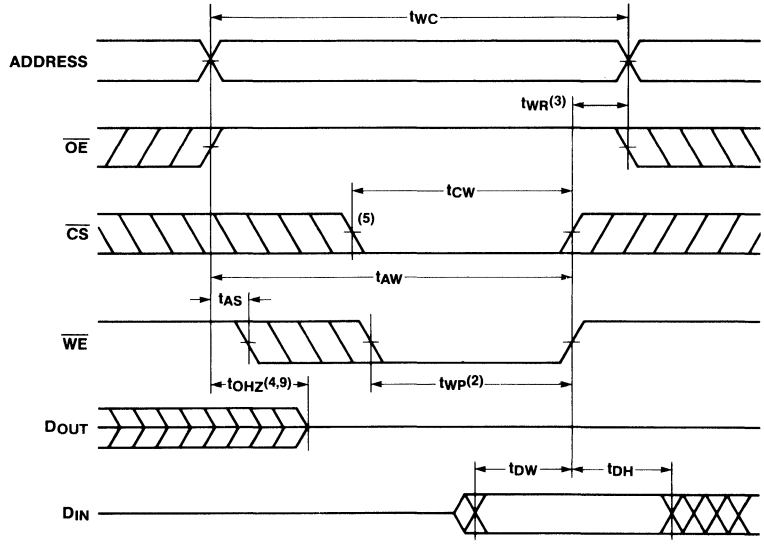
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SRD7198S/L-009

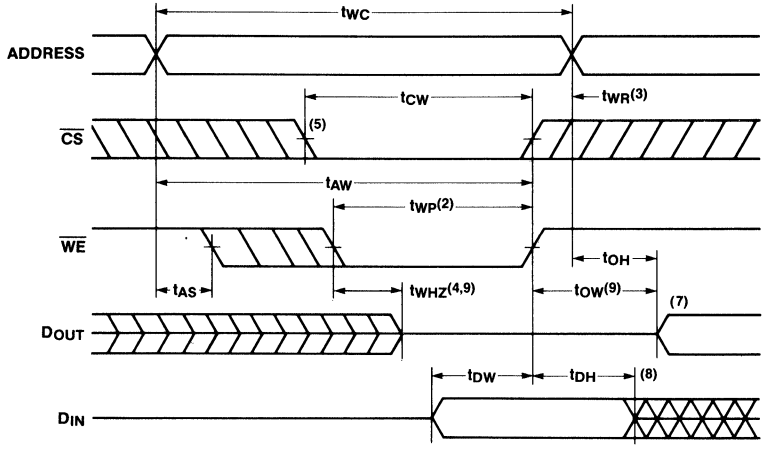
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



SRD7198S/L-010

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



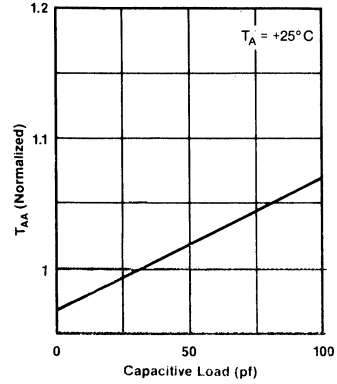
SRD7198S/L-011

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

Address Access Time vs. Capacitive Load



SRD7M656-016

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	26	pF

NOTE:
1. This parameter is sampled and not 100% tested.

Integrated Device Technology, Inc

Subsytems Modules Ordering Information

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7MP624S	Consult Factory			
IDT7M134S70C	70	380	D58	Com'l.
IDT7M134S90C	90			
IDT7M134S90CB				Mil.
IDT7M134S100C	100	380	D58	Com'l.
IDT7M134S100CB				Mil.
IDT7M134S120C	120	380	D58	Com'l.
IDT7M135S120CB				Mil.
IDT7M134S140CB	140	380	D58	Mil.
IDT7M135S70C	70	640	D58	Com'l.
IDT7M135S90C	90	640	D58	Com'l.
IDT7M135S90CB				Mil.
IDT7M135S100C	100	640	D58	Com'l.
IDT7M135S100CB				Mil.
IDT7M135S120C	120	640	D58	Com'l.
IDT7M135S120CB				Mil.
IDT7M135S140CB	140	640	D58	Mil.
IDT7M136	Consult Factory			
IDT7M137	Consult Factory			
IDT7M144S70C	70	380	D58	Com'l.
IDT7M144S90C	90	380	D58	Com'l.
IDT7M144S90CB				Mil.
IDT7M144S100C	100	380	D58	Com'l.
IDT7M144S100CB				Mil.
IDT7M144S120C	120	380	D58	Com'l.
IDT7M144S120CB				Mil.
IDT7M144S140CB	140	380	D58	Mil.
IDT7M145S70C	70	640	D58	Com'l.
IDT7M145S90C	90	640	D58	Com'l.
IDT7M145S90CB				Mil.
IDT7M145S100C	100	640	D58	Com'l.
IDT7M145S100CB				Mil.
IDT7M145S120C	120	640	D58	Com'l.
IDT7M145S120CB				Mil.
IDT7M145S140CB	140	640	D58	Mil.
IDT7M203S40C	40	176	D28-1	Com'l.
IDT7M203S50C	50	176	D28-1	Com'l.
IDT7M203S50CB		230		Mil.

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7M203S55C	55	176	D28-1	Com'l.
IDT7M203S55CB		230		Mil.
IDT7M203S65C	65	176	D28-1	Com'l.
IDT7M203S65CB		230		Mil.
IDT7M203S100C	100	176	D28-1	Com'l.
IDT7M203S100CB		230		Mil.
IDT7M203S140C	140	176	D28-1	Com'l.
IDT7M203S140CB		230		Mil.
IDT7M204S40C	40	176	D28-1	Com'l.
IDT7M204S50C	50	176	D28-1	Com'l.
IDT7M204S50CB		230		Mil.
IDT7M204S55C	55	176	D28-1	Com'l.
IDT7M204S55CB		230		Mil.
IDT7M204S65C	65	176	D28-1	Com'l.
IDT7M204S65CB		230		Mil.
IDT7M204S100C	100	176	D28-1	Com'l.
IDT7M204S100CB		230		Mil.
IDT7M204S140C	140	176	D28-1	Com'l.
IDT7M204S140CB		230		Mil.
IDT7M205	Consult Factory			
IDT7M206	Consult Factory			
IDT7M624S30C	30	x4 = 1100	D40-1	Com'l.
		x8 = 1380		
		x16 = 1950		
IDT7M624S45C	45	x4 = 1100	D40-1	Com'l.
		x8 = 1380		
		x16 = 1950		
IDT7M624S45CB		x4 = 1100		Mil.
		x8 = 1380		
		x16 = 1950		
IDT7M624S55C	55	x4 = 1100	D40-1	Com'l.
		x8 = 1380		
		x16 = 1950		
IDT7M624S55CB		x4 = 1100		Mil.
		x8 = 1380		
		x16 = 1950		
IDT7M624S65C	65	x4 = 1100	D40-1	Com'l.
		x8 = 1380		
		x16 = 1950		

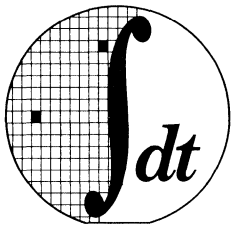
7

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7M624S65CB	65	x4 = 1100	D40-1	Mil.
		x8 = 1380		
		x16 = 1950		
IDT7M624S85C	85	x4 = 1100	D40-1	Com'l.
		x8 = 1380		
		x16 = 1950		
IDT7M624S85CB		x4 = 1100		Mil.
		x8 = 1380		
		x16 = 1950		
IDT7M656L25C	25	x4 = 620	D40-1	Com'l.
		x8 = 840		
		x16 = 1280		
IDT7M656L35C	35	x4 = 620	D40-1	Com'l.
		x8 = 840		
		x16 = 1280		
IDT7M656L35CB		x4 = 620		Mil.
		x8 = 840		
		x16 = 1280		
IDT7M656L55C	55	x4 = 620	D40-1	Com'l.
		x8 = 840		
		x16 = 1280		
IDT7M656L55CB		x4 = 620		Mil.
		x8 = 840		
		x16 = 1280		
IDT7M656L85C	85	x4 = 620	D40-1	Com'l.
		x8 = 840		
		x16 = 1280		
IDT7M656L85CB		x4 = 620		Mil.
		x8 = 840		
		x16 = 1280		
IDT7M656L100CB	100	x4 = 620	D40-1	Mil.
		x8 = 840		
		x16 = 1280		
IDT7M812S45C	45	960	D40-1	Com'l.
IDT7M812S55C	55	960	D40-1	Com'l.
IDT7M812S55CB				Mil.
IDT7M812S65C	65	960	D40-1	Com'l.
IDT7M812S65CB				Mil.
IDT7M812S85C	85	960	D40-1	Com'l.
IDT7M812S85CB				Mil.
IDT7M812S100CB	100	960	D40-1	Mil.
IDT7M824S	Consult Factory			
IDT7M856S40C	40	380	D28-3	Com'l.
IDT7M856S50C	50	380	D28-3	Com'l.

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT7M856S55CB	55	380	D28-3	Mil.
IDT7M856S60C	60	380	D28-3	Com'l.
IDT7M856S65CB	65	380	D28-3	Mil.
IDT7M856S70C	70	380	D28-3	Com'l.
IDT7M856S75CB	75	380	D28-3	Mil.
IDT7M856S85C	85	380	D28-3	Com'l.
IDT7M856S90CB	90	380	D28-3	Mil.
IDT7M856S100CB	100	380	D28-3	Mil.
IDT7M864L65C	65	180	D28-3	Com'l.
IDT7M864L75C	75	180	D28-3	Com'l.
IDT7M864L75CB				Mil.
IDT7M864L85C	85	180	D28-3	Com'l.
IDT7M864L85CB				Mil.
IDT7M864L120C	120	180	D28-3	Com'l.
IDT7M864L120CB				Mil.
IDT7M864L150C	150	180	D28-3	Com'l.
IDT7M864L150CB				Mil.
IDT7M864L200C	200	180	D28-3	Com'l.
IDT7M864L200CB				Mil.
IDT7M912S45C	45	1080	D40-1	Com'l.
IDT7M912S55C	55	1080	D40-1	Com'l.
IDT7M912S55CB				Mil.
IDT7M912S65C	65	1080	D40-1	Com'l.
IDT7M912S65CB				Mil.
IDT7M912S85C	85	1080	D40-1	Com'l.
IDT7M912S85CB				Mil.
IDT7M912S100CB	100	1080	D40-1	Mil.
IDT8MP612S	Consult Factory			
IDT8MP624S	Consult Factory			
IDT8MP628S	Consult Factory			
IDT8MP656S	Consult Factory			
IDT8MP824S	Consult Factory			
IDT8M612S	Consult Factory			
IDT8M624S	Consult Factory			
IDT8M628S50C	50	x8 = 170	D40-1	Com'l.
		x16 = 300		
IDT8M628S60C	60	x8 = 170	D40-1	Com'l.
		x16 = 300		
IDT8M628S60CB		x8 = 170		Mil.
		x16 = 300		

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT8M628S70C	70	x8 = 170	D40-1	Com'l.
		x16 = 300		
IDT8M628S70CB		x8 = 170		Mil.
		x16 = 300		
IDT8M628S85C	85	x8 = 170	D40-1	Com'l.
		x16 = 300		
IDT8M628S85CB		x8 = 170		Mil.
		x16 = 300		
IDT8M628S100CB	100	x8 = 170	D40-1	Mil.
		x16 = 300		
IDT8M656S50C	50	x8 = 200	D40-1	Com'l.
		x16 = 330		
IDT8M656S60C	60	x8 = 200	D40-1	Com'l.
		x16 = 330		
IDT8M656S60CB		x8 = 200		Mil.
		x16 = 330		
IDT8M656S70C	70	x8 = 200	D40-1	Com'l.
		x16 = 330		
IDT8M656S70CB		x8 = 200		Mil.
		x16 = 330		
IDT8M656S85C	85	x8 = 200	D40-1	Com'l.
		x16 = 330		
IDT8M656S85CB		x8 = 200		Mil.
		x16 = 330		
IDT8M656S100CB	100	x8 = 200	D40-1	Mil.
		x16 = 330		
IDT8M824S	Consult Factory			

ORDER PART NUMBER	SPEED (ns)	I_{CC} (MAX.) (mA)	PACKAGE TYPE	OPER. TEMP.
IDT8M856L45C	45	160	D28-3	Com'l.
IDT8M856L50C	50	160	D28-3	Com'l.
IDT8M856L55CB	55	160	D28-3	Mil.
IDT8M856L60C	60	160	D28-3	Com'l.
IDT8M856L65CB	65	160	D28-3	Mil.
IDT8M856L70C	70	160	D28-3	Com'l.
IDT8M856L75CB	75	160	D28-3	Mil.
IDT8M856L85C	85	160	D28-3	Com'l.
IDT8M856L90CB	90	160	D28-3	Mil.
IDT8M856L100CB	100	160	D28-3	Mil.
IDT8M864L65C	65	180	D28-3	Com'l.
IDT8M864L75C	75	180	D28-3	Com'l.
IDT8M864L75CB				Mil.
IDT8M864L85C	85	180	D28-3	Com'l.
IDT8M864L85CB				Mil.
IDT8M864L120C	120	180	D28-3	Com'l.
IDT8M864L120CB				Mil.
IDT8M864L150C	150	180	D28-3	Com'l.
IDT8M864L150CB				Mil.
IDT8M864L200C	200	180	D28-3	Com'l.
IDT8M864L200CB				Mil.



Integrated
Device
Technology

General Product Information

8

GENERAL PRODUCT INFORMATION
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General Product Information

Integrated Device Technology, Inc.

UNDERSTANDING THE IDT7201/7202 FIFO

APPLICATION NOTE AN-01

By Michael J. Miller

INTRODUCTION

This article discusses several different types of FIFO queues, their implementation, their performance and their use. Data, or information in computers, is processed as words or bytes in a predominantly serial fashion. There are producers and consumers of information that are connected by busses. Often there is a mismatch in the rate at which data is produced and the rate at which it can be accepted. The data is therefore buffered in serial lists until it can be used. The serial lists are stored in memory and require overhead to maintain them. These First-In-First-Out (FIFO) structures can be implemented at many levels from all software to all hardware. The software implementations are often the most flexible but yield the lowest performance. The hardware implementations, while less flexible, give the highest performance.

QUEUES

The elements of any computer or controller can be divided into three categories in relation to information: transformation, storage and transfer. Logic gates transform and combine information, memory elements store information and wires transfer information between the other elements.

Memory can be viewed as an element which transfers information with respect to time. The simplest of memory elements are latches and registers. RAMs are dense arrays of latches. While RAMs allow for dense information storage, they require an address to access individual pieces of information in the array. Therefore, addresses (information) must be generated and stored in order to access the desired information. The addresses are stored in programs and data structures such as linked lists.

Queues are a special organization of dense arrays of latches. Queues are a linear organization of groups of latches. Access to the linear string is restricted to either end. While RAMs allow for random access of any data in the array at any point in time, they require address inputs. Queues on the other hand, don't have an address thus avoiding the address generation and storage overhead. Queues can be divided into two categories: FIFOs and LIFOs.

Queues can be observed in the world about us. FIFO is an acronym for "First-In-First-Out". They can be observed in a bank line-up where customers enter at the end of a line and, after some wait, are serviced at the other end. The FIFO queue provides a mechanism by which customers, which arrive at an erratic rate, can wait until a teller can accommodate them.

LIFO is an acronym for "Last-In-First-Out". We can observe this phenomenon in the work place. As a person is working at a desk, interrupts occur. A higher priority interrupt such as a phone call or a request from people higher in management will cause the person to drop the work on the desk and start a new task. When the higher priority task is accomplished, the interrupted task on the desk is resumed. Depending on how many interrupts of sequentially higher priority tasks come in during the day, the stack of tasks on the desk grows. Another time honored example is the stacks of trays at the cafeteria. As trays are washed they are placed on a spring loaded elevator which sinks down to accommodate the new trays. When new customers enter the food line, trays are removed from the stack.

As can be seen in the above examples, queues are used to buffer between the flows of consumers and distributors of services. Groups of computing elements can be divided into consumers and producers of information with rates that must be matched. For example, a rotating Winchester disk is a source of information that must be serviced at a rate that may not be easily matched by the CPU which is consuming the information through the use of a data bus.

SIMPLE FIFO

The implementation of FIFOs is varied and presents many trade-offs. The simplest design treats the FIFO as a fixed number of memory elements in a linear array. When data is written (pushed) in at one end, all of the rest of the elements shift their data over to their neighbor at the same time. One can visualize (Figure 1) the structure as a shift register. The same structure can be implemented in software where the program manages an array of memory locations in RAM. To push data into the queue the program must first start by moving the contents of the next to the last location into the last location. The algorithm continues from the last to the first location. When all of the data has been rippled down, the first location in the queue will be vacated. The data to be pushed into the queue is written into that vacated location.

An improvement in the software solution could be made with the introduction of a pointer. A pointer is a variable which contains an address. The pointer would identify a location from which to read the output of the FIFO. When a new piece of

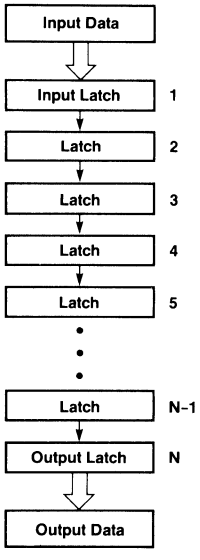

Figure 1. Hardware implementation of a fixed length FIFO.

Printed in U.S.A.

information is written, it would go into the location identified by the pointer after which the pointer would be incremented. The pointer now points at the new output data. When the pointer reaches the end of the array, the next increment would be replaced by setting the pointer to the beginning of the array. The obvious advantage is that the program does less work and therefore is faster. This software technique is called a circular queue with one pointer. (See Figure 2.)

FIXED LENGTH FIFO: NO FALL-THROUGH

The FIFO described previously is called a Fixed Length FIFO and has the characteristic that it takes N cycles for a piece of information that was placed into it to emerge out of it. The number N is the number of locations in the FIFO. This implementation also has the characteristic that, when first started after power up, it will produce unknown data for N cycles until the first valid data arrives at the output. The latency is therefore N read/write cycles. The fixed length FIFO does not allow for differences between the rate of input and output rates. This type of FIFO is used where the arrival of data at the output is delayed to match parallel paths in a pipelined system.

VARIABLE LENGTH FIFO

The variable length FIFO solves the rate mismatch problem but requires more overhead to implement. Where the fixed length FIFO is like a steel pipe which information is fed through and has a fixed number of locations, the variable length FIFO is like a rubber hose that can stretch, holding from one to many items. The items are removed at will instead of being required to at write time. Every variable length system has a limit and therefore must signal when it is at capacity and must be serviced before bursting.

FALL-THROUGH FIFOs

In the real world of silicon and aluminum there is no such thing as rubber. Variable length FIFOs must therefore be implemented using fixed length queues. This fact creates some limitations which translate into trade-offs. The traditional hardware implementation uses two sets of shift registers. One set is used to hold the data in much the same way as in the fixed length FIFO. Data that is placed in the top emerges at the bottom. There is a second shift register that functions in parallel. The second shift register contains flags that indicate whether the associated data element at the same chronological position in the data queue is valid data or not. When data is written into the top location of the data queue, a true flag is placed into the "valid bit" queue. The variable length quality is achieved by allowing the data and its associated valid bit to "sink down" into the next location below it if there is no valid data in that location (see Figure 3). In this way valid data "sinks" to the bottom of the queue and stacks up in much the same way as pearls being dropped into a narrow tube filled with oil. The clocking of data down through the queue is controlled by an internal self-generated clock. The maximum latency or fall-through time is a product of the number of cells in the queue and the internal clock cycle length. This approach meets the requirement that differing rates may be accommodated. The valid bit data is brought out in parallel with the queue data. The valid bit data tells the consumer when valid data is present, thus avoiding the start-up period of invalid data as in the previous implementation of the fixed length FIFO. Examples of this approach are the shorter FIFOs such as the MMI 67401. Fall-through FIFOs tend to have very long undesirable fall-through times if the FIFO is deep.

The software approach could be designed to mirror the typical hardware approach by working with two arrays. One for the data and one of the valid bits. That approach uses too much memory. An alternate could use a wider array which carried the valid bit with the data. The algorithm would then start at the end of the array and pass to the front, advancing all elements which were valid to the end of the array until all valid data was collected at the end of the array. This approach would be very costly in terms of CPU cycles for what is achieved. There is a fall-through latency which is a product of the time to execute the updated software loop times the number of locations in the queue.

TWO-POINTER FIFO

A more economical approach would utilize two pointers and one array that was as wide as the data. One pointer would point to

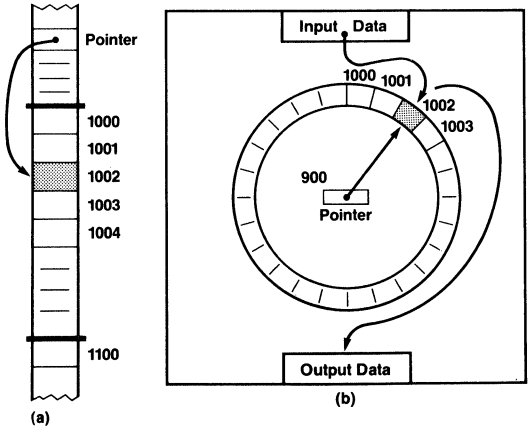

Figure 2. Circular queue with one pointer
a) As it is in memory.
b) Logical view.

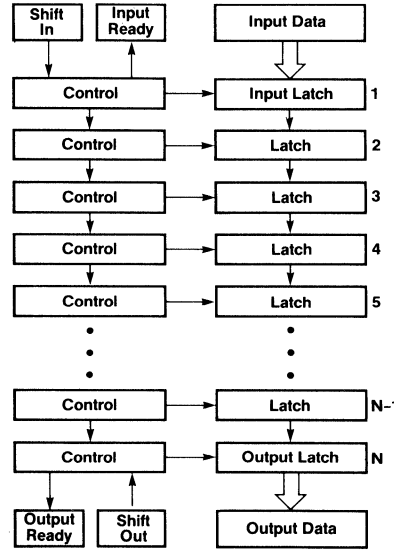

Figure 3. Classical FIFO architecture.

the location at which new data is written into. The second pointer identifies where data is to be read from for output from the queue (see Figure 4). When either pointer is used to access a location, it is incremented. When a pointer is incremented to the last location in the array, the next increment will be substituted with a reset of the pointer to the beginning of the array. The logical view of this structure is a circular queue with a read and a write pointer. This approach results in a much shorter fall-through time while still achieving the variable length feature. The fall-through time is the time that it takes to invoke the software to write the data into the queue, plus the time that it takes to invoke the software to read the data out of the queue. While this is much better than the previous approach, it still requires a reasonable amount of time to accomplish.

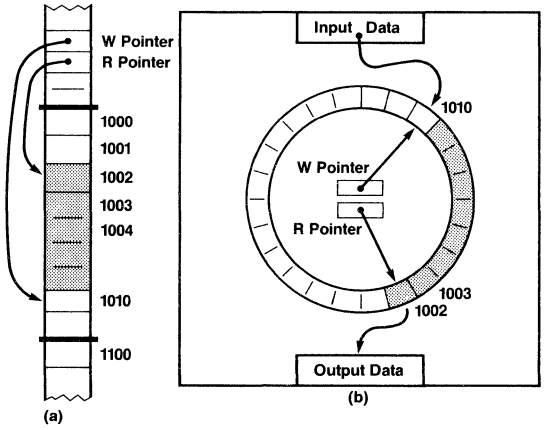

Figure 4. Circular queue with two pointers
a) As it is in memory.
b) Logical view.

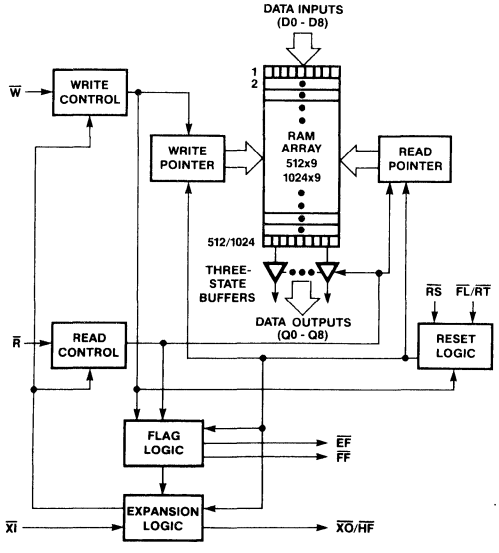

Figure 5. Functional Block diagram of IDT7201/7202 FIFO.

TODAY'S HIGH SPEED FIFOs

The hardware approach, which is used by the IDT7201 and IDT7202 devices, utilizes the software concepts demonstrated in the previous approach but at very fast hardware speeds (50ns typical military). The block diagram in Figure 5 shows the two pointers which locate where reading and writing is to take place in the queue (RAM Array). There is added logic which provides status about the queue: empty ($\overline{EF}$), half full ($\overline{HF}$) and full ($\overline{FF}$) ($\overline{\ }$ means an active LOW signal). Two pins, one input ($\overline{XI}$) and one output ($\overline{XO}$), provide for unlimited expansion while still maintaining the 50ns fall-through time. This part functions identically to the software approach utilizing the two pointers. When either pointer reaches the last location, it is reset to the first location thus achieving a circular queue via a wraparound approach. The status flags reflect the count of how many valid pieces of data are in the queue. After the device is reset, the empty flag ($\overline{EF}$) is asserted. As soon as a datum is written into the queue, the empty flag is deasserted. The empty flag is not asserted again until all pieces of data have been read from the queue. When the count of data elements reaches one-half the number of locations in the RAM array, the half full flag ($\overline{HF}$) is asserted. If a read is performed which reduces the count to just below the half way count, then the ($\overline{HF}$) is deactivated. The full flag is asserted when the count of data elements is exactly equal to the number of locations in the RAM array, thus flagging that there are no more empty locations in the queue.

WIDER FIFOs

Applications may vary widely as to the width and depth of the FIFO required. If an application's maximum requirement is 1024 locations or less and 9 bits in width or less, then the IDT7202 will fit. Wider word widths can be achieved by connecting two or more devices in parallel (control signals). The status flags can be detected from any one device because each device is working in lock step parallel. Figure 6 shows an example of an 18 bit-word composed of two IDT7201/7202 devices. The older classical architecture would require more external circuitry to match the Input Ready and Output Ready signals to account for differences in the internal self-generated clock frequencies. RAM-based FIFOs, such as the IDT7201/7202, do not have this problem.

DEEPER FIFOs

Some applications require deeper FIFOs. In the older architecture, deeper FIFOs mean longer fall-through times because they are connected end to end. The time increases in direct proportion to the number of devices. For example two devices yield a maximum fall-through time of twice that of one device. This can make some applications of FIFOs impractical or totally unusable.

With the two pointer approach used in the IDT7201/7202, the data input busses are connected together and the data output busses are common. This produces a parallel architecture (see Figure 7) as opposed to the serial approach above. The parallel structure is analogous to cascading standard RAM devices to achieve deeper memories.

Since FIFOs do not have chip selects and external decoding mechanisms, the task of choosing which device is selected must be provided for internally. The control (in the IDT7201/7202) is achieved through a unique serial structure. The first (or master)

FIFO is identified by grounding the $\overline{FL}$ input. All other FIFOs in the structure must have the $\overline{FL}$ input pulled up to V_{CC}. The $\overline{XO}$ output of the first FIFO is connected to the $\overline{XI}$ input on the next FIFO in the queue. The $\overline{XO}$ output of that FIFO is connected to the $\overline{XI}$ input of the next and so on until the $\overline{XO}$ output of the last FIFO is connected to the $\overline{XI}$ input of the first FIFO (see Figure 7).

After reset, the active read and write pointers are in the first device. When the write pointer has progressed to the end of the first FIFO device, it outputs a pulse on $\overline{XO}$ which activates the write pointer at the beginning of the next device and simultaneously deactivates the write pointer in the first device. Thus, write enable control is passed to the second device. When the

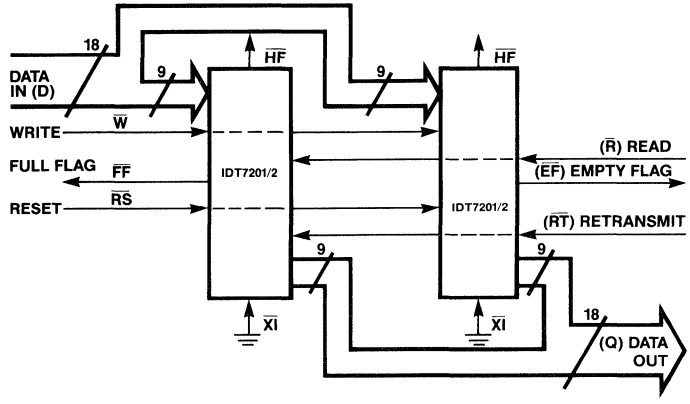

Figure 6. IDT7201/7202 FIFO Word-Width Expansion.

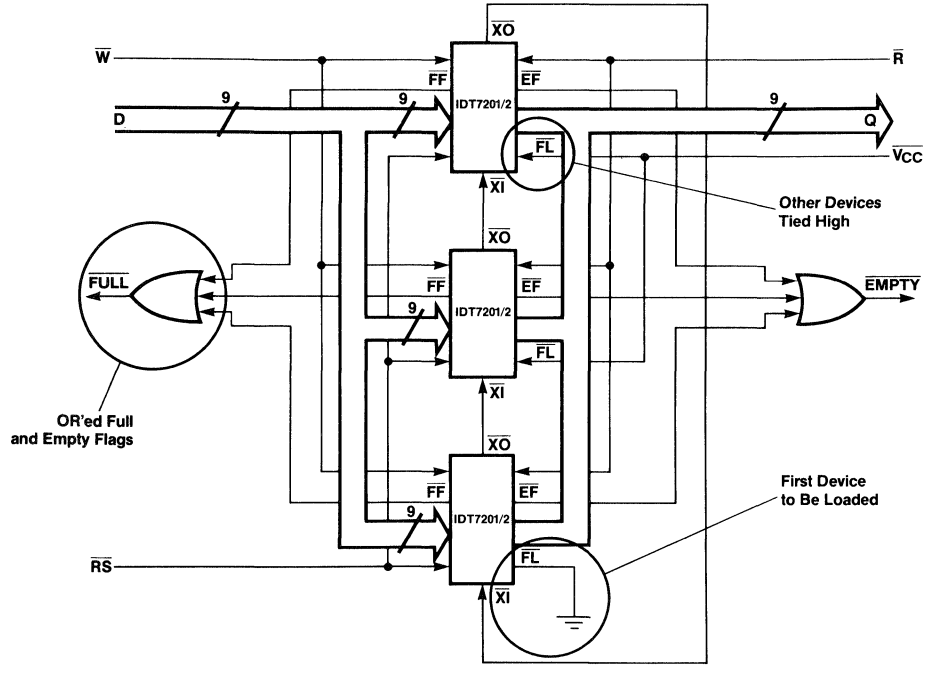

Figure 7. IDT7201/7202 FIFO Word-Depth Expansion.

active read pointer reaches the end of the first device, it terminates and activates the read pointer in the next device with another pulse on the $\overline{XO}$ output of the first device. Figure 8 shows the progression of read and write pointers across two devices. In this ring structure, the read pointer is always chasing the write pointer. The pointer enable crosses the device boundaries via sending an $\overline{XO}$ pulse onto the next device. This continues in a circular queue fashion.

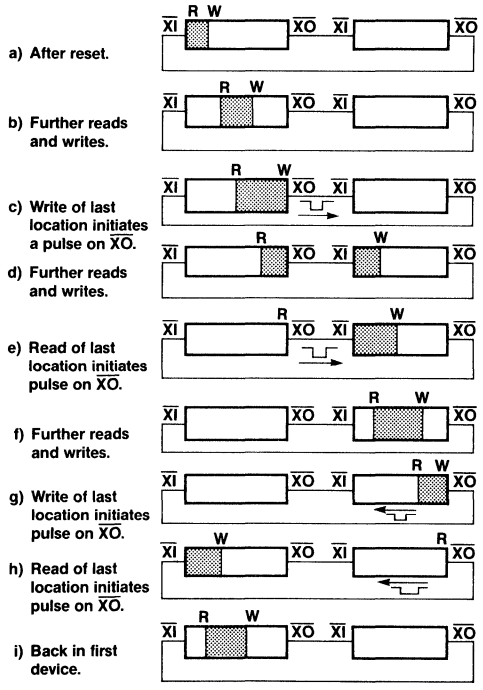

Figure 8. Example on $\overline{XO}/\overline{XI}$ expansion scheme.

The IDT7201/7202 has been designed such that the read and write pointer can never cross over each other even in the cascade mode. The $\overline{XO}$ pulse is synchronous with read and write. When the last location is read or written, the $\overline{XO}$ output goes low with the read or write enable input and back high with the read or write enable. To see why there is no conflict even though reads and writes are asynchronous, the usage must be examined. The case of concern is when the FIFO is empty and the read and write pointers are at the last location. It must be realized that the consumer will not read until the empty flag is deasserted. The empty flag output will go high after the write pulse has gone high again thus ensuring that the $\overline{XO}$ pulse, indicating the write pointer, has been passed on to the next device. The consumer will then read the last location causing another pulse on $\overline{XO}$ which will transfer the read pointer (see Figure 9).

There is one special case regarding read flow-through mode (discussed below). In this mode the consumer can anticipate the write, by producer, by lowering the read enable input. In this case the $\overline{XO}$ input does not go low with read enable. When write enable is lowered, $\overline{XO}$ goes low. $\overline{XO}$ goes high with write enable. At this point the empty flag is cleared, thus signaling to the consumer to terminate the read after the appropriate period specified in the data sheet. During this period the $\overline{XO}$ output, which went high at the end of the write enable pulse, has lowered again. When the read enable is raised by the consumer, the $\overline{XO}$ output goes high. In this way two pulses on $\overline{XO}$ are assured (see Figure 9).

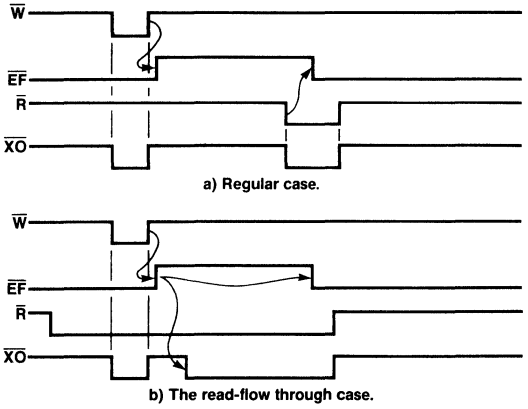

Figure 9. Generation on XO output when the FIFO is empty. a) Regular case. b) The read-flow through case.

Two examples of the IDT7201/7202 in expanded depth configuration are available from IDT commercially. The IDT7M203/204 are Subsystems modules which incorporate onto one ceramic substrate four FIFO LCCs and the $\overline{EF}$ & $\overline{FF}$ "OR" gating to produce 2Kx9 and 4Kx9 FIFOs. The Subsystem module has a lead frame which pins out like the 28-pin 0.6 inch IDT7201/7202. This allows for a plug compatible 4Kx9 FIFO in one socket.

SPECIAL FEATURES OF IDT7201/7202

The architecture used in the IDT7201/7202 provides some features that distinguish it from FIFOs with other architectures. One outstanding feature is the dual port implementation of the RAM array. The RAM is designed in such a way that the read and write ports are separate, allowing for simultaneous asynchronous reads and writes with no hand shaking or arbitration. In the classical architecture the consumer and producer circuits must monitor ready flags for each access.

The IDT7201/7202 support a retransmit function. In the single device solution, the $\overline{FL}/\overline{RT}$ input may be pulsed low signaling a retransmit.

A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 512/1024 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion Mode and will affect HALF FULL FLAG ($\overline{HF}$) depending on the relative locations of the read and write pointers. For example in a communications application, during transmission of a message, the receiver may request a retransmit of the message. This can be accomplished by always starting new messages at the beginning of the queue via a pulse on the reset input. If and when the retransmit request arrives, the $\overline{FL}/\overline{RT}$ line is pulsed. The read pointer is repositioned at the beginning of the queue. The message producer may continue to write more of the same message into the queue as the retransmit

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of the message continues. The retransmit can happen as many times as desired. At the start of the next complete message, the reset line ($\overline{RS}$) must be pulsed after the successful acknowledge by the receiver. The reset ensures that the new message will be placed in the FIFO at the start of internal queue. It should be noted that, when retransmit is possible, messages cannot be bigger than the maximum size of the queue. If the message is longer than the queue, even though the read pointer has progressed far enough to accommodate the extra data, resetting the read pointer back to the beginning with retransmit will produce data from the end of message instead of the beginning.

This architecture supports flow-through modes. In the read flow-through mode, when the buffer is empty, the consumer can anticipate the write, by the producer at the other end, by lowering the read input. When the empty flag ($\overline{EF}$) goes false, the consumer circuitry can terminate the early read cycle by reading the data and deasserting the read signal. The read input must go high for a brief period in order to clock the read pointer. The read flow-through mode avoids the standard sequence of monitoring flag going high before hitting a read cycle.

The write flow-through mode is a mode that is employed when the FIFO is full. The producer can anticipate a read by the consumer by lowering the write input before the read. When the full flag ($\overline{FF}$) raises, the producer knows that the consumer has read a location, thus freeing up a location that can receive the new data. The producer then raises the write input which actually writes the data into the RAM array. This flow-through mode avoids the overhead of monitoring the full flag before initiating a write cycle.

The IDT7201 is pin and functionally compatible with the Mostek MK4501, thus serving as an alternate source. The IDT7202 gives the same functionality as the IDT7201 but is twice as deep (1024x9). The IDT7202 is the largest FIFO made with the zero fall-through time architecture making it the logical choice for FIFO applications.

SOFTWARE VERSUS HARDWARE SOLUTIONS

With every application involving a computer or programmed controller, the designer can trade off between performing certain functions in software or hardware. In general, the software solution is a more flexible design (easily changed) but performs the task more slowly. The hardware solution is less flexible but performs the task very fast.

To clarify these concepts, a discussion of an application and how it could be solved at the various levels from software to hardware is beneficial. A good example is a file server. The server could be connected to a Local Area Network (LAN) and, on the other side, to a Winchester disk drive. Both I/O connections demand attention at unpredictable intervals and must be serviced on demand or data is lost.

If the data rate of both interfaces is sufficiently low, a total software solution might be considered. The data rate would have to be low enough such that the software code could poll the status of either I/O port. As data arrives it could be placed into software FIFO queues. When a full record is buffered, then processing would commence. During the processing, the I/O ports must still be monitored as another user on the LAN might make a request (see Figure 10). It is doubtful that a total software solution could be designed for the server application that would have acceptable system performance.

The next approach to consider might be to include hardware interrupts. Interrupts allow for one task to be running and almost immediately switching to an I/O service routine. Interrupts are something like a hardware subroutine call. This scheme would use the interrupt mechanism to call routines to move data to and from the I/O ports and the software FIFO queues. The overhead of constantly polling the I/O port status flags would be eliminated, thus allowing for higher system performance. An asynchronous-type problem is introduced with interrupts. To use interrupts properly, the I/O service routines may be called at any instance. Therefore, the interrupt routines must be designed in such a way that they do not destroy data that the interrupted task might be using. Usually, the routines must be careful to save the state of the machine, perform their task and restore the state of the machine. The extra code to maintain the state of the machine is an overhead that is not in the polled solution. Worse yet, saving the state of the machine may be too much overhead to allow for an interrupt during a time-critical piece of code. Because interrupts may not be acceptable at certain points in the code, the programmer must insert code to disable and re-enable interrupts around the critical sections.

Where the polling scheme provides a solution which has a more easily definable sequence of execution, the interrupt solution is indefinite. The programmer must spend a lot more time proving that all possible sequences caused by random interrupts will produce desirable results. Because interrupts may not be acceptable at certain points in the code, the programmer must insert code to disable and re-enable interrupts around the critical sections. The interrupt disable solution not only cuts performance by not accepting I/O during some periods, but also adds more overhead with the maintenance of the interrupt enable mechanism. In some sense, interrupts can be to software what the meta-stable flip-flop problem is to hardware.

The interrupt solution can be moved out of the software and more into the hardware realm through the use of a technique called Direct Memory Access (DMA). The DMA solution is provided by a block of circuitry which monitors the I/O ports. When the port requires attention, the DMA logic interrupts the current task at the bus transfer level and steals a memory cycle to transfer the data to or from the port and the FIFO queue in memory. The task that is running on the processor misses only a few memory cycles now and again which is much less than in the interrupt scheme where a whole subroutine of many memory cycles was executed to transfer each element of data. The DMA solution is not for free. DMA controllers are complex devices which must be programmed as well as designed into the bus structure. The DMA mechanism can only serve one source at any given instance in time thus still being a bottleneck in throughput.

So far, each solution proposed has moved the mechanism that feeds data to or from FIFOs in program memory away from the software and closer to the I/O port. The memory bus still remains the bottleneck because both FIFO queues are in memory. To simplify and improve performance, hardware FIFOs such as the IDT7201/7202 can be used. The processor would interface to the FIFO through an I/O port as before, but the FIFO would now be between the I/O port and the rest of the hardware. The software could then service the data at a steady rate and be sure that data was not lost without the problems or overhead of more complicated schemes such as interrupts or DMA.

Because the queues are between the controller and the peripheral, the peripheral can load or read the queue without interrupting the controller. Since the controller is not involved

with maintaining both queues, there is no possibility of lost data because one queue was being serviced while data for the other queue arrived. For these reasons the hardware FIFO represents the highest performance solution.

If the designer uses large FIFOs like the IDT7202, there is a minimum of device count. Assuming 2 FIFOs (transmit and receive) for each I/O port gives a count of four 28-pin devices for the FIFO solution. The DMA solution would at least be one 40-pin device and several bus buffer/control devices. The interrupt solution would require a similar parts count to the DMA solution. Therefore, the FIFO solution is not only the highest performance solution but usually has the lowest part count of the hardware solutions.

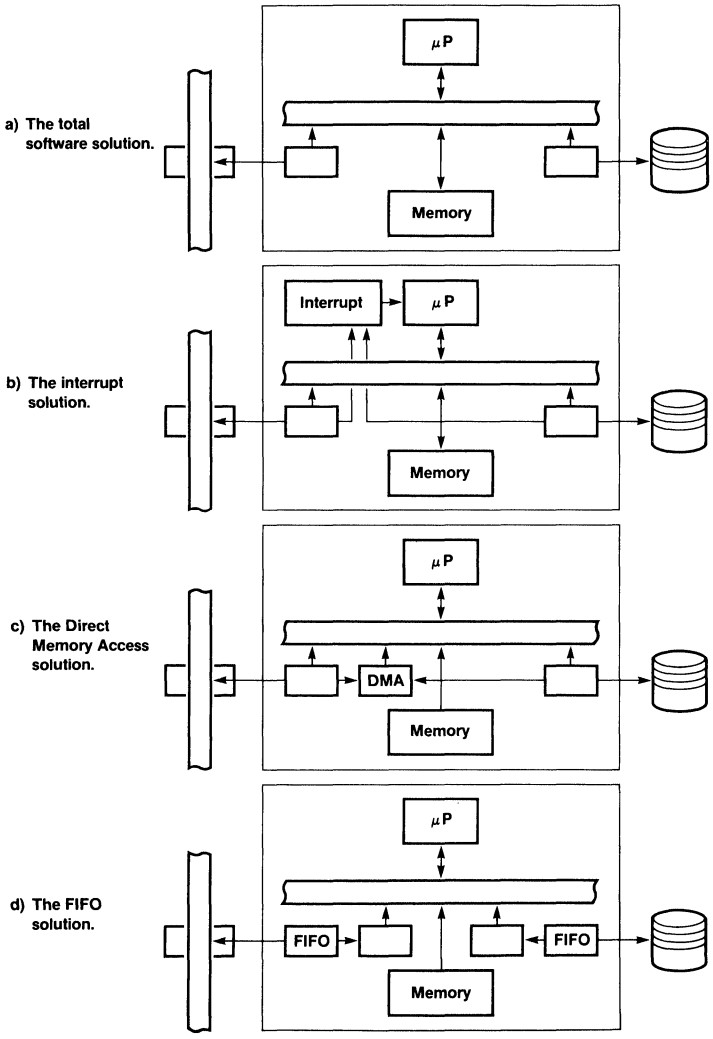

Figure 10. Example solutions for File Servers.

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COMMUNICATIONS-MULTIPLEXOR APPLICATION

Another example of a rate mismatch problem is shown in a CRT terminal and CPU interface. In order to not load the CPU with the burden of monitoring the UARTs of multiple CRTs and printers, a communications controller is employed. The controller can serve as a communications multiplexor and data concentrator (see Figure 11).

As the controller receives characters it must buffer them such that if multiple characters are received close together from several terminals, they will not be lost as more characters come in. The natural structure to store them in is a queue of the FIFO type. The CPU will then need to respond to the characters. If the controller is inputing other characters, the CPU should not have to wait until the controller is done. Therefore, a FIFO can be employed on the transmit side as well as the receive side. To make the design simple, two sets of FIFOs could be placed between the CPU and controller. When characters are received they are placed in one end of a FIFO and read from the other end by the CPU. As the CPU prepares characters for transmission, it places them in a FIFO going the other direction. The controller then reads them from the other end of the transmit FIFO and sends them out through the UART.

Conceivably, there could be a pair of FIFOs for each UART. That way it would be easy for both the controller and the CPU to keep straight which characters correspond with which UART. While this provides for a large total of buffer space for characters, it is more than needed when using a part like the IDT7201/7202. For eight UARTs, this scheme would require a minimum of sixteen FIFO devices. A better solution would be to use one FIFO device in either direction. If an IDT7202 were used, it could provide a maximum of up to 128 characters per UART if all the UARTs input at the same time and rate. While the two FIFO techniques would most likely provide plenty of buffering at a minimal device count, it presents the problem of which character belongs to which UART. The solution is to make a wider FIFO which is 18 bits wide; thus using 4 devices instead of 16 devices for 8 UARTs. This would allow for a UART number to be placed in the FIFO along side each character. The remainder of the word could be used for flag, status and command information between the CPU and the controller. For example, several of the bits in the FIFO word could indicate whether the character information was a character to send or BAUD change rate information.

The empty and full flags of the IDT7201/7202 FIFO would be used as status flags. For example, the transmit buffer must be monitored from both sides. As the CPU prepares a character to transmit, it would first examine the full flag ($\overline{FF}$) to see if the FIFO is full. If the FIFO was full, it would delay outputting the character. If the buffer is not full then it would place the character in the FIFO. The empty flag ($\overline{EF}$) would be monitored by the controller. As soon as the CPU places a character into an empty FIFO, the empty flag would change to not true. At this point the controller would know there was a character in the buffer which could be transmitted. The controller would read characters from the buffer as long as the empty flag was not true (buffer contains more than one character).

CONCLUSION

Hardware FIFOs are an economical memory organization to use when lists of data items are to be buffered. Because they do not require an address to access items in the list, there is less overhead in terms of circuitry and access time. The FIFO buffer is most often used as a "system rubber band" to stretch between the differing and fluctuating rates of different elements in a system. The IDT7201/7202 FIFO device features the newest RAM-based architecture and provides the latest in technology in terms of access time, fall-through time and size, thus providing the most economical solution for today's design needs.

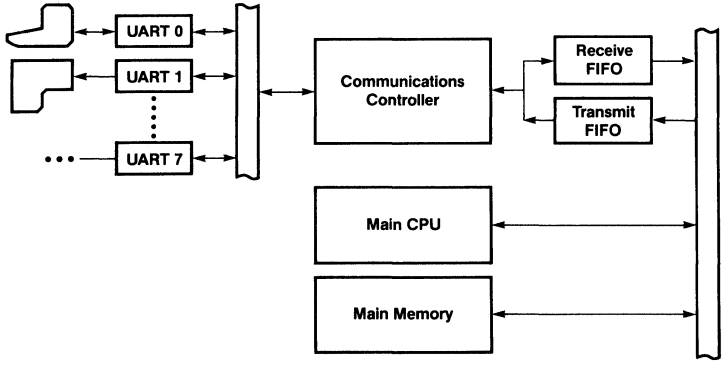

Figure 11. Communications Controller example.

Integrated Device Technology, Inc.

DUAL-PORT RAMS SIMPLIFY COMMUNICATION IN COMPUTER SYSTEMS

APPLICATION NOTE AN-02

By David C. Wyland

INTRODUCTION

Dual-port RAMs allow two independent devices to have simultaneous read and write access to the same memory. This capability allows the two devices to communicate with each other by passing data through the common memory. These devices might be a CPU and a disc controller or two CPUs working on different but related tasks. The dual port memory approach is useful and popular because it allows the same memory to be used for both working storage and communication by both devices and avoids the need for any special data communication hardware between the devices. The latest development in dual-port RAMs has been the appearance of high-speed dual-port RAM chips. These chips allow high-speed access by both devices with the minimum amount of interference and delay. Integrated Device Technology offers a family of these devices as shown in Table 1.

TABLE 1. DUAL-PORT RAMS AVAILABLE FROM INTEGRATED DEVICE TECHNOLOGY

SIZE	TYPE	PART NO.	T_{AA}	NOTES
1K x 8	Master	IDT7130	55/70/90ns	Includes interrupt logic
1K x 8	Slave	IDT7140	55/70/90ns	
2K x 8	Master	IDT7132	55/70/90ns	
2K x 8	Slave	IDT7142	55/70/90ns	

DUAL-PORT RAMS: SIMULTANEOUS ACCESS

A dual-port memory has two sets of address, data and read/write control signals, each of which access the same set of memory cells. This is shown in Figure 1. Each set of memory controls can independently and simultaneously access any word in the memory including the case where both sides are accessing the same memory location at the same time. Up to this time there have been very few true dual port memories available. Conventional memories have a single set of controls for address, data and read/write logic and are thus single port RAMs. In the past, if you wanted a dual-port RAM function, you had to design special logic to make the single port RAM simulate a dual-port RAM in operation.

DIRECT MEMORY ACCESS (DMA) AS A DUAL-PORT MEMORY SIMULATION

The concept of using a conventional memory to simulate a dual-port RAM has been common in computer systems almost from the beginning. It is known under the name Direct Memory Access, or DMA. In the DMA concept, a single memory is shared between the CPU and one or more I/O devices as shown in Figure 2.

Each device wishing to use memory submits a request to the arbitration logic. The arbitration logic responds by connecting the memory address, data and control lines to one of the requesters and tells any other requesting devices to wait by

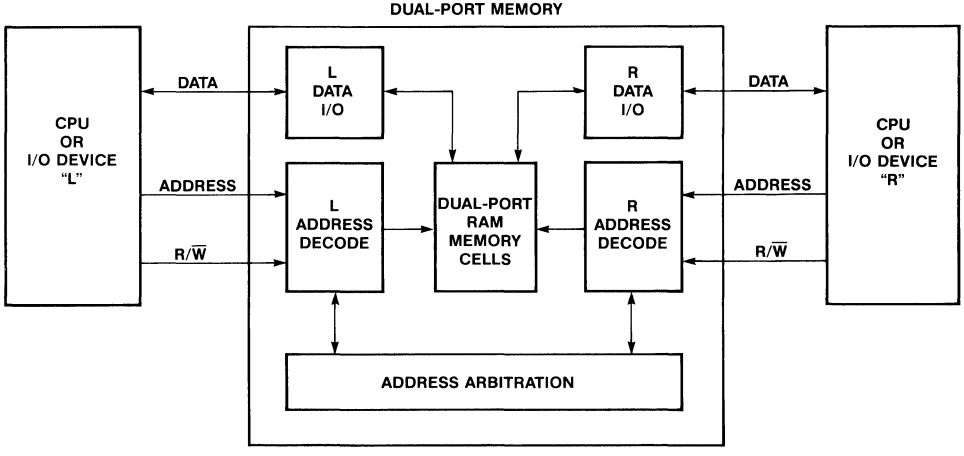

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Figure 1: Dual-Port Memory Block Diagram

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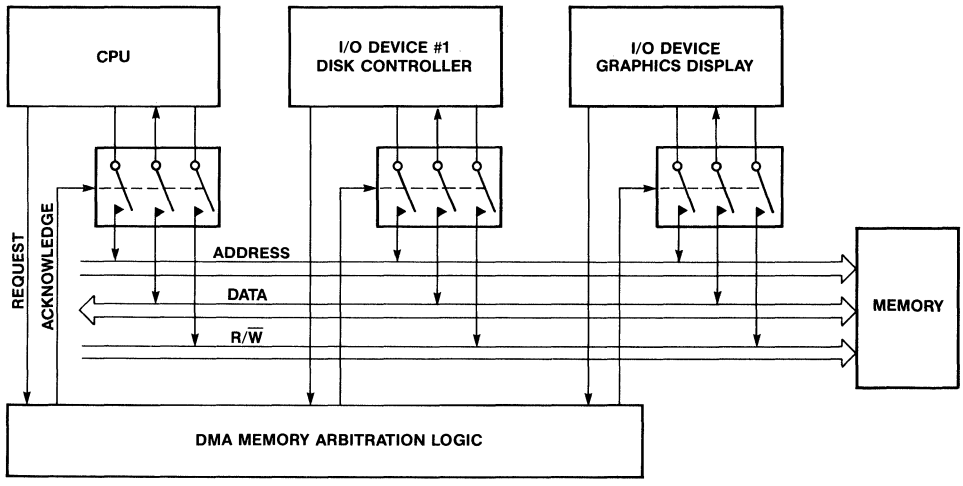

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Figure 2: DMA Memory System Block Diagram

issuing a busy signal. The busy signal causes the memory access logic in the device to wait until BUSY has gone away before performing a memory transfer.

DMA LIMITATIONS: WAITING FOR THE BUS

In a computer system with DMA, the CPU must stop and wait while an I/O device is doing DMA transfers to memory. This works well in typical systems where the I/O devices are transferring data only a small percentage of the time and the impact on CPU processing time is minimal. These assumptions do not hold where you have two CPUs trying to use the same memory. In this case one CPU must wait while the other uses the memory. As a result, the average speed of the CPUs will typically be cut in half.

There are two solutions to this problem: 1) You can provide local memory for both CPUs and limit use of the common memory to CPU/CPU communication only in an attempt to reduce the time impact of DMA waiting, or 2) You can provide true hardware dual port memory between the CPUs and allow simultaneous high-speed access by both CPUs to the same memory without waiting. The introduction of high-speed dual port RAM chips now makes the second option practical.

DUAL-PORT RAM CHIPS: HOW THEY WORK

A true dual-port memory allows independent and simultaneous access of the same memory cells by both devices. This means two complete and independent sets of address, data and read/write logic, and memory cells that are capable of being read and written by two different sources. An example of the dual-port memory cell is shown in Figure 3. In this cell both the left and right hand select lines independently and simultaneously select the cell for readout. In addition, either side can write data into the cell independent of the other side. The only problem would be when both sides try to write into the same cell at the same time. We will discuss this in a moment.

ARBITRATION: USING THE SAME ADDRESS

A problem that can occur with dual port memories is when both ports attempt to access the same address at the same time. There are two significant cases: when one port is trying to read the same data that the other port is writing, and when both ports attempt to write to the same word at the same time. If one port is reading while the other port is writing, the data on the read side will be changing during the read, and a read error can be caused. If both ports attempt to write at the same time, the memory cell is being driven by both sides, and the result can be a random combination of both data words rather than the data from one side or the other. The solution to these problems is arbitration. Arbitration, usually implemented in hardware, insures that both sides can't use to the same cell at the same time.

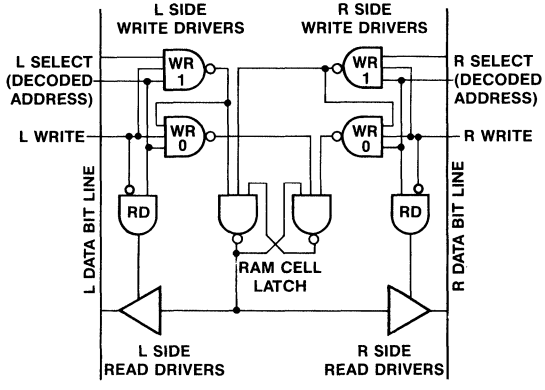

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Figure 3: Dual-Port RAM Cell

One way to avoid the arbitration problem is to design the system so that both sides can never use the same address at the same time. This can be done by separating the memory into two areas. One area is used by the left side, and the other area is used by the right side. At the appropriate time, the access to these blocks is swapped. This can be practical in systems where the dual-port RAM is being used primarily as a communication medium between the two processors. This approach will allow the highest performance for the dual-port memory system since there is no arbitration logic delay to be taken into account.

SOFTWARE ARBITRATION BY SEMPAPHORES

A variation of the software arbitration approach is to temporarily assign memory access capability to one processor or the other using flag bits in the memory called semaphores. A semaphore is a bit in the memory which can be read or written by either CPU. This bit is used as a token to indicate which CPU has permission to use the memory. For example: if the semaphore bit is zero, the left side would be enabled, and if a one the right side would be enabled. A single bit can be used for the whole memory, or a block of bits could be used to selectively enable different portions of the memory. In use, the semaphores are initially set to enable one of the processors. When that processor is through using the memory, it sets the semaphores to the opposite state, enabling the other CPU.

Although semaphores are a software technique they can benefit from hardware support. One problem with semaphores is that the CPU that is waiting to access the memory must continually test the semaphore. An alternative to this is to provide hardware that will allow one CPU to interrupt the other when there has been a change in the semaphore status. In this case the CPU does not have to wait for the semaphore but can be doing other tasks until the interrupt comes that indicates that the semaphore has changed.

HARDWARE SUPPORT FOR SEMAPHORES

Hardware support for semaphore interrupt activity is provided by certain IDT dual-port RAM chips. A block diagram of this logic is shown in Figure 4. In these chips, the top two addresses of the memory chip also serve as interrupt generators for each of the ports. If the left side CPU writes into the odd address of this pair, (3FF in a 1K RAM), an interrupt latch is set and the interrupt line to the right hand port is activated. This interrupt latch is cleared when the right hand CPU reads from the odd address. A similar set of logic is provided to allow the right hand CPU to interrupt the left hand one. This logic is associated with the even address of the pair (3FE in a 1K memory). Providing this logic on-chip saves the system designer from having to design in extra logic to allow one CPU to interrupt the other.

HARDWARE ARBITRATION FOR MAXIMUM SPEED

Hardware arbitration detects when an actual attempt is made by both sides to use the same cell at the same time. If this condition is detected, one port is allowed access, and the other port is inhibited from access. The port which is inhibited also receives a busy signal indicating that its CPU is to wait until the contention no longer exists. This solves the arbitration problems of one port trying to read while the other port is writing and both ports attempting to write to the same address at the same time.

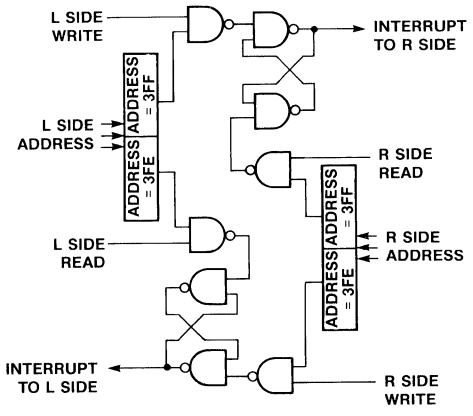

Figure 4: IDT7130 Semaphore Interrupt Logic

Arbitration in hardware provides the fastest and most general solution to the dual-port arbitration problem. Hardware arbitration provides high speed in the system sense because neither CPU has to spend time testing to see if it is allowed to write into the dual-port RAM. Also, the time spent by a CPU waiting to access the RAM but delayed because of arbitration, is small when measured as a percentage of the total time the memory is used. For example, if there are a thousand words in memory with a relatively uniform and random access of these locations by either side, the probability of a given location being accessed by one side is of the order of one part of a thousand. The probability of both sides accessing the same location at the same time is therefore of the order of one part in a million. As a result, the average throughput of the system is reduced by only one part per million due to dual-port RAM access contention (again, assuming uniform random address access by both sides).

HARDWARE ARBITRATOR DESIGN

A hardware arbitrator consists of common address detection logic and a cross coupled arbitration latch. A logic diagram of a hardware arbitrator of the type used in the IDT dual-port RAM chips is shown in Figure 5. The purpose of this logic is to provide a busy signal for the address that arrived last, to inhibit writing to the busy port, and to make a decision in favor of one side or the other when both addresses arrive at the same time. This logic consists of a pair of address comparators, a pair of delay buffers, a cross-coupled latch, and a set of busy output drivers. Each address comparator output goes true when its address inputs are equal.

In the logic shown in Figure 5, the ability to detect which address arrived last is provided by the time delay buffers between address lines and the comparators. If we assume that the L address is stable and the R address changes to match the L address, the R address comparator will go true immediately while the L address comparator will become active some time later as determined by the time delay gates.

The arbitration latch formed by the L and R gates reflects the address comparator output timing. This latch has three stable states: both latch outputs A and B high, A low/B high, and A

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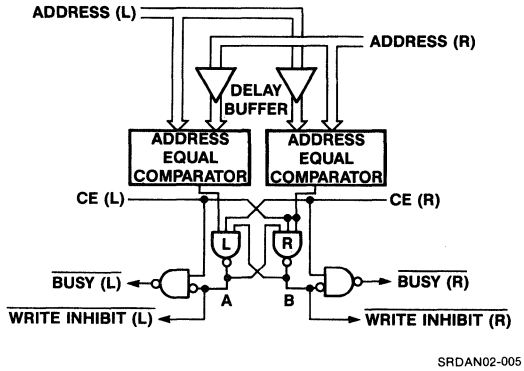

Figure 5: Hardware Arbitrator Logic

high/B low. Initially, both A and B are high because the outputs of both address comparators are low. We start with the L address stable and the R address arriving later. When the R comparator becomes active, its output will go high, and B will go low. The A output will remain high because its address comparator input will go high sometime later, and the L gate input from B output will go low before this occurs. The result is that the R gate B output will be active inhibiting writing to the R side of the dual-port RAM and activating the busy signal to the R port.

The extreme case of hardware address arbitration is when both addresses arrive at exactly the same time. In this case, the outputs of both address comparators go high at the same time, activating both sides of the arbitration latch. The latch will settle into one of two states with either the A or the B latch output being active. The latch design insures that a decision will be made in favor of one side or the other.

The chip enable lines come directly into the arbitration latch, although they could have been brought into the address comparators along with the other address lines. This is because, if the chip enable for one side is inactive, both reading and writing for that side is automatically inhibited and/or arbitration is not needed. If the addresses are equal, the chip enable that arrives last will lose the arbitration. If both chip enables are active then arbitration will be determined by the settling of the address lines.

DUAL-PORT RAM CHIP TIMING

The timing diagram shown in Figure 6 shows the relationships between address, data, read/write, chip select and busy signals for a dual-port RAM chip and hardware arbitrator. In this diagram, the chip select is used to enable the chip for a read or write operation after the addresses have settled. An arbitration is performed at the leading edge of the chip select.

HARDWARE ARBITRATOR TIMING

In the case of address contention, the busy signal from the losing RAM port stabilizes some time after the leading edge of its chip select (or its address settles, whichever comes last). If the busy signal is going to become active, it will become active during this time or not at all. If the busy signal is generated, the CPU must wait for busy to go away before completing the read or write cycle. Once the busy signal has gone high, the memory read or write cycle can proceed to completion.

Note that during the arbitration time following the chip select, the busy signal may be changing. Since it is possible to have a glitch on the busy line during this indeterminant period, the busy line should be sensed as a level rather than as an edge.

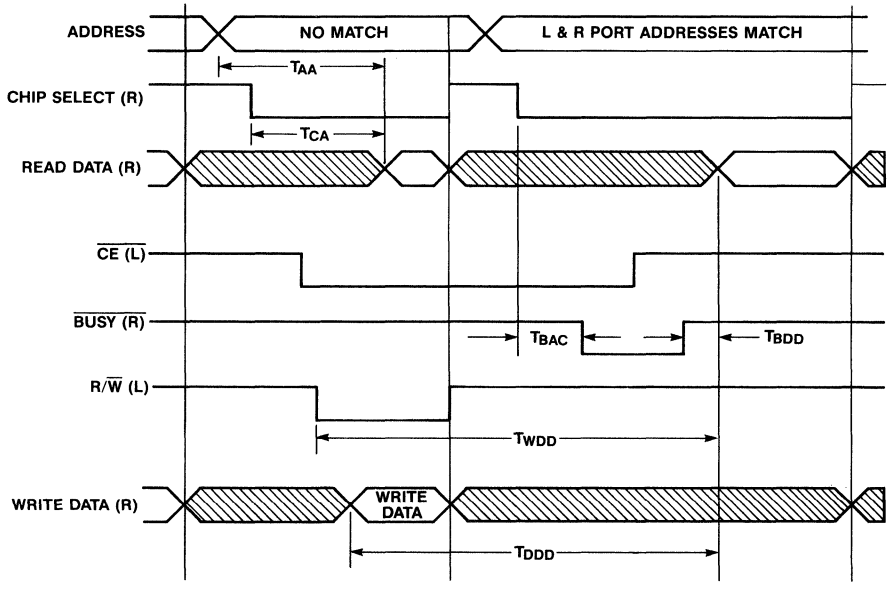

Figure 6: Dual-Port RAM Timing Diagram

Busy arbitration will be somewhat slower in the extreme case where both addresses arrive at exactly the same time. This is because both gates of the arbitrator latch are initially inactive and must settle into a state where only one of them is active. There will be a period of time when both gates are in transition. This is called the metastable condition and is a classic and unavoidable problem in latch and flip-flop design. The metastable condition can typically exist for several gate delay times. As a result, hardware arbitration times are somewhat longer in the worst case than might be expected by simply adding gate delays. The maximum arbitration times, T_{BAA} and T_{BAC}, on the data sheet give the worst case values for these times.

READ/WRITE TIMING

The read and write timing for either port of the dual-port RAM chip is the same as a simple static RAM in the absence of address contention. All the standard timing measures apply: read data address access time is T_{AA}, etc.

Dual-port RAMs have additional timing specifications for the case of address contention where one port is busy and waiting for access. For the most general and conservative case, the read or write cycle for the waiting side should begin after the busy signal goes away. The actual timing can be somewhat shorter than this in most cases.

For the case where the waiting side is waiting to write, the write timing requirement is that the write pulse width be measured from $\overline{BUSY}$ going away. For the case where both sides are reading, the data will be available at the outputs one access time after the address/chip select lines settle even though the busy line is active. In the most common case, the trailing edge of busy will occur more than one access time after the address and data for the busy side have settled. As a result, the read access time as measured for the trailing edge of $\overline{BUSY}$ for this case, T_{BDD}, is effectively zero.

The write/read case of waiting to read while the other side is writing to the same location has some additional timing specifications. Since writing to a location by the L side, for example, will involve changing the data the cell being read by the R side, there is a write-to-read propagation delay time. This time is T_{WDD} for the delay for constant write data from the leading of the write pulse to the read data, and T_{DDD} for the delay for changing write data from a change of the write data to the read data.

If the writing side is running at minimum values for the write pulse or write data set-up times, the read access time, T_{BDD}, will no longer be zero. The actual T_{BDD} will be somewhat less than T_{WDD} minus the actual write pulse width or T_{DDD} minus the actual write data set-up time, which ever is larger (and greater than zero). Note: T_{BDD} is always less than T_{AA} for the worst case of minimum write values. This is why the read or write cycle is begun from the trailing edge of busy for the most conservative case recommended above.

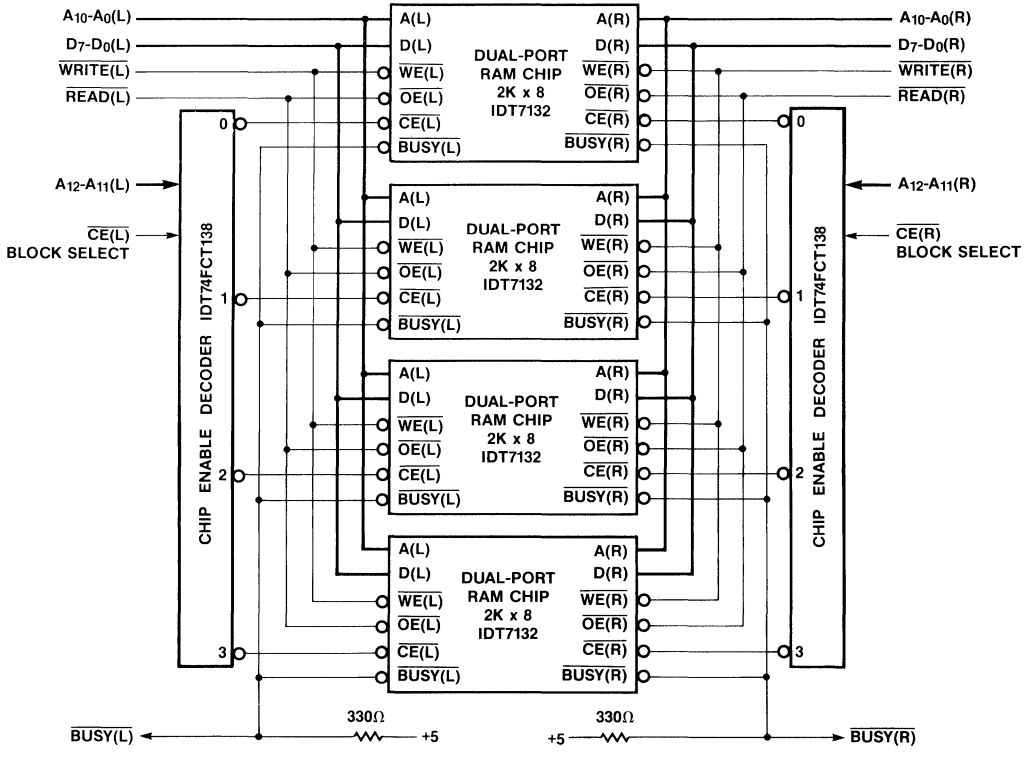

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Figure 7: Depth Expansion of Dual-Port RAMs

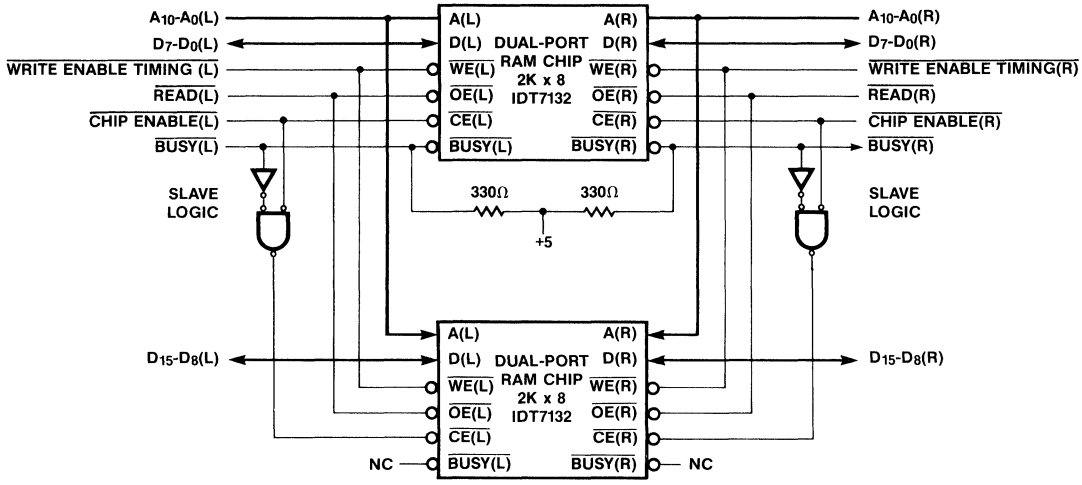
DUAL-PORT MEMORY EXPANSION: MAKING BIG ONES OUT OF LITTLE ONES

Dual-port RAM chips can be combined to form large dual-port memories. Expansion in memory depth with dual-port RAMs is similar to expansion in depth for conventional RAMs. An example of this kind of expansion is shown in Figure 7 where an 8K x 8 dual-port RAM has been made out of 2K x 8 dual-port RAM chips.

WIDTH EXPANSION: THE BUSY LOCK-UP PROBLEM

Dual-port RAMs can also be expanded in width. However in this case, we have a subtle problem. Expansion in width implies that several dual-port RAM chips will be active at the same time. This is a problem if several hardware arbitrators are active at the same time. If we examine the case of a 16-bit RAM made out of two 8-bit RAMs, we can better understand the

WIDTH EXPANSION WITH SLAVE LOGIC (NOT RECOMMENDED)



WIDTH EXPANSION WITH SLAVE CHIPS (RECOMMENDED)

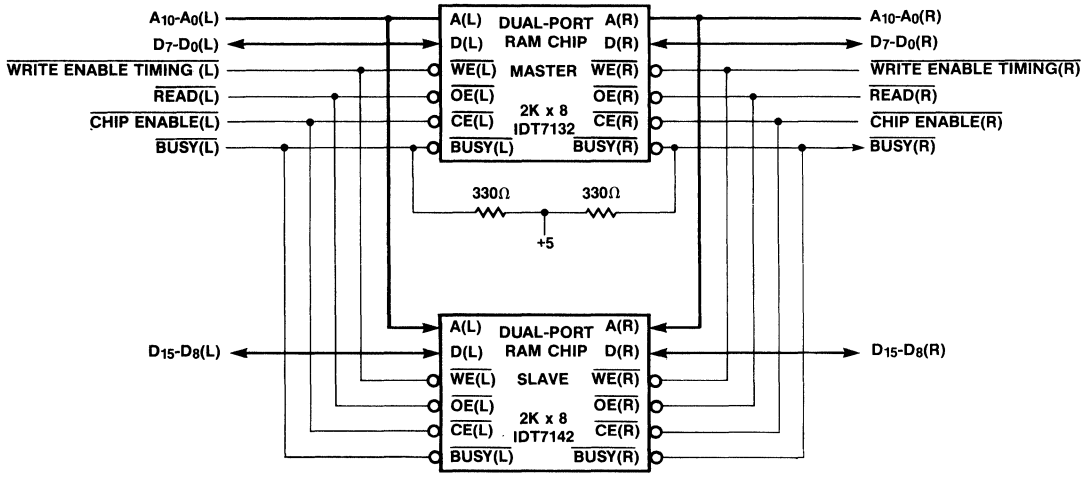


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Figure 8: Width Expansion of Dual-Port RAMs

problem. If the addresses for both ports arrive simultaneously at both RAMs, it is possible for one RAM arbitrator to activate its L busy signal and the other RAM to activate its R busy signal. If both busy signals are used on each side, we now have a situation where both sides are simultaneously busy. The system is now locked up since both sides will be busy and both CPUs will wait indefinitely for their port to become free.

THE BUSY LOCK-UP SOLUTION: USE ONLY ONE ARBITRATOR

The solution to this busy lock-up problem is to use the arbitration logic in only one RAM and to force the other RAM to follow it. In this case one RAM is dedicated as the arbitration master and additional RAMs are designated as slaves. Two solutions to this problem are shown in Figure 8. One solution is to add external logic to the chip-enables of additional dual-port RAM chips. The logic gates shown cause the slave RAM chip select to be disabled if the master RAM is busy. Since only one set of arbitration logic is controlling the system, the problem of slave lock-up is avoided.

The second, more desirable solution is to use specially designed dual-port RAM slave chips, which are part of IDT's product line. These slave chips incorporate the slave disable logic internally so that no additional logic is required to make a master/slave combination. In the slave chip, the busy pin serves as an input rather than an output. If the master chip activates $\overline{BUSY}$, the slave chip will sense this busy state and internally disable its write enable. Slave chips provide a speed advantage over systems which use external logic to implement the slave function. Since the slave logic is built into the slave RAM chip, it can be designed so that there is no speed penalty when using slave chips to expand the dual-port RAM width.

WIDTH EXPANSION: WRITE TIMING

When expanding dual-port RAMs in width, the writing of the slave RAMs must be delayed until after the busy input at the slave has settled. Otherwise, the slave chip may begin writing while the busy signal is settling. This is true for systems using slave chips and for systems using conventional dual-port RAMs with slave logic. This delay can be accomplished by delaying the write enable to the slave by the arbitration time of the master. This is shown in Figure 9.

Note that the write delay is required only in width expanded systems which use slave RAMs; not in single chip or depth expanded systems where only one chip is active at a time. This is because the individual chips have a built-in delay between the chip select and write enable inputs and the internal write enable to the RAM. Separate timing must be supplied in the slave case because this internal delay time can be balanced to the arbitration time only within a chip and can vary from chip to chip. If the delay time for the slave is less than the arbitration time of the master, writing could begin before $\overline{BUSY}$ became active, as above. This will increase the write cycle time in most cases.

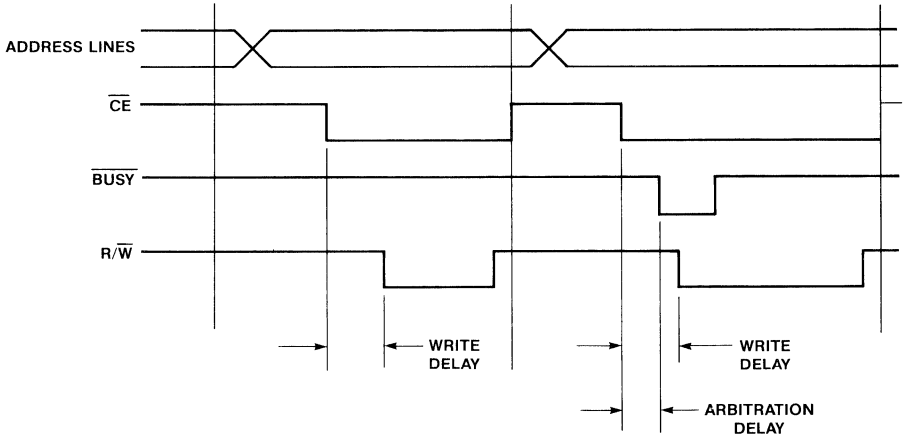

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Figure 9: Master/Slave Write Timing

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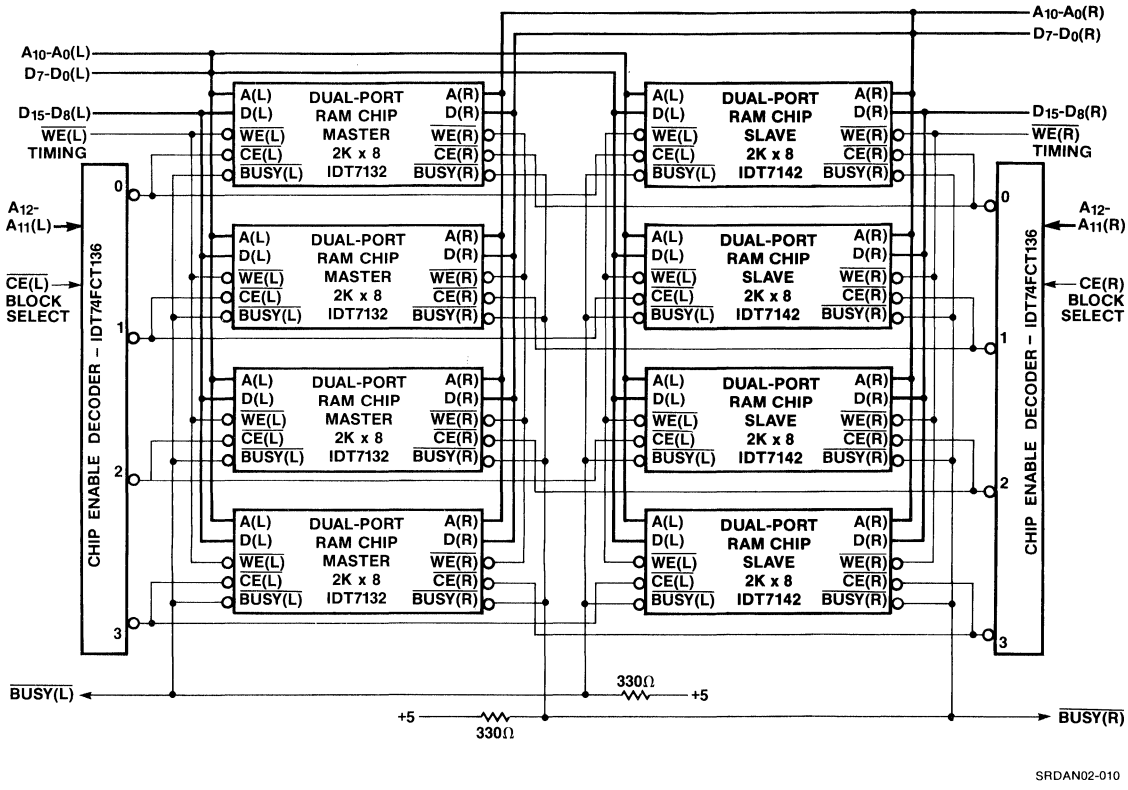

Figure 10: Width and Depth Expansion of Dual-Port RAMs

WIDTH AND DEPTH EXPANSION: AN EXAMPLE

These techniques for expanding dual-port memories in width and depth are combined in the example shown in Figure 10. In this example an 8K x 16 dual-port memory is made from 2K x 8 chips in master/slave combination.

USING THEM: DUAL-PORT RAM APPLICATION EXAMPLES

Examples of dual-port RAMs used for CPU-to-CPU communication are shown in Figures 11, 12 and 13. In Figure 11 a pair of 8-bit processors communicate using a single 2K x 8 dual-port RAM chip. Figure 12 shows a similar system where a pair of 16-bit processors communicate using a pair of dual-port RAM chips and a master-slave configuration. Finally in Figure 13 we have an 8-bit processor communicating with a 16-bit processor through two 2K x 8 dual-port RAMs.

In Figure 11, two Z80 microprocessors communicate using a single IDT7132 dual-port RAM chip. The IDT7132 is controlled by the chip enable. The write enable is set-up in advance by the $\overline{WR}$ signal from the Z80, and the chip enable is used to write data into the RAM or to gate the read data onto the Z80 bus. The output enable (not shown) is tied to ground (continuous enable). The write enable is used to disable the output drivers.

In Figure 12, two 68000 microprocessors communicate through a pair of dual-port RAMs. An IDT7132/7142 master/slave pair is used to avoid the busy lock-up problem. Note that the Address Strobe (AS) from each 68000 is used with an address decoder to enable the dual-port RAM chips. This is to maintain the address for read-modify-write cycles so that arbitration is not lost between the read and the write. This is important for Test and Set instructions, for example.

In Figure 13, a Z80 and a 68000 communicate using a pair of IDT7132 dual-port RAMs. No slave logic is required because the Z80 side chip enable decode insures that only one RAM chip will be enabled at a time. Otherwise, this ficture is a combination of the logic from Figures 11 and 12.

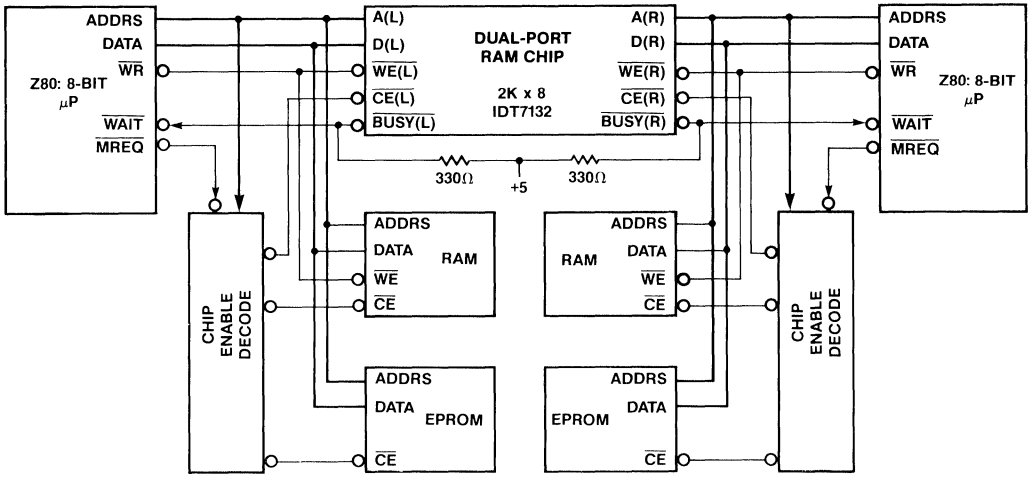

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Figure 11: 8-Bit to 8-Bit CPU Communication

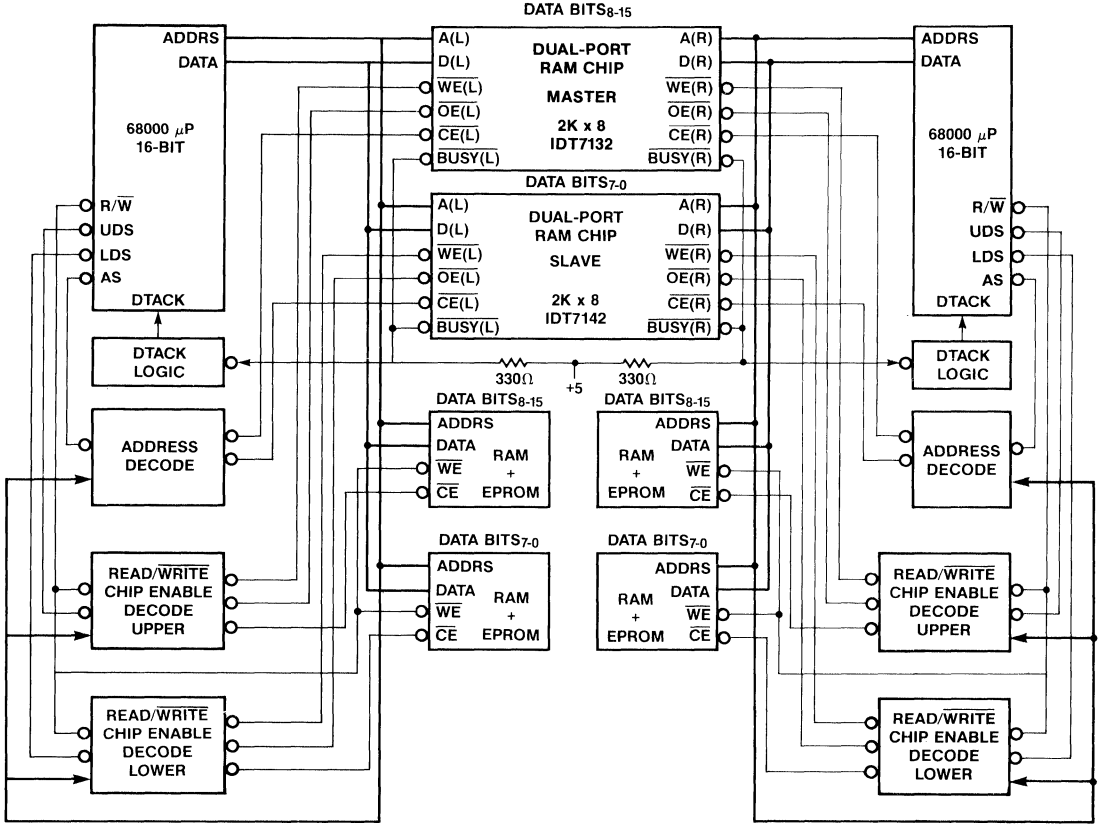

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Figure 12: 16-Bit to 16-Bit CPU Communication

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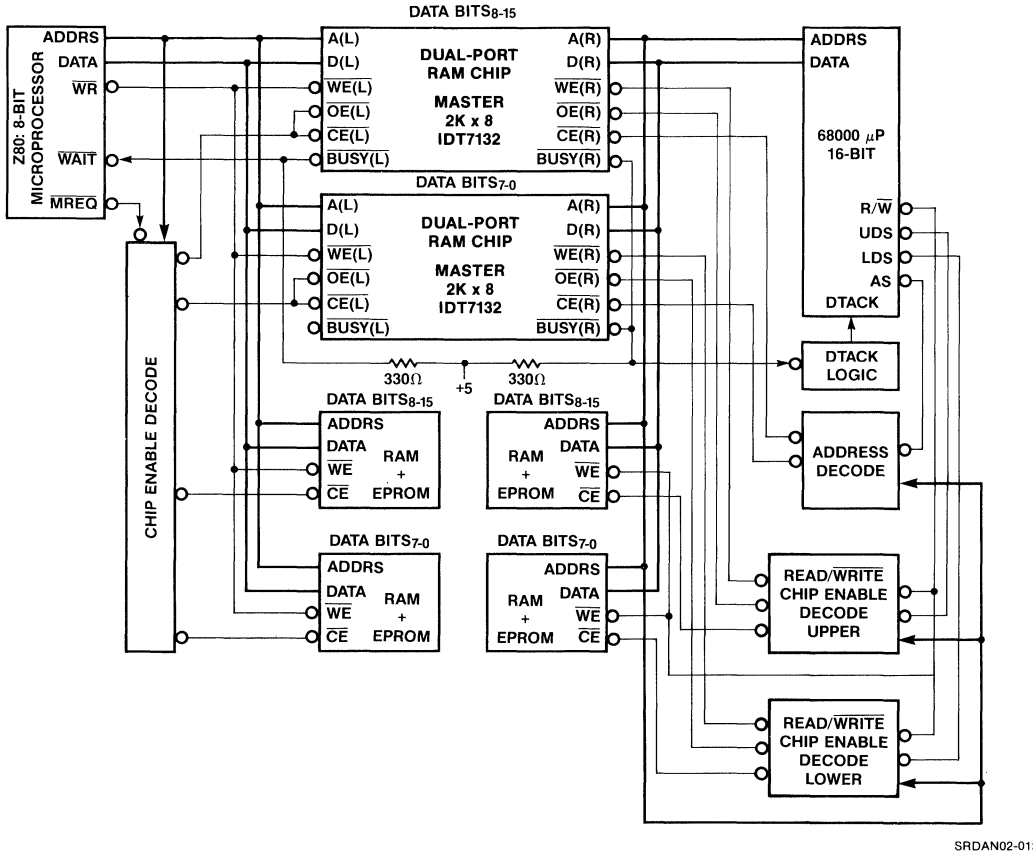

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Figure 13: 8-Bit to 16-Bit CPU Communication

SUMMARY AND CONCLUSION

The development of true dual-port memories in integrated circuit form provides the designer with the ability to set up communication between components fo a computer system while avoiding many of the problems of prior systems. While the concept of dual-port memory has been with us from the early days of computing in the form of DMA, the new dual-port ICs can provide this function at very high speeds and without the delays associated with earlier designs. Because of the utility of the dual-port memory concept, these chips should come into wide spread use and become one of the standard components used by the computer designer.

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TRUST YOUR DATA WITH A HIGH-SPEED CMOS 16-, 32- OR 64-BIT EDC

APPLICATION NOTE AN-03

By Suneel Rajpal and John R. Mick

INTRODUCTION

As a computer-science corollary to Parkinson's First Law, "Work expands to fill the time available," it is observably always true that "Computer software expands to fill the memory available." There is an insatiable demand for higher speed and denser memory, be it dynamic RAM or static RAM. However, there are reliability considerations that have to be made in large memory systems that must always provide correct data. This article deals with methods of enhancing data integrity and system performance by using Error Detection and Correction (EDC) logic circuits.

TYPES AND SOURCES OF ERROR

In memory systems, two types of errors can occur—hard errors or soft errors. A hard error is a permanent error and it occurs when a memory location is stuck-at-one or stuck-at-zero. A soft error is temporary, random and correctable. As these errors are non-recurring and non-destructive they can be corrected using EDC logic.

Hard errors are caused by factors such as interconnect failures, internal shorts and open leads. Soft errors can be caused by system noise, power surges, pattern sensitivity and alpha particle radiation. The charge of an alpha particle can become comparable to the charge on memory cells as geometries shrink. This implies that susceptibility to alpha particle radiation is likely to increase as memory densities increase; however, memory manufacturers try to reduce or eliminate the problem by design or packaging techniques.

In spite of that there is a probability of failure or error, especially where large systems are concerned. A graph that shows the trend of error rate versus chip density for dynamic RAMs is presented in Figure 1. One can calculate the Mean Time Between Failures (MTBF) for a DRAM system quite easily based on such data from a DRAM manufacturer.

A common method to examine data integrity is to incorporate parity. In a simple case of a three bit number and one parity bit, the following relationship exists as shown in Table 1.

TABLE 1

DATA	ODD PARITY
000	1
001	0
010	0
011	1
100	0
101	1
110	1
111	0

The odd parity is generated by an exclusive-NOR operation of the data bits. An error can be identified by taking the entire word and the parity bit, called a code, and performing an exclusive-OR operation. If the exclusive-OR result was a one, it indicates that the data was probably correct and the combination of the data and parity bits represent a valid code; "probably" is mentioned, and will be explained in the following lines. However, if the exclusive-OR result was a zero, then it can only be identified that an error occurred and the combination of the data and parity bits represent an invalid code.

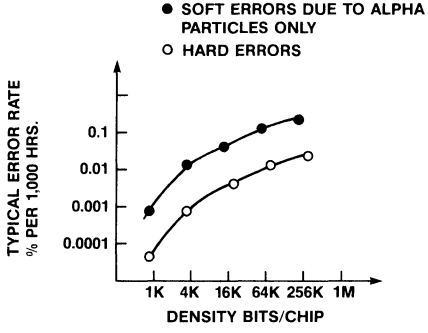

Figure 1: Typical Error Rates

Another interesting aspect of Table 1 is the fact that to go from one valid code, say 0001 to another valid code 0100, at least two bits have to change. This is called a distance of two. If only one bit changed on the code, it could be used to identify an error, but it could not point to the correct valid code. For example, if an invalid code of 0011 is seen, it lies between 0001 and 0010 and it is not possible to tell if the last data bit is in error or the parity bit is in error. Now, back to the mention of the word "probably." If two bits in the data changed erroneously, the parity tree performing the exclusive-OR would not be able to catch that kind of an error. Detection codes using parity are therefore limited and useful only in detecting one bit in error (or any number of odd errors), and they cannot provide any correction. Unfortunately, they cannot detect two errors (or any even number of errors).

The detection capability of the codes with different distances are shown in Figure 2. An invalid code that occurs in the distance of two cannot tell which bit was erring as outlined in the previous paragraph. Codes that keep a distance of three (or at least 3-bits have to change to go from one valid code to another) can detect single bit errors and also correct them. However, codes with a distance of three cannot detect two failing bits. As shown in the distance of three example, if a two-bit error occurs, it would be identified as if one bit failed. An invalid code associates detection/correction with the valid code adjacent to it rather than the other valid code that is a distance of two from it. Codes with a distance of four can detect all single-bit errors, detect all double-bit errors and also correct all single-bit errors. Double-bit errors are equidistant from two valid codes as shown by the central invalid code in Figure 2. The Single Error Correction and Double Error Detection (SECDED) capability is highly desirable for data integrity in high-reliability computer systems.

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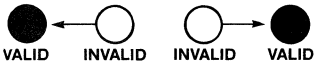
DISTANCE OF TWO — DETECTS SINGLE BIT ERRORS



DISTANCE OF THREE — DETECTS AND CORRECTS SINGLE BIT ERRORS

DISTANCE OF FOUR
— DETECTS AND CORRECTS SINGLE BIT ERRORS
— DETECTS DOUBLE BIT ERRORS

Figure 2: Codes of Various Distances and Their Effectiveness

EDC ICs TO THE RESCUE

Codes with a distance of four are used in the IDT39C60/ IDT49C460 Error Detection and Correction ICs. The overhead in the EDC implementation is additional check bits to the words in memory. For example, 6 bits are needed for 16-bit data, 7 bits for 32-bit data, and 8 bits for 64-bit data to generate a distance of four. The code formed is a catenation of the word bits and the check bits and, as in the parity case, the code can be valid or invalid. The valid codes are a distance of four apart from the next valid code. Valid codes are implemented by generating check bits based on the data word and writing the check bits with the data bits to the memory. On reading the data and check bits from memory, a possibly valid or invalid code could have been read. The determination of whether the code was valid or not is done by regenerating check bits using the data bits; these are compared (ex-ORed) to the check bits that were read and the result is syndrome bits. These syndrome bits are indicative of an error-free situation, or a single or double-bit error, and are used to determine validity of a code, and also to point to single-bit errors and identify the occurrence of two or more bits in error.

As an example, let us write $(FFFF)_H$ as the data word. The corresponding check bits that will be written in the memory are 001100 and can be computed using Table 2 which is based on a modified Hamming code. On reading back, if the data was FFFE and the data in position 15 had erroneously flipped from a "1" to a "0". The regenerated check bits would be 000111 (based on FFFE). The syndrome bits are the ex-OR of the two sets of check bits and are 001011. Referring to Table 3, a syndrome of 001011 indicates bit 15 is in error and has to be flipped.

The internal hardware of the IDT39C60 16-bit EDC, shown in Figure 3A, consists of ex-OR trees that can generate check bits and syndromes and also contains hardware to correct data. In addition, two or four IDT39C60s and some SSI, MSI can be connected to form 32-bit or 64-bit EDC systems. The IDT39C60 is a functional and pin-compatible replacement of the 16-bit 2960, and runs at a quarter of the power. Faster versions, such as the IDT39C60-1 and the IDT39C60A (the IDT39C60-1 replaces the Am2960-1 and the IDT39C60A is the fastest 16-bit EDC available), demonstrate that CMOS circuits can not only run cooler than their equivalent bipolar circuits, but also run faster with higher output drive.

The architecture of a 32-bit EDC, the IDT49C460, is shown in Figure 3B. The IDT49C460 provides efficient means of generating check bits, calculating syndrome bits and correcting data bits on a 32-bit data path. In addition, diagnostic capability is provided to verify data operations in the memory system and verify that the EDC IC is functional too.

TABLE 3: SYNDROME DECODE TO ERROR LOCATION/TYPE

SYNDROME BITS			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = Number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

TABLE 2: 16-BIT MODIFIED HAMMING CODE CHECK BIT GENERATION

GENERATED CHECK BITS	PARITY	PARTICIPATING DATA BITS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

Figures 4A and 4B show the dataflow for the generate and error detect/correct operations in the IDT49C460. In Figure 4A, check bits based on input data are generated by the EDC and are written to the check-bit memory along with the data. In Figure 4B, the data and check bits are read from the memory. Based on their values the syndrome bits are generated inside the IDT49C460. If the EDC is in the correct mode, any single-bit error is corrected and the corrected data is placed in the output data latch. The syndrome bits are also available if error logging is done.

Another necessary operation that is required is byte handling. When the memory is organized as a 32-bit word and an 8-bit update is being performed, it requires a 2-step operation. The first step is to read the 32-bit data and check bits, and correct any erroneous single bit failure. The second step is to write the new byte with the three unmodified bytes back to the system memory. The check bits corresponding to the newly formed 32-bit word are generated and also written to the memory. This operation is supported by having four separate output byte enables in the IDT49C460. The two-step process is shown in Figures 5A and 5B.

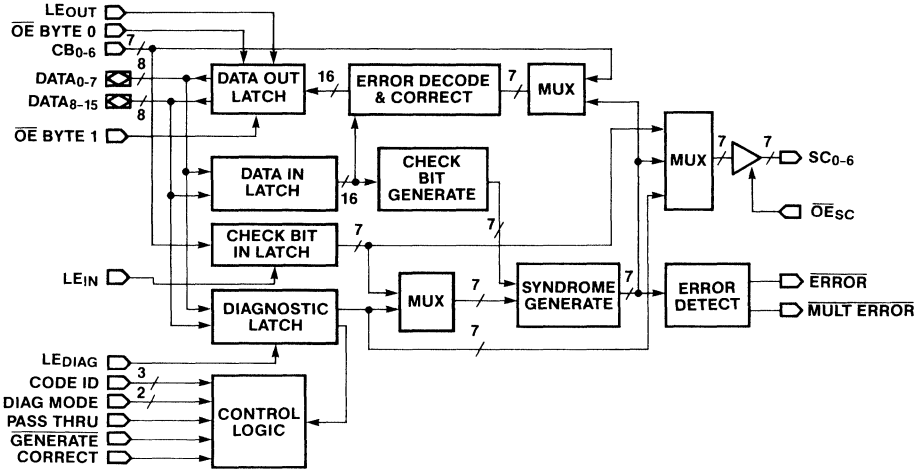


Figure 3A: The IDT39C60/-1/A 16-Bit EDC Architecture

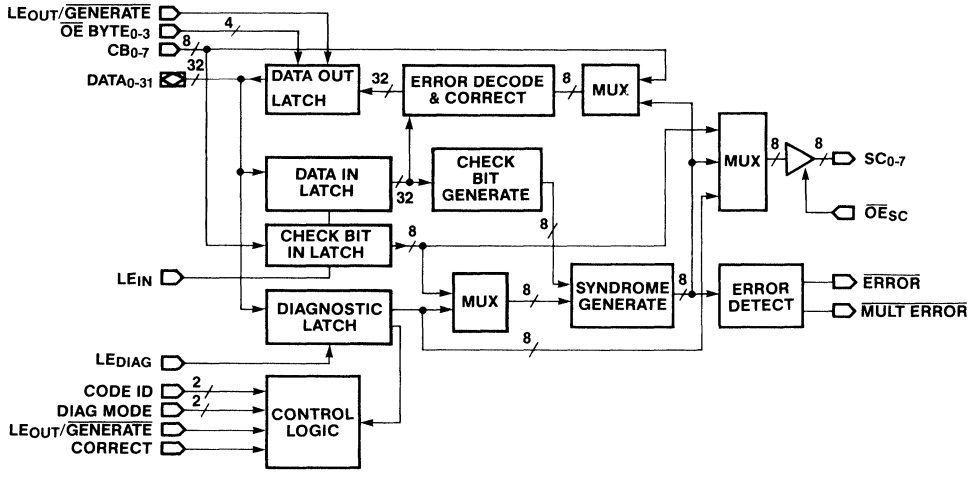


Figure 3B: The IDT49C60/A 32-Bit EDC Architecture

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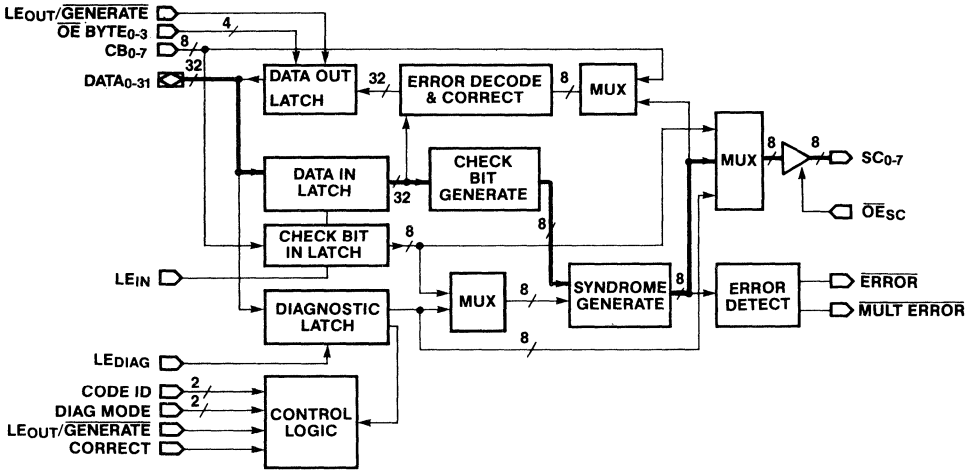

Figure 4A. Check Bit Generation in the IDT49C460

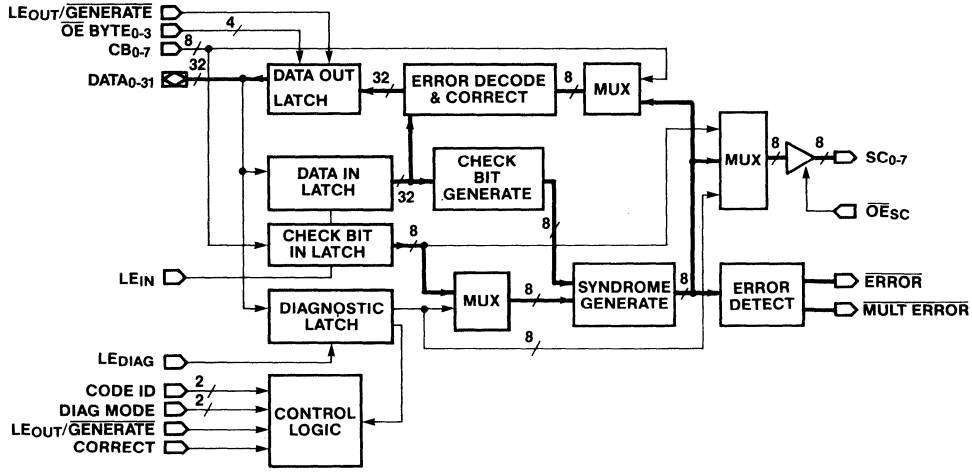

Figure 4B. Error Detection and Correction Data Flow in the IDT49C460

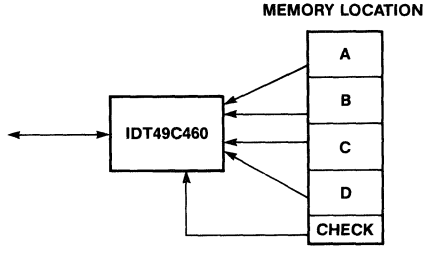

Figure 5A. Byte-Write Operation; Step 1. Read 32-Bit Word and Correct Any Single-Bit Error

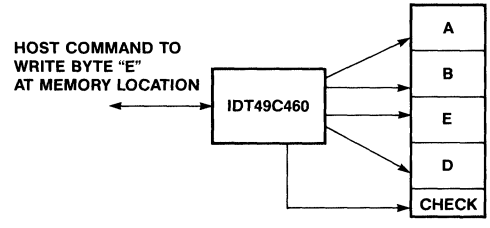

Figure 5B. Byte-Write Operation, Step 2: Newly Generated Check Bits Corresponding To Bytes A, B, E, and D Are Written To Memory Along With Bytes A, B, E, and D

The IDT49C460 is expandable to 64-bit wordlengths as shown in Figure 6A. The external buffer may not be required if the path from the memory already has a three-state buffer in its output stage or externally in the data path to the EDC. Figure 6B shows a 2-step operation when an error detection and correction occurs in bit 32-63 of the 64-bit word. The IC on the first level, with the code ID=10, receives the data bits 0-31 and the entire check bits. In the example shown, bit 63 has erroneously flipped from a "1" to a "0". The partial syndrome bits are passed from the first device to the second. (The actual syndrome bits are generated from a table not shown in this article but are in the IDT49C460 data sheet.) The check input latch of the second device is open, due to its code ID=11, and the partial syndrome bits are combined with the data bits to generate the final syndrome bits. The final syndrome bits indicate that bit 63 is in error and it is inverted to produce a correct result. The final syndrome bits are also sent back to the first device, but the resulting syndrome does not alter any data bits in the first device. Therefore, the error correction is a 2-step process. In Figure 6C, an error occurs in bits 0-31. In this case, the partial syndrome is sent to the second device. The second device generates the final syndrome and sends it back to the first device. Finally the erroneous bit is flipped over. In this case, a 3-step operation takes place.

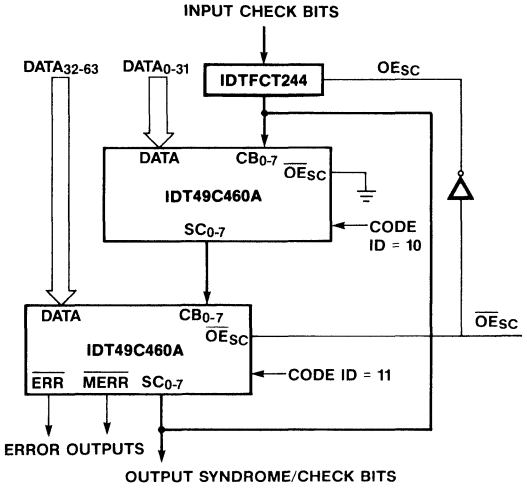

Figure 6A. The IDT49C460 In A 64-Bit Configuration

DATA	CHECK		
FFFFFFFFFFFFFFFF	30	WRITE	
FFFFFFFEFFFFFFFF	30	READ	
CODE=10 FFFFFFFE(BITS 0-31)	30(INPUT CHECK BITS)		STEP 1
	2F(PARTIAL SYNDROME)		
CODE=11 FFFFFFFF(BITS 32-63)	2F(PARTIAL SYNDROME)		STEP 2
FFFFFFFF(BITS 32-63)	2F(FINAL SYNDROME)		
CODE=10 FFFFFFFF(CORRECTED BITS 0-31)	2F(FINAL SYNDROME)	—	STEP 3

Figure 6C. Error Correction On A 64-Bit Word, With Error in Bits 0-31

DATA	CHECK		
FFFFFFFFFFFFFFFF	30	WRITE	
FFFFFFFFFFFFFFFE	30	READ	
CODE=10 FFFFFFFF(BITS 0-31)	30(INPUT CHECK BITS)		STEP 1
	00(PARTIAL SYNDROME)		
CODE=11 FFFFFFFE(BITS 32-63)	00(PARTIAL SYNDROME)		STEP 2
FFFFFFFF(CORRECTED 32-63)	AE(FINAL SYNDROME)		
CODE=10 FFFFFFFF(UNCHANGED 0-31)			

Figure 6B. Error Correction On A 64-bit Word, When Error Is In Bits 32-63

HOW THE IDT49C460 FITS IN A SYSTEM

By virtue of their function, EDC ICs tie in closely with system memory architectures. Figure 7 shows a host that generates addresses and accesses a memory system. The memory contains memory elements, error detection logic and interface circuits. These are needed to start a memory cycle, to send/receive data on the system bus, and to inform the host that it has completed the memory operation.

One may use EDC for dynamic RAM memories or static RAM memories. Figures 8A and 8B show general configurations for DRAM arrays. Normally, in DRAM systems, separate pins exist for the $DATA_{OUT}$ and $DATA_{IN}$. Therefore, IDTFCT244s can be used to provide an isolation between the DATA port of the EDC and the $DATA_{OUT}$ from the RAM. This isolation may be required after a read operation, and the EDC provides corrected data to the system and the DRAM. Another buffer is needed between the DATA port of the EDC and the system data bus to allow the corrected data to be placed on the system bus. The DRAM controller can be implemented using standard off-the-shelf products. An important operation that has to be supported is byte or word handling. The IDT49C460 EDC configuration shown in Figure 8A has four individual byte enable controls going to the IDTFCT244s and their complements to the IDT49C460. The IDT39C60 shown in Figure 8B has two individual byte controls to the IDTFCT244s and their complements going to the IDT39C60.

In static RAM systems, as shown in Figure 9, there is no need for a dynamic memory array controller; however, bidirectional buffers are required on the ports of the static RAMs as RAMs have common I/O lines for data. If the SRAMs had separate I/O pins for the data, the buffer configuration of the DRAM array could be used.

The timing controller, common to both DRAM and SRAM systems, controls the buffers and the EDC ICs. This is an interesting task to the memory system designer, as a choice of EDC architectures are available.

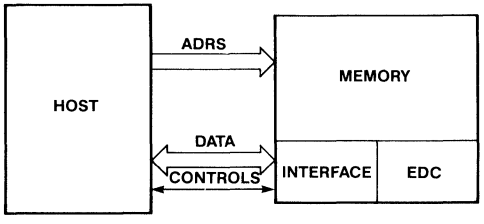

Figure 7. A Typical High-Reliability Memory System

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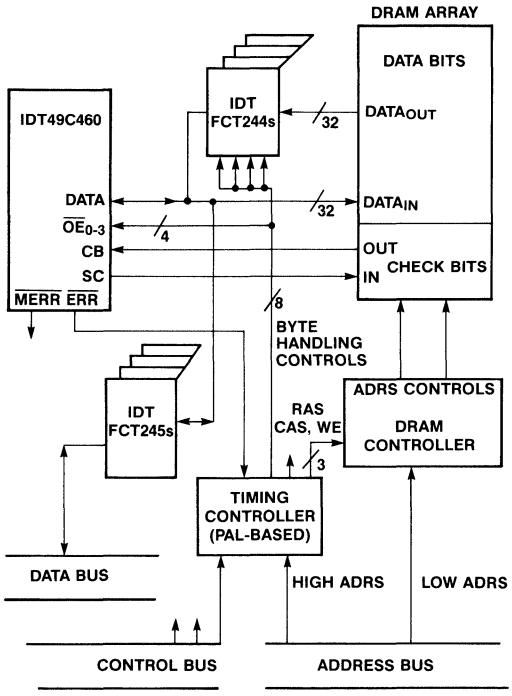

Figure 8A. EDC Logic In 32-Bit DRAM-Based Memory Systems

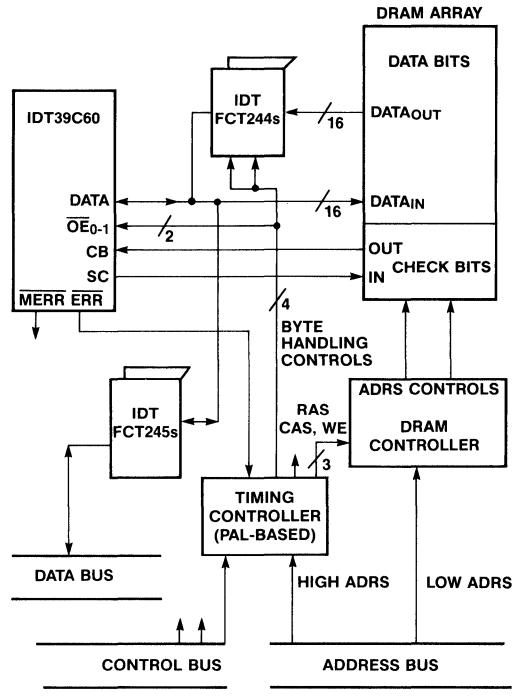

Figure 8B. EDC Logic In 16-Bit DRAM-Based Memory Systems

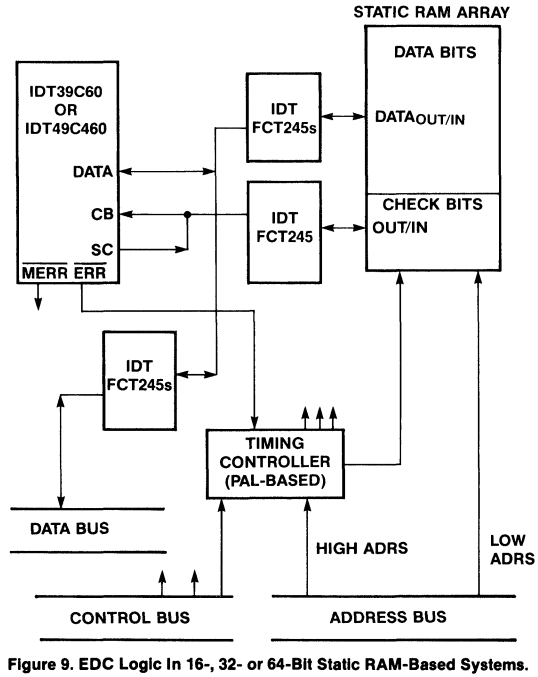

Figure 9. EDC Logic In 16-, 32- or 64-Bit Static RAM-Based Systems.

BUS-WATCH AND FLOW-THROUGH EDC ARCHITECTURES

The architecture of EDC ICs can be categorized as Bus-Watch and Flow-Through as shown in Figure 10. In a bus-watch architecture, there is only one bus to handle the data and one set of pins that handle incoming data from the memory, corrected data from the EDC, and incoming data from the system to be written to the memory. The IDT39C60 and IDT49C460 are based on a bus-watch architecture. In a flow-through architecture, such as Intel's 8206, there are two ports that handle data movement. The WD_{IN}/D_{OUT} handle incoming data from the system, so that the EDC can generate check bits. The second function of the WD_{IN}/D_{OUT} is to supply the corrected data to the system and the memory. The second set of pins, D_{IN}, only handle incoming data from the RAM. These architectures lend themselves to "Check Only" and "Correct Always" configurations.

The "Check Only" method is used in high-performance systems. The memory system always sends data directly to the host when a read is requested. In the event a single bit error occurs, one approach is that the read cycle is delayed and a correction is performed. The corrected data is sent to the host and written into the memory. In this case, the timing control circuit would disable the Memory Data Out Buffer (the IDTFCT244 for the DRAM case and the IDTFCT245 for the static RAM case) and put corrected data from the EDC IC onto the system data bus, also writing the corrected data back into the memory array. For the "Check Only" method, the DATA TO $\overline{ERR}$ parameter is of key concern to designers as this can be used to generate the DTACK, READY or BERR signals to the host.

The other option is that a "Correct Always" method is used. In this case, the EDC always corrects data (regardless of the fact that it may be error-free), sends it on the system data bus and writes it back to the memory. In this case, the cycle time for the data read includes the "$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$" parameter for the EDC. The IDT49C460 and the IDT39C60 provide the fastest timings for the "$DATA_{IN}$ TO $\overline{ERR}$" and "$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$" parameters when compared to other currently available 32-bit and 16-bit EDCs. This was made possible by using IDT's CEMOS™ II 1.2μ process.

The IDT49C460A dissipates only 95mA and the IDT39C60A dissipates only 85mA over the commercial temperature range. The quiescent power consumption is only 5mA for the IDT49C460A and the IDT39C60A.

The delay for the $DATA_{IN}$ TO $\overline{ERR}$ is only 30ns for the stand-alone 32-bit IDT49C460A (worst case commercial) and is 46ns for the 64-bit cascaded case. The delay for the $DATA_{IN}$ TO CORRECTED $DATA_{OUT}$ is only 36ns for the stand-alone case and 63ns for the 64-bit cascaded case. These parameters are very important when considering EDC ICs discussed further in a later section. They are, however, shown in Tables 4 and 5 for the 16-bit IDT39C60 and 32-bit IDT49C460, respectively.

The acid test is how a flow-through architecture compares in performance to a bus-watch architecture in the "Check Only" mode and the "Correct Always" mode. In Figure 11, a flow-through EDC device is connected to a DRAM array system for "Check Only" operations. Data from the memory goes through the IDTFCT244 buffer to the system bus directly and simultaneously to the EDC device. Within the $DATA_{IN}$ TO $\overline{ERR}$ of the device, it is determined if a single-bit error occurred and, if so, a timing controller would disable the IDTFCT244 and allow corrected data to be sent on the system bus via the IDTFCT245.

A bus-watch EDC in a "Check Only" configuration is shown in Figure 12. The data path from the DRAM to the EDC goes through one IDTFCT244 delay and is identical to the flow-through case. After that the $DATA_{IN}$ TO $\overline{ERR}$ delay determines whether or not the cycle would be stretched. The data from the DRAM goes through a IDTFCT244 buffer and an IDTFCT245 buffer in the bus-watch case. One emerging fact is that the time it takes to make a decision to stretch a memory cycle is the same for bus-watch and flow-through EDC parts and is determined by the $DATA_{IN}$ TO $\overline{ERR}$ of the respective devices.

In the flow-through "Correct Always" configuration, as shown in Figure 13, data has to always pass through the EDC and any IDTFCT245 and on to the system bus. In the case of bus-watch ICs, data from the DRAM goes through an IDTFCT244, in and out the EDC device and through an IDTFCT245 as shown in Figure 12. A bus switch has to take place every cycle as memory data comes into the EDC, is corrected and then transferred to the system bus. In a practical design this bus switch may be the longest delay path for "Correct Always".

TABLE 4:
KEY PARAMETERS FOR THE IDT39C60/-1/A FOR COMMERCIAL RANGE

	IDT39C60	IDT39C60-1	IDT39C60A
$DATA_{IN}$ TO $\overline{ERR}$	32ns	25ns	20ns
$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$	65ns	52ns	30ns

TABLE 5:
KEY PARAMETERS FOR THE IDT49C460/A FOR COMMERCIAL RANGE

CONDITIONS	IDT49C460	IDT49C60A	2-49C460As FOR 64-BIT EDC
$DATA_{IN}$ TO $\overline{ERR}$	40ns	30ns	46ns
$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$	49ns	36ns	63ns

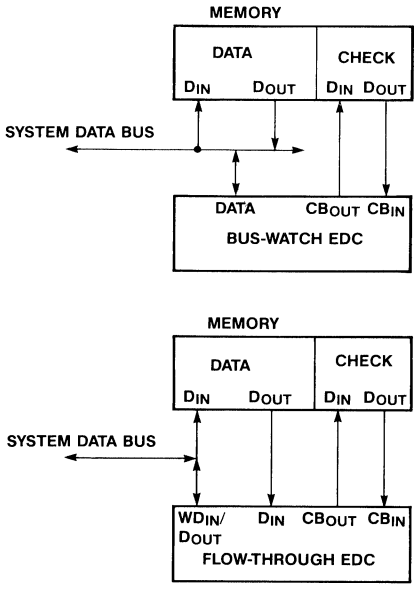

Figure 10. Architecture Of Bus Watch And Flow-Through EDC Logic

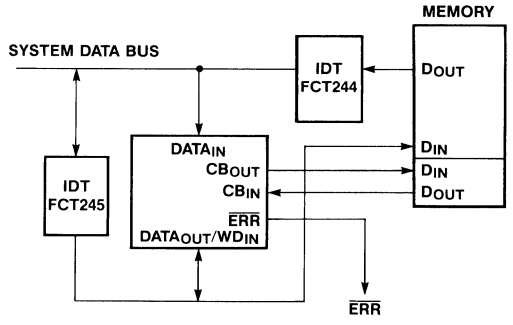

Figure 11. The "Check Only" Configuration for Flow-Through EDC ICs

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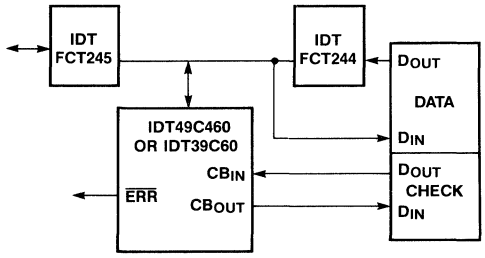


Figure 12. The Bus-Watch EDC In "Check Only" Or "Correct Always" Configurations

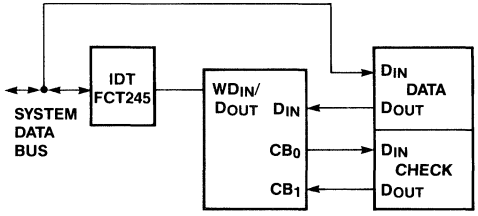
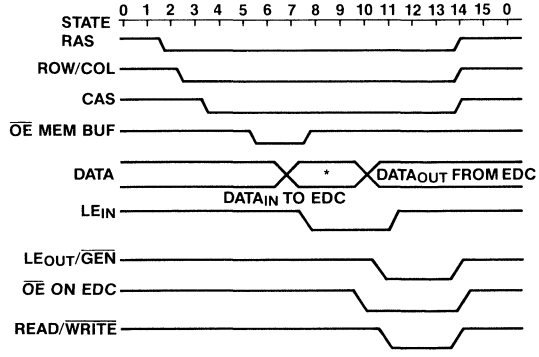


Figure 13. A Flow-Through EDC In "Correct Always" Mode

However, if just the specification is being reviewed, the flow-through path is shorter by an IDTFCT244 delay. A specification comparison is that the "$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$" delay of a flow-through EDC part should be compared to the "$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$" delay of the IDT49C460/A, plus an external 7ns buffer delay (for the IDTFCT244). However, in an actual system such as the one in Figure 8A, a "bus-switch" has to take place, as explained below.

In a DRAM system that has a bus-watch EDC, a sequence of events has to be created by the timing controller that was shown in Figure 8A. The timings that the controller generates are shown in Figure 14. The example being considered is "Correct Always." The RAS, CAS, WE signals have to be generated to read data from the DRAM. The read takes place before state 7, and the read data is latched in the $DATA_{IN}$ latch of the EDC. It is then corrected and the corrected data can be latched in the $DATA_{OUT}$ latch. The data correction can take place between states 7 and 10. Any time after state 10, the EDC can place the corrected data on the bus. The bus that was loading the data in the EDC has to be turned around as the EDC is going to send corrected data to the host. The EDC also writes back the corrected data and the newly generated check bits to the memory. The memory buffers shown in Figure 8A are three-stated, as the $\overline{OE}$ MEM BUFF are high from state 7 onwards and the EDC would be enabling data on the bus. The timing diagram in Figure 14 explains a typical case and users will have to customize it based on their memory speeds and the time the system has for receiving valid data.

Other factors that may be a consideration are package count and board space. The number of packages used in flow-through and bus-watch implementations are the same for "Check Only" configurations. In "Correct Always" configurations the bus-watch implementation requires four more IDTFCT244s than the flow-through implementation. Flow-through ICs have more pins and therefore leave a larger footprint on the PC. However, in terms of board space, since the footprint of the flow-through EDC is larger than the bus-watch, the bus-watch approach takes less space for "Check Only" configurations and there is a tie for the "Correct Always" configuration.



*NOTE: A BUS-SWITCH TAKES PLACE BETWEEN STATES 6 AND 10

Figure 14: Timing Diagram For Correct Always In Figure 7A

SUMMARY

This article has covered reliability issues in memory systems and solutions using EDC devices. In considering EDC devices, two parameters are critical: the "$DATA_{IN}$ TO $\overline{ERR}$" and the "$DATA_{IN}$ TO CORRECTED $DATA_{OUT}$". At Integrated Device Technology, we have optimized these two parameters and produce ultra fast, TTL-compatible CMOS Error Detection and Correction devices for high performance 16-, 32- and 64-bit systems.

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Integrated Device Technology Inc

HIGH-SPEED CMOS TTL-COMPATIBLE NUMBER-CRUNCHING ELEMENTS FOR FIXED- AND FLOATING-POINT ARITHMETIC

APPLICATION NOTE AN-04

by Suneel Rajpal

INTRODUCTION

Traditionally, high-speed number-crunching requirements could only be fulfilled by bipolar (TTL) components. However, with the advent of advanced CMOS technologies, one can not only attain higher densities and lower power consumption, but also attain higher speeds. This paper deals with different building blocks that can be used to build integer or floating-point processors at speeds greater than 10MHz.

FIXED-POINT PROCESSORS

In order to build a high-speed efficient fixed-point processor, a number of computational elements are required. A high-speed ALU and a multiplier are all integral parts of a high-speed processor. These building blocks must be cascadable or expandable for higher-precision numbers. High-speed memories are also required for data storage and for control store which essentially drives the system. A typical microcoded system is shown in Figure 1. It consists of three sections: the control section, the address generation section and the number-crunching section. The key elements in the control block and number-crunching block, shown in Figure 1, are illustrated in Figures 2 and 3. (The address generation can be supported by the architecture in Figure 3.) An instruction is fetched from the main memory (not shown). Then the opcode is decoded to cause a jump to the appropriate address in the control store. This address is the start address of the microinstructions that emulate the macroinstruction.

The next step may be to fetch the operands; this is done by putting the address on the address bus and bringing data into the data input registers. If more parallelism is required, a separate ALU can be used to compute addresses concurrently with an ALU that is computing data from the previous instruction.

Figure 2 contains the microprogram sequencing and the control store section. This typically consists of a microprogram sequencer, a control store, pipelines, registers, and some MSI for condition code selection. The IDT39C10B is a 12-bit microprogram sequencer that is plug-compatible with all versions of the 2910. One of four sources can be selected as the next address: the microprogram address register, the LIFO stack, the internal register/counter, or the direct D input. An added feature in the IDT39C10 is the deeper stack with 33 locations instead of nine provided by the 2910 sequencer. Figure 3 shows a plausible arrangement of ALUs, multiplier/ multiplier-accumulators and extended data storage. A computation for worst-case cycle time for the control path is shown in Figure 4. The corresponding worst-case delay for the data path is shown in Figure 5. It is an interesting exercise to analyze these two delay paths. The control path has a 64ns delay and the data path has a 49ns delay, adding to the IDT49C402 delay and register propagation delay and set-up time. The IDT49C402, shown in Figure 6, is code-compatible

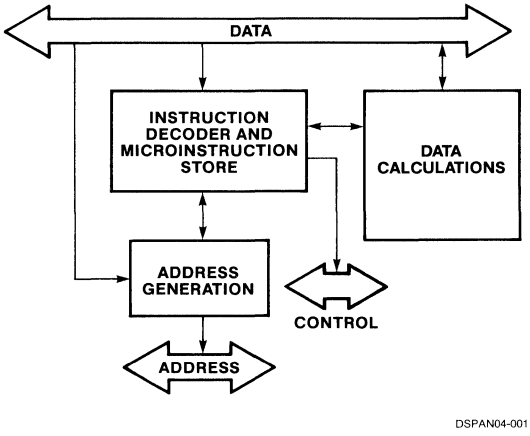

Figure 1. A Typical CPU

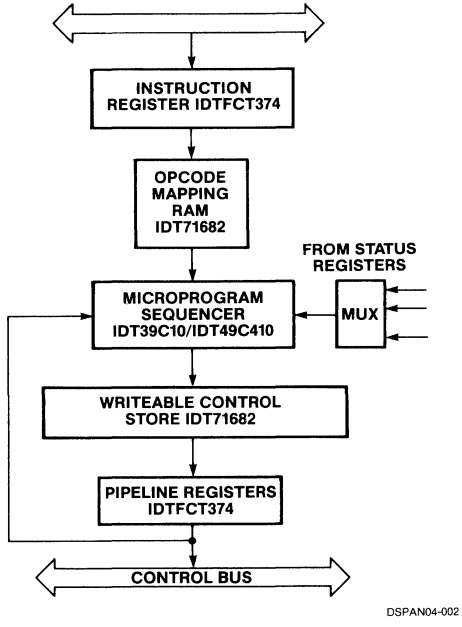

Figure 2. The Instruction Decoder and Microprogram Sequencer

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to the 2901 and has 64 registers in the register file. There are eight additional destination functions that allow direct loading of the Q register or the RAM, thereby enhancing the overall performance. The additional destination functions are shown in Table 1.

If multipliers are used in the data path, the pipelined delay of 35ns for the IDT7216/IDT7217 (16 x 16 multipliers) is far less than the sequencer delays and ALU delays. The other data path of concern is a multiplier output that is added in the IDT49C402, shown as Path 2 in Figure 5. It is only 45ns, less than both the Data Path 1 delay and the Control Path delay. The IDT7216 is pin and functionally compatible to the TRW MPY-016H/K and Am29516. The IDT7217 is pin and functionally compatible to the Am29517. If a multiply-accumulate function is required, an IDT7210/IDT7243 (16 x 16 MACs) can provide sum-of-products at 35ns clocked speeds. The IDT7210/IDT7243 are pin and functionally compatible to the TRW TDC1010/1043 multiplier-accumulators. Generic block diagrams for the multipliers and multiplier-accumulators are shown in Figures 7 and 8.

The multipliers operate on unsigned two's complement or mixed mode numbers. In every clock cycle, a 32-bit product is generated and either the least significant or the most significant half can be read through the output lines. The least significant of the product is also shared with the Y_{0-15} input lines. IDT7216/IDT7217s are capable of running at 35ns clocked multiply rates over the commercial temperature range and 40ns over the military temperature range.

The multiplier-accumulator, IDT7210, provides the multiply, multiply-add and multiply-subtract functions. Three bits of overflow are provided, corresponding to a 35-bit accumulator. The IDT7243 is a trimmed version of the IDT7210 that does internal accumulates of 35 bits; but only the most significant 19 bits are available externally. Also, the IDT7243 has no preload capability. The multiply-accumulate operations can run at 35ns clocked speeds for the commercial temperature range. The summarized performance is shown in Table 2.

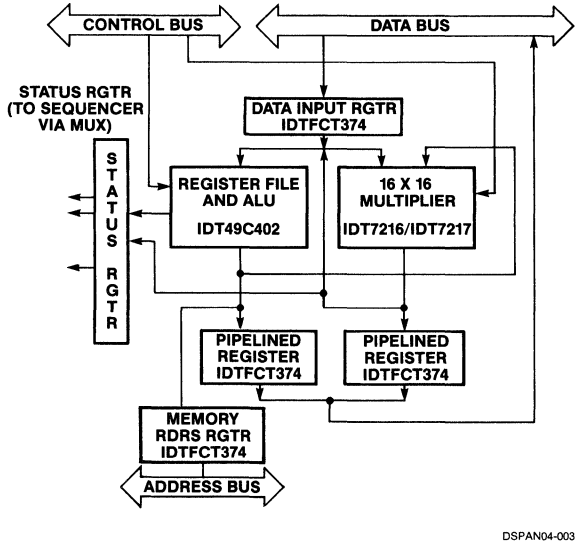


Figure 3. The Address and Data Calculations Unit

Blazing fast speeds of the multipliers are needed in systems where the operands are of longer wordlength (>16 bits). For example, if fixed-point 32-bit operands are to be multiplied, four partial products have to be added, as shown in Figure 9. The four partial products can be generated in parallel using four multipliers and adding the partial products at their appropriate binary weighting. Alternately, the partial products can be added using one multiplier while doing shift and add operations in the IDT49C402, using the register space efficiently.

Pipeline register CLK-Q	10ns
Condition MUX (74F251)	13ns
IDT49C410: CC to Y	16ns
WCS RAM; IDT71682	25ns
Pipeline Register Set-Up	2ns
Total	64ns

Figure 4. The Control Path Delay

Pipeline register CLK-Q	10ns
IDT49C402:A/B to F = 0	37ns
Status Register Set-Up	2ns
Total	49ns

CLK-Q, IDT7216/IDT7217	25ns
Data to RAM, Set-Up	20ns
Total	45ns

Figure 5. The Data Path Delay

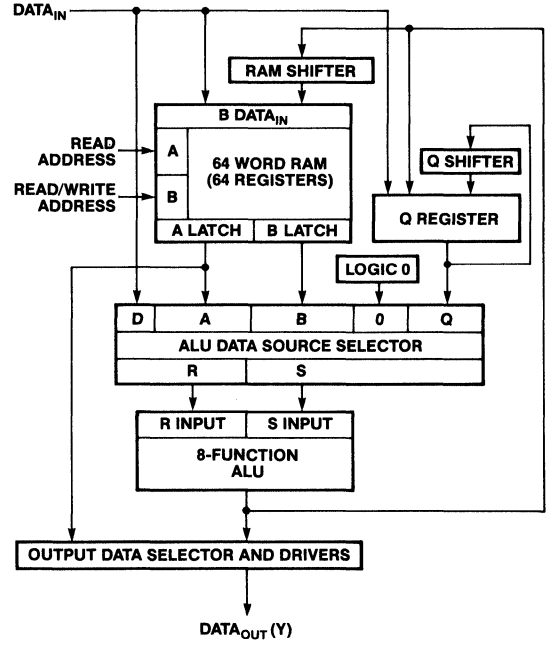
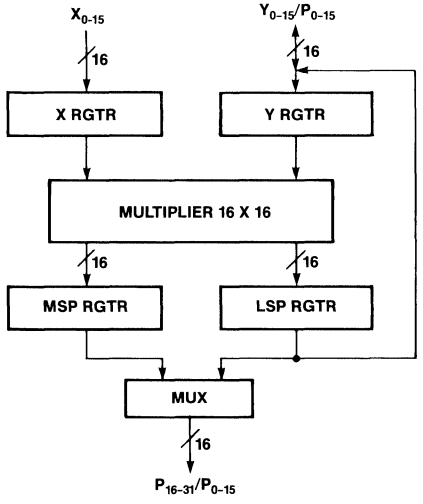


Figure 6. The IDT49C402 Block Diagram

In the example shown in Figure 9, the partial product XA·YA is stored in two locations of the register file. The Most Significant (MS) part of XB·YB is added to the Least Significant (LS) part of XA·YB; the carry-out is saved for the next addition to the LS part of XB·YA. The carry-out again is saved for the next operation for the additional of the MS part of the XB·YA and XA·YB. This result is added to the LS part of XA·YA. Finally, the sign extension of the previous operation is added to the MS part of XA·YA. By using the register file of the IDT49C402 efficiently, one does not have to perform 16-bit shifts with each partial product addition, resulting in a fairly efficient 32 x 32 multiplication.

A high-speed 12MHz fixed-point processor can be built using the parts shown in Figures 2 and 3—namely the IDT39C10 12-bit sequencer or the IDT49C410 16-bit sequencer, the IDT49C402 16-bit ALU, the IDTFCT374, the IDT71682 RAMs, the IDT7216/IDT7217 multipliers or the IDT7210/IDT7243 multiplier-accumulators.



**IDT7216 HAS SEPARATE CLOCKS FOR THE REGISTERS.
IDT7217 HAS A COMMON CLOCK AND SEPARATE ENABLES.**

DSPAN04-007

Figure 7. The IDT7216/IDT7217 Multiplier Block Diagram

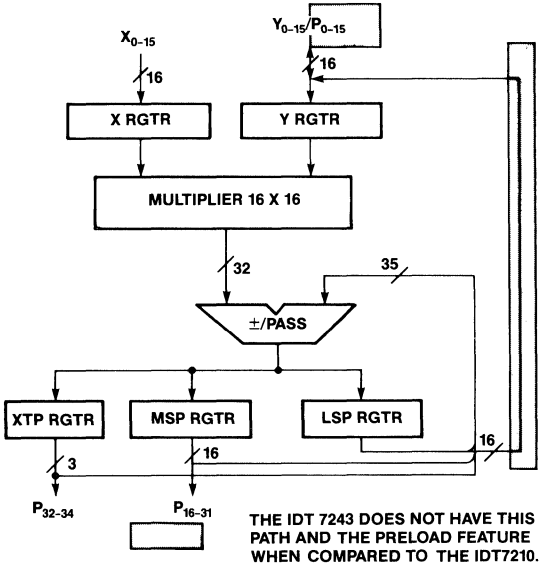


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Figure 8. The Block Diagram of the IDT7210/IDT7243

FLOATING-POINT PROCESSORS

In applications that need a larger dynamic range, floating-point number representation is used. A discrete solution to a 32-bit floating-point processor can be at least one board of SSI and MSI. Most designers prefer an IC or an IC set that implements the IEEE standard over a discrete solution. The implementation problem only worsens for double precision 64-bit floating point processors. The IDT72064/IDT72065 and IDT72264/IDT72265 provide compact, low-powered high-speed solutions to single-, and double-precision IEEE standard 754 version 10.0 calculations.

The IDT72064/IDT72264 are floating-point multipliers; the IDT72065/IDT72265 are floating point ALUs. All the parts have similar I/O structures. Data input and output transfers may occur at twice the maximum pipeline rate, allowing the devices to be used in a variety of bus configurations without degrading performance. The detailed block diagram of the IDT72264 is shown in Figure 10. The detailed block diagram for the IDT72265 is shown in Figure 11. Note that, in Figure 10, the IDT72264 takes two cycles for 32-bit operations and four cycles for 64-bit operations. The IDT72064, very similar to the IDT72264, takes four cycles for a 32-bit operation and eight cycles for a 64-bit operation.

The multiplier and ALU can operate in two modes: one with pipelined levels and the other with the pipelined registers made transparent (called the flow-through operation in the data sheets). For example, the multiplier in Figure 10 can have the following registers made transparent: PIPE1 and the STREG (Status Register), DM and DL registers. This allows the operands to "ripple" through the logic circuitry at a slower time, as compared to the pipelined case. A similar configuration is possible for the ALU,

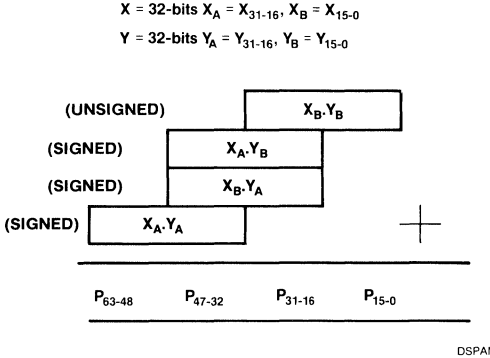

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Figure 9. Partial Products for a 32 x 32 Multiply

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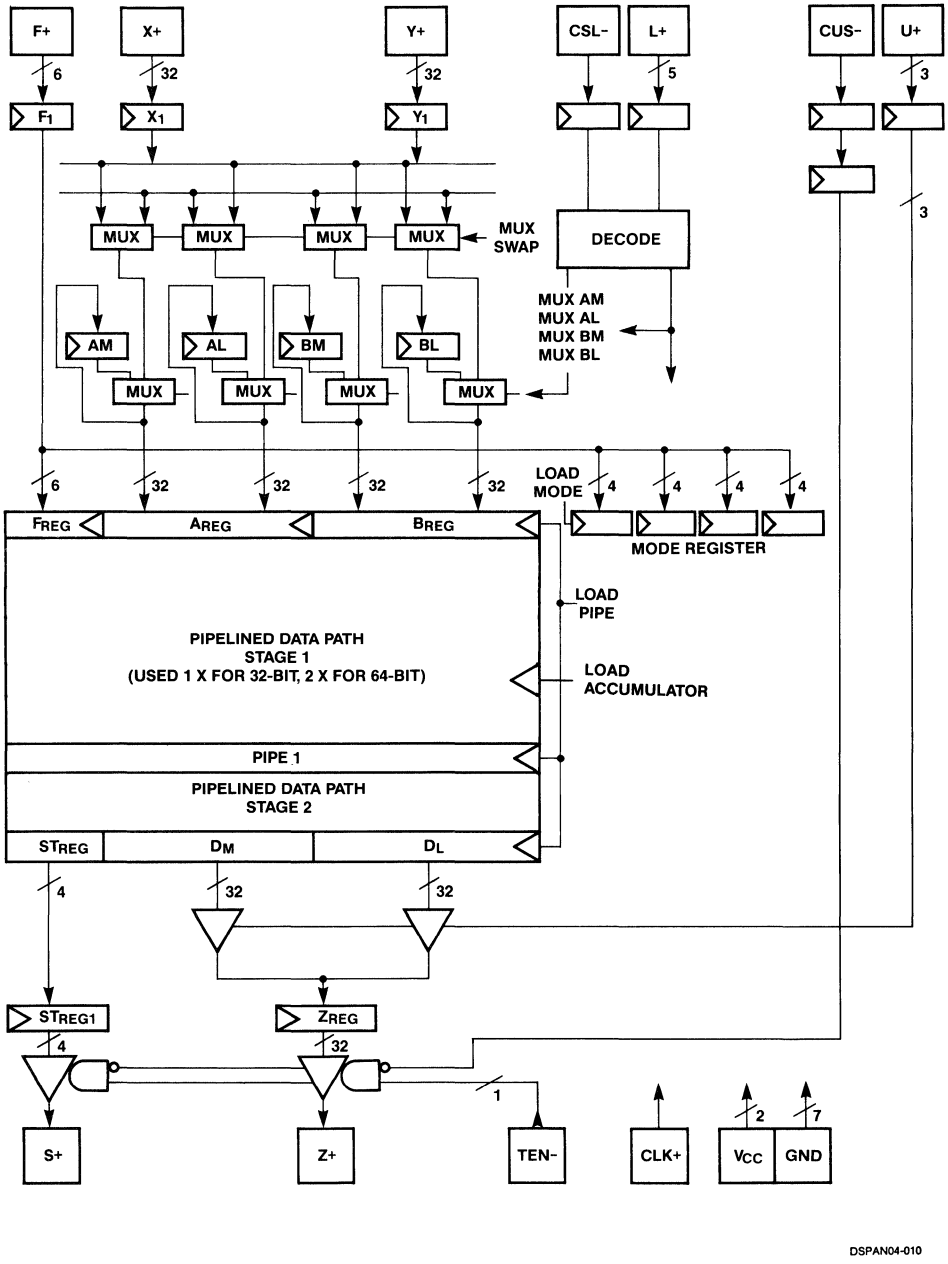

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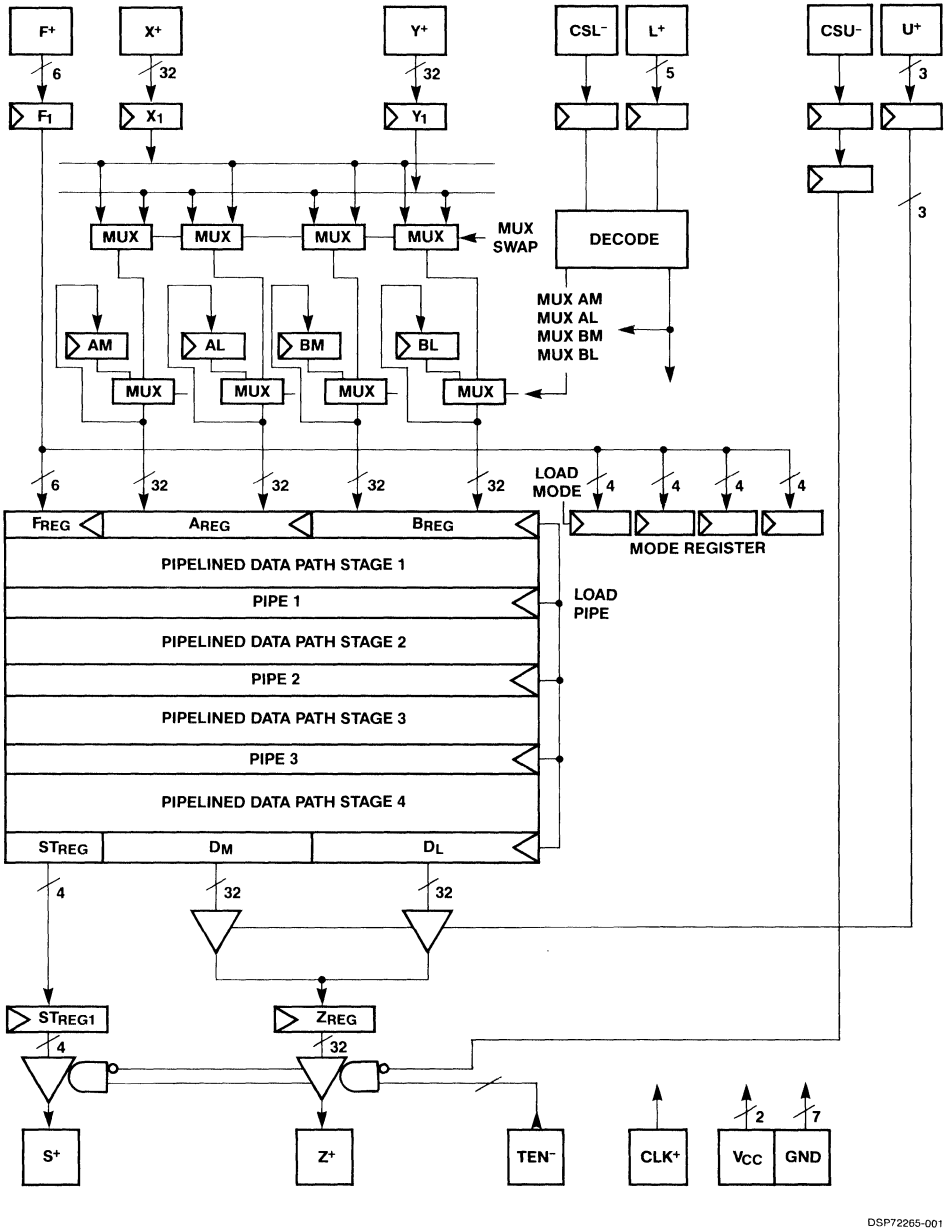
Figure 10. The IDT72264 Floating-Point Multiplier



DSP72265-001

Figure 11. The IDT72265 Floating-Point ALU

shown in Figure 11, where the following registers can be made transparent: PIPE1, PIPE2, PIPE3, and STREG, DM and DL registers. The tradeoff in using pipelining is that one result is available every (pipeline) cycle once the pipe is full. Often this is a preferred method of computing if the pipe is not flushed. In the flow-through situation, one does not present any new operands to the inputs during the duration of the operating time. In a pipelined system, new values of X and Y are loaded every cycle and new results are read every cycle, with an understanding that the result being read currently is from operands loaded "n" cycles ago. "N" depends on the operation being performed and can range from 6 to 14.

The input stage allows easy interfacing to 16-bit, 32-bit, and 64-bit buses. The instruction set of the multipliers include single- and double-precision multiply and handling of wrapped multiply. A wrapped number is one that is smaller than the smallest representable number that is normally used. The ALU has a wide variety of instruction including add, subtract, convert, compare, negate, pass, wrap and unwrap for both single-precision and double precision operands.

The performance for these devices for the pipelined and flow-through operations are listed in Tables 3 and 4. These timings are based on a 50ns clock time. The IDT72064 and IDT72065 are compatible with Weitek's 1064 and 1065 in the IEEE mode. The IDT72264 and IDT72265 replace Weitek's 1264 and 1265. The performance is expected to be 20% faster when compared to currently available Weitek parts.

TABLE 1.
IDT49C402 16-Bit ALU Destination Functions

	RAM	Q	Y-OUT
	F-Up	Q-Up	F
	F-Up	—	F
2901	F-Down	Q-Down	F
Functions	F-Down	—	F
(3-Bits	—	—	F
I_6-I_8	—	Load F	F
	Load F	—	F
I_9 HIGH	Load F	—	A
	Load D	Load F	F
	Load D	Load F	A
Added	Load F	Load D	F
IDT	Load F	Load D	A
Functions	—	Q-Up	F
(1 Additional	—	Q-Down	F
Bit I_9)	Load D	—	F
I_9 LOW	—	Load D	F

TABLE 2.
Multiplier and MAC Performances

	Commercial	Military
IDT7216/IDT7217 16 x 16 Multiply Clocked Times	35ns	40ns
IDT7210/IDT7243 Multiply-Accumulate Clocked Times	35ns	40ns

CONCLUSION

As the need for high-speed computing increases, so does the expected throughput of number-crunching chips. The availability of efficient building blocks from IDT allows users to build a 12MHz fixed-point processor and a 10MHz floating-point processor.

TABLE 3.
The IDT72065/IDT72265 Performance

Single-Precision Pipelined Throughput	100ns
Single-Precision Latency	450ns
Double-Precision Pipelined Throughput	100ns
Double-Precision Latency	450ns

ALU Operations

TABLE 4.
The IDT72064/IDT72264 Performance

Single-Precision Pipelined Throughput	100ns	200ns
Single-Precision Latency	300ns	500ns
Double-Precision Pipelined Throughput	200ns	400ns
Double-Precision Latency	450ns	700ns

SEPARATE I/O RAMS INCREASE SPEED AND REDUCE PART COUNT

APPLICATION NOTE AN-05

Integrated Device Technology, Inc

INTRODUCTION:

Static RAMs with separate data inputs and data outputs, such as the IDT71681/71682 4K x 4-bit RAMs and the IDT71982/71982 16K x 4-bit RAMs, provide memory organizations that can improve system architecture in many applications. IDT makes a series of separate I/O RAMs, as shown in Table 1. In this application note, we will demonstrate several system ideas where RAMs with separate data inputs and data outputs offer improved system performance. Typically, the separate data inputs and data outputs eliminate the need for multiplexing of demultiplexing in the data path. Thus, not only is the output enable or disable time eliminated in a critical speed path, but a potential additional element (multiplexer or demultiplexer) may also be eliminated.

TABLE 1: IDT Separate I/O RAM CHIPS

Size	Organization	Outputs Track Inputs During Write	Outputs High Imped. During Write
16K	16K x 1	—	IDT6167
	4K x 4	IDT71681	IDT71682
64K	64K x 1	—	IDT7187
	16K x 4	IDT71981	IDT71982

SEPARATE I/O RAM APPLICATION EXAMPLES

MICROPROGRAM MEMORY

Separate I/O RAMs can be used in a high-speed writeable control store application and offer both speed improvement and a significant parts count reduction in the interface to a MOS microprocessor used to initialize the RAM at power up. Figure 1 shows a typical writeable control store design for a microprogrammed machine. Here we see an IDT39C10 microprogram sequencer driving the 12-address lines of the IDT71681/71682 4K word array. If we assume a microcode width of 96 bits, this design will use 24 of the IDT71681/71682 24-pin, 300 mil packages. As shown in Figure 1, the 12 address lines to all 24 packages are connected in parallel and are driven by the Y outputs of the IDT39C10 microprogram sequencer. This gives a total microcode depth of 4K words, which is sufficient for most microprogram applications. The four data outputs from each device provide microcode bits to the pipeline register to overlap the microinstruction fetching with the microinstruction execution. The pipeline register always contains the microinstruction currently executing, while the IDT39C10 is generating the next address to the RAM and the RAM is accessing the next microinstruction to be set up at the input to the pipeline register.

The advantages of using the IDT71681/71682 RAM in this application come from the speed of this device and from the parts savings associated with not having to demultiplex the data to be loaded into the memory. If the data path were to be bidirectional, such as would be required if we used the IDT6116 (2K x 8-bit RAM) on the IDT6168 (4K x 4-bit RAM), it would be necessary to demultiplex a MOS microprocessor data bus that provides the microcode at power up. This would require one 8-bit driver for each 8 bits of RAM to interface between the various RAMs and the 8-bit microprocessor data bus—an additional 12 parts in this case.

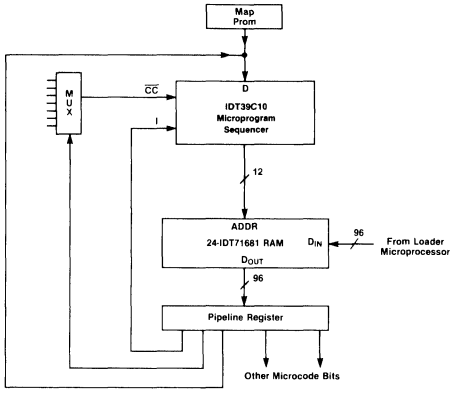


Figure 1. Typical Writeable Control Store in a Microprogrammed Machine.

In a typical system, such as is shown in Figure 1, the microcode is read from a floppy disk and loaded into the writeable control store. An example of this type of microcode loading architecture as shown in Figure 2. The microprocessor system shown in Figure 2 requires three interface points to the writeable control store. First, you must define the address for the write operation. This is provided by means of a WCS address register to select which word in the writeable control store will be written into. Second, you must define the data you are going to write. This is provided by a data register which defines the data for a specific eight bits of the 96-bit word of the control store shown in Figure 1. A total of 12 bytes are required to load one microcode word into the writeable control store depicted in Figure 1. The specific byte to be written is selected by four additional address bits from the WCS address register which are directed to the decoder so that one of the 12 bytes can be selected for loading. Third, a control register is then used to select between the WCS load and operate modes and to manipulate the write enable (WRITE*) line connected to the decoder.

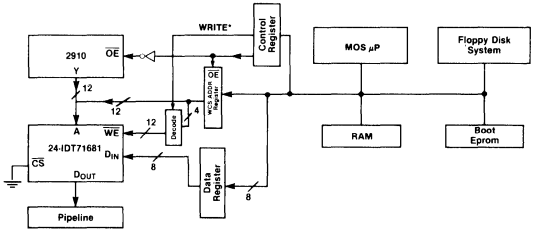


Figure 2. Autoload of the Writeable Control Store.

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The complete cycle required can be described as follows. First, set up the control register to select the WCS address register onto the address bus and disable the IDT39C10 Y outputs. Second, move the address of the first byte to be loaded to the WCS address register. Third, move the data byte to be loaded to the data register. Fourth, change the WRITE* line from high-to-low-to-high by means of two MOS microprocessor I/O cycles. This will write one byte of data to the writeable control store memory. Continue by repeating the steps of loading the WCS address register, data register and then "writing" the data into the writeable control store memory.

A detailed connection diagram of the IDT71681/71682 interface to the MOS microprocessor is shown in Figure 3. Only 10 of the 24 devices are shown, but the connection scheme is similar for all 24-devices. The important point to recognize from the diagram is that the data-in lines are connected on a byte-wide basis. One IDT71681/71682 is connected to the D_0 to D_3 data inputs and the second IDT71681/71682 is connected to the D_4 through D_7 inputs. This means that each two devices are connected so as to accept one byte of data from the MOS microprocessor system. The 12 address lines to IDT71681/71682 are connected in parallel and are driven by a register with three state outputs such as the IDT74FCT374. The remaining address lines from the 29825 WCS address register are connected to decoders such as the IDT74FCT138. Each output for the IDT74FCT138 is connected to two write enable inputs on the IDT71681/71682 memories. This allows one byte to be written when the WRITE* line is changed high-low-high. The chip select line is simply grounded and not used in this application. As can be seen, the IDT71681/71682 offers a convenient interface in a writeable control store for external loading of the data. This connection concept can be extended and changed such that the writeable control store could be loaded with data provided by the host execution CPU itself, rather than the floppy disk.

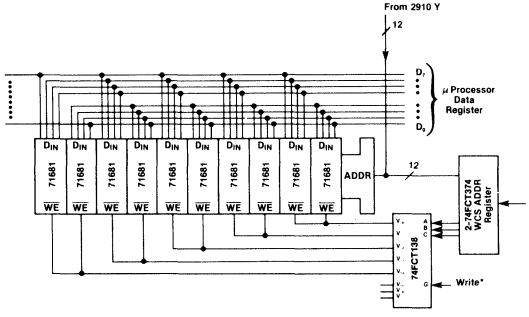

Figure 3. Detail of the MOS Microprocessor Interface to a Writeable Control Store.

VIRTUAL MEMORY AND MEMORY MAPPING

Separate I/O RAMs are ideally suited for use with MOS microprocessors to provide the memory mapping function associated with today's complex microprocessor operating systems. As shown in Figure 4, the IDT71681/71682 can be used to provide mapping from a microprocessor virtual address to a microprocessor physical address in main memory. In addition, status information about the map can also be present in the page table. In this example, a 24-bit virtual address is divided into a 12-bit virtual page consisting of 4K words per page. Depth into the page is provided by a 12-bit offset address. As shown in Figure 4, the 12-bit virtual page address can be connected to the page mapping memory and the resultant output will be a physical page address and status information. A detailed connection diagram is shown in Figure 5.

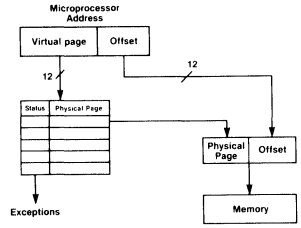

Figure 4. Memory Mapping.

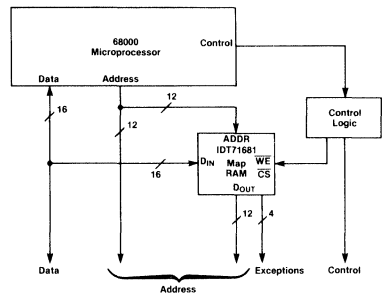

Figure 5. Memory Mapping.

A computer that provides any form of mapping other than the identity map between the central processing unit generated addresses and the physical memory address satisfies the most general definition of virtual memory. In Figure 5, we see the IDT71681/71682 address lines connected to the upper 12 bits of an address bus, such as those provided by the 68000 microprocessor. Here, the separate data output lines are used to provide mapped addresses as well as exception bit status vectors. The separate data-in lines can be connected to the data bus so that the page table provided by this memory is easily updated.

Many use the terminology of virtual memory in a more restrictive fashion. That is, a virtual memory is one where the actual physical memory is smaller than the total memory addressing capability of the machine. A page table memory map, such as that shown in Figure 5, is used to provide a translation from the virtual address to the physical address in such a memory. In a related definition called memory mapping, the physical memory is larger than the logical address space of the machine. This is often applied to such microprocessors as the 8085 and Z80. Here, the machine's logical address space is limited to 64K bytes, but it may be desirable to have a larger physical memory available to the machine. The connection scheme shown in Figure 6 can be used to perform this memory mapping. Some number of address lines, eight in this example,

are connected to eight of the 12 IDT71681/71682 RAM address lines. The additional four RAM address lines are provided by a register and perform an additional mapping select function. The 12 RAM data output lines of the RAM are used in conjunction with the 8 remaining address lines from the microprocessor to provide a total of 20 address lines (1 megabyte) in this example. The 12 RAM data-in lines are connected to the data bus for easy loading of the page table.

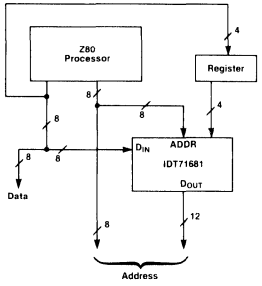

Figure 6. Z80 Memory Mapping.

Figures 5 and 6 indicate that some thought must be given to the exact mechanism for the address to be provided to the mapping RAM while it is being loaded. This can be handled in one of two ways. The simplest way is to provide an address register on one of the microprocessor I/O ports that is loaded with the target address, and then this address is used when the mapping memory is being written into. A more clever technique is to provide a control register that disables the main memory write and enables the mapping memory write such that no additional address register is required. Instead, data to be loaded into the mapping memory is simply moved to the address in the virtual space and is redirected to the mapping memory rather than the main memory.

Again, the examples of Figure 3 through 5 demonstrate the advantage of the IDT71681/71682 in having separate data inputs and data outputs.

CACHE MEMORY

A cache memory is a high-speed memory that is placed between the CPU and the main system bus. The purpose of a cache memory is to make a slow memory look like a fast memory. This is done by using two memories. The first is a small, high-speed memory called a cache memory, and the second is a large, slow memory called the main memory. Both memories are attached to the system bus which is connected to the CPU. The cache memory holds a copy of the most frequently used data in the main memory. If data requested by the CPU is in the cache memory, it responds first; if not, the CPU waits for the data from the slower main memory. If the data and instructions being executed most of the time are in the cache memory, a performance improvement is realized. This is commonly the case because most programs consist of loops and small pieces of code which are executed repetitively, and these occupy a small number of memory locations. The hardware associated with the cache memory attempts to keep this data in the high-speed memory. The term "hit ratio" is used to describe the number of times the data or instructions are in the cache memory versus the total number of memory accesses. It is not unusual to find hit ratios in the 90 percent range for some cache memory designs.

One of the most common cache memory organizations used is called the direct mapped cache memory. Figure 7 shows the block diagram for the implementation of the typical direct mapped cache. In this implementation, the cache memory consists of three main parts. These are the tag store, the data store and the match comparator. In the example shown in Figure 7, the tag buffer and data RAM are each 4K words deep using one row of the IDT71681/71682 static RAMs. The high order 12 bits of the address can be stored in the tag RAM so as to specify the unique memory space for which the data corresponds. The tag RAM usually contains additional bits which represent data validity and parity.

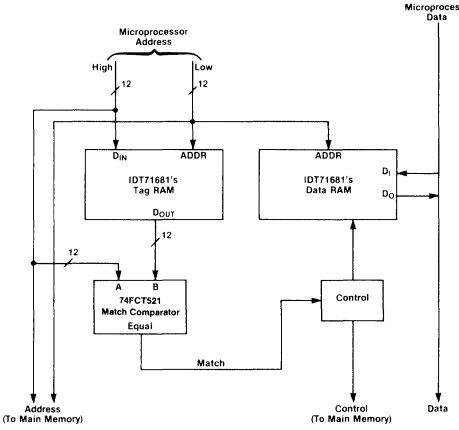

Figure 7. Direct Mapped Cache Memory.

The operation of such a cache memory is as follows. The microprocessor puts out an address on the address bus. The lower 12 bits are connected to the address inputs of the data and tag RAMs and cause the data and tag RAMs to begin fetching the word at the location. Then, the actual data value stored in the tag RAM is compared against the upper 12 address bits to look for a match. If a match is found, the valid bit is true and the data in the data RAM corresponds to the address on the address bus, we have a cache "hit" and the data in the data RAM is placed onto the microprocessor data bus. If no match is found or the valid bit is false, then a cache "miss" occurs and the data must be fetched from the main memory. As the data is brought in from the main memory to the microprocessor, it is also written into the data RAM and, at the same time, the tag RAM is loaded with the high order 12 address bits that represent the tag number from which the data was taken. Hopefully, the next time this address is used, it will still be in the cache memory.

STACK MACHINES AND HIGH-PERFORMANCE ALUS

A bit-slice microprocessor design can utilize separate I/O RAMs in the ALU architecture in several ways. A typical bit-slice microprocessor ALU configuration is shown in Figure 8. Here we see the IDT71681/71682 configured with its data inputs connected to the Y output of the 2903 bit-slice, and its data outputs connected to the DA input of the 2903 bit-slice. Two uses for such a connection are obvious. First, it is possible to use the tightly coupled RAM to increase the number of registers available to the

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ALU. This could be used in certain high-performance algorithms such as floating point, Fast Fourier Transforms (FFTs), etc. Similarly, this register set might be used to allow very high-speed context switching of the processor ALU section. In this fashion, no register would have to be updated during the handling of interrupts or other system/user context switches.

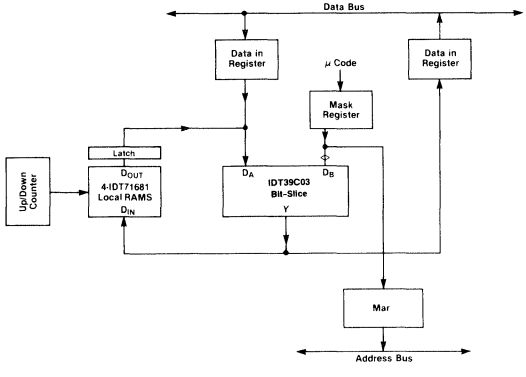

Figure 8. Stack Machines and High-Performance ALUs.

Another use for the IDT71681/71682 RAM shown in Figure 8 would be to provide a local stack for the ALU. This could be implemented using an up-down counter to drive the address lines to the RAM and the appropriate microcode to control pushing and popping of the stack. One or more such stacks could be very useful in high level language machines. For example, two such stacks might be used in a FORTH machine. One stack would be the operand stack, while the second stack would be the return stack.

A typical TTL ALU implementation is shown in Figure 9. Here, an MSI ALU, such as the 74S181, is used in a microprogrammed environment. Local register/accumulator storage is provided by IDT71681/71682 memories. The A and B inputs to the ALU are driven by the accumulator A and accumulator B RAM register/stack, respectively. Again, the advantage of the separate data inputs and data outputs is well displayed.

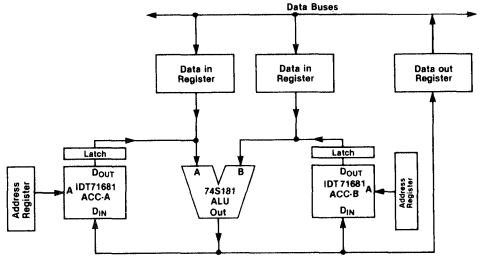

Figure 9. TTL ALU Implementation.

VIDEO DISPLAY CONTROLLER

The video display controller shown in Figure 10 can utilize separate I/O RAMs in two different ways. One area of the video display controller, the character generator, uses two IDT71681/71682s to hold 512 different 5-by-7 dot characters. In this configuration, the CRT controller provides the address to the character generator which generates the dot pattern for a particular line in the selected character. By using RAM in the character generator, the character font can be controlled by the host microprocessor and changed as often as desired. Two additional IDT71681/71682s are used for the screen refresh RAM. In this application, two RAM chips provide the local storage for the characters on the screen. Since a standard 24-row-by-80-column CRT display represents almost 2K bytes of data, the screen refresh RAM shown can store up to two pages of information for display.

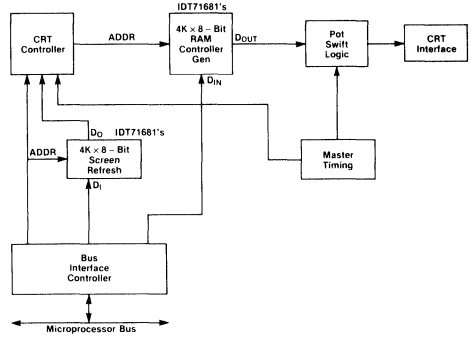

Figure 10. Video Display Controller.

DIGITAL FILTERS

The four-sample non-recursive digital filter in Figure 11 is another application which demonstrates the importance of separate data inputs and data outputs in the RAM memory. In this example, a 4096 word range-gated filter is shown. Digital filters consist primarily of memory, multipliers and adders. Range-gated filters are used in systems that quantify and otherwise process distance-related measurements such as radar, sonar and ultrasonic medical diagnostic instruments. Typically, the return signal is divided into increments of time (or distance) where each increment is to be individually processed. Thus, many different elements are to be processed and all may share the same multipliers and adders. However, different memory locations are needed for each time-sequential element. The example shown in Figure 11 can best be understood with the following description: the current output is equal to the sum of the present sample times the constant A_0, plus previous sample times the constant A_1, plus the second previous sample times the constant A_2, plus the third previous sample times the constant A_3. Four samples participate in generating each output, and because only input samples contribute to the output, the filter is said to have a finite impulse response.

Similarly, Figure 12 shows a range-gated recursive digital filter. It is similar in concept to that shown in Figure 11, except that a recursive filter contains feedback. Because feedback terms contribute to the output, it has an infinite impulse response. Again, separate I/O RAMs provide a unique performance advantage in this application.

Depending on the write timing, it may be necessary to place either latches or registers at the input or output of the RAMs shown in Figure 11 and 12.

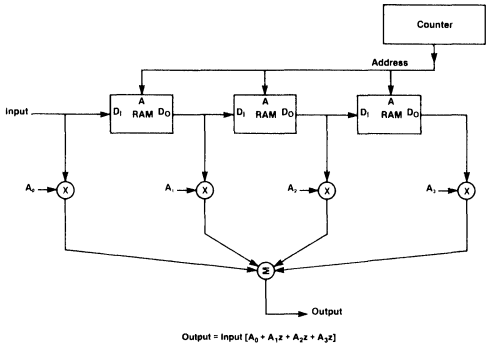

Figure 11. Four-Sample Non-Recursive Digital Filter.

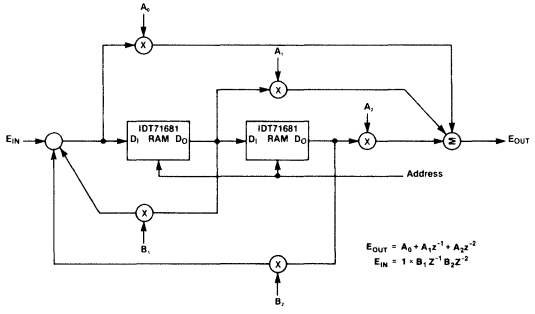

Figure 12. Recursive Digital Filter.

PING PONG RAM

A common problem in digital signal processing is the word-by-word transformation of a block of data, such as adding a constant to each word. This tranformation is usually done by reading each word from on RAM, modifying the data and writing the word into a second RAM. This type of operation may be done several times, with different transformations on each pass. This requires at least two RAMs. It is desirable to use a single bus system to tie the RAMs to the transformation logic, so that only one set of transformation logic is required.

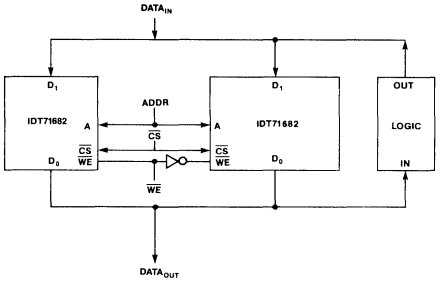

Figure 13. Pin Pong RAM.

A significant speed improvement in a common bus design can be realized by using two separate I/O RAMs in an alternate read/write mode, as shown in Figure 13. In this approach, data is initially read from the first RAM while transformed data is being stored in the second. Then, by changing the state of the $\overline{WE}$ input, data is read from the second RAM and new data can be written into the first RAM. In this fashion, one RAM is always in the read mode and the other is in the write mode. The $\overline{CS}$ can be used to remove both RAMs from the $DATA_{OUT}$ bus so it can be used by other devices. The $\overline{CS}$ line MUST be set inactive during a change of address to the RAM in the example shown in Figure 13. A speed improvement is realized in this configuration because the "data valid to end of write" time is faster than the "write cycle" time. This allows external logic to be performed on the $DATA_{OUT}$ and the result to be written back into the RAM at an overall higher system speed. In some designs, timing advantages can be realized by separating $\overline{CS}$, $\overline{WE}$, or both.

SUMMARY

Separate I/O CMOS static RAMs can provide the system designer with increased speed and reduced part count and their versatility will be demonstrated by creative design engineers in numerous applications beyond those discussed in this application note. These devices offer high-speed access times and high-speed cycle times. The low power inherent in CMOS allows new levels of performance to be achieved in small, compact designs without the thermal problems of earlier bipolar designs. Certainly, these devices offer the system design engineer another tool in the search for improved system performance.

8

Integrated Device Technology, Inc.

16-BIT CMOS SLICES — NEW BUILDING BLOCKS MAINTAIN MICROCODE COMPATIBILITY YET INCREASE PERFORMANCE

APPLICATION NOTE AN-06

by Michael J. Miller

INTRODUCTION

The electronics industry has been an evolutionary succession of dominating technologies. This has been true for semiconductor devices in general, as well as the product family called bit-slice microprocessors. With the extinction of each technology and the emergence of the new, there is an associated transition for both the manufacturer and the consumer. Each company seeks to minimize the effort of this transition.

In the 1950s it was a generation of germanium diodes and transistors. During the 1960s, silicon transistors and bipolar ICs dominated. The last decade saw the emergence of the NMOS microprocessor and dynamic memories. This decade will be dominated by very high-speed CMOS as the primary volume process. This evolution is not only taking place with the industry but, in specific, with the microprogrammed bit-slice microprocessors. Today very high-speed, low-power CMOS is taking the place of high-speed bipolar. CMOS is capable of operating faster and at 1/5 to 1/10 the power of bipolar technologies. Because of this, CMOS is becoming the technology of choice for bit-slice microprocessors.

In the past, technological changeovers have been expensive to the manufacturer as well as the consumer. The MICROSLICE™ Family from IDT seeks to facilitate this transition by offering two families of CMOS bit-slice devices: IDT39C000, IDT49C000. The IDT39C000 family provides high-speed CMOS devices that fit into the sockets of current designs which utilize the 2900 family of bit-slice devices. The IDT39C000 family is pin-for-pin compatible to the 2900 family as well as compatible with its highest speed grade. An easy upgrade path is provided by the IDT49C000 family of bit-slice devices. This family starts off by providing higher densities (families of 16- and 32-bit), improved architecture and progresses on into innovative architectures of the future.

RE-EMERGENCE OF MICROPROGRAMMING

As a result of CMOS, bit-slice microprogram designs are experiencing a new renaissance. In the mid-70s, the emergence of the 2900 family, as heralded by the 2901, was designed entirely using TTL bipolar technology. The 2901 has progressed from a propagation time — A/B to $\overline{G}/\overline{P}$ equal to 80ns — to the 2901C which sports 37ns. To achieve these final speeds though, the total TTL design had to be abandoned and ECL was substituted for the inner workings of the 2901, with TTL buffers interfacing to the outside world. Today at IDT, very high-speed CMOS is being used to produce an IDT39C01E with A/B to $\overline{G}/\overline{P}$ of 21ns, at 1/8 the power of the bipolar 2901C.

In parallel with the evolution of the 2901 has been the blossoming of the 2900 family to a multi-device product family. All of the latest designs use ECL internally. The trend in this family has been to add more and more gates on chip. To achieve this, though, more current has been consumed by each of the ICs starting with the 2901 at 1.25W to the 29300 family at approximately 8W. To handle the 8W, new packaging technology was developed which incorporates heat spreaders and cooling towers mounted on top.

Within the limits of maximum speed and density, tradeoffs can be made. For a given package, more speed can be achieved with less gates; or conversely, more gates can be incorporated at the expense of overall speed in critical paths. This relationship is referred to as the speed/power product of a given technology. The bipolar 2900 family has been extended to the limit of feasible packaging and cooling technology because of the density and speed requirements of today's applications. Very high-speed CMOS, in contrast, has a speed/power product an order-of-magnitude smaller than bipolar for the same speed. Therefore, CMOS requires less expensive packages and cooling systems.

COMPARISON OF FAMILY PERFORMANCE(1)

	MICROSLICE		BIPOLAR		SPEED PATH
	SPEED (ns)	DYNAMIC POWER (mA)	SPEED (ns)	DYNAMIC POWER (mA)	
IDT39C01C	37, 25	30	37, 25	265	A/B → $\overline{G}/\overline{P}$, C_n → F = 0
IDT39C01D	28, 17	35	—	—	A/B → $\overline{G}/\overline{P}$, C_n → F = 0
IDT39C01E	21, 14	40	—	—	A/B → $\overline{G}/\overline{P}$, C_n → F = 0
IDT39C03A	52, 35	60	52, 35	350	A/B → $\overline{G}/\overline{P}$, C_n → Z
IDT39C10B	30	80	30	340	$\overline{CC}$ → Y
IDT39C10C	16	80	—	340	$\overline{CC}$ → Y
IDT39C203	52, 35	60	52, 35	350	A/B → $\overline{G}/\overline{P}$, C_n → Z

NOTE:

1. Reflects performance over commercial temperature and voltage range.

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Printed in the U.S.A. 7/86

A decade ago, CMOS was noted for lower power and low-performance. Today, CMOS is capable of running at speeds faster than bipolar at 1/5 to 1/10 the power. Dramatically smaller power consumption and smaller gate sizes allow for even higher levels of integration to be achieved. In previous bipolar designs, an ALU, a barrel shifter and a multiplier each required a package of their own for heat dissipation, whereas CMOS can incorporate them all on one piece of silicon while still having room to include a reasonable amount of RAM. This means that CMOS has room to grow, thus providing for new innovative architectures in the future.

While the lower power consumption allows for more gates in the same package, there is also freedom to shrink the size of the packages because the package is being used less as a means of dissipating the heat. This is timely because consumers are requesting more and more in smaller volumes of space.

THE LATEST IN CMOS TECHNOLOGY

CEMOS™ is used to produce the MICROSLICE family with its two sub-familes — named, respectively, the IDT39C000 Family and the IDT49C000 Family. These families address microprogrammable designs of the present and future. CEMOS is a trademark for the proprietary CMOS process technology of IDT. CEMOS is an enhanced CMOS technology which includes such features as high ESD protection, latch-up protection and high alpha particle immunity.

MICROSLICE IN EXISTING DESIGNS

The IDT39C000 family allows the designer to take advantage of very high-speed CMOS in existing designs. This family is a pin-for-pin compatible family with the 2900 counterparts. By replacing the current 2900 parts with IDT39C000 parts in existing sockets, the power consumption of that portion of the circuitry may be reduced down to 1/5 to 1/10 of the bipolar power consumption at full operating speeds. The IDT39C000 family is specified around the highest speed grade versions of the current bipolar devices. Currently in the IDT39C000 family are two of the common ALU architectures, the IDT39C01 and the IDT39C03/203. Included in the family are the sequencers IDT39C10 and IDT39C09/11. The IDT39C705/707 are registered file expansions for the IDT39C03/203. The family also includes the 16 x 16 multipliers, IDT39C516/517, and the 16 x 16 multiplier-accumulator, IDT39C510. Not to be ignored, the IDT39C60 family is available for high-performance error correcting memory designs. This family also includes the first speed upgrade beyond the bipolar technology. The IDT39C01D is 25% faster than the 2901C, while the IDT39C01E exhibits speeds 40% faster than the 2901C.

THE IDT49C000 FAMILY, THE NEXT GENERATION

The IDT49C000 family takes advantage of all the benefits that CEMOS has to offer: high-speed, low-power, very large scale integration and smaller packages. Because of the new freedoms imparted by CEMOS, the IDT49C000 family is the next family of innovation for bit-slice microprogrammed designs.

While the IDT39C000 family minimizes upgrade costs by being pin-compatible, the IDT49C000 family addresses the aspect by providing parts in the family which are code-compatible, thus achieving conservation of previously written code. This is significant because, in the last decade, the cost of the software portion of the system has surpassed the hardware. The IDT49C000 family, however, is not limited to code-compatible devices and will, in the future, include devices with new and wider architectures.

THE IDT49C402A 16-BIT ALU PLUS

The first ALU in the IDT49C000 family is the IDT49C402A which is a 16-bit ALU and register file. This device is a superset of the 2901 architecture. It is a very high-speed, fully-cascadable 16-bit CMOS microprocessor slice, which combines the standard functions of four 2901s and one 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs. The IDT49C402A includes all of the normal functions associated with the standard 2901 bit-slice operation: (A) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operands selection of the ALU; (B) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; (C) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and (D) a tenth instruction input (I_9) offering eight additional designation and control functions. This I_9 input, in conjunction with I_6, I_7 and I_8 allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and new combinations of destination functions with the RAM A-port output available at the Y output pins of the device. This eliminates bottlenecks of inputting data into the on-chip RAM.

The block diagram on page 3 shows the familiar architectures of the 2901 with register files which have both A and B data feeding into an ALU data source selector. This combines together the data from the register file along with direct data input (D) and the Q Register. The output of the ALU data source selector produces two operands, R and S. R and S are fed into an eight-function ALU, the output of which can go to the data output pins or be fed back into the register file and/or Q Register.

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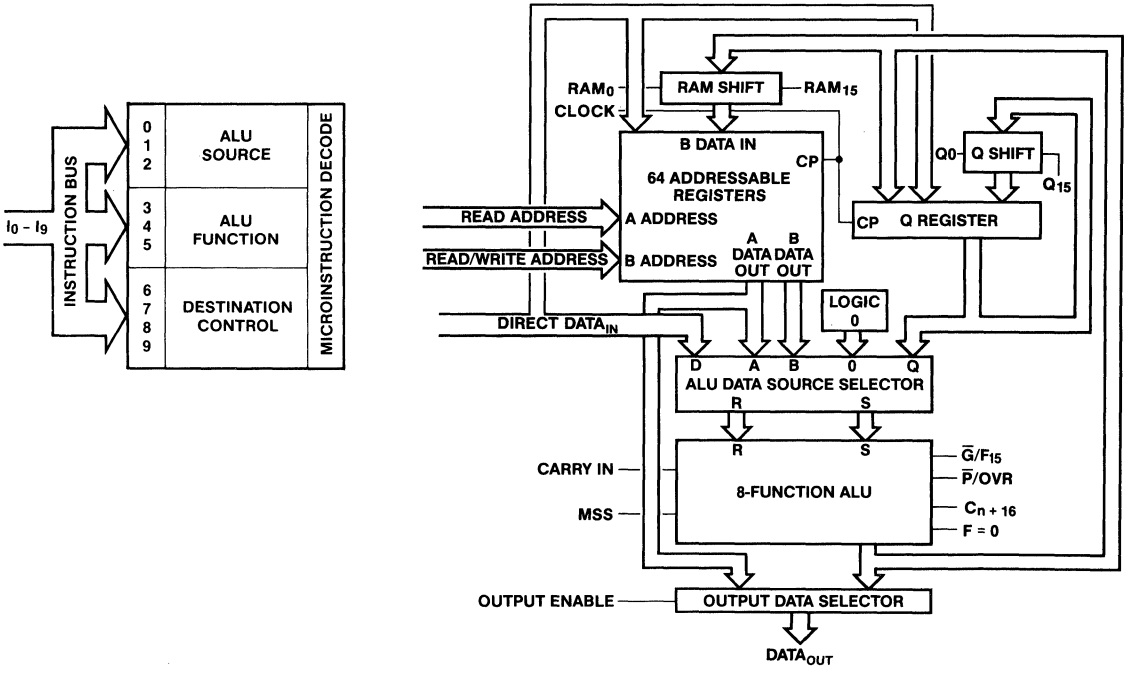


IDT49C402A 16-Bit Microprocessor Slice.

WHERE THE IDT49C402A EXCELS

The IDT49C402A, however, differs from the regular 2901 architecture by the addition of a new data bus that goes from the direct data input pins (D) into the register file and the Q Register, thus providing a data path directly into the register file and Q Register rather than passing through the ALU block. With conventional 2901 architecture, in order to get data into the register file the ALU must be placed in the pass mode taking data directly from the D inputs through the ALU and around to the register file. With this new architecture, data can be operated on out of the register file and the Q Register and the result placed back in the Q Register while new direct data is being brought into the register file. Conversely, the Q Register can be loaded while operations are being performed on the register file and placed back into the register file.

Whereas the 2901 has a 16-deep register file, the IDT49C402A has 64 addressable registers. The 2901 architecture does not allow for direct cascading of the register file. Dead cycles can be eliminated because 4 times more data can be cached on-chip with the ALU. Other applications may use the 64 registers as four banks of 16 registers. The bank selection could be thought of as task switching for interrupt-driven multi-tasked applications.

The third difference from the 2901 is the ALU expansion mechanism. The IDT49C402A incorporates an MSS input which programs the device, being the most significant device or not. When not the most significant slice, the P & G signals are brought out. When the most significant slice, the sign and overflow are brought out on the P & G.

IDT49C402A 16-Bit ALU Destination Functions

	RAM	Q	Y-OUT
2901 Functions (3-Bits I_6-I_8 I_9 HIGH	F-Up	Q-Up	F
	F-Up	—	F
	F-Down	Q-Down	F
	F-Down	—	F
	—	—	F
	—	Load F	F
	Load F	—	F
	Load F	—	A
Added IDT Functions (1 Additional Bit I_9) I_9 LOW	Load D	Load F	F
	Load D	Load F	A
	Load F	Load D	F
	Load F	Load D	A
	—	Q-Up	F
	—	Q-Down	F
	Load D	—	F
	—	Load D	F

CODE CONSERVATION

The microinstruction word of the IDT49C402A looks the same as the 2901 with the exception of the additional destination control line called I_9. Conservation of microcode can be achieved via two methods. The first and the most simple method is to tie the instruction line I_9 high on the socket and not connect it to the microcode. In this way, the remaining destination control lines I_8, I_7 and I_6 are compatible to the 2901.

For those systems that intend to add more code, or rewrite code for performance optimization, the second method is performed by making minor alterations on the microcode. For many designers this can be a fairly easily-achieved task by making minor alterations in the meta assembler used to compile the microcode source. The alteration in the meta assembler would add I_9 such that all previously written code would have this signal default to a Don't Care state of high, thus enabling the standard destination instructions (the traditional 2901 codes). Additional code could then be written which utilizes this instruction line and the extra features provided in the IDT49C402.

An alternative to the second method for achieving microcode compatibility would take the already-compiled microcode and run it through a simple program, written in another language, which would spread the microcode apart and introduce in this additional instruction bit. This method is used for microcode which no longer has existing source.

ONE IDT49C402A WINS RACE AGAINST FOUR 2901s

While the IDT49C402A seeks to improve performance through architectural enhancements, it also achieves improved performance through raw technology. The IDT49C402A achieves an A and B address to Y output of 41ns for military and 37ns for commercial temperature ranges, as compared to four 2901Cs and a 2902A which have A and B to Y and flag of 80ns for military and 68ns for commercial. Thus the IDT49C402A is 45% faster than five discrete parts of the older 2900 family. the IDT49C402A could achieve processing of approximately 15 MIPS.

COMPARISON OF 16-BIT MICROPROGRAMMED SOLUTIONS

	IDT49C402A CMOS	4 — 2901C & 2902A BIPOLAR	29116 BIPOLAR
Dynamic Power(1)	125mA	1049mA	735mA
ABI → Y/FLAG(1)	37ns	68ns	84ns
Package Space Sq. Inches	0.32 LCC 1.5 DIP	1.8 LCC 5.04 DIP	0.56 LCC 2.08 DIP
Features	ALU 64 RAM Q REG SHIFTER	ALU 16 RAM Q REG SHIFTER	ALU 32 RAM ACCUM BAR. SHIFT

NOTE:

1. Reflects performance over commercial temperature and voltage range.

THE IDT49C402A IS COOL

Even though the IDT49C402 has five times the circuitry on-chip as does the 2901, it is 1/2 the power of just one 2901.

The 16-bit solution of the IDT49C402A is 1/8 the power of four 2901Cs and one 2902A. While total power consumption is the concern of many designers because it has impact on power supplies and cooling systems, the lower power consumption also provides other benefits. Because less power is being consumed less of the package is needed as a heat sink. This allows for packages with much smaller outlines. Besides being offered in a standard 68-pin PGA, the IDT49C402A comes in a 68-pin dual in-line package with pins on 70 mil centers, 600 mils wide, which yields a package with an outline of 2.5 x 0.6 inches. A 68-pin LCC with pad spacing of 25 mil centers, as well as a standard 68-pin LCC with pad spacing of 50 mil centers, are offered. When the board space taken up by just the packages are added up, the LCC version of the IDT49C402A is 0.32 square inches, as opposed to 1.8 square inches for four 2901Cs and a 2902A. Respectively, the IDT49C402A in the SHRINK-DIP package (70 mil centers) is 1.5 square inches as opposed to 5 square inches for four 2901Cs and a 2902A. Not included in the calculations for the multi-chip solutions is the spacing between the ICs.

The next ALU, soon to be introduced in the IDT49C000 family, is the IDT49C403 which will be a 16-bit version of the 2903/203. This device will be at least as fast as the four 2903s and a 2902A, and will consume 1/5 to 1/10 the power of the multi-chip solution.

A 16-BIT SEQUENCER TO MATCH A 16-BIT ALU

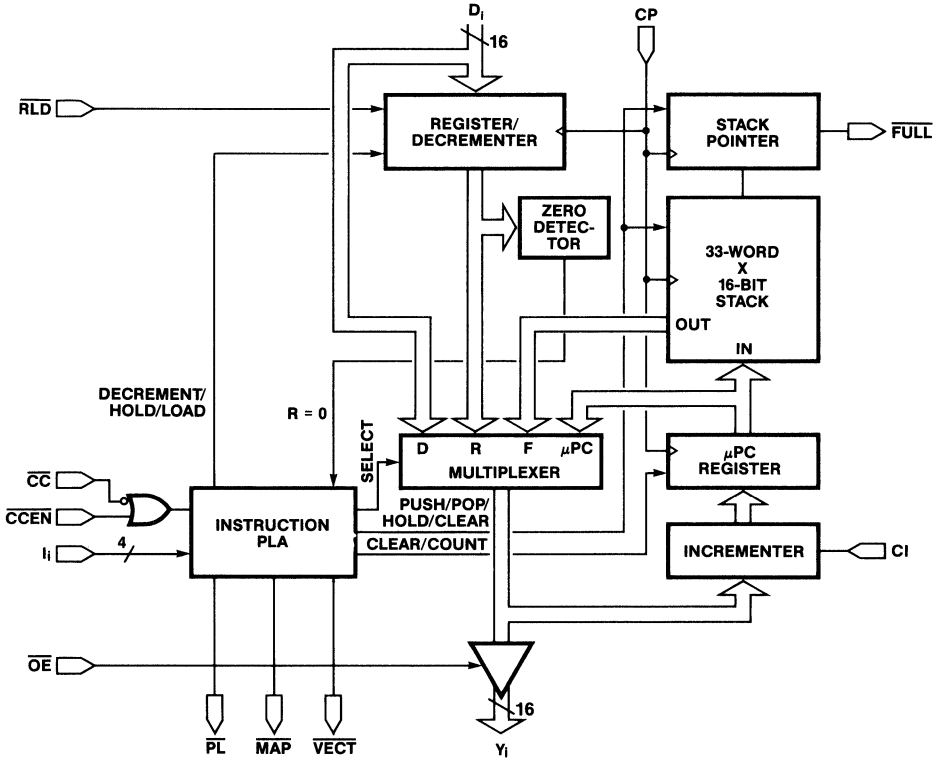
While ALUs provide the data path for performing computations, the sequencer is another important building block which orchestrates the entire machine. The first sequencer in the IDT49C000 family is the IDT49C410. The IDT49C410 is architecture- and function code-compatible to the 2910A, with an expanded 16-bit address path which allows for programs up to 64K words in length.

The IDT49C410 is a microprogram address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the sequential accesses, it provides conditional branching to any microinstruction within its 64K word range.

While the 2910A incorporates a 9-deep stack, the IDT49C410 has a 33-deep stack which provides micro subroutine return linkage and looping capability. This deep stack can be used for highly nested microcode applications.

Referring to the block diagram on page 5, it can be observed that, during each microinstruction,the microprogram controller provides a 16-bit address from one of four sources: 1) the microprogram address register (μPC) which usually contains an address one greater than the previous address; 2) an internal direct input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a last-in first-out stack (F).

The IDT49C410 is completely code-compatible with the 2910A. This allows the IDT49C410 to execute previously written



IDT49C410 16-Bit Microprogram Sequencer.

microcode, while allowing for more microcode to be added to the application and taking the program beyond the 4K word boundary. Because the IDT49C410 is microcode-compatible, older microcode routines can be incorporated in new designs utilizing the IDT49C410.

The 16-bit IDT49C410 uses approximately 1/4 the power consumption of the 2910A (which is a 12-bit sequencer), thus maintaining the 1/5 power consumption on a bit-by-bit basis. The IDT49C410 consumes, over frequency and temperature ranges, 75mA for commercial and 90mA for military. The 2910A compares with 340mA for military and 344mA for commercial. Because of the lower power consumption, smaller packaging may be utilized. While the IDT49C410 is offered in a standard 600 mil wide package with pins on tenth inch spaces, it is also offered in a package which is 400 mils wide with pins on 70 mil centers. This is roughly 1/2 the standard package with regards to area taken up by each package.

COMPARISON OF MICROPROGRAM SEQUENCERS

	IDT49C410A	IDT49C410	2910A
$\overline{CC} \rightarrow Y$(1)	15ns	24ns	24ns
Stack Depth	33	33	9
Address Range	64K	64K	4K
Dynamic Power(1)	75mA	75mA	340mA

NOTE:

1. Reflects performance over commercial temperature and voltage range.

WORKING TOGETHER

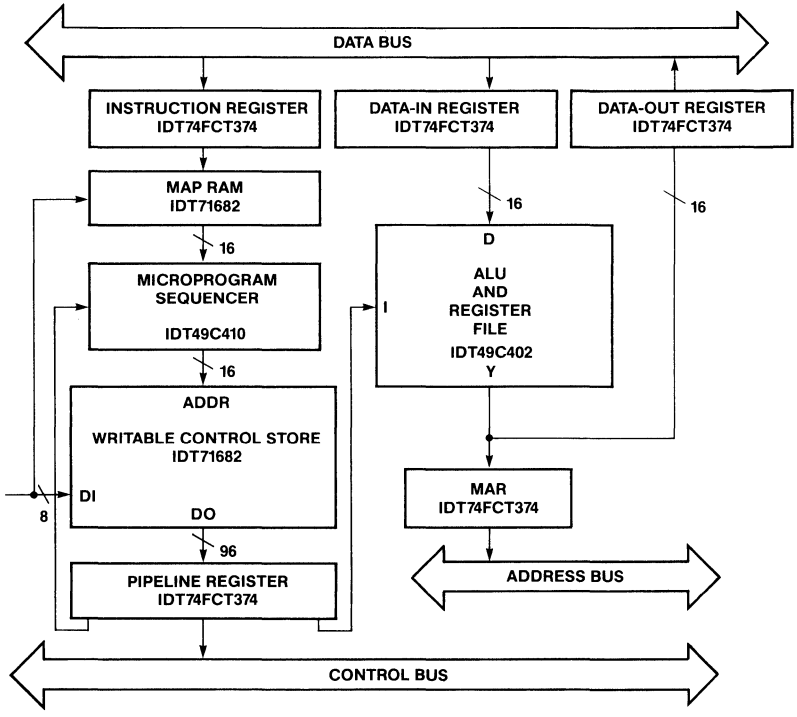
The simplified block diagram of an example Central Processing Unit (CPU) is shown below using devices manufactured by IDT. This CPU architecture can be viewed as two major sections which have a MICROSLICE family part at the heart of each. The major section of the left hand side of the diagram is the control path. The microprogram sequencer at the heart is the IDT49C410 which generates the address for the microprogram stored in the writeable control store (WCS). The output of the WCS is registered by the pipeline register. Together, the sequencer, WCS and pipeline register make up a state machine which controls the operation of the entire CPU. In this CPU, the state machine first fetches a machine instruction and captures it in the instruction register. The instruction register determines the starting address for each sequence of microinstructions associated with each machine opcode.

In this example, both the microprogram store and the instruction mapping memory are formed using RAM. The RAM has separate $DATA_{IN}$ and $DATA_{OUT}$ buses (IDT71682). This allows the input side to be connected conveniently to an 8-bit bus for initialization at power up.

The second major section is on the right hand side. This section is called the data path. The heart of this section is the IDT49C402A. In it is contained all of the working registers and the arithmetic logic unit for performing data computations. One of the internal registers always contains the value of the program counter (PC) which is the address at which the opcode for the machine instruction is fetched. When an opcode is fetched, the memory address register (MAR) is loaded with the value of the PC while, at the same time, the value of the PC plus one is loaded back into the internal register file. The $DATA_{IN}$ and $DATA_{OUT}$ registers are used to buffer data coming from and going to the memory during execution of the machine instruction.

CONCLUSION

The MICROSLICE family from IDT provides high-performance CMOS solutions for microprogrammed applications. Not only does the family provide for yesterday's designs with plug-compatible devices of the IDT39C000 family, it also provides solutions for future applications. With the IDT49C000 family, the designer can take advantage not only of the lower power consumption of CMOS, but utilize higher speeds and smaller board spacing, yielding smaller packaging concepts required by today's customers. In the future, the IDT49C000 MICROSLICE family will provide alternative architectures which will provide for yet higher performance solutions.



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Integrated Device Technology, Inc.

CACHE TAG RAM CHIPS SIMPLIFY CACHE MEMORY DESIGN

APPLICATION NOTE AN-07

By David C. Wyland

ABSTRACT

Cache memories are a widely used tool for increasing the throughput of computer systems. The IDT7174 Cache Tag RAM is a new component designed to support direct mapped cache designs by providing the tag comparison on-chip. This allows relatively large cache memories to be designed with low chip count. The application of the IDT7174 to cache memory design is explored by designing a simple cache memory, reviewing its operation and performance, discussing methods of extending the design, and then reviewing the theory behind the design of cache memories in general.

INTRODUCTION

Cache memories are an important design tool for increasing computer performance by increasing the effective speed of the memory. Computer memories are usually implemented with slow, inexpensive devices such as dynamic RAMs. A cache memory is a small, high-speed memory that fits between the CPU and the main memory in a computer system. It increases the effective speed of the main memory by responding quickly with a copy of the most frequently used main memory data. When the CPU tries to read data from the main memory, the high-speed cache memory will respond first if it has a copy of the requested data. Otherwise, a normal main memory cycle will take place. In typical systems, the read data will be supplied by the cache memory over 90% of the time. The result is that the large main memory appears to the CPU to have the high speed of the cache memory.

The IDT7174 Cache Tag RAM introduced by IDT simplifies the design of high-speed cache memories. It can be used to make a high-performance cache memory with a low part count. The IDT7174 Cache Tag RAM consists of a 64K-bit static RAM organized as 8K x 8 and an 8-bit comparator, as shown in Figure 1. The comparator is used in direct mapped cache memories to perform the address tag comparison, and allows a 16K byte cache for a 68000 microprocessor to be built with four memory chips. The IDT7174 also provides a single pin RAM clear control which clears all words in the internal RAM to zero when activated. This control is used to clear the tag bits for all locations at power-on or system-reset when the cache is empty of data. This allows one of the comparison bits to be used as a cache data valid bit.

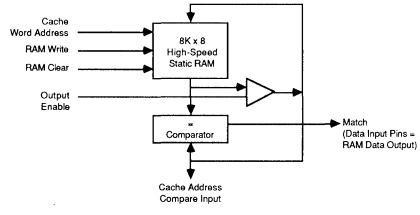

Figure 1: IDT7174 Cache Tag RAM Block Diagram

DESIGN OF A CACHE MEMORY

To understand the application of the IDT7174 to cache memories, we will begin by designing one. A block diagram of a cache memory system using IDT7174 Cache Tag memory chips is shown in Figure 2. The cache memory serves a 16-bit microprocessor with a 24-bit address bus and a main memory. In this system, the 13 least significant bits of the address bus are connected to the address inputs of both the cache tag and the cache data RAM chips. The upper 11 bits of the address bus are connected to the data I/O pins of the cache tag RAMs. The remaining five I/O pins of the cache tag RAMs are connected to a logic 1 (+5).

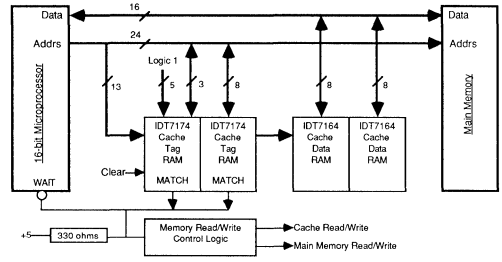

Figure 2: Cache Memory System Block Diagram

The MATCH outputs of the cache tag rams are tied together and connected to the WAIT input of the microprocessor. A 330 ohm pull-up resistor is used because the MATCH outputs are open-drain type. The MATCH outputs are positive-active. The MATCH output goes high when the contents of the internal RAM are equal to the data on the I/O pins. When several cache tag RAMs have their MATCH outputs connected together, a wire-AND function results: all of the comparators must each register a match before the common MATCH signal can go high.

In the system shown, the state of the WAIT input to the microprocessor determines whether the memory data is to come from the cache or the main memory. If the WAIT input to the microprocessor is high, the microprocessor will accept data immediately from the cache data RAMs; if the WAIT input is low, the microprocessor will wait for the slower main memory to respond with the data.

To understand how the cache memory operates, we will follow its operation from start-up in an initially empty state. When the system is powered-up, the cache tag RAMs are cleared to zero by a pulse to the initialize pins of the IDT7174 RAMs. This causes all cells in the RAM to be simultaneously cleared to logic zero. When the microprocessor begins its first read cycle, the 13 least significant bits of the address bus select a location in the cache tag RAMs. The location in the cache tag RAMs is compared against the upper bits of the address bus and against five bits of logic one.

The MATCH output of the cache tag RAMs will be low because all cache tag RAM cells were reset to zero, and the zeros from the selected cell are being compared against the five bits of logic one. In this case, the microprocessor waits for the slower main memory to respond. This is called a cache miss.

When the main memory responds with read data for the microprocessor, this data is also written into the cache data memory at the address defined by the 13 least significant bits of the address bus. At the same time, the upper 11 bits of the address bus and the five bits of logic one are written into the cache tag memory. This 11-bit address tag, in combination with the 13 bits of RAM address select, uniquely identify the copy of the main memory data that was stored. The five logic one bits serve as a data valid bits which indicate that the data in the cell is a valid copy of main memory data.

When the microprocessor requests data from the same location that has been written into the cache, the upper address bits on the address bus will be the same as the bits which were previously written into the cache tag RAM and the MATCH signal will go high. This is called a cache hit. In this case, the cache data is gated onto the data bus and the memory cycle is complete.

If the microprocessor requests data from an address with the same 13 least significant bits as a word in the cache, but with different upper address bits, a cache miss will result and the current (more recent) data will be written into the cache. In this manner, the cache is continuously updated with the most recently used data.

Memory write cycles are treated differently from read cycles. On write cycles, data is written directly into main memory and into the cache. This is called the write-through method of cache updating. Since all data is written immediately into main memory, it always contains current information. Data is written into the cache on full word writes or on byte (i.e. partial word) writes if a match occurred. Writing bytes into the cache only if a cache match occurs ensures that the full word in the cache is valid. For example, this ensures valid data for a byte write followed by a word read.

The design in Figure 2 uses unbuffered writes. In unbuffered writes, all write cycles occur at main memory speeds. This slows down the system for all write cycles at the expense of simple memory controls; however, this may be acceptable since only 15% of all memory cycles are write cycles in typical programs. Buffered write is a slightly more complicated method which improves performance. In buffered write cycles, the write data and address are loaded into registers, and the main memory write cycle proceeds in overlap with other processor operations. Since the next few cycles will probably be read cycles and their data will come from the cache, the result is that buffered write cycles are as short as cache read cycles.

CACHE MEMORY DESIGN: PERFORMANCE

Even a simple cache memory can improve system performance. For a simple, 16-bit cache system such as described above, a hit rate (percentage of read cycles that are from the cache) of 68% can be expected. If IDT7174 Cache Tag RAMs and IDT7164 cache data RAMs are used, an access time at the chip level of 35ns results and a corresponding system cache read or write cycle time of 50ns is practical. Assuming a system cache access time of 50ns and a main memory system access time of 250ns, the average access time of an unbuffered cache would be 134ns and the average access time of a buffered cache would be 104ns. This corresponds to an improvement in access time of 1.9:1 and 2.4:1, respectively.

CACHE DESIGN DETAILS: CONTROL LOGIC

Figure 3 shows a block diagram of a control logic design and a typical timing diagram for the cache memory of Figure 2. The vertical lines in the timing diagram represent 50ns timing intervals. The microprocessor is assumed to have a 50ns clock and a 100ns memory cycle time. In the timing diagram and associated logic, a Read/Write Timing signal is used to determine whether to use the cache data or to start the main memory. This timing signal is the memory read/write request signal from the CPU delayed by 37ns; the address-to-match time of the IDT7174. If main memory is used, this timing signal is used to write the main memory data into the cache RAMs on both the main memory read and write cycles. Data is written into the cache on write cycles only if there is a match or if it is a word write operation. The state of the MATCH line is latched by the Read/write Timing signal so that it remains stable during cache write operations.

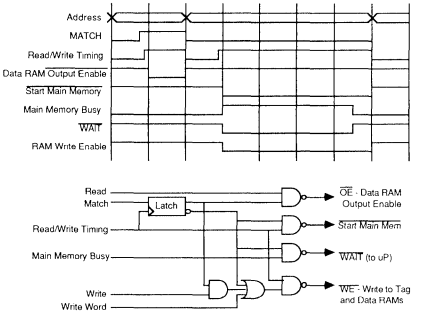

Figure 3: Cache Memory Control Timing and Logic Block Diagrams

CACHE DESIGN DETAILS: UNCACHED ADDRESSES

In the above cache design, we have assumed that all parts of memory are cached; however, there are significant exceptions to this assumption. Hardware I/O addresses should not be cached because they do not respond in the same way as normal memory locations. Bits in an I/O register can and must change at any time, asynchronously, with respect to the rest of the system. A cache copy of an earlier I/O state is clearly not a valid response to an I/O read request under these conditions. Also, an I/O register address may be used for different functions for read and write, so that what is read will not be the same as what was written. For example, write-only control bits will not appear when read, and read-only bits will not be affected by write operations. For these reasons, hardware I/O addresses must always force cache misses. This can be accomplished by adding an I/O address decoder to the memory address bus to force a cache miss. (This decoder aleady exists in many systems to enable the I/O subsystem.)

CACHE DESIGN DETAILS: DMA ADDRESSES

Direct Memory Access (DMA) allows I/O devices such as disk controllers to have direct access to main memory by temporarily stopping the CPU and taking control of the memory address and data busses. If DMA devices are allowed to write into main memory without updating the cache memory, cache data could become invalidated because it would no longer be a copy of the

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contents of main memory. The simplest solution to this problem is to have the cache monitor the memory bus and be updated if an address match occurs in the same manner as CPU write-through operations. Otherwise, the I/O DMA buffer areas of memory must be forced to be uncached in the same manner as hardware I/O addresses.

CACHE DESIGN DETAILS: EXPANDING THE CACHE IN WIDTH

The cache as described above, can be expanded in both width and depth. For a 32-bit system, two additional IDT7164 cache data RAMs (for a total of 4 chips) will be required to store the 32-bit data words. A block diagram of a 32-bit cache system, with a 32-bit address bus, is shown in Figure 4. Compared with Figure 2, the number of cache data RAMs has been expanded from two to four to handle the expansion of the data bus from 16 to 32 bits, and the number of cache tag RAMs has been expanded from two to three to handle the expansion of the address bus from 24 to 32 bits.

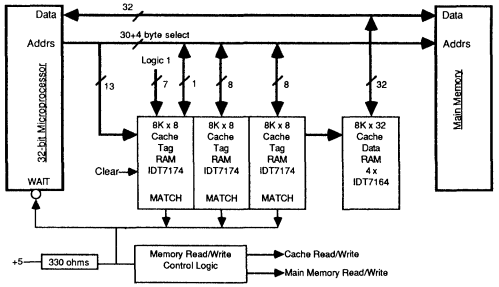

Figure 4: 32-Bit Cache Memory System

Note that the cache memory system uses the memory address lines corresponding to the 32-bit words stored in the cache. If a byte addressing memory address convention is used, the least significant bit of the address lines going to the cache RAM chips is A2, with A1 and A0 used to select the byte(s) within the word to be read or written in the cache data RAMs.

There is a benefit to expanding the cache width by adding data RAMs: the miss rate improves. The miss rate improves because of the increase in width, as well as in the amount of data stored. The miss rate for a 8K x 32-bit cache is estimated at 12.4%, as compared to 32% for a 8K x 16-bit cache. Doubling the cache width by adding RAM chips doubles the amount of data stored. We would expect an improvement in miss rate due to the increased probability of finding the data in the cache.

There is an additional improvement in miss rate, however, specifically due to the increase in width. This is because there is a high probability that the next word the CPU wants is the next word after the current one. If the cache width is doubled, there is a 50% probability that the next word is already in the cache, fetched from main memory along with the current word.

Studies have shown that the miss rate is cut almost in half for each doubling of the cache data word width — called line size in cache theory — up to 16 bytes and larger (Smith 85). The disadvantage of very wide cache data word width is either a wide main memory data bus or complex logic to transfer the word to the cache in a high-speed serial burst. Simply doubling the number of main memory cycles does not work well because you have doubled the effective access time of the main memory but have cut the miss rate by less than half, yielding a net decrease in performance.

CACHE DESIGN DETAILS: EXPANDING THE CACHE IN DEPTH

The cache memory can be expanded in depth by adding copies of the cache tag and data chips and using upper bits of the address bus for chip enable selection. An example of an expanded cache is shown in Figure 5. The primary reason for increasing the size of the cache memory is to decrease the miss rate percentage. For example, increasing the cache size from 8K x 16 to 16K x 16 decreases the estimated miss rate from 32% to 22%.

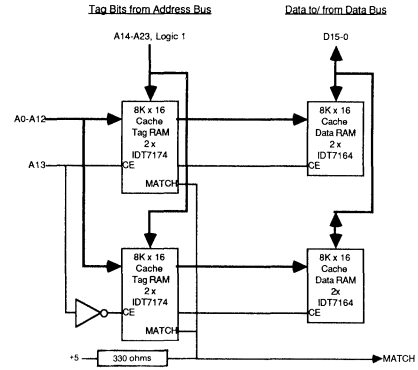

Figure 5: Depth Expanded Cache Memory System

CACHE DESIGN DETAILS: SET ASSOCIATIVE EXPANSION

A better way to expand the cache memory in depth is called set associative expansion (shown in Figure 6), and its control logic (shown in Figure 7). In this example, we have two independent cache memories which results in a two-way set associative cache. If a match is found in one of the memories, its data is gated to the data bus. If no match is found, one of the two memories is selected and updated. Selection of one of the two memories for cache write update is done by using an additional 8K x 1 memory to hold a flag for each cache word, indicating which memory was read last. This way, the least recently used cache word of the pair is updated.

The cache system described above attacks the problem of having two frequently used words mapped to the same cache word. For example, if a program loop included an instruction at 200B2 (hexadecimal) and called a subroutine at 800B2, the cache word 00B2 would be alternately registered as a cache miss and updated with memory data from each of these two addresses. The above design solves this problem by having two independent memories. One would cache the instruction at 200B2 and the other would cache 800B2.

Two way set associative expansion, while more complex in control logic, achieves a better miss rate. For example, the estimated miss rate for a 16K x 16 set associative cache is 18% versus 22% for a simple 16K x 16 cache.

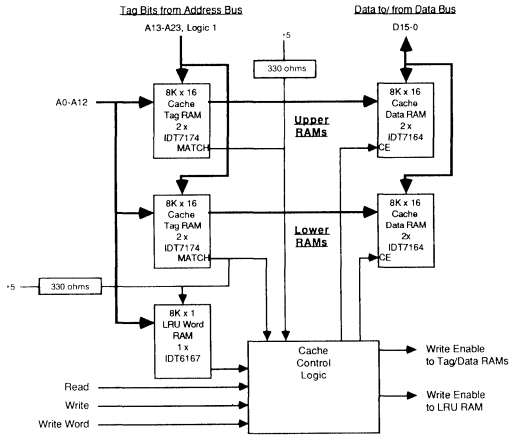

Figure 6: 2-Way Set Associative Cache Memory System

FUNCTION	MATCH	ACTION
Read	Yes	Enable corresponding data RAM for read
Write	Yes	Enable corresponding data RAM for write
Read	No	Write main memory data into LRU RAM
Write Word	No	Write data into LRU RAM

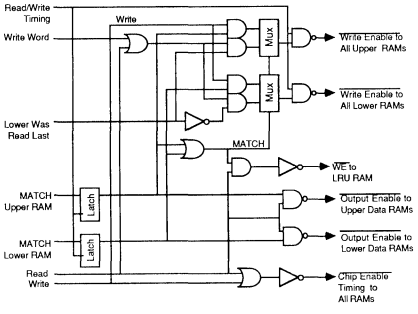

Figure 7: 2-Way Set Associative Cache Control Logic Block Diagram

CACHE THEORY: HOW IT WORKS

A cache memory cell holds a copy of one word of data corresponding to a particular address in main memory. It will respond with this word if the address on the main memory address bus matches the address of the word stored. A cache memory cell therefore has three components. These components are an address memory cell, an address comparator, and a data memory cell, as shown in Figure 8. The data and address memory cells record the cached data and its corresponding address in main memory. The address comparator checks the address cell contents against the address on the memory address bus. If they match, the contents of the data cell are placed on the data bus.

An ideal cache memory would have a large number of cache memory cells with each of them holding a copy of the most frequently used main memory data. This type of cache memory is called fully associative because access to the data in each memory cell is through its associated, stored address. This type of memory is expensive to build because the address cell and address comparator are generally several times larger, in terms of chip area or part count, than the data cell. Also, the address comparator required for each associative memory cell makes the design of the cell different from that of standard RAM memory cells. This makes a fully associative memory a custom design, precluding the use of efficient standard RAM designs.

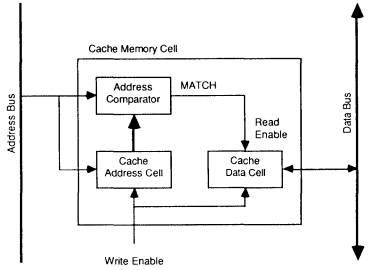

Figure 8: Cache Memory Cell Block Diagram

CACHE THEORY: WHY IT WORKS

Cache memories work because computer programs spend most of their memory cycles accessing a very small part of the memory. This is because most of the time the computer is executing instructions in program loops and using local variables for calculation. Because of this observation, a 64K byte cache can have a 90+% hit rate on programs that are megabytes in size.

HOW THE DIRECT MAPPED CACHE WORKS

The direct mapped cache memory is an alternative to the associative cache memory which uses a single address comparator for the cache memory system and standard RAM cells for the address and data cells. The direct mapped cache is based on an idea borrowed from software called hash coding which is a method for simulating an associative memory. In a hash coding approach, the memory address space is divided into a number of sets of words with the goal of each set having no more than one word of most-frequently-used data. In our case, there are 8K sets of 2048 words each.

Each set is assigned an index number derived from the main memory address by a calculation which is called the hashing algorithm. This algorithm is chosen to maximize the probability that each set has no more than one word of most-frequently-used data. In the direct mapped cache, the hashing algorithm uses the least significant bits of the memory address as the set number. This uses the concept of locality, which assumes that the most often used instructions and data are clustered in memory. If locality holds, the least significant bits of the address should be able to divide this cluster into individual words and assign each one to a separate set.

A memory map of a direct mapped cache of Figure 2 is shown in Figure 9 as an example of how the main memory words are related to the cache words. The 16M Word main memory is divided into 8K word pages, a total of 2048 pages. Each word within each 8K page is mapped to its corresponding word in the 8K words of the cache; i.e., word 0 of the cache corresponds to word 0 in each of the 2048 pages (8K sets at 2048 words/set).

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Each word in the cache stores one word out of its set of 2048 corresponding to one of the 2048 possible pages. Both the data word and the page number (i.e. upper address bits), are stored.

Since only one word in each set (one of 2048 words in our case) is assumed to be one of the most-frequently-used words, each set has a single cache memory cell associated with it. This cache cell consists of an address cell and a data cell, but no comparator. One comparator is used for the cache memory system since only one set can be selected for a given memory cycle and only one comparison need be made. In a memory cycle, one set is selected, and the single cache address cell for that set is read and compared against the memory address, and the data from the cache data cell is placed on the bus if there is a match. The advantage of this scheme is that a single comparator is used, allowing standard RAM memories to be used to store the cache address and data for each set.

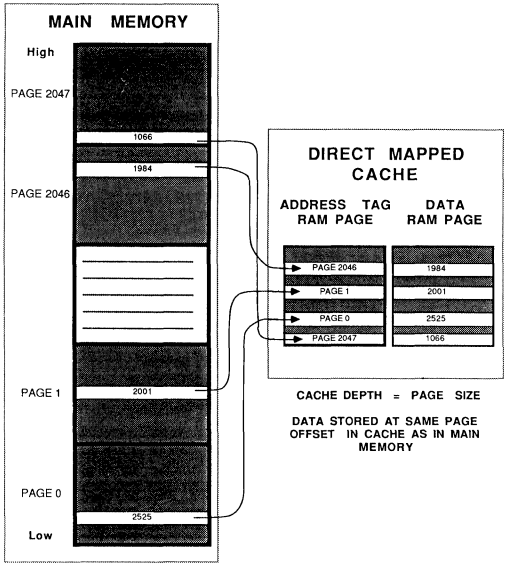

Figure 9: Cache System Memory Map

The cache cell for each set should hold the data that was most frequently used. However, since we do not know which data was the most frequently used until after the program is run, we approximate it by storing the most recently used data and replacing the least recently used (oldest) data. In the direct mapped cache, this is done by replacing the cache cell contents with the newer main memory data in the case of a cache miss.

CACHE PERFORMANCE

A cache memory improves a system by making data available from a small, high-speed memory sooner than would otherwise be possible from a larger, slower main memory. The performance of a cache memory system depends upon the speed of the cache memory relative to the speed of the main memory and on the hit rate or percentage of memory cycles that are serviced by the cache.

The cache performance equations below express the idea that the average speed of the cache memory is the weighted average of the cycle times for cache hits plus the main memory time for cache misses, with memory writes dealt with as a special case of 100% cache miss or 100% cache hit for the unbuffered and buffered cases, respectively.

CACHE SYSTEM PERFORMANCE: MISS RATE

One of the key parameters in a cache memory system is the miss rate. Miss rate figures are estimates derived from statistical studies of cache memory systems. The miss rate is an estimate because it varies, often significantly, with the program being run. Miss rate estimates for various cache memory configurations are given in Table 1. Miss rates for one example of two-way set associative expansion are also shown in this table.

Size: Words/Tag RAM	Miss Rate for Cache Data Word Width - Bits				Notes
	16	32	64	128	
2K	0.57	0.23	0.10	0.04	
4K	0.40	0.18	0.07	<0.04	
8K	0.32	0.12	0.05	<0.04	
16K	0.22	0.09	<0.04	<0.04	
16K (8K + 8K)	0.18	0.07	<0.04	<0.04	2-way Set Assoc

Table 1.

The miss rate estimates given in Table 1 are derived from simulation studies. (See references.) These studies covered cache sizes of up to 32K bytes and cache data word widths (called line sizes in cache terminology) from 4 bytes through 64 bytes. In the case of 16-bit word width caches, the figures given are extrapolations from the 32-bit data. Also, the figures for cache sizes above 32K bytes (i.e., 16K x 32, etc.) are extrapolations from 32K byte data.

CACHE SYSTEM PERFORMANCE FOR READ CYCLES

Cache memory system performance is determined by the access time of the main memory, the access time of the cache, the miss rate (the percentage of memory cycles that are not serviced by the cache) and the write time. The effective access time of a cache memory system can be expressed as a fraction of the main memory access time. This dimensionless number, Ps, is a measure of cache performance. If we consider read cycles only, the access time of a cache memory system is:

$$Ts = (1 - M)Tc + MTm = \underline{(1 - M)Tc + MTm}$$

$$Ps = Ts/Tm = (1 - M)\ (Tc/Tm) + M = \underline{(1 - M)Pc + M}$$

Where:

- Ts = Cache average system cycle time, averaged over read and write
- M = Miss rate of cache
- Tc = Cache cycle time, read or write (assumed to be equal)
- Tm = Main memory cycle time, read or write (assumed to be equal)
- Pc = Cache memory access time as a fraction of main memory cycle time
- Ps = Cache system access time as a fraction of main memory access time

If the miss rate of a cache memory is 100%, Pc = 1.00. If the cache memory is infinitely fast corresponding to a cache access time of zero, Pc will be equal to the miss rate, M. For real cache memories, the access time of the cache is finite. This means that the cache system access time will approach the cache access time as the miss rate approaches zero. This is shown in Figure 10.

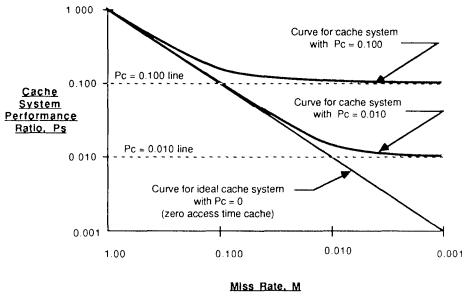

Figure 10: Cache Access Time vs Miss Rate for Read Cycles

CACHE SYSTEM PERFORMANCE FOR READ AND WRITE CYCLES

Memory write cycles affect the average access time of the cache system. In a write-through design, unbuffered write cycles are equivalent to cache misses, while buffered write cycles are equivalent to cache hits. Unbuffered write cycles take a main memory cycle to write data for every write. If the main memory write cycle time is the same as the read cycle time, this is equivalent to a cache miss. In buffered write, data is written into the cache and into a register for later off-line write into the memory. Thus, the write cycle in the buffered write case is equivalent to a cache cycle. Each write cycle in the buffered case is, therefore, equivalent to a cache hit. The performance equations for this case are:

$$Ps = R((1 - M)Pc + M) + W(Tw/Tm)$$

For unbuffered writes:

$$Ps = R((1 - M)Pc + M) + W$$

For buffered writes:

$$Ps = R((1 - M)Pc + M) + WPc$$

Where:

R = Fraction of total memory cycles that are read cycles
W = Fraction of total memory cycles that are write cycles
Tw = Write time = Tm for unbuffered, Tc for buffered writes

The effect of unbuffered write cycles is to limit the maximum performance of the cache system. For the average case where write cycles are approximately 15% of the total number of memory cycles, this is approximately equivalent to a cache memory performance of 0.15, as shown in Figure 11.

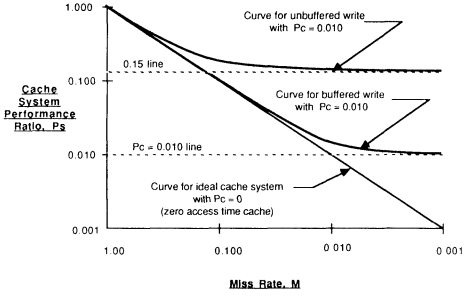

Figure 11: Cache Access Time vs Miss Rate for Buffered and Unbuffered Write Cycles

CACHE SYSTEM PERFORMANCE IN TERMS OF AVERAGE MEMORY ACCESS TIME

Although cache memory systems can be evaluated in terms of the dimensionless performance parameter, Ps, you often need to calculate the actual access time for a specific system. This is expressed by:

$$Ts = R((1 - M) Tcr + MTmr) + WTw$$

Where:

Ts = Cache average system cycle time, averaged over read and write
R = Percentage of memory cycles which are read cycles = 85% typical
W = Percentage of memory cycles which are write cycles = 15% typical
M = Miss rate of cache = 10+% typical
Tcr = Cache read cycle time
Tmr = Main memory read cycle time
Tw = Write cycle time: main memory for unbuffered write, cache for buffered

For typical values:

$$Ts = 0.85(0.9Tcr + 0.1\%mr) + 0.15Tw$$
$$= \underline{0.765Tcr + 0.085Tmr + 0.15Tw}$$

For unbuffered write and Tcr = 50ns, Tmr = Tw = 250ns:

$$Ts = 0.765(50) + 0.085(250) + 0.15(250) = \underline{97.0ns}$$

For buffered write and Tcr = Tw = 50ns, Tmr = 250ns:

$$Ts = 0.765(50) + 0.085(250) + 0.15(50) = \underline{67.0ns}$$

CACHE SYSTEM PERFORMANCE IN TERMS OF CPU WAIT STATES

In many computer and microprocessor systems, the purpose of the cache memory system is to eliminate CPU wait states, clock periods where the processor is stopped waiting for the memory. The cache performance calculations for this condition are more properly expressed in terms of processor wait states as follows:

$$Ncw = R((1 - M) Ncr + (1 - H)Nmr) + WNw$$
$$= RMNmr + WNw \quad \text{If: Ncr = 0 (no wait states for cache)}$$

Where:

Ncw = CPU average number of wait states, averaged over read and write
R = Percentage of memory cycles which are read cycles = 85% typical
W = Percentage of memory cycles which are write cycles = 15% typical
M = Miss rate of cache = 10+% typical
Ncr = Cache read cycle time wait states (typically 0)
Nmr = Main memory read cycle wait states
Nw = Write cycle wait states: main memory wait states for unbuffered write, cache wait states for buffered

For unbuffered write and Ncr = 0 wait states, Nmr = 3 wait states:

$$Ncw = 0.085(3)\ 1m1\ .15(3) = \underline{0.535 \text{ wait states}}$$

For buffered write and Ncr = Nw = 0 wait states, Nmr = 3 wait states:

$$Ncw = 0.085(3) + .15(0) = \underline{0.255 \text{ wait states}}$$

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CACHE SYSTEM PERFORMANCE IN TERMS OF CPU THROUGHPUT

The reason for adding a cache to a CPU is to improve throughput by eliminating wait states. CPU throughput improvement, as a result of adding a cache, can be expressed as the ratio of the speeds before and after adding the cache. For our purposes, CPU throughput improvement can be equated to memory throughput improvement. CPU throughput for this case can be defined as the CPU clock frequency divided by the number of clock states per memory cycle. The speed improvement provided by the cache can therefore be expressed as the ratio of the throughput with the reduced number of wait states provided by the cache to the throughput with full wait states:

$$Fc = \frac{fclk/(No + Ncw)}{fclk/(No + Nm)}$$

$$= (No + Nm)/(No + Ncw)$$

Where:

fclk = Frequency of processor clock
N = Number of clock cycles per memory cycle
Ncw = Number of wait states for cache system (average)
Nm = Number of wait states for main memory
No = Number of processor states per memory cycle with no wait states
Fc = Processor throughput relative to throughput without cache

A 68010 microprocessor requires four clock states per memory cycle, i.e. No = 4. Assuming a 12.5MHz clock and 250ns main memory access time, Nm = 2 wait states. If we use the unbuffered write case from the clock state analysis above, Ncw = 0.535. The throughput improvement provided by the cache is therefore:

Fc = (4 + 2)/(4 + 0.535) = 6/4.535 = 1.32 = 32% throughput increase

This is equivalent to increasing the CPU clock speed from 12.5MHz to 16.5MHz.

CACHE MEMORY PERFORMANCE: HOW MUCH DO YOU NEED?

A simple, direct mapped cache memory system, as described above, is often the most cost effective design. In many cases, the effort to decrease the miss rate beyond that of a simple design may not be worth the increase in system performance.

For example, if Pc is greater than 0.20 corresponding to a cache access time greater than 20% of the main memory access time, it may not be cost effective to improve the hit rate above 90%. This is because there is a knee in the curve of performance improvement versus miss rate at the point where Pc = miss rate, as shown in Figure 10. In some cases, even the added expense of buffered write may not be justified. To examine the relationship between CPU throughput and miss rate, CPU thorughput improvement versus miss rate for various microprocessors is shown in Table 2.

Miss Rate	Throughput Relative to Uncached System			
	68010 Unbuffered	68010 Buffered	68020 Buffered	RISC Buffered
1.00	1.00	1.00	1.00	1.00
0.80	1.06	1.12	1.19	1.27
0.60	1.13	1.20	1.32	1.49
0.40	1.20	1.28	1.49	1.79
0.20	1.29	1.38	1.71	2.24
0.10	1.34	1.44	1.84	2.56
0.05	1.37	1.47	1.92	2.76
0.00	1.40	1.50	2.00	3.00

Table 2.

The data shown is for three CPU/cache systems. The 68010 microprocessor system has a 12.5MHz clock and a cache with unbuffered write. The 68020 system has a 16MHz clock and a buffered write cache. The RISC CPU assumes a 10MHz RISC computer with a 10MHz clock and a buffered write cache, and assumes one clock per memory cycle with wait states equal to an integral number of clock cycles.

Using the data in Table 2, we can make an interesting comparison between chip count and performance gained over an uncached system. Table 3 gives this comparison, showing the chip counts, miss ratios, and performance improvement gain for simple, depth expanded, and two-way set associative expanded caches. The chip counts given are for the cache tag and data RAM chips required, but do not include chip counts for the control logic. One RAM chip is added for the two-way set associative case for the least-recently-used cache flag RAM.

Tag RAM Size	68010 Unbuffered			68020 Buffered			RISC Buffered		
	Chips	Miss	Perf	Chips	Miss	Perf	Chips	Miss	Perf
8K	4	0.32	1.24	7	0.12	1.81	7	0.12	2.49
16K	8	0.22	1.28	14	0.09	1.86	14	0.09	2.60
8K+8K S.A.	9	0.17	1.31	15	0.07	1.89	15	0.07	2.68

Table 3.

Table 3 shows that the throughput improvement created by expanding the cache above a minimum chip count design is small. This table can be interpreted in two ways. In small systems where the goal is to achieve high-performance at minimum chip count, the table indicates that a mimum chip count cache is best since it buys the most performance improvement per chip; doubling the cache chip count purchased less than 10% further increase in performance in all cases. In larger systems where the goal is to achieve maximum performance at moderate chip count, the table indicates that a further increase in performance of 5-8% can be obtained by adding fewer than ten chips.

CACHE DESIGNS: DIFFERENT WAYS TO MAKE ONE

The cache memory described above is a direct mapped cache. It is a simple, commonly used design with respectable performance. Further investigation into the technology of cache memories will reveal a wealth of other approaches to cache design. Much of the variety comes from attempts to maximize the performance of relatively small cache memories typical of earlier technology. Fortunately, there exists some data to help sort out the relative value of the various approaches. This data is in the form of studies on cache memory performance as a function of cache size, organization, word width, etc., such as the excellent work done by Prof. Alan Jay Smith of the University of California

at Berkeley (see references). These studies provide background and insight on how to achieve the highest performance out of cache memory systems, as well as documentation of a wide variety of cache schemes which do and do not work. The following comments are intended to provide a simplified guide to, and summary of, some of this data. The following comments are, in large part, judgments and opinions derived from the data in various reports and do not necessarily reflect the opinions of the original authors of the data.

WHAT WE HAVE LEARNED ABOUT CACHE MEMORY DESIGN

A simple, direct mapped cache as discussed above will give good performance if it is large enough. The ultimate measure of cache memory performance is its effect on system cycle time, which is a function of cache cycle time relative to main memory cycle time and the hit rate of the cache. Given a cache cycle time, miss rate becomes the measure of cache performance. Improving cache perfomrance, therefore, means improving the hit rate. However, a simple design with a moderate miss rate may be sufficient for many applications, giving most of the performance improvement that could be achieved by a more sophisticated design.

Much of the work that has been done on cache architecture and design was aimed at maximizing the performance of relatively small caches, consistent with the capabilities of earlier technologies. With today's technology, in the form of chips such as the IDT7174, we can easily make large cache memories at low chip counts that are at the upper limit of the earlier technologies. As a result, much of the sophistication required in smaller cache designs, in order to achieve an acceptable hit rate, is not required in today's large cache designs.

CACHE ARCHITECTURE: DIRECT MAPPED vs SET ASSOCIATIVE

A pure cache memory should be an associative memory, where the cache contains all of the most recently used data words. The direct mapped and set associative designs are approximations to this which sometimes exclude recently used words when there is more than one frequently used word per set. Fortunately, the difference between associative, set associative and direct mapped can be quantified. The ratios of miss rates for set associative and fully associative, relative to the direct mapped case, are shown in Table 3A. For example, if the miss rate for a direct mapped design is estimated at 0.20, the miss rate for a two-way set associative design of the same size would be (0.78)(0.20) = 0.156.

What this chart tells us is that two-way set associative caches have a significant performance improvement over simple direct mapped caches, but there is little additional improvement beyond four-way set associative designs. As was noted earlier, the set associative method can often be included in depth expanded cache designs where the two (or more) sets of cache hardware required for the expansion can be arranged to work in a set associative manner.

Cache Type	Ratio of Miss Rate to Direct Mapped
Direct Mapped	1.00
2-Way Set Assoc	0.78
4-Way Set Assoc	0.70
8-Way Set Assoc	0.67
Fully Associative	0.66

Table 3a.

CACHE SIZE

Cache sizes on commercial systems have tended to range from 16K to 64K bytes. Caches smaller than 16K can have significantly higher miss rates, while caches larger than 64K may not significantly improve the miss rate. This is shown above in Table 1. Much work has been done on the relationship between cache size and miss rate; however, most of this work is concerned with small caches, 32K bytes and under. The IDT7164/IDT7174 combination allows 16K byte cache memory design for 16-bit systems and a 32K-byte design for 32-bit systems using a minimum number of chips, and can be easily expanded to 64K and larger if desired.

WRITE THROUGH vs COPY BACK

There are two general approaches to handling the memory write problem: write through and copy back. In the write through approach, memory data is written into main memory as it is received from the CPU. In the copy back mode, memory data is written into the cache and flagged with a "dirty write" bit which indicates that the word has been written into the cache but not into the main memory. The cache data is copied into main memory as a separate operation at some later time, and the dirty write bit is cleared. There appears to be little performance difference between the write through and copy back approaches. Since the write through approach is simpler in concept and easier to implement, it is the most often used method.

WRITE BUFFERING

A significant performance increase can be achieved with a single level of write buffering. Complete write buffering requires more than one level of buffering to cover the case of two write cycles closer together than the main memory write cycle time. A FIFO can be used to buffer more than one word of write data; however, the FIFO need be no deeper than four words, since no further performance results from making it deeper.

SPLITTING THE CACHE: INSTRUCTION/DATA, SUPERVISOR/USER

Splitting the cache into two smaller caches, one for instructions and one for data, seems like it would improve the hit rate; however, it doesn't. In theory, the CPU spends most of its instruction cycles in a small part of the program. By caching these separately from the more random data memory, the hit rate on the instruction portion should be improved. Alas, the studies show that splitting the cache into two pieces typically does no better — and in some cases does a lot worse — than leaving the cache in one piece. This is, perhaps, because the miss rate for data is degraded by more than the hit rate for instructions is improved.

LINE SIZE: MAIN MEMORY WORD WIDTH vs CACHE WORD WIDTH

We have considered cache sizes where the CPU word width, memory word width and cache data word width are the same size. Performance improvement can result if the main memory and cache words are wider than the CPU word. If the cache word width (called the line size) is doubled the miss rate is cut almost in half. This is because the next word the CPU wants from memory is often the word adjacent to the one it just used. Increasing the

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line size by a factor of two will lower the miss rate by almost a factor of two up to line sizes of 16 bytes and beyond. This is shown in Table 4.

Cache Size in Bytes	Miss Ratio Reduction for Increasing Line Size			
	Line Size (Size of Block From Main Mem to Cache)			
	4 bytes	8 bytes	16 bytes	32 bytes
4K	1.00	0.586	0.364	0.262
8K	1.00	0.581	0.345	0.222
16K	1.00	0.569	0.330	0.203
32K	1.00	0.564	0.324	0.194

Table 4.

There are two approaches to increasing line size in order to reduce miss rate: by increasing the memory data bus width, and by fetching a block rather than a word of data from memory. Increasing the data bus width (from 16 to 32 bits, for example) may be practical in some systems where additional performance is desired.

The other alternative is to transfer a block of bytes to the cache instead of a single word. This becomes significant in systems where there is a delay before data transfer from main memory, but where several words can be transferred quickly after the initial delay. An example of this concept is the page mode in dynamic RAM designs. In such a system, there may be an initial latency of 200ns to begin a memory read cycle but, once started, the memory may be able to transfer words at 100ns per word for blocks of up to 256 words. In this case, a line (block) size of 2-4 words may be used to significantly reduce the miss rate with moderate increase in the main memory cycle time.

SUMMARY

Cache memories have been extensively used in large computer systems to improve performance. Cache tag RAM chips allow this technology to be adapted to the small-to-medium system design at reasonable cost. Simple, direct mapped cache designs with low chip counts can be used to achieve significant performance improvements. High-performance and low miss rates are possible with simple designs due to the high speed and relatively large cache sizes possible with high-speed CMOS technology.

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Integrated Device Technology, Inc

USING TWO CHIP SELECTS ON THE IDT7198

TECH NOTE

By John R. Mick

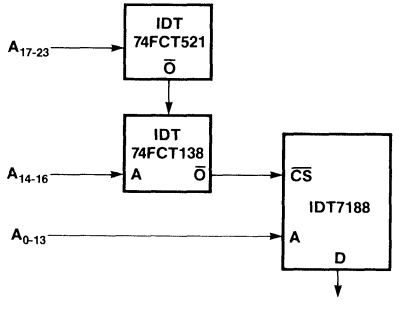
The IDT7198 is a high-performance 64K CMOS static RAM. Compared to the standard 16K x 4 static RAM, it features two active low chip selects and an active low output enable. These additional features provide the designer with a capability that he can use to improve system speed.

The output enable can be used in systems to gate the RAM data onto the bus at the required time. It is independent of the memory access time and thus can be brought low (enabled) later in the memory cycle. This means that other bus activity could be present during the initial part of the access time of the RAM. The benefit here, of course, is maximum bandwidth on the bus.

The advantages of two chip selects are probably not as obvious as the use of an output enable control signal. The second chip select can be used to advantage in high order address decoding or memory block decoding and provides the opportunity for these events to occur in parallel. This parallelism improves system speed at no increase in parts count. This is easily demonstrated in Figure 1. Here we see a memory with a single chip select, shown in Figure 1A, and a memory with two chip selects, shown in Figure 1B. Figure 1A shows the IDT74FCT521 8-bit identity comparator connected in series to the IDT74FCT138 3-line-to-8-line decoder. The output of the decoder is then connected to the single chip select of the RAM. This results in the access time of the memory being equal to the summation of the 3 devices in series. Figure 1B shows the same devices only the identity comparator and the 3-line-to-8-line decoder are each connected to one of the chip selects on the RAM. This results in the propagation delay of these devices occurring in parallel and thus improving the overall performance of the system. The comparative speed advantage is 9ns commercial and 12.5ns military, as shown in Figure 1.

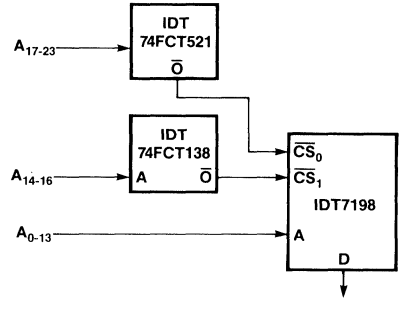
Another method for chip select decoding is shown in Figure 2. Here we see two IDT74FCT138s connected in a matrix arrangement. By using this technique, we are able to perform decoding on the equivalent of 64 different rows of RAM. Normally on a RAM with only one chip select this would require nine IDT74FCT138s. In this arrangement, only two IDT74FCT138s are needed; thus, a savings of seven devices results, with an improved propagation delay performance of one less device in the series.

From these design examples, the design engineer can see the advantages of two chip selects and an output enable.



		COM'L.	MIL.
IDT74FCT521	A → O	11ns	12.5ns
IDT74FCT138	E → O	9ns	14ns
IDT7188	$\overline{CS}$ → Data	35ns	45ns
		55ns	71.5ns

Figure 1A. Standard Memory Design Using One CS



		COM'L.	MIL.
IDT74FCT521	A → O	11ns	—
IDT74FCT138	E → O	—	14ns
IDT7188	CS → Data	35ns	45ns
		46ns	59ns
SPEED SAVINGS		9ns	12.5ns

Figure 1B. Higher-Speed Memory Design Using Two CSs

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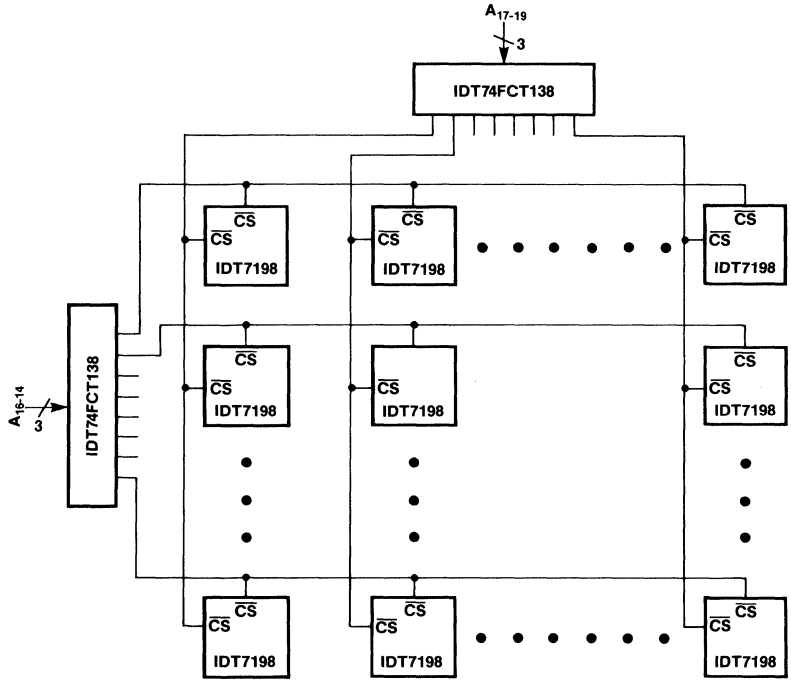

Figure 2.

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CMOS logic with bipolar-enhanced I/O rivals Fast TTL gates

Octal CMOS devices incorporating bipolar transistors race neck and neck with the best low-power Schottky packages on less than a tenth the operating power.

Although the evolving Schottky technology has progressed mightily in increasing the operating frequency limits of TTL devices, in the last reckoning the designer has been left to resolve the ever present problem of excess power. On the other hand, CMOS has advanced from its humble beginnings as a low-power, low-speed technology to the point where it can replace its TTL counterparts in many applications. The 54HCT (high-speed CMOS TTL-compatible) family, for example, has speed and output drive-current characteristics similar to parts in the LS category of TTL devices. Unfortunately, the designer must yet to some degree grapple with the various power-vs-performance considerations.

A new CMOS collection of octal buffers, latches, decoders, registers, and transceivers for supporting high-speed memories and data buses provides both the speed and output drive of 74F (Fast) parts at only a fraction of the operating power (Fig. 1). The IDT 54FCT (Fast CMOS TTL-compatible) family sports typical gate delays of 5 to 10 ns and delivers output currents of up to 48 mA over the full military range of voltage and temperature. With an average power consumption of 20 mW (or a few microwatts in the standby mode), it is also a viable alternative to Schottky and advanced Schottky devices.

The family's enhanced speed and output drive at low operating power are attributed to a proprietary 2-μm, dual-metal-gate process called CEMOS (see "Seeing Mostly Higher Speeds," p. 119), which is used to fabricate both input and output stages having the unusual combination of CMOS and bipolar devices. These components create stages with low capacitance that minimize input currents and output voltage swings, thereby creating low-power, high-speed gates (Fig. 2a). Multiple contacts to all drains and sources of the p-channel and n-channel devices involved are used to minimize the gates' internal resistance, thereby allowing them to drive larger loads than typical CMOS gates can. Particular attention is paid to keeping the gates' source resistance as low as possible, which has a first-order influence on drive because of the current-to-voltage feedback arrangement used in this family.

Of prime importance is the push-pull output stage, which employs two n-channel gates in parallel with an npn transistor and a small-signal p-channel device (Fig. 2b). The npn transistor clamps the output voltage to 4.3 V when loaded by a TTL device (assuming a 5-V supply). This configuration provides a high noise mar-

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gin for high-to-low signal transitions, even when the output is loaded heavily. Furthermore, the switching times are reduced because of the limited output swing.

Channeling the power

The most significant benefit of the series, however, is its power-conserving characteristics. The channel length of the 54FCT CMOS devices is generally less than their 54HCT predecessors and so are the resulting internal gate capacitances. The dynamic power consumed is therefore proportionally less. In the FCT family's push-pull output driver stage, the relatively large cross-over current required to switch a given device is greatly minimized by deskewing (offsetting) the predriver circuit. This unbalancing allows the device to switch at a fraction of the usual dynamic supply current. Even at 10 MHz, the dynamic power drawn by the IDTFCT 374 register buffer (which is the first device in the family) is only 6% of that required by a Fast 374 and only 3% of the AS374 (Fig. 3).

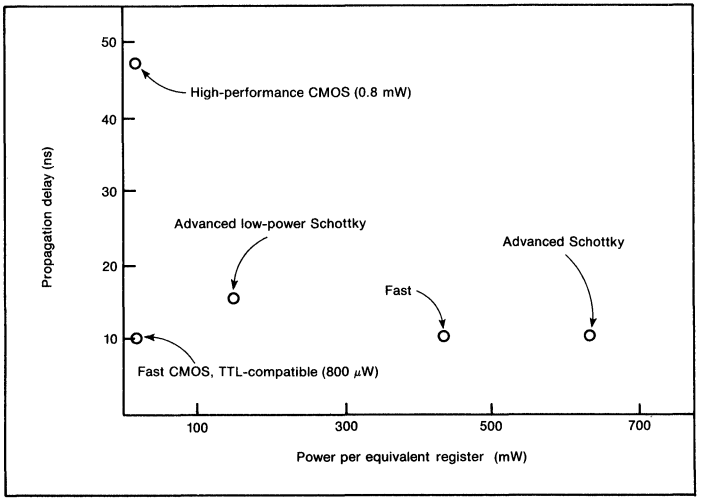
(Note that worst-case parameters are examined. It is much more useful to compare worst-case parameters than those commonly quoted for typical-value operation. The actual values of course, are determined by the circuit.)

When TTL devices drive a CMOS part, the latter's input buffer stage will draw power when the input voltage is other than equal to the supply voltage. When CMOS devices drive FCT parts, however, the static power dissipation is much lower. Specifically, in the case of a 374 driver, the maximum current drain is only 0.16 mA, as compared to 85 mA when the 374 drives the Fast part and 140 mA for the AS part.

Zilching the zaps

Each input has a 500-Ω resistor driving the junction of a grounded-base transistor and a grounded-gate n-channel device to protect all FCT devices against electrostatic discharges that reach 1000 V or more. The n channel is at a common point with the emitter of the npn transistor, and so the junction capacitances and input-switching times are minimized.

Latchup, also a concern in CMOS devices, is virtually eliminated. The FCT family will not



1. The FCT family of bipolar-enhanced CMOS parts delivers the speed and drive current of Fast, as well as of advanced and advanced low-power Schottky TTL devices, but consumes less than a hundredth the static operating power. They are at least four times faster than earlier high-speed CMOS parts.

Seeing mostly higher speeds

The CEMOS method uses a 2-μm, silicon-gate process to allow CMOS parts to work at almost twice their former speeds. CEMOS IIA, the version used for the FCT family, employs a two-layer metallization technique (see the figure). Smaller effective channel lengths make it about 40% faster than the previously used CEMOS I (2.5 μm) process.

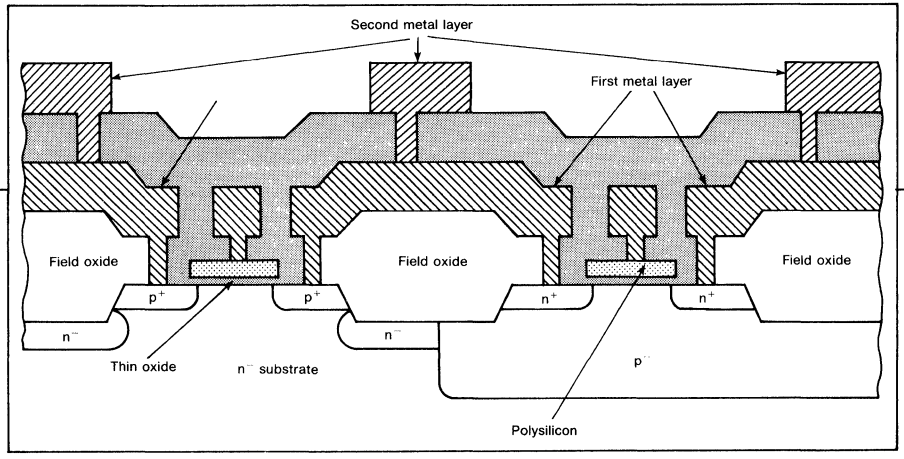
That process yields, for example, 54HCT138 decoders with propagation delays of 8 ns, 10-mA output drive, and 7-mW power dissipation over the full military range of temperature and voltage supply extremes. They operate more than 60% faster than currently available HCT decoders do and are comparable in speed to 54ALS bipolar devices. CEMOS IIB, a 1.5-μm version, is further expected to offer a 20% increase in speed for both the FCT and a class of 9- and 10-bit-wide devices compatible with the AM 29800 series, which are slated for release later this year.

The principal technologies that allow these finer lines, fewer defects, and higher density are wafer-stepping printing and the dry etching of thick films. The most usual approach to fabricating an IC is to cover a wafer with a photoresist and expose it to light passing through a mask that is about the same size as the wafer itself. This 1:1 technique presents problems in aligning the mask when the tolerances must be tight and when defects must be reduced to less than 5/in.^{2}.

These masking problems have been largely alleviated by using wafer stepping, in which an image about the size of a few individual dice is exposed to only a fraction of the total area of a wafer. The image is placed on a glass plate having a 1× reticle that contains 2 to 15 dice in a patterned chrome field. Then the plate is projected onto the wafer and is sequentially stepped until the whole wafer is exposed. Because only a small area of the wafer is exposed at any given time, more precise masks and optics can be used and mask defects can be greatly reduced.

In order to scale the process horizontally, a dry etch method is employed to maintain tighter control of the nitride, oxide, polysilicon, and aluminum films used. CEMOS II employs a plasma etcher, which uses an electric field to control an ion gas that etches only in the vertical plane. Thus much tighter geometries are permitted. This technique overcomes the main objections to the use of wet acids such as hydrofluoric, which etch laterally as well as vertically, thereby limiting the ability to produce finer lines.

In practice, CEMOS IIA deposits oxide at low temperature atop an etched pattern on the first metal layer. This layer is used extensively to reduce the resistance and inductance effects on internal supply lines, thus minimizing noise and internal delays. Interconnection vias are then plasma-etched into the oxide until the metal is exposed. A second layer of metal is then deposited. This top metal layer is etched with the pattern characteristic of the desired circuit.



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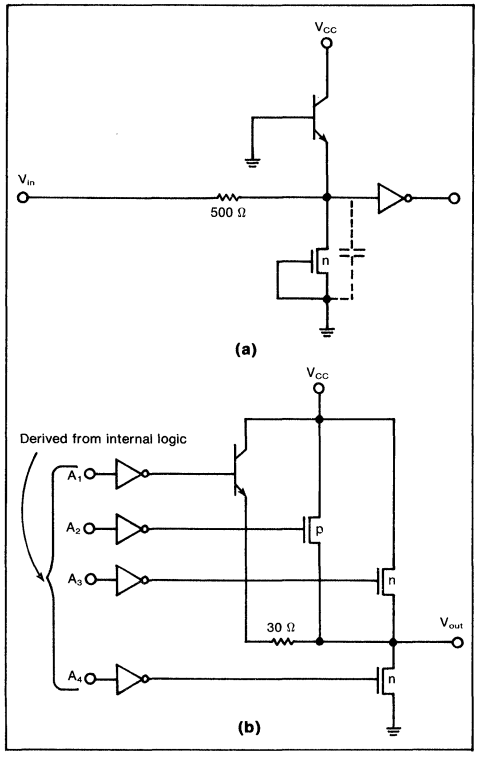
latch up, even for forced trigger currents as high as 300 mA (for worst-case conditions of 125°C and V_{CC} = 7 V). A second type of latch-up in CMOS devices, normally associated with excessive substrate current during fast switching, is also eliminated by judicious selection of supply voltages. Most CMOS devices suffering from this malady run at supply voltages of 9 to 12 V; the operating voltages of the FCT family, being compatible with TTL, run at 7 V.

Noise problems in a high-speed system containing FCT devices will be no worse than in a system built with Fast parts and will often yield an improvement. The designer need only adhere to standard grounding practices. To be more specific, he should use suitable supply and ground planes to reduce inductive supply noise and crosstalk in signal lines. Also, bypass capacitors should be deployed throughout, one per buffer and one for every pair of other logic-type devices.



2. A low-impedance RC circuit protects the standard input circuit of an FCT chip from electrostatic discharges exceeding 1000 V (a). An n-channel gate npn transistor stage keeps input capacitance low, and the push-pull output stage is configured to furnish a high noise margin (b). The npn transistor clamps output swing somewhat, to reduce the stage's switching times.

The value of the bypass capacitor is equal to It/V, where I is the output current of the device, t is the switching time, and V is the variation of supply voltage due to noise. Assume the dynamic load seen by an octal buffer is 50 Ω and the high-to-low output voltage transition is 4 V. Thus the current demand is 80 mA. For eight such devices in the part, each switched every 3 ns., the maximum current demand will be 640 mA. The required bypass value will thus be 0.02 μF, assuming that there is a 0.1-V drop in V_{CC} with noise.

As an added protection against ground noise, the FCT family has 300 mV of hysteresis in the clock and output enable lines. This amount of swing also guards against slow-rising clock pulses in heavily loaded enable lines. When the input voltage is near ground, the device increases V_{IH} by 0.3 V to raise the trip level. Once the stage switches, the trip level is lowered by 0.3 V. Thus, a slowly changing signal with noise on it will not falsely trigger the device.

Taking the long route

Unlike the case with most other logic families, the designer need not perform critical-path or power-management analysis when using FCT devices. Furthermore, the power consumed is virtually a function of only frequency, duty cycle, loading, and the voltage levels of the systems. If incoming signals are at low frequency and at logic levels that switch between the supply-rail values, the FCT devices will draw a maximum static current approximately equal to I_{CC} (that is, 160 μA). When operated at higher frequencies or at worst-case TTL output levels (or both), the device will draw more power, but the drain will still be well below the power drawn by the equivalent TTL device.

Still, several things must be borne in mind in interfacing these devices, especially with TTL parts, if the designer is to maximize the power

savings and minimize latch-up and noise.

Basically, direct interfacing of FCT parts with Fast TTL devices yields immediate advantages in noise immunity. The FCT's input stage exhibits a worst-case level of V_{IL} = 0.8 V and V_{IH} = 2.0 V over the entire specified range of temperature and voltage, the same as for TTL parts (Fig. 4). But the FCT devices draw an input current of less than 1 μA. When they are united with TTL devices, therefore, the latter's worst-case V_{OL} and V_{OH} levels will be close to their unloaded values of V_{OH} = 3 V, V_{OL} = 0.2 V. Consequently, the noise margin will be $V_{OH_{TTL}} - V_{IH_{FCT}}$ = 1 V and $V_{OL_{TTL}} - V_{IL_{FCT}}$ = 0.6 V on the high and low levels, respectively. Comparing these values with the Fast margins of 0.4 V and 0.3 V for TTL-TTL interfaces reveals that the TTL-FCT interface provides superior system noise margins.

When FCT parts are connected directly to Fast devices, the output level will be limited to about 4 V if I_{OH} is less than 1.5 mA. The corresponding fan-out is 75. A greater noise margin (2 V) is thus maintained because the output impedance of the FCT device is lower. For low logic levels, the noise margin is at least 3 V.

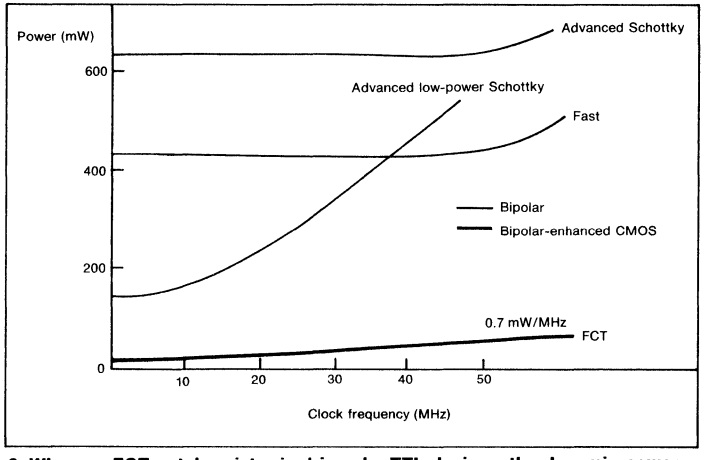
CMOS parts can be united with conventional FCT interfaces, too, but at a sacrifice in noise margin, because the FCT's trip level is much lower.

Of course, the best noise immunity is achieved when a complete FCT logic system is integrated, in which case the noise margins are 2.2 V and 0.6 V. Although the power drain of FCTs is inherently well below that of TTL, the designer may utilize several techniques to reduce it further. The total power drawn by an FCT-TTL interface is given by:

$$P = V_{CC}I_{CC_{CMOS}} + V_{CC}I_{CC_{TTL}}ND + V_{CC}{}^2 f C_{PD} + V_O{}^2 f C_L$$

where I_{CC} relates to quiescent current values for the respective CMOS and TTL input requirements, N is the number of TTL inputs above V_{IH} at any given time, D is the duty cycle, and f is the operating frequency. The summed internal capacitance of all stages of the device being driven is C_{PD}, V_O is the output voltage swing, and C_L is the capacitance of the output stage.

The obvious ways to reduce power dissipation are thus to lower the frequency of operation, reduce the input duty cycle, or lower the number of inputs that remain high at TTL levels. Low-level input signals, especially those that suffer from transient ringing, should be limited to



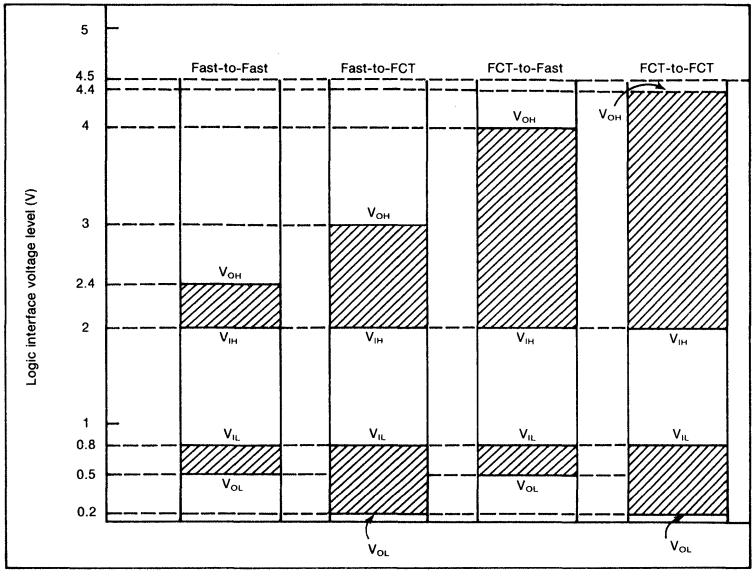
3. When an FCT octal register is driven by TTL devices, the dynamic power drain of each stage is less than 6% that of a Fast register and only 3% that of AS parts, below 10 MHz. The power consumed by the FCT register when driven by CMOS parts is less than 1% that of Fast and AS registers.

0.5 V below V_{SS}. The input protection afforded by the FCT npn transistor will limit the voltage internally, but additional current may flow through the V_{CC} terminal.

For high-level logic levels, there is no extra current flow because the n-channel device breaks down at about 15 V. Nevertheless, input ringing should be limited if the noise margin is to be maintained.

Other techniques include reducing rise and fall times and limiting the number of dc current paths in a given circuit design. No matter what power-conserving methods taken, the FCT-TTL interface will consume no more than one tenth the power of its FAST-TTL and AS-TTL counterparts. Consider the case where a 374 shift register drives a 50-pF load on a bus running at 10 MHz. Assume that half of the registers switch at the worst-case V_{OH} value of 2.4 V, which represents a heavy TTL load of 1 mA. Also assume that the duty cycle is 50%. Thus $I_{CC_{CMOS}} = 160\,\mu A$, $I_{CC_{TTL}} = 1$ mA, N = 4, D = ½, and $f = 10^7$. In addition, it is known that $C_{PD} = 30$ pF, all additional working registers have C_{PD} of 3(15) = 45 pF, and $C_L = 50(4) = 200$ pF. Given that $V_{CC} = 5.5$, and $V_O = 3.5$, then P = 47 mW. With Fast or AS devices replacing the FCT parts, P is found to equal 482 mW and 713 mW, respectively, given that $V_O = 3$.

The FCT device's output can also be connected directly to CMOS or any other conventional TTL devices. When the output voltage is below 1 V, the FCT presents an 8-Ω impedance to external buffers. The $I_{OL} = 60$ mA at 0.5 V; therefore the TTL fan-out is relatively high. Between 2 and 4 V, and FCT's npn and n-channel combination provides an I_{OH} of 30 mA for a V_{OH} of 2.4 V, and the resulting output impedance is 80 Ω. For high-level inputs ($V_{CC} - 0.2u$), the $I_{OH} = 100\,\mu A$; the resulting high output impedance is quite acceptable for interfacing to CMOS devices.□



4. FCT-to-FCT interfaces have the greatest immunity to noise, though both FCT-to-Fast and Fast-to-FCT setups yield acceptable results. Fast-to-Fast links, to date viewed as having a good noise margin, fall far short of the rest.

High-density modules suit military applications

Joe Kraus, Marketing Manager/Subsystems, Integrated Device Technology, Inc., Santa Clara, CA

The ability to produce integrated circuits meeting the high-reliability specifications associated with military systems has taken a number of years to develop. Special attention has always been given to the semiconductor process and circuit design techniques to stimulate the pursuit of the highest density and speed with the lowest power possible for monolithic devices.

This approach, however, is of a one-dimensional nature—an increasing demand in military systems for portability, miniaturization and battery operation is forcing the industry to take a closer look at the wide use of space-inefficient DIP packages.

One of the first approaches was to use flat packs. However, because of their highly flexible leads, many difficulties were incurred in testing and handling. Additionally, problems associated with manufacturing and processing increased the cost of flat packs beyond the budgets of all but the most area-limited military programs. Most recently, the apparent solution was the advent of leadless chip carriers (LCCs).

LCCs come on the scene

Around 1978, LCCs began to emerge as a viable packaging technique, allowing substantially higher board-level IC packing density and overall system weight reduction (see Figure 1). The thought was that not only would LCCs replace the cumbersome-to-test flat packs used in high-rel/high-density military programs, but would eventually find their way into commercial applications in which system size was of major concern.

This obviously did not come about, since system usage of LCCs is still small.

One of the main problems that has kept this idea from culminating as quickly as planned has been the lack of a variety of suitable methods to attach the LCCs to the PC boards—particularly in military applications requiring system temperature extremes, causing the difference in thermal coefficient of expansion (TCE) between the LCC and the polyimide PC board to dislodge the LCC (see Figure 2).

New packaging techniques

The solution was to develop packaging techniques that would take advantage of high-density LCCs while presenting a highly reliable component that could be mounted using traditional techniques. Recent advances in surface mounting techniques, and further understanding of the dislodged LCC phenomenon has given rise to a module approach. In a module, LCCs are mounted, top and bottom, to a cofired ceramic substrate matching the TCEs. The substrate has a dual-in-line pin out and thus can be mounted into the PC board using traditional soldering techniques. The module, therefore, allows packing density equivalent to, or higher than, LCCs with none of the disadvantages, achieving the perfect marriage of old and new packaging methods.

However, since military applications demand the highest level of reliability, this packaging technique can be thought of as a viable solution only after a thorough understanding of the problems.

Thermal coefficient of expansion problems

A better understanding of the mismatching of TCEs can be achieved by referring to Figure 3a. In a case where the system is seeing a large variation in temperature (temperature cycling), the LCC, constructed of cofired ceramic, will expand less than will the flexible polyimide PC board. This difference in expansion produces stresses that will be absorbed by the flexible solder joint. Given enough temperature cycles, though, the solder joints may fatigue to a point of electrical or even physical discontinuity. Matching the coefficient of expansion of the LCCs and the substrate or PC board can alleviate this concern. Integrated Device Technology's modular approach uses a ceramic substrate constructed of identical ceramic material and cofired in exactly the same fashion as the LCCs. As the system heats up and cools down, the LCCs and substrate expand and contract exactly the same amount (see Figure 4 for substrate construction).

Although temperature cycling problems can be lessened in this manner, a bigger problem can exist. Figures 3b and 3c represent differences in TCE that result from power cycling. In a power-up mode, the LCC will heat up at a much faster rate than the substrate since it is the LCC that is generating the heat. Until the heat can be transferred through the solder joints and into the

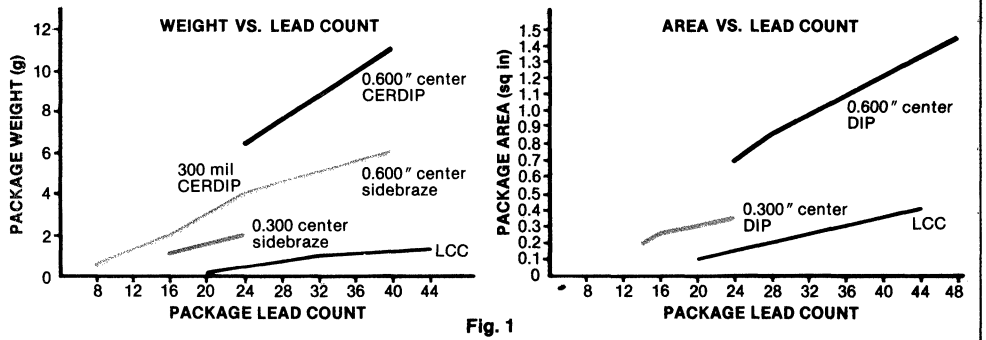


Fig. 1

THERMAL COEFFICIENTS OF EXPANSION

Material	C.O.E. × 10^{-6}/°C
White ceramic chip carriers (94-96% alumina)	6.3
Black ceramic chip carriers (90% alumina)	6.9
Copper clad Invar Porcelain Enameled Metal Substrates (PEMS)	6.8
Steel core PEMS	13.3

Fig. 2

COFIRED CERAMIC SUBSTRATE MANUFACTURING PROCESS

1)	**Green Sheet** (Green Tape)	Unsintered flexible raw ceramic sheet.
2)	**Tooling**	All necessary manufacturing tools such as punching tools, screening patterns, brazing fixtures and electrical test probes and fixtures.
3)	**Punching**	Via holes, cavities and other inside cutting in green sheet (layer by layer).
4)	**Via Hole**	Holes in ceramic layer filled with tungsten paste for electrical connection.
5)	**Cavity**	Recessed structure, such as die attach cavity.
6)	**Screen Printing**	Conductor lines/planes, various pads and markings etc. are printed with tungsten paste on green sheet surface (moly-manganese can also be printed after sintering).
7)	**Lamination**	Each layer of green sheet (with screen printed patterns and filled vias) is stacked in the design sequence and bonded together.
8)	**Shaping**	Cutting or punching operation of outside edge to separate each unit from the master array.
9)	**Scribing**	To groove surface for snap breaking.
10)	**Co-firing**	Simultaneous sintering of ceramic and tungsten metallization. Approximately 1,500 °C to 1,600 °C firing temperature in a reducing atmosphere.
11)	**Ni Plating** (Before brazing)	For better wetting of brazing alloy.
12)	**Brazing**	Bonding of lead frames to metallized pads with molten silver-copper eutectic alloy (or pure silver) at approximately 800 °C to 1,000 °C in a reducing atmosphere.
13)	**Finish Plating**	All exposed metal and metallization surfaces are electroless plated with desired metal for functional purpose and environmental protection.
14)	**Snap Breaking**	Separation of each unit from the master array along a predetermined scribe mark.
15)	**Edge Grinding**	Disconnection of plating tie-bar metallization with an abrasive tool.

Fig. 4.

THERMAL COEFFICIENT OF EXPANSION PROBLEM
(Length of arrow represents amount of stress)

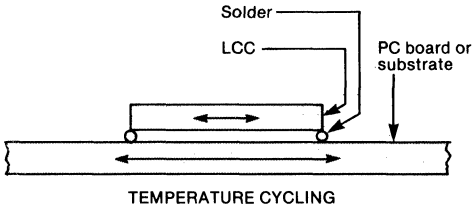


Fig. 3a.

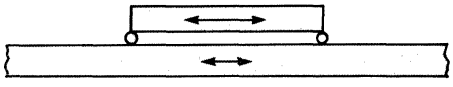


Fig. 3b.

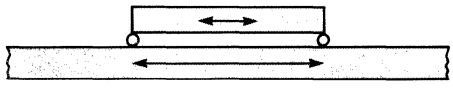


Fig. 3c.

HEAT TRANSFER METHODS

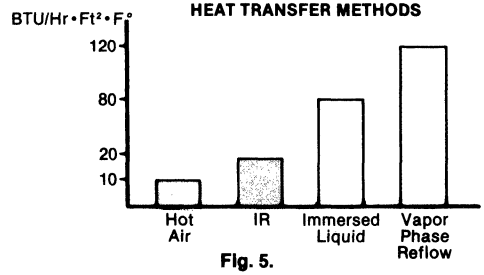


Fig. 5.

substrate, there will be a mismatch of temperature and thus a mismatch of expansion. Likewise, in a power-down mode, the LCC will cool faster than the substrate and again pose a mismatch situation.

Although there is no perfect solution to this problem, IDT has minimized its effect by using only extremely low-power CMOS components, thus reducing the total amount of heat generated by the LCC and limiting the mismatching of expansions.

Surface mounting techniques

No matter how much attention is given to the matching of TCEs, if the LCC is not mounted with the proper surface mounting technique, the solder joint will still become a source of problems. The proper surface mounting technique is one that will evenly heat substrate and LCC to the ideal temperature to flow the solder—with minimum overshoot. The ideal process would be easy to control, would remain clean, and would produce the most reliable solder joint possible. Several techniques were evaluated by IDT to determine the fastest, most efficient and, above all, most reliable.

Forced air—Either the LCC or substrate is screened with a tin/lead solder paste, assembled, then put in a hot air furnace to heat the module to the proper temperature, melting the solder. This technique of heat transfer is the most inefficient of all the methods (see Figure 5) and often leads to inadequate heating of the module, producing cold solder joints and inadequate wicking. Figure 6a shows a typical part using a forced air method. Notice the lack of solder on the gold contact of the LCC, and the appearance of "cold" solder joints, indicating improper heating.

Infrared—Similarly, presilk-screened LCCs are assembled onto the substrate and subjected to an IR heat source. In addition to being an inefficient method of heat transfer (see Figure 5), IR produces a "shadow" effect, i.e., LCCs shielded from the heat source by either the substrate or other LCCs see substantially lower heat than do the non-shielded LCCs. This produces temperature gradients in the module, risking the possibility of overheating some portions of the module and inadequately heating other portions.

Liquid immersion—Although a relatively effective method of heat transfer, liquid immersion is a very unclean process, leaving a substantial amount of residue on the module after solder reflow. Although the module can be cleaned, this procedure is often so harsh that it attacks critical areas of the assembly.

Vapor-phase reflow solder—Vapor-phase reflow solder is the method of choice. This is the most efficient method of heat transfer (see Figure 5) and produces the most reliable solder connection.

A vapor-phase reflow solder system (see Figure 7) consists of vapor chambers with a heating element at the bottom and a set of cooling coils located roughly ⅓ and ⅔ of the way up the sides. A liquid

Fig. 6a. Poor solder wicking and 'cold' solder joints using forced-air technique.

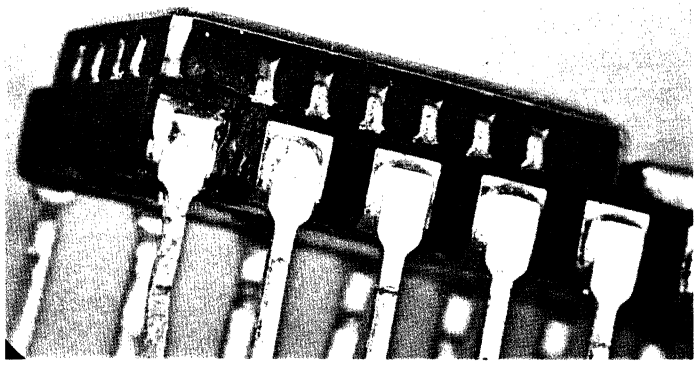
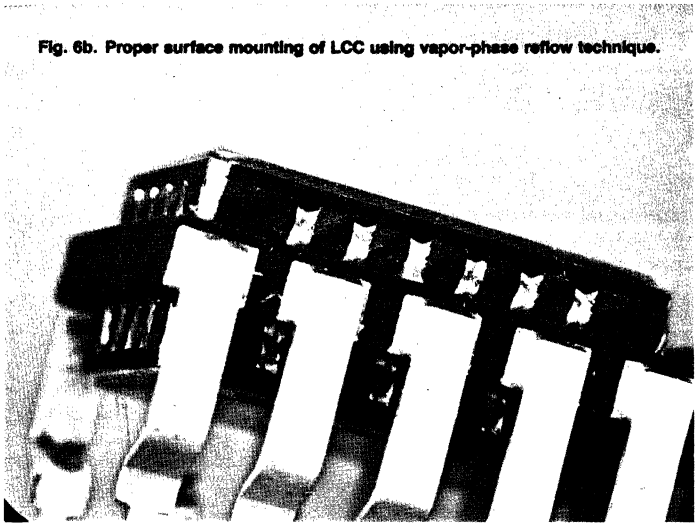


Fig. 6b. Proper surface mounting of LCC using vapor-phase reflow technique.



fluorinet (FC-70) is brought to its boiling temperature (419F) to form a vapor between the bottom of the chamber and the primary cooling coils. The primary cooling coils are kept at 125 to 175F, thus condensing the vapor to liquid to be reused.

However, when assemblies are lowered into the vapor, the vapor "blanket" is disturbed and very costly FC-70 is lost to the ventilation system. To minimize this loss, a second vapor "blanket" is formed between the primary and secondary coils consisting of trifluro ethane. Since trifluro ethane has a boiling point of 117F, it will not condense at the primary coils, but forms a secondary vapor that will condense only at the secondary coils kept at a well - controlled 60F.

Since the primary vapor (FC-70) is kept at 419F, when modules with LCCs mounted on them are lowered in the vapor, the tin/lead eutectic (melting point of 361F) melts and flows evenly. The principal of vapor-phase heating relies on the condensation of saturated vapor on the module. This condensation is accompanied by the release of the latent heat of vaporization which, in turn, causes the cool assembly to heat rapidly (10 to 30 sec) and uniformly.

Since the vapor condenses on all sides simultaneously, the shape of the module is not important. No temperature gradients are incurred, eliminating cold solder joints from too low a temperature, or dissolution of noble metals from too high a temperature. In fact, the 58F difference in temperature from the FC-70, and melting point of the tin/lead eutectic is ideal for maximum adhesion of the LCC (see Figure 6b). Studies indicate that in 1.5 million solder connections less than 0.1% defects were found.

From a manufacturing process view, vapor-phase reflow has additional advantages. Surprisingly, the placement of the LCC is not critical. The high surface tension of the solder will physically move the LCC, assuring perfect alignment of the LCC pad connections to the tin-plated tungsten traces on the substrate. IDT has taken advantage

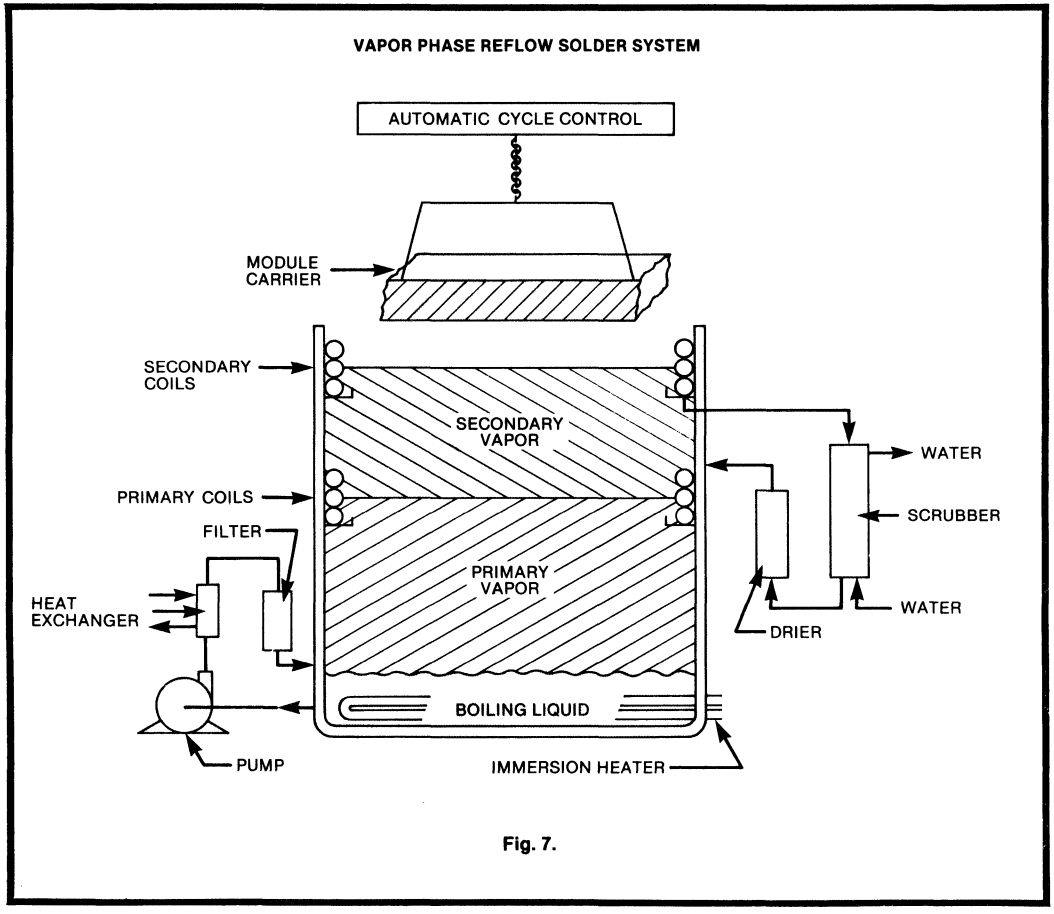


Fig. 7.

of this high surface tension to assure adhesion of LCCs to the bottom of a substrate, while additional LCCs are mounted to the top—producing very high packing density modules.

The use of FC-70 (chemically inert) in vapor-phase soldering eliminates the problem of lead and contact oxidation since the reflow is done in an oxygen-deprived environment. The inert properties of FC-70 also eliminate any flux charring, etching, or polymerization, making cleanup of the final module simple.

Military memory modules

Integrated Device Technology uses the highly reliable vapor-phase reflow solder technique in manufacturing extremely fast, low-power CMOS static RAM modules.

IDT utilizes its existing line of very fast 16K static RAMs, produced in the company's 2.5μm, double-poly, proprietary "CEMOS" I process. Since "CEMOS" I produces the fastest 16K CMOS static RAMs available, the memory modules have the highest performance possible.

The high packing density technique of mounting LCCs to both top and bottom of a substrate allows the construction of 64K RAM modules with equivalent pinout and function to proposed monolithic 64K static RAMs. IDT's volume production of three organizations (8K × 8, 16K × 4 and 64K × 1) allows users to leap the evolutionary boundaries of monolithic devices by designing today with 64K static RAM modules that can be replaced with monolithic devices when they become readily available. In addition, because faster 16K static RAMs are used, speeds of 65 nsec over the full military temperature range can be achieved, outperforming the proposed specifications for 64K monolithics.

Parameter matching

Since a memory module is, in reality, a small subsystem, the interplay of component parameters becomes an important consideration. Expertise in manufacturing and testing of the components becomes an important asset. IDT takes advantage of this knowledge of manufacturing to prescreen each component, analyzing a variety of parameters and comparing those parameters to characterization data of modules, determining the performance of the module before it is even constructed. This painstaking procedure reduces costly rework and, more importantly, eliminates the possibility of matching three high-performance components with a lower one, thus producing a module with lower overall performance.

Rework

Rework of module assemblies is an extremely simple procedure. After identification of the problem, the assembly can be reheated to reflow any inadequate solder joints or to remove a defective component. The difficulties arise in identifying the problem. A thorough understanding of the component interplay and use of a unique cell pattern test is critical for minimizing the amount of rework.

A unique cell pattern test can identify the exact assembly problem. If a failure occurs at the same

COMPONENT SCREENING PROCEDURES
PER MIL-STD-883, METHOD 5004, CLASS B

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal Visual	2010, Condition B	100%
High-Temperature Storage	1008, Condition C	100%
Temperature Cycle	1010, Condition C	100%
Constant Acceleration	2001	100%
Hermeticity Fine and Gross	1014	100%
Burn-In		
Pre-Burn-In Electrical	Per Applicable Device Specification	100%
Burn-In	1015, 160 Hrs. @ +125°C or Equivalent	100%
Final Electrical Tests		
Static (DC)	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Functional	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
Switching (AC) or Dynamic	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
External Visual	2009	100%

FULLY ASSEMBLED MODULE SCREENING
PER MIL-STD-883, METHOD 5004, CLASS B

SCREEN	TEST METHOD	LEVEL
Burn-In		
Pre-Burn-In Electrical	Per Applicable Device Specification	100%
Burn-In	1015, 160 Hrs. @ +125°C or Equivalent	100%
Temperature Cycle	1010 Condition C	100%
Hermeticity Fine and Gross	1014	100%
Final Electrical Tests		
Static (DC)	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Functional	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
Switching (AC) or Dynamic	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
External Visual	2009	100%

Fig. 8.

8

address in each device field, the implication is a bad substrate or an assembly problem with one or more common address lines. Failure in one device memory field indicates an assembly problem with one device, or a grossly mismatched component. In a dynamic failure mode, a unique cell pattern test can mask off all the memory fields but one and characterize the parameters of that individual device. This is essential to determining the overall performance degradation of having one device with lower performance than others.

Screening

To assure the most reliable module possible, screening the components *and* the module is important. IDT processes all components to MIL-STD-883, Level B for all military applications. After assembly of the module, additional screening is performed to test mechanical integrity and to ensure proper interplay of the components (see Fig. 8).

Right for the military

The availability of LCCs, advances in surface mounting techniques, and a dedicated approach to reliability make the module ideal for military applications. System employment of modules and familiarization with its performance advantages will keep the military designer ahead of the competition. Increasingly higher-density modules can be generated much faster and more easily than can monolithic devices, satisfying the higher-density needs of today's military systems. In addition, because of their lower cost, custom modules are applicable for systems requiring only moderate quantities. Unique organizations (×1, ×9, ×16 outputs), or unique functions (cache memories, chip set combinations, etc.), will allow tailoring the components to the system rather than the system to the component.

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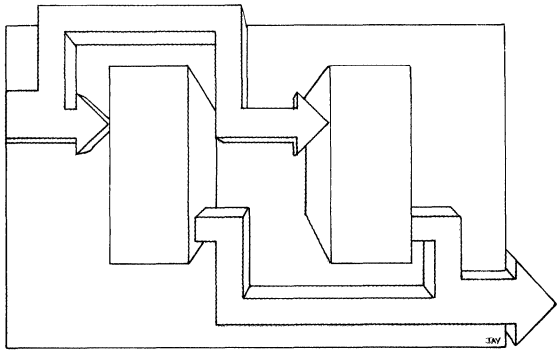
Reprinted from **DESIGN NEWS** October 10, 1983

HIGH-SPEED FIFOs CONTEND WITH WIDELY DIFFERING DATA RATES

Dual-port RAM buffer and a dual-pointer system provide rapid, high-density data storage and reduce overhead.

by Michael J. Miller
Frank L. Toth



High-speed multiprocessors, ideally, store large amounts of sequential data in minimum memory space. They also transfer data between processors that are operating at different data rates. One of the most common buffer/storage architectures developed to meet these needs is the first-in, first-out (FIFO) RAM buffer. Until now, FIFO storage has used high-speed, high-power, but relatively low-density, bipolar RAMS. Alternately, lower-speed, higher-density MOS RAMS could be selected. Both of these solutions, however, require the addition of control circuitry, such as address counters, bus buffers, and flag logic.

The Integrated Device Technology IDT 7201/7202 CMOS FIFO uses a dual-pointer system to provide high-speed, high-density and low-power sequential data storage. Model 7201 is a 512-location by 9-bit wide FIFO. The 7202 FIFO is 1024 location by 9 bits wide. This chip offers an access rate of 50 ns, and sports a dual-port RAM array with separate read and write ports. It allows simultaneous asynchronous reads and writes, eliminating the need for handshaking and bus arbitration. Two pointers within the FIFO indicate the location within the RAM array where the read or write will take place. When either of the pointers reaches the last location in the FIFO queue, the pointer is reset to the first location.

Three flags provide information about the status of data within the array: an empty flag (EF), a full flag (FF), and a half-full flag (HF). These status flags provide a count of how many valid pieces of data are in the memory queue.

Traditional FIFO designs have two sets of shift registers to move data through the FIFO. One set of registers holds the data. When data is placed in the top register, it drops down and emerges at the bottom. There is a second shift register, functioning in parallel, that contains flags. These flags show whether the associated data element at the same chronological position on the data queue is valid.

When data is written into the top location of the data queue, a true flag is placed into the "valid-bit"queue. The length of the FIFO can be varied

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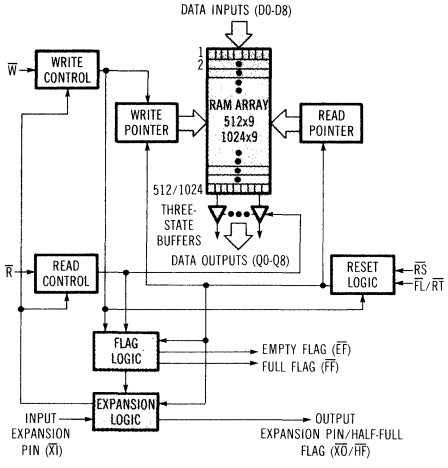


Addresses in the dual-point architecture of the IDT 7201 and 7202 are generated internally by the pointers to perform first-in, first-out functions.

by allowing the data and its associated valid bit to sink down into the next lowest location—as long as there is no valid data there. This process forms a stack of valid data. The timing of data down through the queue is controlled by an internal clock. The maximum latency, fall-through time is the product of the maximum number of locations in the queue and the clock length cycle. The valid-data bit, which tells the system that data is present, is brought out in parallel with the queue data.

Dual-pointer architecture

An alternative to this classic shift-register architecture is one which uses a RAM array and two pointers. In this setup, the RAM array is 9 bits wide. The pointers move sequentially through the data, rather than data moving through the shift registers. RAM dual-pointer architecture allows data to be accessed sequentially, eliminating the problem of fall-through time. The write shows where new data will be written. The read pointer indicates where data will be read from the output. When either pointer accesses its location, it is incremented. When a pointer is incremented to the last location in the array, it is reset to the beginning of the array. This approach shortens the fall-through time and maintains a variable-length queue.

In a typical system cycle, the FIFO is reset, activating the empty flag (EF). As soon as data is written into the RAM array, the empty flag is inactive. The empty flag is not activated again until all data has been read from the array. When the count of data elements reaches more than half the number of locations in the RAM array, the half-full flag (HF) is activated. If a read reduces the count to just below the half-way count, then the (HF) is deactivated. The full flag is activated when the count of data elements is exactly equal to the number of locations in the RAM array.

Wider FIFOs

Width and depth requirements vary widely according to the application. Two expansion pins, one for input (XI) and one for output (XO), enable unlimited expansion of FIFO depth. For applications requiring less than 1024 locations, the maximum width of the IDT FIFO is 9 bits. Wider word width can be achieved by operating the control signals of two or more devices in parallel. With devices working in parallel, status flags can be detected from any device. Two IDT 7201/7202 devices can configure an 18-bit word. Traditional FIFO architecture requires more external circuitry to match the Input Ready and Output Ready signals. This is necessary to account for the data differences in the internal, self-generated clock frequencies.

Traditional FIFO design also increases fall-through time of data in applications calling for deeper FIFOs. Since FIFOs are connected end to end in the older architecture, data takes longer to fall through. Fall-through time, in fact, increases in direct proportion to the number of devices.

With the two-pointer approach, however, the data input and data output bus are connected. This produces a parallel-processing architecture that is analagous to cascading standard RAM devices to achieve deeper memories.

Device selection

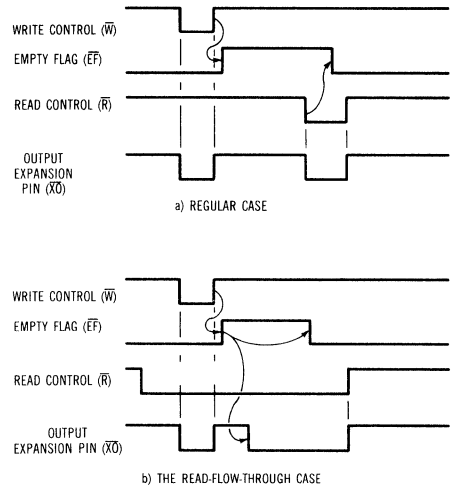
Since FIFOs do not have chip selects and external decoding mechanisms, the task of selecting devices must be done internally. This control is achieved through a unique serial structure. The first (or master) FIFO is identified by grounding the FL input. All other FIFOs in the structure must have the FL input pulled up to Vcc. The XO output of the first FIFO is connected to the XI input on the next FIFO in the queue. The XO output of each FIFO is connect to the XI input of the next, and so on, until all FIFOs are serially connected.The XO output of the last FIFO is then connected to the XI of the first FIFO.

After a reset, the active read and write pointers are in the first device. When the write pointer has progressed to the end of the first FIFO device, it outputs a pulse on XO. This pulse activates the write

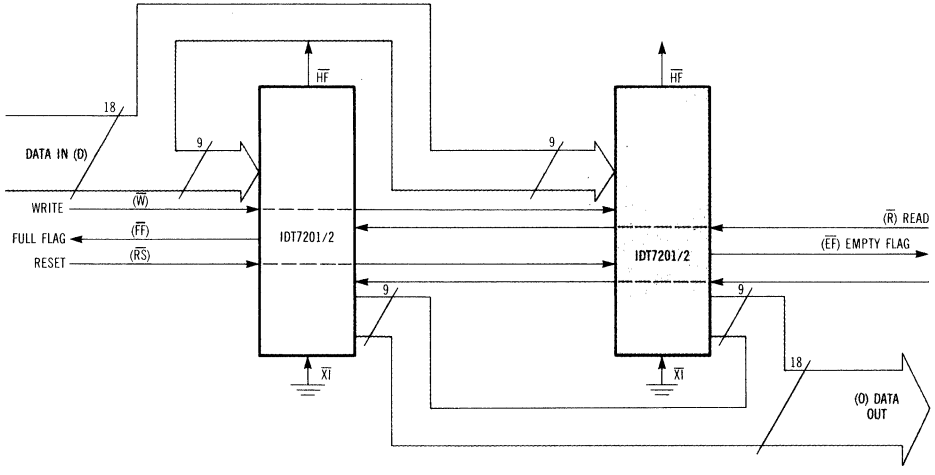
pointer at the beginning of the next device, and simultaneously deactivates the write pointer in the first device. This passes write enable control to the second device. The read pointer functions in the same way, using a pulse on the XO output to activate the read pointer in the next device while terminating the read pointer of the first device. The two pointers form a ring structure, with the read pointer always chasing the write pointer. The pointer enable crosses the device boundaries by sending an XO pulse onto the next device.

The read and write pointers are designed so that they can never cross each other, even in cascade mode. The XO pulse occurs simultaneously with the read and write signals. When the last location is read or written to, the XO output goes low with the read or write enable input, then goes high when this signal goes high. Even though reads and writes are asynchronous, there is no conflict between the write and read pointer.

One special situation occurs when the FIFO is empty, and the read and write pointers are at the last location. The system cannot read from the FIFO until the empty flag is deactivated. To solve this problem, the empty flag output will go high after the write pulse goes high. This ensures that the XO pulse, indicating the write pointer, has been passed on to the next device. The system will then read the last location. At this point, another XO pulse will be issued, transferring the read pointer. The flow-through mode provides maximum performance and design simplification for systems which are pipelined. The read-flow-through mode is a special case where data is allowed to flow through and empty the FIFO by lowering the read-



FIFO is empty, and the read and write pulses are separate and distinct (a). Read-flow-through mode is invoked while the printers are at the device boundaries (b).



Width expansion of the IDT7201 7022 for designs require more storage than 1024 by 9 bits. The parts function in parallel, avoiding system performance degradation.

8

The high-speed FIFO solution

In file server applications, high-speed FIFOs offer lower costs and higher efficiency than other hardware or software approaches. Assume the file server is connected to a local area network (LAN) on one side and a Winchester disk on the other. Both I/O connections demand attention at unpredictable intervals and must be serviced on demand, or data is lost.

A possible software solution would be to place data into software FIFO queues as it arrives. When a full record is buffered, processing begins. To implement this solution, though, the data rates of both interfaces would have to be low enough so that the software code could poll the status of either I/O port. Also, the ports would have to be monitored in case another user on the LAN makes a request. These time-consuming tasks detract from system performance.

One hardware approach to moving data in file server applications uses hardware interrupts. Here, an interrupt mechanism calls routines to move data to and from the I/O ports and the software FIFO queues. Interrupts allow one task to run at a time and can switch to an I/O service routine at any instant. An interrupt solution, therefore, must be designed so that the interrupted task's data is not destroyed . Extra code is required to maintain the state of the machine. This overhead may prevent an interrupt during a critical time for a particular piece of code. This would in turn require code to disable and re-enable interrupts around the critical sections. Also, the programmer must spend additional time proving that all possible sequences caused by random interrupts will produce desirable results. Typically, these complications outweigh the faster execution hardware interrupts offer.

Direct memory access (DMA) offers another hardware solution for a file server application. This approach monitors I/O ports with a block of circuitry. When the port requires attention, the DMA logic interrupts the current task at the bus transfer level and steals a memory cycle to transfer the data to or from the port and the FIFO queue in memory. Although memory cycles are lost, the effect is mimimal when contrasted with the hardware interrupt scheme, where a whole subroutine of many cycles was executed to transfer each element of data. A significant disadvantage of the DMA solution is that the DMA controllers are complex devices which must be programmed and implemented in the bus structure. In addition, since the DMA mechanism can only serve one source at any given instant, they act as a throughput bottleneck.

In file server applications, all of these solutions move the mechanism that feeds data to or from the FIFOs into program memory, away from the software and closer to the I/O port. Because both FIFO queues are in memory, the memory bus remains a bottleneck. Hardware FIFOs avoid this memory bus bottleneck and boost system performance.

The processor would still interface to the FIFO through an I/O port, but the FIFO would now be between the I/O port and the rest of the hardware. The software could service data at a steady rate with no loss of data. without the problems or overhead associated with more complicated schemes such as interrupts or DMA. Because the queues are between the controller and the peripheral, the peripheral can load or read the queue without interrupting the controller. Since the controller is not involved with maintaining both queues, there is no possibility of lost data because one queue was being serviced while data for the other queue arrived.

Large FIFOs, such as the IDT7202 which is 1024 location by 9 bits, offer a minimum device count. Assuming that there are two FIFOs (transmit and receive) for each I/O port, then there will be only four 28-pin devices for the FIFO solution. The DMA approach, however, requires at least one 40-pin device and several bus buffer/control devices as well. A similar parts count can be expected with the interrupt solution.

enable input before data is written into the FIFO. When the empty flag (EF) is finally deactivated, signaling a write from the input side, the receiving circuitry can terminate the read cycle by reading after the appropriate access time, then deactivate the read signal.

The write-flow-through mode is used when the read signal is full. The sending circuitry can anticipate a read by the receiving circuitry by lowering the write input before the full flag (FF) is deactivated. The receiving circuitry knows that the sending circuitry has read a location, freeing up a location to receive new data. The sending circuitry then activates the write input, writing data into the RAM array. This flow-through mode means the full flag does not have to be monitored before initiating a write cycle.

Hardware FIFOs are an economical memory organization to use when lists of data items are to be buffered. Because they do not require an address to access items in the list, there is less overhead in terms of both circuitry and access time.

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16-by-16-bit multipliers fabricated in CMOS rival the speed of bipolars

A pair of CMOS parallel multipliers sports a 65-ns clock multiplication time, allowing them to substitute for bipolar equivalents in digital signal-processing circuits.

The mathematical theories behind digital signal-processing systems have been around for decades, but not until the arrival of inexpensive dedicated ICs could designers readily implement complex digital signal-processing systems. Their availability opens up a wide variety of applications in such areas as real-time speech processing and pattern recognition, not to mention radar and spectrum analysis.

Digital signal processing consists mostly of a series of multiplications and additions—with the multiplications taking up the most time. Thus one of the primary building blocks in any such system is a parallel multiplier that handles large numbers quickly. Fortunately, digital signal processing no longer need depend on power-hungry bipolar multipliers to obtain the requisite speed. A pair of CMOS multipliers—which give designers all the advantages inherent in that process—are now available that are as fast as many of their bipolar equivalents.

Frank Lee, Chun P. Chiu, and **Frank Toth**
Integrated Device Technology Inc.

After working on silicon-on-sapphire technology at Hewlett-Packard's Cupertino Division, Frank Lee helped to found IDT in Santa Clara, Calif., in 1981. He is currently director of product development.

Cofounder Chun P. Chiu also came from HP's Cupertino Division; he is now IDT's director of DSP design engineering.

Before joining IDT last January as marketing manager for the DSP Division, Frank Toth was marketing manager for microprocessors at Synertek.

Some specifications

The two parallel 16-by-16 bit multipliers operate with a 65-ns clock multiplication time and a typical power consumption of only 200 mW, which is less than 1/12 that of comparable bipolar devices. This power advantage demands no sacrifice in speed and is achieved through the use of a CMOS technology known as CEMOS-I.

The architecture of the duo is relatively simple, with each multiplier consisting of three sections: An input-register arrangement for

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Semiconductor Technology: Fast CMOS multipliers

two 16-bit numbers (X and Y), an asynchronous multiplier array, and an output-register arrangement. The last includes a multiplexer that supplies two output paths for the final product (Fig. 1).

The differences between the two multipliers show up mainly in their clocking configurations. The IDT7216 features four independent clocks, one for each of the circuit's two input and two output registers (CLKX, CLKY, CLKL, CLKM). The clocks can thus be arranged to simplify the design of a digital signal-processing system and to maximize its throughput. The IDT7217, on the other hand, employs only a single clock for all the registers, which makes it suitable for pipelined microprogrammed systems. It also furnishes separate register-enable signals ($\overline{ENX}$, $\overline{ENY}$, and $\overline{ENP}$).

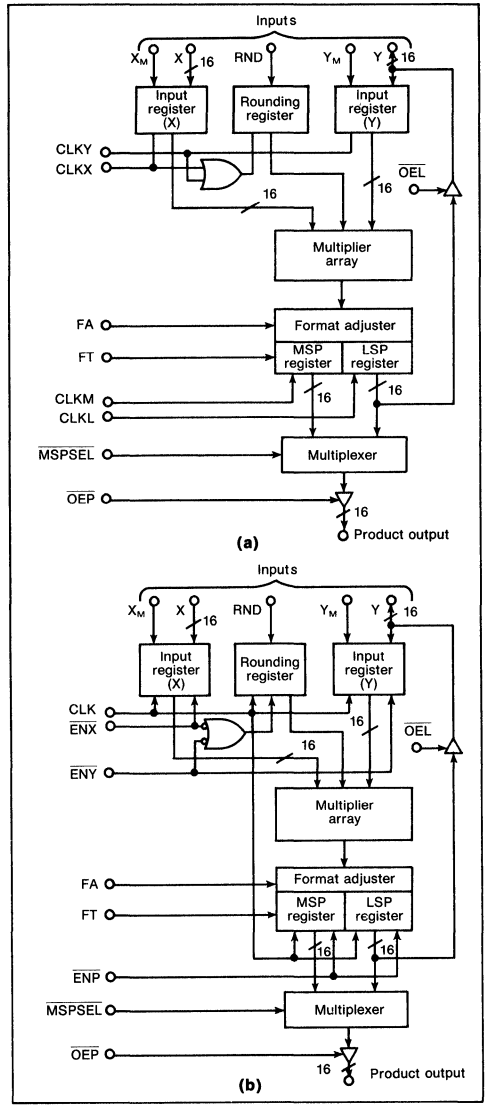
Identical twins, almost

Except for the different clocking and enabling schemes, the devices are identical. In both circuits, a multiplication is performed by an array of adders in accordance with a modified Booth's algorithm with a 4-bit carry-look-ahead circuit, which helps achieve the required high speed. All of the input registers, as well as the output registers for the least significant product (LSP) and the most significant product (MSP) use the same positive-edge-triggered D-type flip flops.

In operation, the two numbers to be multiplied are fed into separate X and Y registers, which also receive two signals (X_M and Y_M) that identify whether the input is in the form of an unsigned magnitude or a two's complement. Consequently, users are able to multiply mixed-format inputs.

Routing the output

Once the multiplication is carried out, a Format Adjuster (FA) signal converts the 32-bit output into the desired format: either a full 32-bit product or a left-shifted 31-bit product with the sign bit replicated in the LSP. The data then passes into two 16-bit latch registers, one for the LSP and another for the MSP part of the output. Each 16-bit segment of the total product can be clocked out separately through the multiplexer under the control



1. Two nearly identical versions of the 16-by-16-bit parallel multiplier are available. The IDT7216 (a) supplies four separate clock-input ports for the two 16-bit input registers and the two 16-bit output registers. The IDT7217 (b) furnishes a single clock input for all the registers but three separate register-enable signals.

of the Most Significant Product Select ($\overline{\text{MSPSEL}}$) signal.

Additionally, the output from the LSP register can be routed to the Y I/O port by means of the output enable ($\overline{\text{OEL}}$) signal, which controls a three-state output buffer. When the input and the output data need not be latched, the Feedthrough (FT) control signal is available to make the MSP and LSP registers transparent.

The twelvefold power advantage of the new multipliers is a result of the aforementioned CEMOS-I process, a 2.5-μm double-polysilicon, dual-well technology that employs a lightly doped substrate and cuts cost by obviating the need for an epitaxial layer. With the process, the delay of an inverter is a mere 0.430 ns at 5 V.

On the level

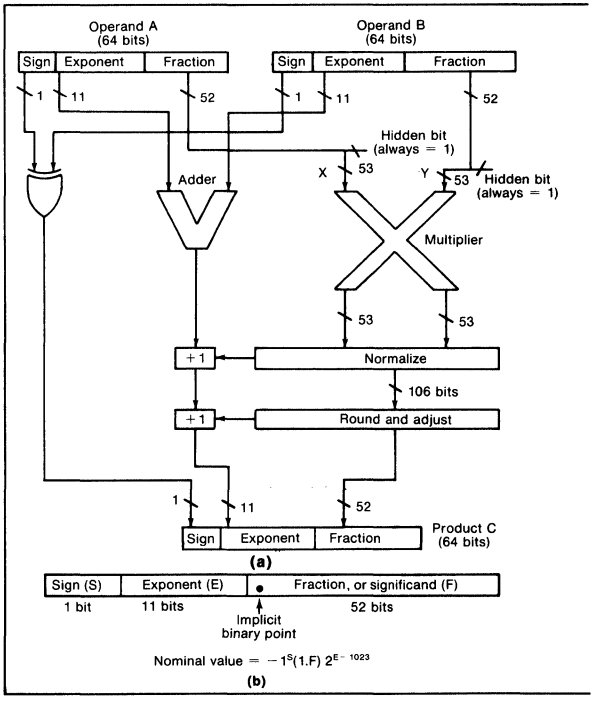
Moreover, since CMOS devices draw power only while switching from one level to another, slowing down the device further decreases the multipliers' power requirements so that it drops below the full-speed figure of 200 mW. Such power savings not only reduce both thermal stress and power supply costs, but equally importantly they allow the designer the option of housing a complete system in a smaller package. That freedom is made possible because elaborate heat-sinking apparatus such as heat rails, cooling pipes, and fans are usually not required.

At the same time, the size of the printed circuit board may be significantly reduced. For example, a system of 12 bipolar multipliers, each in a 64-pin package, takes up 36.84 in.^{2}. Additionally, the thermal expansion and power dissipation problems of such a 3.5-W device are quite substantial. However, with the CMOS multipliers housed in 900-mil leadless chip carriers, the same system can be squeezed into less than 15.36 in.^{2}.

Beat the heat

An added bonus of the leadless chip carriers is that their lead capacitances are about half those of a typical DIP, thereby reducing interconnection propagation delays. Also, the chip carriers weigh approximately 1/10 as much as an equivalent DIP.

Finally, beyond its low power dissipation, the CMOS design also ensures a wide temperature tolerance. Since the CMOS process integrates both n- and p-type devices on one chip, the data output is able to employ an npn transistor as a pull-up device and an n-channel FET as a pull-down circuit. Doing so takes advantage of the fact that increasing temperature slows down FETs but speeds up npn bipolar transistors. The result is a device whose multi-



2. The multipliers can be put to good use in high-speed floating-point applications such as a 64-by-64-bit circuit (a). The operands employed follow the IEEE double-precision standard (b), which designates the first bit as the sign, the next 11 bits as a number's exponent (a power of 2), followed by a 53-bit fraction. In the multiplication process the fractions are multiplied as integers and the exponents are merely added.

8

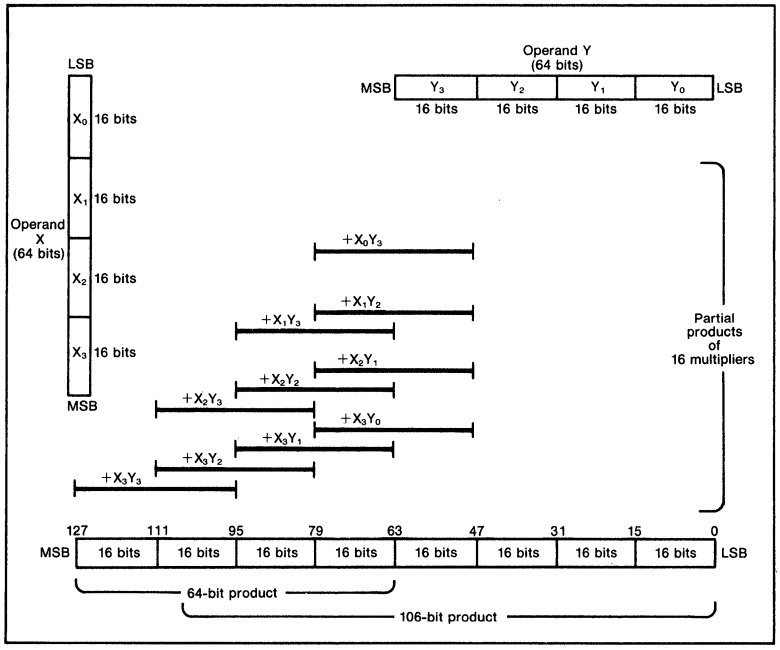
Semiconductor Technology: Fast CMOS multipliers

plication time varies little over the military temperature range. Moreover, its output swing is symmetrical from rail to rail.

Naturally, the self-heating effects of bipolar devices that produce excessive die-surface temperatures and lower overall device reliability are absent. Also absent is an old CMOS problem—latch-up. Large input overshoots, which cause no ill effect in bipolar circuits, can result in latch-up with some types of CMOS devices. That problem occurs when the close proximity of p- and n-channel elements form what is essentially a silicon controlled rectifier. In the multiplier designs, latch-up is suppressed through the selective use of guard rings, which were designed into the chip after a careful analysis of all possible latch-up paths. As a result, no adverse latch-up effects should be observed with as much as 800 mA applied to the I/O pins.

No static

Another significant problem familiar to users of CMOS, especially in systems operating in harsh environments, is damage due to electrostatic discharges. However, the several



3. In an array of sixteen 16-bit CMOS multipliers, two 64-bit operands are multiplied in combinations of 16 by 16 bits and the partial products added to produce a 128-bit output. The six partial products shown in color make no contribution to the 64 MSBS.

forms of input protection circuitry employed in the multipliers, such as large-area gate-modulated diodes, protect against electrostatic discharges to 5000 V. Thus with the major problems generally associated with CMOS solved, especially its speed limitation, applications for the pair of multipliers abound.

Floating-point arithmetic, for instance, demands high-speed multiplication. Virtually all popular 16-bit microprocessor families have coprocessors that are able to carry out such precise floating-point operations. Moreover, a new standard on binary floating-point arithmetic, IEEE 754, has been widely adopted. It designates 32-bit single-, 64-bit double-, and even 80-bit extended-precision output products, all of which are finding wide use in engineering workstations for mechanical and electrical simulation, matrix inversion, and a wide variety of other scientific digital signal-processing applications.

However, although performing an arithmetic operation in tens of microseconds might be a satisfactory rate for simple problem solving, designers are increasingly faced with the need to speed up floating-point operations because of the growing complexity of data processing applications, especially interactive design work. Accordingly, the computing power of large array processors is now required in small table-top workstations.

The 64-bit question

Even though the 32-bit microprocessors and related chip sets now emerging offer some hope of carrying out floating-point operations at high speed and with single precision—the 64-bit double-precision format is another matter. In the past, bulky high-power bipolar devices were the designer's only choice. Now, the CMOS multipliers supply a more attractive alternative.

For instance, consider a common configuration for a 64-bit floating-point multiplier that employs the IEEE double-precision format (Fig. 2). During a multiplication, the 11-bit exponent field of the format is calculated using just simple addition. Calculating the fractional (significand) field, on the other hand, involves the multiplication of two 53-bit integers, which generates a 106-bit product. If the IEEE standard's precision requirement is relaxed to allow a 64-bit product, the significand multiplication can be handled by an array of 10 multipliers.

At first glance it would seem that 16 multipliers are needed (Fig. 3). However, only the 10 most significant partial products contribute to the 64 MSBs of the final product. Thus the lower 6 partial products do not have to be produced and added. In that way, six multipliers and 12 adders can be eliminated.

A part in every port

As mentioned earlier, the 32-bit products from each individual multiplier in the array can either be multiplexed out of the single 16-bit product port in two parts or both parts can be delivered simultaneously, one through the product port and the other through the shared Y-operand I/O port. Naturally, for the greatest speed and the minimum amount of hardware, the Y I/O port should be shared, which is easily done merely by disabling the Y input mode of each circuit after the multiplier has been loaded.

Also contributing to the high speed of the multiplier array is the fact that all the multipliers are loaded simultaneously and produce their output only one multiplication-delay later: Just the summed partial products propagate through the array. Finally, the rounding (RND) input signal is not enabled individually for partial products but is activated at the end of the overall multiplication based on the precision requirements for the final output product.

Indeed, the advantages of the CMOS parallel multipliers are most dramatically demonstrated wherever large arrays of high-speed multipliers are needed. It should be kept in mind, though, that the combination of low power, small size, and high speed that the 7216 and 7217 offer are important benefits in any application—even if only a single multiplier is used.□

QUALITY CONFORMANCE PROGRAM

COMMITMENT TO QUALITY

Integrated Device Technology's monolithic and modular hermetic products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design, processing and assembly criteria of our Quality and Reliability Assurance Program were developed using MIL-M-38510 as the guideline.

Product flow and test procedures for all monolithic hermetic Military Grade products are in accordance with MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all modular hermetic products are patterned after the 100% screening and quality conformance requirements of MIL-STD-883.

Product flow and test procedures for all plastic products are in accordance with industry practices for producing highly reliable plastic molded products. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our Military and Standard Grade monolithic and modular hermetic products consistently meet customer requirements for quality, reliability and performance.

SUMMARY PLASTIC PRODUCT

PROCESSING FLOW

1. **Wafer Fabrication.** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside passivation is applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to scanning electron microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection.** Wafers are cut and separated and the individual die are 100% visually inspected to strict internal criteria.

3. **Die Push Test.** To ensure die attach integrity, product samples are routinely subjected to die push tests.

4. **Wire Bond Monitor.** Product samples are routinely subjected to wire bond pull tests to ensure the integrity of the lead bond process.

5. **Pre-cap Visual.** Before the package is molded, 100% of the product is visually inspected to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure.** Plastic encapsulated devices are baked to insure an optimum plastic seal so as to enhance moisture barrier characteristics.

7. **Pre-Burn-In Electrical.** Each product is 100% electrically tested at T_A = +25°C to IDT data sheet or customer specifications.

8. **Burn-In.** Standard Grade products are burned-in 40 hours or equivalent on memory devices, 16 hours or equivalent on VLSI logic devices and may be obtained as an option on MSI logic family devices (FCT, AHCT and 39C800) utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical.** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at +25°C and the maximum temperature extreme. The minimum temperature extreme, is tested periodically on an audit basis.

10. **Mark.** All product is marked with product type and lot code identifiers.

11. **Quality Conformance Inspection.** Samples of the plastic product which have been processed to the 100% screening requirements of Table I are subjected to the periodic Inspection Program as outlined in Table II. Where indicated the test methods are patterned after MIL-STD-883 criteria.

TABLE I

PLASTIC PACKAGE PRODUCT FLOW

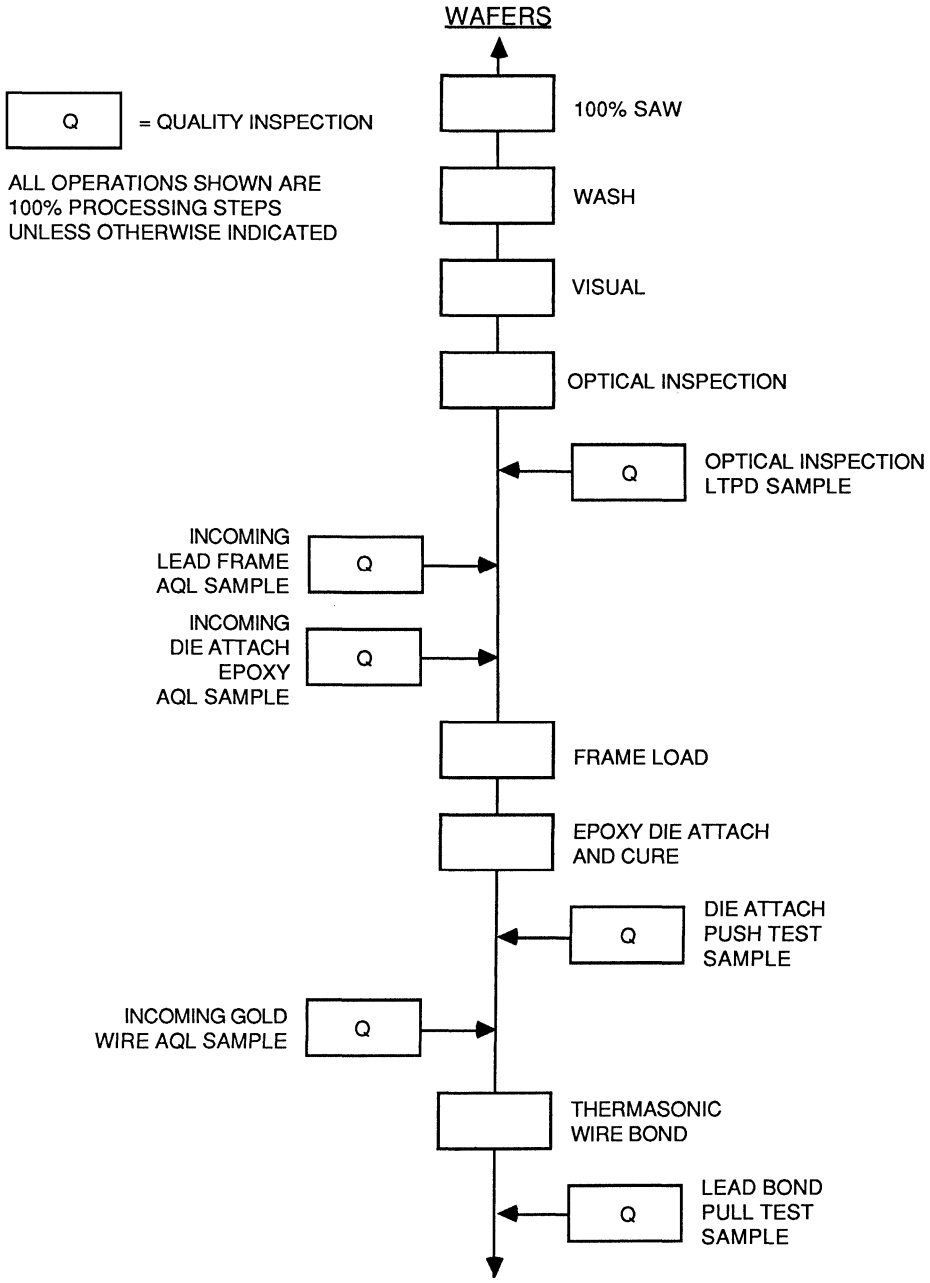


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TABLE I Continued...

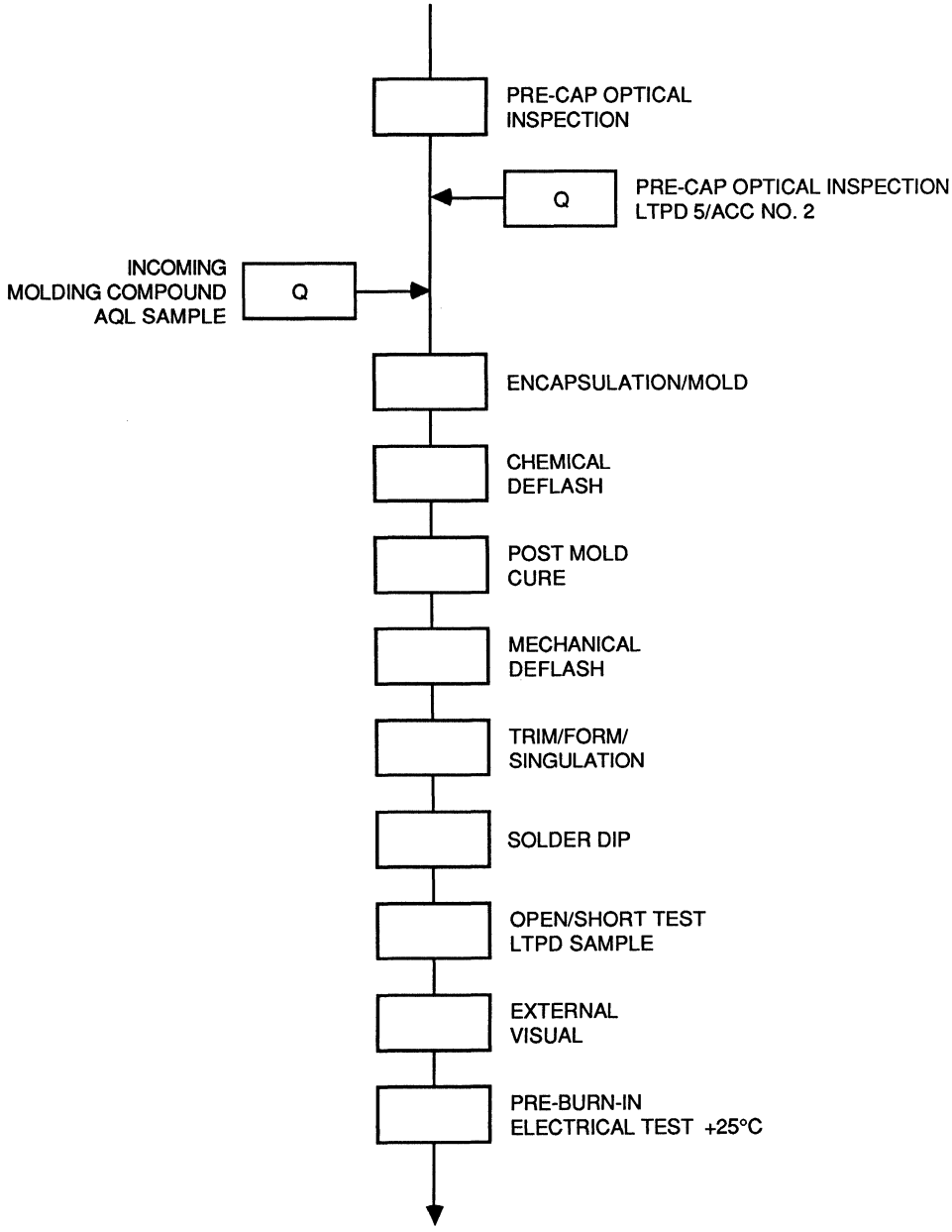


TABLE I Continued...

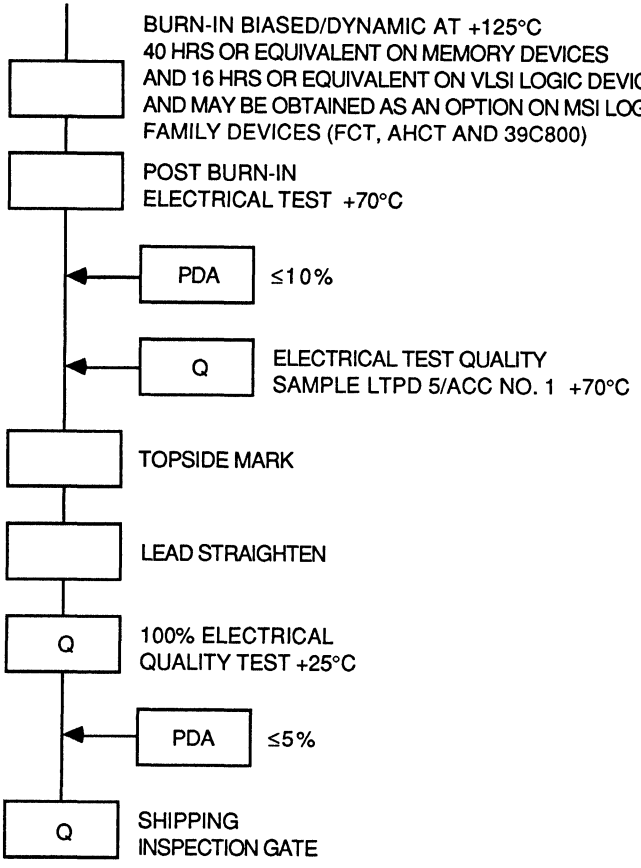


TABLE II
SUMMARY
PLASTIC QUALIFICATION/PERIODIC INSPECTION PROGRAM

	SEQUENCE AND TEST DESCRIPTION	LTPD	QUALITY LEVEL MAXIMUM SAMPLE SIZE/ACCEPT NO.
SEQUENCE A:	**ELECTRICALS**		
	PERFORMED100% EACH INSPECTION LOT.	—	100PPM
SEQUENCE B:	**PACKAGE/PROCESS**		
	PERFORMED EACH 8 WEEKS, EXCEPT FOR B-6, FOR EACH PACKAGE FAMILY.		
B-1	PHYSICAL DIMENSIONS, MIL-STD-883, METHOD 2016	—	2/0
B-2	RESISTANCE TO SOLVENTS, MIL-STD-883, METHOD 2015	—	8/0
B-3	SOLDERABILITY, MIL-STD-883, METHOD 2003	15	25/1
B-4	RESISTANCE TO SOLDERING HEAT, 260°C FOR 10 SECONDS	10	38/1
B-5	AUTOCLAVE: UNBIASED, 2 ATM SATURATED STREAM, +121°C, 96 HOURS	—	100/1
B-6	ESD SENSITIVITY, MIL-STD-883 , METHOD 3015, CAT. A, PERFORMED FOR INITIAL QUALIFICATION ONLY.	—	15/0
SEQUENCE C:	**PACKAGE/CHIP**		
	PERFORMED EACH 9 MONTHS MAXIMUM.		
C-1	STEADY-STATE LIFE TEST, MIL-STD-883, METHOD 1005 +125°C, FULLY DYNAMIC, 1000HR.	5	105/2
C-2	MOISTURE LIFE TEST, 85°C/85%RH, STATIC BIAS, 1000HR.	5	105/2
SEQUENCE D:	**PACKAGE DESIGN**		
	PERFORMED EACH 9 MONTHS MAXIMUM ON EACH PACKAGE FAMILY FROM EACH ASSEMBLY LOCATION.		
D-1	LEAD FATIGUE, MIL-STD-883, METHOD 2004, CONDITION B_2	15	34/2
D-2	THERMAL SHOCK, MIL-STD-883, METHOD 1011, CONDITION A, 0-100°C, 15 CYCLES	5	105/2
D-3	TEMPERATURE CYCLING, MIL-STD-883, METHOD 1010, CONDITION D, -65°C TO +150°C, 100 CYCLES.	5	105/2

SUMMARY OF MONOLITHIC HERMETIC

PRODUCT PROCESSING FLOW*

All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication.** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

2. **Die-Sort Visual Inspection.** Wafers are cut and separated and the individual die are 100% visually inspected to strict internal criteria.

3. **Die Shear Monitor.** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor.** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual.** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning.** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical stress tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing.** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical.** Each product is 100% electrically tested at T_A = +25°C to IDT data sheet or customer specifications.

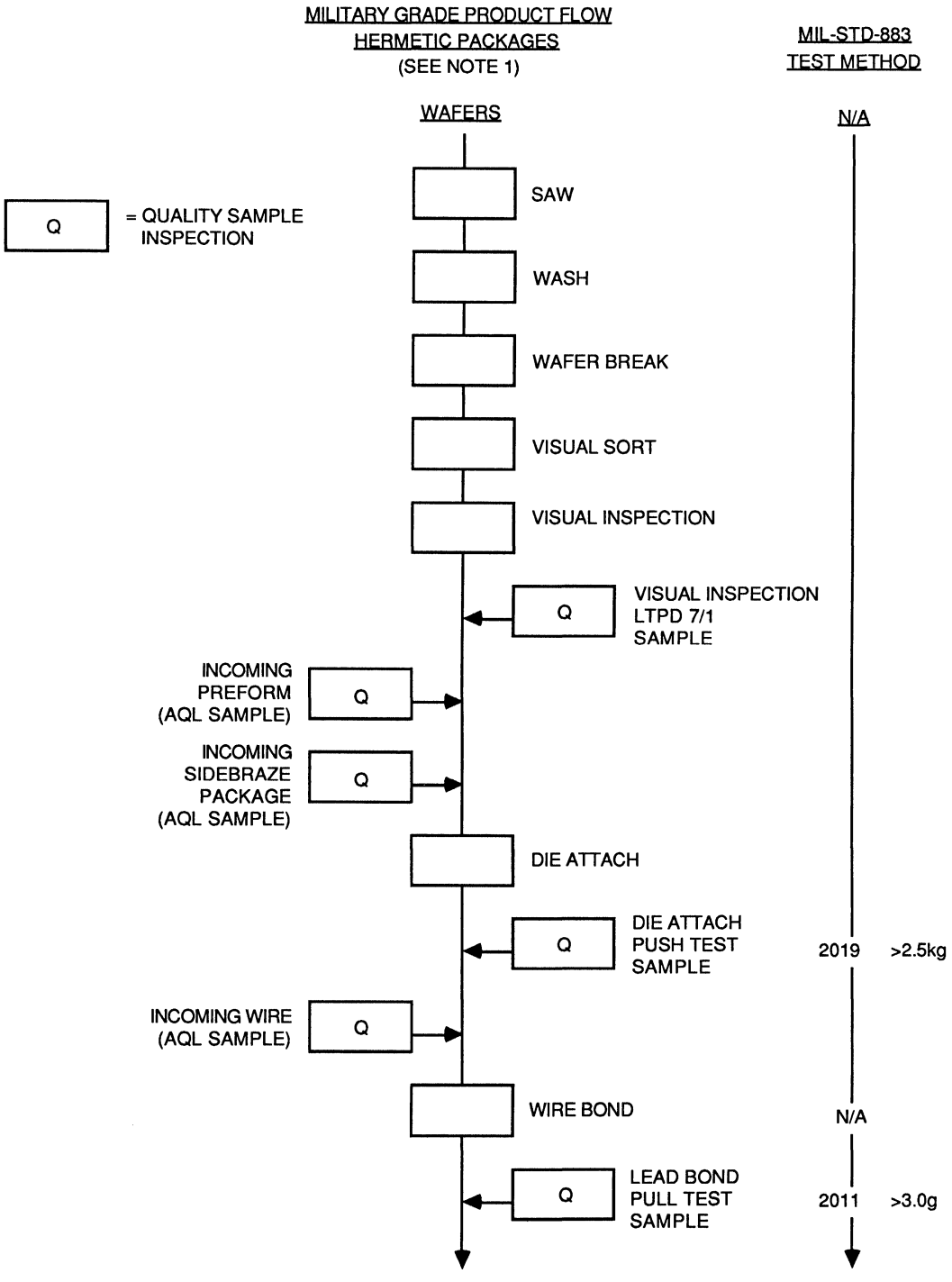
9. **Burn-In.** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D.

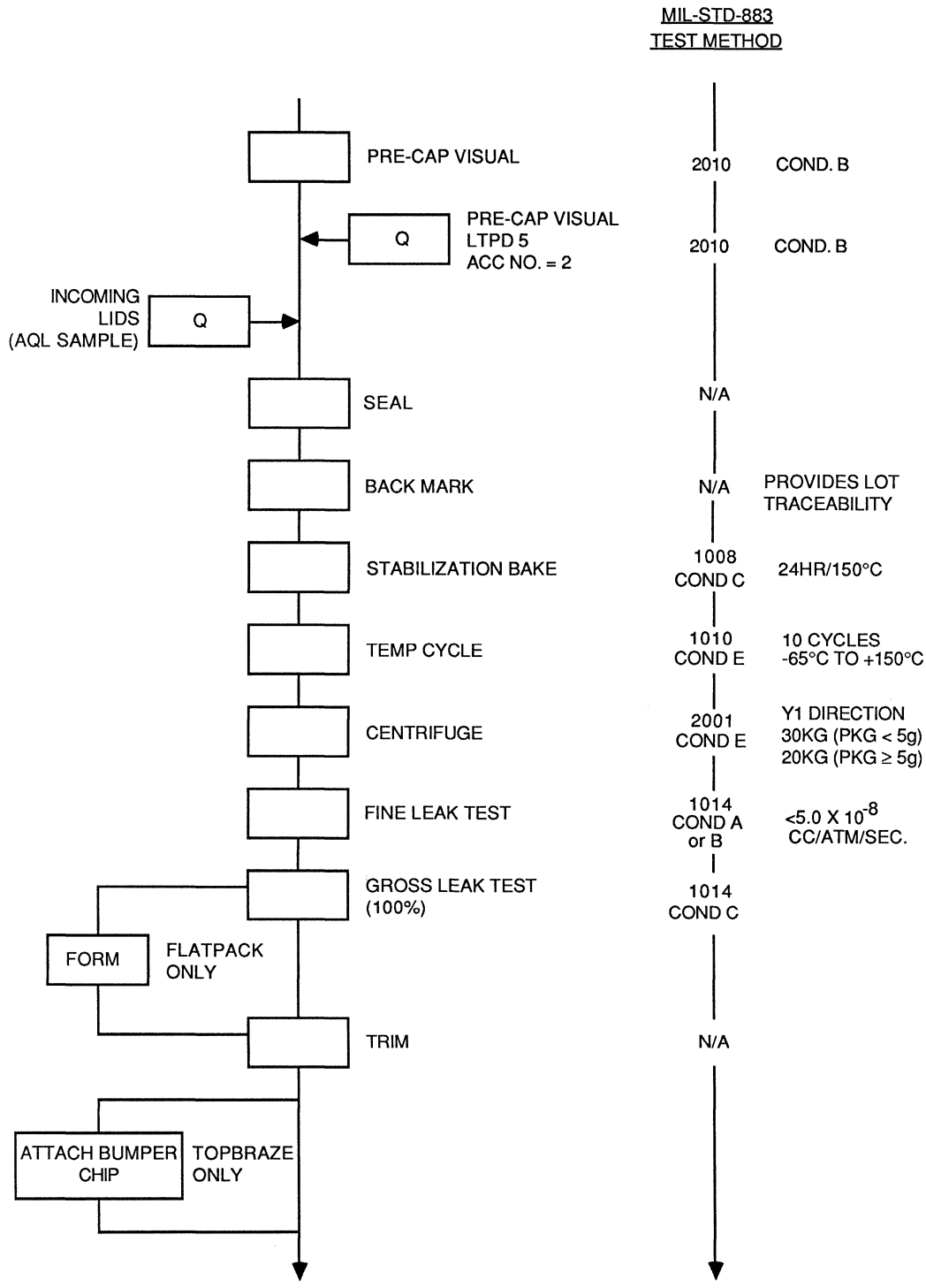
10. **Post-Burn-In Electrical.** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the -55°C to +125°C temperature range. Standard Grade products are sample tested to the applicable temperature extremes.

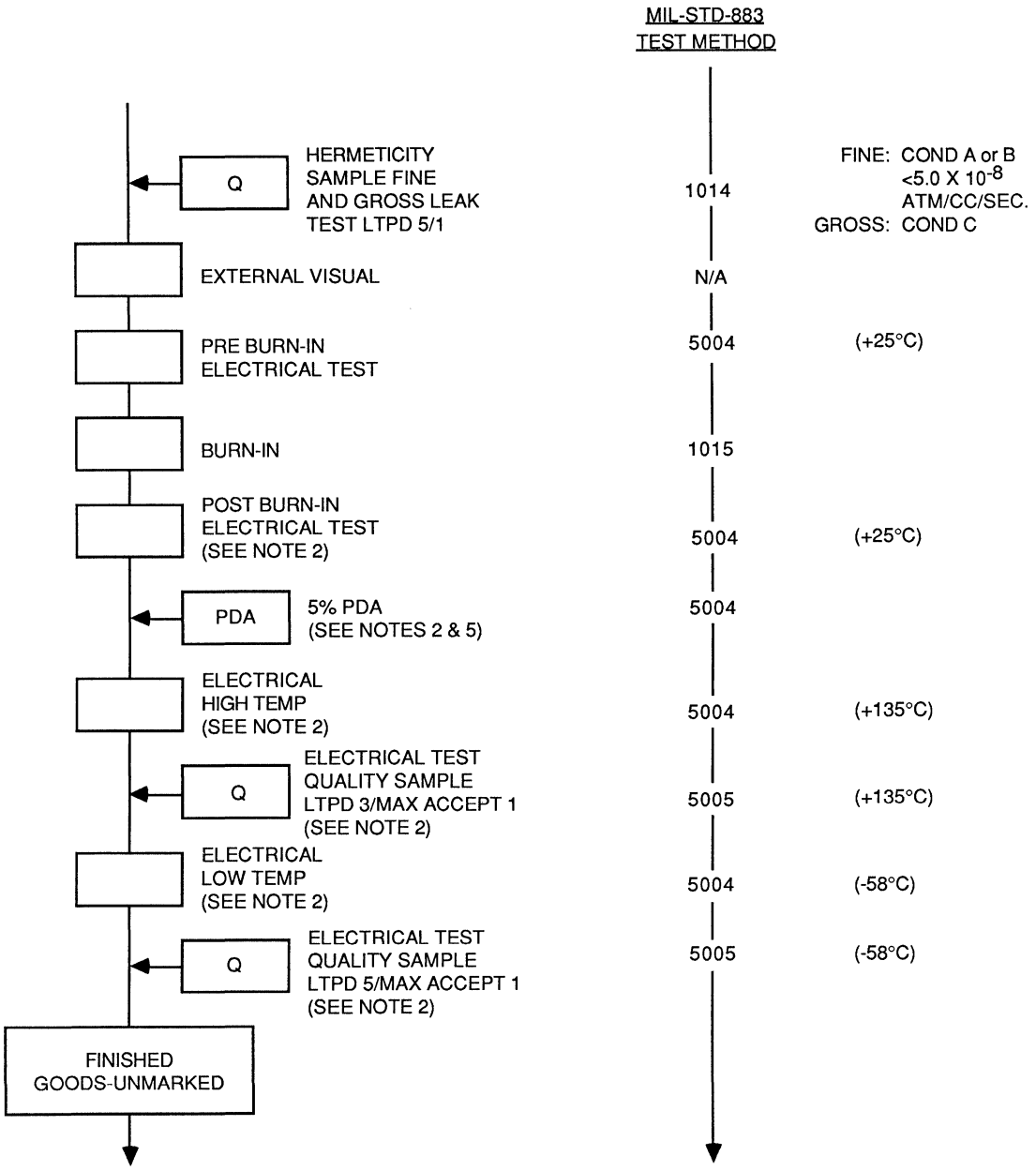
11. **Mark.** All product is marked with product type and lot code identifiers.

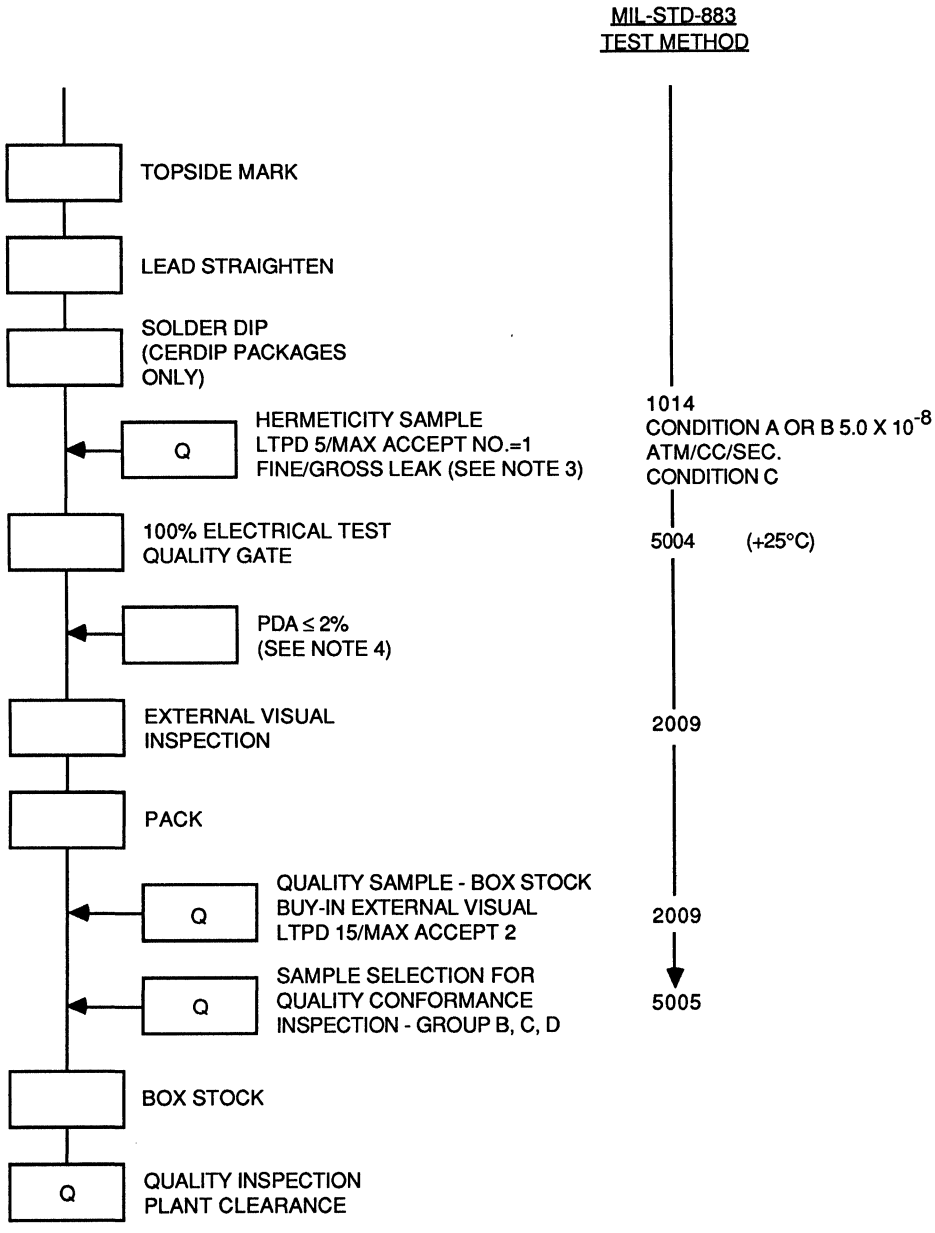
12. **Quality Conformance Tests.** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

* For quality requirements beyond Class B levels, such as SEM analysis, X-ray inspection, particle impact noise detection (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.


MILITARY GRADE PRODUCT FLOW
HERMETIC PACKAGES
(SEE NOTE 1)
MIL-STD-883
TEST METHOD
WAFERS
N/A
Q = QUALITY SAMPLE INSPECTION
SAW
WASH
WAFER BREAK
VISUAL SORT
VISUAL INSPECTION
Q
VISUAL INSPECTION
LTPD 7/1
SAMPLE
INCOMING
PREFORM
(AQL SAMPLE)
Q
INCOMING
SIDEBRAZE
PACKAGE
(AQL SAMPLE)
Q
DIE ATTACH
Q
DIE ATTACH
PUSH TEST
SAMPLE
2019
>2.5kg
INCOMING WIRE
(AQL SAMPLE)
Q
WIRE BOND
N/A
Q
LEAD BOND
PULL TEST
SAMPLE
2011
>3.0g


MIL-STD-883
TEST METHOD
PRE-CAP VISUAL
2010
COND. B
Q
PRE-CAP VISUAL
LTPD 5
ACC NO. = 2
2010
COND. B
INCOMING
LIDS
(AQL SAMPLE)
Q
SEAL
N/A
BACK MARK
N/A
PROVIDES LOT
TRACEABILITY
STABILIZATION BAKE
1008
COND C
24HR/150°C
TEMP CYCLE
1010
COND E
10 CYCLES
-65°C TO +150°C
CENTRIFUGE
2001
COND E
Y1 DIRECTION
30KG (PKG < 5g)
20KG (PKG ≥ 5g)
FINE LEAK TEST
1014
COND A
or B
<5.0 X 10-8
CC/ATM/SEC.
GROSS LEAK TEST
(100%)
1014
COND C
FORM
FLATPACK
ONLY
TRIM
N/A
ATTACH BUMPER
CHIP
TOPBRAZE
ONLY


MIL-STD-883
TEST METHOD
Q
HERMETICITY
SAMPLE FINE
AND GROSS LEAK
TEST LTPD 5/1
1014
FINE: COND A or B
<5.0 X 10-8
ATM/CC/SEC.
GROSS: COND C
EXTERNAL VISUAL
N/A
PRE BURN-IN
ELECTRICAL TEST
5004
(+25°C)
BURN-IN
1015
POST BURN-IN
ELECTRICAL TEST
(SEE NOTE 2)
5004
(+25°C)
PDA
5% PDA
(SEE NOTES 2 & 5)
5004
ELECTRICAL
HIGH TEMP
(SEE NOTE 2)
5004
(+135°C)
Q
ELECTRICAL TEST
QUALITY SAMPLE
LTPD 3/MAX ACCEPT 1
(SEE NOTE 2)
5005
(+135°C)
ELECTRICAL
LOW TEMP
(SEE NOTE 2)
5004
(-58°C)
Q
ELECTRICAL TEST
QUALITY SAMPLE
LTPD 5/MAX ACCEPT 1
(SEE NOTE 2)
5005
(-58°C)
FINISHED
GOODS-UNMARKED


MIL-STD-883
TEST METHOD
TOPSIDE MARK
LEAD STRAIGHTEN
SOLDER DIP
(CERDIP PACKAGES
ONLY)
Q
HERMETICITY SAMPLE
LTPD 5/MAX ACCEPT NO.=1
FINE/GROSS LEAK (SEE NOTE 3)
1014
CONDITION A OR B 5.0 X 10-8
ATM/CC/SEC.
CONDITION C
100% ELECTRICAL TEST
QUALITY GATE
5004 (+25°C)
PDA ≤ 2%
(SEE NOTE 4)
EXTERNAL VISUAL
INSPECTION
2009
PACK
Q
QUALITY SAMPLE - BOX STOCK
BUY-IN EXTERNAL VISUAL
LTPD 15/MAX ACCEPT 2
2009
Q
SAMPLE SELECTION FOR
QUALITY CONFORMANCE
INSPECTION - GROUP B, C, D
5005
BOX STOCK
Q
QUALITY INSPECTION
PLANT CLEARANCE

NOTE:

1. ALL SCREENS ARE 100% UNLESS OTHERWISE NOTED.

2. ALL ELECTRICAL TEST PROGRAMS ARE PER THE APPLICABLE IDT TEST SPECIFICATIONS.

3. THIS HERMETICITY SAMPLE IS APPLICABLE TO 300 MIL 20 LD CERDIP (SUBSYSTEM PRODUCT ONLY, MSC-0202) PACKAGES AND THE 300 MIL 24 LD SIDEBRAZE PACKAGE ONLY.

4. A. IDT PERFORMS A 100% ELECTRICAL TEST AT +25°C WITH A 2% PDA LIMIT AT THIS POINT TO SATISFY GROUP A REQUIREMENTS.

   B. IDT CONSIDERS THIS TO BE EQUIVALENT TO THE GROUP A REQUIREMENT OF AN LTPD OF 2 WITH AN ACCEPT NUMBER OF 2.

   C. IF A LOT FAILS THE 2% PDA LIMIT, IT MAY BE RESCREENED 1 TIME ONLY TO A TIGHTENED PDA LIMIT OF 1.5%

5. IF A LOT FAILS THE 5% PDA BUT IS ≤10%, THE LOT MAY BE RESUBMITTED TO BURN-IN 1 TIME ONLY TO THE SAME TIME AND TEMPERATURE CONDITIONS AS FIRST SUBMISSION. THE SUBSEQUENT POST BURN-IN ELECTRICAL TEST AT +25°C WILL BE PERFORMED TO A PDA OF 3%.

IMPROVED TOLERANCE OF INTEGRATED DEVICE TECHNOLOGY PRODUCTS FOR HIGH-RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The lower power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS(SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by devices in the system due to a pulse event, and is measured in RADS(SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuit. As the ion passes through the silicon, charge is created either through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

RADIATION CATEGORY	PRIMARY PARTICLE	SOURCE	EFFECT
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-Up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, most concern is focused on the first two, *Total Dose Accumulation* and *Dose Rate*. Integrated Device Technology has taken considerable data on these two effects, and has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as error checking and correction (ECC) circuitry, since the occurence of SEUs are not particularly dependent on process technology. Little is yet known about the effects of neutron-induced damage.

Figure 2 itemizes the broad enhancements that IDT has made to its process. The use of epi substrate material accomplishes a lower substrate resistance environment to guarantee latch-up-free CMOS structures. Field and gate oxides are less susceptible to radiation damage, i.e. "hardened," by modifying the process architecture to allow lower-temperature processing. Device implants and Vts have been adjusted allowing more Vt margin. Other mask steps have been added or modified to optimize radiation tolerance.

	STANDARD	ENHANCED
Substrate Material	n-	n- epi/n+
Field Oxide	std	hardened
Gate Oxide	std	hardened
Vt, n	0.75 volts	1.3 volts
Vt, p	-0.75 volts	-0.6 volts
Process Temperature Post Gate Oxide	1000°C	900°C

Figure 2.

RADIATION HARDNESS CATEGORIES

With the process enhancements described above, Integrated Device Technology can now offer integrated circuits with varying grades of radiation tolerance, or radiation "hardness," shown in Figure 3. IDT defines the level of radiation hardness as follows:

Radiation Enhanced integrated circuits are defined as being able to withstand a total dose of 30K RADS(SI) without failure.

Radiation Tolerant integrated circuits are defined as being able to withstand a total dose of 10K RADS(SI) without failure.

Standard IDT products can be expected to exhibit radiation tolerance to the extent of being able to withstand 4K to 6K RADS(SI) without failure.

RADIATION HARDNESS LEVELS	TOTAL[1] DOSE (RADS/SI)	LATCHUP LEVEL
Standard	≤6K	10^8
Tolerant	>10K	10^8
Enhanced	>30K	NONE ($\geq 2.4 \times 10^{10}$)

NOTE:

1. This data is for RAMs. Logic circuits are generally higher.

Figure 3.

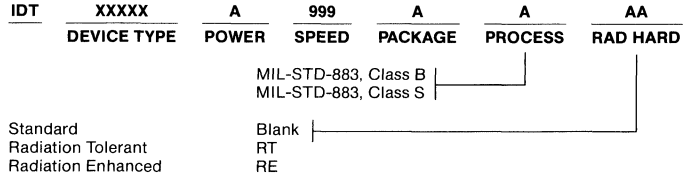


Figure 4.

Integrated Device Technology now offers, or plans to offer, devices processed to each of these radiation tolerance levels across the full product line. The appropriate part number corresponding to these radiation hardness categories is defined in Figure 4.

Please contact your local IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications. Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

SYSTEM CONSIDERATIONS IN THE TESTING OF FAST CMOS DEVICES

In order to evaluate or verify the performance of fast CMOS devices, it is important to implement a measurement environment that does not degrade device operation. The following article outlines techniques for system configuration which may alleviate common degradations of test systems.

Ground Noise is one of the most common and troublesome test problems. Ground noise is the unwanted voltage fluctuation of the ground reference due to current spikes required during the switching of device output logic levels. These voltage variations in the ground reference can be quite significant, and can cause an erroneous perception of the voltage margin or noise immunity tolerance of the device under test (DUT). In a memory tester the ground path incldes handler contacts, connectors and the DUT load board, thus there may be one long, high inductance ground path back to the test system ground.

In practice, ground noise may be minimized by using the following techniques:

- Provide multiple high-quality, high-frequency, ceramic bypass capacitors as close as possible to the DUT and again on the DUT load board. This allows the V_{CC} wiring to serve as an extra AC ground path for high-frequency ground noise.
- Keep the ground path as short as possible; use large diameter or multi-strand wire and "straight-line" wiring techniques. (Note: Multi-strand wire is preferred for high frequency applications because of skin resistance effects.)
- Minimize the number of series connections in the DUT ground path; provide as many parallel ground connections as possible through each remaining connector.
- If the system uses a Kelvin (force-sense) ground system, terminate the system by shorting force to sense on the DUT load board. Kelvin systems provide DC accuracy, but their response times are much too slow to aid in the suppression of ground noise at the test site. Terminating Kelvin early sacrifices a little DC accuracy, but the ability to use the sense line as a second, low impedance ground path usually improves the overall test accuracy.
- Reduce the DUT load capacitance (receiver and interconnect capacitance) as much as possible; avoid using low values of load resistors. Both techniques reduce the transient currents, thus improving test accuracy. When necessary, DUT output drive capability can usually be verified with DC tests.

Reflections, due to impedance mismatch between the DUT output drivers and the circuitry which connects the outputs to the test system, are another common problem. This resonance occurs because the wire connecting the DUT outputs to the receivers is actually an inductor connected in series with the comparator input capacitance, forming a series resonant tank circuit. Uncorrected ringing can cause errors in measuring output timing and increase cross-talk noise.

Note also that ringing also occurs on input signals to the DUT from the test system, and these signals should also be matched. Of particular importance are edge-triggered control lines (e.g. Write Strobe) which, if ringing excessively, will cause double-triggers.

In practice, ringing may be minimized by using the following techniques:

- In instances where severe conditions exist, it is best to try to match the driving source with the transmission line and load. A series resistor of 20 to 70 ohms is likely to tune most normal applications.
- Use short, low inductance connections from the DUT output to the receiver; minimize comparator and interconnect capacitance. Both techniques raise the resonant frequency of the tank circuit which limits the time measurement error and reduces the DUT's ability to stimulate ringing in the tank circuit.
- Use twisted pair wiring techniques to connect DUT outputs to the receivers. Though this raises the capacitance slightly, it reduces the purely inductive character of the interconnect, usually tending to reduce ringing.

Cross-Talk between signals on adjacent lines is also a common problem in high-speed systems. This inductive coupling will tend to add noise to both input and output lines, causing errors in measuring input noise margin and output settling times, respectively. Techniques to reduce cross-talk are as follows:

- Physically separate conductors of critical signals and keep wires as short as possible.
- Reduce output loading to minimize the magnitude of current transients which could be coupled to adjacent lines.
- Use twisted pair or shielded cable wherever possible; take care to tie all grounds from these transmission lines together at both ends.
- Use ground plane or ground mesh techniques in the load board and the handler interface if possible.
- Use pull-up or pull-down resistors on unused inputs. Without these safeguards, device inputs are especially susceptible to cross-talk noise.

Latch-Up is a possiblity with CMOS memories, and good test procedures will ensure that unwanted latch-up does not occur. V_{CC} should never exceed the absolute maximum rating, and input lines should never be taken below ground voltage. Latch-up is discussed in more detail elsewhere in this data book.

In conclusion, the issues in desiging a test environment are identical to designing any high-speed system, but the initial conditions given in designing a test-system interface—and importance of correct results—dictate a higher degree of dedication to the details outlined above.

THERMAL PERFORMANCE DATA OF INTEGRATED DEVICE TECHNOLOGY PACKAGES

When calculating the junction temperature, T_J, at which an operating integrated circuit functions, it is necessary to know the thermal resistance of the package, θ_{JA}, measured in "degrees centigrade per watt." With this data, the following equation is used:

$$T_J = T_A + P\ [\theta_{JA}]$$

where T_A is the ambient temperature and P is the power at which the device operates.

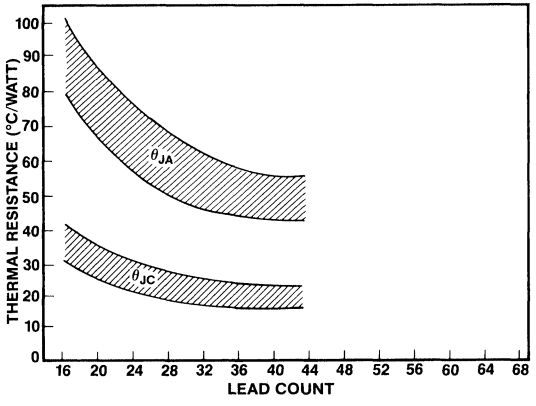
The figures below represent generic thermal performance data for standard IDT production packages. Thermal resistance is influenced by a number of factors, including die size, cavity size, and die bonding; in order to present a comprehensive characterization of these variables, a range of values is provided rather than a single point.

Please note that θ_{JA} is the thermal resistance from the device junction to the surrounding environment which, typically, is "still air" at 25°C with the package inserted into a low cost socket mounted on a printed circuit card.

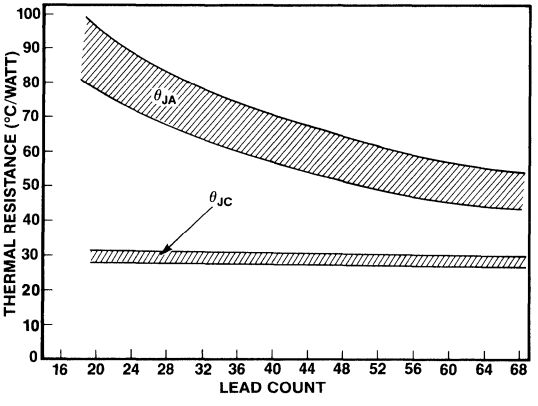
Also included in the figures is θ_{JC}, which is junction to case thermal resistance with the package attached to an "infinite" heat sink. For surrounding conditions that are different, T_J can theoretically be calculated using the following equation:

$$T_J = T_A + P\ [\theta_{JC} + \theta_{CA}]$$

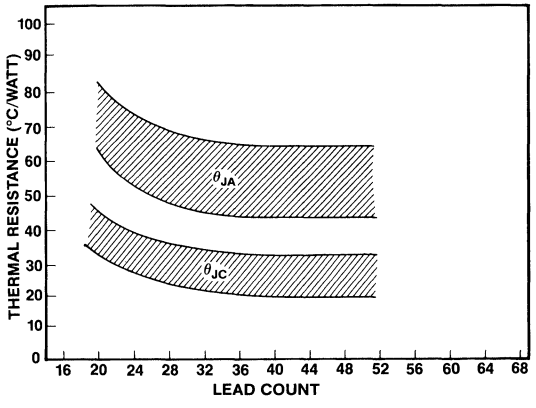
where θ_{CA}, the case-to-ambient thermal resistance, depends on the airflow conditions, etc., and must be known.



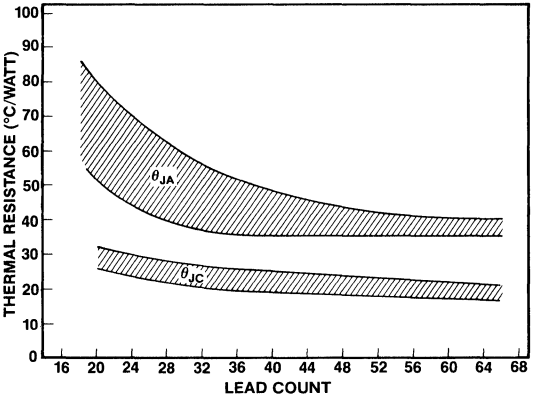
THERMAL RESISTANCE OF CERAMIC CERDIP PACKAGES



THERMAL RESISTANCE OF PLCC/SOIC PACKAGES

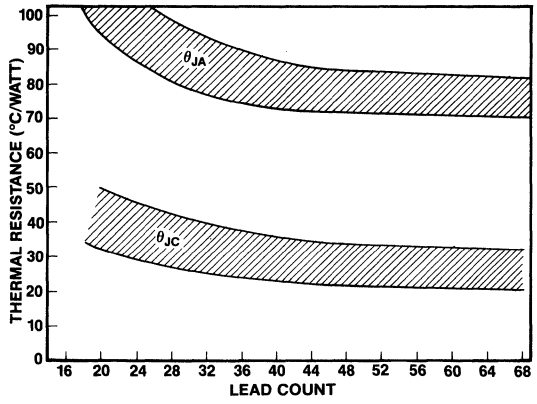


THERMAL RESISTANCE OF PLASTIC PACKAGES



THERMAL RESISTANCE OF CERAMIC SIDEBRAZE PACKAGES

8



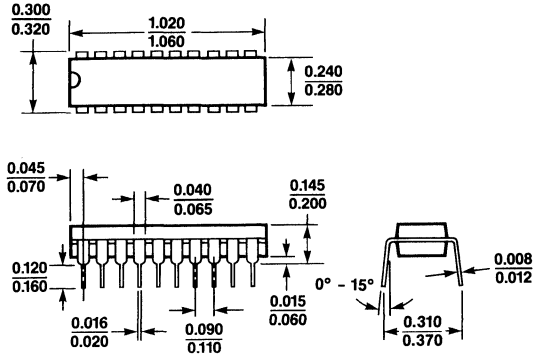
THERMAL RESISTANCE OF CERAMIC LEADLESS CHIP CARRIER (LCC) PACKAGES

Integrated Device Technology, Inc

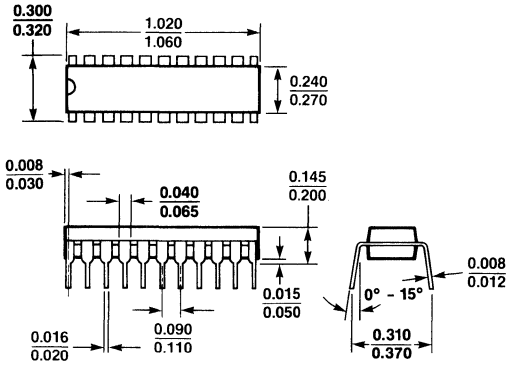
PACKAGE DIAGRAM OUTLINES

PLASTIC DUAL IN-LINE PACKAGES

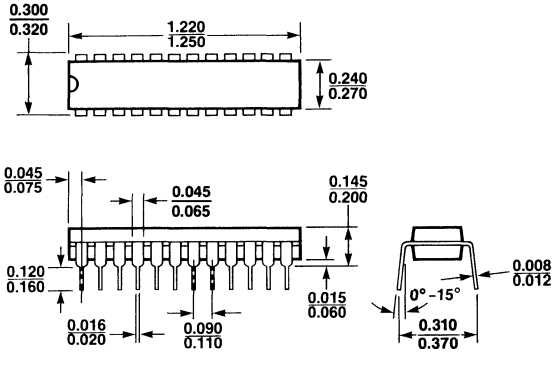
P20 20-PIN PLASTIC DIP



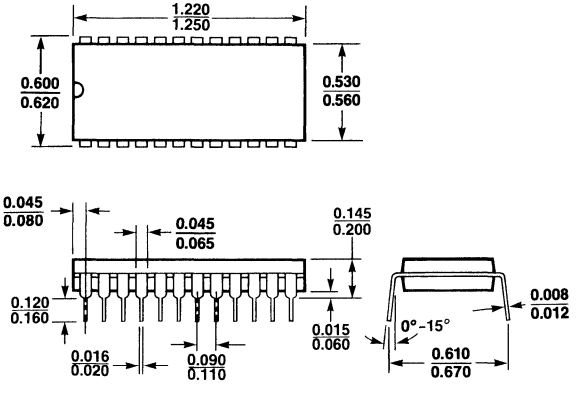
P22 22-PIN PLASTIC DIP



P24-2 24-PIN PLASTIC DIP (300 mil.)



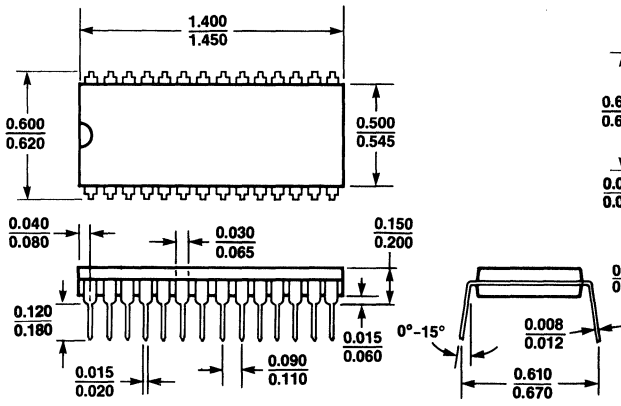
P24-1 24-PIN PLASTIC DIP (600 mil.)



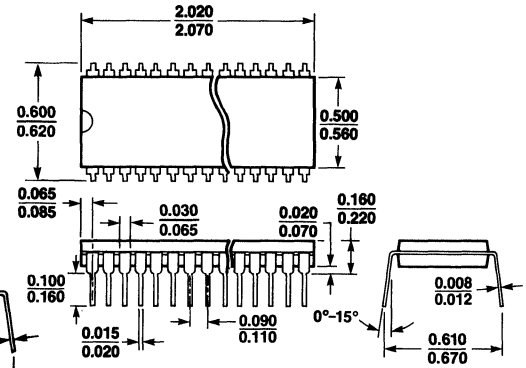
8

PLASTIC DUAL IN-LINE PACKAGES (Continued)

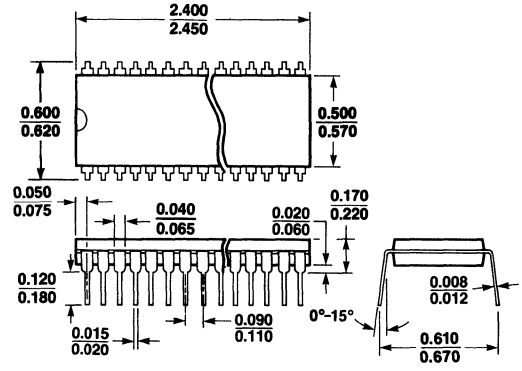
P28 28-PIN PLASTIC DIP



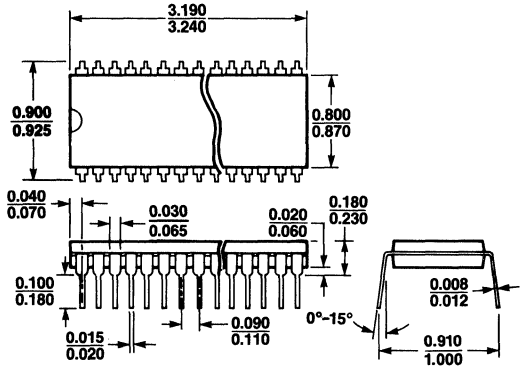
P40 40-PIN PLASTIC DIP



P48 48-PIN PLASTIC DIP



P64 64-PIN PLASTIC DIP



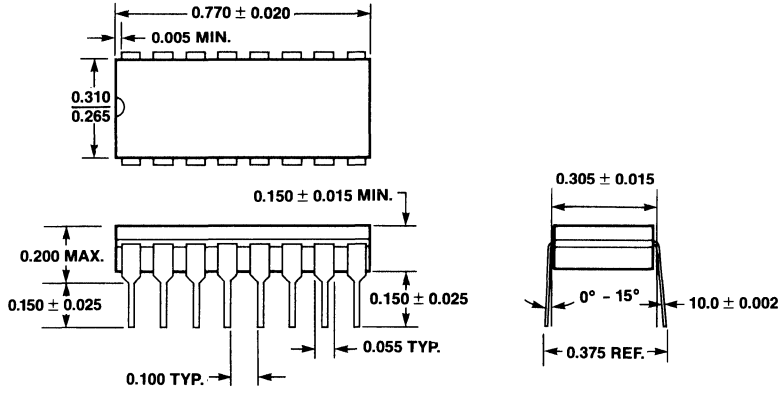
P68 68-PIN PLASTIC DIP (Consult Factory)

Integrated Device Technology, Inc

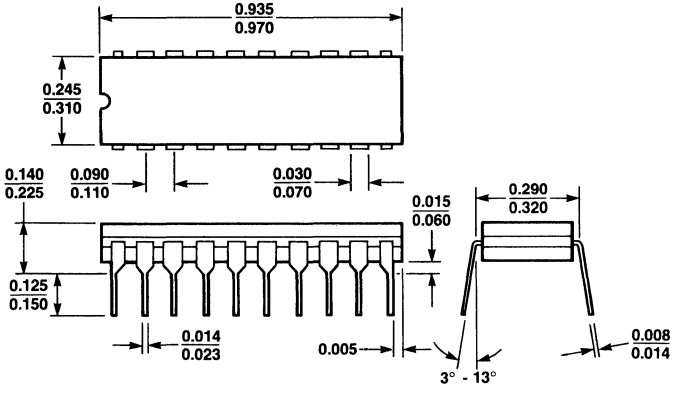
PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES

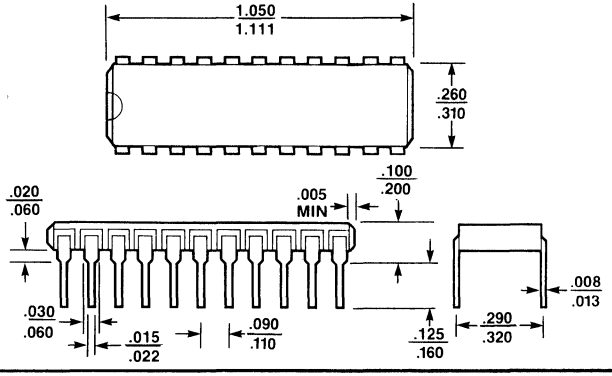
D16 16-PIN CERDIP



D20 20-PIN CERDIP



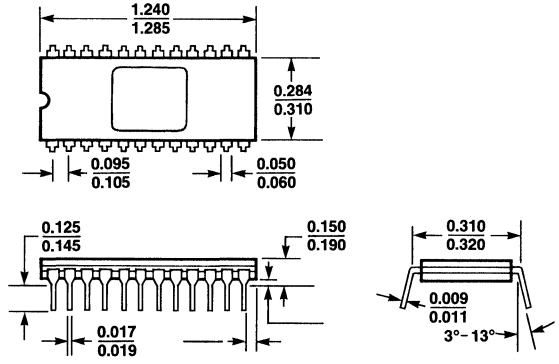
D22 22-PIN CERDIP



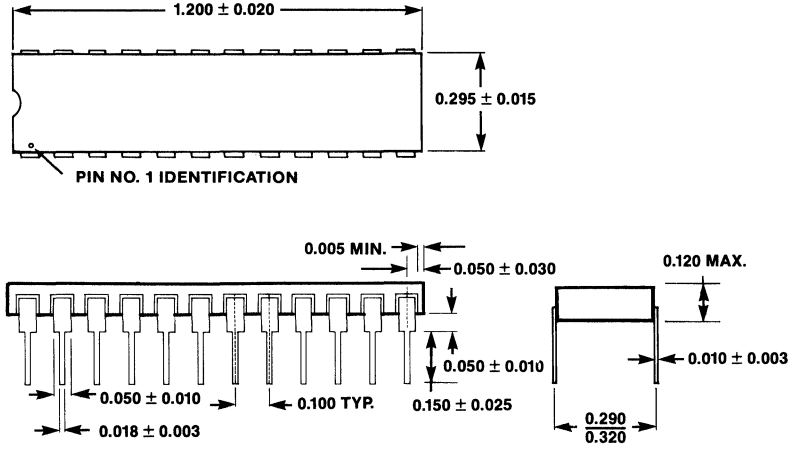
8

DUAL IN-LINE PACKAGES (Continued)

D24-1 24-PIN SIDEBRAZE THINDIP

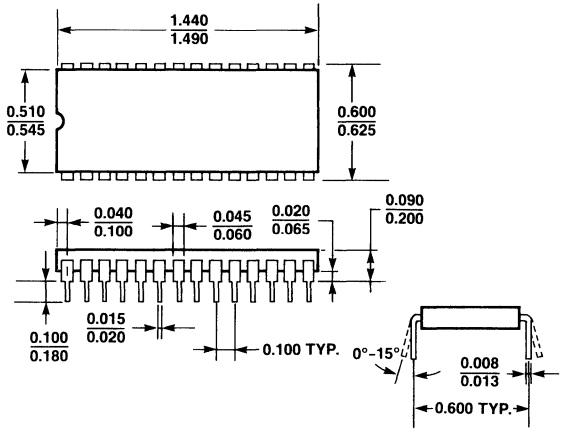


D24-2 24-PIN THINDIP (CERDIP)

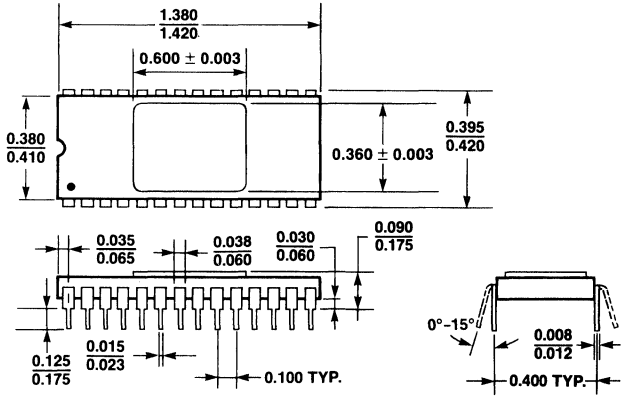


DUAL IN-LINE PACKAGES (Continued)

D28-1 28-PIN CERDIP (600 mil.)



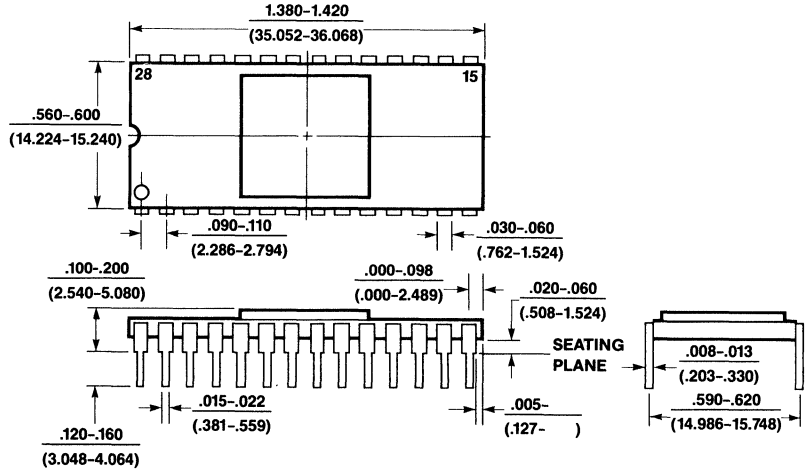
D28-2 28-PIN SIDEBRAZE THINDIP (400 mil.)



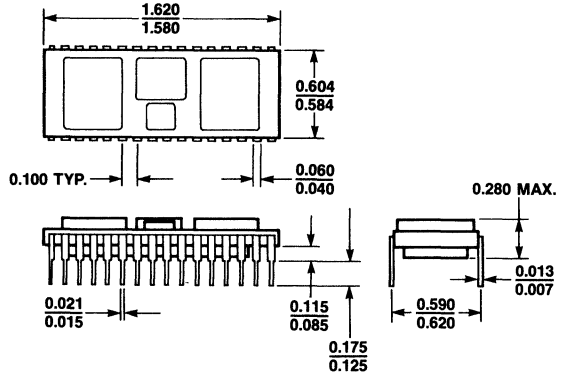
8

DUAL IN-LINE PACKAGES (Continued)

D28-3 28-PIN SIDEBRAZE (600 mil.)

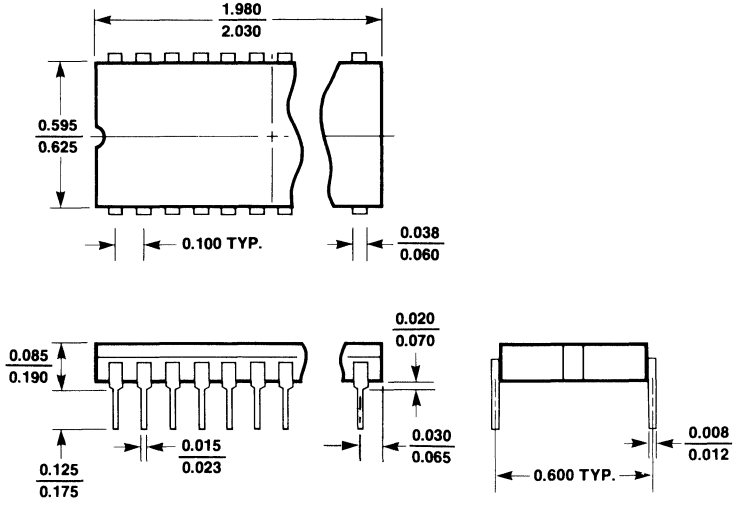


D32 32-PIN SIDEBRAZE

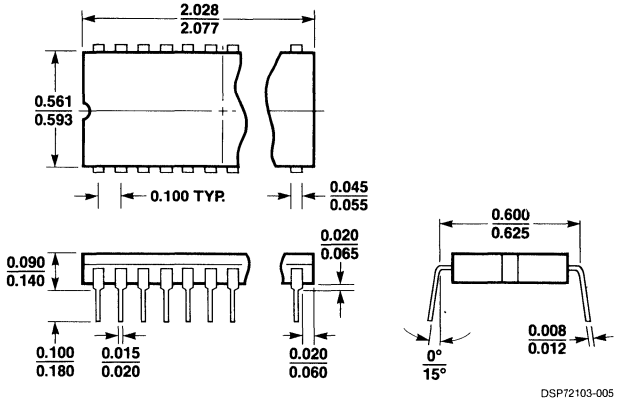


DUAL IN-LINE PACKAGES (Continued)

D40-1 40-PIN SIDEBRAZE



D40-2 40-PIN CERDIP



DSP72103-005

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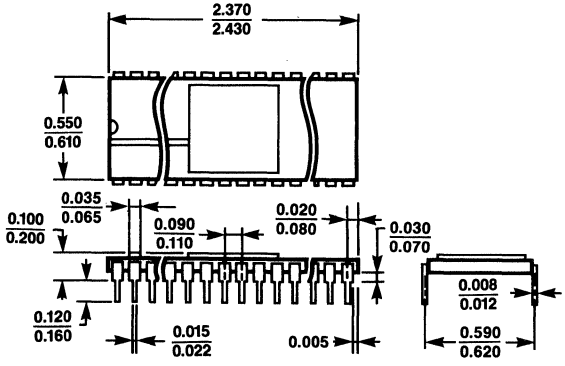
Integrated Device Technology, Inc

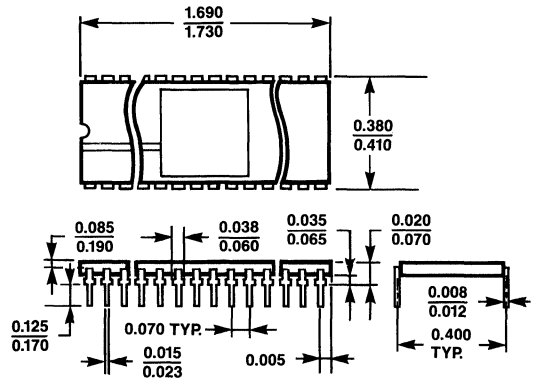
PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES (Continued)

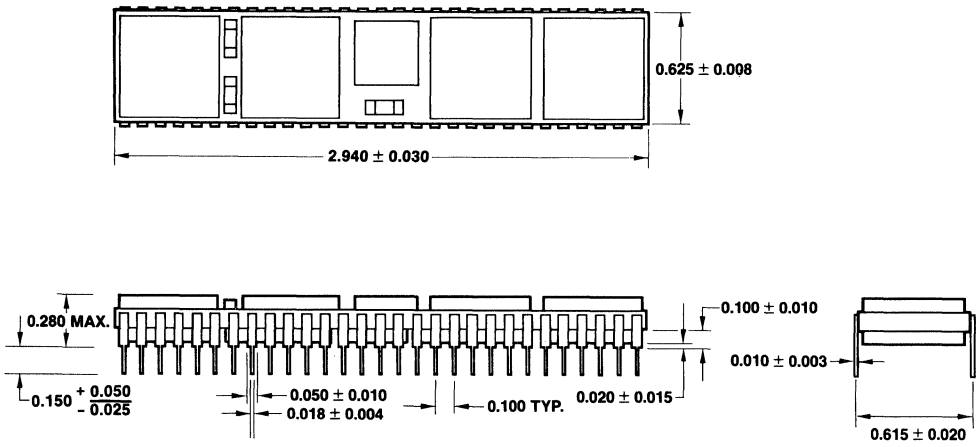
D48-1 48-PIN SIDEBRAZE (600 mil.)



D48-2 48-PIN SHRINK-DIP (400 mil.)

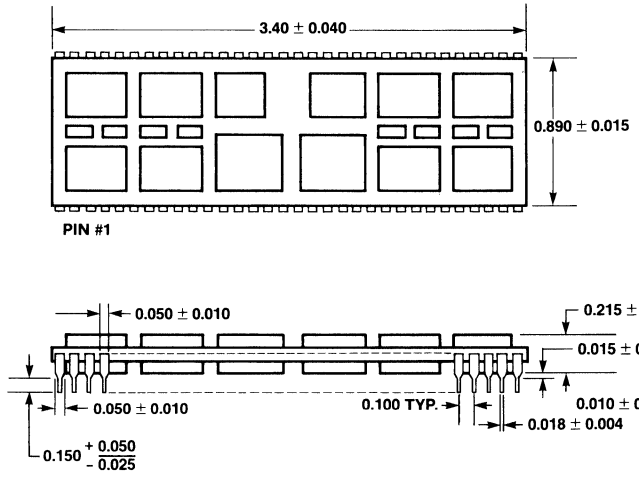


D58 58-PIN SIDEBRAZE

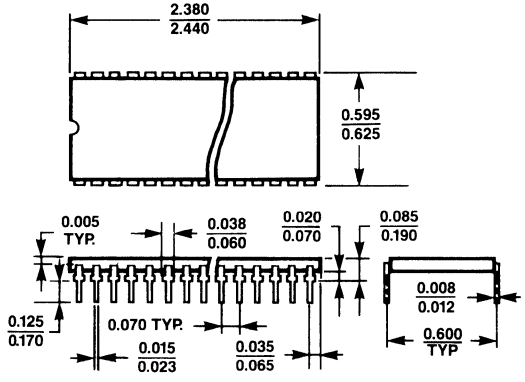


DUAL IN-LINE PACKAGES (Continued)

D64 64-PIN SIDEBRAZE



D68 68-PIN SIDEBRAZE SHRINK-DIP



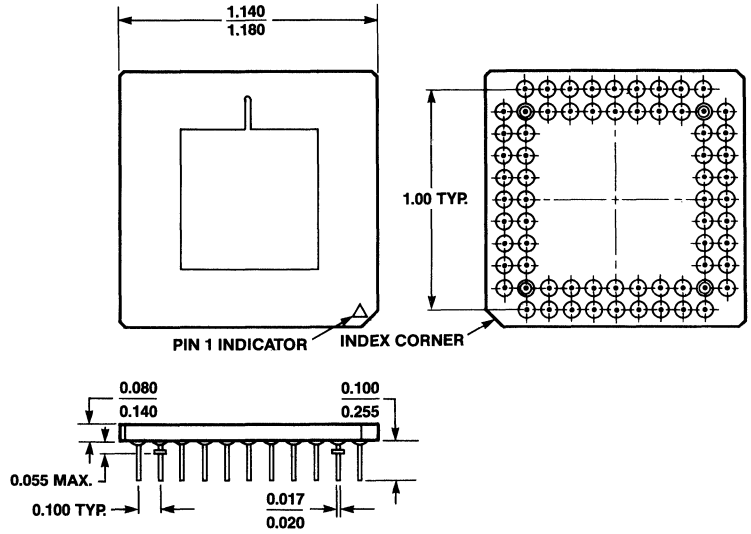
8

Integrated Device Technology, Inc

PACKAGE DIAGRAM OUTLINES

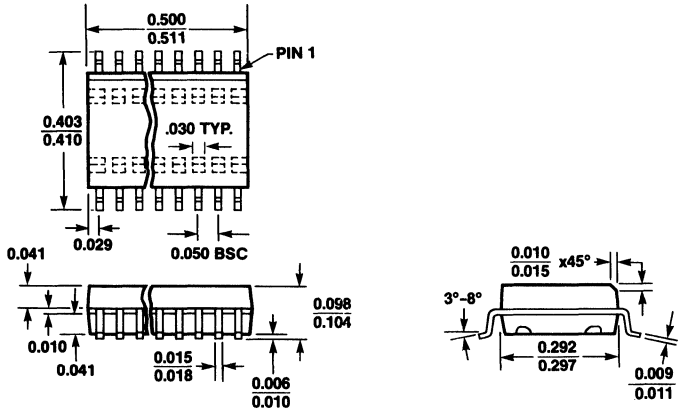
PIN GRID ARRAY

G68 68-PIN PGA



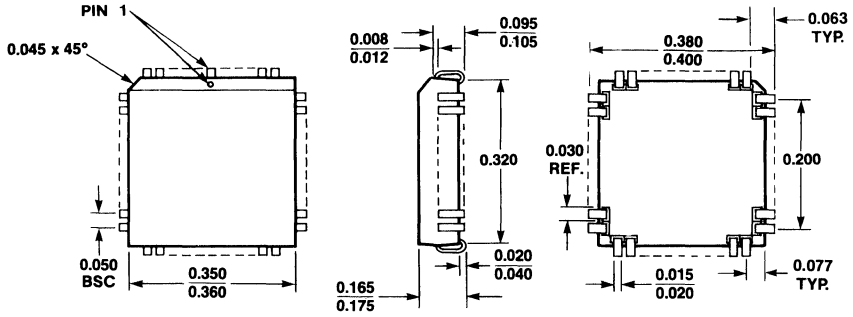
SMALL OUTLINE IC

S20 20-PIN SMALL OUTLINE IC

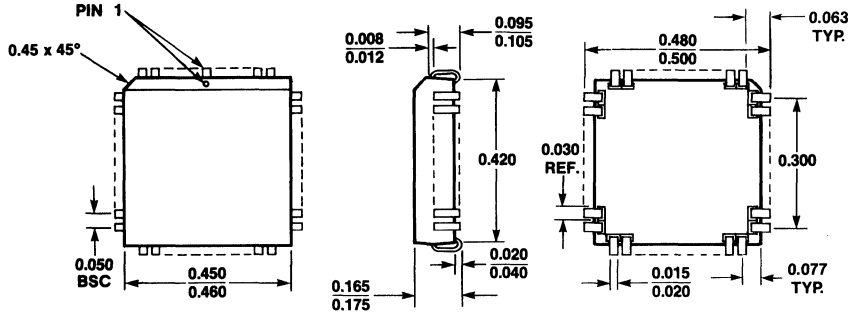


PLASTIC LEADED CHIP CARRIERS

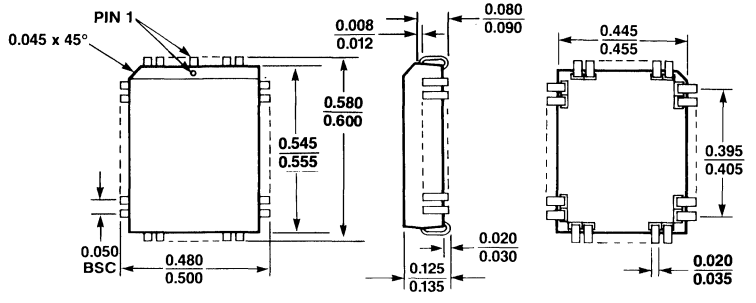
J20 20-PIN PLCC



J28 28-PIN PLCC



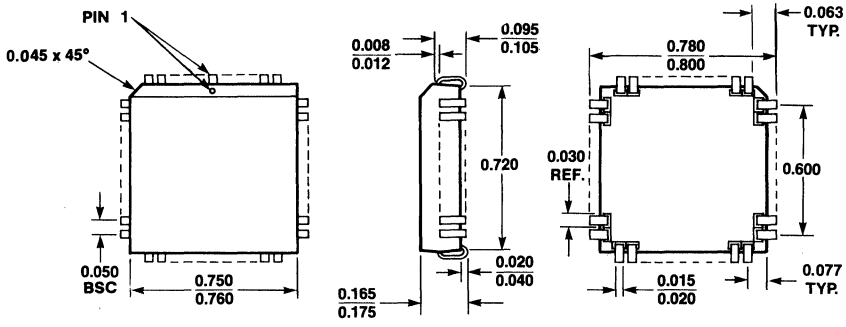
J32 32-PIN PLCC



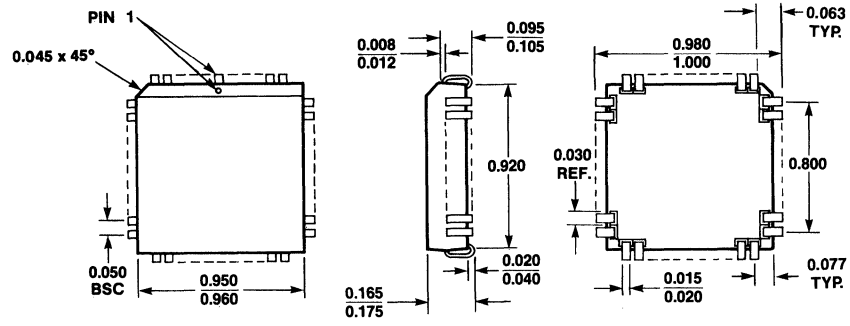
8

PLASTIC LEADED CHIP CARRIERS (Continued)

J52 52-PIN PLCC

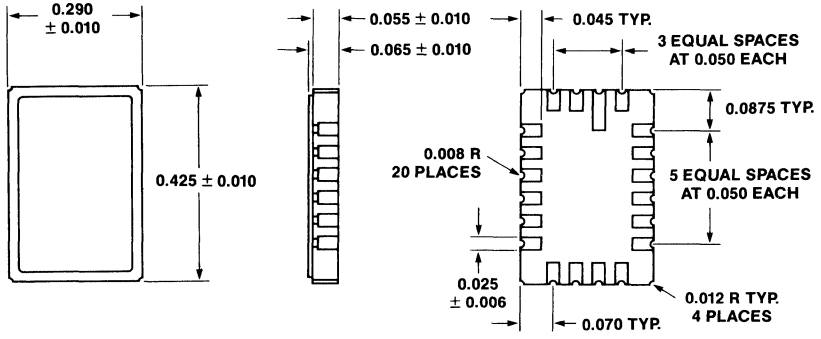


J68 68-PIN PLCC

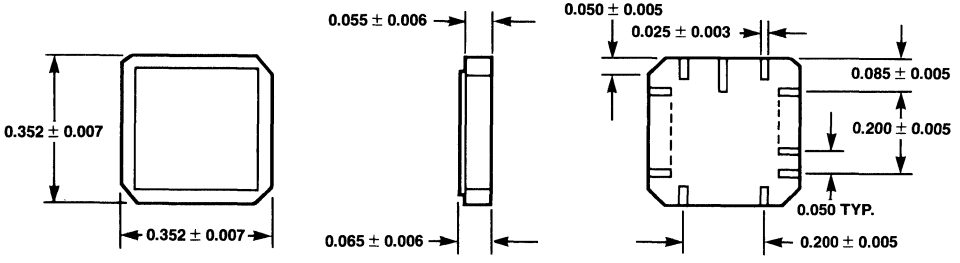


LEADLESS CHIP CARRIERS

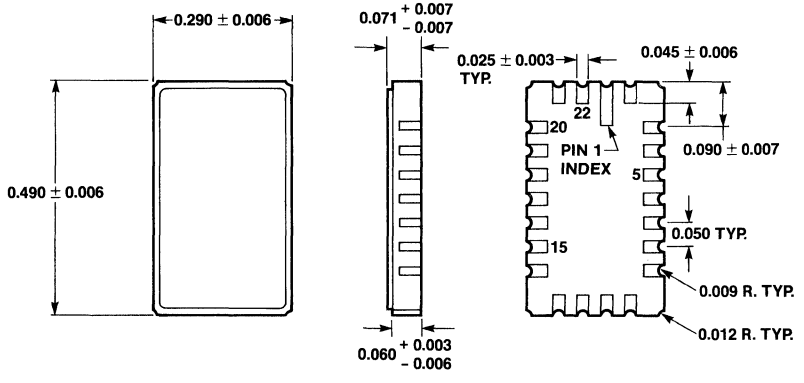
L20-1 20-PIN LCC



L20-2 2-PIN LCC



L22 22-PIN LCC



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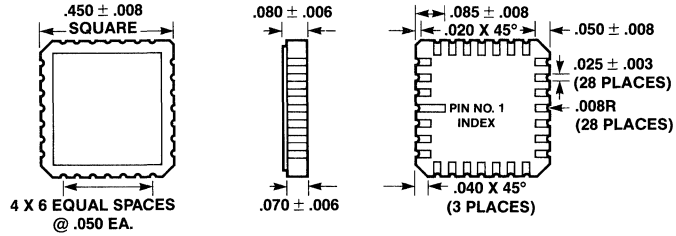
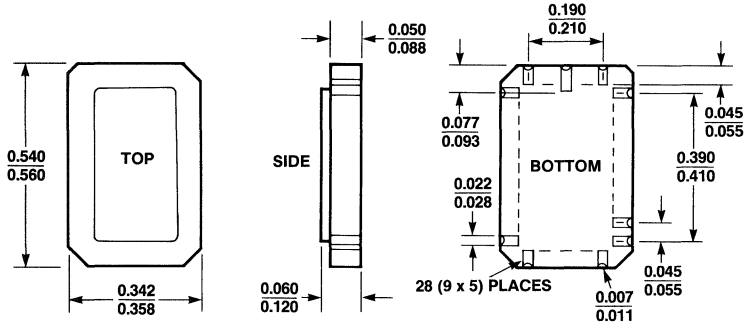
LEADLESS CHIP CARRIERS (Continued)

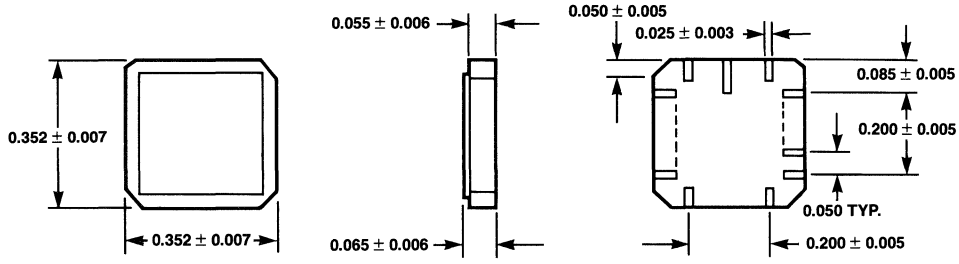
L28-1 28-PIN LCC



L28-2 28-PIN LCC

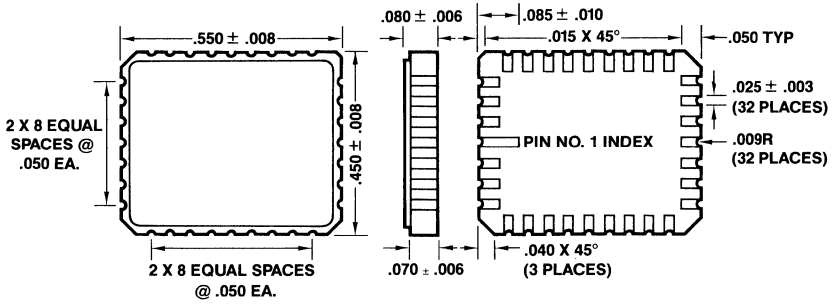


L28-3 28-PIN LCC

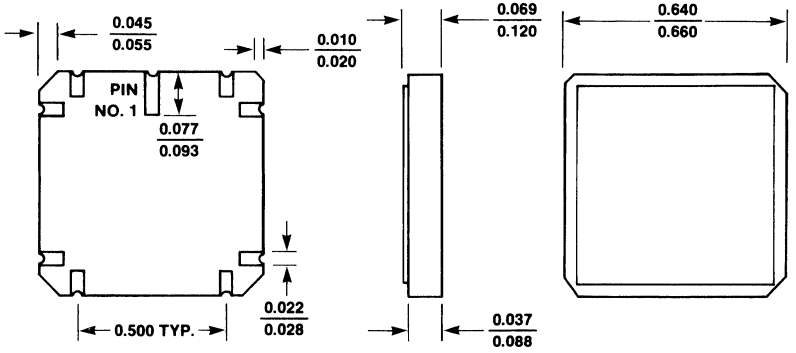


LEADLESS CHIP CARRIERS (Continued)

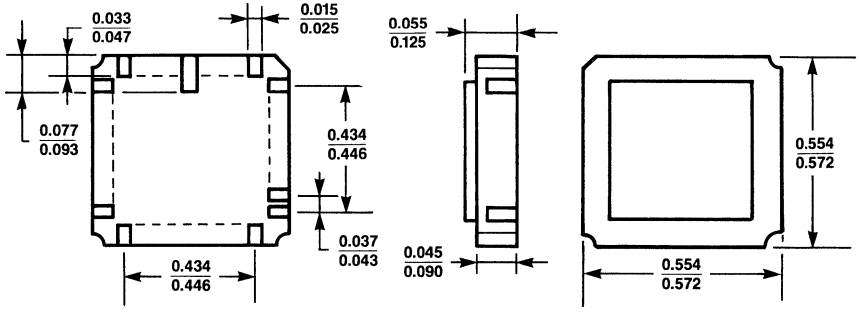
L32 32-PIN LCC



L44 44-PIN LCC



L48 48-PIN LCC



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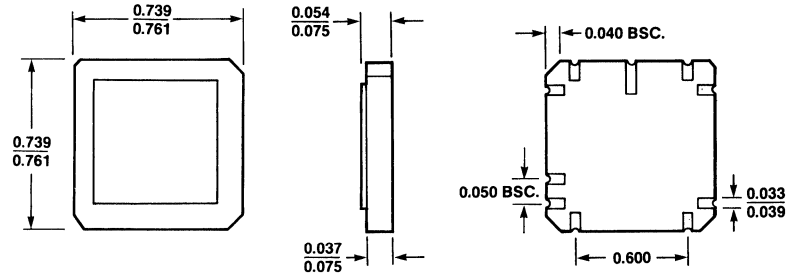
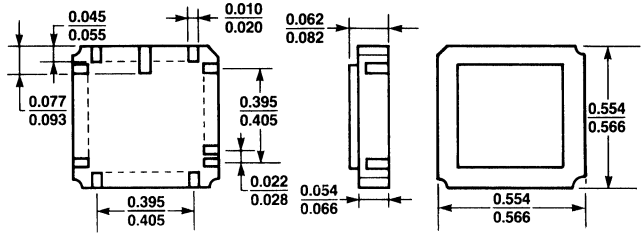
LEADLESS CHIP CARRIERS (Continued)

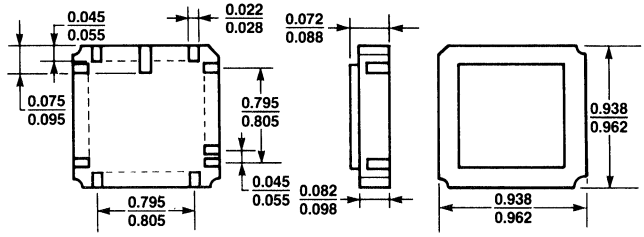
L52 52-PIN LCC



L68-1 68-PIN LCC



L68-2 68-PIN LCC

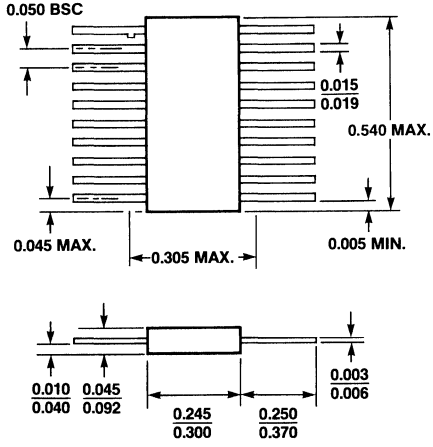


Integrated Device Technology, Inc

PACKAGE DIAGRAM OUTLINES

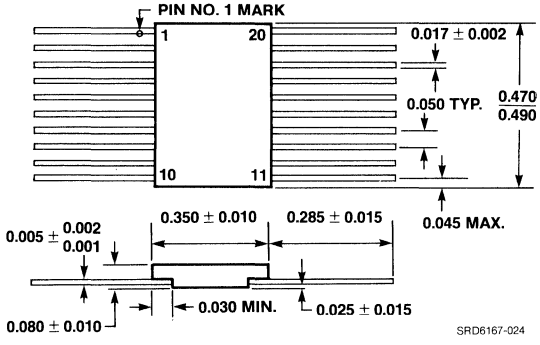
CERPAK

E20 20-LEAD CERPACK

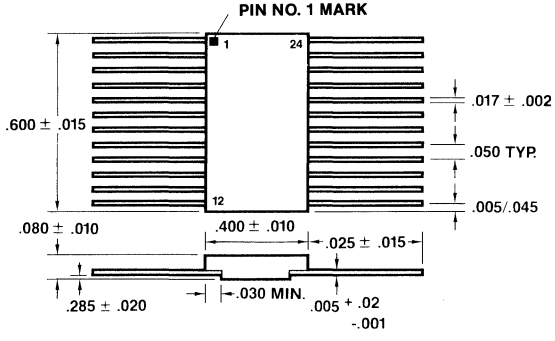


FLATPACKS

F20 20-LEAD FLATPACK



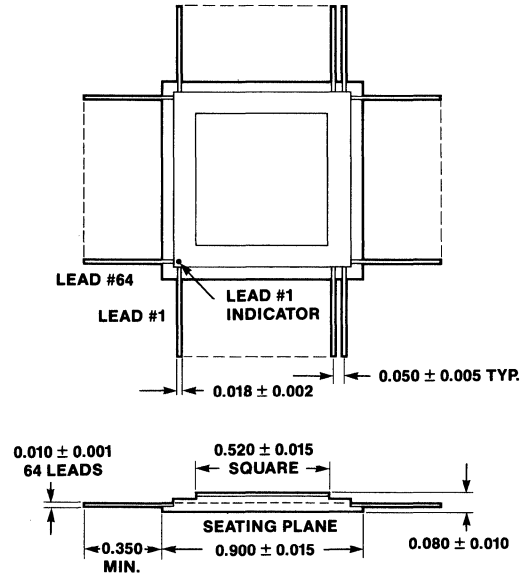
F24 24-LEAD FLATPACK



8

FLATPACKS (Continued)

F64 64-LEAD FLATPACK



ORDERING INFORMATION

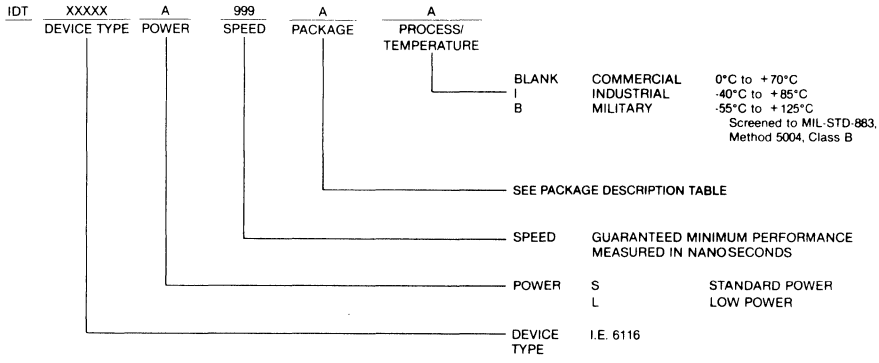
When ordering by TWX or Telex, the following format must be used:

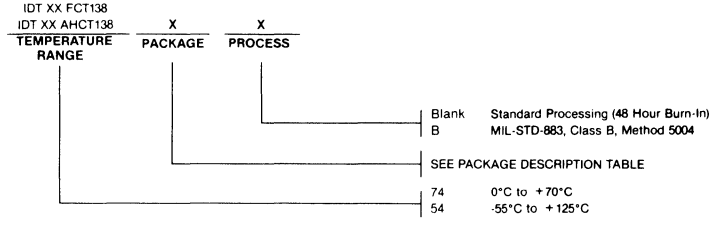
A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N
E. Customer Source Inspection. Y or N
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number —
   Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number.
K. Customer Part Number/Drawing Number/ Revision Level—
   Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses.

Federal Supply Code Number - 61772
Dun & Bradstreet Number - 03-814-2600
Federal Tax I.D. - 94-2669985
TLX# - 887766
FAX# - 408-737-3468

Minimum Order Quantities:
OEM - $500.00/$100 per line item
Distributor - $1,000.00/$100 per line item
100 piece minimum on all Flatpack orders

ORDERING DESCRIPTION





PACKAGE DESCRIPTION TABLE

P	PLASTIC DIP	L	LEADLESS CHIP CARRIER
D	CERDIP	XL	FINE-PITCH LCC
C	CERAMIC SIDEBRAZE	ML	MEDIUM-PITCH LCC
XC	CERAMIC SIDEBRAZE SHRINK-DIP		
T	THINDIP (300 mil, 24-Pin)	E	CERPACK
		F	FLATPACK
G	PIN GRID ARRAY		
		U	DIE
SO	PLASTIC SMALL OUTLINE IC		
J	PLASTIC LEADED CHIP CARRIER		

NOTE:
When a product is available in a package type with more than one pin count or package dimension, please indicate the package designator when ordering — (i.e. IDT6116L70L28-2 or IDT6116L70L32).

8

FACTORY DIRECT OFFICES

CORPORATE HEADQUARTERS
3236 Scott Boulevard
P.O. Box 58015
Santa Clara, CA 95052-8015
(408) 727-6116
TLX: 887766

NORTHWESTERN HEADQUARTERS
3236 Scott Boulevard
P.O. Box 58015
Santa Clara, CA 95052-8015
(408) 727-6116
TLX: 887766

SOUTHWESTERN REGIONAL OFFICE
12777 Valley View Street
Suite 262
Garden Grove, CA 92645
(714) 891-6651 or (213) 598-3076

CENTRAL HEADQUARTERS
999 Plaza Drive
Suite 400
Schaumburg, IL 60195
(312) 843-1262
TWX: 910-651-1910

NORTH CENTRAL REGIONAL OFFICE
3601 W. 77th Street
Suite 880
Minneapolis, MN 55435
(612) 831-5422
TLX: 291013

SOUTH CENTRAL REGIONAL OFFICE
5501 LBJ Freeway
Suite 500
Dallas, TX 75240
(214) 458-0466 or 458-0467
TWX: 910-861-4034

EASTERN HEADQUARTERS
15 Pleasant Street Connector
Suite 502
Framingham, MA 01701
(617) 872-4900
TLX: 855249

NORTHEASTERN REGIONAL OFFICE
111 Smithtown Bypass
Suite 202
Hauppauge, NY 11787
(516) 360-3370
TLX: 62921896

SOUTHEASTERN REGIONAL OFFICE
478 Ballard Drive
Suite 35A
Melbourne, FL 32935
(305) 242-1821
TLX: 592163

EUROPEAN HEADQUARTERS
#5 Bridge Street
Leatherhead
Surrey, UK KT228BL
44-372-377375
TLX: 851-946240

DOMESTIC SALES REPRESENTATIVES

ALABAMA
Montgomery Marketing
Huntsville, AL
(205) 830-0498

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Integrated Device Technology, Inc.
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(408) 727-6116

ARIZONA
Western High Tech Marketing
Scottsdale, AZ
(602) 860-2702

ARKANSAS
Integrated Device Technology, Inc.
Dallas, TX
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Bestronics Inc.
Irvine, CA
(714) 261-7233

Bestronics Inc.
Woodland Hills, CA
(818) 704-5616

Integrated Device Technology, Inc.
Garden Grove, CA
(714) 891-6651

Technology Sales Inc.
Mountain View, CA
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