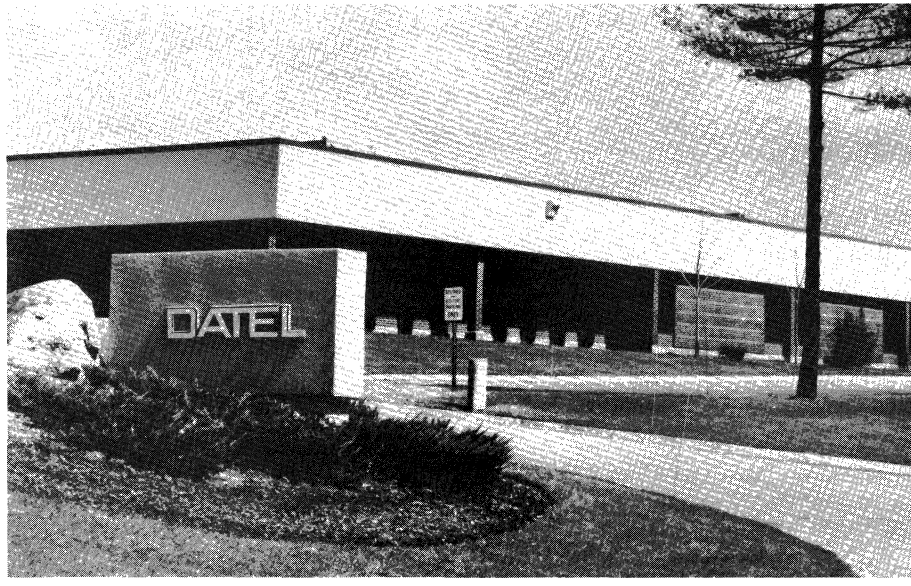
DATEL

DATA CONVERSION CATALOG

DATEL

The Proven Source for Innovation and Excellence in Precision Data Acquisition



COMPANY HISTORY

DATEL is a multinational company which was founded in 1970, and is located approximately 35 miles from Boston in Mansfield, Massachusetts. Our modern 180,000 square-foot facility houses our administrative offices, components and sub-systems engineering groups, modular and sub-systems production facilities, and the most modern thin-film and thick-film hybrid production facility in the industry. DATEL's hybrid manufacturing operation is a fully certified MIL-STD-1772 facility, supporting our high quality standards.

Our worldwide sales network extends to every major data acquisition product marketplace. And, the people who implement this sales network are skilled professionals dedicated to providing our customers with the highest possible standards of data acquisition products available today.

PRODUCT INFORMATION

DATEL offers one of the industry's broadest product lines, meeting the rapidly growing need for data acquisition components and sub-systems to interface with computers in industrial, commercial, scientific and military applications. These products employ five basic technologies: monolithic CMOS, monolithic bipolar, thin-film hybrid, thick-film hybrid and discrete component circuits. Many products employ a combination of these technologies to achieve higher levels of performance and complexity. The present product lines include: data converters, sample-hold amplifiers, analog multiplexers, amplifiers, data acquisition sub-systems, computer analog I/O boards, process monitor/controllers, digital panel meters, thermal printers, digital calibrators and power supplies.

ABOUT THIS CATALOG

This comprehensive catalog includes detailed data sheets on DATEL's complete product line. Products are categorized by function and organized into QUICK SELECTION CHARTS at the beginning of each section for your convenience.

Further details and applications information may be obtained by returning the enclosed reply card. For immediate attention, contact the nearest DATEL sales office.

DATEL application engineers are always available to answer any questions that may arise concerning the application of our products.

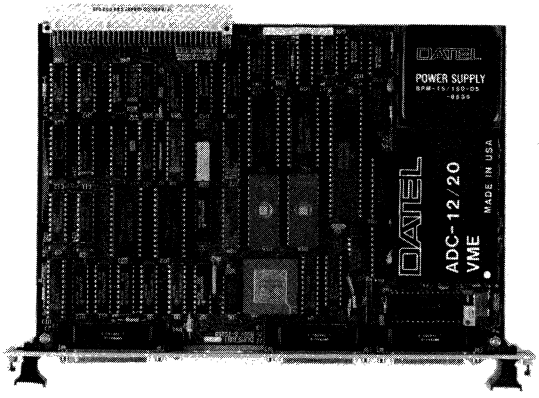
DATEL

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194
TEL. (508) 339-3000/TLX 174388/FAX (508) 339-6356

PRODUCT INDEX

NEW PRODUCTS FROM DATEL

DVME-601
16S or 8D-Channel 68010-based VME A/D Coprocessor Board



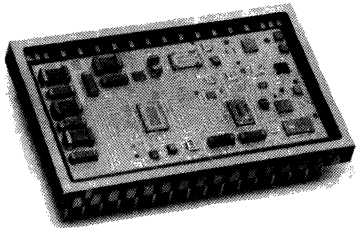
- Local 8 MHz 68010 CPU Plus:
  - 64 Kb Private RAM
  - 64/128 Kb EPROM
  - 64 Kb Dual-ported RAM
- A/D choices 12 to 16 bits, down to 2 µSec.
- 16 Single-ended or 8 differential analog input channels
- Simultaneous A/D scanning. Ideal for DSP, FFT, ATE, and graphics.
- Monitor/Executive firmware to run in "no program mode" or from user programs
- Peripheral 68901 I/O:
  - RS-232 serial port
  - 3 timer/counters, 5 I/O bits
- Sample-to-memory transfers at up to 250 KHz
- Easy interrupt intergration with VERSAdos, PDOS, OS-9, etc.

DC-DC Converters

More than 60 new DC-DC converters have been added to the Product Line which include these features:

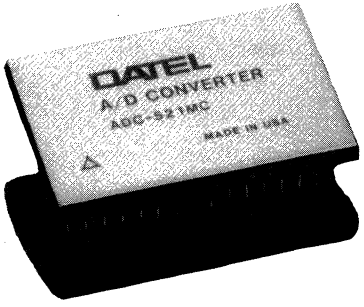
- Efficiency up to 80%
- 2-1 input voltage ranges
- Miniature size
- Single, dual, and triple outputs

ADS-115/116
10-Bit, 1 MHz Sampling A/D Converters



- 10-Bit resolution
- 1 MHz throughput
- 15 M ohm input impedance
- Includes fast Sample/Hold amplifier
- 3-state output TTL and CMOS compatible

ADC-520,521
12-Bit, Ultra-fast Low-power A/D converter

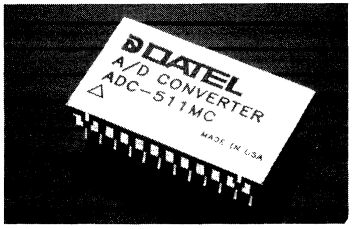


- 12-Bit resolution
- 800 nanosecond maximum conversion time
- Pin-programmable input ranges
- Internal high impedance buffer
- Low 1.6 watts power consumption
- Three-state output buffers
- Small 32-pin DIP

SHM-30C
Very high speed, precision Sample/Hold amplifier

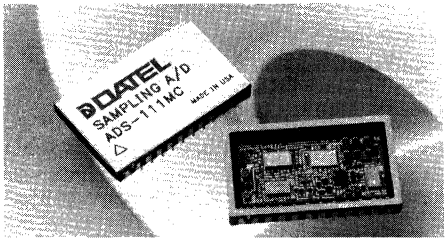
- 500 nSec. acquisition time to 0.01%
- 0.01µV/µSec droop rate
- 90V/µSec slew rate
- Internal hold capacitor

NEW PRODUCTS FROM DATEL



ADC-511
12-Bit, High-Speed,
Low Power A/D Converter

- 1.0 Microsecond maximum conversion time
- Low-power, 925 milliwatts
- Three-state output buffers
- Functionally complete
- Small 24-pin DIP

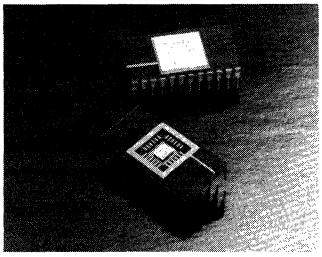


ADS-111
12-Bit, 500 KHz, Low Power
Sampling A/D Converter

- Internal Sample/Hold
- Functionally complete
- Small 24-pin DIP
- Low-power, 1.4 Watts
- Three-state output buffers

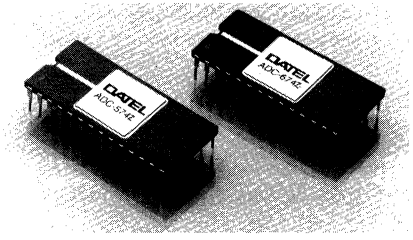
ADS-125, ADS-126
12-Bit, 700 KHz, Low Power
Sampling A/D Converters

- 15 M ohm input impedance
- Pin-programmable input ranges
- Low-power, 2.1 Watts
- Three-state output buffers



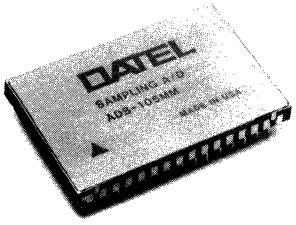
ADC-208
8-Bit, 20 MSPS
1.2 Micron CMOS Flash A/D Converter

- 10 MHz full power bandwidth
- Sample-hold not required
- Low power CMOS
- +5V dc operation
- 8-Bit latched three-state outputs with overflow bit
- MIL-STD-883B versions



ADC-574Z, ADC-674Z
Complete 12-Bit A/D Converters
with Sample-Hold, Reference, and Clock

- Pin-to-pin compatible with industry standard HI574A/674A
- No missing codes over temperature
- 15 μSec. conversion time (ADC-674Z)
- 150 mW max. power dissipation



ADS-105/106
12-Bit, 1 MHz
Sampling A/D Converters

- 12-Bit resolution
- 1 MHz throughput
- 15 M ohm input impedance
- Includes fast Sample/Hold amplifier
- 3-state output, TTL and CMOS compatible

NEW PRODUCTS FROM DATEL

PM-5050
Thermocouple Input
Process Monitor/Controller

- Supports direct connection of thermocouple types J, K, T, S, B, E, N, and R
- °C or °F display; 0.1 or 1.0 degree resolution
- Cold junction compensation disable option
- Automatic display of open TC input condition

PM-5060
RTD and Thermistor Input
Process Monitor/Controller

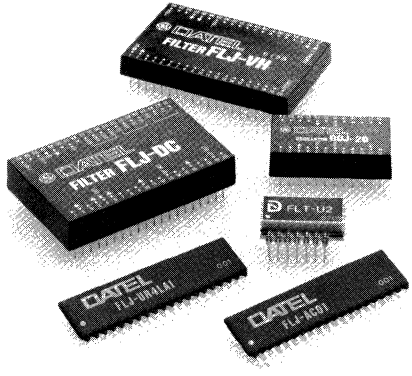
- Supports direct connection of 100Ω platinum RTD's (American or European standards) and thermistors (2252Ω, 3000Ω, 5000Ω, 10000Ω)
- Two-, Three-, or four-wire operation
- °C or °F display; 0.1 or 1.0 degree resolution
- Automatic display of open circuit condition

PM-5070
Strain Gage
Process Monitor/Controller

- Two inputs: ±50 mV (bridge output) ±10V reference
- Simple bridge calibration and scaling function
- Two user-defines math functions for sophisticated output manipulation and control algorithms
- Cycling six digit display of up to eight system variables, including input peaks and valleys

PM-5080
Dual-Channel Voltage/Current Signal Input
Process Monitor/Controller

- Two input channels: 0-100 mV (jumper selectable for 0-20 mA) and 10V
- Two user-defined math functions for sophisticated output manipulation and control algorithms
- Cycling six digit display of up to eight system variables, including input peaks and valleys
- Simple scaling procedure with standard or user-defined engineering units



Tunable Active Filters
More than 30 new Active Filters have been added to the Product Line

- Digital, Voltage, and Resistive Tuning
- State Ready Filters
- Selectable for Bessel, Butterworth, Chebychev, or Elliptical Response
- Small Hybrid Packaging
- Rolloffs up to 140 dB/Octave
- High Pass, Low Pass, Band Pass, Band Reject Filters
- Switched Capacitor 7th Order Low Pass Filtering

HIGH-RELIABILITY PROGRAMS

DATEL is committed to meeting the demanding requirements of military, aerospace and severe environment applications. Toward that end, DATEL offers a few options in its quality programs.

OPTION 1 MIL-STD-883 CLASS B COMPLIANT DEVICES

DATEL has received MIL-STD-1772 certification for its hybrid facility. This approval certifies that DATEL meets the stringent standards requirements surrounding the facilities, material, processes, personnel training, design analysis, documentation and equipment used to manufacture hybrid microcircuits. MIL-STD-883 establishes uniform methods, controls and procedures for designing, testing and certifying microelectronic devices.

New contracts negotiated after December 31, 1984 require that, if MIL-STD-883 compliancy is called for, parts supplied must meet the current intent of MIL-STD-883 (i.e., Element Evaluation and MIL-STD-1772 Certification, etc). DATEL's -883 program offers products in full compliance with MIL-STD-883, Class B.

The accompanying chart gives a concise overview of MIL-STD-883 screening requirements and their implications for DATEL customers.

TEST	METHOD	PURPOSE
Internal Visual (Precap)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical or thermal stress
Stabilization Bake	Method 1008 Test Condition C, 24 hrs. at 150 °C	Eliminates device failure due to storage at elevated temperatures.
Temperature Cycling	Method 1010, Test Condition C, -65 °C to 150 °C	Determines resistance of device to sudden exposure to extreme temperature changes. Removes potential failures due to thermal stress on bonds, etc.
Constant Acceleration	Method 2001, Test Condition A, Y AXIS, 5 kg.	Eliminates potential failures due to structural or mechanical weakness not detected in shock or vibration tests.
Burn-in Test	Method 1015, Test Condition B, 160 hrs. at +125 °C	Stresses devices at temperature in order to eliminate infant mortailty failures.
PDA 10%	Static Tests performed at +25 °C	Percent defective allowable—Rejects lots with static test failures greater than 10%.
Final Electrical Tests	Performed at +25 °C and at max. and min. operating temperatures	Verifies that device still meets specified data sheet parameters.
Seal Fine and Gross	Method 1014, Test Condition A (fine), 1 x 10^{-7} cc/Sec. for volume of $\geq$0.5 to <1.0 cm^3 and 5 x 10^{-8} cc/Sec. for volume of $\geq$1.0 to <10.0 cm^3. Test condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
External Visual	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

MIL-STD-883 compliancy also requires that complete documentation be available to support the product. An analysis of the design along with element and package evaluations are performed to ensure a high quality product. The manufacturing process is also stringently controlled in order to obtain the high quality level.

Initial qualification requires passing the MIL-STD-883 tests for groups A, B, C and D. After initial qualification, groups A & B are tested for all lots. Group C is tested iniitially and to qualify any product changes which may occur. Group D testing is also performed initially and at intervals not exceeding 6 months for future lots.

MIL-STD-883 PRODUCTS

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY
ADC-HZ12B/883B	12 Bits	8 µSec	± 1/2 LSB
ADC-HX12B/883B	12 Bits	20 µSec	± 1/2 LSB
ADC-816/883B	10 Bits	800 nSec	± 1/2 LSB
ADC-208/883B	8 Bits	50 nSec	± 1.5 LSB
ADC-207/883B	7 Bits	50 nSec	± 1 LSB

DIGITAL-TO-ANALOG CONVERTERS

MODEL NO.	RESOLUTION	SETTLING TIME	LINEARITY
DAC-HP16B/883B	16 Bits	15 µSec	± 2 LSB
DAC-HZ12B/883B	12 Bits	3 µSec	± 1/2 LSB
DAC-HK12B/883B	12 Bits	3 µSec	± 1/2 LSB

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT
HDAS-16/883B	12 Bits	16 SINGLE-ENDED	50 KHz

Contact DATEL for information on future MIL-STD-883 compliant devices now being qualified.

OPTION 2 -QL PROGRAM

DATEL's -QL (Quality Level) program offers enhanced reliability over the standard DATEL products through subjecting the devices to environmental stresses. The -QL screening is not intended to imply compliance with MIL-STD-883 and any devices screened to this program are classified as non-compliant devices as defined in paragraph 1.2 of MIL-STD-883.

It should be noted however, that if a contract was negotiated prior to December 31, 1984 and you supplied a part which your Specification Control Drawing (SCD) described as compliant to MIL-STD-883, you may continue to fulfill that contract with parts which satisfy the conditions of that specification. Contact DATEL to determine if a particular -QL product is applicable.

The accompanying chart gives a concise overview of the -QL screening requirements and their implications for DATEL customers.

DATEL QL SCREENING PROGRAM

TEST	TEST CONDITION	PURPOSE
Internal Visual (100% Precap)	Test Method 2017	Eliminate visual defects prior to seal
Stabilization Bake 100%	TM 1008, Condition C 24 hours at + 150 °C (Optional if TM 1030 is used)	Eliminates failures due to high temp storage
Temperature Cycling, 100%	TM 1010, Condition C -65 to +150 °C, 10 cycles	Eliminates failures due to mechanical weakness
100% Constant Acceleration	TM 2001, Condition A Y1 Axis, 5000 G	Eliminates failures due to mechanical weakness
100% Burn-in	Static burn-in 160 hrs. at +125 °C (Similar to TM 1015 or TM 1030)	Eliminates failures due to infant mortality
100% Final Electrical Test	Performed at +25 °C, TMIN, and TMAX operating temperatures	Verifies that devices meet speicifications over temperature range
100% Fine and Gross Leak	Test Method 1014 Condition A (fine) 5 x 10^{-7} cc/Sec. Condition C (gross)	Insures hermeticity for high humidity environments
100% External Visual	Test Method 2009	Insures proper marking, construction, workmanship

-QL PRODUCTS

SAMPLE-HOLD AMPLIFIERS

MODEL NO.	LINEARITY	ACQUISITION TIME	HOLD MODE DROOP
SHM-91MM-QL	0.003%	2 µSec.	5.0 µV/µSec.
SHM-45MM-QL	0.01%	200 nSec.	0.5 µV/µSec.
SHM-4860MM-QL	0.01%	200 nSec.	0.5 µV/µSec.
SHM-9MM-QL	0.01%	6 µSec.	0.2 mV/mSec
SHM-6MM-QL	0.02%	2 µSec.	10 µV/µSec.
SHM-HUMM-QL	0.1%	25 nSec.	50 µV/µSec.
SHM-40MM-QL	0.1%	40 nSec.	100 µV/µSec.

OPERATIONAL AMPLIFIERS

MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT
AM-500MM-QL	3 mV	130 MHz	+10V at 50 mA
AM-1435MM-QL	5 mV	1000 MHz	+ 7V at 14 mA

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT
HDAS-16MM-QL	12 Bits	16 Single-Ended	50 KHz
HDAS-8MM-QL	12 Bits	8 Diff-Ended	50 KHz

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY
ADC-505BMM-QL	12 Bits	550 nSec.	± 1 LSB
ADC-508BMM-QL	12 Bits	700 nSec.	± 1 LSB
ADC-520MM-QL	12 Bits	800 nSec.	± 1/2 LSB
ADC-521MM-QL	12 Bits	800 nSec.	± 1/2 LSB
ADC-817AMM-QL	12 Bits	2 µSec.	± 1 LSB
ADC-810MM-QL	12 Bits	2 µSec.	± 1 LSB
ADC-827AMM-QL	12 Bits	3 µSec.	± 1 LSB
ADC-811MM-QL	12 Bits	3 µSec.	± 1 LSB
ADC-HZ12BMM-QL	12 Bits	8 µSec.	± 1/2 LSB
ADC-5211H-QL	12 Bits	13 µSec.	± 1/2 LSB
ADC-5212H-QL	12 Bits	13 µSec.	± 1/2 LSB
ADC-5214H-QL	12 Bits	13 µSec.	± 1/2 LSB
ADC-5215H-QL	12 Bits	13 µSec.	± 1/2 LSB
ADC-5216H-QL	12 Bits	13 µSec.	± 1/2 LSB
ADC-HX12BMM-QL	12 Bits	20 µSec.	± 1/2 LSB
ADC-HC12BMM-QL	12 Bits	300 µSec.	± 1/2 LSB
ADC-510BMM-QL	10 Bits	510 nSec.	± 1/2 LSB
ADC-515BMM-QL	10 Bits	700 nSec.	± 1/2 LSB
ADC-816MM-QL	10 Bits	800 nSec.	± 1/2 LSB
ADC-826MM-QL	10 Bits	1.4 µSec.	± 1/2 LSB
ADC-815MM-QL	8 Bits	700 nSec.	± 1/2 LSB
ADC-5101H-QL	8 Bits	900 nSec.	± 1/2 LSB
ADC-825MM-QL	8 Bits	1 µSec.	± 1/2 LSB

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

ADS-105MM-QL	12 Bits	1 MHz	± 1 LSB
ADS-106MM-QL	12 Bits	1 MHz	± 1 LSB
ADS-125MM-QL	12 Bits	700 KHz	± 1/2 LSB
ADC-HS12BMM-QL	12 Bits	66 KHz	± 1/2 LSB
ADS-115MM-QL	10 Bits	1 MHz	± 1/2 LSB
ADS-116MM-QL	10 Bits	1 MHz	± 1/2 LSB

DIGITAL-TO-ANALOG CONVERTERS

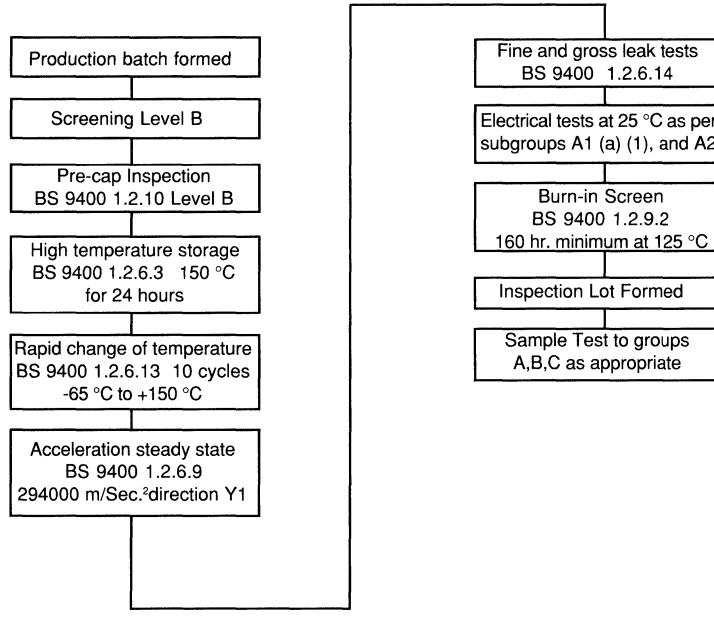
MODEL NO.	RESOLUTION	SETTLING TIME	LINEARITY
DAC-HP16BMM-QL	16 Bits	15 µSec.	± 2 LSB
DAC-HF12BMM-QL	12 Bits	50 nSec.	± 1/2 LSB
DAC-HK12BMM-QL	12 Bits	3 µSec.	± 1/2 LSB
DAC-HZ12BMM-QL	12 Bits	3 µSec.	± 1/2 LSB
DAC-HF10BMM-QL	10 Bits	25 nSec.	± 1/2 LSB
DAC-HF8BMM-QL	10 Bits	25 nSec.	± 1/2 LSB

OPTION 3 BS9000 PROGRAM

DATEL also has a BS9000 program in compliance with British Standards for high reliability devices. BS9000 is the United Kingdom's national system for the independent inspection approval and surveillance of manufacturers, distributors and test laboratories in the electronic component industry.

The accompanying product flow gives an overview of the BS9000 products through screening and quality conformance inspection.

BS9000 Screening Requirements



BS9000 PRODUCTS

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY
ADC-303-XXXXX	8 BITS	10 nsec	+ 1/2 LSB
ADC-208-XXXXX	8 BITS	50 nsec	+ 1.5 LSB

Parts qualified to the BS9000 specification have a quality level equivalent to MIL-M-38510 giving a quality factor of 1.

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GENERAL INDEX

ANALOG-TO-DIGITAL CONVERTERS

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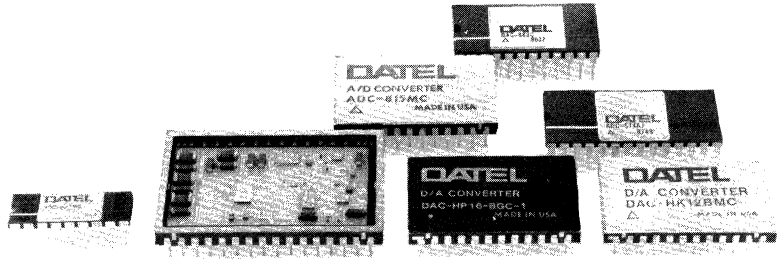
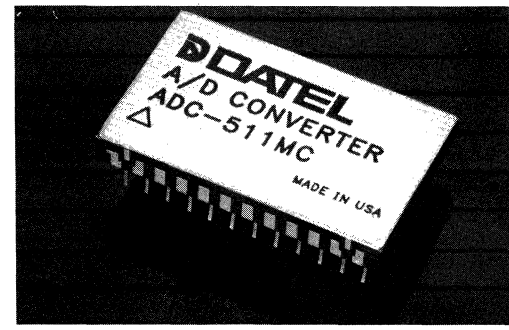


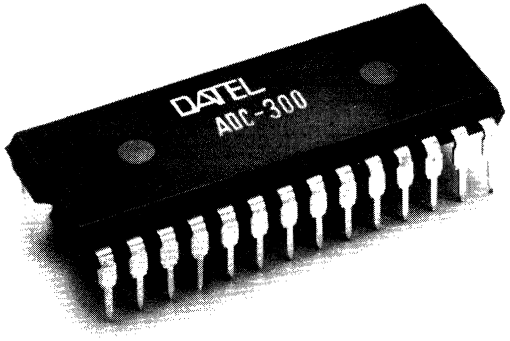
GENERAL PURPOSE A/D CONVERTERS

MODEL	RESOLUTION	CONVERSION TIME (MAX)	LINEARITY (MAX)	INPUT RANGE	OUTPUT CODING	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
ADC-EH8B2	8-Bits	2 µs	±1/2 LSB	0 to +10V	Bin, 2C	2 x 2 x 0.375 in.	0 to +70	1-192
ADC-EH8B1		4 µs		±5V		(51 x 51 x 10 mm)		
ADC-847A	8-Bits	9 µs	±1 LSB	0 to +5V, +10V	Bin	18-pin DIP	0 to +70	1-127
ADC-847B			±1/4 LSB	±5V, ±10V		Monolithic		
ADC-830C	8-Bits	100 µs	±1/2 LSB	0 to +5V	Bin	20-pin DIP Monolithic	0 to +70	1-121
ADC-EK8B	8-Bits	1.8 ms	±1/2 LSB	0 to +10V ±5V	Bin	24-pin DIP Monolithic	0 to +70	1-195
ADC-ET-8BC	8-Bits	1.8 ms	±1/2 LSB	0 to +10V	Bin	24-pin DIP	0 to +70	1-199
ADC-ET8BM				±5V		Monolithic	-55 to +125	
ADC-EH10B2	10-BitS	2 µs	±1/2 LSB	0 to +10V	Bin, 2C	3 x 2 x 0.375 in.	0 to +70	1-183
ADC-EH10B1		4 µs		±5V		(76 x 51 x 10 mm)		
ADC-EK10B	10-Bits	6 ms	±1/2 LSB	0 to +10V ±5V	Bin	24-pin DIP Monolithic	0 to +70	1-195
ADC-EK10BC	10-Bits	6 ms	±1/2 LSB	0 to +10V	Bin	24-pin DIP	0 to +70	1-195
ADC-ET10BM				±5V		Monolithic	-55 to +125	1-199
ADC-856C	10-Bits	1 µs/LSB	±1/2 LSB	0 to +5V, +10V	Bin	28-pin DIP	0 to +70	1-131
ADC-856M				±2.5V, ±5V, ±10V		Monolithic	-55 to +125	
ADC-EH12B3	12-Bits	2 µs	±1/2 LSB	0 to +10V ±5V	Bin, 2C	4 x 2 x 0.375 in. (102 x 51 x 10 mm)	0 to +70	1-189
ADC-EH12B2		4 µs						1-186
ADC-EH12B1		8 µs						
ADC-HZ12BGC	12-Bits	8 µs	±1/2 LSB	0 to +5V, +10V ±2.5V, ±5V, ±10V	C Bin C2C	32-pin DIP Hybrid	0 to +70	1-213
ADC-HZ12BMC							0 to +70	
ADC-HZ12BMM							-55 to +125	
ADC-5211	12-Bits	13 µs	±1/2 LSB	±5V	C Bin	24-pin DIP Hybrid	0 to +70	1-77
ADC-5211H							-55 to +125	
ADC-5212				±10V			0 to +70	
ADC-5212H							-55 to +125	
ADC-5214				±5V			0 to +70	
ADC-5214H							-55 to +125	
ADC-5215				±10V			0 to +70	
ADC-5215H							-55 to +125	
ADC-5216				0 to +10V			0 to +70	
ADC-5216H							-55 to +125	
ADC-HX12BGC	12-Bits	20 µs	±1/2 LSB	0 to +5V, +10V ±2.5V, ±5V, ±10V	C Bin C2C	32-pin DIP Hybrid	0 to +70	1-213
ADC-HX12BMC							0 to +70	
ADC-HX12BMM							-55 to +125	
ADC-HC12BMC	12-Bits	300 µs	±1/2 LSB	0 to +5V, ±10V ±2.5V, ±5V, ±10V	Bin, 2C	32-pin DIP Hybrid	0 to +70	1-205
ADC-HC12BMM							-55 to +125	
ADC-EK12DC	3 1/2 Digits	12 ms	±1/2 LSB	0 to +10V	BCD	24-pin DIP Monolithic	0 to +70	1-195
ADC-EK12DR							-25 to +85	
ADC-EK12DM							-55 to +125	
ADC-EK12B	12-Bits	24 ms	±1/2 LSB	0 to +10V ±5V	Bin	24-pin DIP Monolithic	0 to +70	1-195
ADC-ET12BC	12-Bits	24 ms	±1 1/2 LSB	0 to +10V ±5V	Bin	24-pin DIP Monolithic	0 to +70	1-199
ADC-ET12BR			±1/2 LSB				-25 to +85	
ADC-ET12BM			±1/2 LSB				-55 to +125	
ADC-7109	12-Bits	33 ms	1 Count	V+ to V-	Bin	40-pin DIP Monolithic	0 to +70	1-82



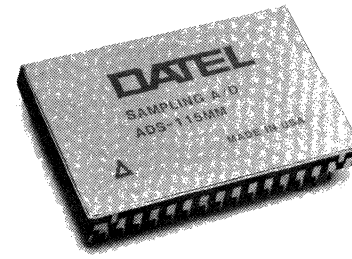
HIGH SPEED A/D CONVERTERS

MODEL	RESOLUTION	CONVERSION TIME (Max)	LINEARITY (Max)	INPUT RANGE	OUTPUT CODING	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
ADC-815MC	8 Bits	700 ns	±1/2 LSB	0 to +5V, +10V, +20V ±2.5V, ±5V, ±10V	Bin, 2C	24-pin DIP Hybrid	0 to +70 -55 to +125	1-106
ADC-815MM								
ADC-5101	8 Bits	900 ns	±1/2 LSB	0 to -5V, -10V, -20V 0 to +5V, +10V, +20V ±2.5V, ±5V, ±10V	Bin	24-pin DIP Hybrid	0 to +70 -55 to +125	1-61
ADC-5101H								
ADC-825MC	8 Bits	1 µs	±1/2 LSB	0 to +5V, +10V, +20V ±2.5V, ±5V, ±10V	Bin, 2C	24-pin DIP Hybrid	0 to +70 -55 to +125	1-106
ADC-825MM								
ADC-881	8 Bits	1 µs	±0.04 LSB	±5V	Bin	MODULE	0 to +70	1-139
ADC-510MC	10 Bits	425 ns	±1/2 LSB	0 to +10V, +20V ±10V	Bin, CBin	32-pin DIP Hybrid	0 to +70 -55 to +125	1-55
ADC-510MM								
ADC-515MC	10 Bits	650 ns	±1/2 LSB	0 to +10V, +20V ±10V	Bin, CBin	32-pin DIP Hybrid	0 to +70 -55 to +125	1-55
ADC-515MM								
ADC-816MC	10 Bits	800 ns	±1/2 LSB	0 to -10V, -20V ±2.5V, ±5V, ±10V	Bin, 2C	32-pin DIP Hybrid	0 to +70 -55 to +125	1-110
ADC-816MM								
ADC-826MC	10 Bits	1.4 µs	±1/2 LSB	0 to -5V, -10V, -20V ±2.5V, ±5V, ±10V	Bin, 2C	32-pin DIP Hybrid	0 to +70 -55 to +125	1-110
ADC-826MM								
ADC-868	12 Bits	500 ns	±1/2 LSB	0 to +5V ±2.5V	Bin	MODULE	0 to +70	1-135
ADC-500BMC	12 Bits	500 ns	0.0125% FSR ±1/2 LSB	0 to +10V ±10V	Bin Offset Bin C Bin C Offset Bin	32-pin DIP Hybrid	0 to +70	1-43
ADC-500BMM		500 ns					-55 to +125	
ADC-505BMC		550 ns					0 to +70	
ADC-505BMM		550 ns					-55 to +125	
ADC-508BMC		700 ns					0 to +70	1-49
ADC-508BMM		700 ns					-55 to +125	
ADC-520MC	12 Bits	800 ns	±1/2 LSB	0 to +10V, +20V, -20V ±10V 0 to +5V ±2.5	Bin, 2C C Bin, C2C Offset Bin C Offset Bin	32-pin DIP	0 to +70 -55 to +125 0 to +70 -55 to +125	1-71
ADC-520MM								
ADC-521MC								
ADC-521MM								
ADC-511MC	12 Bits	1 µs	±3/4 LSB	0 to +10V ±5V	Bin, CBin Offset Bin	24-pin DIP Hybrid	0 to +70 -55 to +125	1-65
ADC-511MM								
ADC-810MC	12 Bits	2 µs	±1 LSB	0 to +10V, +20V	C Bin C2C	32-pin DIP Hybrid	0 to +70 -55 to +125	1-100
ADC-810MM								
ADC-817AMC	12 Bits	2 µs	±1 LSB	0 to -5V, -10V ±2.5V, ±5V, ±10v	Bin, 2C	32-pin DIP Hybrid	0 to +70 -55 to +125	1-115
ADC-817AMM								
ADC-827AMC	12 Bits	3 µs	±1 LSB	0 to -5V, -10V ±2.5V, ±5V, ±10V	Bin, 2C	32-pin DIP Hybrid	0 to +70 -55 to +125	1-115
ADC-827AMM								
ADC-811MC	12 Bits	3 µs	±1 LSB	0 to +10V, +20V ±5V, ±10V	C Bin, C2C	32-pin DIP Hybrid	0 to +70 -55 to +125	1-100
ADC-811MM								
ADC-800	15 Bits	400 ms	2 LSB	-Vs +1.5V to +Vs-1.5V	Bin	40-pin DIP Monolithic	0 to +70	1-92
ADC-974	16 Bits	2.5 µs	±1/2 LSB @ 14 Bits	±5V	C2C	MODULE	0 to +70	1-143



FLASH A/D CONVERTERS

MODEL	RESOLUTION	CONVERSION TIME (MAX)	LINEARITY (MAX)	INPUT RANGE	OUTPUT CODING	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
ADC-207MC **ADC-207MM**	7 Bits	50 nS	±1/2 LSB	0 to +5V	Bin	18-pin DIP Monolithic	0 to +70 -55 to +125	1-5
ADC-303	8 Bits	10 nS	±1/2 LSB	0 to -2V	Bin, C Bin C2C, 2C	42-pin DIP Monolithic	-20 to +100	1-27
ADC-302	8 Bits	20 nS	±1/2 LSB	0 to -2V	Bin, C Bin C2C, 2C	28-pin DIP Monolithic	-20 to +100	1-23
ADC-301	8 Bits	33 nS	±1/2 LSB	0 to -2V	Bin, C Bin C2C, 2C	28-pin DIP Monolithic	-20 to +100	1-23
ADC-300	8 Bits	50 nS	±1/2 LSB	0 to -2V	Bin, C Bin C2C, 2C	28-pin DIP Monolithic	-20 to +100	1-19
ADC-304	8 Bits	50 nS	±1/2 LSB	0 to -2V	Bin, C Bin C2C, 2C	28-pin DIP Monolithic	-20 to +100	1-33
ADC-208MC **ADC-208MM**	8 Bits	50 nS	±0.6 LSB	0 to +5V	Bin	24-pin DIP Monolithic	0 to +70 -55 to +125	1-11
ADC-310	10 Bits	50 nS	±1.75 LSB	0 to -2V	C Bin	28-pin DIP Monolithic	-20 to +75	1-39



SAMPLING A/D CONVERTERS

MODEL	RESOLUTION	THROUGHPUT	LINEARITY (MAX)	INPUT RANGE	OUTPUT CODING	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
ADS-115MC **ADS-115MM**	10 Bits	1 MHz	±1/2 LSB	0 to +10V	Bin, CBin	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-229
ADS-116MC **ADS-116MM**	10 Bits	1 MHz	±1/2 LSB	-10 to + 10V	Off. Bin C Off. Bin	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-229
ADS-21	12 Bits	1.3 MHz	±0.0125% FSR ±1/2 LSB	0 to +10V 0 to -5V, -10V, -20V ±5V, ±10V	Bin, C Bin Off. Bin C Off. Bin	46 - pin DIP Module	0 to +70	1-241
ADS-22	12 Bits	1 MHz	±0.0125% FSR ±1/2 LSB	0 to +10V 0 to -5V, -10V, -20V ±5V, ±10V	Bin, C Bin Off. Bin C Off. Bin	46 - pin DIP Module	0 to +70	1-247
ADS-105MC **ADS-105MM**	12 Bits	1 MHz	±0.0125% FSR ±1/2 LSB	0 to +10V	Bin, C Bin	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-217
ADS-106MC **ADS-106MM**	12 Bits	1 MHz	±0.0125% FSR ±1/2 LSB	±10V	Off. Bin C Off. Bin	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-217
ADS-125MC **ADS-125MM**	12 Bits	700 kHz	±1/2 LSB	0 to +10V ±10V	Bin, C Bin, Off. Bin C Off. Bin, 2C, C2C	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-235
ADS-126MC **ADS-126MM**	12 Bits	700 kHz	±1/2 LSB	0 to +5V ±2.5V	Bin, C Bin, Off. Bin C Off. Bin, 2C, C2C	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-235
ADS-111MC **ADS-111MM**	12 Bits	500 kHz	±3/4 LSB	0 to +10V ±5V	Bin, C Bin Off. Bin, C Off. Bin	24 - pin DIP Hybrid	0 to +70 -55 to +125	1-223
ADC-HS12BMC **ADC-HS12BMM**	12 Bits	66 kHz	±1/2 LSB	0 to +5V, +10V ±2.5V, ±5V, ±10V	C Bin, C2C	32 - pin DIP Hybrid	0 to +70 -55 to +125	1-209
ADC-674ZA **ADC-674ZB** **ADC-674ZC**	12 Bits	55 kHz	±1 LSB ±1/2 LSB	0 to +10V, +20V ±5V, ±10V	Bin Off. Bin	28 - pin DIP Monolithic	0 to +70 -55 to +125	1-253
ADC-574ZA **ADC-574ZB** **ADC-574ZC**	12 Bits	35 kHz	±1 LSB ±1/2 LSB ±1/2 LSB	0 to +10V, +20V ±5V, ±10V	Bin Off. Bin	28 - pin DIP Monolithic	0 to +70	1-253
ADC-B207/208	7/8 Bits	20 MHz	±0.6 LSB	0 to +5V	Bin	6.3 X 4 in. (160 X 102 mm)	0 to +70	—
ADC-B303E	8 Bits	100 MHz	±1/2 LSB	0 to +1V ±0.5V	Bin, C Bin, Off. Bin C Off Bin, 2C, C2C	Eurocard size Pin connector	0 to +70	1-157
ADC-B302E	8 Bits	50 MHz	±1/2 LSB	0 to +1V ±0.5V	Bin, C2C Off. Bin, 2C	Eurocard size Pin connector	0 to +70	1-152
ADC-B301E	8 Bits	30 MHz	±1/2 LSB	0 to +1V ±0.5V	Bin, C2C Off. Bin, 2C	Eurocard size Pin connector	0 to +70	1-147
ADC-B304E	8 Bits	20 MHz	±1/2 LSB	0 to 1V ±0.5V	Bin, C Bin, Off. Bin C Off. Bin, 2C, C2C	Eurocard size Pin connector	0 to +70	1-163
ADC-B10E	10 Bits	12 MHz	±1.75 LSB	0 to 1V ±0.5V	Bin Off Bin	Eurocard size Pin connector	0 to +70	1-169
ADC-B500 * **ADC-B500-1**	12 Bits	1.25 MHz	±0.0125% FSR ±1/2 LSB	0 to -5V, -10V 0 to -20V, +10V ±5V, ±10V	Bin, C Bin Off. Bin, C Off. Bin	3.8 X 4.5 in (97 X 114 mm) Board	0 to +70	1-175
ADC-B505	12 Bits	1.1 MHz	±0.0125% FSR ±1/2 LSB	0 to -5V, -10V 0 to -20V, +10V ±5V, ±10V	Bin, C Bin Off. Bin, C Off. Bin	3.8 X 4.5 (97 X 114 mm) Board	0 to +70	1-175

* Includes **ADC-500** and **SHM-45**

ADC-207
VIDEO FLASH CONVERTER

FEATURES

- **7 Bit Flash A/D Converter**
- **35 MHz Sampling Rate**
- **Low Power (250 mw)**
- **+5V dc Operation**
- **1.2 micron CMOS**
- **7-Bit Latched 3-state Output With Overflow Bit**

APPLICATIONS

- **TV video digitizing**
- **Radar**
- **High-speed digital oscilloscopes**
- **Medical imaging (ultrasound)**
- **Robotic vision**
- **High-Speed, low power applications**

GENERAL DESCRIPTION

The ADC-207 is the industry's first 7-bit flash converter using a high-speed 1.2 micron CMOS process. This process offers some very distinctive advantages over other processes, making the ADC-207 a very unique device. The smaller geometrics of the process achieves high-speed, better linearity and better temperature performance. Since the ADC-207 is a CMOS device, it also has very low power consumption (250 mw). The device draws power from a single +5V supply, and is conservatively rated for 20 MHz operation. The ADC-207 allows using sampling apertures as small as 12nS, making it more closely approach an ideal sampler. The small sampling apertures also let the device operate at greater than 20 MHz.

The ADC-207 has 128 comparators which are auto-balanced on every conversion so as to cancel out any offsets due to temperature and/or dynamic effects. The resistor ladder has a midpoint tap for use with an external voltage source to improve integral linearity beyond 7 bits. The ADC-207 also provides the user with 3-state outputs for easy interfacing to other components. There are two models of the ADC-207 covering two operating temperature ranges, 0 to 70 degrees C and −55 to +125 degrees C. For MIL-Std-883C versions, consult factory.

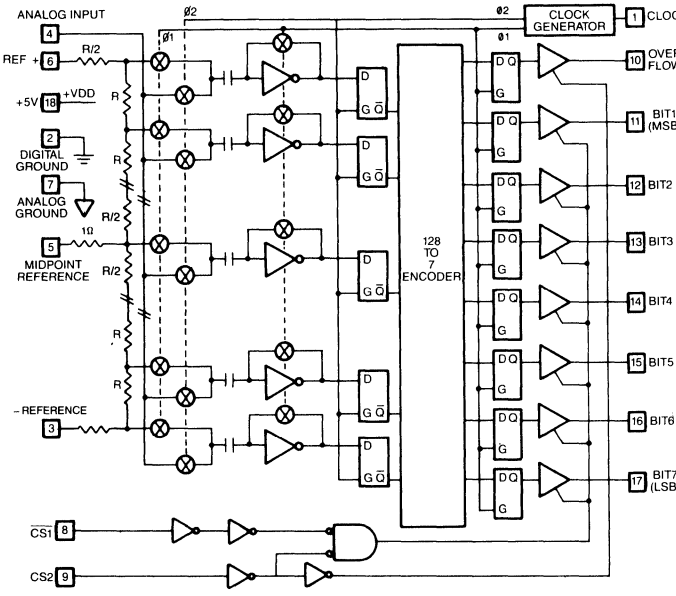
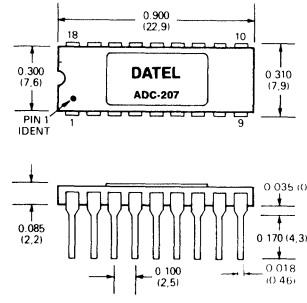


Figure 1. ADC-207 Simplified Block Diagram

MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK	10	OVERFLOW
2	DIGITAL GROUND	11	BIT 1 (MSB)
3	- REFERENCE	12	BIT 2
4	ANALOG INPUT	13	BIT 3
5	MID POINT	14	BIT 4
6	+ REFERENCE	15	BIT 5
7	ANALOG GROUND	16	BIT 6
8	CHIP SELECT 1	17	BIT 7 (LSB)
9	CHIP SELECT 2	18	+VDD SUPPLY

FUNCTIONAL SPECIFICATIONS

(Typical at +5Vdc power, +25 deg. C, 20 MHz clock, +Reference = 5V, −Reference = Ground, unless noted)

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
ABSOLUTE MAXIMUM RATINGS				
Power supply voltage (+Vdd, pin 18)	−0.5	—	+7.0	V dc
Digital inputs	−0.5	—	+5.5	V dc
Analog input	−0.5	—	+Vdd +0.5	V dc
Reference inputs	−0.5	—	+Vdd	V dc
Digital outputs (short circuit protected to ground)	−0.5	—	+5.5	V dc
Lead temperature, 10 sec. ma	—	—	+300	°C
Ambient temperature	−65	—	+150	°C
INPUTS				
ANALOG SIGNAL INPUT single-ended, non-isolated				
Input range dc-20 MHz	0	—	+5.0	V
Input impedance	—	1000	—	Ohms
Input capacitance, full input range	—	10	—	pF
DIGITAL INPUTS:				
Logic "1" level	2.0	—	—	V
Logic "0" level	—	—	0.8	V
Logic "1" loading	—	+/−1	+/−5	microamps
Logic "0" loading	—	+/−1	+/−5	microamps
Sample pulse width, during sampling portion of clock	12	—	—	nS
Reference ladder resistance	—	330	—	Ohms
DIGITAL OUTPUTS				
Data coding		Straight binary		
Data output resolution	7	—	—	
Logic "1" level	2.4	4.5	—	V
Logic "0" level at 1.6 mA	—	—	0.4	V
Logic "1" loading	4	—	—	mA
Logic "0" loading	4	—	—	mA
Output data valid delay from rising edge	—	15	17	nS
PERFORMANCE				
Conversion rate[1]	20	35	—	mega samples/sec
Harmonic distortion[2] (8 MHz 2nd order harmonic)	—	−40	—	dB
Differential gain[3]	—	3	—	%
Differential phase[3]	—	1.5	—	degrees
Aperture delay	—	8	—	nS
Aperture jitter	—	50	—	pS
No missing codes				
MC grade	0	—	+70	°C
MM grade	−55	—	+125	°C
Integral linearity at 25°C	—	+/−0.8	+/−1	LSB
Adjustable over temp. range	—	+/−1.0	—	LSB
Differential nonlinearity at 25°C	—	+/−0.3	+/−0.5	LSB
Over temp. range	—	+/−0.4	+/−0.6	LSB
Power supply rejection	—	0.02	—	%FSR/%Vs

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
POWER REQUIREMENTS				
Power supply range (+Vdd)	+3.0	+5.0	+5.5	V dc
Power supply current	—	+50	+70	mA
Power dissipation	—	250	385	mW
ENVIRONMENTAL — MECHANICAL				
Operating temp. range:				
MC grade	0	—	+70	°C
MM grade	−55	—	+125	°C
Storage temp. range	−65	—	+150	°C
Package type	hermetically sealed, ceramic dual inline package			
Pins	18 pins, 0.100" centers, 0.300"between rows			
Pin material	.010 x .018 inch Kovar			

NOTES: 1. At full power input and chip selects enabled

2. At 4 MHz input and 20 MHz clock

3. For 10-step, 40 IRE NTSC ramp test

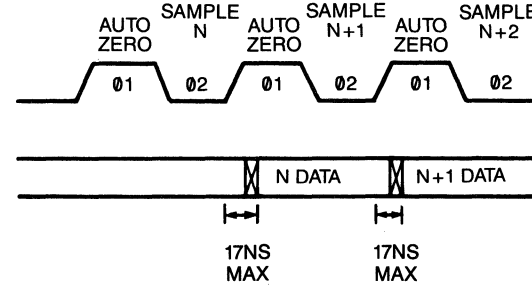
TECHNICAL NOTES

1. Input Buffer Amplifier—Since the ADC-207 has a switched capacitor type input, the input impedance of the 207 is dependent on the clock frequency. At relatively slow conversion rates a general purpose type input buffer can be used; at high coversion rates DATEL recommends either the HA-5033, the LH-0033 or Elantec 2003.
2. Reference Ladder—Adjusting the voltage at +Ref adjusts the gain of the ADC-207. Adjusting the voltage at −Ref adjusts the offset or zero of the ADC-207. The midpoint pin is usually bypassed to ground through a .1uf capacitor, although it can be tied to a precision voltage halfway between +Ref and -Ref. This would improve integral linearity beyond 7 bits.
3. Clock Pulse Width—To improve performance at Nyguist bandwidths, the clock duty cycle can be adjusted so that the low portion of the clock pulse is 12 nseconds wide. The smaller aperature allows the ADC-207 to closely resemble an ideal sampler.

CAUTION

Since the ADC-207 is a CMOS device, normal precautions against static electricity should be taken. use ground straps, grounded mats, etc. The Absolute Maximum Ratings of the device MUST NOT BE EXCEEDED as irrevocable damage to the ADC-207 will occur.

TIMING DIAGRAM



DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

OUTPUT CODING

(+Ref=+5.12V, −Ref=Gnd, MID POINT=no connection)

NOTE: The reference should be held to 0.1% accuracy or better. Do not use the +5V power supply as a reference input without precision regulation and high frequency decoupling.

Values shown here are for a 5.12Vdc reference. Scale other references proportionally. Calibration equipment should test for code changes at the midpoints between these center values shown in Table 1. For example, at the half-scale major carry, set the input to 2.54V and adjust the reference until the code flickers equally between 63 and 64. Note also that the weighting for the comparator resistor network leaves the first and last thresholds to within ½ LSB of the end points to adjust the code transition to the proper midpoint values.

Table 1. ADC-207 Output Coding

Analog In (Center Value)	Code	Overflow	1 MSB	2 D	3 A	4 T	5 A	6	7 LSB	Decimal	Hexadecimal (incl. 0V)
0.00V	Zero	0	0	0	0	0	0	0	0	0	00
+0.04V	+1 LSB	0	0	0	0	0	0	0	1	1	01
+1.28V	+1/4 FS	0	0	1	0	0	0	0	0	32	20
+2.52V	+1/2FS−1 LSB	0	0	1	1	1	1	1	1	63	3F
+2.56V	+1/2FS	0	1	0	0	0	0	0	0	64	40
+2.60V	+1/2FS +1 LSB	0	1	0	0	0	0	0	1	65	41
+3.84V	+3/4FS	0	1	1	0	0	0	0	0	96	60
+5.08V	+FS	0	1	1	1	1	1	1	1	127	7F
+5.12V	Overflow	1	1	1	1	1	1	1	1	255*	FF

* — Note that the overflow code does not clear the data bits.

THEORY OF OPERATION

The ADC-207 uses a switched capacitor scheme in which there is an auto-zero phase and a sampling phase. (Figure 1 shows the simplified block diagram of the ADC-207.) The ADC-207 uses a single clock input. When the clock is at a high state (logic 1), the ADC-207 is in the auto-zero phase (Ø1). When the clock is at a low state (logic 0), the ADC-207 is in the sampling phase (Ø2). During phase 1, the 128 comparator outputs are shorted to their inputs through CMOS switches. This serves the purpose of bringing the inputs and outputs to the transition levels of the respective comparators. The inputs to the comparators are also connected to 128 sampling capacitors. The other end of the 128 capacitors are also shorted to 128 taps of a resistor ladder, via CMOS switches. Therefore during phase 1 the sampling capacitors are charged to the differential voltage between a resistor tap and its respective comparator transition voltage.

This eliminates offset differences between comparators and yields better temperature performance. During phase 2 (Ø2) the input voltage is applied to the 128 capacitors, via CMOS switches. This forces the comparators to trip either high or low. Since the comparators during phase 1 were sitting at their transition point, they can trip very quickly to the correct state. Also during phase 2 the outputs of the comparators are loaded into internal latches which in turn feed a 128 to 7 encoder. When going back into phase 1 the output of the encoder is loaded into an output latch. This latch then feeds the 3-state output buffer.

This means that the ADC-207 is of pipeline design. To do a single conversion, the ADC-207 requires a positive pulse followed by a negative pulse followed by a positive pulse. Continuous conversion requires one cycle/sample (one positive pulse and one negative pulse). The 3-state buffer has two enable lines, CS1 and CS2. Table 2 shows the truth table for chip select signals. CS1 has the function of enabling/disabling bits 1 through 7. CS2 has the function of enabling/disabling Bits 1 through 7 and the overflow bit. Also a full-scale input produces all ones, including the overflow bit at the output. The ADC-207 has an adjustable resistor ladder string. The top end, middle point, and bottom end are brought out for use with applications circuits.

These pins are called +Ref, MID POINT, and −Ref, respectively. In typical operation +Ref is tied to +5V, −Ref is tied to ground, and MID POINT is bypassed to ground. Such a configuration results in a 0 to 5V dc input voltage range. The MID POINT pin can also be tied to a 2.5V source to further improve integral linearity. This is usually not necessary unless better than 7 bit linearity is needed.

Table 2. Chip Select Truth Table

$\overline{CS1}$	CS2	Bits 1-7	Overflow Bit
0	0	3 State Mode	3 State Mode
1	0	3 State Mode	3 State Mode
0	1	DATA Outputed	DATA Outputed
1	1	3 State Mode	DATA Outputed

APPLICATION #1: Using the ADC-207

Figure 2 shows typical connections for using the ADC-207. In this configuration the input voltage range is 0 to 5V dc. The input voltage range is determined by the reference voltage. For operating in lower input voltage ranges, the reference input must be tied to the corresponding lower voltage value. For example to operate the ADC-207 in 0 to 3V input voltage range the +REF input must be tied to +3V dc. Further, for higher speed operation (above 20 MHz) user may modify the clock signal to facilitate duty cycle adjustment. Figure 3 shows a pulse shaping circuit which is usable to modify the clock signal.

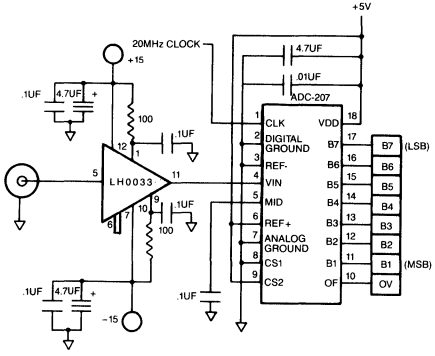
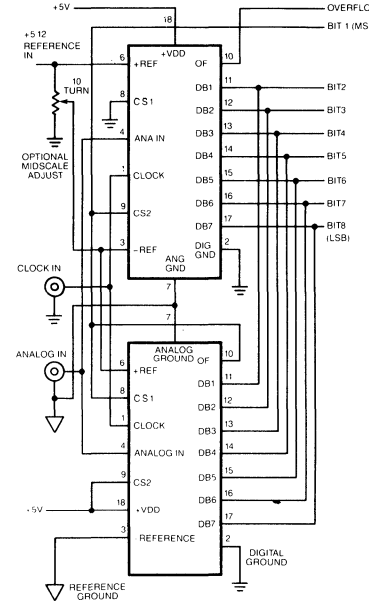


Figure 2. Typical Connections for Using the ADC-207

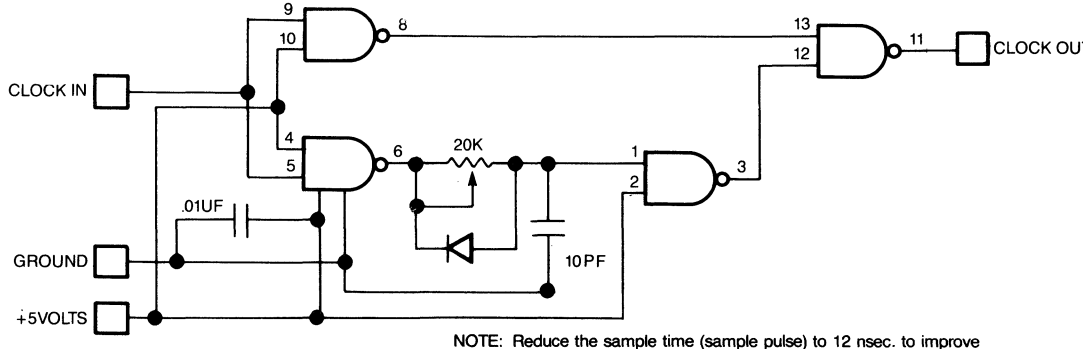
APPLICATION #2: Using Two ADC-207's for 8-bit resolution.

Two ADC-207's (A and B) are cascadable for applications requiring 8-bit resolution. The device A provides a typical 7-bit output. The OVERFLOW signal of device A turns off device A and turns on the device B. The OVERFLOW signal of device A is also used as MSB for 8-bit operation. The device B provides the other seven bits from the input signal. Figure 4 shows the circuit connections for the application.



Note: The output data bit numbering is offset by a bit to the device B's output.

Figure 4. Using ADC-207's for 8-bit Operations



NOTE: Reduce the sample time (sample pulse) to 12 nsec. to improve performance above 20 MHz. Such a configuration will closely resemble an ideal sampler.

Figure 3. Optional Pulse Shaping Circuit

APPLICATION #3: Beat Frequency And Envelope Tests

Figure 5 shows the actual plot of the Beat Frequency Test. This test uses a 20 MHz clock input to the ADC-207 with a 20.002 MHz full-scale sine wave input. Although the converter would not normally be used in this mode because the input frequency violates Nyquist criteria for full recovery of signal information, the test is an excellent demonstration of the ADC-207's high-frequency performance.

The effect of the 2 KHz frequency difference between the input and the clock is that the output will be a 2 KHz sinusoidal digital data array which "walks" along the acutal input at the 2 KHz beat note frequency. Any inability to follow the 20.002 MHz input will be immediately obvious by plotting the digital data array. Further arithmetic analysis may be done on the data array to determine spectral purity, harmonic distortion, etc. This test is an excellent indication of:

1. Full power input bandwidth of all 128 comparators. (Any gain loss would show as signal distortion.)
2. Phase response linearity vs. instantaneous signal magnitude. (Phase problems would show as improper codes.)
3. Comparator slew rate limiting.

Envelope Test:

Figure 6 shows the actual plot of the Envelope Test. This test is a variation of the previous test but uses a 10.002 MHz sine input to give two overlapping cycles when the data is reconstructed by a D/A converter output to an oscilloscope. The scope is triggered by the 20 MHz clock used by the A/D. Any assymmetry between positive and negative portions of the signal will be very obvious. This test is an excellent indication of slew rate capability. At the peaks of the Envelope, consecutive samples swing completely through the input voltage range.

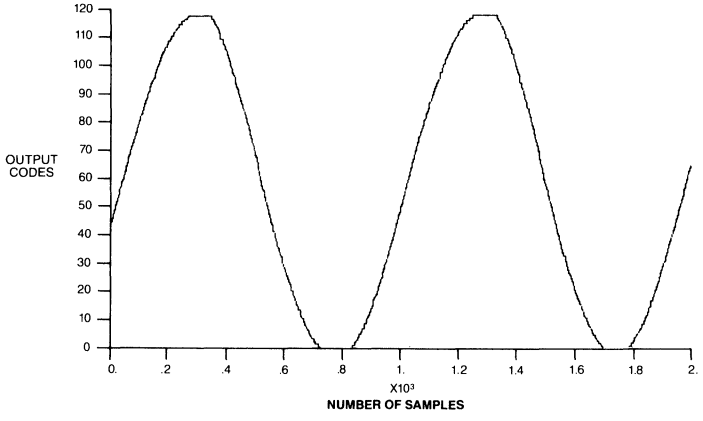


Figure 5. Beat Frequency Test at 20 MHz

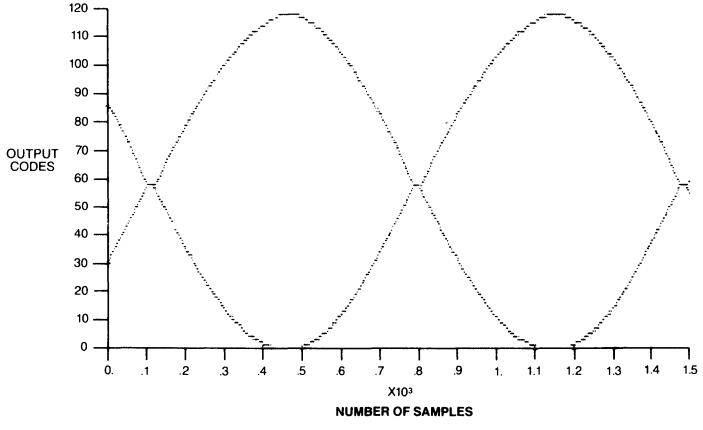


Figure 6. 10 MHz Envelope Test

APPLICATION #4: FFT Test

This test actually produces an amplitude versus frequency graph (Figure 7) which indicates harmonic distortion and signal to noise ratio. The theorectical RMS signal-to-noise ratio for a 7-bit converter is +43.8 dB.

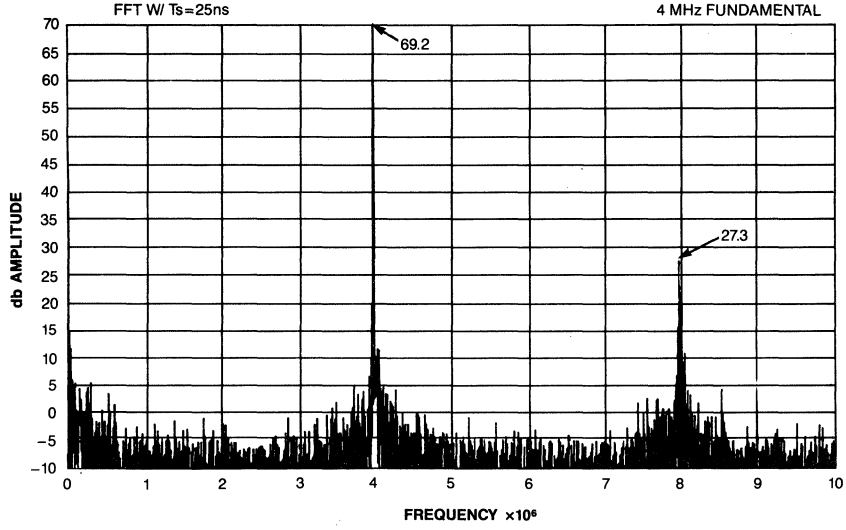


Figure 7. FFT Test Using the ADC-207

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SEAL
ADC-207MC	0 to +70°C	Hermetic
ADC-207MM	−55 to 125°C	Hermetic

For military devices compliant with MIL-STD-883, contact DATEL.

ADC-208
8-BIT, 20 MSPS CMOS FLASH A/D

FEATURES

- **8-Bit Flash A/D Converter**
- **20 MHz Sampling Rate**
- **10 MHz Full Power Bandwidth**
- **Sample-Hold not required**
- **Low Power CMOS**
- **+5V dc Operation**
- **1.2 micron CMOS**
- **8-Bit Latched Three-State Outputs With Overflow Bit**
- **Surface Mount versions**
- **MIL-STD-883B versions**

APPLICATIONS

- **Video digitizing**
- **Radar**
- **High-speed digital oscilloscopes**
- **Medical imaging**
- **Robotic vision**
- **High-speed, low power applications**

GENERAL DESCRIPTION

The ADC-208 utilizes an advanced VLSI 1.2 micron CMOS in providing 20 MHz sampling rates at 8-bits. The flexibility of the design architecture and process delivers effective bit rates to 30 MHz in the burst mode, one shot mode conversion times of 35 nanoseconds, low power modes to 150 mW, latch-up free operation without external components and operation over the full military temperature range.

The ADC-208 has 256 auto-zeroing comparators which are auto-balanced on every conversion to cancel out any offsets due to temperature and/or dynamic effects. These comparators sample the difference between the analog input and the reference voltages generated by the precision reference ladder network. Parallel output data and the overflow pin have Three-State outputs. The overflow pin allows cascading two devices for 9-bit operation.

The ADC-208 has no missing codes over the full operating temperature range of -55°C to +125°C. Operation is from a single +5V dc power supply.

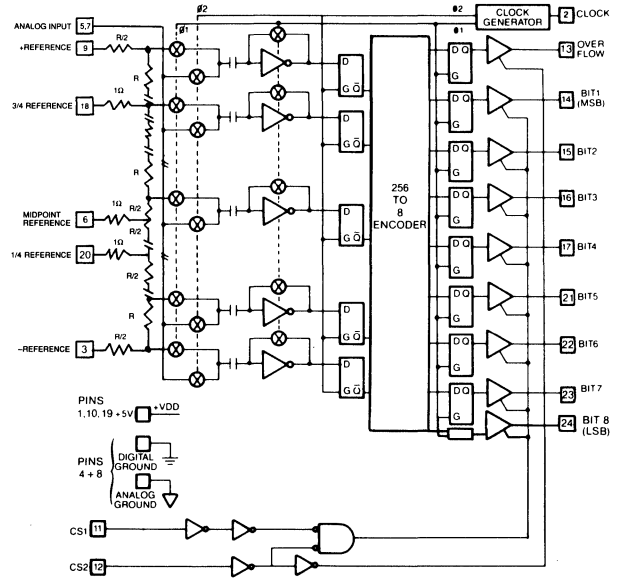
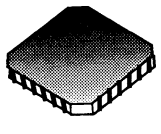
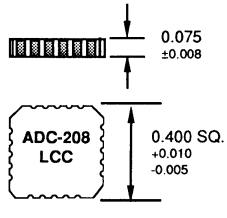


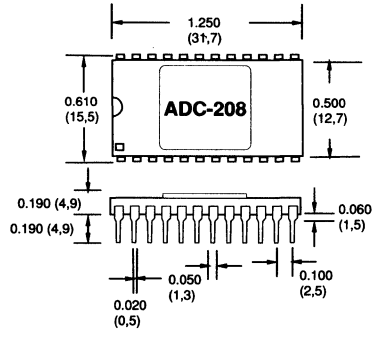
Figure 1. ADC-208 Simplified Block Diagram

ADC-208 LCC





ADC-208 DIP



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	V_{DD}
2	CLOCK
3	– REFERENCE
4	ANA/DIG GND (VSS)
5	ANALOG INPUT
6	REFERENCE MID-POINT
7	ANALOG INPUT
8	ANA/DIG GND (VSS)
9	+ REFERENCE
10	V_{DD}
11	$\overline{CS1}$ (OUTPUT ENABLE)
12	CS2 (OVERFLOW ENABLE)
13	OVERFLOW BIT
14	BIT 1 (MSB)
15	BIT 2
16.	BIT 3
17	BIT 4
18	REF 3/4 FS
19	V_{DD}
20	REF 1/4 FS
21	BIT 5
22	BIT 6
23	BIT 7
24	BIT 8 (LSB)

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	LIMITS	UNITS
Power Supply Voltage (V_{DD} Pin 1,10,19)	-0.5 to +7.0	V dc
Digital Inputs	-0.5 to +5.5	V dc
Analog Input	-0.5 to +V_{DD} +0.5	V dc
Reference Inputs	-0.5 to +V_{DD} +0.5	V dc
Digital Outputs (short circuit protected to ground)	-0.5 to +5.5	V dc
Lead Temperature(10 sec)	+300 max.	°C
Storage Temperature	-65 to +150	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified (15 MHz clock, +Reference = +5V, –Reference = Ground, unless otherwise noted).

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Single-Ended,Non-Isolated Input Range dc-20 MHz	0	–	+5.0	V
Analog Input Capacitance				
(static - Pin 5 to Pin 7)①	–	10	–	pF
(dynamic- Pin 5 to Pin 7)	–	64	–	pF
Ref. Ladder Resistance	–	300	–	Ohms
Ref. input (Note 5)	-0.5	–	V_{DD} +0.5	V dc
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	+1	+5	µA
Logic 0	–	+1	+5	µA
Clock Low Pulse Width	15	25	–	nSec.
DIGITAL OUTPUTS				
Logic Levels				
Logic 1	–	4.5	5.0	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	4	–	–	mA
Logic 0	4	–	–	mA
Output Data Valid Delay from Rising Edge	5	10	15	nSec.
Coding	Straight Binary			
Resolution	8 Bits			
PERFORMANCE				
Sampling Rate.②	15	20	–	MSPS
Full Power Bandwidth	10	–	–	MHz
Diff. Linearity at +25 °C (See Tech, Note 7)				
Code Transitions	–	±0.5	±0.75	LSB
Center of Codes	–	±0.25	–	LSB
Diff. Lin. Over Temp.				
Code Transitions	–	±0.5	±1.0	LSB
Center of Codes	–	±0.25	–	LSB

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Int. Lin. at +25 °C (See Tech. Note 7) (Ref. adjusted)				
End-point	–	–	±1/2	LSB
Best-fit Line	–	–	±1/2	LSB
Int. Lin. Over Temp. (Ref. adjusted)				
Best-fit Line	–	±1/2	±1	LSB
Int. Lin. at +25 °C (Ref. unadjusted)				
End-point	–	±2	±2.5	LSB
Best-fit Line	–	±1.6	±1.9	LSB
Int. Lin. Over Temp. (Ref. unadjusted)				
End-point	–	±2.3	±2.6	LSB
Best-fit Line	–	1.8	±2.0	LSB
Zero-Scale Offset (Code "0" to "1" Transition)	–	1	3	LSB
Gain Error	–	–	±1	LSB
Differential Gain③	–	2	–	%
Differential Phase③	–	1.1	–	degree
Aperture Delay	–	8	–	nSec.
Aperture Jitter	–	50	–	pSec.
Harmonic Distortion (8 MHz 2nd Order Harm.)	-40	-46	–	dB
Ref.Bandwidth (See Tech. Note 5)	–	10	–	MHz
Power Supply Rej.	–	–	0.02	%FSR/%/Vs
No Missing Codes	Over the operating temperature range			
POWER REQUIREMENTS				
Pwr. Supply Range (+V_{DD})	+3.5	+5.0	+5.5	V dc
Power Supply Current	–	+100	+130	mA
Power Dissipation	–	500	715	mW
PHYSICAL-ENVIRONMENTAL				
Oper. Temp. Range				
MC/LC Grade	0	–	+70	°C
MM/LM/883B	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Types				
(DIP)	24-pin hermetic sealed, ceramic DIP			
(LCC)	24-pin hermetic sealed, ceramic LCC			
Pins (DIP)	0.01 x 0.018 inch Kovar			

NOTES:
① Maximum input impedance is a function of clock frequency. See Technical Note 4.
② At full power input and chip selects enabled.
③ For 10-step, 40 IRE NTSC ramp test.

TECHNICAL NOTES

1. Tie all V_{DD} pins (1,10, & 19) together.

2. Tie both Analog Input pins (5 & 7) together.

3. Connect both ANA/DIG GNDs (Vss pins 4 & 8) to one point, the ground plane beneath the converter.

4. Input Buffer Amplifier - Since the ADC-208 has a switched-capacitor type input, the input impedance of the ADC-208 is dependent on the clock frequency. At relatively slow conversion rates, a general purpose type input buffer can be used; at high conversion rates DATEL recommends the National LH-0033 , the Elantec EL-2003, or the Harris HA-5002.

Table 1. ADC-208 Output Coding

ANALOG INPUT	CODE	OVER FLOW	DATA 1234	BITS 5678	DECIMAL	HEX
0.00 V	Zero	0	0000	0000	0	00
+0.02 V	+1 LSB	0	0000	0001	1	01
+1.28 V	+1/4 FS	0	0100	0000	64	40
+2.54 V	+1/2 FS-1 LSB	0	0111	1111	127	7F
+2.56 V	+1/2 FS	0	1000	0000	128	80
+2.58 V	+1/2 FS+1 LSB	0	1000	0001	129	81
+3.84 V	+3/4 FS	0	1100	0000	192	C0
+5.10 V	+FS	0	1111	1111	255	FF
+5.12 V	Overflow	1	1111	1111	511*	1FF

* Note the overflow code does not clear the data bits.
Values shown here are for a +5.12Vdc reference. Scale other references proportionally.
(+REF = +5.12V, -REF = GND, 1/4,1/2, and 3/4 Reference FS = No Connection)

5. The Reference ladder is floating with respect to V_{DD} and may be referenced anywhere within the specified limits. AC modulation of the reference voltage may also be utilized; contact DATEL for further information.

6. Clock Pulse Width - To improve performance when input signals may exceed Nyquist bandwidths, the clock duty cycle can be adjusted so that the low portion (sample mode) of the clock pulse is 15 nanoseconds wide. Reducing the sampling time period minimizes the amount the input voltage slews and prevents the comparators from saturating.

7. DATEL uses the conservative definitions when specifying Integral Linearity (end-point) and Differential Linearity (code transition). The specifications using the less conservative definition have also been provided as a comparative specification for products specified this way.

8. The process that is used to fabricate the ADC-208 eliminates the latchup phenomena that has plagued CMOS devices in the past. The ADC-208 does not require external protection diodes.

CAUTION

Since the ADC-208 is a CMOS device, normal precautions against static electricity should be taken. Ground straps, grounded mats, etc. should be employed when handling this device. Also, the Absolute Maximum Ratings of the device MUST NOT BE EXCEEDED as irrevocable damage to the ADC-208 will occur.

CALIBRATION PROCEDURE

1. Connect the converter appropriately per the typical connection circuits shown in Figure 2 or Figure 3. Then apply an appropriate clock input. The ADC-208's reference input should be held to ±0.1% accuracy or better. Do not use the +5V power supply as a reference without precision regulation and high frequency decoupling capacitors.

2. Zero Adjustment
Apply a precision voltage reference source between the analog input (pins 5 & 7) and ground. Adjust the output of the reference source per Table 1 for the Unipolar Zero adjustment (+ 1/2 LSB). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 and 0000 0001. Ground -REFERENCE (pin 3) for operation without adjustment.

3. Full Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 1 for the Unipolar Gain Adjustment (+FS - 1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1110 and 1111 1111. The + REFERENCE (pin 9) should be tied directly to a +5V reference for operation without adjustment.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 1.

5. Integral Nonlinearity Adjustments
Provision is made for optional adjustment of Integral Nonlinearity through access of the reference's 1/4, 1/2 & 3/4 Full Scale points. For example, at the half-scale major carry, set the input to 2.55V and adjust the reference until the code flickers equally between 127 and 128 for a 5.12V Full Scale input.

Figure 3 shows a typical circuit with reference adjustment circuitry. Figure 2 shows a typical circuit where zero, gain and Integral Nonlinearity adjustments are not used. Reference adjust pins not being utilized should be decoupled to ground with a 0.1 µF ceramic capacitor.

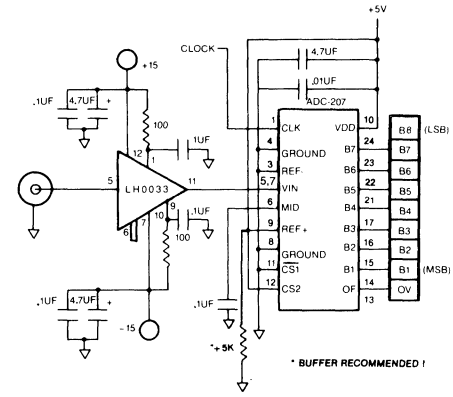


Figure 2. ADC-208 Typical Connections (Adjustment-free)

Table 2. Chip Select Truth Table

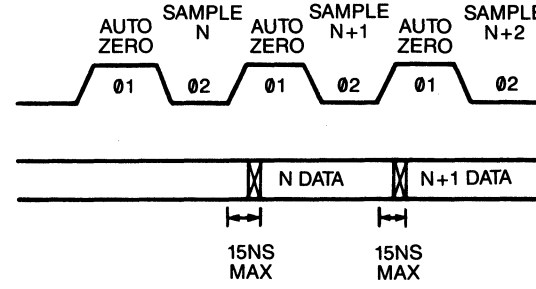
$\overline{CS1}$	CS2	BITS 1-8	OVERFLOW BIT
0	0	Three-State Mode	Three-State Mode
1	0	Three-State Mode	Three-State Mode
0	1	DATA Outputted	DATA Outputted
1	1	Three-State Mode	DATA Outputted

THEORY OF OPERATION

The ADC-208 uses a switched capacitor scheme in which there is an auto-zero phase and a sampling phase (Figure 1 shows the simplified block diagram of the ADC-208).

Inputs

The ADC-208 has an adjustable resistor ladder string. The top end (+ REFERENCE), three quarters (REF 3/4 FS), mid-point (REFERENCE MID-POINT), quarter (REF 1/4 FS) and bottom end (- REFERENCE) are available to the user. In a typical operation, +REFERENCE is tied to +5V, -REFERENCE is tied to ground and REFERENCE taps are by-passed to ground with 0.1 mF capacitors. Since this configuration results in a 0 to +5V dc input voltage range, the MID POINT pin can be tied to a +2.5V source, the REF 3/4 FS tied to +3.75V, and the REF 1/4 FS to +1.25V to further improve integral linearity.



Timing Diagram

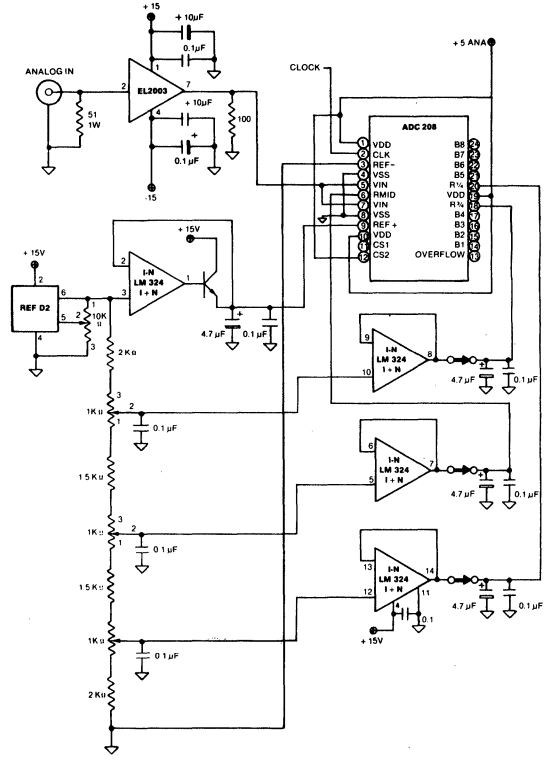


Figure 3. ADC-208 Typical Connections (with Reference Adjustments)

Auto-zero Phase

The auto-zero phase occurs when the clock input is high (logic "1"). During the auto-zero phase, the 256 comparator outputs are shorted to their inputs through CMOS switches. This serves the purpose of bringing the inputs and outputs to the transition levels of the respective comparators.

The input to the comparators are also connected to 256 sampling capacitors. The other end of the 256 sampling capacitors are shorted to 256 taps of the reference resistor ladder, via one set of CMOS switches. Therefore, during the auto-zero phase, the sampling capacitors are charged to the differential voltage between the reference resistor tap and its respective comparator transition voltage. This eliminates offset differences between comparators and yields better temperature performance.

Sampling Phase

The sampling phase occurs when the clock is at a low state (logic "0"). During the sampling phase, the sampling capacitors are switched from being connected to the reference ladder's taps to the analog input. The switches shorting the comparator's input to output are now opened also. The comparators, which were at their transition point, now set to a "1" or "0" state dependent upon if the analog input was greater

than the reference ladder's voltage. During the sampling phase, the comparator's outputs are loaded into internal latches which are the inputs for a 256 to 8 encoder.

Data Output

The ADC-208 has a "pipeline" architecture. Upon completion of one clock cycle of the auto-zero and sampling phases, output data from this conversion is not available until the clock is brought high again for the next conversion's auto-zero stage. At this time, the output of the encoder is loaded into the output latch. To do a single conversion, the ADC-208 requires a positive pulse followed by a negative pulse followed by a positive pulse. Continuous conversion yields one cycle/sample (one positive pulse and one negative pulse).

The parallel output data and Overflow pin become available at the three-state buffer output when enabled. A full-scale input produces all "1"s on the data outputs. The OVERFLOW pin goes "high" when the analog input level exceeds + REF minus 1/2 LSB. Table 2 shows the truth table for the chip select enable signals.

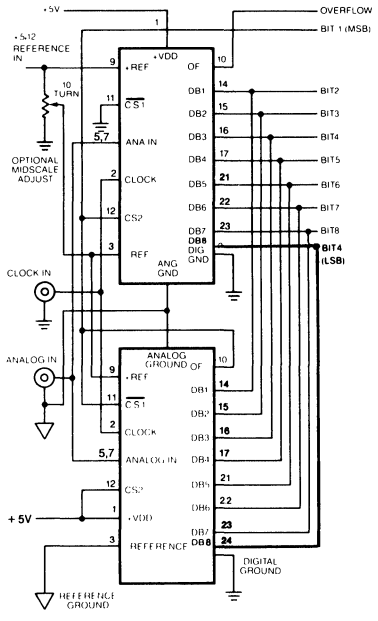


Figure 4. Obtaining 9-Bit Resolution Using Two ADC-208's

Two ADC-208's (A and B) are cascadable for applications requiring 9-bit resolution (see Figure 4). Bit 1 (MSB) of the 9-bit device is derived from the overflow pin of device A. Bits 2 through Bit 9 (LSB) are taken from the 8-bits of parallel output data of either device A or device B. Bits 1-8 of the ADC-208s are connected in parallel to become bits 2 through Bit 9.

The - REFERENCE of device B is connected to the + REFERENCE of device A. For inputs below 1/2 Full Scale, device A does not give an OVERFLOW flag and the parallel output data of device B is in a three-state mode. Device A provides the lower 8-bits. For inputs above 1/2 Full Scale, device A gives an OVERFLOW flag, disabling device A's parallel output and enabling device B's parallel output.

BEAT FREQUENCY TESTING

Figures 5a, 5b, and 5c show the actual plot of some Beat Frequency Tests. These tests use various clock inputs to the ADC-208 with a full-scale sine wave input offset from the clock frequency by an amount equal to the beat frequency. Although the converter would not normally be used in this mode because the input frequency violates the Nyquist criteria for full recovery of signal information, the test is an excellent demonstration of the ADC-208's high frequency performance.

The effect of the frequency difference between the input and the clock is that the output will be a sinusoidal digital data array which "walks" along the actual input at a beat note frequency. Any inability to follow the input will be immediately obvious by plotting the digital data array. Further arithmetic analysis may be done on the data array to determine spectral purity, harmonic distortion, etc. This test is an excellent indication of:

1. Full power input bandwidth of all 256 comparators (Any gain loss would show as signal distortion).

2. Phase response linearity vs. instantaneous signal magnitude (Phase problems would show as improper codes).

3. Comparator slew rate limiting.

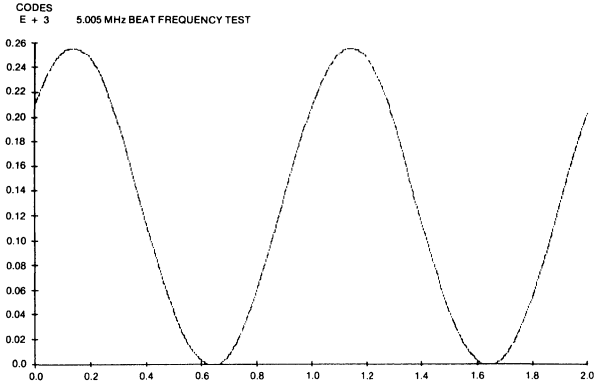


Figure 5a. Beat Frequency Test at Fclock = 5 MHz, Fin = 5.005 MHz

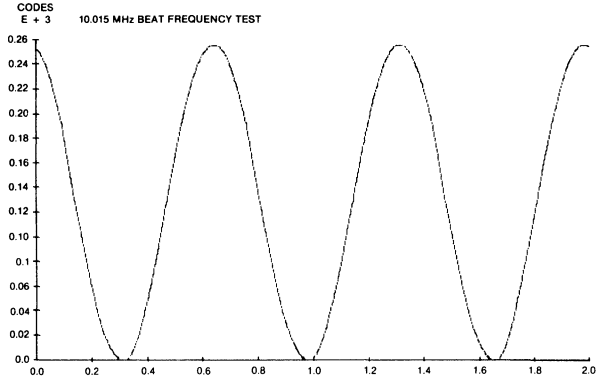


Figure 5b. Beat Frequency Test at Fclock = 10 MHz, Fin = 10.015 MHz

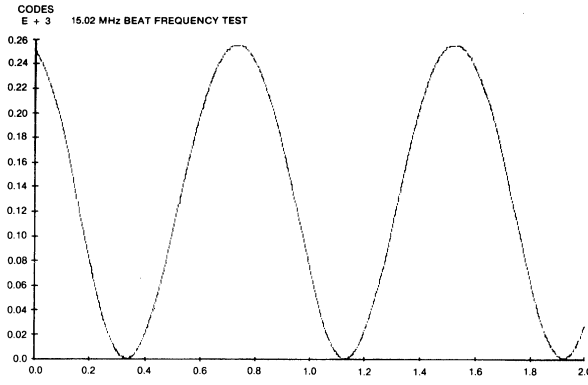


Figure 5c. Beat Frequency Test at Fclock = 15 MHz, Fin = 15.02 MHz

ENVELOPE TEST

Figures 6a, 6b, 6c, and 6d show the actual plot of the Envelope Test. This test is a variation of the Beat Frequency test using a sine wave input to give two overlapping cycles when the data is reconstructed by a D/A converter output to an oscilloscope. An input signal offset in frequency from the Nyquist Rate will result in consecutive samples at 180 degree intervals on the waveform.

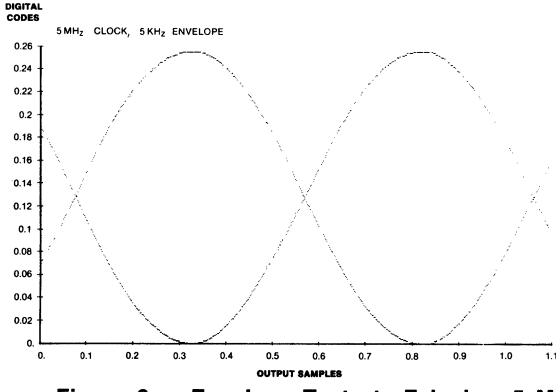


Figure 6a. Envelope Test at Fclock = 5 MHz

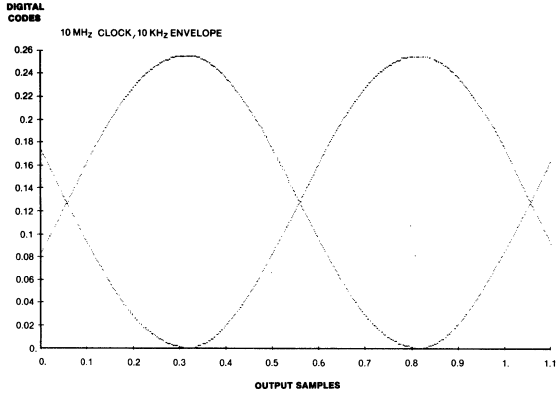


Figure 6b. Envelope Test at Fclock = 10 MHz

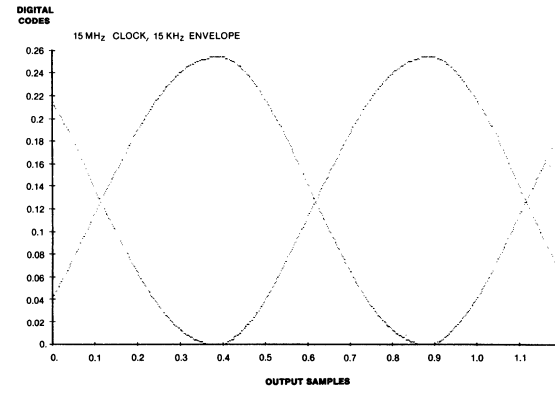


Figure 6c. Envelope Test at Fclock = 15 MHz

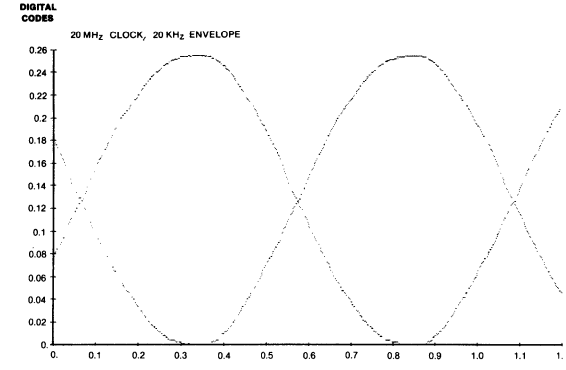


Figure 6d. Envelope Test at Fclock = 20 MHz

The scope is triggered by the clock used by the A/D. Any asymmetry between positive and negative portions of the signal will be very obvious. This test is a an excellent indication of slew rate capability. At the peaks of the envelope, consecutive samples swing completely through the input voltage range.

FFT TESTS

These tests produce an amplitude versus frequency graph (Figures 7a, 7b, 7c, and 7d) which indicates harmonic distortion and signal to noise ratio. The theoretical RMS signal-to-noise ratio for an 8-bit converter is 49.8 dB.

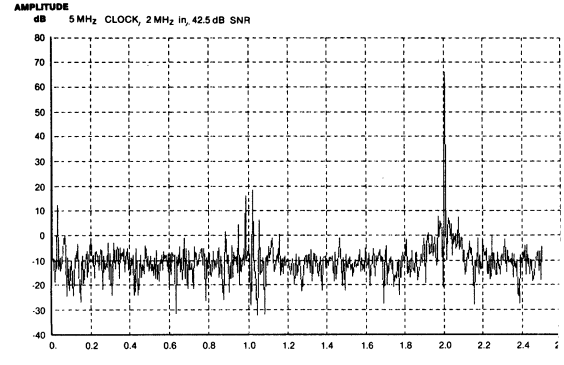


Figure 7a. FFT Test at Fclock = 5 MHz, Fin = 2 MHz

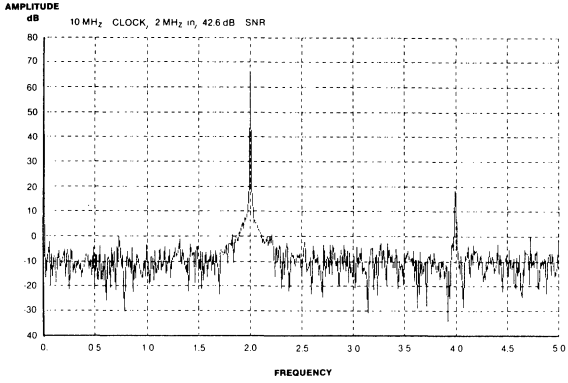


Figure 7b. FFT Test at Fclock = 10 MHz, Fin = 2 MHz

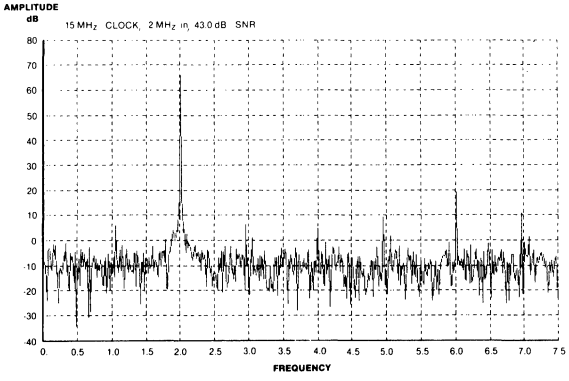


Figure 7c. FFT Test at Fclock = 15 MHz, Fin = 2 MHz

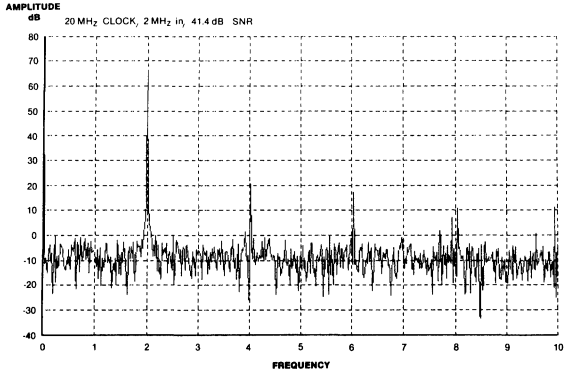


Figure 7d. FFT Test at Fclock = 20 MHz, Fin = 2 MHz

LOW POWER MODES

Power Supply Aspect of Power Dissipation

Reduction of the V_{DD} power supply of the ADC-208 results in lower power dissipation. Refer to the curve of Figure 8 for power dissipation as a function of V_{DD}. The limiting factor is V_{DD} must be greater than the TTL or CMOS output levels. Interfacing to standard logic families presents little problem as the output drivers go to V_{DD} for a high state and to VSS for a low state.

BURST MODE

Applications can utilize an inherent system clock up to 30 MHz in the burst mode. The system clock can generate a one shot for a single conversion without requiring generation of a separate clock at a lower frequency.

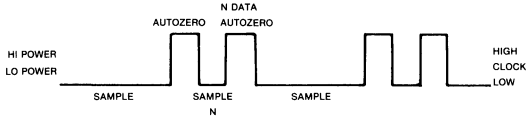


Figure 9a. Burst Mode for Low Power

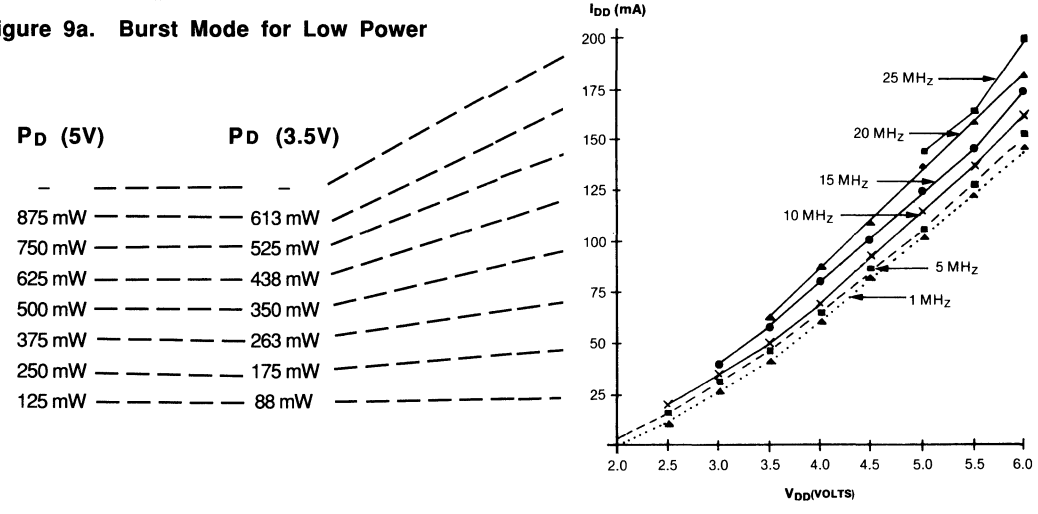
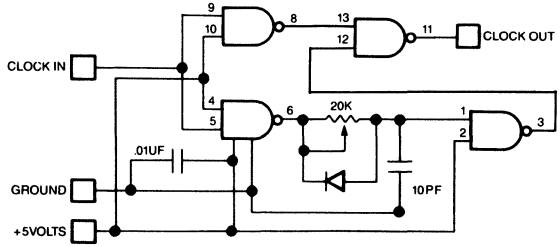


Figure 8. Power Dissipation Versus V_{DD}

Clock Aspects of Power Dissipation

Varying the CLOCK rate or duty cycle results in lower power dissipation. The majority of the power dissipation occurs during the auto zero mode.



NOTE: Reduce the sample time (sample pulse) to 12 nsec. to improve performance above 20 MHz. Such a configuration will closely resemble an ideal sampler.

Figure 9b. Optional Clock Pulse Shaping Circuit

Figure 10 shows power dissipation as a function of burst rate and repetition rate. Applications not requiring continuous conversions can give a double clock pulse, the clock returning low between conversions to reduce power dissipation. Power dissipation is essentially eliminated when the clock and signal input are turned off.

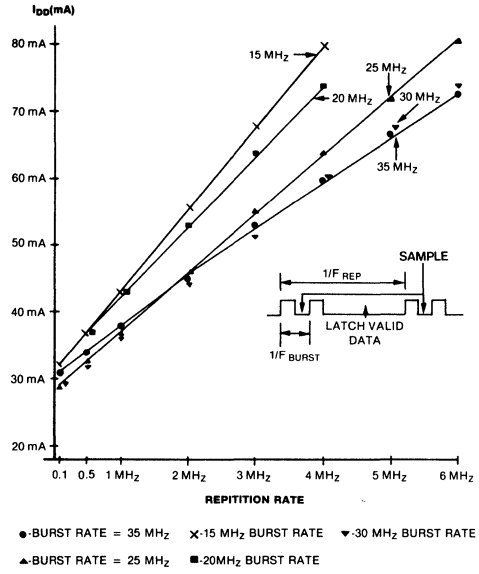


Figure 10. Power Dissipation vs. Burst Rate vs. Repetition Rate

Figure 11 shows power dissipation as a function of the clock duty cycle. A conversion time of 35 nanoseconds can be obtained for a single conversion by leaving the clock in the Auto-zero mode. To initiate a conversion, the clock is put in the sample mode for 25 nanoseconds and then brought back high to the Auto-zero mode. Data is valid 15 nanoseconds after the clock goes high, eliminating the pipeline delay.

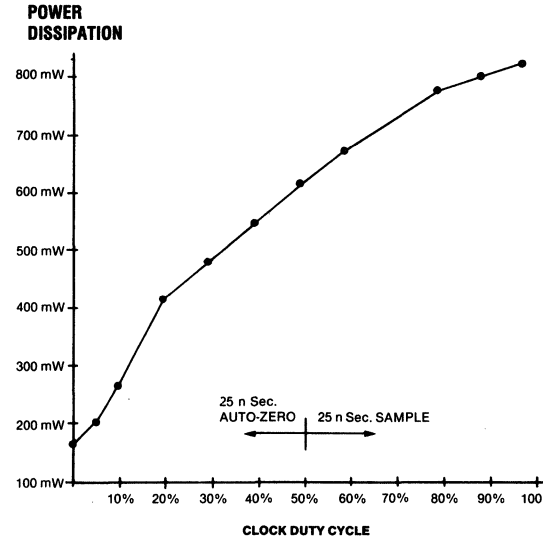


Figure 11. Power Dissipation vs. Duty Cycle for One-Shot Mode

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE
ADC-208MC	0 °C to +70 °C	24-pin DIP
ADC-208MM	-55 °C to +125 °C	24-pin DIP
ADC-208/883B	-55 °C to +125 °C	24-pin DIP
ADC-208LC	0 °C to +70 °C	24-pin LCC
ADC-208LM	-55 °C to +125 °C	24-pin LCC
ADC-208L/883B	-55 °C to +125 °C	24-pin LCC

ADC-300
8-Bit Video
A/D Converter

FEATURES

- **8 Bits at 20 MHz**
- **700 mW power dissipation**
- **+ ½ LSB linearity**
- **Buffered outputs**
- **Single supply operation**
- **ECL-compatible**
- **Input bandwidth 5.5 MHz**

GENERAL DESCRIPTION

DATEL's ADC-300 is a bipolar monolithic video speed, low power, 8-bit flash A/D converter capable of digitizing an analog signal at conversion rates up to 20 MHz minimum with power consumption of only 700 mW.

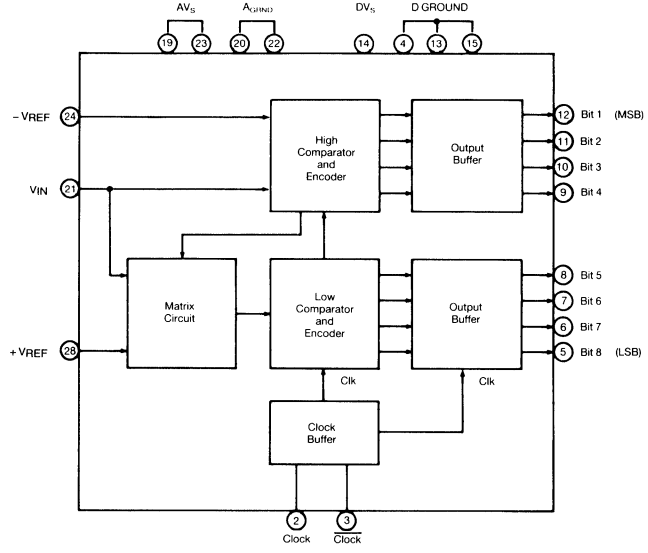
A serial/parallel technique is employed to obtain the high conversion speed using a single -5.0V power source. The analog input range is 0 to -2V (with -2V ref) and digital inputs and outputs are ECL-compatible. The outputs are buffered and provide an open emitter output.

The ADC-300 is designed to operate with an external sample and hold together with external clock and reference sources. It is ideally suited for applications that require high speed digitization and low power, e.g. CRT graphics, radar pulse analysis, motion signature analysis and optical character recognition.

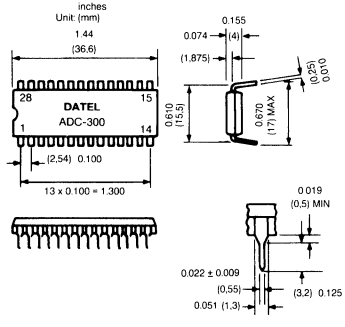
The ADC-300 is supplied in a 28-pin DIP and operates over temperature range of -10 to +70°C.

APPLICATIONS

- **High speed data acquisition**
- **Radar pulse analysis**
- **TV video encoding**
- **High energy physics**
- **Transient analysis**
- **Medical electronics**
- **Fluid flow analysis**
- **Sonar systems**



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIAS (NOT TO BE CONNECTED)	28	REF. VOLTAGE (-2.0V)
2	CLOCK INPUT	27	ADJUST REF. (AR3)
3	$\overline{\text{CLOCK}}$ INPUT	26	ADJUST REF. (AR2)
4	DIGITAL GROUND	25	ADJUST REF. (AR1)
5	BIT 8 (LSB)	24	REF. VOLTAGE (0V)
6	BIT 7	23	V. SUPPLY (-5V)
7	BIT 6	22	ANALOG GROUND
8	BIT 5	21	ANALOG INPUT
9	BIT 4	20	ANALOG GROUND
10	BIT 3	19	V. SUPPLY (-5V)
11	BIT 2	18	NO CONNECTION
12	BIT 1	17	NO CONNECTION
13	DIGITAL GROUND	16	NO CONNECTION
14	V. SUPPLY (-5V)	15	DIGITAL GROUND

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_S)	-9.0V
Analog Input (V_{IN})	V_S to +0.3V
Clock Input	V_S to +0.3V
Reference Voltage Input	V_S to +0.3V
Digital Output Current	10 mA
Package Dissipation	1.47 Watts

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, V_S = -5V dc, reference volt. = -2V dc unless otherwise stated.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Input Range	0	-	-2.0	V
Analog Input Current V_{IN} = -1.0V	-	20	37	μA
Analog Input Capacitance	-	70	-	pF
Ladder Impedence	45	50	56	Ohms
Reference Voltage	-1.90	-2.0V	-2.10	V
Clock Voltage (1)	-0.74	-0.89	-1.04	V
Clock Voltage (0)	-1.60	-1.75	-1.90	V
Clock Current	-	20	34.5	μA
Clock Frequency	20	30	-	MHz
OUTPUTS				
Output Logic (1) RL = 4.3K	-	-0.75	-0.90	V
Output Logic (0) RL = 4.3K	-1.35	-1.50	-	V
POWER				
Power Requirement RL = 4.3K	110	140	160	mA
Supply Voltage	-4.75	-5.0	-5.25	V
PERFORMANCE				
Resolution	8 Bits			
Conversion Speed (Min)	20 MHz			
Non Linearity (Max)	±½ LSB			
Differential Non Linearity (Max)	±½ LSB			
Differential Gain (Typ)	0.7%			
Differential Phase (Typ)	0.3 Degrees			
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range	-10°C to 70°C			
Storage Temperature Range	-50°C to 150°C			
Package	28-Pin plastic DIP			

TECHNICAL NOTES

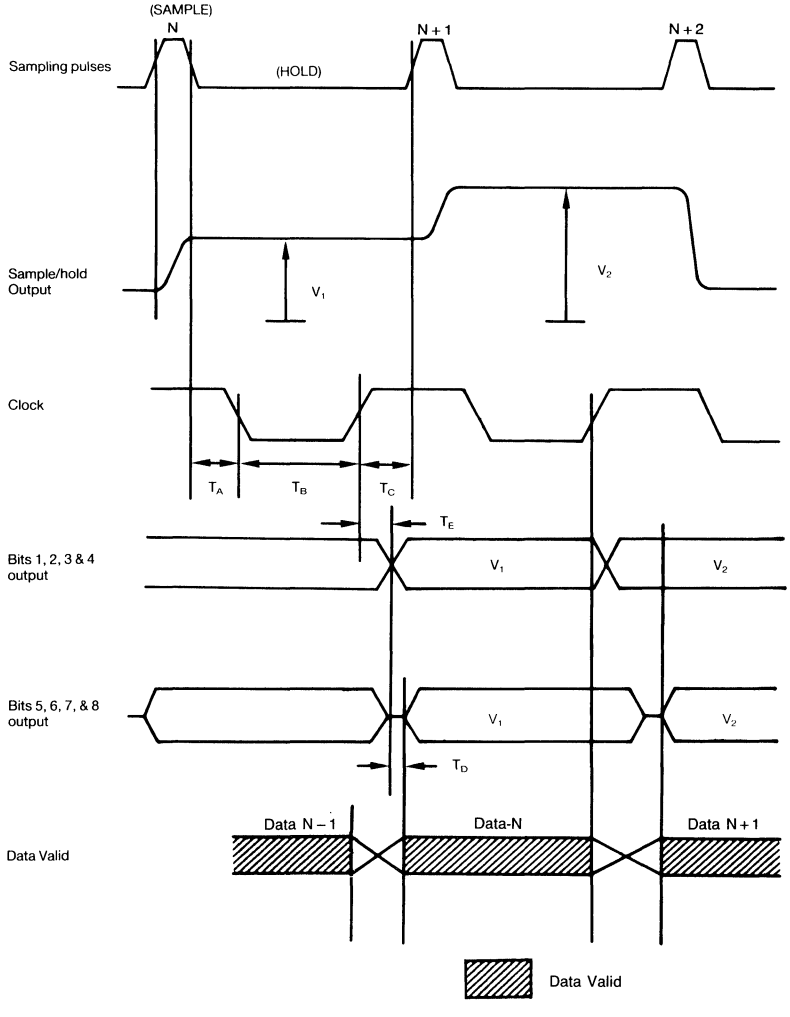
1. Analog input signals must be 'held' by an external sample-hold e.g. using a DATEL SHM-40, SHM-360 or SHM-361. Careful attention must be paid to the timing relationship between the sample-hold transition of the sample-hold amplifier and positive transition of the clock pulse — see timing diagram.
2. The input capacitance to the converter, pin 21, is 70 pF (typical) and the input bias current 20 μA (typical).
3. The reference voltage, -2.0 volts, is connected to pin 28 with pin 24, the upper end of the resistor chain, grounded. The 'R' value between pins 24 and 28 is 50 Ohms (typical). It is recommended the reference input is decoupled using a 1 μF (tantalum) and a 1000 pF (ceramic) capacitor located as close to pin 28 as possible.
4. For most applications, the ADC-300 accuracy will be more than sufficient. However where accuracy greater than that specified is required, the VREF/4, VREF/2 and VREF3/4 points can be trimmed using external resistors connected from pins 25, 26 and 27 to ground, pin (24), or VREF, pin (28), as required.

   When pins 20, 26, and 27 are not being used, they should be connected to ground via a 0.047 μF capacitor.
5. The printed circuit board should be laid out to have substantial analog and digital ground planes. The ground plane separation is required as part of the chip design and should be maintained on the PCB. The planes should be connected at one point only, usually power common.
6. The -5.0V supply should be decoupled using 3.3 μF tantalum and 0.022 μF ceramic capacitors.
7. The digital output terminals are driven from open emitters. The output current should not exceed 10 mA (4.3K Ohms are equivalent to 1 mA). Table 1 shows the digital codes relating to the analog input voltages.
8. An external complementary ECL signal source is required to drive the clock input terminals.
9. Pin 1 must be left open and not used; pins 16, 17 and 18 are not internally connected and should be grounded.

TABLE 1. DIGITAL OUTPUT CODES

STEP	INPUT VOLTS (-2V FSR)	OUTPUT CODE MSB				LSB			
0	0.0000V	1	1	1	1	1	1	1	1
1	-0.0078V	1	1	1	1	1	1	1	1
2	-0.0156V	1	1	1	1	1	1	0	1
127	-0.9961V	1	0	0	0	0	0	0	0
128	-1.0039V	0	1	1	1	1	1	1	1
129	-1.0118V	0	1	1	1	1	1	1	0
255	-2.0000V	0	0	0	0	0	0	0	0

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. The high comparator (MSB, Bits 2, 3 and 4) compares V_{REF} with V_{IN} on the negative transition of the clock. The timing must be such that the sample/hold has acquired the input level and settled in the hold mode. If T_A is the time between the sample/hold transition to the negative transition of the clock then:

   $T_A >$ sample hold aperature delay + settling time.

2. **The positive transition of the external clock should occur after time T_B where: $T_B > 22$ nsec. where:**

   From this transition three operations will be timed.

   (a) In time T_C the next sample/hold pulse can be sent where:

   $T_C > 2$ nsec.

   (b) In time T_E the data for MSB, bits 2, 3, and 4 become valid where:

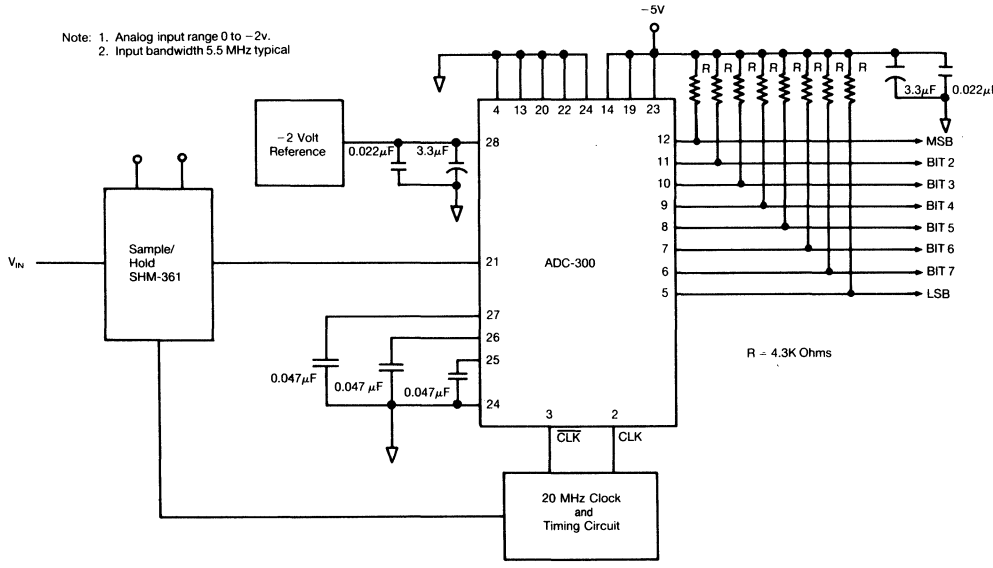
   $T_E < 8$ nsec.

   (c) In time $T_E + T_D$ the data for bits 5, 6, 7, and 8 become valid where:

   $T_E + T_D < 12$ nsec.

3. At the time $T_A + T_B + T_E + T_D$, all data outputs become valid. The output data can be latched at this time, however, the simpler and more reliable time to latch the outputs is the negative transition of the clock.

CONNECTION AND APPLICATION



ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
ADC-300	-10°C to + 70°C

NOTE: For units with high-reliability processing, contact the factory.

ADC-301, ADC-302
8-Bit Video
Flash A/D Converter

FEATURES

ADC-301

- **8-Bit resolution**
- **Non-linearity ±½ LSB**
- **Conversion rate 30 MHz**
- **15 MHz bandwidth**
- **35 pF input capacitance**
- **Power dissipation 420 mW**

ADC-302

- **8-Bit resolution**
- **Non-linearity ±½ LSB**
- **Conversion rate 50 MHz**
- **25 MHz bandwidth**
- **35 pF input capacitance**
- **Power dissipation 550 mW**

GENERAL DESCRIPTION

These ADC's are video speed 8-bit flashes capable of digitizing analog signals at conversion rates of 30 MHz (ADC-301) and 50 MHz (ADC-302) with a power consumption of 420 mW and 550 mW respectively.

The 256 clocked comparators have the analog voltage applied to one input and a voltage derived from the reference voltage and reference resistors applied to the other comparator input.

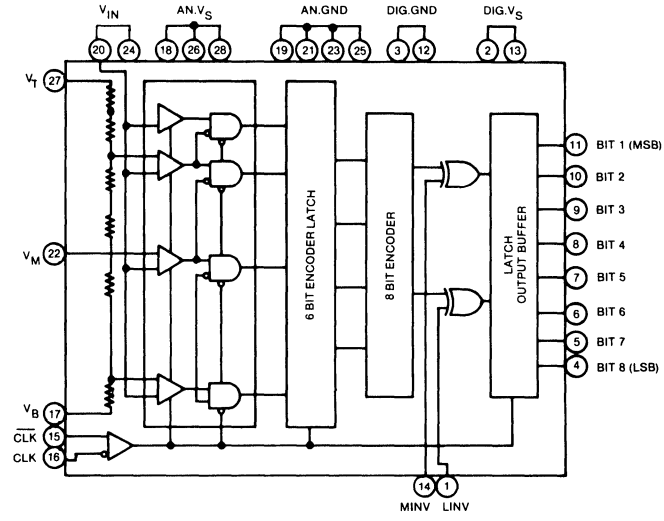
The comparator outputs are 'anded' with adjacent outputs and these outputs latched into a 6-bit encoder. These 6-bit codes are further encoded to 8-bit codes and latched. The final ECL output buffer stage requires external pull down resistors, the output being delayed from the sampling point by the time of one clock cycle.

Output polarity of the MSB and LSB's respectively can be controlled on two digital input lines.

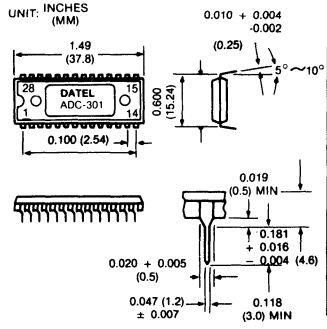
With a reference of -2V the analog input range will be 0 to -2V.

APPLICATIONS

- **High speed data acquisition**
- **Radar pulse analysis**
- **TV video encoding**
- **High energy physics**
- **Transient analysis**
- **Medical electronics**
- **Fluid flow analysis**
- **Sonar systems**



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT POLARITY (LINV)	28	ANALOG Vs (−5.2V)
2	DIGITAL Vs (−5.2V)	27	REFERENCE INPUT Vt (−0V)
3	DIGITAL GROUND	26	ANALOG Vs (−5.2V)
4	BIT 8 (LSB)	25	ANALOG GROUND
5	BIT 7	24	ANALOG INPUT
6	BIT 6	23	ANALOG GROUND
7	BIT 5	22	REFERENCE Vm
8	BIT 4	21	ANALOG GROUND
9	BIT 3	20	ANALOG INPUT
10	BIT 2	19	ANALOG GROUND
11	BIT 1 (MSB)	18	ANALOG Vs (−5.2V)
12	DIGITAL GROUND	17	REFERENCE INPUT Vb (−2V)
13	DIGITAL Vs (−5.2V)	16	CLOCK INPUT
14	OUTPUT POLARITY (MINV)	15	$\overline{\text{CLOCK}}$ INPUT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_S	0 to -7V
Input Voltage (V_{IN})	0.5V to V_S
Reference Voltage V_t, V_b, V_m	0.5V to V_S
Reference Voltage (V_b -V_t)	-2.5V
Digital Inputs	0.5V to -4V
Vm Input Current	-3 mA to +3 mA
Digital Outputs	0 to -10 mA
Operating Temperature	-20°C to +100°C
Storage Temperature	-55°C to +150°C
Allowable Power Dissipation	1.48 W

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, V_S = -5.2V dc, V_B = -2.0V unless otherwise stated.

PERFORMANCE	ADC-301	ADC-302
Resolution	8 Bits	8 Bits
Conversion Rate (Min)	30 MHz	50 MHz
Non-Linearity (Max)	+½ LSB	+½ LSB
Diff. Non-Linearity (Max)	+½ LSB	+½ LSB
Diff. Gain (Max)	1.5%	1.5%
Diff. Phase (Max)	0.5 Deg.	0.5 Deg.
Aperture Jitter (Typ)	45 psec.	30 psec.
Input Bandwidth (Typ)	15 MHz	25 MHz
Power Dissipation (Typ)	420 mW	550 mW

INPUTS	MIN.	TYP.	MAX.	UNITS
Reference Input Voltage	-1.8	-2.0	-2.2	V
Reference Resistance	70	80	100	Ohms
Analog Input Voltage	0.1	—	-2.2	V
Analog Input Capacitance	—	35	40	pF
Analog Input Bias Current				
(ADC-301)	—	60	90	µA
(ADC-302)	—	75	115	µA
Offset Voltage V_t	7	9	11	mV
V_b	15	17	19	mV
Digital Input Voltage				
V_h	-0.7	-0.9	-1.0	V
V_l	-1.6	-1.75	-1.9	V
Digital Input Current				
(V_h = -0.9V)	0	—	0.4	mA
(V_l = -1.75V)	-0.05	—	0.35	mA
OUTPUTS				
Digital Output Voltage				
V_h (R_L = 620 Ω)	-1.0	—	—	V
V_l (R_L = 620 Ω)	—	—	-1.6	V
Output Data Delay (R_L = 620 Ω)	—	4.0	5.0	nsec.
POWER				
Supply Voltage, V_S	-5.0	-5.2	-5.7	V
Supply Current				
(ADC-301)	—	-75	-100	mA
(ADC-302)	—	-95	-120	mA

TECHNICAL NOTES

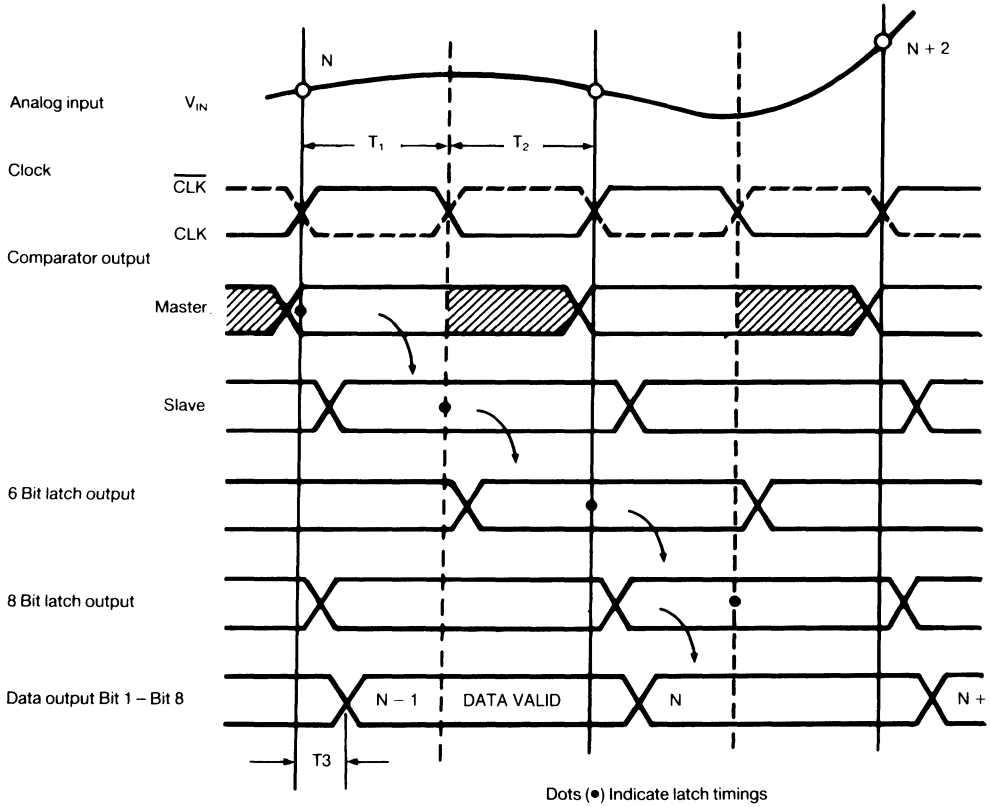
1. Even with the input capacitance down to 35 pF, or less, the converter still requires an input amplifier with good drive capability. The amplifier will require wide bandwidth and a high slew rate (250V/ µS typical) to take full advantage of the input bandwidth of the converter.
2. The input impedance of the A/D's are capacitive which may result in the input amplifier becoming unstable and cause oscillations. A resistor with a value between 2 and 10 Ohms between the amplifier and the input to the converter will stop any oscillations.
3. Clock and $\overline{\text{Clock}}$ (ECL) are usually differentially supplied to pins 16 and 15.
4. The polarity of the output data is controlled by two polarity inversion inputs, MINV (pin 14) which controls the MSB alone and LINV (pin 1) which controls Bit 2 to Bit 8 (LSB). The combination of '0's and '1' on these inputs offer the user various code options. Detailed coding is shown in Table 1. Logic level '0' is obtained by leaving inputs open, logic level '1' is obtained by connecting a 3.9K Ohm resistor to digital ground.
5. The digital outputs Bits 1 to 8 require pull down resistors, in the range 500 to 1000 Ohms, connected to the negative supply rail to prevent waveform distortions by reflection.
6. The reference voltage range (-2.0V to 0V typical) determines the dynamic range of the input voltage.

   Adjustments to this range can be made within the range V_B = 2V ± 0.2V and V_T = 0V ±0.1V. The reference input V_B (pin 17) should be decoupled to analog ground using 1 µF and 0.01 µF capacitors. Improvement in the high frequency stability can be achieved by decoupling terminal V_M (pin 22) using a 0.01 µF.
7. Terminal V_M is used to achieve less than a ± ½ LSB nonlinearity error. The external circuit to achieve this is shown in the application drawing.
8. All pins not being used should be grounded.
9. Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground line, as close to the converter as possible.
10. The power supplies to analog and digital inputs (-5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second there is a possibility the device may be destroyed. Both -5.2V lines should be decoupled using 1 µF and 0.01 µF capacitors located as close to the pins as possible.

TABLE 1. DIGITAL OUTPUT CODES

MINV / LINV	0 / 0	0 / 1	1 / 0	1 / 1
0.0000V	1111 1111	1000 0000	0111 1111	0000 0000
-0.0078V	1111 1110	1000 0001	0111 1110	0000 0001
-0.9961V	1000 0000	1111 1111	0000 0000	0111 1111
-1.0039V	0111 1111	0000 0000	1111 1111	1000 0000
-1.9922V	0000 0001	0111 1110	1000 0001	1111 1110
-2.0000V	0000 0000	0111 1111	1000 0000	1111 1111

TIMING DIAGRAM



Dots (•) Indicate latch timings

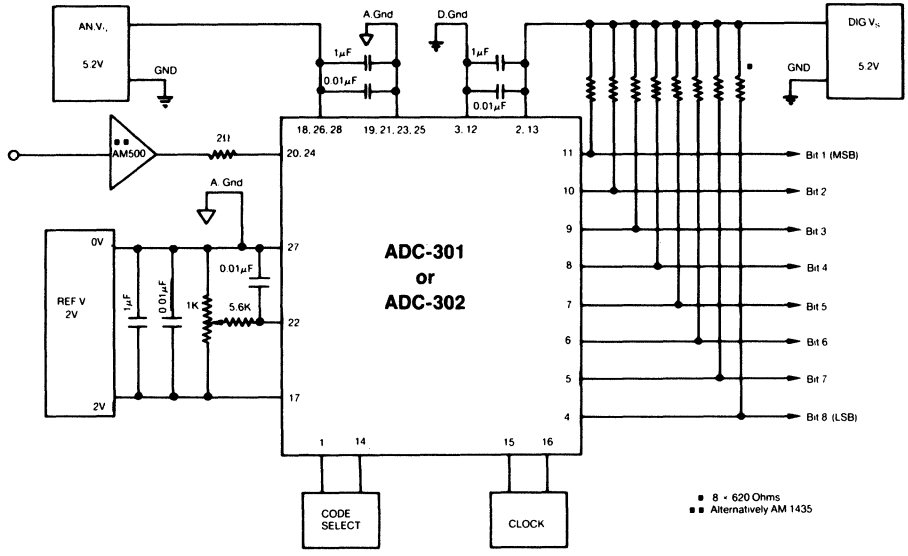
TIMING NOTES

1. Both Clock and $\overline{Clock}$ are required and the input levels are ECL. The timing T_1 and T_2 should be:

	T_1 (MIN)	T_2 (MIN)
ADC-301	25 nsec.	8 nsec.
ADC-302	15 nsec.	5 nsec.

2. The positive transition of the clock latches the comparator outputs into the 'and' gates.
3. The negative transition latches the 'anded' outputs into the 6-bit encoder.
4. The next positive transition will latch the 6-bit encoder output as well as starting the next conversion cycle.
5. The 8-bit encoder output will appear at the output pins 4.0 nsec. (typical) T_3 after 6-bit encoder output has been latched on the next negative transition of the clock.

CONNECTION AND APPLICATION



ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
ADC-301	-20°C to + 100°C
ADC-302	-20°C to + 100°C

ACCESSORIES

Part Number	Description
TP 1K	Trimming Potentiometer

Note: For units with high-reliability processing, contact the factory.

ADC-303
8-Bit Video
Flash A/D Converter

FEATURES

- **8-Bit resolution**
- **Speed up to 100 MHz guaranteed**
- **±½LSB linearity**
- **Input bandwidth 40 MHz**
- **Output latch and buffer**
- **Low input capacitance, 35 pF typical**

GENERAL DESCRIPTION

The ADC-303 is a video speed 8-bit flash converter capable of digitizing analog signals at conversion rates up to 100 MHz minimum and with a power consumption of only 1.2 watts at 100 MHz sampling rate.

The 256 clocked comparators have the analog voltage applied to one input and a voltage derived from the reference voltage and reference resistors applied to the other comparator input.

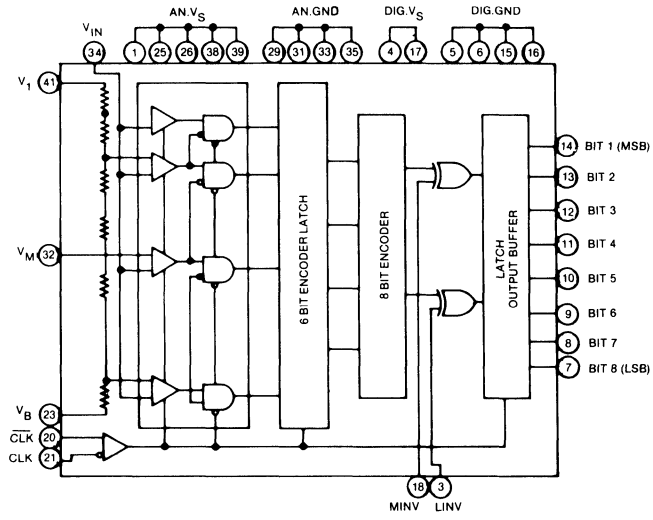
The comparator outputs are 'anded' with adjacent outputs and these outputs latched into a 6-bit encoder. These 6-bit codes are further encoded to 8-bit codes and latched. The final ECL output buffer stage requires external pull down resistors, the output being delayed from the sampling point by the time of one clock cycle.

Output polarity of the MSB and LSB's respectively can be controlled on two digital input lines.

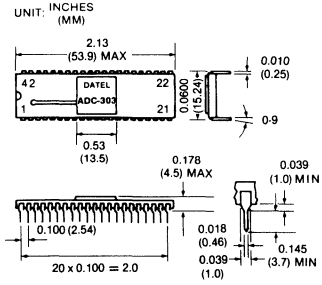
With a reference of -2V the analog input range will be 0 to -2V.

APPLICATIONS

- **High speed data acquisition**
- **Radar pulse analysis**
- **TV video encoding**
- **High energy physics**
- **Transient analysis**
- **Medical electronics**
- **Fluid flow analysis**
- **Sonar systems**



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG SUPPLY (+5.2V)	42	N/C
2	N/C	41	REFERENCE V_1 (0V)
3	LINV	40	N/C
4	DIGITAL SUPPLY DV$_1$ (+5.2V)	39	ANALOG SUPPLY AV$_1$ (+5.2V)
5	DIGITAL GROUND	38	ANALOG SUPPLY AV$_1$ (+5.2V)
6	DIGITAL GROUND	37	N/C
7	BIT 8 (LSB)	36	N/C
8	BIT 7	35	ANALOG GROUND
9	BIT 6	34	INPUT
10	BIT 5	33	ANALOG GROUND
11	BIT 4	32	REFERENCE V_M
12	BIT 3	31	ANALOG GROUND
13	BIT 2	30	INPUT
14	BIT 1 (MSB)	29	ANALOG GROUND
15	DIGITAL GROUND	28	N/C
16	DIGITAL GROUND	27	N/C
17	DIGITAL SUPPLY DV$_1$ (+5.2V)	26	ANALOG SUPPLY V$_1$ (+5.2V)
18	MINV	25	ANALOG SUPPLY V$_1$ (+5.2V)
19	N/C	24	N/C
20	Clk	23	REFERENCE V_B (-2.0V)
21	Clk	22	N/C

ABSOLUTE MAXIMUM RATINGS

Power Supply — V_S	0 to -7V
Analog Input (V_{IN})	+0.5V to V_S
Reference Voltage	
$V_T + V_M + V_B$	+0.5V to V_S
$[V_T - V_B]$	2.5V
Input current at V_M	-3 mA to +3 mA
Digital Inputs	0.5V to -4.0V
Digital Output Current	0 to -10 mA
Operating Temp.	-20°C to +100°C
Storage Temp.	-55°C to +150°C
Power Dissipation	3.1 Watts

FUNCTIONAL SPECIFICATIONS.

Typical at +25°C, V_s = -5.2 V dc, V_B = -2.0V unless otherwise stated.

ELECTRICAL PERFORMANCE	MIN.	TYP.	MAX.	UNIT
Conversion Rate	100	—	—	MHz
Input Capacitance	—	35	40	pF
Input Bias Current (V_{IN} = -1V)	—	150	220	μA
Ref. Voltage	-1.8	-2.0	-2.2	V
Reference Resistance (V_T to V_B)	70	80	100	Ohms
Offset Voltage V_T	6	9	12	mV
V_B	14	17	20	mV
Digital Input Voltage V_{IH}	-0.7	-0.9	-1.0	V
V_{IL}	-1.6	-1.75	-1.9	V
Digital Input Current				
(V_{IH} Typ.) I_{IH}	0	—	0.4	mA
(V_{IL} Typ.) I_{IL}	-0.05	—	0.35	mA
Digital Output Voltage (R_L = 620) V_{OH}	-1.0	—	—	V
V_{OL}	—	—	-1.6	V
Integral Non-Linearity (100 MHz)	—	—	± ½	LSB
Differential Non-Linearity (35 MHz)	—	—	± ½	LSB
Differential Gain	—	—	1.5	%
Differential Phase	—	—	0.5	Deg.
Aperture Jitter	—	15	—	psec.
Supply Voltage	-5.2	-5.2	-5.7	V
Supply Current	-180	-220	-260	mA
Output Data Delay (R_L=620)	3.0	3.5	4.2	nSec
Sampling Delay	1.9	2.2	2.5	nSec

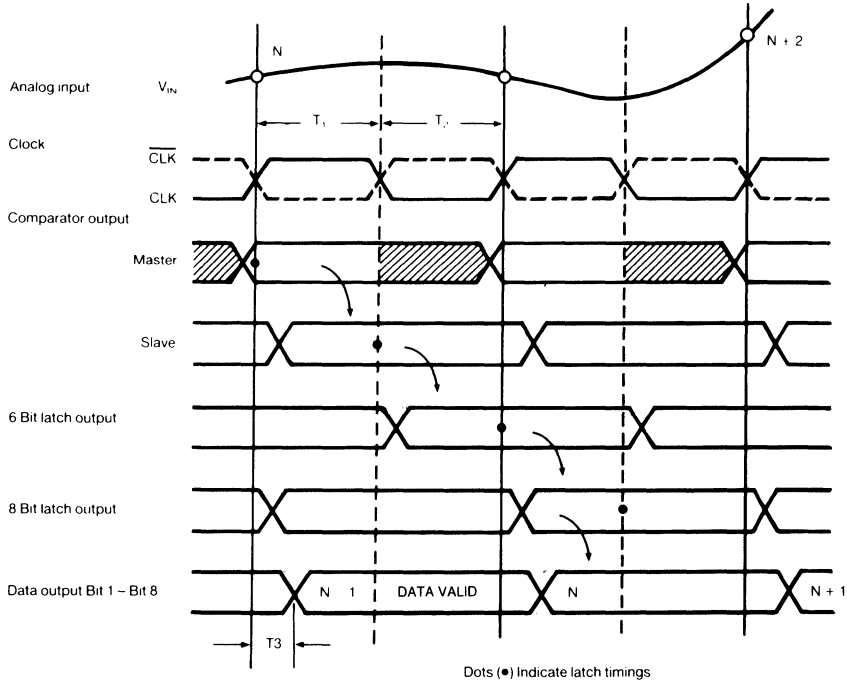
TECHNICAL NOTES

1. Even with the input capacitance down to 35 pF, or less, the converter still requires an input amplifier with good drive capability. The amplifier will require wide bandwidth and high slew rate (250V/ μS typical) to take full advantage of the 40 MHz bandwidth of the converter.
2. The input impedence of the A/D is capacitive which may result in the input amplifier becoming unstable and cause oscillations. A resistor with a value between 2 and 10 Ohms between the amplifier and the input to the converter will stop any oscillations.
3. **Clock and $\overline{\text{Clock}}$ (ECL) are usually differentially supplied to pins 20 and 21. However a single clock input can be used if a 1000 pF capacitor is added between pin 20 (clock) and pin 16 (digital ground).**
4. The polarity of the output data is controlled by two polarity inversion inputs, MINV (pin 18) which controls the MSB alone and LINV (pin 3) which controls bit-2 to bit-8 (LSB). The combination of '0's and '1' on these inputs offer the user various code options. Refer to the coding table. Logic level '0' is obtained by leaving inputs open, logic level '1' is obtained by connecting a 3.9K Ohm resistor to digital ground.
5. The digital outputs, bits 1 to 8, require pull down resistors, in the range of 500 to 1000 Ohms, connected to the negative supply rail to prevent waveform distortion by reflection.
6. The reference voltage range (-2.0V to 0V typical) determines the dynamic range of the input voltage. Adjustments to this range can be made within the range of V_B = 2 ±0.2V and V_T = 0V ±0.1V. The reference input V_B (pin 23) should be decoupled to analog ground using 1 μF and 0.01 μF capacitors. Improvement in the high frequency stability can be achieved by decoupling terminal V_M (pin 32) using a 0.01 μF.
7. Terminal V_M is used to achieve a less than ±½ LSB linearity error. The external circuit to achieve this is shown in the application drawing.
8. All pins not being used should be grounded.
9. Substantial analog and digital ground planes must be provided. It is recommended that these ground planes are taken to a common point, the power ground line, as close to the ADC-303 as possible.
10. The power supplies to analog and digital inputs (-5.2V) should be supplied from separate, isolated power supplies. If one of the power supplies fails or is shorted to ground for more than 1 second there is a possibility the device may be destroyed. Both -5.2V lines should be decoupled using 1 μF and 0.01 μF capacitors located as close to the pins as possible.

DIGITAL OUTPUT CODES

MINV / LINV	0 / 0	0 / 1	1 / 0	1 / 1
0.0000V	1111 1111	1000 0000	0111 1111	0000 0000
-0.0078V	1111 1110	1000 0001	0111 1110	0000 0001
-0.9961V	1000 0000	1111 1111	0000 0000	0111 1111
-1.0039V	0111 1111	0000 0000	1111 1111	1000 0000
-1.9922V	0000 0001	0111 1110	1000 0001	1111 1110
-2.0000V	0000 0000	0111 1111	1000 0000	1111 1111

TIMING DIAGRAM



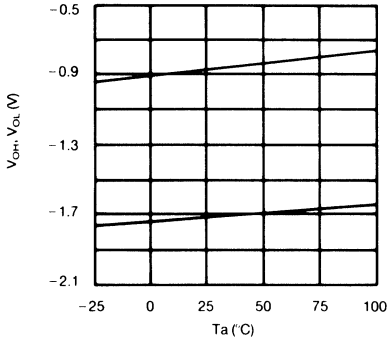
Dots (•) Indicate latch timings

TIMING NOTES

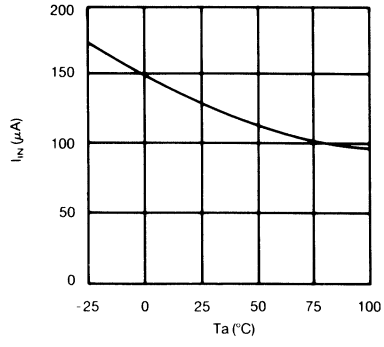
1. Both Clock and $\overline{Clock}$ are required and the input levels are ECL. The timing T_1 and T_2 should be T_1 min. = 7.5 nsec. T_2 min. = 2.5 nsec.
2. The positive transition of the clock latches the comparator outputs into the 'and' gates.
3. The negative transition latches the 'anded' outputs into the 6-bit encoder.
4. The next positive transition will latch the 6-bit encoder output as well as starting the next conversion cycle.
5. The 8-bit encoder will appear at the output pins 3.5 nsec. (typical) T_3 after 6-bit encoder output has been latched on the next negative transition of the clock.

PERFORMANCE CURVES

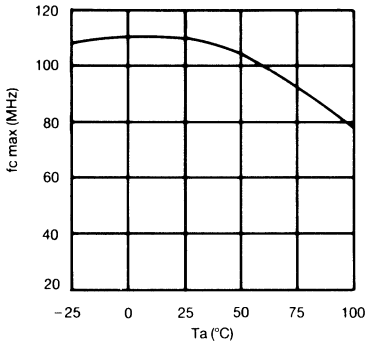
Digital Output Voltage



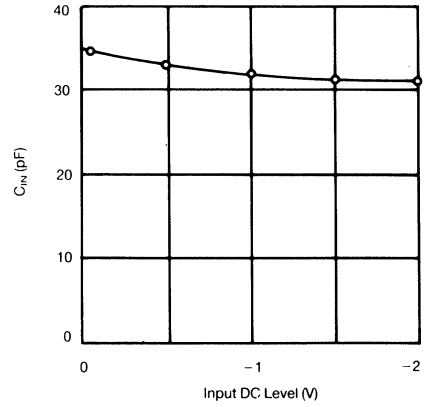
Input Bias current



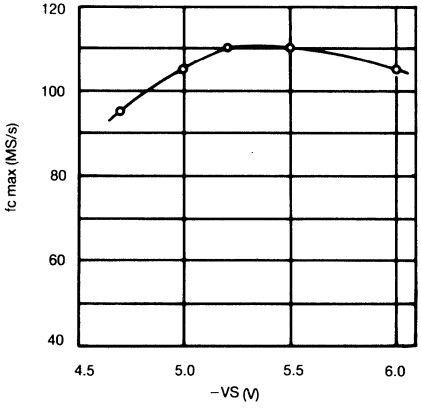
Maximum Conversion Rate



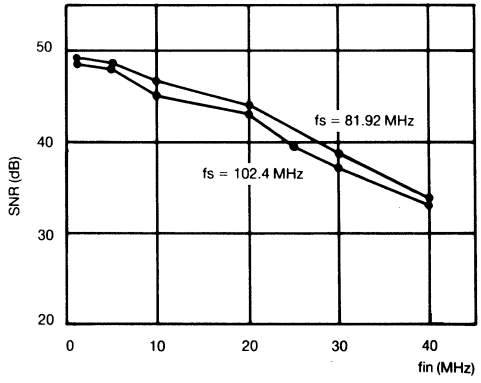
Input Bias Voltage-Analog Input Capacitance (typ.)



Supply Voltage-Maximum Conversion Frequency (typ.)

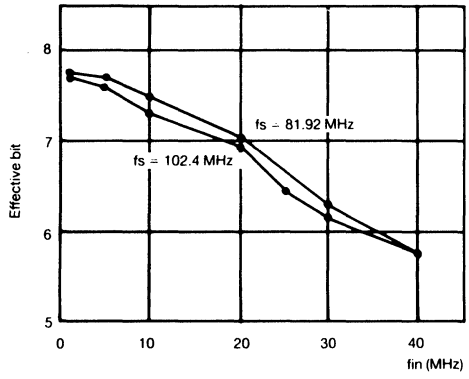


SNR

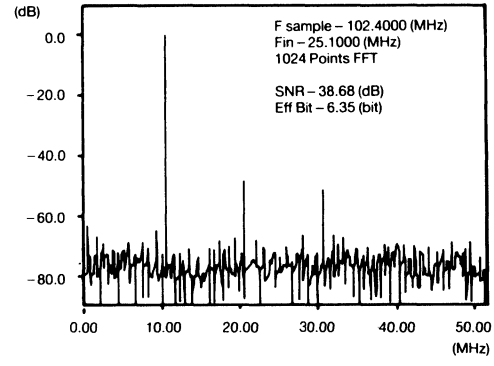


PERFORMANCE CURVES

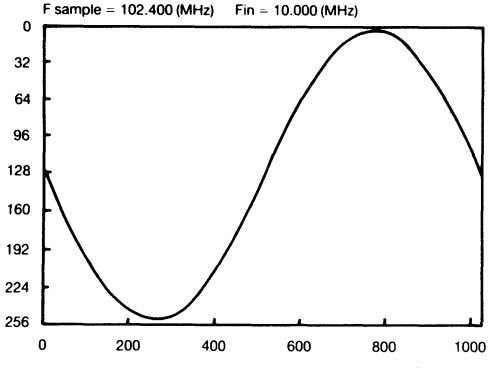
Effective bit



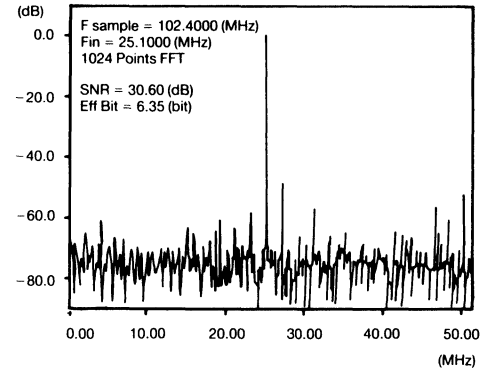
Spectrum with the aid of FFT at 102.4 MHz sampling and 10.1 MHz input.



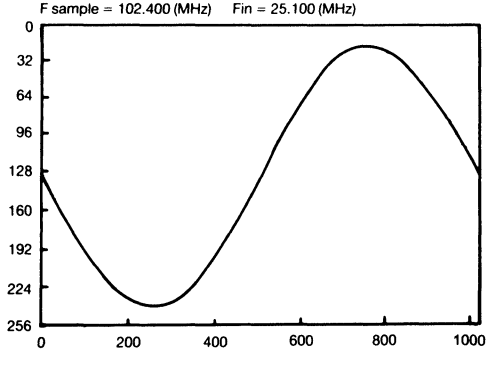
Reconstructed waveform. 102.4 MHz sampling, 10.1 MHz input.



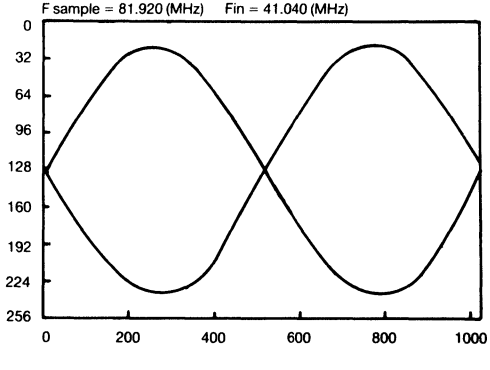
Spectrum with the aid of FFT at 102.4 MHz sampling and 25.1 MHz input.



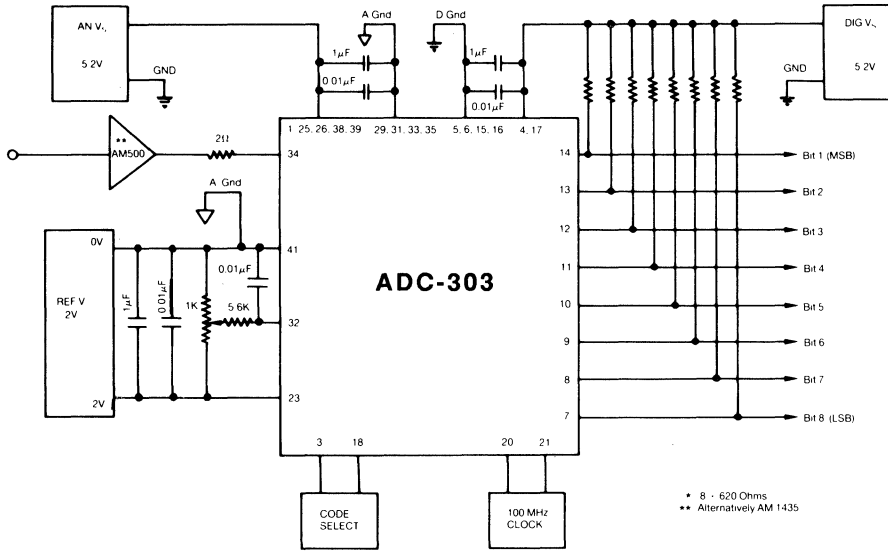
Reconstructed waveform with the best fitted sine wave. 102.4 MHz sampling, 25.1 MHz input.



Envelope test waveform at 41.04 MHz input and 81.92 MHz sampling.



CONNECTION AND APPLICATION



ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
ADC-303	-20°C to +100°C

NOTE: For units with British Standard BS-9000 or other high-reliability processing, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-304
8-BIT, 20 MHz
LOW POWER, FLASH A/D

FEATURES

- 8-Bit resolution.
- ±½ LSB non-linearity.
- 20 MHz conversion rate.
- 8 MHz input bandwidth (−3 dB).
- Low power consumption (390 mW).
- TTL-compatible.
- Single or dual supply operation.

APPLICATIONS

- High-speed data acquisition.
- Radar pulse analysis.
- TV video encoding.
- High energy physics.
- Transient analysis.
- Medical electronics.
- Sonar systems.

GENERAL DESCRIPTION

DATEL's ADC-304 is an 8-bit, 20 MHz analog-to-digital flash converter. The ADC-304 offers many performance features not obtainable from other flash A/D's.

Key features include a low-power dissipation of 390 mW and TTL compatible outputs. A wide analog input bandwidth of 8 MHz (−3 dB) allows operation without the need of a sample-hold. Also, single +5V supply operation is obtainable with an input range of +3 to +5V, eliminating the need for an additional power supply. A 0 to −2V input range is available with ±5V supply operation.

Another novel feature of the ADC-304 is its user-selectable output coding. The MINV and LINV pins allow selection of Binary, Complementary Binary and if external offset circuitry is used for bipolar inputs, Offset Binary, Two's Complement and Complementary Two's Complement coding.

The ADC-304 is supplied in a 28-pin dual in-line package and operates over a −20°C to +75°C temperature range. Storage temperature range is from −65°C to +150°C.

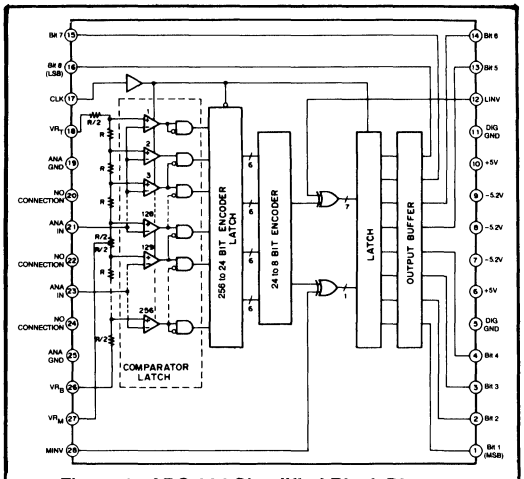
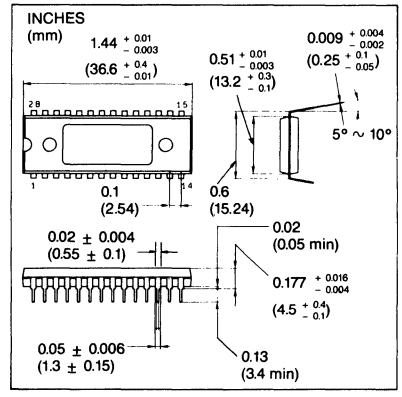


Figure 1: ADC-304 Simplified Block Diagram

Table 1. ADC-304 Input/Output Connections

Pin	Function	Pin	Function
1	BIT 1 OUT (MSB)	15	BIT 7 OUT
2	BIT 2 OUT	16	BIT 8 OUT (LSB)
3	BIT 3 OUT	17	CLOCK INPUT
4	BIT 4 OUT	18	V_{RT}
5	DIG GND	19	ANA GND
6	+5V POWER (V_{CC})	20	NO CONNECTION
7	−5.2V POWER (V_{EE})	21	ANA IN
8	−5.2V POWER (V_{EE})	22	NO CONNECTION
9	−5.2V POWER (V_{EE})	23	ANA IN
10	+5V POWER (V_{CC})	24	NO CONNECTION
11	DIG GND	25	ANA GND
12	LINV	26	V_{RB}
13	BIT 5 OUT	27	V_{RM}
14	BIT 6 OUT	28	MINV

MECHANICAL DIMENSIONS



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)			
Supply Voltage	V_{CC}-GND V_{EE}-GND	0 to +6 0 to −6	V V
Input Voltage (analog)	Vin (Dual Power Supply)	V_{EE} to ANA GND +0.3	V
Input Voltage (reference)	V_{RT}, V_{RB}, V_{RM} (Dual Power Supply) $\lvert V_{RT}—V_{RB} \rvert$	V_{EE} to ANA GND +0.3 2.5	V V
Input Current	I_{VRM}	−3.0 to +3.0	mA
Input Voltage	Digital Inputs	−0.5 to V_{CC}	V

FUNCTIONAL SPECIFICATIONS

Unless otherwise noted, the following specifications apply to the ADC-304 when used either with a single or dual power source. The test conditions are:

For Single Power Supply Operation:
V_{CC} (Pins 6 + 10) = +5V, DIG GND = 0V
V_{EE} (Pins 7, 8 + 9) = 0V, V_{RT} (Pin 18) = +5V
V_{RB} (Pin 26) = +3V, Ta = 25°C
ANA GND (Pins 19 + 25) = +5V

For Dual Power Supply Operation:
V_{CC} (Pins 6 + 10) = +5V, DIG GND (Pins 5 + 11) = 0V
ANA GND = 0V, V_{EE} = -5V
V_{RT} (Pin 18) = 0V, V_{RB} (Pin 26) = -2V
Ta = 25°C

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Inputs				
Analog				
Input Range	V_{RB}		V_{RT}	V
Input Capacitance[1]	-	30	35	pF
Input Bias Current[2]	-	50	100	μA
Offset Voltage:				
(V_{RT})	8	13	19	mV
(V_{RB})	0	5	11	mV
Digital				
Logic Levels:				
Logic "1"	2.0	-	-	V
Logic "0"	-	-	0.8	V
Logic Input Currents[3]:				
Logic "1"	-	−100	0	μA
Logic "0"	-	−0.32	−0.5	mA
Outputs				
Resolution	8			Bits
Output Coding	Straight Binary Complementary Binary 2's Complement Complementary 2's Complement			
Logic levels:				
Logic "1"	2.7	3.4	-	V
Logic "0"	-	-	0.5	V
Logic Level Loading:				
Logic "1"	-	−500	-	μA
Logic "0"	-	-	3	mA
Output Data Delay				
(TDLH)	-	25	30	nSec.
(TDHL)	-	26	35	nSec.

TECHNICAL NOTES

1. DIG GND pins (5 and 11) and V_{CC} pins (6 and 10) connect to separate internal circuits within the ADC-304. Connect these pins to their respective PCB patterns.
2. Layout of the analog and digital sections should be separated to reduce interference from noise. To further guard against unwanted noise, it is recommended to bypass, as close as possible, the voltage supply pins (6,10) to their respective ground pins (5,11) with a 1 μF and a 0.01 μF ceramic disk capacitor in parallel.
3. The input capacitance of the analog input is much smaller than that of a typical Flash A/D Converter. It is necessary to use an amplifier with sufficient bandwidth and driving power. The analog input pins (21,23) are separated internally, so they should be connected together externally. If the ADC-304 is driven with a low- output impedance amplifier, parasitic oscillations may occur.

   These parasitic oscillations can be prevented by introducing a small resistance of 2 to 10Ω between the amplifier output and the ADC-304's A/D input. This resistance must be of very low value of inductance at high frequencies.

   Note that each of the analog input pins are divided in this manner with these resistances. Connect the driving amplifier as close as possible to the A/D input of the ADC-304.
4. The voltage between V_{RT} (pin 18) and V_{RB} (pin 26) is equivalent to the dynamic range of the analog input. Bypass V_{RB} to ANA GND (pins 19 and 25) by means of a 1 μF and 0.01 μF capacitor in parallel. To balance the characteristics of the ADC-304 at high frequencies, bypass V_{RM} (pin 27) with a 0.01μF capacitor to ANA GND (pins 19 and 25).

   Also, V_{RM} (pin 27) can be used as a trimming pin for more precise linearity compensation. A stable voltage source with a potential equal to −FSR and a 1 KΩ potentiometer can be connected to V_{RM} (pin 27) as shown in Figure 3 for this purpose.
5. Separate the clock input, CLK (pin 17), from other leads as much as possible, observing proper EMI and RFI wiring techniques. This will reduce the inductive pick-up of this lead from interfering with the "clean" operation of the ADC-304.

Performance	MIN.	TYP.	MAX.	UNITS
Conversion Rate[4]	20	-	-	MHz
Non-Linearity	-	-	±1/2	LSB
Differential Non-Linearity	-	-	±1/2	LSB
Differential Gain Error[5]	-	-	1.5	%
Differential Phase Error[5]	-	-	0.5	Degrees
Aperture Delay	5	7	9	nSec.
Aperture Jitter	-	30	-	pSec.
Clock pulse width: Tpw1	35	-	-	nSec.
Tpw0	10	-	-	nSec.
Reference				
Reference Pin Current	-	15	18	mA
Reference Resistance (VRT to VRB)	-	130	-	ohms
Reference Input (Dual Supply)				
(VRT)	−0.1	0	+0.1	V
(VRB)	−1.8	−2.0	−2.2	V
Power Supply Requirements				
Single Power Supply				
Supply voltage				
(VCC)	4.75	-	5.25	V
(VEE)	-	0	-	V
Supply Current:				
(ICC + IEE)	-	71	88	mA
Power Dissipation	-	360	442	mW
Dual Power Supply				
Supply Voltage:				
(VCC)	4.75	5.0	5.25	V
(VEE)	−4.75	−5.2	−5.5	V
Supply Current				
(ICC)	-	10	14	mA
(IEE)	-	62	75	mA
Power Dissipation	-	390	440	mW
Physical/Environmental				
Operating Temperature	−20	-	+75	°C
Storage Temperature	−55	-	+150	°C

Footnotes:

1. Vin = 4V + 0.07 VRMS for single power supply
   Vin = −1V + 0.07 VRMS for dual power supply
2. Vin = 4V for single power supply
   Vin = −1V for dual power supply
3. Logic "1" = 2.7V
   Logic "0" = 0.5V
4. fin = 1 KHz, ramp
5. NTSC 40 IRE-modulated ramp, Fc = 14.3 MSPS

TECHNICAL NOTES (CONT.)

6. The analog input signal is sampled on the positive-going edge of CLK. Corresponding digital data appears at the output on the negative-going edge of the CLK pulse after a small delay of 35 nSec. maximum (TDLH, TDHL). Refer to the Timing diagram, Figure 4, for more information.
7. Connect all free pins to ANA GND (pins 19 and 25) to reduce unwanted noise.

   The analog input range is equal to a 2V spread. The voltage on VRT-VRB will equal 2V. The connection of VRT and ANA GND is 2V higher than VRB. Whether using a single or dual power supply, the analog input will range from the value of VRT to VRB. If VRT equals +5V, then VRB will equal +3V and the analog input range will be from +5 to +3V.

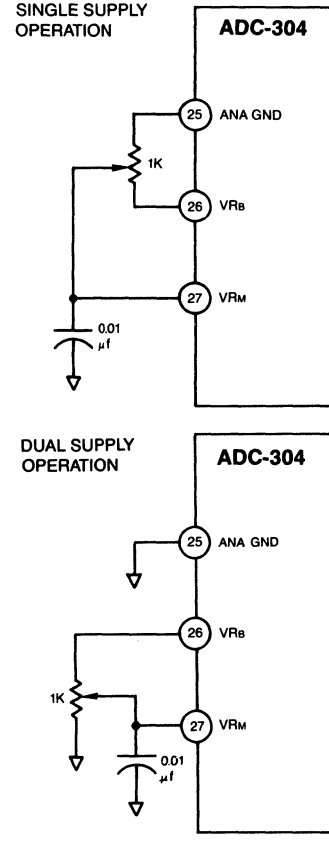


Figure 3: Improving Linearity Compensation

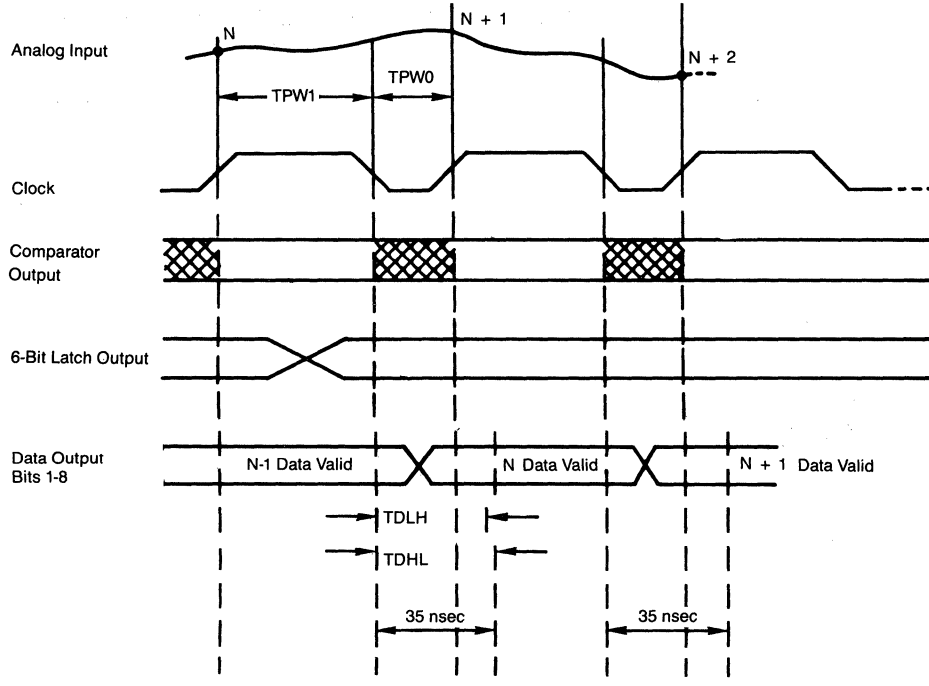


Figure 4: ADC-304 Timing Diagram

THEORY OF OPERATION

The ADC-304 consists of 4 sections: the resistor string, the comparator latches, the encoder, and the latchable output buffer. Refer to the block diagram (Figure 1) and timing diagram (Figure 4) as needed.

The reference resistor string consists of 256 equal value resistors with 256 internal taps and 3 external taps. The external taps are represented as V_{RT}, V_{RB} and V_{RM}. V_{RT} is the top of the resistor string, V_{RM} is the mid point of the resistor string and V_{RB} is the bottom of the resistor string. V_{RM} can be used as a trimming pin for an improved linearity specification. See Figure 3 for more information.

The 256 internal taps feed 256 comparator inputs. The reference voltage is applied to the +(positive) input side of the 256 clocked comparators. The analog input is applied to the – (negative) input of the comparators. The comparator section consists of 256 comparators which compare the analog input signal to the voltage at the reference ladder's resistor taps for each comparator. All the comparators' clock (CLK) inputs are tied together so they are clocked simultaneously.

The comparison between the reference ladder taps and input voltage is made on the positive going edge of the clock. The latched comparator output then goes to the Latch/256-to-24 bit encoder. Each of the four groups of 64 comparators are encoded once into 6-bit data. The four 6-bit data groups are then encoded to the 8-bit output data word. This latch is enabled when CLK is high and the latched comparator outputs proceed through the 256-to-24-bit encoder, the 24-bit-to-8-bit encoder, and the Exclusive-OR gates to the input of the output latch. The output latch, with the clock in a high state, has the previous conversion latched. The clock is required to be high for a minimum of 35 nSec.

Upon the clock going low, the latch shown on the block diagram with the 256 to 24 bit encoder is latched. This allows the comparators to be in the sampling mode in preparation for the next conversion. The now latched and encoded data word proceeds into the output latch which became enabled with the clock going low (10 nSec. minimum required). The data will be ready at the output 35 nSec. maximum after the negative edge of the clock.

Output coding of Binary, Complementary Binary, and if external offset circuitry is used, Offset Binary, Two's Complement and Complementary Two's Complement is selectable using the MINV and LINV pins. The most significant bit is Exclusive OR-ed with an external pin labeled MINV.

This pin allows for inversion of the MSB, simply by applying the correct logic level to MINV. The remaining 7 bits are exclusive OR-ed with an external pin labeled LINV. This pin allows for inversion of the 7 LSB's, by applying the correct logic to LINV. Both MINV and LINV have TTL-compatible inputs. Refer to Tables 2 and 3 for appropriate connections.

APPLICATION CIRCUITS

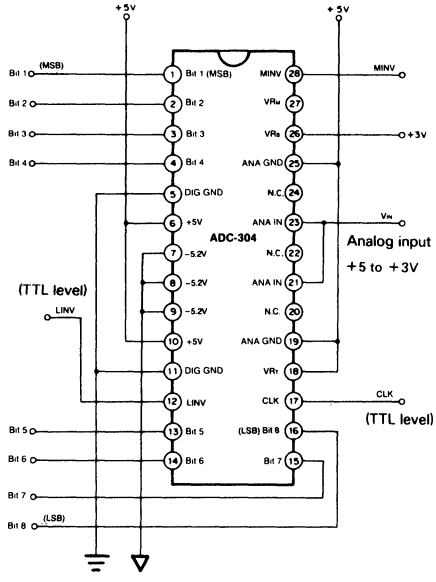


Figure 5: Connections for +5V Power Supply Operation

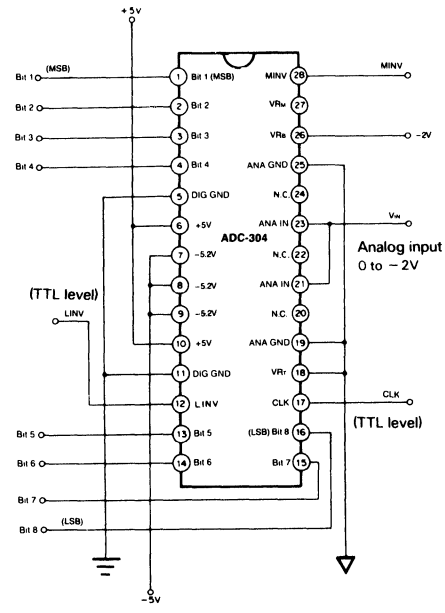


Figure 6: Connections for ±5V Power Supply Operation

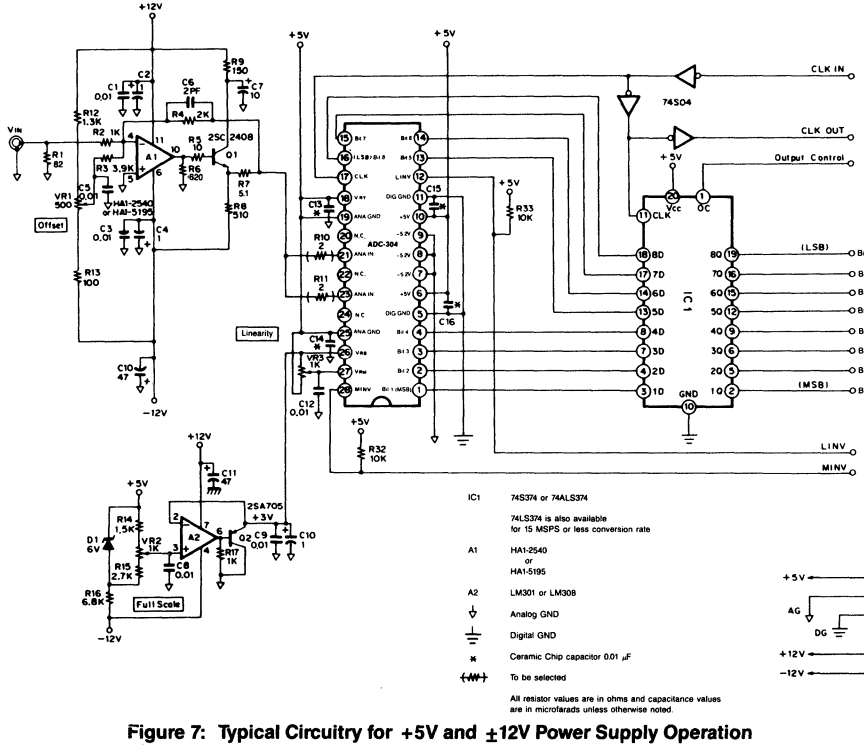


Figure 7: Typical Circuitry for +5V and ±12V Power Supply Operation

Table 2. Output Coding for +5V Power Supply Operation (+5 to +3V Signal Input)

		Straight Binary	Complement 2's Complement	2's Complement	Complement Binary
Unipolar Scale	MINV	0	0	1	1
	LINV	0	1	0	1
+FS – 1 LSB	+4.9922V	11111111	10000000	01111111	00000000
+7/8 FS	+4.7500V	11011111	10100000	01011111	00100000
+3/4 FS	+4.5000V	10111111	11000000	00111111	01000000
+1/2 FS	+4.0000V	01111111	00000000	11111111	10000000
+1/4 FS	+3.5000V	00111111	01000000	10111111	11000000
+1/8 FS	+3.2500V	00011111	00100000	11011111	11100000
+1 LSB	+3.0078V	00000001	01111110	10000001	11111110
Zero	+3.0000V	00000000	01111111	10000000	11111111

Table 3. Output Coding for ±5V Power Supply Operation (0 to –2V Signal Input)

		Straight Binary	Complement 2's Complement	2's Complement	Complement Binary
Unipolar Scale	Min. V	0	0	1	1
	Lin. V	0	1	0	1
0	0V	11111111	10000000	01111111	00000000
– 1 LSB	– 7.813 mV	11111110	10000001	01111110	00000000
– 1/8 FS	– 250.00 mV	11011111	10100000	01011111	00100000
– 1/4 FS	– 500.00 mV	10111111	11000000	00111111	01000000
– 1/2 FS	– 1.0V	01111111	00000000	11111111	10000000
– 3/4 FS	– 1.5V	00111111	01000000	10111111	11000000
– 7/8 FS	– 1.75V	00011111	00100000	11011111	11100000
– FS + 1 LSB	– 1.9922V	00000000	01111111	10000000	11111111

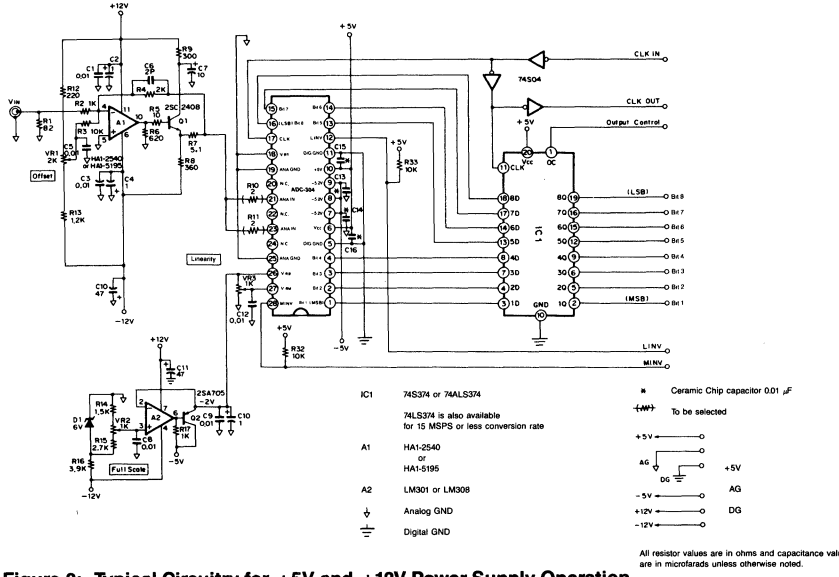


Figure 8: Typical Circuitry for ±5V and ±12V Power Supply Operation

ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-304	8-bit, 20 MHZ, Low-power, flash A/D
	For higher reliability versions, contact the factory

ADC-310
10-Bit Video A/D Converter

1

FEATURES

- **10-Bit resolution**
- **20 MHz conversion rate**
- **Very low power 360 mW**
- **Buffered output**
- **ECL-compatible**
- **Input bandwidth 10 MHz**

GENERAL DESCRIPTION

The ADC-310 is a bipolar monolithic 10-bit video analog to digital converter capable of digitizing analog input signals at conversion rates up to 20 MHz minimum with a typical power consumption of only 360 mW.

A serial/parallel technique is used to obtain the high conversion speed using dual power source of +1.6 volts and -5.0 volts.

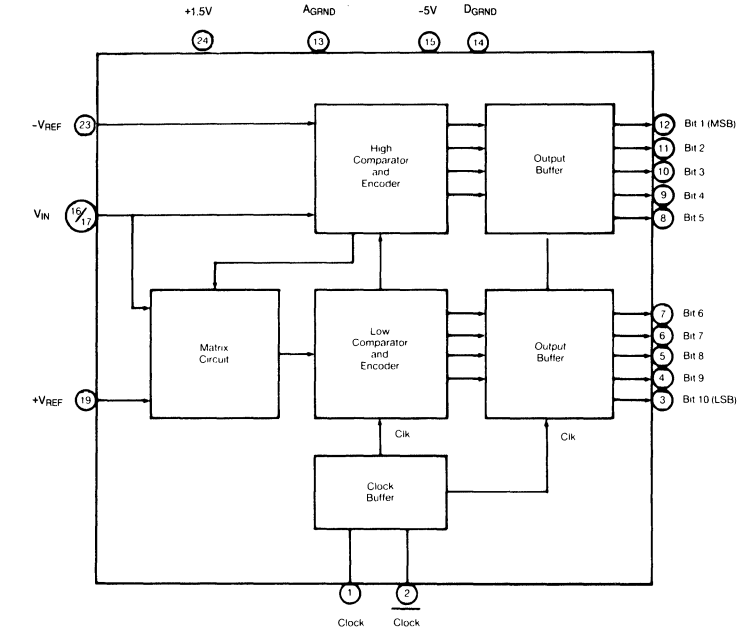
The analog input range, with -2V reference, is 0V to -2V and digital inputs and outputs are ECL compatible with outputs buffered.

The converter is designed to operate with an external sample and hold (SHM-40, or similar) together with external clock and reference source.

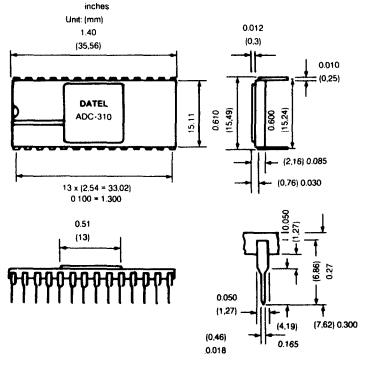
The ADC-310 is packaged in a 28 pin DIP and operates over temperature range -20°C to +75°C.

APPLICATIONS

- **High speed data acquisition**
- **Radar pulse analysis**
- **TV video encoding**
- **High energy physics**
- **Transient analysis**
- **Medical electronics**
- **Fluid flow analysis**
- **Sonar systems**



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CLK INPUT	28	INTERNAL CONNECTION – LEAVE OPEN
2	$\overline{\text{CLK INPUT}}$	27	INTERNAL CONNECTION – LEAVE OPEN
3	BIT 10 (LSB)	26	INTERNAL CONNECTION – LEAVE OPEN
4	BIT 9	25	INTERNAL CONNECTION – LEAVE OPEN
5	BIT 8	24	+1.5 VOLT SUPPLY
6	BIT 7	23	-2.0 VOLT REFERENCE SUPPLY
7	BIT 6	22	VREF ADJUST 3
8	BIT 5	21	VREF ADJUST 2
9	BIT 4	20	VREF ADJUST 1
10	BIT 3	19	0 VOLT REFERENCE SUPPLY
11	BIT 2	18	INTERNAL CONNECTION – LEAVE OPEN
12	BIT 1 (MSB)	17	ANALOG INPUT
13	ANALOG GROUND	16	ANALOG INPUT
14	DIGITAL GROUND	15	-5.2 VOLT POWER SUPPLY

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage V_S	0 to -7.0V
Supply Voltage V_{CC}	0 to +2.5V
Analog Input Voltage	V_S to 0.3V
Reference Voltage	V_S to 0.3V
Digital Output Current	0 to -20 mA
Power Dissipation	1.23 Watts
Storage Temperature	-55°C to +150°C
Operating Temperature	-20°C to +75°C

FUNCTIONAL SPECIFICATIONS.

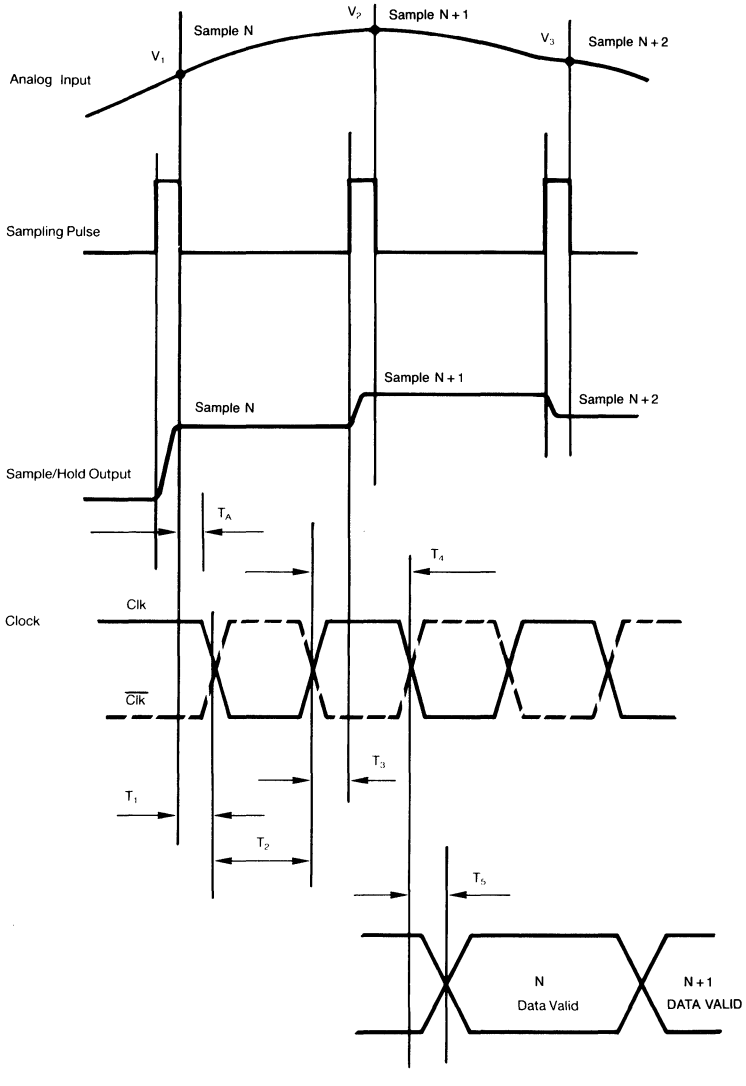
Typical at +25°C, V_S = -5.2 V dc, Vcc = +1.6, Vref = -2.0 V dc unless otherwise stated.

PERFORMANCE				
Resolution		10 Bits		
Conversion Rate (Min)		20 MHz		
Integral Non-Linearity		±1.75 LSB		
Differential Non-Linearity		±1.75 LSB		
Input Bandwidth		10 MHz		
INPUTS	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Input Voltage	0	—	-2.0	V
Input Bias Current	—	40	80	μA
Input Capacitance	—	230	—	ρF
REFERENCE				
Current	—	-12.5	-14	mA
VR1	-0.49	-0.5	-0.51	V
VR2	-0.99	-1.0	V	
VR3	-1.49	-1.5	-1.51	V
VREF	-1.90	-2.0	-2.10	V
CLOCK				
Bias Current	—	5	8	μA
OUTPUT				
Digital (high)	-0.9	—	—	V
Digital (low)	—	—	-1.5	V
POWER				
-5.0V ±0.25V	—	55	80	mA
+1.6V to 2.1	—	17	25	mA

TECHNICAL NOTES

1. Analog input signals must be 'held' by an external sample/hold e.g. DATEL SHM-40, with careful attention being paid to the timing relationship between the sample/hold transition of the sample/hold amplifier and the positive transition of the clock pulse — see timing diagram.
2. Analog input, pins 16 and 17, must be linked externally. The input bias current is 15 μA typical.
3. The -2.0 volt reference voltage is connected between pins 23 (-2V) and pin 19 (analog ground). The 'R' value between pins 19 and 23 is 200 Ohms (typical).
4. The reference input should be decoupled using 0.1 μF capacitor located as close as possible to pin 23. It is also recommended that the external connections to the resistor network, pins 20, 21 and 22, are also decoupled using 0.1 μF capacitors whether they are used or not.
5. For most applications, the ADC-310 accuracy will be more than sufficient. However, it is possible that some improvement may be achieved at the ¼ 'full-scale', ½ 'full-scale', and the ¾ 'full-scale' points by connecting external resistors from pins 20, 21, and 22 to analog ground pin 19, or to VREF (pin 23).
6. The printed circuit board should be laid out to have substantial analog and digital ground planes. The planes should be connected at one point only — usually power common and as close to the source as possible.
7. Internal pull down resistors (10K Ohms typ.) to the digital output terminals are provided. However, to boost the transition, external resistors greater than 3K Ohms can be added.
8. An external complementary ECL signal source is required to drive the clock input terminals pins 1 and 2.
9. The -5.0V power supply and +1.6V power should be decoupled using 3.3 uF tantalum and 0.022 uF ceramic capacitors. Mount these components as close as possible to pins 15 and 24.
10. Under no circumstances must external circuits be connected to pin 18 and pins 25 to 28. These five terminals must be left open circuit.

TIMING DIAGRAM



TIMING DIAGRAM NOTES

1. The timing must be set such that the negative transition of the clock (clk) occurs time T_1 after the sample pulse, and the time T_1 being greater than sample/hold aperture delay and settling time

$$T_1 > TA$$

2. The first half cycle of clock must not be less than 22 nsec.

$$T_2 \geq 22 \text{ nsec.}$$

3. The next sample/hold pulse must not occur less than 2 nsec. after the positive transition of the first half cycle of the clock.

$$T_3 \geqslant 2 \text{ nsec.}$$

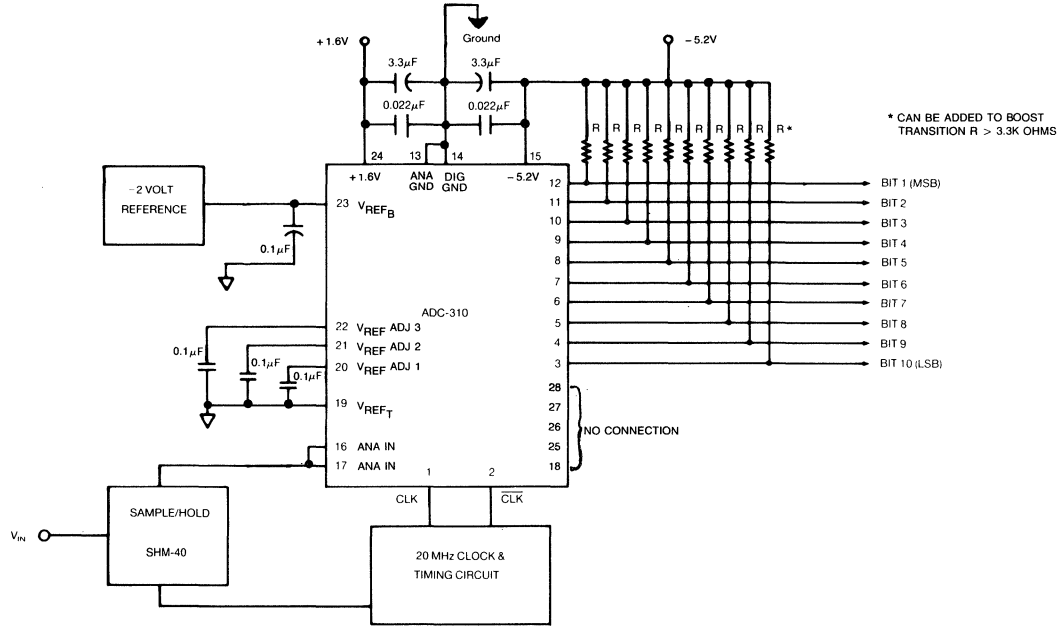
4. The second half cycle of the clock must not be less than 20 nsec.

$$T_4 \geqslant 20 \text{ nsec.}$$

5. Data becomes valid in not less than 15 nsec. after the first clock cycle.

$$T_5 \geqslant 15 \text{ nsec.}$$

CONNECTION AND APPLICATION



DIGITAL OUTPUT CODES

INPUT VOLTAGE		MSB					DIGITAL OUTPUT CODE				LSB
V_{REF_T}	0.0000V	1	1	1	1	1	1	1	1	1	1
	−0.0020V	1	1	1	1	1	1	1	1	1	0
	−0.9990V	1	0	0	0	0	0	0	0	0	0
	−1.0010V	0	1	1	1	1	1	1	1	1	1
	−1.9980V	0	0	0	0	0	0	0	0	0	1
V_{REF_B}	−2.0000V	0	0	0	0	0	0	0	0	0	0

ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
ADC-310	-20°C to + 75°C

NOTE: For units with high-reliability processing, contact DATEL.

ADC-500, ADC-505
12-Bit, Ultra-fast, Low-power A/D Converters

FEATURES

- **12-Bit resolution**
- **500 Nanosecond maximum conversion time**
- **Low-power, 1.6W**
- **Small initial errors**
- **Three-state output buffers**
- **−55°C to +125°C operation**
- **Small 32-pin DIP**

GENERAL DESCRIPTION

DATEL's ADC-500 and ADC-505 reflect the ultimate in state-of-the-art analog signal conversion technology. The ADC-500 boasts a remarkable conversion speed of 500 nanoseconds, along with a low-power consumption of 1.6 watts.

DATEL's ADC-500 and ADC-505 are 12-bit analog-to-digital converters which have small initial errors and can also provide adjustment capability for system errors. Both models have identical specifications except for conversion times. The ADC-505 has a maximum conversion time of 550 nanoseconds while the ultra-fast ADC-500 accomplishes a 12-bit conversion in less than or equal to 500 nanoseconds. Figure 1 is a simplified block diagram applicable to both devices.

Manufactured using thick-film and thin-film hybrid technology, these converters' remarkable performances are based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADC-500 and ADC-505 are packaged in a 32-pin ceramic DIP and consume 1.6 watts.

The ADC-500 and ADC-505 feature three pin-programmable input ranges: 0 to +10V, 0 to +20V, and ±10V dc. The input impedance is specified at 1.75K minimum for unipolar ranges and 3.75K minimum for the bipolar range, reducing stringent drive requirements. Other specifications include no missing codes over temperature, a maximum gain tempco of ±35 ppm/°C and a maximum differential linearity tempco of ±2.5 ppm/°C.

All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary by using the $\overline{\text{COMP}}$ $\overline{\text{BIN}}$ pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

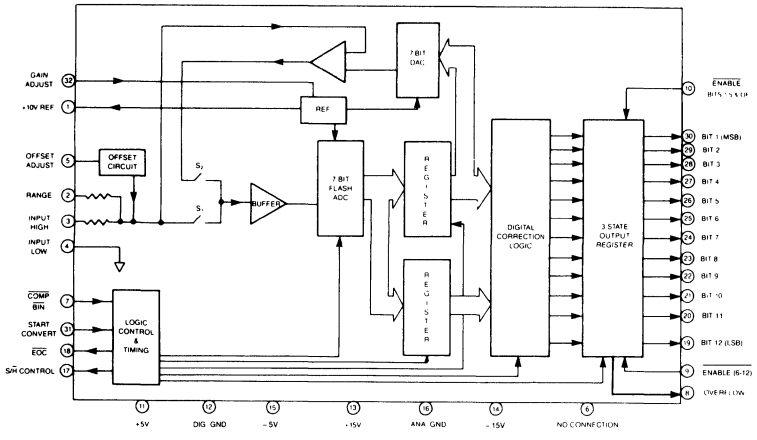
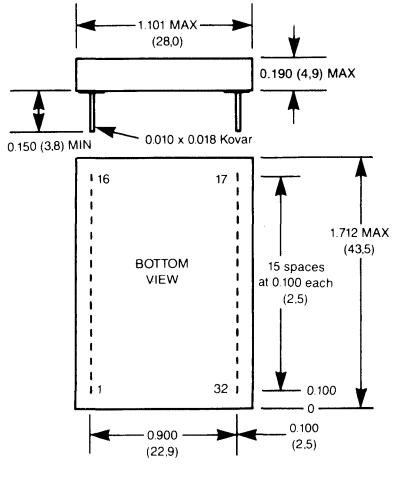


Figure 1. ADC-500, ADC-505 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have 0.025 inch, ±0.01 stand off from case

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF
2	RANGE
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST
6	NO CONNECTION
7	$\overline{\text{COMP BIN}}$
8	OVERFLOW
9	$\overline{\text{ENABLE (6-10)}}$
10	$\overline{\text{ENABLE (1-5, O.F)}}$
11	+5V
12	DIGITAL GROUND
13	+15V
14	−15V
15	−5V
16	ANALOG GROUND
17	$\overline{\text{S/H}}$ CONTROL
18	$\overline{\text{EOC}}$
19	BIT 12 (LSB)
20	BIT 11
21	BIT 10
22	BIT 9
23	BIT 8
24	BIT 7
25	BIT 6
26	BIT 5
27	BIT 4
28	BIT 3
29	BIT 2
30	BIT 1 (MSB)
31	START CONVERT
32	GAIN ADJUST

Another novel feature of the ADC-500 is the provision of a Sample/Hold control pin for applications where a sample-hold is used in conjunction with the ADC-500. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

Power required for both models is ±15V dc and ±5V dc. Models are available in the commercial 0°C to +70°C, and military −55°C to +125°C operating temperature range. Typical applications include spectrum, transient, vibration, and waveform analysis. These devices are also ideally suited for radar, sonar and video digitization, medical instrumentation, and high-speed data acquisition systems. For information on versions with high reliability screening, contact the factory.

ABSOLUTE MAXIMUM RATINGS

Parameters	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 13)	0	+18	Volts dc
−15V Supply (Pin 14)	0	−18	Volts dc
+5V Supply (Pin 11)	−0.5	+7	Volts dc
−5V Supply (Pin 15)	+0.5	−7	Volts dc
Digital Inputs (Pins 7, 9, 10 & 31)	−0.3	+6	Volts dc
Analog Input (Pin 3)	−15	+15	Volts dc
Lead temp. (10 sec)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Range	—	0 to +10	—	Volts dc
(See Tech. Note 9)	—	0 to +20	—	Volts dc
	—	±10	—	Volts dc
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	μA
Logic 0	—	—	−100	μA
OUTPUTS				
Output Coding:	straight binary/offset binary			
(Pin 7 High)	complementary binary			
(Pin 7 Low)	complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	μA
Logic 0	—	—	6.4	mA
Internal Reference:				
Voltage, +25°C	9.98	—	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
PERFORMANCE				
Integral Nonlinearity:				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
−55°C to +125°C	—	—	±0.0125	%FSR ±3 LSB
Integral Nonlin. Tempco.	—	±3	±8	ppm/°C
Differential Nonlinearity				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
−55°C to +125°C	—	—	±0.0125	%FSR ±1 LSB
Differential Nonlin. Tempco	—	—	±2.5	ppm/°C
Full-Scale Absol. Accuracy:				
+25°C	—	±3	±8	LSB
0°C to +70°C	—	±4	±14	LSB
−55°C to +125°C	—	±8	±29	LSB

PERFORMANCE (cont.)

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Unipolar Zero Error, +25°C	—	±1	±3	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Zero Error, +25°C	—	±1	±3	LSB
Bipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±5	LSB
Bipolar Offset Error Tempco	—	±17.5	±35	ppm/°C
Gain Error, +25°C	—	±2	±5	LSB
Gain Tempco	—	±17.5	±35	ppm/°C
Conversion Times:				
ADC-500				
+25°C	—	—	500	nsec.
0°C to +70°C	—	—	540	nsec.
−55°C to +125°C			560	nsec.
ADC-505				
+25°C	—	—	550	nsec.
0°C to +70°C	—	—	590	nsec.
−55°C to +125°C	—	—	620	nsec.
No Missing Codes (12 Bits)	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current:				
+15V Supply	—	+23	+30	mA
−15V Supply	—	−11	−15	mA
+5V Supply*	—	+55	+90	mA
−5V Supply	—	−175	−210	mA
Power Dissipation	—	1.6	1.8	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range:				
−BMC	0	—	+70	°C
−BMM	−55	—	+125	°C
Storage Temperature Range	−65	—	+150	°C
Package Type	32-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12) grams			

* +5V power usage at 1TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).
2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 μF, 25V tantalum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16). The −5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.
4. Obtain straight binary/offset binary output coding by tieing $\overline{\text{COMP BIN}}$ (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.
5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 ($\overline{\text{Enable}}$ bits 1–5 & O.F.).
6. The Sample/$\overline{\text{Hold}}$ control signal, pin 17, goes low following the rising edge of a START CONVERT pulse and high 30 nanoseconds minimum before $\overline{\text{EOC}}$ goes low. This indicates that the converter can accept a new analog input.
7. The drive requirements of the ADC-500/505 may be satisfied with a wide-bandwidth, low output impedance input source. Applications of these converters that require the use of a sample-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.
8. Over temperature, input capacitance is 50 pF maximum and input impedance is 1.75K minimum (2.5K typical) for unipolar and 3.75K minimum (5K typical) for bipolar. These values are guaranteed by design.
9. Requirements for ±2.5V inputs can be satisfied using DATEL's AM-1435 amplifier in front of the SHM-45/ADC-500 configuration, shown in Figure 4, at the appropriate gain. The SHM-45's gain of 2 mode allows 0 to +5V or ±5V input ranges.

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

TABLE 1. SIGNAL TIMING SUMMARY

LINE	DURATION IN NANOSECONDS
Start Convert (A/D)	50 nsec. minimum
Analog Input Settling Time	150 nsec. minimum
Start Convert Low to $\overline{\text{EOC}}$ High Propagation Delay	35 nsec. maximum
Start Convert Low to Previous Output Data Invalid	350 nsec. minimum
Data Valid Before $\overline{\text{EOC}}$ Goes Low	25 nsec. minimum
$\overline{\text{Enable}}$ to Output Data Valid Propagation Delay	10 nsec. maximum

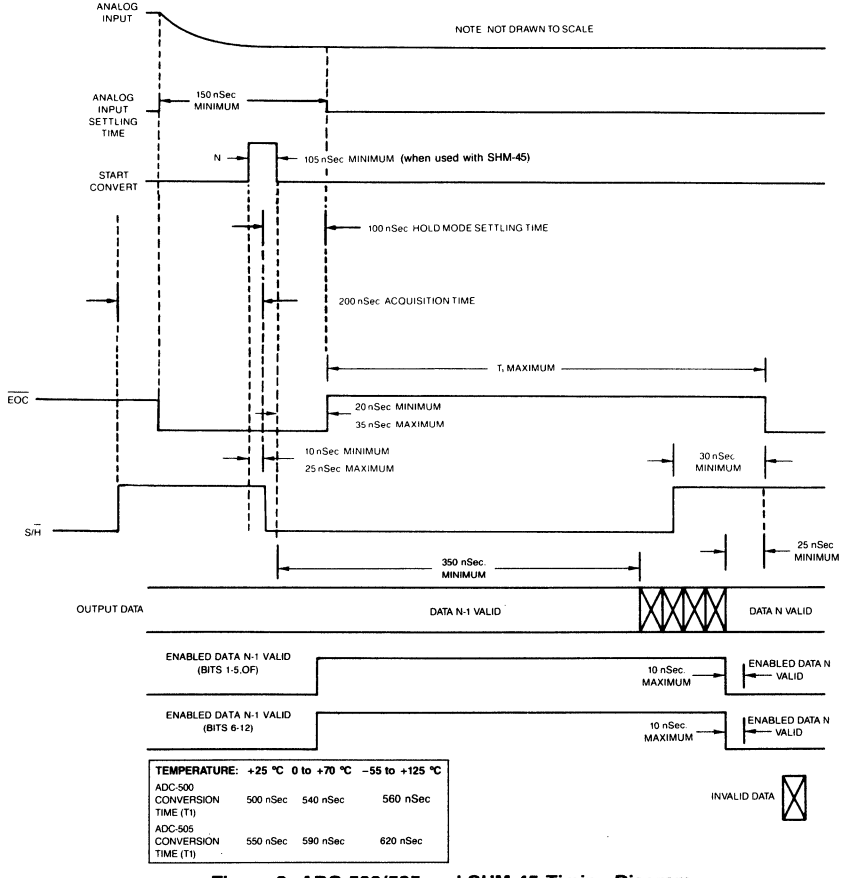


Figure 2. ADC-500/505 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 kHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ ½ LSB) or the bipolar zero adjustment (zero + ½ LSB) for the appropriate FSR. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the $\overline{\text{COMP BIN}}$ (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with the $\overline{\text{COMP BIN}}$ tied low.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with $\overline{\text{COMP BIN}}$ tied high or between 0111 1111 1111 and 0111 1111 1110 with $\overline{\text{COMP BIN}}$ tied low.
3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+ FS − 1½ LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for $\overline{\text{COMP BIN}}$ (pin 7) tied high or between 0000 0000 0001 and 0000 0000 0000 for $\overline{\text{COMP BIN}}$ tied low.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

TABLE 2. INPUT CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to + 10V dc	3	3
0 to + 20V dc	3	16
± 10V dc	3	1

TABLE 3a. ZERO AND GAIN ADJUST FOR UNIPOLAR USE

UNIPOLAR FSR	ZERO ADJUST + ½ LSB	GAIN ADJUST + FS − 1½ LSB
0 to + 10V dc	+ 1.22 mV	+ 9.9963V dc
0 to + 20V dc	+ 2.44 mV	+ 19.9927V dc

TABLE 3b. ZERO AND GAIN ADJUST FOR BIPOLAR USE

BIPOLAR FSR	ZERO ADJUST ZERO + ½ LSB	GAIN ADJUST + FS − 1½ LSB
± 10V dc	+ 2.44 mV	+ 9.9927V dc

TABLE 4. OUTPUT CODING FOR UNIPOLAR OPERATION

UNIPOLAR SCALE	INPUT RANGES, VOLTS dc		OUTPUT CODING					
			STRAIGHT BINARY			COMP. BINARY		
	0 to + 10V	0 to + 20V	MSB		LSB	MSB		LSB
+ FS − 1 LSB	+ 9.9976V	+ 19.9951V	1111	1111	1111	0000	0000	0000
⅞ FS	+ 8.7500V	+ 17.500V	1110	0000	0000	0001	1111	1111
¾ FS	+ 7.5000V	+ 15.000V	1100	0000	0000	0011	1111	1111
½ FS	+ 5.0000V	+ 10.000V	1000	0000	0000	0111	1111	1111
¼ FS	+ 2.5000V	+ 5.0000V	0100	0000	0000	1011	1111	1111
⅛ FS	+ 1.2500V	+ 2.5000V	0010	0000	0000	1101	1111	1111
1 LSB	+ 0.0024V	+ 0.0049V	0000	0000	0001	1111	1111	1110
0	0.0000V	0.0000V	0000	0000	0000	1111	1111	1111

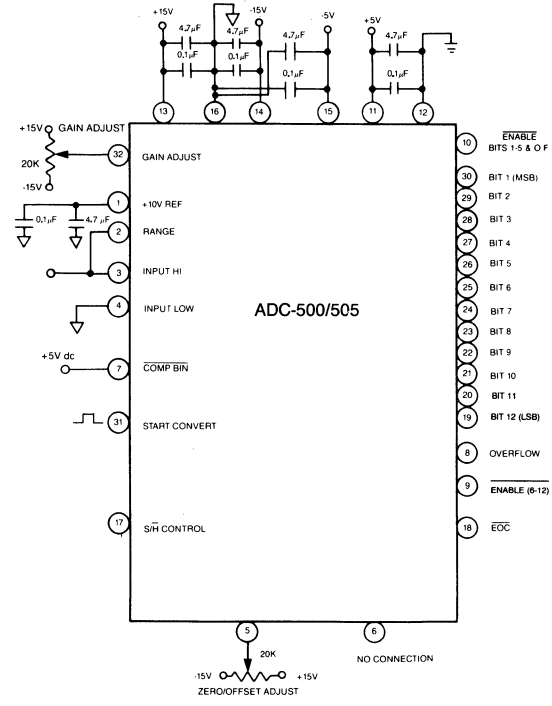


Figure 3. ADC-500/505 Calibration Circuit

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TABLE 5. OUTPUT CODING FOR BIPOLAR OPERATION

BIPOLAR SCALE	INPUT RANGE	OUTPUT CODING					
		OFFSET BINARY			COMP. OFFSET BINARY		
	±10V dc	MSB		LSB	MSB		LSB
+FS −1 LSB	+9.9951V	1111	1111	1111	0000	0000	0000
+¾ FS	+7.5000V	1110	0000	0000	0001	1111	1111
+½ FS	+5.0000V	1100	0000	0000	0011	1111	1111
0	0.0000V	1000	0000	0000	0111	1111	1111
−½ FS	−5.0000V	0100	0000	0000	1011	1111	1111
−¾ FS	−7.5000V	0010	0000	0000	1101	1111	1111
−FS +1 LSB	−9.9951V	0000	0000	0001	1111	1111	1110
−FS	−10.000V	0000	0000	0000	1111	1111	1111

THEORY OF OPERATION (ADC-500 AND SHM-45)

This theory of operation describes the ADC-500's operation in conjunction with DATEL's SHM-45. The SHM-45 sample-and-hold device captures fast signals for an ADC-500 to then digitize. Figure 4 shows a typical ADC-SHM circuit. The ADC-500 employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the ADC-SHM connection diagram, the ADC block diagram, and the timing diagram as needed (Figures 4, 1 and 2 respectively).

The SHM-45, upon acquiring the input signal on the hold capacitor (200 nanoseconds maximum acquisition time to 0.01%), is put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-500 requires a maximum of 150 nanoseconds for the input signal to settle before starting a conversion. The input of the ADC-500 starts settling to its final value while the SHM-45 is in the acquisition mode.

At the end of the SHM-45's hold mode settling time, the ADC-500's input is fully settled. The missing 50 nanoseconds of the required maximum analog input settling time is made up by the time the Sample/$\overline{\text{Hold}}$ is in the acquisition mode. the end of the SHM-45's hold mode settling time, the ADC-500's input is fully settled.

The SHM-45 is in the sample mode when the ADC-500's S/$\overline{\text{H}}$ control (Pin 17) is high. The S/$\overline{\text{H}}$ control pin is high and thus in the sample mode when the A/D is not performing a conversion.

The S/$\overline{\text{H}}$ control pin goes low after the rising edge of the START CONVERT pulse a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. To assure the SHM has 200 nanoseconds maximum acquisition time, the START CONVERT pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the START CONVERT pulse should be 105 nanoseconds minimum to assure the hold mode settling time of 100 nanoseconds is observed. The 105 nanoseconds takes into account the min-max propagation delays of the START CONVERT high to S/$\overline{\text{H}}$ control low propagation delays and the START CONVERT low to $\overline{\text{EOC}}$ high propagation delays.

Conversion being initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate range (± 10V range shown), is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

The first pass finished, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{\text{EOC}}$ goes low, indicating the conversion is complete, and the output passes to three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{\text{EOC}}$ going low). The Sample/$\overline{\text{Hold}}$ control pin goes high a minimum of 30 nanoseconds before $\overline{\text{EOC}}$ goes low, indicating that the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{\text{EOC}}$ goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput using the ADC-500 and the SHM-45 consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds for observance of min-max propagation delays and 470 nanoseconds for the conversion process (S/$\overline{\text{H}}$ control pin saves 30 nanoseconds). Total throughput is a maximum of 785 nanoseconds for the system for a guaranteed throughput rate of 1.25 MHz.

The ADC-500's conversion rate without a sample-hold would be 150 nanoseconds for input settling time and 500 nanoseconds for the ADC-500, yielding a minimum of 1.5 MHz conversion rate. Retriggering of the start convert pulse before $\overline{\text{EOC}}$ goes low will not initiate a new conversion.

The performance characteristics shown in Table 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These charateristics are guaranteed by design.

TABLE 6. PERFORMANCE CHARACTERISTICS AT DIFFERENT TEMPERATURES

CHARACTERISTIC	VALUE
Conversion Rate (Changing Inputs):	
ADC-500	
+25°C	1.5 MHz minimum
0°C to +70°C	1.4 MHz minimum
−55°C to +125°C	1.4 MHz minimum
ADC-505	
+25°C	1.39 MHz minimum
0°C to +70°C	1.35 MHz minimum
−55°C to +125°C	1.29 MHz minimum
Harmonic Distortion (Below FS):	
+25°C	−72 dB minimum
0°C to +70°C	−72 dB minimum
−55°C to +125°C	−65 dB minimum

To fully utilize the dynamic range of the ADC-500 and ADC-505, the SHM-45 can be hardware-programmed to provide the appropriate output voltage range. Table 7 shows the different input ranges which can be obtained by selecting the appropriate SHM-45. See the SHM-45 data sheet for connection details.

TABLE 7. ADC-SHM INPUT RANGES

V_{IN} Range	Gain
0 to +10	+1
0 to −10	−1
−5 to +5	−2
−10 to +10	−1
0 to −20	−0.5
0 to −5	−2

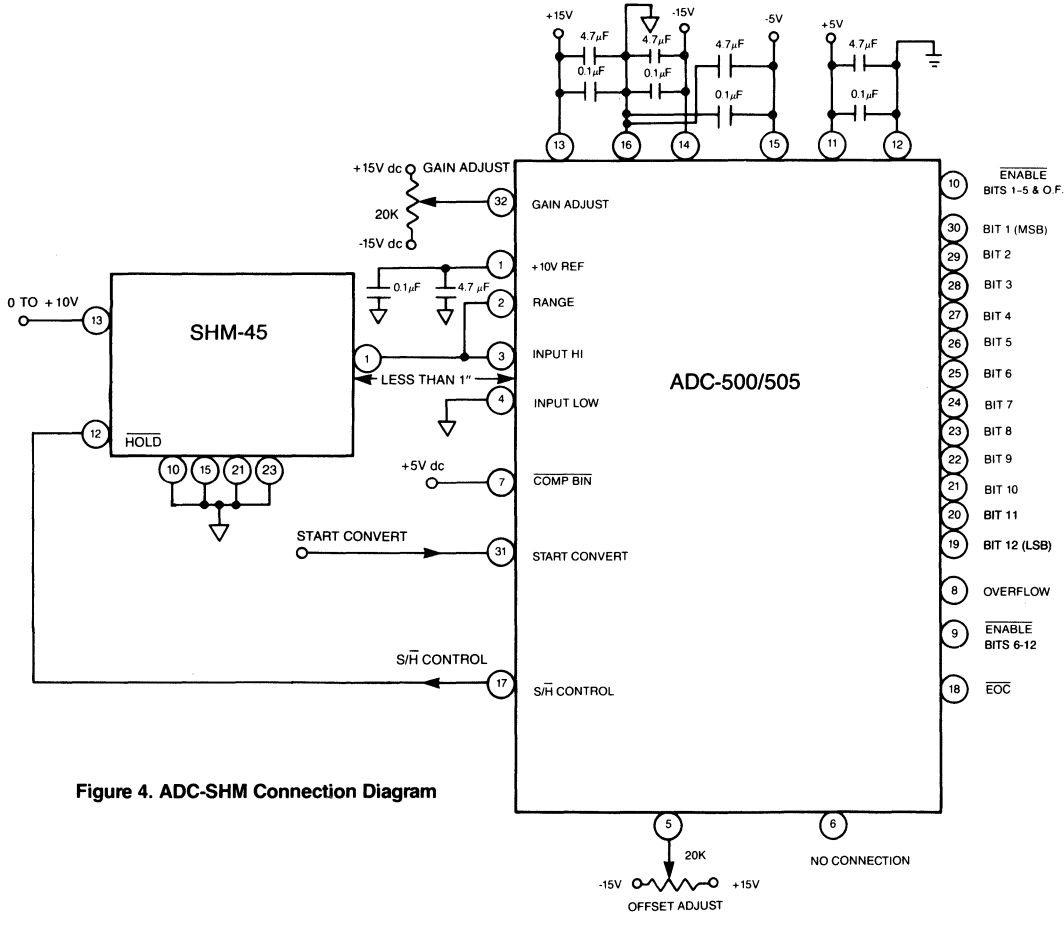


Figure 4. ADC-SHM Connection Diagram

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
ADC-500-BMC	0°C to +70°C	Hermetic
ADC-500-BMM	−55°C to +125°C	Hermetic
ADC-505-BMC	0°C to +70°C	Hermetic
ADC-505-BMM	−55°C to +125°C	Hermetic

ACCESSORIES

Part Number	Description
TP20K	Trimming Potentiometers: (Two required).

Receptable for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For high reliability version of the ADC-500 and ADC-505, contact DATEL.

ADC-508
12-Bit, Ultra-fast, Low-power A/D Converter

FEATURES

- **12-Bit resolution**
- **700 Nanosecond maximum conversion time**
- **Low-power, 1.6W**
- **Small initial errors**
- **Three-state output buffers**
- **−55°C to +125°C operation**
- **Small 32-pin DIP**

GENERAL DESCRIPTION

DATEL's ADC-508 reflects the ultimate in state-of-the-art analog signal conversion technology. The ADC-508 boasts a conversion speed of 700 nanoseconds, along with a low-power consumption of 1.6 watts.

DATEL's ADC-508 is a 12-bit, analog-to-digital converter which has small initial errors and can also provide adjustment capability for system errors. The ADC-508 has a maximum conversion time of 700 nanoseconds. Figure 1 is a simplified block diagram.

Manufactured using thick-film and thin-film hybrid technology, this converter's remarkable performance is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADC-508 is packaged in a 32-pin ceramic DIP and consumes 1.6 watts.

The ADC-508 features three pin-programmable input ranges: 0 to +10V, 0 to +20V, and ±10V dc. The input impedance is specified at 1.75K minimum for unipolar ranges and 3.75K minimum for the bipolar range, reducing stringent drive requirements. Other specifications include no missing codes over temperature, a maximum gain tempco of ±35 ppm/°C and a maximum differential linearity tempco of ±2.5 ppm/°C.

All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary by using the COMP BIN pin, An overflow pin indicates when inputs are below or above the normal full-scale range.

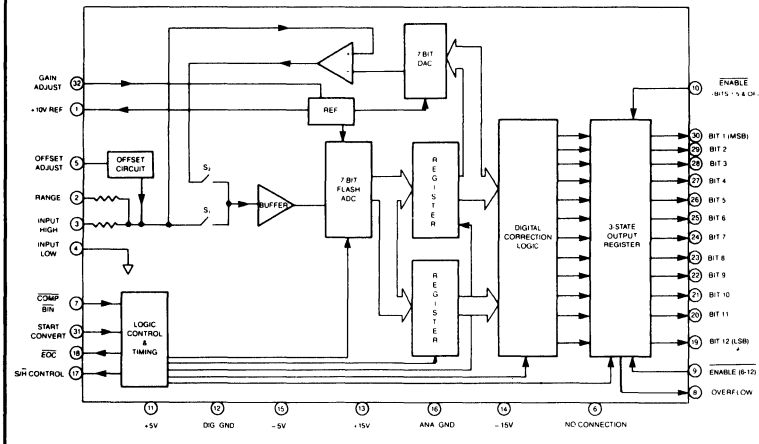
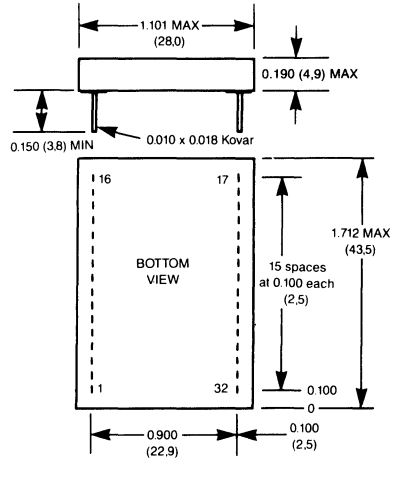


Figure 1. ADC-508 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have 0.025 inch, ±0.01 stand off from case

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF
2	RANGE
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST
6	NO CONNECTION
7	COMP BIN
8	OVERFLOW
9	ENABLE (6-12)
10	ENABLE (1-5, O.F.)
11	+5V
12	DIGITAL GROUND
13	+15V
14	−15V
15	−5V
16	ANALOG GROUND
17	S/H CONTROL
18	EOC
19	BIT 12 (LSB)
20	BIT 11
21	BIT 10
22	BIT 9
23	BIT 8
24	BIT 7
25	BIT 6
26	BIT 5
27	BIT 4
28	BIT 3
29	BIT 2
30	BIT 1 (MSB)
31	START CONVERT
32	GAIN ADJUST

3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 μF, 25V tantalum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16). The −5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.
4. Obtain straight binary/offset binary output coding by tieing COMP BIN (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.
5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 ($\overline{\text{Enable}}$ bits 1–5 & O.F.).
6. The Sample/$\overline{\text{Hold}}$ control signal, pin 17, goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before $\overline{\text{EOC}}$ goes low. This indicates that the converter can accept a new analog input.
7. The drive requirements of the ADC-508 may be satisfied with a wide-bandwidth, low output impedance input source. Applications of these converters that require the use of a sample-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.
8. Over temperature, input capacitance is 50 pF maximum and input impedance is 1.75K minimum (2.5K typical) for unipolar and 3.75K minimum (5K typical) for bipolar. These values are guaranteed by design.
9. Requirements for ±2.5V inputs can be satisfied using DATEL's AM-1435 amplifier in front of the SHM-45/ADC-508 configuration, shown in Figure 4, at the appropriate gain. The SHM-45's gain of 2 mode allows 0 to +5V or ±5V input ranges.

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

TABLE 1. SIGNAL TIMING SUMMARY

LINE	DURATION IN NANOSECONDS
Start Convert (A/D)	50 nsec. minimum
Analog Input Settling Time	150 nsec. minimum
Start Convert Low to $\overline{\text{EOC}}$ High Propagation Delay	35 nsec. maximum
Start Convert Low to Previous Output Data Invalid	350 nsec. minimum
Data Valid Before $\overline{\text{EOC}}$ Goes Low	25 nsec. minimum
$\overline{\text{Enable}}$ to Output Data Valid Propagation Delay	10 nsec. maximum

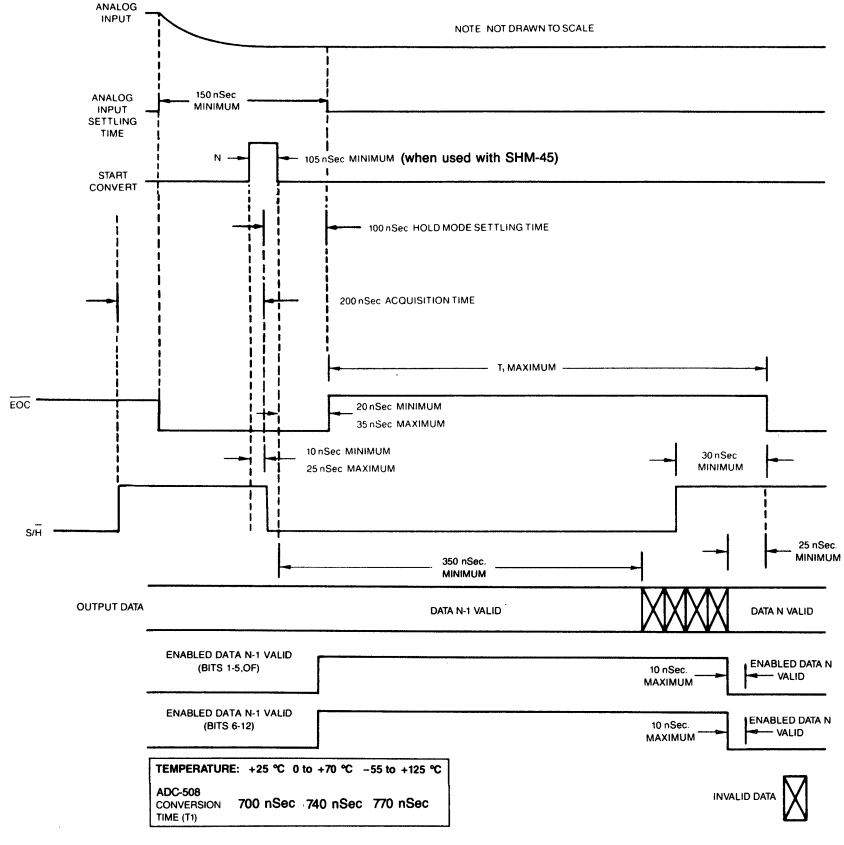


Figure 2. ADC-508 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 kHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ ½ LSB) or the bipolar zero adjustment (zero + ½ LSB) for the appropriate FSR. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN tied low.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low.
3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS − 1½ LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 7) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

TABLE 2. INPUT CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to +10V dc	3	3
0 to +20V dc	3	16
±10V dc	3	1

TABLE 3a. ZERO AND GAIN ADJUST FOR UNIPOLAR USE

UNIPOLAR FSR	ZERO ADJUST +½ LSB	GAIN ADJUST +FS −1½ LSB
0 to +10V dc	+1.22 mV	+9.9963V dc
0 to +20V dc	+2.44 mV	+19.9927V dc

TABLE 3b. ZERO AND GAIN ADJUST FOR BIPOLAR USE

BIPOLAR FSR	ZERO ADJUST ZERO +½ LSB	GAIN ADJUST +FS −1½ LSB
±10V dc	+2.44 mV	+9.9927V dc

TABLE 4. OUTPUT CODING FOR UNIPOLAR OPERATION

UNIPOLAR SCALE	INPUT RANGES, VOLTS dc		OUTPUT CODING							
			STRAIGHT BINARY				COMP. BINARY			
	0 to +10V	0 to +20V	MSB			LSB	MSB			LSB
+FS − LSB	+9.9976V	+19.9951V	1111	1111	1111		0000	0000	0000	
⅞ FS	+8.7500V	+17.500V	1110	0000	0000		0001	1111	1111	
¾ FS	+7.5000V	+15.000V	1100	0000	0000		0011	1111	1111	
½ FS	+5.0000V	+10.000V	1000	0000	0000		0111	1111	1111	
¼ FS	+2.5000V	+5.0000V	0100	0000	0000		1011	1111	1111	
⅛ FS	+1.2500V	+2.5000V	0010	0000	0000		1101	1111	1111	
1 LSB	+0.0024V	+0.0049V	0000	0000	0001		1111	1111	1110	
0	0.0000V	0.0000V	0000	0000	0000		1111	1111	1111	

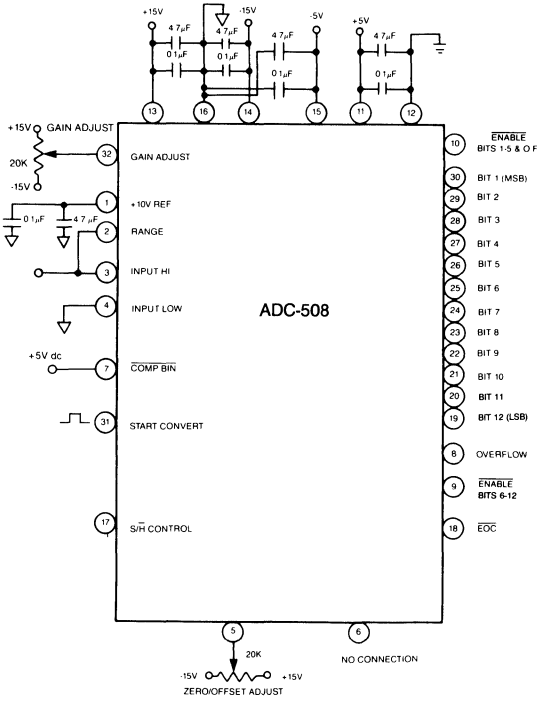


Figure 3. ADC-508 Calibration Circuit

Another novel feature of the ADC-508 is the provision of a Sample/Hold control pin for applications where a sample-hold is used in conjunction with the ADC-508. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

Power required is ±15V dc and ±5V dc. Models are available in the commercial 0°C to +70°C, and military −55°C to +125°C operating temperature range. Typical applications include spectrum, transient, vibration, and waveform analysis. These devices are also ideally suited for radar, sonar and video digitization, medical instrumentation, and high-speed data acquisition systems. For information on versions with high reliability screening, contact the factory.

ABSOLUTE MAXIMUM RATINGS Parameters	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 13)	0	+18	Volts dc
−15V Supply (Pin 14)	0	−18	Volts dc
+5V Supply (Pin 11)	−0.5	+7	Volts dc
−5V Supply (Pin 15)	+0.5	−7	Volts dc
Digital Inputs (Pins 7, 9, 10 & 31)	−0.3	+6	Volts dc
Analog Input (Pin 3)	−15	+15	Volts dc
Lead temp. (10 sec)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Range	—	0 to +10	—	Volts dc
(See Tech. Note 9)	—	0 to +20	—	Volts dc
	—	±10	—	Volts dc
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	μA
Logic 0	—	—	−100	μA
OUTPUTS				
Output Coding: (Pin 7 High)	straight binary/offset binary			
(Pin 7 Low)	complementary binary complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	μA
Logic 0	—	—	6.4	mA
Internal Reference:				
Voltage, +25°C	9.98	—	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
PERFORMANCE				
Integral Nonlinearity:				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
−55°C to +125°C	—	—	±0.0125	%FSR ±3 LSB
Integral Nonlin. Tempco.	—	±3	±8	ppm/°C
Differential Nonlinearity				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
−55°C to +125°C	—	±½	±0.0125	%FSR ±1 LSB
Differential Nonlin. Tempco	—	—	±2.5	ppm/°C
Full-Scale Absol. Accuracy:				
+25°C	—	±3	±8	LSB
0°C to +70°C	—	±4	±14	LSB
−55°C to +125°C	—	±8	±29	LSB

PERFORMANCE (cont.) DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Unipolar Zero Error, +25°C	—	±1	±3	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Zero Error, +25°C	—	±1	±3	LSB
Bipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±5	LSB
Bipolar Offset Error Tempco	—	±17.5	±35	ppm/°C
Gain Error, +25°C	—	±2	±5	LSB
Gain Tempco	—	±17.5	±35	ppm/°C
Conversion Times: ADC-508				
+25°C	—	—	700	nsec.
0°C to +70°C	—	—	740	nsec.
−55°C to +125°C	—	—	770	nsec.
No Missing Codes (12 Bits):	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current:				
+15V Supply	—	+23	+30	mA
−15V Supply	—	−11	−15	mA
+5V Supply*	—	+55	+90	mA
−5V Supply	—	−175	−210	mA
Power Dissipation	—	1.6	1.8	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range:				
−BMC	0	—	+70	°C
−BMM	−55	—	+125	°C
Storage Temperature Range	−65	—	+150	°C
Package Type	32-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12) grams			

* +5V power usage at 1TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).
2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

TABLE 5. OUTPUT CODING FOR UNIPOLAR OPERATION

BIPOLAR SCALE	INPUT RANGE	OUTPUT CODING					
		OFFSET BINARY			COMP. OFFSET BINARY		
	±10V dc	MSB		LSB	MSB		LSB
+FS −1 LSB	+9.9951V	1111	1111	1111	0000	0000	0000
+¾ FS	+7.5000V	1110	0000	0000	0001	1111	1111
+½ FS	+5.0000V	1100	0000	0000	0011	1111	1111
0	0.0000V	1000	0000	0000	0111	1111	1111
−½ FS	−5.0000V	0100	0000	0000	1011	1111	1111
−¾ FS	−7.5000V	0010	0000	0000	1101	1111	1111
−FS +1 LSB	−9.9951V	0000	0000	0001	1111	1111	1110
−FS	−10.000V	0000	0000	0000	1111	1111	1111

THEORY OF OPERATION (ADC-508 and SHM-45)

This theory of operation describes the ADC-508's operation in conjunction with DATEL's SHM-45. The SHM-45 sample-and-hold device captures fast signals for an ADC-508 to then digitize. Figure 4 shows a typical ADC-SHM circuit. The ADC-508 employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the ADC-SHM connection diagram, the ADC block diagram, and the timing diagram as needed (Figures 4, 1 and 2 respectively).

The SHM-45, upon acquiring the input signal on the hold capacitor (200 nanoseconds maximum acquisition time to 0.01%), is put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-508 requires a maximum of 150 nanoseconds for the input signal to settle before starting a conversion. The input of the ADC-508 starts settling to its final value while the SHM-45 is in the acquisition mode.

At the end of the SHM-45's hold mode settling time, the ADC-508's input is fully settled. The missing 50 nanoseconds of the required maximum analog input settling time is made up by the time the sample/hold is in the acquisition mode.

The SHM-45 is in the sample mode when the ADC-508's S/$\overline{H}$ control (Pin 17) is high. The S/H control pin is high and thus in the sample mode when the A/D is not performing a conversion.

The S/$\overline{H}$ control pin goes low after the rising edge of the START CONVERT pulse a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. To assure the SHM has 200 nanoseconds maximum acquisition time, the START CONVERT pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the START CONVERT pulse should be 105 nanoseconds minimum to assure the hold mode setting time of 100 nanoseconds is observed. The 105 nanoseconds takes into account the min-max propagation delays of the START CONVERT high to S/$\overline{H}$ control low propagation delays and the START CONVERT low to $\overline{EOC}$ high propagation delays.

Conversion being initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate range (± 10V range shown), is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

The first pass finished, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the output passes to three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{EOC}$ going low). The Sample/Hold control pin goes high a minimum of 30 nanoseconds before $\overline{EOC}$ goes low, indicating that the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{EOC}$ goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput using the ADC-508 and the SHM-45 consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds for observance of min-max propagation delays and 770 nanoseconds for the conversion process (S/H control pin saves 30 nanoseconds). Total throughput is a maximum of 1085 nanoseconds for the system for a guaranteed throughput rate of 920 KHz.

The ADC-508's conversion rate without a sample-hold would be 150 nanoseconds for input settling time and 800 nanoseconds for the ADC-508, yielding a minimum of 1.0 MHz conversion rate. Retriggering of the start convert pulse before $\overline{EOC}$ goes low will not initiate a new conversion.

The performance characteristics shown in Table 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These charateristics are guaranteed by design.

TABLE 6. PERFORMANCE CHARACTERISTICS AT DIFFERENT TEMPERATURES

CHARACTERISTIC	VALUE
Conversion Rate (Changing Inputs):	
ADC-508	
0°C to +70°C	1.0 MHz minimum
−55°C to +125°C	960 KHz minimum
Harmonic Distortion (Below FS):	
+25°C	−72 dB minimum
0°C to +70°C	−72 dB minimum
−55°C to +125°C	−65 dB minimum

To fully utilize the dynamic range of the ADC-508 , the SHM-45 can be hardware-programmed to provide the appropriate output voltage range. Table 7 shows the different input ranges which can be obtained by selecting the appropriate SHM-45. See the SHM-45 data sheet for connection details.

TABLE 7. ADC-SHM INPUT RANGES

V_{IN} Range	Gain
0 to +10	+1
0 to −10	−1
−5 to +5	−2
−10 to +10	−1
0 to −20	−0.5
0 to −5	−2

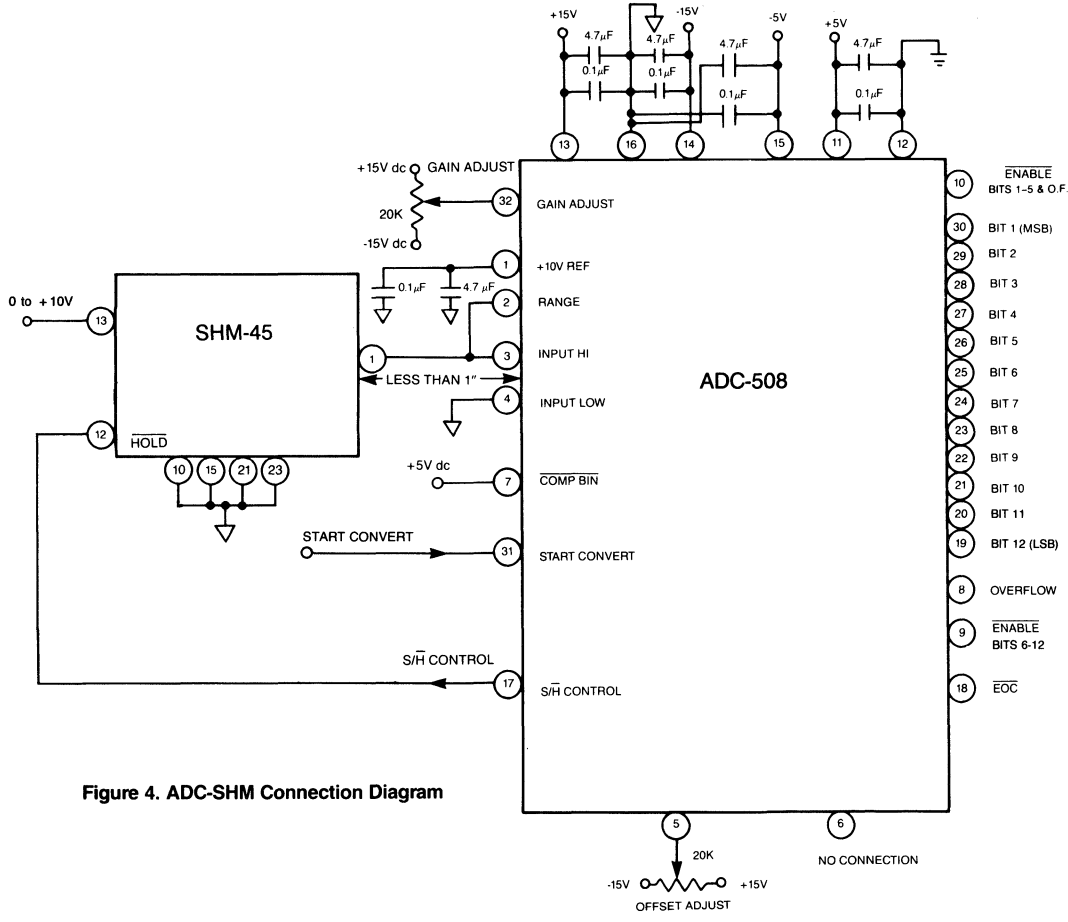


Figure 4. ADC-SHM Connection Diagram

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
ADC-508-MC	0°C to +70°C	Hermetic
ADC-508-MM	−55°C to +125°C	Hermetic

ACCESSORIES

Part Number	Description
TP20K	Trimming Potentiometers: (Two required).

Receptable for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For high reliability version of the ADC-508 contact DATEL.

ADC-510, ADC-515
10-Bit, Ultra-fast, Low-power A/D Converters

FEATURES

- 10-Bit resolution
- 450 Nanosecond conversion time
- Lower-power, 1.6W
- Small initial errors
- Three-state output buffers
- −55°C to +125°C operation
- Small 32-pin DIP

GENERAL DESCRIPTION

DATEL's ADC-510 and ADC-515 reflect the ultimate in state-of-the-art analog signal conversion technology. The ADC-510 boasts a remarkable conversion speed of 380 nanoseconds, along with a low-power consumption of 1.6 watts.

DATEL's ADC-510 and ADC-515 are 10-bit analog-to-digital converters which have small initial errors and can also provide adjustment capability for system errors. Both models have identical specifications except for conversion times. The ADC-515 has a maximum conversion time of 650 nanoseconds while the ultra-fast ADC-510 accomplishes a 10-bit conversion in less than or equal to 425 nanoseconds. Figure 1 is a simplified block diagram applicable to both devices.

Manufactured using thick-film and thin-film hybrid technology, these converters' remarkable performances are based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADC-510 and ADC-515 are packaged in a 32-pin ceramic DIP.

The ADC-510 and ADC-515 feature three pin-programmable input ranges: 0 to +10V, 0 to +20V, and ±10V dc. The input impedance is specified at 1.75K minimum for unipolar ranges and 3.75K minimum for the bipolar range, reducing stringent drive requirements. Other specifications include a maximum nonlinearity of ±½ LSB, a maximum gain tempco of ±35 ppm/°C and a maximum differential linearity tempco of ±2.5 ppm/°C.

All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary by using the $\overline{\text{COMP BIN}}$ pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

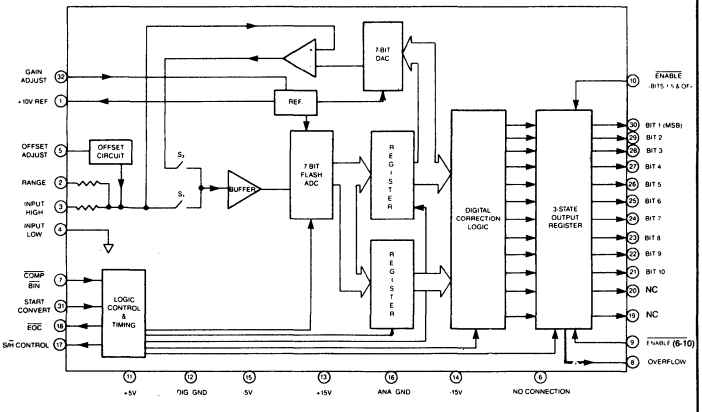
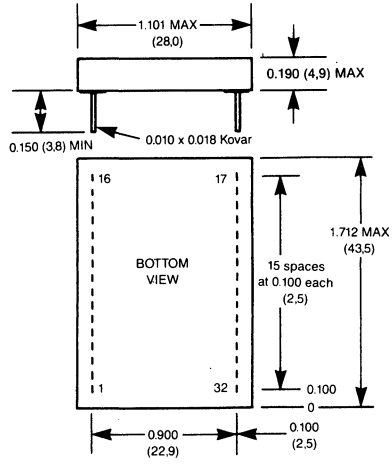


Figure 1. ADC-510, ADC-515 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have 0.025 inch, ±0.01 stand off from case

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF
2	RANGE
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST
6	NO CONNECTION
7	$\overline{\text{COMP BIN}}$
8	OVERFLOW
9	$\overline{\text{ENABLE (6-10)}}$
10	$\overline{\text{ENABLE (1-5, O.F.)}}$
11	+5V
12	DIGITAL GROUND
13	+15V
14	−15V
15	−5V
16	ANALOG GROUND
17	$\overline{\text{S/H}}$ CONTROL
18	$\overline{\text{EOC}}$
19	NC
20	NC
21	BIT 10 (LSB)
22	BIT 9
23	BIT 8
24	BIT 7
25	BIT 6
26	BIT 5
27	BIT 4
28	BIT 3
29	BIT 2
30	BIT 1 (MSB)
31	START CONVERT
32	GAIN ADJUST

Another novel feature of the ADC-510 is the provision of a Sample/Hold control pin for applications where a sample-hold is used in conjunction with the ADC-510. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

Power required for both models is ±15V dc and ±5V dc. Models are available in the commercial 0°C to +70°C, and military −55°C to +125°C operating temperature range. Typical applications include spectrum, transient, vibration, and waveform analysis. These devices are also ideally suited for radar, sonar and video digitization, medical instrumentation, and high-speed data acquisition systems. For information on versions with high reliability screening, contact the factory.

ABSOLUTE MAXIMUM RATINGS

Parameters	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 13)	0	+18	Volts dc
−15V Supply (Pin 14)	0	−18	Volts dc
+5V Supply (Pin 11)	−0.5	+7	Volts dc
−5V Supply (Pin 15)	+0.5	−7	Volts dc
Digital Inputs (Pins 7, 9, 10 & 31)	−0.3	+6	Volts dc
Analog Input (Pin 3)	−15	+15	Volts dc
Lead temp. (10 sec)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Range	—	0 to +10	—	Volts dc
	—	0 to +20	—	Volts dc
	—	±10	—	Volts dc
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	μA
Logic 0	—	—	−100	μA
OUTPUTS				
Output Coding: (Pin 7 High)	straight binary/offset binary			
(Pin 7 Low)	complementary binary complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	μA
Logic 0	—	—	6.4	mA
Internal Reference: Voltage, +25°C	9.98	—	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
PERFORMANCE				
Integral Nonlinearity: +25°C	—	—	±½	LSB
0°C to +70°C	—	—	±½	LSB
−55°C to +125°C	—	—	±1	LSB
Integral Nonlin. Tempco.	—	—	±10	ppm/°C
Differential Nonlinearity +25°C	—	—	±½	LSB
0°C to +70°C	—	—	±½	LSB
−55°C to +125°C	—	±½	±¾	LSB
Differential Nonlin. Tempco	—	—	±7.5	ppm/°C
Full-Scale Absol. Accuracy: +25°C	—	±2	±6	LSB
0°C to +70°C	—	±4	±9	LSB
−55°C to +125°C	—	±8	±1.5	LSB

PERFORMANCE (cont.) DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Unipolar Zero Error, +25°C	—	±¼	±1	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±5	LSB
Bipolar Offset Tempco	—	±13	±25	ppm/°C
Gain Error, +25°C	—	±2	±5	LSB
Gain Tempco	—	±17.5	±35	ppm/°C
Conversion Times: ADC-515, +25°C 0°C to +70°C(-BMC)	—	—	450	nsec.
-55°C to +125°C (-BMM)	—	—	510	nsec.
ADC-510, +25°C 0°C to +70°C (-BMC)	—	—	630	nsec.
-55°C to +125°C (-BMM)	—	—	700	nsec.
No Missing Codes (10 Bits):	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current: +15V Supply	—	—	+30	mA
−15V Supply	—	—	−15	mA
+5V Supply	—	—	+90	mA
−5V Supply	—	—	−210	mA
Power Dissipation	—	1.6	1.8	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range: -BMC	0	—	+70	°C
-BMM	−55	—	+125	°C
Storage Temperature Range	−65	—	+150	°C
Package Type	32-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12) grams			

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).
2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16). The −5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.
4. Obtain straight binary/offset binary output coding by tieing COMP BIN (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.
5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (Enable bits 1–5 & O.F.).
6. The Sample/Hold control signal, pin 17, goes low following the rising edge of a START CONVERT pulse and high 30 nanoseconds minimum before EOC goes low. This indicates that the converter can accept a new analog input.
7. The drive requirements of the ADC-510/515 may be satisfied with a wide-bandwidth, low output impedance input source. Applications of these converters that require the use of a sample-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.
8. Over temperature, input capacitance is 50 pF maximum and input impedance is 1.75K minimum (2.5K typical) for unipolar and 3.75K minimum (5K typical) for bipolar. These values are guaranteed by design.

1

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

TABLE 1. SIGNAL TIMING SUMMARY

LINE	DURATION IN NANOSECONDS
Start Convert	50 nsec. minimum
Analog Input Settling Time	150 nsec. minimum
Start Convert Low to EOC High Propagation Delay	35 nsec. maximum
Start Convert Low to Previous Output Data Invalid	275 nsec. minimum
Data Valid Before EOC Goes Low	25 nsec. minimum
Enable to Output Data Valid Propagation Delay	10 nsec. maximum

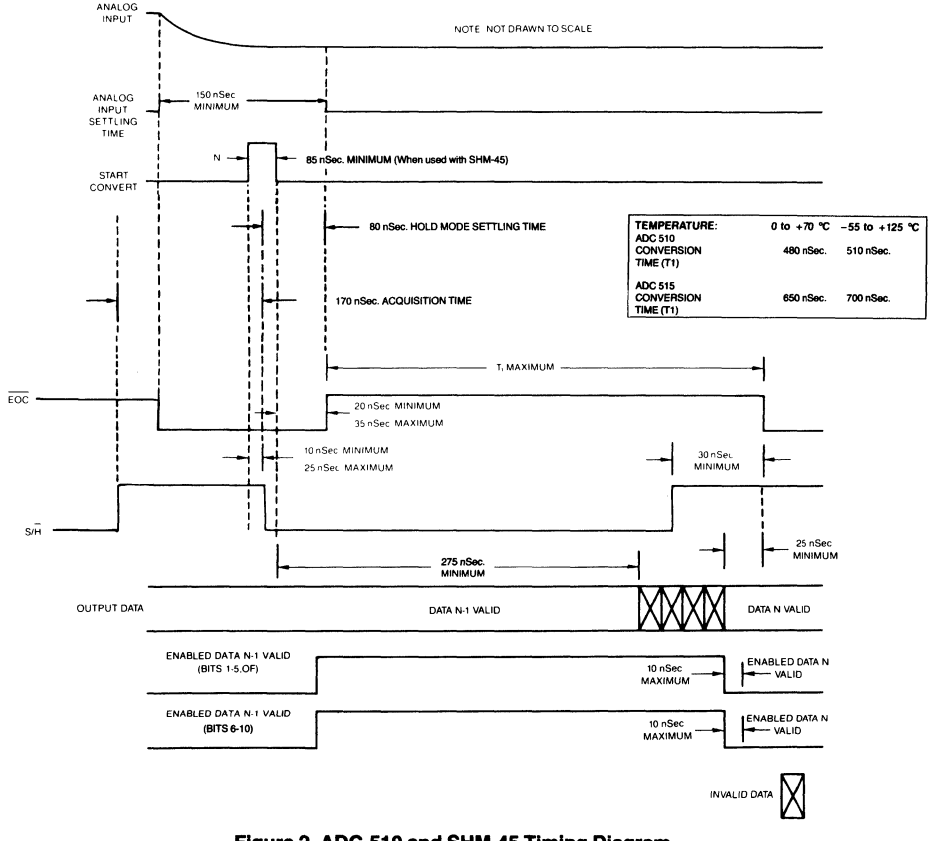


Figure 2. ADC-510 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 kHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero and Offset Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+½LBS) or the bipolar zero adjustment (Zero +½LBS) for the appropriate FSR. Adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 and 00 0000 0001 with the COMP BIN (pin 7) tied high or between 11 1111 1111 and 11 1111 1110 with the COMP BIN tied low.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low.
3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS −1½LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1110 and 11 1111 1111 for $\overline{\text{COMP BIN}}$ (pin 7) tied high or between 00 0000 0001 and 00 0000 0000 for $\overline{\text{COMP BIN}}$ tied low.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

TABLE 2. INPUT CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to +10V dc	3	3
0 to +20V dc	3	16
±10V dc	3	1

TABLE 3a. ZERO AND GAIN ADJUST FOR UNIPOLAR USE

UNIPOLAR FSR	ZERO ADJUST +½ LSB	GAIN ADJUST +FS −1½ LSB
0 to +10V dc	+4.88mV	+9.9927V dc
0 to +20V dc	+9.77mV	+19.9854V dc

TABLE 3b. ZERO AND GAIN ADJUST FOR BIPOLAR USE

BIPOLAR FSR	ZERO ADJUST ZERO +½LBS	GAIN ADJUST +FS −1½ LSB
±10V dc	+9.77mV	+9.9707V dc

TABLE 4. OUTPUT CODING FOR UNIPOLAR OPERATION

UNIPOLAR SCALE	INPUT RANGES, VOLTS dc		OUTPUT CODING					
			STRAIGHT BINARY			COMP. BINARY		
	0 to +10V	0 to +20V	MSB		LSB	MSB		LSB
+FS −1 LSB	+9.99023V	+19.9804V	11	1111	1111	00	0000	0000
7/8 FS	+8.7500V	+17.500V	11	1000	0000	00	0111	1111
3/4 FS	+7.5000V	+15.000V	11	0000	0000	00	1111	1111
1/2 FS	+5.0000V	+10.000V	10	0000	0000	01	1111	1111
1/4 FS	+2.5000V	+5.0000V	01	0000	0000	10	1111	1111
1/8 FS	+1.2500V	+2.5000V	00	1000	0000	11	0111	1111
+1 LSB	+0.00977V	+0.0195V	00	0000	0001	11	1111	1110
0	0.0000V	0.0000V	00	0000	0000	11	1111	1111

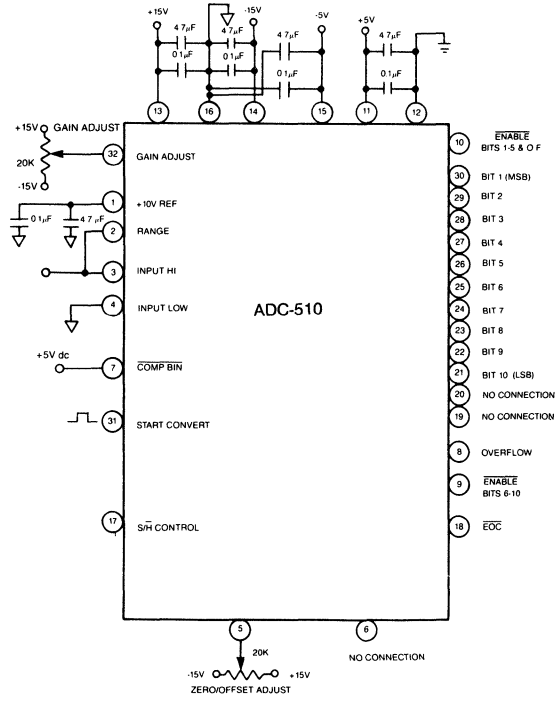


Figure 3. ADC-510 Calibration Circuit

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TABLE 5. OUTPUT CODING FOR UNIPOLAR OPERATION

BIPOLAR SCALE	INPUT RANGE -+10V dc	OUTPUT CODING					
		OFFSET BINARY			COMP. OFFSET BINARY		
		MSB		LSB	MSB		LSB
+FS-1LSB	+9.9805V	11	1111	1111	00	0000	0000
+¾ FS	+7.5000V	11	1000	0000	00	0111	1111
+½ FS	+5.0000V	11	0000	0000	00	1111	1111
0	0.0000V	10	0000	0000	01	1111	1111
-½ FS	-5.0000V	01	0000	0000	10	1111	1111
-¾ FS	-7.5000V	11	1000	0000	11	0111	1111
-FS +1 LSB	-9.9805V	00	0000	0001	11	1111	1110
-FS	-10.000V	00	0000	0000	11	1111	1111

THEORY OF OPERATION (ADC-510 and SHM-45)

This theory of operation describes the ADC-510's operation in conjunction with DATEL's SHM-45. The SHM-45 sample-and-hold device can be used to capture fast signals for an ADC-510 to then digitize. Figure 4 shows a typical ADC-SHM circuit. The ADC-510 employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 10 bits. Refer to the ADC-SHM connection diagram, the ADC block diagram, and the timing diagram as needed (Figures 4, 1, and 2 respectively).

The SHM-45, upon acquiring the input signal on the hold capacitor (170 nanoseconds maximum acquisition time to 0.1%), is put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 80 nanoseconds to have its output buffer settle to 0.1% accuracy. The ADC-510 requires a maximum of 150 nanoseconds for the input signal to settle before starting a conversion. The input of the ADC-510 starts settling to its final value while the SHM-45 is in the acquisition mode. At the end of the SHM-45's hold mode settling time, the ADC-510's input is fully settled.

A minimum START CONVERT pulse of 85 nanoseconds is required, conversion starting on the falling edge of the START CONVERT pulse with $\overline{EOC}$ going high a maximum of 35 nanoseconds later. The missing 30 nanoseconds of the required maximum analog input settling time is made up by the time the sample/$\overline{hold}$ is in the acquisition mode.

The SHM-45 is in the sample mode when the ADC-510's S/$\overline{H}$ control (Pin 17) is high. The S/H control pin is high and thus in the sample mode when the A/D is not performing a conversion.

The S/H control pin goes low after the rising edge of the START CONVERT pulse a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. To assure the SHM has 170 nanoseconds maximum acquisition time, the START CONVERT pulse should be given a minimum of 160 nanoseconds after the desired start of the acquisition time. The width of the START CONVERT pulse should be 85 nanoseconds minimum to assure the hold mode settling time of 80 nanoseconds is observed. The 85 nanoseconds takes into account the min-max propagation delays of the START CONVERT high to S/H control low propagation delays and the START CONVERT low to $\overline{EOC}$ high propagation delays.

Conversion being initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate range (± 10V range shown), is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

The first pass finished, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 10-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the output passes to three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{EOC}$ going low). The Sample/$\overline{Hold}$ control pin goes high a minimum of 30 nanoseconds before $\overline{EOC}$ goes low, indicating the the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 275 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid up to 275 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput of the ADC-510 and the SHM-45 configuration consists of the 170 nanoseconds for the sample time, 80 nanoseconds for the hold and input settling time, and 480 nanoseconds for the conversion process (S/H control pin saves 30 nanoseconds). Total throughput is a maximum of 730 nanoseconds for the system or a throughput rate of 1.35 MHz. The ADC-510's conversion rate without a sample-hold would be 150 nanoseconds for input settling time and 480 nanoseconds for the ADC-510, yielding a minimum of 1.55 MHz conversion rate. Retriggering of the START CONVERT pulse before $\overline{EOC}$ goes low will not initiate a new conversion.

The performance characteristics shown in Table 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

TABLE 6. PERFORMANCE CHARACTERISTICS AT DIFFERENT TEMPERATURES

CHARACTERISTIC	VALUE
Conversion Rate (Changing Inputs):	
0°C to +70°C (ADC-510)	1.55 MHz minimum
-55°C to +125°C (ADC-515)	1.25 MHz minimum
Harmonic Distortion (Below FS):	
+25°C	-60db minimum
0°C to +70°C	-60db minimum
-55°C to +125°C	-60db minimum

To fully utilize the dynamic range of the ADC-510/515, the SHM-45 can be hardware programmed to provide the appropriate output voltage range. Table 7 shows the different input ranges which can be obtained by selecting the appropriate SHM-45 gain. See the SHM-45 data sheet for connection details.

TABLE 7. ADC-SHM INPUT RANGES

V_{IN} Range	Gain
0 to +10	+1
0 to -10	-1
-5 to +5	-2
-10 to +10	-1
0 to -20	-0.5
0 to -5	-2

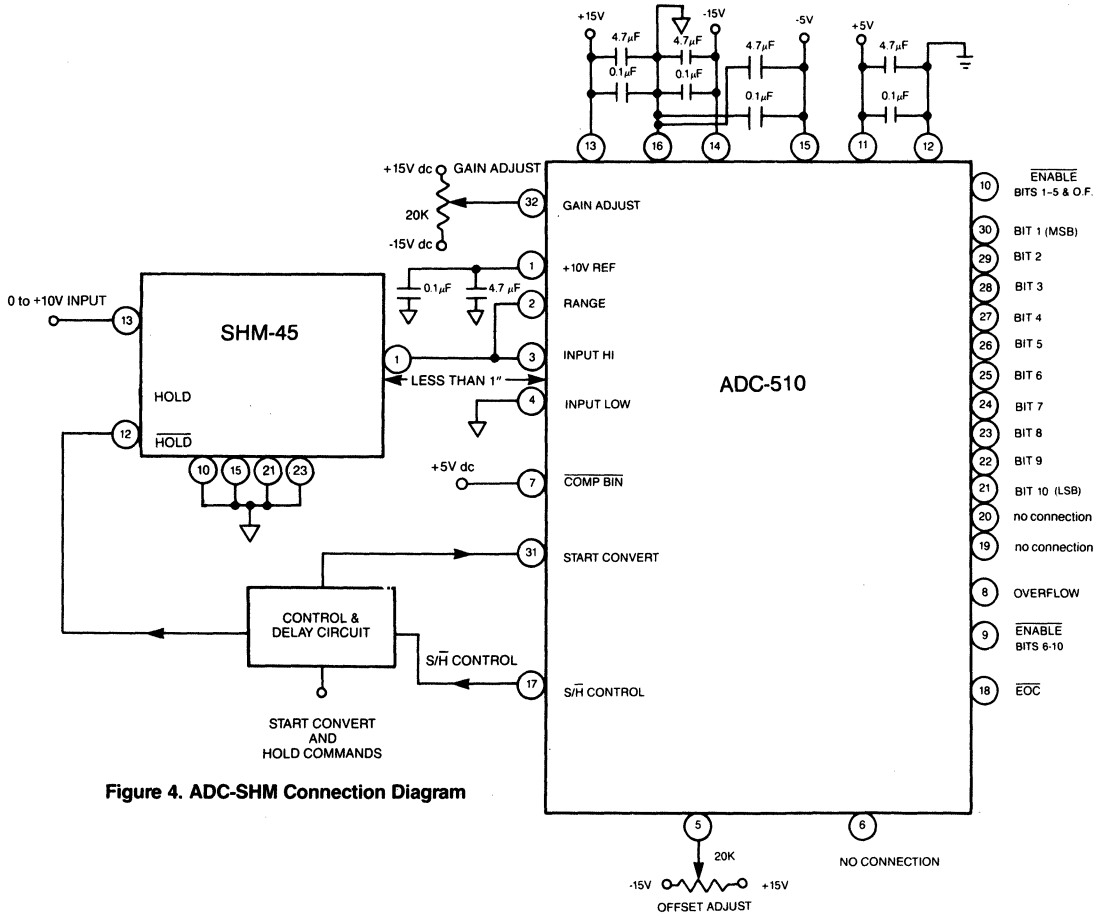


Figure 4. ADC-SHM Connection Diagram

ORDERING INFORMATION

MODEL	OPERATING TEMP.RANGE	SEAL
ADC-510-BMC	0°C to +70°C	Hermetic
ADC-510 BMM	−55°C to +125°C	Hermetic
ADC-515-BMC	0°C to +70°C	Hermetic
ADC-515-BMM	−55°C to +125°C	Hermetic

ACCESSORIES

Part Number	Description
TP20K	Trimming Potentiometers: (Two required).

Receptable for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For high reliability version of the ADC-510 and ADC-515, contact DATEL.

ADC-5101
Adjustment-Free
8-Bit A/D Converter

1

FEATURES

- **900 Nanoseconds maximum conversion time**
- **Adjustment-free operation**
- **Industry standard converter**
- **−55°C to +125°C Version**
- **Wide power supply range**

GENERAL DESCRIPTION

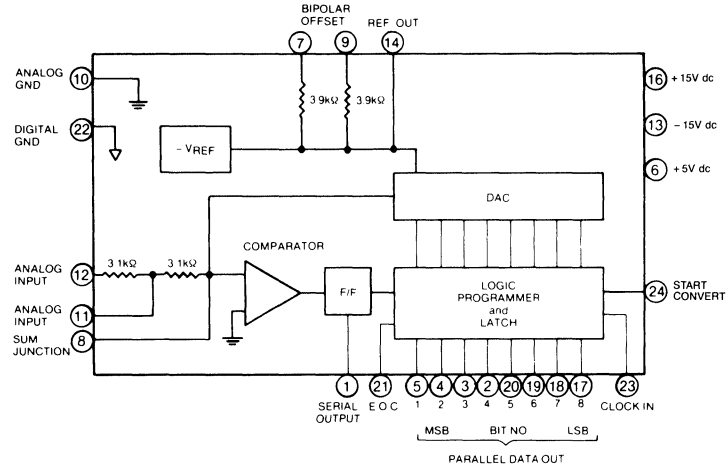
DATEL's ADC-5101 is a high-speed, adjustment-free, 8-bit analog-to-digital converter. Pin-compatible with industry-standard 5101 converters, these devices offer high speed and high accuracy with a full military temperature range version available.

Using the successive approximation method, the ADC-5101 achieves a conversion time of only 900 nanoseconds maximum, making it an ideal choice for high speed, multiplexed data acquisition systems. Active laser trimming of highly stable thin-film resistor networks eliminates the need for external gain or offset adjustments. Overall full-scale absolute accuracy is only ±½ LSB at +25°C and only ±2 LSB over the full military operating temperature range.

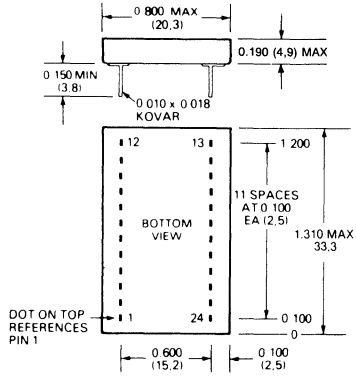
Output coding is straight binary for unipolar operation and offset binary for bipolar operations with both parallel and serial outputs brought out. Digital outputs are TTL-compatible and can drive 5 TTL loads. Nine analog input voltage ranges are programmable by external pin connection.

The ADC-5101H is specified for operation over the full military operating temperature range of −55°C to +125°C. Other models are specified for operation over the commercial 0°C to +70°C operating temperature.

All models require ±15V dc and +5V dc for operation and are packaged in a 24-pin, hermetically sealed ceramic package.



MECHANICAL DIMENSIONS
INCHES (MM)
24-PIN CERAMIC



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL DATA OUT	13	− 15V POWER
2	BIT 4 OUT	14	REF. OUT
3	BIT 3 OUT	15	N/C
4	BIT 2 OUT	16	+ 15V POWER
5	BIT 1 OUT (MSB)	17	BIT 8 OUT (LSB)
6	+ 5V POWER	18	BIT 7 OUT
7	BIPOLAR OFF.	19	BIT 6 OUT
8	SUM JUNCTION	20	BIT 5 OUT
9	BIPOLAR OFF.	21	E.O.C. (STATUS)
10	ANALOG GND.	22	DIGITAL GND.
11	ANALOG INPUT	23	CLOCK INPUT
12	ANALOG INPUT	24	START CONVERT

ABSOLUTE MAXIMUM RATINGS	
Analog Supply	±0.5V dc to ±17V dc
Logic Supply	−0.5V dc to +7V dc
Analog Input	±25V dc
Digital Inputs	−0.5V dc to +5.5V dc

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to −5V dc, 0 to −10V dc, 0 to −20V dc
	0 to +5V dc, 0 to +10V dc, 0 to +20V dc
bipolar	±2.5V dc, ±5V dc, ±10V dc
Input Impedance, 5V range	1.5 kΩ
10V range	3.0 kΩ
20V range	6.0 kΩ
Input Logic Levels, Logic "1", min.	+2.0V
Logic "0", max.	+0.8V
Start Conversion	Negative going pulse with duration of 25 nsec. min. Loading:[2] 2 TTL loads
Clock Input, Pulse width high, min.	20 nsec.
Pulse width low, min.	46 nsec.

OUTPUTS	
Parallel Output Data	8 parallel lines of data held until next conversion command.
Output Logic Levels	
Logic "1", min.	+2.4V
Logic "0", max.	+0.4V
Fanout	5 TTL loads
Coding, unipolar	Straight binary
bipolar	Offset binary
Serial Output Data	NRZ successive decision pulses out, MSB first, at the clock frequency.
End of Conversion (E.O.C.)[4]	Conversion Status Signal. Output is high during reset and conversion, low when conversion is complete
Reference Output Voltage	−6.2V

PERFORMANCE	
Resolution	8 Bits
Conversion Time, max.	900 nsec. max.
Nonlinearity max.	±½ LSB
Differential Nonlinearity, max.	±½ LSB
Absolute Accuracy, max.[5]	±½ LSB
Absolute Accuracy vs. temperature	
0 to +70°C, max.	+1 LSB
−55 to +125°C, max.	±2 LSB
Reference Output Tempco	5 ppm/°C typ., 20 ppm/°C max.
Power Supply Rejection	
Positive Supply	±0.002% FSR[6]/% Supply
Negative Supply	±0.002% FSR/% Supply
Logic Supply	±0.01% FSR/% Supply
No Missing Codes	Over operating temperature range

POWER REQUIREMENTS	
Analog Supply, Pin 16	+10V dc to +16V dc at 35 mA max.
Pin 13	−10V dc to −16V dc at 35 mA max.
Logic Supply, Pin 6	+5V dc ±0.25V dc at 100 mA max.
Power Dissipation, max.	1.2W

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range,	
ADC-5101	0°C to +70°C
ADC-5101H	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C
Package Type	24 pin hermetically sealed ceramic

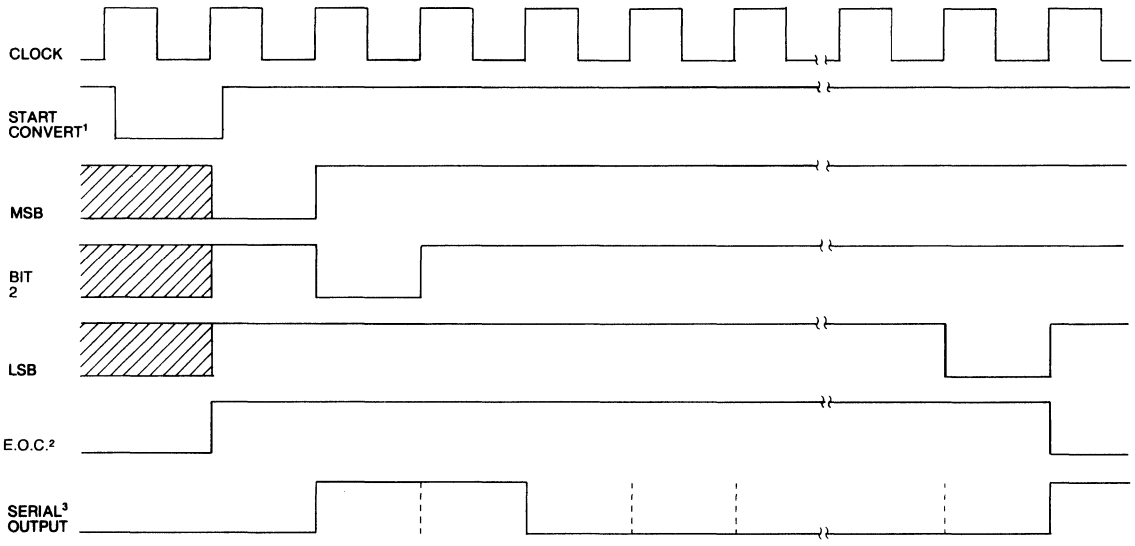
FOOTNOTES:

1. Converter will reset on the first edge of the clock after START CONVERT goes low and will convert the MSB on the next rising edge of the clock. If the START CONVERT is held low, the converter will be reset but will not convert the MSB until the first rising edge of clock after the START CONVERT returns high.
2. One TTL load is defined as 40 μA at logic "1" and −1.6 mA at Logic "0".
3. Clock input loading is 1 TTL load.
4. At the end of the conversion, the E.O.C. signal will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. signal is low.
5. Absolute accuracy includes offset, gain, linearity, and all other errors. See Technical Note 3.
6. FSR is full-scale range.

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for optimum performance. The analog common (Pin 10) and digital common (Pin 22) are not connected internally and therefore should be connected externally as close to the package as possible. For best results, this common connection should be a large ground plane running under the device package.
2. Both analog and digital supplies should be bypassed to ground with 1.0 μF electrolytic capacitors in parallel with 0.1 μF disc ceramic capacitors. Bypass capacitors should be located directly adjacent to, or on, each supply pin.
3. The absolute accuracy error of an A/D converter is defined as the difference between the theoretical analog input voltage required to produce a given digital output and the unadjusted analog input voltage actually required to produce that same code. Because this error is measured and specified without adjustment, it includes all factors that may effect the devices accuracy at the point of measurement: offset error, linearity error, gain error, and noise error.
4. The ADC-5101 should be driven from low impedance sources capable of high frequency current variations. DATEL AM-452, a wide bandwidth, fast settling, monolithic operational amplifier is recommended for use as a driving amplifier.

TIMING DIAGRAM



FOOTNOTES:

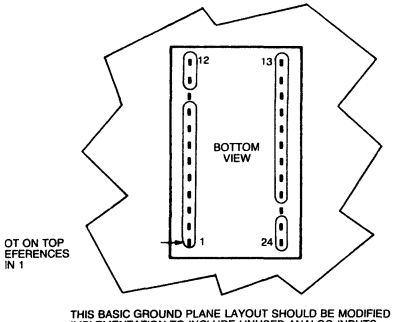
1. The converter is reset by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nanoseconds prior to the clock transition. After the START is set high, the conversion will begin on the next rising clock edge. The START CONVERT may be set low at any time during a conversion to reset and begin again.
2. At the end of the conversion, the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
3. The serial output is non-return to zero.

OUTPUT CODING AND RANGE SELECTION

DIGITAL OUTPUT	ANALOG INPUT—UNIPOLAR RANGES					
	0 TO −5V	0 TO −10V	0 TO −20V	0 TO +5V	0 TO +10V	0 TO +20V
0000 0000	0.000V	0.000V	0.000V	+4.981V	+9.961V	+19.922V
0000 0001	−0.019V	−0.039V	−0.078V	+4.961V	+9.922V	+19.844V
0111 1111	−2.481V	−4.961V	−9.922V	+2.500V	+5.000V	+10.000V
1000 0000	−2.500V	−5.000V	−10.000V	+2.481V	+4.961V	+9.922V
1111 1110	−4.961V	−9.922V	−19.844V	+0.019V	+0.039V	+0.078V
1111 1111	−4.981V	−9.961V	−19.922V	0.000V	0.000V	0.000V

DIGITAL OUTPUT	ANALOG INPUT — BIPOLAR RANGES		
	±2.5V	±5.0V	±10.0V
0000 0000	+2.500V	+5.00V	+10.000V
0000 0001	+2.481V	+4.961V	+9.922V
0111 1111	+0.019V	+0.039V	+0.078V
1000 0000	0.000V	0.000V	0.000V
1111 1110	−2.461V	−4.922V	−9.844V
1111 1111	−2.481V	−4.961V	−9.922V

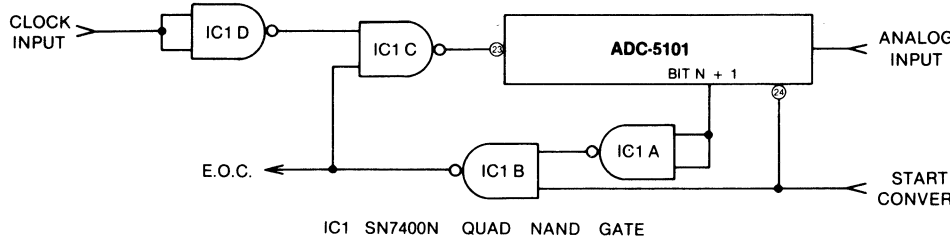
BASIC GROUND PLANE LAYOUT



THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

INPUT RANGE SELECTION

INPUT VOLTAGE RANGE	CONNECT ANALOG INPUT TO PIN	CONNECT PIN 8 TO PIN	CONNECT PIN 10 TO PIN
0 to −5V	11	12	7,9
0 to −10V	11	—	7,9
0 to −20V	12	—	7,9
0 to +5V	11	7,9,12	—
0 to +10V	11	7,9	—
0 to +20V	12	7,9	—
±2.5V	11	9,12	7
±5V	11	9	7
±10V	12	9	7



When less than 8-bit resolution is required, the ADC-5101 may be operated at higher conversion speeds by truncating the conversion when the desired number of bits have been converted. Connect the converter as shown in the logic diagram. The bit output used to drive gate "A" should be one more than the number of bits to be converted; for example, for 6 bits resolution, connect this gate to the bit 7 output.

MAXIMUM CONVERSION SPEEDS

BITS	CONVERSION SPEED
7	750 nanoseconds
6	650 nanoseconds
5	500 nanoseconds
4	400 nanoseconds

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-5101	0°C to +70°C
ADC-5101H	−55°C to +125°C

For military versions compliant to MIL-STD-883, contact DATEL.

ADC-511
12-Bit, High-Speed, Low-Power A/D Converter

FEATURES

- **12-Bit resolution**
- **1.0 Microsecond maximum conversion time**
- **Low-power, 925 milliwatts**
- **Three-state output buffers**
- **Functionally complete**
- **Small 24-pin DIP**

GENERAL DESCRIPTION

DATEL's ADC-511 uses an advanced design to provide a high-speed, functionally complete 12-bit A/D converter in a small 24-pin DIP. The ADC-511 delivers a conversion speed of 1 microsecond while consuming only 925 milliwatts of power.

Manufactured using thin- and thick-film hybrid technology, the ADC-511's exclusive performance is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes.

Functionally complete, the ADC-511 contains an internal clock, three-state outputs and an internal reference. The internal reference can supply +10V at 1.5 milliamps externally. System errors or small initial errors can be adjusted to zero using external circuitry.

The ADC-511 features two pin programmable analog input ranges: 0 to +10V, and ±5V dc. The input impedance is specified at 2.0 Kohms minimum, reducing stringent drive requirements. Other specifications include no missing codes over temperature, a maximum gain tempco of +35 ppm/ °C and a maximum differential linearity tempco of +2.5 ppm/ °C.

All digital inputs and three-state outputs are TTL and CMOS compatible. Output coding can be in straight binary/ offset binary or complementary binary/ complementary offset binary by using the COMP BIN pin.

Power required is ±15V dc and +5V dc. Models are available in the commercial 0 °C to +70 °C and military -55 °C to +125 °C operating temperature ranges.

For information on versions with high reliability screening, contact DATEL.

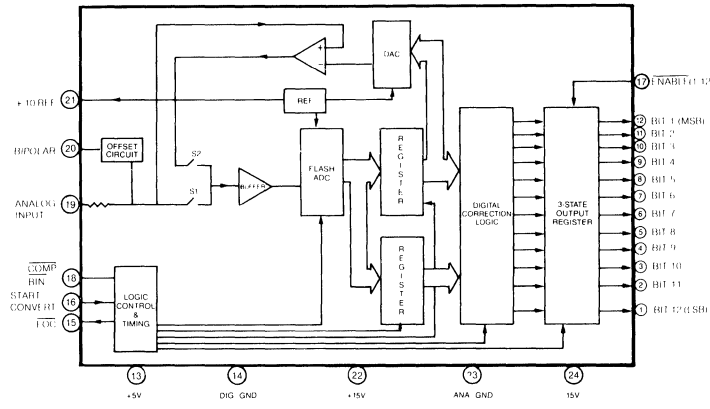
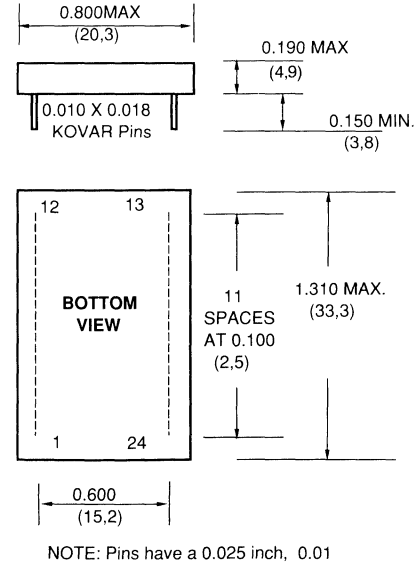


Figure 1. ADC-511 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, 0.01 stand-off from case.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	Bit 12 OUT (LSB)
2	Bit 11 OUT
3	Bit 10 OUT
4	Bit 9 OUT
5	Bit 8 OUT
6	Bit 7 OUT
7	Bit 6 OUT
8	Bit 5 OUT
9	Bit 4 OUT
10	Bit 3 OUT
11	Bit 2 OUT
12	Bit 1 OUT (MSB)
13	+5V
14	DIGITAL GROUND
15	EOC
16	START CONVERT
17	ENABLE (1-12)
18	COMP BIN
19	ANALOG INPUT
20	BIPOLAR
21	+10V REF
22	+15V
23	ANALOG GROUND
24	-15V

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply(Pin 13)	-0.5 to +7	Volts dc
Digital inputs (Pins 16, 17, and 18)	-0.3 to +7	Volts dc
Analog input	-25 to +25	Volts dc
Lead temp. (10 sec.)	300	° C max.

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range	–	0 to+10	–	Volts
(See Table 5 also)	–	±5	–	Volts
Input Impedance				
Resistance	2	2.5	–	K Ohms
Capacitance	–	–	50	pF
Logic Levels:				
Logic 1	2.0	–	–	Volts
Logic 0	–	–	0.8	Volts
Logic Loading:				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA
OUTPUTS				
Resolution	12	–	–	Bits
Logic Levels:				
Logic 1	2.4	–	–	Volts
Logic 0	–	–	0.4	Volts
Logic Loading:				
Logic 1	–	–	- 160	µA
Logic 0	–	–	6.4	mA
Internal Reference:				
+Voltage, +25° C	9.98	10	10.02	Volts dc
Tempco	–	±5	±30	ppm/ °C
External current	–	–	1.5	mA
Output Coding: (Pin 18 High)	Straight binary/Offset binary			
(Pin 18 Low)	Complementary binary / Complementary offset binary			
PERFORMANCE				
Integral Nonlinearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 °C to +125 °C	–	–	±3	LSB
Integral Nonlinearity Tempco	–	±3	±8	ppm/°C
Differential Nonlinearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 °C to +125 °C	–	–	±1	LSB
Differential Nonlinearity Tempco	–	–	±2.5	ppm/ °C

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Full-Scale Absolute Accuracy				
+25 °C	–	±3	±7	LSB
0 °C to +70 °C	–	±4	±13	LSB
-55 °C to +125 °C	–	±8	±28	LSB
Unipolar Zero Error ①	–	±1	±3	LSB
Unipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Zero Error ①	–	±1	±3	LSB
Bipolar Zero Tempco	–	±2	±5	ppm/ °C
Bipolar Offset Error ①	–	±2	±4	LSB
Bipolar Offset Tempco	–	±17.5	±35	ppm/ °C
Gain Error ①	–	±2	± 4	LSB
Gain Error Tempco	–	±17.5	±35	ppm/ °C
Conversion Time				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.0	µSec.
-55 °C to +125 °C	–	–	1.15	µSec.
No missing codes (For 12 binary bits)	Guaranteed over operating temp. range			
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
-15V dc Supply	-14.25	-15	-15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
Supply Current				
+15V Supply	–	+20	+25	mA
-15V Supply	–	-20	-28	mA
+5V Supply *	–	+65	+75	mA
Power Dissipation	–	925	1200	mW
Supply Rejection	–	–	±0.01	%FSR/%V
PHYSICAL/ ENVIRONMENTAL				
Operating Temperature Range				
—MC Models	0	–	+70	°C
—MM Models	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetically sealed ceramic DIP			
Pin Type	0.010 x 0.018 inch Kovar			
Weight	0.42(12)oz.(gram)			

* + 5V power usage at 1 TTL logic loading per data output bit.

① Specifications cited are at +25 °C. See Techical Note 1 for further information.

APPLICATIONS

- **High-speed Data Acquisition Systems**
- **Vibration and Resonance/transient Analysis**
- **Medical Imaging and Scanning**
- **Spectrum and Noise Analyzers**
- **Radar, Sonar, and Video Processing Systems**

TECHNICAL NOTES

1. Applications unaffected by endpoint errors or those that remove them through software will use the typical connections shown in Figure 2. The optional external circuitry of Figure 4 removes system errors or helps adjust the small initial errors of the ADC-511 to zero . The external adjustment circuit has no affect on the throughput rate. Table 1 shows how to select the input range.

2. Additional input ranges are available by using optional external adjustment circuitry. Refer to Figure 4 and Table 5.

3. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

4. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 μF, 25V tantalum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

5. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ (pin 18) to ground. The complementary signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

6. To obtain Three-State outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). Otherwise, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "1" (high).

INPUT CONNECTIONS

Table 1. Input Connections

INPUT VOLTAGE RANGE	INPUT PIN	JUMPER THESE PINS:
0 to +10V dc	19	Pin 20 to GROUND
±5V dc	19	Pin 20 to Pin 21

TIMING

Figure 3 shows the relationship between the various input signals. The timing shown in Table 2 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 2. Signal Timing Summary

SIGNAL	DURATION IN NANOSECONDS
Start Convert Pulse Width	200 nSec minimum
Analog Input Settling Time	600 nSec minimum
Start Convert Low to $\overline{\text{EOC}}$ High Propagation Delay	35 nSec maximum
$\overline{\text{EOC}}$ Low to Previous Output Data Invalid	1320 nSec minimum
Data Valid After $\overline{\text{EOC}}$ Goes Low	20 nSec maximum
$\overline{\text{Enable}}$ to Output Data Valid Propagation Delay	10 nSec maximum

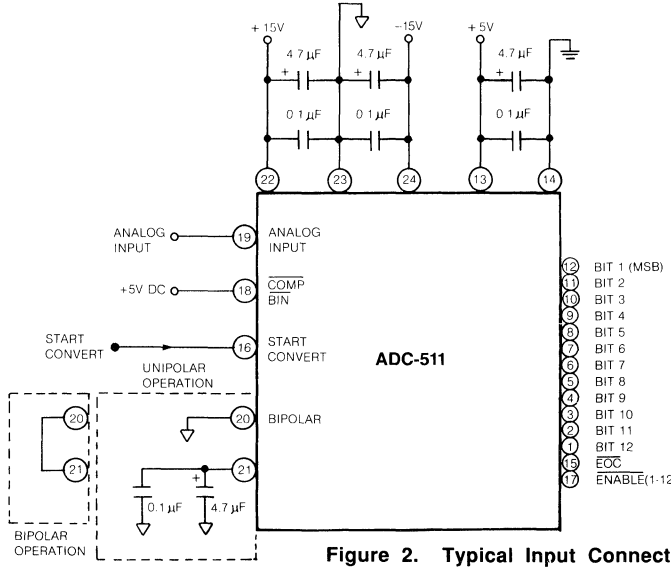
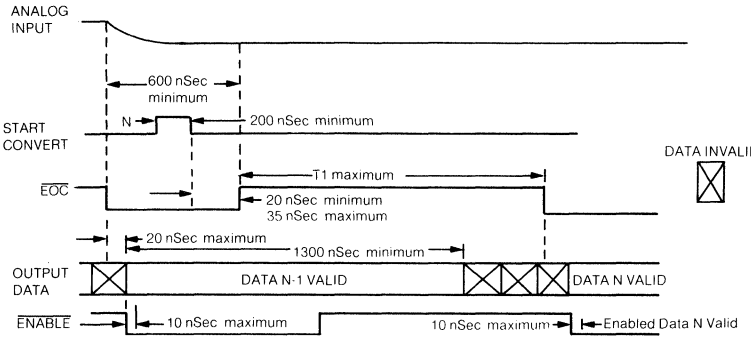


Figure 2. Typical Input Connections for the ADC-511.

Temperature	0 to +70 C	-55 C to +125 C
Conversion Time (T1)	1.0 µSec.	1.15 µSec.



NOTE: NOT DRAWN TO SCALE

Figure 3. ADC-511 Timing Diagram

THEORY OF OPERATION

The ADC-511 employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses 7-bits of a single flash converter in the conversion process twice to yield a final resolution of 12 bits. Refer to the connection diagram, block diagram, and timing diagram as needed.

The ADC-511 requires a maximum of 600 nanoseconds for the input signal to settle before starting a conversion. Upon conversion , switch S1 of the ADC closes and S2 opens. The input, having been configured for the appropriate range, is buffered and then digitized to 7-bits by the flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

The first pass finished, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the output passes to the three-state output buffers.

Data from the conversion is valid and capable of being latched 20 nanoseconds after the falling edge of $\overline{EOC}$ and remains valid for 1300 nanoseconds. Data from the new conversion is valid a maximum of 20 nanoseconds after the next $\overline{EOC}$ low transition. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The ADC-511's conversion rate is based upon 600 nanoseconds for analog input settling time and a 1 microsecond conversion time, yielding a minimum of 600 KHz conversion rate (changing inputs, A/D only). Retriggering of the START CONVERT pulse before $\overline{EOC}$ goes low will not initiate a new conversion.

The performance characteristics shown in Table 3 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

Table 3. Performance vs. Temperature

Characteristic	Value
Conversion Rate (Changing Inputs):	
+25 °C	600 KHz minimum
0 °C to +70 °C	600 KHz minimum
-55 °C to +125 °C	575 KHz minimum
Harmonic Distortion (Below FS)	
+25 °C	-72 dB minimum
0 °C to +70 °C	-72 dB minimum
-55 °C to +125 °C	-65 dB minimum

Table 4a. Zero and Gain Adjust, Unipolar Operation

UNIPOLAR FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc

Table 4b. Zero and Gain Adjust, Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 +1/2 LSB	GAIN ADJUST +FS -1 1/2 LSB
±5V dc	+1.22 mV dc	+4.9963V dc

CALIBRATION

Remove system errors or the small initial errors by adjusting the zero and full-scale adjustment potentiometers of the user-supplied circuit shown in Figure 4. Connect this circuit to the ADC-511's ANALOG INPUT (pin 19). Apply power and other connections as shown in Figure 2 .

Procedure

1. Refer to Table 1 for the appropriate full-scale input range (FSR). The data outputs should be connected to LED's to observe the resulting data values. Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments:

Apply a precision voltage reference source between the amplifier's signal input and analog ground. Use a very low-noise signal source for accurate calibration.

Adjust the output of the reference source per Tables 4a and 4b for the unipolar zero adjustment (+1/2 LSB) or the bipolar zero adjustment (zero + 1/2 LSB) for the appropriate full-scale range. For unipolar operation, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 18) tied high or between 1111 1111 1111 and 1111 1111 1110 with COMP BIN tied low.

Table 5. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	Unit
0 to +10V,+5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V,+1.25V	2	14	K Ohms

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with the COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low.

3. Full-Scale Adjustment:

Set the output of the voltage reference used in step 2 to the value shown in the Tables 4a and 4b for the unipolar or bipolar gain adjustment (+F.S. -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 18) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 5 and 6.

Table 6. Output Coding for Uniplar Operation

UNIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Straight Binary		Complementary Straight Binary	
	0 to +10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.9976V	1111 1111	1111	0000 0000	0000
7/8 FS	+8.7500V	1110 0000	0000	0001 1111	1111
3/4 FS	+7.5000V	1100 0000	0000	0011 1111	1111
1/2 FS	+5.0000V	1000 0000	0000	0111 1111	1111
1/4 FS	+2.5000V	0100 0000	0000	1011 1111	1111
1/8 FS	+1.2500V	0010 0000	0000	1101 1111	1111
1 LSB	+0.0024V	0000 0000	0001	1111 1111	1110
0	0.0000V	0000 0000	0000	1111 1111	1111

Table 7. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Offset Binary		Complementary Offset Binary	
	± 5V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+4.9976V	1111 1111	1111	0000 0000	0000
+3/4 FS	+3.7500V	1110 0000	0000	0001 1111	1111
+1/2 FS	+2.5000V	1100 0000	0000	0011 1111	1111
0	0.0000V	1000 0000	0000	0111 1111	1111
-1/2 FS	-2.5000V	0100 0000	0000	1011 1111	1111
-3/4 FS	-3.7500V	0010 0000	0000	1101 1111	1111
-FS + 1 LSB	-4.9976V	0000 0000	0001	1111 1111	1110
-FS	-5.0000V	0000 0000	0000	1111 1111	1111

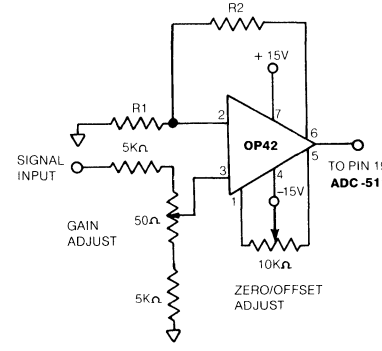


Figure 4. Optional Calibration Circuit

Combining the ADC-511 with Datel's SHM-45 Sample-and-Hold Device

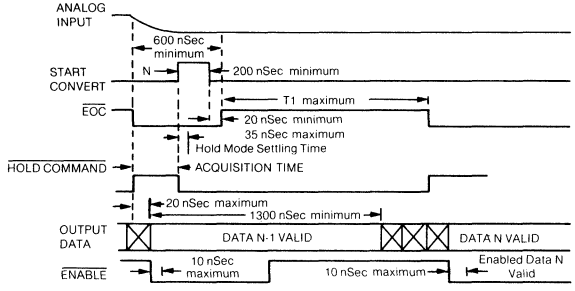
The application shown in Figure 6 uses the ADC-511 in conjunction with DATEL's SHM-45, a 0.01% accurate, 200 nanosecond acquisition time sample-hold. This configuration obtains a 600 KHz (minimum) throughput rate. An optional end-point calibration circuit may also be used. The optional calibration circuit has no effect on the throughput rate.

This capability is based upon the sample-hold acquisition and hold mode settling times occurring during the ADC-511's analog input settling time period of 600 nanoseconds. This timing relationship is shown in Figure 5. The optional calibration circuit would also use this time period in settling to the required accuracy before the ADC-511 determines the seven most significant bits of data.

The SHM-45 is put into the sample mode when the $\overline{\text{HOLD COMMAND}}$ is high. For continuous conversions, the sample mode would be initiated upon $\overline{\text{EOC}}$ going low.

Upon completion of the SHM-45's acquisition mode (200 nanoseconds maximum), there is still an additional 400 nanoseconds required to meet the analog input settling time of the ADC-511. The SHM-45 requires 100 nanoseconds for hold mode settling. The user would adapt the START CONVERT pulse width to meet the additional time required for analog input settling. There is a 20 nanosecond minimum delay from START CONVERT low to $\overline{\text{EOC}}$ high. Therefore, if the START CONVERT pulse goes high as the $\overline{\text{HOLD COMMAND}}$ goes low, the start convert pulse width would be 380 nanoseconds wide.

As long as the 600 nanosecond analog input settling time is met, the time in the acquisition or hold mode could be varied as long as the minimum times are observed.



NOTE: NOT DRAWN TO SCALE

Figure 5. ADC-511 and SHM-45 Timing Diagram

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SEAL
ADC-511MC	0 °C to +70 °C	Hermetic
ADC-511MM	-55 °C to +125 °C	Hermetic

ACCESSORIES

Part Number	Description
TP10K	Trimming Potentiometer
TP50	Trimming Potentiometer

A receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 24 required.

For high-reliability versions of the ADC-511, contact DATEL.

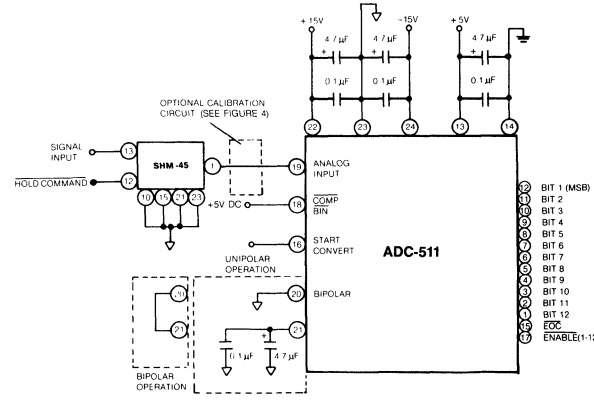


Figure 6. ADC-511 and SHM-45 Connection Drawing

ADC-520, ADC-521
12-Bit, Ultra-Fast, Low-Power A/D Converters

FEATURES

- **12-Bit resolution**
- **800 Nanosecond maximum conversion time**
- **Pin-programmable input ranges**
- **Internal high impedance buffer**
- **Low 1.6 Watts power consumption**
- **Three-state output buffers**
- **Small 32-pin DIP**

GENERAL DESCRIPTION

DATEL's ADC-520 and ADC-521 are 12-bit analog-to-digital converters with conversion speeds of up to 800 nanoseconds.

Both models are identical except for the analog input voltage ranges. The ADC-520 has input voltage ranges of ±10V, 0 to +10V, 0 to +20V and 0 to -20 Volts dc. The ADC-521 has input voltage ranges of ±2.5V and 0 to +5 Volts dc. Both models have internal buffer amplifiers.

The performance of these converters is based upon a digitally-correcting subranging architecture. DATEL further enhances this technology by using unique laser trimming schemes. The ADC-520 and ADC-521 are packaged in a 32-pin ceramic DIP and consume 1.6 watts.

All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in two's complement, complementary two's complement, straight binary/offset binary or complementary binary/complementary offset binary.

Both models require ±15V dc and +5V dc power. Models are available in the commercial 0 °C to +70 °C and military -55 °C to +125 °C operating temperature range. Typical applications include spectrum, transient, vibration and waveform analysis.

These devices are also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems. For information on versions with high reliability screening, contact the factory.

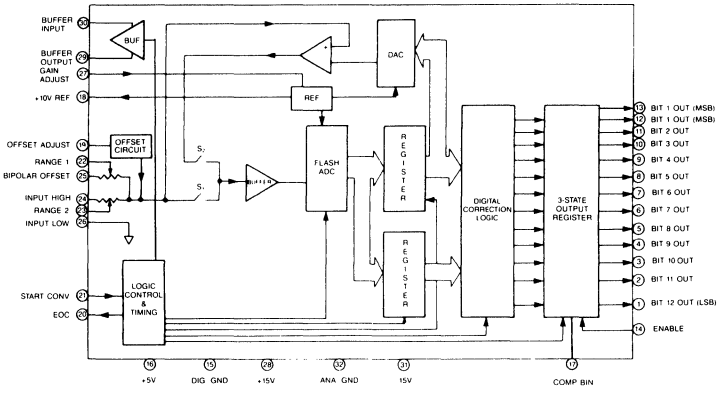
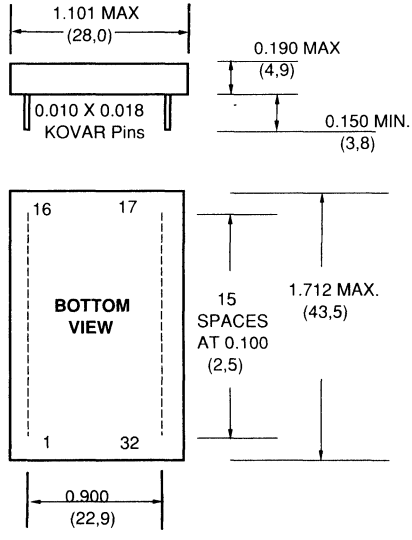


Figure 1. ADC-520, ADC-521 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	BIT 12 OUT (LSB)
2	BIT 11 OUT
3	BIT 10 OUT
4	BIT 9 OUT
5	BIT 8 OUT
6	BIT 7 OUT
7	BIT 6 OUT
8	BIT 5 OUT
9	BIT 4 OUT
10	BIT 3 OUT
11	BIT 2 OUT
12	BIT 1 OUT (MSB)
13	BIT 1 OUT (MSB)
14	ENABLE
15	DIGITAL GROUND
16	+5V
17	COMP BIN
18	REF. OUT (+10V dc)
19	OFFSET ADJUST
20	EOC
21	START CONVERT
22	RANGE 1
23	RANGE 2
24	INPUT HIGH
25	BIPOLAR OFFSET
26	INPUT LOW
27	GAIN ADJUST
28	+15V
29	BUFFER OUTPUT
30	BUFFER INPUT
31	-15V
32	ANALOG GROUND

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 28)	0 to +18	Volts dc
-15V Supply (Pin 31)	0 to -18	Volts dc
+5V Supply (Pin 16)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 14, 17, 21)	-0.3 to +6.0	Volts dc
Analog Input (Pin 24)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and over the operating power supply range unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Range				
(ADC-520)	–	±10	–	Volts dc
	–	0 to +10	–	Volts dc
	–	0 to +20	–	Volts dc
	–	0 to -20	–	Volts dc
(ADC-521)	–	±2.5	–	Volts dc
	–	0 to +5	–	Volts dc
Input Impedance				
(ADC-520)				
Unipolar:	1.75	2.5	–	K Ohms
Bipolar:	3.75	5.0	–	K Ohms
(ADC-521)				
Unipolar:	2.0	2.5	–	K Ohms
Bipolar:	1.6	2.0	–	K Ohms
Input Capacitance	–	–	50	pf
Buffer Amplifier				
Input Voltage	+10	–	–	Volts dc
Input Impedance	–	10^{12}	–	Ohms
Settling Time	–	700	1000	nSec.
DIGITAL INPUTS				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	2.5	µA
Logic Loading "0"	–	–	-100	µA
OUTPUTS				
Resolution	12	–	–	Bits
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	9.98	10.0	10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Output Coding				
(Pin 17 Hi)	Straight binary/offset binary			
(Pin 17 Low)	Complementary binary Complementary offset binary			
(Note 4)	Two's complement			
(Note 4)	Complementary two's complement			

* +5V power usage at 1 TTL logic loading per data output bit.

① Specifications cited are at +25 °C. See Technical Note 1 for further information.

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Integral Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	±3	LSB
Integral Non-Lin. Tempco	–	±3	±8	ppm/ °C
Differential Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	±1	LSB
Differential Non-Lin. Tempco	–	–	±2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	±3	±8	LSB
0 °C to +70 °C	–	±4	±14	LSB
-55 °C to +125 °C	–	±8	±29	LSB
Unipolar Operation				
Zero Error ①	–	±1	±5	LSB
Zero Tempco	–	±13	±25	ppm/ °C
Zero Adjust Range	±5	–	–	LSB
Bipolar Operation				
Zero Error ①	–	±1	±5	LSB
Zero Tempco	–	±2	±5	ppm/ °C
Zero Adjust Range	±5	–	–	LSB
Offset Error ①	–	±2	±5	LSB
Offset Tempco	–	±17.5	±35	ppm/ °C
Offset Adjust Range	±5	–	–	LSB
Gain Error ①	–	±2	±5	LSB
Gain Tempco	–	±17.5	±35	ppm/ °C
Gain Error Adjust Range	±5	–	–	LSB
Conversion Times				
+25 °C	–	–	800	nSec.
0 °C to +70 °C	–	–	850	nSec.
-55 °C to +125 °C	–	–	880	nSec.
No Missing Codes (12 Bits)	Over the Operating Temperature Range			
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+52	+65	mA
-15V dc Supply	–	-36	-45	mA
+5V dc Supply*	–	+66	+70	mA
Power Dissipation	–	1.6	1.9	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-Pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 20K ohm trimming potentiometer for gain adjustment with the wiper tied to pin 27. Use a 20K ohm trimming potentiometer with the wiper tied to pin 19 for zero/offset adjustment. To operate without adjustment, ground pin 27 and leave pin 19 open.

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass the analog and digital supplies and the +10V reference (pin 18) to their respective grounds with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 18) to analog ground (pin 32) the same way.

4. Obtain straight binary/offset binary output coding by typing $\overline{\text{COMP BIN}}$ (pin 17) to +5V dc or leaving it open. The device has an internal pull-resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. In the bipolar mode, two's complement output coding is available by using the $\overline{\text{MSB}}$ output (pin 13). The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. Enable the three-state outputs by connecting $\overline{\text{ENABLE}}$ (pin 14) to a logic "0" (low). The $\overline{\text{ENABLE}}$ signal has no effect on $\overline{\text{MSB}}$ (pin 13) which is not a three-state output and therefore is not controlled by the enable pin.

6. Satisfy high-speed drive requirements of the ADC-520 and ADC-521 with a wide-bandwidth, low output impedance input source such as Datel's SHM-45 sample-and-hold or AM-1435 amplifier.

7. The ADC-520 and ADC-521 provide an internal buffer amplifier. Using this buffer provides an input impedance of 10^{12} Ohms, allowing the A/D to be driven from a high impedance source or directly from an analog multiplexer. When using the input buffer, allow a delay equal to its settling time between input level change and the negative going edge of the START CONVERT pulse. If the buffer is not required, its input should be connected to analog ground to avoid introducing noise into the converter.

THEORY OF OPERATION

The ADC-520 and ADC-521 employ a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses seven bits of a single flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, block diagram, and timing diagram as needed.

The ADC-520 and ADC-521 require a maximum of 250 nanoseconds for the input signal to settle before starting a conversion. Conversion being initiated, switch S1 of the ADC closes and S2 opens. The input, having been configured for the appropriate range, is buffered and then digitized to seven bits by the flash ADC to determine the seven most signifcant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

The first pass finished, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least seven significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{\text{EOC}}$ goes low, indicating the conversion is complete, and the output passes to the three-state output buffers.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{\text{EOC}}$ goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The ADC-520 and ADC-521's conversion rate is based upon 250 nanoseconds for input settling time and 800 nanoseconds conversion time, yielding a minimum of 950 KHz conversion rate. Re-triggering of the START CONVERT pulse before $\overline{\text{EOC}}$ goes low will not initiate a new conversion.

INPUT CONNECTIONS

Table 2a. ADC-520 Input Connections

INPUT RANGE	INPUT PIN W/O BUFFER	INPUT PIN WITH BUFFER	CONNECT
±10V dc	Pin 24	Pin 30, tie 29 to 24	Pin 18 to 25
0 to +10V dc	Pin 24	Pin 30, tie 29 to 24	Pin 24 to 25
0 to +20V dc	Pin 24	DO NOT USE	Pin 26 to 25
0 to -20V dc	Pin 25	DO NOT USE	Pin 18 to 24, 22 to 23 to 24

Table 2b. ADC-521 Input Connections

INPUT RANGE	INPUT PIN W/O BUFFER	INPUT PIN WITH BUFFER	CONNECT
±2.5V dc	Pin 24,22,23	Pin 30, tie 29 to 24	Pin 25 to 18
0 to +5V dc	Pin 24,22,23	Pin 30, tie 29 to 24	Pin 25 to 26

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

ADC-520/521 T1 Timing Over Temperature

TEMPERATURE:	+25 °C	0 °C to +70 °C	-55 °C to +125 °C
Conversion Time(T1) MAX.	800 nS	850 nS	880 nS

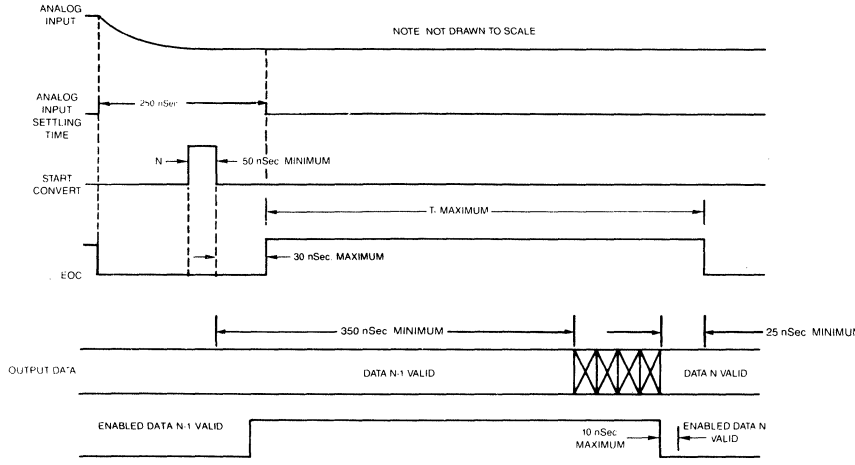


Figure 2. ADC-520, ADC-521 Timing Diagram

Table 1. Signal Timing Summary

LINE	DURATION IN NANOSECONDS
START CONVERT Pulse Width	50 nSec minimum
Analog Input Settling Time	250 nSec maximum
START CONVERT Low to EOC High Propagation Delay	30 nSec maximum
START CONVERT Low to Previous Output Data Invalid	350 nSec minimum
Data Valid Before EOC goes Low	25 nSec minimum
ENABLE to Output Data Valid Propagation Delay	10 nSec maximum

CALIBRATION PROCEDURE

Remove system errors or the small initial errors as follows:

1. Connect the converter per Figure 3 and Tables 2a and 2b for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 21) at a rate of 500 KHz. This rate reduces flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
Apply a precision voltage reference source between the analog input and ground. Refer to Table 2a and 2b for the correct input pin. Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ 1/2 LSB) or the bipolar zero adjustment (zero +1/2 LSB) for the appropriate FSR. For unipolar,adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 17) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN pin tied low (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 17) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 17) tied low (complementary offset binary).

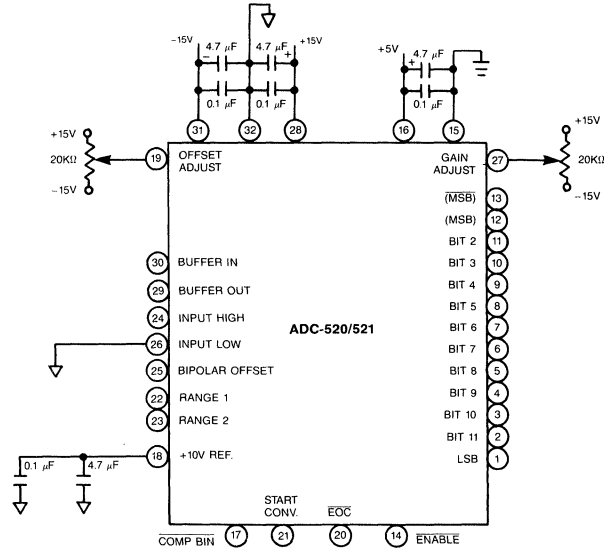


Figure 3. ADC-520, ADC-521 Calibration Circuit

Calibration (Cont.)

Two's complement and complementary two's complement requires the use of $\overline{\text{MSB}}$ (pin 13) versus MSB (pin 12) as given for offset binary or complementary offset binary respectively.

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for $\overline{\text{COMP BIN}}$ (pin 17) tied high or between 0000 0000 0001 and 0000 0000 0000 for $\overline{\text{COMP BIN}}$ pin tied low. Two's complement and complementary two's complement respectively requires using $\overline{\text{MSB}}$, pin 13.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

Table 3a. Zero and Gain Adjust, Unipolar Operation

UNIPOLAR FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +5V dc	+.610 mV dc	+4.9971V dc
0 to +10V dc	+1.22 mV dc	+9.9963V dc
0 to +20V dc	+2.44 mV dc	+19.9927V dc
0 to -20V dc	-2.44 mV dc	-19.9927V dc

Table 3b. Zero and Gain Adjust, Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
+10V dc	+2.44 mV dc	+9.9927V dc
+2.5V dc	+.610 mV dc	+2.4982V dc

Table 4. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES,VOLTS dc			OUTPUT CODING	
				STRAIGHT BINARY	COMP. BINARY
	0 to +5V	0 to +10V	0 to +20V	MSB LSB	MSB LSB
+FS-1LSB	+4.9988V	+9.9976V	+19.9951V	1111 1111 1111	0000 0000 0000
7/8 FS	+4.3750V	+8.7500V	+17.500V	1110 0000 0000	0001 1111 1111
3/4 FS	+3.7500V	+7.5000V	+15.000V	1100 0000 0000	0011 1111 1111
1/2 FS	+2.5000V	+5.0000V	+10.000V	1000 0000 0000	0111 1111 1111
1/4 FS	+1.2500V	+2.5000V	+5.0000V	0100 0000 0000	1011 1111 1111
1/8 FS	+0.0024V	+1.2500V	+2.5000V	0010 0000 0000	1101 1111 1111
1 LSB	+0.0012V	+0.0024V	+0.0048V	0000 0000 0001	1111 1111 1110
0	0.0000V	0.0000V	0.0000V	0000 0000 0000	1111 1111 1111

Table 5. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGES,VOLTS dc		OUTPUT CODING		
			OFFSET BINARY	COMP TWO'S COMP	TWO'S COMP.
	±2.5V	±10V	MSB LSB	MSB LSB	MSB LSB
+FS -1 LSB	+2.4988V	+9.9951V	1111 1111 1111	1000 0000 0000	0111 1111 1111
+3/4 FS	+1.8750V	+7.5000V	1110 0000 0000	1001 1111 1111	0110 0000 0000
+1/2 FS	+1.2500V	+5.0000V	1100 0000 0000	1011 1111 1111	0100 0000 0000
0	0.0000V	0.0000V	1000 0000 0000	1111 1111 1111	0000 0000 0000
-1/2 FS	-1.2500V	-5.0000V	0100 0000 0000	0011 1111 1111	1100 0000 0000
-3/4 FS	-1.8750V	-7.5000V	0010 0000 0000	0101 1111 1111	1010 0000 0000
-FS +1 LSB	-2.4988V	-9.9951V	0000 0000 0001	0111 1111 1110	1000 0000 0001
-FS	-2.5000V	-10.000V	0000 0000 0000	1111 1111 1111	1000 0000 0000

THEORY OF OPERATION (ADC-520/521 and SHM-45)

This theory of operation describes the ADC-520 and ADC-521 operation in conjunction with DATEL'S SHM-45. The SHM-45 sample-and-hold device captures fast signals for the ADC-520/521 to then digitize. Figure 4 shows a typical ADC/SHM circuit.

The SHM-45, upon acquiring the input signal on the hold capacitor (200 nanoseconds maximum acquisition time to 0.01%), is put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-520 and ADC-521 require a maximum of 250 nanoseconds for the input signal to settle before starting a conversion. The input of the ADC-520 and ADC-521 starts settling to its final value while the SHM-45 is in the acquisition mode.

At the end of the SHM-45's hold mode settling time, the A/D's input is fully settled. The missing 150 nanoseconds of the required maximum analog input settling time is made up by the time the sample/hold is in the acquisition mode.

To assure the SHM-45 has 200 nanoseconds maximum acquisition time, the START CONVERT pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the START CONVERT pulse should be 105 nanoseconds minimum to assure a hold mode settling time of 100 nanoseconds. The 105 nanoseconds takes into account the min/max propagation delays of the start convert low to $\overline{\text{EOC}}$ high propagation delays.

The overall throughput using the ADC-520/521 and the SHM-45 consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds

Table 6. Performance Characteristics

CHARACTERISTIC	VALUE
Conversion Rate (Changing Inputs):	
+25 °C	950 KHz minimum
0 °C to +70 °C	900 KHz minimum
-55 °C to +125 °C	880 KHz minimum
Harmonic Distortion (Below FS)	
+25 °C	-72 dB minimum
0 °C to +70 °C	-72 dB minimum
-55 °C to +125 °C	-65 dB minimum

for observance of min/max propagation delays and 800 nanoseconds for the conversion process. The system achieves a guaranteed throughput rate of 897 KHz over a period of 1,115 nanoseconds maximum.

Refer to Figure 5 for the ADC-520/521 and SHM-45 timing. The performance characteristics shown in Table 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

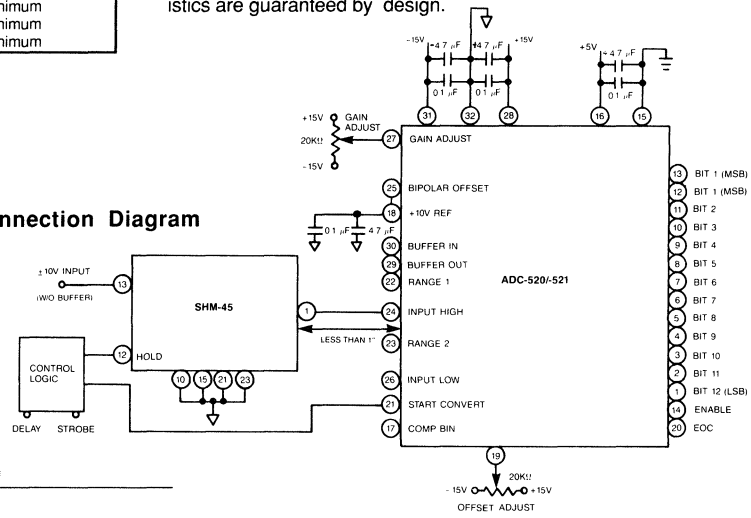


Figure 4. ADC/SHM Connection Diagram

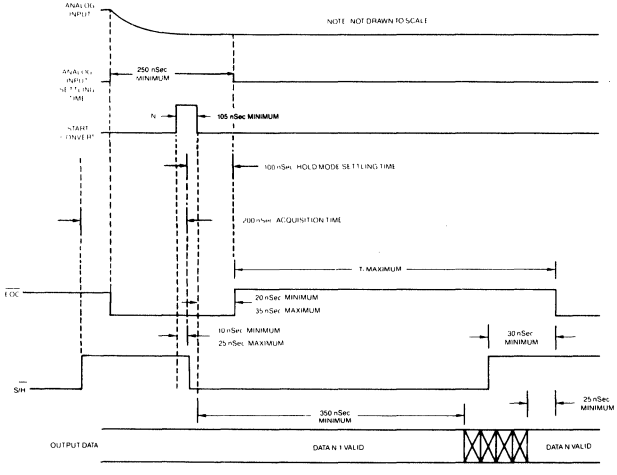


Figure 5. ADC/SHM Timing Diagram

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE
ADC-520MC	0 °C to +70 °C
ADC-520MM	-55 °C to +125 °C
ADC-521MC	0 °C to +70 °C
ADC-521MM	-55 °C to +125 °C

ACCESSORIES

Part Number	Description
TP20K	Trimming Potentiometers (Two required)

Order PC board mounting receptacle through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

For high reliability versions of the ADC-520 and ADC-521 contact the DATEL.

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-5210 Series Adjustment-Free 12-Bit A/D Converters

1

FEATURES

- **13 Microseconds maximum conversion time**
- **Totally adjustment-free**
- **Industry standard converter**
- **High-reliability versions available**
- **Low power consumption**

GENERAL DESCRIPTION

DATEL's ADC-5210 Series are high performance, hybrid, 12-bit successive approximation A/D converters. These devices combine high speed with extreme accuracy to provide the best possible performance in systems that require low power consumption, adjustment free operation, and miniature size.

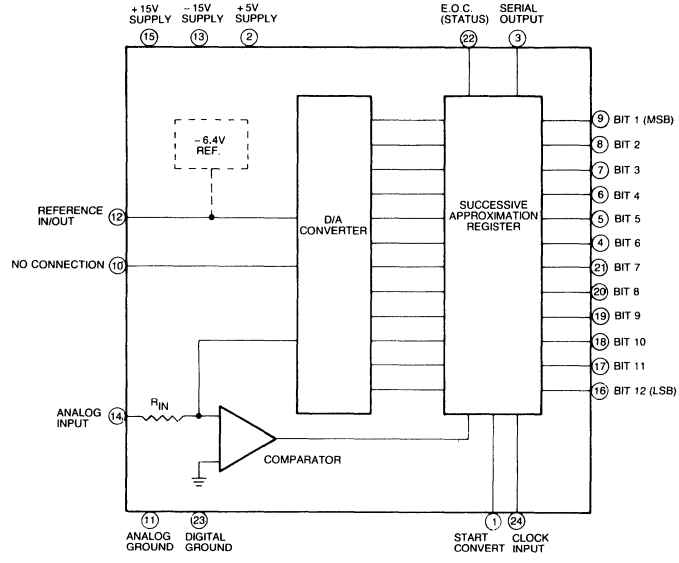
Active laser trimming of highly stable thin-film resistor networks eliminates the need for external adjustment circuits. Full-scale absolute accuracy error is ±0.05% FSR maximum at +25°C and only ±0.4% FSR maximum over the full military operating temperature range. Zero error is a maximum of only ±0.025% FSR. Conversion Time is 13 μseconds maximum, allowing full accuracy with a 1 MHz clock.

These devices are available in three factory set input ranges: 0 to +10V dc, ±5V dc, and ±10V dc. Models are available with an internal reference, or, for improved overall accuracy, requiring an external reference. Each model guarantees no missing codes over the full operating temperature range.

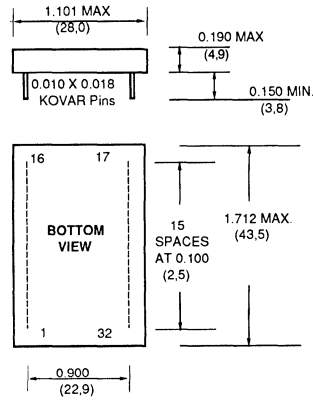
Other significant features include serial or parallel output data, 1W maximum power consumption, and a 10 ppm/°C Gain Tempco. Digital outputs are TTL-compatible and output coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation.

Models are available specified over the full military operating temperature range of −55 to +125°C and commercial, 0°C to +70°, operating temperature ranges.

All models require ±15V dc and +5V dc for operation and are packaged in a 24-pin, hermetically sealed, ceramic package.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STAND OFF FROM CASE, ±0.01

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	13	−15V SUPPLY
2	+5V SUPPLY	14	ANALOG INPUT
3	SERIAL OUTPUT	15	+15V SUPPLY
4	BIT 6 OUT	16	BIT 12 OUT (LSB)
5	BIT 5 OUT	17	BIT 11 OUT
6	BIT 4 OUT	18	BIT 10 OUT
7	BIT 3 OUT	19	BIT 9 OUT
8	BIT 2 OUT	20	BIT 8 OUT
9	BIT 1 OUT (MSB)	21	BIT 7 OUT
10	NO CONNECTION	22	E.O.C. (STATUS)
11	ANALOG GROUND	23	DIGITAL GROUND
12	REF. IN/OUT*	24	CLOCK INPUT

*THE ADC-5211, 5212, AND 5216 HAVE AN INTERNAL REFERENCE. THE ADC-5214 AND 5215 REQUIRE AN EXTERNAL REFERENCE.

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature Range:	
ADC-521X	0°C to +70°C
ADC-521XH	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Positive Supply, Pin 15	+18V
Negative Supply, Pin 13	−18V
Logic Supply, Pin 2	−0.5V to +7V
Analog Input, Pin 14	25V
Digital Inputs, Pins 1, 24	−0.5V to +5.5V
Digital Outputs	Logic Supply
Reference Input[1]	0 to −15V

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, V_{REF} = −10.000V, unless otherwise noted.

ANALOG INPUTS[2]	MODEL NUMBER[1]		MODEL NUMBER[1]	
Input Range (Input Impedance)				
−5V to +5V (5KΩ)	ADC-5211		ADC-5214	
−10V to +10V (10KΩ)	ADC-5212		ADC-5215	
0 to +10V (5 KΩ)	ADC-5216			
TRANSFER CHARACTERISTICS	**TYPICAL**	**MAXIMUM**	**TYPICAL**	**MAXIMUM**
Linearity Error: +25°C	±¼ LSB	±½ LSB	±¼ LSB	±½ LSB
0°C to +70°C	±¼ LSB	±½ LSB	±¼ LSB	±½ LSB
−55°C to +125°C	—	±¾ LSB	—	±¾ LSB
Differential Linearity Error	±½ LSB		±½ LSB	
No Missing Codes	Guaranteed over temperature			
Full-scale Absolute Accuracy Error[3]				
+25°C	±0.025% FSR	±0.05% FSR	±0.025% FSR	±0.05% FSR
0°C to +70°C	±0.1% FSR	±0.2% FSR	±0.05% FSR	±0.1% FSR
−55°C to +125°C	±0.1% FSR	±0.4% FSR	±0.05% FSR	±0.1% FSR
Zero Error: +25°C	±0.01% FSR	±0.025% FSR	±0.01% FSR	±0.025% FSR
0°C to +70°C	±0.025% FSR	±0.05% FSR	±0.025% FSR	±0.05% FSR
−55°C to +125°C	—	±0.05% FSR	—	±0.05% FSR
Zero Error: ADC-5216				
+25°C	—	±0.05% FSR	—	—
0°C to +70°C	—	±0.75% FSR	—	—
−55°C to +125°C	—	±0.75% FSR	—	—
Gain Error	±0.025%	—	±0.025%	—
Gain Drift	±10 ppm/°C	—	±3 ppm/°C	—
Conversion Time[5]	—	13 μsec.	—	13 μsec.
POWER SUPPLIES				
Power Supply Range: ±15V dc supplies	—	±3%	—	±3%
+5V dc supply	—	±5%	—	±5%
Power Supply Rejection[6]: +15V dc supply	±0.005% FSR/%V_S	±0.02% FSR/%V_S	±0.005% FSR/%V_S	±0.01% FSR/V_S
−15V dc supply	±0.01% FSR/%V_S	±0.05% FSR/%V_S	±0.005% FSR/%V_S	±0.01% FSR/V_S
Current Drain: +15V dc supply	+9 mA	28 mA	+9 mA	28 mA
−15V dc supply	−23 mA	−35 mA	−23 mA	−35 mA
+5V dc supply	+35 mA	68 mA	+35 mA	68 mA
±12V dc, +5V dc supplies[11]	—	—	—	—
−10V dc reference[1]	—	—	−1.5 mA	−2 mA
Power Consumption	695 mW	1 W	695 mW	800 mW

DIGITAL INPUTS (All Models)	MINIMUM	TYPICAL	MAXIMUM
Logic Levels: Logic "1"	2.0V	—	—
Logic "0"	—	—	0.8V
Clock Input:			
Pulse Width High	100 nanoseconds	—	—
Pulse Width Low	175 nanoseconds	—	—
Loading High (V_{IN} = 2.4V)	—	2 μA	20 μA
Loading Low (V_{IN} = 0.3V)	—	−0.25 mA	−0.4 mA
Frequency	—	—	1 MHz
Start Convert Input:			
Loading High (V_{IN} = 2.4V)	—	4 μA	40 μA
Loading Low (V_{IN} = 0.3V)	—	−0.25 mA	−0.4 mA
Set-up Time Start Low to Clock[8]	25 nanoseconds	—	—

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

DIGITAL OUTPUTS (All Models)			
Logic Coding[9]: Unipolar range Bipolar ranges	Complementary Straight Binary Complementary Offset Binary		
Logic Levels: Logic "1" Logic "0" Output Drive Capability, All Outputs[10]: Logic "1" Logic "0"	+2.4V — 8 TTL Loads 2 TTL Loads	+3.6V +0.15V — —	— +0.3V — —
REFERENCE INPUT/OUTPUT[1]			
Internal Reference: Voltage Accuracy Tempco of Drift Maximum External Current External Reference: Voltage Loading	— — — — — —	−6.4V ±2% ±5 ppm/°C — −10.000V —	— — — 100 μA −2 mA

FOOTNOTES:

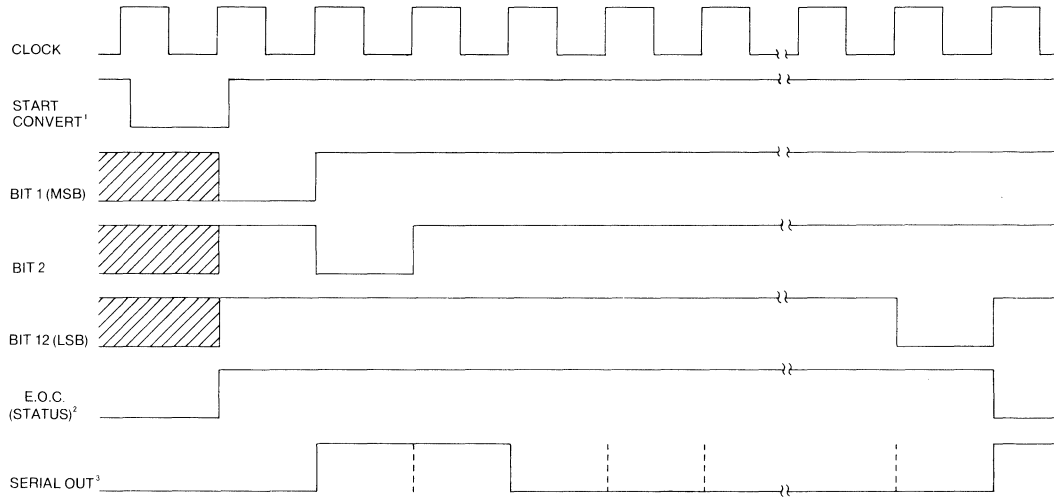
1. The ADC-5211, 5212, and 5216 include a −6.4V internal reference. The ADC-5214 and 5215 require an external −10.000V reference for specified operation.
2. Analog input ranges are internally set at the factory.
3. Absolute Accuracy Error includes offset, gain, linearity and all other errors. See Technical Notes for further information.
4. FSR stands for Full Scale Range and is equal to the peak voltage of the selected analog input range.
5. Conversion Time is defined as the width of the converter's STATUS (E.O.C.) pulse. The ADC-5210 Series will meet all specifications with clock frequencies up to 1 MHz. A 1 MHz clock gives a STATUS pulse that is 12 microseconds wide, however, unless careful timing precautions are taken, it will usually take 13 microseconds to update digital output data.
6. Power Supply rejection is guaranteed over the ±15V ±3% range.
7. The clock may be asymmetrical with minimum positive or negative pulse width.
8. In order to reset the converter, START CONVERT must be brought low at least 25 nanoseconds prior to a low-to-high clock transition. See Timing Diagram.
9. Serial and Parallel output data have the same coding. Serial data is NRZ successive decision pulses out, MSB first, at the clock frequency. Both serial and parallel output data become valid on the same rising clock edge. Serial data is valid on subsequent falling edges, and these edges can be used to clock serial data into receiving registers.
10. One TTL load is defined as sinking 40 μA with a logic 1 applied and sourcing 1.6 mA with a logic 0 applied.
11. For ±12V dc, +5V dc operation, contact the factory.

TECHNICAL NOTES

1. The use of proper layout and decoupling techniques are required to obtain rated performance. The ground pins (pins 11 & 23) are not connected internally, and therefore must be connected externally as directly as possible. They should be connected to the system analog ground, preferably through a large ground plane underneath the package. Power supplies should be bypassed to ground at the supply pins with 1 μF electrolytic capacitors in parallel with 0.01 F ceramic capacitors.
2. These converters can be made to continuously convert by tying the E.O.C. output (Pin 22) to the start convert input (Pin 1). When connected in this manner, the E.O.C. (START CONVERT) will go low at the end of conversion and the next rising edge of the clock will reset the converter and bring the E.O.C. (START CONVERT) high again. The MSB will be set on the next rising clock edge. The E.O.C. (status) will be low for approximately one clock period following each conversion.
3. The absolute accuracy error of an A/D converter is defined as the difference between the theoretical analog input voltage required to produce a given digital output and the unadjusted analog input voltage actually required to produce the same code. Because this error is measured and specified without adjustment, it includes all factors that may affect the devices accuracy at the point of measurement: offset error, linearity error, gain error, and noise error.
4. Because of propagation delays, the LSB of any given conversion may not be valid until a maximum of 30 nanoseconds after the E.O.C. (status) output has returned low. If the E.O.C. is used to strobe latches holding output data, adequate delays must be provided. Gate delays may be employed or the E.O.C. can be made the input of a D flip flop whose clock input is the same as the converter clock. Connected in this manner, the Q output will change one clock period after the E.O.C. changes. If the converter is connected in the continuous mode, the E.O.C. can be NORed with the converter clock to produce a positive strobe pulse ½ period wide, ½ period after the E.O.C. output has gone low. The rising edge of the pulse can be used to latch data after each conversion.
5. Applications of these converters that require the use of sample-hold may be satisfied by DATEL's SHM-4860, a high speed hybrid unit featuring a 200 nanosecond acquisition time and 0.01% accuracy.

TIMING & CONNECTION

TIMING DIAGRAM



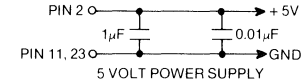
NOTES: 1. The converter is reset by holding the START CONVERT low during a low to high clock transition. The START CONVERT must be low for a minimum of 25 nanoseconds prior to the clock transition. After the START is set high, the conversion will begin on the next rising clock edge. The START CONVERT may be set low at any time during a conversion to reset and begin again.

2. At the end of conversion, the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
3. The serial output is non-return to zero.

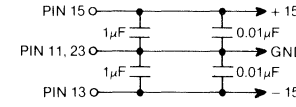
DIGITAL OUTPUT CODING

DIGITAL OUTPUT	ANALOG INPUT VOLTAGE		
	0 TO +10V ADC-5216	±5V ADC-5211, 5214	±10V ADC-5212, 5215
0000 0000 0000	+10.0000V	+5.0000V	+10.0000V
0000 0000 0001	+9.9976V	+4.9976V	+9.9951V
0111 1111 1111	+5.0024V	+0.0024V	+0.0049V
1000 0000 0000	+5.0000V	0.0000V	0.0000V
1111 1111 1110	+0.0024V	−4.9976V	−9.9951V
1111 1111 1111	0.0000V	−5.0000V	−10.0000V

POWER SUPPLY DECOUPLING

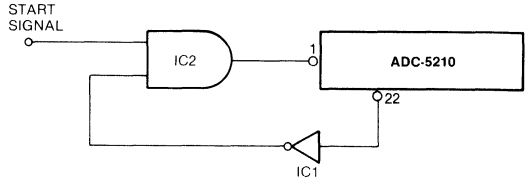


5 VOLT POWER SUPPLY



± 15 VOLT POWER SUPPLY

TRIGGERING WITH A POSITIVE EDGE



The ADC-5210 Series A/D's may be made to start converting on a positive going edge by employing the circuit shown. The rising edge of the start signal will drive the output of IC2 low. The converter will reset on the next rising clock edge. When the converter resets, the status output (pin 22) goes high, the output of IC1 goes low; and since the start signal is still high, the output of IC2 goes high allowing the conversion to continue immediately. The start signal should be brought low before the conversion is complete.

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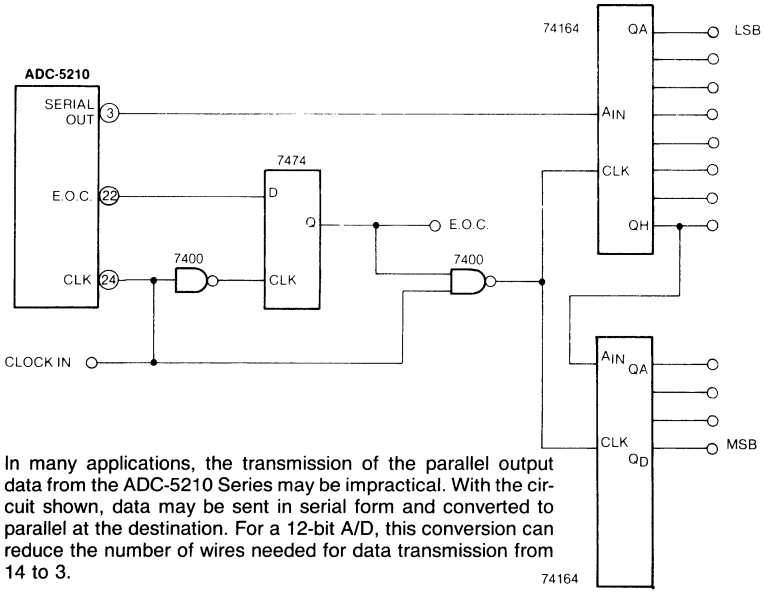
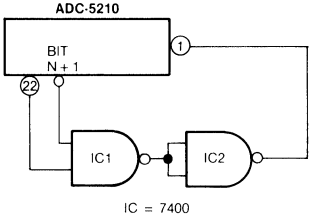
APPLICATIONS

SERIAL TO PARALLEL CONVERSION



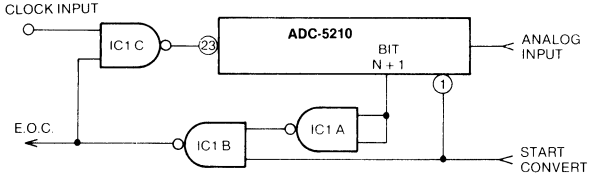
In many applications, the transmission of the parallel output data from the ADC-5210 Series may be impractical. With the circuit shown, data may be sent in serial form and converted to parallel at the destination. For a 12-bit A/D, this conversion can reduce the number of wires needed for data transmission from 14 to 3.

SHORT CYCLE — CONTINUOUS CONVERTING



To continuously convert at N bits, the circuit shown may be used. The output of bit (N + 1) acts like a status when one converts at N bits. The START CONVERT input is made the AND function of bit (N + 1) and the STATUS output to prevent the possibility of a lock up condition at power-on.

SHORT CYCLE OPERATION



IC1 SN7400N QUAD NAND GATE

If an application requires less than 12 bits resolution, the ADC-5210 Series may be truncated to the desired number of bits, with a proportionate decrease in conversion time, by using the circuit shown. With this circuit the start convert and E.O.C. signals function normally.

ORDERING INFORMATION

MODEL NO.	INPUT VOLT. RANGE	REFERENCE	OPERATING TEMP. RANGE
ADC-5211	±5V	Internal	0 to +70°C
ADC-5211H	±5V	Internal	−55 to +125°C
ADC-5212	±10V	Internal	0 to +70°C
ADC-5212H	±10V	Internal	−55 to +125°C
ADC-5214	±5V	External	0 to +70°C
ADC-5214H	±5V	External	−55 to +125°C
ADC-5215	±10V	External	0 to +70°C
ADC-5215H	±10V	External	−55 to +125°C
ADC-5216	0 to +10V	Internal	0 to +70°C
ADC-5216H	0 to +10V	Internal	−55 to +125°C

For military devices compliant to MIL-STD-883, consult the factory.

ADC-7109
12-Bit A/D Converter with Microprocessor Interface

FEATURES

- **Parallel or serial bus interface**
- **12 Bits with plus sign and overrange**
- **Differential signal and reference inputs**
- **Low noise**
- **Low power**

GENERAL DESCRIPTION

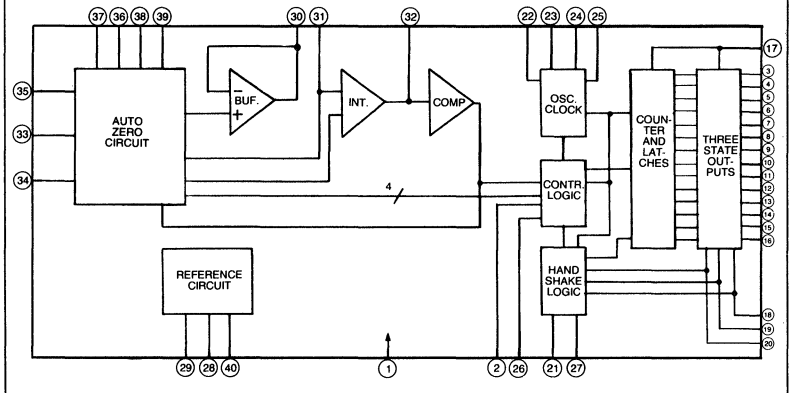
DATEL's ADC-7109 is a low power, 12-bit integrating A/D converter designed to interface directly to 8- or 16-bit μP data busses without any external active component requirements. Output data may be accessed directly under the control of two byte enable and chip select inputs for parallel bus interface or data may be transmitted serially via industry standard UART in the handshake mode.

The ADC-7109 is completely self contained including a buffer amplifier, integrator, comparator, clock oscillator with scaling circuit, 12-bit binary counter with output latches and TTL-compatible three-state output drivers, data bus control and UART handshake logic.

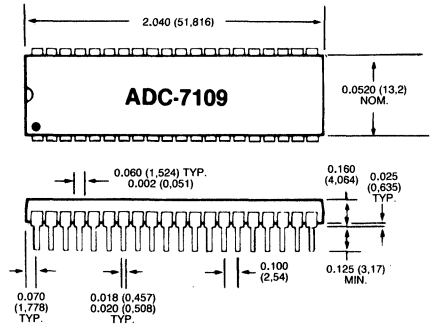
Important features of the ADC-7109 include a typical input bias current of 1 pA, less than 1 μV/°C zero drift, typical input noise of 15 $\mu V_{peak\text{-}to\text{-}peak}$ and a power consumption of only 20 mW. The combination of μP compatibility, low cost and high accuracy make the ADC-7109 an ideal choice for remote data logging applications and true differential analog and reference inputs allow for measurement of bridge type transducers.

The ADC-7109 is available for operation over the commercial, 0°C to +70°C temperature range and is packaged in a 40-pin plastic DIP.

NOTE: The ADC-7109 is a CMOS device. However, all the inputs are fully protected against static discharge and no special handling precautions are necessary.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIG. GND.	21	MODE
2	STATUS	22	OSC IN
3	POLARITY	23	OSC OUT
4	OVERRANGE	24	OSC SELECT
5	BIT 12	25	BUF OSC
6	BIT 11	26	RUN/HOLD
7	BIT 10	27	SEND
8	BIT 9	28	$-V_S$
9	BIT 8	29	REF OUT
10	BIT 7	30	BUFFER
11	BIT 6	31	AUTO ZERO
12	BIT 5	32	INTEGRATOR
13	BIT 4	33	COMMON
14	BIT 3	34	-INPUT
15	BIT 2	35	+INPUT
16	BIT 1	36	+REF IN
17	TEST	37	+REF CAP
18	$\overline{LBEN}$	38	-REF CAP
19	$\overline{HBEN}$	39	-REF IN
20	$\overline{CE/LOAD}$	40	$+V_S$

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ABSOLUTE MAXIMUM RATINGS	
$+V_S$	+6.2V
$-V_S$	−9V
Analog Input Voltage Range[1]	$+V_S$ to $-V_S$
Reference Input Voltage Range[1]	$+V_S$ to $-V_S$
Digital Input Voltage Range (Pins 2-27)[2]	$+V_S$ +0.3V, GND −0.3V
Power Dissipation	500 mW at 70°C

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V Supplies unless otherwise noted.

ANALOG INPUT CHARACTERISTICS	
Type Analog Input	Differential
Zero Input Reading, max. (Octal Reading)[3]	$+0000_8$
Ratiometric Reading, max. (Octal Reading)[4]	4000_8
Input Leakage Current, max. (V_{IN} = 0V)	10 pA
Common Mode Rejection Ratio[13]	86 dB
Input Common Mode Voltage Range, min.	$-V_S$ plus 1.5V
max.	$+V_S$ minus 1.0V

DIGITAL INPUT	
Control I/O Pull-up Current[5]	5 µA
Control I/O Loading, max.[6]	50 pF
Input Voltage Range[7] (Pins 18-21, 26, 27)	
High, min.	2.5V
Low, max.	1V
Input Pull-up Current[8] (Pins 26, 27)	5 µA
(Pins 17, 24)	25 µA
Input Pull-down Current (Pin 21)[9]	5 µA
Mode Input Pulse Width, min.	50 nsec.

OUTPUT CHARACTERISTICS	
Output Voltage,[10] high min.	3.5V at 100 µA
low max.	0.4V at 1.6 mA
Output Leakage Current, max. (Pins 3-16)	1 µA
Reference Output Voltage, min.	−2.4V
max.	−3.2V
Oscillator Output Current,[11] high	1 mA
low	1.5 mA
Buffered Oscillator Output Current,[11] high	2 mA
low	5 mA

PERFORMANCE	
Resolution	12-bits, plus sign and overrange
Non-Linearity, max.	±1 Count
Roll-over Error[12]	±1 Count
Noise, peak-to-peak[14]	15 µV
Zero Drift, max.	1 µV/°C
Scale Factor Tempco, max.[15]	5 ppm/°C
Reference Output Tempco[16]	80 ppm/°C

FOOTNOTES:

1. Positive or negative input. Input voltage can exceed the supply voltage provided the input current is limited to 100 µA.
2. It is recommended that no inputs from sources other than the devices power supply be applied to the device before its power supply is established, and that in multiple supply systems, the supply to the device be activated first. This will avoid destructive device latchup.
3. Vin = 0.0V, Full-Scale = 409.6 mV.
4. Vin = Vref = 204.8 mV.
5. Pins 18, 19, 20. Vout = $+V_s$ minus 3V. Mode input at ground.
6. $\overline{HBEN}$ (Pin 19) $\overline{LBEN}$ (pin 18).
7. With respect to ground.
8. Vout = $+V_s$ minus 3V.
9. Vout = Ground plus 3V.
10. Pins 2 through 16, 18, 19 and 20.
11. Vout = 2.5V.
12. Difference in reading for equal positive and negative inputs near full-scale.
13. Vcm ± 1V, Vin = 0V. Full-scale = 409.6 mV.
14. Not exceeded 95% of the time.
15. Vin = 408.9 mV. External reference tempco = 0 ppm/°C.
16. 25 kΩ between $+V_s$ and reference output.
17. Vin = 0. Crystal oscillator 3.58 MHz. Pins 2-21, 25, 26, 27, 29, open.

POWER REQUIREMENTS	
Supply Voltage	±5V dc
Supply Current ($+V_s$ to GND.) max.[17]	1.5 mA
Supply Current ($+V_s$ to $-V_s$) max.[17]	1.5 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (soldering 60 sec.)	300°C
Package	40 Pin Plastic DIP

1

TECHNICAL NOTES

1. Differential voltages from 1.0V below the positive supply to 1.5V above the negative supply can be applied to the device's input. In this range, the system has a typical CMRR of 86 dB. However, since the integrator also swings with the common mode voltage, care must be taken to assure that the integrator output does not saturate. To avoid this, the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.
2. The buffer amplifier and integrator have a Class A output stage with 100 µA of quiescent current. They supply 20 µA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For a full-scale range of 4.096V, 200 kΩ is optimum; for 409.6 mV, 20 kΩ should be used. For other values of full-scale: $R_{INT} = V_{FS}/20\ \mu A$.
3. The integrating capacitor should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3V from either supply). The value for the integrating capacitor is given by the following equation: $C_{INT} = (2048 \times T_{CLOCK})\ (20\ \mu A)$/Integrator V_{OUT} Swing. The integrating capacitor should be selected to have low dielectric absorption to prevent roll-over errors. Many types of capacitors are adequate for this application, however, polypropylene capacitors will give undetectable errors up to +70°C.
4. The value of the auto zero capacitors depends upon the requirements of the applications. For example, for a full-scale voltage range of 409.6 mV, where noise is a major consideration and the integrating resistor is very small, a value of C_{AZ} twice C_{INT} is optimum. Similarly, for a full-scale range of 4.096V, where recovery is more important than noise, a value of C_{AZ} equal to half C_{INT} is recommended.
5. The analog input required to generate a full-scale output of 4096 counts is $V_{IN} = 2\ V_{REF}$. Thus, for a normalized scale, a reference of 2.048V should be used for a 4.096V full-scale, and 204.8 mV for a 0.4096V full-scale. However, in many applications where the A/D is sensing the output from a transducer, a scale factor other than the unity between the absolute output voltage to be measured and a desired digital output will exist. For example, in a weighing system, a full-scale reading may be desired with 0.682V from the transducer. In this case, rather than dividing the input down to 409.6 mV, it should be applied directly and a reference voltage of 0.341V should be used. Values for R_{INT} and C_{INT} would be 34K and 0.15 µF.

6. The stability of the reference is a major factor in the overall absolute accuracy of the converter. It is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

If using the internal reference, REF OUT (Pin 29) should be connected to −REF IN (Pin 39), and +REF IN should be connected to the wiper of a precision trimpot between REF OUT and $+V_S$. (See typical connections.)

PIN DESCRIPTION

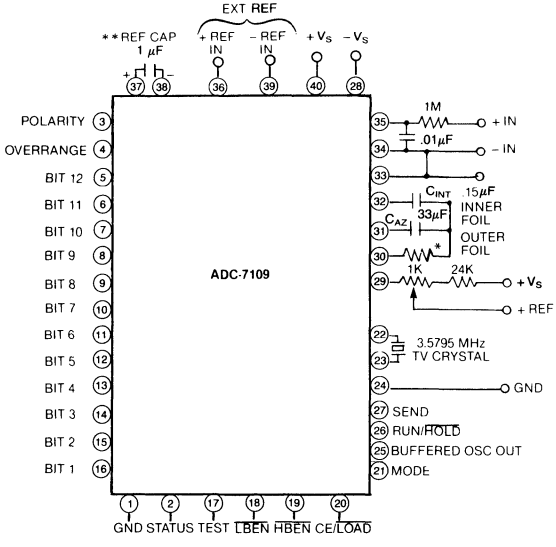
INPUT/OUTPUT CONNECTION AND DESCRIPTION

PIN	FUNCTION	DESCRIPTION
1	DIGITAL GROUND	Ground return for all digital logic.
2	STATUS	Output — High during integrate and deintegrate until data is latched. — Low when analog section is in Auto-Zero configuration.
3	POLARITY	High for Positive Input
4	OVER-RANGE	High if Overranged
5	Bit 12 (MSB)	Data Bits. Three-State Output
6	Bit 11	
7	Bit 10	
8	Bit 9	
9	Bit 8	
10	Bit 7	
11	Bit 6	
12	Bit 5	
13	Bit 4	
14	Bit 3	
15	Bit 2	
16	Bit 1 (LSB)	
17	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high, and disables internal clock. When returned high and 1 clock pulse is input, the counter outputs will enter negative state. Must be tied high if not used. Note: This input is used for test purposes only.
18	$\overline{\text{LBEN}}$	Low Byte Enable — With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8.
19	$\overline{\text{HBEN}}$	High Byte Enable — With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, polarity and overrange outputs.
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load — With Mode (Pin 21) low, $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1-B12, polarity and overrange outputs are disabled. — With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode.
21	MODE	Input Low — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode. Input High — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and will be valid at the end of conversion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SELECT	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. — Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Must be tied high if not used.
28	$-V_S$	Negative Supply Voltage — Nominally −5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally, 2.8V down from $+V_S$ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Mode Select
32	INTEGRATOR	Integrator Output
33	COMMON	Analog Common — System is auto-zeroed to COMMON.
34	− ANALOG IN	Negative Differential Analog Input
35	+ ANALOG IN	Positive Differential Analog Input
36	+ REF IN	Positive-Differential Reference Input
37	+ REF CAP	Positive Reference Capacitor Connection
38	− REF CAP	Negative Reference Capacitor Connection
39	− REF IN	Negative Differential Reference Input
40	$+V_S$	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

TIMING AND CONNECTION

TYPICAL CONNECTION

(TEST CIRCUIT)

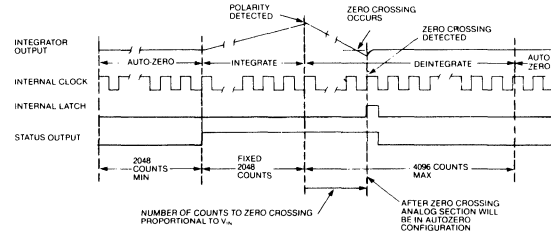


* R_{INT} = 20K FOR 0.2V REF
200K FOR 2.0V REF

** IF USING 409-6 mV SCALE AND HIGH CMV EXISTS, USE 10μF REF. CAP.

NOTES: INPUTS SHOULD SWING FROM GND TO +V_S FOR MINIMUM POWER CONSUMPTION. TTL DRIVEN INPUT SHOULD HAVE 3-5KΩ PULL-UP RESISTORS ADDED FOR MAXIMUM NOISE IMMUNITY.

CONVERSION TIMING



THE CONVERSION PROCESS

There are three steps in the conversion process for the ADC-7109:

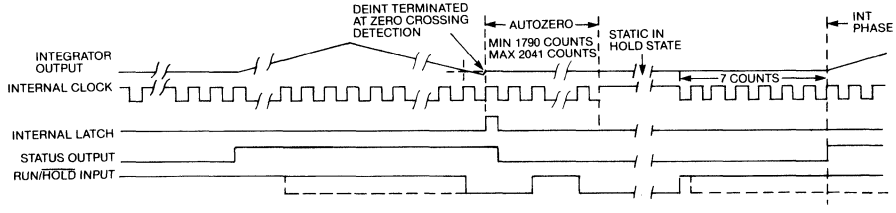
1. Auto Zero
2. Signal Integrate
3. Deintegrate

In the auto zero step, the high and low inputs are internally disconnected from the pins and shorted to analog common. At this point, the reference capacitor is charged to the reference voltage. Then a feedback loop is closed to charge the autozero capacitor (C_{AZ}) which compensates for offset voltages in the buffer amplifier, integrator and comparator. The offset referred to the input is less than 10 μV.

In the signal integrate step, the auto-zero loop is opened and the inputs are connected (internally) back to the external pins. At this point, the differential signal between the inputs is integrated for a fixed time of 2048 clock periods. Upon completion of this phase, the polarity of the integrated signal is determined.

The deintegrate step is the final phase. Here, the negative input is connected to analog common and the positive input is connected across the previously charged reference capacitor, which returns the integrator output to the zero crossing (from auto-zero step) with a fixed slope. Thus, the time for the output to return to zero is proportional to the input signal.

RUN/HOLD OPERATION



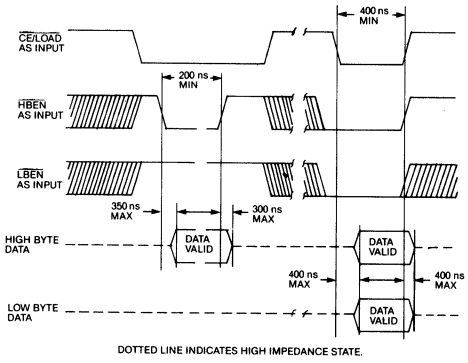
NOTE

The conversion rate is determined by the clock rate (8192 clock periods per cycle) with the RUN/HOLD input left open or connected to +V_S.

If RUN/HOLD goes low any time during the Deintegrate phase after zero crossing has occurred, the deintegrate phase will terminate and the converter will go to auto zero. This feature can be used to save time in deintegrate after zero crossing.

TIMING AND OPERATION

DIRECT MODE OUTPUT



With MODE input low, the data outputs (bits 1-8 low order byte, bits 9-12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are active low, and are provided with pullup resistors to ensure an active high level when left open.

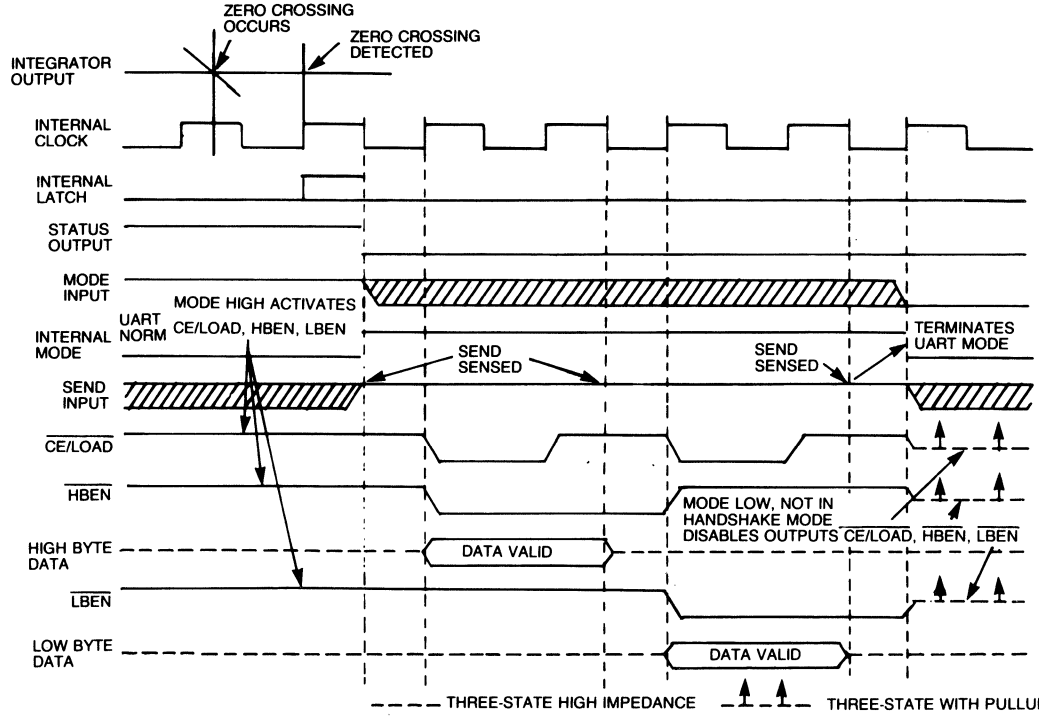
Note that the control inputs are asynchronous with respect to the internal clock—the data may be accessed at any time. Therefore it is possible to access the data while it is being updated which could result in scrambled output data. To prevent this, the access of data should be synchronized with the conversion cycle by monitoring the STATUS output. Data is never updated while STATUS is low.

HANDSHAKE MODE

The handshake mode is an alternative means of interfacing the ADC-7109 to digital systems. In this mode, the A/D actively controls the flow of data rather than passively responding to chip and byte enable inputs and can be interfaced directly to industry standard UART's with no external logic.

The device enters the handshake mode when the MODE input is held high after new data has entered the output latches at the end of every conversion performed. (See timing diagrams.) The MODE input may also be used to trigger entry into the handshake mode on demand. Any time during the conversion cycle,

HANDSHAKE TIMING WITH SEND HELD POSITIVE



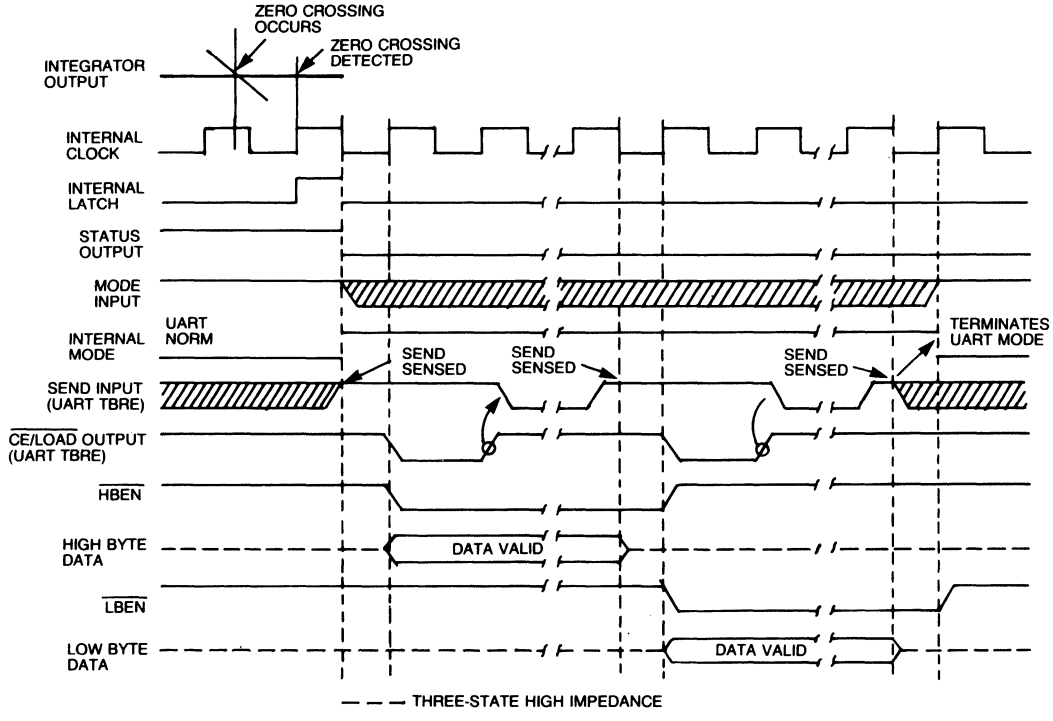
TIMING AND OPERATION (CONT)

the MODE input can be pulsed from low to high and the device will immediately enter the handshake mode. If the pulse occurs while new data is being stored, entry into handshake mode will be delayed until the data is stable. While in the handshake mode, the MODE Input will be ignored, and although conversions will still be performed, data updating will be inhibited until the output cycle is completed and clears the handshake mode.

The timing diagram (Handshake With SEND Held High) shows the sequence of the output cycle with the SEND input held high. The handshake mode is entered after the data latch pulse (generated internally). The SEND input (held high) is sensed on the same high to low internal clock edge. On the next low to high clock edge, the $\overline{\text{CE/LOAD}}$ and $\overline{\text{HBEN}}$ terminals go low enabling the high-order byte (bits 9 through 12, polarity and overrange). The $\overline{\text{CE/LOAD}}$ terminal remains low for one clock period only, the data outputs remain active for 1½ clock periods, and the high byte enable remains low for 2 clock periods. Note that the $\overline{\text{CE/LOAD}}$ terminals low level or low to high edge may be used as a synchronizing "OUTPUT" signal to ensure valid data, and the byte enable terminal as an "OUTPUT" may be used as a byte identification flag (in the handshake mode only). With the SEND input remaining high, the converter completes the output cycle using $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent, the handshake mode is terminated.

1

TYPICAL UART INTERFACE TIMING. (HANDSHAKE MODE)



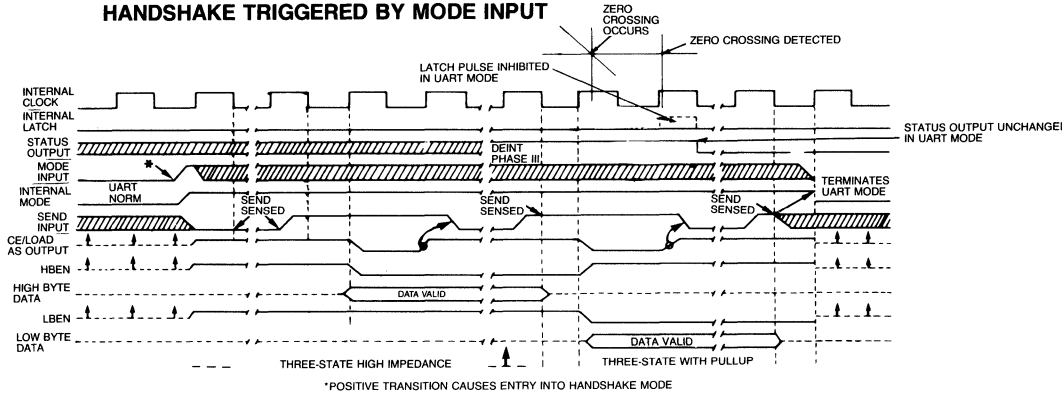
HANDSHAKE MODE (CONT)

The send input may be utilized in delaying portions of the output sequence, or handshake to ensure correct data transfer. The timing diagram (typical UART interface timing) shows the relationships when using the ADC-7109 with an industry standard UART to interface to serial data channels. In this type of interface, the SEND input of the ADC-7109 is driven from the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{\text{CE/LOAD}}$ terminal drives the TBRL (Transmitter Buffer Register Load) input of the UART. The data outputs of the ADC-7109 are paralleled into the Transmitter Buffer Register inputs of the UART.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. After the SEND input is sensed, the $\overline{\text{CE/LOAD}}$ and $\overline{\text{HBEN}}$ terminals will go low, activating the high order byte outputs. At the end of 1 clock period, the $\overline{\text{CE/LOAD}}$ goes low and the high order byte data is clocked into the UART TBR. The UART TBR output will now go low, which stops the output cycle with the $\overline{\text{HBEN}}$ output low, and high order byte outputs active. After the output data has been transferred to the UART transmitter register and cleared the TBR, the TBRE output returns high. On the next clock high to low edge, the high order byte outputs are disabled, and ½ clock pulse later, the $\overline{\text{HBEN}}$ terminal returns high, and the $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ outputs go low, activating the low order byte outputs. The low order byte outputs are similarly clocked into the UART (when $\overline{\text{CE/LOAD}}$ returns high) transmitter buffer register and TBRE again goes low. When TBRE returns high, it is sensed on the next high to low clock edge, disabling the data outputs. One half clock pulse later, the handshake mode is cleared, and the $\overline{\text{CE/LOAD}}$, $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ terminals return high and stay active as long as the MODE input stays high.

While the MODE input is high, the ADC-7109 will output the results of every conversion except those completed during a handshake operation. A low to high pulse (edge triggered) on the MODE input will enter the handshake mode and handshake output sequence may be performed on demand.

HANDSHAKE TRIGGERED BY MODE INPUT



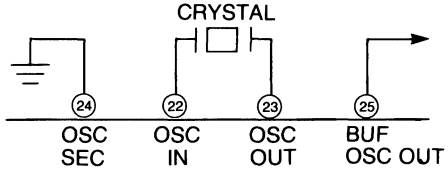
*POSITIVE TRANSITION CAUSES ENTRY INTO HANDSHAKE MODE

TIMING AND OPERATION (CONT)

The timing diagram (Handshake Triggered by Mode Input) shows a handshake output sequence triggered by such an edge. The SEND input is shown as being low when the converter enters the handshake mode. In this case, the entire output sequence is under the control of the SEND input, and the sequence for the high order byte is similar to the low order byte. This timing diagram also shows the output sequence taking longer than the conversion cycle. Note that conversions are still performed with the STATUS output and RUN/HOLD input functioning normally. The only difference is that new data will not be latched when in handshake mode and is therefore lost.

OSCILLATOR[1]

CRYSTAL OSCILLATOR



CRYSTAL OSCILLATOR

Using an inexpensive 3.58 MHz TV crystal provides an integration time given by:

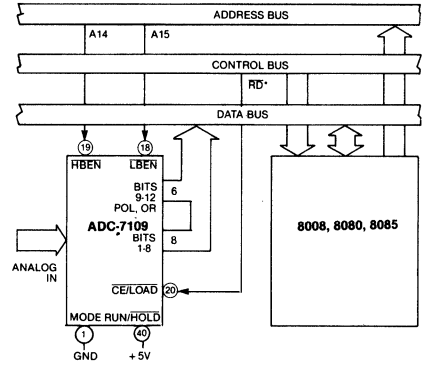
$$T = (2048 \text{ clock periods}) \times \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ msec.}$$

Note this is very close to two 60 Hz periods or 33.33 milliseconds. The error is less than 1% which yields better than 40 dB 60 Hz rejection. The ADC-7109 will operate reliably at conversion speeds of up to 30/second, which corresponds to a clock frequency of 245.8 kHz. See Crystal Oscillator Connection.

To overdrive the internal oscillator, the overdriving signal is applied to the OSCILLATOR INPUT and the OSCILLATOR OUTPUT is left open. The internal clock frequency will be of the same frequency, duty cycle and phase as the input when the OSCILLATOR SELECT input is left open. With the OSCILLATOR SELECT at ground, the clock will be a factor of 58 below the input frequency.

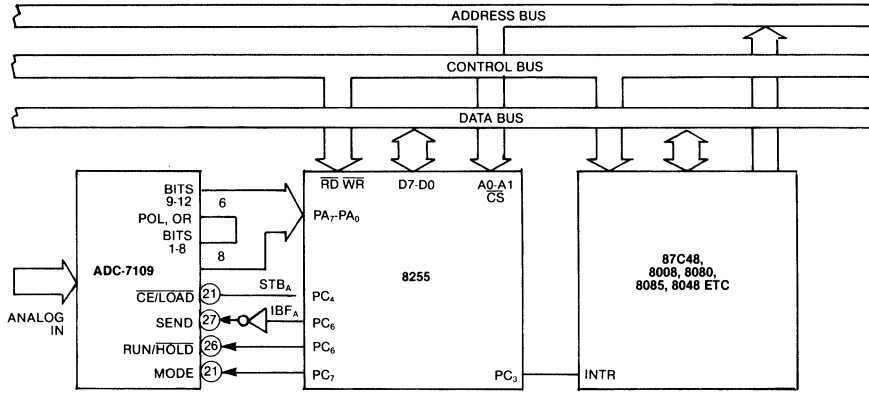
APPLICATIONS

DIRECT INTERFACE TO INTEL 8080/8055



The three-state output capability of the ADC-7109 enables it to be interfaced directly to most microprocessor busses. Note that system timing in this type of interface should be carefully considered to be sure that requirements for set-up and hold times, and minimum pulse widths are met. Drive limitations on long busses should also be considered. This type of interface is favored if the memory peripheral address density is low so that simple address decoding can be used.

HANDSHAKE INTERFACE TO AN INTEL MICROPROCESSOR

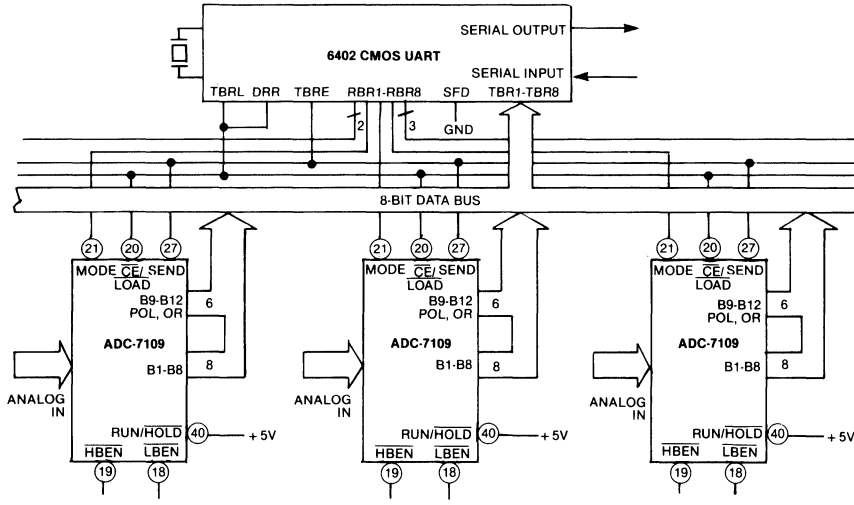


The handshake mode allows ready interface with a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of the $\overline{CE/LOAD}$.

This application shows a handshake interface to Intel microprocessors using an 8255 programmable peripheral interface. Handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ADC-7109 and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the 8255 should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the ADC-7109 is in handshake mode, the next word will be strobed into the port. The strobe will cause IBF (of the 8255) to go high (SEND goes low), which will keep the enabled byte outputs active. Th 8255 will generate an interrupt which when executed will resu in the data being read. The IBF will be reset low when the byte i read, causing the converter to sequence into the next byte. Th MODE input to the ADC-7109 is connected to a control line o the 8255.

The data from every conversion will be sequenced in two byte in the system, if the output is left high, or tied high separatel Data access must take less time than a conversion. The outpı sequence can be obtained on demand if this output is force from low to high and the interrupt may be used to reset th MODE bit. Conversions may be performed on command und software control by driving the $\overline{RUN/HOLD}$ input to the co verter by a bit from the 8255.

MULTIPLEXING SEVERAL CONVERTERS TO A SINGLE UART



In this application, several ADC-7109's are multiplexed to one UART. The word received by the UART (at the UART's RBR outputs when DR is high) is used to select which converter will handshake with the UART. This configuration will allow up to eight ADC-7109's to interface with one UART with no external component requirements.

ORDERING INFORMATION

ACCESSORIES Part Number	Description
ADC-7109	Mating Sockets
TP 1k	Trimming Potentiometers

ADC-800
15-Bit Plus Sign A/D Converter with Microprocessor Interface

DATEL

FEATURES
- 15-Bits Plus Sign Bit
- Parallel or Serial Bus Interface
- Three State Outputs
- High Impedance Differential Input
- UART Control Signals
- Low Noise

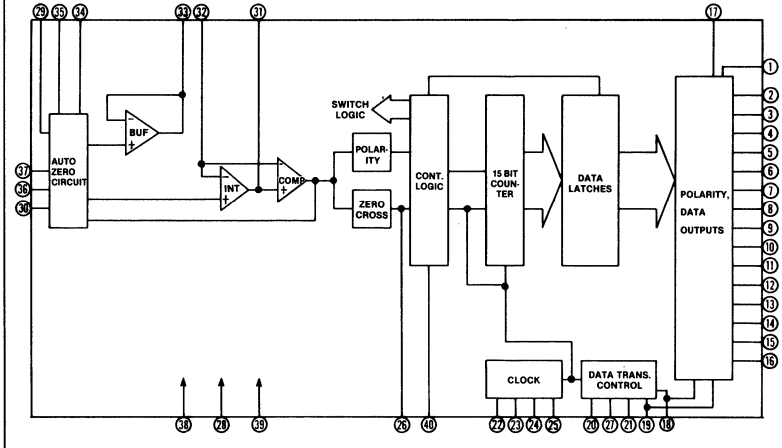
GENERAL DESCRIPTION

DATEL's ADC-800 is a low power, 15-bit plus sign integrating A/D converter. Microprocessor interface signals allow 16-bit, single byte or 8-bit, two byte parallel data transfer or data may be transmitted serially via industry standard UART in the "handshake" mode. Conversion time is typically 2.5 conv/sec with a maximum differential linearity error of ± ½ LSB.

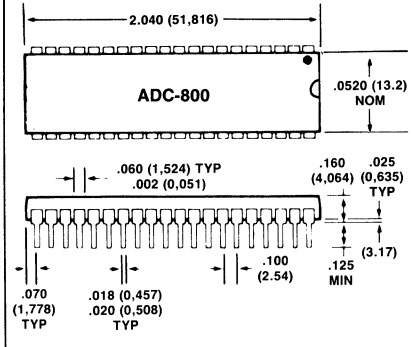
The ADC-800 uses an improved dual slope conversion technique which incorporates system zero and integrator output zero phases. Offset error sources are automatically zeroed. The externally adjustable clock allows integration periods which are integral multiples of 50 or 60 Hz for maximum power-line noise rejection. By using the 2.4576 MHz crystal oscillator mode, 50, 60 and 400 Hz signals are rejected. A serial count output can be derived by gating the clock signal with data valid ($\overline{DVD}$). The count output pulses may be used in serial fiber optic transmission systems.

Other important features of the ADC-800 include: high impedance differential inputs, 5 pA typical input bias current, 15 μV peak-to-peak typical input noise, 20 mW power dissipation and static discharge protected inputs. the combination of low cost, high accuracy and low power consumption make the ADC-800 an ideal choice for process control, data logging and intelligent measurement system applications.

The ADC-800 operates over the commercial, 0°C to +70°C temperature range and is packaged in a 40-pin plastic DIP.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SGN	21	$\overline{BUS}$/HAND
2	DB15 (MSB)	22	OSC IN
3	DB14	23	OSC OUT
4	DB13	24	OSC CON
5	DB12	25	BUF OSC
6	DB11	26	CONVERT/$\overline{STOP}$
7	DB10	27	DRQST
8	DB9	28	$-V_S$
9	DB8	29	V_{REF}
10	DB7	30	COM
11	DB6	31	V_{INT}
12	DB5	32	C_{SZ}
13	DB4	33	V_{BUF}
14	DB3	34	$-C_R$
15	DB2	35	$+C_R$
16	DB1 (LSB)	36	$-V_{IN}$
17	TEST	37	$+V_{IN}$
18	$\overline{LBEN}$/$\overline{LBFLG}$	38	$+V_S$
19	$\overline{HBEN}$/$\overline{HBFLG}$	39	DIG GND
20	$\overline{CE}$/$\overline{LDSTRB}$	40	$\overline{DVD}$

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ABSOLUTE MAXIMUM RATINGS	
Positive Supply Voltage ($+V_S$ to gnd)	+6.2V
Negative Supply Voltage ($-V_S$ to gnd)	−9.0V
Analog Input Voltage Range (+ or − Vin)	$+V_S$ to $-V_S$
Reference Input Voltage Range (Vref)	$+V_S$ to $-V_S$
Digital Input Voltage Range	$+V_S$ +0.3V to gnd −0.3V
Power Dissipation (package)	0.5W to 70°C

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V supplies, 2.5 conv/sec. conversion speed, 2.4576 MHz crystal, 3.2768V full-scale voltage unless otherwise noted.

ANALOG INPUTS	
Type Analog Input	Differential
Zero-Scale Error, max.[1]	±0.5 LSB
Input Current,[2] max.	15 pA
Common Mode Input Range	$-V_S$ + 1.5V to $+V_S$ − 1.0V
Common Mode Rejection Ratio[3]	80 μV/V
Input Noise[4]	15 μV peak-to-peak
DIGITAL INPUTS	
Control Input Pull-Up Current[5]	5 μA
Input Voltage, (Pins 18-21, 26, 27)	
High Min.	2.5V
Low Max.	2V
Input Pull-up Current[6] (pins 26, 27)	5 μA
(pins 17, 24)	25 μA
Input Pin Pulldown Current[7] (pin 21)	5 μA
Input Capacitance, max. (pins 18, 19)	50 pF
$\overline{BUS}$/Hand Control Pulse Width, min.[8]	70 nsec.
Byte Enable Pulse Width, min.[8]	350 nsec.
Chip Enable Pulse Width, min.[8]	500 nsec.
Byte Enable Access Time, max.[8]	350 nsec.
Chip Enable Access Time, max.[8]	400 nsec.
Data Hold from Byte Enable Change, max.[8]	300 nsec.
Data Hold from Chip Enable Change, max.[8]	400 nsec.
OUTPUTS	
Output Voltage, high min.	3.5V at 100 mA
low max.[9]	0.4V at 1.6 mA
Output Leakage Current (high Z state), max.	1 μA
Oscillator Output Current, (V_0 = 2.5V)	1 mA
Buffered Oscillator Output Current (V_0 = 2.5V)	5 mA
PERFORMANCE	
Resolution	15-bits plus sign
Linearity Error,[10] max.	2 LSB
Differential Linearity, max.	±0.5 LSB
Conversion Time	2.5 conv/sec. (400 msec.)
Full-Scale Gain Tempco[11] max.	5 ppm/°C
Zero-Scale Error Tempco, max.	2 μV/°C
Full-Scale Magnitude Symmetry Error, max.[12]	2 LSB
POWER REQUIREMENTS	
Supply Voltage	±5V
Supply Current, max.	±3.5 mA
typical	±2.0 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering 60 sec)	+300°C
Package	40-pin Plastic DIP

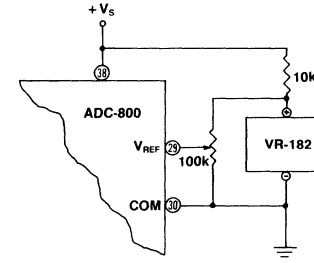
FOOTNOTES:

1. Vin = 0V
2. At 25°C, Vin = 0V. For 0°C to +70°C, Iin = 125 pA.
3. Vcm = ±1V.
4. Not exceeded 95% of the time.
5. Pin 18, 19, 20, 21 = 0V. Vout = 2V.
6. V = 2V.
7. V = 3V.
8. Parallel data transfer. ($\overline{BUS}$/Hand = 0)
9. For pins 18, 19, 20. Iout = 750 μA.
10. −F.S. ≤ Vin ≤ +F.S., best straight line. End point is typically 2.8 LSB.
11. External Reference Tempco = 0 ppm/°C 0°C ≤ T_A ≤ +70°C.
12. Vin = 3.27V.
13. Static sensitive device. Unused units must be stored in conductive material. Protect devices from static discharge and static fields.

TECHNICAL NOTES

1. The internal class A output stage amplifiers will supply a 20 μA drive current with minimal linearity error. R_{INT} is calculated for a 20 μA full-scale current using the following expression: R_{INT} (MΩ) = Full-Scale Input Voltage (V)/20.
2. The integrating capacitor should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.4V from either supply). With a 20 μA full-scale buffer output current, the integrating capacitor (C_{INT}) is calculated as follows: C_{INT} (μF) = 16.384 (1/F_{CLK} (kHz) (20 μA)/Integrator Output Voltage Swing (V). With an external 2.4576 MHz crystal, the clock frequency will be 163.8 kHz and conversion time is 2.5 CONV/SEC. A 0.47 μF C_{INT} is recommended with low dielectric absorption such as polypropylene to prevent roll-over errors. The outer foil of C_{INT} should be connected to Pin 31.
3. A 1.0 μF polypropylene capacitor is recommended for C_{SZ}. (System Zero Capacitor.) The inner foil should be connected to Pin 32.
4. For the reference capacitor, a 1.0 μF is recommended. Larger values may be used to limit roll-over errors. Low leakage capacitors, such as polypropylene should be used.
5. The analog input required to generate the 32,768 8 full-scale count is 2 V_{REF}. The reference voltage source should be selected for temperature stability. The ADC-800 will provide 30 ppm resolution. With a 5 ppm/°C reference, a 6° change in temperature will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed. The reference voltage input must be a positive voltage with respect to analog common. A reference circuit is shown below.
6. The R_S (delay resistor) in combination with C_{INT} compensate for comparator delay time. With a 0.47 μF C_{INT}, a 20Ω series resistor is recommended.

REFERENCE VOLTAGE CIRCUIT



PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	SGN	Sign Bit: Logic "1" indicates positive input. Input signal polarity is determined at the end of the signal integrate phase.
2	DB15 (MSB)	Data Bits. Three-State Outputs
3	DB14	
4	DB13	
5	DB12	
6	DB11	
7	DB10	
8	DB9	
9	DB8	
10	DB7	
11	DB6	
12	DB5	
13	DB4	
14	DB3	
15	DB2	
16	DB1 (LSB)	
17	TEST	Test: Logic "0" forces data bits to Logic "1" and disables clock. Logic "1" enables counter latches.
18	$\overline{\text{LBEN}}/\overline{\text{LBFLG}}$ (Input/Output)	Low data byte enable input or flag output depending on $\overline{\text{BUS}}$/HAND (Pin 21) status. With $\overline{\text{BUS}}$/HAND (Pin 21) low and $\overline{\text{CE}}/\overline{\text{LDSTRB}}$ (Pin 20) low, DB8 through DB1 (low data byte) are output, when input $\overline{\text{LBEN}}$ is low. With $\overline{\text{BUS}}$/HAND high, valid data (DB8-DB1) is indicated by the flag output $\overline{\text{LBFLG}}$ when low.
19	$\overline{\text{HBEN}}/\overline{\text{HBFLG}}$ (Input/Output)	High data byte enable input or flag output depending on $\overline{\text{BUS}}$/HAND (Pin 21) status. With $\overline{\text{BUS}}$/HAND (Pin 21) low and $\overline{\text{CE}}/\overline{\text{LDSTRB}}$ low, the sign bit and DB15-DB9 (high data byte) are output, when input $\overline{\text{HBEN}}$ is low. With $\overline{\text{BUS}}$/HAND (Pin 21) high, valid data (sign and DB15-DB9) is indicated by the flag output $\overline{\text{HBFLG}}$ when low.
20	$\overline{\text{CE}}/\overline{\text{LDSTRB}}$ (Input/Output)	With $\overline{\text{BUS}}$/HAND (Pin 21) low, $\overline{\text{CE}}$ (Pin 20) is the master CHIP ENABLE. When $\overline{\text{CE}}$ input is high, the sign bit and DB15-DB1 are in the high impedance state. With $\overline{\text{CE}}$ low, data is transferred under control of $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ input signals as follows: $\overline{\text{CE}}$ $\overline{\text{LBEN}}$ $\overline{\text{HBEN}}$ FUNCTION 0 0 1 Low data byte output 0 1 0 High data byte output 0 0 0 Low and high data byte output 0 1 1 High impedance state With $\overline{\text{BUS}}$/HAND high (Pin 21), $\overline{\text{LDSTRB}}$ Pin 20) is a load strobe output sign and a low output signal instructs the receiving device to accept data.

PIN	SYMBOL	DESCRIPTION
21	$\overline{\text{BUS}}$/HAND	Input low, yields parallel output data mode. The $\overline{\text{CE}}$, $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ (Pins 20, 19, 18) are inputs and directly control the 16 data bits. Input pulsed HIGH causes immediate entry into handshake data transfer mode for UART interfacing. $\overline{\text{LDSTRB}}$, $\overline{\text{LBFLG}}$ and $\overline{\text{HBFLG}}$ are TTL compatible outputs in this mode.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC CON	Selects internal oscillator structure. Input high: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC (Pin 25). Input Low: Crystal oscillator. Internal clock frequency is frequency at BUS OSC ÷ 15.
25	BUF OSC	Buffered oscillator output
26	CONVERT/$\overline{\text{STOP}}$	Input high: Performs continuous conversion. Input low: Stops conversion process 7 counts before entering signal integrate phase. Conversion in progress is completed.
27	DRQST	Data output request signal. Input used in the handshake mode to indicate an external device is ready to accept data.
28	$-V_S$	Negative supply (−5V)
29	V_{REF}	Voltage reference input
30	COM	Analog common. The device is auto-zeroed to the analog common potential.
31	V_{INT}	Integrator output
32	C_{SZ}	System zero capacitor
33	V_{BUF}	Input signal buffer output
34	−CR	Negative reference capacitor connection
35	+CR	Positive reference capacitor connection
36	$-V_{IN}$	Negative differential analog input
37	$+V_{IN}$	Positive differential analog input
38	$+V_S$	Positive supply (+5V)
39	DIG GND	Ground return for all digital logic
40	$\overline{\text{DVD}}$	Data valid signal: high during signal integrate and reference integrate phases until data is latched. Low when in auto zero phase. Data does not change when $\overline{\text{DVD}}$ = 0

TIMING AND OPERATION

THE CONVERSION PROCESS

The conventional dual-slope converter measurement cycle has two distinct phases: Input signal Integration, and Reference Voltage Integration (deintegration).

The analog input signal is integrated for a fixed time period which is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output returns to zero. The reference voltage integration time is directly proportional to the input signal. A complete conversion requires the integrator output to "ramp-up" and "ramp-down".

The ADC-800's accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent advantage in the dual-slope converter is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods.

The following equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} Vin(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

Where: V_R = Reference Voltage
T_{SI} = Signal Integration Time (fixed)
T_{RI} = Reference Voltage Integration Time (variable)

For a constant Vin: $Vin = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$

ANALOG INPUT DESCRIPTION

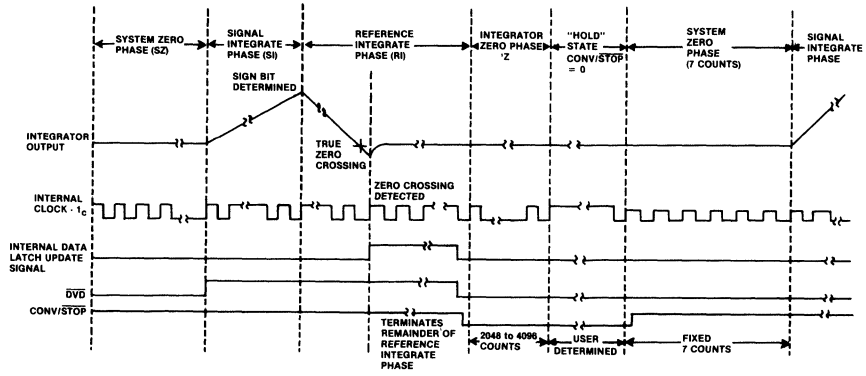
System Zero Phase: Errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{SZ} with a compensating error voltage.

Input Signal Integration Phase: The differential voltage between the inputs is integrated. The differential voltage must be within the specified common-mode range. The input signal is integrated for 16,384 clock cycles. The polarity is determined at the end of the phase.

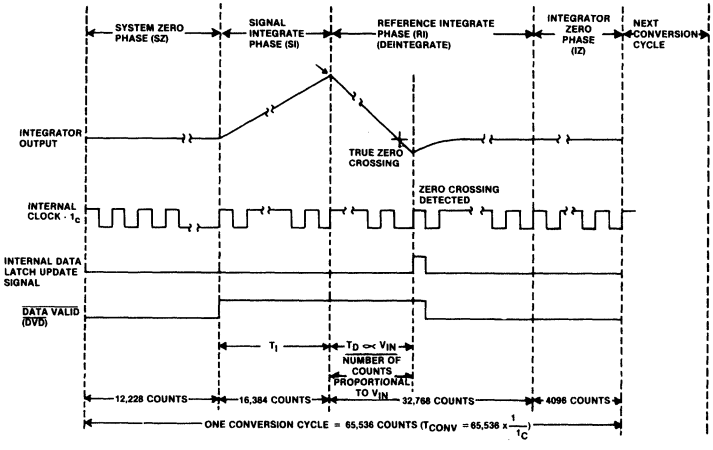
Reference Voltage Integration: C_R (Reference Capacitor), which was previously charged is connected with proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. This phase lasts for a maximum of 32,768 clock periods.

Integrator Output Zero: This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase lasts for 4096 clock cycles.

CONVERT ON COMMAND OPERATION
(CONV/$\overline{STOP}$ = 0 AFTER ZERO CROSSING IS DETECTED)



CONTINUOUS CONVERSION
(CONV/$\overline{STOP}$ = 1)



TIMING AND OPERATION (CONT.)

PARALLEL MODE DATA TRANSFER

With BUS/HAND at logic "0", the sign and data bits are controlled by the $\overline{CE}$/$\overline{LDSTRB}$ (Pin 20), $\overline{LBEN}$/$\overline{LBFLG}$ (Pin 18) and $\overline{HBEN}$/$\overline{HBFLG}$ (Pin 19) inputs. These inputs include internal pull-up resistors. Inactive data bits are in the high impedance state.

The $\overline{HBEN}$/$\overline{HBFLG}$ signal controls the most significant data byte (SGN, DB15-DB9) and $\overline{LBEN}$/$\overline{LBFLG}$ (Pin 18) controls the least significant data byte (DB8-DB1). See adjacent TRUTH TABLE.

These input signals are asynchronous with the internal clock. Output data is immediately available. To avoid accessing data as it is updated, the DATA VALID (Pin 40) can be used to control data access. Data will not change if $\overline{DVD}$ = 0.

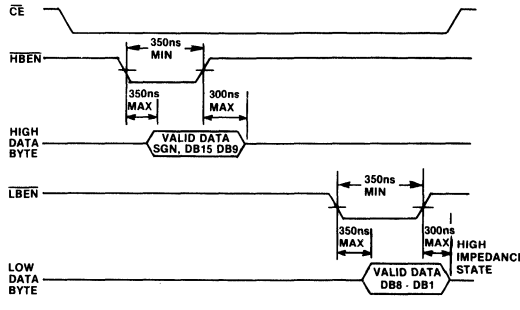
TRUTH TABLE

$\overline{CE}$/$\overline{LDSTRB}$ (Pin 20)	$\overline{HBEN}$/$\overline{HBFLG}$ (Pin 19)	$\overline{LBEN}$/$\overline{LBFLG}$ (Pin 18)	HIGH DATA BYTE (SGN,DB15-DB9)	LOW DATA BYTE (DB8-DB1)
1	X	X	Inactive	Inactive
0	0	0	Active	Active
0	0	1	Active	Inactive
0	1	0	Inactive	Active
0	1	1	Inactive	Inactive

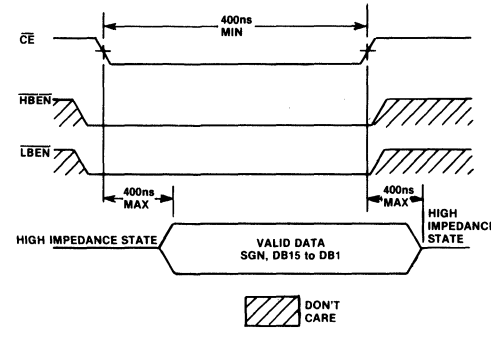
Inactive = High "Z" state
"X" = 1 or 0

PARALLEL DATA TRANSFER

TWO 8-BIT BYTES



SINGLE 16-BIT BYTE

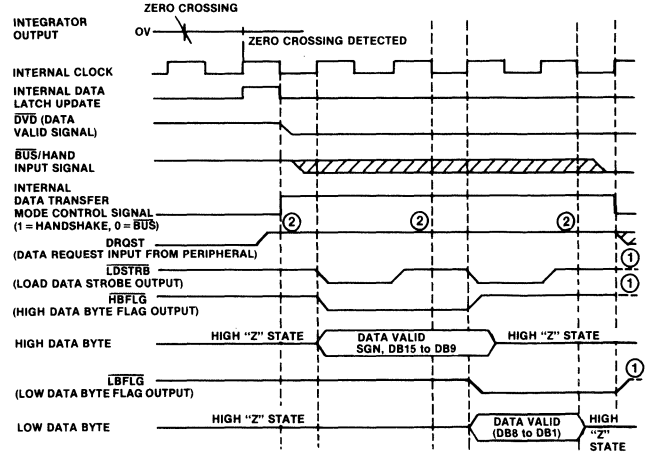


HANDSHAKE MODE DATA TRANSFER

The ADC-800 actively controls the data transfer to peripherals through the handshake data transfer mode. In this mode $\overline{LBEN}$/$\overline{LBFLG}$, $\overline{HBEN}$/$\overline{HBFLG}$ and $\overline{CE}$/$\overline{LDSTRB}$ (Pins 18, 19, 20) are TTL compatible outputs. The $\overline{LDSTRB}$ signal indicates valid data is available for the peripheral. The $\overline{LBFLG}$ and $\overline{HBFLG}$ signals indicate which data byte is being transferred. DRQST (Pin 27) informs the A/D that a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

A logic "1" on $\overline{BUS}$/HAND (Pin 21) enters the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch is set, the $\overline{BUS}$/HAND signal is ignored, the DRQST signal controls data transfer to the external requesting peripheral. (See adjacent diagram.)

This diagram shows the timing for the data transfer with $\overline{BUS}$/HAND at logic "1" (throughout the transfer). Note that the DRQST is at logic "1" throughout the transfer. The transfer rate is set by the internal clock. A complete data transfer occurs in 4 clock periods after a DRQST logic "1" is detected on a high to low clock edge transition.



Note:
1. High Impedance Output with Internal Pullup.
2. DRQST Signal Sensed at H → L Clock Transition.

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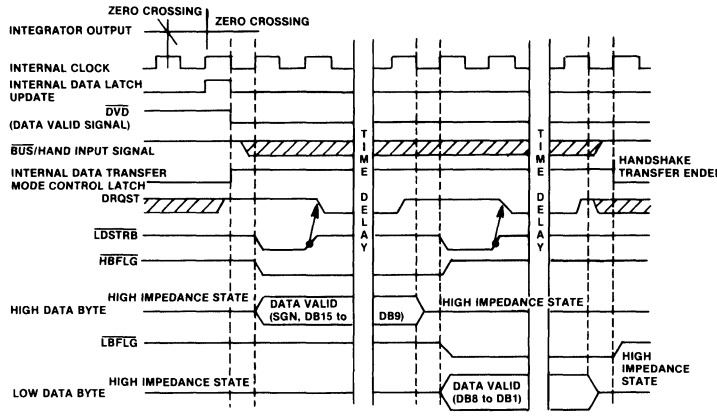
TIMING AND OPERATION (CONT.)

TYPICAL UART INTERFACE TIMING



For peripherals that are unable to accept data at the ADC-800 clock rate, the DRQST input signal can be used to delay the transmit sequence. This mode is useful in interfacing to UART's. (See above Timing Diagram.)

The UART data transfer sequence begins with a logic "1" on DRQST. This indicates the UART transmitter buffer register is empty (TBMT = 1). LDSTRB and HBFLG become active when DRQST is sensed synchronously. The high order data byte is stored in the UART transmitter buffer register when LDSTRB is logic "1". This occurs one clock period after DRQST is sensed. The DRQST signal (TBMT) goes low, stopping the cycle with the SGN and DB15-DB9 data bits active. After the UART transfers the received data to the transmitter register, the DRQST input (TBMT) again goes high. On the first high to low internal clock transition, the high data byte is disabled and one-half clock period later HBFLG goes to logic "1". Concurrently, LDSTRB is logic "0" and DB8-DB1 become active. One clock pulse later, LDSTRB is logic "1" and the low data byte is clocked into the UART transmitter buffer register. DRQST goes low.

When DRQST returns high, it will be sensed on the first internal clock high to low edge transition, thus causing all outputs to be disabled. One half clock period later, the internal handshake mode latch is cleared and LDSTRB = HBFLG = LBFLG = logic "1". The outputs remain active as long as the BUS/HAND (Pin 21) is high.

NOTES:

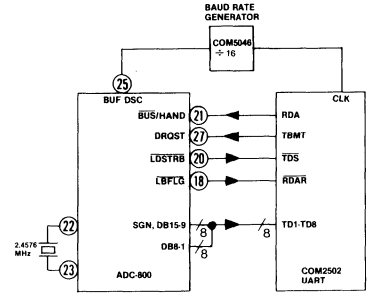
RDA = Receiver Data Available. Set high when character received & transferred to receiver buffer register.

TBMT = Transmitter Buffer Empty. Set high when transmitter buffer register is available for loading with new data.

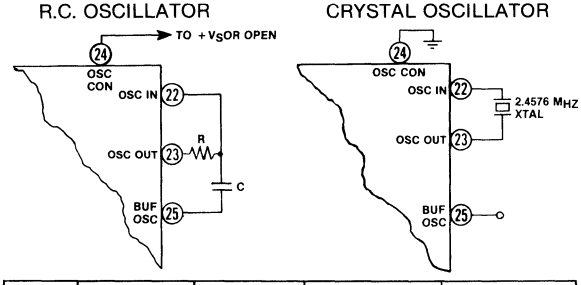
TDS = Transmitter Data Strobe. Low level input transfers data into transmitter register.

RDAR = Receiver Data Available Reset. Low level resets RDA output to logic "0".

TYPICAL CONNECTION TO UART



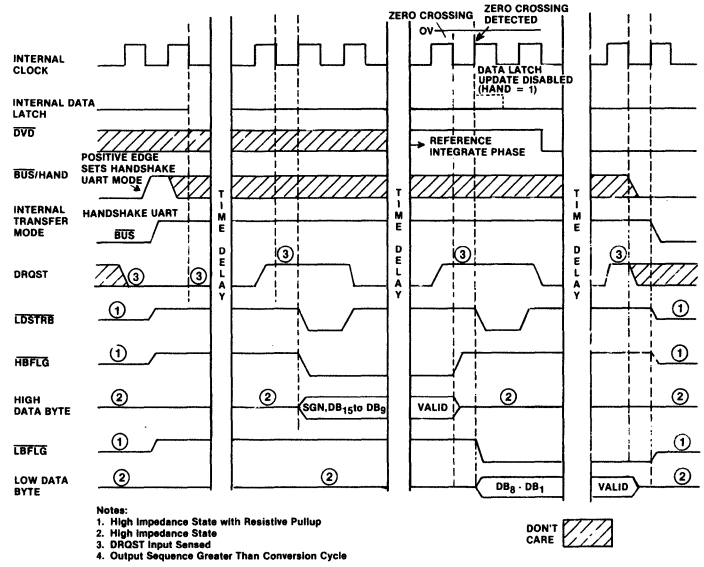
OSCILLATOR OPERATION



OSC TYP	OSC CON (PIN 24)	INT. CLK FREQUENCY	SIGNAL INTEG. TIME	CONVERSION TIME
RC	+ Vs or open	.45/RC	16384(RC/.45)	65536(RC/.45)
XTAL	GROUND	FXTAL/15	16384(15/FXTAL)	65536(15/FXTAL)

TIMING, CONNECTION AND APPLICATION

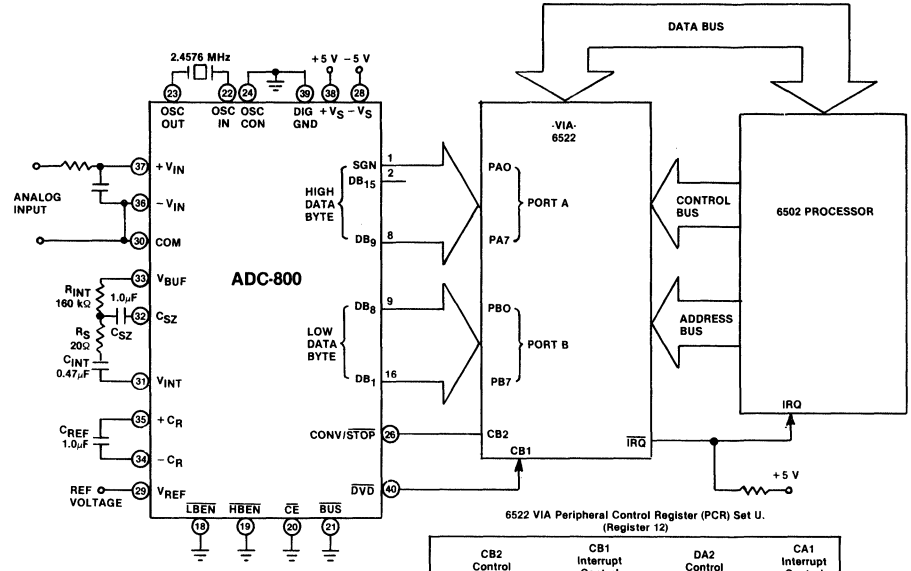
HANDSHAKE OUTPUT ON COMMAND



The ADC-800 will output every conversion with $\overline{BUS}$/HAND at logic "1" (except those completed during a handshake transfer). Handshake output sequences on demand are possible by triggering the $\overline{BUS}$/HAND control input with a low to high edge. The diagram, "HANDSHAKE OUTPUT ON COMMAND" shows a typical data transfer.

The output cycle is controlled by the DRQST input signal. The complete two byte data transfer can take any length of time. Conversions are performed and the $\overline{DVD}$ and CONV/$\overline{STOP}$ inputs function normally but new data will not be latched until the handshake mode is ended.

PARALLEL INTERFACE TO 6522 VERSATILE INTERFACE ADAPTER



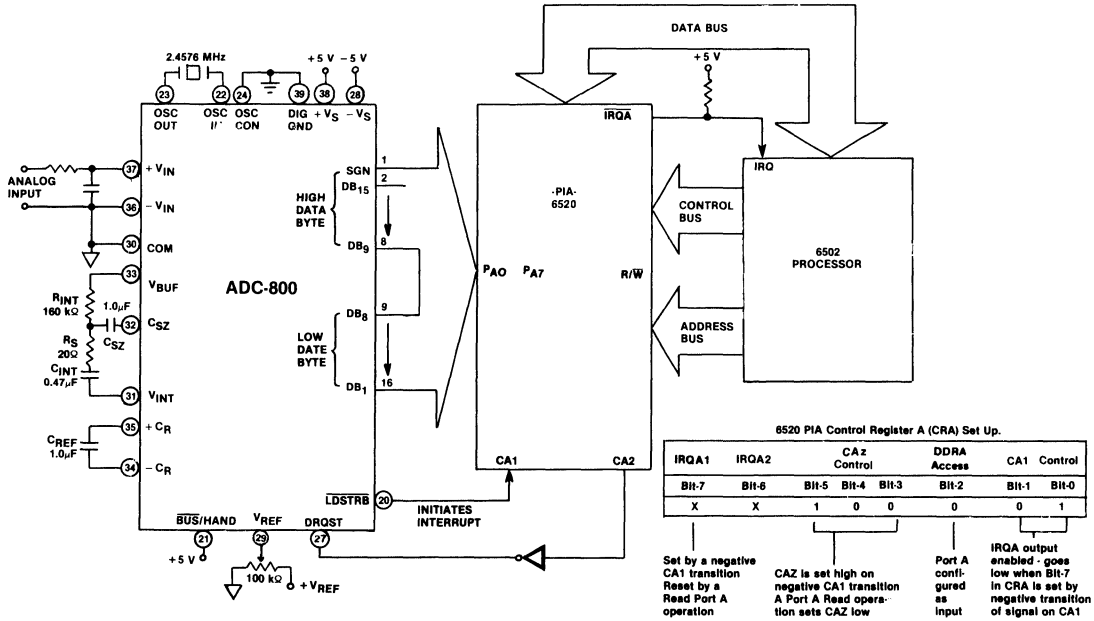
6522 VIA Peripheral Control Register (PCR) Set U. (Register 12)

CB2 Control			CB1 Interrupt Control	DA2 Control			CA1 Interrupt Control
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0/1[1]	—	—	—	—	

[1]May be programmed for convert on command or continuous conversions

APPLICATION

INTERFACE TO 6520 PIA



6520 PIA Control Register A (CRA) Set Up.

IRQA1	IRQA2	CAz Control			DDRA Access	CA1 Control	
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
X	X	1	0	0	0	0	1

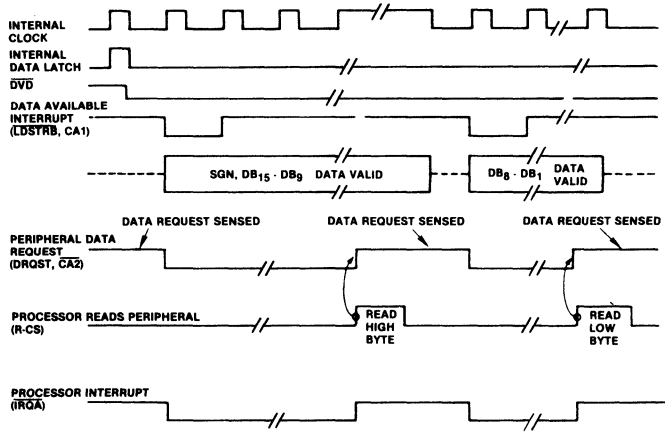
Set by a negative CA1 transition Reset by a Read Port A operation

CAZ is set high on negative CA1 transition A Port A Read operation sets CAZ low

Port A configured as input

IRQA output enabled · goes low when Bit-7 in CRA is set by negative transition of signal on CA1

HANDSHAKE TIMING DIAGRAM



Note: Data from every conversion is transmitted in two bytes (Data read cycle is less than conversion time)

HIGH "Z" STATE.--------

ORDERING INFORMATION

MODEL NO.

ADC-800

ADC-810, ADC-811
12-Bit, High-Speed
Hybrid A/D Converter

FEATURES

- **2 Microsecond maximum conversion time**
- **12-Bit resolution**
- **Industry-standard pinout**
- **−55°C to +125°C Operation**

GENERAL DESCRIPTION

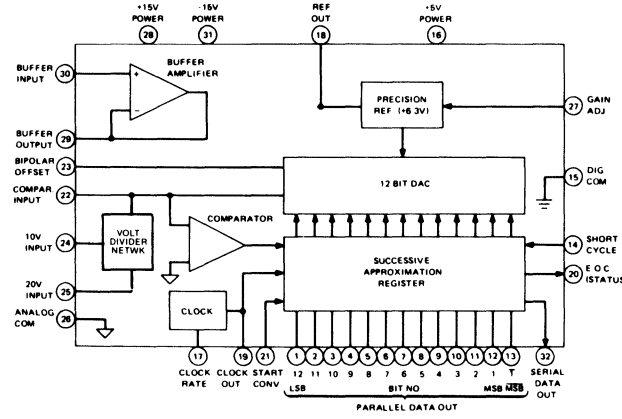
DATEL's ADC-810 and ADC-811 are high speed, high performance 12-bit analog-to-digital converters manufactured with thick- and thin-film hybrid technology. Utilizing the successive approximation conversion technique, the ADC-810 achieves a 12-bit conversion in a maximum of only 2 microseconds. Conversion time for the ADC-811 is 3 microseconds maximum, this being the only difference between the two units. Both models are pin-compatible with industry standard ADC-85/87 converters, offering increased speed, high accuracy and reliability over the full military temperature range.

These converters feature four pin-programmable input voltage ranges: 0 to +10V dc, 0 to +20V dc, ±5V dc, and ±10V dc. A user selectable input buffer amplifier is included for applications where 100 MΩ input impedance is required. Other specifications include a maximum nonlinearity of ±1 LSB, and a gain tempco of 20 ppm/°C maximum. The differential nonlinearity tempco is ±5 ppm/°C maximum.

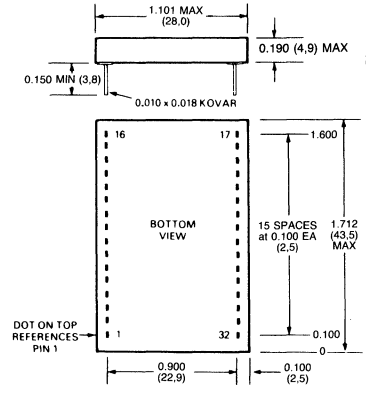
Output data is available in parallel or serial form. Output coding is complementary binary, complementary offset binary or complementary two's complement. All digital outputs are TTL-compatible.

The ADC-810 and ADC-811 are a good choice for numerous commercial, industrial and military applications requiring high speed, hybrid reliability, low cost and small size. Such applications include FFT analysis, radar digitization, medical instrumentation, and high speed multiplexed data acquisition systems.

Power requirement for both converters is ±15V and +5V. Models are available for operation over the commercial, 0°C to +70°C, and military −55°C to +125°C temperature ranges. All devices are packaged in a 32-pin, hermetically sealed, ceramic case.



MECHANICAL DIMENSIONS



*NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT
9	BIT 4 OUT	25	20V INPUT
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT ($\overline{\text{MSB}}$)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM.	31	-15V POWER
16	+5V POWER	32	SERIAL OUTPUT

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FUNCTIONAL SPECIFICATIONS, ADC-810, ADC-811

Typical at 25°C, ±15V and +5V supplies unless otherwise noted

DESCRIPTION		
INPUTS		
Analog Input Ranges, unipolar[1]	0 to +10V FS, 0 to +20V FS	
Analog Input Ranges, bipolar[1]	±5V, ±10V FS	
Input Impedance	1.05 kΩ (0 to +10V, ±5V) 4.2 kΩ (0 to +20V, ±10V)	
Input Impedance with Buffer	100 Megohms	
Input Bias Current of Buffer	125 nA typical, 250 nA max.	
Input Overvoltage[2]	±15V	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 50 nsec. min. Rise and fall times <30 nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 1 TTL load	
OUTPUTS[3]		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V	
Coding, unipolar	Complementary Binary	
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Complementary Binary or Complementary Offset Binary Coding.	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V, 70 nsec. pulses. 6.5 MHz for ADC-810, and 4.3 MHz for ADC-811 (Pin 17 grounded).	
PERFORMANCE		
Resolution	12-bits (1 part in 4096)	
Nonlinearity, max.	±1 LSB	
Differential Nonlinearity, max.	±1 LSB	
Gain Error, max., before adj.	±0.1%	
Zero Error, max., unipolar, before adj.	±0.15% of FSR[4]	
Offset Error, max., bipolar, before adj.	±0.15% of FSR[4]	
Temp. Coeff. of Gain, max.	±20 ppm/°C	
Temp. Coeff. of Zero, unipolar, max.	±10 ppm/°C of FSR[5]	
Temp. Coeff. of Offset, bipolar, max.	±10 ppm/°C of FSR[5]	
Diff. Nonlinearity Tempco, max.	±5 ppm/°C of FSR	**ADC-811 only**
Conversion Time[4], 12 bits	2.0 μsec. max.	3.0 μsec. max.
10 bits[6]	1.7 μsec. max.	2.6 μsec. max.
8 bits[6]	1.4 μsec. max.	2.1 μsec. max.
Buffer Settling Time, 10V step	500 nsec. to 0.01%	
Power Supply Rejection max.	0.01%/% Supply max.	
POWER REQUIREMENTS		
Analog Supply, positive	+15V dc ±0.5V at 70 mA max.	
negative	−15V dc ±0.5V at 30 mA max.	
Logic Supply	+5V dc ±0.25V at 240 mA max.	
PHYSICAL/ENVIRONMENTAL		
Operating Temperature Range, MC	0°C to +70°C	
MM	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Package Size	1.700 x 1.100 x 0.160 inches	
Package Type	32 pin ceramic	
Pins	0.010 x 0.018 inch Kovar	
Weight	0.5 ounces (14 grams)	

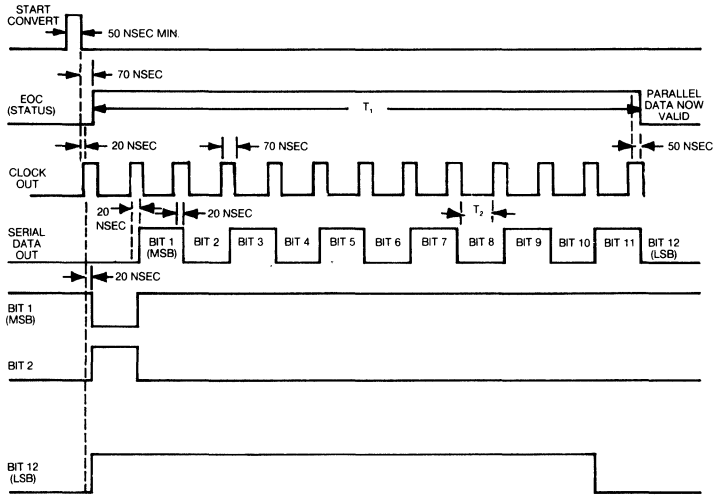
FOOTNOTES:

1. For information on models with 0 to +5V dc and ± 2.5V dc input voltage ranges, please contact the factory.
2. The input buffer cannot be used with the 0 to +20V dc input range.
3. All digital outputs can drive 5 TTL loads.
4. Without buffer amplifier used. ADC-810/811 may require external adjustment of clock rate using the buffer amplifier.
5. FSR is full scale range and is 10V dc for 0 to +10V dc or ±5V dc input and 20V dc for ±10V dc input.
6. Short cycled operation.

TECHNICAL NOTES

1. Use of good high frequency circuit board layout techniques is required for rated performance. Digital common (Pin 15) and analog common (Pin 26) are not connected internally and therefore must be connected as directly as possible externally. Also, it is recommended that the analog and digital supplies be externally bypassed with a 0.01 μF ceramic capacitor in parallel with a 1 μF electrolytic capacitor. The ±5V dc supply should be bypassed to ground with a 10 μF electrolytic capacitor. Additionally, Pin 27 (Gain Adjust) should be bypassed to ground with a 0.01 μF ceramic capacitor.
2. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10 k and 100 k ohms and should be 100 ppm/°C cermet types (such as DATEL's TP Series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise.
3. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting Pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, Pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases, the clock rate is also speeded up by connecting the clock rate adjust (Pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.
4. These converters dissipate 2.8 watts of power. The case to ambient thermal resistance is approximately 20°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter. Also, it is recommended that the converter be mounted directly to the circuit board (without the use of a mounting socket) and that good thermal contact be established between the case bottom and the circuit board grounded plane by use of a silicone thermal joint compound such as Wakefield type 120 or equivalent. For operation in ambient temperatures exceeding 85°C, air flow of at least 400 linear feet per minute is recommended.

TIMING DIAGRAM FOR ADC-810, ADC-811

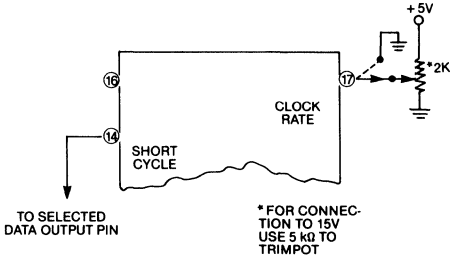


TIMING DIAGRAM OPERATING PERIODS

	ADC-810	ADC-811
T_1	2.0 μsec.	3.0 μsec.
T_2	98 nsec.	258 nsec.

OUTPUT: 101010101010

CLOCK RATE ADJUSTMENT



SHORT CYCLE OPERATION

Refer to Technical Note 3 for methods of reducing the overall ADC-810 or ADC-811 conversion time.

CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE ADC-811	CLOCK RATE ADC-810
0V	4.3 MHz	6.5 MHz
+5V	5.2 MHz	7.8 MHz
+15V	5.4 MHz	8.1 MHz

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

CLOCK RATE ADJUSTMENT RANGE

5V, 2kΩ Trim Pot
6.5 MHz to 7.8 MHz (ADC-810)
3.2 MHz to 3.6 MHz (ADC-811)

15V, 5KΩ Trim Pot
6.5 MHz to 8.1 MHz (ADC-810)
3.2 MHz to 4 MHz (ADC-811)

8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-810 CONV. TIME	2 μsec	1.7 μsec	1.4 μsec
ADC-811 CONV. TIME	3 μsec	2.6 μsec	2.1 μsec
CONNECT THESE PINS TOGETHER	17 & 15 14 & 16	17 & 16 14 & 2	17 & 28 14 & 4

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INPUT CONNECTIONS

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0V to +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
0V to +20V	25	—	23 & 26	30	—	NA	NA
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 25

1

OUTPUT CODING TABLES

BIPOLAR OPERATION

INPUT VOLTAGE RANGE		COMP. OFFSET BINARY			COMP. TWO'S COMPLEMENT		
±10V	±5V	MSB		LSB	MSB		LSB
+9.9951V	+4.9976V	0000	0000	0000	1000	0000	0000
+7.5000	+3.7500	0001	1111	1111	1001	1111	1111
+5.500	+2.5000	0011	1111	1111	1011	1111	1111
0.0000	0.0000	0111	1111	1111	1111	1111	1111
−5.0000	−2.5000	1011	1111	1111	0011	1111	1111
−7.5000	−3.7500	1101	1111	1111	0101	1111	1111
−10.000	−5.0000	1111	1111	1111	0111	1111	1111

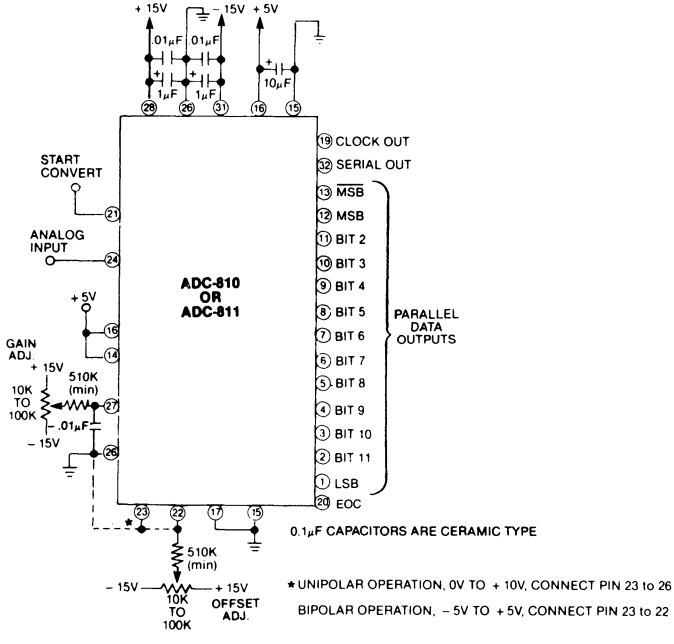
UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +20V	MSB		LSB
+9.9976V	+19.9952V	0000	0000	0000
+8.7500	+17.5000V	0001	1111	1111
+7.5000	+15.0000V	0011	1111	1111
+5.0000	+10.0000V	0111	1111	1111
+2.50000	+5.0000V	1011	1111	1111
+0.0024	+0.0049V	1111	1111	1110
0.0000	+0.0000V	1111	1111	1111

CALIBRATION PROCEDURE

1. **Connect the converter** as shown in the applicable connections diagram. A trigger pulse of 50 nanoseconds minimum is applied to the start conversion input (pin 21) at a rate of 200 kHz.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0 + ½ LSB) or the bipolar offset adjustment (0 − ½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110 for the unipolar range and between 0111 1111 1111 and 1000 0000 0000 for the bipolar range.
3. **Full Scale Adjustment**
   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+ FS − 1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

TYPICAL CONNECTIONS



CALIBRATION TABLE

UNIPOLAR RANGE	+ ½ LSB	+ F.S.-1½ LSB
0 to +10V	+1.22 mV	+9.9963 V
0 to +20V	+2.44 mV	+19.9927V
BIPOLAR RANGE	**− ½ LSB**	**+ F.S.-1½ LSB**
±5V	−1.22 mV	+4.9963 V
±10V	−2.44 mV	+9.9927 V

For information on models with 0 to +5V and ±2.5V input voltage ranges please contact the factory.

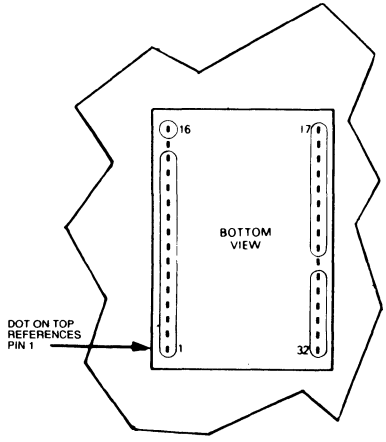
NOTE

In any application using the ADC-810 or the ADC-811, signal integrity and noise isolation are a function of grounding. The suggested ground plane shown should be used whenever possible.

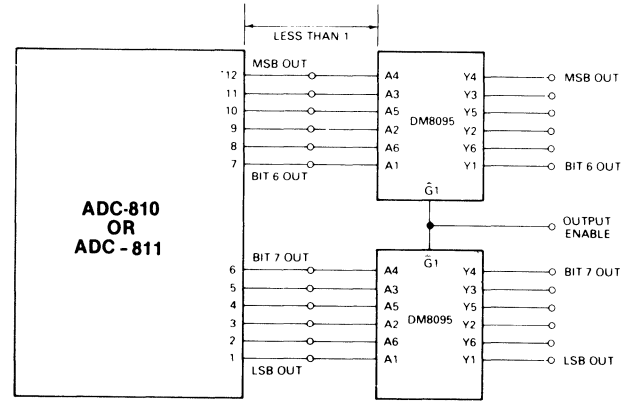
Providing Three-State Outputs

For applications where the coverted input must interface to tri-state TTL or CMOS logic, the ADC-810 or ADC-811 outputs are easily converted using buffers such as the DM8095's shown in the diagram. Signal length must be less than one inch between devices to ensure signal integrity. Also note that two's complement outputs are available from the ADC-810 and ADC-811 by using pin 13 instead of Pin 12 as the MSB output. The timing diagram shows the delays incurred as the signal passes through the buffers.

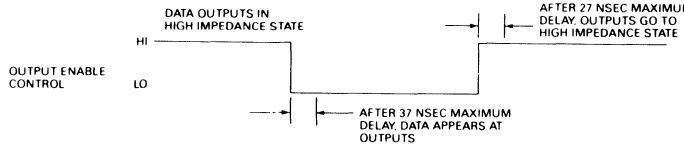
GROUND PLANE LAYOUT



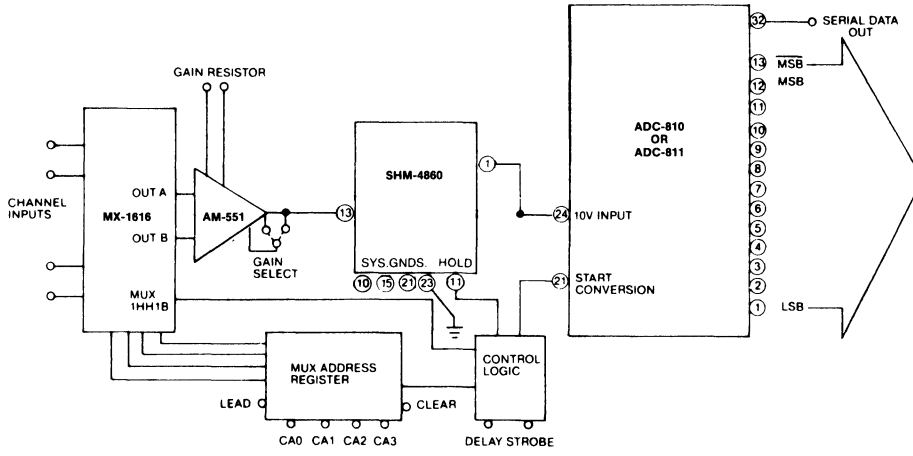
HIGH SPEED THREE-STATE OUTPUT BUFFER



*FOR TWO'S COMPLEMENT OUTPUT CODING THIS CONNECTION IS PIN 13 ($\overline{MSB}$)



HIGH SPEED DATA ACQUISITION SYSTEM



The four DATEL components shown in the diagram make up a 12-bit, high-speed data acquisition system capable of throughput rates of 200 kHz. The system can accept up to 16 single-ended input channels using DATEL's MX-1616 CMOS multiplexer or up to eight differential channels using the MX-808.

Other DATEL components in the system are the AM-551, a hybrid precision programmable gain instrumentation amplifier and the SHM-4860, a 200 nanosecond, 0.01% hybrid sample-and-hold device.

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-810MC	0° C to + 70° C
ADC-810MM	-55° C to + 125° C
ADC-811MC	0° C to + 70° C
ADC-811MM	-55° C to + 125° C

ACCESSORIES

Part Number	Description
TP10K or TP100K	Trimming Potentiometers

ADC-815, ADC-825
Ultra-Fast 8-Bit
A/D Converters

DATEL

FEATURES

- **8-Bit resolution**
- **700 Nanoseconds or 1 microsecond conversion time**
- **6 Input ranges**
- **Parallel or serial outputs**
- **No calibration required**

GENERAL DESCRIPTION

DATEL's ADC-815 and ADC-825 are very-high-speed-8-bit successive approximation A/D converters in miniature hybrid form. Both models have identical specifications except for conversion time. The ADC-825 has a maximum conversion time of 1 microsecond while the ultra-fast ADC-815 accomplishes an 8-bit conversion in only 700 nanoseconds, maximum.

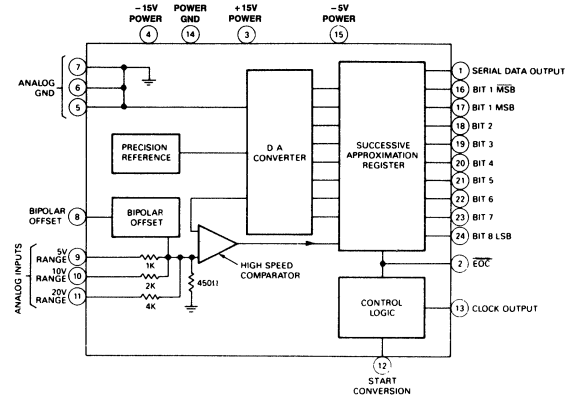
These converters feature six analog input voltage ranges: 0 to + 5V dc, 0 to + 10V dc, 0 to + 20V dc, ± 2.5V dc, ± 5V dc and ± 10V dc. Selection of input ranges is accomplished by simple external pin connection.

Operation of these devices is further simplified by complete functional laser trimming, resulting in a factory-trimmed converter that requires no external adjustments.

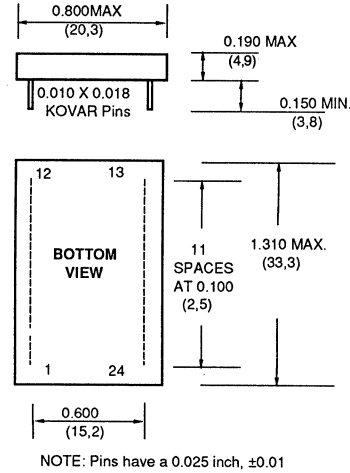
Each converter is a functionally complete unit requiring a minimum of passive external components for operation, and is packaged in a miniature, hermetically sealed 24-pin ceramic DIP.

Output data is available in parallel or serial form by external pin connection. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. Output coding in the parallel mode is accomplished by connection to either the $\overline{MSB}$ output or the MSB output. Serial output data is coded as straight binary for unipolar operation or offset binary for bipolar operation.

Both models have max. integral nonlinearity of ±½ LSB, differential nonlinearity of ±½ LSB max., gain tempco of 20 ppm/°C max., power supply rejection of ±0.06%/% supply max., and long-term stability of ±0.02%/year. Both models require ±15V and 5V supplies, and are available in different versions for operating temperature ranges of 0°C to +70°C, or −55°C to +125°C.



MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL DATA OUTPUT	13	CLOCK OUTPUT
2	$\overline{EOC}$	14	POWER GROUND
3	+15V POWER IN	15	+5V POWER IN
4	−15V POWER IN	16	BIT 1 OUT ($\overline{MSB}$)
5	ANALOG GROUND	17	BIT 1 OUT (MSB)
6	ANALOG GROUND	18	BIT 2 OUT
7	ANALOG GROUND	19	BIT 3 OUT
8	BIPOLAR OFFSET	20	BIT 4 OUT
9	ANALOG INPUT, 5V RANGE	21	BIT 5 OUT
10	ANALOG INPUT, 10V RANGE	22	BIT 6 OUT
11	ANALOG INPUT, 20V RANGE	23	BIT 7 OUT
12	START CONVERSION	24	BIT 8 OUT (LSB)

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ABSOLUTE MAXIMUM RATINGS	ADC-815	ADC-825
Positive Supply	+18V	
Negative Supply	−18V	
Logic Supply	+7V	
Digital Inputs	+5.5V	
Analog Inputs	±25V	

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS	
Analog Input Ranges,[1] Unipolar	0 to +5V, 0 to +10V, 0 to +20V
Bipolar	±2.5V, ±5V, ±10V
Input Impedance, 5V Range	1.34K
10V Range	2.3K
20V Range	4.27K
Start Conversion	+2V min. to +5.5V max. Positive Pulse 50 nsec. min. duration, 10 nsec. typ. rise and fall times. Positive Going Edge resets outputs to 011...1 and sets $\overline{EOC}$ high. Negative going edge initiates conversion. Loading: 2 TTL loads.
Bipolar Offset	Hold high (+5V) for bipolar operation, hold low (ground) for unipolar operation.
OUTPUTS	
Parallel Output Data	9 parallel lines (8 binary bits plus $\overline{MSB}$) V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V Loading: 4 TTL loads
Serial Output Data	NRZ format successive Decision pulse output at internal clock rate generated during conversion. MSB first. Loading: 4 TTL loads
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary, Two's Complement
$\overline{EOC}$	Conversion Status Signal. High ≥ +2.4V during conversion and reset periods. Low ≤ +0.4V when conversion complete. Loading: 4 TTL loads
Clock Output	Internal clock pulse train of negative going pulses[2] from +5V to 0V. Loading: 6 TTL loads

PERFORMANCE		
Conversion Time[3], max.	700 nsec.	1 μsec.
Resolution	8 bits	
Nonlinearity	± ½ LSB max.	
Differential Nonlinearity	± ½ LSB max.	
Gain Error	± ½ LSB max.	
Zero Error	± ½ LSB max.	
Gain Tempco, 0°C to +70°C[4]	±20 ppm of FSR/°C max.[5]	
Zero Drift	±150 μV/°C max.	
Offset Tempco	±15 ppm of FSR/°C Max.[5]	
Long Term Stability	±0.02% year	
No Missing Codes	Over Operating Temp. Range	
Power Supply Rejection, max.	±0.06%/% Supply	

POWER REQUIREMENTS	
Analog Supply	±15V ±0.5V at 35 mA max. −15V ±0.5V at 15 mA max.
Logic Supply	+5V ±0.25V at 100 mA max.
Power Dissipation	1.25W max.
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, MC	0°C to +70°C
MR	−25°C to +85°C
MM	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C
Package Type	24 pin Ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

FOOTNOTES:

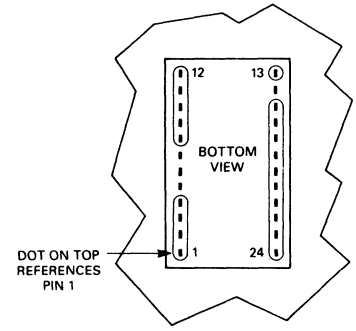
1. Unused analog inputs must be grounded.
2. At 15.9 MHz for the ADC-815, 9.52 MHz for the ADC-825.
3. The conversion time temperature coefficient for these converters is 0.15%/°C. This tempco is positive.
4. Doubles outside this temperature range.
5. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Use of a ground plane is particularly important with high-speed data converters as it reduces high frequency noise and aids in decoupling analog signals from digital signals. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. The basic configuration of the ground plane directly below the ADC-815 or ADC-825 is shown in the ground plane layout diagram. This layout should be modified after selection of analog input range to include unused analog inputs.
2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference. Unused analog inputs should be grounded.
3. Applications of the ADC-815 and ADC-825 that require an input buffer amplifier may be satisfied by the use of DATEL's AM-1435, an ultra fast hybrid device featuring a maximum settling time of 85 nanoseconds.
4. Analog and digital supplies are internally bypassed to ground with 0.01 μF capacitors; however, it is recommended that the +15V, −15V and +5V supplies be additionally bypassed externally with 1 μF electrolytic capacitors as shown in the connection diagrams.
5. In the bipolar mode, two's complement output coding is available by using the $\overline{MSB}$ output (pin 16); offset binary coding is obtained by using the MSB output (pin 17). Unipolar operation requires use of the MSB output (pin 17) to achieve straight binary output coding.

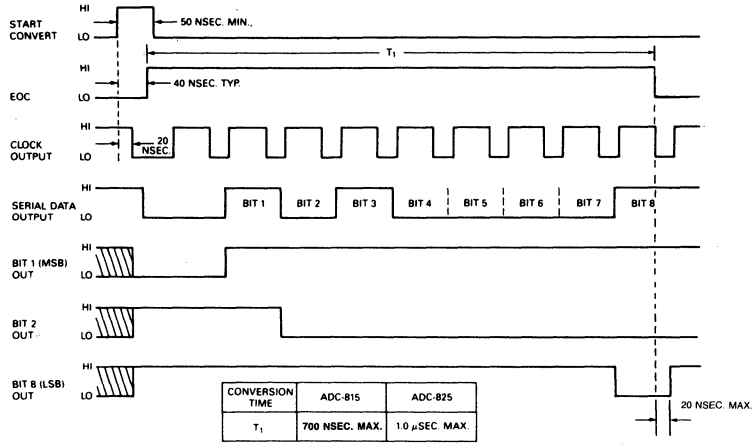
6. Serial output data is available at pin 1 in standard NRZ format with the MSB appearing first. Coding is straight binary for unipolar operation or offset binary for bipolar operation. Synchronization of serial output data is achieved by use of the clock output (pin 13). Each data bit is valid when the clock output is high and appears in succession from the MSB at the second clock low to high transition to the LSB at the ninth clock low to high transition.
7. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-40, an ultra-fast hybrid unit featuring 40 nanosecond acquisition time and a ±2.5V input range.
8. These converters have a maximum power dissipation of 1.25W. The case-to-ambient thermal resistance for this package is approximately 33°C per watt. For operation in ambient temperatures exceeding +83°C, airflow of at least 400 linear feet per minute is recommended.

BASIC GROUND PLANE LAYOUT



THIS BASIC GROUND PLANE LAYOUT SHOULD BE MODIFIED BEFORE IMPLEMENTATION TO INCLUDE UNUSED ANALOG INPUTS.

TIMING DIAGRAM FOR ADC-815, ADC-825
OUTPUT: 10100001



CONVERSION TIME	ADC-815	ADC-825
T_1	700 NSEC. MAX.	1.0 µSEC. MAX.

CODING TABLES

UNIPOLAR OPERATION

UNIPOLAR SCALE	OUTPUT CODING* STRAIGHT BINARY	ANALOG INPUT 0 to +5V	0 to +10V	0 to +20V
F.S. - 1 LSB	1111 1111	+4.980V	+9.961V	+19.922V
¾ F.S.	1100 0000	+3.750V	+7.500V	+15.000V
½ F.S.	1000 0000	+2.500V	+5.000V	+10.000V
¼ F.S.	0100 0000	+1.250V	+2.500V	+5.000V
1 LSB	0000 0001	+0.020V	+0.039V	+0.078V
0	0000 0000	0.000V	0.000V	0.000V

*FOR PARALLEL OR SERIAL OUTPUT DATA

BIPOLAR OPERATION

BIPOLAR SCALE	OUTPUT CODING OFFSET BINARY[1]	OUTPUT CODING TWO'S COMPLEMENT[2]	INPUT VOLTAGE RANGE ±2.5V	±5V	±10V
+F.S.−1 LSB	1111 1111	0111 1111	+2.480V	+4.961V	+9.922V
+½ F.S.	1100 0000	0100 0000	+1.250V	+2.500V	+5.000V
+1 LSB	1000 0001	0000 0001	+0.020V	+0.039V	+0.078V
0	1000 0000	0000 0000	0.000V	0.000V	0.000V
−½ F.S.	0100 0000	1100 0000	−1.250V	−2.500V	−5.000V
−F.S.+1 LSB	0000 0001	1000 0001	−2.480V	−4.961V	+9.922V
−F.S.	0000 0000	1000 0000	−2.500V	−5.000V	+10.000V

NOTES: 1. FOR PARALLEL OR SERIAL OUTPUT DATA
2. FOR PARALLEL OUTPUT DATA ONLY

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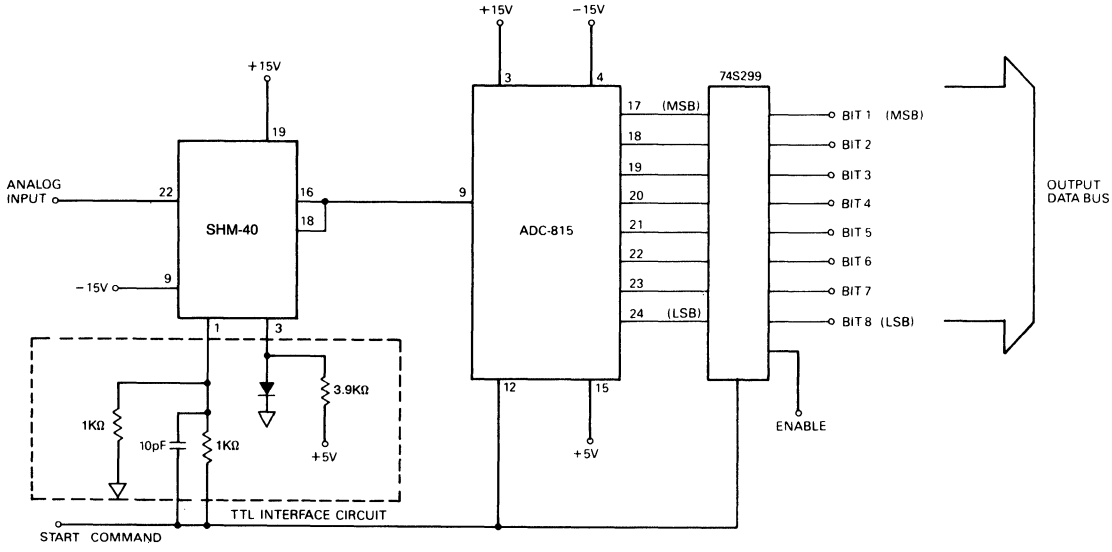
HIGH SPEED DATA SYSTEM



This diagram represents a high speed data system using DATEL's SHM-40 and ADC-815, with an output register, to drive a data bus. The Start Command is a 60 nsec wide, TTL-compatible pulse with a maximum frequency of 1.5 MHz. Upon receipt of a start command, the SHM-40 will track the input voltage and the ADC-815 will reset. On the trailing edge of the start command, the SHM-40 will hold the input and the ADC-815 will begin its conversion. On the leading edge of the next start command, the output data will be clocked out of the output three-state register. The ADC-815 is an 8-bit, 700 nsec, analog-to-digital converter. With this system, a ±2.5V input step can be acquired to 0.1% accuracy in 40 nsec and held to within 80 μV while the A/D conversion takes place. The SHM-40 can also be used with the DATEL's ADC-816, which will yield 10 bits of resolution.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-815MC	0°C to +70°C
ADC-815MM	−55°C to +125°C
ADC-825MC	0°C to +70°C
ADC-825MM	−55°C to +125°C

ACCESSORIES

Part Number	Description
DILS-3	Mating Socket, 24-pin socket

For military devices compliant with MIL-STD-883, contact DATEL.

ADC-816, ADC-826 Ultra-Fast 10-Bit A/D Converters

DATEL

FEATURES

- **10-Bit resolution**
- **800 Nanoseconds or 1.25 microseconds conversion time**
- **6 Input ranges**
- **Unipolar and bipolar operation**
- **Programmable output coding**

GENERAL DESCRIPTION

DATEL's ADC-816 and ADC-826 are very high speed 10-bit successive approximation A/D converters, realized as miniature thick and thin-film hybrids. Both models have identical specifications except for conversion time. The ADC-826 has a maximum conversion time of 1.4 microseconds. The ultra-fast ADC-816 offers a maximum conversion time of only 800 nanoseconds.

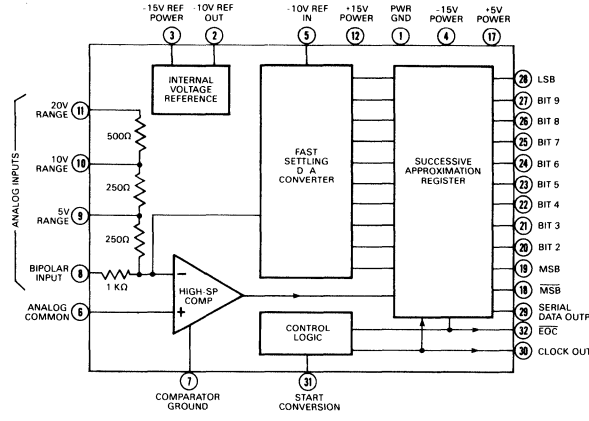
These converters feature six analog input voltage ranges: 0 to −5V dc, 0 to −10V dc, 0 to −20V dc, ±2.5V dc, ±5V dc and ±10V dc. Selection of input range is accomplished by simple external pin connection.

Output data is available in parallel or serial form by external connection. Data is coded as straight binary for unipolar operation and as either offset binary or two's complement for bipolar operation. Two's complement is available in the parallel output mode only and is selected by pin connection.

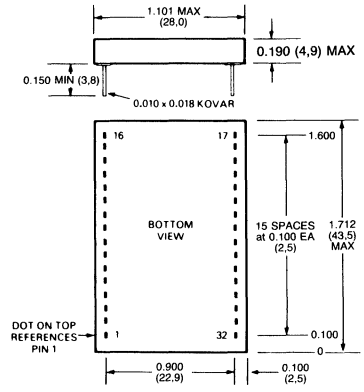
Specifications shared by both models include maximum nonlinearity of ±½ LSB and differential nonlinearity of ±½ LSB maximum.

These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a high-speed comparator, an ultra-fast settling D/A converter, a precision voltage reference, successive approximation register, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a miniature hermetically sealed 32-pin ceramic DIP package.

Both models require ±15V dc and +5V dc supplies, and are available in versions for the 0 to +70°C or −55 to +125°C operating temperature ranges.



MECHANICAL DIMENSIONS



*NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER COM	17	+5V POWER
2	REF OUT	18	$\overline{\text{MSB}}$ 1
3	REF POWER	19	MSB 1
4	−15V POWER	20	BIT 2
5	REF IN	21	BIT 3
6	SIG COM	22	BIT 4
7	COMPARATOR COM	23	BIT 5
8	BIP IN	24	BIT 6
9	5V IN	25	BIT 7
10	10V IN	26	BIT 8
11	20V IN	27	BIT 9
12	+15V POWER	28	LSB 10
13	NC	29	SERIAL DATA OUT
14	NC	30	CLOCK OUT
15	NC	31	START
16	NC	32	$\overline{\text{EOC}}$

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ABSOLUTE MAXIMUM RATINGS

Positive Supply, pin 12	+16V dc
Negative Supply, pin 4	−16V dc
Logic Supply, pin 17	+7V dc
Logic Inputs	+7V dc
Analog Inputs	± Twice selected analog input range

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS

Analog Input Ranges	**unipolar**[1]	0 to −5V, 0 to −10V, 0 to −20V
	bipolar	±2.5V, ±5V, ±10V
	reference	−9.5V to −10.5V
Input Impedance[2]	**5V range**	312Ω
	10V range	625Ω
	20V range	1.25 KΩ
	bipolar input	1 KΩ
	reference (pin 5)	2 KΩ
Start Conversion		2V min. to 5.5V max. positive pulse with duration of 25 nsec. min. Rise and fall times typical 10 nsec. Logic "1" resets converter. Logic "0" initiates conversion. Loading: 1 TTL load.

OUTPUTS

Parallel Output Data	11 Parallel lines of data (10 binary bits + $\overline{\text{MSB}}$) held until next conversion command. V_{OUT} ("0") ≤ +0.4V. V_{OUT} ("1") ≥ +2.4V. Loading: 2 TTL loads
Coding[3]**, unipolar**	Straight Binary
bipolar[4]	Offset Binary, Two's Complement
Serial Output Data	NRZ successive decision pulses out, MSB first, at internal clock frequency Loading: 4 TTL loads.
End of Conversion ($\overline{\text{EOC}}$)	Conversion Status Signal. Output is logic high during reset and conversion, low when conversion is complete. Loading: 4 TTL loads.
Clock Output	Train of positive going, 0 to +5V, 30 nsec. pulses.
Clock Frequency ADC-816MC/MM	14.6 MHz
ADC-826MC/MM	8.1 MHz
Reference Output, Voltage	−10.00V ±0.02V
Current	0 to +20 mA (sink only)
Impedance	10Ω max. f_O ≤ 10 MHz

PERFORMANCE

Resolution	10 bits
Conversion Time[5]**, ADC-816MC**	800 nsec. max.
ADC-826MC/MM	1.4 μsec. max.
Nonlinearity	±½ LSB max.
Differential Nonlinearity[6]	±½ LSB max.
Gain Error[7]**, before adjustment, unipolar**	±0.3% of FSR max.[8]
bipolar	±0.2% of FSR max.
Zero Error, before adjustment, unipolar	±0.2% of FSR max.
Offset Error, before adjustment, bipolar	±0.1% of FSR max.
Gain Tempco[9]**, unipolar**	±37 ppm/°C max.
bipolar	±28 ppm/°C max.
Zero Tempco, unipolar	±12 ppm/°C max.
bipolar	±23 ppm/°C max.
Conversion Time Tempco	±0.1%/°C
Reference Output Tempco	±20 ppm/°C max.
Power Supply Rejection	±0.008%/% supply
No missing codes	Over operating Temp. Range

POWER REQUIREMENTS

Analog Supply, pin 12	+15V dc ±1V dc at 106 mA max.
pin 4	−15V dc ±1V dc at 60 mA max.
Reference Supply, pin 3	−15V dc ±0.5V dc at 34 mA max.
Logic Supply, pin 17	+5V dc ±0.25V dc at 80 mA max.
Power Dissipation	1.7 watts typical, 2.9 watts max.

PHYSICAL/ENVIRONMENTAL

Operating Temp. Range Suffix C	0°C to +70°C
Suffix M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Type	32-pin hermetically sealed Ceramic DIP
Pins	0.010 x 0.018 inch gold plated Kovar
Weight	0.8 ounces (23 grams)

FOOTNOTES:

1. Bipolar input must be tied to ground.
2. Resistance tolerance is −30%, +50%, ±50 ppm/°C.
3. All coding is inverted analog.
4. Two's Complement Binary available for parallel output only.
5. Maximum conversion time is specified at full rated operating temperature. The ADC-816MM has a maximum conversion time of 900 nanoseconds at full rated operating temperature. See Technical note 3 for 25°C conversion time.
6. Tested over full rated operating temperature range.
7. Includes Zero Error.
8. FSR is Full-Scale Range.
9. Includes internal reference Tempco. Given as a maximum for 5V FSR, these values improve by 10% for 10V FSR, and by 20% for 20V FSR.

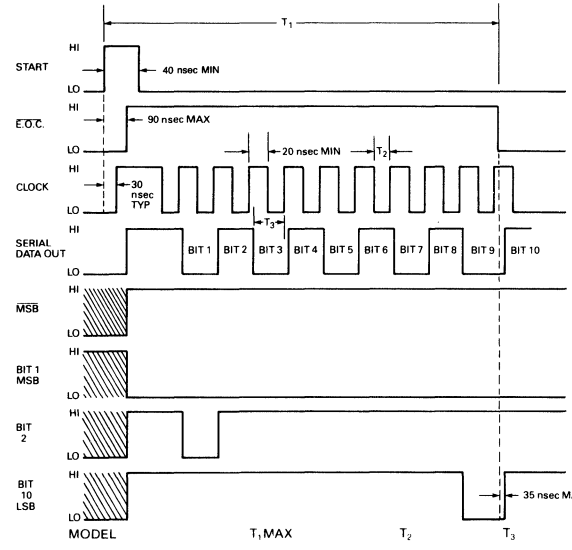
TECHNICAL NOTES

1. Use of good high frequency circuit board layout techniques is required for rated performance. The power common (pin 1), comparator common (pin 7), and signal common (pin 6) are not connected internally, and therefore must be connected externally as directly as possible, through a low resistance, low inductance path. The extensive use of a ground plane for all common connections is highly recommended. Also, it is recommended that the analog and digital supplies, although they are internally bypassed with 0.033 μF capacitors, be additionally bypassed externally at the supply pins with 1 μF electrolytic capacitors.
2. The digital outputs are not buffered from their internal application and so are sensitive to unusual loading or long lines. Terminate these outputs with normal TTL inputs not more than 3 inches from the data output pin. Analog inputs must be non-reactive such that leads should be short and purely resistive. The reactive component of any analog input source, as seen at the analog input pin, should be less than 0.3% of the analog input resistance at that pin, for frequencies below 20 MHz.
3. Conversion time is measured from the rising edge of a 40 nanosecond start input pulse to the falling edge of the $\overline{\text{EOC}}$ output. The conversion time is factory set at +25°C for the ADC-816MC/MM at 750 nanoseconds and 1.25 microseconds for the ADC-826MC/MM. The worst case conversion time at the maximum rated operating temperature is given as a maximum specification.
4. To use the internal reference, the reference supply pin (pin 3) must be connected to the −15V supply. If the reference supply pin (pin 3) is disconnected or grounded, the internal reference will be disabled at a power saving of approximately 200 mW.

5. Serial output data is available in NRZ format successive decision pulses, MSB first, in straight binary or offset binary coding. Synchronization of the serial output data is achieved through the use of the clock output (pin 30). This same clock output also controls the output register such that at the rising edge of the output clock the previous data bit may be clocked out. However, there will be no clock edge to clock out the LSB. A Serial DATA Recovery circuit is diagrammed on the applications page that will correct this.
6. These converters have a case-to-ambient thermal resistance of 22°C per watt. At temperatures above +70°C, an air flow of at least 400 linear feet per minute is recommended. To operate at elevated temperatures it is recommended that the converter be mounted directly to the circuit board (without the use of a mounting socket) and that good thermal contact be established between the case bottom and the circuit board ground plane by use of a silicone thermal joint compound such as Wakefield Type 120 or equivalent.
7. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-HU, an ultra-fast hybrid unit featuring 25 nanoseconds acquisition time and a ±2.5V input range.

APPLICATIONS

TIMING DIAGRAM FOR ADC-816, ADC-826



MODEL	T_1 MAX	T_2	T_3
ADC-816MC/MM	800 n sec	44 n sec	23-64 n sec
ADC-826MC/MM	1.4 μ sec	100 n sec	79-114 n sec

CALIBRATION PROCEDURE

1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of between 40 nanoseconds and 100 nanoseconds is applied to the start conversion input (pin 31) at the rate of 200 kHz.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0 – ½ LSB) or the bipolar offset adjustment (+FS-½ LSB). Adjust the appropriate timing potentiometer so that the output code flickers equally between X0000 00000 and X0000 00001. The MSB indicated by X will be 0 for straight binary and offset binary coding or 1 for two's complement output coding.
3. **Full Scale Adjustment**
   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (–FS + 1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X1111 11111 and X1111 11110. The MSB indicated by X, will be 1 for straight binary and offset binary coding or coding or 0 for two's complement output coding.

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 To –5V	Zero	–2.4 mV
	Gain	–4.9927V
0 To –10V	Zero	–4.9 mV
	Gain	–9.9854V
0 To –20V	Zero	–9.8 mV
	Gain	–19.9707V

BIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
±2.5V	Offset	±2.4975V
	Gain	–2.4927V
±5V	Offset	±4.9951V
	Gain	–4.9854V
±10V	Offset	±9.9902V
	Gain	–9.9707V

CODING TABLES

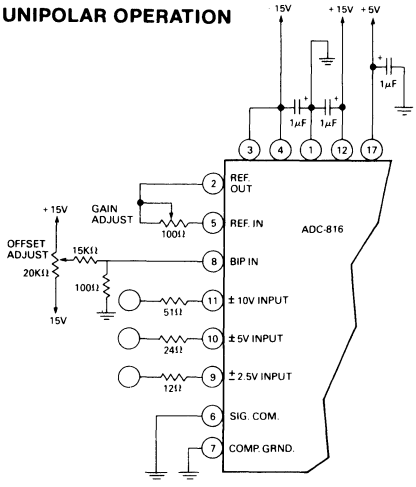
UNIPOLAR OPERATION

INPUT RANGE			STRAIGHT BINARY		
0 to –20V	0 to –10V	0 to –5V	MSB		LSB
–19.9805	–9.9902V	–4.9951	1111	11	1111
–17.5000	–8.7500	–4.3750	1110	00	0000
–15.0000	–7.5000	–3.7500	1100	00	0000
–10.0000	–5.0000	–2.5000	1000	00	0000
–5.0000	–2.5000	–1.2500	0100	00	0000
–2.5000	–1.2500	–0.6250	0010	00	0000
–0.0198	–0.0098	–0.0049	0000	00	0001
0.0000	0.0000	0.0000	0000	00	0000

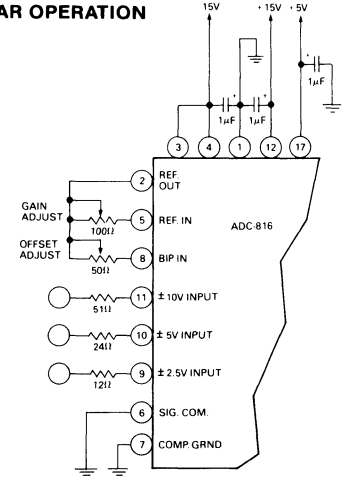
BINARY OPERATION

INPUT RANGE			OFFSET BINARY			TWO'S COMPLEMENT		
±10V	±5V	±2.5V	MSB		LSB	MSB		LSB
–9.9805	–4.9902	–2.4951	1111	11	1111	0111	11	1111
–7.5000	–3.7500	–1.8750	1110	00	0000	0110	00	0000
–5.0000	–2.5000	–1.2500	1100	00	0000	0100	00	0000
0.0000	0.0000	0.0000	1000	00	0000	0000	00	0000
+5.0000	+2.5000	+1.2500	0100	00	0000	1100	00	0000
+7.5000	+3.7500	+1.8750	0010	00	0000	1010	00	0000
+9.9805	+4.9902	+2.4951	0000	00	0001	1000	00	0001
+10.0000	+5.0000	+2.5000	0000	00	0000	1000	00	0000

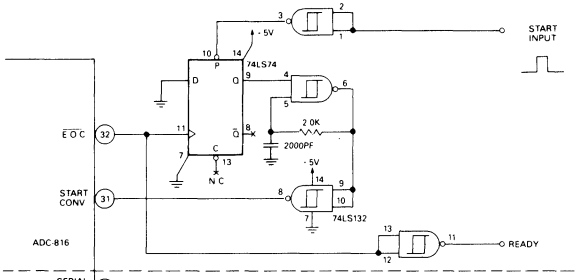
UNIPOLAR OPERATION



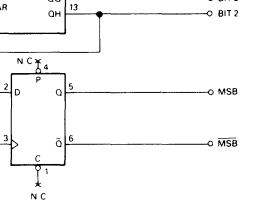
BIPOLAR OPERATION



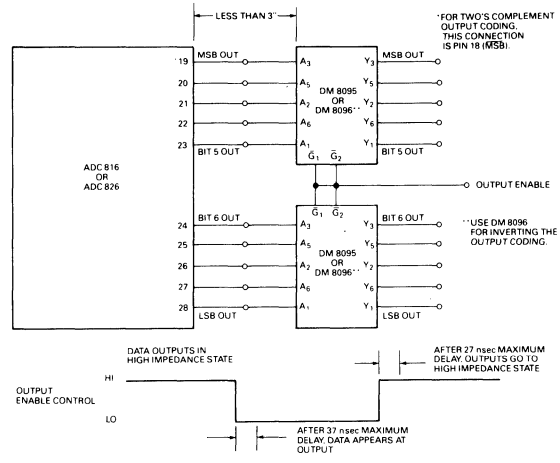
UNCONDITIONAL/START CIRCUIT



SERIAL DATA RECOVERY CIRCUIT



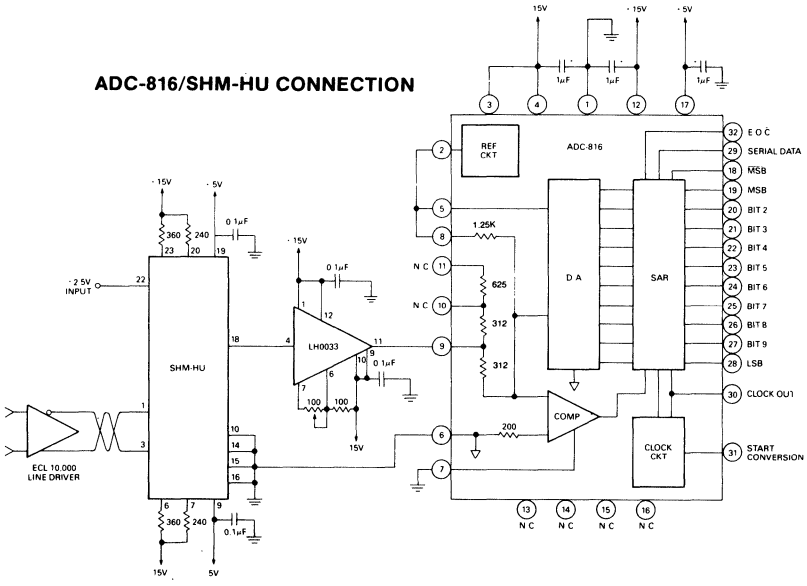
HIGH SPEED THREE-STATE OUTPUT BUFFER GROUND PLANE LAYOUT



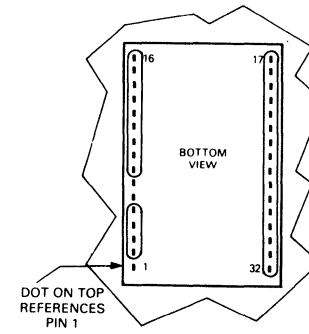
The Unconditional Start Circuit, shown for the ADC-816/826 insures the initiation of a conversion cycle upon the application of one start pulse of 40 nanoseconds minimum pulse width regardless of converter status.

The serial data output of the ADC-816/826 is converted into parallel form, with the addition of an $\overline{\text{MSB}}$ output, by the Serial Data Recovery circuit. Users should refer to technical note No. 2 on the loading of the ADC-816/826 digital outputs when using these circuits.

ADC-816/SHM-HU CONNECTION



GROUND PLANE LAYOUT



When the ADC-816 or ADC-826 is configured as shown here with DATEL's SHM-HU hybrid sample-hold, a ±2.5V input step can be acquired to 0.1% accuracy in 30 nanoseconds and held to within 40 μV while the A/D conversion takes place. Use of the SHM-HU reduces the time over which the input signal is averaged to a few nanoseconds (an A/D converter without a sample-hold averages the analog input signal over the total conversion time of the A/D).

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-816MC	0°C To +70°C
ADC-816MM	−55°C To +125°C
ADC-826MC	−0°C To +70°C
ADC-826MM	−55°C To +125°C

ACCESSORIES

Part Number	Description
DILS-2	Mating Socket (2 per converter)
TP20K, TP100, TP50	Trimming Potentiometers

For military devices compliant to MIL-STD-883, consult DATEL.

ADC-817A, ADC-827A Fast 12-Bit A/D Converters

FEATURES

- **12-Bit resolution**
- **2 Microseconds or 3 microseconds conversion times**
- **Unipolar and bipolar operation**
- **6 Programmable input ranges**
- **Parallel data output**

GENERAL DESCRIPTION

The ADC-817A and ADC-827A are high-speed two-pass A/D converters in miniature hybrid from using thick-and thin-film hybrid technology. Both models have identical specifications except for conversion times. The ADC-827 has a maximum conversion time of 3.0 microseconds, while the ADC-817A accomplishes a 12-bit conversion in only 2.0 microseconds, maximum.

These converters feature six analog input voltage ranges: 0 to -5V dc, 0 to -10V dc, 0 to -20V dc, ±2.5V dc, ±5V dc, and ±10V dc. Selection of input range is accomplished by simple external pin connection. Both devices provide a user-selectable, fast settling precision input buffer with input impedance of 100MΩ, allowing them to be driven directly from a high impedance source. The input buffer may be bypassed.

Output data is coded as straight binary for unipolar operation and as either offset binary or two's complement for bipolar operation.

Specifications shared by both models include maximum nonlinearity of ±1 LSB maximum and a gain tempco of 25 ppm/ °C maximum.

These converters are functionally complete units requiring a minimum of passive external components for operation. Each unit is composed of a fast settling precision input buffer, an ultrafast settling D/A converter, a precision voltage reference, clock generator and control logic circuits. The combination of unique design and the latest hybrid fabrication technology allows this level of performance to be achieved in a minature, hermetically sealed 32-pin ceramic DIP package.

Both models require ±15V dc and +5V supplies, and are available in versions for the 0 to 70 °C or -55 to +125 °C operating temperature ranges.

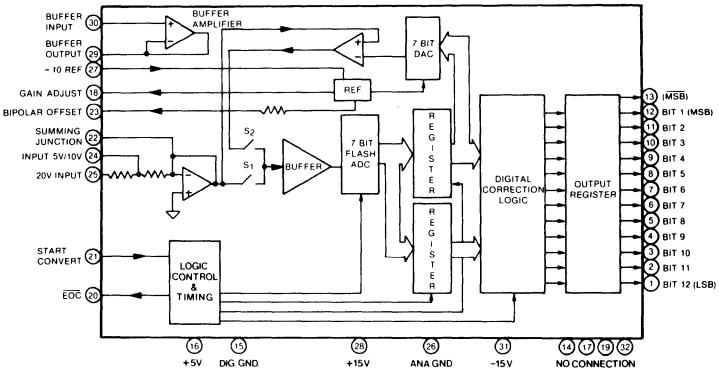
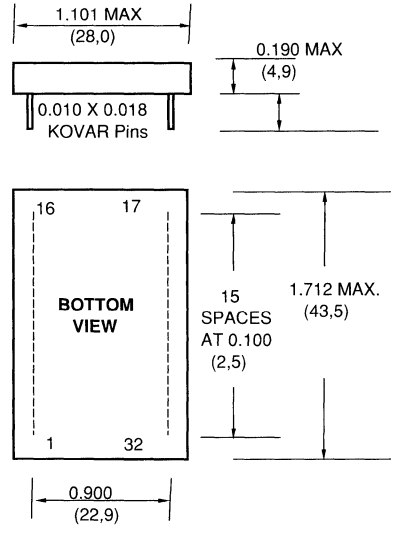


Figure 1. ADC-817A,-827A Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	BIT 12 OUT (LBS)
2	BIT 11 OUT
3	BIT 10 OUT
4	BIT 9 OUT
5	BIT 8 OUT
6	BIT 7 OUT
7	BIT 6 OUT
8	BIT 5 OUT
9	BIT 4 OUT
10	BIT 3 OUT
11	BIT 2 OUT
12	BIT 1 OUT (MSB)
13	BIT 1 OUT (MSB)
14	NO CONNECTION
15	DIGITAL GROUND
16	+5V POWER
17	NO CONNECTION
18	REFERENCE OUTPUT
19	NO CONNECTION
20	EOC OUTPUT
21	START CONVERSION
22	SUMMING JUNCTION
23	BIPOLAR OFFSET
24	5/10V INPUT RANGE
25	20V INPUT RANGE
26	ANALOG GROUND
27	REFERENCE INPUT
28	+15V POWER
29	BUFFER OUTPUT
30	BUFFER INPUT
31	-15V POWER
32	NO CONNECTION

ABSOLUTE MAXIMUM RATINGS

Positive Supply	+18V
Negative Supply	-18V
Logic Supply	+7V
Digital Inputs	+5.5V
Analog Inputs	±20V
Buffer Amplifier Input	±15V

FUNCTIONAL SPECIFICATIONS

Typical at 25 °C, ±15V supplies, unless otherwise noted.

INPUTS

Analog Input Ranges Unipolar	0 to -5V, 0 to -10V, 0 to -20V
Bipolar	±2.5Vm ±5V, ±10V
Input Impedance	
5V/10V Ranges	1.05 KΩ
20V Range	4Ω
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 50 nsec. min. Rise and fall times <30 nsec. Logic "1" to "0" transition initiates next conversion.
Logic Levels:	
Logic "1"	2.4V min.
Logic "0"	0.4V max.
Logic Loading:	
Logic"1"	-160 µA max.
Logic "0"	6.4 mA max.
Buffer Amplifier Gain	±1
Buffer Amplifier Input Voltage	±10.0V
Buffer Amplifier Input Impedance	100 MΩ
Buffer Amplifier Settling Time[1]	500 nsec. max.

OUTPUTS

Parallel Output Data	13 parallel lines (12 binary bits plus MSB) valid from negative going edge of EOC pulse to positive going edge of START CONVERSION pulse. Vout "0" ≤ +0.4V V_{OUT} "1" ≥ +2.4V Loading: 4 TTL loads
Coding:	
Unipolar[2]	Straight Binary
Bipolar[3]	Offset Binary, Two's Complement[3]
End of Conversion (EOC)	Conversion Status Signal: 4 TTL Loads V_{OUT} "0" ≤ +0.4V for conversion complete V_{OUT} "1" ≤ +2.4V for conversion in progress

PERFORMANCE

Resolution	12 binary bits[4]
Nonlinearity, max	±1 LSB
Differential Nonlinearity, max	±1LSB
Temp. Coeff. of Gain, max[4]	±25 ppm/ °C of FSR
Temp. Coeff. of Zero, unipolar max.	±150 µV/ °C of FSR
Temp. Coeff. of bipolar, zero error, max.[4]	±15 ppm of FSR/ °C[6]
Diff. Nonlinearity Tempco, max	±5 ppm/ °C of FSR
Power Supply Rejection	±0.01%/% Supply max.
Conversion Time Over Full Temp	2.0 µsec. max., ADC-817A 3.0 µsec. max., ADC-827A

POWER REQUIREMENTS

Supply Voltage	+15V dc ±0.5V at +70 mA max. -15V dc ±0.5V at -50 mA max. +5V dc ±0.25V at +65 mA max.
Power Dissipation	2.2 W max.

PHYSICAL/ENVIRONMENTAL

Operating Temp. Range,	
MC	0 °C to +70 °C
MM	-55 °C to +125 °C
Storage Temp. Range	-65 °C to +150 °C
Package Type	32 pin hermetically sealed ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounce (14 grams)

FOOTNOTES

1. 10V step to 0.01%, 5V and 20V steps settle to 0.01% in 150 nanoseconds and 800 nanoseconds, respectively.
2. These converters operate with inverted analog, that is F.S. +1 LSB is encoded as 1111 1111 1111 and +FS is encoded as 0000 0000 0000 (examples given are for offset binary coding).
3. Parallel output data only is available in offset binary (uses MSB out) or two's complement coding (uses MSB out).
4. For 0°C to +70°C operation, these values double outside of this temperature range.
5. FSR is Full Scale Range.

TECHNICAL NOTES

1. The high operating speed of these converters requires that good high frequency board layout techniques be used. Capacitance from long leads on the data outputs can prevent the internal DAC from turning on in time, creating linearity errors. Leads from data outputs should be kept as short as possible, output leads longer than 1 inch (2.5 cm) require the use of an output register. Ground loop problems are avoided by connecting all grounds on the board to the ground plane. Analog and digital grounds are connected internally.

2. Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference.

3. The ADC-817A/827A provides an internal buffer amplifier. Use of this buffer provides an input impedance greater than 100 MΩ, allowing the A/D to be driven from a high impedance source or directly from an analog multiplexer. When using the input buffer, a delay equal to its setting time must be allowed between input level change and the negative going edge of the start conversion pulse. If the buffer is not required, its input should be connected to analog ground to avoid introducing noise in to the converter.

4. Both analog and digital supplies should be bypassed to ground with 1 µF electrolytic capacitors in parallel with 0.1 µF ceramic capacitors as shown in the connections diagrams. Bypass capacitors should be located directly

adjacent to, or on, each supply pin. The -10V reference output (pin 18) should be bypassed to ground with a 2.2 µF electrolytic capacitor mounted as previously indicated.

5. In the bipolar mode, two's complement output coding is available by using the MSB output (pin 13); offset binary coding is obtained by using the MSB output (pin 12). Unipolar operation requires use of the MSB output (pin 12) to achieve straight binary output coding.

6. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-45 or SHM-4860 featuring 200 nanosecond acquisition time and 0.01% accuracy. The SHM-45 offers gains of -1 or -2.

7. These converters have a maximum power dissipation of 2.2W. The case-to-ambient thermal resistance for this package is approximately 28°C per watt. For operation in ambient temperatures exceeding +70°C, care must be taken to ensure free air circulation in the vicinity of the converter.

NOTE

In any application using the ADC-817A or the ADC-827A, signal integrity and noise isolation are a function of grounding. The suggested ground plane shown should be used whenever possible.

1

GROUND PLANE LAYOUT

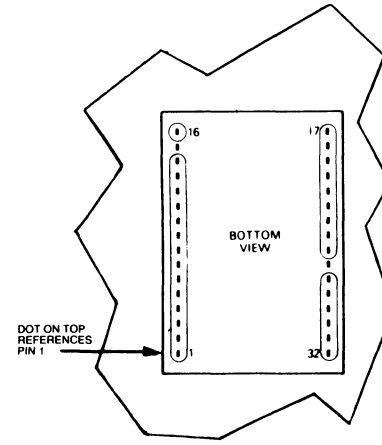


Figure 3. Ground Plane Layout

TIMING DIAGRAM OPERATING PERIODS

ADC-817A	ADC-827A
T1 2.0 µSEC.	3.0 µSEC.

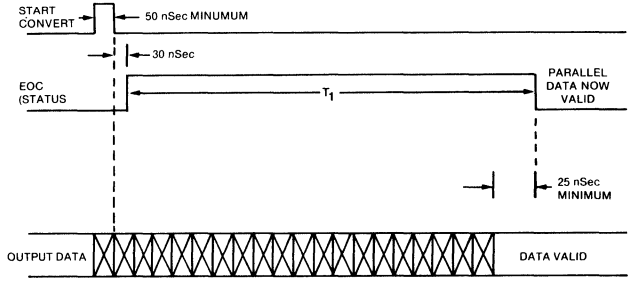


Figure 2. Timing Diagram for ADC-817A, ADC-827A

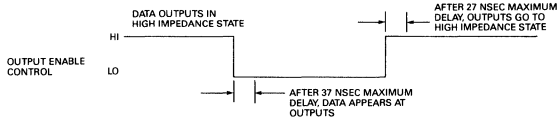
OUTPUT CODING

UNIPOLAR SCALE	UNIPOLAR ANALOG INPUT -20V RANGE	-10V RANGE	-5V RANGE	STRAIGHT BINARY OUTPUT CODE
-FS + 1 LSB	-19.9952V	-9.9976V	-4.9988V	1111 1111 1111
-7/8 FS	-17.5000V	-8.7500V	-4.3750V	1110 0000 0000
-3/4 FS	-15.0000V	-7.5000V	-3.7500V	1100 0000 0000
-1/2 FS	-10.0000V	-5.0000V	-2.5000V	1000 0000 0000
-1/4 FS	-5.0000V	-2.5000V	-1.2500V	0100 0000 0000
-1 LSB	-0.0049V	-0.0024V	-0.0012V	0000 0000 0001
0	-0.0000V	-0.0000V	-0.0000V	0000 0000 0000

BIPOLAR SCALE	ANALOG INPUT ±10V RANGE	±5V RANGE	±2.5V RANGE	DATA OUTPUT CODING OFFSET BINARY	TWO's COMPLEMENT
-FS + 1 LSB	-9.9951V	-4.9976V	-2.4988V	1111 1111 1111	0111 1111 1111
-1/2 FS	-5.0000V	-2.5000V	-1.2500V	1100 0000 0000	0100 0000 0000
-1 LSB	-0.0049V	-0.0024V	-0.0012V	1000 0000 0001	0000 0000 0001
0	0.0000V	0.0000V	0.0000V	1000 0000 0000	0000 0000 0000
+1 LSB	+0.0049V	+0.0024V	+0.0012V	0111 1111 1111	1111 1111 1111
+1/2 FS	+5.0000V	+2.5000V	+1.2500V	0100 0000 0000	1100 0000 0000
+FS -1 LSB	+9.9951V	+4.9976V	+2.4988V	0000 0000 0001	1000 0000 0001
+FS	+10.0000V	+5.0000V	+2.5000V	0000 0000 0000	1000 0000 0000

Providing Three-State Outputs

For applications where the converted input must interface to tri-state TTL or CMOS logic, the ADC-817A OR ADC-827A outputs are easily converted using buffers such as the DM8095's shown in the diagram. Signal length must be less than one inch between devices to ensure signal integrity. Also note that two's complement outputs are available from the ADC-817A and ADC-827A by using pin 13 instead of pin 12 as the MSB output. The timing diagram shows the delays incurred as the signal passes through the buffers.



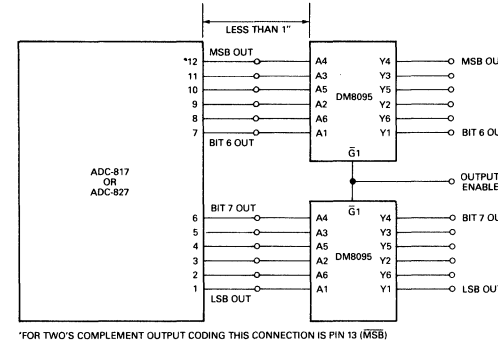
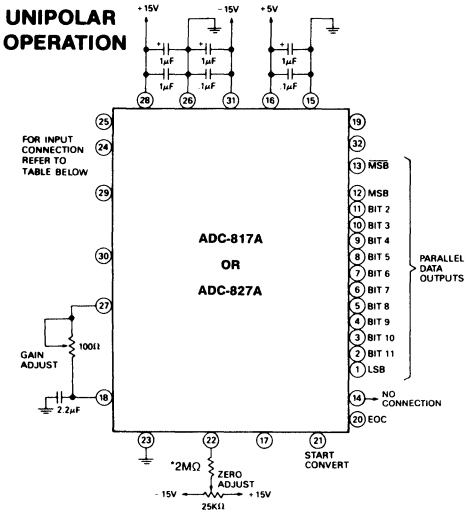


Figure 4. High Speed Three-State Output Buffer

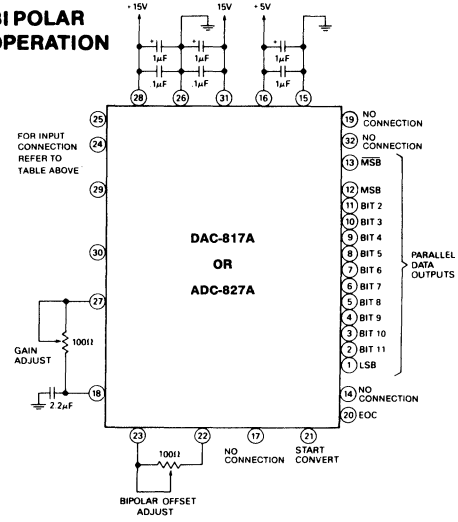
TYPICAL CONNECTIONS

UNIPOLAR OPERATION



*FOR GREATER UNIPOLAR ZERO GAIN ADJUSTMENT THE 2 MEG OHM RESISTOR MAY BE REDUCED TO A VALUE OF 500 KΩ

BIPOLAR OPERATION



CALIBRATION PROCEDURE

1. Connect the converter as shown in the applicable connections diagram. A trigger pulse of 50 nanoseconds minimum is applied to the start conversion input (pin 21) at a rate of 200 kHz.

2. **Zero and Offset Adjustments**

   Apply a precision voltage reference source between the appropriate input for the selected full scale range and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (0 -1/2 LSB) or the bipolar offset adjustment (+FS -1/2 LSB). Adjust the appropriate trimming potentiometer so that the output code flickers equally between X000 0000 0000 and X000 0000 0001. The MSB, indicated by X, will be 0 for straight binary and offset binary output coding, or 1 for two's complement output coding.

3. **Full Scale Adjustment**

   Set the output of the voltage reference source used in step 2 to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (-FS +1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between X1111 1111 1111 and X111 1111 1110. The MSB, indicated by X, will be 1 for straight binary and offset binary output coding, or 0 for two's complement output coding.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 TO -5V	ZERO GAIN	-0.6 mV -4.9982V
0 TO -10V	ZERO GAIN	-1.2mV -9.9963V
0 TO -20V	ZERO GAIN	-2.44mV -19.9925V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	+2.4994V -2.4982V
±5V	OFFSET GAIN	+4.9988V -4.9963V
±10V	OFFSET GAIN	+9.9976V -9.9927V

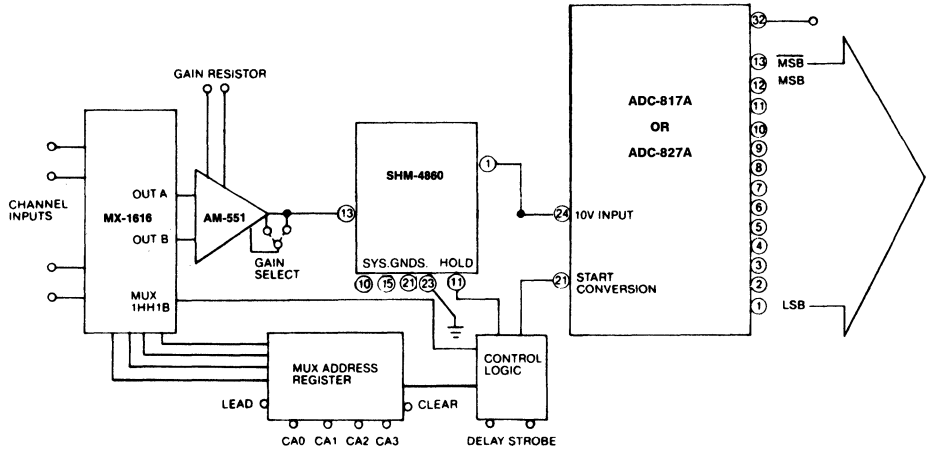


Figure 5. High Speed Data Acquisition System

The ADC-817A/827A configured as shown with DATEL's MX-1616, a high speed CMOS multiplexer, AM-551, a hybrid precision programmable gain instrumentation amplifier, and SHM-4860, a 200 nanosecond, 0.01% hybrid sample hold forms an 8-channel (differential), 12-bit, hight speed data acquisition system capable of throughput rates of 200 kHz.

INPUT CONNECTIONS

INPUT VOLTAGE RANGE	*WITH INPUT BUFFER			WITHOUT INPUT BUFFER		
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER	
0 to -5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
0 to -10V	30	29 to 24	–	24	–	30 to 26
±2.5V	30	29 to 24	22 to 25	24	22 to 25	30 to 26
±5V	30	29 to 24	–	24	–	30 to 26
±10V	30	29 to 25	–	25	–	30 to 26

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-817A MC	0 °C to +70 °C
ADC-817A MM	-55 °C to +125 °C
ADC-827A MC	0 °C to +70 °C
ADC-827A MM	-55 °C to +125 °C

ACCESSORIES

Part Number	Description
TP25K or TP100K	Trimming Potentiometers

For military devices compliant to MIL-STD-883, consult the factory.

ADC-830
Microprocessor-Compatible 8-Bit A/D Converter

FEATURES

- **Microprocessor-compatible**
- **± ½ LSB total adjustment error**
- **100 Microseconds conversion time**
- **Differential analog inputs**
- **Ratiometric operation**
- **Single-supply operation**

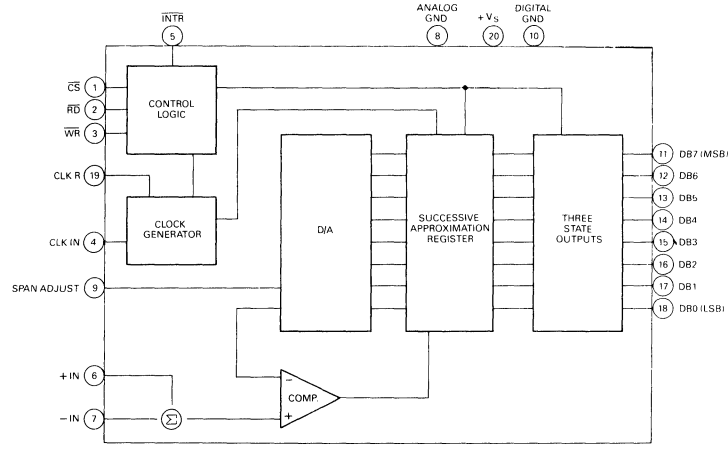
GENERAL DESCRIPTION

DATEL's ADC-830 is a low cost, 8-bit, CMOS A/D converter designed to operate directly with the 8080A control bus via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic. The ADC-830's digital control inputs, $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$, are active low, and are available in all microprocessor memory systems. Upon completion of a conversion, an Interrupt signal is generated at the converter's output. The ADC-830 will operate as a normal A/D for non-microprocessor based applications.

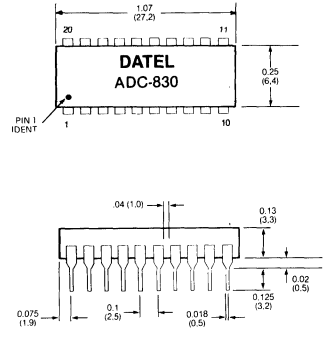
Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8-bit conversion in 100 microseconds with a maximum total adjusted error of only ± ½ LSB. No zero adjust is required. Also, the differential analog input allows the user to increase the common mode rejection and offset the zero value of the analog input.

Other features include single supply operation and an internal clock generator. The clock generator requires only an external RC network or, it may be driven by an external clock. The clock frequency range is 100 kHz to 1.2 MHz. In addition, the ADC-830 operates ratiometrically or with a 2,5V dc, 5V dc, or, to allow the encoding of smaller analog input voltage ranges, an analog-span-adjusted reference.

The ADC-830 is packaged in 20-pin plastic DIP and operates over the 0°C to +70°C commercial temperature range. Power requirement is +5V dc. With it's combination of low cost, small size, ease of digital interfacing, and versatility of analog interfacing, the ADC-830 is the ideal choice for many process control and instrumentation applications.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)	11	DB 7 (MSB)
2	$\overline{RD}$ (READ STROBE)	12	DB 6
3	$\overline{WR}$ (WRITE STROBE)	13	DB 5
4	CLOCK IN	14	DB 4
5	$\overline{INTERRUPT}$	15	DB 3
6	+ ANALOG IN	16	DB 2
7	− ANALOG IN	17	DB 1
8	ANALOG GROUND	18	DB 0 (LSB)
9	SPAN ADJUST	19	CLOCK RETURN
10	DIGITAL GROUND	20	+ V SUPPLY

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage	+6.5V
Digital Input Voltage	−0.3V to +18V
Analog Input Voltage	−0.3V to (V_S +0.3V)
Package Dissipation	875 mW

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, +5V dc supply voltage, unless otherwise noted.

ANALOG INPUTS	
Analog Input Range[1]	−0.05V to +V_S +0.05V
Common Mode Voltage Range	Gnd to +V_S
Common Mode Rejection, dc, max.	±2.44 mV
Input Resistance, Span Adjust, min.	2.5 kΩ

DIGITAL INPUTS	
Input Logic Level, Vin ("1")[2]	+2.0V min. to +15V max.
Input Logic Level, Vin("0")[3]	+0.8V max.
Clock IN Threshold Voltage[4], Pos.	+2.7V min. to +3.5V max.
Neg.	+1.5V min. to +2.1V max.
Clock IN Hysteresis[4]	+0.6V min. to +2.0V max.
$\overline{CS}$ (Chip Select)	Active low state, enables the ADC-830 for read and write operations.
$\overline{WR}$ (Write Strobe)	Start conversion pulse. Input low of 100 nsec. min., in conjunction with a low on $\overline{CS}$, resets S.A.R. and shift register.
$\overline{RD}$ (Read Strobe)	Ouput enable pulse. Input low, in conjunction with a low on $\overline{CS}$, enables three-state outputs. Max. enable delay is 200 nsec.
Digital Input Capacitance, max.	7.5 pF

DIGITAL OUTPUTS	
Parallel Output Data	8 parallel lines of three-state, gateable output data.
$\overline{INT}$ (Interrupt)	Device status signal. Low when conversion complete. High when conversion in progress and when output data enabled.
Output Logic Level, Vout ("1")[5]	+2.4V min. at −360 μA
Vout ("0")[6]	+0.4V max. at 1.6 mA
Output Short Circuit Current, Gnd, min.	4.5 mA
Vs., min.	9.0 mA
Off-State Output Current	±3 μA
Digital Output Capacitance, max.	7.5 pF

PERFORMANCE	
Resolution	8 binary bits
Total Adjusted Error[7], max.	±½ LSB
Conversion Time[8]	100 μsec.
Conversion Rate[9], max.	8770 CPS
Clock Frequency Range[10]	100 kHz to 1.2 MHz
Output Enable Delay[11], max.	200 nsec.
Three-State Control Delay[12], max.	250 nsec.
Interrupt Output Delay, max.	450 nsec.
Power Supply Sensitivity[13]	±2.44 mV

POWER REQUIREMENTS	
Supply Voltage Range	+4.5V dc to +6.3V dc
Supply Current, max.	1.8 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Package Type	20 pin plastic DIP

FOOTNOTES

1. When − Analog IN (Pin 7) is ≥ + Analog IN (Pin 6), the digital output code will be 0000 0000. Two internal diodes are connected to each analog input which will forward conduct for input voltages one diode drop below ground or above V_S.
2. V_S = +5.25V dc, at V_S = +5V dc, high level input current = 1 μA maximum.
3. V_S = +4.75V dc, at V_S = +5V dc, low level input current = 1 μA maximum.
4. Clock IN (Pin 4) is the input of a Schmitt Trigger circuit.
5. V_S = +4.75V. For Vout ("1") = 4.5V high level output current = −10 μA.
6. V_S = +4.75V. Low level output current for the $\overline{Interrupt}$ Output is 1.0 mA.
7. Specified after full-scale adjustment.
8. With an asynchronous start pulse, up to 8 clock periods may be required before conversion starts.
9. Conversion rate in free-running mode; $\overline{INTR}$ (Pin 5) connected to $\overline{WR}$ (Pin 3), CS (Pin 1) = OV, and f_{clk} = 740 kHz.
10. V_S = +6V. Clock frequency range at V_S = +5V is 100 kHz to 800 kHz.
11. C_L = 100 pf, use bus driver for large C_L.
12. C_L = 10 pf, R_L = 10 KΩ.
13. V_S = +5V ±10% over full analog input range.

TECHNICAL NOTES

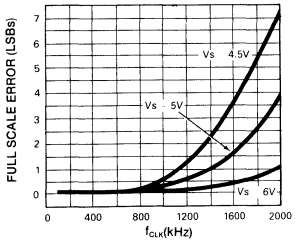
1. The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) are active low to allow easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (Pin 1) can be grounded and the standard A/D START function is obtained by an active low pulse on the $\overline{WR}$ input (Pin 3) and the Output ENABLE function is obtained by an active low pulse on the $\overline{RD}$ input (Pin 2).
2. The ADC-830 has a differential analog voltage input (Pins 6 & 7). The switching time between the inputs is 4.5 clock periods. The maximum error voltage due to this sampling delay is ΔV_e (maximum) = (V_P) ($2\pi f_{cm}$) ($4.5/f_{clk}$) where: ΔV_e is the error voltage due to sampling delay, V_P is the peak value of the common-mode voltage, and f_{cm} is the common-mode frequency. Because of this internal switching action, displacement currents will flow at the analog inputs. These current transients occur at the leading edge of the internal clock, rapidly decay, and do not cause errors as the comparator is strobed at the end of the clock period. However, if the voltage source applied to Ana. IN + (Pin 6) exceeds V_S by more than 50 mV, a large current may flow through a parasitic diode to V_S. If these currents could exceed 1 mA, an external diode should be connected between Ana. IN + (Pin 6) and V_S (Pin 20).
3. The leads to the analog inputs should be kept as short as possible to prevent noise pickup. The source resistance for these inputs should be kept below 5 kΩ. Input bypass capacitors should not be used as they will average the transient input switching currents of the converter causing scale errors.

4. The ADC-830 may be used with a 5V, 2.5V or adjusted voltage reference. The reference is either ½ the value of V_S or equal to a voltage applied to the span adjust pin (Pin 9). This allows for operation in either a ratiometric mode or an absolute mode. The internal gain for the span adjust input is 2.
5. The clock for the ADC-830 may be derived from the CPU or an external RC can be added to provide self clocking. A resistor ($\approx$10 kΩ) is connected between CLK Return (Pin 19) and CLOCK IN (Pin 4) and a capacitor is connected between CLOCK IN and ground. The resultant clock frequency is f_{clk} = 1/1.1 RC. Heavy capacitive or dc loading of the Clock Return pin should be avoided, a CMOS or low power TTL Buffer should be used to drive loads greater than 50 pF.
6. For continuous conversion operation, the $\overline{CS}$ input (Pin 1) is grounded and the $\overline{WR}$ input (Pin 3) is connected to the $\overline{INTR}$ output (Pin 5). $\overline{WR}$ and $\overline{INTR}$ should be momentarily forced low following a power-up cycle to guarantee operation.
7. The ADC-830 will require a bus driver when the total capacitance of the data bus gets large. For systems with a slow CPU clock frequency, higher capacitive loads may be driven. Low power Schottky or high current bipolar bus drivers with PNP inputs are recommended.
8. The use of good circuit board layout techniques is required for rated performance. Sockets on a PC board should be used, all logic signal leads should be grouped and kept as far as possible from the analog inputs, and the analog inputs should be shielded. A single point analog ground should be used that is separate from the digital ground. V_S should be bypassed, as close to the V_S pin as possible, with a low inductance 1 μF tantalum capacitor. The V_S bypass capacitor and self-clocking capacitor (if used) should be returned to digital ground.

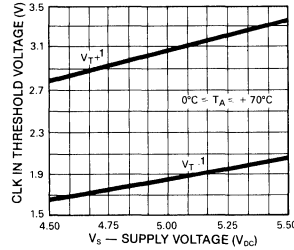
1

TYPICAL PERFORMANCE CHARACTERISTICS

FULL-SCALE ERROR VS f_{CLK}

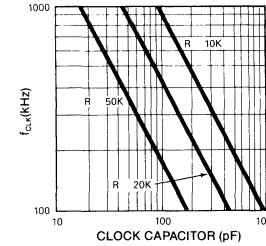


CLK IN SCHMITT TRIP LEVELS VS SUPPLY VOLTAGE

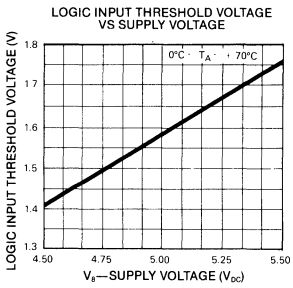


1. V_T = The positive or negative clock IN threshold voltage

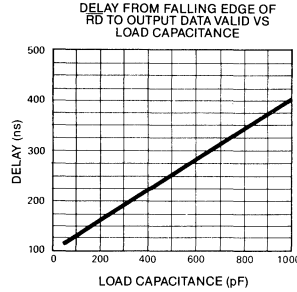
f_{CLK} VS CLOCK CAPACITOR



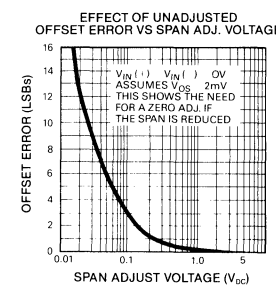
LOGIC INPUT THRESHOLD VOLTAGE VS SUPPLY VOLTAGE



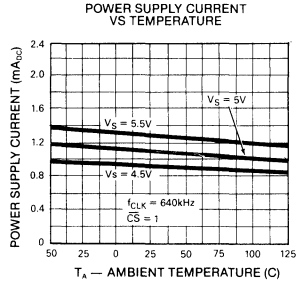
DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID VS LOAD CAPACITANCE



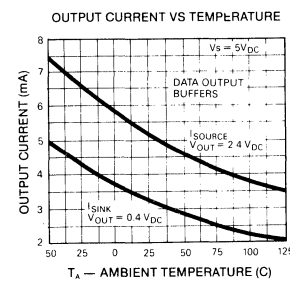
EFFECT OF UNADJUSTED OFFSET ERROR VS SPAN ADJ. VOLTAGE



POWER SUPPLY CURRENT VS TEMPERATURE

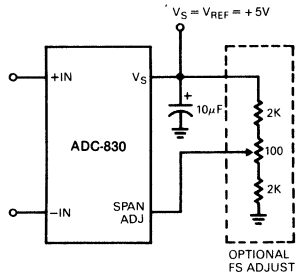


OUTPUT CURRENT VS TEMPERATURE

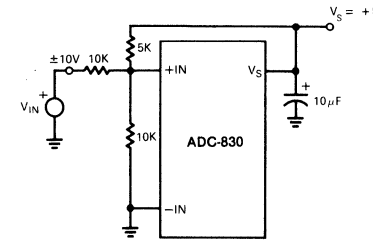


TYPICAL APPLICATIONS

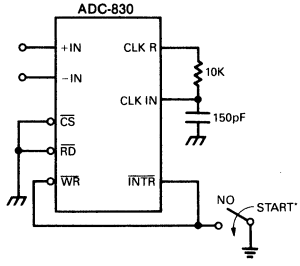
ABSOLUTE WITH A +5V REFERENCE



HANDLING ± 10V ANALOG INPUTS

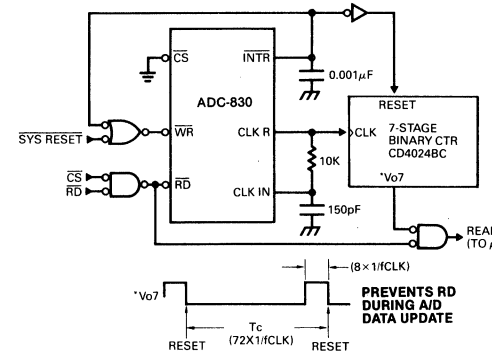


SELF—CLOCKING IN FREE-RUNNING MODE



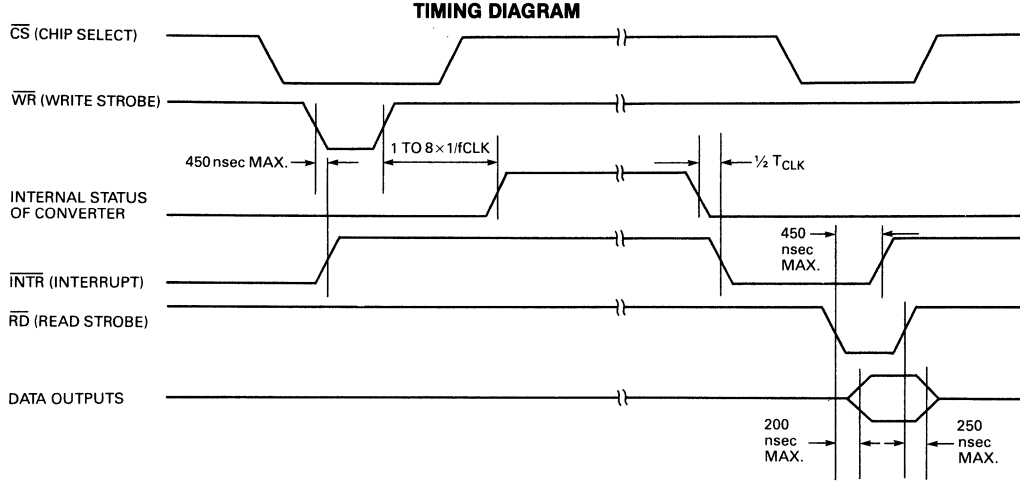
AFTER POWER-UP, A MOMENTARY GROUNDING OF THE $\overline{WR}$ INPUT IS NEEDED TO GUARANTEE OPERATION.

μP INTERFACE FOR FREE-RUNNING A/D



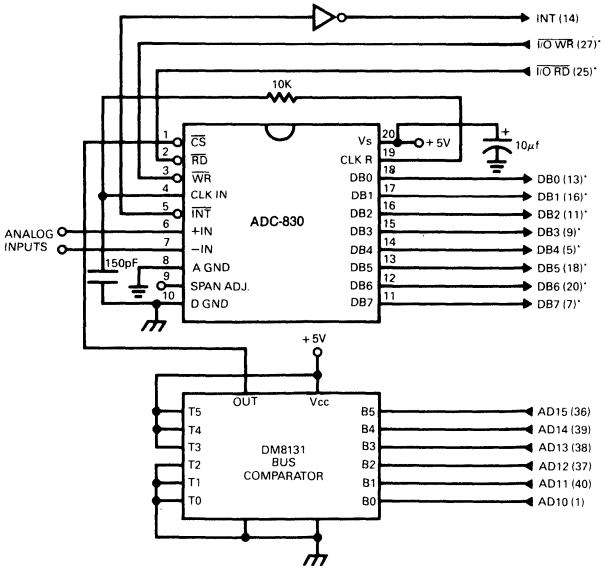
TIMING AND PERFORMANCE

TIMING DIAGRAM



MICROPROCESSOR INTERFACING

INS 8080A CPU INTERFACE

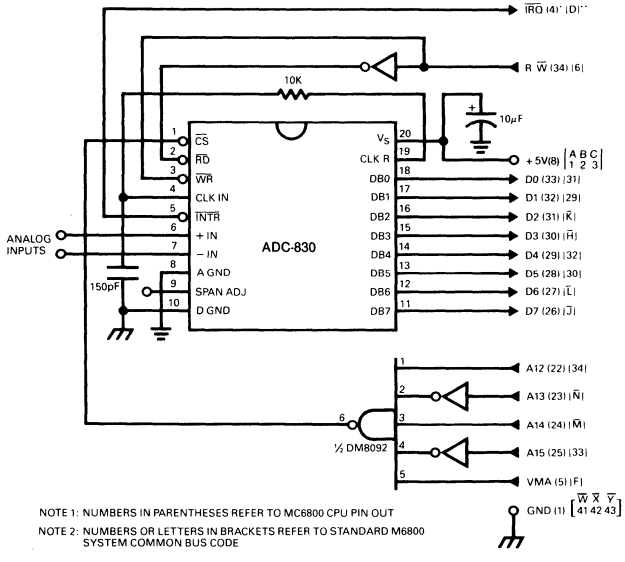


NOTE 1: *PIN NUMBERS FOR THE INS8228 SYSTEM CONTROLLER, OTHERS ARE INS8080A.

NOTE 2: PIN 23 OF THE INS8228 MUST BE TIED TO +12V THROUGH A 1KΩ RESISTOR TO GENERATE THE RST7 INSTRUCTION WHEN AN INTERRUPT IS ACKNOWLEDGED AS REQUIRED BY THE ACCOMPANYING SAMPLE PROGRAM.

The ADC-830 is designed to interface directly with derivatives of the 8080 µP. The converter can be mapped into memory space using standard memory address decoding, or it can be controlled as an I/O device by using the I/O R and I/O W strobes and decoding address bits A0 → A7 (or A8 → A15) to obtain the CS input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. In systems where the A/D converter is 1 of 8 or less I/O mapped devices, no address decoding circuitry is required. Each of the 8 address bits (A0 to A7) can be directly used as CS inputs, one for each I/O device.

MC 6800 CPU INTERFACE



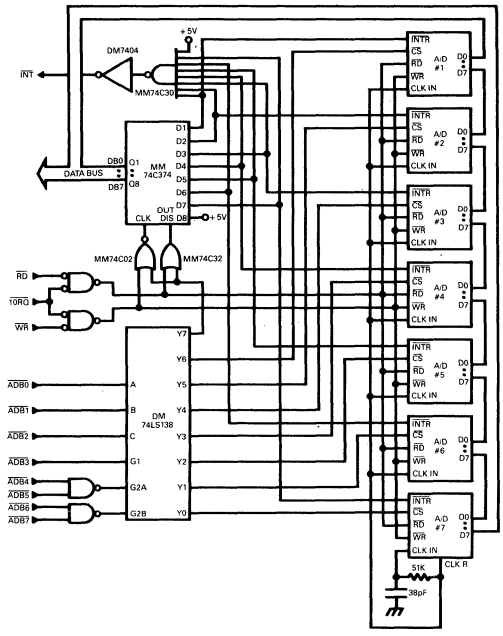
NOTE 1: NUMBERS IN PARENTHESES REFER TO MC6800 CPU PIN OUT

NOTE 2: NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD M6800 SYSTEM COMMON BUS CODE

The control bus for the 6800 µP derivatives does not use the RD and WR strobe signals. Instead it employs a single R/W line and additional timing, if needed, can be derived from the Ø2 clock. All I/O devices are memory mapped in the 6800 system and a special signal, VMA, indicates that the current address is valid. In many 6800 systems an already decoded 4/5 line is brought out to the common bus at pin 21. This can be tied directly to the ADC-830's CS pin if no other devices are addressed at Hex ADDR: 4XXX or 5XXX.

MICROPROCESSOR INTERFACING

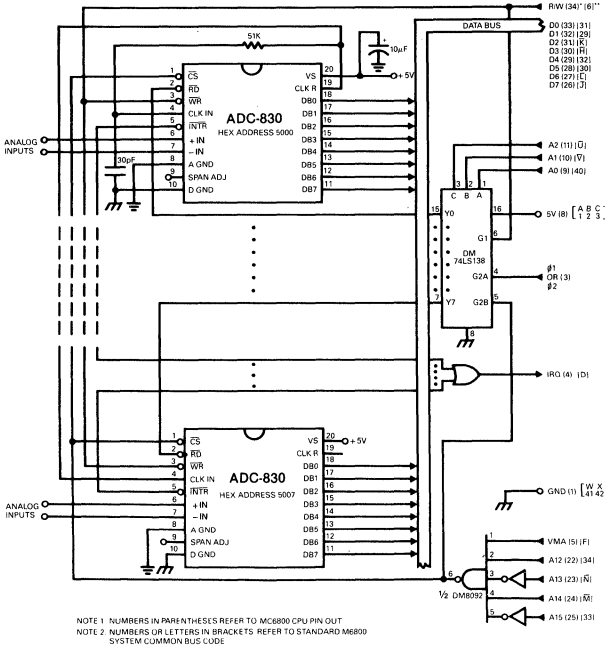
MULTIPLE ADC-830's IN A MC6800 SYSTEM



When transferring analog data from several channels to a single μP system, a multiple converter scheme presents several advantages over the conventional multiplexer single converter approach. With the ADC-830, the differential inputs allow individual span adjust for each channel. Also, the channels are sensed simultaneously, reducing the microprocessor's total system servicing time.

In the system shown, the ADC-830's have been arbitrarily located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. The system can easily be extended to allow the interfacing of more converters.

MULTIPLE ADC-830'S IN A Z-80 INTERRUPT DRIVE MODE



NOTE 1 NUMBERS IN PARENTHESES REFER TO MC6800 CPU PIN OUT
NOTE 2 NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD M6800 SYSTEM COMMON BUS CODE

In data acquisition systems where more than one peripheral device will be interrupting program execution of a microprocessor, the CPU must determine which device requires servicing. The circuit shown allows the ADC-830's to be started in any sequence, but will input and store valid data with a priority sequence of A/D #1 through A/D #7. Only the converters whose $\overline{INT}$ is asserted will be read.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
ADC-830C	0°C to +70°C

ACCESSORIES

Part Number	Description
TP100, TP10K	Trimming Potentiometers

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-847
Microprocessor-Compatible 8-Bit A/D Converter

FEATURES

- **Microprocessor compatible**
- **9 Microseconds conversion time**
- **8-Bit resolution**
- **± ¼ LSB linearity error**
- **Ratiometric operation**

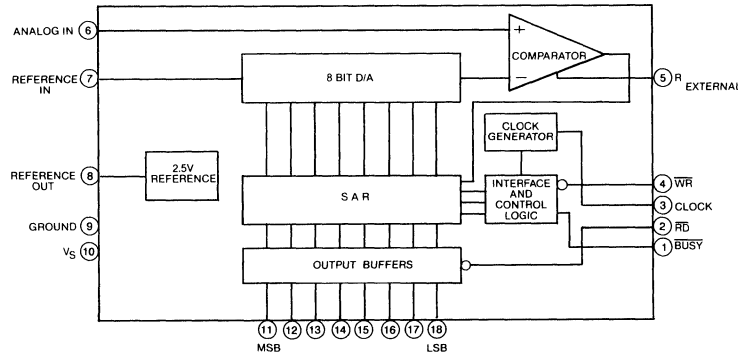
GENERAL DESCRIPTION

DATEL ADC-847 is a low cost, monolithic, 8-bit A/D converter designed to interface directly with a microprocessor via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus requires a minimum of interfacing logic. Using the successive approximation technique, the ADC-847 completes an 8-bit conversion in 9 microseconds with a maximum linearity error as low as ± ¼ LSB.

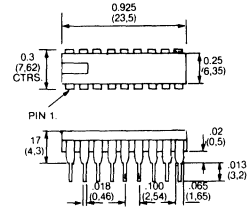
The data outputs of the ADC-847 are provided with three-state buffers to allow connection to a common data bus. The digital control lines; $\overline{WR}$, $\overline{RD}$ and $\overline{BUSY}$ are active low and are available in most microprocessor memory systems. The $\overline{BUSY}$ output uses a passive pull-up for CMOS/TTL compatibility which also allows up to four $\overline{BUSY}$ outputs to be connected together to form a common interrupt line. The ADC-847 will operate as a normal A/D converter for non-microprocessor applications.

Other important features include single supply operation capability, ratiometric operation, internal reference circuit and internal clock generator. The clock generator requires only an external capacitor or the device may be driven with an external clock. The reference circuit only requires an external resistor and capacitor or an external reference voltage can be connected to the reference input (Pin 7) if required. The ADC-847 is an ideal choice for many process control and instrumentation applications.

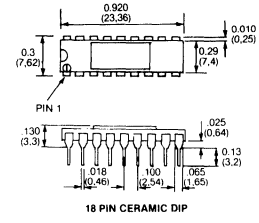
The ADC-847 is available for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges and is packaged in either an 18 pin plastic or ceramic DIP.



MECHANICAL DIMENSIONS INCHES (MM)



18 PIN PLASTIC DIP



18 PIN CERAMIC DIP

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	$\overline{BUSY}$ (STATUS)
2	$\overline{RD}$ (OUTPUT ENABLE)
3	CLOCK
4	$\overline{WR}$ (START CONVERSION)
5	EXTERNAL RESISTOR
6	ANALOG INPUT
7	REFERENCE INPUT
8	REFERENCE OUTPUT
9	GROUND
10	+ V SUPPLY
11	DB7 (MSB)
12	DB6
13	DB5
14	DB4
15	DB3
16	DB2
17	DB1
18	DBO (LSB)

ABSOLUTE MAXIMUM RATINGS, ALL MODELS	ADC-847A	ADC-847B	ADC-847M
Supply Voltage		+7.0V	
Digital Input Voltage		V_S	
Analog Input Voltage		V_S	

FUNCTIONAL SPECIFICATIONS, ALL MODELS

Typical at +25°C, +5V dc supply voltage, 900 kHz clock frequency, unless otherwise noted.

ANALOG INPUTS	ADC-847A	ADC-847B	ADC-847M
Analog Input Ranges		0 to +5V, 0 to +10V, ±5V, ±10V	
Input Resistance		100 kΩ	
Reference Input Range		+1V to +3V	
Input Current[1]		1 μA	
DIGITAL INPUTS			
Input Logic Level, Vin ("1"), minimum		2V	
Input Logic Level, Vin ("0"), maximum		0.8V	
Input Logic Level, Iin ("1")[2]		300 μA	
Input Logic Level, Iin ("0")[3]		±10 μA	
Clock Input Voltage (pin 3)			
high level, minimum		4.0V	
low level, maximum		0.8V	
Clock Input Current, high level, maximum		800 μA	
low level, maximum		−500 μA	
Clock Pulse Width, minimum		500 nsec.	
$\overline{WR}$ (Write)		Start conversion pulse. 200 nsec. minimum pulse width. Active low input.	
$\overline{RD}$ (Read)		Active low state enables 3-state outputs.	
Input Clamp Diode Voltage, maximum		−1.5V	
DIGITAL OUTPUTS			
Parallel Output Data		8 parallel lines of three-state, gateable output data.	
Output Coding, Unipolar		Binary	
Bipolar		Offset Binary	
$\overline{BUSY}$		Active low output. High when conversion complete. Low when conversion in progress.	
Output Logic Level, Vout ("1"), minimum		2.4V	
Vout ("0"), maximum		0.4V	
Output Logic Level, Iout ("1"), maximum		100 μA	
Iout ("0"), maximum		1.6 mA	
Off-state output leakage current, maximum		2 μA	
PERFORMANCE			
Resolution		8 binary bits	
Linearity Error, maximum	±1 LSB	±¼ LSB	±¼ LSB
Differential Linearity Error, maximum	±1 LSB	±½ LSB	±½ LSB
Conversion Time		9 μsec.	
Internal Clock Frequency, maximum		1 MHz	
External Clock Frequency, maximum		1 MHz	
Reference Output Voltage, maximum[4]	2.600V	2.570V	2.570V
Reference Slope Resistance, maximum		2 Ω	
Reference Voltage Tempco		50 ppm/°C	
Reference Current, maximum		15 mA	
minimum		4 mA	
Linearity Tempco		±3.0 ppm/°C	
Zero Tempco		±8.0 ppm/°C	
Full-Scale Tempco		±2.5 ppm/°C	
POWER REQUIREMENTS			
Supply Voltage Range		+4.5V dc to +5.5V dc	
Supply Current, maximum		40 mA	
Power Consumption		125 mW	

PHYSICAL/ENVIRONMENTAL			
Operating Temp. Range			
ADC-847 A	0°C to +70°C		
ADC-847 B	0°C to +70°C		
ADC-847 M	−55°C to +125°C		
Storage Temp. Range	−55°C to +125°C		
Package Type, 18-Pin DIP	Plastic	Plastic	Ceramic

FOOTNOTES:

1. Input voltage = +3V and Rext = 82 kΩ.
2. Input voltage = 2.4V, supply voltage = 5.5V. For $\overline{RD}$ input, Iin ("1") = −150 μA.
3. Input voltage = +0.4V, supply voltage = 5.5V. For $\overline{RD}$ input, Iin ("0") = −300 μA.
4. Rref = 390Ω, Cref = 4.7 μF.

TECHNICAL NOTES

1. The internal clock generator requires an external capacitor (100 pf for 1 MHz) connected between Pin 3 and ground. The oscillator frequency may be trimmed with an external trim resistor (2 KΩ maximum) connected in series with the capacitor. For optimum accuracy and stability of the oscillator frequency without trimming, the use of a crystal or ceramic resonator connected between Pins 3 and 9 is recommended.

   An external clock signal from a TTL or CMOS gate to Pin 3 may be used if the application requires.

2. A 390Ω reference resistor (Rref) should be connected between Pins 8 and 10. This will supply a nominal reference current of 6.4 mA. Also, a 4.7 μF stabilizing/decoupling capacitor (Cref) should be connected between Pins 8 and 9. For internal reference operation, Vref OUT (Pin 8) is connected to Vref IN (Pin 7).

3. An external reference may be used if required. Voltage should be in the range of +1.5 to +3.0 volts and may be connected to Vref IN. The slope of such a reference source should be less than 2.5 Ω/n, where n is the number of converters supplied.

4. A continuous conversion can be accomplished by inverting the $\overline{BUSY}$ and feeding it to the convert ($\overline{WR}$) input. To ensure reliable operation, an initial start pulse is required. This can be accomplished by using a NOR gate instead of an inverter and feeding it with a positive going pulse. The pulse can be derived from a simple R.C. network that gives a single pulse when power is applied.

5. For ratiometric operation, if the output from a transducer varies with its supply, then an external reference for the A/D should be derived from the same supply. The external reference can vary

from +1.5V to +3.0V. Operation with a reference voltage less than +1.5V is possible but reduced overdrive to the comparator will increase its delay and the conversion time will need to be increased.

6. The $\overline{WR}$ (start conversion pulse) can be completely asynchronous with respect to the clock, and will produce valid data between 7½ and 8½ clock pulses later depending on the timing of the clock and CONVERT signals.
7. Upon receiving a convert pulse, the A/D is reset. (The MSB is set to "1" all other bits are set to "0" and the $\overline{BUSY}$ output goes low.) The A/D will remain in this state until the convert pulse returns high. After the start conversion input goes high, the MSB decision will be made on the falling clock edge after a rising clock edge (See timing diagram). This will insure that the MSB is allowed to settle for at least half a clock period or 550 nanoseconds at maximum clock frequency.

   The START CONVERSION ($\overline{WR}$) input is not locked out during a conversion. Therefore, if pulsed low at any time, the conversion will restart.
8. The ADC-847 can be operated with a single supply. However, a negative supply voltage is required to supply the tail current of the comparator. Since this current is only 25 to 150 μA and does not have to be well stabilized, it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output. (See single supply operation.)

CALIBRATION PROCEDURE

For calibration procedure, unipolar and bipolar, apply continuous convert pulses to start conversion ($\overline{WR}$) input long enough to allow a complete conversion and monitor the digital outputs.

CALIBRATION

UNIPOLAR

Zero Adjust Apply 0.5 LSB to the analog input and adjust the ZERO ADJUST pot until the LSB (Bit 8) just flickers between 0 and 1 with all other bits at 0.

Gain Adjust Apply FS — 1.5 LSB to the analog input and adjust the GAIN ADJUST pot until the LSB (Bit 8) output just flickers between 0 and 1 with all other bits at 1.

COMPONENT VALUES					
INPUT RANGE	TP_1	TP_2	R_1	R_2	R_3
+5V	5k	1M	5.6k	8.2k	680k
+10V	10k	1M	11k	5.6k	680k

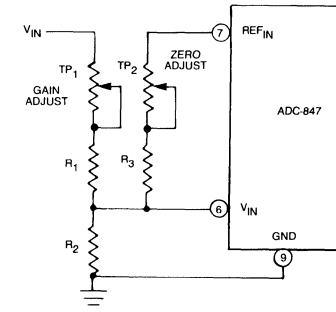
BIPOLAR

Offset Adjust Apply −(FS − 0.5 LSB) to the analog input and adjust the OFFSET ADJUST pot until the LSB (Bit 8) output just flickers between 0 and 1 with all other bits at 0.

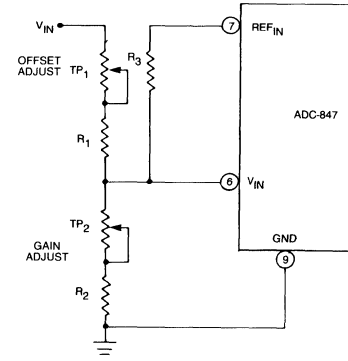
Gain Adjust Apply +(FS − 1.5 LSB) to the analog input and adjust the GAIN ADJUST pot until the LSB (Bit 8) just flickers between 0 and 1 with all other bits at 1.

After gain adjust, repeat offset adjust procedure.

COMPONENT VALUES					
INPUT RANGE	TP_1	TP_2	R_1	R_2	R_3
±5V	5k	5k	13k	13k	7.5k
±10V	10k	5k	27k	8.2k	8.2k



CONNECTION FOR UNIPOLAR OPERATION



CONNECTIONS FOR BIPOLAR OPERATION

CODING TABLES

UNIPOLAR

DIGITAL OUTPUT	ANALOG INPUT
11111111	FS-1 LSB
11000000	0.75 FS
10000000	0.5 FS
01000000	0.25 FS
00000000	0

$$1\ LSB = \frac{FS}{256}$$

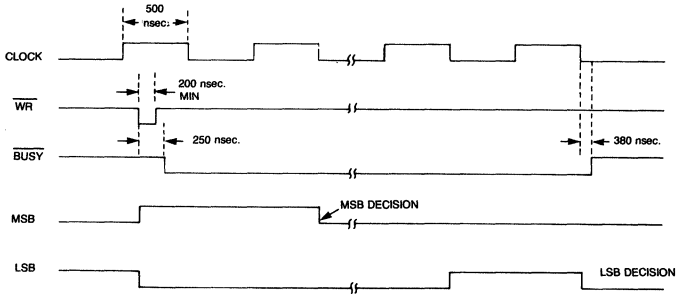
BIPOLAR

DIGITAL OUTPUT	ANALOG INPUT
11111111	+ (FS-1 LSB)
11000000	+ 0.5 FS
10000000	0
01000000	−0.5 FS

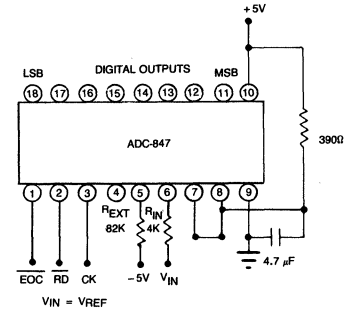
$$1\ LSB = \frac{2\ FS}{256}$$

TIMING AND CONNECTION

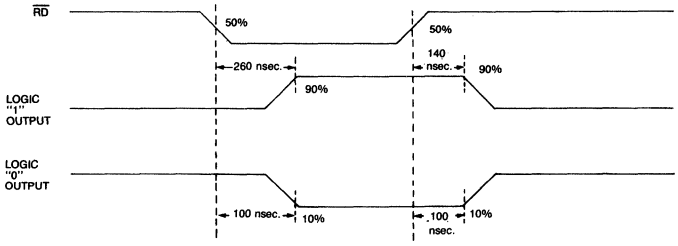
TIMING DIAGRAM



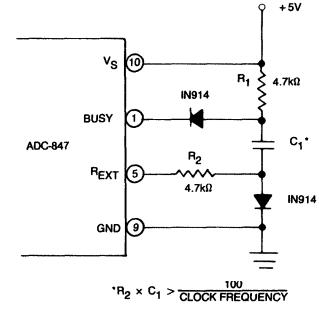
TYPICAL CONNECTION



OUTPUT ENABLE/DISABLE DELAYS

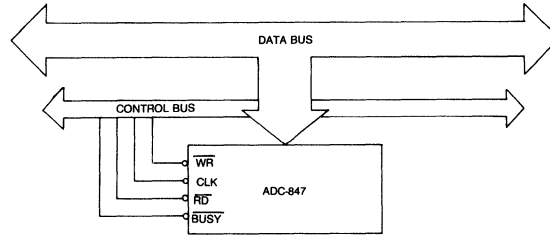


SINGLE SUPPLY OPERATION



DIODE PUMP CIRCUIT TO SUPPLY COMPARATOR TAIL CURRENT. SEE TECHNICAL NOTE 8.

TYPICAL CONNECTION TO MICROPROCESSOR DATABASE



The ADC-847 is primarily designed to interface directly to a microprocessor via three-state outputs. The device appears as a memory location or I/O peripheral to the microprocessor thus requiring a minimum of external interface logic.

ORDERING INFORMATION

MODEL NO.	LINEARITY ERROR	OPERATING TEMP. RANGE
ADC-847A	±1 LSB	0°C to +70°C
ADC-847B	±¼ LSB	0°C to +70°C
ADC-847M	±¼ LSB	−55°C to +125°C

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-856
Monolithic 10-Bit Tracking A/D Converter

FEATURES

- **Continuous tracking operation**
- **10^6 conversions/second**
- **10-Bit resolution**
- **Monotonic over temperature**
- **Controllable outputs**
- **TTL/CMOS compatible**

GENERAL DESCRIPTION

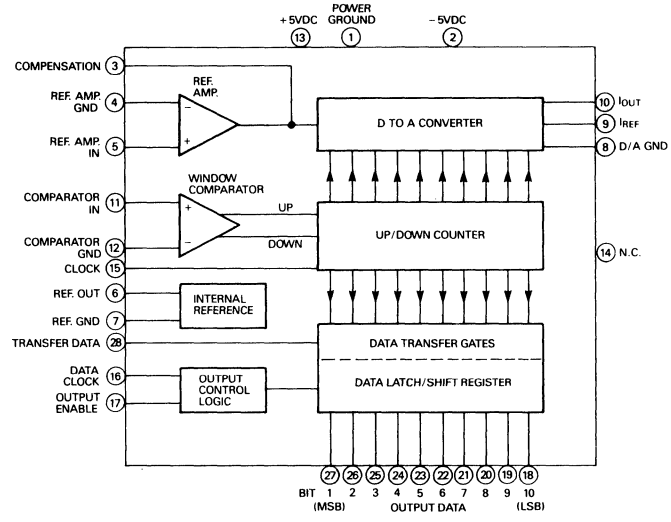
The ADC-856 is a 10-bit tracking A/D converter, capable of supplying continuously updated conversion data on full-scale sinusoidal signals up to 300 Hz without the need for a sample and hold. This converter is linear to ±½ LSB minimum and is monotonic over its operating temperature range. A number of innovative features give this device the flexibility for a wide range of applications.

The circuit is implemented in bipolar, monolithic form. The chip contains a fast window comparator, tracking logic, an up/down counter, a D/A converter, a precision voltage reference with amplifier, data transfer gates, and a data latch/shift register. The external parts required for operation have been held to a few passive components, and allow external programming of the analog input voltage range. Gain temperature coefficient of the circuit is ±10 ppm/°C, exclusive of reference.

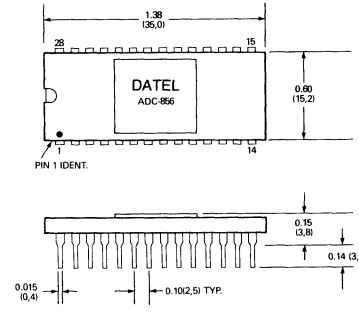
The ADC-856 is optimized for operation in a continuous tracking mode. In this conversion technique each conversion of an analog signal is based on the last converted value of that signal. For signals that do not vary faster than the converter can track, or 1 LSB/microsecond, continuous tracking will provide a valid, updated conversion result every microsecond.

Logic control inputs contribute to this device's usefulness in many different applications. The data transfer gates allow selection of the rate at which the output latch/shift register is updated. The rate may vary from once every microsecond to updating only upon receipt of a command from an external controller. External control also allows selection of output data form, which may be parallel or serial (by supplying an optional clock input). The outputs may be disabled completely in either mode by holding the output enable input low.

The ADC-856 operates on ±5V dc power at 50 mA with a power supply rejection of 0.1%/V. The device is packaged in a 28 ceramic DIP and is available in two operating temperature ranges: 0°C to +70°C and −55°C to +125°C.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER GROUND	15	CLOCK
2	−5VDC	16	DATA CLOCK
3	COMPENSATION	17	OUTPUT ENABLE
4	REF. AMP. GND.	18	BIT 10 OUT (LSB)
5	REF. AMP. IN	19	BIT 9 OUT
6	REF. OUT	20	BIT 8 OUT
7	REF. GND.	21	BIT 7 OUT
8	D/A GND.	22	BIT 6 OUT
9	I_{REF}	23	BIT 5 OUT
10	I_{OUT}	24	BIT 4 OUT
11	COMPARATOR IN	25	BIT 3 OUT
12	COMPARATOR GND.	26	BIT 2 OUT
13	+5VDC	27	BIT 1 OUT* (MSB)
14	N.C.	28	TRANSFER DATA

*Serial data output when in serial data mode

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage	±7 Volts
Logic Input Voltage	0V to +V_{CC}

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V Supply and Internal Reference, unless otherwise noted.

PERFORMANCE	
Resolution	10 Bits
Linearity Error	±½ LSB maximum
Differential Linearity Error	±½ LSB
No Missing Codes	Over Oper. Temp. Range
Conversion Time, 1 LSB change	1 μsec.
Conversion Time, Full Scale Change	1.024 msec.[1]
Tracking Speed	1 LSB/μsec. maximum
Tracking Bandwidth, Full Scale	300 Hz[2]
Gain Tempco	10 ppm/°C[4]
Zero Tempco	7 ppm/°C of FSR[6]
Power Supply Rejection	0.1%/V

INPUTS	
Analog Input Range[7], Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V
Reference Current	1 mA ±0.2 mA
Input Logic Level, high ("1")	+2.0V minimum at 50 μA[3]
Input Logic Level, low ("0")	+0.8V maximum at 1 μA[3]
Clock Pulse Width	100 nsec. minimum
Clock Rate	1 MHz maximum
Data Transfer Input	Hold high for 50 nsec. minimum to load output latches
Output Enable Input	When low, disables data clock and turns outputs off (high)
Data Clock Input	When driven by clock at ≤1 MHz with minimum pulse width of 100 nsec., provides serial data output at Pin 27.

OUTPUTS	
Reference Voltage	2.48V ±1.5%
Reference Tempco	40 ppm/°C
Reference Load Current, maximum	4 mA
D/A Output Current, Full Scale	4 mA[5]
Data Output	Parallel or Serial
Output Logic Level, high ("1")	+2.4V minimum at −40 μA
Output Logic Level, low ("0")	+0.4V maximum at 1.6 mA
Coding, Unipolar	Straight Binary
Coding, Bipolar	Offset Binary

POWER REQUIREMENTS	
Supply Voltage Range	±4.5V to ±5.5V
Supply Current	50 mA
Power Consumption	500 mW
Operating Temperature Range	
ADC-856C	0°C to +70°C
ADC-856M	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Package	28 Pin Ceramic DIP

FOOTNOTES:

1. Conversion time is directly dependent on the magnitude of input signal change.
2. Tracking bandwidth is inversely proportional to input signal amplitude, e.g. bandwidth is 600 Hz at half scale.
3. V_S = ±5.5V
4. Exclusive of Reference.
5. The full scale D/A output current is 4 times I_{REF}.
6. FSR is the Full Scale Range, the difference between maximum and minimum inputs.
7. Analog input range is programmed by an external resistor.

TECHNICAL NOTES

1. The transfer of conversion data to the outputs is controlled by the transfer gates. When TRANSFER DATA is held high the outputs update with each conversion. To update the outputs upon command. TRANSFER DATA is taken high for a minimum of 50 nanoseconds, no sooner than 150 nanoseconds after the active (negative going) edge of the main clock. TRANSFER DATA must go low before the next main clock edge. When TRANSFER DATA is low, the data is held in the output register.
2. Conversion data appears at the outputs in parallel form. Data may be obtained in serial form by clocking DATA CLOCK at up to 1 MHz, with a minimum pulse width of 100 nanoseconds and TRANSFER DATA low. Serial output data (MSB first) is then available at pin 27.
3. When OUTPUT ENABLE is taken low DATA CLOCK is disabled and all output transistors are turned off (all bit outputs go high).
4. The converter tracks the input signal level at a speed of 1 LSB/microsecond; thus the conversion time for any input signal change is given by

$$\frac{\Delta V_{IN}}{1\ LSB} = \text{conversion time in microseconds.}$$

5. Full Scale D/A output current is four times the reference current; for optimum performance the reference current should be 1 mA. An external reference can be used which can range from 0.8 mA to 1.2 mA.
6. The tracking bandwidth is inversely proportional to the amplitude of the input signal, e.g., at half scale the bandwidth is 600 Hz.
7. The window comparator and tracking logic determine whether the up/down counter will count up/count down or retain the same value on the negative going edge of the clock pulse.
8. Since the gain tempco of the converter is typically 10 ppm/°C, it is recommended that 10 ppm/°C metal film resistors be used for R_3, R_4 and R_5 for best performance over temperature. The internal reference will typically add 40 ppm/°C to the gain tempco. For improved performance a high quality external reference should be used.
9. R_1 and R_2 compensate for the input bias currents of the reference amplifier and comparator whose inputs are at virtual ground. Thus $R_1 = R_3$ and R_2 = the parallel combination of R_4, R_5 and R_6. The parallel combination of R_4, R_5 and R_6 should be as close to 625Ω as possible as this determines the D/A setting time and therefore the conversion time. Refer to the resistor tables for a list of typical values for these resistors.

THEORY OF OPERATION

The ADC-856 converters employ a tracking conversion technique. Tracking converters are most effectively used in single-channel operations on a continuous signal. In this technique each conversion is based on the previous conversion value. A fast window comparator determines whether an up/down counter increments by 1 LSB, decrements by 1 LSB or remains at its last value. The digital word in the counter controls a D/A converter with a precision reference; the analog output goes to the comparator and is compared with the analog input signal.

For signals with a rate of change less than the converter's maximum rate of change (tracking speed), each comparison represents a valid conversion and the converter is therefore tracking the signal. Tracking is not possible when the input signal varies at a rate greater than the converter's maximum or is discontinuous, as in multiplexed applications. In these cases the converter will change at its maximum rate (1 LSB/microsecond) until it attains the new signal level. While this acquisition is in progress, each converter step is available to the output as data, even though it does not yet represent the input signal level. The time required to acquire a new signal level is directly proportional to its difference from the previous level; for a full scale change this period is over 1 microsecond. Allowance should be made for the acquisition time when a rapid signal change is introduced.

UNIPOLAR OPERATION

Zero and Gain Adjustments

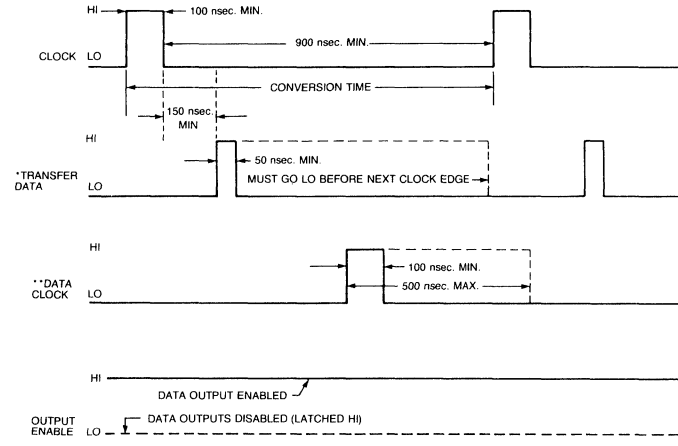
1. Apply an analog input voltage of zero + ½ LSB.
2. Adjust the zero adjustment so that the ouput code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of + F.S. – 1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

BIPOLAR OPERATION

Offset and Gain Adjustments

1. Apply an analog input voltage of – full-scale + ½ LSB.
2. Adjust the offset adjustment (R_4) so that the output code flickers between 000...000 and 000...001.
3. Apply an analog input voltage of + full-scale – 1½ LSB.
4. Adjust the gain adjustment (R_3) so that the output code flickers between 111...110 and 111...111.

TIMING DIAGRAM



*IF TRANSFER DATA IS HELD HI, THEN THE COUNTER OUTPUTS APPEAR DIRECTLY AT THE BIT OUTPUTS.
**DRIVEN FOR SERIAL DATA OUTPUT ONLY.

CODING TABLES

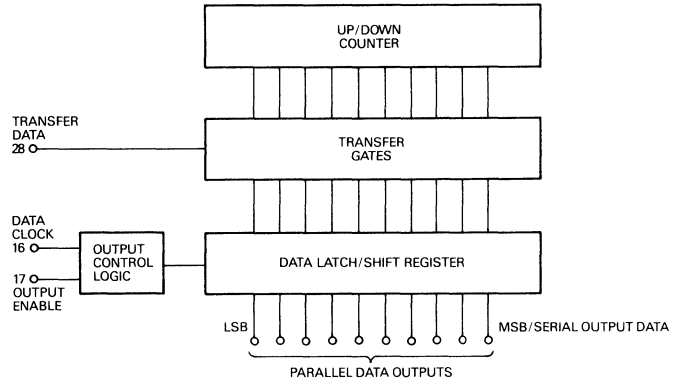
UNIPOLAR OPERATION STRAIGHT BINARY

SCALE	CODE
+ FS – 1 LSB	1111111111
+ ¾ FS	1100000000
+ ½ FS	1000000000
+ ¼ FS	0100000000
+ 1 LSB	0000000001
0	0000000000

BIPOLAR OPERATION OFFSET BINARY

SCALE	CODE
+ FS – 1 LSB	1111111111
+ ½ FS	1100000000
+ 1 LSB	1000000001
0	1000000000
– 1 LSB	0111111111
– ½ FS	0100000000
– FS + 1 LSB	0000000001
– FS	0000000000

OUTPUT LOGIC CONTROL



TRANSFER DATA (PIN 28)

HI: Min. 50 nsec pulse transfers parallel data from the up/down counter to the data latch/shift register. May be held high for continuous data transfer

LO: Data in latches held, new data from counter not transferred to data latches

DATA CLOCK (PIN 16)

HI: Clocked at up to 1 MHz for serial data output at Pin 27, MSB first

LO: Output data in parallel format at pins 18-27

OUTPUT ENABLE (PIN 17)

HI: Data available at outputs (parallel or serial)

LO: Output transistors turned OFF, all data outputs latched HI

CONNECTION AND CALIBRATION

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram. Note that Pin 6 is connected to R_3 and R_4 only when the internal reference is used (dotted line on diagram).
2. Select R_1 through R_6 from values given in the resistor table or calculate from the equations that accompany it.
3. Drive the MAIN CLOCK input (Pin 15) with a compatible clock signal at up to 1 MHz and apply a logic high to TRANSFER DATA (Pin 28).

CALIBRATION RESISTOR VALUES

R_4 adjusts the offset for bipolar operations; in unipolar operations R_4 is replaced with a zero adjustment circuit shown in applications. In either mode R_3 adjusts the gain. If the predicted values of these resistors do not supply the transition points expected, their values should be recalculated. Each may be trimmed with a 100 ppm/°C trimming pot used in series with the resistor. The trim pots should be constrained to approximately 1% of the nominal value calculated.

The values of R_1 through R_6 are calculated from the following:

*R_1 = R_3 *R_2 = the parallel combination of R_4, R_5 and R_6.

$$R_3 = \frac{V_{REF}}{1.0\ mA} \qquad R_4 = \frac{-V_{REF}R_5}{V_{IN}min}$$

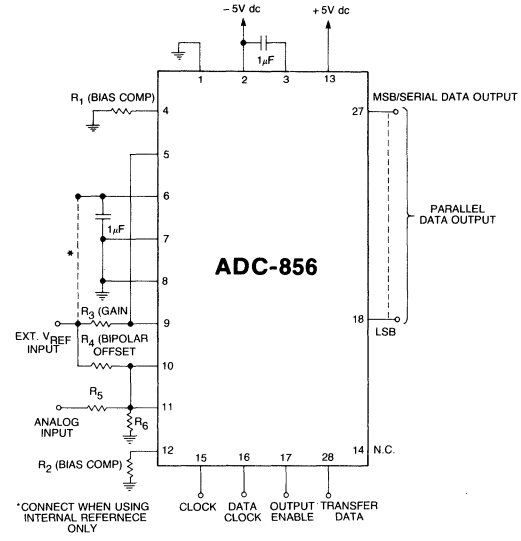
$$R_5 = \frac{FSR^{**}}{I_{OUT}(max)}$$

*R_6 is chosen so that the parallel combination of R_4, R_5 and R_6 is approximately 625Ω. This determines the D/A time constant and conversion time.

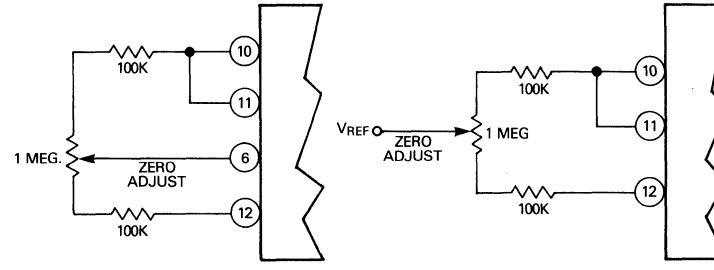
*The nearest preferred value may be used for these resistors.

**F.S.R. is the Full Scale Range, the difference between maximum input voltage and minimum input voltage.

CONNECTION AND CALIBRATION DIAGRAM



UNIPOLAR ZERO



FOR UNIPOLAR OPERATION WHERE R_4 APPROACHES ∞ AND A ZERO ADJUSTMENT IS REQUIRED, THIS CIRCUIT MAY BE USED TO REPLACE R_4.

RESISTOR TABLES

ANALOG INPUT RANGE	V_{REF}[2]	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
0 to +2.5V	2.5V	2.5K	625Ω	2.5K	∞	625Ω	∞
0 to +5.0V	2.5V	2.5K	625Ω	2.5K	∞	1.25K	1.25K
±2.5V	2.5V	2.5K	625Ω	2.5K	1.25K	1.25K	∞
0 to +10V	2.5V	2.5K	625Ω	2.5K	∞	2.5K	835Ω
±5V	2.5V	2.5K	625Ω	2.5K	1.25K	2.5K	2.5K
±10V	2.5V	2.5K	625Ω	2.5K	1.25K	5K	1.67K

NOTES: 1. The nearest preferred value may be used for R_1, R_2 and R_6.
2. For external reference set R_1 = V_{REF} (Kohms)

ORDERING INFORMATION

MODEL	OPER. TEMP. RANGE
ADC-856C	0°C to +70°C
ADC-856M	-55°C to +125°C

THESE CONVERTERS ARE COVERED BY GSA CONTRACT

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-868
Ultra High Speed, 12-Bit Modular A/D Converter

1

FEATURES

- **12-Bit resolution**
- **500 Nanoseconds (maximum) conversion time**
- **3-State output**
- **± ½ LSB linearity**
- **On board offset & gain adjustments**
- **No missing codes guaranteed**

GENERAL DESCRIPTION

DATEL's ADC-868 is an ultra high speed, 12-bit, modular A/D converter. Providing a maximum conversion time of 500 nanoseconds, this converter guarantees no missing codes over the 0°C to +70°C temperature range.

Standard input ranges are 0V to +5V for unipolar operation and ±2.5V for bipolar operation. Extended input ranges of 0V to +10V and ±5V can be implemented by the addition of 2 external resistors. A low input impedance of 1K allows for maximum speed applications with low impedance sources such as a sample and hold amplifier.

Output data is available through a 3-state output register, as 12 parallel lines with 2 enable inputs providing accurate data transferal. Data is coded as straight binary for unipolar operation and offset binary for bipolar operation.

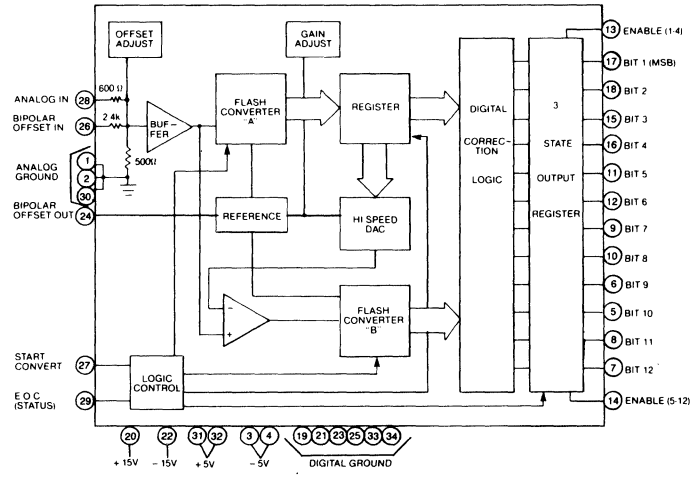
The ADC-868 is comprised of a fast settling precision input buffer, flash converter, high-speed DAC, high-speed comparator, precision voltage reference, clock generator and control logic circuits. Complete with on-board offset and gain adjustments, no external components are required.

Excellent specifications include a maximum gain tempco of 30 ppm/°C, and ± ½ LSB maximum differential nonlinearity.

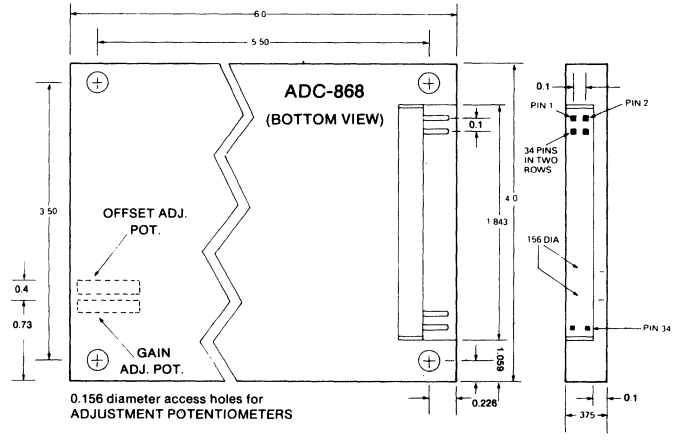
The combined use of a high-speed A/D with "state-of-the-art" flash conversion techniques, makes the ADC-868 an ideal selection for high speed data acquisition, real time waveform analysis, radar signal processing and analytic instrumentation.

This module is packaged in a 4 x 6 x 0.375 inch black enameled CR steel case with a 34 pin male connector located at one end.

Power requirements are ±15V dc and ±5V dc with a total current drain of 1070 mA, maximum.



MECHANICAL DIMENSIONS



0.156 diameter access holes for ADJUSTMENT POTENTIOMETERS

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	ANALOG GROUND
2	ANALOG GROUND
3	-5V dc
4	-5V dc
5	BIT 10
6	BIT 9
7	BIT 12 (LSB)
8	BIT 11
9	BIT 7
10	BIT 8

PIN	FUNCTION
11	BIT 5
12	BIT 6
13	ENABLE BITS 1-4
14	ENABLE BITS 5-12
15	BIT 3
16	BIT 4
17	BIT 1 (MSB)
18	BIT 2
19	DIGITAL GROUND

PIN	FUNCTION
20	+15V dc
21	DIGITAL GROUND
22	-15V dc
23	DIGITAL GROUND
24	BIPOLAR OFFSET OUT
25	DIGITAL GROUND
26	BIPOLAR OFFSET IN

PIN	FUNCTION
27	START CONVERT
28	ANALOG IN
29	E.O.C. (STATUS)
30	ANALOG GROUND
31	+5V dc
32	+5V dc
33	DIGITAL GROUND
34	DIGITAL GROUND

ABSOLUTE MAXIMUM RATINGS	
Positive Supply	+16V dc
Negative Supply	−16V dc
Logic Supply	±7V dc
Logic Inputs	+5.5V
Analog Inputs	±6.25V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ± 15V and ± 5V supplies, unless otherwise noted.

DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM
ANALOG INPUTS (See Technical Note #2 for extended input ranges.)			
Unipolar	—	0V to +5V	—
Bipolar	—	±2.5V	—
Impedance, Unipolar (with Pin 26 grounded)	—	1KΩ	1.01KΩ
DIGITAL INPUTS			
Start Conversion	A 2V (minimum to 5V (maximum) positive pulse with a 50 nsec. (minimum) duration. Positive going edge initiates conversion		
Loading	2 TTL Loads		
Enable	Logic low "0" enables bits 1 (MSB) thru 4		
Enable 5-12	Logic low "0" enables bits 5 thru 12 (LSB)		
Loading	1 TTL Load		
OUTPUTS			
Unipolar Coding	Straight Binary		
Bipolar Coding	Offset Binary		
Output Data	12 Parallel lines		
End of Conversion	2V (minimum) to 5V (maximum) positive going pulse, 500 nsec. (maximum) width. Negative going edge indicates conversion complete.		
Loading	10 TTL Loads		
Output Logic Levels (enable lines low)			
V_{out} "0"	—	+ 0.25V	+ 0.4V
V_{out} "1"	+ 2.4V	+ 3.1V	—
Loading	7 TTL Loads		
PERFORMANCE			
Resolution	—	—	12 bits
Conversion Time	—	450 nsec.	500 nsec.
Differential Linearity Error	—	± ¼ LSB	± ½ LSB
Integral Linearity Error	—	± ½ LSB	± 1 LSB
No Missing Codes	—	0°C to +70°C	
Gain Tempco	—	± 20 ppm/°C	± 30 ppm/°C
Zero Drift	—	± 15 ppm/°C	± 20 ppm/°C
Offset Tempco	—	± 10 ppm/°C	± 20 ppm/°C
Long Term Stability	—		± 0.25%/year
Output Enable Delay	—	20 nsec.	28 nsec.
POWER SUPPLY SENSITIVITY, %/% Supply			
±15V dc	—	—	±0.03
±5V dc	—	—	±0.01
POWER REQUIREMENTS			
Supply Voltage: Analog	± 14.5V dc	± 15V dc	± 15.5V dc
Logic	± 4.75V dc	± 5V dc	± 5.25V dc
Supply Current: ± 15V	—	150 mA	200 mA
- 15V	—	100 mA	120 mA
+ 5V	—	450 mA	500 mA
- 5V	—	225 mA	250 mA
Power Dissipation	—	7.1 watts	8.6 watts
PHYSICAL/ENVIRONMENTAL			
Operating Temperature	0°C to + 70°C		
Storage Temperature	-25°C to + 85°C		
M.T.B.F.	125,000 hrs.		
Package Type	4 x 6 x 0.375 inch black enameled 25 gauge CR steel, with a 34 pin male connector at one end.		

TECHNICAL NOTES

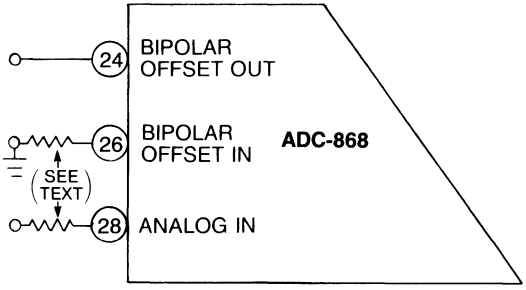
1. Configuration for unipolar or bipolar operation is as follows:
   Unipolar operation—ground pin 26 leaving pin 24 open.
   Bipolar operation—strap pin 24 to pin 26.
2. Analog input ranges may be extended to 0V to +10V unipolar and ±5V bipolar by the addition of two precision resistors. See Extended Input Configuration.
3. The high operating speed of these converters requires that good high frequency board layout techniques be used.

   Analog input leads should be as short and direct as possible. The use of shielded cable as an analog input lead will ensure isolation of analog signals from environmental interference and digital crosstalk.
4. Applications of these converters that require the use of a sample-hold may be satisfied by DATEL's model SHM-4860, a high-speed hybrid unit featuring 200 nanoseconds acquisition time to 0.01% accuracy. See Sample-Hold Diagram.
5. These converters have a maximum power dissipation of 8.6W. The case-to-ambient thermal resistance for this package is approximately 40°C maximum.
6. For TTL operation, tie both enable inputs to digital ground.
7. Logic and analog supply lines are internally bypassed so that external bypass capacitors are not necessary.

EXTENDED INPUT CONFIGURATION

Unipolar

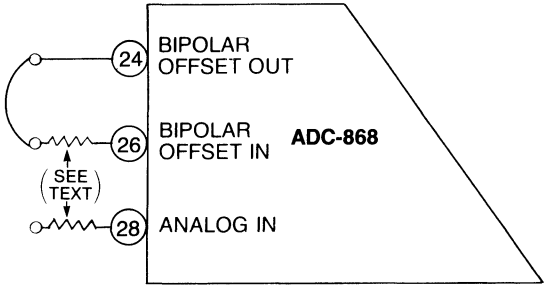
An extended unipolar input range of 0 to 10V can be achieved by the termination of the bipolar OFFSET IN (pin 26) to ground through a 1.02 kΩ, .1% resistor and connecting a 1.10 kΩ, .1% resistor in series with the ANALOG IN (pin 28).



Extended Input, Unipolar Configuration

Bipolar

An extended bipolar input range of ±5V can be attained by strapping the bipolar OFFSET OUT (pin 24) to the bipolar OFFSET in (pin 26) through a 1.02 kΩ, .1% resistor and connecting a 1.10 kΩ, 1% resistor in series with the ANALOG IN (pin 28).



Extended Input, Bipolar Configuration

GAIN AND OFFSET ADJUSTMENTS

Unipolar Operation

For extended input range operation, see Extended Input Configuration.

1. Apply start convert pulses to pin 27. (Pin 26 grounded)
2. Connect a precision voltage reference of +½ LSB (+0.61 mV or +1.22 mV for extended input range operation) to the analog input. Adjust the offset potentiometer so that the LSB is flickering at 0000 0000 000X.
3. Connect a precision voltage reference of +full-scale −1½ LSB (+4.9982V or +6.34V for extended range input operation) to the analog input. Adjust the gain potentiometer so that the LSB is flickering at 1111 1111 111X.

Bipolar Operation

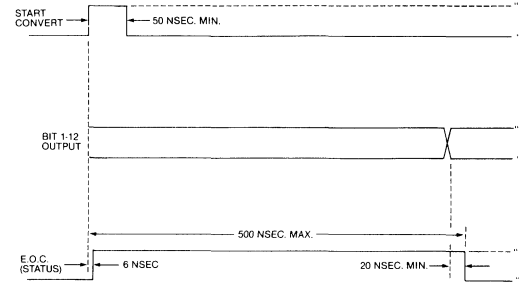
For extended input range operation, see Extended Input Configuration.

1. Apply START CONVERT PULSES to Pin 27. (Pin 26 connected to Pin 24.)
2. Connect a precision voltage reference of −full-scale +½ LSB (−2.4994V or −4.9988V for extended input range operation) to the analog input. Adjust the offset potentiometer so that the LSB is flickering at 0000 0000 000X.
3. Connect a precision voltage reference of +F.S. −1½ LSB (+2.4982V or +4.9963V for extended input range operation) to the analog input. Adjust the gain potentiometer so that the LSB is flickering at 1111 1111 111X.

OUTPUT CODING

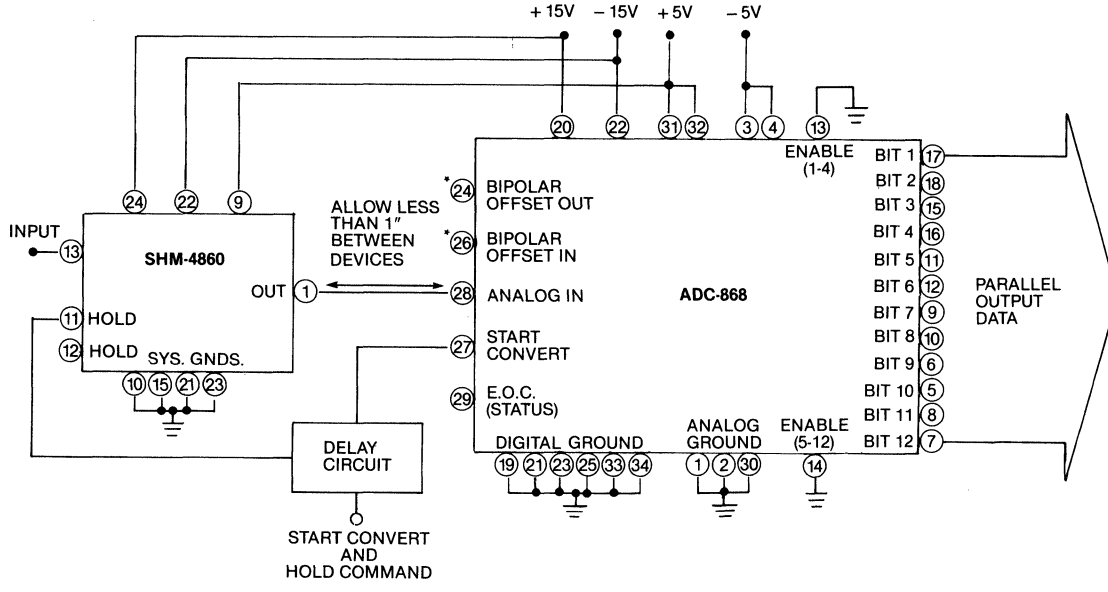
UNIPOLAR SCALE	10V RANGE	5V RANGE	STRAIGHT BINARY
+F.S. − 1 LSB	+9.9976V	+4.9988V	1111 1111 1111
+⅞ F.S.	+8.7500V	+4.3750V	1110 0000 0000
+¾ F.S.	+7.5000V	+3.7500V	1100 0000 0000
+½ F.S.	+5.0000V	+2.5000V	1000 0000 0000
+¼ F.S.	+2.5000V	+1.2500V	0100 0000 0000
+1 LSB	+0.0024V	+0.0012V	0000 0000 0001
0	0.0000V	0.0000V	0000 0000 0000

BIPOLAR SCALE	±5V RANGE	±2.5V RANGE	OFFSET BINARY
+F.S. − 1 LSB	+4.9976V	+2.4988V	1111 1111 1111
+¾ F.S.	+3.7500V	+1.8750V	1110 0000 0000
+½ F.S.	+2.5000V	+1.2500V	1100 0000 0000
0	0.0000V	0.0000V	1000 0000 0000
−½ F.S.	−2.5000V	−1.2500V	0100 0000 0000
−¾ F.S.	−3.7500V	−1.8750V	0010 0000 0000
−F.S. + 1 LSB	−4.9976V	−2.4988V	0000 0000 0001
−F.S.	−5.0000V	−2.5000V	0000 0000 0000



ADC-868 TIMING DIAGRAM

ULTRA HIGH SPEED A/D WITH SAMPLE/HOLD



When DATEL's ultra-high speed ADC-868 is used in conjunction with a high speed sample-hold amplifier, such as DATEL's SHM-4860, a throughput rate of 1.25 MHz can be achieved.

*See Technical Notes for configuration.

ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-868	500 nanoseconds, 12-bit A/D Converter
Mating Connector	34-Pin AMP #1-86063-3

ADC-881
Ultra-Linear, 8-Bit A/D Converter

FEATURES

- **8-Bit resolution**
- **Statistically linearized conversion**
- **14-Bit linearity**
- **±5V dc Input range**
- **1.5 Microseconds conversion time**
- **Out-of-range indication**

GENERAL DESCRIPTION

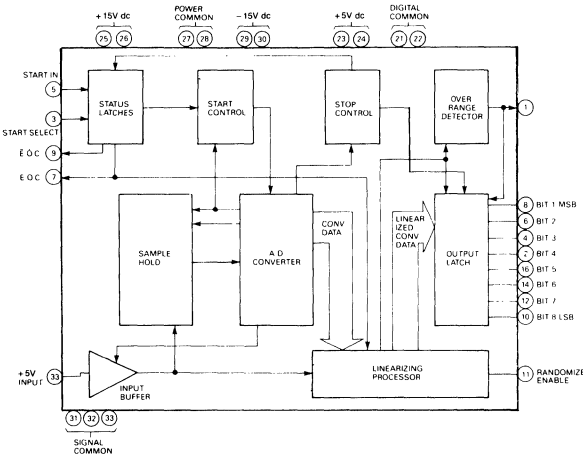
The ADC-881 is an 8-bit analog-to-digital converter with an internal sample-hold. This converter employs a stochastic distributional technique to enhance the statistical (average) linearity by a factor of 11.2, thus achieving a linearity error of only 0.005%. Systematic nonlinearities are scattered in a pseudorandom fashion over the range of the converter, thus appearing as noise rather than nonlinearities. This result is particularly desirable in applications that use the digital output of an A/D converter to compile a histogram. The fundamental properties of any non-distributive A/D converter cause class widths within the histogram to vary from the ideal, thereby artificially increasing or decreasing the frequency within discrete class widths.

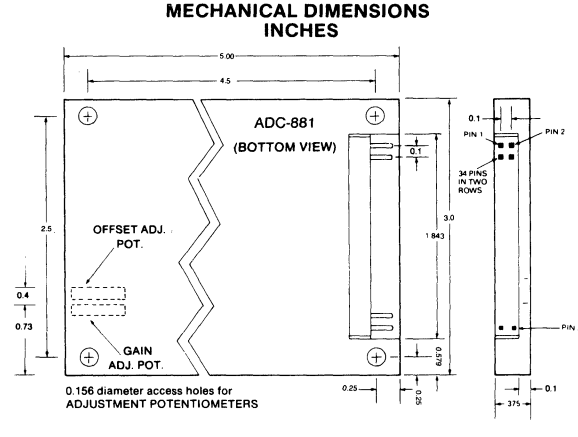
The ultra-linear A/D has a wide range of applications in spectrum analysis, nuclear research, vibration analysis, geological research, sonar digitizing, medical imaging systems, industrial testing and other signal analysis applications.

The ADC-881 has an analog input range of ±5V dc and will accomplish an eight-bit sample and conversion in 1.5 microseconds maximum. Output data is coded as offset binary with an over range output to indicate analog values out of the converter's range.

Additional specifications include a gain tempco of 25 ppm/°C maximum, offset tempco of 25 ppm/°C maximum, zero crossing tempco of 8 ppm/°C maximum and long term stability of ±0.02%/year.

Each converter is a functionally complete unit requiring only ±15V dc and +5V power supplies for operation. The device is packaged in a compact 5″ x 3″ x 0.375″ black enameled steel module. For information on extended temperature range versions contact the factory.





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OVER RANGE
2	BIT 4
3	START SELECT
4	BIT 3
5	START in
6	BIT 2
7	EOC
8	BIT 1 (MSB)
9	EOC
10	BIT 8 (LSB)
11	Random, Enable
12	BIT 7
13	NC
14	BIT 6
15	NC
16	BIT 5
17	Do Not Connect
18	Do Not Connect
19	Do Not Connect
20	Do Not Connect
21	Digital Common
22	Digital Common
23	+5V dc
24	+5V dc
25	+15V dc
26	15V dc
27	Power Common
28	Power Common
29	– 15V dc
30	– 15V dc
31	Signal Common
32	Signal Common
33	Analog Input
34	Signal Common

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS

Analog Input Range ..... ±5V
Analog Input Impedance ..... 14 kΩ
Start Conversion ..... A pulse[1] 20 nsec. to 80 nsec. duration with rise and fall times less than 10 nsec. Logic "0" = 0V to +0.8V. Logic "1" +2.0 to +5.5V. Conversion commences on the leading edge of the pulse. Loading: 1 LSTTL load.
Start Select ..... For positive start input pulses, set Start Select to a Logic "1". For negative start input pulses, set Start Select to a Logic "0" or ground.
Randomizer Reset ..... Hold at logical high for randomizing operations after reset[2]. Loading: 4 LSTTL loads.

OUTPUTS

Parallel Output Data ..... 8 parallel latched data lines -8 bits binary. V out "0" ≤ +0.4V, V out "1" ≥ +2.4V. Loading: 5 TTL loads
Coding ..... Offset Binary
$\overline{EOC}$ ..... Conversion Status Signal; High (V out "1" ≥2.4V) from 32 nsec. typical after leading edge of Start Convert to 14 nsec. typical after all data outputs are valid. V out "0" ≤ +0.4V. Loading: 5 TTL loads.
EOC ..... Conversion Status Signal. Complement of EOC. Loading: 5 TTL loads
$\overline{Over\ Range}$[3] ..... Out of Range Signal. High (Vout "1" ≥ +2.4V) for all Signal Input values within ±5V, Low (V out "0" ≤ +0.4V for all Signal Input values beyond ±5V.

PERFORMANCE

Conversion time[4], max. ..... 1.5 μsec
Resolution ..... 8 Bits
Integral Linearity Error[4] ..... 0.005% of FSR
Differential Linearity Error[5] ..... 0.005% of FSR
Noise (RMS)[6] ..... 0.2% of FSR
Gain Error ..... Adjustable to zero
Offset Error ..... Adjustable to zero
Gain Tempco, max. ..... ±25 ppm of FSR/°C
Offset Tempco, max. ..... ±25 ppm of FSR/°C
Zero Crossing Tempco, max. .... ±8 ppm of FSR/°C
Long Term Stability ..... ±0.02% / year

POWER REQUIREMENTS

Analog Supply ..... +15V ±0.5V at 100 mA max.
−15V ±0.5V at 100 mA max.
Logic Supply ..... +5V ±0.25V at 300 mA max.
Power Dissipation, max. ..... 4.5 Watts.
Power Supply Rejection ..... ±0.002%/% supply

PHYSICAL/ENVIRONMENTAL

Operating Temperature Range
ADC-881 ..... 0°C to +70°C
ADC-881-EX ..... −25°C to +85°C
ADC-881-EXX-HS ..... −25°C to +85°C Hermetic Sealed Semiconductors
Storage Temperature Range ... −55°C to +125°C
Package Type ..... Black enameled 25 gauge CR steel. 5 x 3 x 0.375 in. (127 x 76 x 10 mm)
Weight ..... 6.5 ounces (184 grams)
Connector ..... 0.25" square pins, gold plated phosphor bronze. Mating connector—supplied—is similar to AMP #1-85930-1.

FOOTNOTES:

1. An alternate method for generating Start Input pulses is to drive the Start Input with a rising edge and the Start Select with a falling edge delayed 20 nanoseconds to 80 nanoseconds.
2. After power-up, pin 11 (RANDOMIZER ENABLE) must remain low for at least 25 nanoseconds to reset the pseudo-random signal generator and to clear other gating circuitry.
3. When the Signal Input is less than −5V, the Data Output lines are all "0". When the Signal Input is greater than +5V, the Data Output lines are all "1".
4. Conversion Time is measured from the leading edge of the Start Conversion input to the trailing edge of the $\overline{EOC}$ output.
5. The Linearity Error is the systematic error which remains after a sufficient number of samples have been averaged to suppress the noise.
6. The RMS noise value is reduced by the second root of the number of samples that have been averaged.

ABSOLUTE MAXIMUM RATINGS

Positive Supply ..... +18V dc
Negative Supply ..... +18V dc
Logic Supply ..... +7V dc
Digital Supply ..... +5.5V dc

THEORY OF OPERATION

The ADC-881 employs a statistically linearized conversion technique that yields unique advantages in many applications. This technique uses a fundamental property of all A/D converters, differential nonlinearity, in a pseudo-random distributional technique to yield a converter with an "ideal" transfer function. This technique scatters the effects of systematic nonlinearities over the full range of the A/D in pseudo-random (a random sequence of finite length) fashion. The average transfer function, taken over the full range of the pseudo-random sequence, has extremely good integral linearity and minimal differential non-linearity. The trade-off appears here as "noisy" codes, this is the result of distributing systemic nonlinearities over a wide range. Noise may be suppressed by repeated sampling of the data since the average value of true random noise is zero. The RMS noise value of the data is reduced by the second root of the number of samples less one that have been averaged.

Since this converter's extreme linearity is realized in an average transfer function, it follows that averaging a larger number of conversions will improve linearity. This is true, with maximal linearity resulting as an average of all values within the pseudo-random sequence (127 random values). Since the ADC-881 has conversion times of 1.2 microseconds typical and 1.5 microseconds maximum, this averaging procedure will require between 165 and 191 microseconds (127 conversions x conversion time). In applications where repeated sampling is employed to reduce noise, this converter yields optimal linearity when the number of samples averaged is an integral multiple of 127 (this is inherent in the stochastic distributional technique used).

OFFSET AND GAIN CALIBRATION PROCEDURE

1. Connect the A/D converter to external test circuitry shown in "Calibration Connection" diagram with no power applied.
2. Apply power to the A/D converter and test circuitry and allow them to reach operating temperature.
3. Observe the A/D output as a crossplot on the oscilloscope. Calibrate the axis gain for one cm per step and adjust the crossplot dither amplitude for 10 cm. Calibrate the Y axis for an easily read crossplot.
4. Apply a precision voltage reference set to −5V dc to the analog input (pin 33). Observe the crossplot as shown in Figure 1. The last step should be centered on the vertical grid line one cm to the left of center. Adjust the offset potentiometer as necessary to achieve this positioning.
5. Set the precision voltage reference to +5V dc. Observe the crossplot as shown in Figure 2. The last step should be centered on the vertical grid line two cm. to the right of center. Adjust the gain potentiometer as necessary to achieve this position.
6. Repeat steps 4 and 5 until no further adjustment is required. Repetition is necessary, as the offset and gain adjustments interact. The following technique will minimize the number of adjustments. After the initial adjustment outlined in steps 4 and 5, repeat step 4. At this point repeat step 5, overadjusting the gain potentiometer so that the error displayed maintains its initial magnitude but occurs in a direction opposite from its original one. For instance, if the crossplot is 1.5 cm to the left of its desired position, adjust the gain potentiometer so that the crossplot is 1.5 cm to the right of its desired position. Repeat steps 4 and 5; the crossplot should now show optimum position.

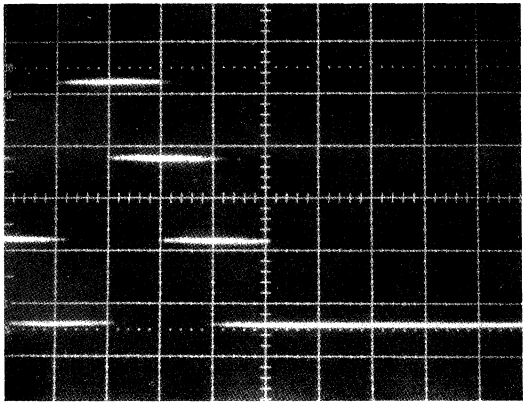


Figure 1. Negative Voltage Display

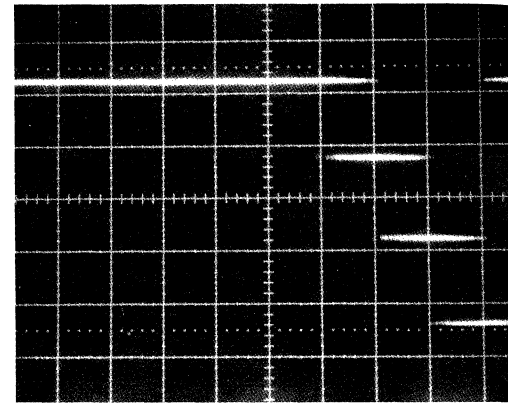
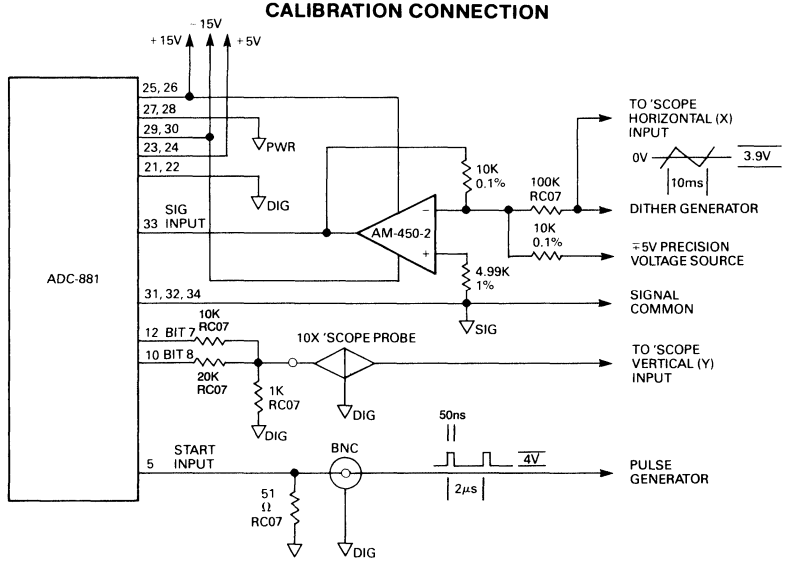


Figure 2. Positive Voltage Display

CALIBRATION CONNECTION



APPLICATION NOTE

The largest group of applications for this class of converters is in areas in which recurring systematic nonlinearities have an adverse effect on the distribution of acquired data values. This is particularly of interest in situations where data is required to compile a histogram (a frequency distribution of sample data into discrete categories). The effects of converter nonlinearities cause some categories to be artificially "widened" while others are "narrowed", thus increasing and decreasing, respectively, the frequence of occurrence of data values within these categories.

This effect causes a non-linearized converter to yield a "converter distorted" histogram. Until now many users had to resort to extensive computational processing of digitized data simply to minimize the effects of "converter distortion." The architecture of the ADC-881 obviates the need for this, allowing statistically valid processing of analog data in real-time. Thus we see that the ADC-881 is ideally suited for applications in spectrum analysis, particle event monitors, fast signal processing, vibration analysis, sonar digitizing, and a whole spectrum of imaging applications, from medical imaging to industrial nondestructive testing.

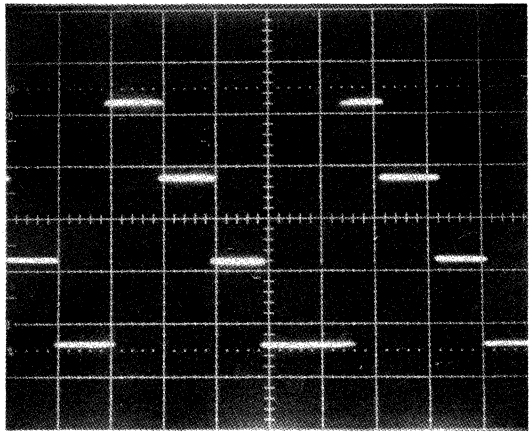


Figure 3. The output of a non-linearized 8 bit A/D converter is shown above. The display shows the 4 least significant bits at the major carry transition demonstrating differential nonlinearity. This is a property of all nonlinearized A/D converters. (The unit used for this example is a typical non-linearized A/D with ± ½ LSB of integral linearity and ± ½ LSB of differential nonlinearity).

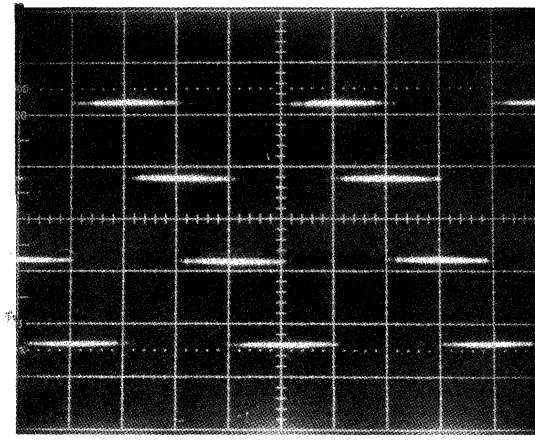


Figure 4. The output of a linearized 8 bit A/D shown for the 4 least significant bits at the major carry. Notice the improvement in differential nonlinearity. This photo shows the effect of averaging multiple conversions performed with the linearizing technique employed in the ADC-881.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-881	0°C to +70°C

For information on extended temperature range and high reliability versions of this product, contact factory.

THIS PRODUCT IS COVERED BY GSA CONTRACT.

ADC-974
High-Resolution, Ultra-Fast A/D

FEATURES

- **16 Bits of resolution**
- **2.5 μSec. conversion time**
- **14 Bits of linearity**
- **±5V Analog input range**
- **6″ x 4″ x 0.375″ module**

GENERAL DESCRIPTION

The ADC-974 is a 16-bit A/D converter with ±1/2 LSB linearity to 14 bits. This ultra-fast, high-resolution converter uses a two-pass, or sub-ranging, architecture to obtain conversion times of 2.5 microseconds.

The ADC-974 achieves this level of performance by implementing key functions using a number of high-performance hybrid components as part of a modular design.

The ADC-974 accepts analog inputs over a ±5V range and completes a full conversion in 2.5 microseconds maximum, including all set-up, settling and delay times. The device codes the conversion result as complementary two's complement, sending the result into the TTL-compatible output latches.

The ADC-974 features ±1/2 LSB maximum nonlinearity and +1/2 LSB maximum differential nonlinearity to 14 bits. Offset drift is only ±1 LSB at 14 bits over the rated operating temperature range and the reference output tempco is ±5 ppm/°C.

The converter measures 6″ x 4″ x 0.375″, housed in a black enameled steel module. A 34-pin AMP connector mounted at one end supplies all interconnect points without extending case size. Each module is functionally complete, requiring only ±15V dc and +5V supplies for operation, and has an operating temperature range of 0°C to +70°C.

Applications include analytical and automatic test equipment, imaging, seismic, communications, sonar, radar, and robotics.

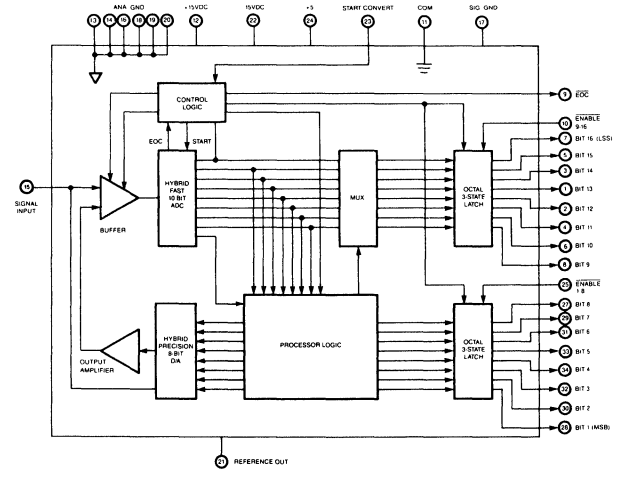


Figure 1. ADC-974 Simplified Block Diagram

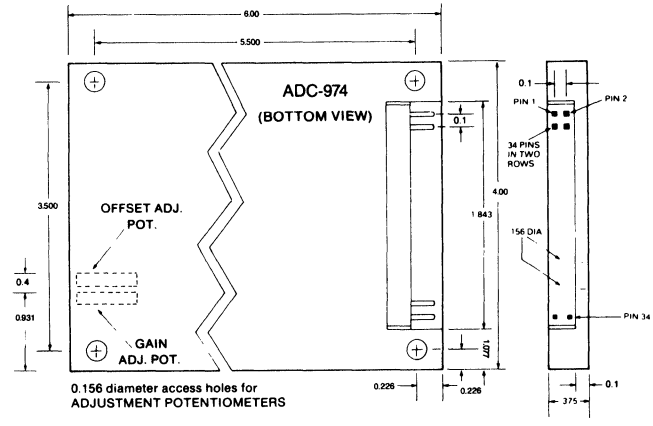


Figure 2. Mechanical Dimensions

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, ±15V dc and +5V dc supplies unless otherwise noted.)

INPUTS	
Analog Input Range	±5V
Input Impedance	1.25K, ±20%
Analog Input Step Loading[1]	+0.4 mA
Analog Input Source Step Load	
Recovery Required	≤30 nSec. to 0.1% ≤200 nSec. to 0.003%, for a ±0.4 mA step load
Common Mode Range	±10 mV
Common Mode Rejection Ratio	40 dB, Fo ≤10 MHz
Start Conversion	+2.0V min. to +5.5V max. positive pulse. 25 nSec. minimum duration if $\overline{EOC}$ is low when pulse is applied. 125 nSec. minimum duration if $\overline{EOC}$ is high when pulse is applied.
Loading	2 LSTTL loads
Enable Inputs[2]	TTL-compatible logic levels
Loading	1/4 LSTTL load for each input
OUTPUTS	
Parallel Output Data	16 parallel lines of data
Loading	20 LSTTL loads in enabled state, and ±50 μA max. in disabled state
Coding	Complementary 2's complement
EOC Output	TTL-compatible logic levels
Loading	9 LSTTL loads
Reference Output Voltage[3]	+10.00V, ± 0.01V
Reference Output Impedence	≤5.0 Ω, Fo ≤1 MHz
Reference Output Noise[4]	≤20 μV RMS
PERFORMANCE	
Conversion Time	2.5 μSec.
Resolution	16 Bits
Nonlinearity	±0.003% FSR max. (±1/2 LSB at 14 bits)
Tempco	±0.0061% FSR, 0°C to +70°C
Differential Nonlinearity	±0.003% FSR max. (±1/2 LSB at 14 bits)
Tempco	±0.0061% FSR, 0°C to +70°C
Relative Accuracy	±0.003% FSR max. (±1/2 LSB at 14 bits)
Tempco	±0.0061% FSR, 0°C to +70°C
Initial Offset Error	Adjustable to ≤0.00075% FSR
Offset Adjustment Range	0.075% FSR
Tempco, Max.	±0.0061% FSR, 0°C to +70°C
Stability	±10 ppm/1000 hrs.
PSRR, Max.	±1.5 mV/V
Initial Gain Error	Adjustable to ≤0.00075% FSR
Gain Adjustment Range	0.075% FSR
Tempco, Max.	±0.0061% FSR, 0°C to +70°C
Stability	±25 ppm/1000 hrs.
PSRR, Max.	±1.5 mV/V
Reference Output Tempco	±5 ppm/°C, 0°C to +70°C
POWER REQUIREMENTS	
Supply voltage[5]	+15V, ± 0.5V at 187 mA max. −15V, ± 0.5V at 187 mA max. +5V, ± 0.5V at 472 mA max.
Power dissipation, Max.	8.0 Watts
PHYSICAL ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Package Type	Black enameled 25 guage CR steel. 6″ × 4″ × 0.375″ (153 × 102 × 10 mm)
Weight	6.5 oz. (184 grams)
Connector	34-Pin AMP # 1-86063-3 at one end of case (mating connector supplied)

SPECIFICATIONS NOTES:

1. At 14.7 MHz during first 1000 nSec. of the conversion cycle.
2. For two-state operation, tie both enable inputs to digital common.
3. For 0 mA ≤ Vref ≤ 5 mA.
4. Bandwidth = 10 MHz.
5. The internal reference heater draws 14 mA from the ±15V at +25°C, decreasing at 2.5 mA/°C and dropping to zero +70°C. At turn-on, an inrush of 130 mA to the heater decays to 15 mA in less than 10 seconds.

TECHNICAL NOTES

1. $\overline{EOC}$ may be high or low on power-up. The first conversion needs a 125 nSec. minimum start convert pulse if $\overline{EOC}$ is high. The first conversion should be ignored if continuous 25 nSec. start convert pulses are used. The $\overline{EOC}$ falls 15 nSec. maximum after the new data has been strobed into the data output storage registers. Typically, it takes 3 nSec. before data is available at the outputs after $\overline{EOC}$ goes low. Refer to Figure 3.

2. There are two enable inputs, one for bits 1 through 8 and one for bits 9 through 16. These inputs control the state of the three-state data output registers to allow for 8- or 16-bit data bussing.

3. The bottom of the case has four 4-40 threaded holes. DATEL recommends securing the case to a .032 glass epoxy board or equivalent to reduce the case temperature resulting from internal power dissipation. Attain good thermal contact between the case bottom and the circuit board by using a silicone thermal joint compound such as Wakefield type 120 or equivalent.

Table 1. Input/Output Connections

PIN	FUNCTION
1	Bit 13
2	Bit 12
3	Bit 14
4	Bit 11
5	Bit 15
6	Bit 10
7	Bit 16 (LSB)
8	Bit 9
9	$\overline{EOC}$
10	$\overline{Enable\ 9\text{-}16}$
11	Digital GND
12	+15V
13	Analog GND
14	Analog GND
15	Signal Input
16	Analog GND
17	Signal GND
18	Analog GND
19	Analog GND
20	Analog GND
21	Reference Output
22	−15V
23	Start Convert
24	+5V
25	$\overline{Enable\ 1\text{-}8}$
26	Do not connect
27	Bit 8
28	Bit 1
29	Bit 7
30	Bit 2
31	Bit 6
32	Bit 3
33	Bit 5
34	Bit 4

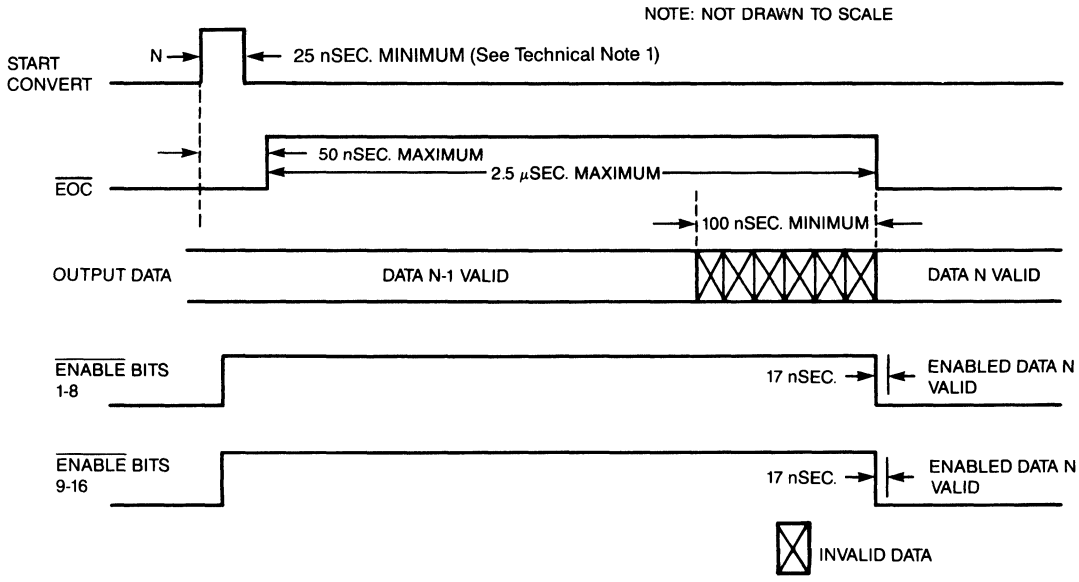


Figure 3. ADC-974 Timing Diagram

Offset and Gain Adjustments

Offset and gain error are calibrated at the factory prior to shipment. The ADC-974 has offset and gain error adjustment potentiometers should adjustment be required.

The circuit in Figure 4 shows how an ADC-974 would connect to a low-noise, wide-bandwidth buffer amplifier such as DATEL's AM-453.

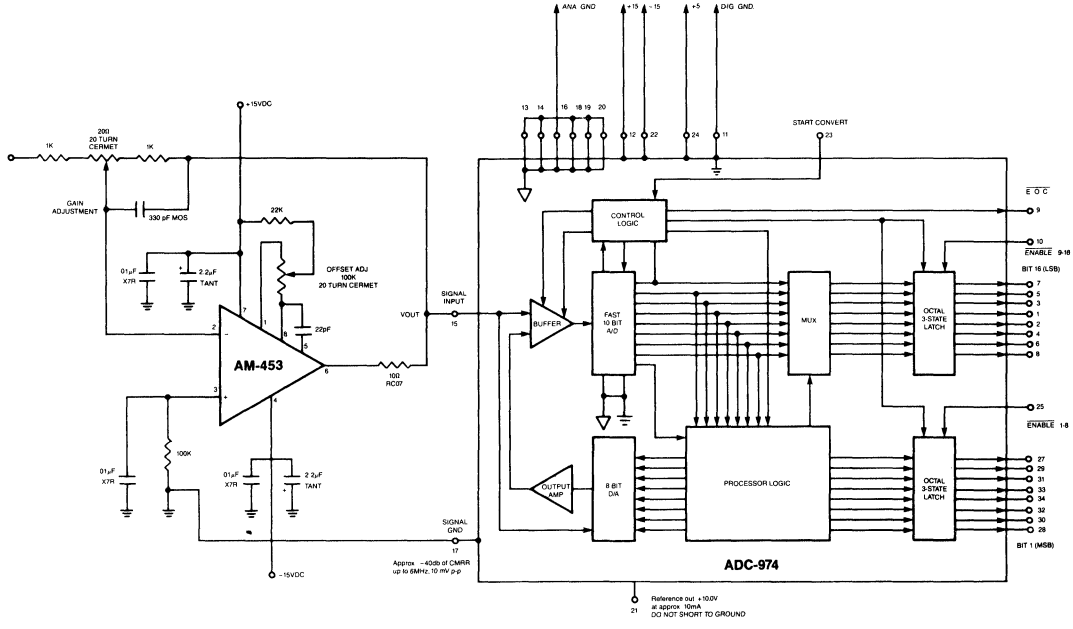


Figure 4. Typical Connection Drawing

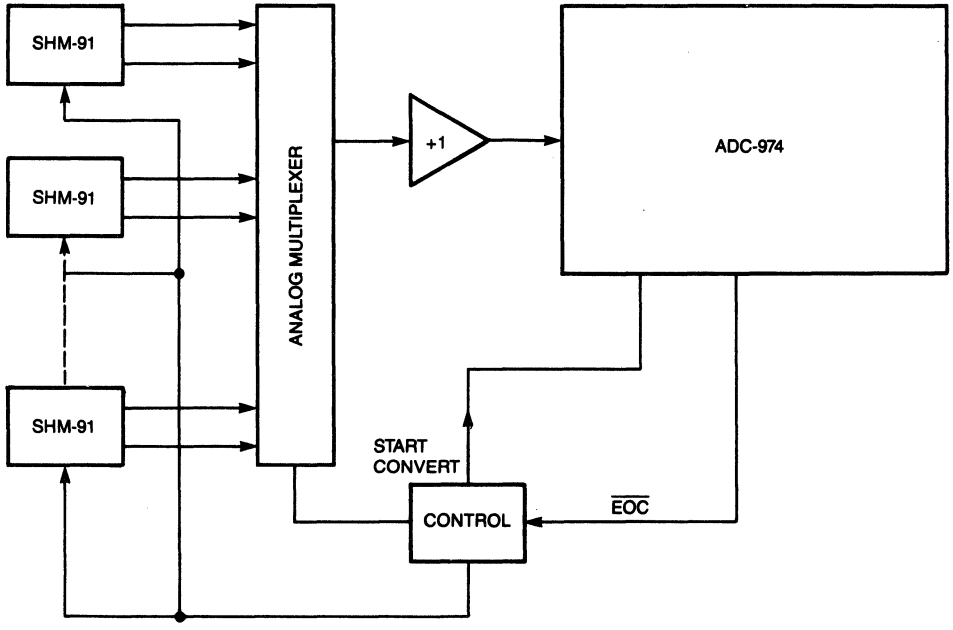


Figure 5. A/D Application with Simultaneous Sample-and-Hold

In the application depicted in Figure 5, the input circuitry shown samples all analog inputs at the same time, holding the samples for conversion by the ADC-974.

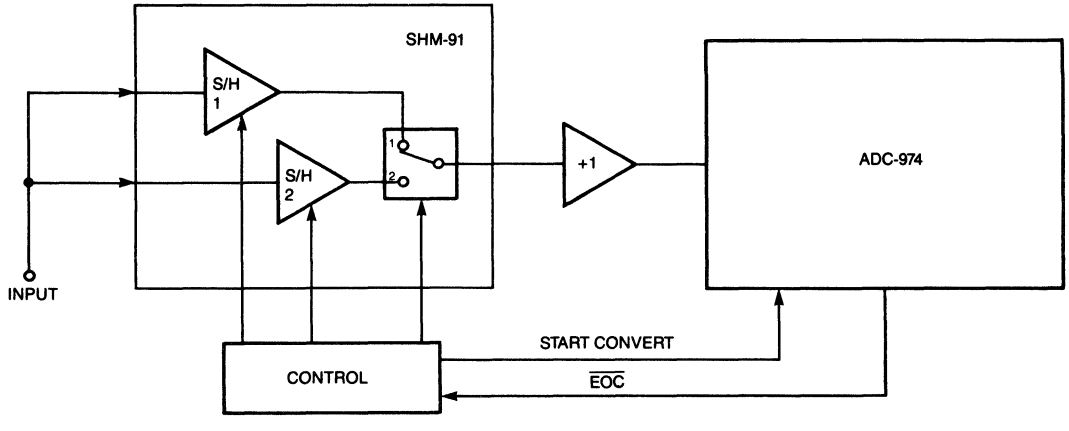


Figure 6. Ultra-Fast A/D Conversion Application

Acquisition time of a sample-and-hold sometimes takes up a sizeable part of the analog-to-digital conversion cycle. As shown in Figure 6, interleaving two sample-and-hold devices (using DATEL's SHM-91) lets one device acquire the signal while the ADC-974 converts the other device's output.

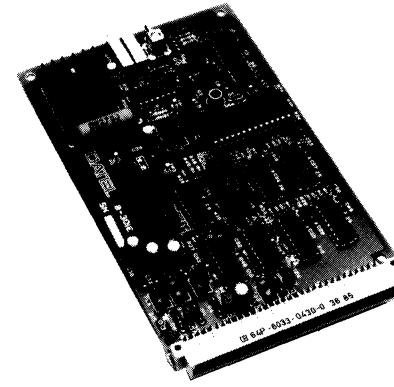
ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-974	16-bit resolution (14-bit linearity) 2.5 μSec. conversion time A/D Converter

ADC-B301E
SAMPLING A/D BOARD

FEATURES

- 10 MHz Input bandwidth
- High-speed sampling rate of 40 MHz
- 8-Bit resolution across entire bandwidth
- TTL logic compatible
- Eurocard size, DIN connector



APPLICATIONS

- Video signal processing
- High speed voice signal analysis
- Radar system
- Transient analysis
- Atomic energy-related instrument control

DATEL's ADC-B301E is a stand-alone Eurocard-sized sampling A/D board offering true 8-bit accuracy across the entire dc to 10 MHz bandwidth. Also, the ADC-B301E eliminates the need for custom test equipment when evaluating DATEL's ADC-301 Flash Converter.

GENERAL DESCRIPTION

The ADC-B301E is a complete sampling A/D conversion board designed around DATEL's ADC-301 flash A/D converter. The ADC-B301E is functionally complete containing a buffer amplifier, offset and gain adjustment circuitry, filtering and timing circuitry.

DATEL designed the ADC-B301E with two purposes in mind; first, as a self-supporting, high-speed sampling analog-to-digital converter board. Secondly, as a means to evaluate DATEL's ADC-301 flash A/D converter.

DATEL's design takes into consideration crucial factors such as board layout, impedance matching, input buffering, filtering and timing.

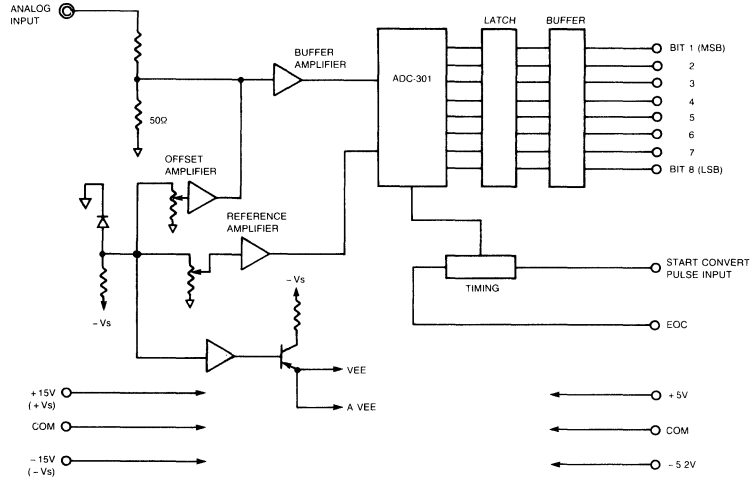


Figure 1. ADC-B301E Simplified Block Diagram

The ADC-B301E performs A/D conversions at sampling rates up to 40 MHz. Using a four-layer printed circuit board and high frequency noise filtering techniques assures perfect conversions free from noise problems. Linearity error and differential linearity error are guaranteed to be less than one half LSB.

The ADC-B301E sampling board provides true 8-bit accuracy across the entire 10 MHz input bandwidth. Video signal digitizing, radar signal processing, and transient signal analysis are ideal applications for this wide-bandwidth, highly-accurate front-end board.

As a design tool, the board relieves the design engineer of the labor- and time-intensive task of constructing an evaluation circuit to test the applicability of the DATEL's ADC-301 flash converter in their design. The board allows fast hook-up and prototype evaluation, shortening the design cycle. The ADC-B301E also makes an ideal test fixture for incoming inspection and component qualification.

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V, –5.2V, +5V dc power unless otherwise specified.

INPUTS

Analog Input Range (See Technical Note 2)	0 to +1V, ±0.5V
Input Impedance (See Technical Note 4)	50 ohms
Input Signal Bandwidth	10 MHz
Digital Input	TTL-compatible
Logic Level 0	0V to +0.8V dc
1	+2V to +5.5V dc
Convert Pulse Width	10 nSec. minimum

OUTPUTS
(See Technical Note 7)

PERFORMANCE

Conversion Rate	30 MHz minimum, 40 MHz typical
Non-Linearity	±1/2 LSB maximum
Differential Non-Linearity	±1/2 LSB maximum
Missing Codes	None
Differential Gain Error	1.5%
Differential Phase Error	0.5 degrees

POWER REQUIREMENTS

$+V_S/+I_S$	+14.5 to +15.5V/+45 mA
$-V_S/-I_S$	–14.5 to –15.5V/–150 mA
V_{ee}/I_{ee}	–5.7 to –4.7V/480 mA
V_{cc}/I_{cc}	+4.5 to +5.5V/110 mA

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range	0 to +70 °C
Storage Temperature Range	–25 to +85 °C
Mechanical Dimensions	100(W) x 160(D) x 19 (H) mm Eurocard Size

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages
- **±Vs (Pins A30, A32)** . . ±17.5V
- **Vee (Pins A18, B18)** . . . –8V to 0V
- **Vcc (Pin A26)** . . . . . +7V

Digital Input (A21) . . . . . +7V

Analog Inputs
- **(Pins A28, B28)** . . . . . ±5V

TECHNICAL NOTES

Refer to the Simplified Block Diagram (Figure 1) and the Schematic Diagram (Figure 2) for further information.

1. The ±15V dc analog power supply commons and the ±5V dc digital power supply common are grounded to one point at J1 on the board. DATEL does not recommend having this common ground outside the board; noise problems may result from ground loops. If it is, however, required to have a common point outside the board, cut the etch to J1. In this case, avoid creating different potentials between digital and analog grounds.
2. The analog input voltage signal range is adjusted at ±0.5V dc at the time of the shipment from the factory. An offset adjustment trimpot, labeled 'OFFSET' on the board, allows shifting the input level to, for instance, a 0 to +1V dc range. Input voltage amplitude to the ADC-301 is always 1V peak-to-peak.
3. Supply the analog input signal to the coaxial cable input terminal (CN1). This input signal can be also supplied via the DIN connector. In this case, connect the two sets of feedthrough holes labeled 'SIG' in Figure 3 with a short coaxial cable and then supply the signal to the A28 (signal) and B28 (signal GND) terminals.
4. Resistor R1 is not installed, but is short-circuited with a jumper wire at the time of shipment from the factory; this sets the input impedance at 50 ohms. Replace this jumper wire with a 24 ohm resistor when 75 ohms of input impedance is required.
5. A gain adjustment trimpot, labeled 'GAIN', is installed on the board to adjust the –2V reference voltage required for the A/D converter. This trimpot is adjusted at the time of shipment. If necessary, fine tune the gain while taking the input from test point TP1 into a high-impedance digital multimeter.
6. A trimpot, labeled 'LIN', is installed on the board to fine tune the board's linearity. This trimmer is strictly fine tuned at the time of shipment. When linearity is suspect, use this trimpot to maintain one-half the reference voltage present on TP1. Use a high-impedance multimeter to measure the linearity voltage at pin 22 of the ADC-301.
7. Digital output coding is factory-set to positive true, offset binary coding. There are LINV and MINV etch pads on the board. These are used to change the output code to 2's complement, or negative true, logic. These points connect to analog ground through 3.9K ohm resistors (R48, R49) at the time of shipment to keep both points at logic "1" level.

   To obtain a logic "0" level, cut the etch, leaving LINV and MINV open. Refer to Table 1 for output coding information. To re-establish logic "1" levels, solder jumper wires between the feedthrough holes provided.

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

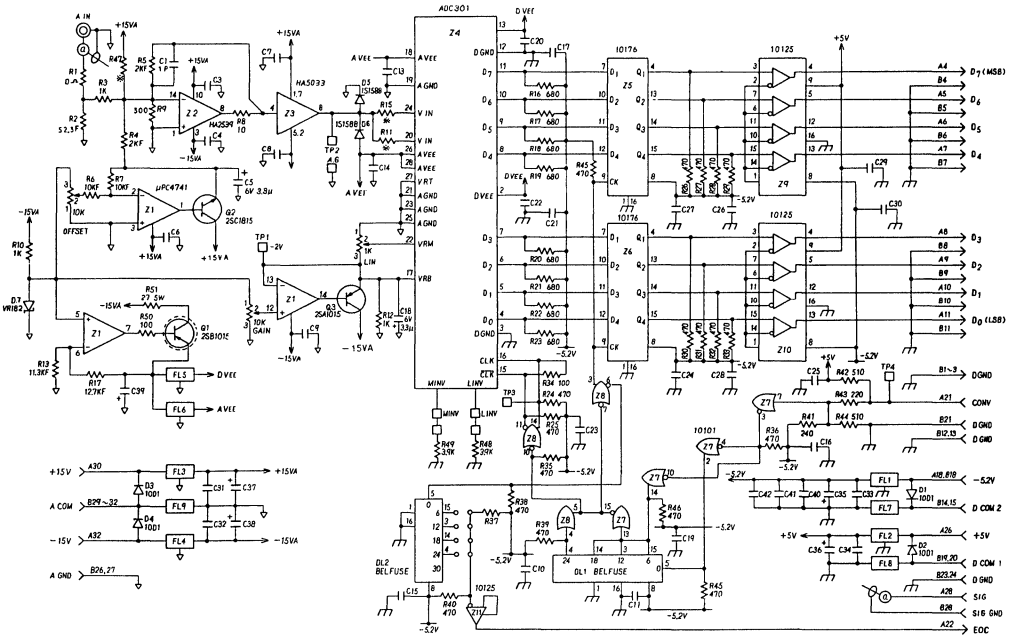


Figure 2. ADC-B301E Schematic Diagram

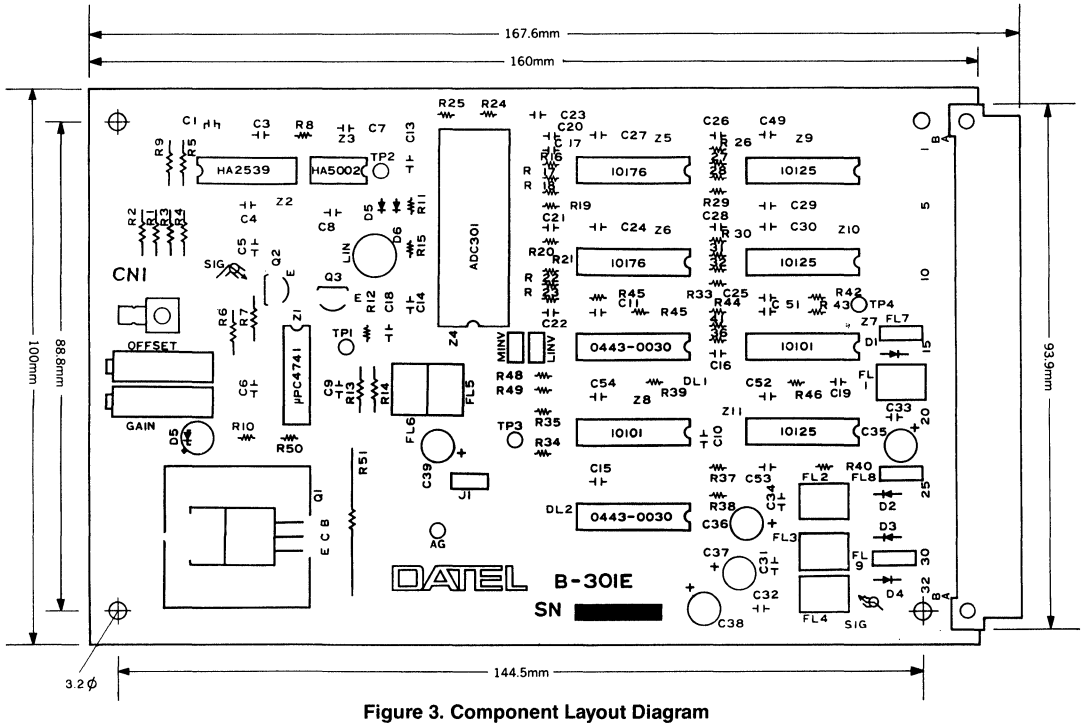


Figure 3. Component Layout Diagram

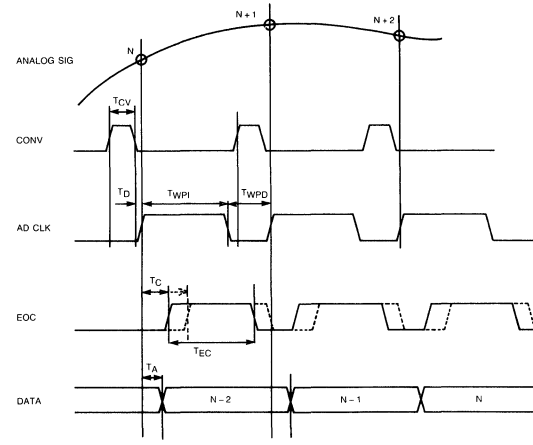
TECHNICAL NOTES (cont.)

8. Output digital data is valid after three START CONVERT pulses. Output data is then available on the falling edge of the EOC pulse. Refer to Figure 4, the ADC-B301E timing diagram.
9. There are several test points (TP2, TP3, TP4) for checking the performance of the board. While these points are available, the user should check the signals with high-impedance test probes only.

   Performance of the board deteriorates if large external loads are applied to these points. The following signals are present on the indicated test points:

TEST POINT	SIGNAL
TP2	ANALOG INPUT signal to the ADC-301
TP3	CLOCK
TP4	START CONVERT pulse

10. Digital input and output signals are all TTL-compatible. The START CONVERT pulse width should be 10 nanoseconds minimum and should be supplied through a buffer such as an 74LS240. Logic circuits on the board are driven on the rising edge of the START CONVERT pulse with a minimum 10 nanoseconds pulse width.
11. An EOC signal output is available through a delay circuit in order to optimize timing with any external circuits. Four delay steps of 6 nanoseconds each are available. The delay time is set at zero nanoseconds at the time of shipment. Figure 5 shows jumper positions to set the EOC delay time.
12. The ADC-B301E's design allows it to convert analog input signals from dc up to 10 MHz. A capacitor in the feedback loop of the buffer amplifier regulates this analog input signal bandwidth.



	T_{CV} MIN nSEC	T_{WPI} nSEC	T_{WPD} MIN nSEC	T_D nSEC	T_A nSEC	T_{EC} nSEC	T_C nSEC
ADC-B301E	10	25	8	2	5	25	10

Figure 4. ADC-B301E Timing Diagram (not drawn to scale)

Table 1. Output Coding

INPUT/OUTPUT CODE		
Input Voltage	**Step**	**Output Code**
0 V	0	00000000
3.9 mV	0	00000001
7.7 mV	2	00000010
15.6 mV	4	00000100
35.25 mV	8	00001000
62.5 mV	16	00010000
125.0 mV	32	00100000
250.0 mV	64	01000000
500.0 mV	128	10000000
750.0 mV	192	11000000
996.1 mV	255	11111111
BIPOLAR INPUT/OUTPUT CODE		
Input Voltage	**Step**	**Output Code**
−0.500V	0	00000000
−0.496V	1	00000001
−0.492V	2	00000010
−0.484V	4	00000100
−0.469V	8	00001000
−0.438V	16	00010000
−0.375V	32	00100000
−0.250V	64	01000000
0.000V	128	10000000
+0.250V	192	11000000
+0.496V	255	11111111

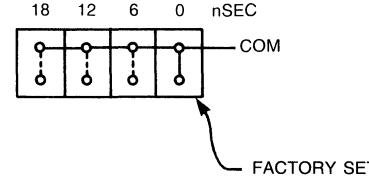


Figure 5. EOC Selection Chart

Table 2. ADC-B301E Pin Connections

FUNCTION	CONNECTOR PINS A	B	FUNCTION
NC	1	1	Digital Ground
NC	2	2	"
NC	3	3	"
Bit 1 (MSB)	4	4	"
2	5	5	"
3	6	6	"
4	7	7	"
5	8	8	"
6	9	9	"
7	10	10	"
8 (LSB)	11	11	"
NC	12	12	"
NC	13	13	"
NC	14	14	Digital Common
NC	15	15	"
NC	16	16	NC
NC	17	17	NC
−5.2V (Vee)	18	18	−5.2V (Vee)
NC	19	19	DIG COM
NC	20	20	"
Start Convert Input	21	21	Digital Gnd
EOC	22	22	NC
NC	23	23	Digital Gnd
NC	24	24	"
NC	25	25	NC
+5V (Vcc)	26	26	Analog Gnd
NC	27	27	"
Analog Input Signal	28	28	Analog Input Signal Gnd
NC	29	29	Analog Common
+15V (+Vs)	30	30	"
NC	31	31	"
−15V (−Vs)	32	32	"

Dynamically Testing The ADC-301

Using basic lab equipment and popular software, the design engineer can perform advanced, dynamic tests of the ADC-B301E board, and the ADC-301, with relative ease.

The user may wish to dynamically test the ADC-301 using the equipment configuration shown in Figure 6. A sine wave generator, with a low noise floor (below 8 bits), feeds an input signal to the ADC-B301E board to provide a clean signal source. A clock generator then provides a clock signal to the START CONVERT input at the specified conversion rate.

Once power is applied, the ADC-B301E produces a digitized version of the input signal. This output is then stored in RAM, sampled over a period of time to ensure an adequate sample base. Using widely-available Fast Fourier Transform programs, the data in RAM provides the basis for total system response analysis. Parameters such as second harmonic distortion, total harmonic distortion, and signal-to-noise ratios can be derived from this information.

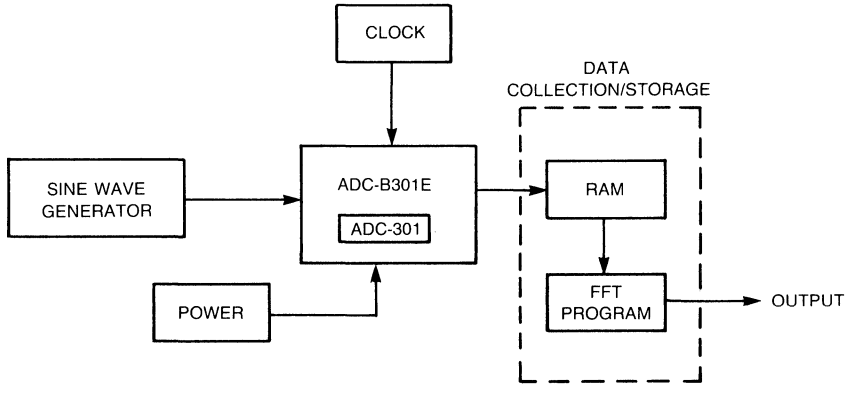


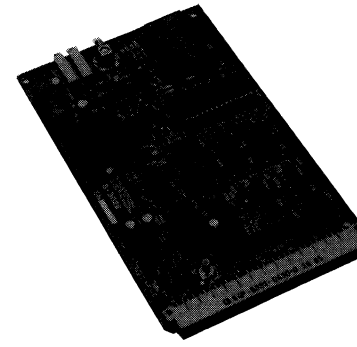
Figure 6. Dynamically Testing the ADC-301

ORDERING INFORMATION	
ADC-B301E	SAMPLING A/D BOARD

ADC-B302E
SAMPLING A/D BOARD

FEATURES

- **15 MHz Input bandwidth**
- **High-speed sampling rate of 60 MHz**
- **8-Bit resolution across entire bandwidth**
- **ECL logic compatible**
- **Eurocard size, DIN connector**



APPLICATIONS

- **Video signal processing**
- **High speed voice signal analysis**
- **Radar system**
- **Transient analysis**
- **Atomic energy-related instrument control**

DATEL's ADC-B302E is a stand-alone Eurocard-sized sampling A/D board offering true 8-bit accuracy across the entire dc to 15 MHz bandwidth. Also, the ADC-B302E eliminates the need for custom test equipment when evaluating DATEL's ADC-302 Flash Converter.

GENERAL DESCRIPTION

The ADC-B302E is a complete sampling A/D conversion board designed around DATEL's ADC-302 flash A/D converter. The ADC-B302E is functionally complete containing a buffer amplifier, offset and gain adjustment circuitry, filtering and timing circuitry.

DATEL designed the ADC-B302E with two purposes in mind; first as a self-supporting, high-speed sampling analog-to-digital converter board. Secondly as a means to evaluate DATEL's ADC-302 flash A/D converter.

DATEL's design takes into consideration crucial factors such as board layout, impedance matching, input buffering, filtering and timing

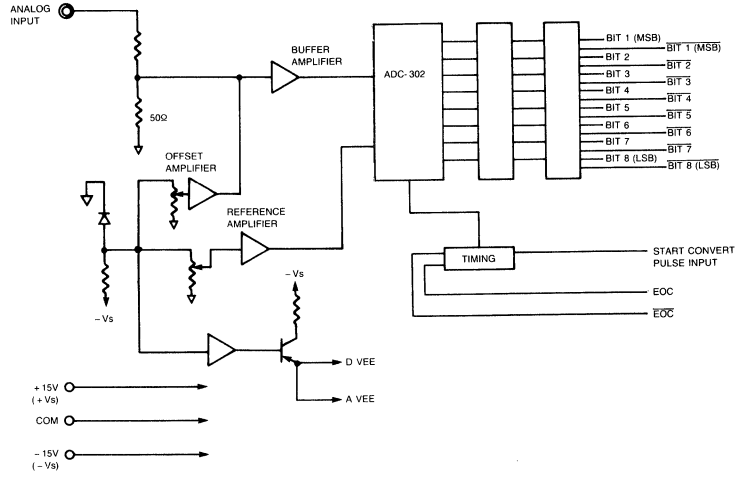


Figure 1. ADC-B302E Simplified Block Diagram

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

The ADC-B302E performs A/D conversions at sampling rates up to 60 MHz. Using a four-layer printed circuit board and high frequency noise filtering techniques assures perfect conversions free from noise problems. Linearity error and differential linearity error are guaranteed to be less than one half LSB.

The ADC-B302E sampling board provides true 8-bit accuracy across the entire 15 MHz input bandwidth. Video signal digitizing, radar signal processing, and transient signal analysis are ideal applications for this wide-bandwidth, highly-accurate front-end board.

As a design tool, the board relieves the design engineer of the labor- and time-intensive task of constructing an evaluation circuit to test the applicablilty of the DATEL's ADC-302 flash conerter in their design. The board allows fast hook-up and prototype evaluation, shortening the design cycle. The ADC-B302E also makes an ideal test fixture for incoming inspection and component qualification.

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V, -5.2V dc power unless otherwise specified.

INPUTS	
Analog Input Range (See Technical Note 2)	0 to +1V, ±0.5V
Input Impedance (See Technical Note 4)	50 ohms
Input Signal Bandwidth	15 MHz
Digital Input	ECL-compatible
Logic Level 0	−1.85V to −1.65V dc
1	−0.96V to −0.81V dc
Convert Pulse Width	8 nSec. minimum
OUTPUTS (See Technical Note 7)	
PERFORMANCE	
Conversion Rate	50 MHz minumum, 60 MHz typical
Nonlinearity	±1/2 LSB maximum
Differential Nonlinearity	±1/2 LSB maximum
Missing Codes	None
Differential Gain Error	1.5%
Differential Phase Error	0.5 degrees
POWER REQUIREMENTS	
$+V_S/+I_S$	+14.5 to +15.5V/+30 mA
$-V_S/-I_S$	−14.5 to −15.5V/−210 mA
V_{ee}/I_{ee}	−5.7 to −4.7V/780 mA
PHYSICAL-ENVIRONMENTAL	
Operating Temperature Range	0 to +70 °C
Storage Temperature Range	−25 to +85 °C
Mechanical Dimensions	100(W) x 160(D) x 19 (H) mm Eurocard Size

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages
+Vs (Pins A30, A32) . . ±16V
Vee (Pins A18, B18) . . . −8V to 0V
Digital Inputs
(Pins A4 through A11) . . . . . −8V to 0V
Analog Inputs
(Pins A28, B28) . . . . . ±5V

TECHNICAL NOTES

Refer to the Simplified Block Diagram (Figure 1) and the Schematic Diagram (Figure 2) for further information.

1. The ±15V dc analog power supply commons and the +5V dc digital power supply common are grounded to one point at J1 on the board. DATEL does not recommend having this common ground outside the board; noise problems may result from ground loops. If it is, however, required to have a common point outside the board, cut the etch to J1. In this case, avoid creating different potentials between digital and analog grounds.
2. The analog input voltage signal range is adjusted at ±0.5V dc at the time of the shipment from the factory. An offset adjustment trimpot, labeled 'OFFSET' on the board, allows shifting the input level to, for instance, a 0 to +1V dc range. Input voltage amplitude to the ADC-302 is always 1V peak-to-peak.
3. Supply the analog input signal to the coaxial cable input terminal (CN1). This input signal can be also supplied via the DIN connector. In this case, connect the two sets of feedthrough holes labeled 'SIG' in Figure 3 with a short coaxial cable and then supply the signal to the A28 (signal) and B28 (signal GND) terminals.
4. Resistor R1 is not installed, but is short-circuited with a jumper wire at the time of shipment from the factory; this sets the input impedance at 50 ohms. Replace this jumper wire with a 24 ohm resistor when 75 ohms of input impedance is required.
5. A gain adjustment trimpot, labeled 'GAIN', is installed on the board to adjust the −2V reference voltage required for the A/D converter. This trimpot is adjusted at the time of shipment. If necessary, fine tune the gain while taking the input from test point TP1 into a high-impedance digital multimeter.
6. A trimpot, labeled 'LIN', is installed on the board to fine tune the board's linearity. This trimmer is strictly fine tuned at the time of shipment. When linearity is suspect, use this trimpot to maintain one-half the reference voltage present on TP1. Use a high-impedance multimeter to measure the linearity voltage at pin 22 of the ADC-302.
7. Digital output coding is factory-set to positive true, offset binary coding. There are LINV and MINV etch pads on the board. These are used to change the output code to 2's complement, or negative true, logic. These points connect to analog ground through 3.9K ohm resistors (R48, R49) at the time of shipment to keep both points at logic "1" level.

   To obtain a logic "0" level, cut the etch, leaving LINV and MINV open. Refer to Table 1 for output coding information. To re-establish logic "1" levels, solder jumper wires between the feedthrough holes provided.

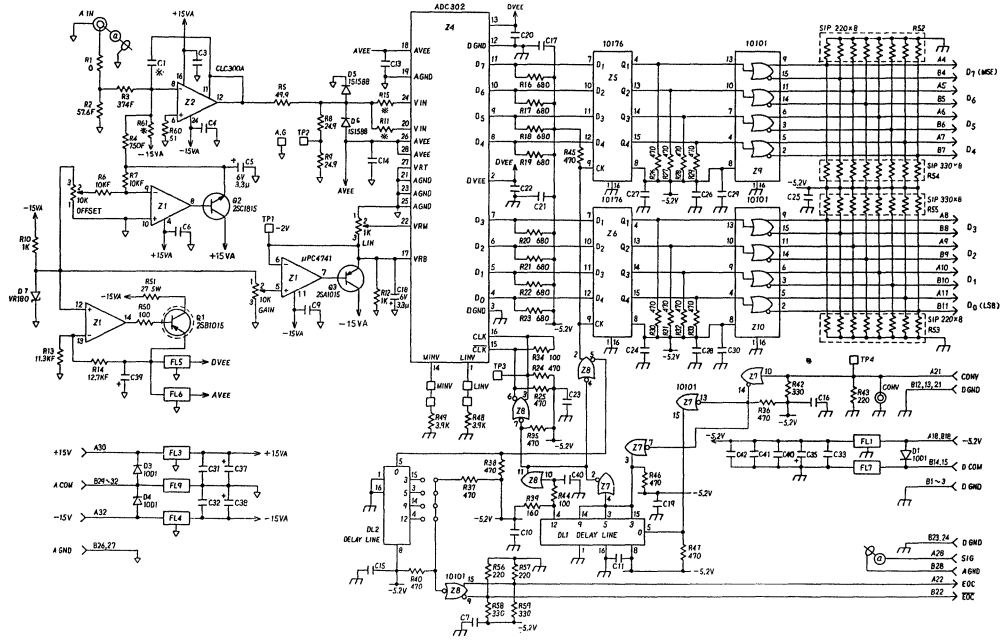


Figure 2. ADC-B302E Schematic Diagram

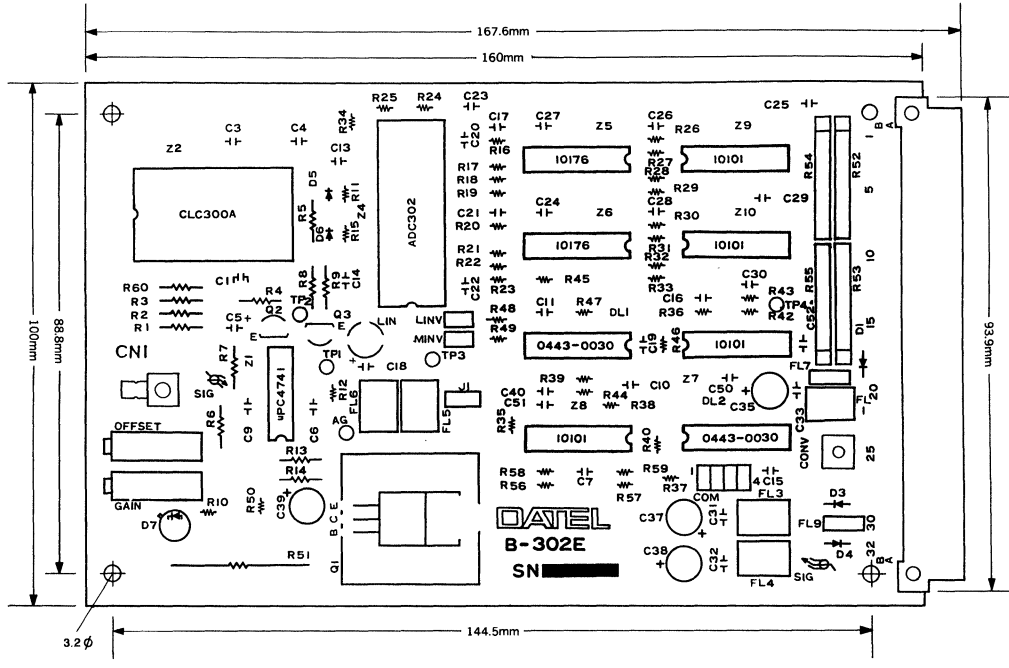


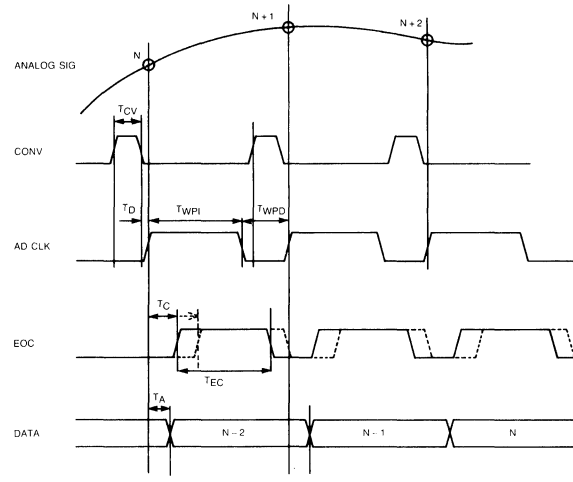
Figure 3. Component Layout Diagram

8. Output digital data is valid after three START CONVERT pulses. Output data is then available on the falling edge of the EOC pulse. Refer to Figure 4, the ADC-B302E timing diagram.
9. There are several test points (TP2, TP3, TP4) for checking the performance of the board. While these points are available, the user should check the signals with high-impedance test probes only.

   Performance of the board deteriorates if large external loads are applied to these points. The following signals are present on the indicated test points:

TEST POINT	SIGNAL
TP2	ANALOG INPUT signal to the ADC-302
TP3	CLOCK
TP4	START CONVERT pulse

10. Digital input and output signals are all differential ECL-compatible except the START CONVERT pulse which is an ECL-compatible, positive true input. This start convert pulse is pulled up to ground with 220 ohms and pulled down to the −5.2V power supply with a 300 ohm resistor.
11. Output data lines and the EOC signal are differential. The pull-up and pull-down resistors can be removed at the board side, then installed at the signal receiver side in applications requiring long signal transfer distances.
12. An EOC signal output is available through a delay circuit in order to optimize timing with any external circuits. Four delay steps of 3 nanoseconds each are available. The delay time is set at zero nanoseconds at the time of shipment. Figure 5 shows jumper positions to set the EOC delay time.



	TCV MIN nSEC	TWPI nSEC	TWPD MIN nSEC	TD nSEC	TA nSEC	TEC nSEC	TC nSEC
ADC-B302E	8	15	5	2	5	15	6

Figure 4. ADC-B302E Timing Diagram (not drawn to scale)

Table 1. Output Coding

INPUT/OUTPUT CODE		
Input Voltage	**Step**	**Output Code**
0 V	0	00000000
3.9 mV	0	00000001
7.7 mV	2	00000010
15.6 mV	4	00000100
35.25 mV	8	00001000
62.5 mV	16	00010000
125.0 mV	32	00100000
250.0 mV	64	01000000
500.0 mV	128	10000000
750.0 mV	192	11000000
996.1 mV	255	11111111
BIPOLAR INPUT/OUTPUT CODE		
Input Voltage	**Step**	**Output Code**
−0.500V	0	00000000
−0.496V	1	00000001
−0.492V	2	00000010
−0.484V	4	00000100
−0.469V	8	00001000
−0.438V	16	00010000
−0.375V	32	00100000
−0.250V	64	01000000
0.000V	128	10000000
+0.250V	192	11000000
+0.496V	255	11111111

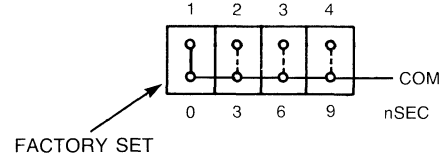


Figure 5. EOC Selection Chart

Table 2. Pin Connections

FUNCTION	CONNECTOR PINS A	B	FUNCTION
NC	1	1	Digital Ground
NC	2	2	Digital Ground
NC	3	3	Digital Ground
Bit 1 (MSB)	4	4	$\overline{\text{Bit 1 (MSB)}}$
Bit 2	5	5	$\overline{\text{Bit 2}}$
Bit 3	6	6	$\overline{\text{Bit 3}}$
Bit 4	7	7	$\overline{\text{Bit 4}}$
Bit 5	8	8	$\overline{\text{Bit 5}}$
Bit 6	9	9	$\overline{\text{Bit 6}}$
Bit 7	10	10	$\overline{\text{Bit 7}}$
Bit 8 (LSB)	11	11	$\overline{\text{Bit 8 (LSB)}}$
NC	12	12	Digital Ground
NC	13	13	Digital Ground
NC	14	14	Digital Common
NC	15	15	Digital Common
NC	16	16	NC
NC	17	17	NC
−5.2V (Vee)	18	18	−5.2V (Vee)
NC	19	19	NC
NC	20	20	NC
Start Convert Input	21	21	Digital Gnd
EOC	22	22	$\overline{\text{EOC}}$
NC	23	23	Digital Gnd
NC	24	24	Digital Ground
NC	25	25	NC
NC	26	26	Analog Gnd
NC	27	27	Analog Gnd
Analog Input Signal	28	28	Analog Input Signal Gnd
NC	29	29	Analog Common
+15V (+Vs)	30	30	Analog Common
NC	31	31	Analog Common
−15V (-Vs)	32	32	Analog Common

Dynamically Testing The ADC-302

Using basic lab equipment and popular software, the design engineer can perform advanced, dynamic tests of the ADC-B302E board, and the ADC-302, with relative ease.

The user may wish to dynamically test the ADC-302 using the equipment configuration shown in Figure 6. A sine wave generator, with a low noise floor (below 8 bits), feeds an input signal to the ADC-B302E board to provide a clean signal source. A clock generator then provides a clock signal to the START CONVERT input at the specified conversion rate.

Once power is applied, the ADC-B302E produces a digitized version of the input signal. This output is then stored in RAM, sampled over a period of time to ensure an adequate sample base. Using widely-available Fast Fourier Transform programs, the data in RAM provides the basis for total system response analysis. Parameters such as second harmonic distortion, total harmonic distortion, and signal-to-noise ratios can be derived from this information.

ORDERING INFORMATION

ADC-B302E	SAMPLING A/D BOARD

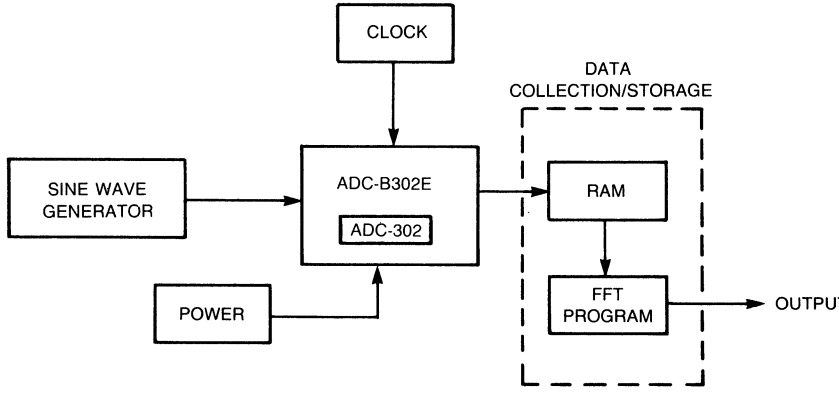


Figure 6. Dynamically Testing the ADC-302

ADC-B303E
8-BIT, 100 MHz SAMPLING A/D BOARD

FEATURES

- **8-Bit Resolution**
- **40 MHz (-3dB) Input Bandwidth**
- **100 MHz Sampling Rate**
- **ECL Logic Compatible**
- **Eurocard Size, Din Connector**

APPLICATIONS

- **Video signal processing**
- **High-speed voice signal analysis**
- **Transient analysis**
- **Atomic energy-related instrument control**

DATEL's ADC-B303E is an 8-bit, 100 MHz Sampling A/D board, offering an input bandwith of dc to 40 MHz. Also, the ADC-B303E eliminates the need for developing a test board when evaluating DATEL's ADC-303 flash converter.

GENERAL DESCRIPTION

The ADC-B303E is a complete video A/D converter board designed around DATEL's ADC-303, 8-bit, 100MHz flash converter. Contained on the board are local power supplies, timing circuitry, input buffer amplifier, linearity adjustment circuitry, filtering, timing and an output buffer register.

The ADC-B303E performs analog-to-digital conversions with linearity and differential linearity errors less than 1/2 LSB for input signal bandwidths up to 40MHz (-3dB).

The Eurocard board also contains offset and gain circuitry, is ECL logic compatible and can perform ultra high-speed conversions up to 100MHz. The board serves as a self-supporting high-speed analog-to-digital converter board. The four-layer printed circuit board and high frequency noise filtering construction techniques by DATEL, assure perfect conversions free from noise problems.

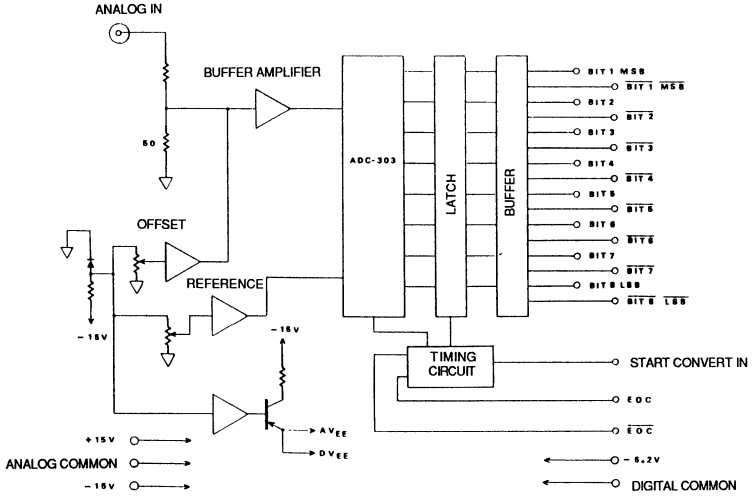


Figure 1. ADC-B303E Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltages:	
+15V Supply (Pin A30)	+18V
-15V Supply (Pin A32)	-18V
-5.2V Supply (Pin A18, B18)	-8V
Clock Pulse Input Voltage (Pin A21)	-8V
Analog Input Volgate (ANA IN) (Pin A28)	±5V

FUNCTIONAL SPECIFICATIONS

Typical at 25 degrees C, ±15V, -5.2V power unless otherwise stated.

DESCRIPTION	MIN.	TYP.	MAX.	UNIT
ANALOG INPUTS				
Input Ranges	—	0 to +1	—	Volts
	—	±0.5	—	Volts
Input Impedance				
R1 = 0 Ω (standard)	—	50	—	Ohms
R2 = 24 Ω (user-supplied)	—	75	—	Ohms
Input Signal Bandwidth (-3 dB)	40	—	—	MHz
DIGITAL INPUT				
Start Convert Pulse Width	5	—	—	nS
OUTPUTS				
Resolution	8	—	—	Bits
Digital Output Logic Levels:				
Logic 1	-0.81	—	-0.96	Volts
Logic 0	-1.65	-1.75	-1.85	Volts
Logic Loading 1	—	—	265	µA
Logic Loading 0	0.5	—	—	µA
PERFORMANCE				
Conversion Rate	100	—	—	MHz
Non-Linearity	—	—	± 1/2	LSB
Differential Non-Linearity	—	—	± 1/2	LSB
Differential Gain Error	—	1.5	—	%
Differential Phase Error	—	0.5	—	Deg.
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V Supply	+14.5	+15.0	+15.5	Volts
-15V Supply	-14.5	-15.0	-15.5	Volts
-5.2V Supply	-4.7	-5.2	-5.7	Volts
Power Supply Current:				
+15V Supply	—	+40	—	mA
-15V Supply	—	-350	—	mA
-5.2V Supply	—	-750	—	mA
PHYSICAL-ENVIRONMENTAL				
Operating Temperature Range	0	—	+70	°C
Storage Temperature Range	-25	—	+85	°C
Mechanical Dimensions	3.94" (W) x 6.3" (D) x 0.67" (H) 100 (W) x 160 (D) x 17 (H) mm			
Weight	0.31 Lbs. (165 Grams)			

GENERAL DESCRIPTION (*cont.*)

The board also offers the design engineer fast hook-up for prototype evaluation. The labor-and-time intensive task of constructing an evaluation circuit to test the applicability of the ADC-303 flash converter is virtually elimintated. The ADC-B303E also makes an ideal test fixture for incoming inspection and component qualification.

TECHNICAL NOTES

Refer to the Simplified Block Diagram and the Schematic Diagram for more information.

1. The ±15V dc analog power supply commons and the - 5.2V dc digital power supply common are grounded to one point on the board. The analog and digital grounds should not be connected externally as the ground loop created may result in unwanted noise. If a common ground is outside the board, cut the etch to J1. In this case, avoid creating potentials between digital and analog grounds on the ADC-B303E Sampling A/D board.

2. The digital input and output signals are differential ECL-compatible except the START CONVERT pulse. It is supplied from the coaxial cable connector labled "CONV" on the board or the terminals of the DIN connector, A21 (START CONVERT) and B21 (START CONVERT signal GND).

The START CONVERT pulse is pulled up to ground with an 82 ohm resistor and pulled down to the -5.2V dc power supply with an 130 ohm resistor. As a result, input impedance of the START CONVERT pulse is 50 ohms.

4. The START CONVERT pulse width must be a minimum of 5 nanoseconds. Care should be taken to match the impedance of the START CONVERT pulse signal to the characteristic impedance of the START CONVERT input on the ADC-B303E board.

5. The pull-up and pull-down resistors of the output data lines and $\overline{EOC}$ can be removed from the board and installed on the receiver side of the digital outputs for applications requiring a long signal transfer distance.

6. Approximately 15 minutes of warm-up time is required for maximum accuracy and stable performance.

7. The surface temperature of some components on the board reach 70°C when the board is operated at room temperature (25°C). It is recommended to operate the board with adequate air circulation.

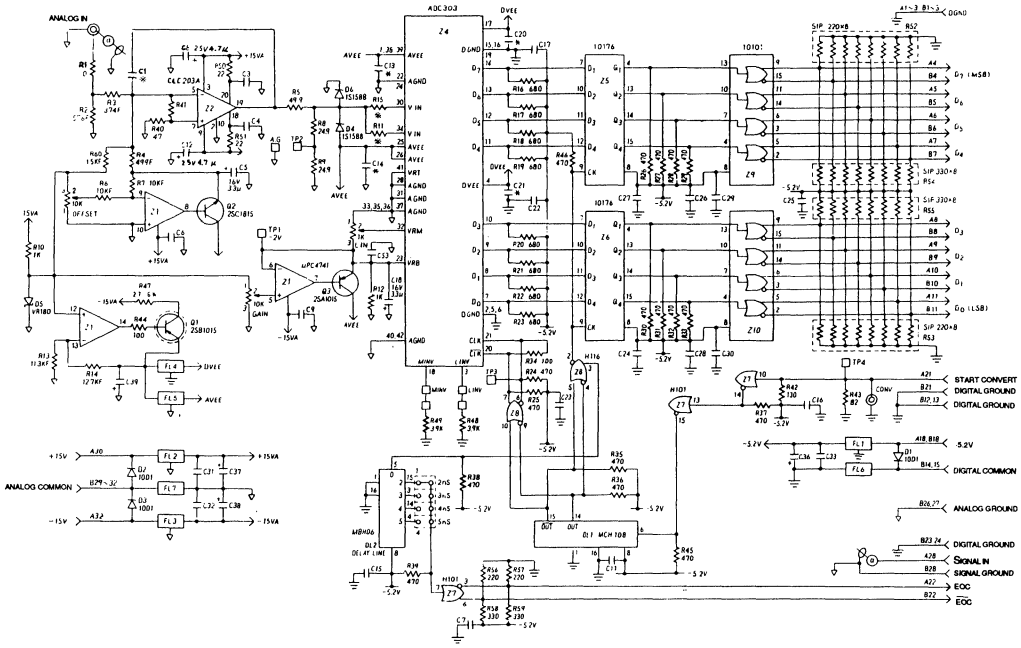


Figure 2. ADC-B303E Schematic Diagram

THEORY OF OPERATION

Refer to the timing diagram, schematic and board layout of the ADC-B303E board as necessary. The ADC-B303E Sampling A/D board has built-in offset, gain and reference adjustment trimpots plus an analog input signal amplifier which accepts 1Vp-p input signals. The board also contains regulated, on-board power supplies which adds stability to the board's functions. Supporting timing circuitry, and easy signal and power connections make the board easy to use.

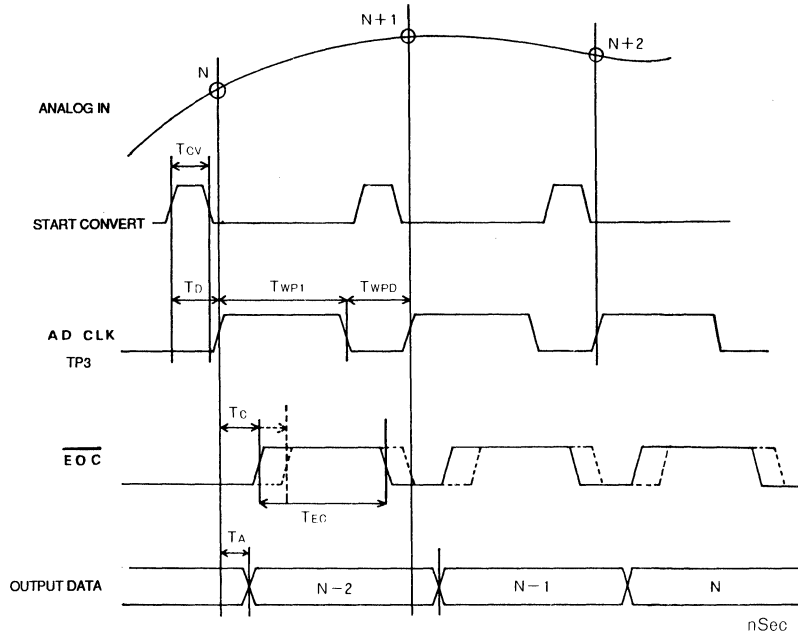
The analog input signal can be applied to either the analog input connection (AIN) or to the pins on the DIN card edge connector ANA IN. If the signal is to be applied to AIN, insert a piece of coax of the same characteristic impedance as the input impedance of the ADC-B303E. Connect one end of the coax to the feed-through holes labled "SIG" and the other end to terminals A28 (ANA IN) and B28 (SIG GND).

Analog input impedance matching of 50 or 75 ohms is obtained by placing a jumper wire in resistor R1's mounting feedthrough holes for 50 ohms impedance, or a 24 ohm resistor if 75 ohms of input impedance is required. Other input impedances are calculated by subtracting 50 ohms from the desired input impedance, and placing the difference value in the feed through holes to resistor R1.

After the analog input signal is offset adjusted on the board, it is fed to the input terminals of the ADC-303 Flash A/D.

Table 1. ADC-B303E Pin Connections

FUNCTION	PIN	PIN	FUNCTION
NC	A1	B1	DIG. GND.
NC	A2	B2	DIG. GND.
NC	A3	B3	DIG. GND.
BIT 1 (MSB)	A4	B4	$\overline{\text{BIT 1 (MSB)}}$
BIT 2	A5	B5	$\overline{\text{BIT 2}}$
BIT 3	A6	B6	$\overline{\text{BIT 3}}$
BIT 4	A7	B7	$\overline{\text{BIT 4}}$
BIT 5	A8	B8	$\overline{\text{BIT 5}}$
BIT 6	A9	B9	$\overline{\text{BIT 6}}$
BIT 7	A10	B10	$\overline{\text{BIT 7}}$
BIT 8 (LSB)	A11	B11	$\overline{\text{BIT 8 (LSB)}}$
NC	A12	B12	DIG. GND.
NC	A13	B13	DIB. GND.
NC	A14	B14	DIG. COM.
NC	A15	B15	DIG. COM.
NC	A16	B16	NC
NC	A17	B17	NC
−5.2V	A18	B18	−5.2V
NC	A19	B19	NC
NC	A20	B20	NC
START CONVERT	A21	B21	DIG. GND.
EOC	A22	B22	$\overline{\text{EOC}}$
NC	A23	B23	DIG. GND.
NC	A24	B24	DIG. GND.
NC	A25	B25	NC
NC	A26	B26	ANA. GND.
NC	A27	B27	ANA. GND.
ANA. IN	A28	B28	SIG. GND.
NC	A29	B29	ANA. COM.
+15V	A30	B30	ANA. COM.
NC	A31	B31	ANA. COM.
−15V	A32	B32	ANA. COM.



TCW min.	TWP1	TWPD min.	TD	TA	TEC	TC
5	7.5	2.5	7	5	7.5	4

Figure 3. ADC-B303E Timing Diagram

The input of the ADC-303 has two series resistors that inhibit parasitic oscillations, thus imporving the overall performance of the board. Supporting gain and reference circuitry adjusts the input range of the ADC-303.

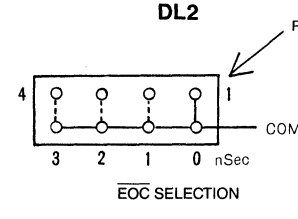
The gain and offset adjustments are described in detail in the calibration section of this data sheet. The output of the ADC-B303E is ECL compatible, and its timing is described as follows:

The START CONVERT pulse is applied to pin A21 and B21 or to the connector located on the board. Seven (7) nanoseconds later, the ADC-303 and the "10176" Master-Slave D-type latch are clocked simultaneously. Data that was at the output of the ADC-303 is now clocked into the "10176" latch, and the data that was in the "10176" master-slave latch goes to the slave and proceeds through an output buffer.

The data from the two previous A/D conversions is now at the output of the ADC-B303E board. It takes a total of three A/D clock pulses before the data is displayed at the output of the ADC-B303E board. The A/D clock signal from the delay circuitry gives a positive pulse 7.5 nanoseconds in duration and returns to a "low" state for the remainder of 2.5 nanoseconds for a total of ten (10) nanoseconds between the rising edge of each CLK pulse. Consequently, the data at the output of the ADC-B303E board changes every 10 nanoseconds. It is from this data change time duration that the 100MHz Sampling rate is derived.

An $\overline{EOC}$ signal is available to the user which indicates when the data is valid after the rising edge of the A/D clock pulse to the ADC-303. There is another delay line (DL2) which adds a delay of 0 to 3 nanoseconds to where the $\overline{EOC}$ pulse will go high. Therefore, a minimum of four (4) nanoseconds to a maximum of 7 nanoseconds after the rising edge of the A/D CLK pulse the $\overline{EOC}$ signal goes high.

The $\overline{EOC}$ pulse train is shifted (delayed) a minimum of 4 nanoseconds from the A/D CLK pulse train, and it takes a total of three (3) A/D CLK pulses before the first A/D conversion that was taken can be read. There is an elapsed time of 25 nanoseconds that exists between the rising edge pulse of the "first" A/D conversion when this "first" data can be outputted from the ADC-B303E board.



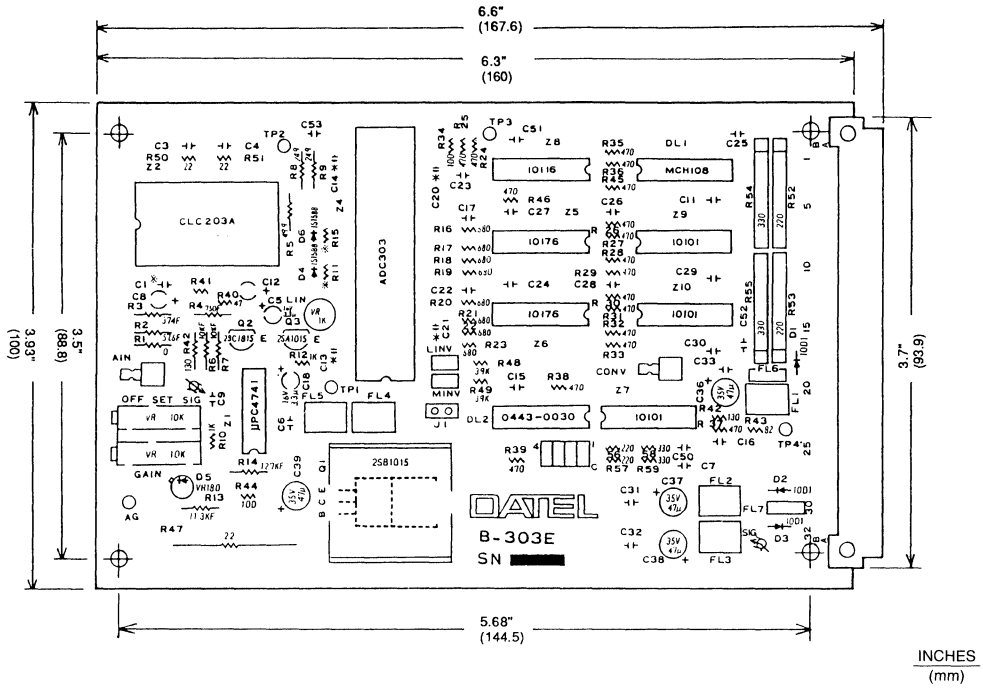


Figure 4. ADC-B303E Component Layout Drawing

CALIBRATION

There are three trimpots on the board, labeled "Offset", "Gain" and "LIN". Each function of these trimpots is described as follows:

1. OFFSET TRIMMER
The analog input signal voltage range is 1V peak-to-peak. This trimpot permits the user to match the output of their application to the input of the ADC-B303E board. For example, input voltage ranges may be adjusted from 0 to +1V, ± 0.5V, -0.4V to +0.6V, etc. This trimpot permits the offset adjustment range from 0 to -2.000V dc.

Unipolar Operation (0 to +1V)
Adjust the Offset trimpot with +1.9531 mV (+1/2 LSB) applied to ANA IN so the straight binary output code flickers between 0000 0000 and 0000 0001.

Bipolar Operation (±0.5V)
Adjust the Offset trimpot with +0.4980 mV (-FS + 1/2 LSB) applied to ANA IN so the offset binary output code flickers between 0000 0000 and 0000 0001.

2. GAIN TRIMMER (0 to +1V, ±5V)
This trimpot is installed to adjust the -2V reference voltage required for the ADC-303. Adjust the Gain adjust trimpot with +FS - 1 1/2 LSB applied to ANA IN (+0.99414V for Unipolar or +0.49414V for Bipolar operation) so the straight binary or offset binary output code flickers between 1111 1110 and 1111 1111.

3. LINEARITY TRIMMER
This trimpot is used to fine tune the linearity of the board. Connect a high-impedance digital multimeter to test point TP1 and ANA GND and measure this voltage. Reconnect the multimeter to pin 32 (VRM of the ADC-303 and ANA GND and adjust the Linearity trimpot to one-half (1/2) of the voltage indicated on test point TP1.

The following test points are provided on the board for calibration purposes. Care must be taken to minimize the loading of these test points when performing calibration and warranted adjustments.

TEST POINT	DESCRIPTION
TP1	Reference Voltage
TP2	Analog Input signal with offset compensation
TP3	A/D Clock
TP4	Start Convert pulse

Table 2. Output Coding for Unipolar and Bipolar Operation

UNIPOLAR OPERATION			STRAIGHT BINARY	COMP. BINARY
UNIPOLAR SCALE	INPUT VOLTAGE	MINV	1	0
		LINV	1	0
+ FS - 1 LSB	+ .9961 V		11111111	00000000
+ 7/8 FS	+ 875 mV		11100000	00011111
+ 3/4 FS	+ 750 mV		11000000	00111111
+ 1/2 FS	+ 500 mV		10000000	01111111
+ 1/4 FS	+ 250 mV		01000000	10111111
+ 1 LSB	+3.906 mV		00000001	11111110
0	0 V		00000000	11111111

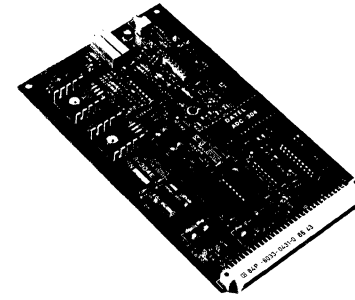
BIPOLAR OPERATION			OFFSET BINARY	COMP. OFFSET BINARY	2's COMP.	COMP. 2's COMP.
BIPOLAR SCALE	INPUT VOLTAGE	MINV	1	0	0	1
		LINV	1	0	1	0
+ FS - 1 LSB	+ 496.1 mV		11111111	00000000	01111111	10000000
+ 3/4 FS	+ 375 mV		11100000	00011111	01100000	10011111
+ 1/2 FS	+ 250 mV		11000000	00111111	01000000	10111111
+ 0	+ 0 mV		10000000	01111111	00000000	11111111
- 1/2 FS	- 250 mV		01000000	10111111	11000000	00111111
- 3/4 FS	- 375 mV		00100000	11011111	10100000	01011111
- FS + 1 LSB	- 496.1 mV		00000001	11111110	10000001	01111110
- FS	- 500 mV		00000000	11111111	10000000	01111111

NOTES: MINV is the output control pin for data bit 1 (MSB).
LINV controls output data bits 2 through 8.

ORDERING INFORMATION

ADC-B303E	100 MHz, 8-Bit Sampling A/D Board

ADC-B304E
8-BIT, 20 MHz SAMPLING A/D BOARD



FEATURES

- 8-Bit resolution
- 20 MHz sampling rate
- 8 MHz Input bandwidth
- TTL logic compatible
- Eurocard size, DIN connector

APPLICATIONS

- Video signal processing
- High-speed voice signal analysis
- Radar systems
- Transient analysis
- Atomic energy-related instrument control

GENERAL DESCRIPTION

The ADC-B304E Sampling A/D board is a complete A/D conversion board designed around DATEL's ADC-304 flash converter. The ADC-B304E is TTL logic compatible and offers built-in offset and gain adjustment circuitry. The board contains a buffer amplifier as well as filtering and timing circuitry.

DATEL designed the ADC-B304E sampling A/D board with two purposes in mind; first, to serve as a self-supporting, high-speed analog-to-digital converter board and secondly, as a means of evaluating DATEL's ADC-304 flash converter.

DATEL's design takes into consideration crucial factors such as board layout, impedance matching, input buffering and filtering. Design engineers must consider these factors when evaluating high-speed flash converters.

As a design tool, the board relieves the design engineer of the labor- and time-intensive task of constructing an evaluation circuit to test the applicability of the ADC-304 flash converter in their design. The board allows fast hook-up and prototype evaluation, shortening the design cycle.

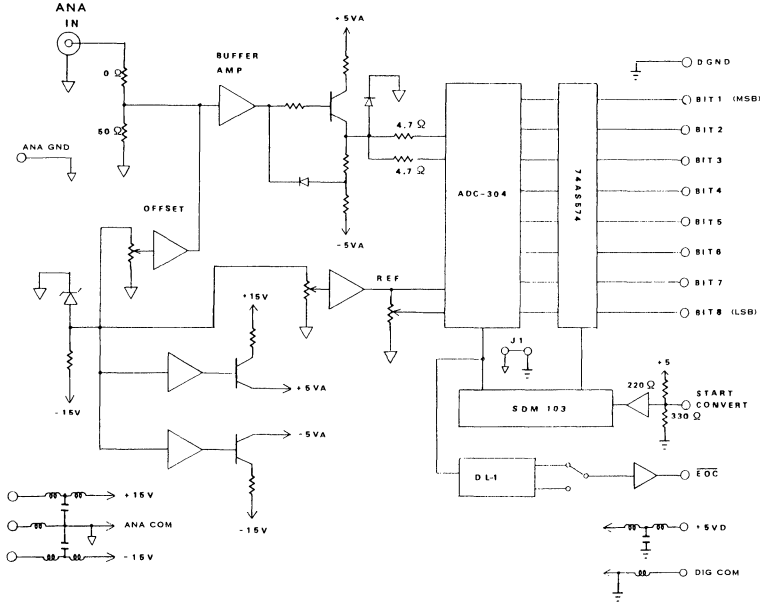


Figure 1. ADC-304 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltages:	
+15V Supply (Pin A30)	+18V
-15V Supply (Pin A32)	-18V
+ 5V Supply (Pin A26)	+7V
Clock Pulse Input Voltage (Pin A21)	+7V
Analog Input Voltage (ANA IN) (Pin A28)	±6V

FUNCTIONAL SPECIFICATIONS

Typical at 25 degrees C, ±15V, +5V power unless otherwise stated.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
ANALOG INPUTS				
Input Ranges	–	0 to +1	–	Volts
	–	± 0.5	–	Volts
Input Impedance				
R1 = 0 ohms (standard)	–	50	–	Ohms
R1 = 24 ohms (user-supplied)	–	75	–	Ohms
Input Signal Bandwidth (-3dB)	–	8	–	MHz
DIGITAL INPUTS				
Digital Input Logic Levels:				
Logic "1"	+ 2	–	+ 5.5	Volts
Logic "0"	0	–	+ 0.8	Volts
Logic Loading "1"	–	–	20	µA
Logic Loading "0"	–	–	24	mA
OUTPUTS				
Resolution	8	–	–	Bits
Digital Output Logic Levels:				
Logic "1"	+ 2.4	–	–	Volts
Logic "0"	0	–	+ 0.4	Volts
Logic Loading "1"	–	–	2.6	mA
Logic Loading "0"	–	–	24	mA
EOC Output Logic Levels:				
Logic "1"	+ 2.4	–	+ 5.5	Volts
Logic "0"	0	–	+ 0.4	Volts
Logic Loading "1"	–	–	2.5	mA
Logic Loading "0"	–	–		mA
PERFORMANCE				
Conversion Rate	20	–	–	MHz
Non-Linearity	–	–	±1/2	LSB
Differential Non-Linearity	–	–	±1/2	LSB
Differential Gain Error	–	1.5	–	%
Differential Phase Error	–	0.5	–	Degrees
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V Supply	+14.5	+15.0	+15.5	Volts
-15V Supply	-14.5	-15.0	-15.5	Volts
+5V Supply	+ 4.5	+ 5.0	+ 5.5	Volts
Power Supply Current:				
+15V Supply	–	–	+65	mA
-15V Supply	–	–	-140	mA
+5V Supply	–	–	+200	mA
PHYSICAL-ENVIRONMENTAL				
Operating Temperature Range	0	–	+70	°C
Storage Temperature Range	-25	–	+85	°C
Mechanical Dimensions	3.93″(W) × 6.3″(D) × 0.55″(H) 100(W) × 160(D) × 14(H) mm			
Weight	0.308 Lbs. (140 Grams)			

As a stand-alone analog-to-digital converter board, the wide 8 MHz input bandwidth makes the ADC-B304E adaptable to many advanced design-in applications.

The ADC-B304E sampling A/D board provides true 8-bit accuracy across the entire 8 MHz input bandwidth. Video signal digitization, radar signal processing, and transient signal analysis are ideal applications for this wide-bandwidth, highly-accurate front-end board.

The ADC-B304E sampling A/D board also makes an ideal test fixture for incoming inspection and component qualification.

The ADC-B304E performs A/D conversions at sampling rates up to 20 MHz. Using a four-layer printed circuit board and high frequency noise filtering assures perfect conversions free from noise problems. Linearity error and differential linearity error are guaranteed to be less than one half LSB.

TECHNICAL NOTES

Refer to the ADC-B304E's Block Diagram (Figure 1) and Schematic Drawing (Figure 2) for further information.

1. The on-board ±15V dc analog power grounds and the +5V dc digital power grounds are joined at a point labeled J1 on the board. DATEL does not recommend having this common ground outside the board, otherwise noise problems may result from ground loops. If it is required to have a common point outside the board, cut the etch between the J1 pins. In every case, avoid creating different potentials between the digital and analog grounds on the board.
2. Supply the analog input signal to the coaxial cable input terminal labeled AIN. This input signal can be also supplied via the DIN connector. In this case, connect two sets of feedthrough holes labeled "SIG" in Figure 4 with a short coaxial cable and then supply the signal to the A28 (ANA IN) and B28 (SIG GND) terminals. The short coaxial cable should have a characteristic impedance matching the ADC-B304E's input impedance.

   Analog input impedance matching of 50 or 75 ohms is available. As shipped from the factory, the ADC-B304E has an input impedance of 50 ohms. A jumper wire in resistor R1's mounting feedthrough holes selects this value. Replacing the jumper wire with a 24 ohm resistor provides an input impedance of 75 ohms. Refer to the Functional Specifications section for more information.

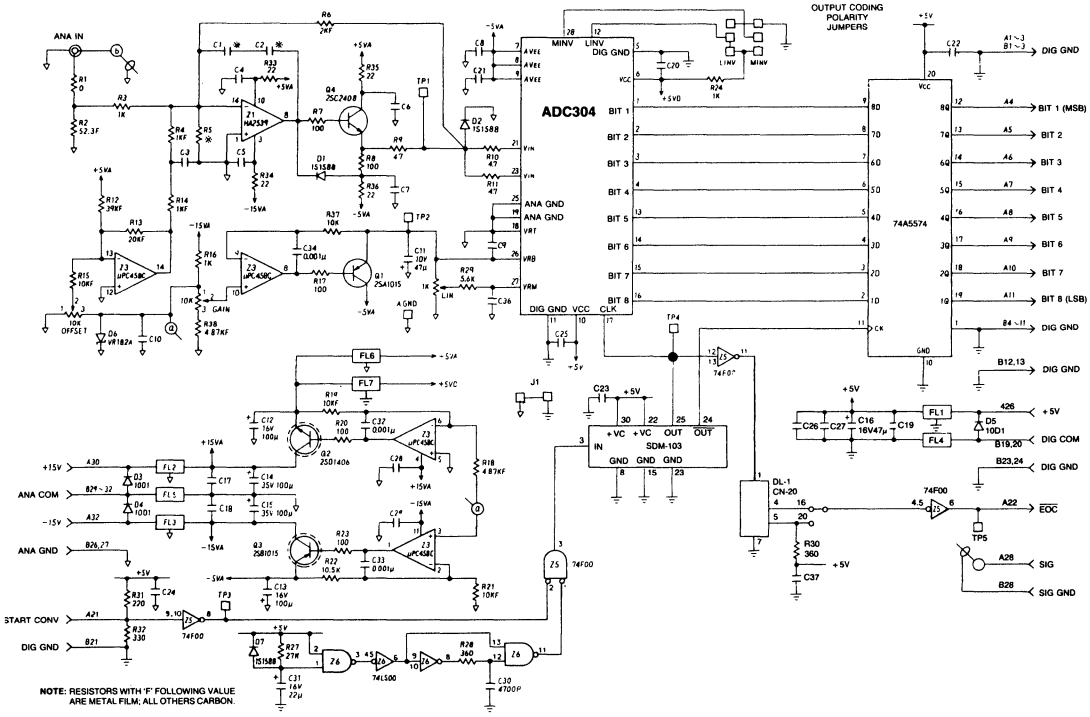


Figure 2. ADC-B304E Schematic Diagram

TECHNICAL NOTES (cont.)

3. Output digital data is obtained at the falling edge of $\overline{EOC}$. Refer to the timing diagram of the ADC-B304E.
4. Digital input and output signals are all TTL-compatible. The START CONVERT pulse width should be a minimum of 15 nanoseconds and Ts-15 nanoseconds maximum. Ts is the sampling period. The START CONVERT pulse should also be supplied through a buffer such as the 74LS240.

Table 1. ADC-B304E Pin Connections

FUNCTION	PIN	PIN	FUNCTION
DIG GND	A1	B1	DIG GND
DIG GND	A2	B2	DIG GND
DIG GND	A3	B3	DIG GND
BIT 1 (MSB)	A4	B4	DIG GND
BIT 2	A5	B5	DIG GND
BIT 3	A6	B6	DIG GND
BIT 4	A7	B7	DIG GND
BIT 5	A8	B8	DIG GND
BIT 6	A9	B9	DIG GND
BIT 7	A10	B10	DIG GND
BIT 8 (LSB)	A11	B11	DIG GND
NC	A12	B12	DIG GND
NC	A13	B13	DIG GND
NC	A14	B14	NC
NC	A15	B15	NC
NC	A16	B16	NC
NC	A17	B17	NC
NC	A18	B18	NC
NC	A19	B19	DIG COM
NC	A20	B20	DIG COM
START CONVERT	A21	B21	DIG GND
$\overline{EOC}$	A22	B22	NC
NC	A23	B23	DIG GND
NC	A24	B24	DIG GND
NC	A25	B25	NC
+5V	A26	B26	ANA GND
NC	A27	B27	ANA GND
ANA IN	A28	B28	SIG GND
NC	A29	B29	ANA COM
+15V	A30	B30	ANA COM
NC	A31	B31	ANA COM
−15V	A32	B32	ANA COM

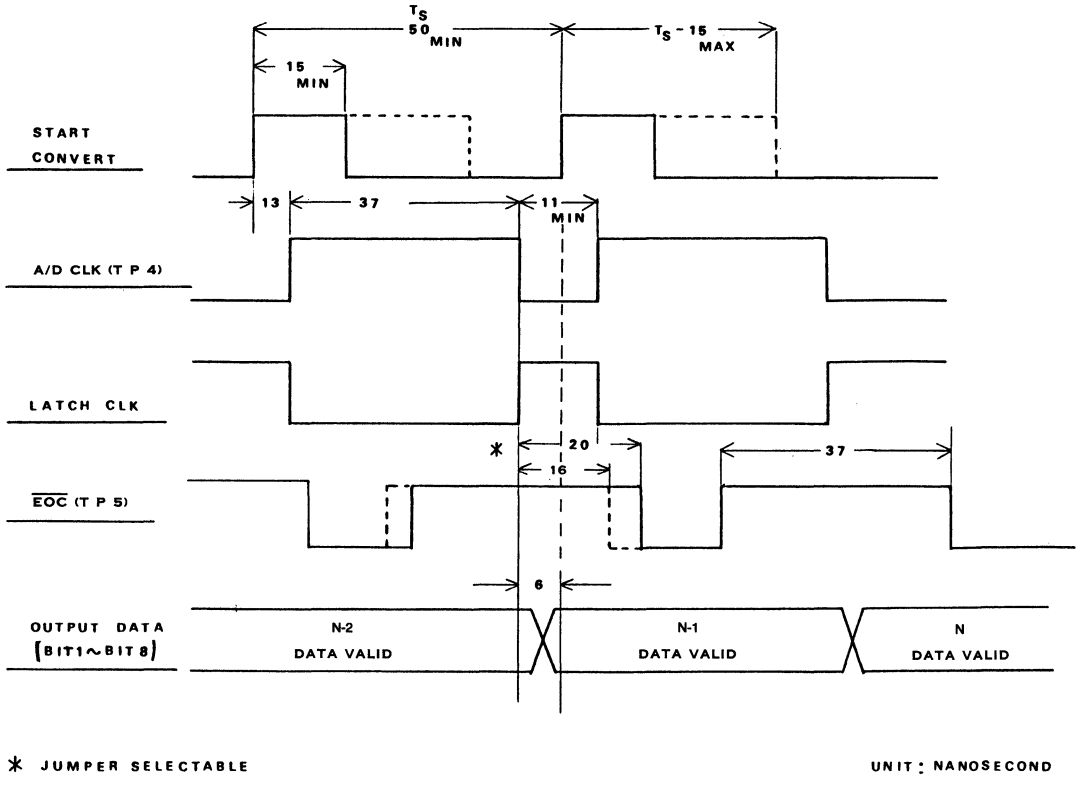


Figure 3. ADC-B304E Timing Diagram

THEORY OF OPERATION

The ADC-B304E is a fully functional sampling A/D board with on-board offset, gain, and linearity adjustments. The buffered analog input provides for 0 to + 1V and ±0.5V full scale input ranges. The ADC-B304E also contains regulated on-board power supplies to assure stable operation. Refer to the block diagram and timing diagram as needed.

Figure 3 shows the timing relationships between the START CONVERT pulse, clocks, $\overline{EOC}$, and the output data.

The START CONVERT pulse must be at least 15 nanoseconds long and can be no longer than the sampling period minus 15 nanoseconds. The rising edge of the START CONVERT pulse generates an internal clock command to the ADC-304. This A/D clock typically goes high after a delay of 13 nanoseconds. This signal causes the ADC-304's comparators to latch the comparison between the internal reference ladder taps and the input voltage.

NOTE

In the following discussion, the present conversion, and its associated data, is called the 'N conversion' while the previous conversion is called the 'N-1 conversion'.

During the time the clock to the ADC-304 is high, the N-1 conversion is latched at the output of the ADC-304. The output latch of the ADC-B304E is enabled while this internal A/D clock pulse is high, allowing the N-1 conversion to become present at the output of the ADC-B304E. The internal A/D clock is typically high for 37 nanoseconds.

When the internal A/D clock pulse goes low, the N-1 conversion is now latched at the output of the ADC-B304E. The N conversion now becomes available at the output of the ADC-304. This N conversion becomes available at the output of the ADC-B304E upon the next START CONVERT (and consequently A/D clock going high), and becomes latched on the next A/D clock low cycle. Upon the A/D clock pulse going low, the comparators of the ADC-304 go back into the sampling mode in preparation for the next conversion.

Output data becomes valid typically 6 nanoseconds after the A/D clock goes low and stays valid for the duration of the A/D clock pulse. The $\overline{EOC}$ signal, when low, indicates that the data at the output of the ADC-B304E is valid. $\overline{EOC}$ goes low 20 nanoseconds after the A/D clock goes low to assure data stability. The 20 nanosecond delay (factory setting) can be jumper-selectable to 16 nanoseconds if shorter set-up time requirements of external gates allow.

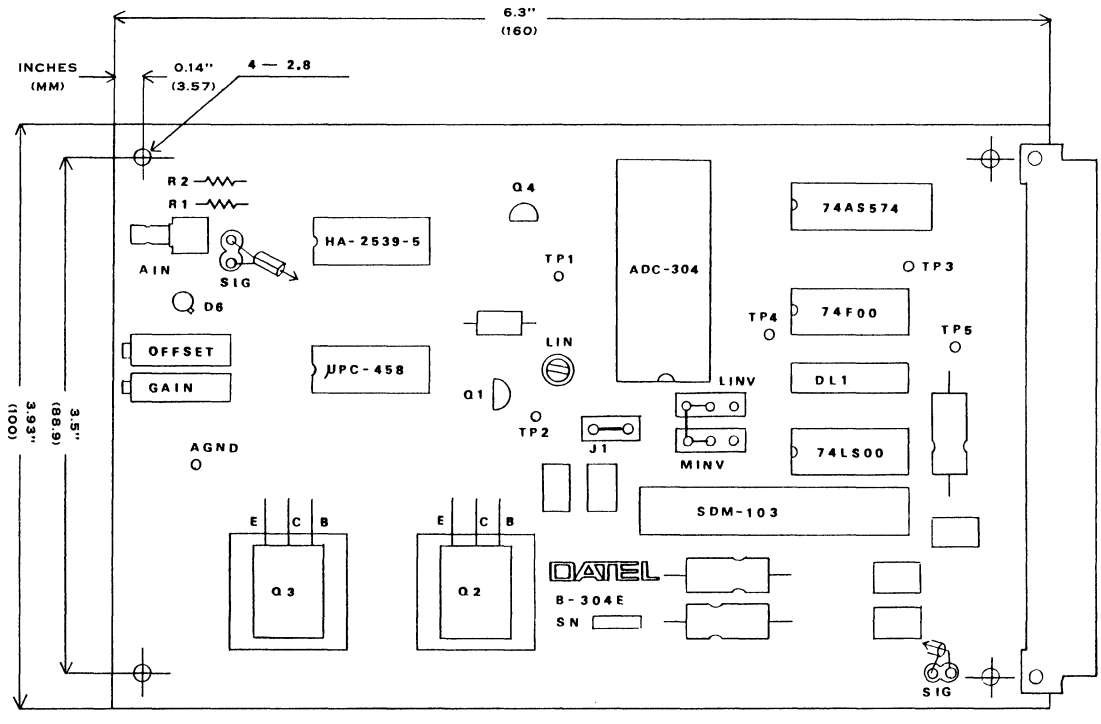


Figure 4. ADC-B304E Component Layout Drawing

CALIBRATION

There are three trimpots on the board labeled "Offset," "Gain" and "LIN." The following information describes the functions of each of these trimpots.

1. Offset Adjust

   The analog signal voltage range is adjusted to ±0.5V dc at the time of shipment from the factory. The input voltage amplitude to the ADC-B304E is always 1V peak-to-peak. The offset range can be adjusted between −2.3V and +2.3V. To measure this offset voltage, connect the two leads of a high-impedance digital multimeter to test point TP1 and ANA GND.

   Unipolar Operation

   Adjust the Offset trimpot with +1.953 mV (+1/2 LSB) applied to ANA IN (pin A28) so that the straight binary output code flickers between 0000 0000 and 0000 0001.

   Bipolar Operation

   Adjust the Offset trimpot with −498.05 mV (−FS + 1/2 LSB) applied to AIN IN (pin A28) so that the offset binary output code flickers between 0000 0000 and 0000 0001.

2. Gain Adjust

   This trimmer adjusts the −2V reference voltage required for the ADC-304. Vary this trimpot with +FS − 1-1/2 LSB applied to ANA IN (pin A28). This value should be +0.9941V for unipolar operation or +0.4941V for bipolar operation. Adjust the trimpot so that the straight or offset binary output code flickers between 1111 1110 and 1111 1111.

3. Linearity Trimmer

   This trimpot fine tunes the linearity of the board. Connect a high-impedance digital multimeter to test point TP2 and ANA GND (pins B26 or B27) and measure the reference voltage. Reconnect the multimeter to Pin 27 (VRM) of the ADC-304 and ANA GND (pins B26 or B27) and adjust the "LIN" trimpot to one-half (1/2) of the reference voltage measured on TP2.

To confirm the operation of the ADC-B304E, vary the input voltage with a precise reference voltage source to obtain the output coding listed in Table 2. Repeat the previous steps, if necessary, to achieve the desired operation of the ADC-B304E.

The following Test Points are available to the user of the ADC-B304E. Refer to Figure 4 for the exact location of these test points on the board.

TEST POINT	DESCRIPTION
TP1	Buffered, Offset, Analog Input Voltage
TP2	Reference Voltage
TP3	Start Convert Pulse
TP4	A/D Clock Input
TP5	$\overline{EOC}$

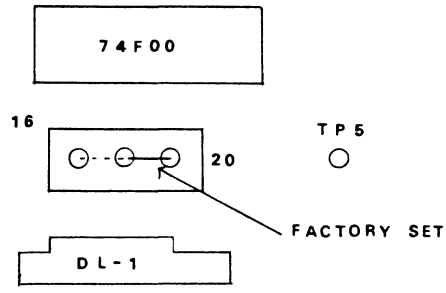


Figure 5. $\overline{EOC}$ Selection

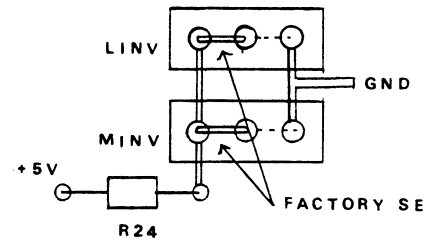


Figure 6. Output Inversion Control Pins

OUTPUT CODING

Digital output coding is factory-set to positive true offset binary coding. There are LINV and MINV etch pads on the board. These are used to change the output code to 2's complement or negative true logic. These points connect to +5V through a 1K ohm pull-up resistor on the board, making these points a "logic 1."

To obtain a "logic 0" on either or both of these points, short the selected point to ground with a jumper(s). Refer to Table 2 and Figure 6 for coding information and "LINV/MINV Selection." Figure 4 shows the locations of these jumpers and etch.

Table 2. Output Coding for Unipolar and Bipolar Operation

UNIPOLAR OPERATION			STRAIGHT BINARY	COMP. BINARY	2's COMP.	COMP. 2's COMP.
UNIPOLAR SCALE	INPUT VOLTAGE	MINV LINV	1 1	0 0	0 1	1 0
+ FS - 1 LSB	+ 996.1 mV		11111111	00000000	01111111	10000000
+ 7/8 FS	+ 875 mV		11100000	00011111	00100000	11011111
+ 3/4 FS	+ 750 mV		11000000	00111111	01000000	10111111
+ 1/2 FS	+ 500 mV		10000000	01111111	00000000	11111111
+ 1/4 FS	+ 250 mV		01000000	10111111	11000000	00111111
+ 1/8 FS	+ 125 mV		00100000	11011111	10100000	01011111
+ 1 LSB	+3.906 mV		00000001	11111110	10000001	01111110
0	0 mV		00000000	11111111	10000000	01111111
BIPOLAR OPERATION			**OFFSET BINARY**	**COMP. OFFSET BINARY**	**2's COMP.**	**COMP. 2's COMP.**
BIPOLAR SCALE	INPUT VOLTAGE	MINV LINV	1 1	0 0	0 1	1 0
+ FS - 1 LSB	+ 496.1 mV		11111111	00000000	01111111	10000000
+ 3/4 FS	+ 375 mV		11100000	00011111	01100000	10111111
+ 1/2 FS	+ 250 mV		11000000	00111111	01000000	10111111
+ 0	0 mV		10000000	01111111	00000000	11111111
- 1/2 FS	- 250 mV		01000000	10111111	11000000	00111111
- 3/4 FS	- 375 mV		00100000	11011111	10100000	01011111
- FS+1 LSB	- 496.1 mV		00000001	11111110	10000001	01111110
- FS	- 500 mV		00000000	11111111	10000000	01111111

NOTES: MINV is the output control pin for data bit 1 (MSB).
LINV controls output data bits 2 through 8.

ORDERING INFORMATION	
ADC-B304E	ADC-304 Sampling A/D Board

ADC-B310E
10-BIT, 12 MHz
SAMPLING A/D BOARD

FEATURES

- **10-Bit resolution**
- **12 MHz sampling rate**
- **10 MHz input bandwidth**
- **TTL logic compatible**
- **Eurocard size, DIN connector**

APPLICATIONS

- **Video signal processing**
- **High-speed voice signal analysis**
- **Radar systems**
- **Transient analysis**
- **Atomic energy-related instrument control**

DATEL's ADC-B310E is a 10-bit, 12 MHz sampling A/D board, offering an input bandwidth of dc to 10 MHz. The ADC-B310E eliminates the need for custom test equipment when evaluating DATEL's ADC-310 flash converter.

GENERAL DESCRIPTION

The ADC-B310E is a complete sampling A/D conversion board designed around DATEL's ADC-310 flash converter. The ADC-B310E is functionally complete containing a sample-hold amplifier, offset and gain adjustments, filtering and timing circuitry.

DATEL designed the ADC-B310E with two purposes in mind; first, as a self-supporting, high-speed sampling analog-to-digital converter board. Secondly, as a means of evaluating DATEL's ADC-310 flash converter. The ADC-B310E also makes an ideal test fixture for incoming inspection and component evaluation.

DATEL's design takes into consideration crucial factors such as board layout, impedance matching, input buffering, filtering and timing.

The ADC-B310E performs A/D conversions at sampling rates up to 12 MHz. Using a four-layer printed circuit board and high frequency noise filtering techniques permits perfect conversions, free of noise problems.

Video signal digitizing, radar signal processing, and transient signal analysis are ideal applications for this wide-bandwidth, highly-accurate front-end board.

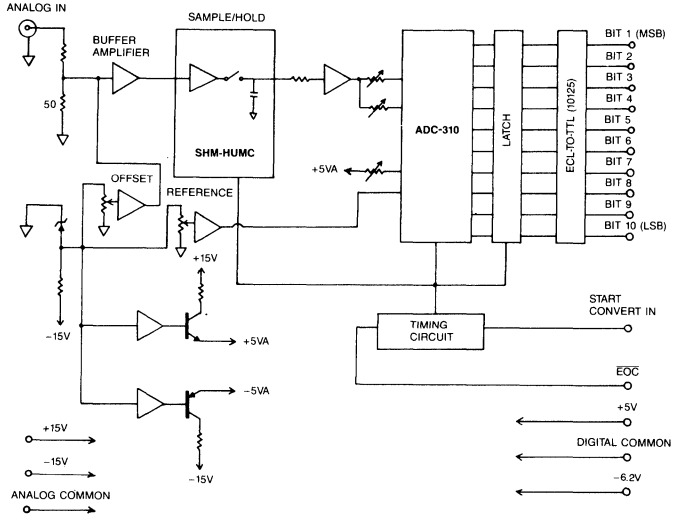


Figure 1. ADC-B310E Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltages:	
+15V Supply (Pin A30)	+17V dc
−15V Supply (Pin A32)	−17V dc
−5.2V Supply (Pins A18, B18)	−7V dc
+5.2V Supply (Pin A26)	+7V dc
Clock Pulse Input Voltage (Pin A21)	+7V dc
Analog Input Voltage (Pin A28)	±2.5V dc

FUNCTIONAL SPECIFICATIONS
Typical at 25°C, ±15V, −5.2V, +5V dc power unless otherwise specified.

	MIN.	TYP.	MAX.	UNITS
ANALOG INPUTS				
Analog Input Range		0 to +1 ±0.5		Volts Volts
Input Impedance				
R54 = 0 Ω (standard)	–	50	–	Ohms
R54 = 24 Ω (user supplied)	–	75	–	Ohms
Input Signal Bandwidth	–	10	–	MHz
DIGITAL INPUTS				
Digital Input (START CONVERT)				
Logic "1"	+2	–	+5.5	V dc
Logic "0"	0	–	+0.8	V dc
Logic Loading "1"	–	–	40	μA
Logic Loading "0"	–	–	1.6	mA
OUTPUTS				
Resolution	8	–	–	Bits
EOC, Data Outputs				
Logic "1"	+2.4	–	+5.5	V dc
Logic "0"	0	–	+0.4	V dc
Logic Loading "1"	–	–	0.4	mA
Logic loading "0"	–	–	16	mA
PERFORMANCE				
Resolution	10	–	–	Bits
Convert Pulse Width	25	–	–	nSec.
Conversion Rate	12	–	–	MHz
Non-Linearity	–	–	±1.75	LSB
Differential Non-Linearity	–	–	±1.75	LSB
Warm-Up Time for Stable Operation	–	15	–	Minutes
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V Supply	+14.5	+15.0	+15.5	V dc
−15V Supply	−14.5	−15.0	−15.5	V dc
−5.2V Supply	−4.7	−5.2	−5.7	V dc
+5V Supply	+4.5	+5.0	+5.5	V dc
Power Supply Current:				
+15V Supply	–	+140	–	mA
−15V Supply	–	−210	–	mA
−5.2V Supply	–	−500	–	mA
+5V Supply	–	+140	–	mA
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range	0	–	+70	°C
Storage Temp. Range	−25	–	+85	°C
Mechanical Dimensions	3.93"(W) × 6.3"(D) × 0.67"(H) 100(W) × 160(D) × 17(H)mm Eurocard Size			
Weight	0.4 Lbs. (175 Grams)			

As a design tool, the board relieves the design engineer of the labor-and-time-intensive task of constructing an evaluation cir-cuit to test the applicability of the ADC-310 flash converter in their design. The board allows fast hook-up and prototype evaluation, shortening the design cycle.

TECHNICAL NOTES

Refer to the Simplified Block Diagram and the Schematic Diagram for further information. Also refer to Table 1 for complete signal pinout information.

1. The ± 15V dc analog power supply commons labeled "ANA COM" and the +5V, −5.2V dc digital power supply commons labeled "DIG COM" are grounded to one point at J1 on the board. DATEL does not recommend having this common ground outside the board; noise problems may result from ground loops.

   If it is, however, required to have a common point outside the board, cut the etch to J1. In this case, avoid creating different potentials between digital and analog grounds on the board. Points labeled "DIG GND" on the ADC-B310E board are used for the digital signal grounds. Likewise, points labeled "ANA GND" refer to the analog circuitry grounds.

2. Supply the analog input signal to the coaxial cable input terminal (AIN). This input signal can be also applied via the DIN connector. In this case, connect the two sets of feedthrough holes labeled "SIG" in Figure 4 with a short coaxial cable and then supply the signal to the A28 (ANA IN) and B28 (SIG GND) terminals.

   The short coax cable should be of the same characteristic impedance as the input of the ADC-B310E. Refer to "INPUTS" of the Functional Specifications section for more information.

3. Some components on the board operate at high temperatures. The ADC-310 operates at 60°C when the board is at room temperature. DATEL recommends using the board in a free air circulation environment.

4. There are several test points (TP1 through TP8) for checking the performance of the board. When using these test points, only use high-impedance test probes to check the signals.

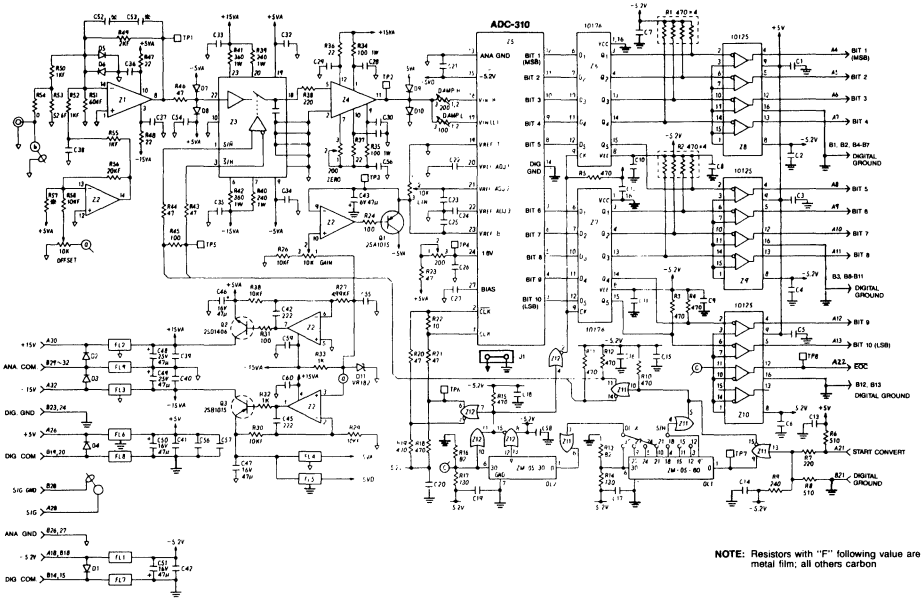


Figure 2. ADC-B310E Schematic Diagram

Performance of the board deteriorates if large external loads are applied to these points. The following signals are present on the indicated test points:

TEST POINT	SIGNAL
TP1	Analog input signal before the S/H with offset adjustment.
TP2	Analog input signal to the ADC-310
TP3	Vref B
TP4	Vcc
TP5	S/$\overline{H}$ Signal
TP6	Clock to the ADC-310
TP7	START CONVERT pulse
TP8	$\overline{EOC}$ Signal

Digital input and output signals are TTL-compatible. The width of the START CONVERT pulse should be a minimum of 25 nanoseconds and should be supplied through a buffer such as a 74LS240. Logic circuits on the board are driven by the rising edge of the START CONVERT pulse.

5. The ADC-B310E's design allows it to convert analog input signals from dc up to 10 MHz. A capacitor in the feedback loop of the buffer amplifier regulates this analog input signal bandwidth.

Table 1. ADC-B310E Pin Connections

FUNCTION	PIN	PIN	FUNCTION
DIG GND	A1	B1	DIG GND
DIG GND	A2	B2	DIG GND
DIG GND	A3	B3	DIG GND
BIT 1 (MSB)	A4	B4	DIG GND
BIT 2	A5	B5	DIG GND
BIT 3	A6	B6	DIG GND
BIT 4	A7	B7	DIG GND
BIT 5	A8	B8	DIG GND
BIT 6	A9	B9	DIG GND
BIT 7	A10	B10	DIG GND
BIT 8	A11	B11	DIG GND
BIT 9	A12	B12	DIG GND
BIT 10 (LSB)	A13	B13	DIG GND
NC	A14	B14	DIG COM
NC	A15	B15	DIG COM
NC	A16	B16	NC
NC	A17	B17	NC
−5.2V	A18	B18	−5.2V
NC	A19	B19	DIG COM
NC	A20	B20	DIG COM
START CONVERT	A21	B21	DIG GND
$\overline{EOC}$	A22	B22	DIG GND
NC	A23	B23	DIG GND
NC	A24	B24	DIG GND
NC	A25	B25	NC
+5V	A26	B26	ANA GND
NC	A27	B27	ANA GND
ANA IN	A28	B28	SIG GND
NC	A29	B29	ANA COM
+15V	A30	B30	ANA COM
NC	A31	B31	ANA COM
−15V	A32	B32	ANA COM

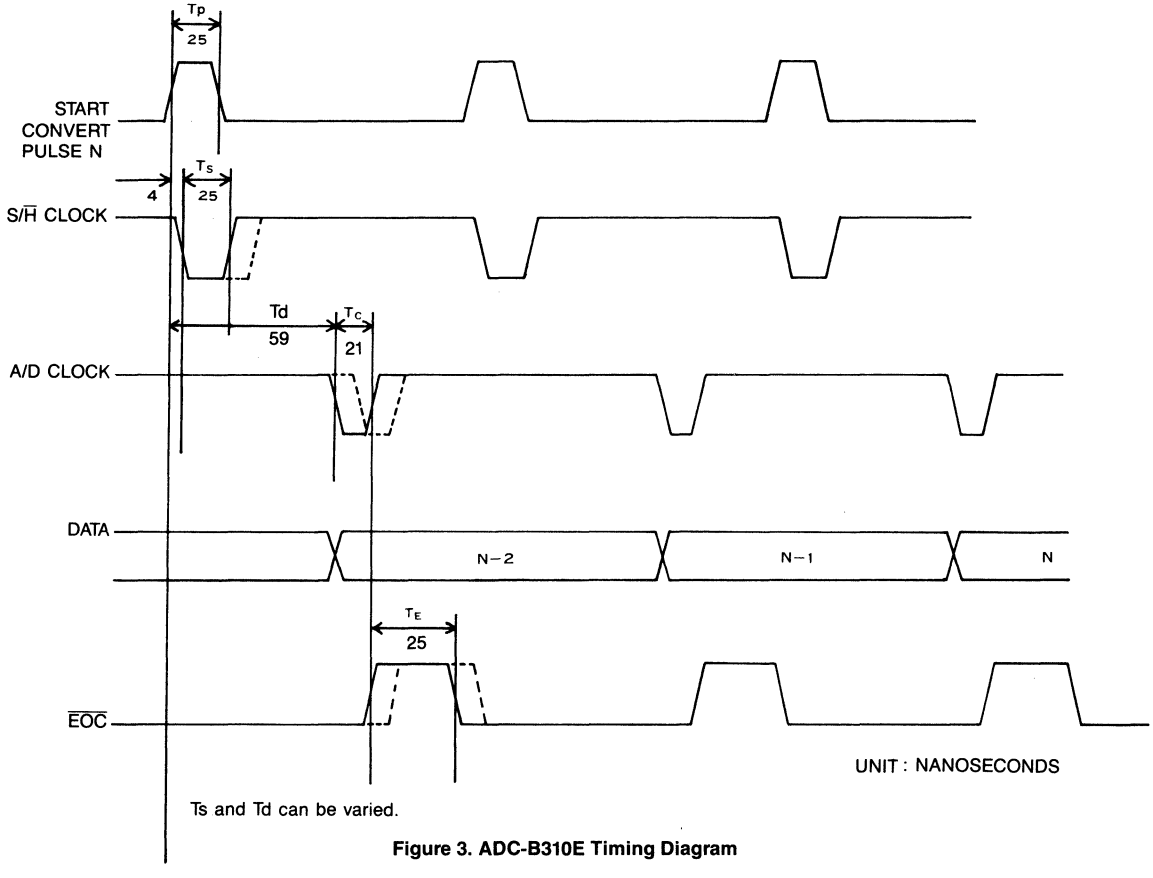


Figure 3. ADC-B310E Timing Diagram

THEORY OF OPERATION

The following describes the operation of the ADC-B310E Sampling A/D board as configured from the factory. Refer to the ADC-B310E schematic diagram (Figure 2) and timing diagram (Figure 3) as needed.

The ADC-B310E receives the analog input signal through either the board-edge pin (pin A28) or the coaxial analog input connector (refer to Technical Note 2). The signal is offset adjusted and sent to the sample-and-hold amplifier. The next START CONVERT pulse "locks-in" the sampled signal to the gain-compensated amplifier.

There are two resistors connected between this amplifier output and the input to the ADC-310. These resistors are adjustable and designed to prevent parasitic oscillations. There are two on-board power supplies/regulators providing the voltages necessary for stable operation of the ADC-310 and its supporting circuitry.

The ADC-310 analog-to-digital conversion is done in two steps. The ADC-310 contains two 5-bit flash A/D's consisting of comparators. These two stages are done sequentially. The analog input to the ADC-310 must be stable throughout the conversion, a requirement satisfied by the on-board sample-and-hold (S/H) device.

The rising edge of the START CONVERT pulse (for conversion N), changes the S/H device from the hold mode into the sample (or acquisition) mode. The acquisition mode lasts for 25 nanoseconds (factory setting) and is determined by the internal gate delays and delay line 1 (DL1). To lengthen the acquisition time, vary the setting of DL1 (see Figure 5).

Upon going into the hold mode, a delay time occurs, allowing the signal to settle at the output buffer of the S/H. This delay is approximately 37 nanoseconds, determined by the internal gate delays as well as DL1 and DL2. DL1 can be varied per Figure 5 to lengthen the duration of the hold mode.

Upon the internal clock pin going low (Pin 1 of the ADC-310), the internal comparators of the ADC-310 latch the analog input. When the CLK goes high, the previous conversion, N-1, is present at the 10176 output latch of the ADC-310. The N-2 data is now available at the output of the 10125 buffer, thus at the output of the ADC-B310E.

Data from conversion "N" will become available at the output of the ADC-B310E after three START CONVERT pulses have been issued. An $\overline{EOC}$ signal is given after the START CONVERT pulse for conversion "N" is given, indicating data from conversion "N-2" is now valid to be read.

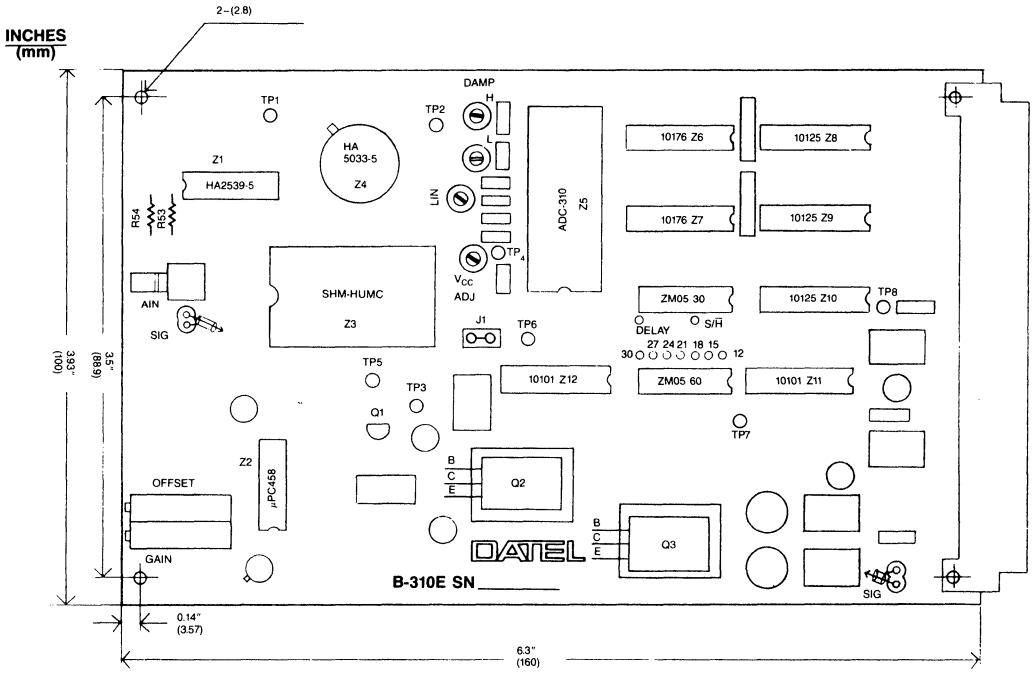


Figure 4. ADC-B310E Component Layout Diagram

CALIBRATION

Following are descriptions of the six trimpots on the ADC-B310E board. All of the six trimpots are adjusted for optimum performance at the time of shipment. Should adjustment be required, use the following procedures. Refer to Figure 4 for the locations of these components.

Vcc Trimmer

It is necessary to supply +1.6V to the Vcc pin of the ADC-310. This supply voltage is generated from a +5V regulator (+5 VA) on the ADC-B310E board and adjusted by the trimpot labeled "VCC ADJ". Connect a high-impedance digital multimeter to test point TP4 and adjust the VCC trimpot for +1.600V.

Adjust this trimpot correctly since the overall linearity of the device is sensitive to this adjustment. Repeat this adjustment whenever replacing the ADC-310 on the ADC-B310E Sampling A/D board.

Offset Trimmer

Using this trimpot allows an offset range adjustment between −2.4V to +2.4V dc.

1. Unipolar Operation
   Adjust the Offset trimpot with +0.4883 mV (+½ LSB) applied to ANA IN so the straight binary output code flickers between 0000 0000 00 and 0000 0000 01.
2. Bipolar Operation
   Adjust the Offset trimpot with −499.51 mV (−FS +½ LSB) applied to ANA IN so the offset binary output code flickers between 0000 0000 00 and 0000 0000 01.

Gain Trimmer

This trimmer adjusts the −2V reference voltage required for the ADC-310. Adjust the Gain adjust trimpot with +FS−1½ LSB applied to ANA IN (+0.99853V for Unipolar or +0.49853V for Bipolar operation) so that the straight or offset binary output code flickers between 1111 1111 10 and 1111 1111 11.

Linearity Trimmer

This trimpot fine tunes the linearity of the board. Connect a high-impedance digital multimeter to test point TP3 and ANA GND and measure this voltage. Reconnect the multimeter to pin 21 (VREF ADJ 2) of the ADC-310 and ANA GND, and adjust the Linearity trimpot to one half (½) of the voltage indicated on test point TP3.

Damping Trimmers "DAMP H" and "DAMP L"

The differential linearity of the board is sensitive to the frequency of the analog input signal. At the time of shipment, the differential linearity of the board is fine tuned under conditions of Vin = ±0.5V, Fin = 5 MHz and Fs = 10 MHz using the envelope method. When the differential linearity is suspect, use these two trimmers to re-adjust the differential linearity.

Differential linearity is most sensitive to changes in the setting of the DAMP L potentiometer. Adjust the DAMP L potentiometer first without moving DAMP H.

The value of DAMP H will be around zero ohms at the time of shipment. When the differential linearity is not adjustable with DAMP L, increase the value of DAMP H by a small amount and then adjust the differential linearity with DAMP L. Repeat these two adjustments until proper operation is attained. When the values of DAMP H and DAMP L are varied, gain error is introduced into the ADC-B310E. It will be necessary to adjust the gain at this time.

To confirm the operation of the ADC-B310E, vary the input voltage with a precision reference voltage source to obtain the output coding listed in Tables 2 and 3. Repeat the previous steps if necessary to achieve the desired operation of the ADC-B310E.

Table 2. Unipolar Output Coding

UNIPOLAR SCALE	INPUT VOLTAGE	STRAIGHT BINARY
0	+0.0000 V	0000 0000 00
+1 LSB	+0.9766 mV	0000 0000 01
+¼ FS	+250 mV	0100 0000 00
+⅜ FS	+375 mV	0110 0000 00
+½ FS	+500 mV	1000 0000 00
+¾ FS	+750 mV	1100 0000 00
+⅞ FS	+875 mV	1110 0000 00
+FS – 1 LSB	+999.02 mV	1111 1111 11

Table 3. Bipolar Output Coding

BIPOLAR INPUT SCALE	INPUT VOLTAGE	OFFSET BINARY
– FS	–500 mV	0000 0000 00
– FS +1 LSB	–499.02 mV	0000 0000 01
–¾ FS	–375 mV	0110 0000 00
–½ FS	–250 mV	0100 0000 00
+0	+0 mV	1000 0000 00
+½ FS	+250 mV	1100 0000 00
+¾ FS	+375 mV	1110 0000 00
+FS – 1 LSB	+499.02 mV	1111 1111 11

TIMING SETTING

1. There are feedthrough holes labeled as "12, 15,...30" close to the DL1 delay line component and two more holes labeled as "DELAY" and "S/H" close to these holes. Refer to Figure 5 for the specific locations of these holes.
2. At the time of shipment from the factory, DELAY is connected to 21 yielding a Td of 42 nanoseconds and S/$\overline{H}$ is connected to Tap 9 of DL1 yielding a Ts of 18 nanoseconds.
3. Delay time increases by 6 nanoseconds by connecting to a higher order tap. For example, Td is increased from 42 to 48 nanoseconds by changing the DELAY jumper wire connection from tap 21 to 24. Likewise, Ts increases from 18 nanoseconds to 24 nanoseconds once the jumper wire connection is changed from tap 9 of DL1 to tap 12.

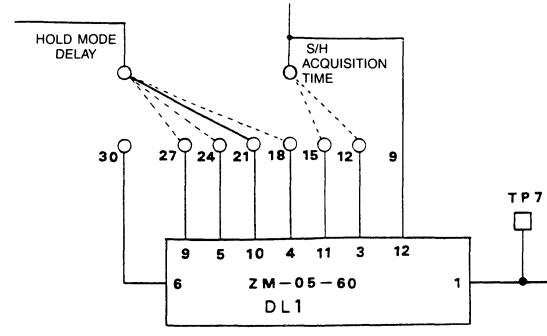


Figure 5. S/$\overline{H}$ and Delay Selection Settings

The time delays for DL1 are listed in the following table:

ACQUISITION MODE TIME SETTING

TAP	S/H SETTING (Ts)
15	30 nSec.
12	24 nSec.
9	18 nSec. "S/H" (Factory Setting)

HOLD MODE SETTLING TIME DELAY

TAP	TIME DELAY (Td)
30	60 nSec.
27	54 nSec.
24	48 nSec.
21	42 nSec. "Delay" (Factory Setting)
18	36 nSec.

TIMING CHANGE

It is possible to change the timing relation of S/H CLK and ADC CLK. If the analog input signal frequency is lower than 100 KHz or it is not necessary to obtain ±1.75 LSB bit accuracy, then the conversion rate can be increased to a value greater than 12 MHZ. The values of Ts and Td depend on the jumper setting of delay line DL1 on the board.

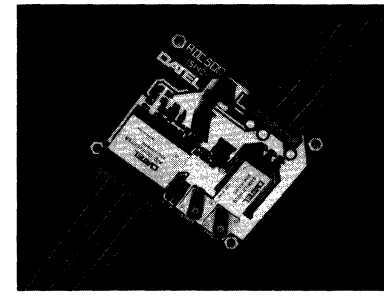
ORDERING INFORMATION	
ADC-B310E	**ADC-310 Sampling A/D Board**

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-B500, ADC-B505
HIGH-SPEED A/D-SHM EVALUATION BOARDS

FEATURES

- 12-Bit, 1.25 MHz/1.1 MHz conversion rates
- Includes ADC-500/505MC
- Includes SHM-45MC
- Jumper-plug selectable input ranges
- On-board offset and gain adjustments
- On-board −5V supply
- BNC connectors for start convert/analog inputs
- Connectors provided with 2 foot flat ribbon cables using interwoven grounds.



DESIGNED FOR PERFORMANCE EVALUATION OF DATEL'S ADC-500/505 AND SHM-45, THE ADC-B500 AND ADC-B505 EVALUATION BOARDS ARE COMPLETE 12-BIT A/D SYSTEMS WITH 1.25 MHz AND 1.1 MHz CONVERSION RATES RESPECTIVELY.

GENERAL DESCRIPTION

DATEL offers three models of its ADC-B500 Series high-speed evaluation boards. The ADC-B500 includes the ADC-500BMC and SHM-45MC while the ADC-B505 includes the ADC-505BMC and SHM-45MC. The final version offered is the ADC-B500-1 which is an evaluation board without the A/D and SHM hybrid converters. The ADC-B500-1 is usable as an incoming inspection test fixture. Additionally, users purchasing military temperature grades of the ADC-505 and SHM-45 would be able to evaluate these converters over the commercial temperature range using the ADC-B500-1 for initial system prototyping.

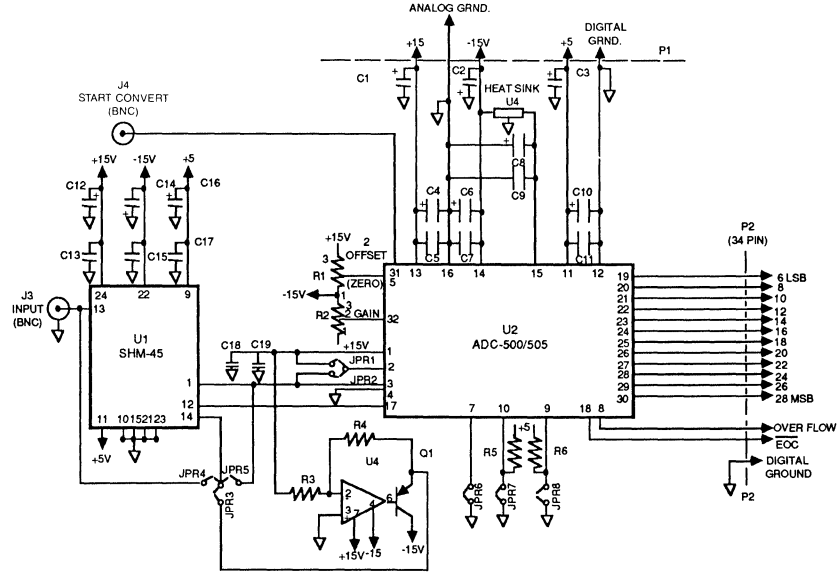


Figure 1. ADC-B500/B505 Evaluation Board Schematic

GENERAL DESCRIPTION (cont.)

The ADC-B500's conversion rate is 1.25 MHz while the ADC-B505 offers a 1.1 MHz conversion rate. The evaluation boards feature selection of six full scale input ranges: 0 to −5V, 0 to −10V, 0 to −20V, 0 to +10V, ±5V, and ±10Vdc. Jumper-plugs are used for ease of range selection.

The functionality of the evaluation boards includes adjustments for calibration of the offset and gain errors. A minus 5V supply required for the ADC-500/505 is generated by the evaluation boards to aid in quick prototype set-up. BNC inputs are provided for easy interface to start convert and analog input signal generators. Connectors for power supply and digital outputs are provided with 2 feet of flat ribbon cables for ease of use. The flat ribbon cables use interwoven grounds to assure good ground connections.

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the power supply range unless otherwise specified.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS		0 to −5 0 to −10		
Input Voltage Ranges	—	0 to +10	—	Volts dc
	—	0 to −20	—	Volts dc
	—	±10, ±5	—	Volts dc
Input, Impedance				
20V FSR	—	1K	—	ohm
10V FSR	—	1K	—	ohm
5V FSR	—	500	—	ohm
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	μA
Logic 0	—	—	−100	μA
OUTPUTS				
Output Coding:	straight binary/offset binary complementary binary complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	μA
Logic 0	—	—	6.4	mA
Internal Reference				
Voltage, +25°C	9.98	—	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
TRACK MODE DYNAMICS				
Frequency Response:				
Small Signal (−3dB)	—	16	—	MHz
Slew Rate	—	300	—	V/μS
TRACK TO HOLD SWITCHING				
Aperture Delay Time	—	6	—	nS
Aperture Uncertainty (Jitter)	—	±50	—	pS
Setting Time:				
10V to ±0.1% FS (±1 mV)	—	60	100	nS
10V to ±.1% FS (±10mV)	—	40	—	nS
HOLD TO TRACK DYNAMICS				
Acquisition Time:				
10V step to ±1.0mV (.01% FS)	—	160	200	nS
10V step to ±10mV (.1% FS)	—	100	170	nS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	MINIMUM	MAXIMUM	UNITS
+15V Supply	0	+18	Volts dc
−15V Supply	0	−18	Volts dc
+5V Supply	−0.5	+7	Volts dc
Digital Inputs	−0.3	+5.5	Volts dc
Analog Input	− 15	+ 15	Volts dc

FUNCTIONAL SPECIFICATIONS (cont.)

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
DYNAMIC PERFORMANCE				
Feedthrough Rejection	—	−74	—	dB
Signal to Noise Ratio (SNR)	−72	−80 below FS	—	dB
Inband Harmonics				
dc to 100KHz	−72	−80 below FS	—	dB
100KHz to 500KHz	−72	−75 below FS	—	dB
PERFORMANCE FOR ±10V RANGE				
Integral Nonlinearity:				
+25°C		±0.0125% FSR max		±½LSB
0°C to +70°C		±0.0125% FSR max		±½LSB
Integral Nonlin. Tempco	—	—	±3	ppm/°C
Differential Nonlinearity:				
+25°C		±0.0125% FSR	±½	LSB
0°C to +70°C		±0.0125% FSR	±½	LSB
Differential Nonlin. Tempco	—	—	±2	ppm/°C
Full-Scale Absol. Accuracy:				
+25°C	—	±5	±12	LSB
0°C to +70°C	—	±6	±15	LSB
Unipolar Zero Error, +25°C	—	±2	±5	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±5	LSB
Bipolar Offset Tempco	—	±13	±25	ppm/°C
Gain Error, +25°C	—	±3	±8	LSB
Gain Tempco	—	±18	±40	ppm/°C
Conversion Rate:				
ADC-B500:				
+25°C	1.25	1.5	—	MHz
0 to 70°C	1.20	—	—	MHz
ADC-B505:				
+25°C	1.19	—	—	MHz
0 to 70°C	1.14	—	—	MHz
No Missing Codes (12 Bits):	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
Power Supply Current:				
+15V Supply	—	—	+48	mA
−15V Supply	—	—	−325	mA
+5V Supply	—	—	+85	mA
Power Dissipation	—	—	*6.1	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range:				
ADC-B500	0	—	+70	°C
Storage Temperature Range	−55	—	+85	°C
Weight			6	oz.

*The ADC-500/505 and SHM-45 combined maximum power dissipation is 2.7W.

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

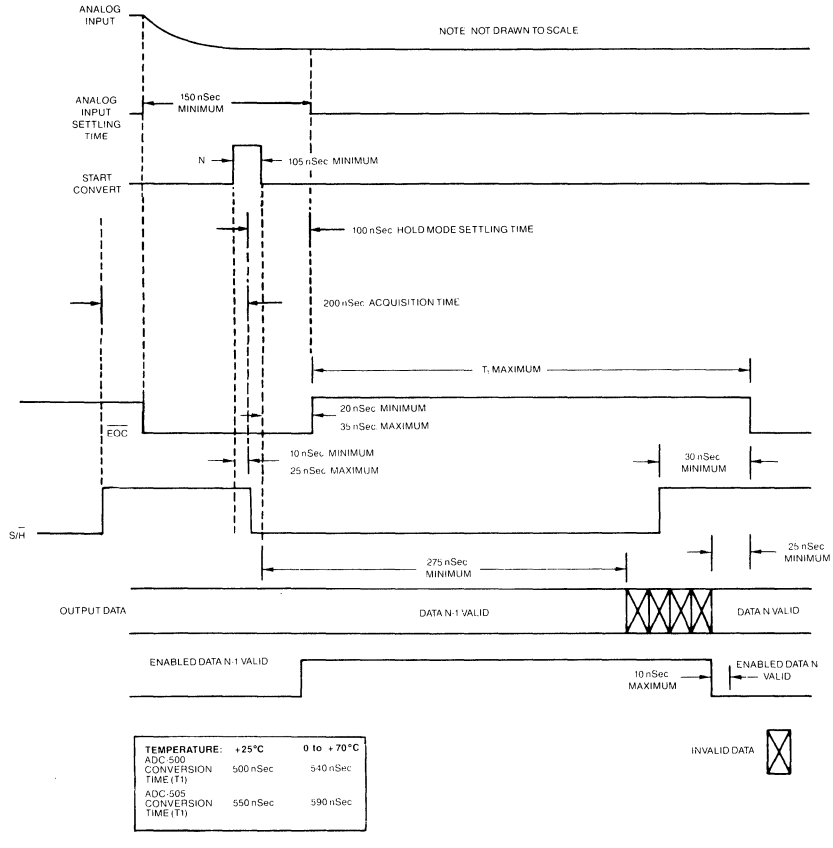


Figure 2. ADC-B500/B505 Evaluation Board Timing Diagram

THEORY OF OPERATION (ADC-B500)

The ADC-B500's operation is as follows. The sample and hold captures fast signals for the ADC to then digitize. Figure 1 shows the ADC-SHM schematic circuit. The ADC-500 used in the ADC-B500 employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the Timing Diagram shown in Figure 2 for further clarification.

The SHM-45 used in the ADC-B500 acquires the input signal on the internal hold capacitor (200 nanoseconds maximum acquisition time to 0.01%). The SHM-45 is then put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-500 requires a maximum of 150 nanoseconds since the previous conversion for the input signal to settle before initiating a conversion. The input of the ADC-500 starts settling to its final value while the SHM-45 is in the acquisition mode. The missing 50 nanoseconds of the required maximum analog input settling time is made up by the time the sample/hold is in the acquisition mode. Thus, the end of the SHM-45's hold mode settling time, the ADC-500's input is fully settled.

The SHM-45 is in the sample mode when the ADC-500's S/$\overline{H}$ control (Pin 17) is high. The S/H control pin is high and thus in the sample mode when the A/D is not performing a conversion.

The S/$\overline{H}$ control pin goes low after the rising edge of the start convert pulse a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. Thus to assure the SHM has 200 nSec maximum acquisition time, the start convert pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the start convert pulse should be 105 nsec minimum to assure the hold mode settling time of 100 nanoseconds is observed. The 105 nanoseconds takes into account the min-max propagation delays of the start convert high to S/$\overline{H}$ control low propagation delays and the start convert low to $\overline{EOC}$ high propagation delays.

The analog input, having been configured for the appropriate range, is buffered and then digitized by the 7 bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

THEORY OF OPERATION (cont.)

The first pass finished, internal switching occurs effectively subtracting the output of the DAC from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. EOC goes low, indicating the conversion is complete, and the output is present at the three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed (EOC going low). The internal Sample/Hold control signal line goes low a minimum of 30 nanoseconds before EOC goes low, indicating that the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the start convert pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before EOC goes low and valid up to 350 nanoseconds after the falling edge of the next start convert pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the evaluation board's output.

The overall throughput of the ADC-B500 using the ADC-500 and the SHM-45 internally consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds for observance of min-max propagation delays and 470 nanoseconds for the conversion process (S/H control pin saves 30 nanoseconds). Total throughput is a maximum of 785 nanoseconds for the system for a guaranteed throughput rate of 1.25 MHz. Retriggering of the start convert pulse before EOC goes low will not initiate a new A/D conversion.

Table 1. Performance Characteristics At Different Temperatures

CHARACTERISTICS	VALUE
Conversion Rate (Changing Inputs):	
ADC-B500:	
+25°C	1.25 MHz minimum
0°C to +70°C	1.2 MHz minimum
ADC-B505:	
+25°C	1.19 MHz minimum
0°C to +70°C	1.14 MHz, minimum
Harmonic Distortion (Below FS):	
+25°C	−72 dB minimum
0°C to +70°C	−72 dB minimum

CAUTION

Note: The connectors used for P1 and P2 do not have a shell surrounding the pins. This allows maximum flexibility in making connections, but it also makes it physically possible to insert the mating connectors backwards or offset from their correct positions. Use care in making these connections (Pin 1 connects to a brown wire in each of the supplied cables.)

The performance characteristics shown in Table 1 apply over the operating temperature range and over the operating power supply range unless otherwise specified. Figure 7 demonstrates the total harmonic distortion performance.

Table 2. ADC-B500/B505 Evaluation Board Cable Pin-Outs

P1—POWER SUPPLY CONNECTOR		
PIN	**COLOR**	**FUNCTION**
1	Brown	+5 Volts Input
2	Red	Digital Ground
3	Orange	+5 Volts Input
4	Yellow	Digital Ground
5	Green	+5 Volts Input
6	Blue	Digital Ground
7	Violet	+5 Volts Input
8	Gray	Digital Ground
9	White	−15 Volts Input
10	Black	Analog Ground
11	Brown	−15 Volts Input
12	Red	Analog Ground
13	Orange	−15 Volts Input
14	Yellow	Analog Ground
15	Green	−15 Volts Input
16	Blue	Analog Ground
17	Violet	+15 Volts Input
18	Grey	Analog Ground
19	White	+15 Volts Input
20	Black	Analog Ground
21	Brown	+15 Volts Input
22	Red	Analog Ground
23	Orange	+15 Volts Input
24	Yellow	Analog Ground
25	Green	Analog Ground
26	Blue	Analog Ground

P2—SIGNAL CONNECTOR		
PIN	**COLOR**	**FUNCTION**
1	Brown	Digital Ground
2	Red	Overflow
3	Orange	Digital Ground
4	Yellow	EOC
5	Green	Digital Ground
6	Blue	Bit 12 (LSB)
7	Violet	Digital Ground
8	Gray	Bit 11
9	White	Digital Ground
10	Black	Bit 10
11	Brown	Digital Ground
12	Red	Bit 9
13	Orange	Digital Ground
14	Yellow	Bit 8
15	Green	Digital Ground
16	Blue	Bit 7
17	Violet	Digital Ground
18	Grey	Bit 6
19	White	Digital Ground
20	Black	Bit 5
21	Brown	Digital Ground
22	Red	Bit 4
23	Orange	Digital Ground
24	Yellow	Bit 3
25	Green	Digital Ground
26	Blue	Bit 2
27	Violet	Digital Ground
28	Grey	Bit 1 (MSB)
29	White	Digital Ground
30	Black	Digital Ground
31	Brown	Digital Ground
32	Red	Digital Ground
33	Orange	Digital Ground
34	Yellow	Digital Ground

CALIBRATION PROCEDURE

Removal of system errors is accomplished as follows:

1. Connect the converter per Figure 1 and refer to Tables 3 and 4 to establish the appropriate full-scale range (FSR). Apply a pulse of 105 nanoseconds minimum to the START CONVERT input at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Apply a precision reference source to the analog input through the BNC connector. Adjust the output of the reference source per Tables 3 and 4 for the unipolar zero adjustment (+½ LSB) or the bipolar zero adjustment (zero +½ LSB) for the appropriate FSR. For unipolar, adjust the zero/offset trimming potentiometer (R1) so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 or between 1111 1111 1111 and 1111 1111 1110 depending upon the coding selected per Table 6.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with $\overline{\text{COMP BIN}}$ tied high or between 0111 1111 1111 and 0111 1111 1110 with $\overline{\text{COMP BIN}}$ tied low per Table 7.

3. Full-Scale Adjustment.

   Set the output of the voltage reference used in step 2 to the value shown in Tables 3 and 4 for the unipolar or bipolar gain adjustment (+FS-1½ LSB) for the appropriate FSR. Adjust the gain trimming potentiometer (R2) so that the output code flickers between 1111 1111 1110 and 1111 1111 1111 or between 0000 0000 0001 and 0000 0000 0000 depending upon the coding selected per Tables 6 and 7.

4. To confirm proper operation, vary the precision reference voltage source to obtain the output coding listed in the tables.

Table 3. Zero and Gain Adjust for Unipolar Use

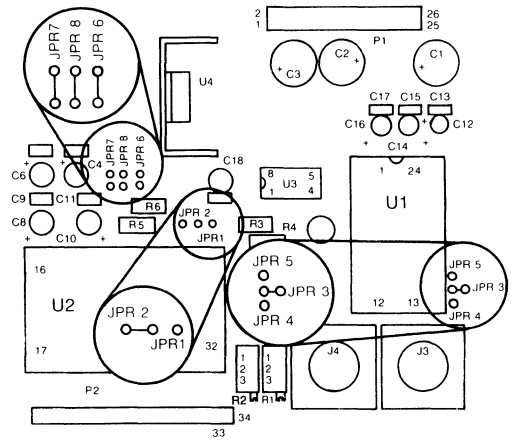
UNIPOLAR FSR	ZERO ADJUST(R1) +½ LSB	GAIN ADJUST(R2) +FS-1½ LSB
0 to −5V	−0.61mV	− 4.9982V
0 to −10V	−1.22mV	− 9.9963V
0 to −20V	−2.44mV	−19.9927V
0 to +10V	+1.22mV	+ 9.9963V

Table 4. Offset and Gain Adjust for Bipolar Use

BIPOLAR FSR	OFFSET ADJUST(R1) −FS +½ LSB	GAIN ADJUST(R2) +FS-1½ LSB
±10V	− 9.9976V	+ 9.9927V
±5V	− 4.9988V	+ 4.9963V

EVALUATION BOARD CONSTRUCTION

Figures 3, 4, 6, 7 and 8 present printed circuit board layouts and construction information for the evaluation boards.



NOTE: Jumpers shown as set from factory for 0 to +10V input, complementary binary/complementary offset binary outputs.

Figure 3. ADC-B500/B505 Evaluation Board Component Layout and Jumper Locations

Table 5. Jumper Selections for Vin Ranges, Coding and Output Enables

Vin RANGE	INSTALL JUMPERS	BINARY/ COMP. OFFSET	COMP. BINARY/ COMP. OFFSET BINARY INSTALL JUMPERS	OUTPUTS ENABLED
0 to −5V	J2,J4	—	J6	J7,J8
0 to −10	J2	—	J6	J7,J8
0 to −20V	J1,J5	—	J6	J7,J8
0 to +10V	J2,J3	J6	—	J7,J8
±5V	J1,J4	J6	—	J7,J8
±10V	J1	J6	—	J7,J8

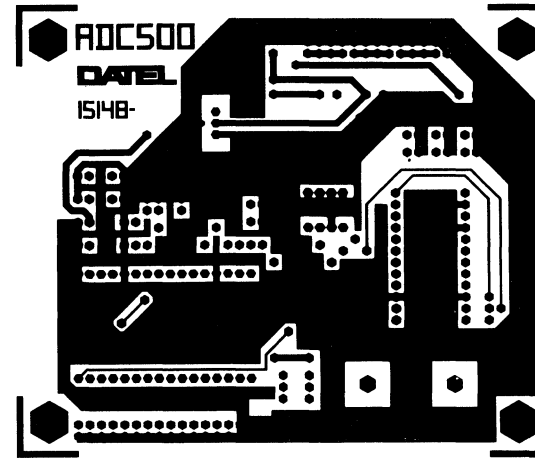


Figure 4. ADC-B500/B505 Board, Component Side (Black=Copper)

Table 6. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES VOLTS dc				OUTPUT CODING SEE TABLE			
	0 to −5V	0 to −10V	0 to +10V	0 to −20V	MSB LSB		MSB LSB	
+FS − 1 LSB	−4.998V	−9.9976V	+9.9976V	−19.9951V	1111 1111	1111	0000 0000	0000
7/8 FS	−4.375V	−9.740V	+8.750V	−17.500V	1110 0000	0000	0001 1111	1111
3/4 FS	−3.750V	−7.500V	+7.500V	−15.00V	1100 0000	0000	0011 1111	1111
1/2 FS	−2.500V	−5.00V	+5.00V	−10.00V	1000 0000	0000	0111 1111	1111
1/4 FS	−1.250V	−2.500V	+2.500V	−5.000V	0100 0000	0000	1011 1111	1111
1/8 FS	−0.625V	−1.250V	+1.250V	−2.500V	0010 0000	0000	1101 1111	1111
1 LSB	−0.0012V	−0.0024V	+0.0024V	−0.0048V	0000 0000	0001	1111 1111	1110
0	0.0000V	0.0000V	0.0000V	0.0000V	0000 0000	0000	1111 1111	1111

Table 7. Output Coding for Bipolar Operation

UNIPOLAR SCALE	INPUT RANGES VOLTS dc		OUTPUT CODING SEE TABLE					
	±5V	±10V	MSB		LSB	MSB		LSB
+FS-1 LSB	+4.9976V	+9.9951V	1111	1111	1111	0000	0000	0000
+3/4 FS	+3.7500V	+7.5000V	1110	0000	0000	0001	1111	1111
+1/2 FS	+2.5000V	+5.0000V	1100	0000	0000	0011	1111	1111
0	0.0000V	0.0000V	1000	0000	0000	0111	1111	1111
−1/2 FS	−2.5000V	−5.0000V	0100	0000	0000	1011	1111	1111
−3/4 FS	−3.7500V	−7.5000V	0010	0000	0000	1101	1111	1111
−FS +1 LSB	−4.9976V	−9.9951V	0000	0000	0001	1111	1111	1110
−FS	−5.0000V	−10.0000V	0000	0000	0000	1111	1111	1111

RESISTORS

R1, R2 20K TRIMPOT
R3, R4 10K, 0.1%
R5, R6 4.7K

CAPACITORS

C1, C2, C3 100μ F @25V
C4, C6, C8, C10, C12, C16, C18 4.7μ F @25V
C5, C7, C9, C11, C13, C15, C17, C19 0.1μ F

SEMICONDUCTORS

U1 SHM-45MC
U2 ADC-500MC/ ADC-505MC
U3 LP411 OP. AMP.
U4 7905 −5V Regulator
Q1 2N2907

MISCELLANEOUS

1 — PC Board
2 — BNC Female Connectors
13 — Terminal Pins
4 — Jumper Plugs
1 — 25-Pin Connector w/Flat Cable
1 — 34-Pin Connector w/Flat Cable
1 — 26-Pin Terminal Strip Dip
1 — 34-Pin Terminal Strip Dip
1 — 24-Pin IC Socket
1 — 32-Pin IC Socket
4 — Standoffs
1 — 4-40 x 1/4″ Screws
1 — Heat Sink
1 — 4-40 x 3/8″ Nylon Screw
1 — 4-40 Nylon Nut

Figure 5. ADC-B500/B505 Evaluation Board Components

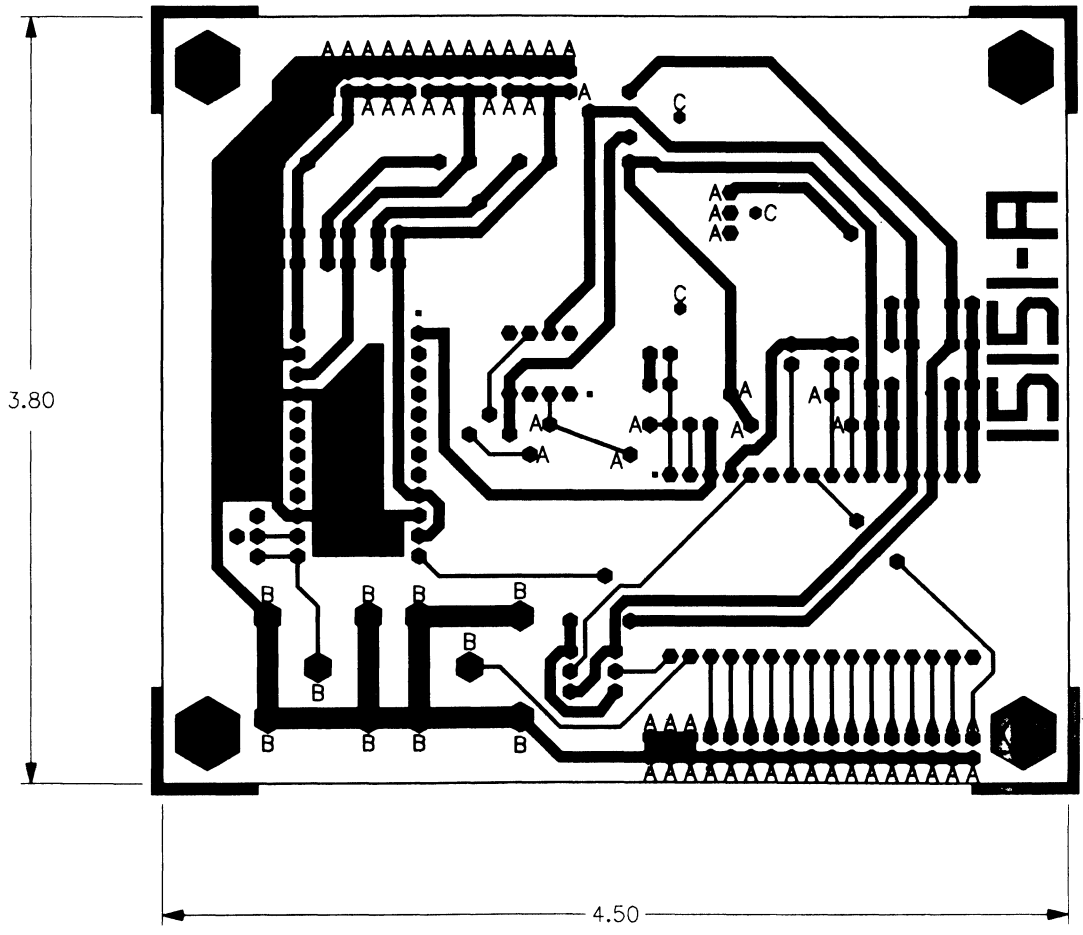
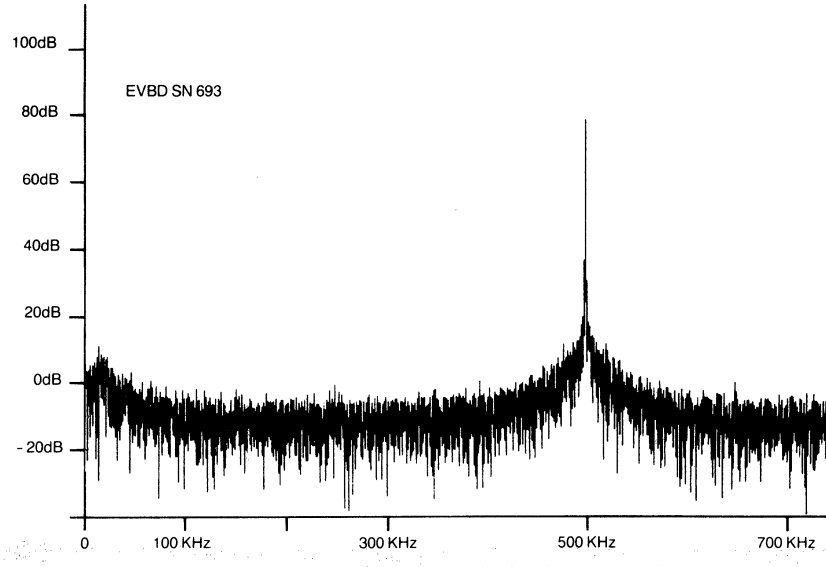


Figure 6. ADC-B500/B505 Board, Underside (Black = Copper) with Hole Dimensions

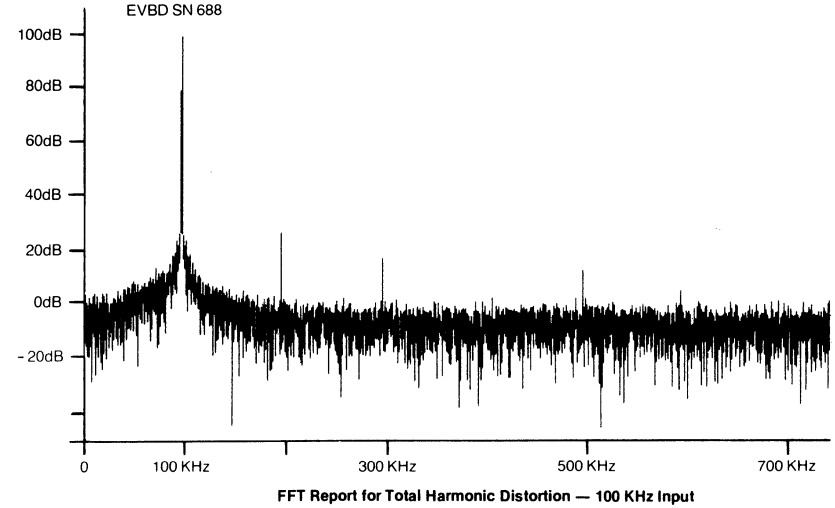
Figure 6 shows the etch for the underside of the ADC-B500, B505 Evaluation Board. Hole dimensions are given in Table 8. This drawing shows actual dimensions for Figures 3 and 4 as well.

Table 8. Hole Dimensions

HOLE LEGEND		
UNLESS OTHERWISE SPECIFIED ALL HOLES ARE PLATED-THRU		
SYM	DESCRIPTION	REF QTY
NONE	.028—.034 DIA	138
A	.039—.034 DIA	71
B	.060—.066 DIA	10
C	.125—.131 DIA	7



FFT Report for Total Harmonic Distortion — 500 KHz Input



FFT Report for Total Harmonic Distortion — 100 KHz Input

Figure 7. Harmonic Distortion Performance

ORDERING INFORMATION

MODEL	CONVERSION RATE
ADC-B500	1.25 MHz
ADC-B505	1.1 MHz
ADC-B500-1	Evaluation Board Without ADC-SHM

For information on the ADC-500/505 and SHM-45, contact the factory or a local sales office.

ADC-EH10B
10-Bit, 2.0 and 4.0 Microsecond Analog-to-Digital Converters

FEATURES

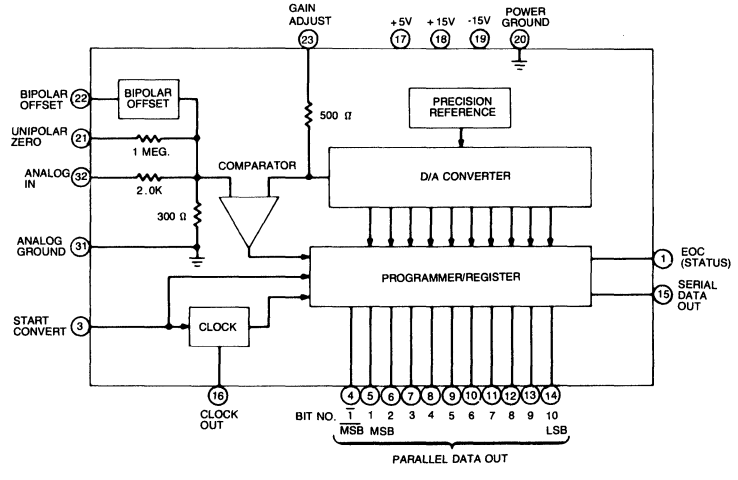
- **2.0 Microseconds conversion— ADC-EH10B2**
- **4.0 Microseconds conversion— ADC-EH10B1**
- **10-Bit resolution**
- **Compact 3″ x 2″ x 0.375″ module**
- **±30 ppm/°C maximum tempco**

GENERAL DESCRIPTION

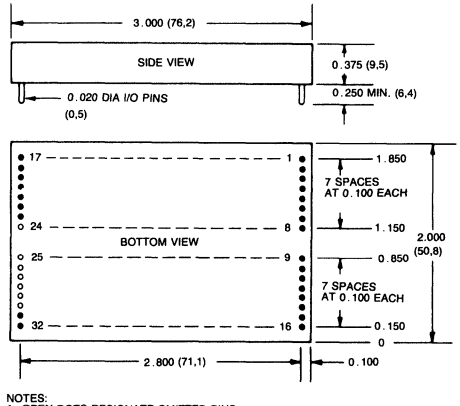
Model ADC-EH10B is a very fast 10-bit successive approximation type A/D converter in a compact low profile package. Low pricing makes this converter an ideal choice for many applications including fast scanning data acquisition systems, PCM systems, and fast pulse analysis. This converter is available in two versions based on conversion speed: ADC-EH10B1 with 4.0 microseconds (250kHz rate) and ADC-EH10B2 with 2.0 microseconds (500kHz rate).

High speed and moderate power consumption (1.7 watts) in a compact size (3″ x 2″ x 0.375″) are made possible by use of an MSI integrated circuit successive approximation programmer/register used with 10 fast switching current sources driving a low impedance R-2R ladder network. A fast precision comparator and precision voltage reference circuit are also used.

Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. The converter has a maximum full scale temperature coefficient of ±30 ppm/°C and is monotonic over the full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronizing serial data, $\overline{\text{MSB}}$ output for two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible. Power requirement is ±15V dc and +5V dc. The ADC-EH10B is also available in extended temperature range versions.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS.
2. 0.100 INCH = 2,5 mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	NO CONNECTION
3	START CONVERT
4	BIT 1 OUT ($\overline{\text{MSB}}$)
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT (LSB)
15	SERIAL DATA OUT
16	CLOCK OUT
17	+5V POWER IN
18	+15V POWER IN
19	−15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST.
31	ANALOG GROUND
32	ANALOG IN

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V Supplies, unless otherwise indicated.

INPUTS

Analog Input Range ..... 0V to +10V FS or ±5V FS
Input Impedance ..... 2.3K ±0.1%
Input Overvoltage ..... ±20V, no damage
Start Conversion ..... 2V minimum to 5.5V maximum positive pulse with duration of 50 nanoseconds minimum. Rise and fall times <500 nanoseconds.
Logic "1" resets converter
Logic "0" initiates conversion
Loading: 1 TTL load

OUTPUTS

Parallel Output Data ..... 10 parallel lines of data held until next conversion command.
V out ("0") ≤ +0.4V
V out ("1") ≥ +2.4V
Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation . Straight Binary, positive true
Bipolar operation .. Offset Binary, positive true
Two's complement, positive true
Serial Output Data ..... NRZ successive decision pulse output generated during conversion with MSB first.
Straight binary or offset binary, positive true coding.
Loading: 4 TTL loads
End of Conversion (EOC) ... Conversion Status Signal.
V out ("0") ≤ +0.4V indicates conversion completed.
V out ("1") ≥ +2.4V during reset and conversion.
Loading: 4 TTL loads.
Clock Output ..... Internal clock pulse train of negative going pulses from +5V to 0V gated ON during conversion time.
Loading: 6 TTL loads

PERFORMANCE

Resolution ..... 10 Bits (1 part in 1024)
Nonlinearity ..... ±½ LSB maximum
Differential Nonlinearity .... ±½ LSB maximum
Differential Nonlinearity T.C. ±10 ppm/°C maximum
Temp. Coeff. of Gain ..... ±30 ppm/°C maximum
Temp. Coeff. of Zero, unipolar ..... ±150 μV/°C maximum
Temp. Coeff. of Offset, bipolar ..... ±20 ppm/°C maximum
Power Supply Rejection ... 0.01% FS/% supply, maximum
Conversion Time ..... 4.0 microseconds maximum, ADC-EH10B1
2.0 microseconds maximum, ADC-EH10B2

POWER REQUIREMENTS

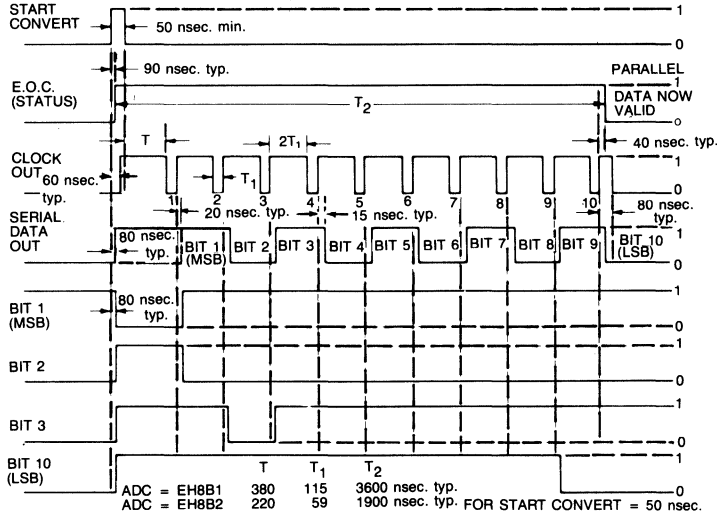
Power Supply Voltage ..... +15V dc ±0.5V dc at 75 mA maximum
−15V dc ±0.5V dc at 20 mA maximum
+5V dc ±0.25V dc at 150 mA maximum

PHYSICAL/ENVIRONMENTAL

Operating Temp. Range ... 0°C to 70°C
Storage Temp. Range ..... −25°C to +85°C
Relative Humidity ..... Up to 100% non-condensing
Case Size ..... 3 x 2 x 0.375 inches (76,2 x 30,8 x 9,5 mm)
Case Material ..... Black Diallyl Phthalate per MIL-M-14
Pins ..... 0.020″ round, gold plated, 0.250″ long minimum
Weight ..... 3 ounces maximum (85 grams)

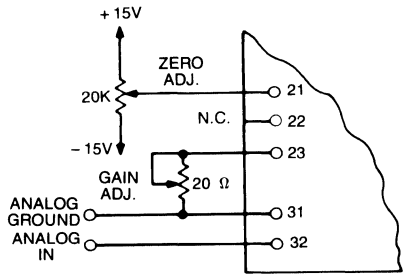
FOOTNOTE:
ADC-EH10B1 replaces former DATEL model ADC-EH10B and is an improved version of the model. The only differences from the previous model is the change in input impedance from 10K ohms to 2.3K ohms, and the reduction in 5V supply current from 280 mA to 150 mA.

Output: 1010101010



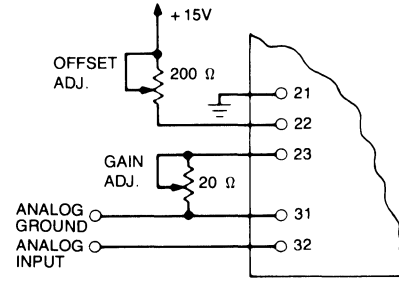
TIMING DIAGRAM FOR ADC-EH10B

GAIN & OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 3 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANLOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero + ½ LSB (+4.9mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 00 and 0000 0000 01.
3. Adjust the output of the voltage reference to +F.S. − 1½ LSB (+9.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 10 and 1111 1111 11.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 3 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to 0.0000V. Adjust the offset trimming potentiometer so that the output code is 1000 0000 00.
3. Adjust the output of the voltage reference to +F.S. − 1½ LSB (+4.9854V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 10 and 1111 1111 11.

OUTPUT CODING

UNIPOLAR (0V TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS − 1 LSB	+9.9902V	1111 1111 11
+⅞ FS	+8.7500V	1110 0000 00
+¾ FS	+7.5000V	1100 0000 00
+½ FS	+5.0000V	1000 0000 00
+¼ FS	+2.5000V	0100 0000 00
+1 LSB	+0.0098V	0000 0000 01
0	0.0000V	0000 0000 00

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS − 1 LSB	+4.9902V	1111 1111 11	0111 1111 11
+¾ FS	+3.7500V	1110 0000 00	0110 0000 00
+½ FS	+2.5000V	1100 0000 00	0100 0000 00
0	0.0000V	1000 0000 00	0000 0000 00
−½ FS	−2.5000V	0100 0000 00	1100 0000 00
−¾ FS	−3.7500V	0010 0000 00	1010 0000 00
−FS +1 LSB	−4.9902V	0000 0000 01	1000 0000 01
−FS	−5.0000V	0000 0000 00	1000 0000 00

*Using $\overline{\text{MSB}}$ output for Bit 1

ORDERING INFORMATION

ADC-EH10B____

CONVERSION TIME
1 = 4.0 Microseconds
2 = 2.0 Microseconds

ACCESSORIES

Part Number	Description
DILS-2	Mating Sockets: (2 per module)
TP20, TP200, TP20K	Trimming Potentiometers

ADC-EH12B1, B2
12-Bit, 4.0 and 8.0 Microseconds Analog-to-Digital Converters

DATEL

FEATURES

- **4.0 Microseconds conversion time—ADC-EH12B2**
- **8.0 Microseconds conversion time—ADC-EH12B1**
- **12-Bit resolution**
- **30 ppm/°C tempco**
- **Low profile—0.4 inches high**

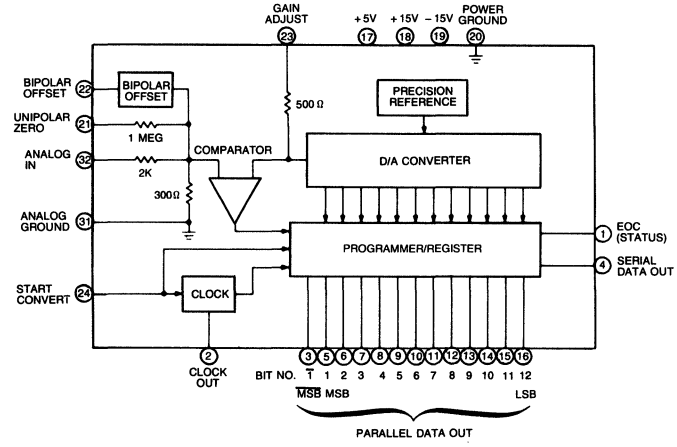
GENERAL DESCRIPTION

Model ADC-EH12B2 is a 4 microsecond, 12-bit successive approximation type A/D converter in a low profile 4 x 2 x 0.4 inch module. This high performance converter is priced at about half that of other competing models; in addition, it consumes only 2.0 watts of power, much less than competing devices. It is ideal for application in PCM systems, data acquisition systems, and other instrumentation and control systems requiring very fast data conversion rates up to 250,000 per second. The ADC-EH12B1 is also available in an even lower cost 8.0 microseconds version.

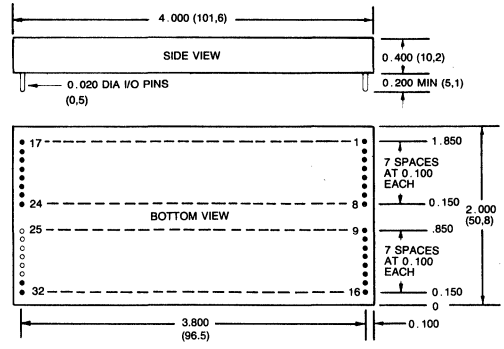
The ADC-EH12B design utilizes an MSI integrated circuit successive approximation programmer/register, 12 fast switching current sources, a low impedance R-2R resistor network, a precision voltage reference circuit, and a fast precision comparator to achieve its very fast conversion rate.

Operating features include unipolar (0 to +10V) or bipolar (±5V) operation by external pin connection. Full scale temperature coefficient is 30 ppm/°C maximum and the converter is monotonic over its full operating temperature range of 0°C to 70°C. External offset and gain adjustments are provided for precise calibration of zero and full scale. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight binary or offset binary coding. Other outputs include clock output for synchronization with serial data, $\overline{\text{MSB}}$ output for use in two's complement coding, and end of conversion (status) signal. All outputs are DTL/TTL compatible.

Power requirement is ±15V dc and +5V dc. Extended temperature range versions are also available.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2,5 mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	CLOCK OUT
3	BIT 1 OUT ($\overline{\text{MSB}}$)
4	SERIAL DATA OUT
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT
15	BIT 11 OUT
16	BIT 12 OUT (LSB)
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST
24	START CONVERT IN
31	ANALOG GROUND
32	ANALOG IN

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FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated.

INPUTS

Analog Input Range	0V to +10V FS or ±5V FS
Input Impedance	2.3K ohms ±0.1%
Input Overvoltage	±20V, no damage
Start Conversion	2V minimum to 5.5V maximum positive pulse with duration of 100 nanoseconds minimum. Rise and fall times <500 nanoseconds Logic "1" resets converter Logic "0" initiates conversion Loading: 1 TTL load

OUTPUTS

Parallel Ouput Data	12 parallel lines of data held until next conversion command. V out ("0") ≤ +0.4V V out ("1") ≥ +2.4V Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation	Straight Binary, positive true
Bipolar operation	Offset Binary, positive true Two's complement, positive true
Serial Output Data	NRZ successive decision pulse output generated during conversion with MSB first. Straight binary or offset binary, positive true coding. Loading: 4 TTL loads
End of Conversion (EOC)	Conversion Status Signal. V out ("0") ≤ +0.4V indicates conversion completed. V out ("1") ≥ +2.4V during reset and conversion. Loading: 4 TTL loads
Clock Output	Internal clock pulse train or negative going pulses from +5V to 0V gated on during conversion time. Loading: 6 TTL loads

PERFORMANCE

Resolution	12 Bits (1 part in 4096)
Nonlinearity	±½ LSB maximum
Differential Nonlinearity	±½ LSB maximum
Differential Nonlinearity T.C.	±3 ppm/°C maximum
Temp. Coeff. of Gain	±30 ppm/°C maximum
Temp. Coeff. of Zero, unipolar	±150 μV/°C maximum
Temp. Coeff. of Offset, bipolar	±15 ppm of F.S./°C maximum
Power Supply Rejection	0.01% FS/% supply, maximum
Conversion Time	8.0 microseconds maximum, ADC-EH12B1 4.0 microseconds maximum, ADC-EH12B2

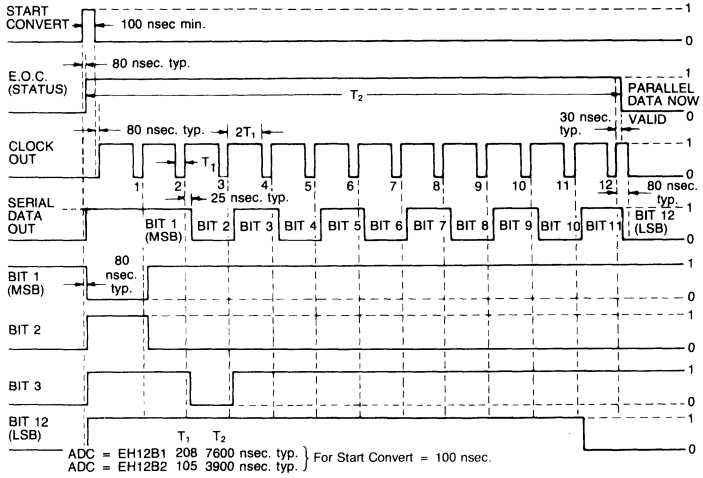
POWER REQUIREMENTS

Power Supply Voltage	±15V dc ±0.5V dc at 40 mA maximum +5V dc ±0.25V dc at 150 mA maximum

PHYSICAL/ENVIRONMENTAL

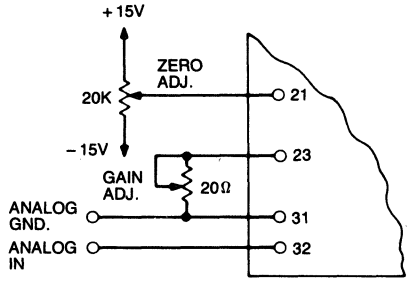
Operating Temp. Range	0°C to 70°C
Storage Temp. Range	−25°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2 mm)
Case Material	Black Diallyl Phthalate per MIL-M-14
Pins	0.020" round, gold plated, 0.200" long minimum
Weight	4 ounces maximum (114 grams)

Output: 101010101010



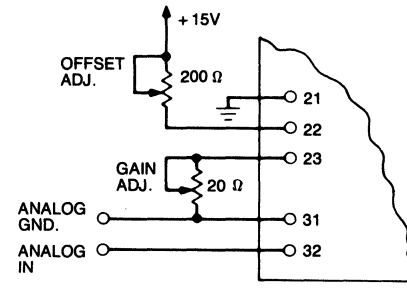
TIMING DIAGRAM FOR ADC-EH12B

GAIN AND OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero + ½ LSB (+1.2mV). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to +FS − 1½ LSB (+9.9963V). Adjust the GAIN trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24 (see specifications and timing diagram).
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to 0.0000V. Adjust the offset trimming potentiometer so that the output code is 1000 0000 0000.
3. Adjust the output of the voltage reference to +FS − 1½ LSB (+4.9963V). Adjust the Gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

OUTPUT CODING

UNIPOLAR (0V TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS −1 LSB	+9.9976V	1111 1111 1111
+⅞ FS	+8.7500V	1110 0000 0000
+¾ FS	+7.5000V	1100 0000 0000
+½ FS	+5.0000V	1000 0000 0000
+¼	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS −1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+¾ FS	+3.7500V	1110 0000 0000	0110 0000 0000
+½ FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
−½ FS	−2.5000V	0100 0000 0000	1100 0000 0000
−¾ FS	−3.7500V	0010 0000 0000	1010 0000 0000
−FS +1 LSB	−4.9976V	0000 0000 0001	1000 0000 0001
−FS	−5.0000V	0000 0000 0000	1000 0000 0000

*Using $\overline{\text{MSB}}$ output for Bit 1

ORDERING INFORMATION

ADC-EH12B_____

CONVERSION TIME

1 = 8.0 Microseconds
2 = 4.0 Microseconds

ACCESSORIES

Part Number	Description
DILS-2	Mating Sockets: (2 per module)
TP20, TP200, TP20K	Trimming Potentiometers

ADC-EH12B3
Ultra-Fast, 12-Bit Analog-to-Digital Converter

1

FEATURES

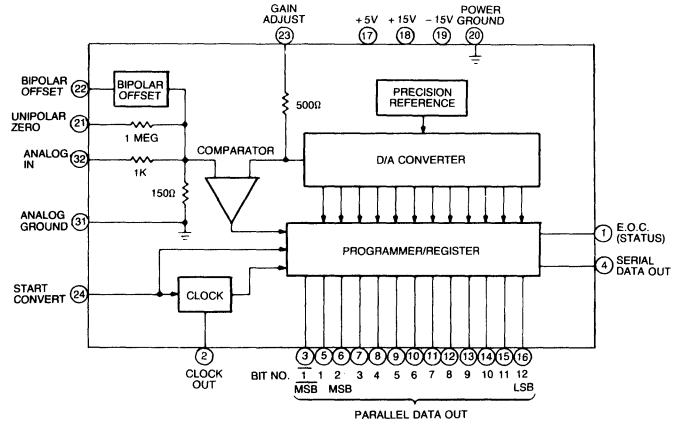
- **2.0 Microseconds conversion time**
- **12-Bit resolution**
- **Low power consumption—2.25W**
- **Low profile case—0.4 inches high**
- **Low cost**

GENERAL DESCRIPTION

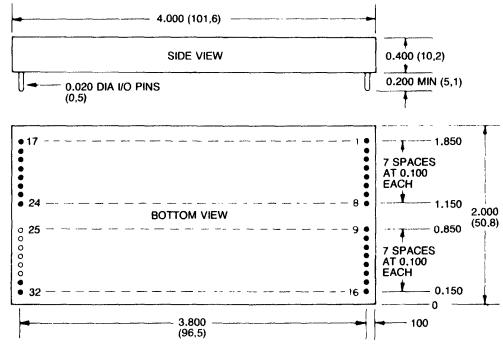
Model ADC-EH12B3 is a new, ultra-fast, 12-bit successive approximation A/D converter with a 2.0 microsecond maximum conversion time. This converter utilizes 12 very fast switched current sources with a low impedance R-2R ladder network, a fast precision comparator, a precision zener reference source, and an MSI integrated circuit successive approximation register to achieve its state of the art performance. It is encapsuiated in a low profile 2 x 4 x 0.4 inch module and consumes only 2.25 watts of power. The ADC-EH12B3 opens up a broad range of fast data conversion applications where conversion rates up to 500,000 per second are required.

Input voltage ranges are 0 to +10V unipolar or ±5V bipolar by external pin connection; input impedance is 1.15K ohms. The parallel output is in straight binary, offset binary, or two's complement coding. Serial output data is also brought out in the form of an NRZ format MSB first pulse train. Full scale temperature coefficient is ±30 ppm/°C maximum and zero temperature coefficient is ±150 μV/°C maximum. Due to its low differential linearity temperature coefficient there are no missing codes over the 0°C to +70°C operating temperature range. Provision is made for precise alignment in a given application.

Other DTL/TTL compatible outputs include clock, $\overline{\text{MSB}}$ output (for two's complement coding), and end of conversion (status) output. Power supply requirement is ±15V dc and +5V dc.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATED OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	CLOCK OUT
3	$\overline{\text{BIT 1 OUT (MSB)}}$
4	SERIAL DATA OUT
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT
13	BIT 9 OUT
14	BIT 10 OUT
15	BIT 11 OUT
16	BIT 12 OUT (LSB)
17	+5V POWER IN
18	+15V POWER IN
19	-15V POWER IN
20	POWER GROUND
21	UNIPOLAR ZERO
22	BIPOLAR OFFSET
23	GAIN ADJUST
24	START CONVERT IN
31	ANALOG GROUND
32	ANALOG IN

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V & +5V Supplies, unless otherwise indicated.

INPUTS

Analog Input Range ..... 0V to +10V FS or ±5V FS
Input Impedance ..... 1.15K ohms ±0.1%
Input Overvoltage ..... ±20V, no damage
Start Conversion ..... 2V minimum to 5.5V maximum positive pulse with duration of 100 nanoseconds minimum. Rise and fall times <500 nanoseconds.
Logic "1" resets converter
Logic "0" initiates conversion
Loading: 3 TTL loads

OUTPUTS

Parallel Output Data ..... 12 parallel lines of data held until next conversion command.
V out ("0") ≤ +0.4V
V out ("1") ≥ +2.4V
Each output capable of driving up to 4 TTL loads.
Coding, Unipolar operation .. Straight Binary, positive true
Bipolar operation ..... Offset Binary, positive true
Two's complement, positive true
Serial Output Data ..... NRZ successive decision pulse output generated during conversion with MSB first.
Straight binary or offset binary, positive true coding.
Loading: 4 TTL loads
End of Conversion (EOC) .... Conversion Status Signal.
V out ("0") ≤ +0.4V indicates conversion completed.
V out ("1") ≥ +2.4V during reset and conversion.
Loading: 4 TTL loads
Clock Output ..... Internal clock pulse train of negative going pulses from +5V to 0V gated ON during conversion time.
Loading: 6 TTL loads

PERFORMANCE

Resolution ..... 12 Bits (1 part in 4096)
Nonlinearity ..... ±½ LSB maximum
Differential Nonlinearity ..... ±½ LSB maximum
Differential Nonlinearity T.C. .. ±3 ppm/°C maximum
Temp. Coeff. of Gain ..... ±30 ppm/°C maximum
Temp. Coeff. of Zero, unipolar ..... ±150 μV/°C maximum
Temp. Coeff. of Offset, bipolar ..... ±15 ppm of F.S./°C maximum
Power Supply Rejection ..... 0.01% FS/% supply, maximum
Conversion Time ..... 2.0 microseconds maximum

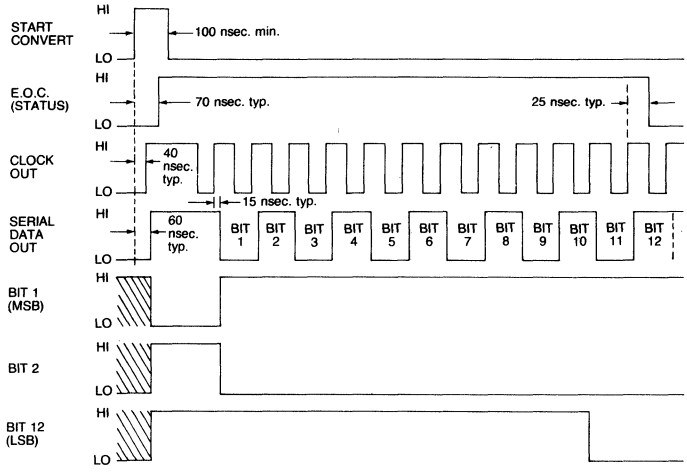
POWER REQUIREMENTS

Power Supply Voltage ..... +15V dc ±0.5V at 80 mA maximum
−15V dc ±0.5V at 20 mA maximum
+5V dc ±0.25V at 150 mA maximum

PHYSICAL/ENVIRONMENTAL

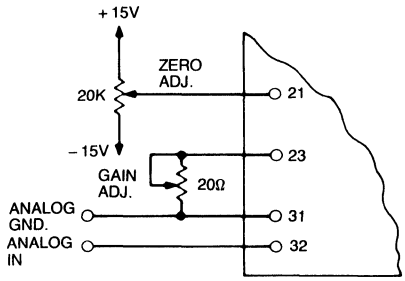
Operating Temp. Range ..... 0°C to 70°C
Storage Temp. Range ..... −25°C to +85°C
Relative Humidity ..... Up to 100% non-condensing
Case Size ..... 4 x 2 x 0.4 inches (101,6 x 50,8 x 10,2 mm)
Case Material ..... Black Diallyl Phthalate per MIL-M-14
Pins ..... 0.020" round, gold plated, 0.200" long minimum
Weight ..... 4 ounces maximum (114 grams)

Output 101010101010



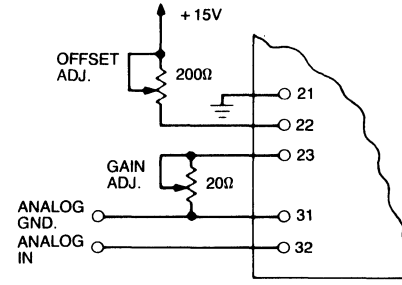
TIMING DIAGRAM FOR ADC-EH12B

GAIN AND OFFSET ADJUSTMENTS



UNIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24.
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to Zero + ½ LSB (+1.2mV). Adjust the zero trim for an output code of between 0000 0000 0000 and 0000 0000 0001.
3. Adjust the output of the voltage reference to +F.S. −1½ LSB (+9.9963V). Adjust the GAIN trim for an output code of between 1111 1111 1110 and 1111 1111 1111.



BIPOLAR OPERATION

1. Apply START CONVERT pulses to pin 24.
2. Apply a precision reference voltage source to ANALOG IN (pin 32) and ANALOG GROUND (pin 31). Adjust the output of the voltage reference to 0.0000V. Adjust the offset trim for an output code of 1000 0000 0000.
3. Adjust the output of the voltage reference to +F.S. −1½ LSB (+4.9963V). Adjust the GAIN trim for an output code of 1111 1111 1110 and 1111 1111 1111.

OUTPUT CODING

UNIPOLAR (0V TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS −1 LSB	+9.9976V	1111 1111 1111
+⅞ FS	+8.7500V	1110 0000 0000
+¾ FS	+7.5000V	1100 0000 0000
+½ FS	+5.0000V	1000 0000 0000
+¼	+2.5000V	0100 0000 0000
+1 LSB	+0.0024V	0000 0000 0001
0	0.0000V	0000 0000 0000

BIPOLAR (−5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BINARY	TWO'S COMPLEMENT*
+FS −1 LSB	+4.9976V	1111 1111 1111	0111 1111 1111
+¾ FS	+3.7500V	1110 0000 0000	0110 0000 0000
+½ FS	+2.5000V	1100 0000 0000	0100 0000 0000
0	0.0000V	1000 0000 0000	0000 0000 0000
−½ FS	−2.5000V	0100 0000 0000	1100 0000 0000
−¾ FS	−3.7500V	0010 0000 0000	1010 0000 0000
−FS + 1 LSB	−4.9976V	0000 0000 0001	1000 0000 0001
−FS	−5.0000V	0000 0000 0000	1000 0000 0000

*Using $\overline{\text{MSB}}$ output for Bit 1

ORDERING INFORMATION

ADC-EH12B3

ACCESSORIES

Part Number	Description
DILS-2	Mating Sockets: (2 per module)
TP20, TP200, TP20K	Trimming Potentiometers

ADC-EH8B
Fast, 8-Bit Analog-to-Digital Converters

FEATURES

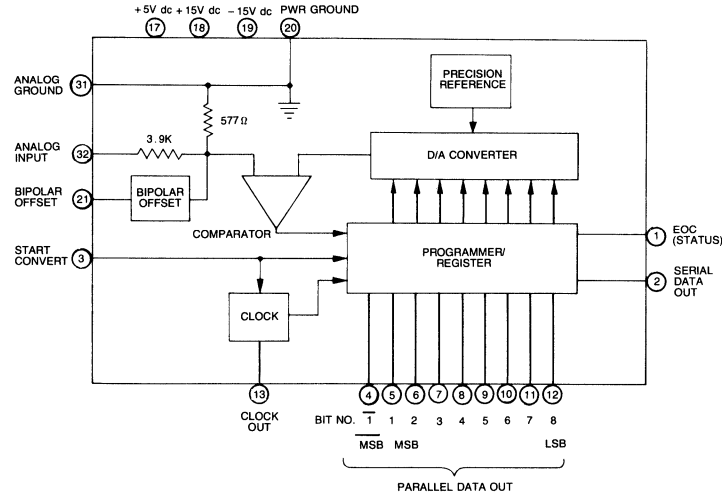
- **8-Bit resolution**
- **4.0 and 2.0 microseconds conversion time**
- **Unipolar or bipolar operation**
- **Parallel and serial outputs**
- **Low cost**

GENERAL DESCRIPTION

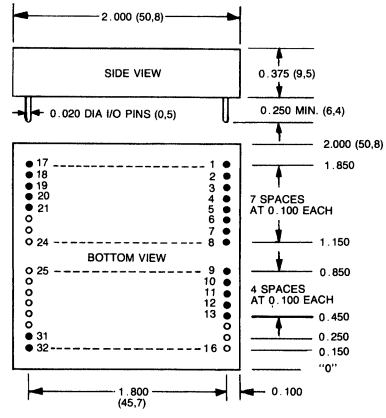
The model ADC-EH8B is a fast, 8-bit successive approximation type analog-to-digital converter in a compact 2 x 2 x 0.375 inch module. These converters are low cost devices with application in pulse code modulation systems and instrumentation and control systems requiring fast data conversion rates up to 500,000 per second. There are two models to choose from based on conversion speed: ADC-EH8B1 with a conversion time of 4.0 microseconds (250 kHz rate), and ADC-EH8B2 with a conversion time of 2.0 microseconds (500 kHz rate).

The high speed in a small size is made possible by the use of an MSI integrated circuit which provides all the necessary successive approximation logic, along with other new integrated circuit components. The analog input range is either unipolar 0 to +10V or bipolar −5V to +5V, determined by external pin connection. For unipolar operation no external adjustments are necessary; for bipolar operation only a bipolar offset adjustment must be made externally. Parallel output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation. A serial output gives successive decision pulses in NRZ format with straight or offset binary coding. Other outputs are clock output for synchronization with serial data, and $\overline{\text{MSB}}$ output for two's complement coding.

Other specifications include full scale temperature coefficient of 50 ppm/°C maximum, long term stability of 0.05%/year, and linearity of ± 1/2 LSB. Power requirement is ± 15V dc and +5V dc.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS.
2. 0.100 INCH = 2,5 mm, 0.150 INCH = 3,8 mm.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	E.O.C. (STATUS)
2	SERIAL DATA OUTPUT
3	START CONVERT
4	BIT 1 OUT (MSB)
5	BIT 1 OUT (MSB)
6	BIT 2 OUT
7	BIT 3 OUT
8	BIT 4 OUT
9	BIT 5 OUT
10	BIT 6 OUT
11	BIT 7 OUT
12	BIT 8 OUT (LSB)
13	CLOCK OUT
17	+5V POWER IN
18	+15V POWER IN
19	−15V POWER IN
20	POWER GROUND
21	BIPOLAR OFFSET
31	ANALOG GROUND
32	ANALOG INPUT

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FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies, unless otherwise indicated.

INPUTS

Analog Input Range ..... 0V to +10V Full-Scale or ±5V Full-Scale
Input Impedance ..... 4.45K ohms ±50 ohms
Input Overvoltage ..... ±20V (no damage)
Start Conversion ..... 2V minimum to 5.5V maximum positive pulse with duration of 100 nanoseconds minimum. Rise and fall times <50 nanoseconds.
Logic "1" resets converter.
Logic "0" initiates conversion.
Loading: 1 TTL load

OUTPUTS

Parallel Output Data ..... 8 parallel lines of data held until next conversion command.
V out ("0") ≤ +0.4V
V out ("1") ≥ +2.4V
Each output capable of driving up to 4 TTL loads.
Coding, Unipolar Operation .. Straight Binary, positive true.
Bipolar Operation ... Offset Binary, positive true.
Two's Complement, positive true.
Serial Output Data ..... NRZ successive decision pulse output generated during conversion, with MSB first. Straight binary or offset binary coding.
Loading: 4 TTL loads.
End of Conversion (EOC) .... Conversion Status Signal.
V out ("0") ≤0.4V indicates conversion time completed.
V out ("1") ≥ +2.4V during reset and conversion periods.
Loading: 4 TTL loads.
Clock Output ..... Internal clock pulse train of negative going pulses from +5V to 0V gated on during conversion time.
Loading: 6 TTL loads.

PERFORMANCE

Resolution ..... 8 Bits (1 part in 256)
Linearity Error ..... ±1/2 LSB maximum.
Differential Nonlinearity ..... ±1/2 LSB maximum.
Temp. Coeff. of Gain ..... ±50 ppm/°C maximum.
Temp. Coeff. of Zero, Unipolar ..... ±100 μV/°C maximum.
Temp. Coeff. of Offset, Bipolar ..... ±35 ppm of FS/°C maximum.
Long Term Stability ..... ±0.05%/year
Power Supply Rejection ..... ±0.02% of Full-Scale/% supply, maximum.
Conversion Time ..... 4.0 microseconds maximum, ADC-EH8B1
2.0 microseconds maximum, ADC-EH8B2

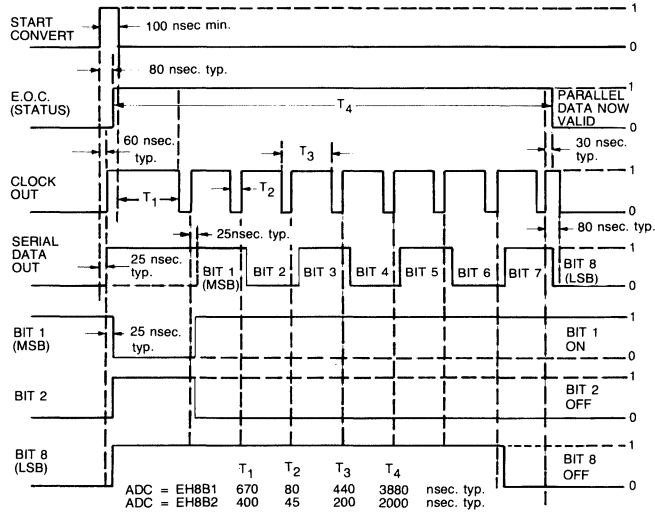
POWER REQUIREMENTS

Power Supply Voltage ..... ±15V dc ±0.5V at 25 mA maximum.
+5V dc ±0.25V at 125 mA maximum.

PHYSICAL/ENVIRONMENTAL

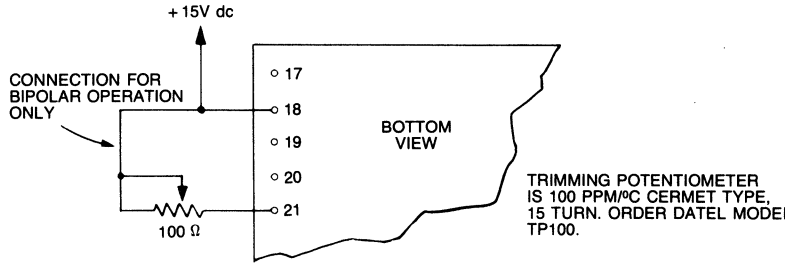
Operating Temp. Range ..... 0°C to +70°C
Storage Temp. Range ..... −55°C to +85°C
Relative Humidity ..... Up to 100% non-condensing
Case Size ..... 2 x 2 x 0.375 inches (50,8 x 50,8 x 9,5 mm)
Case Material ..... Black diallyl phthalate per MIL-M-14
Pins ..... 0.020" round, gold plated, 0.250" long minimum.
Weight ..... 2 ounces maximum (57 grams)

Output: 10101010



TIMING DIAGRAM FOR ADC-EH8B

ADC-EH8B CALIBRATION



UNIPOLAR OPERATION

1. UNIPOLAR — No adjustments are necessary and 100Ω trimming pot is not used. Full scale and zero are internally set to better than ½ LSB. Pin 21 is left open.

BIPOLAR OPERATION

2. BIPOLAR — Connect pin 18 (+15 V dc) to pin 21 through a 100Ω trimming potentiometer as shown. Connect a precision voltage source to pin 32 and set the input voltage to +½ LSB or +0.020V. Adjust the trimming potentiometer so that the output code flickers equally between 1000 0000 and 1000 0001.

OUTPUT CODING

UNIPOLAR (0 TO +10V)

SCALE	INPUT VOLTAGE	STRAIGHT BINARY
+FS – 1 LSB	+9.96V	1111 1111
+⅞ FS	+8.75V	1110 0000
+¾ FS	+7.50V	1100 0000
+½ FS	+5.00V	1000 0000
+¼ FS	+2.50V	0100 0000
+1 LSB	+0.04V	0000 0001
0	0.00V	0000 0000

BIPOLAR (–5V TO +5V)

SCALE	INPUT VOLTAGE	OFFSET BIN	2'S COMPLEMENT
+FS – 1 LSB	+4.96V	1111 1111	0111 1111
+¾ FS	+3.75V	1110 0000	0110 0000
+½ FS	+2.50V	1100 0000	0100 0000
0	0.00V	1000 0000	0000 0000
–½ FS	–2.50V	0100 0000	1100 0000
–¾ FS	–3.75V	0010 0000	1010 0000
–FS + 1 LSB	–4.96V	0000 0001	1000 0001
–FS	–5.00V	0000 0000	1000 0000

ORDERING INFORMATION

ADC-EH8B ____

CONVERSION TIME

1 = 4.0 Microseconds
2 = 2.0 Microseconds

ACCESSORIES

Part Number	Description
DILS-2	Mating Sockets: (2 per module)
TP100	Trimming Potentiometers

ADC-EK Series
Monolithic Integrating Analog-to-Digital Converters

1

FEATURES

- **Monolithic CMOS**
- **Binary or BCD models**
- **20 mW power consumption**
- **To 12-bit accuracy**
- **No missing codes**
- **Low cost**

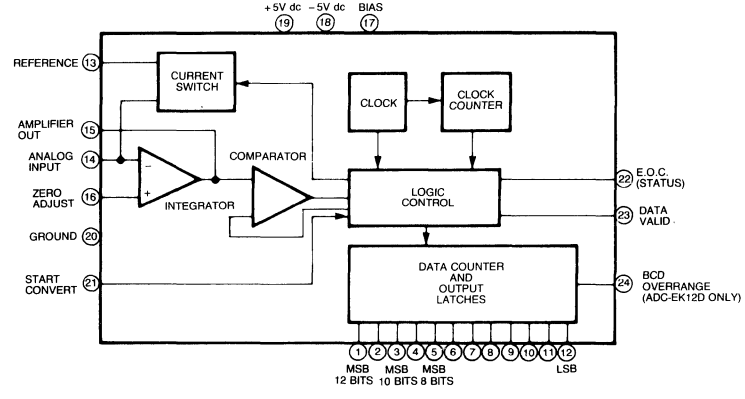
GENERAL DESCRIPTION

The ADC-EK series are low power, integrating A/D converters fabricated on a single monolithic chip using CMOS technology. The circuit employs a charge balancing integrator, current switch comparator, clock counter, data counter, and control logic circuitry to implement conversion. The charge balancing integration technique gives high linearity and noise immunity along with inherent monotonicity resulting in no missing codes. Output data appears in parallel form on latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The ADC-EK series consists of 5 different models with 8-, 10-, and 12-bit binary coding and 3½ digit BCD coding.

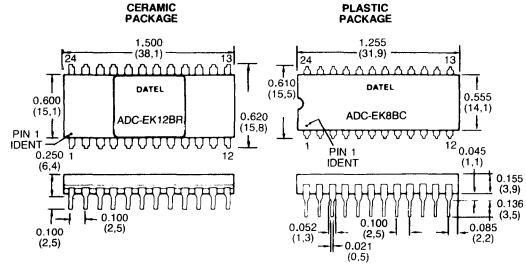
Conversion time is 1.8 to 24 milliseconds maximum depending on model. Nonlinearity is ±½ LSB maximum while differential nonlinearity is ±¼ LSB typical. Other specifications include gain tempco of ±25 ppm/°C typical and zero drift of ±50 μV/°C maximum. An external reference, integrating capacitor, and several other components are required for operation. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10 μA full scale. Standard operating mode is unipolar but bipolar operation is accomplished using an external op amp to provide an offset current from the reference.

Power requirement is ±5V dc at 2 mA, giving a power consumption of only 20 mW. The units are packaged in 24 pin ceramic or plastic DIP's.

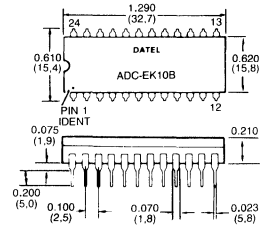
CAUTION: The ADC-EK Series are CMOS devices and should be handled carefully to prevent static charge pickup which might damage the devices. The devices should be kept in the shipping containers until ready for installation.



MECHANICAL DIMENSIONS INCHES (MM)



CERDIP



INPUT/OUTPUT CONNECTORS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB – 12 BITS)	13	REFERENCE
2	BIT 2 OUT	14	ANALOG INPUT
3	BIT 3 OUT (MSB) – 10 BITS	15	AMPLIFIER OUT
4	BIT 4 OUT	16	ZERO ADJUST
5	BIT 5 OUT (MSB – 8 BITS)	17	BIAS
6	BIT 6 OUT	18	–5V POWER
7	BIT 7 OUT	19	+5V POWER
8	BIT 8 OUT	20	GROUND
9	BIT 9 OUT	21	START CONVERT
10	BIT 10 OUT	22	E.O.C. (STATUS)
11	BIT 11 OUT	23	DATA VALID
12	BIT 12 OUT (LSB-ALL)	24	BCD OVERRANGE*

*NO CONNECTION FOR OTHER MODELS

NOTE:
For 8- and 10-bit models, do not connect to unused data output terminals since they have internal connections.

ABSOLUTE MAXIMUM RATINGS	ADC-EK8B/ 10B/12B	ADC-EK12DC/ DR/DM
I_{IN}	±10 mA	
I_{REF}	±10 mA	
Digital Input Voltage	−0.3V to V_{DD} + 0.3V	
V_{DD} − V_{SS}	18V	
Package Dissipation	500 mW	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	See Ordering Information
Storage Temp. Range	−65°C to +150°C
Package	24 Pin DIP

FOOTNOTES:
1. For the ADC-EK 12DM only. Initial gain error is ±5%. Gain. Tempco is ±40 ppm/°C typical, ±80 ppm/°C maximum and Zero Drift Tempco is 80 µV/°C.
2. ADC-EK 12DM outputs can sink and source 500 µA.
3. Supply Sensitivity given for V_{DD} = V_{SS} = 5V ±1V.

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V Supplies, R_{BIAS} = 100K, unless otherwise noted.

ANALOG INPUTS		
Type Analog Input	Single Ended	
Full Scale Input Current	+10 µA	
Reference Current	−20 µA	
DIGITAL INPUTS		
Logical "1" V_{IN}	3.5V minimum	
Logical "0" V_{IN}	1.5V maximum	
Start Convert Pulse	>3.5V for 500 nanoseconds minimum	
OUTPUTS		
Parallel Output Data	8, 10, 12 Lines	12 Lines and Overrange
Logic "1" Output Voltage	+4.5V minimum at −10 µA. +2.4V minimum at −360 µA[2]	
Logic "0" Output Voltage	+0.4 maximum at −360 µA[2]	
E.O.C. (Status)	High During Conversion, Low When Completed	
Data Valid	High When Data Valid. Low When Data Changing	
PERFORMANCE		
Resolution	8, 10, 12 Bits	3½ Digits
Coding	Straight Binary	BCD
Nonlinearity	½ LSB, maximum	0.025% maximum
Differential Nonlinearity	¼ LSB, typical, ½ LSB maximum	0.025% maximum
Diff. Nonlinearity Tempco	±2.5 ppm/°C typical, ±5 ppm/°C maximum	
No Missing Codes	Over Operating Temperature Range	
Initial Gain Error, Adj. to Zero	+5, −3% maximum[1]	
Gain Temperature Coefficient	±25 ppm/°C typical, ±75 ppm/°C maximum[1]	
Initial Zero Error, Adj. to Zero	±50 mV maximum	
Zero Drift Tempco	±50 µV/°C maximum[1]	
Conversion Time, maximum	1.8 milliseconds (8 Bits) 6 milliseconds (10 Bits) 24 milliseconds (12 Bits)	12 milliseconds (3½ Digits)
Power Supply Sensitivity	±0.05% of Full-Scale Gain[3]	
POWER REQUIREMENTS		
Voltage, Rated Performance	±5V dc	
Voltage Range, Operating	±3.5V dc to ±7V dc	
Supply Quiescent Current		
ADC-EK8B, EK12DC	±5.0 mA	
ADC-EK10B, EK12B, EK12DR	±2.5 mA maximum	
ADC-EK12DM	±3.5 mA maximum	

TECHNICAL NOTES

1. The ADC-EK series are CMOS devices and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive form or shorting all pins together with aluminum foil. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open circuits the zero adjust, reference, or start convert pins while power is on. It should also be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference, and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and +5% −3% tolerance on the converter scale factor, the actual resistor value can vary by almost ±10% R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and R_T be 1% of R_{OFF} (nominal). They should both be 100 ppm/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is to set the R_G and R_T to center of range and then choose 1% metal film resistor which gives the nearest fit at the full scale point 1111...111 for R_{IN} and one that gives the nearest fit to zero scale point 1000...000 for R_T.
3. To choose any intermediate scale values for R_{IN} and R_T or values of R_{REF} for other reference voltages, use the following formulas:

$$R_{IN}\,(\text{nominal}) = \frac{FSR}{10\ \mu A}$$

FSR is the full scale range or total input voltage span for the converter.

$$R_{OFF}\,(\text{nominal}) = \frac{V_{REF}}{5\ \mu A}$$

$$R_{REF}\,(\text{nominal}) = \frac{V_{REF}}{20\ \mu A}$$

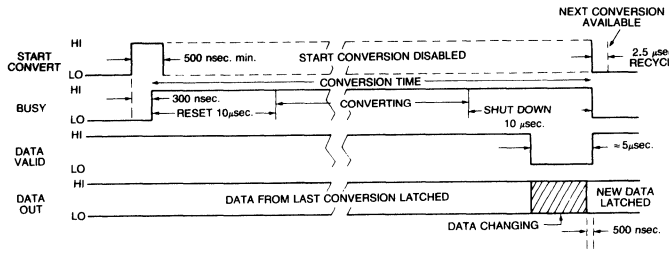
It is recommended that large full-scale voltage ranges be chosen such as 0 to +10V, 0 to +5V etc., in order to keep the error due to input offset voltage drift to a minimum.

4. The temperature stability of the ADC-EK converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF}, and V_{REF}. Since the converter is typically ±20 ppm/°C it is recommended that a 10 ppm/°C reference be used along with 10 ppm/°C metal film resistors for R_{IN}, R_{REF}, and R_{OFF} for best performance over temperature. On a statistical basis this would give about 28 ppm/°C stability for the complete converter.

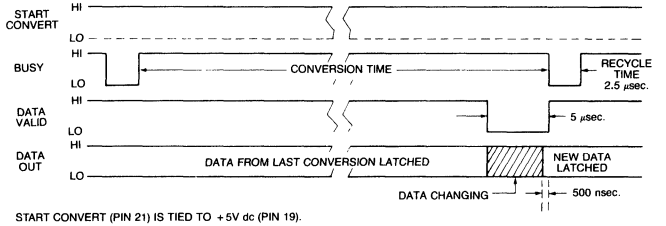
TECHNICAL NOTES (Cont'd)

5. Other passive components used with the converter may have tolerances as indicated here: R_C is a ±10% carbon composition resistor; C_C is a ±20% ceramic capacitor; C_{INT} is a ±10% glass or ceramic capacitor; R_{BIAS} is a ±10% carbon composition resistor; and the two zero adjust resistors are ±10% carbon composition type. It is recommended that two 0.1 μF bypass capacitors be used right at the power supply pins. C_{INT} should be connected as close as possible to pins 14 and 15 away from any noisy lines.
6. The start convert pulse initiates conversion on the low to high transition after which the conversion cycle cannot be interrupted and must run to completion.
7. Logic signals should not be routed under these devices or near the input reference, or zero adjust pins.
8. The unused data output pins on the 8- and 10-bit models should not be used for external connection points since they have internal connections to the converter.
9. All digital outputs will drive 2 low power TTL loads or 1 low power Schottky TTL load. They should not be overloaded as this will affect the performance of the converter.
10. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be ±0.04% for 8 bit models, ±0.01% for 10-bit models and ±0.0025% for 12-bit models.

CLOCKED OPERATION



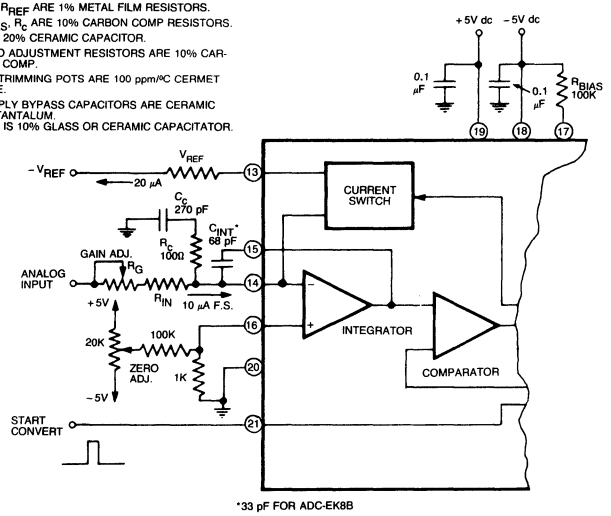
FREE RUNNING OPERATION



START CONVERT (PIN 21) IS TIED TO +5V dc (PIN 19).

CONNECTION FOR UNIPOLAR OPERATION

R_{IN}, R_{REF} ARE 1% METAL FILM RESISTORS.
R_{BIAS}, R_C ARE 10% CARBON COMP RESISTORS.
C_C IS 20% CERAMIC CAPACITOR.
ZERO ADJUSTMENT RESISTORS ARE 10% CARBON COMP.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.
C_{INT} IS 10% GLASS OR CERAMIC CAPACITOR.



*33 pF FOR ADC-EK8B

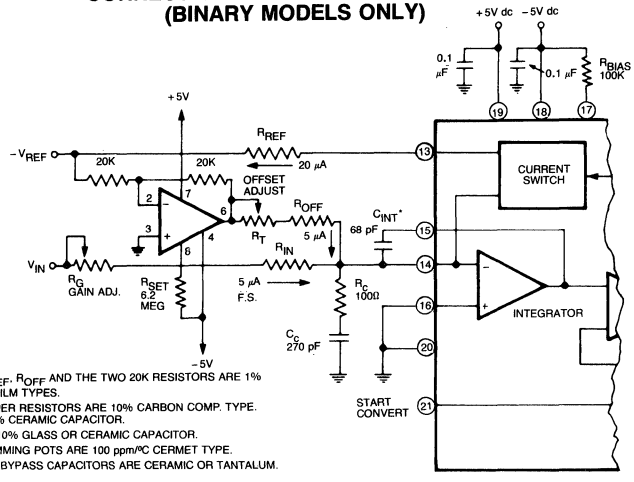
RESISTOR TABLES

UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOMINAL)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG.
0 TO +20V	±10V	2 MEG.

V_{REF}	R_{REF} (NOMINAL)	R_{OFF} (NOMINAL)
-1.22V	61K	244K
-2.5V	125K	500K
-6.4V	320K	1.28 MEG.

CONNECTIONS

CONNECTION OF BIPOLAR OPERATION (BINARY MODELS ONLY)

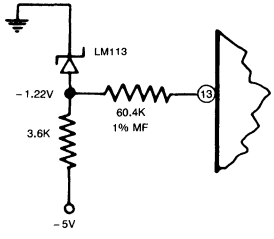


RIN, RREF, ROFF AND THE TWO 20K RESISTORS ARE 1% METAL FILM TYPES.
ALL OTHER RESISTORS ARE 10% CARBON COMP. TYPE.
CC IS 20% CERAMIC CAPACITOR.
CINT IS 10% GLASS OR CERAMIC CAPACITOR.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.

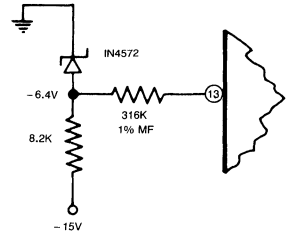
*33 pF FOR ADC-EK8B

REFERENCE CIRCUITS

1.22V BAND GAP REFERENCE USES EXISTING −5V SUPPLY



6.4V ZENER REFERENCE REQUIRES −15V SUPPLY



CODING TABLES

STRAIGHT BINARY

	8-BIT		10-BIT		12-BIT	
SCALE	0 TO +10V	CODE	0 TO +10V	CODE	0 TO +10V	CODE
FS − 1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1 LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

	8-BIT		10-BIT		12-BIT	
SCALE	±5V	CODE	±5V	CODE	±5V	CODE
+FS − 1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
−FS + 1 LSB	−4.96	0000 0001	−4.990	00 0000 0001	−4.9976	0000 0000 0001
−FS	−5.00	0000 0000	−5.000	00 0000 0000	−5.0000	0000 0000 0000

BCD

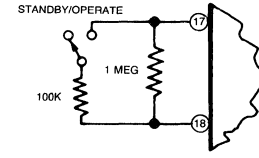
	FULL SCALE RANGE			
SCALE	0 TO +2V	0 TO +10V	0 TO +20V	CODE
FS − 1 LSB	+1.999V	+9.995V	+19.990V	1 1001 1001 1001
½ FS	+1.000	+5.000	+10.000	1 0000 0000 0000
1 LSB	+0.001	+0.005	+0.010	0 0000 0000 0001
0	0.000	0.000	0.000	0 0000 0000 0000

CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic high to the start convert input (pin 21) to give free-running operation.
2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or −FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000....000 and 000....001.
3. **Gain Adjustment.** Set the output of the reference source to +FS − 1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111....110 and 111....111.

   For BCD coding the output code should flicker between 1001 1001 1000 and 1001 1001 1001.

REDUCTION OF STAND-BY POWER



THIS REDUCES POWER CONSUMPTION TO ABOUT 200 µA DURING STANDBY.

ORDERING INFORMATION

MODEL NO.	OPER. TEMP. RANGE	PACKAGE
BINARY		
ADC-EK8B	0°C to +70°C	Plastic
ADC-EK10B	−25°C to +85°C	Cerdip
ADC-EK12B	−25°C to +85°C	Ceramic
BCD		
ADC-EK12DC	0°C to +70°C	Plastic
ADC-EK12DR	−25°C to +85°C	Ceramic
ADC-EK12DM	−55°C to +125°C	Ceramic

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADC-ET Series
Monolithic A/D Converters with Three-State Outputs

FEATURES

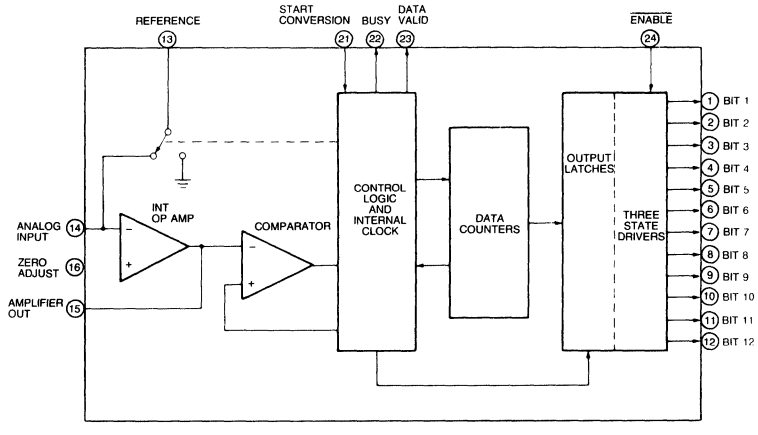
- **Monolithic CMOS**
- **Three-state outputs**
- **12-Bit accuracy**
- **No missing codes**
- **Low cost**
- **Microprocessor-compatible**

GENERAL DESCRIPTION

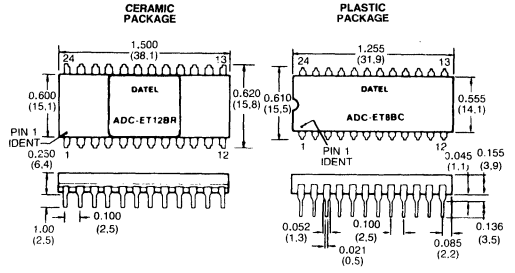
The ADC-ET series devices are low cost integrating A/D converters optimized for high accuracy, linearity and noise immunity. They operate at low power consumption, with sufficient speed to handle most industrial and instrumentation requirements. Discretely controllable three state outputs allow bus organized output connections making these units ideal for microprocessor interfacing.

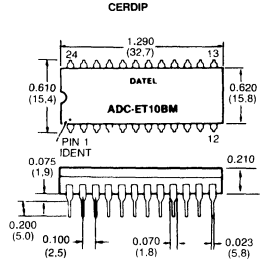
Fabricated with monolithic CMOS techniques, each device is housed in a single 24 pin dual in-line package. The converter consists of an integrating operational amplifier, comparator, current switch, internal clock, two counters, latching output buffers and control logic circuitry. Operation of the circuit requires only a few external passive components and connection to external reference and power supplies. Conversion is accomplished by an incremental charge balancing technique which assures high linearity and noise immunity, along with inherent monotonicity resulting in no missing codes. At the completion of a conversion, the binary coded result appears in parallel form on discretely controlled latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The controllable outputs may be switched to a high impedance or off state by holding the $\overline{\text{ENABLE}}$ high.

Conversion times are 1.8, 6, and 24 milliseconds for the 8-, 10- and 12-bit units respectively. Other typical specifications include linearity to ¼ LSB and a gain tempco of 25 ppm/°C. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10 μA full scale. Standard operating mode is unipolar but bipolar operation can be implemented by using an external operational amplifier to provide an offset current from the reference. Power requirement is ±5V dc at 2 mA which, for intermittent duty applications, may be reduced to only 200 μA during standby periods without affecting data in the output latches.



MECHANICAL DIMENSIONS INCHES (MM)





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB-12 BITS)	13	REFERENCE
2	BIT 2	14	ANALOG INPUT
3	BIT 3 (MSB-10 BITS)	14	AMPLIFIER OUT
4	BIT 4	16	ZERO ADJUST
5	BIT 5 (MSB-8 BITS)	17	BIAS
6	BIT 6	18	−5V POWER
7	BIT 7	19	+5V POWER
8	BIT 8	20	GROUND
9	BIT 9	21	START CONVERT
10	BIT 10	22	BUSY OUTPUT
11	BIT 11	23	DATA VALID
12	BIT 12 (LSB-ALL)	24	$\overline{\text{ENABLE}}$

NOTE: Do not connect unused data output pins on 8- and 10-bit models, they are internally connected to the converter.

ABSOLUTE MAXIMUM RATINGS	
I_{IN}	± 10 mA
I_{REF}	± 10 mA
Digital Input Voltage	−0.3V to V_{DD} +0.3V
V_{DD}-V_{SS}	18V
Package Dissipation	500 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, 5V Supplies, R_{BIAS} 100K, unless otherwise noted.

ANALOG INPUTS	
Type Analog Input	Single-Ended
Input Current Range	0 to +10 μA
Reference Current	−20 μA

DIGITAL INPUTS	
Logical "1" V_{IN}	3.5V minimum
Logical "0" V_{IN}	1.5V maximum
Start Convert Pulse Width	500 nanoseconds minimum
ENABLE Propagation Delay	500 nanoseconds

OUTPUTS	
Output Off State Current	0.1 μA typical, ± 10 μA maximum
Logic "1" Output Voltage	+4.5V minimum at −10 μA +2.4V minimum at −360 μA[4]
Logic "0" Output Voltage	+0.4V maximum at 360 μA[4]
Data Valid Output	High for Data Valid, Low When Loading
Busy Output	High During Conversion

PERFORMANCE	
Resolution	8, 10, 12 Bits
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary
Conversion Times	
8 Bits	1.8 milliseconds maximum
10 Bits	6 milliseconds maximum
12 Bits	24 milliseconds maximum
Nonlinearity	± ¼ LSB typical, ± ½ LSB maximum[1]
Differential Nonlinearity	± ¼ LSB typical, ± ½ LSB maximum
Diff. Nonlinearity Tempco	± 2.5 ppm/°C
No Missing Codes	Over Operating Temp. Range
Initial Gain Error, (Adj. to Zero)	± 5% maximum
Gain Temperature Coefficient	± 25 ppm/°C typical, ± 75 ppm/°C maximum[2]
Initial Zero Error (Adj. to Zero)	± 50 mV maximum
Zero Drift Tempco	± 50 μV/°C maximum[2]
Power Supply Sensitivity	± 0.05%/% maximum[3]

POWER REQUIREMENTS	
Voltage, Rated Performance	± 5V dc
Voltage Range, Operating	± 3.5V dc to ± 7V dc
Supply Quiescent Current	
C Suffix	± 5.0 mA maximum
R Suffix	± 2.5 mA maximum
M Suffix	± 3.5 mA maximum

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
C Suffix	0°C to +70°C
R Suffix	−25°C to +85°C
M Suffix	−55°C to +125°C
Package	
C Suffix	24 Pin Plastic DIP
R & M Suffix	24 Pin Ceramic DIP

FOOTNOTES:
1. Nonlinearity for model ADC-ET12BC only is typically ± ¼ LSB, ± ½ LSB maximum.
2. For M suffix units only gain tempco is typically 40 ppm/°C, 80 ppm/°C maximum and zero drift tempco is ± 80 μV/°C.
3. V_{DD} ± 1V, V_{SS} ± 1V.
4. M suffix logic outputs can sink and source 500 μA.

TECHNICAL NOTES

1. The ADC-ET series are CMOS devices and must be properly handled to prevent damage due to static discharge. Proper anti-static precautions should be taken, including storage and transport in anti-static containers or conductive foam, and grounding of work stations, handling equipment and personnel. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open the circuitry for the zero adjust, reference or start convert pins while the power is on. It should be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference and offset resistors are given in the resistor table. Due to the possible ± 5% tolerance of the external reference and the +5%, −3% tolerance of the converter scale factor, the actual resistor value can vary by almost ± 10%. R_G and R_T in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that R_G be 1% of R_{IN} (nominal) and that R_T be 1% of R_{OFF} (nominal). They should both be 100 ppm/°C cermet trimming pots. The recommended procedure for selecting R_{IN} and R_{OFF} is set to R_G and R_T to the center of their ranges and choose a 1% metal film resistor which gives the closest fit at the full scale point 1111....111 for R_{IN} and one that gives the closest fit to the zero scale point 0000...000 for R_T.
3. The temperature stability of the ADC-ET converters depends directly on the converter itself, R_{IN}, R_{REF}, R_{OFF} and V_{REF}. Since the converter is typically ± 25 ppm/°C. It is recommended that a 10 ppm/°C reference be used along with 10 ppm/°C metal film resistors for R_{IN}, R_{REF} and R_{OFF} for best performance over temperature.
4. Passive components used with the converter may have tolerances as indicated here: C_c is a ± 20% ceramic capacitor; C_{INT} is a ± 10% glass or ceramic capacitor; R_{c1}, R_{BIAS} and the two zero adjust resistors are ± 10% carbon composition type.
5. It is recommended that two 0.1 μF bypass capacitors be used at the power supply pins as shown in the connection diagram. C_{INT} should be connected as close as possible to pins 14 and 15 and as far as possible from any noisy lines.
6. Logic signals should not be routed under these devices or near the input, reference or zero adjust pins.
7. All digital outputs will drive two low power TTL loads or one low power Schottky TTL load. The outputs should not be overloaded as this will affect the performance of the converter.

TECHNICAL NOTES (Cont'd)

8. It should be noted that there is a propagation delay of approximately 500 nanoseconds between the time ENABLE changes state and the time that the outputs change state.
9. Two's complement coding can be implemented by inverting the MSB signal.
10. I_{IN} and I_{REF}, pins 14 and 13 respectively, connect to the summing junction of an operational amplifier which requires a current input. Voltage sources cannot be attached directly to them, but must be buffered by external resistors. Refer to Test Circuit Diagrams. Analog input can be any positive voltage when applied through the proper scaling resistor.
11. Conversion accuracy is directly dependent on V_{REF}. In order to avoid degrading accuracy, V_{REF} voltage regulation must be $\pm 0.04\%$ for 8-bit models, $\pm 0.01\%$ for 10-bit models and $\pm 0.0025\%$ for 12-bit models.

DESCRIPTION OF OPERATION

When the START CONVERT input is strobed with a positive pulse of at least 500 nanoseconds duration, the busy line latches high and a start up cycle of approximately 10 microseconds begins, during which the integrating capacitor is discharged and both counters are reset. Conversion begins at the end of an internal reset pulse.

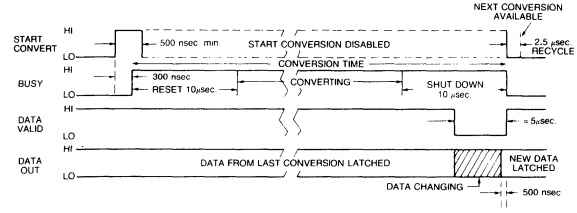
During conversion, the sum of a continuous current, I_{IN} and pulses of an inversely signed reference current I_{REF}, is integrated. I_{IN} is proportional to the analog input voltage and I_{REF} is proportional to the reference voltage. A pulse of I_{REF} is applied as required to maintain the summing input of the integrating operational amplifier near zero. The total number of pulses of I_{REF} required to maintain the summing input near zero is counted and the binary coded result is latched into the outputs at the end of conversion.

The end of conversion is signaled by a pulse generated by the clock counter or by the data counter when an overflow condition occurs; this pulse disables further inputs into both counters and begins a 10 microseconds shutdown cycle. During the shutdown cycle, Data Valid goes low for 5 microseconds, while the result of the latest conversion is being transferred to the outputs. Until transfer is complete, the data at the outputs is not valid. At the end of the shutdown cycle, Data Valid goes high indicating that the outputs are latched with the result of the last conversion, and the Busy Output goes low indicating the completion of the conversion cycle and the availability of the converter for the next conversion.

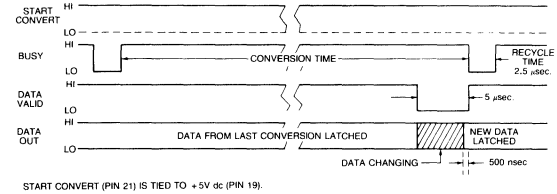
When the converter is employed in a free-running mode, the START CONVERT input is held high (simply connect pin 21 to pin 19), the Busy Output will go low for aproximately 2.5 microseconds to mark the completion and initiation of consecutive conversion cycles. It should be noted that once conversion is initiated, the cycle cannot be interrupted; the START CONVERT pin is disabled when the Busy Output is high, and thus its logic state has no effect until completion of the conversion cycle. After the completion of a conversion, the output data remains valid for as long as power is applied to the circuit, or until Data Valid goes low at the end of a conversion.

TIMING DIAGRAMS

CLOCKED OPERATION



FREE RUNNING OPERATION



START CONVERT (PIN 21) IS TIED TO +5V dc (PIN 19).

CODING TABLES

STRAIGHT BINARY

	8 BIT		10 BIT		12 BIT	
SCALE	0 TO + 10V	CODE	0 TO +10V	CODE	0 TO +10V	CODE
FS-1 LSB	+9.96V	1111 1111	+9.990V	11 1111 1111	+9.9976V	1111 1111 1111
½ FS	+5.00	1000 0000	+5.000	10 0000 0000	+5.0000	1000 0000 0000
1LSB	+0.04	0000 0001	+0.010	00 0000 0001	+0.0024	0000 0000 0001
0	0.00	0000 0000	0.000	00 0000 0000	0.0000	0000 0000 0000

OFFSET BINARY

	8 BIT		10 BIT		12 BIT	
SCALE	±5V	CODE	±5V	CODE	±5V	CODE
+FS-1 LSB	+4.96V	1111 1111	+4.990V	11 1111 1111	+4.9976V	1111 1111 1111
0	0.00	1000 0000	0.000	10 0000 0000	0.0000	1000 0000 0000
-FS + 1 LSB	-4.96	0000 0001	-4.990	00 0000 0001	-4.9976	0000 0000 0001
-FS	-5.00	0000 0000	-5.000	00 0000 0000	-5.0000	0000 0000 0000

RESISTOR TABLES

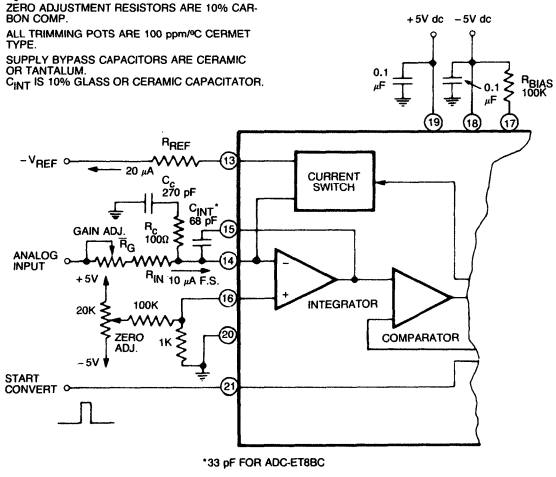
UNIPOLAR RANGE	BIPOLAR RANGE	R_{IN} (NOMINAL)
0 TO +2V	±1V	200K
0 TO +5V	±2.5V	500K
0 TO +10V	±5V	1 MEG
0 TO +20V	±10V	2 MEG

V_{REF}	R_{REF} (NOMINAL)	R_{OFF} (NOMINAL)
-1.22V	61K	244K
-2.5V	125K	500K
-6.4V	320K	1.28 MEG.

CONNECTIONS AND CALIBRATION

CONNECTION FOR UNIPOLAR OPERATION

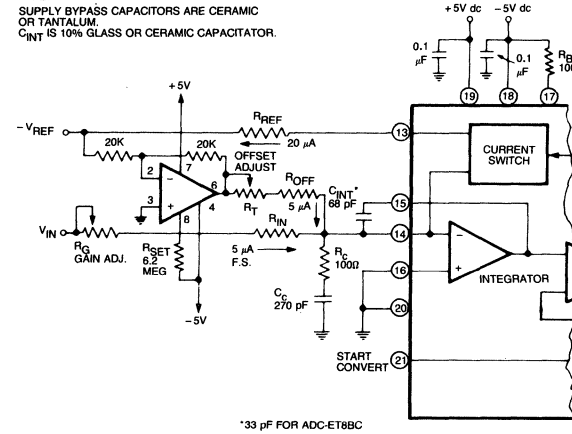
R_{IN}, R_{REF} ARE 1% METAL FILM RESISTORS.
R_{BIAS}, R_C ARE 10% CARBON COMP RESISTORS.
C_C is 20% CERAMIC CAPACITOR.
ZERO ADJUSTMENT RESISTORS ARE 10% CARBON COMP.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.
C_{INT} IS 10% GLASS OR CERAMIC CAPACITATOR.



*33 pF FOR ADC-ET8BC

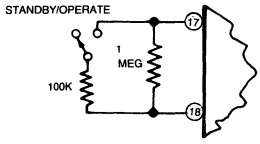
CONNECTION FOR BIPOLAR OPERATION

R_{IN}, R_{REF} ARE 1% METAL FILM RESISTORS.
R_{BIAS}, R_C ARE 10% CARBON COMP RESISTORS.
C_C is 20% CERAMIC CAPACITOR.
ZERO ADJUSTMENT RESISTORS ARE 10% CARBON COMP.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.
C_{INT} IS 10% GLASS OR CERAMIC CAPACITATOR.



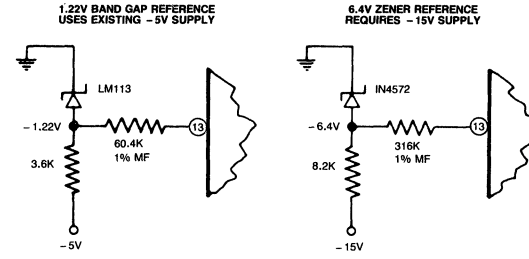
*33 pF FOR ADC-ET8BC

REDUCTION OF STAND-BY POWER



THIS REDUCES POWER CONSUMPTION TO ABOUT 200 µA DURING STANDBY.

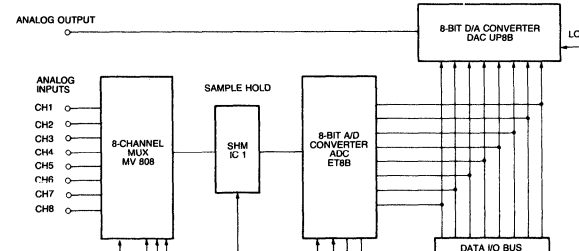
REFERENCE CIRCUITS



CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic high to the start convert input (pin 21) to give free-running operation.
2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or −FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000....000 and 000....001.
3. **Gain Adjustment.** Set the output of the reference source to +FS − 1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111....110 and 111....111.

LOW COST MICROPROCESSOR A/D, D/A INTERFACE



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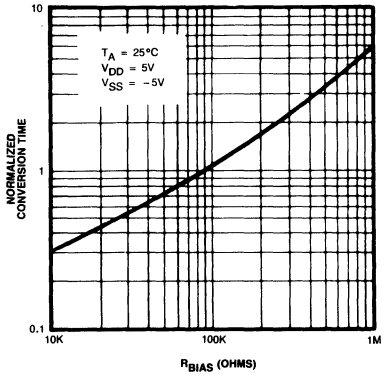
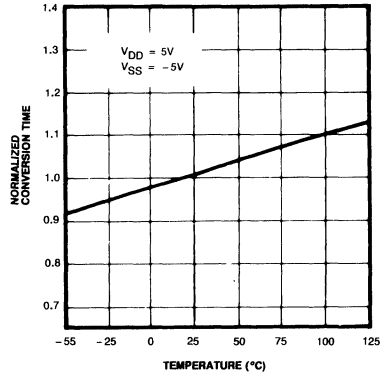
TYPICAL PERFORMANCE CURVES

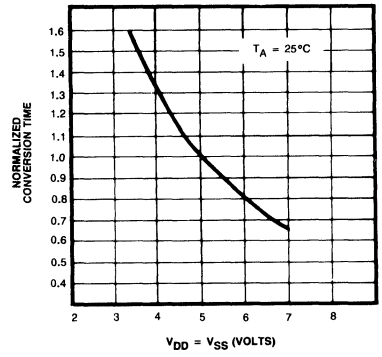
CONVERSION TIME VS. R_{BIAS}



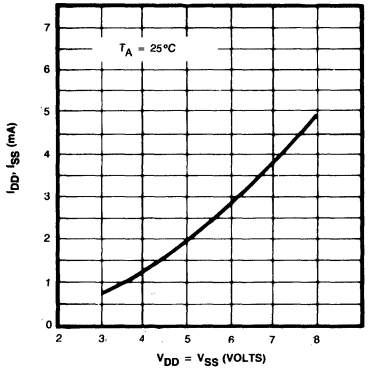
CONVERSION TIME VS. TEMPERATURE



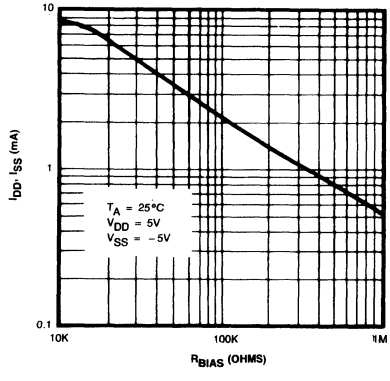
CONVERSION TIME VS. SUPPLY VOLTAGE



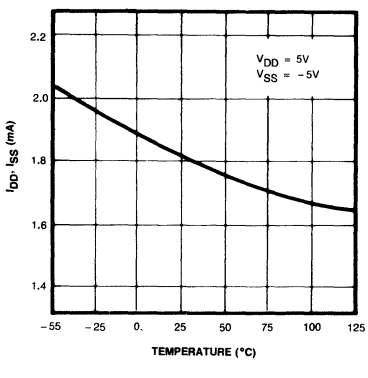
SUPPLY CURRENT VS. SUPPLY VOLTAGE



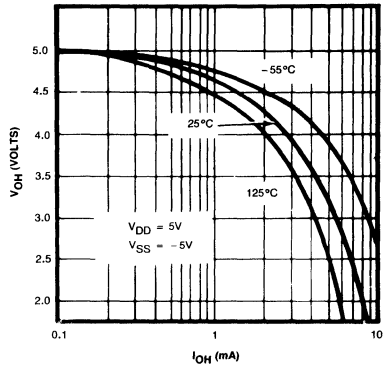
SUPPLY CURRENT VS. R_{BIAS}



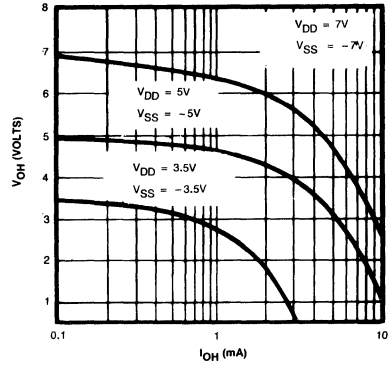
SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SOURCE CURRENT VS. TEMPERATURE

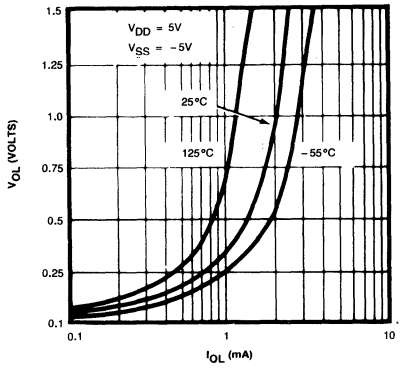


OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE

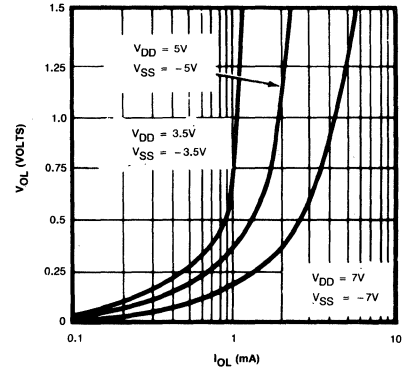


TYPICAL PERFORMANCE CURVES

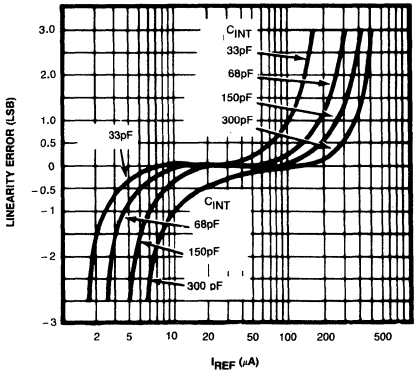
OUTPUT SINK CURRENT VS. TEMPERATURE



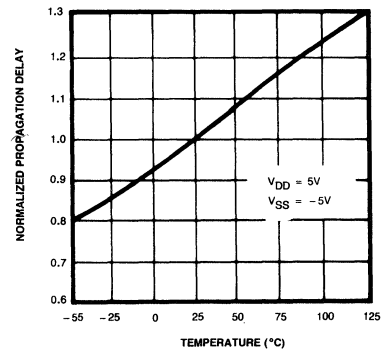
OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE



LINEARITY VS. I_{REF}



THREE-STATE PROPAGATION DELAY



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	PACKAGE
ADC-ET8BC	0°C to +70°C	Plastic
ADC-ET8BM	−55°C to +125°C	Cerdip
ADC-ET10BC	0°C to +70°C	Plastic
ADC-ET10BM	−55°C to +125°C	Cerdip
ADC-ET12BC	0°C to +70°C	Plastic
ADC-ET12BR	−25°C to +85°C	Ceramic
ADC-ET12BM	−55°C to +125°C	Ceramic

ADC-HC12B
12-Bit, Low-Power A/D Converter

1

FEATURES

- **Single supply operation**
- **Automatic standby mode control**
- **Low power consumption**
- **Six input ranges**
- **MIL temperature ranges available**

GENERAL DESCRIPTION

The ADC-HC is a complete, 12-bit, low-power, analog-to-digital converter utilizing CMOS technology. This hybrid IC incorporates active laser trimming of highly stable thin-film resistors to provide module performance with IC price, size and reliability.

The device is ideal for portable and remote applications such as seismology, oceanography, meteorology, and pollution monitoring. Other key applications include military and aerospace, requiring wide operating temperature ranges and high reliability.

The ADC-HC converter can operate from either a single +9V dc to +15V dc power source (interrupt power mode) or from a ±9V dc to ±15V dc power source (continuous power mode) at a maximum conversion rate of 3.3 kHz.

A key feature of this unit when operating in the interrupt power mode is the extremely low quiescent power consumption (less than 10 μA at 12V, 25°C).

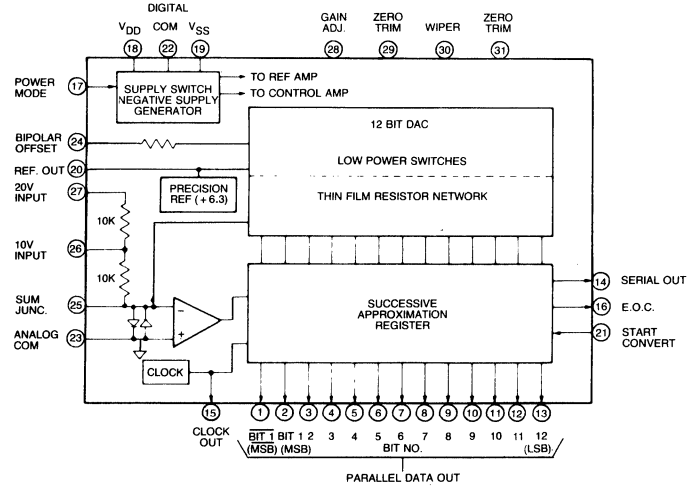
Upon receipt of a convert command, the analog circuitry of the converter is energized and stabilizes in 50 microseconds. A complete conversion is performed at which time the EOC goes low, turning off the analog circuitry, and returns to its quiescent state. The digital data remains valid until it is updated by the next conversion.

Power consumption is a function of conversion rate. For 100, 1K and 2K conversions per second, the average power drain is approximately 3.5, 26 and 50 milliwatts respectively.

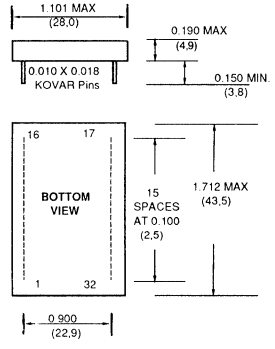
Six input voltage ranges are provided by external pin connection: 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V, and ±10V dc. Nonlinearity is specified at ±½ LSB maximum with a gain tempco of ±30 ppm/°C. Output coding is straight binary, offset binary or 2's complement. Serial data is also brought out.

The converters are cased in 32-pin DIP packages. Models are available for two different operating temperature ranges: 0 to +70°C, and −55 to +125°C. High reliability versions of each temperature range are also available.

CAUTION: The ADC-HC Series are CMOS devices and should be handled carefully to prevent static charge pickup which might damage the devices. The devices should be kept in the shipping containers until ready for installation.



MECHANICAL DIMENSIONS INCHES (MM)



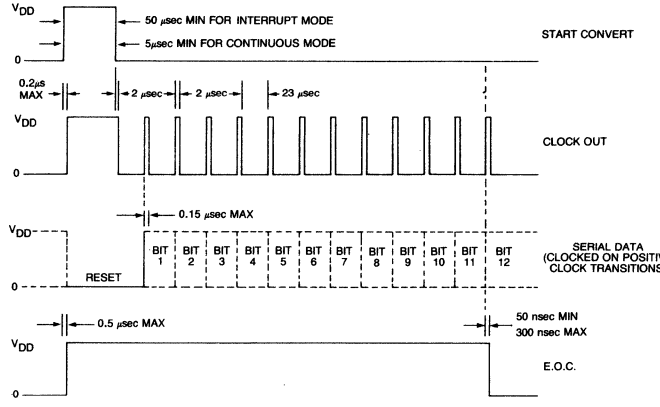
NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01

INPUT/OUTPUT CONNECTIONS

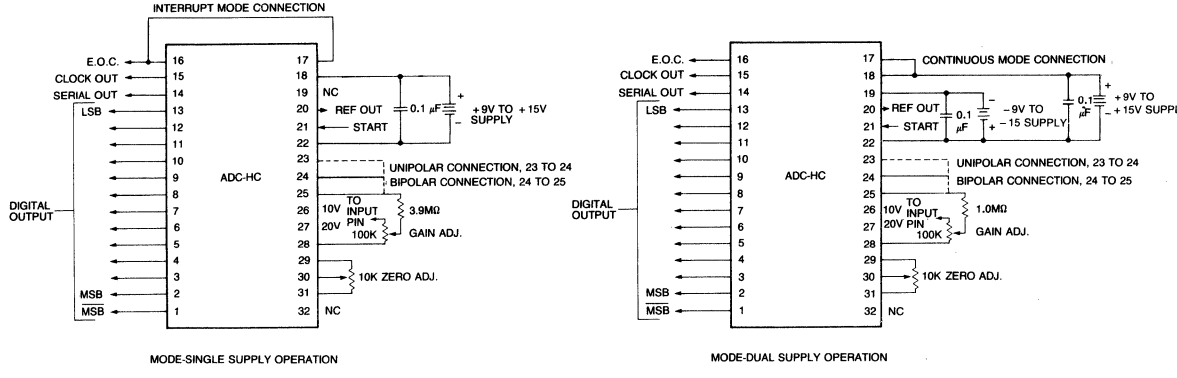
PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	17	POWER MODE
2	BIT 1 (MSB)	18	V_{DD}
3	BIT 2	19	V_{SS}
4	BIT 3	20	REF OUT
5	BIT 4	21	START CONVERT
6	BIT 5	22	DITITAL COM.
7	BIT 6	23	ANALOG COM.
8	BIT 7	24	BIPOLAR OFFSET
9	BIT 8	25	SUM. JUNC.
10	BIT 9	26	10V INPUT
11	BIT 10	27	20V INPUT
12	BIT 11	28	GAIN ADJ.
13	BIT 12 (LSB)	29	ZERO TRIM
14	SERIAL OUT	30	ZERO ADJ (WIPER)
15	CLOCK OUT	31	ZERO TRIM
16	E.O.C. (STATUS)	32	N.C.

CONNECTIONS AND CALIBRATION

ADC-HC TIMING DIAGRAM



CONNECTIONS DIAGRAM



OUTPUT CODING

INPUT VOLTAGE RANGE			CODING
UNIPOLAR			STRAIGHT BINARY
0 to +20V	0 to +10V	0 to +5V	MSB LSB
+FS – 1 LSB	+19.9951	+9.9976	+4.9988	1111 1111 1111
+½FS	+10.0000	+5.0000	+2.5000	1000 0000 0000
+1 LSB	+0.0049	+0.0024	+0.0012	0000 0000 0001
ZERO	0.0000	0.0000	0.0000	0000 0000 0000

BIPOLAR			OFFSET BINARY*
±10V	±5V	±2.5V	MSB LSB
+FS – 1 LSB	+9.9951	+4.9976	+2.4988	1111 1111 1111
+½FS	+5.0000	+2.5000	+1.2500	1100 0000 0000
+1 LSB	+0.0049	+0.0024	+0.0012	1000 0000 0001
ZERO	0.0000	0.0000	0.0000	1000 0000 0000
–FS – 1 LSB	–9.9951	–4.9976	–2.4988	0000 0000 0001
–FS	–10.0000	–5.0000	–2.5000	0000 0000 0000

*For 2's COMPLEMENT, MSB is inverted, use $\overline{\text{MSB}}$ (pin 1)

INPUT PIN CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT THESE PINS TOGETHER
0 to +5V	26	23 to 24, 25 to 27
0 to +10V	26	23 to 24
0 to +20V	27	23 to 24
±2.5V	26	24 to 25, 25 to 27
±5V	26	24 to 25
±10V	27	24 to 25

CALIBRATION PROCEDURE

1. Connect the converter as shown in the Connection Diagram Use the Input Pin Connections table for the desired inpu voltage range. Apply start conversion pulses to start pin.
2. **Zero and Offset Adjustment**
   Apply a precision voltage reference source between the selected analog input range and ground. Adjust the output o the reference source to +½ LSB. Adjust the zero trimmin potentiometer so that the output code flickers equally be tween 0000 0000 0000 and 0000 0000 0001 for unipolar an 1000 0000 0000 and 1000 0000 0001 for bipolar mode.
3. **Full Scale Adjustment**
   Change the output of the precision reference source fo +FS – 1½ LSB. Adjust the gain trimming potentiometer s that the output code flickers equally between 1111 111 1110 and 1111 1111 1111.
4. For bipolar operation, the offset and Full Scale Adjustme are interactive. Repeat the offset and Full Scale Adjustme procedure as necessary until both points are set.

ABSOLUTE MAXIMUM RATINGS	
Positive Supply (V_{DD})	+18V
Negative Supply (V_{SS})	−18V
Analog Inputs	±25V
Digital Inputs	0 to V_{DD}

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BGC, BMC) −55°C to +125°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounces (14 g.)

1

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±12V, unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V, 0 to +20V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance	5K (0 to +5V, ±2.5V) 10K (0 to +10V, ±5V) 20K (0 to +20V, ±10V)
Start Convert, Interrupt Mode	Positive Pulse with duration of 50 microseconds minimum
Start Convert, Continuous Mode	Positive Pulse with duration of 5 microseconds minimum
V_{IL} (Logic "0")	0.3 V_{DD} maximum
V_{IH} (Logic "1")	0.7 V_{DD} minimum
Input Current	30 pA
Input Capacitance	15 pF

OUTPUTS	
Parallel Output Data	12 parallel lines of data, held until next conversion command
V_{OL} (Logic "0")	0V, −2.0 mA
V_{OH} (Logic "1")	V_{DD}, +4.0 mA
All Digital Outputs	CMOS Compatible
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary, 2's Complement
Serial Output	NRZ successive decision pulses out MSB first, Straight Binary or Offset Binary
Clock Output	Train of positive going (V_{DD}) 25 microseconds pulses, 40 kHz
E.O.C. (Status)	Conversion Status Signal, Logic "1" during reset and conversion, Logic "0" when conversion complete (data valid)

PERFORMANCE	
Resolution	12 Bits
Nonlinearity	±½ LSB maximum
Differential Nonlinearity	±½ LSB maximum
Gain Error	Adjust to zero
Offset or Zero Error	Adjust to zero
Gain Tempco	±30 ppm/°C maximum
Offset Tempco	±20 ppm/°C of FSR maximum
Zero Tempco	±10 ppm/°C of FSR
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR
No Missing Codes	Guaranteed over operating temperature range
Conversion Time	300 microseconds maximum
Throughput Time	305 microseconds maximum continuous power mode 350 microseconds maximum interrupt power mode
Power Supply Rejection	003%/% Supply

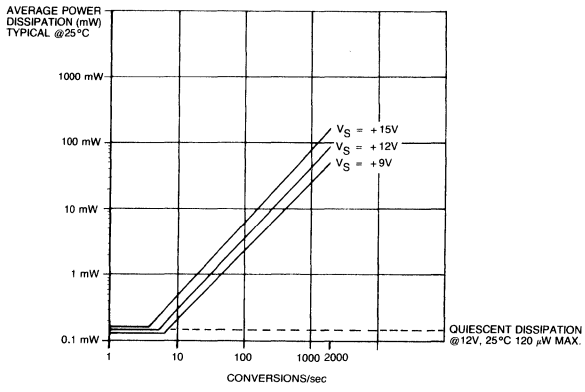
POWER REQUIREMENTS	
Continuous Power Mode	
V_{DD}	+9.0V to +15.0V
V_{SS}	−9.0V to −15.0V
nterrupt Power Mode V_{DD}	+9V to +15.0V
ower Consumption, Continuous Mode	165 mW typical, 200 mW maximum
Quiescent Mode	150 µW maximum, 15 µW typical

TECHNICAL NOTES

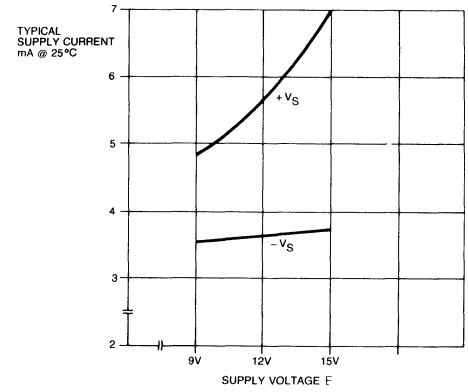
1. The ADC-HC contains CMOS components and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive foam or shorting all pins together with aluminum foil. Do not connect in circuit under "power on" conditions. Digital signals should be applied after the converter's power has been turned on.
2. For single supply (+12V nominal) or dual supply (±12V nominal) operation, bypass the power input pins to ground with a 0.1 µF ceramic capacitor. It is not critical that the supplies be balanced.
3. Analog and digital grounds should be kept separate whenever possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Common (Pin 23) and Digital Ground (Pin 22) are not connected internally and must be tied together externally.
4. The ADC-HC can operate from either a single or dual supply. When using dual supplies, tie POWER MODE (Pin 17) to V_{DD} (Pin 18). In this continuous power mode, an A/D conversion will take place when a 5 microseconds or greater positive going pulse is applied to START CONVERT (Pin 21). For single supply operation (interrupt power mode), tie Power Mode (Pin 17) to E.O.C. (Pin 16). When EOC goes low, the converter is switched to standby mode (power is disconnected to analog circuitry) and digital output data becomes valid and remains valid until next start pulse is applied. Upon receipt of a 50 microseconds minimum, 500 microseconds maximum pulse on START CONVERT (Pin 21), the converter will stabilize, make a complete conversion and return to standby mode.
5. Digital output codes are listed in coding tables. Parallel data is valid when EOC is in low state. This data can be transferred into latches during a logic "1" to logic "0" transition of the EOC line. Serial data out (Pin 14) is in NRZ (non-return to zero) format. This data is guaranteed valid in a 50 nanoseconds to 300 nanoseconds time frame after the positive edge of the clock. All digital inputs and outputs are CMOS compatible. See application notes for CMOS-TTL interface.
6. REF OUT (Pin 20) is a 6.3V ±5% internal reference pin connection.
7. For zero or offset and gain adjustment, refer to connections and calibration notes. The trim pots should be located as close as possible to the converter to avoid noise pickup. Zero point is always adjusted first, followed by gain, the adjustment with analog input at the most positive end of analog range. The range of the OFFSET (ZERO) ADJ. is ±15 mV. The range of GAIN ADJ. is 0.1% of full scale range can also be increased by decreasing the value of the series resistor (3.9 MΩ nominal). Potentiometer values are 10K and should be 100 ppm/°C ceramic type (such as DATEL's TP series).

APPLICATIONS

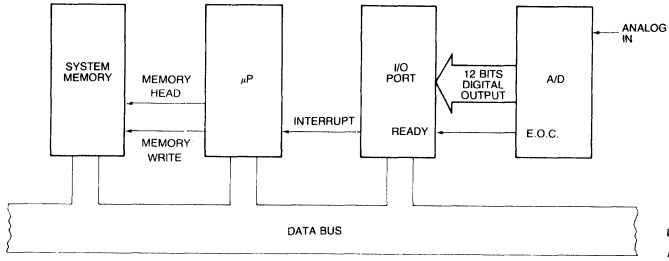
ADC-HC INTERRUPT POWER MODE



ADC-HC CONTINUOUS POWER MODE

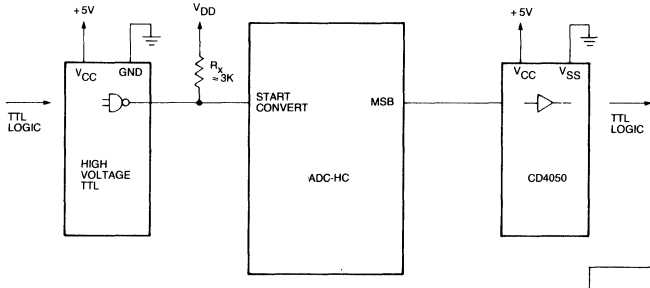


LOW POWER MICRO-PROCESSOR INTERFACE



SYSTEMS COMPONENTS	MANUFACTURE	MODEL	DATA BITS	TYPE
LOW POWER MICROPROCESSOR	RCA	CDP1802	8	CMOS
	INTERSIL	IM6100	12	CMOS
A/D CONVERTER	DATEL SYSTEMS	ADC-HC	12	CMOS

TTL-CMOS INTERFACE



CMOS and TTL logic are not compatible due to different threshold levels. They can, however, be interfaced by simple techniques.

The START CONVERT (Pin 21) can be driven directly from an open collector, high voltage TTL gate. Resistor Rx is used to source current and bring the TTL output up to the CMOS threshold level. Typical values of Rx are 3.3K to 10K ohms.

CMOS to TTL interface requires sufficient sink current in the low state. The CD4049 (inverting) and CD4050 (noninverting) buffers, powered from +5V logic supply can accept input voltage swings of +5 to +15V from the CMOS system. Each buffer gate can drive at least one input from any TTL family.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
ADC-HC12BMC	0 to +70°C	Hermeti
ADC-HC12BMM	−55°C to +125°C	Hermeti

ACCESSORIES

Part Number	Description
TPK 10K (10K ohms)	Trimming Potentiometers
TP 100K (100K ohms)	

For military devices compliant with MIL-STD-883, contact DATEL

ADC-HS12B
12-Bit Microelectronic A/D Converter With Sample-Hold

1

FEATURES

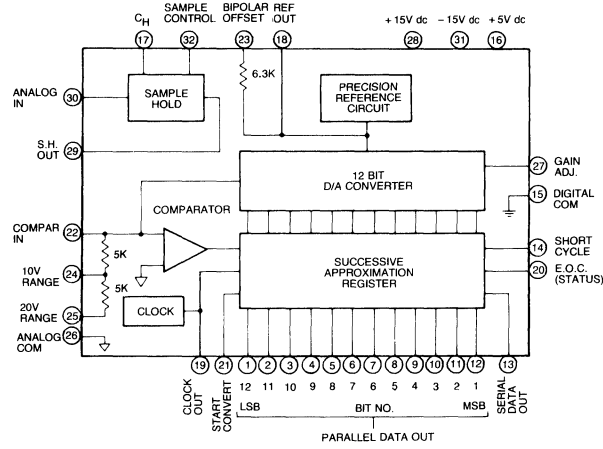
- **12-Bit resolution**
- **Internal sample and hold**
- **6 Microseconds acquisition time**
- **9 Microseconds conversion time**
- **Programmable input ranges**
- **Parallel & serial outputs**

GENERAL DESCRIPTION

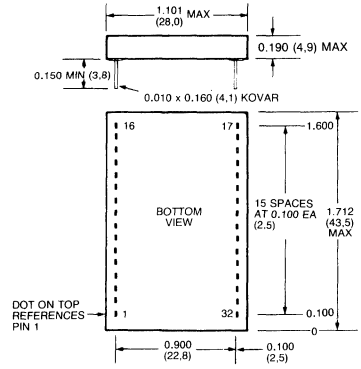
The ADC-HS12B is a high performance 12-bit hybrid A/D converter with a self-contained sample-hold. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The internal sample-hold has a 6 microseconds acquisition time for a full 10V dc input change; the A/D converter has a fast 9 microseconds conversion time. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. Input impedance to the sample-hold is 100 megohms. Output coding is complementary binary for unipolar operation and complementary offset binary for bipolar operation, with both parallel and serial outputs brought out.

The ADC-HS12B uses a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12-bit successive approximation register, a clock and a monolithic sample-hold.

Other features include a gain tempco of 20 ppm/°C maximum and differential nonlinearity tempco of ±2 ppm/°C; there are no missing codes over the operating temperature range. The package is a miniature 32 pin triple spaced DIP and different models are offered for each of the operating temperature ranges: 0 to 70°C and −55 to +125°C. Power supply requirement is ±15V dc and +5V dc. High reliability versions are also available.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	C_H
2	BIT 11 OUT	18	REF OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ.
12	BIT 1 OUT (MSB)	28	+15V POWER
13	SERIAL DATA OUT	29	S.H. OUTPUT
14	SHORT CYCLE	30	ANALOG IN
15	DIGITAL COM	31	−15V POWER
16	+5V POWER	32	SAMPLE CONTROL

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, pin 28	+18V
Negative Supply, pin 31	−18V
Logic Supply Voltage, pin 16	+5.5V
Digital Input Voltage, pins 14, 21, 32	+5.5V
Analog Input Voltage, pin 30	±15V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance[1]	100 megohms
Input Bias Current[1]	50 nA typical, 200 nA max.
Start Conversion	2V min. to +5.5V max. positive pulse with 100 nsec. duration min. Rise and fall times <30 nsec. Logic high to low transition resets converter and initiates next conversion. Loading: 2 TTL loads
Sample Control Input	Logic high = hold Logic low = sample Loading: 1 TTL load

OUTPUTS[2]	
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary
Serial Output Data	Successive decision pulses out, NRZ format. MSB first
End of Conversion (status)	Conversion status signal. Output is logic high during reset and conversion and low when conversion is complete.
Clock Output	Train of positive going +5V, 100 nsec. pulses at 1.5 MHz rate.

SAMPLE-HOLD PERFORMANCE[3]	
Input Offset Drift	25 µV/°C
Acquisition Time, 10V to 0.01%	6 µsec.
Bandwidth	1 MHz
Aperture Delay Time	100 nsec.
Aperture Uncertainty Time	10 nsec.
Sample to Hold Error	2.5 mV max.
Hold Mode Droop	200 nV/µsec. max.
Hold Mode Feedthrough	0.01% max.

CONVERTER PERFORMANCE	
Resolution	12 bits (1 part in 4096)
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±¾ LSB max.
Temp. Coefficient of Gain	±20 ppm/°C max.
Temp. Coefficient of Zero, unipolar	±5 ppm/°C of FSR max.
Temp. Coefficient of Offset, bipolar	±10 ppm/°C of FSR max.
Differential Nonlinearity Tempco	±2 ppm/°C of FSR
Missing Codes	None over oper. temp. range
Conversion Time	9 µsec. max.
Power Supply Rejection	0.004%/% max.

POWER REQUIREMENTS	
Power Suppy Voltage	+15V dc ±0.5V at 20 mA −15V dc ±0.5V at 25 mA +5V dc ±0.25V at 85 mA ±12V dc, +5V dc operation[4]

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to 70°C (BMC) −55°C to +125°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounce (14 grams)

FOOTNOTES:

1. For sample-hold input
2. All digital outputs can drive 2 TTL loads
3. For 1000 pF external hold capacitor
4. For ±12V dc or +5V dc operation, contact the factory

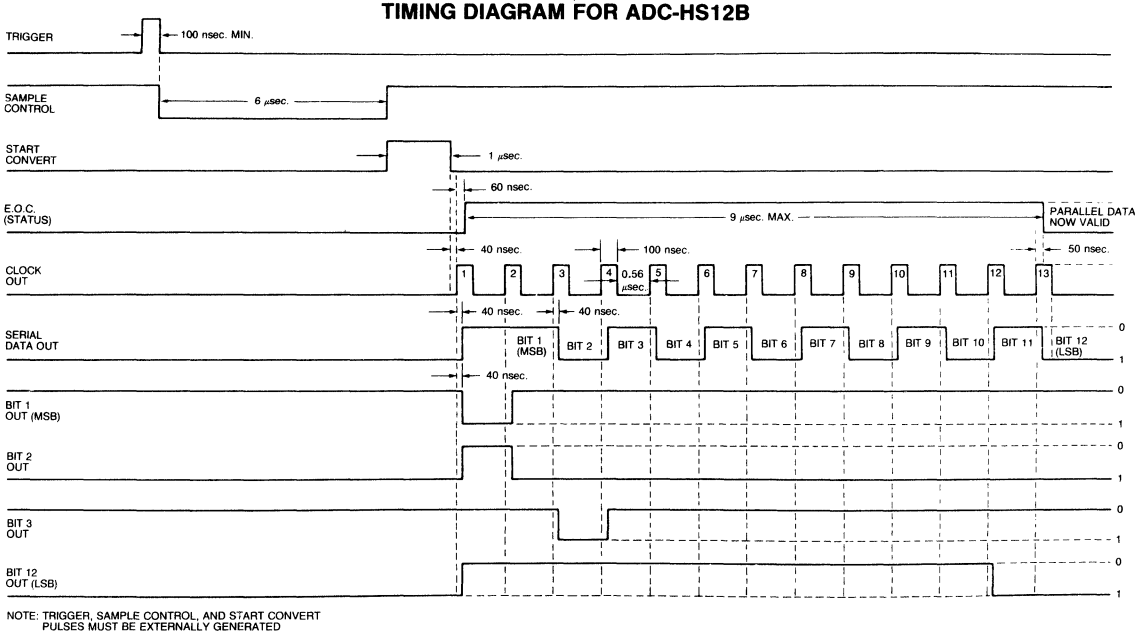
TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01 µF ceramic capacitor in parallel with a 1 µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 1 µF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01 µF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V dc ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10k and 100k ohms and should be 100 ppm/°C cermet types (such as DATEL's TP series). The adjustment range is ±0.5% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. Calibration of the ADC-HS12B is performed with the sample-hold connected and operating dynamically. This results in adjusting out the sample-hold errors along with the A/D converter. For slow throughput applications it is recommended that a 0.01 µF hold capacitor be used for best accuracy. With this value the acquisition time becomes 25 microseconds and the externa timing must be adjusted accordingly.
4. The recommended timing shown in the Timing Diagram allows 6 microseconds for the sample-hold acquisition and then 1 microsecond after the sample-hold goes into the hold mode to allow for output settling before the A/D begins its conversion cycle.
5. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions in the Table.
6. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary. In cases where bipolar coding of offset binary is required, this can be achieved by inverting the analog input to the converter (using an operational amplifier connected for gain of −1.0000). Th

converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS − 1 LSB gives 1111 1111 1111.

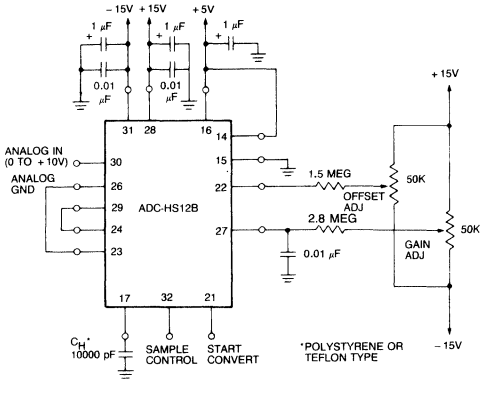
7. These converters dissipate 1.81 watts maximum of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
8. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock. The pulse width of the external clock should be between 100 nanoseconds and 300 nanoseconds. Each N bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

TIMING DIAGRAM FOR ADC-HS12B

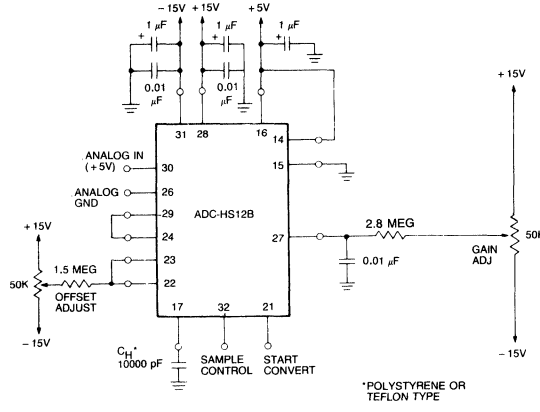


NOTE: TRIGGER, SAMPLE CONTROL, AND START CONVERT PULSES MUST BE EXTERNALLY GENERATED

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, ±5V



CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING		
0 TO +10V	0 TO +5V	MSB		LSB
+9.9976V	+4.9988V	0000	0000	0000
+8.7500	+4.3750	0001	1111	1111
+7.5000	+3.7500	0011	1111	1111
+5.0000	+2.5000	0111	1111	1111
+2.5000	+1.2500	1011	1111	1111
+1.2500	+0.6250	1101	1111	1111
+0.0024	+0.0012	1111	1111	1110
0.0000	0.0000	1111	1111	1111

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		
±10V	±5V	±2.5V	MSB		LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000
+7.5000	+3.7500	+1.8750	0001	1111	1111
+5.0000	+2.5000	+1.2500	0011	1111	1111
0.0000	0.0000	0.0000	0111	1111	1111
−5.0000	−2.5000	−1.2500	1011	1111	1111
−7.5000	−3.7500	−1.8750	1101	1111	1111
−9.9951	−4.9976	−2.4988	1111	1111	1110
−10.0000	−5.0000	−2.5000	1111	1111	1111

CALIBRATION PROCEDURE

1. Connect the ADC-HS12B as shown in one of the connection diagrams. The sample-hold and A/D converter should be timed as shown in the timing diagram. The trigger pulse should be applied at a rate of 70 kHz or less and should be 100 nanoseconds minimum width.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

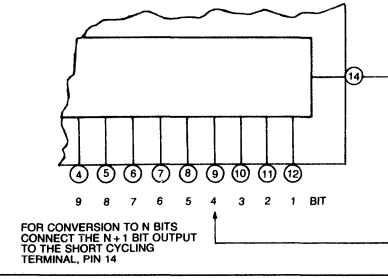
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 to +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 to +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

PIN 14 CONNECTION FOR SHORT CYCLE OPERATION

RES. (BITS)	PIN 14 TO	CONV. TIME
1	PIN 11	0.7 µsec.
2	PIN 10	1.3
3	PIN 9	2.0
4	PIN 8	2.6
5	PIN 7	3.3
6	PIN 6	4.0
7	PIN 5	4.6
8	PIN 4	5.3
9	PIN 3	6.0
10	PIN 2	6.6
11	PIN 1	7.3
12	PIN 16	9.0

SHORT CYCLE OPERATION



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER		
0 to +5V	29 & 24	22 & 25	23 & 26
0 to +10V	29 & 24	—	23 & 26
±2.5V	29 & 24	22 & 25	23 & 22
±5V	29 & 24	—	23 & 22
±10V	29 & 25	—	23 & 22

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-HS12BMC	0 to +70°C
ADC-HS12BMM	−55 to +125°C

ACCESSORIES

Part Number	Description
DILS-2	Mating Sockets: (2 required per converter)
TP50K	Trimming Potentiometers

For military devices compliant to MIL-STD-883, contact DATEL.

ADC-HX, ADC-HZ Series 12-Bit, Analog-to-Digital Converters

1

FEATURES

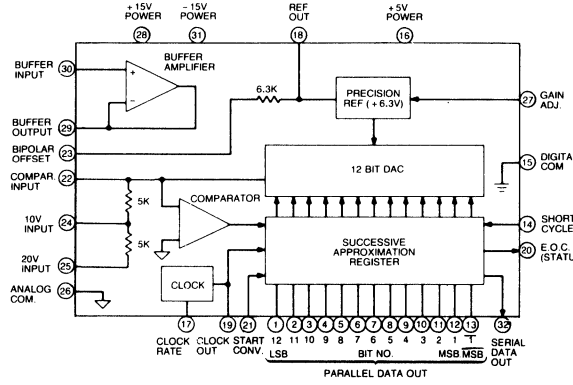
- **12-Bit resolution**
- **8- or 20-Microseconds conversions**
- **5 Input ranges**
- **Internal high Z buffer**
- **Short-cycle operation**

GENERAL DESCRIPTION

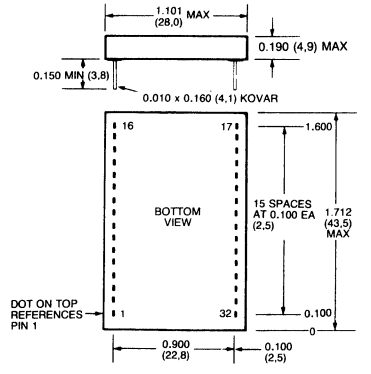
The ADC-HX12B and ADC-HZ12B are self-contained, high performance, 12-bit A/D converters manufactured with thick- and thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12-bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

These converters utilize a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12-bit successive approximation register, a clock and a monolithic buffer amplifier. Nonlinearity is specified at ±½ LSB maximum. Other specifications include a differential nonlinearity tempco of ±2 ppm/°C and a gain tempco of ±20 ppm/°C maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3 microseconds, the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary 2's complement. Serial data is also brought out. The package is a 32-pin ceramic case. Six different models are offered covering the operating temperature ranges of 0 to +70°C and −55 to +125°C. For military devices compliant to MIL-STD-883, consult the factory.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ.
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT (MSB)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM	31	-15V POWER
16	+5V POWER	32	SERIAL OUTPUT

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	ADC-HX12B	ADC-HZ12B
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V FS	
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V FS	
Input Impedance	2.5K (0 to +5V, ±2.5V) 5K (0 to +10V, ±5V) 10K (±10V)	
Input Impedance with Buffer	100 Megohms	
Input Bias Current of Buffer	125 nA typical, 250 nA max.	
Input Overvoltage	±15V	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <30 nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 2 TTL loads	
OUTPUTS[1]		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V	
Coding, unipolar	Complementary Binary	
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V 100 nsec. pulses. 600 kHz for ADC-HX12B and 1.5 MHz for ADC-HZ12B (pin 17 grounded).	
PERFORMANCE		
Resolution	12 bits (1 part in 4096)	
Nonlinearity	±½ LSB max.	
Differential Nonlinearity	±¾ LSB max.	
Gain Error, before adjustment	±0.1%	
Zero Error, unipolar, before adj.	±0.05% of FSR[3]	
Offset Error, bipolar, before adj.	±0.1% of FSR[3]	
Temp. Coeff. of Gain	±20 ppm/°C max.	
Temp. Coeff. of Zero, unipolar	±5 ppm/°C of FSR max.[3]	
Temp. Coeff. of Offset, bipolar	±10 ppm/°C of FSR max.[3]	
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR[3]	
No Missing Codes	Over oper. temp. range	
Conversion Time[2], 12 bits	20 μsec. max.	8.0 μsec. max.
10 bits[4]	15 μsec. max.	6.0 μsec. max.
8 bits[4]	10 μsec. max.	4.0 μsec. max.
Buffer Settling Time, 10V step	3.0 μsec. to 0.01%	
Power Supply Rejection	0.004%/% Supply max.	
POWER REQUIREMENTS		
Power Supply Voltage	+15V dc ±0.5V dc at 20 mA −15V dc ±0.5V dc at 25 mA + 5V dc ±0.25V dc at 85 mA ±12V dc, +5V dc Operation[5]	

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0 to +70°C or −55 to +125°C
Storage Temperature Range	−65°C to +150°C
Package Size	1.700 x 1.100 x 0.160 inches
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounces (14 grams)

FOOTNOTES:

1. All digital outputs can drive 2 TTL loads.
2. Without buffer amplifier used. ADC-HZ12B may require external adjustment of clock rate.
3. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.
4. Short cycled operation.
5. For ±12V, +5V operation, contact the factory.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01 μF ceramic capacitor in parallel with a 1 μF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10 μF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01 μF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V dc ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/°C cermet types (such as DATEL TP series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.
4. Short-cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases the clock rate is also speeded up by connecting the clock rate adjust (pin 17) to +5V dc (10 bits) or +15V dc (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.

5. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary or complementary 2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS − 1 LSB gives 1111 1111 1111.
6. These converters dissipate 1.7 watts maximum of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
7. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see clock rate adjustment diagram) for the converter resolution selected. The pulse width of the external clock should be between 100 nanoseconds and 300 nanoseconds. Each N-bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N-bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.
8. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between the input level change, such as a multiplexer channel change, and the negative-going edge of the START CONVERSION pulse. If the buffer is not required, its input (pin 30) should be tied to ANALOG GROUND (pin 26). This prevents the unused amplifier from introducing noise into the converter. For applications not using the internal buffer, the converter must be driven from a source with an extremely low input impedance.

CONNECTIONS AND CALIBRATION

Input Connections

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 to +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 to +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
±2.5V	24	22 & 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 25

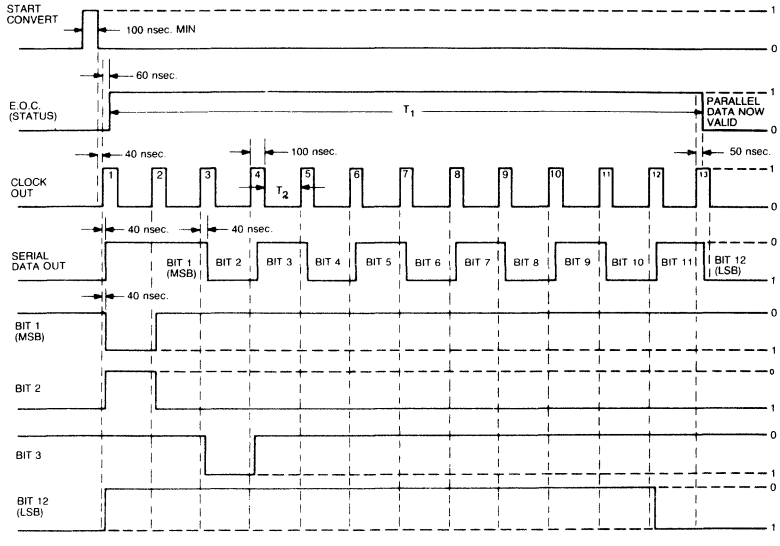
CALIBRATION PROCEDURE

1. Connect the converter for bipolar or unipolar operation. Use the input connection table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nanoseconds minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS + ½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS − 1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

TIMING DIAGRAM OPERATING PERIODS

	ADC-HX12B	ADC-HZ12B
T_1	20 μsec.	8.0 μsec.
T_2	1.56 μsec.	0.56 μsec.

TIMING DIAGRAM FOR ADC-HX12B, ADC-HZ12B OUTPUT: 101010101010



Calibration Table

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 to +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 to +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

Coding Table, Unipolar Operation

INPUT RANGE		COMP. BINARY CODING
0 TO +10V	0 TO +5V	MSB LSB
+9.9976V	+4.9988V	0000 0000 0000
+8.7500	+4.3750	0001 1111 1111
+7.5000	+3.7500	0011 1111 1111
+5.0000	+2.5000	0111 1111 1111
+2.5000	+1.2500	1011 1111 1111
+1.2500	+0.6250	1101 1111 1111
+0.0024	+0.0012	1111 1111 1110
0.0000	0.0000	1111 1111 1111

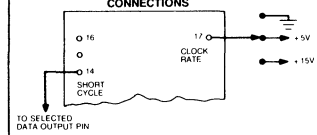
Coding Table, Bipolar Operation

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		COMP. TWO'S COMPLEMENT	
±10V	±5V	2.5V	MSB	LSB	MSB	LSB
+9.9951V	+4.9976V	+2.4988V	0000 0000	0000	1000 0000	0000
+7.5000	+3.7500	+1.8750	0001 1111	1111	1001 1111	1111
+5.0000	+2.5000	+1.2500	0011 1111	1111	1011 1111	1111
0.0000	0.0000	0.0000	0111 1111	1111	1111 1111	1111
−5.0000	−2.5000	−1.2500	1011 1111	1111	0011 1111	1111
−7.5000	−3.7500	−1.8750	1101 1111	1111	0101 1111	1111
−9.9951	−4.9976	−2.4988	1111 1111	1110	0111 1111	1110
−10.0000	−5.0000	−2.5000	1111 1111	1111	0111 1111	1111

SHORT CYCLE OPERATION

Refer to Technical Note 4 for methods of reducing the ADC-HX or ADC-HZ conversion times.

CONNECTIONS



CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE ADC-HX12B	CLOCK RATE ADC-HZ12B
0V	600 kHz	1.5MHz
+5V	720 kHz	1.8MHz
+15V	880 kHz	2.2MHz

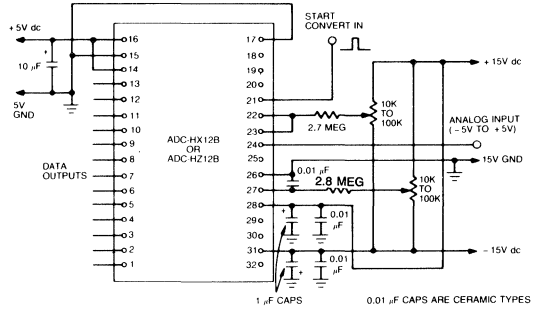
8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX12B CONV. TIME	20 µsec.	15 µsec.	10 µsec.
ADC-HZ12B CONV. TIME	8 µsec.	6 µsec.	4 µsec.
CONNECT THESE PINS TOGETHER	17 & 15	17 & 16	17 & 28
	14 & 16	14 & 2	14 & 4

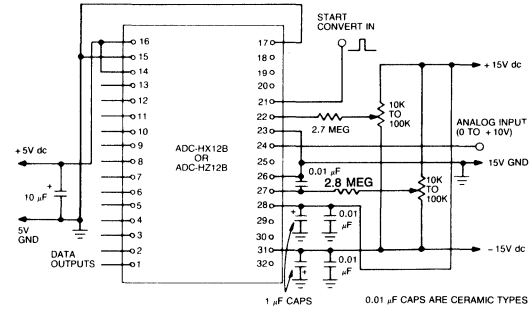
PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

BIPOLAR OPERATION, −5V TO +5V



UNIPOLAR OPERATION, 0 TO +10V



ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SEAL
ADC-HX12BGC	0 to +70°C	EPOXY
ADC-HX12BMC	0 to +70°C	HERM.
ADC-HX12BMM	−55 to +125°C	HERM.
ADC-HZ12BGC	0 to +70°C	EPOXY
ADC-HZ12BMC	0 to +70°C	HERM.
ADC-HZ12BMM	−55 to +125°C	HERM.

ACCESSORIES

Part Number	Description
DILS-2	Mating Socket (2 per converter)
TP10K, or TP100K	Trimming Potentiometers

ADS-105, ADS-106
12-BIT, 1 MHz
SAMPLING A/D CONVERTERS

FEATURES

- **12-Bit resolution**
- **1 MHz throughput**
- **15 Megohm input impedance**
- **Includes fast Sample/Hold amplifier**
- **3-State output, TTL and CMOS compatible**

GENERAL DESCRIPTION

The ADS-105 and ADS-106 provide high-speed, highly accurate, multiple sample digitization of sinusoidal signals. These devices use a two-pass, digitally correcting subranging architecture. Both models have an analog-to-digital (A/D) converter and a sample-and-hold amplifier (S/H). Combining both the A/D and S/H in one device eliminates critical layout problems assuring stable, high-bandwidth operation.

The ADS-105 accepts unipolar analog inputs (0 to +10V) while the ADS-106 accepts full scale bipolar inputs (±10V).

The ADS-105/-106 offer outstanding high speed analog performance. Maximum differential linearity error is 0.025% FSR ±1/2 LSB of full scale (0 °C to +70 °C).The maximum gain temperature coefficient is ±35 ppm of FSR/°C. Both models guarantee no missing codes over the full -55 °C to +125 °C operating temperature range.

Dynamic specifications include a total sampling rate of 1 MHz for sinusoidal signals which do not exceed the internal bandwidth, settling, and slew rate specifications. The input bandwidth of the S/H accepts sinusoidal signals up to 40 KHz (10V peak to peak) with -70 dB typical harmonic distortion.

Applications for the ADS-105/106 include data acquisition and control systems, array processing, vibration and resonance analysis, medical imaging and scanning, communications signal processing, noise and spectrum analyzers, and video processing.

For high-reliability versions of either the ADS-105 or the ADS-106, contact the factory.

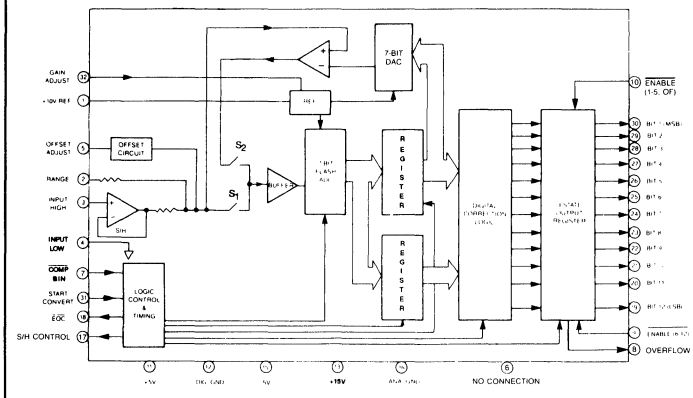
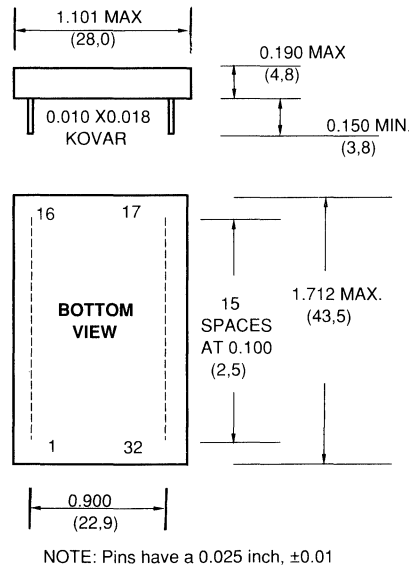


Figure 1. ADS-105, ADS-106 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF OUT
2	RANGE IN
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST IN
6	NO CONNECTION
7	COMP BIN IN
8	OVERFLOW OUT
9	ENABLE (6-12) IN
10	ENABLE (1-5 O.F.) IN
11	+5V POWER IN
12	DIGITAL GROUND
13	+15V POWER IN
14	-15V POWER IN
15	-5V POWER IN
16	ANALOG GROUND
17	S/H CONTROL OUT
18	EOC OUT
19	BIT 12 (LSB) OUT
20	BIT 11 OUT
21	BIT 10 OUT
22	BIT 9 OUT
23	BIT 8 OUT
24	BIT 7 OUT
25	BIT 6 OUT
26	BIT 5 OUT
27	BIT 4 OUT
28	BIT 3 OUT
29	BIT 2 OUT
30	BIT 1 (MSB) OUT
31	START CONVERT IN
32	GAIN ADJUST IN

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 13)	0 to +18	Volts dc
-15V Supply (Pin 14)	0 to -18	Volts dc
+5V Supply(Pin 11)	-0.5 to +7	Volts dc
-5V Supply (Pin 15)	+0.5 to -7	Volts dc
Digital inputs (Pins 7, 9, 10, and 31)	-0.3 to +5.5	Volts dc
Analog input	-15 to +15	Volts dc
Lead temp. (10 sec.)	300	°C max.

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range				
ADS-105	–	0 to +10	–	Volts
ADS-106	–	±10	–	Volts
Input Impedance				
Resistance	5	15	–	M Ohms
Capacitance	–	5	7	pF
Input Bias Current	–	±20	±500	nA
Logic Levels:				
Logic 1	2.0	–	–	Volts
Logic 0	–	–	0.8	Volts
Logic Loading:				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA

SAMPLE/HOLD SPECIFICATIONS	MIN.	TYP.	MAX.	UNITS
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty (Jitter)	–	±100	–	pSec.
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec.
0 °C to +70 °C	–	–	765	nSec.
-55 °C to +125 °C	–	–	900	nSec.
Sinusoidal Input	–	–	395	nSec.

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Integral Nonlinearity				
+25 °C	–	–	±0.0125	%FSR ±1/2LSB
0 °C to +70 °C	–	–	±0.0125	%FSR ±1/2LSB
-55 °C to +125 °C	–	–	±0.0125	%FSR ±3LSB
Integral Nonlinearity Tempco	–	–	±8.5	ppm/°C
Differential Nonlinearity				
+25 °C	–	–	±0.0125	%FSR ±1/2LSB
0 °C to +70 °C	–	–	±0.0125	%FSR ±1/2LSB
-55 °C to +125 °C	–	–	±0.0125	%FSR ±1LSB
Differential Nonlinearity Tempco	–	–	±6.1	ppm/ °C
Full-Scale Absolute Accuracy				
+25 °C	–	±3	±8	LSB
0 °C to +70 °C	–	±4	±14	LSB
-55 °C to +125 °C	–	±8	±29	LSB
ADS-105				
Unipolar Zero Error, +25 °C	–	±1	±3	LSB
Unipolar Zero Error Tempco	–	±13	±25	ppm/ °C
ADS-106				
Bipolar Offset Error, +25 °C	–	±2	±5	LSB
Bipolar Offset Error Tempco	–	±17.5	±35	ppm/ °C
Bipolar Zero Error, +25 °C	–	±1	±3	LSB
Bipolar Zero Error Tempco	–	±13	±25	ppm/ °C
Gain Error	–	±2	± 5	LSB
Gain Error Tempco	–	±17.5	±35	ppm/ °C
No missing codes (For 12 binary bits)	Guaranteed over operating temperature range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels:				
Logic 1	2.4	–	–	Volts
Logic 0	–	–	0.4	Volts
Logic Loading:				
Logic 1	–	–	- 160	µA
Logic 0	–	–	6.4	mA
Internal Reference:				
+Voltage, +25° C	9.98	10	10.02	Volts dc
Tempco	–	±5	±30	ppm/ °C
External current	–	–	1.5	mA
Output Coding:				
ADS-105 (Pin 7 High)	Straight binary			
(Pin 7 Low)	Complementary binary			
ADS-106 (Pin 7 High)	Offset binary			
(Pin 7 Low)	Complementary offset binary			

APPLICATIONS

- **High-speed Data Acquisition and Control Systems**
- **Array Processing, Vibration and Resonance/ transient Analysis**
- **Medical Imaging and Scanning**
- **Communications Signal Processing**
- **Spectrum and Noise Analyzers**
- **Video Processing Systems**

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Conversion Rate:				
+25 °C	1	–	–	MHz
0 °C to +70 °C	1	–	–	MHz
-55 °C to +125 °C	1	–	–	MHz
A/D Conversion Time:				
+25 °C	–	–	500	nSec.
0 °C to +70 °C	–	–	540	nSec.
-55 °C to +125 °C	–	–	560	nSec.
Total Harmonic Distortion:				
DC to 100 KHz, (Vin = <5V pk-pk)				
+25 °C	-65	-70	–	dB
-55 °C to +125 °C	-61	-66	–	dB
DC to 40 KHz, (Vin = 10V pk-pk)				
+25 °C	-65	-70	–	dB
-55 °C to +125 °C	-61	-66	–	dB
DC to 25 KHz, (Vin = 20V pk-pk)				
+25 °C	-65	-70	–	dB
-55 °C to +125 °C	-61	-66	–	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
-15V dc Supply	-14.25	-15	-15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
-5V dc Supply	-4.75	-5	-5.25	Volts dc
Supply Current				
+15V Supply	–	+40	+54	mA
-15V Supply	–	-30	-40	mA
+5V Supply *	–	+56	+90	mA
-5V Supply	–	-173	-210	mA
Power Dissipation	–	2.2	2.7	Watts
Supply Rejection	–	–	±0.01	%FSR/%V
PHYSICAL/ ENVIRONMENTAL	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Operating Temperature Range				
MC Models	0	–	+70	°C
MM Models	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Weight	–	–	0.42(12)	oz.(gram)
Package Type	32-pin hermetically sealed ceramic DIP			
Pin Type	0.010 x 0.018 inch Kovar			

* + 5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or to reduce any small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter.

   Do not connect these grounds together at the power supply terminals when the power supplies are located some distance from the ground plane. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies to ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 1) to ground (pin 16) also using a 4.7μF, 25V capacitor. The -5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.

4. Obtain straight binary/offset binary output coding by tying the COMP BIN signal (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (Enable bits 1-5 & O.F.).

6. The S/H Control signal, pin 17, goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before EOC goes low. This indicates that the converter can accept a new analog input.

7. Full-scale absolute accuracy refers to the unadjusted performance of the ADS-105/106. These figures may be improved substantially using external trim circuits.

THEORY OF OPERATION

This theory of operation describes the ADS-105/106's function in conjunction with its internal Sample/Hold amplifer for digitizing sinusoidal signals. The ADS-105/106 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step conversion method, this technique uses a single 7-bit flash A/D converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, the block diagram, and the timing diagram as needed.

The ADS-105/106 guarantees a 1 MHz throughput rate when the START CONVERT pulse of 50 nanoseconds is provided at a 1 MHz rate. The 1 MHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or level signals is longer and listed under the acquisition specifications (10V step).

The ADS-105/106 is in the sample mode when the S/H CONTROL pin is high (S/H is in high-state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to S/H CONTROL low. This as

THEORY OF OPERATION (Cont.)

sures the sample-hold has the minumum required acquisition time for the particular application mode. Sinusoidal inputs being digitized by using a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 75 nanosecond delay before EOC goes high and the A/D conversion begins. This consists of the remaining 40 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to EOC high. The hold mode settling time and input settling time requirements required are met by observing this timing.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 12-bit word. EOC goes low indicating the conversion is complete, and the output passes to three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed (EOC going low). The S/H Control output goes high shortly before EOC goes low, indicating that the Sample/Hold is back sampling the input. This feature improves the overall throughput of the ADS-105/106.

Data from the previous conversion is valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before the EOC goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput of the ADS-105/106 for sinusoidal inputs consists of 395 nanoseconds for acquisition time, 75 nanoseconds for START CONVERT and min-max propagation delays, 560 nanoseconds for A/D conversion time minus 30 nanoseconds for the S/H CONTROL pin. A throughput time of 1000 nanoseconds is obtained and a 1 Mhz throughput rate is realized.

Combining the A/D and S/H in one device allows the ADS-105/106 to guarantee a total throughput period of 1.0 microsecond maximum over the -55 °C to +125 °C temperature range for the complete system or a throughput rate of 1 MHz. Retriggering the START CONVERT pulse before EOC goes low will not initiate a new conversion.

The practical results of this means that single-channel (non-multiplexed) full-scale inputs with spectral content not exceeding 40 KHz for 10V peak-peak signals may be digitized up to a 1 MHz rate. This will give about 25 data samples per cycle to 12-bit accuracy and linearity. This type of resolution is ideal for capture of signals with a broad spectral content of 40 KHz and below (10V peak-to-peak signals). Because many samples may be taken in a short sampling interval, the ADS-105/106 are ideal for computer-aided spectral analysis of a complex-frequency signal. The 12-bit performance is ideal for larger fast fourier transform sizes of 1024 to 4096 points by reducing frequency binning resolution noise.

For multi-channel multiplexed signals, the very high multiplexing rate allows larger numbers of channels while still retaining moderate bandwidth per channel. Users requiring higher input bandwidth or faster acquisition times should review Datel's ADS-21 or ADS-22 Sampling A/D converter.

Table 1. ADC-105, ADC-106 Timing Specifications

TIMING	MIN.	TYP.	MAX.	UNITS
Start Convert Pulse Width:	50	–	–	nSec.
Start Convert Low to EOC High Delay	20	–	35	nSec.
Start Convert Low to Previous Data Invalid	350	–	–	nSec.
Data Valid Before EOC Goes Low	25	–	–	nSec.
Enable to Output Data Valid Delay	–	–	10	nSec.
EOC Low to Start Convert High (Sinusoidal Inputs)	355	–	–	nSec.

Note: Table 1 applies over the operating temperature range and over the operating power supply range.

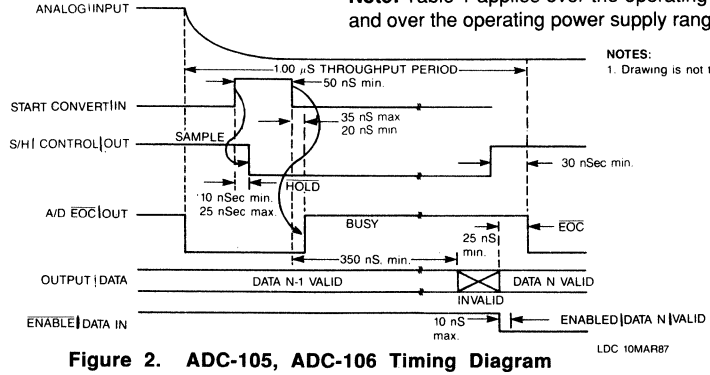


Figure 2. ADC-105, ADC-106 Timing Diagram

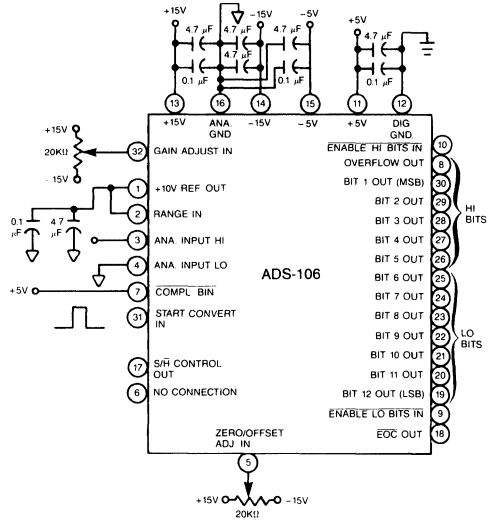


Figure 3. ADS-106 Typical External Connections, ± 10V dc

SYSTEM CALIBRATION PROCEDURE

Remove system errors or the small initial errors as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale input range (FSR). The data outputs should be connected to LED's to observe the resulting data values.

Table 2. Input Connections

INPUT VOLTAGE RANGE	INPUT PIN	JUMP PIN 2 TO PIN:
0 to +10V dc	3	No connection
±10V dc	3	1 (+10V Ref.)

Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments:

Apply a precision voltage reference source between the analog input (pin 3) and analog ground (pin 16). Use a very low-noise signal source for accurate calibration.

Adjust the output of the reference source per Tables 3 and 4 for the unipolar zero adjustment (+1/2 LSB) or the bipolar zero adjustment (zero + 1/2 LSB) for the appropriate full scale range. For unipolar operation, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with COMP BIN tied low.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with the COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low.

3. Full Scale Adjustment:

Set the output of the voltage reference used in step 2 to the value shown in the Tables 3 and 4 for the unipolar or bipolar gain adjustment (+F.S. -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 7) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in the Tables 5 and 6.

Table 3. Zero and Gain Adjust for Unipolar Use

RANGE	ZERO ADJUST	GAIN ADJUST
UNIPOLAR FSR 0 to +10V	(+1/2 LSB) +1.22mV dc	(+FS -1 1/2 LSB) +9.9963V dc

Table 4. Zero and Gain Adjust for Bipolar Use

RANGE	ZERO ADJUST	GAIN ADJUST
BIPOLAR FSR ±10V	(+1/2 LSB) +2.44mV	(+FS -1 1/2 LSB) +9.9927V

Table 5. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Straight Binary		Complementary Straight Binary	
	0 to +10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.9976V	1111	1111 1111	0000	0000 0000
7/8 FS	+8.750V	1110	0000 0000	0001	1111 1111
3/4 FS	+7.500V	1100	0000 0000	0011	1111 1111
1/2 FS	+5.000V	1000	0000 0000	0111	1111 1111
1/4 FS	+2.500V	0100	0000 0000	1011	1111 1111
1/8 FS	+1.250V	0010	0000 0000	1101	1111 1111
1 LSB	+0.0024V	0000	0000 0001	1111	1111 1110
0	0.0000V	0000	0000 0000	1111	1111 1111

Table 6. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Straight Binary		Complementary Straight Binary	
	± 10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.9951V	1111	1111 1111	0000	0000 0000
+3/4 FS	+7.5000V	1110	0000 0000	0001	1111 1111
+1/2 FS	+5.0000V	1100	0000 0000	0011	1111 1111
0	0.00000V	1000	0000 0000	0111	1111 1111
-1/2 FS	-5.0000V	0100	0000 0000	1011	1111 1111
-3/4 FS	-7.5000V	0010	0000 0000	1101	1111 1111
-FS + 1 LSB	-9.9951V	0000	0000 0001	1111	1111 1110
-FS	-10.000V	0000	0000 0000	1111	1111 1111

ORDERING INFORMATION

ADS-105 12-Bit, 1 MHz
ADS-106 Sampling A/D Converters

MODEL	TEMPERATURE RANGE	INPUT VOLTAGE RANGE
ADS-105MC	0°C to +70°C	0 to +10V
ADS-106MC	0°C to +70°C	-10 to +10V
ADS-105MM	-55°C to +125°C	0 to +10V
ADS-106MM	-55°C to +125°C	-10 to +10V

Trimming Potentiometer: TP 20K (2 required)
A receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For high-reliability versions of the ADS-105/-106, contact the factory.

ADS-111
12-Bit, 500 KHz, LowPower Sampling A/D Converter

1

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **500 KHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DIP**
- **Low-power, 1.4 Watts**
- **Three-state output buffers**

GENERAL DESCRIPTION

DATEL's ADS-111 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 500 KHz is achieved while only dissipating 1.4 Watts.

Manufactured using thick-film and thin-film hybrid technology, the ADS-111's exclusive performance is based upon a digitally-corrected subranging architecture.

DATEL further enhances this technology by using a proprietary chip and unique laser trimming schemes. Figure 1 is a simplified block diagram of the ADS-111.

The ADS-111 features two pin-programmable analog input voltage ranges: 0 to +10V and ±5V. The input impedance is specified at 15 M Ohms. The ADS-111 is also guaranteed to have no missing codes over the operating temperature range.

All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary.

The power requirements are ±15V dc and +5V dc. The ADS-111 is available in the commercial 0 degrees Celsius to +70 degrees Celsius and military -55 degrees Celsius to +125 degrees Celsius operating temperature range.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems. For information on high reliability screening, contact DATEL.

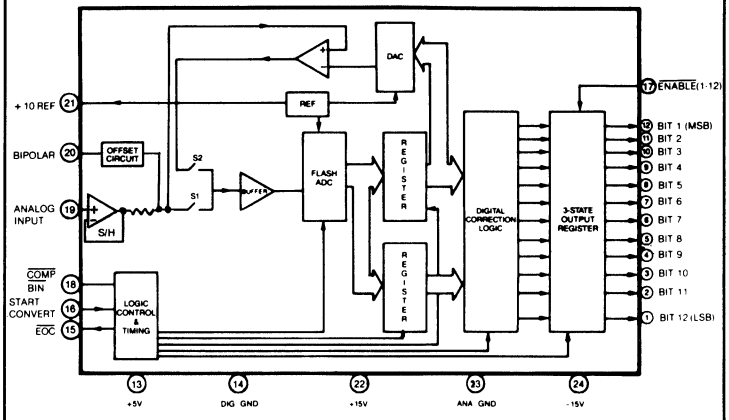
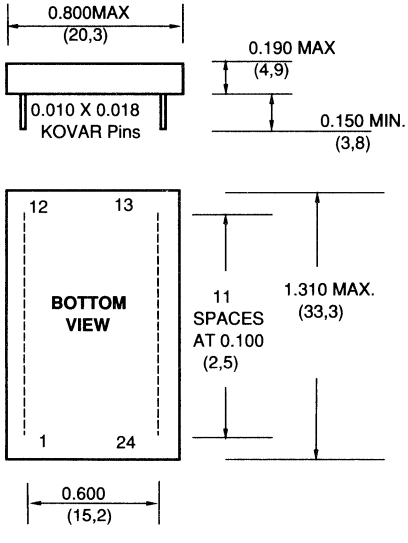


Figure 1. ADS-111 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, 0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	BIT 12 OUT (LSB)
2	BIT 11 OUT
3	BIT 10 OUT
4	BIT 9 OUT
5	BIT 8 OUT
6	BIT 7 OUT
7	BIT 6 OUT
8	BIT 5 OUT
9	BIT 4 OUT
10	BIT 3 OUT
11	BIT 2 OUT
12	BIT 1 OUT (MSB)
13	+5V
14	DIGITAL GROUND
15	$\overline{\text{EOC}}$
16	START CONVERT
17	$\overline{\text{ENABLE}}$ (1-12)
18	COMP BIN
19	ANALOG INPUT
20	BIPOLAR
21	+10V REF
22	+15V
23	ANALOG GROUND
24	-15V

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-111	–	±5	–	Volts dc
(See Table 4 also)	–	0 to +10	–	Volts dc
Input Impedance	5.0	15.0	–	M Ohms
Input Capacitance	–	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	2.5	µA
Logic Loading "0"	–	–	-100	µA
A/D PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 C to +125 °C	–	–	±3	LSB
Integral Non-Lin. Tempco	–	±5	±10	ppm/ °C
Differential Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 C to +125 °C	–	–	±1	LSB
Differential Non-Lin. Tempco	–	–	±2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	±5	±10	LSB
0 °C to +70 °C	–	±6	±18	LSB
-55 C to +125 °C	–	±10	±32	LSB
Unipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±3	±5	LSB
Unipolar Zero Tempco.	–	±15	±30	ppm/ °C
Bipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±3	±5	LSB
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error,				
+25 °C (See Tech Note 1)	–	±4	±8	LSB
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±4	±8	LSB
Gain Tempco	–	±20	±40	ppm/ °C
Conversion Times				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.0	µSec.
-55 °C to +125 °C	–	–	1.15	µSec.
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution	12 Bits			
Output Coding				
(Pin 18 Hi)	Straight binary/offset binary			
(Pin 18 Low)	Complementary binary Complementary offset binary			
SAMPLE/HOLD PERFORMANCE				
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty	–	±100	–	pSec.
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec.
0 °C to +70 °C	–	–	765	nSec.
-55 °C to +125 °C	–	–	900	nSec.
(Sinusoidal Input)	–	–	465	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.5	+5.0	+5.5	Volts dc
Power Supply Current				
+15V dc Supply	–	+38	+43	mA
-15V dc Supply	–	-36	-44	mA
+5V dc Supply*	–	+66	+75	mA
Power Dissipation	–	1.4	1.75	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 4. Remove system errors or adjust the small initial errors of the ADS-111 to zero using the optional external circuitry shown in Figure 3. The external adjustment circuit has no affect on the throughput rate.

2. When the optional external adjustment circuitry is used, additional input ranges are available. Refer to Figure 3 and Table 4.

3. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane).

   Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

4. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

5. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

6. To obtain three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). Otherwise, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "1" (high).

THEORY OF OPERATION

This theory of operation describes the ADS-111's function in conjunction with its internal sample-and-hold amplifier for digitizing sinusoidal signals. The ADS-111 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, block diagram, and timing diagram as needed.

The ADS-111 guarantees a 500 KHz throughput rate over the temperature range when the START CONVERT pulse of 200 nanoseconds is provided at a 500 KHz rate. The 500 KHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or DC level signals is longer and listed under the acquisition specifications (10V step).

The ADS-111 is in the sample mode when the internal S/$\overline{\text{H}}$ CONTROL is high (S/$\overline{\text{H}}$ is in the high state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to S/$\overline{\text{H}}$ CONTROL low. This assures the sample-hold has the minimum required acquisition time for the particular application mode. Sinusoidal inputs being digitized by utilizing a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 225 nanosecond delay before $\overline{\text{EOC}}$ goes high and the A/D conversion begins. This consists of the remaining 190 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to $\overline{\text{EOC}}$ high. The hold mode settling time and input settling time requirements required for the first pass of the A/D conversion are met when observing this time.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 12-bit word. $\overline{\text{EOC}}$ goes low, indicating the conversion is complete, and the output passes to the three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{\text{EOC}}$ going low). The sample/hold control output goes high shortly before $\overline{\text{EOC}}$ goes low, indicating that the S/$\overline{\text{H}}$ is back sampling the input. This feature improves the overall throughput rate of the ADS-111.

Data from the previous conversion is valid and capable of being latched 20 nanoseconds after the falling edge of $\overline{\text{EOC}}$ and remains valid for 1300 nanoseconds. Data from the new conversion is valid a minimum of 20 nanoseconds after the next $\overline{\text{EOC}}$ low transition. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput rate over temperature of the ADS-111 for sinusoidal inputs consists of 465 nanoseconds for the acquisition time, 225 nanoseconds for the START CONVERT and min-max propagation delays, and 1150 nanoseconds for the A/D conversion. An internal function reduces this cumulative time by 30 nanoseconds by putting the sample/hold back into the sample mode 30 nanoseconds before $\overline{\text{EOC}}$ goes low. A throughput time of 1810 nanoseconds is obtained and the minimum throughput rate of 500 KHz is easily met.

Combining the A/D and S/H in one device allows the ADS-111 to guarantee a throughput rate of 500 KHz over the -55 degrees Celsius to +125 degrees Celsius temperature range for the complete system. Retriggering of the START CONVERT pulse before $\overline{\text{EOC}}$ goes low will not initiate a new conversion.

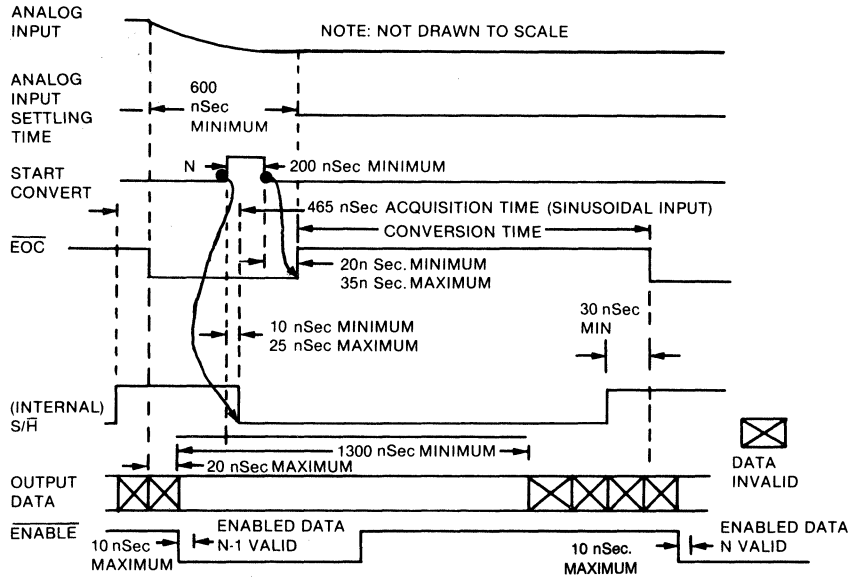


Figure 2. ADS-111 Timing Diagram

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 1. Signal Timing Summary

LINE	DURATION
START CONVERT Pulse Width	200 nSec. minimum
Analog Input Settling Time	600 nSec. minimum
START CONVERT Low to $\overline{EOC}$ High Propagation Delay	35 nSec. maximum
$\overline{EOC}$ Low to Previous Output Data Invalid	1320 nSec. minimum
Data Valid After $\overline{EOC}$ goes Low	20 nSec. maximum
$\overline{ENABLE}$ to Output Data Valid Propagation Delay	10 nSec. maximum
$\overline{EOC}$ Low to START CONVERT High (Sinusoidal Inputs)	425 nSec. minimum

INPUT CONNECTIONS

Table 2. ADS-111 Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to PIN 21
0 to +10V dc	Pin 19	Pin 20 to GROUND

Table 3a. Zero and Gain Adjust, Unipolar Opertion

UNIPOLAR FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc

Table 3b. Zero and Gain Adjust, Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±5V dc	+1.22mV dc	+4.9963V dc

CALIBRATION PROCEDURE

Should removal of system errors or the small initial errors be desired, adjustment is accomplished as follows:

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Calibration con't.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ 1/2 LSB) or the bipolar zero adjustment (zero +1/2 LSB). For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the $\overline{\text{COMP BIN}}$ (pin 18) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the $\overline{\text{COMP BIN}}$ (pin 18) tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 18) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with $\overline{\text{COMP BIN}}$ (pin 18) tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for $\overline{\text{COMP BIN}}$ (pin 18) tied high or between 0000 0000 0001 and 0000 0000 0000 for $\overline{\text{COMP BIN}}$ (pin 18) tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 6 and 7.

Table 4. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, ±1.25V	2	14	K Ohms

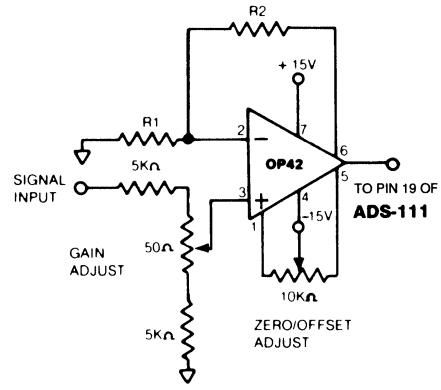


Figure 3. Optional Calibration Circuit

The performance characteristics shown in Table 5 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

Table 5. Dynamic Performance

Throughput Rate (Changing Inputs)	MIN	TYP	MAX	UNITS
+25 °C	500	600	–	KHz
0 °C to +70 °C	500	600	–	KHz
-55 C to +125 °C	500	–	–	KHz
A/D Conversion Time				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.0	µSec.
-55 C to +125 °C	–	–	1.15	µSec.
Total Harmonic Distortion				
DC to 100 KHz at Vin ≤5V p-p	-65	-70	–	dB
DC to 60 KHz at Vin = 10V p-p	-65	-70	–	dB

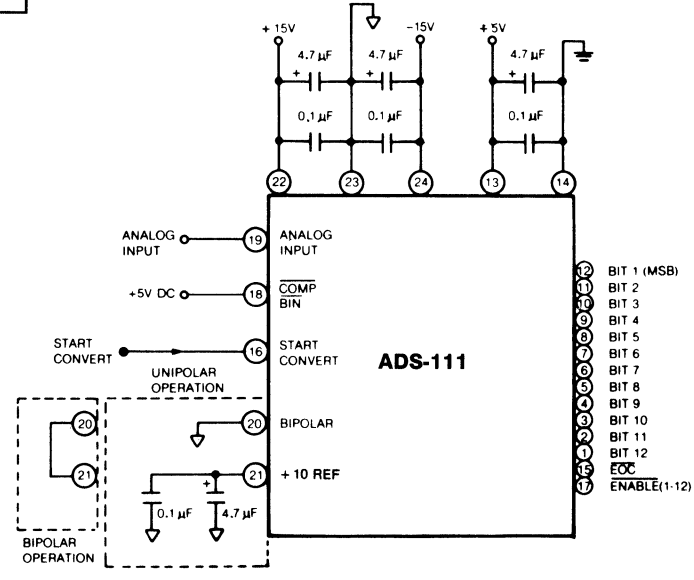


Figure 4. Typical ADS-111 Connection Diagram

Table 6. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE (Volts dc) ±5V	OUTPUT CODING OFFSET BINARY MSB LSB	COMP. OFFSET BINARY MSB LSB
+FS -1 LSB	+4.9976V	1111 1111 1111	0000 0000 0000
+3/4 FS	+3.7500V	1110 0000 0000	0001 1111 1111
+1/2 FS	+2.5000V	1100 0000 0000	0011 1111 1111
0	0.0000V	1000 0000 0000	0111 1111 1111
-1/2 FS	-2.5000V	0100 0000 0000	1011 1111 1111
-3/4 FS	-3.7500V	0010 0000 0000	1101 1111 1111
-FS +1 LSB	-4.9976V	0000 0000 0001	1111 1111 1110
-FS	-5.0000V	0000 0000 0000	1111 1111 1111

Table 7. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGE (Volts dc) 0 to +10V	OUTPUT CODING STRAIGHT BINARY MSB LSB	COMP. BINARY MSB LSB
+FS-1LSB	+9.9976V	1111 1111 1111	0000 0000 0000
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111
1/4 FS	+2.5000V	0100 0000 0000	1011 1111 1111
1/8 FS	+1.2500V	0010 0000 0000	1101 1111 1111
1 LSB	+0.0024V	0000 0000 0001	1111 1111 1110
0	0.0000V	0000 0000 0000	1111 1111 1111

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-111MC	0 °C to +70 °C	Hermetic
ADS-111MM	-55 °C to +125 °C	Hermetic

ACCESSORIES

Part Number	Description
TP10K *	Trimming Potentiometer
TP50*	Trimming Potentiometer

* Only required if optional external calibration circuitry is used.

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For high reliability versions of the ADS-111 contact DATEL.

ADS-115, ADS-116
10-BIT, 1 MHz
SAMPLING A/D CONVERTERS

FEATURES

- **10-Bit resolution**
- **1 MHz throughput**
- **15 Megohm input impedance**
- **Includes fast Sample/Hold amplifier**
- **3-State output, TTL and CMOS compatible**

GENERAL DESCRIPTION

DATEL's ADS-115 and ADS-116 combine a tracking Sample/Hold amplifier and a high-speed, 10- bit Analog-to-Digital converter, all in one small device. The ADS-115 and ADS-116 provide digitized outputs of sinusoidal signals at up to one million samples per second. By combining both the S/H and A/D circuits in one device, critical layout and thermal factors are overcome. This offers stable, high-bandwidth performance with negligible degradation over time.

The ADS-115 accepts unipolar inputs from 0 to +10 volts and the ADS-116 has a ±10 volt input range. Both models are offered in commercial (0 °C to +70 °C) and military (-55 °C to +125 °C) temperature ranges. For 12-bit applications, users should consider Datel's ADS-105/106 or the SHM-45/ADC-500 pair.

Linearity error is ±1/2 LSB (0 °C to +70 °C) and the maximum gain temperature coefficient is ±35 ppm of full scale range per degree Celsius. Maximum power required is 2.7 watts using ±15 and ±5 volt dc supplies.

The ADS-115/116 may be sampled up to 1 MHz . The input bandwidth of the S/H will accept up to 60 KHz (10V pk-pk) with -60 dB typical harmonic distortion.

These miniature hybrid sampling A/D converters are ideal for fast data acquisition and control systems, array processing, DSP applications, imaging, medical scanning, signal processing, acoustic, resonance, and vibration analyzers.

For high reliability versions of either the ADS-115 or the ADS-116, contact the factory.

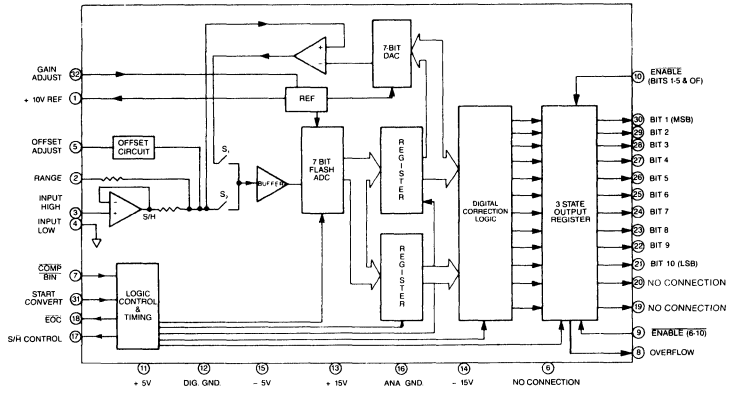
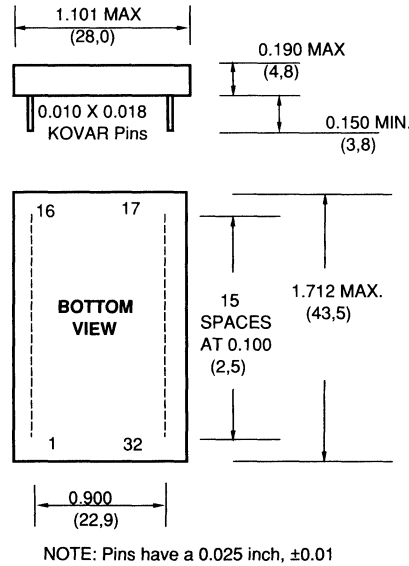


Figure 1. ADS-115, ADS-116 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF OUT
2	RANGE IN
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST IN
6	NO CONNECTION
7	COMP BIN IN
8	OVERFLOW OUT
9	ENABLE (6-10) IN
10	ENABLE (1-5 O.F.) IN
11	+5V POWER IN
12	DIGITAL GROUND
13	+15V POWER IN
14	-15V POWER IN
15	-5V POWER IN
16	ANALOG GROUND
17	S/H CONTROL OUT
18	EOC OUT
19	NO CONNECTION
20	NO CONNECTION
21	BIT 10 OUT
22	BIT 9 OUT
23	BIT 8 OUT
24	BIT 7 OUT
25	BIT 6 OUT
26	BIT 5 OUT
27	BIT 4 OUT
28	BIT 3 OUT
29	BIT 2 OUT
30	BIT 1 (MSB) OUT
31	START CONVERT IN
32	GAIN ADJUST IN

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 13)	0 to +18	Volts dc
-15V Supply (Pin 14)	0 to -18	Volts dc
+5V Supply(Pin 11)	-0.5 to +7	Volts dc
-5V Supply (Pin 15)	+0.5 to -7	Volts dc
Digital inputs (Pins 7, 9, 10, and 31)	-0.3 to +6	Volts dc
Analog input	-15 to +15	Volts dc
Lead temp. (10 sec.)	300	° C max.

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range				
ADS-115	–	0 to +10	–	Volts
ADS-116	–	±10	–	Volts
Input Impedance				
Resistance	5	15	–	M Ohms
Capacitance	–	5	7	pF
Input Bias Current	–	±20	±500	nA
Logic Levels:				
Logic 1	2.0	–	–	Volts
Logic 0	–	–	0.8	Volts
Logic Loading:				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA
SAMPLE/HOLD SPECIFICATIONS	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty (Jitter)	–	±100	–	pSec.
S/H Acquisition Time to 0.048% (10V step)	–	–	500	nSec.
Sinusoidal Input	–	–	395	nSec.

APPLICATIONS

- **High-speed Data Acquisition and Control Systems**
- **Array Processing, Vibration and Resonance/ transient Analysis**
- **Medical Imaging and Scanning**
- **Communications Signal Processing**
- **Spectrum and Noise Analyzers**
- **Video Processing Systems**

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Integral Nonlinearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	±1	LSB
Integral Nonlinearity Tempco	–	–	±10	ppm/°C
Differential Nonlinearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	±1/2	±3/4	LSB
Differential Nonlinearity Tempco	–	–	±7.5	ppm/ °C
Full-Scale Absolute Accuracy				
+25 °C	–	±2	±6	LSB
0 °C to +70 °C	–	±4	±9	LSB
-55 °C to +125 °C	–	±8	±15	LSB
ADS-115				
Unipolar Zero Error, +25 °C	–	±1/4	±1	LSB
Unipolar Zero Error Tempco	–	±13	±25	ppm/ °C
ADS-116				
Bipolar Offset Error, +25 °C	–	±2	±5	LSB
Bipolar Offset Error Tempco	–	±17.5	±35	ppm/ °C
Bipolar Zero Error, +25 °C	–	±1/4	±1	LSB
Bipolar Zero Error Tempco	–	±13	±25	ppm/ °C
Gain Error	–	±2	± 5	LSB
Gain Error Tempco	–	±17.5	±35	ppm/ °C
No missing codes (For 12 binary bits)	Guaranteed over operating temperature range.			
OUTPUTS	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Logic Levels:				
Logic 1	2.4	–	–	Volts
Logic 0	–	–	0.4	Volts
Logic Loading:				
Logic 1	–	–	- 160	µA
Logic 0	–	–	6.4	mA
Internal Reference:				
+Voltage, +25° C	9.98	10	10.02	Volts dc
Tempco	–	±5	±30	ppm/ °C
External current	–	–	1.5	mA
Output Coding: **ADS-115** (Pin 7 High) (Pin 7 Low)	Straight binary Complementary binary			
ADS-116 (Pin 7 High) (Pin 7 Low)	Offset binary Complementary offset binary			

DYNAMIC PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Conversion Rate:				
+25 °C	1	–	–	MHz
0 °C to +70 °C	1	–	–	MHz
-55 °C to +125 °C	1	–	–	MHz
A/D Conversion Time:				
0 °C to +70 °C	–	–	480	nSec.
-55 °C to +125 °C	–	–	510	nSec.
Total Harmonic Distortion:				
DC to 110 KHz, (Vin = <5V pk-pk)				
+25 °C	-55	-60	–	dB
-55 °C to +125 °C	-52	-56	–	dB
DC to 60 KHz, (Vin = 10V pk-pk)				
+25 °C	-55	-60	–	dB
-55 °C to +125 °C	-52	-56	–	dB
DC to 30 KHz, (Vin = 20V pk-pk)				
+25 °C	-55	-60	–	dB
-55 °C to +125 °C	-52	-56	–	dB

POWER REQUIREMENTS	MIN.	TYP.	MAX.	UNITS
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
-15V dc Supply	-14.25	-15	-15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
-5V dc Supply	-4.75	-5	-5.25	Volts dc
Supply Current				
+15V Supply	–	+40	+54	mA
-15V Supply	–	-30	-40	mA
+5V Supply *	–	+56	+90	mA
-5V Supply	–	-173	-210	mA
Power Dissipation	–	2.2	2.7	Watts
Supply Rejection	–	–	±0.01	%FSR/%V
PHYSICAL/ ENVIRONMENTAL	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Operating Temperature Range				
MC Models	0	–	+70	°C
MM Models	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Weight	–	–	0.42(12)	oz.(gram)
Package Type	32-pin hermetically sealed ceramic DIP			
Pin Type	0.010 x 0.018 inch Kovar			

* + 5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or to reduce any small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter.

   Do not connect these grounds together at the power supply terminals when the power supplies are located some distance from the ground plane. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies to ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 1) to ground (pin 16) also using a 4.7μF, 25V capacitor. The -5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.

4. Obtain straight binary/offset binary output coding by tying the $\overline{\text{COMP BIN}}$ signal (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (Enable bits 1-5 & O.F.).

6. The $\overline{\text{S/H}}$ Control signal, pin 17, goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before $\overline{\text{EOC}}$ goes low. This indicates that the converter can accept a new analog input.

7. Full-scale absolute accuracy refers to the unadjusted performance of the ADS-115/116. These figures may be improved substantially using external trim circuits.

THEORY OF OPERATION

This theory of operation describes the ADS-115/116's function in conjunction with its internal Sample/Hold amplifer for digitizing sinusoidal signals. The ADS-115/116 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step conversion method, this technique uses a single 7-bit flash A/D converter twice in the conversion process to yield a final resolution of 10 bits. Refer to the connection diagram, the block diagram, and the timing diagram as needed.

The ADS-115/116 guarantees a 1 MHz throughput rate when the START CONVERT pulse of 50 nanoseconds is provided at a 1 MHz rate. The 1 MHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or dc level signals is longer and listed under the acquisition specifications (10V step).

The ADS-115/116 is in the sample mode when the $\overline{\text{S/H}}$ CONTROL pin is high ($\overline{\text{S/H}}$ is in high-state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to $\overline{\text{S/H}}$ CONTROL low. This

THEORY OF OPERATION (Cont.)

assures the sample-hold has the minimum required acquisition time for the particular application mode. Sinusoidal inputs being digitized by using a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 75 nanosecond delay before EOC goes high and the A/D conversion begins. This consists of the remaining 40 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to EOC high. The hold mode settling time and input settling time requirements required are met by observing this timing.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 10-bit word. EOC goes low indicating the conversion is complete, and the output passes to three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed (EOC going low). The S/H Control output goes high shortly before EOC goes low, indicating that the Sample/Hold is back sampling the input. This feature improves the overall throughput of the ADS-115/116.

Data from the previous conversion is valid up to 275 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before the EOC goes low and valid up to 275 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput of the ADS-115/116 for sinusoidal inputs consists of 355 nanoseconds from $\overline{EOC}$ low to START CONVERT high (logic delays and S/H control going low 30 nanoseconds earlier included), 50 nanoseconds for the hold and input settling time, and 500 nsec for the conversion process. The Sample/Hold control pin saves 30 nanoseconds by allowing the S/H to return to the sample mode 30 nanoseconds before the conversion is complete.

Combining the A/D and S/H in one device guarantees a total throughput of 1.0 microsecond maximum over the -55 °C to +125 °C temperature range for the complete system or a throughput rate of 1 MHz. Retriggering the START CONVERT pulse before EOC goes low will not initiate a new conversion.

The practical results of this means that single-channel (non-multiplexed) full-scale inputs with spectral content not exceeding 60 KHz for 10V peak-peak signals may be digitized up to a 1 MHz rate. This will give about 16 data samples per cycle to 10-bit accuracy and linearity. This type of resolution is ideal for capture of signals with a broad spectral content of 60 KHz and below (10V peak-to-peak signals). Because many samples may be taken in a short sampling interval, the ADS-115/116 are ideal for computer-aided spectral analysis of a complex-frequency signal. The 10-bit performance is ideal for larger fast fourier transform sizes of 256 to 1024 points by reducing frequency binning resolution noise.

For multi-channel multiplexed signals, the very high multiplexing rate allows larger numbers of channels while still retaining moderate bandwidth per channel. Users requiring higher input bandwidth or faster acquisition times should review Datel's ADS-21 or ADS-22 Sampling A/D converters.

Table 1. ADC-115, ADC-116 Timing Specifications

TIMING	MIN.	TYP.	MAX.	UNITS
Start Convert Pulse Width:	50	–	–	nSec.
Start Convert Low to $\overline{EOC}$ High Delay	20	–	35	nSec.
Start Convert Low to Previous Data Invalid	275	–	–	nSec.
Data Valid Before $\overline{EOC}$ Goes Low	25	–	–	nSec.
Enable to Output Data Valid Delay	–	–	10	nSec.
$\overline{EOC}$ Low to Start Convert High (Sinusoidal Inputs)	355	–	–	nSec.

Note: Table 1 applies over the operating temperature range and over the operating power suply range.

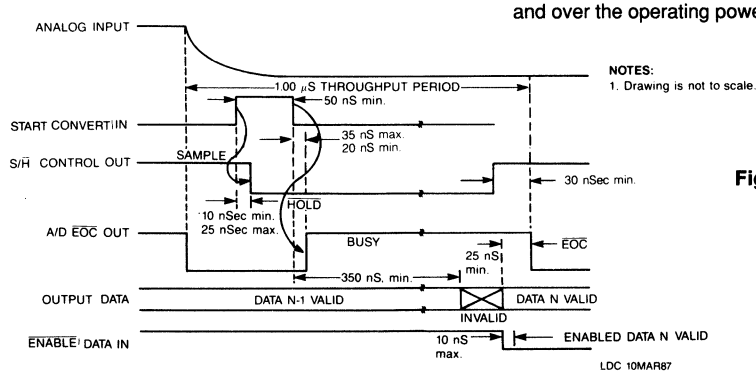


Figure 2. ADC-115, ADC-116 Timing Diagram

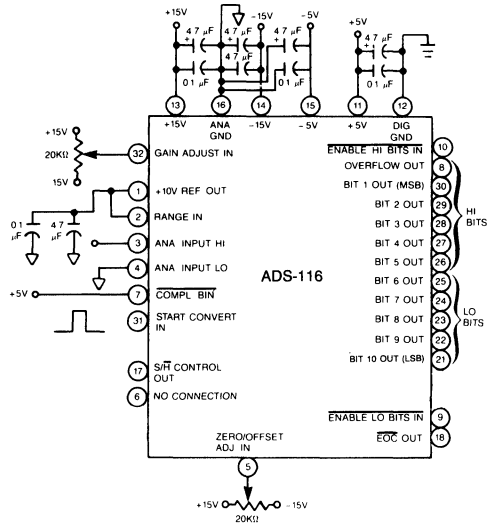


Figure 3. ADS-116 Typical External Connections, ± 10V dc

SYSTEM CALIBRATION PROCEDURE

Remove system errors or the small initial errors as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale input range (FSR). The data outputs should be connected to LED's to observe the resulting data values.

Table 2. Input Connections

INPUT VOLTAGE RANGE	INPUT PIN	JUMP PIN 2 TO PIN:
0 to +10V dc	3	No connection
±10V dc	3	1 (+10V Ref.)

Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments:

Apply a precision voltage reference source between the analog input (pin 3) and analog ground (pin 16). Use a very low-noise signal source for accurate calibration.

Adjust the output of the reference source per Tables 3 and 4 for the unipolar zero adjustment (+1/2 LSB) or the bipolar zero adjustment (zero + 1/2 LSB) for the appropriate full scale range. For unipolar operation, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 and 00 0000 0001 with the COMP BIN (pin 7) tied high or between 11 1111 1111 and 11 1111 1110 with COMP BIN tied low.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 and 10 0000 0001 with the COMP BIN tied high or between 01 1111 1111 and 01 1111 1110 with COMP BIN tied low.

3. Full Scale Adjustment:

Set the output of the voltage reference used in step 2 to the value shown in the Tables 3 and 4 for the unipolar or bipolar gain adjustment (+F.S. -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1110 and 11 1111 1111 for COMP BIN (pin 7) tied high or between 00 0000 0001 and 00 0000 0000 for COMP BIN tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in the Tables 5 and 6.

Table 3. Zero and Gain Adjust for Unipolar Use

RANGE	ZERO ADJUST	GAIN ADJUST
UNIPOLAR FSR 0 to +10V	(+1/2 LSB) +4.88 mV dc	(+FS -1 1/2 LSB) +9.9927V dc

Table 4. Zero and Gain Adjust for Bipolar Use

RANGE	ZERO ADJUST	GAIN ADJUST
BIPOLAR FSR ±10V	(+1/2 LSB) +9.77 mV	(+FS -1 1/2 LSB) +9.9707 V

Table 5. Output Coding for Uniplar Operation

UNIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Straight Binary		Complementary Straight Binary	
	0 to +10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.99023V	1111 1111	11	0000 0000	00
7/8 FS	+8.750V	1110 0000	00	0001 1111	11
3/4 FS	+7.500V	1100 0000	00	0011 1111	11
1/2 FS	+5.000V	1000 0000	00	0111 1111	11
1/4 FS	+2.500V	0100 0000	00	1011 1111	11
1/8 FS	+1.250V	0010 0000	00	1101 1111	11
1 LSB	+0.00977V	0000 0000	00	1111 1111	11
0	0.0000V	0000 0000	00	1111 1111	11

Table 6. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE	OUTPUT CODING Offset Binary		Complementary Offset Binary	
	± 10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+9.9805V	1111 1111	11	0000 0000	00
+3/4 FS	+7.5000V	1110 0000	00	0001 1111	11
+1/2 FS	+5.0000V	1100 0000	00	0011 1111	11
0	0.00000V	1000 0000	00	0111 1111	11
-1/2 FS	-5.0000V	0100 0000	00	1011 1111	11
-3/4 FS	-7.5000V	0010 0000	00	1101 1111	11
-FS + 1 LSB	-9.9805V	0000 0000	00	1111 1111	11
-FS	-10.000V	0000 0000	00	1111 1111	11

ORDERING INFORMATION

ADS-115 10-Bit, 1 MHz
ADS-116 Sampling A/D Converters

MODEL	TEMPERATURE RANGE	INPUT VOLTAGE RANGE
ADS-115MC	0 °C to +70 °C	0 to +10V
ADS-116MC	0 °C to +70 °C	-10 to +10V
ADS-115MM	-55 °C to +125 °C	0 to +10V
ADS-116MM	-55 °C to +125 °C	-10 to +10V

Trimming Potentiometer: TP 20K (2 required)
A receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For high-reliability versions of the ADS-115/-116, contact DATEL.

ADS-125, ADS-126
12-BIT, 700 KHz, LOW-POWER SAMPLING A/D CONVERTERS

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **700 KHz minimum throughput**
- **15Mohm input impedance**
- **Pin-programmable input ranges**
- **Low-power, 2.1 Watts**
- **Three-state output buffers**
- **Small 32-pin DIP**

GENERAL DESCRIPTION

DATEL's ADS-125 and ADS-126 are 12-bit, sampling A/D converters with a 700 KHz minimum throughput rate for sinusoidal inputs.

The performance of these converters is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using unique laser trimming schemes. The ADS-125 and ADS-126 are packaged in 32-pin ceramic DIP's and consume 2.1 Watts.

Input impedance to the sample-and-hold for these devices is 15 Mohms. Both the ADS-125 and the ADS-126 have two pin programmable input voltage ranges. The ADS-125 has ranges of ±10V and 0 to 10V while the ADS-126 has ranges of ±2.5V and 0 to 5V. All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in two's complement, complementary two's complement, straight binary/offset binary or complementary binary/complementary offset binary.

The power requirements are ±15V dc and +5V dc. These parts are available in the commercial 0 degrees Celsius to +70 degrees Celsius and military -55 degrees Celsius to +125 degrees Celsius operating temperature range.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems. For information on high reliability screening, contact the factory.

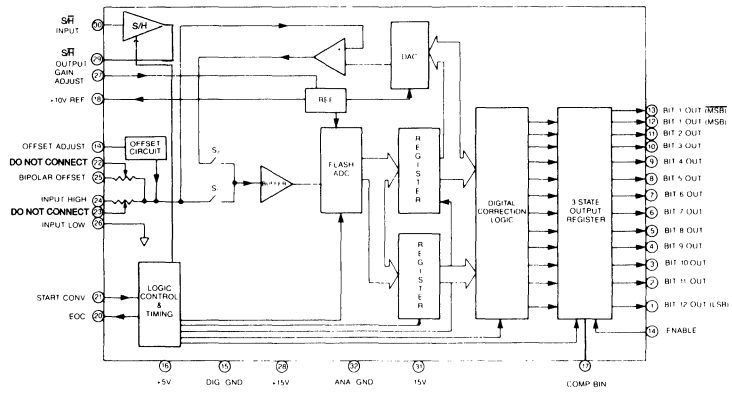
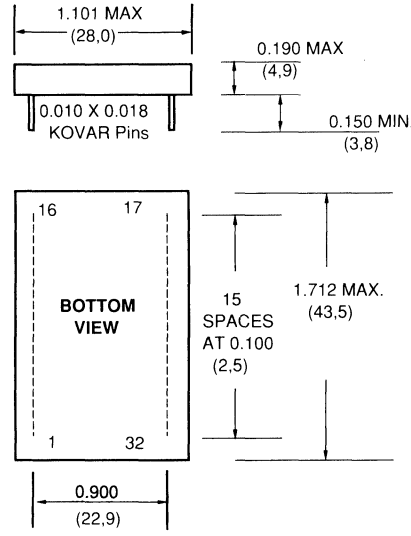


Figure 1. ADS-125, ADS-126 Simplified Block Diagram

MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

I/O CONNECTIONS

PIN	FUNCTION
1	Bit 12 OUT (LSB)
2	Bit 11 OUT
3	Bit 10 OUT
4	Bit 9 OUT
5	Bit 8 OUT
6	Bit 7 OUT
7	Bit 6 OUT
8	Bit 5 OUT
9	Bit 4 OUT
10	Bit 3 OUT
11	Bit 2 OUT
12	Bit 1 OUT (MSB)
13	Bit 1 OUT (MSB)
14	ENABLE
15	DIGITAL GND.
16	+5V
17	COMP BIN
18	REF. OUT (+10V dc)
19	OFFSET ADJUST
20	EOC
21	START CONVERT
22	DO NOT CONNECT
23	DO NOT CONNECT
24	INPUT HIGH
25	BIPOLAR OFFSET
26	INPUT LOW
27	GAIN ADJUST
28	+15V
29	S/H OUTPUT
30	S/H INPUT
31	-15V
32	ANALOG GND.

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 28)	0 to +18	Volts dc
-15V Supply (Pin 31)	0 to -18	Volts dc
+5V Supply (Pin 16)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 14,17,21)	-0.3 to +6.0	Volts dc
Analog Input (Pin 30)	-15 to +15	Volts dc
Lead Temp. (10 sec.)	300 max.	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range:				
ADS-125	–	±10	–	Volts dc
	–	0 to +10	–	Volts dc
ADS-126	–	±2.5	–	Volts dc
	–	0 to +5	–	Volts dc
Input Impedance	5.0	15.0	–	M ohms
Input Capacitance	–	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	2.5	µA
Logic Loading "0"	–	–	-100	µA
A/D PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	± 3	LSB
Integral Non-Lin.Tempco.	–	± 5	±10	ppm/ °C
Differential Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
-55 °C to +125 °C	–	–	±1	LSB
Differential Non-Lin.Tempco.	–	–	± 2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	± 5	±10	LSB
0 °C to +70 °C	–	± 6	±18	LSB
-55 °C to +125 °C	–	±10	± 32	LSB
Unipolar Zero Error,				
+25 °C	–	± 3	± 5	LSB
Unipolar Zero Tempco	–	±15	± 30	ppm/ °C
Unipolar Zero Adjust Range	± 5	–	–	LSB
Bipolar Zero Error,				
+25 °C	–	± 3	± 5	LSB
Bipolar Zero Tempco	–	± 5	± 8	ppm/ °C
Bipolar Zero Adjust Range	± 5	–	–	LSB
Bipolar Offset Error,				
+25 °C	–	± 4	± 8	LSB
Bipolar Offset Tempco	–	± 20	± 40	ppm/ °C
Bipolar Offset Adjust Range	± 5	–	–	LSB
Gain Error, +25 °C	–	± 4	± 8	LSB
Gain Tempco	–	± 20	± 40	ppm/ °C
Gain Error Adjust Range	± 5	–	–	LSB
Conversion Times:				
+25 °C	–	–	800	nSec.
0 °C to +70 °C	–	–	850	nSec.
-55 °C to +125 °C	–	–	880	nSec.
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	12 Bits			
Output Coding:	Straight binary/offset binary			
(Pin 17 Hi)	Complementary binary			
(Pin 17 Low)	Complementary offset binary			
	Two's complement			
(Note 4)	Complementary Two's complement			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	9.98	10.0	10.02	Volts dc
Drift	–	± 5	± 30	ppm/ °C
External Current	–	–	1.5	mA
SAMPLE/HOLD PERFORMANCE				
Slew Rate	–	90	–	V/µSec
Aperture Delay Time	–	20	–	nSec
Aperture Uncertainty	–	±100	–	pSec
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec
0 °C to +70 °C	–	–	765	nSec
-55 °C to +125 °C	–	–	900	nSec
(Sinusoidal Input)	–	–	395	nSec
POWER REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+ 4.75	+ 5.0	+ 5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+ 70	+ 82	mA
-15V dc Supply	–	- 52	- 61	mA
+5V dc Supply*	–	+ 66	+ 71	mA
Power Dissipation	–	2.1	2.4	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	- 55	–	+125	°C
Storage Temperature Range	- 65	–	+150	°C
Package Type	32-Pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.

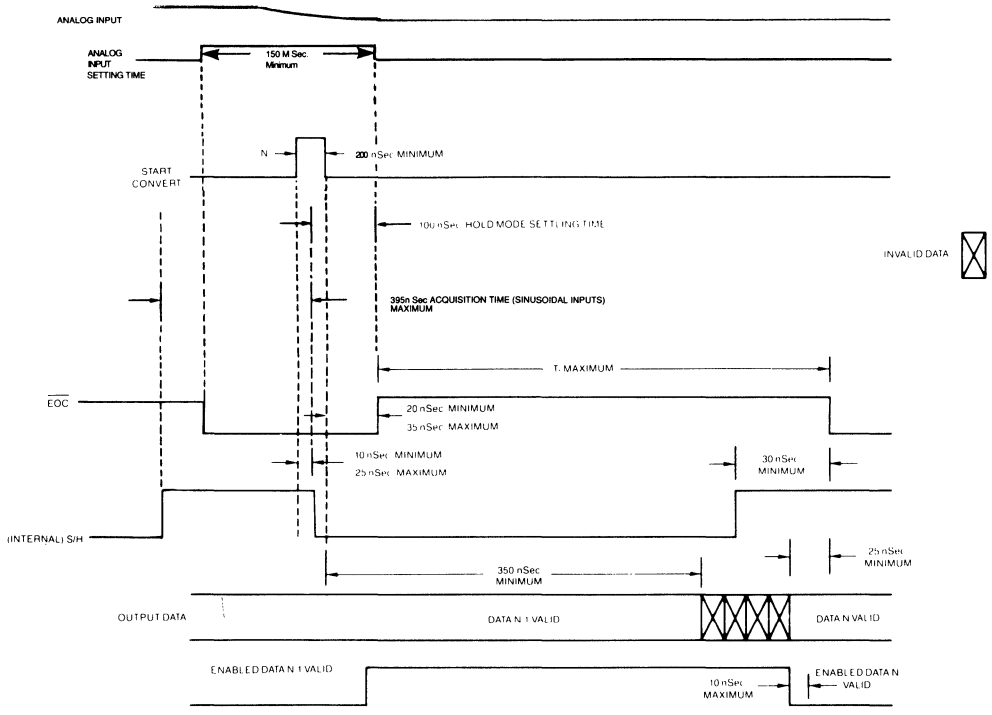


Figure 2. ADS-125, ADS-126 TIMING DIAGRAM

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K Ohm trimming potentiometer for gain adjustment with the wiper tied to pin 27 (ground pin 27 for operation without adjustments). Use a 20K Ohm trimming potentiometer with the wiper tied to pin 19 for zero/offset adjustment (leave pin 19 open for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass the analog and digital supplies and the +10V reference (pin-18) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 18) to analog ground (pin 32).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 17) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP

INPUT CONNECTIONS

Table 2a. ADS-125 Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
Bipolar ± 10Vdc	Pin 30	tie Pin 29 to Pin 24 tie Pin 18 to Pin 25
Unipolar 0 to +10V dc	Pin 30	tie Pin 29 to Pin 24 tie Pin 24 to Pin 25

Table 2b. ADS-126 Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
Bipolar ± 2.5V	Pin 30	tie Pin 29 to Pin 24, & tie Pin 25 to Pin 18
Unipolar 0 to +5V dc	Pin 30	tie Pin 29 to Pin 24 tie Pin 25 to Pin 26

Table 3a. Zero and Gain Adjust for Unipolar Operation

UNIPOLAR FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +5V dc	+0.61mV dc	+4.9982V dc
0 to +10V dc	+1.22mV dc	+9.9963V dc

Table 3b. Zero and Gain Adjust for Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±2.5V dc	+0.61mV dc	+2.4985V dc
±10V dc	+2.44mV dc	+9.9927V dc

users desiring logic control of this function. In the bipolar mode, two's complement or complementary two's complement output coding is available by using the MSB output (pin 13). MSB (pin 13) does not have a three-state output.

5. The three-state outputs are enabled by connecting ENABLE (pin 14) to a logic "0" (low). MSB (pin 13) does not have a three-state output and therefore is not controlled by ENABLE.

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown in Table 1 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 1. Signal Timing Summary

LINE	DURATION IN NANOSECONDS
START CONVERT Pulse Width	200 nSec. minimum
START CONVERT Low to EOC High Propagation Delay	35 nSec. maximum
START CONVERT Low to Previous Output Data Invalid	350 nSec. minimum
Data Valid Before EOC goes Low	25 nSec. minimum
ENABLE to Output Data Valid Propagation Delay	10 nSec. maximum
EOC Low to START CONVERT High (Sinusoidal Inputs)	355 nSec. minimum

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 21) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input and ground, refer to Table 2 for input pin. Adjust the output of the reference source per Tables 3a and 3b for the unipolar zero adjustment (+ 1/2 LSB) or the bipolar zero adjustment (zero +1/2 LSB) for the appropriate FSR. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 17) tied high (Straight Binary) or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN pin tied low (Complementary Binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 17) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 17) tied low (complementary offset binary). Two's complement and complementary two's complement requires the use of MSB versus MSB as given for offset binary or complementary offset binary respectively.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3a or 3b for the unipolar or bipolar gain adjustment (+FS -1 1/2 LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 17) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN pin tied low. Two's Complement and Complementary Two's Complement respectively requires using MSB versus MSB.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

Table 6. Dynamic Performance

Throughput Rate	MIN	TYP	MAX	UNITS
(Sinusoidal Inputs)				
+25 °C	700	–	–	KHz
0 °C to +70 °C	670	–	–	KHz
-55 °C to +125 °C	650	–	–	KHz
A/D Conversion Time				
+25 °C	–	–	800	nSec
0 °C to +70 °C	–	–	850	nSec
-55 °C to +125 °C	–	–	880	nSec
Total Harmonic Distortion				
DC to 100 KHz at Vin = <5V p-p	-65	-70	–	dB
DC to 60 KHz at Vin = 10V p-p	-65	-70	–	dB
DC to 25 KHz at Vin = 20V p-p	-65	-70	–	dB

The performance characteristics shown in Table 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

THEORY OF OPERATION

This theory of operation describes the ADS-125/126's function in conjunction with its internal sample-and-hold amplifier for digitizing sinusoidal signals. The ADS-125/126 employs a subranging A/D conversion architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the connection diagram, block diagram, and timing diagram as needed.

The ADS-125/126 guarantees a 650 KHz throughput rate over the temperature range when the START CONVERT pulse of 200 nanoseconds is provided at a 650 KHz rate. The 650 KHz rate is based upon sinusoidal input frequencies up to those specified in the harmonic distortion specifications. The acquisition time for pulse or DC level signals is longer and listed under the acquisition specifications (10V step).

The ADS-125/126 is in the sample mode when the S/H CONTROL pin is high (S/H is in high-state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to S/H CONTROL low. This assures the sample-hold has the minimum required acquisition time for the

particular application mode. Sinusoidal inputs being digitized by utilizing a repetitive START CONVERT pulse will automatically give the appropriate acquisition time when continuously sampling.

Upon going into the hold mode, there will be a 225 nanosecond delay before $\overline{EOC}$ goes high and the A/D conversion begins. This consists of the remaining 190 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 35 nanosecond maximum delay from START CONVERT low to $\overline{EOC}$ high. The hold mode settling time and input settling time requirements required for the first pass of the A/D conversion are met when observing this time.

After conversion is initiated, switch S1 of the ADC closes and S2 opens. The analog input, having been configured for the appropriate input range, is buffered and then digitized by the 7-bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. The DAC has 13 bits of linearity.

When the first pass finishes, S2 closes and S1 opens. The output of the DAC is then subtracted from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least seven significant bits. The outputs from the two registers are then combined by the digital correction logic to produce a 12-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the output passes to the three-state output buffers.

Once the second step of the flash ADC is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{EOC}$ going low). The Sample/Hold Control output goes high shortly before $\overline{EOC}$ goes low, indicating that the S/$\overline{H}$ is back sampling the input. This feature improves the overall throughput rate of the ADS-125/126.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the START CONVERT pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{EOC}$ goes low and valid up to 350 nanoseconds after the falling edge of the next START CONVERT pulse. There is a 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid at the device output.

The overall throughput rate of the ADS-125/126 for sinusoidal inputs consists of 395 nanoseconds for the acquisition time, 225 nanoseconds for the START CONVERT and min-max propagation delays, 880 nanoseconds for A/D conversion time minus 30 nanoseconds for the S/$\overline{H}$ CONTROL pin. A throughput time of 1470 nanoseconds is obtained and a 650 KHz throughput rate is realized.

Combining the A/D and S/$\overline{H}$ in one device allows the ADS-125/126 to guarantee a throughput rate of 650 KHz over the -55 °C to +125 °C temperature range for the complete system. Retriggering of the START CONVERT pulse before $\overline{EOC}$ goes low will not initiate a new conversion.

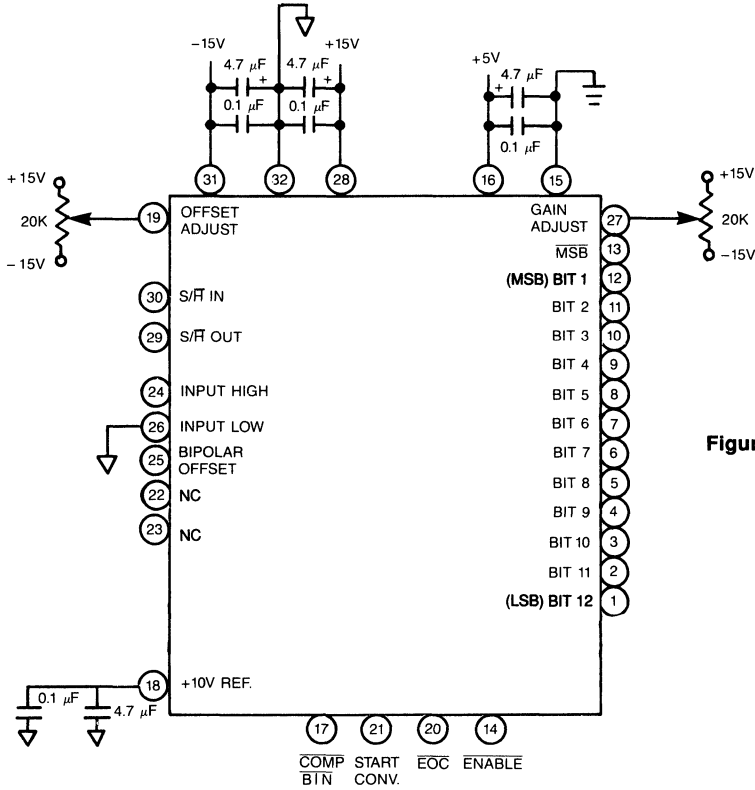


Figure 3. ADS-125, ADS-126 CALIBRATION CIRCUIT

UNIPOLAR SCALE	INPUT RANGES, VOLTS dc		OUTPUT CODING			
			Straight Binary		Comp. Binary	
	0 to +10V	0 to +5V	MSB	LSB	MSB	LSB
+FS-1LSB	+9.9976V	+4.9988V	1111	1111 1111	0000	0000 0000
7/8 FS	+8.7500V	+4.3750V	1110	0000 0000	0001	1111 1111
3/4 FS	+7.5000V	+3.7500V	1100	0000 0000	0011	1111 1111
1/2 FS	+5.0000V	+2.5000V	1000	0000 0000	0111	1111 1111
1/4 FS	+2.5000V	+1.2500V	0100	0000 0000	1011	1111 1111
1/8 FS	+1.2500V	+0.6250V	0010	0000 0000	1101	1111 1111
1 LSB	+0.0024V	+0.0012V	0000	0000 0001	1111	1111 1110
0	0.0000V	0.0000V	0000	0000 0000	1111	1111 1111

Table 5. OUTPUT CODING FOR BIPOLAR OPERATION

BIPOLAR SCALE	INPUT RANGE		OUTPUT CODING							
	±10V dc	±2.5V dc	Offset Binary		Comp Offset Binary		Comp Two's Comp		Two's Comp	
			MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
+FS -1 LSB	+9.9951V	+2.4988	1111	1111 1111	0000	0000 0000	1000	0000 0000	0111	1111 1111
+3/4 FS	+7.5000V	+1.8750	1110	0000 0000	0001	1111 1111	1001	1111 1111	0110	0000 0000
+1/2 FS	+5.0000V	+1.2500	1100	0000 0000	0011	1111 1111	1011	1111 1111	0100	0000 0000
0	0.0000V	0.0000	1000	0000 0000	0111	1111 1111	1111	1111 1111	0000	0000 0000
-1/2 FS	-5.0000V	-1.2500	0100	0000 0000	1011	1111 1111	0011	1111 1111	1100	0000 0000
-3/4 FS	-7.5000V	-1.8750	0010	000 0000	1101	1111 1111	0101	1111 1111	1010	0000 0000
-FS +1 LSB	-9.9951V	-2.4988	0000	0000 0001	1111	1111 1110	0111	1111 1110	1000	0000 0001
-FS	-10.000V	-2.5000	0000	0000 0000	1111	1111 1111	0111	1111 1111	1000	0000 0000

ORDERING INFORMATION

MODEL NO.	OPER. TEMP. RANGE	SEAL
ADS-125MC	0 °C to +70 °C	Hermetic
ADS-126MC	0 °C to +70 °C	Hermetic
ADS-125MM	-55 °C to +125 °C	Hermetic
ADS-126MM	-55 °C to +125 °C	Hermetic

ACCESSORIES

Part Number	Description
TP20K	Trimming Potentiometers (Two required)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket),32 required.

For high reliability versions of the ADS-125 and the ADS-126 contact DATEL.

ADS-21AC
Low-Power, 12-Bit, 1.3 MHz Sampling A/D Converter

FEATURES

- **12-Bit resolution**
- **1.3 MHz throughput rate**
- **S/H included**
- **Single 46-pin DIP**

GENERAL DESCRIPTION

DATEL's ADS-21AC Sampling Converter combines a 12-bit A/D hybrid and a S/H hybrid (the ADC-505 and SHM-45) in one space-saving package. The ADS-21AC functional block diagram shows the A/D conversion technique used to achieve the 1.3 MHz throughput rate in a conservative low-power design. Designed and manufactured at DATEL's modern, certified hybrid assembly facility using state-of-the-art integrated circuits, the ADS-21AC provides the highest quality and performance for signal processing applications.

The ADS-21AC's 1.3 MHz throughput rate can typically be increased to about 1.5 MHz before any performance degradation. This superior performance gives design engineers a high-resolution, high-speed A/D capable of easily meeting the 1.3 MHz throughput rate for many signal processing applications.

The ADS-21AC features six pin-programmable input ranges: 0 to +10V, 0 to −5V, 0 to −10V, 0 to −20V, ±5V and ±10V dc. The input impedance is specified at 1.0 K ohm. Other specifications include no missing codes over temperature, a maximum gain tempco of ±40 ppm/°C and a maximum differential linearity tempco of ±2.5ppm/°C. Power required by both models is +/−15V dc and +/-5V dc at 2.7W maximum.

All digital inputs and three-state outputs are TTL-compatible. Output coding can be selected as straight binary/offset binary or complementary binary/complementary offset binary by using the $\overline{\text{COMP BIN}}$ pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

Manufactured using thick-film and thin-film hybrid technology, this converter's remarkable performance is based on a digital subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADS-21AC uses hermetically sealed hybrids packaged in a 46-pin DIP capable of operation over the 0°C to +70°C temperature range.

These devices are ideally suited for spectrum, waveform, vibration, and transient analysis applications in military and industrial instrumentation systems. For information on versions with high reliability screening or extended temperature operation, contact the factory.

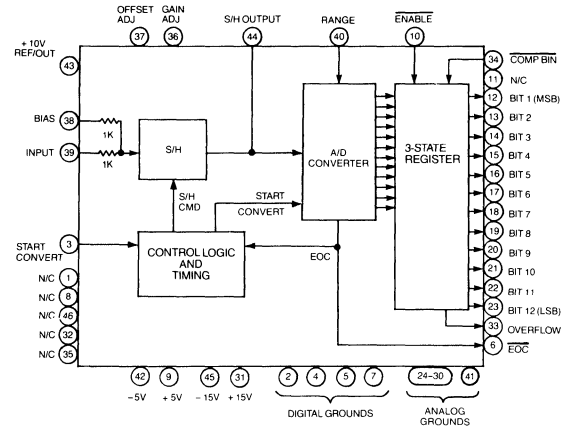


Figure 1. ADS-21AC Functional Diagram

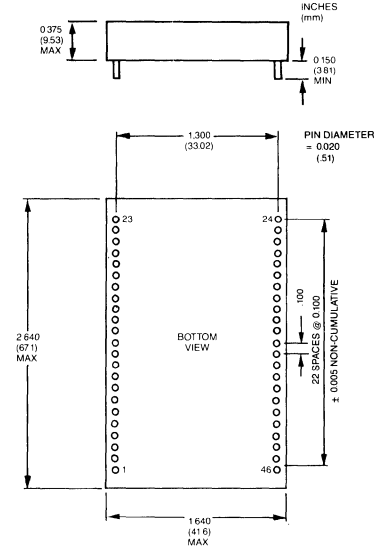


Figure 2. Mechanical Dimensions

ABSOLUTE MAXIMUM RATINGS			
PARAMETERS	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 31)	−0.3	+ 18	Volts dc
−15V Supply (Pin 45)	+0.3	−18	Volts dc
+5V Supply (Pin 9)	−0.5	+7	Volts dc
−5V Supply (Pin 42)	+0.5	−7	Volts dc
Digital Inputs (Pins 3, 10, 34)	−0.3	+5.5	Volts dc
Analog Input (Pin 39)	−15	+15	Volts dc
Lead temp. (10 Sec.)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified. For test aspects, contact the factory.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Ranges	—	0 to +10	—	Volts dc
	—	0 to −5V	—	Volts dc
	—	0 to −10V	—	Volts dc
	—	0 to −20V	—	Volts dc
	—	±10, ±5	—	Volts dc
Input Impendance 0 to −10V, 0 to +10V, 0 to −20V, ±10V	—	1K	—	ohm
0 to −5V, ±5V	—	500	—	ohms
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	µA
Logic 0	—	—	−100	µA
OUTPUTS				
Output Coding Options:	straight binary/offset binary complementary binary complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	µA
Logic 0	—	—	6.4	mA
Internal Reference (Pin 43) Voltage, +25°C	9.98	—	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current (for Pin 39)	—	—	1.5	mA
SAMPLE MODE DYNAMICS				
Frequency Response: Small Signal (−3dB)	—	16	—	MHz
Slew Rate	—	300	—	V/µS
SAMPLE-TO-HOLD SWITCHING				
Aperture Delay Time	—	6	—	nS
Aperture Uncertainty (Jitter)	—	±50	—	pS
Settling Time: 10V to ± .01% FS (± 1mV)	—	60	100	nS
10V to ±.1% FS (± 10mV)	—	40	—	nS
DYNAMIC PERFORMANCE				
Feedthrough Rejection	—	−74	—	dB
Signal to Noise Ratio (SNR)	−72	−80 below FS	—	dB
Inband Harmonics (See Fig. 6) dc to 100KHz	−72	−80 below FS	—	dB
100KHz to 500KHz	−72	−75 below FS	—	dB
HOLD-TO-SAMPLE DYNAMICS				
Acquisition Time: 10V step to ±1.0mV (.01% FS)	—	160	200	nS
10V step to ±10mV (.1% FS)	—	100	170	nS

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
PERFORMANCE FOR ±10V RANGE				
Integral Nonlinearity +25°C	—	—	±0.0125	%FSR±½LSB
0°C to +70°C	—	—	±0.0125	%FSR±½LSB
Integral Nonlin. Tempco	—	—	±3	ppm/°C
Differential Nonlinearity: +25°C	—	—	±0.0125	%FSR±½LSB
0°C to +70°C	—	—	±0.0125	%FSR±½LSB
Differential Nonlin Tempco	—	—	±2	ppm/°C
Full-Scale Absol. Accuracy: +25°C	—	±5	±12	LSB
0°C to +70°C	—	±6	±15	LSB
Unipolar Zero Error, +25°C	—	±2	±5	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Zero Error	—	—	±5	LSB
Bipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±8	LSB
Bipolar Offset Tempco	—	±17	±40	ppm/°C
Gain Error, +25°C	—	±3	±8	LSB
Gain Tempco	—	±18	±40	ppm/°C
Conversion Times: +25°C	—	750	770	nSec
0°C to +70°C	—	—	825	nSec
Throughput Rate: +25°C	1.3	—	—	MHz
0°C to +70°C	1.1	—	—	MHz
No Missing Codes (12 Bits):	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current: +15V Supply	—	+45	+60	mA
−15V Supply	—	−35	−50	mA
+5V Supply	—	+65	+100	mA
−5V Supply	—	−150	−210	mA
Power Dissipation	—	2.3	2.7	Watts
Power Supply Rejection	—	0.01	0.05	%FSRV/%V
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range*	0	—	+70	°C
Storage Temperature Range	−65	—	+125	°C
Package Type	46-pin DIP			
Pins	0.020 brass			
Weight	2 oz (50g) approx.			

*For extended temperature range versions, contact the factory.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 36 (ground pin 36 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 37 for zero/offset adjustment (leave pin 37 open for operation without adjustment).
2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies and the +10V reference (pin 43) to ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 43) to analog ground (pin 30). The −5V dc supply is treated as an analog supply and analog ground (pins 24-30) should be treated as its return path for decoupling purposes.
4. The COMP BIN input (pin 34) allows selection of binary/offset binary or complementary binary/complementary offset binary. Refer to Table 2 for the desired coding selection. The COMP BIN pin has an internal pull-up resistor and is TTL-compatible for those users desiring logic control of this function.
5. An overflow signal, pin 33, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (Enable for bits 1 through 12 and overflow.)
6. The internal Sample/Hold control signal goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before EOC goes low. This S/H low signal indicates that the converter can accept a new analog input.

Table 1. Input/Output Connections

PIN	FUNCTION	PIN	FUNCTION
1	N/C	24	ANA GND
2	DIG GND	25	ANA GND
3	START CONVERT	26	ANA GND
4	DIG GND	27	ANA GND
5	DIG GND	28	ANA GND
6	EOC	29	ANA GND
7	DIG GND	30	ANA GND
8	N/C	31	+15V
9	+5V	32	N/C
10	ENABLE	33	OVERFLOW
11	N/C	34	COMP BIN
12	BIT 1 (MSB)	35	N/C
13	BIT 2	36	GAIN ADJUST
14	BIT 3	37	OFFSET ADJUST
15	BIT 4	38	BIAS
16	BIT 5	39	INPUT
17	BIT 6	40	RANGE
18	BIT 7	41	ANA GND
19	BIT 8	42	−5V
20	BIT 9	43	+10V REF OUT
21	BIT 10	44	S/H OUT
22	BIT 11	45	−15V
23	BIT 12 (LSB)	46	N/C

Table 2. Input Connections

INPUT VOLTAGE RANGE	CONNECT INPUT PIN 38 TO:	CONNECT PIN 40 (RANGE) TO:	BINARY/ OFFSET BINARY	COMP. BINARY/ COMP. OFFSET BINARY
			CONNECT PIN 34 TO:	CONNECT PIN 34 TO:
0 to −5V	39	44	—	2,4,5,7
0 to −10V	—	44	—	2,4,5,7
0 to −20V	44	44	—	2,4,5,7
0 to +10V	EXT. −10V Ref.*	44	2,4,5,7	—
±5V	39	43	2,4,5,7	—
±10V	—	43	2,4,5,7	—

*May be Referenced to +10V Ref. (Pin 43)

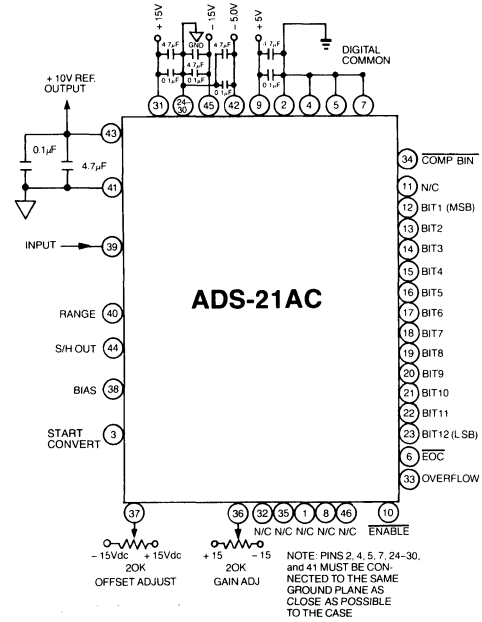


Figure 3. Connection Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 100 nanoseconds minimum to the START CONVERT input (pin 3) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustment.

   Apply a precision voltage reference source between the analog input (pin 39) and ground (pin 24). Adjust the output of the reference source per Table 4a and 4b for the unipolar zero adjustment (+½ LSB) or the bipolar zero adjustment (zero +½ LSB) for the appropriate FSR. Adjust the zero/offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 or between 1111 1111 1111 and 1111 1111 1110 depending on the output coding selected per Tables 2 and 6.

   For bipolar operation, adjust the potentiometer until the displayed code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low. Refer to Table 5.
3. Full-Scale Adjustment.

   Set the output of the voltage reference used in step 2 to the value shown in Table 4a or 4b for the unipolar or bipolar gain adjustment (+FS − 1½ LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 or between 0000 0000 0001 and 0000 0000 0000 depending on the output coding selected per Tables 2 and 4.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 5 and 6.

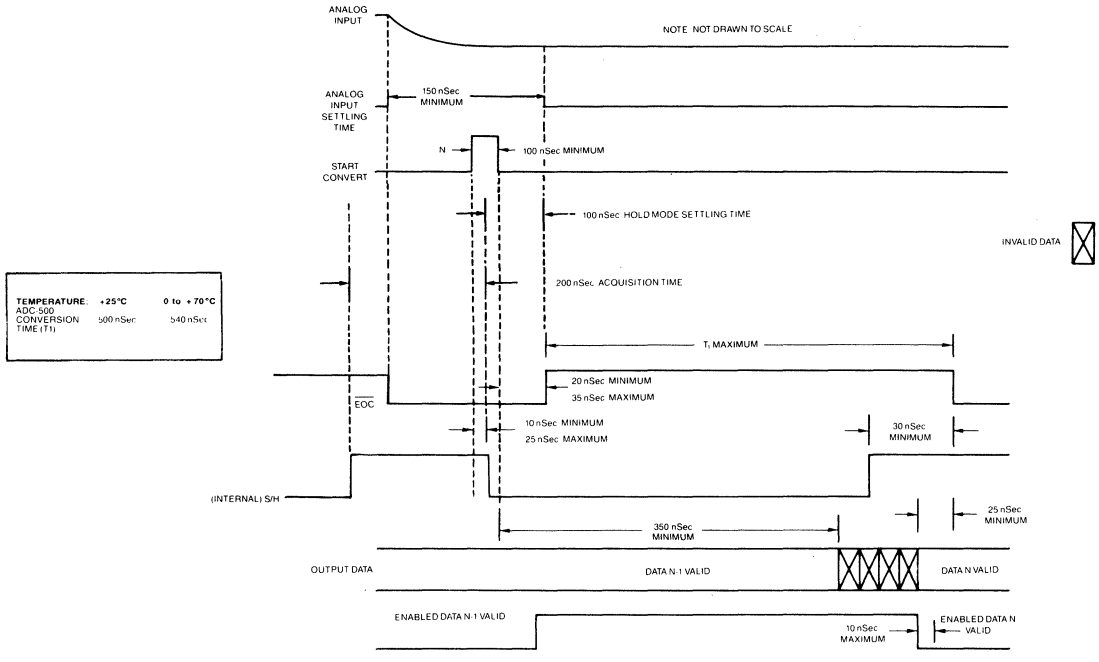


Figure 4. Timing Diagram

TIMING

Figure 4 shows the relationship between the various input signals. The timing cited in Table 3 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 3. Signal Timing Summary

LINE	DURATION IN NANOSECONDS
Start Convert	100 nSec maximum
Analog Input Settling Time	150 nSec minimum
Start Convert Low to $\overline{EOC}$ High Propagation Delay	35 nSec maximum
Start Convert Low to Previous Output Data Invalid	350 nSec minimum
Data Valid Before $\overline{EOC}$ Goes Low	25 nSec minimum
Enable to Output Data Valid Propagation Delay	10 nSec maximum

THEORY OF OPERATION

The sample-and-hold is used to capture fast signals for the ADC to then digitize. The ADS-21AC consists of a fast sample-and-hold device (SHM-45) coupled to a high-performance analog-to-digital converter (ADC-500). Figure 5 is a detailed block diagram showing DATEL's SHM-45 along with the ADC-500's internal registers and logic. The ADC-500 used in the ADS-21AC employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the Timing Diagram shown in Figure 4 for further clarification.

The SHM-45 used in the ADS-21AC acquires the input signal on the internal hold capacitor (200 nanoseconds maximum acquisition time to 0.01%). The SHM-45 is then put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-500 requires a maximum of 150 nanoseconds since the previous conversion for the Input signal to settle before initiating a conversion. The input of the ADC-500 starts settling to its final value while the SHM-45 is in the acquisition mode. The missing 50 nanoseconds of the required maximum analog input settling time is made up by the time the sample/hold is in the acquisition mode. Thus by the end of the SHM-45's hold mode settling time, the ADC-500's input is fully settled.

The SHM-45 is in the sample mode when the internal ADC-500's S/$\overline{H}$ control is high. During this period of time, the A/D is not performing a conversion.

The S/$\overline{H}$ control pin goes low after the rising edge of the start convert pulse, a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. To assure the SHM has 200 nSec maximum acquisition time, the start convert pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the start convert pulse should be 100 nsec minimum to assure the hold mode settling time of 100 nanoseconds is observed. The 100 nanoseconds takes into

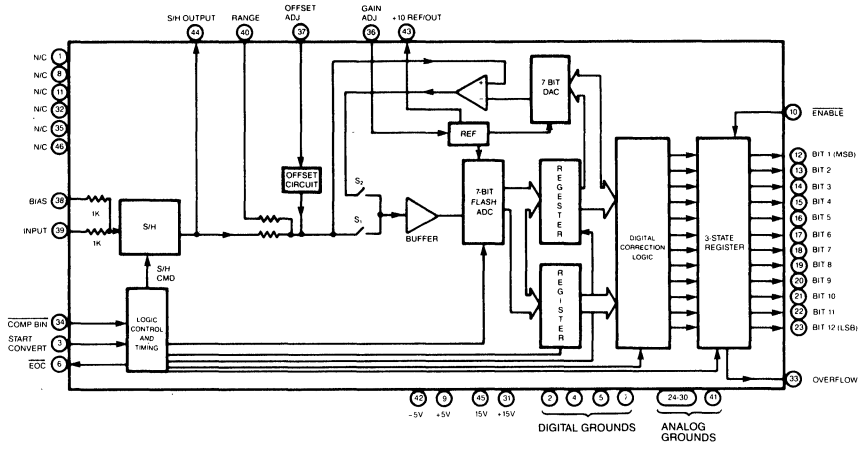


Figure 5. Detailed Block Diagram

account the min-max propagation delays of the start convert high to S/$\overline{H}$ control low propagation delays and the start convert low to $\overline{EOC}$ high propagation delays.

The analog input, having been configured for the appropriate range, is buffered and then digitized by the 7 bit flash analog-to-digital converter to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

The first pass finished, internal switching occurs effectively subtracting the output of the DAC from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit analog-to-digital converter. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the output is present at the three-state output buffers.

Once the second step of the flash analog-to-digital converter is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{EOC}$ going low). The internal Sample/Hold control signal line goes low a minimum of 30 nanoseconds before $\overline{EOC}$ goes low, indicating that the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the start convert pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{EOC}$ goes low and valid up to 350 nanoconds after the falling edge of the next start convert pulse. There is 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid.

The overall throughput of the ADS-21AC using the ADC-500 and the SHM-45 internally consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds for observance of min-max propagation delays and 470 nanoseconds for the conversion process (S/$\overline{H}$ control pin saves 30 nanoseconds). However, total guaranteed throughput of the ADS-21AC is a maximum of 770 nanoseconds for the system for a guaranteed throughput rate of 1.3 MHz. Retriggering of the start convert pulse before $\overline{EOC}$ goes low will not initiate a new A/D conversion.

The performance characteristics shown in Table 7 and Figure 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

Table 4a. Zero And Gain Adjust For Unipolar Use

UNIPOLAR FSR	ZERO ADJUST +½ LSB	GAIN ADJUST +FS – 1½ LSB
0 to –5V	–0.61mV	– 4.9982V
0 to –10V	–1.22mV	– 9.9963V
0 to –20V	–2.44mV	–19.9927V
0 to +10V	+1.22mV	+ 9.9963V

Table 4b. Zero And Gain Adjust For Bipolar Use

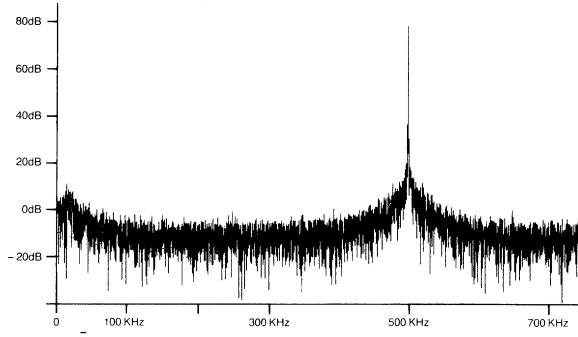
BIPOLAR FSR	ZERO ADJUST ZERO +½ LSB	GAIN ADJUST +FS – 1½ LSB
±10V dc	+2.44 mV	+9.9927V dc
±5V dc	+1.22 mV	+4.9963V dc

Table 5. Output Coding for Bipolar Operation

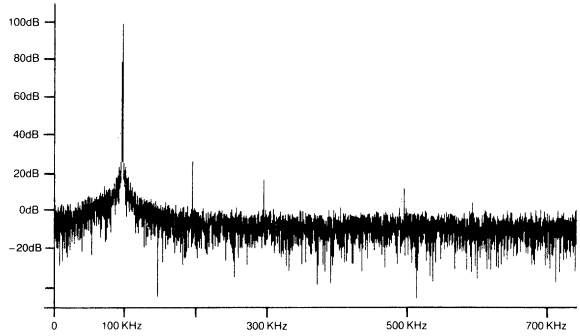
BIPOLAR SCALE	INPUT RANGES VOLTS dc		OUTPUT COMING	
			OFFSET BINARY	COMP. OFFSET BINARY
	±5V	±10V	MSB LSB	MSB LSB
+ FS – 1 LSB	+4.9976V	+9.9951V	1111 1111 1111	0000 0000 0000
+ ¾ FS	+3.7500V	+7.5000V	1110 0000 0000	0001 1111 1111
+ ½ FS	+2.5000V	+5.0000V	1100 0000 0000	0011 1111 1111
0	0.0000V	0.0000V	1000 0000 0000	0111 1111 1111
– ½ FS	–2.5000V	–5.0000V	0100 0000 0000	1011 1111 1111
– ¾ FS	–3.7500V	–7.5000V	0010 0000 0000	1101 1111 1111
–FS +1 LSB	–4.9976V	–9.9951V	0000 0000 0001	1111 1111 1110
–FS	–5.0000V	–10.0000V	0000 0000 0000	1111 1111 1111

Table 6. Output Coding For Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES VOLTS dc				OUTPUT CODING					
					STRAIGHT BINARY			COMP. BINARY		
	0 to −5V	0 to −10V	0 to +10V	0 to −20V	MSB		LSB	MSB		LSB
+FS −1 LSB	−4.998V	−9.9976V	+9.9976V	−19.9951V	1111	1111	1111	0000	0000	0000
7/8 FS	−4.375V	−8.750V	+8.750V	−17.500V	1110	0000	0000	0001	1111	1111
3/4 FS	−3.750V	−7.500V	+7.500V	−15.00V	1100	0000	0000	0011	1111	1111
1/2 FS	−2.500V	−5.00V	+5.00V	−10.00V	1000	0000	0000	0111	1111	1111
1/4 FS	−1.250V	−2.500V	+2.500V	−5.000V	0100	0000	0000	1011	1111	1111
1/8 FS	−0.625V	−1.250V	+1.250V	−2.500V	0010	0000	0000	1101	1111	1111
1 LSB	−0.0012V	−0.0024V	+0.0024V	−0.0049V	0000	0000	0001	1111	1111	1110
0	0.0000V	0.0000V	0.000V	0.0000V	0000	0000	0000	1111	1111	1111



ADS-21AC FFT Report for Total Harmonic Distortion — 500 KHz Input



ADS-21AC FFT Report for Total Harmonic Distortion — 100 KHz Input

Figure 6. Harmonic Distortion Performance

Table 7. Performance Characteristics At Different Temperatures

CHARACTERISTICS	VALUE
Conversion Rate (Changing Inputs): +25°C 0°C to +70°C	 1.3 MHz minimum 1.1 MHz minimum
Harmonic Distortion (Below E5) +25°C 0°C to +70°C	 −72dB minimum −72dB minimum

ORDERING INFORMATION

MODEL NO.	TEMP RANGE	THROUGHPUT RATE
ADS-21AC*	0 to +70°C	1.3MHz

*Contact factory for high reliability or extended temperature range versions.

ADS-22AC
Low-Power, 12-Bit, 1.0 MHz Sampling A/D Converter

1

FEATURES

- **12-Bit resolution**
- **1.0 MHz throughput rate**
- **S/H included**
- **Single 46-pin DIP**

GENERAL DESCRIPTION

DATEL's ADS-22AC sampling converter combines a 12-bit A/D hybrid and a S/H hybrid (the ADC-505 and SHM-45) in one space - saving package. The ADS-22AC functional block diagram at the right shows the A/D conversion technique used to achieve the 1.0 MHz throughput rate in a conservative low power design. Designed and manufactured at DATEL's modern, certified hybrid assembly facility using state of the art integrated circuits, the ADS-22AC provides the highest quality and performance for signal processing applications.

The ADS-22AC's 1.0 MHz throughput rate can typically be increased to about 1.25 MHz before any performance degradation. This superior performance gives design engineers a high-resolution, high-speed A/D capable of easily meeting the 1.0 MHz throughput rate for many signal processing applications.

The ADS-22AC features six pin-programmable input ranges: 0 to +10V, 0 to −5V, 0 to −10V, 0 to −20V, ±5V and ±10V dc. The input impedance is specified at 1.0 K ohms. Other specifications include no missing codes over temperature, a maximum gain tempco of ±40 ppm/°C and a maximum differential linearity tempco of ±2.5ppm/°C. Power required by both models is ±15V dc and ±5V dc at 2.8 W maximum.

All digital inputs and three-state outputs are TTL-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary by using the $\overline{\text{COMP BIN}}$ pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

Manufactured using thick-film and thin-film hybrid technology, this converter's remarkable performance is based on a digital subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADS-22AC uses hermetically sealed hybrids packaged in a 46-pin DIP capable of operation over the 0°C to +70°C temperature range.

These devices are ideally suited for spectrum, waveform, vibration, and transient analysis applications in military and industrial instrumentation systems. For information on versions with high reliability screening or extended temperature operation, contact the factory.

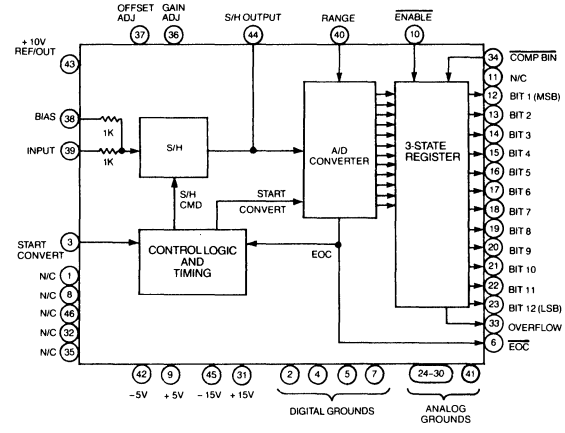


Figure 1. ADS-22AC Functional Diagram

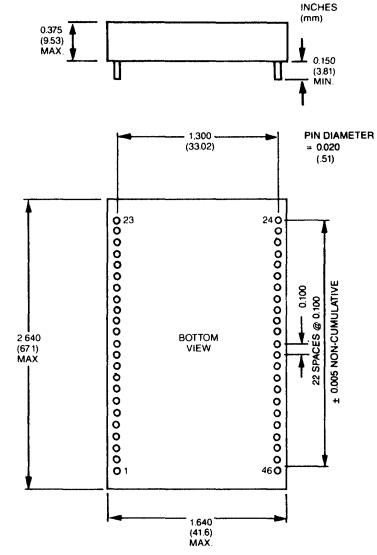


Figure 2. Mechanical Dimensions

ABSOLUTE MAXIMUM RATINGS			
PARAMETERS	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 31)	−0.3	+ 18	Volts dc
−15V Supply (Pin 45)	+0.3	−18	Volts dc
+5V Supply (Pin 9)	−0.5	+7	Volts dc
−5V Supply (Pin 42)	+0.5	−7	Volts dc
Digital Inputs (Pins 3, 10, 34)	−0.3	+5.5	Volts dc
Analog Input (Pin 39)	−15	+15	Volts dc
Lead temp. (10 Sec.)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified. For test aspects, contact the factory.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Ranges	—	0 to +10	—	Volts dc
	—	0 to −5V	—	Volts dc
	—	0 to −10V	—	Volts dc
	—	0 to −20V	—	Volts dc
	—	±10, ±5	—	Volts dc
Input Impendance				
0 to −10V, 0 to +10V,				
0 to −20V, +10V	—	1K	—	ohm
0 to −5V, ±5V	—	500	—	ohms
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Leading: Logic 1	—	—	2.5	µA
Logic 0	—	—	−100	µA
OUTPUTS				
Output Coding Options:	straight binary/offset binary complementary binary complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Leading: Logic 1	—	—	−160	µA
Logic 0	—	—	6.4	mA
Internal Reference (Pin 43)				
Voltage, +25°C	9.98	—	10.02	Volts dc
Drift	—	±5	±30	PPM/°C
External Current (for Pin 39)	—	—	1.5	mA
SAMPLE MODE DYNAMICS				
Frequency Response:				
Small Signal (−3dB)	—	16	—	MHz
Slew Rate	—	300	—	V/µS
SAMPLE-TO-HOLD SWITCHING				
Aperture Display Time	—	6	—	nS
Aperture Uncertainty (Jitter)	—	±50	—	pS
Settling Time:				
10V to ±.01% FS (±1mV	—	60	100	nS
10V to ±.1% FS (±10mV)	—	40	—	nS
DYNAMIC PERFORMANCE				
Feedthrough Rejection	—	−74	—	dB
Signal to Noise Ratio (SNR)	−72	−80 below FS	—	dB
Inband Harmonics (see Fig 6)				
dc to 100KHz	−72	−80 below FS	—	dB
100KHz to 500KHz FS	−72	−75 below FS	—	dB
HOLD-TO-SAMPLE DYNAMICS				
Acquisition Time:				
10V step to ±1.0mV (.01% FS)	—	160	200	nS
10V step to ±10mV (.1% FS)	—	100	170	nS

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
PERFORMANCE FOR ±10V RANGE				
Integral Nonlinearity				
+25°C	—	—	±0.0125	%FSR±½LSB
0°C to +70°C	—	—	±0.0125	%FSR±½LSB
Integral Nonlin. Tempco	—	—	±3	ppm/°C
Differential Nonlinearity:				
+25°C	—	—	±0.0125	%FSR±½LSB
0°C to +70°C	—	—	±0.0125	%FSR±½LSB
Differential Nonlin Tempco	—	—	±2.5	ppm/°C
Full-Scale Absol. Accuracy:				
+25°C	—	±5	±12	LSB
0°C to +70°C	—	±6	±15	LSB
Unipolar Zero Error, +25°C	—	±2	±5	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Zero Error	—	—	±5	LSB
Bipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±8	LSB
Bipolar Offset Tempco	—	±17	±40	ppm/°C
Gain Error, +25°C	—	±3	±8	LSB
Gain Tempco	—	±18	±40	ppm/°C
Conversion Times:				
ADS-22AC	—	900	1µsec	nSec
Throughput Rate:				
ADS-22AC	1.0	—	—	MHz
No Missing Codes (12 Bits):	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current:				
+15V Supply	—	+45	+60	mA
−15V Supply	—	−35	−50	mA
+5V Supply	—	+65	+100	mA
−5V Supply	—	−150	−210	mA
Power Dissipation	—	2.3	2.7	Watts
Power Supply Rejection	—	0.01	0.05	%FSRV/%V
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range*	0	—	+70	°C
Storage Temperature Range	−65	—	+125	°C
Package Type	46-pin DIP			
Pins	0.020 brass			
Weight	2 oz (50g) approx.			

*For extended temperature range versions, contact the factory.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 36 (ground pin 36 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 37 for zero/ offset adjustment (leave pin 37 open for operation without adjustment).
2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital supplies and the +10V reference (pin 43) ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 43) to analog ground (pin 30). The −5V dc supply is treated as an analog supply and analog ground (pins 24-30) should be treated as its return path for decoupling purposes.
4. The COMP BIN input (pin 34) allows selection of binary/offset binary or complementary binary/complementary offset binary. Refer to Table 2 for the desired coding selection. The COMP BIN pin has an internal pull-up resistor and is TTL compatible for those users desiring logic control of this function.
5. An overflow signal, pin 33, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (Enable for bits 1 through 12 and overflow).
6. The internal Sample/Hold control signal goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before EOC goes low. This S/H low signal indicates that the converter can accept a new analog input.

Table 1. Input/Output Connections

PIN	FUNCTION	PIN	FUCTION
1	N/C	24	ANA GND
2	DIG GND	25	ANA GND
3	START CONVERT	26	ANA GND
4	DIG GND	27	ANA GND
5	DIG GND	28	ANA GND
6	EOC	29	ANA GND
7	DIG GND	30	ANA GND
8	N/C	31	+15V
9	+5V	32	N/C
10	ENABLE	33	OVERFLOW
11	N/C	34	COMP BIN
12	BIT 1 (MSB)	35	N/C
13	BIT 2	36	GAIN ADJUST
14	BIT 3	37	OFFSET ADJUST
15	BIT 4	38	BIAS
16	BIT 5	39	INPUT
17	BIT 6	40	RANGE
18	BIT 7	41	ANA GND
19	BIT 8	42	−5V
20	BIT 9	43	+10V REF OUT
21	BIT 10	44	S/H OUT
22	BIT 11	45	−15V
23	BIT 12 (LSB)	46	N/C

Table 2. Input Connections

INPUT VOLTAGE RANGE	CONNECT INPUT PIN 38 TO:	CONNECT PIN 40 (RANGE) TO:	BINARY/ OFFSET BINARY CONNECT PIN 34 TO:	COMP. BINARY/ COMP. OFFSET BINARY CONNECT PIN 34 TO:
0 to −5V	39	44	—	2,4,5,7
0 to −10V	—	44	—	2,4,5,7
0 to −20V	44	44	—	2,4,5,7
0 to +10V	EXT. −10V Ref.*	44	2,4,5,7	—
±5V	39	43	2,4,5,7	—
±10V	—	43	2,4,5,7	—

*May be Referenced to +10V Ref. (Pin 43)

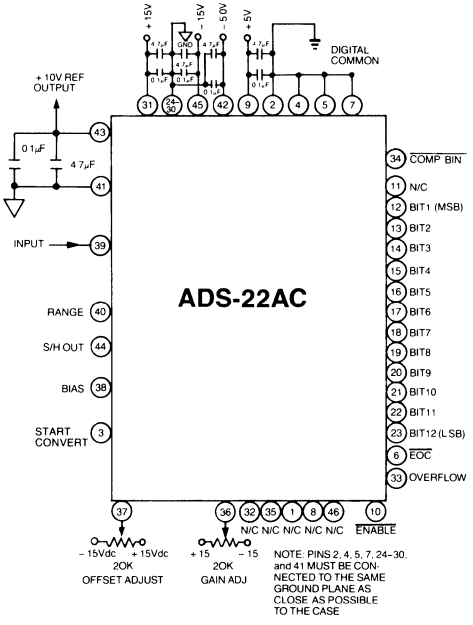


Figure 3. Connection Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 100 nanoseconds minimum to the START CONVERT input (pin 3) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustment.
   Apply a precision voltage reference source between the analog input (pin 39) and ground (pin 24). Adjust the outut of the reference source per Table 4a and 4b for the unpolar zero adjustment (+ ½ LSB) or the bipolar zero adjustment (zero + ½ LSB) for the appropriate FSR. Adjust the zero/offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 or between 1111 1111 1111 and 1111 1111 1110 depending on the output coding selected per Tables 2 and 6.
   For bipolar operation, adjust the potentiometer until the displayed code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low. Refer to Table 5.
3. Full-Scale Adjustment.
   Set the output of the voltage reference used in step 2 to the value shown in Table 4a or 4b for the unipolar or bipolar gain adjustment (+ FS − 1½ LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 or between 0000 0000 0001 and 0000 0000 0000 depending on the output coding selected per Tables 2 and 4.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 5 and 6.

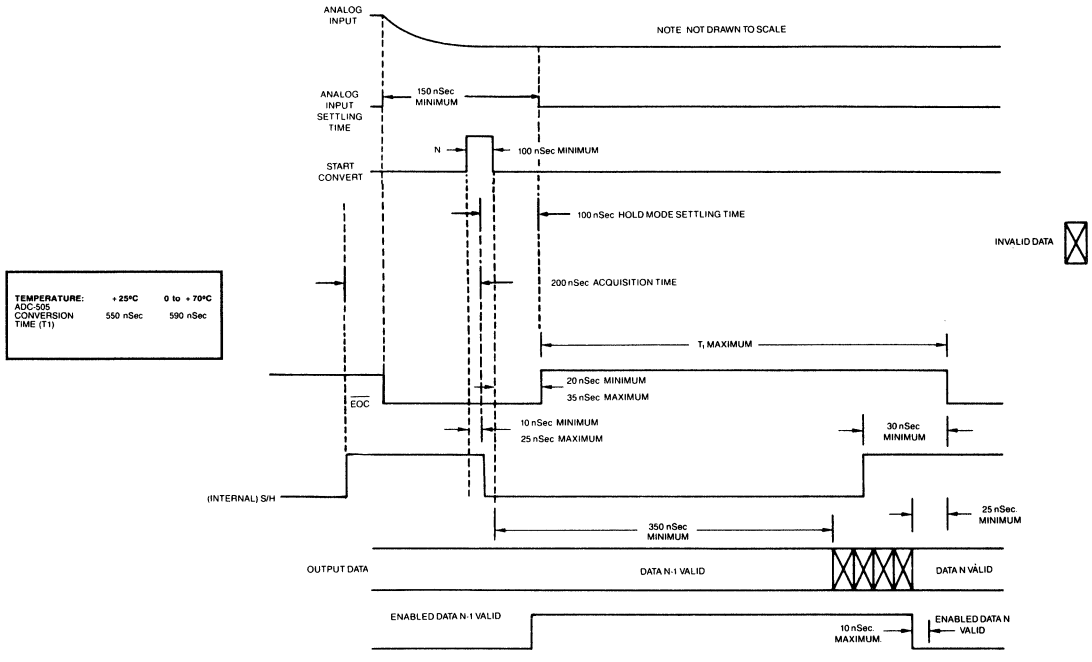


Figure 4. Timing Diagram

TIMING

Figure 4 shows the relationship between the various input signals. The timing cited in Table 3 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

Table 3. Signal Timing Summary

LINE	DURATION IN NANOSECONDS
Start Convert	100 nSec maximum
Analog Input Settling Time	150 n Sec minimum
Start Convert Low to $\overline{EOC}$ High Propagation Delay	35 nSec maximum
Start Convert Low to Previous Output Data Invalid	350 nSec minimum
Data Valid Before $\overline{EOC}$ Goes Low	25 nSec minimum
Enable to Output Data Valid Propagation Delay	10 nSec maximum

THEORY OF OPERATION

This theory of operation describes how the ADS-22AC uses an internal sample-and-hold to capture fast signals for an internal ADC to then digitize. The ADS-22AC consists of a fast sample-and- hold device (DATEL's SHM-45) and a high performance analog- to-digital converter (DATEL's ADC-505). Figure 5 is a detailed block diagram showing the SHM-45 along with the ADC-505's internal registers and logic. The ADC-505 used in the ADS-22AC employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the Timing Diagram shown in Figure 4 for further clarification.

The SHM-45 used in the ADS-22AC acquires the input signal on the internal hold capacitor (200 nanoseconds maximum acquisition time to 0.01%). The SHM-45 is then put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-505 requires a maximum of 150 nanoseconds since the previous conversion for the Input signal to settle before initiating a conversion. The input of the ADC-505 starts settling to its final value while the SHM-45 is in the acquisition mode. The missing 50 nanoseconds of the required maximum analog input settling time is made up by the time the sample/hold is in the acquisition mode. Thus, by the end of the SHM-45's hold mode settling time, the ADC-505's input is fully settled.

The SHM-45 is in the sample mode when the internal ADC-505's S/$\overline{H}$ control is high. During this period of time, the A/D is not performing a conversion.

The S/$\overline{H}$ control pin goes low after the rising edge of the start convert pulse a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. To assure the SHM has 200 nSec maximum acquisition time, the start convert pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the start convert pulse should be

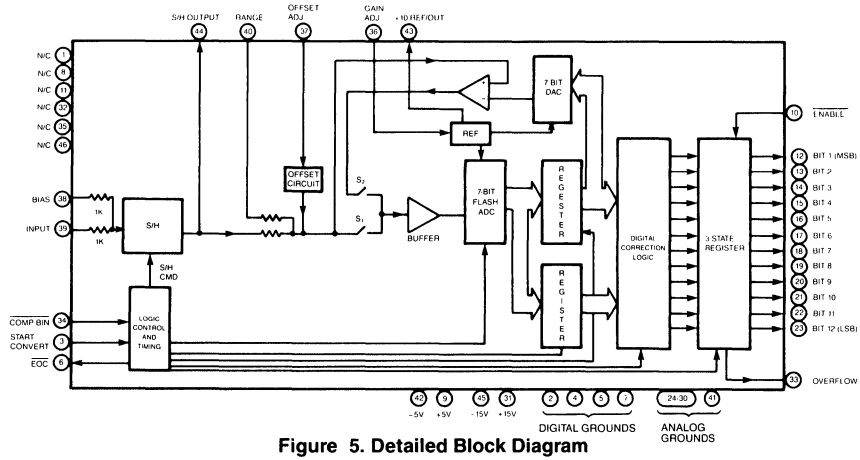


Figure 5. Detailed Block Diagram

100 nsec minimum to assure the hold mode settling time of 100 nanoseconds is observed. The 100 nanoseconds takes into account the min-max propagation delays of the start convert high to S/$\overline{H}$ control low propagation delays and the start convert low to $\overline{EOC}$ high propagation delays.

The analog input, having been configured for the appropriate range, is buffered and then digitized by the 7 bit flash ADC to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

The first pass finished, internal switching occurs effectively subtracting the output of the digital-to-analog converter from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit ADC. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the out put is present at the three-state output buffers.

Once the second step of the flash analog-to-digital conversion is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{EOC}$ going low). The internal Sample/Hold control signal line goes low a minimum of 30 nanoseconds before $\overline{EOC}$ goes low, indicating that the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the start convert pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{EOC}$ goes low and valid up to 350 nanoseconds after the falling edge of the next start convert pulse. There is 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid.

The overall throughput of the ADS-22AC using the ADC-505 and the SHM-45 internally consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds for observance of min-max propagation delays and 560 nanoseconds for the conversion process (S/$\overline{H}$ control pin saves 30 nanoseconds). Total guaranteed throughput is a maximum of 1 microsecond for the system for a guaranteed throughput rate of 1.0 MHz. Retriggering of the start convert pulse before $\overline{EOC}$ goes low will not initiate a new A/D conversion.

The performance characteristics shown in Table 7 and in Figure 6 apply over the operating temperature range and over the power supply operating range unless otherwise specified. These characteristics are guaranteed by design.

Table 4a. Zero And Gain Adjust For Unipolar Use

UNIPOLAR FSR	ZERO ADJUST +½ LSB	GAIN ADJUST +FS − 1½ LSB
0 to −5V	−0.61mV	− 4.9982V
0 to −10V	−1.22mV	− 9.9963V
0 to −20V	−2.44mV	−19.9927V
0 to +10V	+1.22mV	+ 9.9963V

Table 4b. Zero And Gain Adjust For Bipolar Use

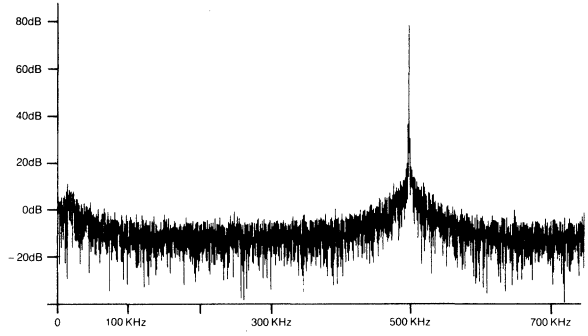
BIPOLAR FSR	ZERO ADJUST Zero +½ LSB	GAIN ADJUST +FS − 1½ LSB
±10V	+2.44mV	+9.9927V
±5V	+1.22mV	+4.9963V

Table 5. Output Coding for Bipolar Operation

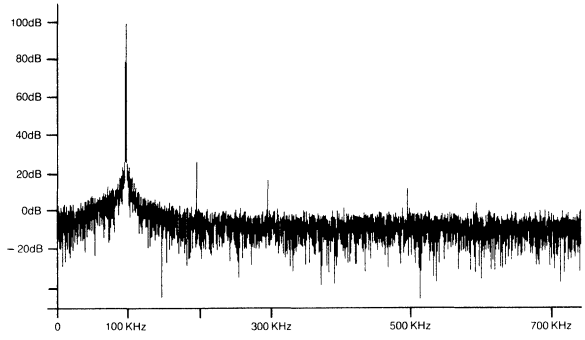
BIPOLAR SCALE	INPUT RANGES VOLTS dc		OUTPUT COMING	
			OFFSET BINARY	COMP. . OFFSET BINARY
	±5V	±10V	MSB LSB	MSB LSB
+ FS − 1 LSB	+4.9976V	+9.9951V	1111 1111 1111	0000 0000 0000
+ ¾ FS	+3.7500V	+7.5000V	1110 0000 0000	0001 1111 1111
+ ½ FS	+2.5000V	+5.0000V	1100 0000 0000	0011 1111 1111
0	0.0000V	0.0000V	1000 0000 0000	0111 1111 1111
− ½ FS	−2.5000V	−5.0000V	0100 0000 0000	1011 1111 1111
− ¾ FS	−3.7500V	−7.5000V	0010 0000 0000	1101 1111 1111
−FS +1 LSB	−4.9975V	−9.9951V	0000 0000 0001	1111 1111 1110
−FS	−5.0000V	−10.0000V	0000 0000 0000	1111 1111 1111

Table 6. Output Coding For Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES VOLTS dc				OUTPUT CODING					
					STRAIGHT BINARY			COMP. BINARY		
	0 to −5V	0 to −10V	0 to +10V	0 to −20V	MSB		LSB	MSB		LSB
+FS −1 LSB	−4.998V	−9.9976V	+9.9976V	−19.9951V	1111	1111	1111	0000	0000	0000
7/8 FS	−4.375V	−8.750V	+8.750V	−17.500V	1110	0000	0000	0001	1111	1111
3/4 FS	−3.750V	−7.500V	+7.500V	−15.00V	1100	0000	0000	0011	1111	1111
1/2 FS	−2.500V	−5.00V	+5.00V	−10.00V	1000	0000	0000	0111	1111	1111
1/4 FS	−1.250V	−2.500V	+2.500V	−5.000V	0100	0000	0000	1011	1111	1111
1/8 FS	−0.625V	−1.250V	+1.250V	−2.500V	0010	0000	0000	1101	1111	1111
1 LSB	−0.0012V	−0.0024V	+0.0024V	−0.0049V	0000	0000	0001	1111	1111	1110
0	0.0000V	0.0000V	0.000V	0.0000V	0000	0000	0000	1111	1111	1111



ADS-22AC FFT Report for Total Harmonic Distortion — 500 KHz Input



ADS-22AC FFT Report for Total Harmonic Distortion — 100 KHz Input

Figure 6. Harmonic Distortion Performance

Table 7. Performance Characteristics At Different Temperatures

CHARACTERISTICS	VALUE
Conversion Rate (Changing Inputs): 0°C to +70°C	 1.0 MHz minimum
Harmonic Distortion (Below E5) +25°C 0°C to +70°C	 −72dB minimum −72dB minimum

ORDERING INFORMATION

MODEL NO.	TEMP RANGE	THROUGHPUT RATE
ADS-22AC*	0 to + 70°C	1.0MHz

*Contact factory for high reliability or extended temperature range versions.

ADC-574Z, -674Z
12-Bit, Microprocessor-Compatible A/D Converter with S/H

FEATURES

- **Complete 12-Bit A/D converters with sample-hold, reference, and clock**
- **Pin-to-pin compatible with industry standard HI574A/674A**
- **No missing codes over temperature**
- **15 μSec. Conversion time (ADC-674Z)**
- **150 mW maximum power dissipation**

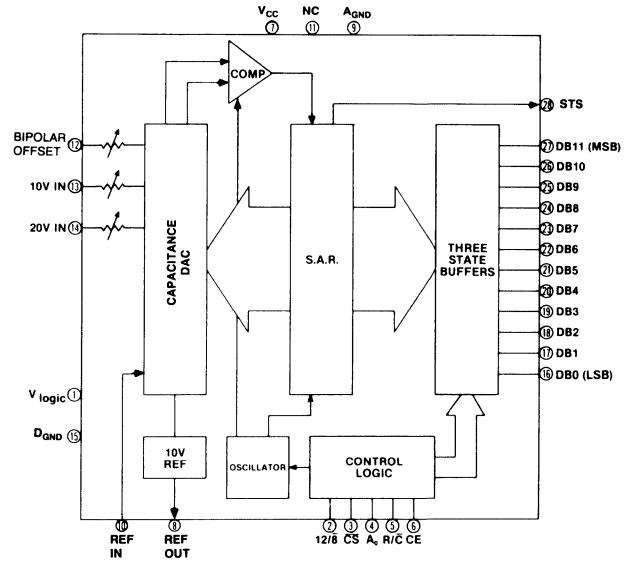
GENERAL DESCRIPTION

DATEL's ADC-574Z/674Z family of A/D converters are single chip monolithic CMOS versions of the industry standard devices. The sample-hold feature of this device allows conversion of input frequencies of up to 5 KHz without requiring an external circuit.

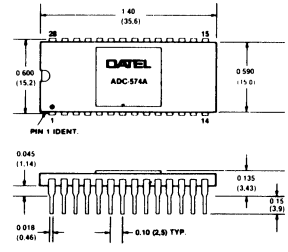
These units include a reference, clock, three-state outputs, and digital interface circuit which allows direct connection to the microprocessor address bus and control lines. The ADC-574Z completes a 12-bit conversion in 25 microseconds, while the ADC-674Z converts in 15 microseconds. Four user selectable input ranges are provided: 0 to +10V, 0 to +20V, ±5V, and ±10V dc. Laser trimming ensures specified linearity, gain, and offset accuracy.

Monolithic CMOS construction keeps the power consumption to a low 150 mW maximum, plus it reduces ground noise and parasitics.

The ADC-574Z/674Z are available for operation over the commercial, 0°C to +70°C temperature range. All models are packaged in 28-pin dual-in-line sidebrazed ceramic packages.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	V_{logic}, +5V	15	D_{GND}
2	12/8, DATA MODE SELECT	16	DB0 (LSB)
3	$\overline{CS}$, CHIP SELECT	17	DB1
4	A_0, BYTE ADDRESS/SHORT CYCLE	18	DB2
5	R/$\overline{C}$, READ/CONVERT	19	DB3
6	CE, CHIP ENABLE	20	DB4
7	V_{CC}	21	DB5
8	REFERENCE OUT	22	DB6
9	A_{GND}	23	DB7
10	REFERENCE IN	24	DB8
11	NC	25	DB9
12	BIPOLAR OFFSET	26	DB10
13	10V IN	27	DB11 (MSB)
14	20V IN	28	STS

ABSOLUTE MAXIMUM RATINGS	
Analog Supply Voltage (V_{CC} to D_{GND})	0 to +16.5
Logic Supply Voltage (Pin 1)	0V to +7V
Analog Common (Pin 9) to Digital Common (Pin 15)	±1V
Digital Control Inputs (Pins 2–6) to Digital Common	−0.5V to V_{logic} +0.5V
Analog Inputs (Pins 10, 12, 13) to Analog Common	±16.5V
20V Input (Pin 14) to Analog Common	±24V
Ref. Out (Pin 8) Short Circuit Duration	Indefinite to common momentary to V_S
Chip Temperature	100°C
Package Dissipation	1000 mW
Lead Temperature, soldering	300°C, 10 Sec.
Thermal Resistance, Junction-to-Ambient	48°C/W

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +15V dc (or +12V dc) and +5V dc supply voltage, unless otherwise noted.

ANALOG INPUTS	
Input Voltage Range, unipolar	0 to +10V, 0 to +20V
bipolar	±5V, ±10V
Input Impedance, 10V range	5 KΩ ±25%
20V range	10 KΩ ±25%
ANALOG OUTPUTS[1]	
Internal Reference, voltage	+10.00V ±0.1 max.
current	2.0 mA max.
DIGITAL INPUTS[2]	
Logic Levels: logic "1"	+2.4V min. to +5.5V max.
logic "0"	−0.5V min. to +0.8V max.
Loading: logic current, min.	−5 μA
max.	+5 μA
Capacitance	5 pF
DIGITAL OUTPUTS[3]	
Logic Levels: logic "0" (I sink, 1.6 mA)	+0.4V max.
logic "1" (I source, 500 μA)	+2.4V min.
Leakage (high impedance state)	−5 μA min. to +5 μA max.
Capacitance	5 pF
POWER REQUIREMENTS	
Analog Supply Voltage Range	+11.4V to +16.5V
Logic Supply Voltage Range	+4.5V to +5.5V
Supply Current max., Analog Supply	+7 mA
Logic Supply	+1 mA
Power Consumption ($\pm V_S$ = ±15V), max.	150 mW
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Type	28 pin side brazed ceramic DIP

	574ZC 674ZC	574ZB 674ZB	574ZA 674ZA
Resolution	12 Bits	12 Bits	12 Bits
Unipolar Offset, max.[5]	±2 LSB	±2 LSB	±2 LSB
Conversion Time, max.	25 μSec. 15 μSec.	25 μSec. 15 μSec.	25 μSec. 15 μSec.
Full Scale Calibration Error, max.[6]			
at 25°C	0.3% of F.S.	0.3% of F.S.	0.3% of F.S.
over temp.[7]	0.5%	0.4%	0.35%
over temp.[8]	0.22%	0.12%	0.05%
Linearity Error, max. (over temp)	±1 LSB	±½ LSB	±½ LSB
Differential Linearity Error[4]	±1 LSB	±½ LSB	±½ LSB
Bipolar Offset, max.[5]	±10 LSB	±4 LSB	±4 LSB
Tempco:[9]			
Unipolar Offset	10 ppm/°C	5 ppm/°C	5 ppm/°C
Bipolar Offset	10 ppm/°C	5 ppm/°C	5 ppm/°C
Full Scale Calibration	45 ppm/°C	25 ppm/°C	10 ppm/°C
Power Supply Rejection:[10]			
$+V_S$ = 13.5V to 16.5V or +11.4V to +12.6V	±2 LSB	±1 LSB	±1 LSB
$\pm V_{logic}$ = +4.5V to +5.5V	±½ LSB	±½ LSB	±½ LSB

FOOTNOTES:

1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.
2. Logic Inputs — CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$.
3. Logic Outputs — DB11-DB0, $\overline{STS}$.
4. Over temperature.
5. Adjustable to zero.
6. With 50 Ω fixed resistor from REF OUT to REF IN. Adjustable to zero.
7. No adjustment at 25°C.
8. With adjustment at 25°C.
9. Guaranteed maximum change, Tmin to Tmax (using internal reference).
10. Maximum change in full scale calibration.

TECHNICAL NOTES

1. The ADC-574Z, -674Z may interface directly to a microprocessor which can take full control of each conversion, or the device can be operated in the "stand alone" mode (controlled only by the R/$\overline{C}$ input). Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion and reading the output data when ready. The data may be read 12 bits at once or 8 followed by 4 in a left-justified format. There are five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE) and all are TTL/CMOS compatible. (See Control Input Truth Table.)

2. A conversion is initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$. One, two, or all three may be dynamically controlled. The nominal delay for each of the three inputs is the same and if necessary, all three may change states simultaneously. If it is required that a particular input controls the start of conversion, the other two should be set up at least 50 nanoseconds earlier. (See Start Convert Timing.)

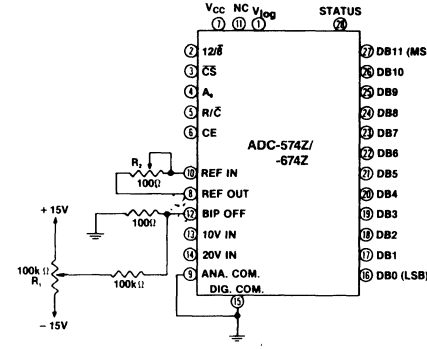
3. To read the output data, four conditions must be met (or the output buffers will remain in high impedance state): R/$\overline{C}$ taken high, STS low, CE high and $\overline{CS}$ low. When this is accomplished, the data lines are activated according to the state of the 12/$\overline{8}$ and A_0 inputs. (See START CONVERT, READ CYCLE TIMING and APPLICATION.)

4. The analog signal source driving the ADC-574Z, -674Z's input will see a nominal load of 5 KΩ (10V range) or 10 KΩ (20V range). However, the other end of these input resistors may change 400 mV with each bit decision, causing sudden changes in current at the analog input. Therefore, the signal source must maintain its output voltage while supplying these step changes in load current which occur at 1.6 microsecond intervals. This requires low output impedance and fast settling by the signal source. If a sample/hold is required to precede the converter, DATEL's SHM-20 is recommended.

5. The power supply used should be low noise and well regulated. Voltage spikes can affect accuracy. If a switching supply is used, the outputs should be carefully filtered to assure "noise free" dc voltage to the converter. Decoupling capacitors should be used on all power supply pins; the +5V dc supply decoupling capacitor should be connected directly from $+V_{logic}$ (Pin 1) to digital common (Pin 15). V_{CC} (Pin 7) should be decoupled directly to A_{GND} (Pin 9). It is recommended that a 10 μF tantalum type in parallel with a 0.1 μF ceramic type be used for decoupling.

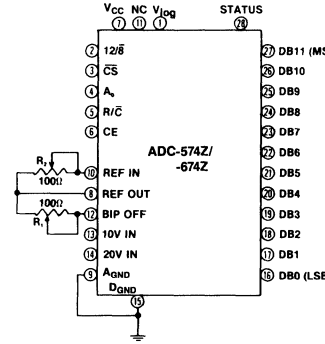
6. The use of good circuit board layout techniques is required for rated performance. It is recommended that a double sided printed circuit board with a ground plane on the component side is used. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard will have an unpredictable effect on accuracy. Sensitive analog signals should be routed between ground traces and kept away from digital lines. If analog and digital lines must cross, they should do so at right angles.

TYPICAL CONNECTIONS



UNIPOLAR CONFIGURATION

NOTES: The trimpots shown are for calibration of offset and gain. If adjustment is not required in unipolar; replace R_2 with a 50Ω, 1% metal film resistor, omit the network on Pin 12 and connect Pin 12 to Pin 9. In bipolar; either R_1, or R_2 or both can be replaced by 50Ω, 1% metal film resistors.



BIPOLAR CONFIGURATION

CODING TABLES

INPUT RANGE		OUTPUT CODING		
0 to + 10V	0 to + 20V	MSB		LSB
+10.000	+20.0000	1111	1111	1111
+9.9963	+19.9927	1111	1111	111Ø*
+5.0012	+10.0024	1000	0000	000Ø*
+4.9988	+9.9976	Ø000	0000	000Ø*
+4.9963	+9.9927	0111	1111	111Ø*
+0.0012	+0.0024	0000	0000	000Ø*
0.0000	+0.0000	0000	0000	0000

INPUT RANGE		OUTPUT CODING		
±5V	±10V	MSB		LSB
+5.0000	+10.0000	1111	1111	1111
+4.9963	+9.9927	1111	1111	111Ø*
+0.0012	+0.0024	1000	0000	000Ø*
-0.0012	-0.0024	Ø000	0000	000Ø*
-0.0037	-0.0073	0111	1111	111Ø*
-4.9988	-9.9976	0000	0000	000Ø*
-5.0000	-10.0000	0000	0000	0000

*Voltages shown are theoretical values for the transitions indicated. Ideally, in the continuous conversion mode, the output bits indicated as Ø will change from "1" to "0" or "0" to "1" as the input voltage passes through the level indicated.

Output coding is straight binary for unipolar and offset binary for bipolar.

CALIBRATION

UNIPOLAR CALIBRATION

Offset Adjust

Apply an input of + ½ LSB (+1.22 mV for the 10V range; +2.44 mV for the 20V range). Adjust the offset trimpot (R_1) until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Gain Adjust

Apply 1½ LSB's below the nominal full-scale (+9.9963V for the l0V range; +19.9927V for the 20V range). Adjust the gain trimpot (R_2) so that the output flickers between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR CALIBRATION

Offset Adjust

Apply ½ LSB above negative full-scale (−4.9988V for the ±5V range; −9.9976V for the ±10V range.) Adjust the offset trimpot (R_1) so that the output flickers between 0000 0000 0000 and 0000 0000 0001.

Gain Adjust

Apply 1½ LSB's below positive full scale (+4.9963V for the ±5V range; +9.9927V for the ±10V range). Adjust the gain trimpot (R_2) so that the output flickers between 1111 1111 1110 and 1111 1111 1111.

TIMING CONTROL

The variety of the ADC-574Z, -674Z's control modes (as shown in the "CONTROL INPUTS TRUTH TABLE") allow for simple interface in most system applications.

The output signal STS indicates the status of the device; high during a conversion, and low at the completion of a conversion. During a conversion (STS output high), the output buffers remain in the high impedance state and data cannot be read. A start convert during conversion will not reset the converter or reinitiate a conversion. However, if A_0, changes state after a conversion begins, an additional start convert pulse will latch the new state of A_0, causing a wrong cycle length for that conversion.

Control Inputs Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
0-1	0	0	X	0	Initiate 12-bit conversion
0-1	0	0	X	1	Initiate 8-bit conversion
1	1-0	0	X	0	Initiate 12-bit conversion
1	1-0	0	X	1	Initiate 8-bit conversion
1	0	1-0	X	0	Initiate 12-bit conversion
1	0	1-0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Initiate 12-bit conversion
1	0	1	0	0	Enable's 8 MSB's only
1	0	1	0	1	Enable's 4 LSB's plus 4 trailing zeroes

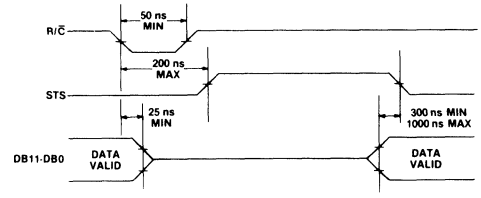
TIMING AND OPERATION

Stand-Alone Mode Timing

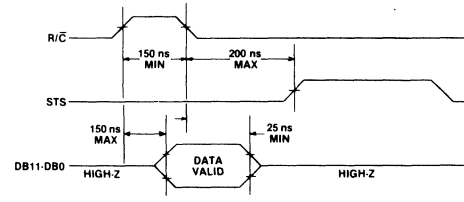
For stand-alone operation, all that is required is a single control line to R/$\overline{C}$. CE and 12/$\overline{8}$ are tied high, $\overline{CS}$ and A_0 are tied low, and the output appears in words of 12 bits.

The R/$\overline{C}$ signal may have any duty cycle within the limits shown in the diagrams below.

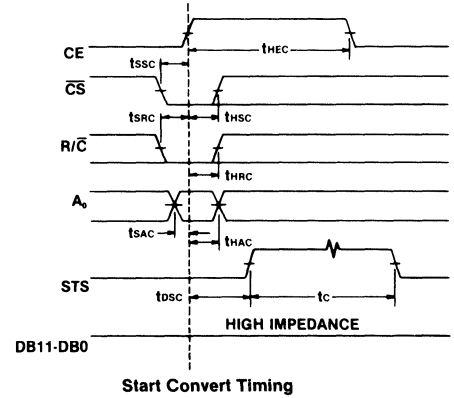
The data may be read when R/$\overline{C}$ is high unless STS is also high indicating a conversion is in progress.



Outputs Enabled After Conversion

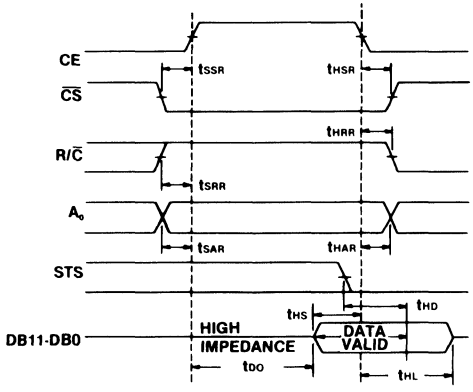


Outputs Enabled With R/$\overline{C}$ High



Start Convert Timing

A read operation in most applications begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. (See Technical Note 3.)



Read Cycle Timing

Read Mode

Symbol	Parameter	Min.	Typ.	Max.
t_{DD}	Access Time from CE	—	75 nS	150 nS
t_{HD}	Data Valid after CE Low	25 nS	35 nS	—
t_{HL}	Output Float Delay	—	100 nS	150 nS
t_{SSR}	$\overline{CS}$ to CE Setup	50 nS	0	—
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	—
t_{SAR}	A_0 to CE Setup	50 nS	25 nS	—
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0	0
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0	0
t_{HAR}	A_0 Valid after CE Low	50 nS	25 nS	—
t_{HS}	STS Delay after Data Valid	300 nS	500 nS	1000 nS

ADC-674Z Convert Mode

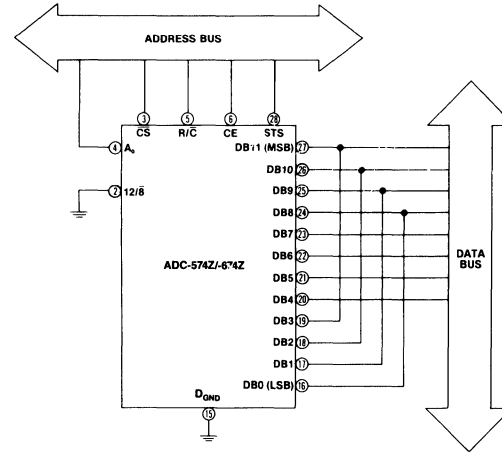
Symbol	Parameter	Min.	Typ.	Max.
t_{DSC}	STS Delay From CE	—	100 nS	200 nS
t_{HEC}	CE Pulse Width	50 nS	30 nS	—
t_{SSC}	$\overline{CS}$ to CE Setup	50 nS	20 nS	—
t_{HSC}	$\overline{CS}$ Low during CE High	50 nS	20 nS	—
t_{SRC}	R/$\overline{C}$ to CE Setup	50 nS	0	—
t_{HRC}	R/$\overline{C}$ Low during CE High	50 nS	20 nS	—
t_{SAC}	A_0 to CE Setup	0	0	0
t_{HAC}	A_0 Valid during CE High	50 nS	20 nS	—
t_C	Conversion Time, 12 bit cycle	15 µS	18 µS	25 µS
	8 bit cycle	10 µS	13 µS	17 µS

ADC-574Z Convert Mode

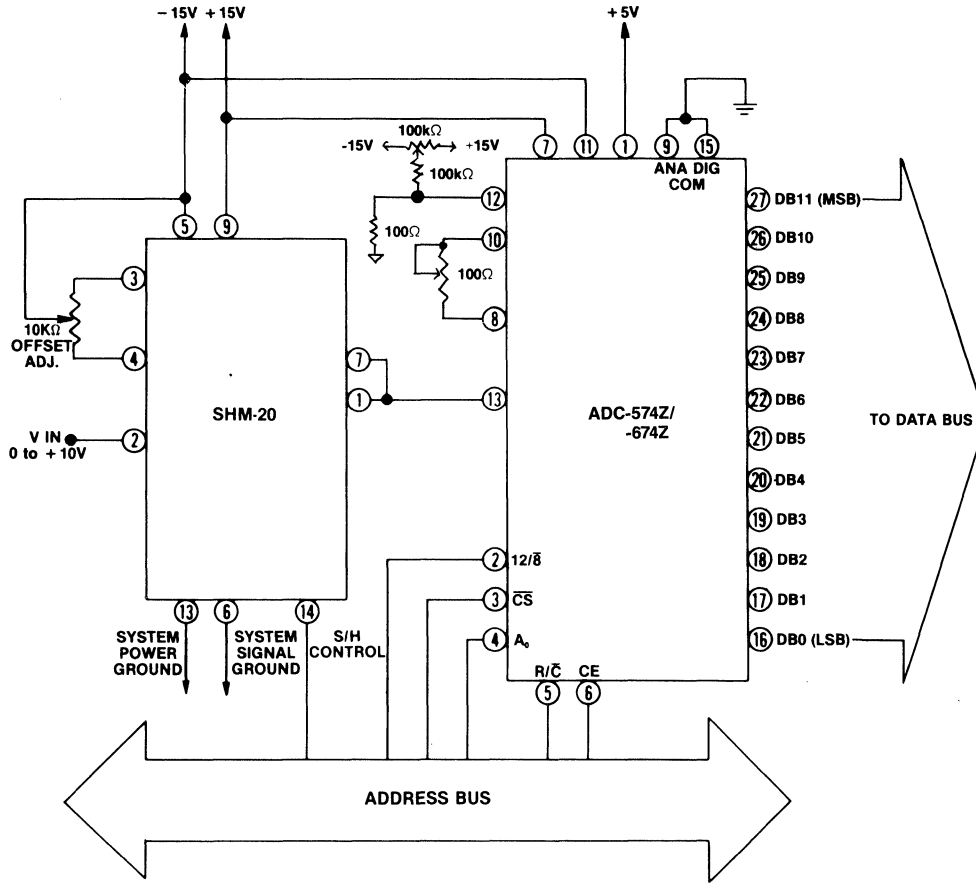
Symbol	Parameter	Min.	Typ.	Max.
t_{DSC}	STS Delay From CE	—	200 ms	200 nS
t_{HEC}	CE Pulse Width	—	—	—
t_{SSC}	$\overline{CS}$ to CE Setup	—	—	—
t_{HSC}	$\overline{CS}$ Low during CE High	—	—	—
t_{SRC}	R/$\overline{C}$ to CE Setup	—	—	—
t_{HRC}	R/$\overline{C}$ Low during CE High	—	—	—
t_{SAC}	A_0 to CE Setup	0	0	0
t_{HAC}	A_0 Valid during CE High	—	—	—
t_C	Conversion Time, 12 bit cycle	—	15 µS	25 µS
	8 bit cycle	—	10 µS	17 µS

Interface To An 8-Bit Data Bus

The 12/$\overline{8}$ input will be tied either high or low in most applications. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously for interface to a 12- or 16-bit data bus. A_0 is ignored. Taking 12/$\overline{8}$ low organizes the output in two 8-bit bytes, which are selected one at a time by A_0. This allows an 8-bit data bus to be connected as shown above. A_0 is normally tied to the LSB of the address bus for storing the converter's output in two consecutive memory locations. This two byte format is called "left justified data" for which a decimal point is assumed to the left of byte 1. In addition, A_0 may be toggled at any time without damage to the converter. Break-before-make switching is guaranteed between two data bytes, which assures that the outputs strapped together as shown are never enabled at the same time.



FAST A/D WITH SAMPLE HOLD



The above diagram shows the ADC-574Z, -674Z configured for unipolar (0 to + 10V) operation. Preceding the ADC-574Z, -674Z is DATEL's SHM-20, a 1 microsecond precision sample/hold. All sample/hold amplifiers are compatible with the ADC-574Z, -674Z; however, many will require an additional wide-band buffer amplifier to reduce their output impedance.

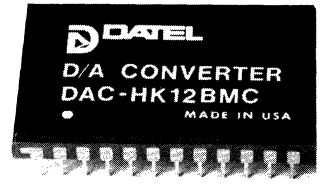
ORDERING INFORMATION

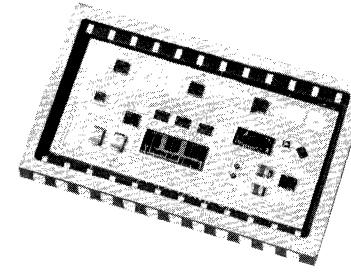
MODEL NO.	TEMPCO
ADC-574ZC	45 ppm/°C
ADC-574ZB	25 ppm/°C
ADC-574ZA	10 ppm/°C
ADC-674ZC	45 ppm/°C
ADC-674ZB	25 ppm/°C
ADC-674ZA	10 ppm/°C

ACCESSORIES

Part Number	Description
TP100 or TP100K	Trimming Potentiometers

DIGITAL-TO-ANALOG CONVERTERS



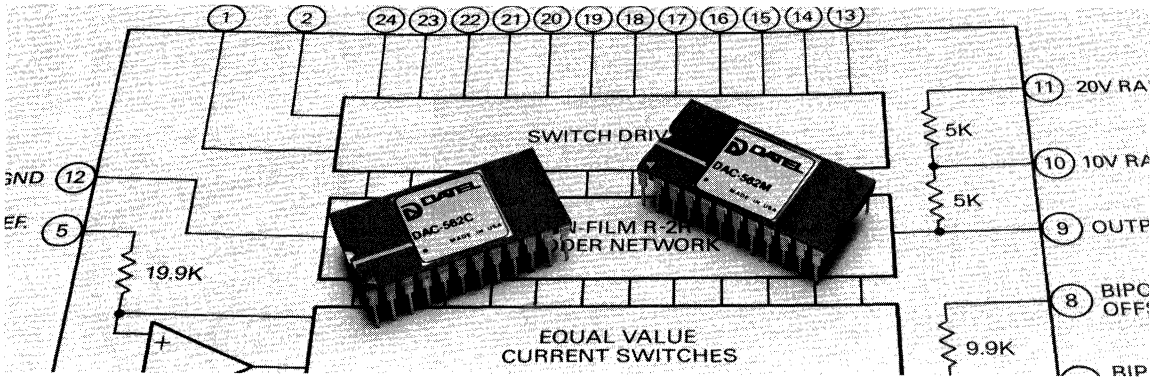


2

D/A CONVERTERS

MODEL	RESOLUTION	SETTLING TIME (MAX)	LINEARITY ERROR (MAX)	OUPUT RANGE	CODING	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
DAC-8303	8 Bits	7.5 ns	±1/2 LSB	0 to -1.054V	Bin	2 x 3 x 0.375 in. (50 x 75 x 10 mm) Module	0 to +70	2-35
DAC-0805	8 Bits	8 ns	±1/2 LSB	0 to -637.5 mV	C Bin	24-pin DIP Hybrid	-25 to +85	2-7
DAC-HF8BMC	8 Bits	25 ns	±1/2 LSB	0 to +5 mA ±2.5 mA	Bin	24-pin DIP Hybrid	0 to +70	2-39
DAC-HF8BMM							-55 to +125	
DAC-08BC	8 Bits	150 ns	±1/2 LSB	0 to -2 mA	Bin	16-pin DIP Monolithic	0 to +70	2-3
DAC-08BM							-55 to +125	
DAC-7523	8 Bits	200 ns	±1/2 LSB	±Vref / Rin	Bin	16-pin DIP Monolithic	0 to +70	2-31
DAC-IC8BC	8 Bits	300 ns	±1/2 LSB	0 to -2 mA	Bin	16-pin DIP Monolithic	0 to +70	2-59
							-55 to +125	
DAC-608C	8 Bits	1 µs	±1/2 LSB	$\frac{\text{Vref}}{15\text{k}\Omega}$ $\frac{\text{D}}{256}$	Bin	20-pin DIP Monolithic	0 to +70	2-19
DAC-UP8BC	8 Bits	2 µs	±1/2 LSB	0 to +10 V ±5 V	Bin	22-pin DIP Monolithic	0 to +70	2-68
DAC-UP8BM							-55 to +125	
DAC-330	10 Bits	4.7 ns	±1 LSB	0 to -1V	Bin	28-pin DIP Monolithic	-20 to +75	2-11
DAC-HF10BMC	10 Bits	25 ns	±1/2 LSB	0 to +5 mA ±2.5 mA	Bin	24-pin DIP Hybrid	0 to +70	2-39
DAC-HF10BMM							-55 to +125	
DAC-IC10B	10 Bits	250 ns	±1/2 LSB	0 to -4 mA	Bin	16-pin DIP Monolithic	0 to +70	2-55
DAC-IC10BC			±1 LSB				0 to +70	
DAC-IC10BM			±1/2 LSB				-55 to +125	
DAC-610C	10 Bits	500 ns	±1/2 LSB	$\frac{\text{Vref}}{15\text{k}\Omega}$ $\frac{\text{D}}{256}$	Bin	20-pin DIP Monolithic	0 to +70	2-19
DAC-7533	10 Bits	800 ns	±0.1%	±Vref / Rin	Bin	16-pin DIP Monolithic	0 to +70	2-31

DIGITAL-TO-ANALOG CONVERTERS



D/A CONVERTERS

MODEL	RESOLUTION	SETTLING TIME (MAX)	LINEARITY ERROR (MAX)	OUPUT RANGE	CODING	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
DAC-HF12BMC	12 Bits	50 ns	±1/2 LSB	0 to +5 mA	Bin	24-pin DIP Hybrid	0 to +70	2-39
DAC-HF12BMM				±2.5 mA			-55 to +125	
DAC-562C	12 Bits	400 ns	±1/2 LSB	0 to -2 mA	Bin	24-pin DIP Hybrid	0 to +70	2-15
DAC-562M			±1/4 LSB	±1 mA			-55 to +125	
DAC-DG12B1	12 Bits	50 ns	±1/2 LSB	0 to -10, ±5 V, ±10 V	C Bin	4 x 2 x 0.4 in. (102 x 51 x 10 mm)	0 to +70	-
DAC-DG12B2				±5 V, ±10 V	C2C			
DAC-612C	12 Bits	1 µs	±1/2 LSB	$\frac{Vref}{15k\Omega}$ $\frac{D}{4096}$	Bin	24-pin DIP Hybrid	0 to +70	2-19
DAC-7541	12 Bits	1 µs	±0.012%	±Vref / Rin	Bin	18-pin DIP Monolithic	0 to +70	2-31
DAC-7134BJ	12 Bits	3 µs	±1/2 LSB	±Vref/ Rin	2C	28-pin DIP Monolithic	0 to +70	2-25
DAC-7134UJ				Vref / Rin	Bin			
DAC-HK12BGC	12 Bits	3 µs	±1/2 LSB	0 to +5 V, +10 V	Bin	24-pin DIP Hybrid	0 to +70	2-43
DAC-HK12BMC				±2.5 V, ±5 V, ±10 V			0 to +70	
DAC-HK12BMM							-55 to +125	
DAC-HK12BGC-2	12 Bits	3 µs	±1/2 LSB	0 to ±5 V, ±10 V	Bin	24-pin DIP Hybrid	0 to +70	2-43
DAC-HK12BMC-2				±2.5 V, ±5 V, ±10 V			0 to +70	
DAC-HK12BMM-2							-55 to +125	
DAC-HZ12BGC	12 Bits	3 µs	±1/2 LSB	0 to ±5 V, ±10 V	C Bin	24-pin DIP Hybrid	0 to +70	2-51
DAC-HZ12BMC				±2.5 V, ±5 V, ±10 V			0 to +70	
DAC-HZ12BMM							-55 to +125	
DAC-HZ12DGC	3 Digits	3 µs	±1/4 LSB	0 to 2.5 V	C BCD	24-pin DIP Hybrid	0 to +70	2-51
DAC-HZ12DMC				0 to +5 V			0 to +70	
DAC-HZ12DMM				0 to +10 V			-55 to +125	
DAC-7134BK	13 Bits	3 µs	±1/2 LSB	±Vref / Rin	2C	28-pin DIP Hybrid	0 to +70	2-25
DAC-7134UK				Vref / Rin	Bin			
DAC-7134BL	14 Bits	3 µs	±1/2 LSB	±Vref / Rin	2C	28-pin DIP Hybrid	0 to +70	2-25
DAC-7134UL				Vref / Rin	Bin			
DAC-HP16BGC	16 Bits	15 µs	0.003%	0 to ±10 V	C Bin	24-pin DIP Hybrid	0 to +70	2-47
DAC-HP16BMC				0 to ±5 V			0 to +70	
DAC-HP16BMM							-55 to +125	

DAC-08B
High Speed, 8-Bit Monolithic Digital-to-Analog Converter

FEATURES

- **85 Nanoseconds settling time**
- **−10 to +18V compliance**
- **±4.5 to ±18V supply**
- **8-Bit resolution**
- **1- or 2-Quadrant multiplication**
- **Low cost**

GENERAL DESCRIPTION

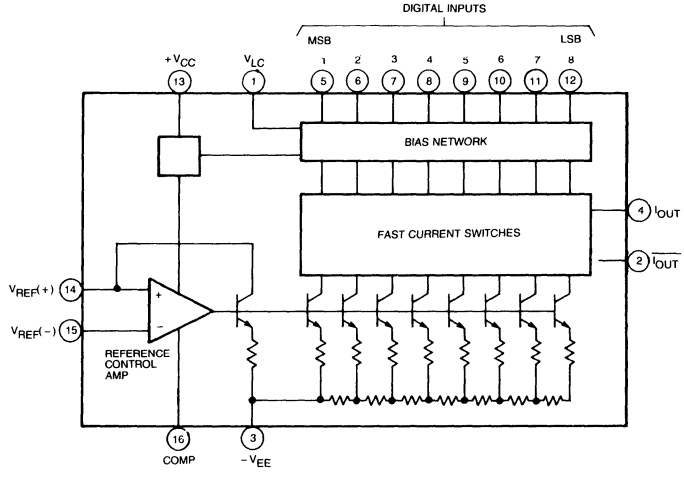
The DAC-08BC and DAC-08BM provide very high speed performance coupled with low cost and application flexibility. These units have guaranteed full 8-bit monotonicity with nonlinearity of 0.19% over the full operating temperature range. High-speed current steering switches achieve 85 nanoseconds settling time with a very low glitch for full-scale changes. A large output voltage compliance range (−10 to +18V) allows direct current to voltage conversion with just an output resistor, omitting the need for an operational amplifier in many cases.

The DAC-08 consists of 8 fast-switching current sources, a diffused R-2R resistor ladder, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking, resulting in a gain temperature coefficient of 10 ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling and low cost. Linearity is ±½ LSB.

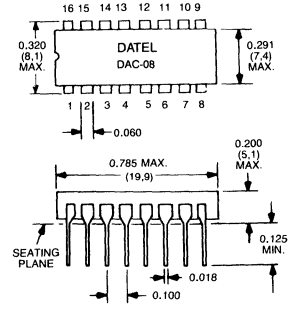
An external reference current of 2 mA nominal programs the scale factor of the DAC. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar dependent upon the connection of the two complementary output sink currents.

DAC-08 applications include fast A/D converters, waveform generators, audio encoder and attenuators, CRT display drivers, and high-speed modems.

Power supply requirements are ±4.5V to ±18V. Operating temperature range is 0°C to 70°C for the DAC-08BC and −55°C to +125°C for the DAC-08BM. These models have equivalent specifications and pinouts to industry standard DAC-08's.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	THRESHOLD CONTROL (VLC)
2	$\overline{I_{OUT}}$
3	V_{EE}
4	I_{OUT}
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (MSB)
13	V_{CC}
14	$V_{REF}+$
15	$V_{REF}-$
16	COMPENSTION

ABSOLUTE MAXIMUM RATINGS	
V_{CC} Supply to V_{EE} Supply	36V
Digital Input Voltage	$-V_{EE}$ to $-V_{EE}$ plus 36V
V_{LC}	$-V_{EE}$ to $+V_{CC}$
Reference Input Voltage	$-V_{EE}$ to $+V_{CC}$
Reference Input Current	5.0 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, V_S = ±15V, I_{REF} = 2.0 mA unless otherwise noted.

INPUTS	
Resolution	8 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Logic Level, Bit ON ("1")	+2.0V minimum at +10.0 μA
Input Logic Level, Bit OFF("0")	+0.8V maximum at −10.0 μA[1]
Nominal Reference Current	2.0 mA
Reference Bias Current	−1.0 μA
Reference Input Slew Rate	8 mA/μsec.
OUTPUTS	
Output Current, I_{REF} = 2.0 mA	1.99 mA ±0.05 mA[2]
Output Current Range, V_{EE} = −5V	0 to 2.1 mA
Output Current Range, V_{EE} = −7 to −18V	0 to 4.2 mA
Output Current, all bits OFF	±0.2 μA typical ±2.0 μA maximum
Full-Scale Symmetry	±1.0 μA typical ±8.0 μA maximum
Output Voltage Compliance	−10 to +18V
PERFORMANCE	
Relative Accuracy	±½ LSB (±0.19%) maximum
Nonlinearity	±½ LSB (±0.19%) maximum
Differential Nonlinearity	±½ LSB (±0.19%)
Full-Scale Tempco	±10 ppm/°C typical ±50 ppm/°C maximum
Settling Time, 2 mA to ½ LSB	85 nsec. typical 150 nsec. maximum
Propagation Delay	60 nsec. maximum
Power Supply Sensitivity, I_{REF} = 1 mA	±0.002%/%
POWER REQUIREMENTS	
V_{CC}	+4.5V to +18V
V_{EE}	−4.5V to −18V
Power Supply Current, I_{REF} = 1.0 mA V = ±5V	+3.8, −5.8 mA maximum
Power Supply Current, I_{REF} = 2.0 mA V = +5V, −15V	+3.8, −7.8 mA maximum
V = ±15V	+3.8, −7.8 mA maximum
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
DAC-08BC	0°C to +70°C
DAC-08BM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package	16 Pin Dip

FOOTNOTES

1. For TTL, DTL Interface, V_{LC} = 0V. For other digital interfaces see TECHNICAL NOTE 3.
2. I_{OUT} (Pin 4) + I_{OUT} (Pin 2) = Output Current

TECHNICAL NOTES

1. The DAC-08 series is a multiplying D/A converter in which the output current is a product of the digital word and the input reference current. Excellent performance is obtained for I_{REF} from 4.0 mA to 4.0 μA. Monotonic operation is maintained from 4.0 mA to 100 μA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \quad (I_{REF} \text{ is current at Pin 14})$$

2. **Reference Amplifier Set-up.** If a regulated power supply is used as the reference, a resistor divider should be used with the junction by-passed to ground with a 0.1 μf capacitor. TTL logic supplies are not recommended to be used as the reference. AC and dc reference applications will require the reference amplifier to be compensated using a capacitor (C_C) from pin 16 to V_{EE}. For fixed reference application (dc), a 0.01 μF capacitor is recommended. For AC reference applications, the value of C_C depends on the impedance present at pin 14. For R_{REF} values of 1.0, 2.5 and 5.0 KΩ, minimum values of C_C are 15, 37 and 75 pf respectively. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin. See Graph on Reference Input Frequency Response. Low R_{REF} values enable small C_C achieving highest throughput on V_{REF}. If pin 14 is driven by a high impedance such as a transistor current source, the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{REF} = 1.0 KΩ and C_C = 15 pf, the reference amplifier slews at 4.0 mA/microsecond, enabling a transition from I_{REF} = 0 to I_{REF} = 2.0 mA in 500 nanoseconds.
3. **Interfacing Various Logic Families.** The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. A large input swing capability allows adjustable logic threshold voltage and 200 μA maximum source current on pin 1. Mimimum input logic swing and minimum logic threshold voltage is given by V_{EE} + (I_{REF} x 1.0 KΩ) + 2.5V. Logic threshold is adjusted by appropriate voltage at V_{LC}. The Interfacing Various Logic Families Diagram shows appropriate connections. Fastest settling times are obtained when V_{LC} sees a low impedance. Use 0.01 μF by-pass capacitors whenever possible.
4. **Analog Output Currents.** Both true and complemented output sink currents are provided, $I_O + \overline{I_O} = I_{FS}$. Both outputs can be used simultaneously. If one of the outputs is not required, it must be connected to ground or a point capable of sourcing I_{FS}. **Do not leave unused output pin (I_O or $\overline{I_O}$) open.** The compliance voltage is the voltage swing on output pin without affecting DAC accuracy. Positive compliance is 36V above V_{EE} and is independent of V+. Negative compliance is V_{EE} + (I_{REF} x 1 KΩ) +2.5V.
5. **Settling Time.** The DAC-08 is capable of extremely fast settling times, typically 85 nanoseconds at I_{REF} = 2.0 mA. Judicious circuit design and careful board layout must be employed to obtain full performance. The output capacitance of the DAC including the package is approximately 15 pf, therefore the output RC time constant dominates at $R_L > 500\ \Omega$.

   Settling time remains essentially constant for I_{REF} values down to 1.0 mA, with gradual increases for lower I_{REF} values. The switching transients (glitches) are very low and may be further reduced by small capacitive loads at the output. Settling time will be increased slightly.

TECHNICAL NOTES (Cont'd)

6. **Power Supplies.** The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1$ mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. For example, operation at −4.5V with I_{REF} = 2 mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network. It is recommended that V_{CC} and V_{EE} always be bypassed to ground with at least 0.1 μf capacitors.

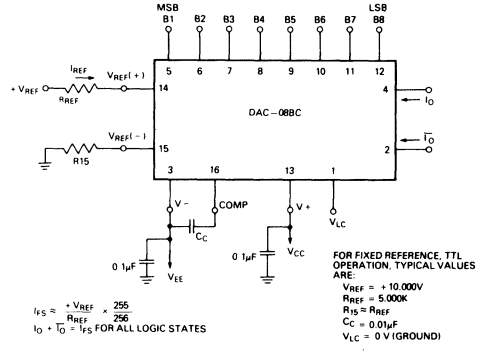
   Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible, as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc. remain between acceptable limits.

   Power consumption may be calculated as follows:
   $P_d = (I+)(V+) + (I-)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

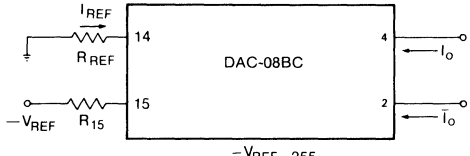
7. **Temperature Performance.** For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. Full scale trimming may be accomplished by adjusting I_{REF} (changing value of R_{REF}). R_{REF} and R_L should be selected for similar temperature coefficient to minimize accuracy error. Setting time of the DAC decreases approximately 10% at −55°C and increases 15% at +125°C.

APPLICATION DIAGRAMS

BASIC POSITIVE REFERENCE OPERATION



BASIC NEGATIVE REFERENCE OPERATION

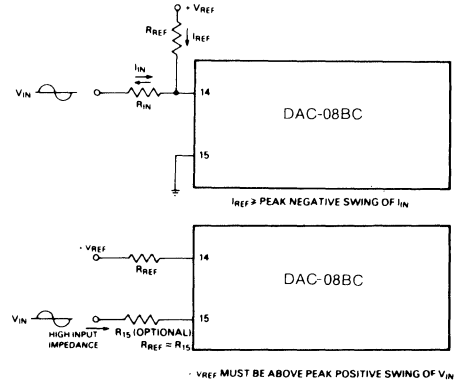


$$I_{FS} \approx \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

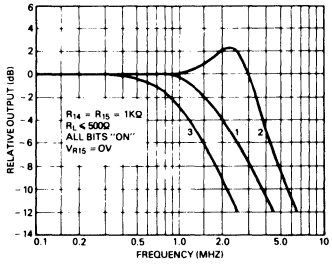
$(R_{15} \approx R_{REF})$

APPLICATION DIAGRAMS (Cont'd)

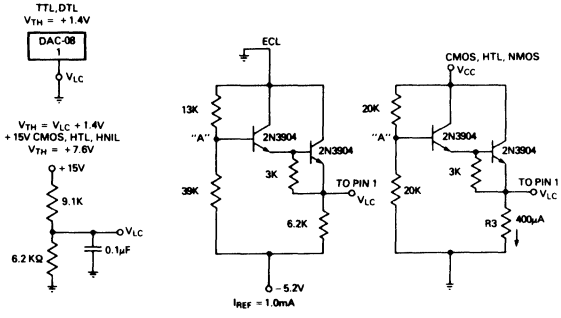
ACCOMMODATING BIPOLAR REFERENCES



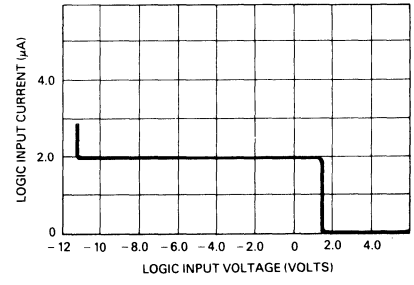
REFERENCE INPUT FREQUENCY RESPONSE



INTERFACING VARIOUS LOGIC FAMILIES

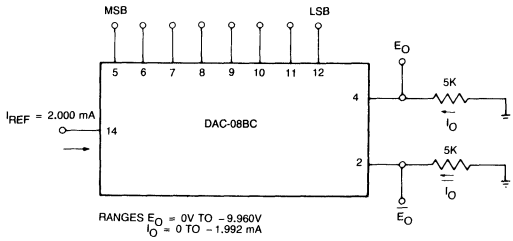


LOGIC INPUT CURRENT VS. INPUT VOLTAGE



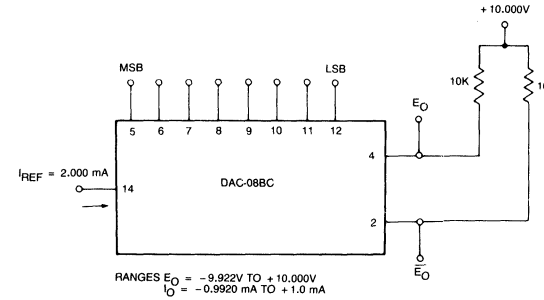
APPLICATION DIAGRAMS (Cont'd)

BASIC UNIPOLAR NEGATIVE OPERATION



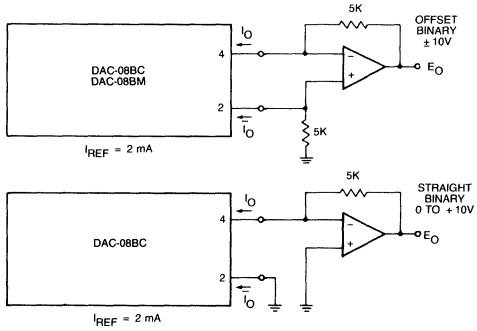
SEE CODING TABLE

BASIC BIPOLAR OUTPUT OPERATION

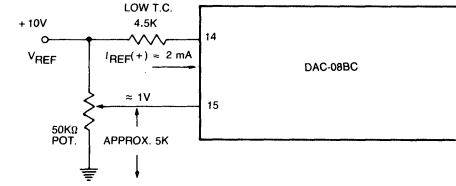


SEE CODING TABLE

VOLTAGE OUTPUT OPERATION



RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT



CALIBRATION AND CODING TABLES

CALIBRATION PROCEDURE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. **Zero and Offset Adjustments**
   For unipolar operation, set all digital inputs to "0" and adjust the output amplifier zero adjustment for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust the offset adjustment for the negative full-scale voltage shown in the Coding Table.
3. **Gain Adjustment**
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust the gain adjustment for the positive full-scale voltage shown in the DAC-08B Coding Table.

UNIPOLAR OPERATION—STRAIGHT BINARY CODING
For 5k load resistors at pins 2 and 4

INPUT CODE	E_O	$\overline{E}_O$	I_O	$\overline{I}_O$
1111 1111	−9.961	0.000	1.992	0.000
1110 0000	−8.750	−1.211	1.750	0.242
1100 0000	−7.500	−2.461	1.500	0.492
1000 0000	−5.000	−4.961	1.000	0.992
0100 0000	−2.500	−7.461	0.500	1.492
0000 0001	−0.039	−9.922	0.008	1.984
0000 0000	0.000	−9.961	0.000	1.992

BIPOLAR OPERATION—OFFSET BINARY CODING
For 10k load resistors from pins 2 and 4 to +10V.

INPUT CODE	E_O	$\overline{E}_O$
1111 1111	− 9.922	+10.000
1110 0000	− 7.500	+ 7.578
1100 0000	− 5.000	+ 5.078
1000 0000	0.000	+ 0.078
0100 0000	+ 5.000	− 4.922
0000 0001	+ 9.922	− 9.844
0000 0000	+10.000	− 9.922

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	PACKAGE
DAC-08BC	0°C to +70°C	Plastic
DAC-08BM	−55°C to +125°C	Ceramic

DAC-0805
Ultra-Fast, Low-Glitch Composite Video D/A

FEATURES

- **Composite Video Output**
- **8-Bit resolution**
- **8 Nanoseconds maximum settling time**
- **Single supply operation**
- **Industry-standard pin-out**

GENERAL DESCRIPTION

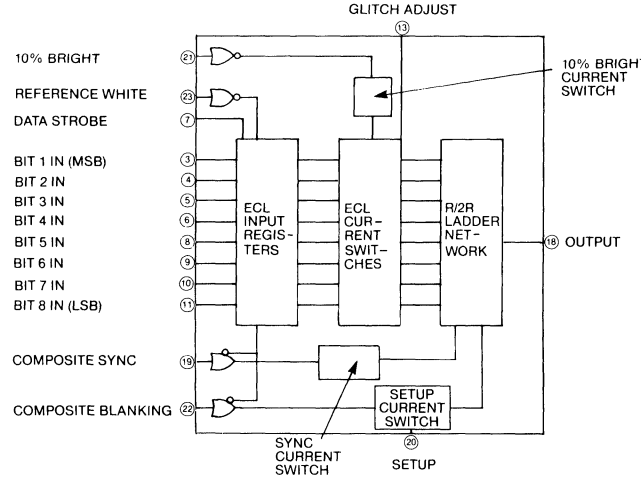
DATEL's DAC-0805 is a high performance, ultra-fast, hybrid digital-to-analog converter specifically designed for video and graphic display applications. This converter has the self-contained digital sync, blanking, 10% bright, and reference white control inputs required for compatibility with EIA standards RS-170 and RS-343A.

The DAC-0805 provides 8 bits of resolution, or 256 levels of gray scale, and settles in a maximum of only 8 nanoseconds.

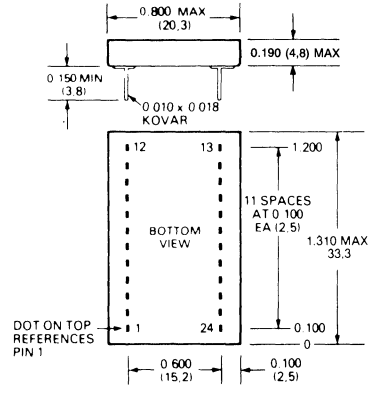
The DAC-0805 uses high speed ECL input registers and current switches to minimize time skew and glitch amplitude. Glitch energy, typically 50 pV-S, may be optimized for individual system performance with the glitch adjust input.

Other important features include an output impedance of 75Ω, full-scale output current of −17 mA, ±½ LSB linearity and guaranteed monotonic performance.

Model DAC-0805 is cased in a 24-pin ceramic package and operates over the industrial, −25°C to +85°C temperature range. Power requirement is −5.2V. The ultra-high speed, low cost, small size and circuit completeness of these converters make them an excellent choice for applications including high resolution raster scan graphics displays (both color and monochrome) TV video reconstruction, and function generation.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN FUNCTION	PIN FUNCTION
1 Ground	13 Glitch Adjust
2 −5.2V Supply	14 Ground
3 Bit 1 (MSB)	15 Ground
4 Bit 2	16 Ground
5 Bit 3	17 Ground
6 Bit 4	18 Analog Output
7 Data Strobe	19 Composite Sync
8 Bit 5	20 Setup
9 Bit 6	21 10% Bright
10 Bit 7	22 Composite Blanking
11 Bit 8 (LSB)	23 Reference White
12 Ground	24 −5.2V Supply

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, −5.2V dc supply, unless otherwise noted.

DIGITAL INPUTS	DAC-0805
Resolution	8 bits
LSB Weight, Voltage	2.5 mV
Current	6.7 μA
Coding	Complementary Binary
Logic Compatibility	ECL
Input Logic Level, Bit ON, "0"	−1.7V
Input Logic Level, Bit OFF, "1"	−0.9V
Logic Loading[1]	5 pF and 50 kΩ to −5.2V
Data Strobe Input: Set Up Time, min.	2.5 nsec.
Hold Time, min.	1.5 nsec.
Propagation Delay	3 nsec.
Logic Loading	50 pF and 5 kΩ to −5.2V
SETUP CONTROL[2] **(Pin 20)**	
Setup Grounded	0 mV (0 IRE Units)
Setup Open	71 mV (10 IRE Units)
Setup at −5.2V	142 mV (20 IRE Units)
OUTPUTS	
Output Current	0 to −17 mA
Output Voltage, 75Ω Load[3]	0 to −600 mV 0 to −630 mV 0 to −637.5 mV
Compliance Voltage	±1.1V
Output, 10% Bright (Pin 21) = Logic "0"	
Current	−1.9 mA ±5%
Voltage	−71 mV ±5%
Output, Composite Sync (Pin 19) = Logic "0"	
Current	−7.6 mA ±5%
Voltage	−286 mV ±5%
Output, Composite Blanking (Pin 22) = Logic "0"	
Current[4] **(±1%)**	−17 mA, −18.9 mA or −20.8 mA
Voltage[4] **(±1%)**	−637.5 mV, −708.75 mV or −780 mV
PERFORMANCE	
Absolute Accuracy[5]	±½ LSB
Integral Linearity Error	±½ LSB
Integral Linearity Tempco	16 ppm of FSR/°C
Monotonicity	Guaranteed
Zero Offset Error	0.9 mV
Zero Offset Tempco	6 ppm of FSR/°C
Gain Tempco	17 ppm/°C
Voltage Output Settling Time, max.	8 nsec. to 0.4% GS
Output Slew Rate	200 V/μsec.
Output Rise Time	3 nsec.
Update Rate[6]	100 MHz
Glitch Energy[7]	50 pV − S
Digital Input Settling Time[8]	8 nsec.
POWER REQUIREMENTS	
Power Supply Voltage	−5.2V
Power Supply Range	−4.75V to −5.45V
Quiescent Current	320 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−55°C to +125°C
Package Type	24-Pin Ceramic DIP
Pins	0.010 x 0.018 inch Kovar

FOOTNOTES:

1. Except Data Strobe input (Pin 7).
2. Setup refers to the difference between the reference black level and the blanking level.
3. The difference between the full-scale output of 637.5 mV and 643 mV shown elsewhere in this data sheet is because an LSB value of 2.5 mV was chosen for ease of calibration. This difference is well within the tolerance allowed by RS-170.
4. The three currents and voltages correspond to setup levels of 0, 10 and 20 IRE units.
5. Absolute accuracy error is relative to gray scale and includes linearity.
6. These converters may be updated to a maximum of 125 MHz with some degradation of settling time.
7. Reducible to less than 25 pV − S with glitch adjustment.
8. Settling time to 10% of final value. Specified for sync, blanking, reference white, reference black and 10% bright inputs.

TECHNICAL NOTES

1. The use of a good ground plane around the device must be used. A double sided copper board with ground plane on one side and conductors on the other side is recommended. All ground pins should be soldered to the ground plane as close as possible to where they leave the package.
2. Standard 24-pin sockets are not recommended for use with the DAC-0805 series. If sockets must be used, use only spring-loaded pin sockets for each pin. Insert through plated holes on the printed circuit board and solder them to pads on the conductor side.
3. The power supply should be bypassed with a 1 μF or larger tantalum capacitor and a 0.1 μF high frequency ceramic capacitor as close as possible to the power pin (within ½ inch).
4. A well regulated and ripple free, −5.2V power supply must be used for maximum accuracy. The output of these devices will change 1 mV for every 1 mV of power supply change. Therefore, it is important that the supply ripple be less than ½ LSB or less than 1 mV for the DAC-0805. The use of a stable power supply will also enhance the accuracy of the devices over the effects of time and temperature.
5. The minimum set-up time for these D/A's is specified at 2.5 nanoseconds; this is the time the data must remain on the inputs before the strobe is applied. A minimum strobe hold time of 1.5 nanoseconds must be allowed to ensure that the data is latched.
6. The DAC-0805 has extremely low glitch energy levels and normally needs no adjustment. However, if glitch adjustment is required, an external 200Ω trimpot should be connected to the GLITCH ADJUST (pin 13) as close to the pin as possible, and adjusted for equal positive and negative peak glitch signal levels. (See typical connections.)

GLOSSARY OF VIDEO TERMS

COMPOSITE VIDEO SIGNAL
The combined video signal, with or without Setup, plus the Sync signal.

VIDEO SIGNAL
The visually perceived portion of the composite video signal which varies in gray scale levels from Reference White to Reference Black. Also known as the picture signal.

GLOSSARY OF VIDEO TERMS (Con't)

SYNC OR COMPOSITE SYNC SIGNAL
That portion of the composite video signal which synchronizes the scanning process.

SYNC LEVEL
The peak level of the composite Sync signal.

SETUP
The difference between the Reference Black level and the Blanking level. Not to be confused with setup as used in conjunction with digital logic.

RASTER-SCAN
The basic method of sweeping across a CRT, a line at a time, to generate and display pictures as commonly used in commercial TV in the USA.

MONOCHROME VIDEO
Conventional black-and-white television video in which the Z-axis, or intensity, of the beam is modified during scanning to shade and/or outline images.

BLANKING LEVEL
The level which separates the Sync portion from the video signal, with or without Setup. This level is sometimes also called the pedestal, back porch or front porch. It usually refers to the level which will cut off the CRT, producing the blackest possible picture.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

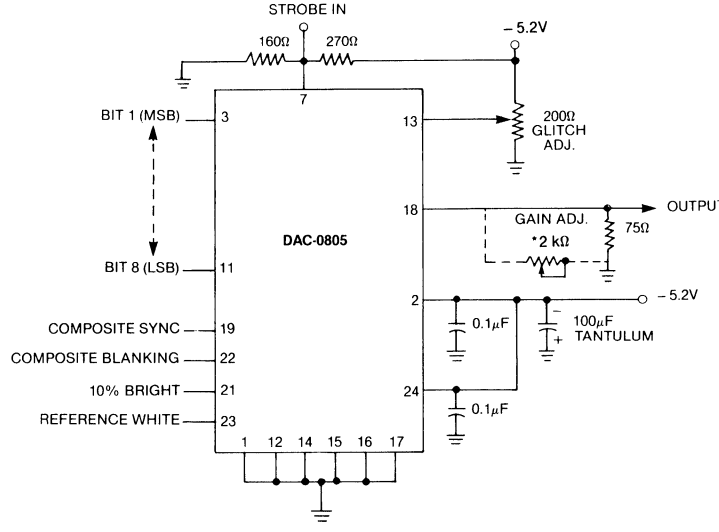
10% BRIGHT LEVEL
A "Whiter than White" Level not within the range of the normal picture. Sometimes used for generating cursors or outlines because it contrasts with all gray shades including white.

GRAY SCALE
The discrete levels of the video signal between Reference White and Reference Black levels.

COLOR VIDEO (RGB)
As used herein, this refers to the method of generating color images by combining the three primary colors of red-green-blue (RGB). The associated monitor would be identified as an "RGB" monitor. Three DAC-0805 series D/A converters are required to drive such a monitor, one each for red, green and blue.

CONNECTIONS AND PERFORMANCE

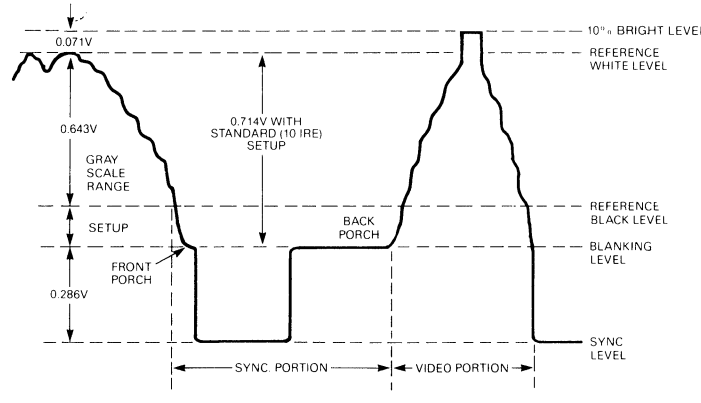
TYPICAL CONNECTIONS



*OPTIONAL

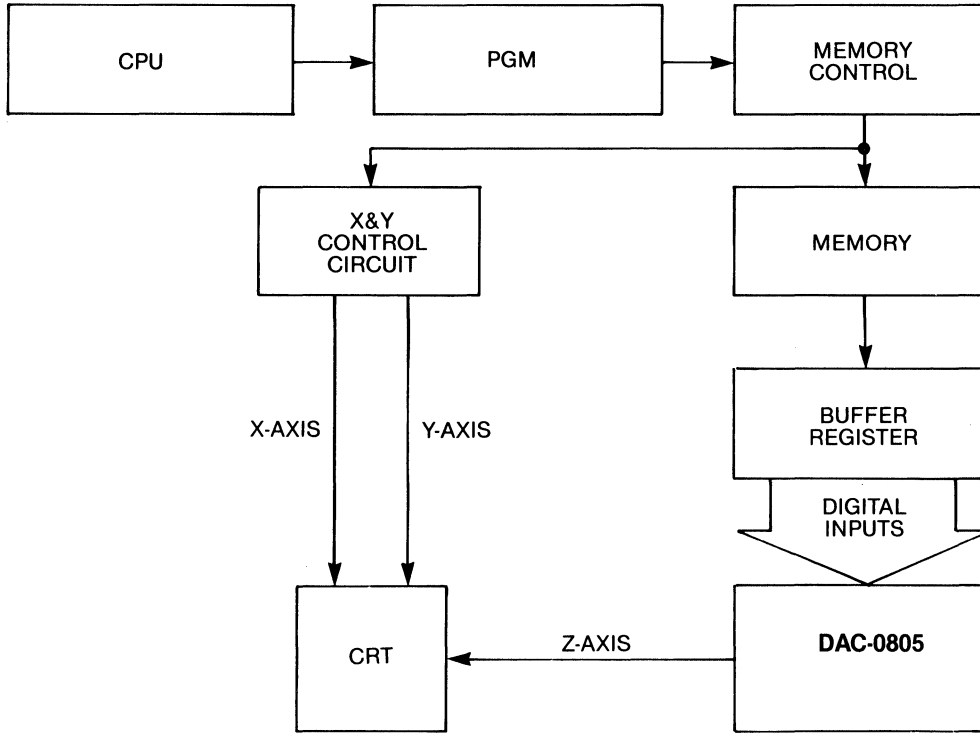
NOTE: All digital inputs terminated to – 5.2V through 2 kΩ except strobe.

COMPOSITE VIDEO OUTPUT SIGNAL



APPLICATION

TYPICAL RASTER SCAN DISPLAY SYSTEM



The DAC-0805 is particularly useful in raster scan display systems. The above system functions as an intelligent peripheral to the host CPU, and drives a standard television monitor.

The system consists of a MOS RAM memory buffer for storing display data, a memory controller for updating the CRT display, and a programmable microprocessor for graphics generation and image manipulation.

DIGITAL CONTROL INPUTS

STROBE-(Pin 7)
Logic "0" to Logic "1" transition transfers digital input data to the register.

SETUP-(Pin 20)
Three user programmable levels:

INPUT	BLANKING LEVEL (from Reference Black)	IRE Units
1. Grounded	0 mV	0
2. Open	−71 mV	10
3. −5.2V	−142 mV	20

10% BRIGHT-(Pin 21)
Logic "0" causes output to go positive by 71 mV. The most positive voltage remains 0V absolute. All other levels are shifted down by 71 mV.

REFERENCE WHITE-(Pin 23)
Logic "0" set the D/A's output to Full-Scale (Reference White Level). This is 0V absolute or 714 mV more positive than the Blanking Level (643 mV more positive than the Reference Black Level) with Standard Setup.
NOTE: This pin should be held at a logic "1" when the Composite Blanking input is activated.

COMPOSITE SYNC-(Pin 19)
Logic "0" resets the input register to all "0's" and the output voltage goes negative by 286 mV with respect to the Composite Blanking Level.

COMPOSITE BLANKING-(Pin 22)
Logic "0" resets the input register to all "0's" and sets the output voltage negative by the amount of setup voltage with respect to the Reference Black Level.

ORDERING INFORMATION

MODEL	RESOLUTION	SETTLING TIME
DAC-0805MR	8 Bits	8 nsec.

For military devices compliant to MIL-STD-883, consult the factory.

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DAC-330
10-Bit, Multiplying D/A Converter

FEATURES

- **10-Bit resolution**
- **160 MHz conversion rate**
- **Multiplying — 14 MHz bandwidth**
- **ECL compatible**
- **Single (−5V) supply**
- **Low-power**
- **Low-glitch**

APPLICATIONS

- **Graphic displays**
- **High definition video displays**
- **Ultra high-speed signal processing**
- **Digital VTR**
- **Digital attenuators**
- **High-speed function generators**

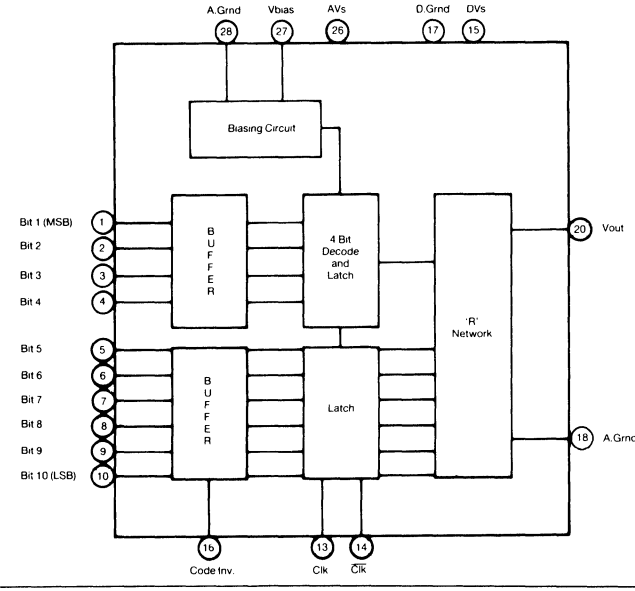
GENERAL DESCRIPTION

The monolithic DAC-330 is an ultra high-speed, 10-bit digital-to-analog converter. This ECL-compatible device has a 160 MHz update rate and a 14 MHz multiplying bandwidth capability.

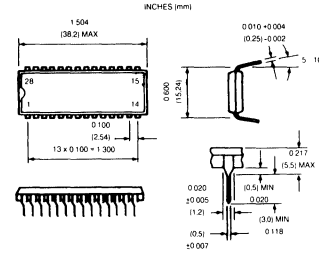
The DAC-330 develops an output voltage of 0 to −1.0V and can directly drive a 75Ω impedance load. Settling time is 5.2 nSec. while glitch energy is a low 15 picovolt/second. Other features of this D/A are integral linearity of 0.1% FS, and a differential linearity of ±1/2 LSB maximum.

Input coding of the DAC-330 can be programmed for straight binary or complementary binary through use of the COMP BIN control input line.

The DAC-330 is a low-power device requiring only a single −5.2V supply with a maximum current draw of 100 mA. The DAC-330 is packaged in a 28-pin plastic DIP and has an operating temperature range of −20°C to +75°C.



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	ANALOG GROUND
2	BIT 2	27	VBIAS
3	BIT 3	26	ANALOG SUPPLY (−5.0V)
4	BIT 4	25	N/C
5	BIT 5	24	N/C
6	BIT 6	23	N/C
7	BIT 7	22	N/C
8	BIT 8	21	N/C
9	BIT 6	20	ANALOG OUTPUT
10	BIT 10 (LSB)	19	N/C
11	N/C	18	ANALOG GROUND (R−2R)
12	N/C	17	DIGITAL GROUND
13	CLOCK INPUT (CLK)	16	CODE INVERSE INPUT
14	CLOCK INPUT (C̄L̄K̄)	15	DIGITAL SUPPLY (−5.0V)

ABSOLUTE MAXIMUM RATINGS (1) (T_A = +25°C unless otherwise specified.)	
Power Supply Voltage, (Vs), (pins 15 + 26)	−7.0V dc
Digital Input Voltages	−Vs to +0.3V dc
Analog Output Current	20 mA
Operating Temperature Range	−20°C to +75°C
Storage Temperature Range	−65°C to +150°C
Reference Input Voltage	Vs to +0.3V
Allowable Power Dissipation	1.43 W

FUNCTIONAL SPECIFICATIONS
Typical at +25°C, ANA Vs = −5.2V dc, DIG Vs = −5.2V dc unless otherwise noted.

DIGITAL INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	10	—	—	bits
Coding (using Pin 16)				
Comp Bin = 0V		Straight Binary		
Comp Bin = −5.2V		Complementary Binary		
Data and Clock Inputs				
Logic "1" voltage	−0.74	−0.89	−1.04	V dc
Logic "0" voltage	−1.60	−1.75	−1.90	V dc
4 MSB's Data				
Logic "1" current	0.1	1.5	6.0	μA
Logic "0" current	0.1	1.5	6.0	μA
6 LSB's Data				
Logic "1" current	0.1	0.75	3.0	μA
Logic "0" current	0.1	0.75	3.0	μA
Clock				
Logic "1"current	2.0	23	70	μA
Comp Bin				
Logic "1" current	0.1	1.5	6.0	μA
Data				
Set Up Time (Tsu)	—	—	5.0	nSec.
Hold Time (Thd)	—	—	1.0	nSec.
REFERENCE				
Reference Input Voltage	−3.8	−4.2	−4.7	V dc
Reference Input Current	−0.1	−0.4	−3.0	μA
ANALOG OUTPUTS				
Output Resistance	.52	65	78	Ω
Output Voltage F.S.				
R ≥ 10K	−0.8	−1.0	−1.6	V dc
R = 75	−0.8	−1.0	−1.2	VDC
PERFORMANCE				
Conversion Rate (2)	160	—	—	MHz
Linearity Error	—	—	±0.1	% FS
Differential Linearity	—	—	±1/2	LSB
Gain Tempco				
R ≥ 10 kΩ	—	−140	−280	ppm/°C
R = 75Ω	—	−580	−1200	ppm/°C
Zero Offset	—	−7	−21	mV
Zero Offset Tempco (3)	6	16	22	μV/°C
Propagation Delay (Tpd) (2)	—	3.8	—	nSec.
Settling Time (Tset)	—	4.7	—	nSec.
Rise Time (Tr) (2)	—	1.5	—	nSec.
Fall Time (Tf) (2)	—	1.5	—	nSec.
Glitch Energy	—	15	—	pV/Sec.
Multiplying Bandwidth −3 dB, (2)	10	14	—	MHz
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range	−4.75	−5.2	−5.45	V
Supply Current	−65	−85	−100	mA
PHYSICAL-ENVIRONMENTAL				
Operating Temp Range	−20°C to +75°C (ambient)			
Storage Temperature Range	−55°C to +150°C			
Package Type	28-pin plastic DIP			

(1)Absolute maximum ratings are limiting values, which when exceeded will yield derated performance of the device and may cause damage to the device.
(2)R = 75 Ω, −3 dB
(3)R ≥ 10 KΩ

TABLE 1. INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	ANA GND
2	BIT 2	27	V REF
3	BIT 3	26	ANA VS (−5.2V)
4	BIT 4	25	N/C
5	BIT 5	24	N/C
6	BIT 6	23	N/C
7	BIT 7	22	N/C
8	BIT 8	21	N/C
9	BIT 9	20	ANA OUT
10	BIT 10 (LSB)	19	N/C
11	N/C	18	ANA GND
12	N/C	17	DIG GND
13	$\overline{CLK}$	16	COMP. BIN.
14	CLK	15	DIG VS (−5.2V)

TABLE 2. INPUT/OUTPUT CODING

RANGE	DIGITAL INPUT CODE	ANALOG OUTPUT VOLTAGE Comp. Bin = 0V (Pin 16 to DIG GND) STRAIGHT BINARY		ANALOG OUTPUT VOLTAGE Comp. Bin. = −5.2V (Pin 16 to −5.2V) COMP. BINARY	
−FS + 1 LSB	1111 1111 11	−999.02	mV	−0.9766	mV
−15/16 FS	1111 0000 00	−937.5	mV	−62.5	mV
−7/8 FS	1110 0000 00	−865	mV	−124	mV
−3/4 FS	1100 0000 00	−750	mV	−250	mV
−1/2 FS	1000 0000 00	−500	mV	−500	mV
−1/4 FS	0100 0000 00	−250	mV	−750	mV
−1/8 FS	0010 0000 00	−125	mV	−875	mV
−1/16 FS	0001 0000 00	−62.5	mV	−937.5	mV
−1 LSB	0000 0000 01	−0.9766	mV	−999.02	mV
0	0000 0000 00	0.0000	mV	−1.0000	VS

TECHNICAL NOTES

1. **Data Input Coding**
The relation between the binary input code and the analog output voltage is programmed by the COMP BIN control line (pin 16). When COMP BIN is connected to DIG GND (Pin 17) the input coding is straight binary, if COMP BIN is connected to DIG Vs (Pin 15) the input coding is complementary binary.

2. **Clock Inputs**
Input data to the DAC-330 is latched on the rising edge (0 to 1) of CLK (pin 14). The clock inputs $\overline{CLK}$ and CLK (pins 13 and 14 respectively) must be at ECL levels. An alternative method is to drive the CLK (pin 14) and set pin 13 ($\overline{CLK}$) to the mid-point of an ECL level by an external source. Refer to Figure 4 for typical connections.

3. **Digital Input Considerations**
When the DAC-330 is operated at the maximum conversion rate (160 MHz), it is suggested that ECL-100K logic gates be used to drive the inputs of the DAC. The data and clock drivers, for maximum performance, must be terminated at the DAC inputs with the Thevenin equivalent resistance of 50Ω at a dc level of −2V. Further the termination resistors should be placed as close as possible to the digital input pins of the D/A. Refer to Figure 11 for typical connections.

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4. **Reference Voltage**
The full-scale output voltage (ANA OUT) of the DAC is determined by the reference voltage (VREF) on pin 27. Also ANA OUT varies in proportion to the voltage difference between pin 27 (VREF) and pin 26 (ANA Vs). The range in which a linear relationship is established beatween ANA IN and VREF is:

0.50V to 1.5V

To reduce high-frequency noise on the analog output (ANA OUT, pin 20), install a 0.01 μF ceramic capacitor as close as possible between pin 26 (ANA IN) and pin 27 (VREF).

Two circuits for deriving the reference voltage (VREF) are shown in Figures 3 and 4. Figure 3 simply divides the power supply voltage with two resistors. However the analog output voltage of this circuit will vary with any deviation in the supply voltage. Figure 4 eliminates the influence of supply deviations by using a voltage regulator resulting in a more stable analog output voltage.

5. **Output Load Considerations:**
The DAC-330 is a device which uses a load resistance to develop an output voltage. A typical value of the load resistance is 75Ω. Both the full scale output voltage and the zero offset voltage temperature coefficients are dependent on the load resistance. Larger value load resistances result in a lower value temperature coefficient. Refer to output versus temperature chart in Figure 10.

6. **Multiplying Operation:**
To use the DAC-330 in the multiplying mode, apply an external modulation signal coupled by a .001 μF capacitor to pin 27 (VREF). Also remove the 0.01 μF ceramic capacitor connected between pins 26 and 27. Refer to the schematic in Figure 5.

To set up the DAC-330 for multiplying operation:

a. Set the digital inputs (all 1s for straight binary or all 0s for complementary binary for full scale output ANA OUT on Pin 20.

b. With no AC signal applied to pin 27, adjust the 1.5 KΩ potentiometer so that the analog output (pin 20) is −1.0V. The DC voltage at pin 27 is then defined as VREF.

c. Then apply the AC signal such that the amplitude of the signal at pin 27 becomes (VREF +5.2)/2

7. **Power Supply Considerations:**
The board layout should have a ground plane and Vs (supply voltage) plane (−5.2V) as large as possible to reduce parasitic reactance and resistance. The analog and digital grounds should be separated on the printed circuit board, as well as the analog and digital −5.2V (Vs) power lines. For the best system noise reduction, the only place the analog and digital power and ground lines should be interconnected is at the main system power supply.

Both the analog and digital supplies should be bypassed by a 47 μF Tantalum and a 100 pF ceramic capacitor installed as close as possible to the DAC-330.

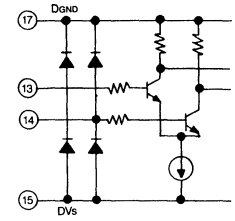


Figure 1. Clock Inputs

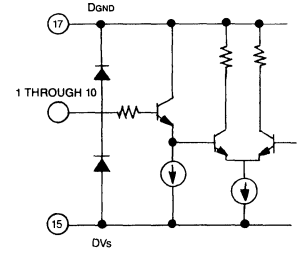


Figure 2. Data Inputs

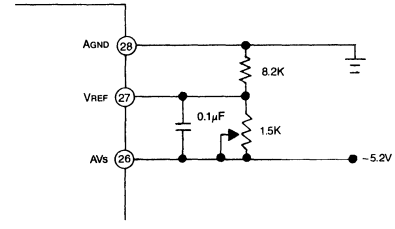


Figure 3. Voltage Reference

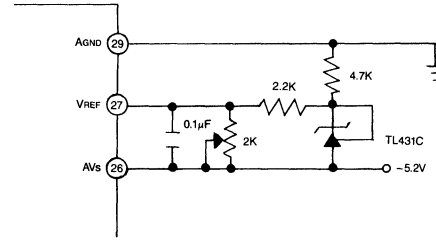


Figure 4. Voltage Reference

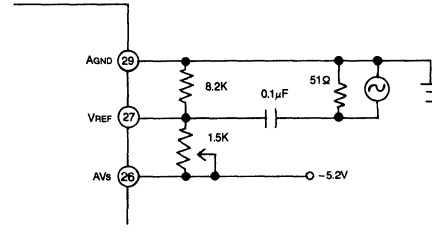


Figure 5. Multiple Circuits

TIMING NOTES

Data input update must be completed at least 5 nSec. before the positive transition of the clock (CLK).

$$T_S \geq 5 \text{ nSec.}$$

The input data is latched into the converter at the CLK and $\overline{CLK}$ crossover points. The data at the input must be held for at least 1 nSec. after this.

$$Thd \geq 1 \text{ nSec.}$$

The analog output will start to change to a new value after a propagation delay of typically 3.8 nSec.

$$Tpd = 3.8 \text{ nSec. (Typ.)}$$

Rise time (Tr) and fall time (Tf) for a full-scale change in analog output is typically 1.5 nSec.

$$Tr = Tf = 1.5 \text{ nSec. (Typ.)}$$

The settling time is calculated from the fall or rise time using the formula.

$$T \text{ (setting)} = 3.45 \times Tr \text{ (or } Tf) \text{ nSec.}$$
$$= 5.2 \text{ nSec.}$$

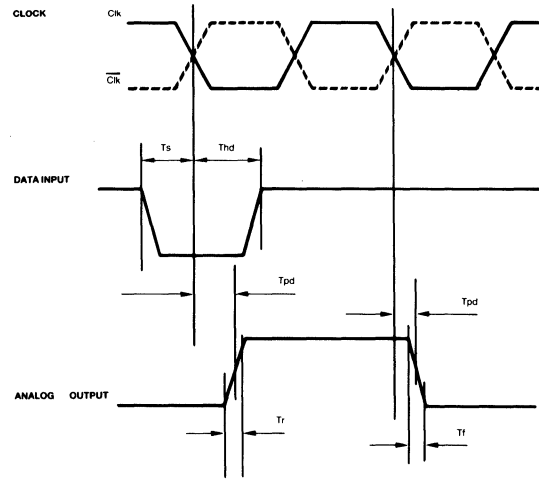


Figure 6. Timing Diagram

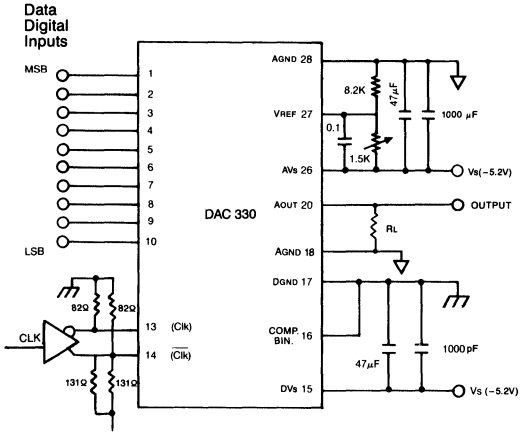


Figure 7. Connection Diagram

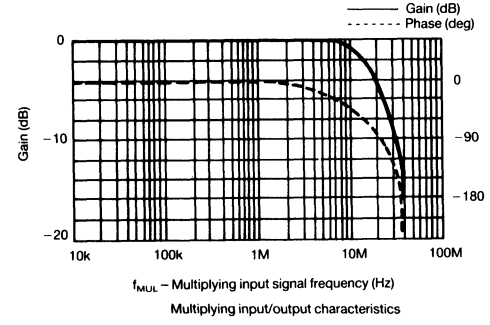


Figure 8. Multiplying Input/Output Characteristics

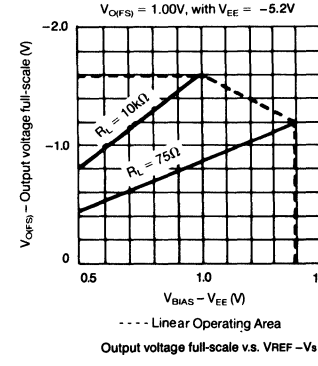


Figure 9. Output Voltage Full-Scale vs V_{REF} –Vs

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE
DAC-330	–20°C to +75°C

DAC-562
Monolithic, High Performance 12-Bit D/A Converter

FEATURES

- **12-Bit resolution**
- **300 Nanoseconds settling time**
- **±10 ppm/°C maximum tempco**
- **5 Output ranges**
- **±¼ LSB linearity**
- **562 Pin compatibility**

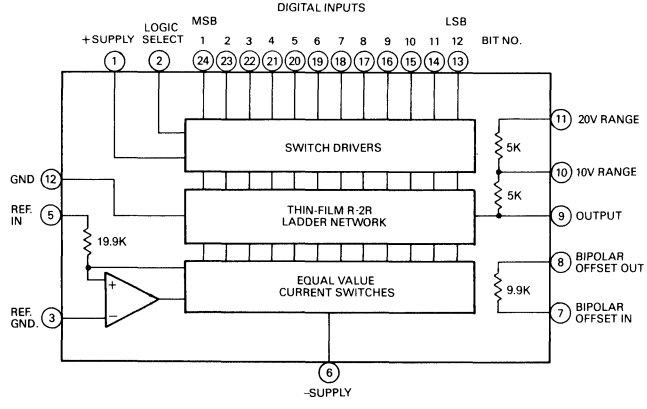
GENERAL DESCRIPTION

The DAC-562 is a new high performance monolithic 12-bit D/A converter fabricated with advanced bipolar technology. The circuit uses a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources to achieve ¼ LSB typical linearity, 300 nanoseconds setting time, and ±10 ppm/°C maximum gain tempco.

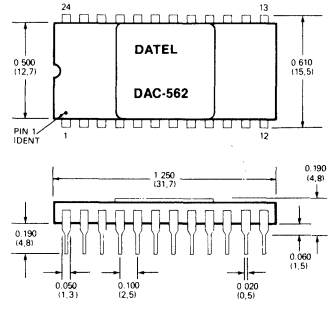
The DAC-562 operates from TTL or CMOS input logic and provides a 0 to 2 mA or ±1 mA output current. The converter contains tracking feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to +5V, 0 to +10V, ±2.5, ±5V, and ±10V. Since these resistors closely track the R-2R ladder with temperature, gain stability of better than 10 ppm/°C is achieved. Differential linearity error is ¼ LSB typical and ½ LSB maximum, with output monotonicity guaranteed over the operating temperature range.

Output settling time for a full-scale change to ½ LSB is 300 nanoseconds typical and 400 nanoseconds maximum.

The DAC-562 is completely pin and function compatible with industry standard 562 D/A converters. The package is a 24-pin hermetically sealed ceramic DIP; power requirement is +5V to +15V and −15V dc. The DAC-562C operates over a 0°C to +70°C temperature range.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+ SUPPLY	13	BIT 12 IN (LSB)
2	LOGIC SELECT	14	BIT 11 IN
3	REF. GROUND	15	BIT 10 IN
4	N.C.	16	BIT 9 IN
5	REFERENCE IN	17	BIT 8 IN
6	− SUPPLY	18	BIT 7 IN
7	BIP. OFF IN	19	BIT 6 IN
8	BIP. OFF OUT	20	BIT 5 IN
9	OUTPUT	21	BIT 4 IN
10	10V RANGE	22	BIT 3 IN
11	20V RANGE	23	BIT 2 IN
12	GROUND	24	BIT 1 IN (MSB)

ABSOLUTE MAXIMUM RATINGS	DAC-562C
Positive Supply, pin 1	+20V
Negative Supply, pin 6	−20V
Reference Input, pin 5	± Supply
Reference Ground, pin 3	0V
Digital Inputs, pins 13-24	−1V to +12V
Logic Select Input, pin 2	−1V to +12V
Output, pin 9	+ Supply, −5V
Resistors, pins 7, 8, 10, 11	± Supply

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +5V and −15V Supplies, +10V reference unless otherwise noted.

INPUTS	DAC-562C
Resolution	12 Bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")[1]	+2.0 min. at 100 nA max.
Input Logic Level, bit OFF ("1")[1]	+0.8V max. at −100 μA max.
Reference Input Voltage	+10V
Reference Input Resistance	20 KΩ
OUTPUTS	
Output Current, unipolar	0 to −2 mA
Output Current, bipolar	±1 mA
Output Voltage Ranges, unipolar	0 to +5V
	0 to +10V
Output Voltage Ranges, bipolar	±2.5V
	±5V
	±10V
Output Voltage Compliance	±1V
Output Resistance	2 KΩ
Output Capacitance	20 pF
PERFORMANCE	
Linearity Error, max.	±½ LSB
Linearity Error Over Temp., max.	±1 LSB
Differential Linearity Error, max.	±½ LSB
Monotonicity	Over Oper. Temp. Range
Gain Error, max.[2]	±0.25%
Unipolar Zero Error, max.[2]	±0.05%
Bipolar Offset Error, max.[2]	±0.25%
Gain Tempco, max.[3]	±10 ppm/°C
Zero Tempco, max.[3]	±2 ppm/°C
Bipolar Offset Tempco, max.[3]	±4 ppm/°C
Settling Time to ½ LSB[4]	300 nsec. typ., 400 nsec. max.
Power Supply Sensitivity, max.	±3.5 ppm of FSR/% Supply
POWER REQUIREMENTS	
Rated Power Supply Voltage	+5V dc, −15V dc
Positive Supply Range[5]	+4.75V to +16.5V
Negative Supply Range	−15V dc ±10%
Power Supply Quiescent Current, max.[6]	+15 mA, −23 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	−65°C to +150°C
Package, Hermetically Sealed	24 pin ceramic DIP
*Specifications same as first column	

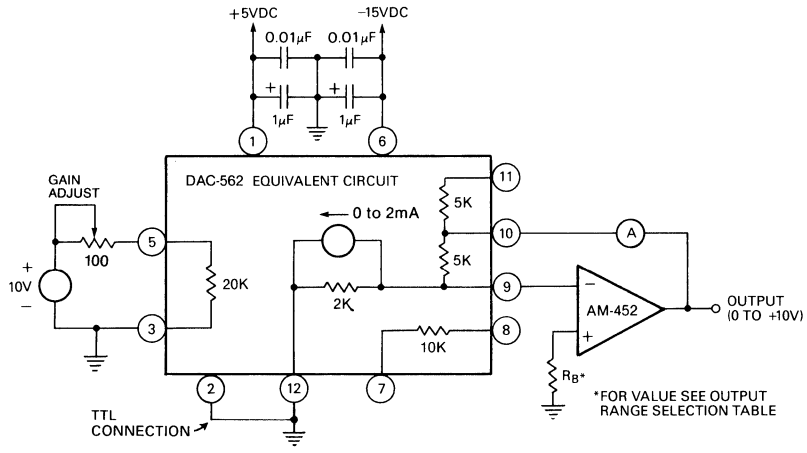
FOOTNOTES:

1. + Supply must be +5V ±5%. For operation with CMOS logic, see Technical Note 1.
2. Adjustable to zero using external potentiometers. Specified error is for 100 ohm trim resistors and external operational amplifier using internal feedback resistor.
3. Using external operational amplifier and internal feedback and offset resistor. Zero Tempco and Bipolar Offset Tempco are in ppm/°C or FSR (Full Scale Range)
4. For full-scale change: all bits ON-to-OFF, or all bits OFF-to-ON.
5. Maximum Positive Supply Voltage is +16V for high level logic only, i.e., when Pin 2 is tied to Pin 1. See Technical Note 1.
6. Allow 30 seconds warm-up time.

TECHNICAL NOTES

1. For TTL input logic; pin 2 should be connected to pin 12 and the + supply must be +5V dc (±5%). For CMOS input logic, connect pin 2 to pin 1 and use any + supply voltage from +9.5V to +12V dc. CMOS threshold levels are then + Vs x 0.7 for bit ON and + Vs x 0.3 for bit OFF. Logic input current is the same as that specified for TTL.
2. Gain and bipolar offset errors are adjustable to zero by means of two 100 ohm trimming pots. The adjustment range is ±0.3% of FSR for gain and ±0.6% of FSR for bipolar offset. The unipolar zero error is adjustable to zero by means of the offset adjustment of the external output amplifier.
3. The output voltage compliance range of ±1V should not be exceeded or else accuracy will be affected. If a resistor load is driven instead of an operational amplifier summing junction then the maximum resistor value is 500 ohms for unipolar operation and 1K ohms for bipolar operation.
4. Output settling time is specified for current output and is measured with a small current sampling resistor to ground (100 ohms). Voltage output settling time depends on the output operational amplifier used. DATEL's AM-500 is recommended for about 500 nanoseconds settling and AM-452-2 is recommended for about 1.5 microseconds settling. Both should be used with a 3-20 pF variable compensating capacitor across the feedback resistor which should be adjusted for optimum settling time.
5. For best high speed performance, both power supplies should be bypassed with 1 μF electrolytics in parallel with 0.01 μF ceramic capacitors as close as possible to the ± supply pins.
6. The gain and bipolar offset temperature coefficients are specified with the internal feedback and offset resistors used in conjunction with an external operational amplifier. This is because these resistors track the R-2R ladder with temperature and therefore the tempco's do not depend on absolute resistor tempco. The tempco of the external +10V reference must also be included in the total converter tempco, however.
7. The DAC-562 wideband output noise with all bits ON is typically 100 μV peak-to-peak over 0.1 Hz to 5 MHz.

UNIPOLAR OPERATION—See Output Range Selection Table

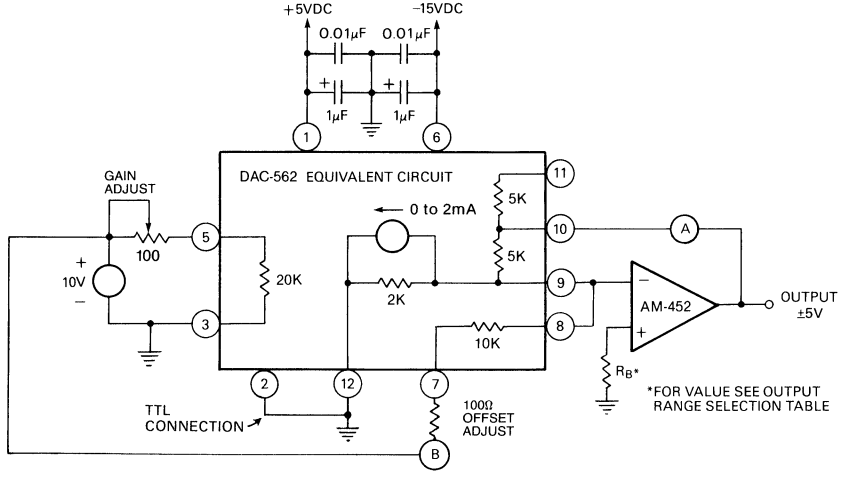


OUTPUT VOLTAGE RANGE SELECTION (See Connection Diagrams)

OUTPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER				R_B, BIAS COMP. RESISTOR*
0 to +5V	A & 10	9 & 11			1.11 kΩ
0 to +10V	A & 10				1.43 kΩ
±2.5V	A & 10	9 & 11	8 & 9	7 & B	1 kΩ
±5V	A & 10		8 & 9	7 & B	1.25 kΩ
±10V	A & 11		8 & 9	7 & B	1.43 kΩ

*Carbon composition resistor value used from amplifier positive input terminal to ground to compensate for offset due to bias current.

BIPOLAR OPERATION—See Output Range Selection Table



CALIBRATION AND APPLICATION

CODING TABLE—See Calibration Procedure

INPUT CODE	OUTPUT VOLTAGE RANGE				
	0 to +5V	0 TO +10V	±2.5V	±5V	±10V
1111 1111 1111	+4.9988V	+9.9976V	+2.4988V	+4.9976V	+9.9951V
1100 0000 0000	+3.7500	+7.5000	+1.2500	+2.5000	+5.0000
1000 0000 0000	+2.5000	+5.0000	0.0000	0.0000	0.0000
0100 0000 0000	+1.2500	+2.5000	−1.2500	−2.5000	−5.0000
0000 0000 0001	+0.0012	+0.0024	−2.4988	−4.9976	− 9.9951
0000 0000 0000	0.0000	0.0000	−2.5000	−5.0000	−10.0000

CALIBRATION PROCEDURE

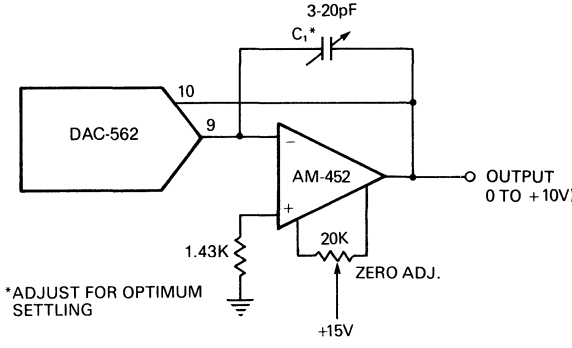
UNIPOLAR OPERATION

1. Set all digital inputs low. Adjust the output amplifier offset for 0 volts output.
2. Set all digital inputs high. Adjust Gain trimming pot for an output of +FS − 1 LSB.
   FS − 1 LSB = +9.9976V for 0 to +10V range.
   = +4.9988V for 0 to +5V range.

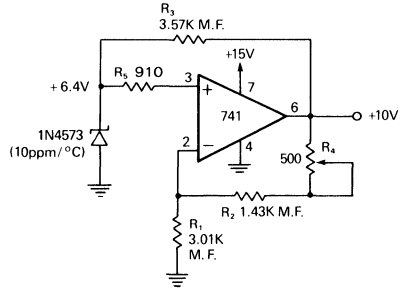
BIPOLAR OPERATION

1. Set all digital inputs low. Adjust Bipolar Offset trimming pot for one of the following output voltages:
   −2.5V for ±2.5V range
   −5.0V for ±5V range
   −10.0V for ±10V range
2. Set bit 1 (MSB) input high and all other digital inputs low. Adjust Gain trimming pot for 0 volts output.

CIRCUIT FOR FAST VOLTAGE OUTPUT (≈1.5 μSEC. SETTLING)

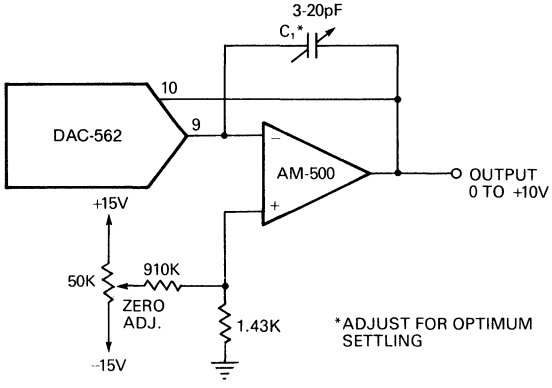


+10V REFERENCE CIRCUIT



Adjust R_4 for +10.000V output. For best stability R_1 & R_2 should track each other closely with temperature. R_4 should be a low tempco trimming pot or else a selected metal film trim resistor.

CIRCUIT FOR FAST VOLTAGE OUTPUT (≈0.5 μSEC. SETTLING)



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
DAC-562C	0 to +70°C

ACCESSORIES

Part Number	Description
TP50 —	Trimming potentiometer

DAC-608, DAC-610, DAC-612
Microprocessor-Compatible, Double-Buffered D/A Converters

FEATURES

- **Microprocessor-compatible**
- **Double-buffered inputs**
- **8-, 10- and 12-Bit resolution**
- **500 Nanoseconds settling time— DAC-610**
- **4-Quadrant multiplication**

GENERAL DESCRIPTION

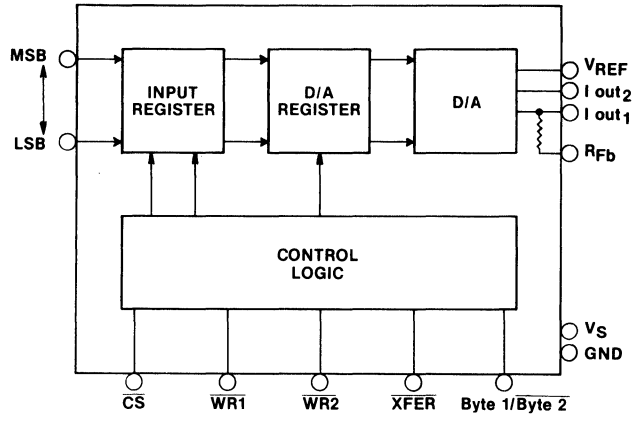
DATEL's DAC-608, DAC-610 and DAC-612 are low cost monolithic 8-, 10-and 12-bit multiplying D/A converters designed to operate directly with most popular microprocessors. Double-buffered inputs allow the converters to output an analog voltage corresponding to one digital word while holding the next, permitting simultaneous updating of multiple D/A's via a common strobe signal. The converters appear as a memory location or I/O port to the microprocessor and thus do not require interfacing logic. All models will operate as normal D/A's for non-microprocessor based applications.

Excellent temperature tracking characteristics are provided by precision silicon-chromium R-2R resistor ladder networks. Output settling time for a full-scale change to ½ LSB, is as low as 500 nanoseconds and the maximum linearity error on all models is ±½ LSB. Monotonicity is guaranteed over the full operating temperature range.

Other features include a low, 3 mV peak-to-peak, digital feedthrough error, 30 mW power dissipation and single supply operation. The reference input is selectable over a range of ± 10V and may also be used as the analog input for four quadrant multiplication applications.

The DAC-612C is packaged in a 24-pin ceramic DIP. Models DAC-608 and DAC-610 are packaged in a 20-pin plastic DIP. All units are specified to operate over the commerical 0° C to +70° C temperature range. These devices are an ideal choice for innumerable applications involving industrial process control, programmable attenuators, audio signal processing and low frequency sine wave generation.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.



INPUT/OUTPUT CONNECTIONS

DAC-608

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR1}$ (WRITE 1)
3	ANALOG GROUND
4	DI3
5	DI2
6	DI1
7	DI0 (LSB)
8	REFERENCE IN
9	FEEDBACK
10	DIGITAL GROUND
11	OUTPUT 1
12	OUTPUT 2
13	DI7 (MSB)
14	DI6
15	DI5
16	DI4
17	$\overline{XFER}$ (Trans. Contl.)
18	$\overline{WR2}$ (Write 2)
19	ILE (In. Latch ENB)
20	VS

DAC-610

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR}$ (WRITE)
3	BYTE 1/$\overline{BYTE\ 2}$
4	$\overline{XFER}$
5	DI5
6	DI6
7	DI7
8	DI8
9	DI9 (MSB)
10	GROUND
11	OUTPUT 2
12	OUTPUT 1
13	REFERENCE IN
14	FEEDBACK
15	DI0 (LSB)
16	DI1
17	DI2
18	DI3
19	DI4
20	VS

DAC-612

PIN	FUNCTION
1	$\overline{CS}$ (CHIP SELECT)
2	$\overline{WR1}$
3	ANALOG GROUND
4	DI5
5	DI4
6	DI3
7	DI2
8	DI1
9	DI0 (LSB)
10	REFERENCE IN
11	FEEDBACK
12	DIGITAL GROUND
13	OUTPUT 1
14	OUTPUT 2
15	DI11 (MSB)
16	DI10
17	DI9
18	DI8
19	DI7
20	DI6
21	$\overline{XFER}$ (Trans. Contl.)
22	$\overline{WR2}$ (Write 2)
23	BYTE 1/$\overline{BYTE\ 2}$
24	VS

ABSOLUTE MAXIMUM RATINGS	DAC-608	DAC-610	DAC-612C
Power Supply Voltage		+17V dc	
Logic Input Voltage		V_S to ground	
Reference Input Voltage		±25V	
Output Voltage		V_S to 100 mV	
Package Dissipation		500 mW	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Package Type:	
DAC-608/610	20-pin plastic DIP
DAC-612	24-pin ceramic DIP

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, 15V Supply, Reference In = +10V unless otherwise noted.

INPUTS	DAC-608	DAC-610	DAC-612
Resolution	8 bits	10 bits	12 bits
Coding, Unipolar operation		Straight Binary	
Bipolar operation		Offset Binary	
Input Logic Level, bit ON ("1")		+2.2V minimum at + 10 µA maximum	
Input Logic Level, bit OFF ("0")		+0.8V maximum at −200 µA maximum	
$\overline{CS}$ (Chip Select)	Active low state in combination with ILE enables the D/A for Write 1 operation. Minimum pulse duration is 320 nsec.. $\overline{CS}$ must remain low an additional 10 nsec. after Write Pulse returns high.		
ILE (Input Latch Enable)[1]	Active high state in combination with $\overline{CS}$ enables the D/A for Write 1 operation. Minimum Pulse duration is 320 nsec. ILE must remain high an additional 10 nsec. after Write Pulse returns high.		
$\overline{WR1}$ (Write 1)	Active low state is used to load the digital data bits into the input latch. A high ON $\overline{WR1}$, and a high on ILE will update the input latch. Minimum Pulse duration is 320 nsec.		
$\overline{WR2}$ (Write 2)	Active low in combination with $\overline{XFER}$ transfers available data in the input latch to the D/A register. The data in the D/A register is latched when $\overline{WR2}$ is high. Minimum Pulse Duration is 320 nsec.		
Byte 1/$\overline{Byte\ 2}$ (Byte Sequence Control)[2]	All locations of the input latch are enabled when this control is high. When low, only least significant bits are enabled. Pulse Duration is 320 nsec.		
$\overline{XFER}$ (Transfer Control Signal)	Active low in combination with $\overline{WR2}$, will transfer the data available in the input latch to the D/A register.		

OUTPUTS			
Output Capacitance, Output 1[3]	70 pF	60 pF	70 pF
Output 2[3]	200 pF	250 pF	200 pF
Output 1[4]	200 pF	250 pF	200 pF
Output 2[4]	70 pF	60 pF	70 pF
Output 1, Current Range[5]	$\frac{V_{REF}}{15\ k\Omega}\ \frac{D}{256}$	$\frac{V_{REF}}{15\ k\Omega}\ \frac{D}{1024}$	$\frac{V_{REF}}{15\ k\Omega}\ \frac{D}{4096}$
Output 2, Current Range[5]	$\frac{V_{REF}}{15\ k\Omega}\ \frac{256-D}{256}$	$\frac{V_{REF}}{15\ k\Omega}\ \frac{1024-D}{1024}$	$\frac{V_{REF}}{15\ k\Omega}\ \frac{4006-D}{4096}$
Feedthrough Error[3]	3 mV P-P	90 mV P-P	3 mV P-P

PERFORMANCE			
Linearity Error Maximum		±½ LSB	
Differential Linearity Error Maximum		±0.018% FSR	
Monotonicity		Over operating temperature range	
Gain Error[6]		Adjustable to Zero	
Zero Error[6]		Adjustable to Zero	
Gain Tempco Maximum	±6 ppm/°C	±10 ppm/°C	±6 ppm/°C
Settling Time, Full Scale change to ±½ LSB	1 µsec.	500 nsec.	1 µsec.
Power Supply Rejection[4]	±2 ppm/V	±30 ppm/V	±3 ppm/V

POWER REQUIREMENTS	
Rated Power Supply Voltage	+15V dc
Power Supply Voltage Range	+4.7V dc to +15.75V dc
Supply Current Maximum	2 mA

FOOTNOTES:

1. DAC-608 only.
2. DAC-610/612 only.
3. All data inputs latched low. To achieve this low feedthrough on the DAC-612, the metal lid must be grounded. If the lid is left floating the feedthrough is typically 6 mV.
4. All data inputs latched high.
5. "D" stands for digital input.
6. Using internal feedback resistor.

TECHNICAL NOTES

1. The output operational amplifier to be used should have as low a value of input bias current as possible. DATEL's AM-410 operational amplifiers are highly recommended for use with these devices.

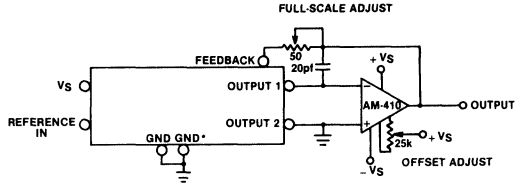
   In order to maintain the specified temperature tracking specifications, the D/A's internal feedback resistor should be used in the operational amplifier feedback loop.
2. The voltage at the current outputs must be as close to ground potential as possible so that the changes in the applied digital codes do not affect the output current linearity.
3. In fast data acquisition applications, the addition of a 10 to 22 pF capacitor (Cc) in parallel with the feedback resistor of the operational amplifier may be required to minimize overshoot and ringing at the output.
4. Due to the rapid switching of internal logic gates that respond to the input changes, a narrow spike could flow out from the current output terminals. In order to minimize this effect, the input register must always be used as the data latch. Reducing V_S from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, however, this causes a loss of internal switching speed. Also, increasing capacitor Cc (if being used) to a value consistent with the actual circuit bandwidth requirements, can provide a substantial damping effect on any output spikes.
5. For flow through operation, (operation with the buffers continuously enabled) $\overline{CS}$, $\overline{WR1}$, $\overline{WR2}$ and $\overline{XFER}$ must be tied to ground and Byte 1/Byte 2 (ILE for DAC-608) must be high. This will allow

both internal registers to follow the applied digital inputs, directly affecting the device output.

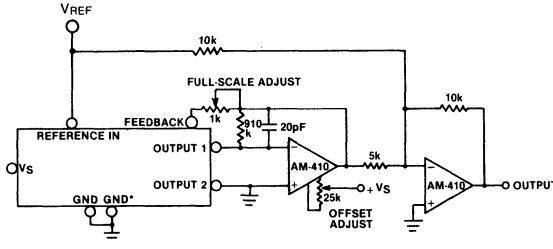
6. For stand alone operation where control signals are generated by discrete logic, double buffering can be controlled by applying a logic "0" to $\overline{CS}$ and $\overline{XFER}$ and a logic "1" to ILE and pulling $\overline{WR1}$ low to load data in the input latch. Pulling $\overline{WR2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.
7. All unused digital inputs should be tied to V_S or ground in order to prevent damage to the chip from static discharge. If any of the digital inputs are inadvertently left floating, the D/A will interpret the pin as a logic "1".
8. The input registers of the DAC-610 and DAC-612 are arranged to accept a left justified data word from the microprocessor with 8 bits coming first and the lower bits second. Left-justified means that the binary point is assumed to be located to the left of the most significant bit.
9. The use of good circuit board layout techniques are required for rated performance. Minimization of lead lengths around analog circuitry is recommended. It is important that a good ground be used. A single point ground distribution technique for analog signals and supply returns will prevent other devices in the system from affecting the output of the D/A's. V_S should be bypassed as close to the V_S pin as possible with a low inductance 1 μF tantalum capacitor.

CODING AND CALIBRATION

CALIBRATION PROCEDURE



UNIPOLAR CONFIGURATION



BIPOLAR CONFIGURATION

*ONE GROUND ON DAC-610

UNIPOLAR

Zero Adjust—Set all data bits to logic "0" (logic "1" if using output 2) and adjust the OFFSET ADJUST pot on the external operational amplifier for 0.000V.

Full Scale—Set all data bits to logic "1" (logic "0" if using output 2) and set the FULL Scale ADJUST for an output equal to: Vout = – Vref (N – 1)/N, where "N" is equal to: 256 (DAC-608), 1024 (DAC-610) or 4096 (DAC-612).

BIPOLAR

Zero Adjust—Set all data bits to logic "0" and adjust the OFFSET ADJUST for an output voltage equal to Vref.

Full Scale—Set all data bits to logic "1" and adjust the FULL SCALE ADJUST for an output voltage equal to: Vout = Vref (N-X)/X where "N" is equal to: 255 (DAC-608), 1023 (DAC-610) or 4095 (DAC-612); and "X" is equal to: 128 (DAC-608), 512 (DAC-610) or 2048 (DAC-612).

OUTPUT CODING TABLES

UNIPOLAR OPERATION

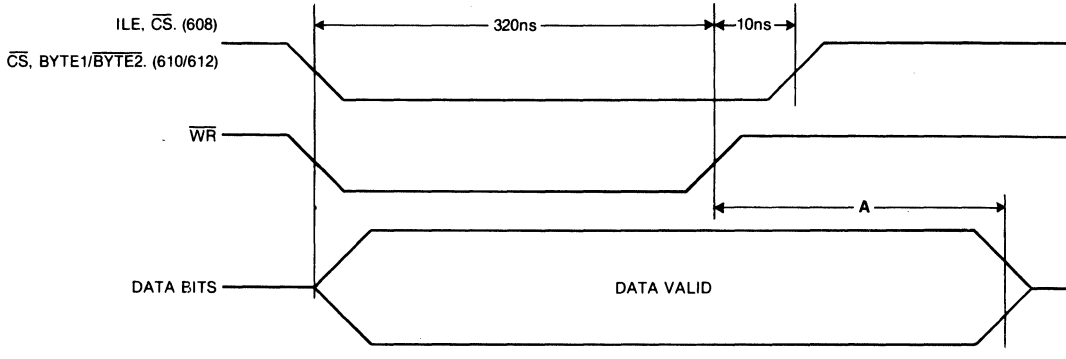
INPUT CODE MSB ..... LSB	IDEAL OUTPUT
111 111	– (V_{REF} + 1 LSB)
110 000	– 0.75 (V_{REF})
100 000	– 0.5 (V_{REF})
010 000	– 0.25 (V_{REF})
000 000	0

BIPOLAR OPERATION

INPUT CODE MSB ..... LSB	IDEAL OUTPUT + V_{REF}	IDEAL OUTPUT – V_{REF}
111 111	+ V_{REF} – 1 LSB	– V_{REF} + 1 LSB
110 000	0.5 (+ V_{REF})	0.5 (– V_{REF})
100 000	0	0
010 000	0.5 (– V_{REF})	0.5 (+ V_{REF})
000 000	– V_{REF}	+ V_{REF}

TIMING AND PERFORMANCE

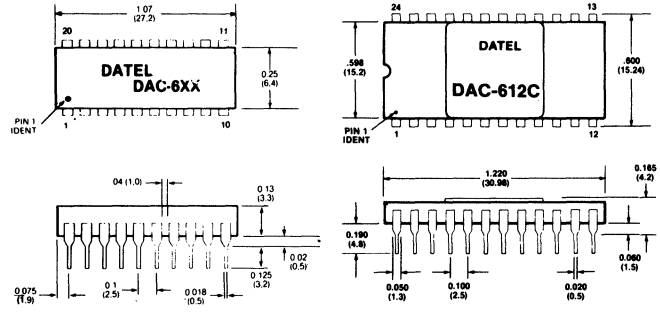
TIMING DIAGRAM



MODEL	A
DAC-608	90ns
DAC-610	200ns
DAC-612	90ns

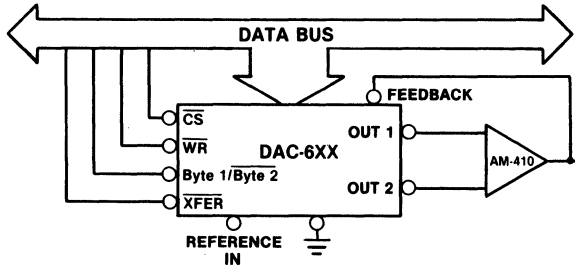
NOTE:
1. Settling time is measured from the leading edge of the WR pulse.
2. All digital controls are level actuated.

MECHANICAL DIMENSIONS
INCHES (MM)



APPLICATIONS

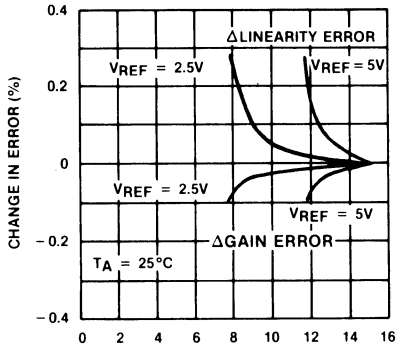
Typical Connection to Popular Microprocessor Data Bus



The logic functions of the DAC-608/610/612 have been oriented towards an ease of interface with all popular microprocessors.

The devices are treated as a typical memory device or I/O peripheral requiring no external logic in most systems due to the timing and logic level convention of the input control signals.

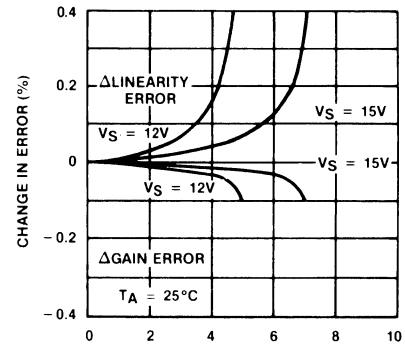
DAC-608 Gain and Linearity Error Variation vs. Supply Voltage



VOLTAGE MODE OPERATION

VS SUPPLY VOLTAGE (VDC)

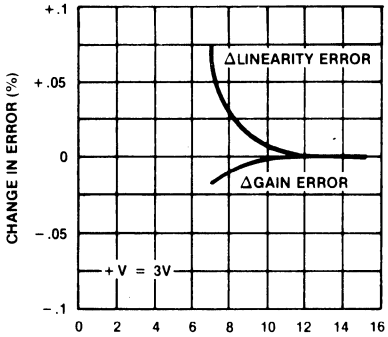
DAC-608 Gain and Linearity Error Variation vs. Reference Voltage



VOLTAGE MODE OPERATION

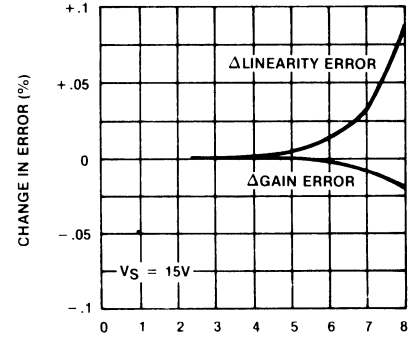
VREF, REFERENCE VOLTAGE (VDC)

DAC-610 Gain and Linearity Error Variation vs. Supply Voltage



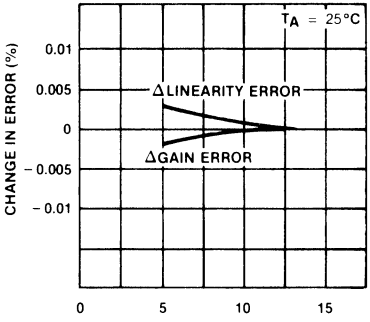
SUPPLY VOLTAGE, VS (VDC)

DAC-610 Gain and Linearity Error Variation vs. Reference Voltage



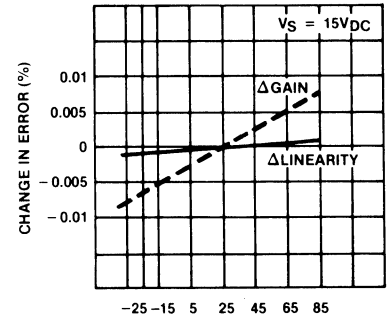
REFERENCE VOLTAGE +V (VDC)

DAC-612 Gain and Linearity Error Variation vs. Supply Voltage



VS — SUPPLY VOLTAGE (VDC)

DAC-612 Gain and Linearity Error Variation vs. Temperature

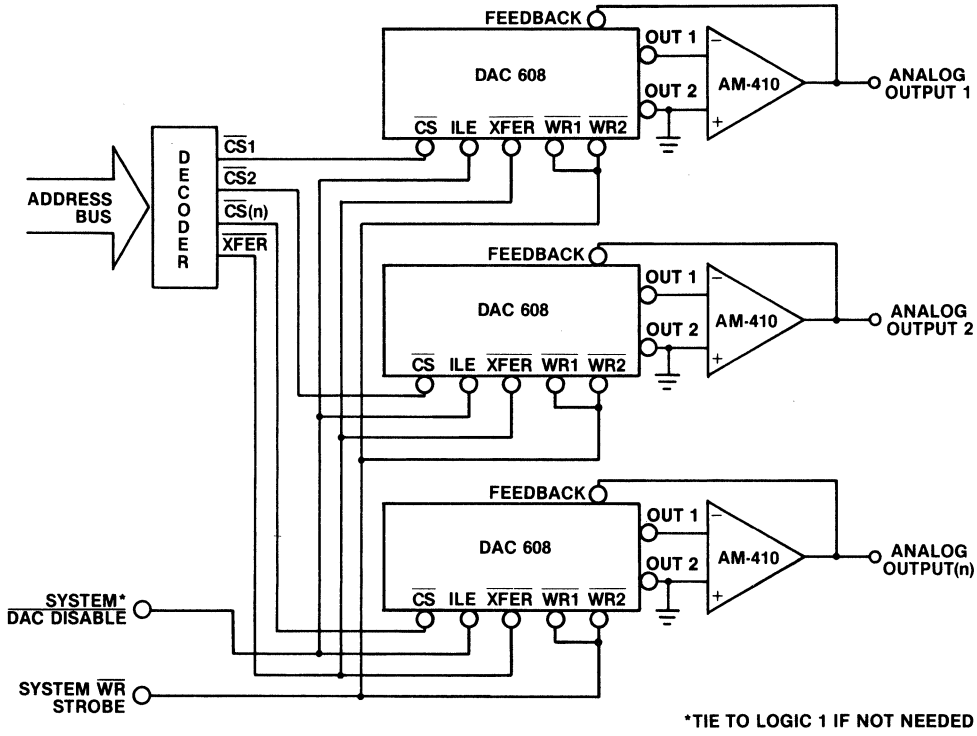


TA — AMBIENT TEMPERATURE (°C)

2

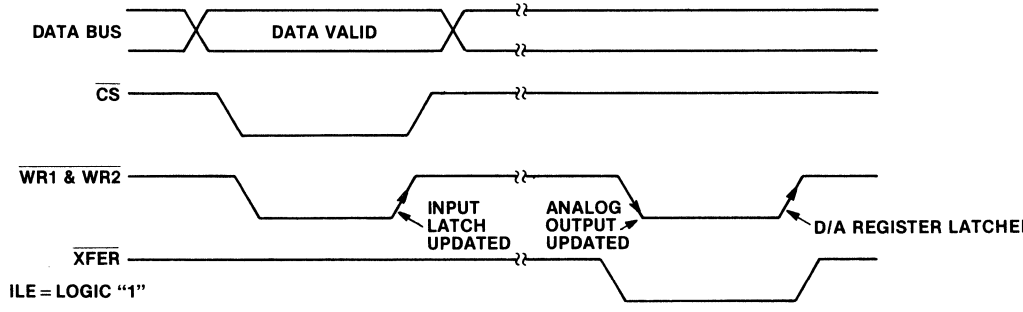
APPLICATIONS

MULTIPLE D/A SYSTEM



*TIE TO LOGIC 1 IF NOT NEEDED

TIMING DIAGRAM



For simultaneous updating of multiple D/A's, the $\overline{CS}$ line of each device is decoded individually. However, the converter can share a common $\overline{XFER}$.

The ILE function is very useful in applications where more than one processor is being used. If another processor took control of the data bus and control lines using the same addresses as the first, a low on the ILE pin would latch the data in the input register holding the outputs at their present state.

ORDERING INFORMATION

MODEL NO.	RESOLUTION	OPERATING TEMP. RANGE
DAC-608C	8 Bits	0°C to +70°C
DAC-610C	10 Bits	0°C to +70°C
DAC-612C	12 Bits	

DAC-7134B, DAC-7134U
14-Bit Microprocessor-compatible Multiplying D/A Converters

FEATURES

- 14-Bit linearity (0.003% FSR)
- Microprocessor-compatible with doubled-buffered inputs
- 3 Microsecond maximum output current settling time (0.9μS typical)
- Low power dissipation
- Full four-quadrant multiplication
- Gain Tempco of +/-8ppm/degree C maximum
- PROM-controlled correction circuits

GENERAL DESCRIPTION

The DAC-7134 achieves true 14-bit linearity by combining a four-quadrant, multiplying DAC with on-chip, PROM-controlled correction circuits. The DAC uses thin-film resistors and CMOS circuitry for stability while the PROM-controlled correction circuit eliminates errors introduced by the thermal stresses of packaging.

There are two versions of the DAC-7134, both represented by the block diagram, Figure 1. The DAC-7134U is programmed for unipolar operation while the DAC-7134B is programmed for bipolar applications. Microprocessor bus interfacing is easy using standard memory write cycle timing and control signals. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs.

There are two reference voltage inputs feeding the resistor ladder network. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder.

For unipolar use, the two reference inputs are tied together. For bipolar applications, the polarity of the MSB reference is reversed through an external operational amplifier. This flexibility gives the DAC a true 2's complement input transfer function. The DAC-7134 contains two resistors used along with the external op-amp to invert the reference. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

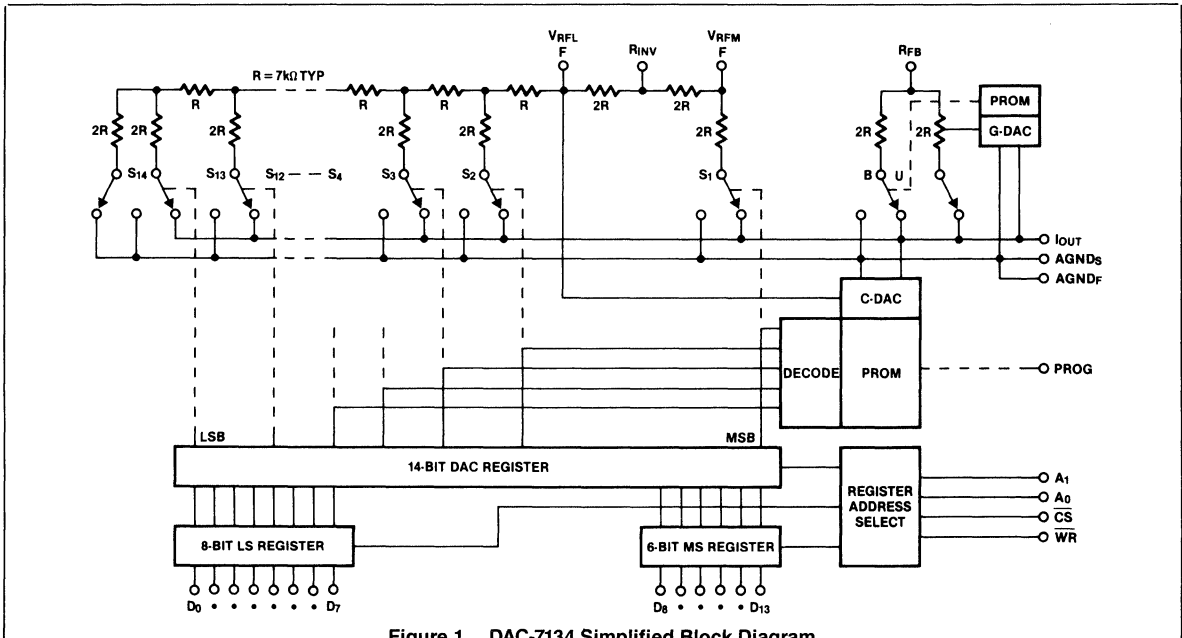


Figure 1. DAC-7134 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage:	
V^+ to DGND	-0.3V dc to +7.5V dc
Analog Signals:	
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND	+/-15V dc
I_{OUT}, $AGND_F$, $AGND_S$	-0.1V dc to V^+
Current in $AGND_S$, $AGND_F$	25 mA
Digital Signals:	
A_0, A_1, D_0 to D_{13}, $\overline{WR}$, $\overline{CS}$, PROG	-0.3V to V^+ +0.3V dc

FUNCTIONAL SPECIFICATIONS

Valid at +25 degrees C, +5V dc power supply, and V_{REF} = +10V dc, unless otherwise specified.

DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
INPUT				
Resolution	14	-	-	bits
Logic Levels				
Logical 0	-	-	0.8	V
Logical 1	2.4	-		V
Logic Input Currents	-	-	1.0	µA
Reference Input Resistance	4.0	7.0	10	K ohms
Reference Input Voltage Range	-	-	±12	V
Coding				
Unipolar		straight binary		
Bipolar		2's complement		
ACCURACY				
Non-linearity [1,2]				
J	-	-	0.012	% FSR
K	-	-	0.006	% FSR
L	-	-	0.003	% FSR
Non-linearity Temp. Coef.	-	1	2	ppm/°C
Gain Error [1,2]				
J	-	-	0.024	% FSR
K	-	-	0.012	% FSR
L	-	-	0.006	% FSR
Gain Error Temp. Coef.	-	2	8	ppm/°C
Monotonicity				
J	12	-	-	bits
K	13	-	-	bits
L	14	-	-	bits
Settling Time	-	0.9	3	µSec.
Power Supply Rejection	-	10	100	ppm/V
OUTPUT				
Output Current Range	-	2.14	±3.75	mA
Output Capacitance				
DAC all 0's	-	160	-	pf
DAC all 1's	-	235	-	pf
Output Noise (Equiv. Johnson Noise)	-	7	-	K ohm
Feedthrough Error				
DAC-7134U	-	250	-	µVp-p
DAC-7134B	-	500	-	µVp-p

FOOTNOTES:

1. Full-scale range (FSR) is 10 volts for unipolar mode, 20 volts (± 10 volts) for bipolar mode.
2. Using internal feedback and reference inverting resistors.

DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
POWER				
Supply Voltage Range	+3.5	-	+6.0	V dc
Supply Current (Excluding ladder)	-	1.0	2.5	mA
Power Dissipation	-	-	500	mW
PHYSICAL / ENVIRONMENTAL				
Operating Temperature Range	0	-	+70	°C
Storage Temperature Range	-65	-	+150	°C
Package	28-pin CERDIP only			

The timing diagram represented in Figure 2 shows the relationships between the various bus interface signals. These AC characteristics are listed in Table 1.

DETAILED DESCRIPTION

The DAC-7134 consists of a 14-bit primary DAC, two PROM-controlled correction DAC's, input buffer registers, and microprocessor interface logic (refer back to Figure 1). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC (G-DAC) diverts up to 2% of the feedback resistor's current to analog ground and reduces the gain error to less than 1 LSB, or 0.006%.

The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC (C-DAC). For every combination of the primary DAC's most significant bits, a different C-DAC code is selected. This corrects summation errors (caused when more than one bit is turned on simultaneously) and voltage non-linearity in the feedback resistor.

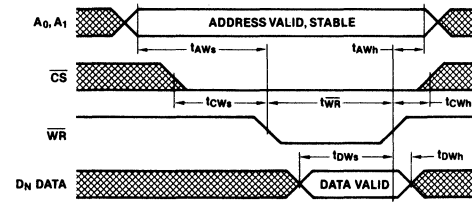


Figure 2. DAC-7134 Timing Diagram

Table 1. AC Characteristics

PARAMETER (V+ = +5V dc)	SYMBOL	MINIMUM (nS)
Address write set-up time	T_{AWs}	100
Address-write hold time	T_{AWh}	0
Chip select-write set-up time	T_{CWs}	0
Chip select-write hold time	T_{CWh}	0
WRITE pulse width, low	$T_{\overline{WR}}$	200
Data write set-up time	T_{DWs}	200
Data write hold time	T_{DWh}	0

PIN DESCRIPTIONS

The input and output pins for both the analog and digital signals used by the DAC-7134 are listed in Table 2 and shown in Figure 3.

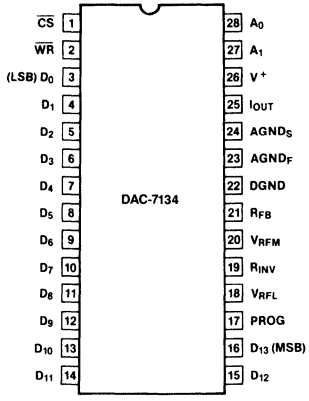


Figure 3. DAC-7134 Pin Configuration

Table 2. Pin Assignment and Function Description

PIN	DESCRIPTION	
1	$\overline{\text{CHIP SELECT}}$ (active low). Enables writing to the register.	
2	$\overline{\text{WRITE}}$, (active low). Enables writing to the register along with $\overline{\text{CHIP SELECT}}$.	
3	Bit 0	Least Significant Bit
4	Bit 1	INPUT DATA BITS High = True
5	Bit 2	
6	Bit 3	
7	Bit 4	
8	Bit 5	
9	Bit 6	
10	Bit 7	
11	Bit 8	
12	Bit 9	
13	Bit 10	
14	Bit 11	
15	Bit 12	
16	Bit 13	Most Significant Bit
17	Used for programming only. Tie to +5V dc for normal operation.	
18	V_{REF} for lower bits	
19	Summing node for reference inverting amplifier	
20	V_{REF} for MSB only (bipolar).	
21	Feedback resistor for voltage output applications	
22	Digital ground return	
23	Analog ground force line. Carries current from internal analog ground connections. Tied internally to $AGND_S$.	
24	Analog ground sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	Current output pin	
26	Positive supply voltage	
27	Address 1	Control register lines
28	Address 0	

ANALOG SECTION

The DAC-7134 provides both unipolar and bipolar operation. The bipolar application circuit (Figure 4) requires one additional operational amplifier, but no external resistors. Two on-chip resistors (R_{INV1}, R_{INV2}), together with the op-amp, form a voltage inverter which drives the MSB reference terminal (V_{RFM}) to $-V_{REF}$.

V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL}. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF}, and the R_{INV} pin is left unconnected.

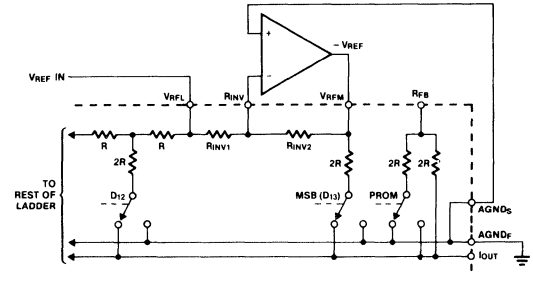


Figure 4. Bipolar Operation, with Inverted V_{REF} to MSB

Since the PROM correction codes required are different for bipolar and unipolar operation, the DAC-7134 is available in two different versions; the DAC-7134U, which is corrected for unipolar operation, and the DAC-7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from "R" in the unipolar device to "2R" in the bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

DIGITAL SECTION

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations:

1. Load the LS buffer register with the data at inputs D_0 to D_7,
2. Load the MS buffer register with the data at inputs D_8 to D_{13},
3. Load the DAC register with the contents of the MS and LS buffer registers, and,
4. Load the DAC register directly from the data input pins. (See Table 3).

The $\overline{CS}$ and $\overline{WR}$ pins must be low to allow data transfer to occur. When direct loading is selected ($\overline{CS}$, $\overline{WR}$, A_0 and A_1 low), the registers are transparent and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal read-only use the PROG pin should be tied to V^+ (+5V dc).

Table 3. Data Loading Controls

CONTROL LINES				DAC-7134 OPERATION
A_0	A_1	$\overline{CS}$	$\overline{WR}$	
X	X	X	1	No operation, device not selected
X	X	1	X	
0	0	0	0	Load registers from data bus
0	1	0	0	Load LS register from data bus
1	0	0	0	Load MS register from data bus
1	1	0	0	Load DAC register from MS and LS register

Note: Data is latched on low-to-high transitions of either $\overline{WR}$ or $\overline{CS}$.

UNIPOLAR BINARY OPERATION

Figure 5 shows a typical circuit configuration for unipolar mode operation using a DAC-7134U. With positive and negative V_{REF} values, the circuit is capable of two-quadrant multiplication. Table 4 presents a digital input code/analog output value' reference for unipolar mode operation. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers.

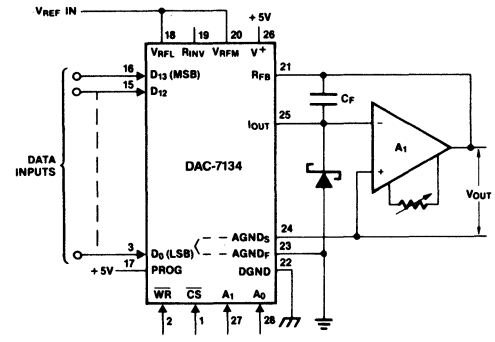


Figure 5. Unipolar Binary, Two-Quadrant Multiplying Circuit

Table 4. Code Table—Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
MSB LSB	
1 1 1 ..... 1 1 1	$-(V_{REF} + 1\ LSB)$
1 1 0 ..... 0 0 0	$-0.75 \times (V_{REF})$
1 0 0 ..... 0 0 0	$-0.5 \times (V_{REF})$
0 1 0 ..... 0 0 0	$-0.25 \times (V_{REF})$
0 0 0 ..... 0 0 0	0

Zero Offset Adjustment
(See Figure 5)

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND. (Connect pins 1 through 16, 27, and 28 to pin 22).
2. Adjust the offset zero-adjust trim-pot of op-amp A2, if used, for a maximum of 0V $\pm 50\mu V$ dc at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of output op-amp A1 for a maximum of 0V $\pm 50\mu V$ dc at V_{OUT}.

Gain Adjustment (Optional)

1. Connect all data inputs (pins 1 through 16) to V^+ (pin 26). Connect $\overline{CS}$, $\overline{WR}$, A_1 and A_0 (pins 1, 2, 27, and 28 respectively) to DGND (pin 22).
2. Monitor V_{OUT} for a $-(V_{REF} + 1\ LSB)$ reading.
3. To decrease V_{OUT}, connect a series resistor of 100 ohms or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT}, connect a series resistor of 100 ohms or less between OP-AMP A1's output and the R_{FB} terminal (pin 21).

For applications where the output reference ground point is established somewhere other than at the DAC, a circuit similar to that shown in Figure 6 could be used. Here, op-amp A2 removes the slight error due to IR voltage drop between the internal analog ground node and the external ground connection. For 13-bit or lower accuracy, omit A2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.

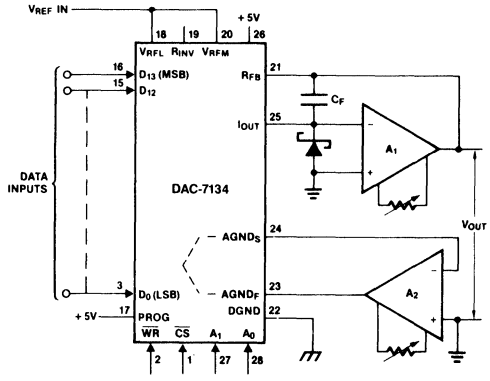


Figure 6. Unipolar Binary Operation with Forced Ground

BIPOLAR (2's COMPLEMENT) OPERATION

Figure 7 shows a circuit configuration for bipolar mode operation using a DAC-7134B. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. Table 5 lists the digital input codes and their respective analog output values for bipolar mode operation.

Amplifier A2, together with internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the DAC-7134B's feedback resistance switches to 2R under PROM control.

The resultant bipolar output range is $+V_{REF}$ to $-(V_{REF} + 1\ LSB)$. Again, the grounding arrangement of Figure 6 can be used.

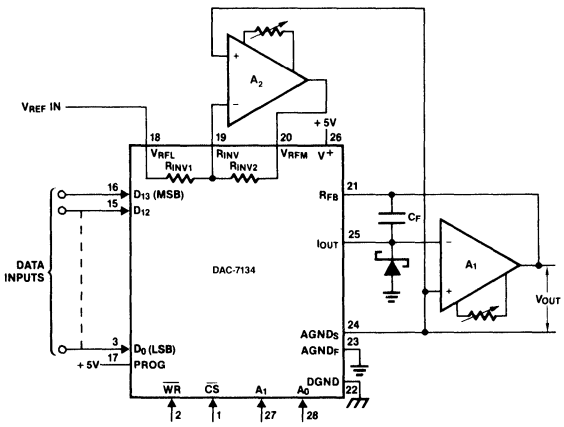


Figure 7. Bipolar (2's Complement), Four-Quadrant Multiplying Circuit

Table 5. Code Table—Bipolar (2's complement) Operation

DIGITAL INPUT MSB ..... LSB	ANALOG OUTPUT $+V_{REF}$	ANALOG OUTPUT $-V_{REF}$
011 111	$+V_{REF}$—1LSB	$-V_{REF}$ + 1LSB
010 000	0.5($+V_{REF}$)	0.5($-V_{REF}$)
000 000	0	0
110 000	0.5($-V_{REF}$)	0.5($+V_{REF}$)
100 000	$-V_{REF}$	$+V_{REF}$

Offset Adjustment
(See Figure 7)

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND. (Connect pins 1 through 16, 27, and 28 to pin 22).
2. Set data to 00000 . . . . 00. Adjust the offset zero adjust trim-pot of output op-amp A1 for a maximum of 0V ±50μV dc V_{OUT}.
3. Connect D_{13} (MSB, pin 16) data input to V^+ (pin 26).
4. Adjust the offset zero-adjust trim-pot of op-amp A2 for a maximum of 0V ±50uV dc at the R_{INV} terminal (pin 19).

Gain Adjustment (Optional)

1. Connect $\overline{CS}$, $\overline{WR}$, A_1 and A_0 (pins 1, 2, 27, and 28 respectively) to DGND (pin 22).
2. Connect D_0 through D_{12} (pins 3 through 15) to V^+ (pin 26). Connect D_{13} (MSB, pin 16) to DGND (pin 22).
3. Monitor V_{OUT} for a $-V_{REF}$ + 1LSB reading.
4. To increase V_{OUT}, connect a series resistor of 200 ohms or less between op-amp A1's output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT}, connect a series resistor of 100 ohms or less between the reference voltage and the V_{RFL} terminal (pin 18).

APPLICATIONS

General Recommendations

Ground Loops

Careful consideration must be given to ground loops in any system with 14-bit accuracy. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, and $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point. Thus, output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

Power Supplies

The V^+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum digital input voltage allowed is V^+, which therefore must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V^+ for proper operation.

Operational Amplifier Selection

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus, output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than 25μV) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10Vdc range also requires that the output amplifier has a high open loop gain (A_{VOL} > 400k for effective input offset less than 25μV).

The reference inverting amplifier used in the biopolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than 50μV), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the analog ground line (op-amp A_2 in Figure 6). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than 50μV).

The op-amp requirements can be readily met using an AM-7650 chopper stabilized device. For faster settling time, DATEL's AM-460 or AM-462 can be used with an AM-7650 providing automatic offset null.

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trimpots should be selected.

PACKAGE DIMENSIONS

The DAC-7134B and DAC-1734U differ only in the programming instructions. Therefore, the same package dimensions, as shown in Figure 8, apply to both model numbers. The device is available only in a standard 28-pin CERDIP package.

PACKAGE DIMENSIONS All dimensions in inches (millimeters)

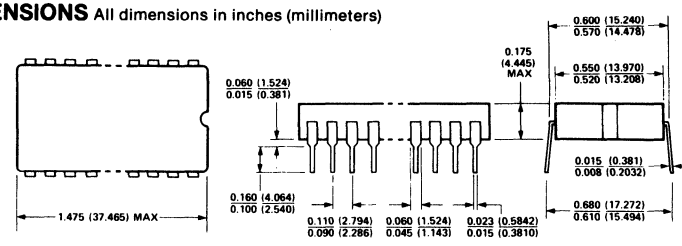


Figure 8. 28-Pin CERDIP Package Dimensions

ORDERING INFORMATION

DAC-7134

- J = 12-Bit Linearity (0.01% FSR)
- K = 13-Bit Linearity (0.006% FSR)
- L = 14-Bit Linearity (0.003% FSR)

- B = Bipolar Version
- U = Unipolar Version

DAC-7523, DAC-7533, DAC-7541
Monolithic 8-, 10-, and 12-Bit Multiplying D/A Converters

FEATURES

- **8-, 10-, and 12-Bit resolution**
- **150 Nanoseconds settling time — DAC-7523**
- **4-Quadrant multiplication**
- **Low gain and linearity tempco's**
- **Single supply operation**
- **DTL/TTL/CMOS-compatible**
- **Industry standard pin-out**

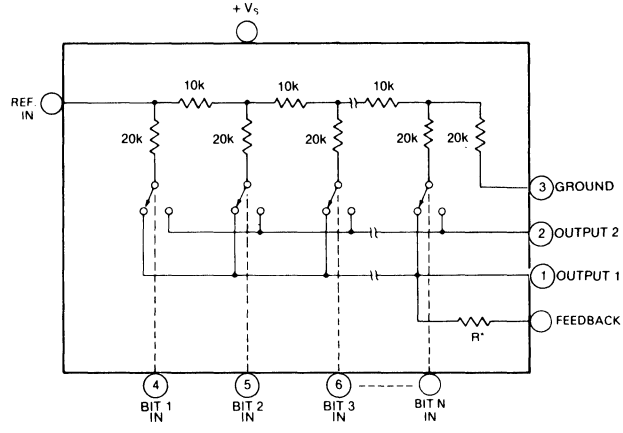
DESCRIPTION

DATEL'S DAC-7523, DAC-7533 and DAC-7541 are monolithic 8-, 10-, and 12-bit multiplying digital-to-analog converters. These devices use advanced thin-film-on-CMOS technology to fabricate a highly stable thin-film R-2R resistor ladder network and NMOS SPDT switches. CMOS level shifters provide low power DTL/ TTL/CMOS compatible operation. All that is required for most voltage output applications are an external voltage or current reference and output operational amplifier. All models are capable of four quadrant multiplication and the inputs are fully static protected.

Important features include a settling time for the DAC-7523, DAC-7533 and DAC-7541 of 150 nanoseconds, 600 nanoseconds and 1 microsecond respectively to ± ½ LSB maximum. Maximum linearity error tempco is 2 ppm/°C and feedthrough error is ± ½ LSB maximum. Power supply rejection is as low as 0.005% of FSR/%. The devices require only a single supply for operation. Power supply range is +5V dc to +15V dc.

The combination of low cost, four quadrant multiplication, full input protection and low power dissipation make these devices an ideal choice for many applications including digitally controlled gain circuits, attenuators, CRT character generation, programmable power supplies, motor speed controls and low noise audio gain control circuits.

The DAC-7523 and DAC-7533 are packaged in 16-pin plastic cases with the DAC-7541 being packaged in an 18 pin plastic case. All models are specified for operation over the commercial, 0°C to +70°C temperature range.



INPUT/OUTPUT CONNECTIONS

DAC-7523

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 (MSB)
5	BIT 2
6	BIT 3
7	BIT 4
8	BIT 5
9	BIT 6
10	BIT 7
11	BIT 8 (LSB)
12	N.C.
13	N.C.
14	V_S
15	REFERENCE IN
16	FEEDBACK

DAC-7533

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 (MSB)
5	BIT 2
6	BIT 3
7	BIT 4
8	BIT 5
9	BIT 6
10	BIT 7
11	BIT 8
12	BIT 9
13	BIT 10 (LSB)
14	V_S
15	REFERENCE IN
16	FEEDBACK

DAC-7541

PIN	FUNCTION
1	OUTPUT 1
2	OUTPUT 2
3	GROUND
4	BIT 1 (MSB)
5	BIT 2
6	BIT 3
7	BIT 4
8	BIT 5
9	BIT 6
10	BIT 7
11	BIT 8
12	BIT 9
13	BIT 10
14	BIT 11
15	BIT 12 (LSB)
16	V_S
17	REFERENCE IN
18	FEEDBACK

ABSOLUTE MAXIMUM RATINGS	DAC-7523	DAC-7533	DAC-7541
Supply Voltage, (V_S)	*	+17V	*
Logic Input Voltage Range	*	V_S to GND	*
Reference Input Voltage Range	*	±25V	*
Output Voltage Compliance	−0.3V to V_S	−0.3V to V_S	−100mV to V_S

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +15V Supply, +10V Reference unless otherwise noted.

INPUTS	DAC-7523	DAC-7533	DAC-7541
Resolution	8 Bits	10 Bits	12 Bits
Coding, Unipolar Operation	*	Straight Binary	*
Coding, Bipolar Operation	*	Offset Binary	*
Logic Threshold, Bit ON ("1"), min.	*	2.4V	*
Logic Threshold, Bit OFF ("0"), max.	*	0.8V	*
Logic Input Current, max.[1]	*	±1μA	*
Input Capacitance, max.	*	4 pF	*
Reference Input Voltage Range	*	±10V	*
Reference Input Resistance[2]	*	10 kΩ	*
OUTPUTS			
Output Voltage Compliance	*	−100 mV to V_S	*
Output Capacitance, output 1, max.[3]	100 pF	100 pF	100 pF
Output Capacitance, output 2, max.[3]	30 pF	35 pF	60 pF
Output Capacitance, output 1, max.[4]	30 pF	35 pF	60 pF
Output Capacitance, output 2, max.[4]	100 pF	100 pF	200 pF
PERFORMANCE			
Non Linearity, max.[5]	*	±½ LSB	*
Non Linearity Tempco, max.[5]	*	2 ppm/°C	*
Gain Error, max.[5]	±1.5% of FSR	±1.4% of FSR	±0.3% of FSR
Gain Error Tempco, max.[6]	10 ppm FSR/°C	15 ppm FSR/°C	15 ppm FSR/°C
Output Leakage Current, max.[7]	*	±50 nA	*
Output Current Settling Time, max.[8]	150 nsec.	600 nsec.	1 μsec.
Feedthrough Error, max.[9]	*	±½ LSB	*
Power Supply Rejection	0.02% FSR/%	0.005% FSR/%	0.01% FSR/%
POWER REQUIREMENTS			
Power Supply Voltage Range	*	+5V to +16V	*
Power Supply Current, max.	100 μA	2 mA	2 mA
PHYSICAL/ENVIRONMENTAL			
Operating Temp. Range	*	0°C to +70°C	*
Storage Temp. Range	*	−65°C to +150°C	*
Package Type, Plastic	16-Pin DIP	16-Pin DIP	18-Pin DIP

*Same specification as listed for DAC-7533

FOOTNOTES:

1. For input voltage = 0V or +15V.
2. All digital inputs tied high, OUTPUT 1 tied to ground.
3. All digital inputs high.
4. All digital inputs low.
5. Using internal feedback resistor.
6. Using internal feedback resistor. Specification for DAC-7523 only is maximum.
7. Accuracy not guaranteed unless outputs at ground potential.
8. Either output. Specified to ±½ LSB for a full scale change. Load resistance = 100Ω
9. Reference voltage = ±10V, 200 kHz for DAC-7523, 100 kHz for DAC-7533, and 10 kHz for DAC-7541. All digital inputs low.

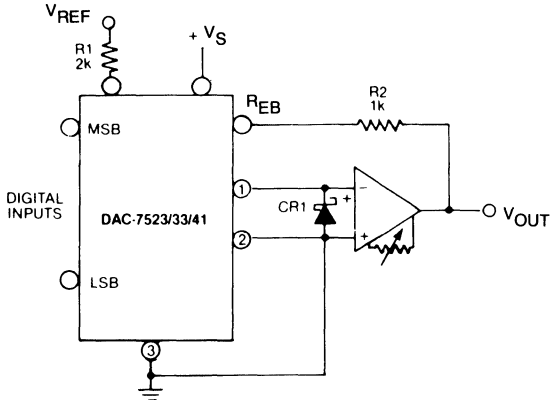
TECHNICAL NOTES

1. The digital control inputs are zener protected, however, permanent damage may occur to unconnected units under high electrostatic fields. All unused devices should be kept in conductive foam at all times.

   Unused digital inputs must be connected to V_S or ground for proper operation of the device. Voltages higher than V_S or less than ground should not be applied to any terminal except V_{ref} or damage may occur.
2. Static performance of these devices depends on output 1 and output 2 (Pins 1 and 2) being exactly at ground potential (Pin 3).
3. The output amplifier should be selected to have a low input bias current (typically less than 75 nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than ±200 μV). A bias current compensation resistor in the output amplifier's non-inverting input (when used) can cause a variable offset. To prevent this, the non-inverting input should be connected directly to ground with a low resistance wire.
4. To prevent ground loop problems, connect all pins going to ground to a common point using separate connections.
5. The power supply used should have a low noise level and should not have any transients which exceed +17V.
6. If gain adjustment is required, low tempco (approximately 50 ppm/°C) resistors or trim-pots should be selected.

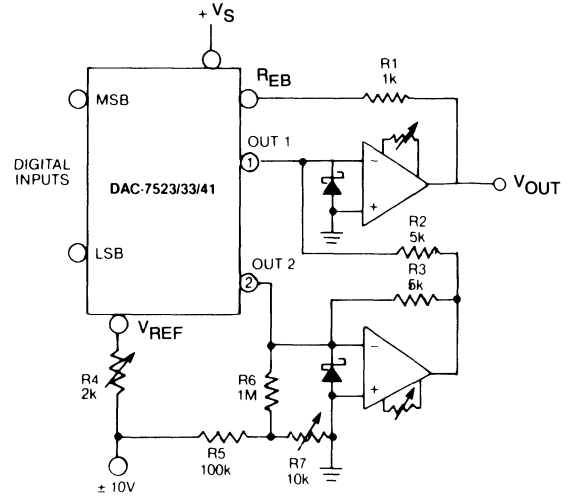
CODING AND CALIBRATION

CONNECTION-UNIPOLAR MODE



NOTES: Do not use R1 and R2 if gain adjustment is not required.
CR1 (HP5082-2811 or euivalent) protects the D/A from negative transients and is necessary only with certain high speed amplifiers.

CONNECTION—BIPOLAR MODE



NOTES: R5, R6 and R7 are used to adjust Vout = 0v at input 1000.
Do not use R1 and R4 if gain adjust is not required.
R2 and R3 should be 0.01% low-TCR resistors.

CALIBRATION

UNIPOLAR MODE

ZERO ADJUST — Set all digital inputs to logic low and adjust the zero adjust trimpot of the output operational amplifier to 0V.

GAIN ADJUST — Set all digital inputs to logic high and adjust R1 and R2 for an output equal to: Vout = Vref (N-1)/N, where "N" equals: 256 (DAC-7523), 1024 (DAC-7533), 4096 (DAC-7541).

BIPOLAR MODE

OFFSET ADJUST — Set all digital inputs to logic high and adjust the output of A2 (with A2 offset adjust trimpot) for 0V. Set MSB "Bit 1" high and all others low and adjust the output of A1 (with A1 offset adjust trimpot) for 0V. Adjust R7 for 0V at Vout.

GAIN ADJUST — Set all digital input's to logic high and adjust Vout for: Vout = Vref (N-X)/X using R1 and R4. Where "N" = 255 (DAC-7523), 1023 (DAC-7533) or 4095 (DAC-7541); and "X" = 128 (DAC-7523), 512 (DAC-7533) or 2048 (DAC-7541).

CODING TABLES

UNIPOLAR CODING TABLE

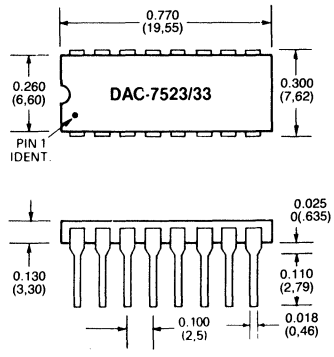
INPUT CODE MSB LSB	ANALOG OUTPUT
111 111	$-V_{REF}$ + 1 LSB
110 000	$-0.75\ (V_{REF})$
100 000	$-0.5\ (V_{REF})$
010 000	$-0.25\ (V_{REF})$
000 000	0V

BIPOLAR CODING TABLE

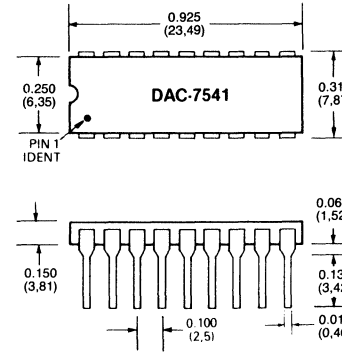
INPUT CODE MSB LSB	ANALOG OUTPUT
111 111	$-V_{REF}$ + 1 LSB
110 000	$-0.5\ (V_{REF})$
100 000	0
010 000	$+0.5\ (V_{REF})$
000 000	V_{REF}

MECHANICAL DIMENSIONS
INCHES (mm)

16-PIN DIP CERAMIC PACKAGE

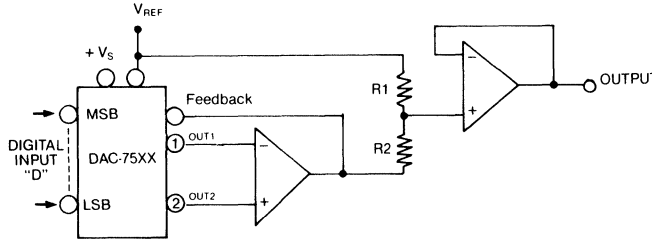


18-PIN DIP CERAMIC PACKAGE



TYPICAL CONNECTION AND APPLICATION

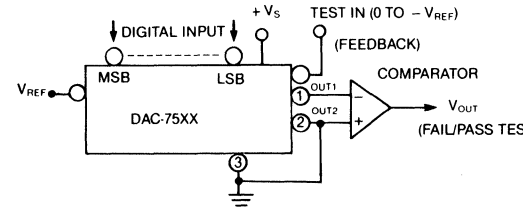
MODIFIED SCALE FACTOR AND OFFSET



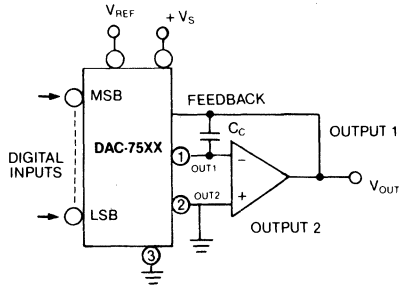
$$OUTPUT = V_{REF}\left|\left(\frac{R2}{R1+R2}\right) - \left(\frac{R1 \times D}{R1+R2}\right)\right|$$

$$WHERE: D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ N}{2^N}$$

DIGITALLY CONTROLLED LIMIT DETECTOR



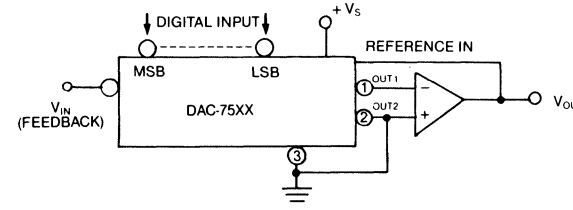
TYPICAL CONNECTION WITH COMPENSATION CAPACITOR



The output amplifier should be selected carefully in order to maintain the dynamic performance of the D/A. In low speed or static applications, AC specifications of the op-amp are not critical. However, in high speed applications slew-rate, settling time, open loop gain and gain/phase margin specifications should be selected for the desired performance.

A compensation capacitor C_C should be used when a high speed operational amplifier is used on the output.

DIGITALLY CONTROLLED GAIN



$$V_{OUT} = V_{IN}/D$$

WHERE:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ N}{2^N}$$

ORDERING INFORMATION

MODEL NO.	RESOLUTION
DAC-7523	8 Bits
DAC-7533	10 Bits
DAC-7541	12 Bits

DAC-8308
Ultra-Fast 8-Bit Composite Video D/A

FEATURES

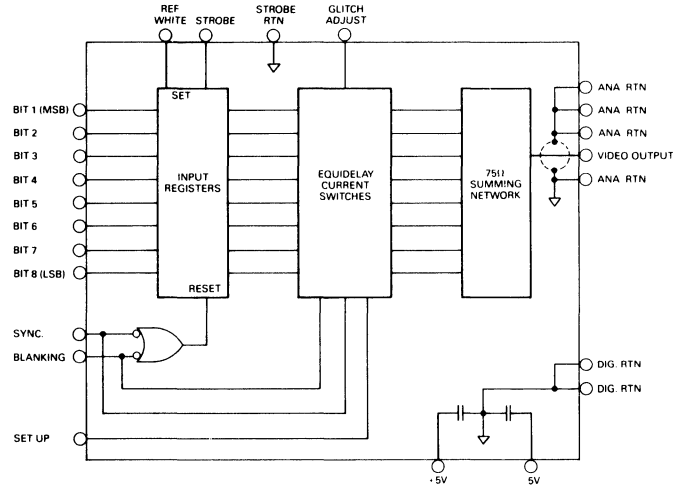
- **40 MHz update rate**
- **Composite synchronization and blanking**
- **No deglitching required**
- **Direct drive to 75 Ω load**
- **Adjustable setup**
- **0°C to +70°C operation**

GENERAL DESCRIPTION

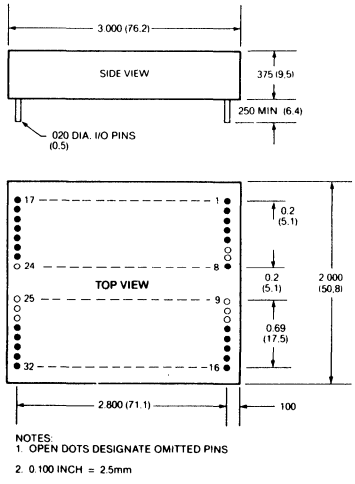
DATEL's DAC-8308 is a high performance, ultra-fast, 8-bit digital-to-analog converter. Functionally complete, including an internal input register, equidelay current switches and a high speed 75 Ω summation network; these devices are specifically designed for video and graphic display applications.

The DAC-8308 accepts 8 bits at throughput rates up to 40 MHz and produces a composite video output signal with 256 gray levels, including setup, blanking and sync., all derived from separate digital inputs. The output will directly drive a terminated 75 ohm coaxial cable giving a 0 to −1.054V output that is in general conformance with EIA standards RS170 and RS343A. Models with a "B" suffix have the output voltage offset by +392 mV so that an input code of 0111 1111 (the middle of the gray scale) produces an output of approximately 0V. Output steps are so clean that deglitching is not required.

The DAC-8308 is packaged in 2 × 3 × 0.375 inch cases, allowing ½ inch board spacing and operates over the 0°C to +70°C temperature range. Digital inputs are TTL compatible and power requirement is ±5V. These devices are an excellent choice for applications involving raster scan high resolution video (both color and monochrome), graphic display systems, function generation and time base correction.



MECHANICAL DIMENSIONS INCHES (MM)



NOTES:
1. OPEN DOTS DESIGNATE OMITTED PINS
2. 0.100 INCH = 2.5mm

INPUT/OUTPUT CONNECTIONS

DAC-8308

PIN	FUNCTION
1	ANALOG RETURN
2	ANALOG RETURN
3	ANALOG RETURN
4	VIDEO OUT
5	ANALOG RETURN
8	SETUP
12	STROBE RETURN
13	STROBE
14	SYNC.
15	PEAK WHITE
16	BLANKING
17	−5V POWER IN
18	DIGITAL RETURN
19	DIGITAL RETURN
20	+5V POWER IN
21	BIT 1 (MSB) INPUT
22	BIT 2 INPUT
23	BIT 3 INPUT
24	BIT 4 INPUT
28	GLITCH ADJUST
29	BIT 5 INPUT
30	BIT 6 INPUT
31	BIT 7 INPUT
32	BIT 8 (LSB) INPUT

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±5V supplies unless otherwise noted.

OUTPUT CHARACTERISTICS

Output Voltage Range[1]	0V to −1V ±5% into 75 Ω termination.
Output Current	−28 mA short circuit, −14 mA into 75 Ω.
Recommended Load Impedance	75 Ω ±5%, dc to 10 MHz.
Source (Thevenin) Impedance	75 Ω ±5%, dc to 50 MHz.
Output Bandwidth minimum	100 MHz at −3 dB.
LSB Size; DAC-8308	2.52 mV nominal.
Rise and Fall Time, 10% to 90%	3 nsec. typical, 4 nsec. maximum.
Full Step Settling Time, to 1 LSB	7.5 nsec.
Glitch Settling Time, to 1 LSB[2]	5 nsec.
Glitch Area; DAC-8308	70 pV-sec. maximum, 50 pV-sec. typical.

TRANSFER CHARACTERISTICS

Resolution	8 bits, 256 levels.
Coding[3]	Binary.
Differential Linearity, maximum	±½ LSB.
Monotonicity	Guaranteed, 10°C to 70°C.
Offset[4]	±½ LSB maximum, 0°C to 70°C.
Transfer Gain (Slope) Tempco, maximum	±0.02%/°C.
Propagation Delay	10 nsec. typical, strobe to output, 50% points.

INPUT CHARACTERISTICS

Update Rate	40 MHz.
Input Register[5]	8 ECL Type D Flip-Flops
Strobe Input	Data entered on positive-going edge (timing reference).
Setup, minimum	7.0 nsec. before strobe.
Hold, minimum	6.0 nsec.
Logic Levels	Standard 7400 TTL Levels.
Data Input Loading (Each of 8 Inputs)	Two-unit load.
Strobe Input Loading	Two-unit load.
Control Input Loading, maximum	2 units each line.

POWER SUPPLY REQUIREMENTS

Supply Voltage	+5V and −5V, nominal.
Positive Supply: DAC-8308	5.0V ±5% at 50 mA.
Negative Supply	−4.75V to −5.5V at 400 mA.
Supply Regulation	Negative supply should not have more than 5 mV peak-to-peak ripple.
Supply Common	Digital Return is the common for the +5V and −5V supplies.

ENVIRONMENTAL AND PACKAGING

Operating Temp. Range	0°C to +70°C.
Storage Temp.	−25°C to +85°C.
Relative Humidity	0 to 100%, non-condensing.
Mechanical Dimensions	2″ x 3″ x 0.375″ (50 x 75 x 10 mm).

FOOTNOTES:

1. The output of the DAC-8308 will be 0 to −1.054V.
2. For worst case (MSB) transition.
3. DAC-8308: 1111 1111 input code produces −71 mV
   0000 0000 input code produces −714 mV with standard setup
   —see "Video Characteristics".
4. DAC-8308—dc output with peak white input
5. Includes built-in TTL to ECL translaters in data input lines and strobe.

VIDEO CHARACTERISTICS; DAC-8308

Typical at +25°C, ±5V supplies unless otherwise noted.

Composite Video Signal	Consists of 256 gray levels plus Peak or 110% white, blanking level and sync level.
Gray Scale Range	0.643V peak-to-peak.
Step Size	2.52 mV step.
Peak White Level	0V, absolute; +0.768V (110 IRE Units) relative to blanking level with standard Setup; +0.714V relative to Reference Black, +0.071V (10 IRE units) relative to Reference White.
Input Code for White Level	11111111.
Peak White Control	Logic "0" (TTL) on Peak White line overrides video input data and drives the output to 0V.
Reference Black Level	−0.714V absolute; +54 mV (7.5 IRE Units) relative to blanking level with standard Setup.
Input Code for Reference Black Level	00000000.
Composite Blanking Level	−0.768V absolute, with standard Setup.
Input Command for Blanking/ Pedestal Level	Logic "0" (TTL) on "Blanking" line simultaneously resets input register to 00000000.
Composite Sync Level	−1.054V absolute with standard Setup; −0.286V (−40 IRE Units) with respect to blanking level (back porch).
Input Command for Sync Level	Logic "0" (TTL) on "Sync" line simultaneously resets input register to 00000000.
Sync and Blanking Rise and Fall Times, maximum	100 nanoseconds.
Sync and Blanking Overshoot, maximum	2%.
Setup (Reference Black-to-Blanking)	Externally programmable from 0 mV (0 IRE Units) to 142 mV (20 IRE Units).
Setup Control Line	Input ground: Standard 54 mV (7.5 IRE Units) Input Open: 71 mV (10 IRE Units) Setup. Input tied to −5V: 142 mV (20 IRE Units). Input tied to +5V: 0 mV (0 IRE Units).

TECHNICAL NOTES

1. The DAC-8308 has three additional current switches in the equi-delay bank: One to inject the Blanking level and one for the Synchronizing level, as required to generate a composite video signal. The Setup Control provides a means for varying brightness in reproducible steps. TV monitors cut off the picture tube in response to the Blanking level, producing the blackest possible visible picture. The Setup control varies the offset between Reference Black level and Blanking level which produces an apparent shift in the "brightness" of Reference Black.

   The Blanking and Sync. control lines are asynchronous. The DAC output goes to the command level in about 12 nanoseconds. 12 nanoseconds after removal, the DAC output goes to Reference Black until the next strobe command.

   The DAC-8308 has additional user flexibility, achieved by the addition of a Peak White control. Assertion of this input drives the output to its most positive voltage: The whiter than white level, or 110% white to be used for cursors etc.

   Peak White sets the input register which turns off the eight gray scale current switches, and the third additional current switch. The Sync or Blanking inputs reset the input register, producing full scale output from the gray scale current

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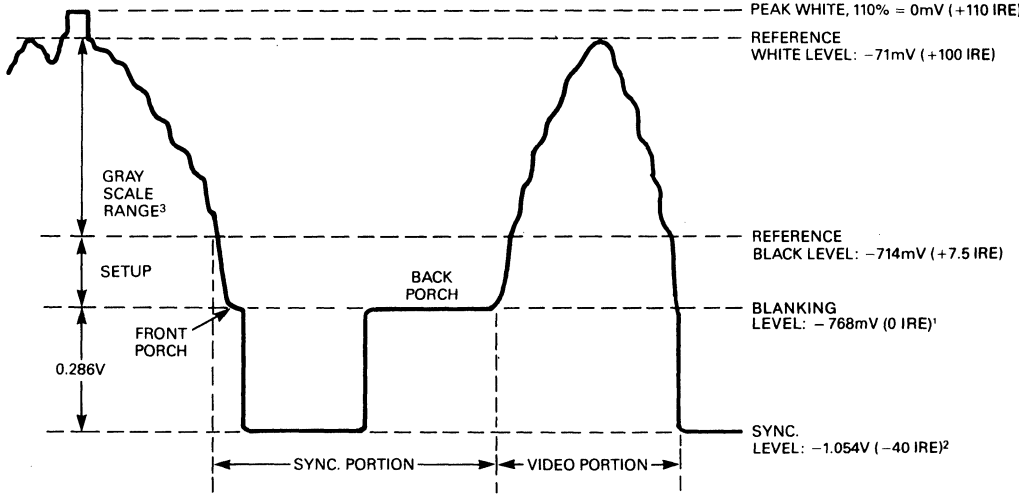
switches; the output from the Sync. or Blanking current switches is added to the full scale output. Obviously, Peak White should not be activated during the Sync. or Blanking intervals.

2. The DAC-8308 is capable of operation from a negative supply voltage between −4.75V to −5.5V. The output amplitudes specified are nominal values set by internal reference. However, if user adjustment is required, the glitch area will vary slightly as a function of the negative supply voltage. The factory trim is carried out at −5.0V, connect a 10K potentiometer to the Glitch Adjust Terminal. Adjust this pot for minimum glitch area at the major carry transition. This pot may be omitted and the Glitch Adjust Terminal left open.
3. EIA Industrial Electronics Tentative Standard No. 1 which will, in the future, become a part of RS170-A, details the exact waveform and timing characteristics of the composite video signal at the output of a color television studio.

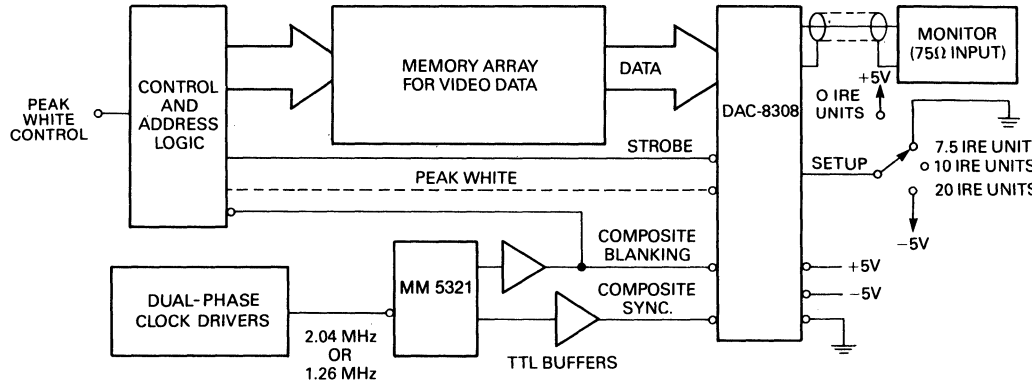
   The products described in this data sheet are in general conformance with such needs. Exact compliance requires additional circuitry which would, at a minimum, provide Sin X/X correction and bandwidth filtering.
4. The output bandwidth may be reduced, if desired, by adding a small capacitor across the DAC output. This will result in slower rise times. The absolute glitch amplitude will decrease, but the energy (or net area) of the glitch will be unchanged.
5. The DIG RTN, ANA RTN and STROBE RTN terminals are all tied together internally. The +5V and −5V supply common should be connected to DIG RTN. If a long printed circuit wiring connection is required for integration of the DAC into a video system, stripline wiring techniques may be implemented by taking advantage of the physical arrangement of the output terminals i.e., the ANA RTN terminals are located on each side of the VIDEO OUT terminal. ANA RTN normally connects to the shield of an external 75 ohm coaxial cable. STROBE RTN is included as a convenience and may be used optionally to facilitate connection.
6. The sync and blanking outputs of the MM5320 TV Timing ROM may not be capable of driving the DAC-8308 series, under worst case conditions, without the use of a logic driver.
7. All timing is referenced to the positive edge of the strobe. Setup and Hold require 7.0 nanoseconds and 6.0 nanoseconds, respectively.

2

COMPOSITE VIDEO OUTPUT (NOT TO SCALE)



1. For Standard −7.5 IRE Setup. For −10 IRE Setup = −785 mV, −20 IRE = −857 mV.
2. For Standard −7.5 IRE Setup with Blanking present during Sync time.
   For −10 IRE Setup = 1.071V, −20 IRE = −1.143V.
   0 IRE Setup or with Blanking not present during Sync = −1.000V
3. Gray Scale: LSB = 2.52 mV = 0.363 IRE
   MSB = 321 mV = 46.43 IRE



TYPICAL SMALL DISPLAY SYSTEM

With this circuit, digital video data, digital sync. and digital blanking are converted directly to a composite monitor input. Analog mixing and/or generation of the sync/blanking is not required, nor is a separate high power driver amplifier required ahead of the monitor. With the inherently low glitch of the DAC-8308, a deglitcher is not required and video data need not be "aligned" to achieve low glitch performance.

GLOSSARY OF VIDEO TERMS

COMPOSITE VIDEO SIGNAL
The combined video signal, with or without Setup, plus the Sync signal.

VIDEO SIGNAL
The visually perceived portion of the composite video signal which varies in gray scale levels from Reference White to Reference Black. Also known as the picture signal.

SYNC OR COMPOSITE SYNC SIGNAL
That portion of the composite video signal which synchronizes the scanning process.

SYNC LEVEL
The level of the peak of the Sync signal.

SETUP
The difference in level between the Reference Black level and the Blanking level. Not to be confused with setup as used in conjunction with digital logic.

RASTER-SCAN
The basic method of sweeping across a CRT, a line at a time, to generate and display pictures such as used in commercial TV in the USA.

MONOCHROME VIDEO
Conventional black-and-white television video in which the Z-axis, or intensity, of the beam is modified during scanning to shade and/or outline images.

BLANKING LEVEL
The level which separates the Sync portion from the video signal, with or without Setup. This level is sometimes also called the pedestal, back porch or front porch. It usually refers to the level which will cut off the TV tube, producing the blackest possible visual picture.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

PEAK WHITE LEVEL
A "Whiter than White" Level not within the range of the normal picture. Sometimes used for generating cursors or outlines because it contrasts with all gray shades including white.

GRAY SCALE
The discrete levels for the video signal between Reference White and Reference Black levels.

COLOR VIDEO (RGB)
As used herein, this refers to the method of generating color images by combining the three primary colors of red-green-blue (RGB). The associated monitor would be identified as an "RGB" monitor. Three DAC-8308 series D/A converters are required to drive such a monitor, one each for red, green and blue.

ORDERING INFORMATION

MODEL NO.	OUTPUT
DAC-8308	Unipolar

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FEATURES

- **8-, 10-, 12-Bit resolution**
- **Settling times to 25 nanoseconds**
- **20 ppm/°C tempco**
- **Unipolar or bipolar operation**
- **Current output**
- **Internal feedback resistor**

GENERAL DESCRIPTION

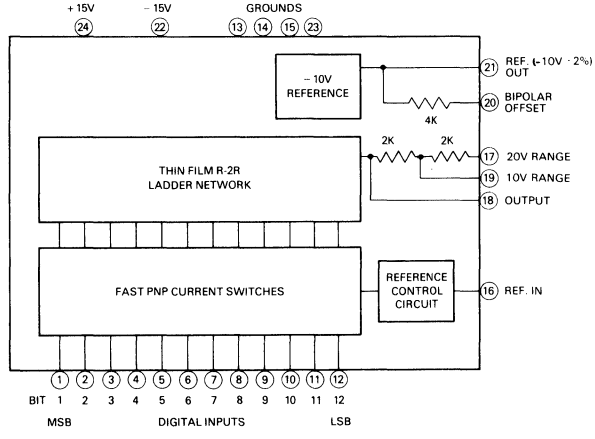
The DAC-HF Series of hybrid DAC's are ultra high-speed, current output devices. They incorporate state-of-the-art performance in a miniature package, achieving maximum output settling times of 25 nanoseconds for the 8- and 10-bit models and 50 nanoseconds for the 12-bit model. They can be used to drive a resistor load directly for up to ±1V output or a fast operational amplifier (such as DATEL's AM-500) for higher voltage outputs with sub-microsecond settling times. A tapped feedback resistor and a bipolar offset resistor are included internally to give five programmable output voltage ranges with an external operational amplifier.

The DAC-HF design combines proven hybrid production techniques with advanced circuit design to realize high speed current switching. The design incorporates fast PNP current switches driving a low impedance R-2R thin-film ladder network. The nichrome thin-film resistor network is deposited by electron beam evaporation on a low capacitance substrate to assure high-speed performance. The resistors are then functionally trimmed by laser for optimum linearity.

The digital inputs are TTL-compatible and use straight binary coding for unipolar operation and offset binary coding for bipolar operation. Output current is 0 to +5 mA for unipolar operation and ±2.5 mA for bipolar operation into an output amplifier summing junction. Linearity is ±1 LSB, and the converters are monotonic over the operating temperature range specified for each. Gain temperature coefficient is ±20 ppm/°C maximum.

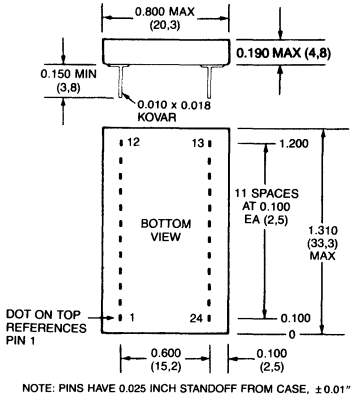
Applications for the DAC-HF series include high-speed function generators, fast computer control systems, graphic display systems, and CRT displays.

Power supply requirements is ±15V dc with less than 780 milliwatts consumption. The DAC-HF is available in models covering three operating temperature ranges.



NOTE: FOR DAC-HF10B PINS 11 & 12 ARE NO CONNECTION
FOR DAC-HF8B PINS 9, 10, 11 & 12 ARE NO CONNECTION

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	GROUND
2	BIT 2 IN	14	GROUND
3	BIT 3 IN	15	GROUND
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	20 V RANGE
6	BIT 6 IN	18	OUTPUT
7	BIT 7 IN	19	10 V RANGE
8	BIT 8 IN	20	BIPOLAR OFFSET
9	BIT 9 IN	21	REF. OUT
10	BIT 10 IN	22	-15 VDC
11	BIT 11 IN	23	GROUND
12	BIT 12 IN (LSB)	24	+15 VDC

ABSOLUTE MAXIMUM RATINGS, ALL MODELS

Positive Supply, Pin 24 ..... +18V
Negative Supply, Pin 22 ..... −18V
Digital Input Voltage, Pins 1 to 12 .. +15V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies unless otherwise specified.

DESCRIPTION	8B	10B	12B
INPUTS			
Resolution, Bits	8	10	12
Coding, Unipolar Output	Straight Binary		
Coding, Bipolar Output	Offset Binary		
Input Logic Level, Bit ON ("1")	+2.0 to +5.5V at +40μA		
Input Logic Level, Bit OFF ("0")	0V to +0.8V at 2.6 mA		
OUTPUTS			
Output Current Range, Unipolar	0 to +5 mA		
Output Current Range, Bipolar	±2.5 mA		
Output Voltage Compliance	±1.2V		
Output Voltage Ranges[2]	0 to −5V 0 to −10V ±2.5V ±5V ±10V		
Output Resistance	400 ohms		
Output Capacitance	15 pF		
Output Leakage Current, All Bits OFF	15 nA		
PERFORMANCE			
Linearity Error, max	0.012%		
TMIN to TMAX	0.024%		
Differential Linearity Error, Max	0.012%		
TMIN to TMAX	0.024%		
Monotonicity	Guaranteed over oper. temp. range		
Gain Tempco, max.	±20 ppm/°C		
Offset Tempco, Bipolar, max.	±10 ppm/°C of F.S.R.[3]		
Zero Tempco, max.	±1.5 ppm/°C of F.S.R.[3]		
Settling Time, nsec. max.[1]	25	25	50
Power Supply Sensitivity	0.01%/% Supply		
POWER REQUIREMENTS			
Supply Voltage	±15V dc ±0.5V		
Positive Quiescent Current, max.	35mA	40mA	45mA
Negative Quiescent Current, max.	15mA	15mA	15mA
PHYSICAL/ENVIRONMENTAL			
Operating Temperature Range	0°C to +70°C (BMC) −55°C to +125°C (BMM)		
Storage Temperature Range	−65°C to +150°C		
Package Type	24-Pin Ceramic DIP		
Pins	0.010 x 0.018 inch Kovar		
Weight	0.2 oz (6g.)		

FOOTNOTES:

1. Full scale current change to 1 LSB with 400Ω load.
2. With External Operational Amplifier.
3. F.S.R. is Full Scale Range, or the difference between minimum and maximum output values.

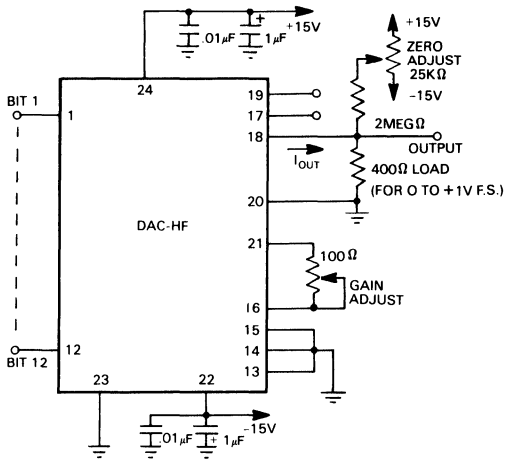
TECHNICAL NOTES

1. Proper operation of the DAC-HF series converters is dependent on good board layout and connection practices. Bypass supplies as shown in the connection diagrams. Mount bypass capacitors close to the converter, directly to the supply pins where possible.
2. Use of a ground plane is particularly important in high speed D to A converters as it reduces high frequency noise and aids in decoupling the digital inputs from the analog output. Avoid ground loop problems by connecting all grounds on the board to the ground plane. The remainder of the ground plane should include as much of the circuit board as possible.
3. When the converter is configured for voltage output with an external operational amplifier, keep the leads from the converter to the ouptut amplifier as short as possible.
4. The high speed current switching technique used in the DAC-HF series inherently reduces the amplitude and duration of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011 ... 1 to 100 ... 0 or vice versa. At this time, a skewing of the input codes can create a transition state code of 111 ... 1. The duration of the "transition state code" is dependent on the degree of skewing but its effect is dependent on the speed of the DAC (an ultra-fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC). Minimize the effects of input skewing by using a high-speed input register to match input switching times. The input register recommended for use with the DAC-HF is easily implemented with two Texas Instruments SN74S174 hex D-type flip-flops. This register will reduce glitches to a very low level and ensure fast output settling times.
5. Test the DAC-HF using a low capacitance test probe (such as a 10X probe). Take care to assure the shortest possible connection between probe ground and circuit ground. Long probe ground leads may pick up environmental E.M.I. causing artifacts on the scope display, i.e., signals that do not originate at the unit under test.
6. Passive components used with the DAC-HF may be as indicated here: 0.1 μF and 1 μF bypass capacitors should be ceramic type and tantalum type respectively; the 400Ω output load is a 0.1% 10 ppm/°C metal film type; adjustment potentiometers are ceremet types: other resistors may be ±10% carbon composition types.
7. Output voltage compliance is ±1.2V to preserve the linearity of the converter. In the bipolar mode, the DAC-HF can be operated with no load to give an output voltage of ±1.0V. In the unipolar mode, the load resistance must be less than 600Ω to give less than +1.2V output. The specified output currents of 0 to +5 mA and ±2.5 mA are measured into a short circuit or an operational amplifier summing junction.

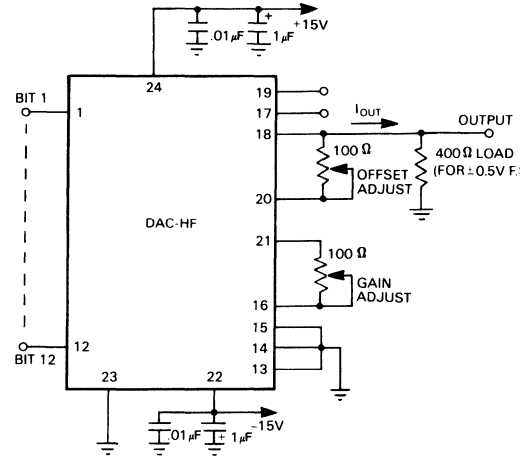
DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

CONNECTION AND CALIBRATION

UNIPOLAR CURRENT OUTPUT CONNECTIONS



BIPOLAR CURRENT OUTPUT CONNECTIONS



UNIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs low and adjust the ZERO ADJUST potentiometer for a reading of 0V at the output.
3. Set all inputs high and adjust the GAIN ADJUST potentiometer for a reading of −F.S. +1 LSB (given in the coding table for 12-bit units).

BIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs low and adjust the OFFSET ADJUST potentiometer for an output reading of +F.S., (given in the coding table for 12-bit units).
3. Set all inputs high and adjust the GAIN ADJUST potentiometer for an output reading of −F.S. +1 LSB, (given in the coding table for 12-bit units).

CODING TABLES UNIPOLAR OUTPUT

UNIPOLAR SCALE	INPUT CODING STRAIGHT BINARY	ANALOG OUTPUT 0 to +1V F.S.	0 to −5V F.S	0 to −10V F.S
−F.S. +1 LSB	1111 1111 1111	+0.9998V	−4.9988V	−9.9976V
−¾ F.S.	1100 0000 0000	+0.7500V	−3.7500V	−7.5000V
−½ F.S.	1000 0000 0000	+0.5000V	−2.5000V	−5.0000V
−¼ F.S.	0100 0000 0000	+0.2500V	−1.2500V	−2.5000V
−1 LSB	0000 0000 0001	+0.0002V	−0.0012V	−0.0024V
0	0000 0000 0000	+0.0000V	+0.0000V	0.0000V

BIPOLAR OUTPUT

BIPOLAR SCALE	INPUT CODING OFFSET BINARY	ANALOG OUTPUT ±0.5V F.S.	±2.5V F.S.	±5V F.S.	±10V F.S.
−F.S. +1LSB	1111 1111 1111	+0.4998V	−2.4988V	−4.9976V	−9.9951V
−½ F.S.	1100 0000 0000	+0.1250V	−1.2500V	−2.5000V	−5.0000V
−1 LSB	1000 0000 0001	+0.0002V	−0.0012V	−0.0024V	−0.0049V
0	1000 0000 0000	0.0000V	0.0000V	0.0000V	0.0000V
+½ F.S.	0100 0000 0000	−0.1250V	+1.2500V	+2.500V	+5.0000V
+F.S. −1LSB	0000 0000 0001	−0.4998V	+2.4988V	+4.9976V	+9.9951V
+F.S.	0000 0000 0000	−0.5000V	+2.5000V	+5.0000V	+10.0000V

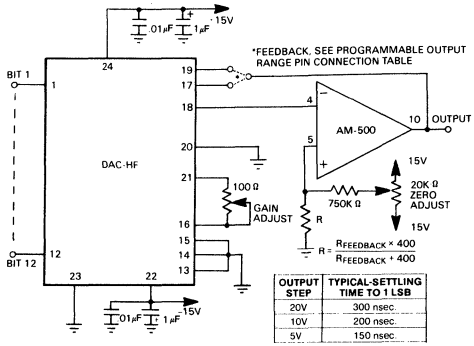
PROGRAMMABLE OUTPUT RANGE PIN CONNECTIONS

OUTPUT VOLTAGE RANGE	FEEDBACK CONNECTION	CONNECT THESE PINS TOGETHER
0 to −5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
0 to −10V	PIN 19	PIN 20 to PIN 23
±2.5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 18
±5V	PIN 19	PIN 20 to PIN 18
±10V	PIN 17	PIN 20 to PIN 18

In all programmable output ranges pin 18 connects to external operational amplifier inverting input

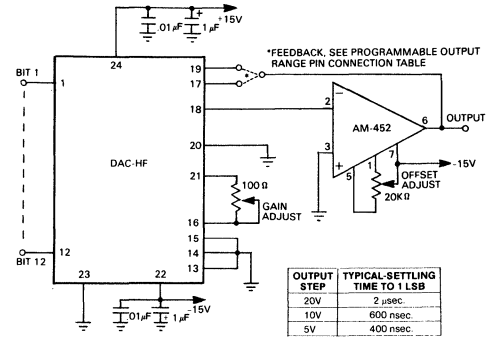
APPLICATIONS

UNIPOLAR ULTRA-FAST VOLTAGE OUTPUT



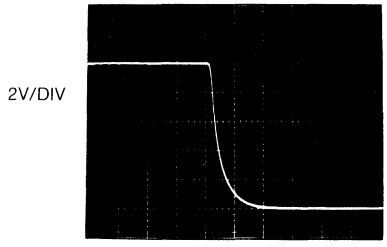
OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	300 nsec.
10V	200 nsec.
5V	150 nsec.

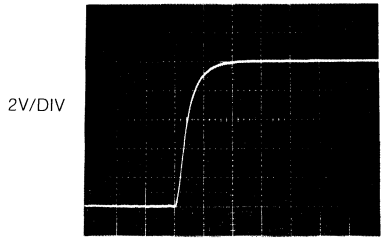
UNIPOLAR FAST VOLTAGE OUTPUT CIRCUIT



OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	2 μsec.
10V	600 nsec.
5V	400 nsec.

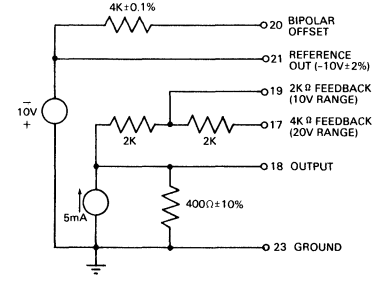
VOLTAGE OUTPUT WAVEFORMS



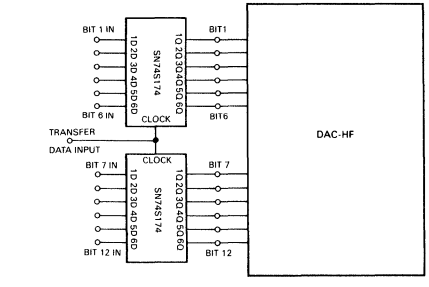


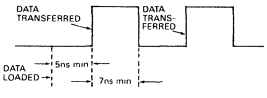
DAC-HF with AM-500, ±5V output full scale (10V) step

EQUIVALENT OUTPUT CIRCUIT



HIGH SPEED INPUT REGISTER





ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
DAC-HF8BMC	0°C to + 70°C	Hermetic
DAC-HF8BMM	−55°C to +125°C	Hermetic
DAC-HF10BMC	0°C to + 70°C	Hermetic
DAC-HF10BMM	−55°C to +125°C	Hermetic
DAC-HF12BMC	0°C to + 70°C	Hermetic
DAC-HF12BMM	−55°C to +125°C	Hermetic

ACCESSORIES

Parts Number	Description
DILS-3	Mating Socket (24-pin socket)
TP-100 or TP25K	Trimming Potentiometers

For high reliability versions of the DAC-HF series including units screened to MIL-STD-883 Level B, contact factory.

DAC-HK Series
12-Bit Hybrid DAC's with Input Register

FEATURES

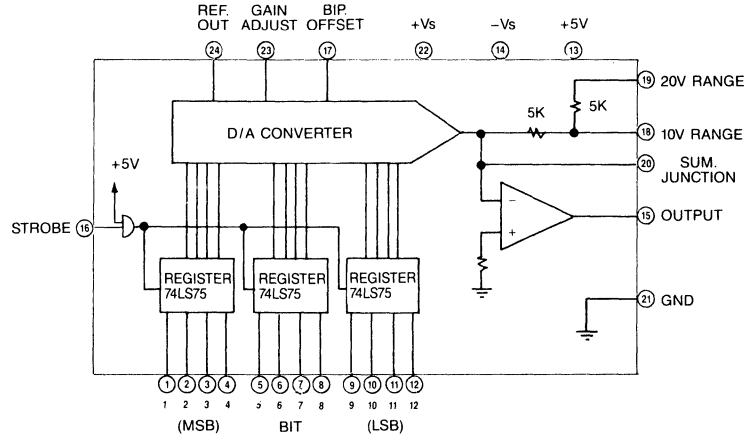
- **12-Bit resolution**
- **20 ppm/°C Tempco**
- **Input register**
- **2 Coding options**
- **Fast settling time**

GENERAL DESCRIPTION

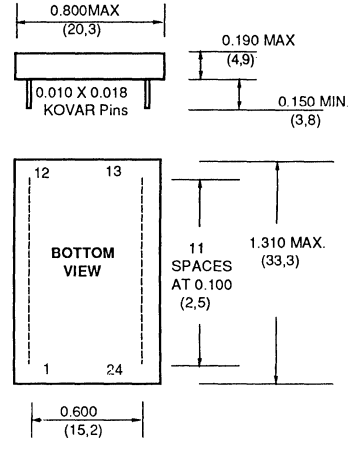
The DAC-HK series hybrid D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high, data in the storage register is held and when the load input is low, data is transferred through to the DAC. There are two basic models available by coding option: binary, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5V, 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V.

The DAC-HK Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of 2 ppm/°C maximum. The temperature coefficient of gain is 20 ppm/°C maximum and tempco of zero is ±3 ppm/°C maximum.

The converters are cased in 24-pin ceramic packages. Models are available for operating temperature ranges of 0 to +70, and −55 to +125°C. Power requirement is ±15V dc and +5V dc. Total power dissipation is 700 milliwatts.



MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	+5 VDC
2	BIT 2 IN	14	−15 VDC
3	BIT 3 IN	15	OUTPUT
4	BIT 4 IN	16	LOAD
5	BIT 5 IN	17	BIPOLAR OFF.
6	BIT 6 IN	18	10 V RANGE
7	BIT 7 IN	19	20 V RANGE
8	BIT 8 IN	20	SUM. JUNCTION
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15 VDC
11	BIT 11 IN	23	GAIN ADJ.
12	BIT 12 IN (LSB)	24	REF. OUT

ABSOLUTE MAXIMUM RATINGS	DAC-HK12B
Positive Supply, pin 22	+18V
Negative Supply, pin 14	−18V
Logic Supply, pin 13	+5.25V
Digital Input Voltage, pins 1-12 & 16	+5.5V
Output Current, pin 15	±20 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	
Resolution	12 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary Two's Complement[1]
Input Logic Level, bit ON ("1")	+2.0V to +5.5V
Input Logic Level, bit OFF ("0")	0V to +0.8V
Logic Loading	1 LSTTL load
Load Input[2]	High ("1") = hold data Low ("0") = transfer data
Load Input Loading	3 LSTTL loads

OUTPUT	
Output Voltage Ranges[3], unipolar	0 to +10V
Output Voltage Ranges[3], bipolar	±2.5V ±5V ±10V
Output Current	±5 mA min.
Output Impedance	0.05 ohm

PERFORMANCE	
Linearity Error, max.	±½ LSB
Differential Linearity Error, max.	±¾ LSB
Gain Error, before trimming	±0.1%
Zero Error, before trimming	±0.05%
Gain Tempco, max.	±20 ppm/°C
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR
Diff. Linearity Error Tempco, max.	±2 ppm/°C of FSR
Monotonicity	Guaranteed over oper. temp. range
Settling Time, 5V change	3 µsec.
Settling Time, 10V change	3 µsec.
Settling Time, 20V change	4 µsec.
Settling Time, 1 LSB change	800 nsec.
Slew Rate	20V/µsec.
Power Supply Rejection	±0.002% FSR/%

POWER REQUIREMENTS	
Power Supply Voltage	+15V dc ±0.5V dc at 10 mA −15V dc ±0.5V dc at 25 mA +5V dc ±0.25V dc at 35 mA ±12V dc, +5V operation[4]

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BGC, BMC) −55°C to +125°C (BMM)
Storage Temperature Range	−65°C to +125°C
Package Type	24-pin Ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

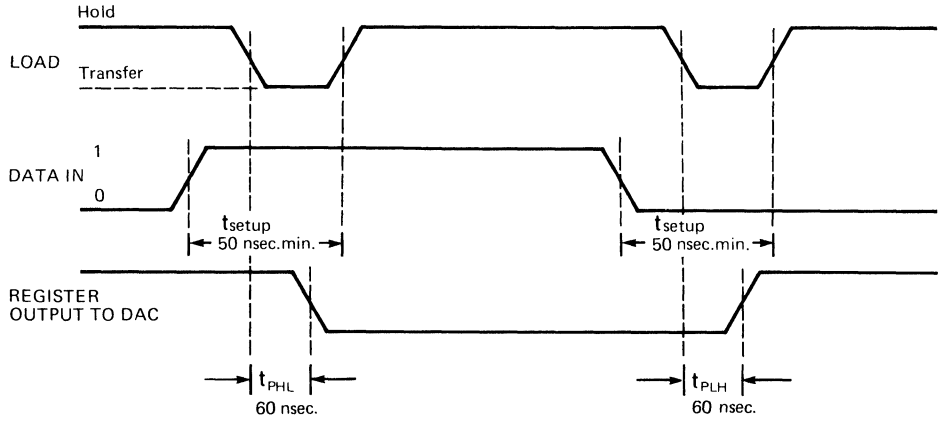
FOOTNOTES:

1. For two's complement coding order the model described under ordering information.
2. Logic levels are the same as for data inputs.
3. By external pin connection.
4. For ±12V dc, +5V dc operation, contact factory.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1 µF (tantalum type) at the +15, −15, and +5V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments these capacitors should be shunted with 0.01 µF ceramic capacitors.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level triggered input which causes the register to hold data with a high input and transfer data to the DAC with a low input.
4. A setup time of 50 nanoseconds minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. The external gain adjustment shown in the Connection Diagrams has a range of ±0.2% of full scale. If a wider range is desired the 2.8 Megohm resistor can be decreased slightly in value. The full-scale output is typically accurate within ±0.1% with no adjustment. The zero, or offset, adjustment has a range of ±0.35% of FS.
6. If the reference output terminal (pin 24) is used, an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10 µA in order not to affect the T.C. of the reference.

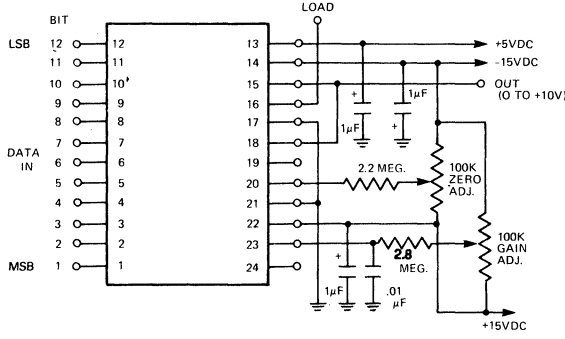
TIMING DIAGRAM



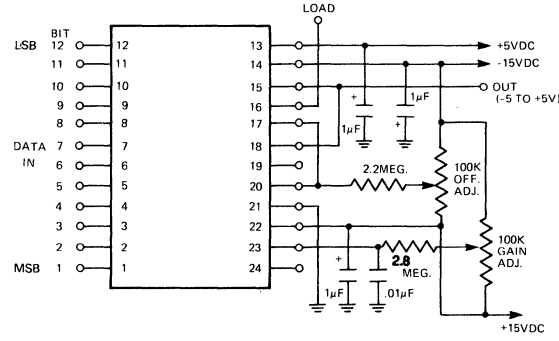
All rise and fall times ≤10 nsec.

CONNECTION DIAGRAMS

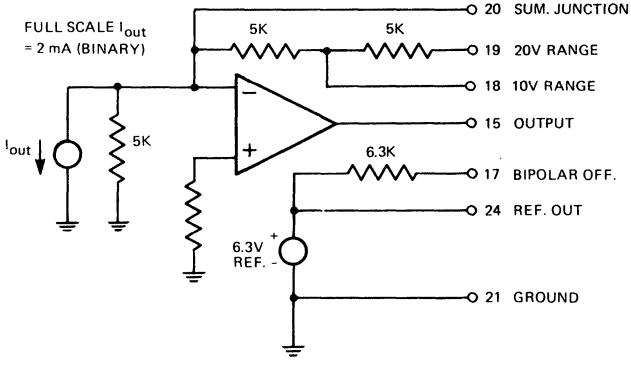
UNIPOLAR OPERATION (0 to +10V)



BIPOLAR OPERATION (±5 V)



OUTPUT CIRCUIT



OUTPUT RANGE SELECTION

RANGE	CONNECT THESE PINS TOGETHER		
±10 V	15 & 19	17 & 20	
±5 V	15 & 18	17 & 20	
±2.5 V	15 & 18	17 & 20	19 & 20
+10 V	15 & 18	17 & 21	
+5 V	15 & 18	17 & 21	19 & 20

CODING TABLES

UNIPOLAR OPERATION

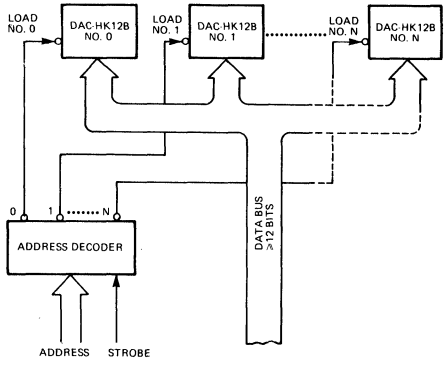
STRAIGHT BINARY	OUTPUT RANGES	
MSB LSB	0 to +10V	0 to +5V
1111 1111 1111	+9.9976	+4.9988
1100 0000 0000	+7.5000	+3.7500
1000 0000 0000	+5.0000	+2.5000
0100 0000 0000	+2.5000	+1.2500
0000 0000 0001	+0.0024	+0.0012
0000 0000 0000	0.0000	0.0000

BIPOLAR OPERATION

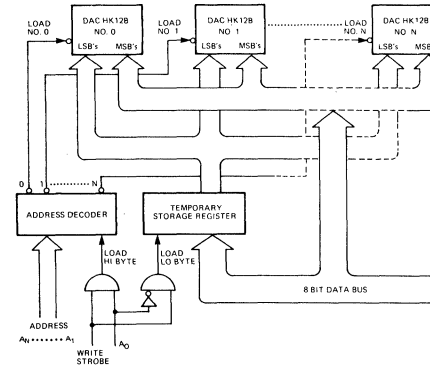
OFFSET BINARY	TWO's COMPLEMENT	OUTPUT RANGES		
MSB LSB	MSB LSB	±10V	±5V	±2.5V
1111 1111 1111	0111 1111 1111	+9.9951	+4.9976	+2.4988
1100 0000 0000	0100 0000 0000	+5.0000	+2.5000	+1.2500
1000 0000 0000	0000 0000 0000	0.0000	0.0000	0.0000
0100 0000 0000	1100 0000 0000	−5.0000	−2.5000	−1.2500
0000 0000 0001	1000 0000 0001	−9.9951	−4.9976	−2.4988
0000 0000 0000	1000 0000 0000	−10.0000	−5.0000	−2.5000

APPLICATIONS

INTERFACING TO ≥ 12 BIT DATA BUS



INTERFACING TO 8 BIT DATA BUS



CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter up as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) and adjust the GAIN ADJ. potentiometer to give the full-scale output voltage shown in the Coding Table.

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full-scale output voltage shown in the Coding Table.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or a 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full-scale output voltage shown in the Coding Table.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
Binary Coding		
DAC-HK12BGC	0°C to +70°C	Epoxy
DAC-HK12BMC	0°C to +70°C	Herm.
DAC-HK12BMM	−55°C to +125°C	Herm.
2's Complement Coding		
DAC-HK12BGC-2	0°C to +70°C	Epoxy
DAC-HK12BMC-2	0°C to +70°C	Herm.
DAC-HK12BMM-2	−55°C to +125°C	Herm.

ACCESSORIES

Part Number	Description
DILS-3	24-pin Mating Socket
TP100K	Trimming Potentiometer

For military devices compliant to MIL-STD-883, contact DATEL.

DAC-HP16B
16-Bit, Micro-electronic Digital-to-Analog Converter

FEATURES

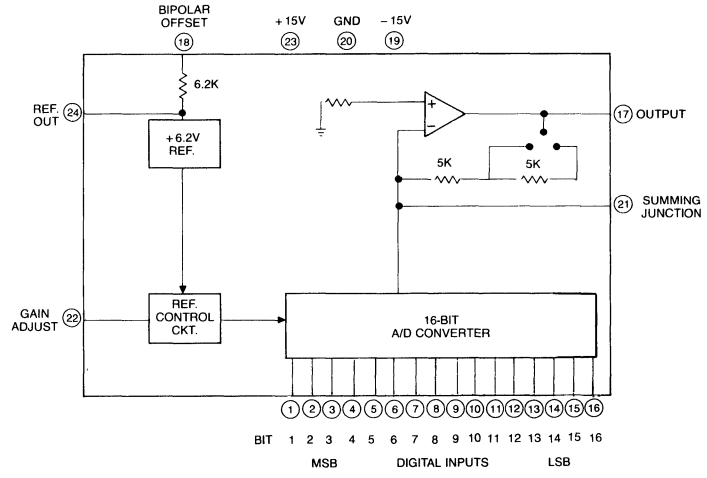
- **16-Bit binary model**
- **Voltage outputs**
- **15 ppm/°C Maximum gain tempco**
- **Linearity to ±0.003%**

GENERAL DESCRIPTION

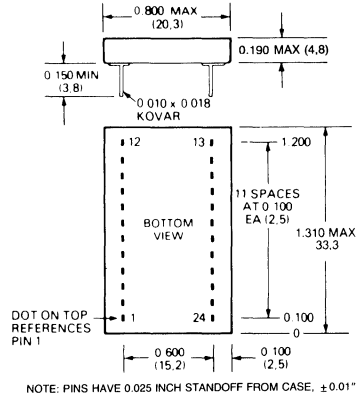
The DAC-HP series are high resolution hybrid D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24-pin double spaced ceramic DIP package. The DAC-HP16B has 16-bit binary resolution with ±0.003% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B. This device operates in both unipolar and bipolar modes with output voltages of 0 to +10V dc and ±5V dc respectively. Binary versions with a bipolar output voltage range of ±10V dc are available, denoted by the suffix "–1" after the model designation.

The DAC-HP design incorporates both thin- and thick-film hybrid technology. The design includes an on-board amplifier and precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of 2 ppm/°C maximum. The temperature coefficient of gain is 15 ppm/°C maximum and tempco of zero is ±5 ppm/°C maximum.

The resolution, stability and voltage output of these converters make them ideal for precision applications such as speech and waveform reconstruction, precision ramp generators, and computer controlled testing. They are available in operating temperature ranges 0 to +70°C and –55° to +125°C. Power requirement is ±15V dc.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	BIT 13 IN
2	BIT 2 IN	14	BIT 14 IN
3	BIT 3 IN	15	BIT 15 IN
4	BIT 4 IN	16	BIT 16 IN (LSB)
5	BIT 5 IN	17	OUTPUT
6	BIT 6 IN	18	BIPOLAR OFF
7	BIT 7 IN	19	–15VDC
8	BIT 8 IN	20	GROUND
9	BIT 9 IN	21	SUM JUNCTION
10	BIT 10 IN	22	GAIN ADJ
11	BIT 11 IN	23	+15VDC
12	BIT 12 IN	24	REF OUT

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, pin 23	+18V
Negative Supply, pin 19	−18V
Digital Input Voltage, pins 1-16	+5.5V
Output Current, pin 17	±20 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, and ±15V supplies unless otherwise noted.

INPUTS	
Resolution	16 bits
Coding, unipolar output	Comp. Binary
Coding, bipolar output	Comp. Off. Binary
Input Logic Level, bit ON ("0")[1]	0V to +0.8V at −1 mA
Input Logic Level, bit OFF ("1")[1]	+2.4V to +5.5V at +40 μA
Logic Loading	1 TTL load

OUTPUTS	
Output Voltage Range, Unipolar[2]	0 to +10V
Output Voltage Range, Bipolar	±5V
Output Voltage Range, "−1" Suffix	±10V
Output Current, min.[6]	±5 mA
Output Impedance	0.05 ohm

PERFORMANCE	
Linearity Error, max.	±0.003%
Monotonicity, 10°C to 40°C	14 bits
Gain Error, before trimming	±0.1%
Zero Error, before trimming	±0.1%
Gain Tempco, max.[3]	±15 ppm/°C
Gain Tempco, max. BGC	±20 ppm/°C
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR[4]
Offset Tempco, bipolar, max.	±8 ppm/°C of FSR[4]
Differential Linearity Tempco, max.	±2 ppm/°C of FSR[4]
Settling Time, 10V change[5]	15 μsec.
Slew Rate	20V/μsec.
Power Supply Rejection	±0.002% FSR/%

POWER REQUIREMENTS	
(Quiescent, all bits high)	+15V dc, ±0.5V dc at 20 mA −15V dc, ±0.5V dc at 25 mA ±12V dc operation[7]

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BMC, BGC) −55°C to +125°C (BMM)
Storage Temperature Range	−65°C to +150°C
Package Type	24 pin ceramic
Pins	0.010 x 0.018 inch diameter Kovar
Weight	0.2 ounces (6 grams)

FOOTNOTES:

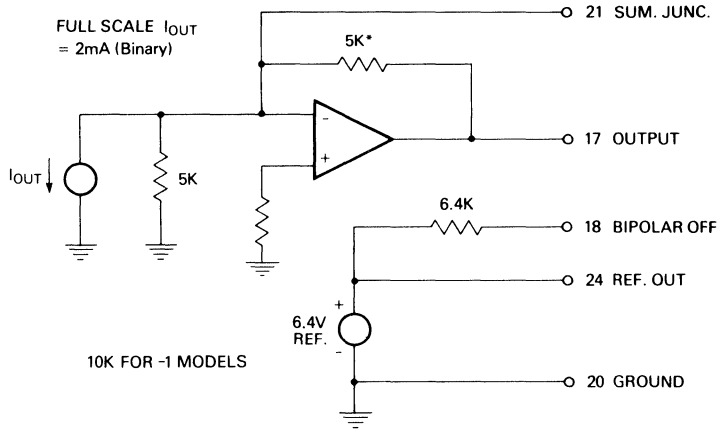
1. Drive from TTL output with only the DAC-HP as load.
2. Unipolar output range for suffix "−1" models, 0 to +10V, is reached at ½ scale input.
3. For all models except DAC-HP16BGC.
4. FSR is 0 to +FS or −FS to +FS voltage.
5. To 0.005% FSR.
6. Pin 17.
7. For ±12V dc operation, consult factory.

TECHNICAL NOTES

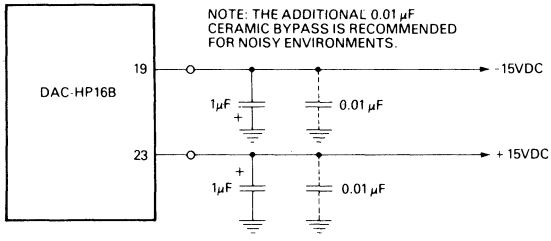
1. It is recommended that these converters be operated with local supply bypass capacitors of 1 μF (tantalum type) at the +15V and −15V supply pins. The capacitors should be connected as close to the pins as possible. In high frequency noise environments an additional 0.01 μF ceramic capacitor should be used in parallel with each tantalum bypass.
2. When laying out the circuit board for this device, isolate the analog, digital, and power grounds as much as possible from each other before joining them at pin 20.
3. The external gain adjustment shown in the diagrams gives an adjustment of ±0.2% of full-scale range. The converters are internally trimmed to ±0.1% at full scale. A wider range of adjustment may be achieved by decreasing the value of the 510 kohm resistor.
4. The zero adjustment, or offset adjustment, has an adjustment range of ±0.35% of full-scale range. The unipolar zero is internally set to zero within ±0.1% of full-scale range.
5. If the reference output (pin 24) is used, it must be buffered by an operational amplifier in the noninverting mode. Current drawn from pin 24 should be limited to ±10 μA in order that the temperature coefficient of the reference circuit not be affected. This is sufficient current for the bias current of most of the popular operational amplifier types.

APPLICATION

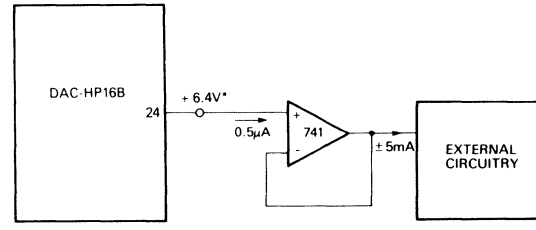
OUTPUT CIRCUIT



POWER SUPPLY BYPASSING

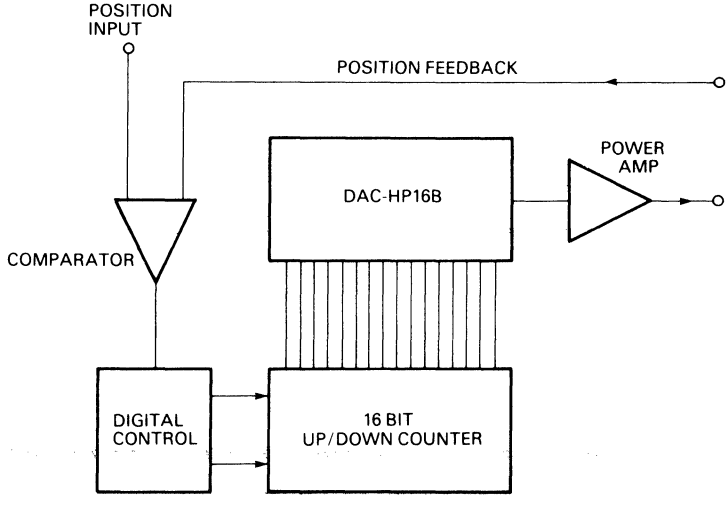


USE OF REFERENCE OUTPUT



*MAXIMUM OUTPUT
CURRENT IS ± 10µA

PRECISION INDUSTRIAL POSITION CONTROLLER



CONNECTION AND CALIBRATION

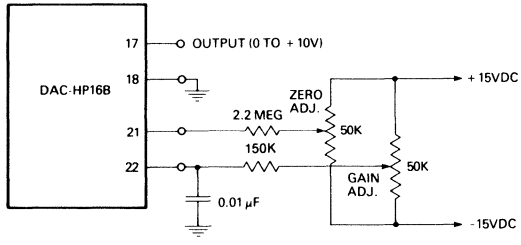
CODING TABLES
BIPOLAR OUTPUT — Complementary Offset Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE	OUTPUT VOLTAGE SUFFIX "–1" MODELS
0000 0000 0000 0000	+FS – 1 LSB	+4.99985V	+9.99969V
0011 1111 1111 1111	+½FS	+2.50000	+5.00000
0111 1111 1111 1111	0	0.00000	0.00000
1011 1111 1111 1111	–½FS	–2.50000	–5.00000
1111 1111 1111 1110	–FS + 1 LSB	–4.99985	–9.99969
1111 1111 1111 1111	–FS	–5.00000V	–10.00000V

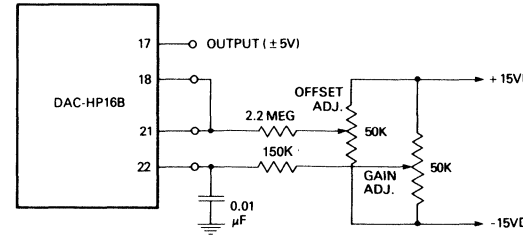
UNIPOLAR OUTPUT — Complementary Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0000 0000 0000 0000	+FS – 1 LSB	+9.99985V
0011 1111 1111 1111	+¾ FS	+7.50000
0111 1111 1111 1111	+½ FS	+5.00000
1011 1111 1111 1111	+¼ FS	+2.50000
1111 1111 1111 1110	+1 LSB	+153 μV
1111 1111 1111 1111	0	0

UNIPOLAR OPERATION



BIPOLAR OPERATION



CALIBRATION PROCEDURE

Connect the converter as shown in the application diagrams. For bipolar operation connect Bipolar Offset (pin 18) to Summing Junction (pin 21). For unipolar operation connect Bipolar Offset (pin 18) to Ground (pin 20). In making the following adjustments, refer to the coding tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 1111 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.00000V output.
2. **Gain Adjustment.** Set the input digital code to 0000 0000 0000 0000 (complementary binary) and adjust the GAIN ADJ. potentiometer to give +9.99985V output.

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the digital input code to 1111 1111 1111 1111 and adjust the OFFSET ADJ. potentiometer to give the –F.S. output shown in the coding table above for the model being calibrated.
2. **Gain Adjustment.** Set the digital input code to 0000 0000 0000 0000 and adjust the GAIN ADJ. potentiometer to give the +FS – 1 LSB output shown in the coding table above the model being calibrated.

ORDERING INFORMATION

MODEL NO.	OPERERATING TEMP. RANGE	SEAL
DAC-HP16BCG	0°C to +70°C	EPOXY
DAC-HP16BMC	0°C to +70°C	HERM.
DAC-HP16BMM	–55°C to +125°C	HERM.
DAC-HP16BMC-1	0°C to +70°C	HERM.
DAC-HP16BMM-1	–55°C to +125°C	HERM.

ACCESSORIES

Part Number	Description
DILS-3	Mating Socket (24-pin socket)
TP50K	Trimming Potentiometer

For military devices compliant to MIL-STD-883, consult the factory.

DAC-HZ Series
12-Bit Hybrid
Digital-to-Analog Converters

FEATURES

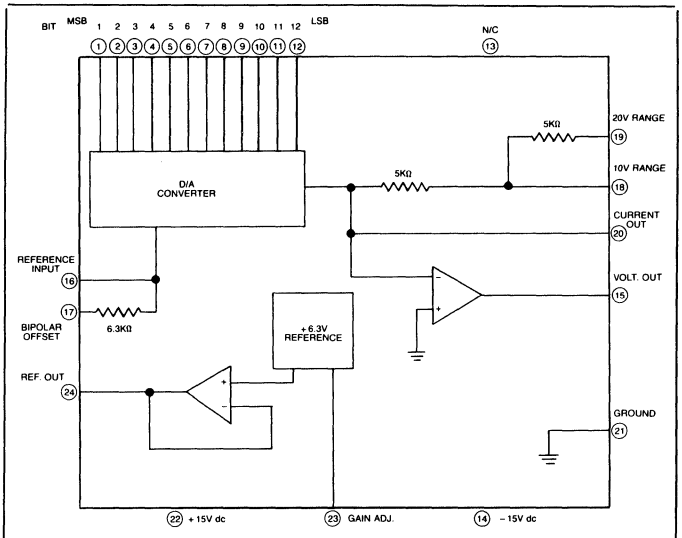
- **12-Bit binary**
- **5 Output ranges**
- **3 Microseconds settling time**
- **Internal reference and output amplifier**
- **High performance**

GENERAL DESCRIPTION

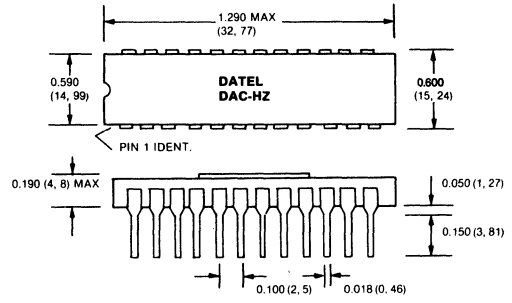
The DAC-HZ Series are high performance, hybrid 12-bit binary digital-to-analog converters. These converters are manufactured using thin- and thick-film technology. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin-programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to +5V dc, 0 to +10V dc, ±2.5V dc, ±5V dc, and ±10V dc. Current output is also provided.

The DAC-HZ Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of 2 ppm/°C maximum. The temperature coefficient of gain is 20 ppm/°C maximum and tempco of zero is ±3 ppm/°C maximum.

The DAC-HZ Series consists of 6 different models covering the operating temperature ranges of 0°C to +70°C, and −55°C to +125°C. The models come in a 24-pin ceramic package. Power requirement is ±15V dc with no 5V dc logic supply required. Input coding is complementary binary. Voltage output settling time is 3 microseconds to ½ LSB.



MECHANICAL DIMENSIONS
INCHES (MM)



ALL DIMENSIONS ARE IN INCHES (MM)

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN	7	BIT 7 IN	13	NO CONN.	19	20V RANGE
2	BIT 2 IN	8	BIT 8 IN	14	-15VDC	20	CURRENT OUT
3	BIT 3 IN	9	BIT 9 IN	15	VOLT. OUT	21	GROUND
4	BIT 4 IN	10	BIT 10 IN	16	REF. IN	22	+15VDC
5	BIT 5 IN	11	BIT 11 IN	17	BIPOLAR OFF.	23	GAIN ADJ.
6	BIT 6 IN	12	BIT 12 IN	18	10V RANGE	24	REF. OUT

FUNCTIONAL SPECIFICATIONS

Typical at 25°C and ±15V supplies unless otherwise noted.

INPUTS	DAC-HZ12B (Binary)	DAC-HZ12D (BCD)
Resolution	12 Binary bits	3 BCD Digits
Coding, unipolar output	Comp. Binary	Comp. BCD
Coding, bipolar output	Comp. Off. Binary	—
Input Logic Level, bit ON ("0")	0V to +0.8V at −1 mA	
Input Logic Level, bit OFF ("1")	+2.4V to +5.5V at +40 µA	
Logic Loading	1 TTL load	
OUTPUTS		
Output Current, unipolar	0 to −2 mA, ±20%	0 to −1.25 mA, ±10%
Output Current, bipolar	±1 mA, ±20%	—
Voltage Compliance, Iout	±2.5V	*
Output Impedance, Iout, unipolar	5 k ohms	*
Output Impedance, Iout, bipolar	2.8 k ohms	—
Output Voltage Ranges, unipolar	0V to + 5V 0V to + 10V	0 to + 2.5V 0 to +5V 0 to +10V
Output Voltage Ranges, bipolar	±2.5V ±5V ±10V	— — —
Output Current, Vout	±5 mA min.	*
Output Impedance, Vout	0.05 ohm	*
PERFORMANCE		
Voltage Output Nonlinearity	±½ LSB max.	±¼ LSB max.
Differential Nonlinearity	±¾ LSB max.	±¼ LSB max.
Gain Error, before trimming	±0.1% of FSR[1]	*
Zero Error, before trimming	±0.05% of FSR[1]	*
Gain Tempco, max.	±20 ppm/°C	*
Zero Tempco, unipolar, max.	±3 ppm/°C of FSR[1]	*
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR[1]	*
Diff. Nonlinearity Tempco, max.	±2 ppm/°C of FSR[1]	*
Monotonicity	Over oper. temp. range	*
Setting Time, Iout to ½ LSB[2]	300 nsec.	*
Settling Time, Vout to ½ LSB	3 µsec.[3]	*
Slew Rate	20V/µsec.	*
Power Supply Rejection	±0.002% FSR/% Supply[1]	*
POWER REQUIREMENTS		
Power Supply Voltage	+15V dc, ±0.5V dc at 10 mA −15V dc, ±0.5V dc at 16 mA ±12V dc operation[4]	
PHYSICAL/ENVIRONMENTAL		
Operating Temperature Ranges	0°C to +70°C and -55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Package Size	1.300 x 0.800 x 0.160 inches	
Package Type	24 Pin Ceramic DIP	
Pins	Kovar 0.010 x 0.018 inches	
Weight	0.22 ounces (63 grams)	

*Specifications same as first column

FOOTNOTES:

1. FSR is full scale range and is 10V for 0 to +10V or −5V to +5V output; 20V for ±10V output, etc.
2. Current output mode.
3. For 2.5k or 5k feedback. For 10k feedback the settling time is 4 microseconds.
4. For ±12V dc operation, contact factory.

TECHNICAL NOTES

1. The DAC-HZ12 series converters are designed and factory calibrated to give ±½ LSB linearity (binary version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be ±½ LSB everywhere over the full output range without any additional adjustments.
2. These converters must be operated with local supply by-pass capacitors from +15V to ground and −15V to ground. Tantalum type capacitors of 1 µF are recommended and should be mounted as close as possible to the converter. If the converters are used in a high frequency noise environment a 0.01 µF ceramic capacitor should be used across each tantalum capacitor.
3. When operating in the current output mode the equivalent internal current source of 2 mA must drive both the internal source resistances and the external load resistor. A 300 nanosecond output settling time is achieved for the voltage across a 100 ohm load resistor; for higher value resistors the settling time becomes longer due to the output capacitance of the converter. For fastest possible voltage output for a large transition, an external fast settling amplifier such as DATEL's AM-500 should be used in the inverting mode. Settling time of less than 1 microsecond can be achieved. See application diagram.

CALIBRATION PROCEDURE

1. Select the desired output range and connect the converter up as shown in the Output Range Selection table and the Standard Connection diagrams.
2. To calibrate, refer to the Coding Tables. Note that complementary coding is used.
3. **Zero and Offset Adjustments**
   For unipolar operation set all digital inputs to "1" (+2.0 to +5.5V) and adjust the ZERO ADJ. potentiometer for zero output voltage or current. For bipolar operation set all digital inputs to "1" and adjust the OFFSET ADJ. potentiometer for the negative full scale (for voltage out) or positive full scale (for current out) output value shown in the Coding Table.
4. **Gain Adjustment**
   Set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.

OUTPUT RANGE SELECTION

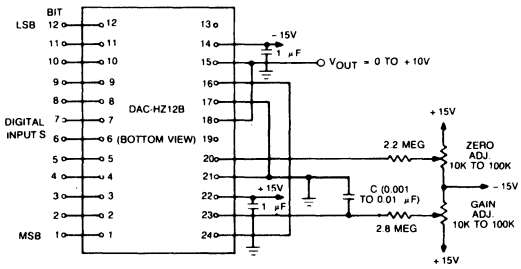
BIN. RANGE	CONNECT THESE PINS TOGETHER			
±10V	15 & 19	17 & 20	—	16 & 24
±5V	15 & 18	17 & 20	—	16 & 24
±2.5V	15 & 18	17 & 20	19 & 20	16 & 24
+10V	15 & 18	17 & 21	—	16 & 24
+5V	15 & 18	17 & 21	19 & 20	16 & 24
±1 mA	—	17 & 20	—	16 & 24
−2 mA	—	17 & 21	—	16 & 24

VOLTAGE OUTPUT IS AT PIN 15.
CURRENT OUTPUT IS AT PIN 20.

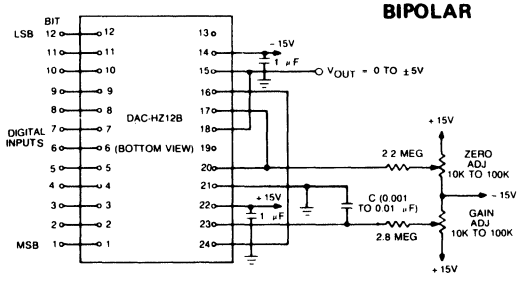
VOLTAGE OUTPUT CONNECTIONS

(FOR DIFFERENT OUTPUT SCALING REFER TO OUTPUT RANGE SELECTION TABLE)

UNIPOLAR

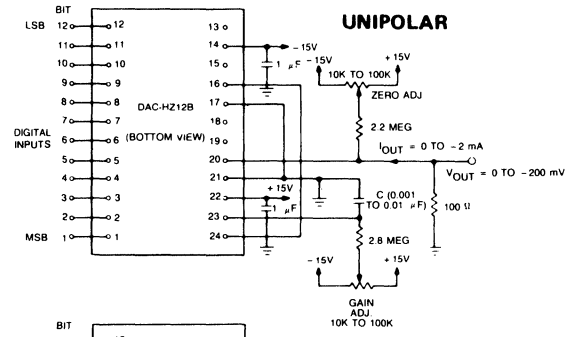


BIPOLAR

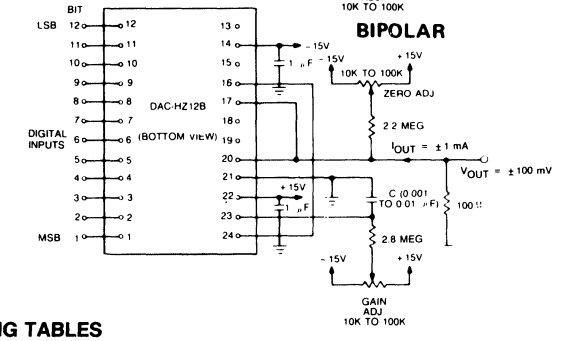


CURRENT OUTPUT CONNECTIONS

UNIPOLAR



BIPOLAR



CODING TABLES

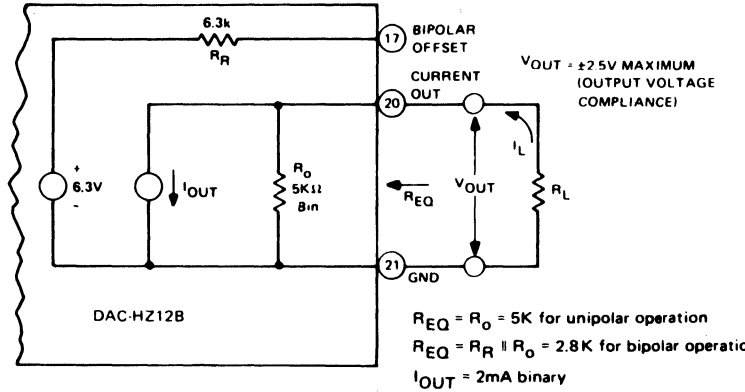
UNIPOLAR OUTPUT — COMPLEMENTARY BINARY

BINARY INPUT CODE			UNIPOLAR OUTPUT RANGES		
MSB		LSB	0 TO +10V	0 TO +5V	0 TO −2 mA
0000	0000	0000	+9.9976V	+4.9988V	−1.9995 mA
0011	1111	1111	+7.5000	+3.7500	−1.5000
0111	1111	1111	+5.0000	+2.5000	−1.0000
1011	1111	1111	+2.5000	+1.2500	−0.5000
1111	1111	1110	+0.0024	+0.0012	−0.0005
1111	1111	1111	0.0000	0.0000	0.0000

BIPOLAR OUTPUT — COMPLEMENTARY OFFSET BINARY

INPUT CODE			BIPOLAR OUTPUT RANGES			
MSB		LSB	±10V	±5V	±2.5V	±1 mA
0000	0000	0000	+9.9951V	+4.9976V	+2.4988V	−0.9995 mA
0011	1111	1111	+5.0000	+2.5000	+1.2500	−0.5000
0111	1111	1111	0.0000	0.0000	0.0000	0.0000
1011	1111	1111	−5.0000	−2.5000	−1.2500	+0.5000
1111	1111	1110	−9.9951	−4.9976	−2.4988	+0.9995
1111	1111	1111	−10.0000	−5.0000	−2.5000	+1.0000

EQUIVALENT CURRENT MODE OUTPUT CIRCUIT

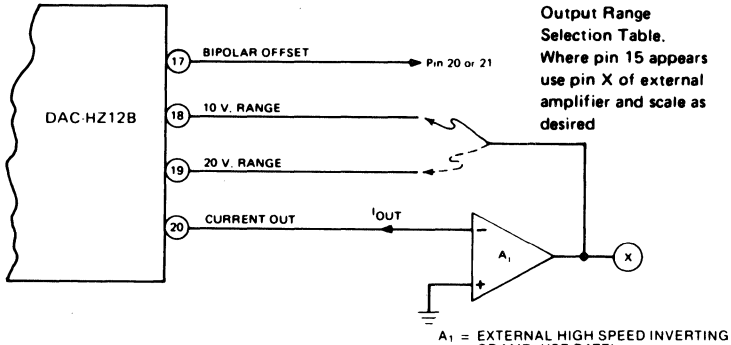


$R_{EQ} = R_O = 5K$ for unipolar operation

$R_{EQ} = R_R \parallel R_O = 2.8K$ for bipolar operation

$I_{OUT} = 2mA$ binary

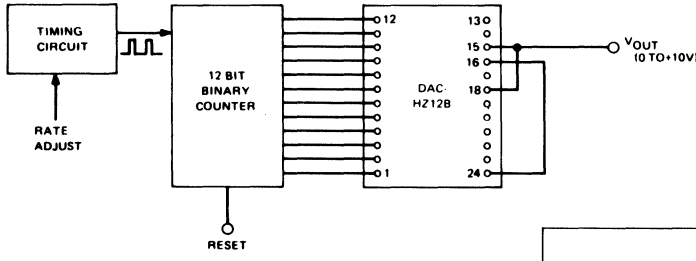
USE OF HIGH SPEED EXTERNAL OP AMP FOR FASTER SETTLING

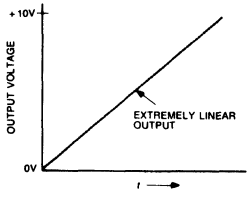


Refer to the Output Range Selection Table. Where pin 15 appears use pin X of external amplifier and scale as desired

A_1 = EXTERNAL HIGH SPEED INVERTING OP AMP. USE DATEL AM-500 FOR LESS THAN 1.0μSEC. OUTPUT SETTLING.

PRECISION, LOW COST BASE LINE RAMP GENERATOR





THIS CIRCUIT DEVELOPS A HIGHLY LINEAR (.01%) OUTPUT VOLTAGE RAMP FROM 0 TO +10V. THE RAMP CAN BE MADE AS SLOW AS DESIRED WITHOUT AFFECTING LINEARITY BY SETTING THE PULSE RATE OF THE TIMING CIRCUIT TO THE PROPER VALUE. THE OUTPUT RAMP IS GENERATED IN DISCRETE STEPS OF .024% FS (4096 STEPS FOR FS CHANGE).

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
DAC-HZ12BGC	0°C to +70°C	Epoxy
DAC-HZ12BMC	0°C to +70°C	Hermetic
DAC-HZ12BMM	−55°C to +125°C	Hermetic
DAC-HZ12DGC	0°C to +70°C	Epoxy
DAC-HZ12DMC	0°C to +70°C	Hermetic
DAC-HZ12DMM	0°C to +70°C	Hermetic

ACCESSORIES

Part Number	Description
DILS-3	24-pin Mating Socket
TP10K or TP100K	Trimming Potentiometers

For military devices compliant to MIL-STD-883, consult DATEL

DAC-IC10B Series
Low Cost, 10-Bit Monolithic Digital-to-Analog Converter

FEATURES

- **10-Bit resolution**
- **Straight binary coding**
- **Current output**
- **250 Nanosecond settling time**
- **TTL/CMOS-compatible**
- **Low cost**

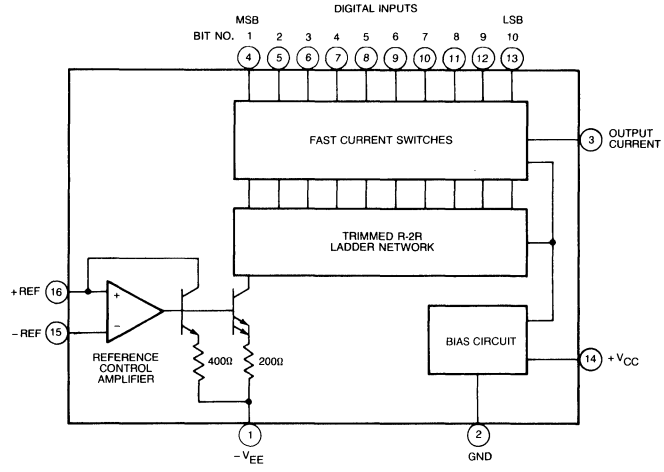
GENERAL DESCRIPTION

The DAC-IC10B is a low cost, 10-bit monolithic DAC with fast output current settling time. It is packaged in a 16-pin ceramic DIP and requires only an external reference and operational amplifier for voltage output operation. A full-scale change in output current settles in 250 nanoseconds, and with a fast I.C. operational amplifier (such as DATEL's AM-452) a 10V output change can settle within 1 microsecond. Digital input coding is straight binary for unipolar operation, and offset binary for bipolar operation; the logic inputs are compatible with TTL or CMOS.

This converter is manufactured with monolithic bipolar technology. The circuit incorporates 10 fast switching current sources which drive a diffused resistor R-2R network. The ladder network is laser trimmed by cutting aluminum links. The circuit also contains a reference control amplifier and a bias circuit. An external reference current of 2 mA is required at the + Reference input terminal; this is accomplished by an external voltage reference and a metal film resistor.

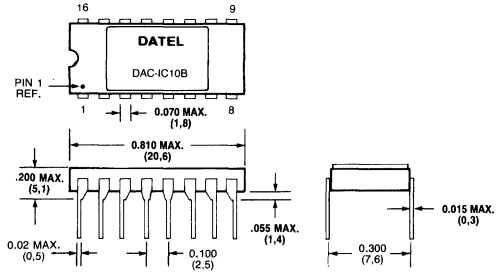
Other characteristics of the DAC-IC10B include linearity to ± ½ LSB and guaranteed monotonic performance. The gain temperature coefficient of this unit is typically −20 ppm/°C. Output voltage compliance is −2.5V to +0.2V, permitting direct driving of a 625Ω resistor for a voltage output. The reference input current can be varied from 0.5 mA to 2.5 mA to give monotonic operation as a one- or two-quadrant multiplier.

Power supply requirement is +5V dc and −15V dc. The DAC-IC10B is available in three models covering two temperature ranges, 0°C to +70°C and −55°C to +125°C.



MECHANICAL DIMENSIONS

INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−VEE
2	GROUND
3	*OUTPUT CURRENT*
4	BIT 1 IN (MSB)
5	BIT 2 IN
6	BIT 3 IN
7	BIT 4 IN
8	BIT 5 IN
9	BIT 6 IN
10	BIT 7 IN
11	BIT 8 IN
12	BIT 9 IN
13	BIT 10 IN
14	+VCC
15	−REFERENCE
16	+REFERENCE

ABSOLUTE MAXIMUM RATINGS	
V_{CC}	+7.0V
V_{EE}	+18.0V
Digital Input Voltage	+15V
Output Voltage, Pin 3	+0.5, −5.0V
Reference Current	2.5 mA
Different Reference Voltage	0.7V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, V_{CC} = +5V, V_{EE} = −15V, I_{REF} = 2.0 mA.

INPUTS	
Resolution	10 Bits
Coding, Unipolar Output	Straight Binary
Coding, Bipolar Output	Offset Binary
Input Level, Logic "1"	+2.0 to +15V at +20 μA
Input Level, Logic "0"	0 to +0.8V at −.02 mA
Nominal Reference Current, Pin 16	2.0 mA
Reference Current Range	0.5 mA to 2.5 mA
Reference Bias Current, Pin 15	−5 μA maximum

OUTPUTS	
Output Current	4.0 mA ±0.2 mA
Output Current Range	0 to 5.0 mA
Output Current, All Bits "0"	2.0 μA maximum[1]
Output Voltage Compliance	−2.5 to +0.2V
Output Capacitance	25 pF

PERFORMANCE	
Linearity Error, B, BM	±½ LSB, maximum
BC	±1 LSB, maximum
Differential Linearity Error	±½ LSB
Monotonicity, B, BM	Full Temperature Range[2]
BC	At 25°C
Gain Tempco	−20 ppm/°C, 60 ppm/°C maximum[3]
Reference Current, Slew Rate	20 mA/microseconds
Reference Current Settling	2.0 microseconds[4]
Output Current Settling	250 nanoseconds[5]
Update Rate	4 MHz
Power Supply Sensitivity	02%/% maximum

POWER REQUIREMENTS	
V_{CC} Voltage	+5V dc ±0.25V
V_{CC} Current	+4 mA maximum
V_{EE} Voltage	−15V dc ±0.75V
V_{EE} Current	−18 mA maximum

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
DAC-IC10B, BC	0°C to +70°C
DAC-IC10BM	−55°C to +125°C
Storage Temperature Range	−65°C to +125°C
Package	16-Pin Ceramic DIP

FOOTNOTES:

1. 4.0 μA maximum for DAC-IC10BC only.
2. All converters in this series typically retain rated monotonicity for values of input reference current from 0.5 mA to 2.5 mA.
3. 70 ppm/°C maximum for DAC-IC10BM only.
4. Zero to 4 mA output change to rated accuracy.
5. Full scale change to ½ LSB.

TECHNICAL NOTES

1. The *General Connection Diagram* shows the basic connections for the converter. The scale factor is set by a reference current injected into pin 16. Pins 15 and 16 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R_{15} and pin 16 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R_{16}: $I_{REF} = V_{REF}/R_{16}$. R_{16} should be a stable metal film resistor. R_{15} is used only to compensate for the input bias current into pin 15 (1 μA typical). R_{15}, if used, should be equal to R_{16} and may be a carbon composition type. An I_{REF} of 2.0 mA is recommended for most applications.
2. There is a second method of connecting the reference shown in *Two Ways to Connect Reference.* A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 16 is at the negative voltage and I_{REF} still flows into pin 16. Again, R_{15} is used only to compensate for bias current. There is an important requirement for this connection: **the negative reference voltage must always be 3 volts above V_{EE}.**
3. I_{OUT} is inversely proportional to the reference input current (I_{REF}) times the digital word. Scaling of the applied reference can be represented as follows:

$$I_{OUT} = -2 \frac{V_{REF}}{R_{REF}} \frac{A_n}{2^n}$$

where n = 10 (10-bit DAC)
A_n = digital code

Note: 1) The largest digital code for a 10 bit DAC is 1023.
2) The reference current is scaled by a factor of 2 within the DAC.

Example:

$$I_{OUT}\,(FS) = -2 \frac{2.5V}{1.25K} \frac{1023}{1024}$$

$$= -3.996 \text{ mA (nominal)}$$

$$I_{OUT}\,(ZERO) = -2 \frac{2.5V}{1.25K} \frac{0}{1024}$$

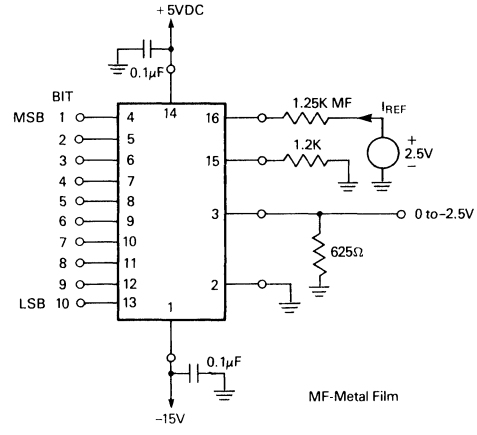
$$= 0 \text{ mA (nominal)}$$

4. The reference amplifier is internally compensated. The minimum reference current supplied from a current source is 0.5 mA for stability.
5. The voltage on pin 3 is restricted to a range of −2.5V to +0.2V. This compliance voltage is guaranteed at 25°C and nearly constant over temperature.
6. Full-scale output current of 3.996 mA is guaranteed for input reference currents to pin 16 between 1.9 and 2.1 mA.
7. It is recommended that pin 14 (V_{CC}) and pin 1 V_{EE}) always be bypassed to ground with at least 0.1 μF capacitors located close to the pins.
8. The accuracy of the converter is specified for a reference current of 2.0 mA; the accuracy, however, is essentially constant for reference currents from 1.5 mA to 2.5 mA. Typically, this device is monotonic for all values of reference current above 0.5 mA.

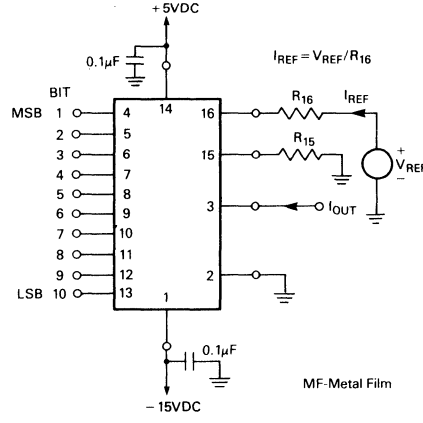
TECHNICAL NOTES (Cont'd.)

9. For fastest voltage output settling times in either unipolar or bipolar modes, two circuits using DATEL AM-452 monolithic operational amplifiers are recommended. These circuits, with the compensation shown, result in output settling times of typically 550 nanoseconds for a 10V change to 1 LSB. This is the worst case settling time which occurs when all bits are turned on. For current output and R_L less than 500 ohms, this time is 250 nanoseconds; when all bits are turned off the time is shorter, typically 100 nanoseconds. The two circuits shown also illustrate a simple method of deriving both reference current and offset current from a precision 6.4V Zener reference diode.
10. Both one and two quadrant multiplication are also possible with the converter as shown in the two diagrams. V_{IN} is shown operating into pin 16; this results in an input impedance of 2.5K. Alternatively, V_{IN} can be applied to pin 15 for a high impedance input as explained previously. The range of V_{IN} is then 0 to −10V. For two quadrant multiplication V_{IN} is unipolar and the digital input is bipolar with offset binary coding. V_{OUT} then varies over the bipolar range of ±5V. In multiplication applications, it is recommended that full scale I_{REF} be set to 2.0 mA; the output is then monotonic as the reference current varies over 0.5 mA to 2.0 mA.

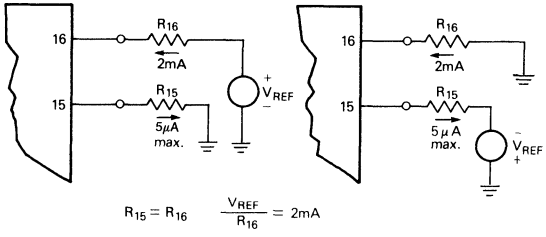
CONNECTION FOR DIRECT VOLTAGE OUTPUT



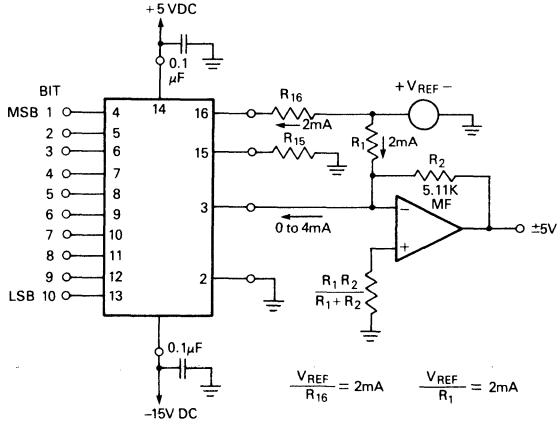
GENERAL CONNECTION DIAGRAM



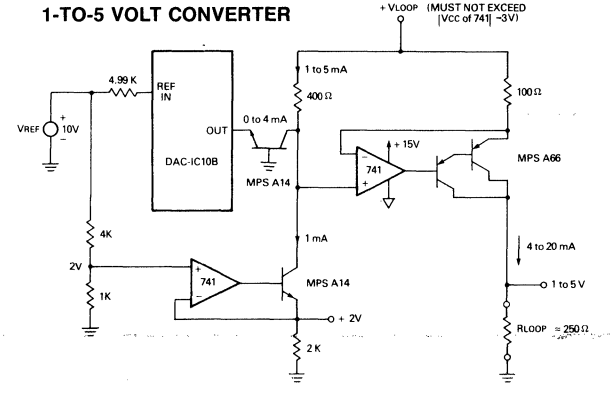
TWO WAYS TO CONNECT REFERENCE



CONNECTION FOR BIPOLAR VOLTAGE OUT

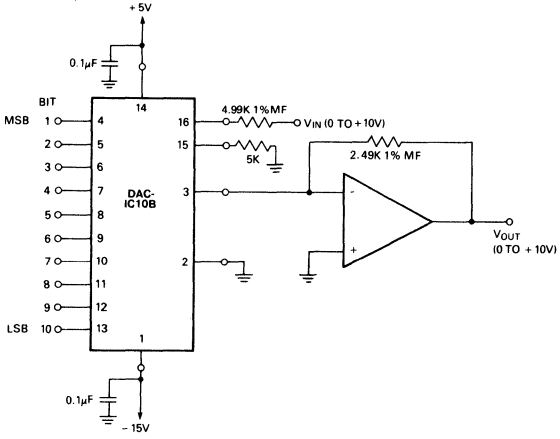


DIGITAL 4-TO-20 MA OR 1-TO-5 VOLT CONVERTER

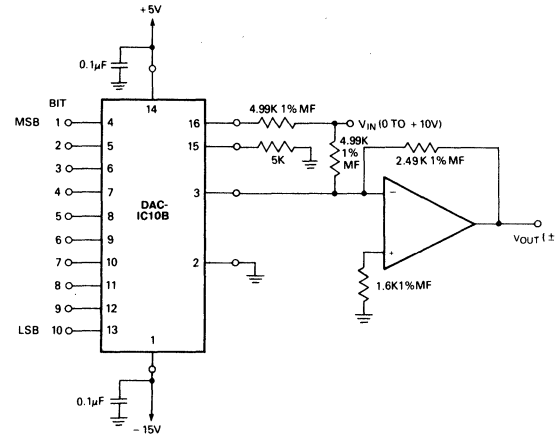


APPLICATION DIAGRAMS

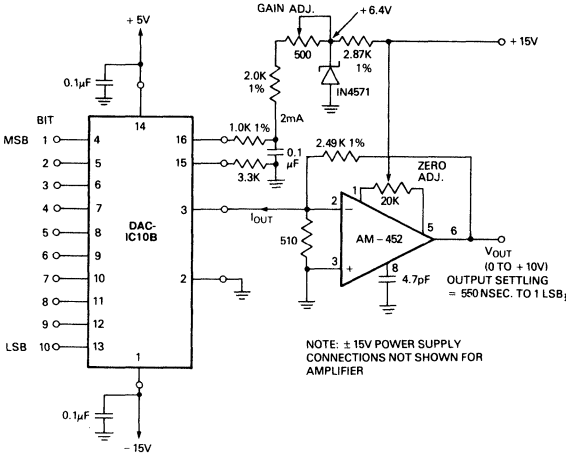
ONE QUADRANT MULTIPLICATION



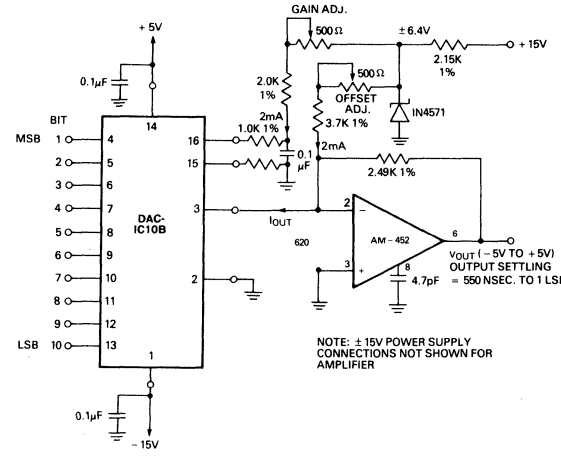
TWO QUADRANT MULTIPLICATION



FAST, UNIPOLAR VOLTAGE OUTPUT



FAST, BIPOLAR VOLTAGE OUTPUT



CALIBRATION AND CODING TABLE

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. *Zero and Offset Adjustments*/For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full-scale voltage shown in the Coding Table.
3. *Gain Adjustment*/For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full-scale voltage shown in the Coding Table.

INPUT CODE		UNIPOLAR OPERATION—STRAIGHT BINARY			
MSB	LSB	0 TO +5V	0 TO +10V	0 TO −2 mA	0 to −4 mA
11 1111	1111	+4.995V	+9.990	−1.998 mA	−3.996
11 1000	0000	+4.375	+8.750	−1.750	−3.500
11 0000	0000	+3.750	+7.500	−1.500	−3.000
10 0000	0000	+2.500	+5.000	−1.000	−2.000
01 0000	0000	+1.250	+2.500	−0.500	−0.100
00 0000	0001	+0.005	+0.010	−0.002	−0.004
00 0000	0000	0.000	0.000	0.000	0.000

INPUT CODE		BIPOLAR OPERATION—OFFSET BINARY CODING			
MSB	LSB	±5V	±10V	±1 mA	±2 mA
11 1111	1111	+4.990V	+ 9.980V	−0.998 mA	−1.996 mA
11 1000	0000	+3.750	+ 7.500	−0.750	−1.500
11 0000	0000	+2.500	+ 5.000	−0.500	−1.000
10 0000	0000	0.000	0.000	0.000	0.000
01 0000	0000	−2.500	− 5.000	+0.500	+1.000
00 0000	0001	−4.990	− 9.980	+0.998	+1.996
00 0000	0000	−5.000	−10.000	+1.000	+2.000

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
DAC-IC10BC	0°C to +70°C
DAC-IC10B	0°C to +70°C
DAC-IC10BM	−55°C to +125°C

Model DAC-IC8B
Low Cost, 8-Bit Monolithic Digital-to-Analog Converters

FEATURES

- **Low cost**
- **8-Bit resolution**
- **Fast settling—300 nanoseconds**
- **1- or 2-quadrant multiplication**
- **± ½ LSB linearity**
- **DTL/TTL compatible inputs**

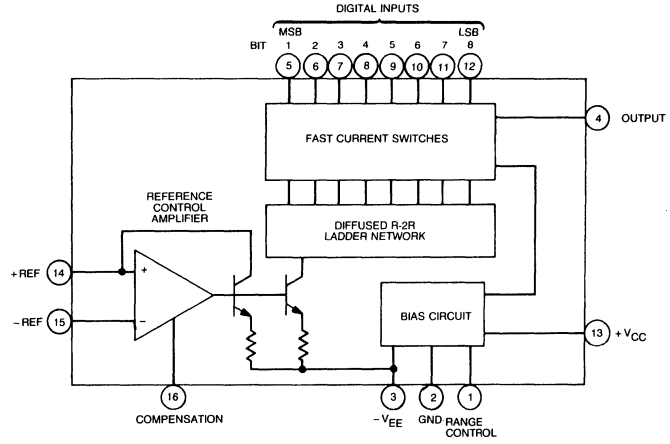
GENERAL DESCRIPTION

The DAC-IC8BC and DAC-IC8BM are 8-bit monolithic DAC's with fast settling current outputs. The units are housed in a 16 pin ceramic DIP and require only an external reference and output amplifier for fast voltage output operation. A full scale output change settles in only 300 nanoseconds for current output operation and 600 nanoseconds for voltage output operation using a fast monolithic output amplifier (DATEL's AM-452). Digital input coding is straight binary for unipolar operation and offset binary for bipolar operation and is compatible with standard DTL/TTL logic.

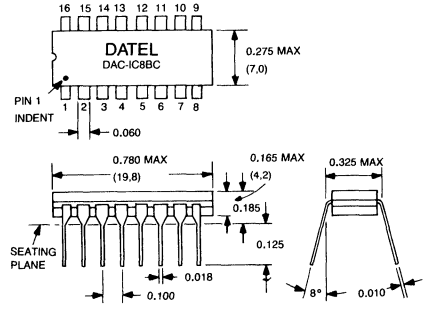
The DAC-IC8B converters consist of 8 fast-switching current sources, a diffused R-2R resistor ladder network, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of −20 ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling, and low cost. Linearity is ± ½ LSB.

An external reference current of 2 mA nominal programs the scale factor for the DAC; this is done by means of an external voltage reference source (such as Zener diode) and a resistor. This reference current can also be varied, resulting in one or two quadrant multiplying operation. The output voltage can be unipolar or bipolar depending on whether an external offsetting current (derived from the reference) is used. Output voltage compliance of the DAC is −0.6V to +0.5V; this can be made as large as −5V to +0.5V by external pin connection for cases where direct voltage output from a load resistor is desired.

Power supply requirement is +5V dc and −5V to −15V dc. Model DAC-IC8BC has an operating temperature range of 0°C to 70°C while DAC-IC8BM operates over −55°C to +125°C. The two models are pin compatible with industry standard devices 1408L-8 and 1508L-8 respectively.



MECHANICAL DIMENSIONS
INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	RANGE CONTROL
2	GROUND
3	VEE
4	OUTPUT
5	BIT 1 IN (MSB)
6	BIT 2 IN
7	BIT 3 IN
8	BIT 4 IN
9	BIT 5 IN
10	BIT 6 IN
11	BIT 7 IN
12	BIT 8 IN (LSB)
13	VCC
14	+REFERENCE
15	−REFERENCE
16	COMPENSATION

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltage, V_{CC}	+5.5V
V_{EE}	−16.5V
Digital Input Voltage	+5.5V
Reference Current	5.0 mA
Reference Amp. Inputs	$+V_{CC}$, $-V_{EE}$
Power Dissipation	1.0 watt

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, V_{CC} = +5V, V_{EE} = −15V, and I_{REF} = 2 mA unless otherwise specified.

INPUTS	
Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+2.0V to +5.5V at 40 μA
Input Logic Level, bit OFF ("0")	0V to +0.8V at −0.8 mA
Logic Loading	1 TTL load
Nominal Reference Current (+ Reference)	2.0 mA
Reference Current Range (+ Reference)	0 to 4.2 mA
Reference Bias Current (− Reference)	−3 μA max.

OUTPUTS	
Output Current, I_{REF} = 2.0 mA	2.0 mA ±0.1 mA
Output Current Range, V_{EE} = −5V	0 to 2.1 mA
Output Current Range, V_{EE} = −6 to −15V	0 to 4.2 mA
Output Current, all bits OFF	4 μA max.
Output Voltage Compliance, pin 1 gnded	−0.6 to +0.5V
Output Voltage Comp., pin 1 open, $V_{EE} \leq -10V$	−5.0V to +0.5V

PERFORMANCE	
Relative Accuracy[1]	±½ LSB (±0.19%) max.
Nonlinearity	±½ LSB (±0.19%) max.
Differential Nonlinearity	±½ LSB (±0.19%)
Temp. Coefficient of Gain	−20 ppm/°C
Power Supply Rejection (V_{EE})	2.7 μA/V max.
Settling Time, 2 mA to ½ LSB	300 nsec.
Update Rate	3.3 MHz
Reference Current Slew Rate	4.0 mA/μsec.

POWER REQUIREMENTS	
V_{CC} Voltage	+5V dc ±0.5V
V_{CC} Current	22 mA max.
V_{EE} Voltage	−4.5V to −16.5V dc
V_{EE} Current	13 mA max.

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, DAC-IC8BC	0°C to 70°C
Operating Temp. Range, DAC-IC8BM	−55°C to +125°C
Storage Temp. Range, either model	−65°C to +150°C
Package, DAC-IC8BC	16 Pin Plastic DIP
Package, DAC-IC8BM	16 Pin Ceramic DIP

FOOTNOTE:

1. With zero and full scale adjustments made.

TECHNICAL NOTES

1. The General Connection Diagram shows the basic connections for the DAC-IC8B converter. The scale factor is set by a reference current injected into pin 14. Pins 14 and 15 are the input terminals to the reference control amplifier. When connected as shown, pin 15 is grounded through R_{15} and pin 14 is at virtual ground. Therefore, the reference current is determined by the external voltage reference and R_{14}: $I_{REF} = V_{REF}/R_{14}$. R_{14} should be a stable metal film resistor. R_{15} is used only to compensate for the input bias current into pin 15 (1 μA typical) and can be shorted out with negligible effect. R_{15}, if used, should be equal to R_{14} and may be carbon composition type. An I_{REF} of 2.0 mA is recommended for most applications.
2. There is a second method of connecting the reference shown in Two Ways to Connect Reference. A negative reference can be applied to pin 15. In this case only the bias current must be supplied from the reference since pin 15 is a high impedance input. Pin 14 is at the negative voltage and I_{REF} still flows into pin 14. Again, R_{15} is used only to compensate for bias current and may be omitted. There is an important requirement for this connection: *the negative reference voltage must always be 3 volts above V_{EE}.*
3. The reference amplifier must be externally compensated, and this is done by capacitor C_c, connected from pin 16 to pin 3 (V_{EE}). C_c may also be connected from pin 16 to ground, but connection to pin 3 improves the negative supply rejection. The value of C_c depends on R_{14}, and typical values are given in the compensation table. Compensation is particularly important when the DAC-IC8B is used as a multiplying D/A converter. Proper compensation assures that output peaking does not occur when the reference voltage steps to a new value. If pin 14 is driven from a high impedance current source such as a transistor collector, then much larger values of C_c must be used and the bandwidth of the reference amplifier is significantly reduced.
4. The Alternative Compensation Diagram shows another way of achieving the desired compensation. Here a 1.0K resistor is always used at pin 14, but it is in series with another R to the reference voltage. The junction of the two resistors is bypassed to ground by a 0.1 μF capacitor. For high frequencies pin 14 always "sees" a 1K resistance, thus allowing a 15 pF capacitor for C_c. R_{15}, if used, should be the sum of 1.0K and R. This compensation scheme is useful with voltage references such as 6.2 or 6.4 volt Zener diodes.
5. It is recommended that pin 13 (V_{CC}) and pin 3 (V_{EE}) always be bypassed to ground with at least 0.1 μF capacitors located close to the pins.
6. As shown in the General Connection Diagram, pin 1 may be either connected to ground or left open. This connection determines the voltage compliance at pin 4 (I_{OUT}). For pin 1 grounded, the output compliance is −0.6 to +0.5 volt. This is satisfactory when pin 4 is used to drive a current to voltage converter and pin 4 is held at virtual ground. It is also satisfactory for low values of R_L connected to pin 4 to directly convert the output current to a voltage. The voltage compliance may be extended to −5.0 volts by leaving pin 1 open and using a V_{EE} more negative than −10 volts. In this way a 2.5K load resistor may be used at pin 14 to give an output voltage range of 0 to −5 volts (with reference current of 2 mA). As shown in the table of *Settling Time vs R_L*, the output settling time is constant (300 nseconds) for R_L values from 0 to 500 ohms; thereafter it increases to 1.2 μseconds for R_L = 2.5K.

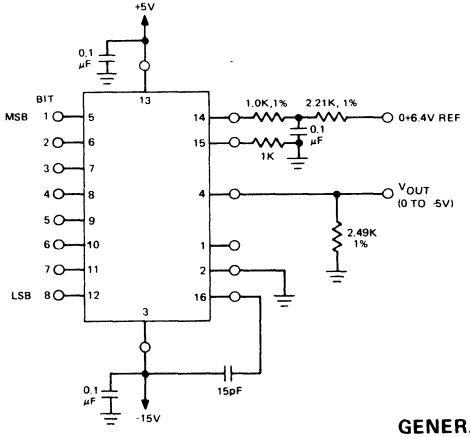
TECHNICAL NOTES (Con't)

7. The accuracy of the DAC-IC8B is specified for a reference current of 2.0 mA; the accuracy, however, is essentially constant for reference currents from 1.5 mA to 2.5 mA. Typically, this device is monotonic for all values of reference current above 0.5 mA. Reference currents up to 4.2 mA may be used. *When using a 4 mA reference current, V_{EE} must be more negative than −6 volts.*
8. For fastest voltage output settling times in either unipolar or bipolar modes, two circuits using DATEL's AM-452 monolithic operational amplifiers are recommended. These circuits, with the compensation shown, result in output settling times of typically 600 nanoseconds for a 10 volt change to 1 LSB. This is the worst case settling time which occurs when all bits are turned on. For current output and R_L less than 500 ohms, this time is 300 nanoseconds; when all bits are turned off the time is shorter, typically 100 nanoseconds. The two circuits shown also illustrate a simple method of deriving both reference current and offset current from a precision 6.4 volt Zener reference diode.
9. Both one and two quadrant multiplication are also possible with the DAC-IC8B as shown in the two diagrams. V_{IN} is shown operating into pin 14; this results in an input impedance of 2.5K. Alternatively, V_{IN} can be applied to pin 15 for a high impedance input as explained previously. The range of V_{IN} is then 0 to −10V. For two quadrant multiplication V_{IN} is unipolar and the digital input is bipolar with offset binary coding. V_{OUT} then varies over the bipolar range of ±5 volts. In multiplication applications, it is recommended that full scale I_{REF} be set to 4.0 mA; the output is then monotonic as the reference current varies over 0.5 mA to 4.0 mA.

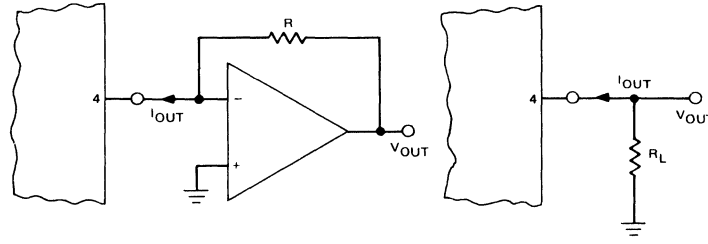
2

CONNECTION DIAGRAMS

HIGH COMPLIANCE OUTPUT



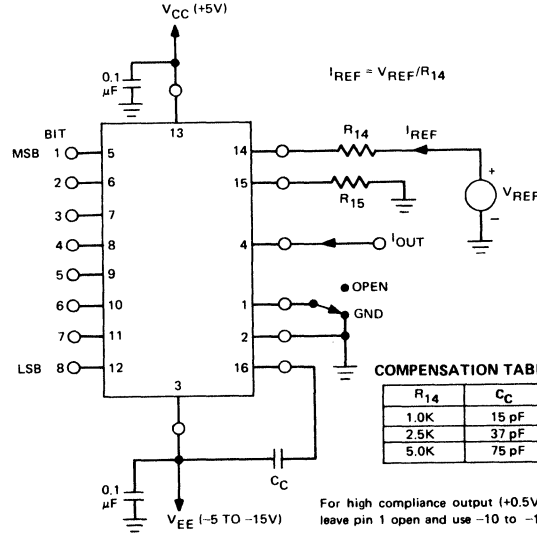
OUTPUT CONNECTIONS



SETTLING TIME VS. R_L

R_L	S.T.
0	300 nsec.
500	300 nsec.
1 K	400 nsec.
2.5 K	1.2 µsec.

GENERAL CONNECTION DIAGRAM



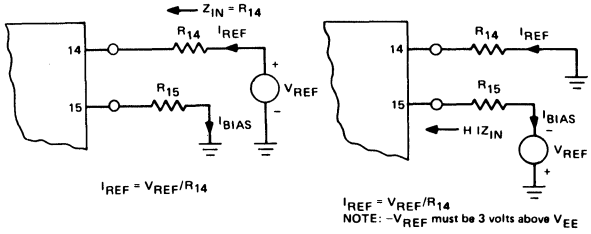
COMPENSATION TABLE

R_{14}	C_C
1.0K	15 pF
2.5K	37 pF
5.0K	75 pF

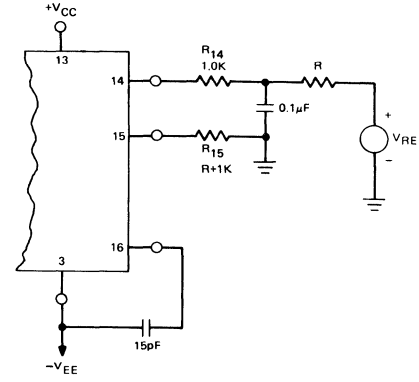
For high compliance output (+0.5V to −5.0V) leave pin 1 open and use −10 to −15V for V_{EE}.

CONNECTION DIAGRAMS

TWO WAYS TO CONNECT REFERENCE

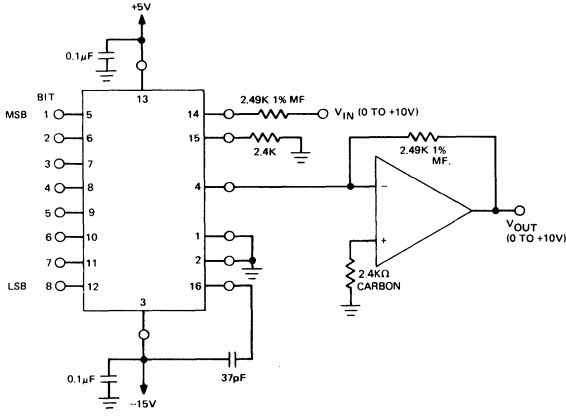


ALTERNATIVE COMPENSATION

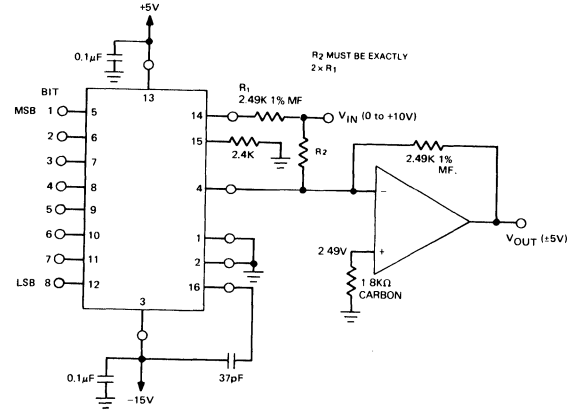


APPLICATION DIAGRAMS

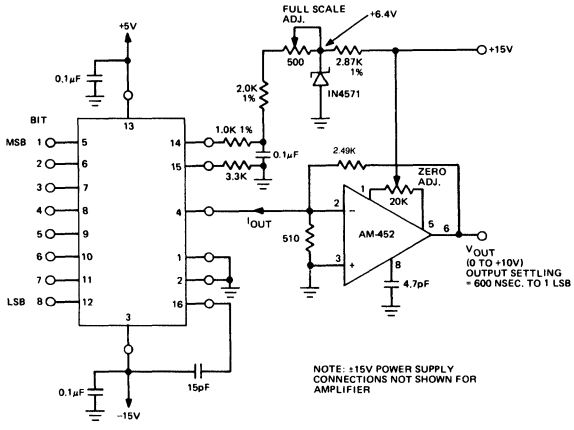
ONE QUADRANT MULTIPLICATION



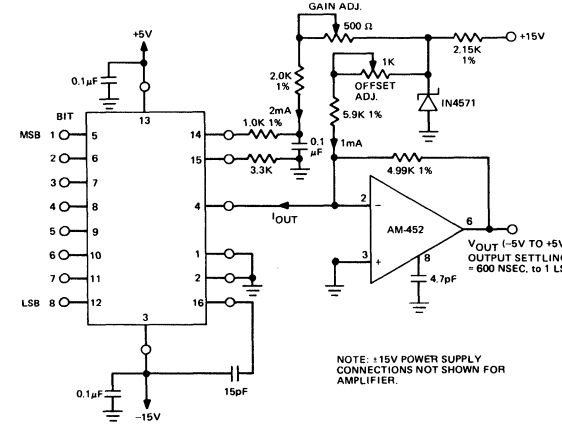
TWO QUADRANT MULTIPLICATION



FAST, UNIPOLAR VOLTAGE OUTPUT



FAST, BIPOLAR VOLTAGE OUTPUT



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CALIBRATION AND CODING TABLES

1. Select the desired output range by means of the feedback resistor of the external operational amplifier and the externally programmed reference current.
2. *Zero and Offset Adjustments*
   For unipolar operation, set all digital inputs to "0" (0V to +0.8V) and adjust the output amplifier ZERO ADJUSTMENT for zero output voltage. For bipolar operation, set all digital inputs to "0" (0 to +0.8V) and adjust the OFFSET ADJUSTMENT for the negative full scale voltage shown in the Coding Table.
3. *Gain Adjustment*
   For either unipolar or bipolar operation, set all digital inputs to "1" (+2.0 to +5.5V) and adjust the GAIN ADJUSTMENT for the positive full scale voltage shown in the Coding Table.

UNIPOLAR OPERATION—STRAIGHT BINARY CODING

INPUT CODE		UNIPOLAR OUTPUT RANGES			
MSB	LSB	0 TO +5V	0 TO +10V	0 TO −2 mA	0 TO −4 mA
1111	1111	+4.980	+9.961V	−1.992 mA	−3.984 mA
1110	0000	+4.375	+8.750	−1.750	−3.500
1100	0000	+3.750	+7.500	−1.500	−3.000
1000	0000	+2.500	+5.000	−1.000	−2.000
0100	0000	+1.250	+2.500	−0.500	−1.000
0000	0001	+0.020	+0.039	−0.008	−0.016
0000	0000	0.000	0.000	0.000	0.000

BIPOLAR OPERATION—OFFSET BINARY CODING

INPUT CODE		BIPOLAR OUTPUT RANGES			
MSB	LSB	±5V	±10V	±1 mA	±2 mA
1111	1111	+4.961V	+9.922V	−0.992 mA	−1.984 mA
1110	0000	+3.750	+7.500	−0.750	−1.500
1100	0000	+2.500	+5.000	−0.500	−1.000
1000	0000	0.000	0.000	0.000	0.000
0100	0000	−2.500	−5.000	+0.500	+1.000
0000	0001	−4.961	−9.922	+0.992	+1.984
0000	0000	−5.000	−10.000	+1.000	+2.000

2

ORDERING INFORMATION

DAC-IC8B_____

OPER. TEMP. RANGE

C = 0°C TO +70°C
M = −55°C TO +125°C

ACCESSORIES

Part Number	Description
TP500, TP1K, and TP20K are available from DATEL	Trimming Potentiometers

DAC-UP10B
10-Bit Monolithic DAC With Input Registers

FEATURES

- **Input registers**
- **10-Bit resolution**
- **Voltage output**
- **Internal reference**
- **Guaranteed monotonicity**

GENERAL DESCRIPTION

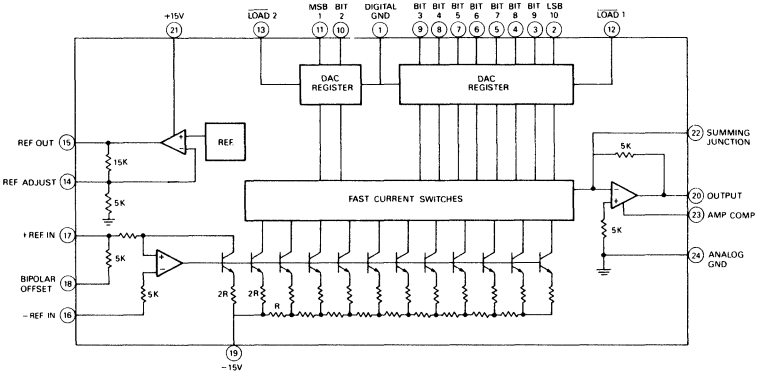
The DAC-UP10B is a low cost, monolithic 10-bit D/A converter with internal registers. The device also includes a high speed output amplifier, stable internal reference, and an input reference amplifier. Low loading latches, adjustable logic thresholds and addressing capability allow the DAC-UP10B to directly interface with many microprocessor and logic controlled systems.

The input registers are controlled by two enable lines ($\overline{\text{LOAD}}$ 1, $\overline{\text{LOAD}}$ 2). When the enable inputs are low, the registers are active, and any change on the digital inputs will be reflected on the analog output. When the enable inputs are high, the digital inputs become very high impedances and the data present is retained until the enable lines go low. The two enable inputs allow the converter to be directly interfaced with an 8-bit data bus.

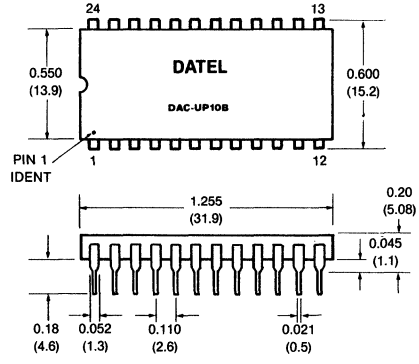
The output voltage range is 0 to +10V dc for unipolar mode, ±5V dc for bipolar. A full-scale output change settles to within 0.05% in 5 microseconds. The internal band gap reference is buffered and amplified to provide the 5V reference output. Either the internal reference or, for increased accuracy, an external reference can be used to bias the current switching networks.

Other characteristics of the DAC-UP10B include guaranteed monotonic performance, a Gain Temperature Coefficient of only 20 ppm/°C, and Zero Tempco of 5 ppm/°C. The power supply voltage range is ±11.4V dc to ±16.5V dc.

The DAC-UP10B is packaged in a 24-pin plastic DIP, and operation is specified over the 0 to +70°C operating temperature range.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIG. GRND	13	$\overline{\text{LOAD}}$ 2
2	BIT 10 IN (LSB)	14	REF. ADJ
3	BIT 9 IN	15	REF. OUT
4	BIT 8 IN	16	- REF IN
5	BIT 7 IN	17	+ REF IN
6	BIT 6 IN	18	BIPOLAR OFF.
7	BIT 5 IN	19	- 15 VDC
8	BIT 4 IN	20	OUTPUT
9	BIT 3 IN	21	+ 15 VDC
10	BIT 2 IN	22	SUM. JUNC.
11	BIT 1 IN	23	AMP. COMP.
12	$\overline{\text{LOAD}}$ 1	24	ANALOG GRND.

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ABSOLUTE MAXIMUM RATINGS	
Positive Supply, Pin 21	+18V dc
Negative Supply, Pin 19	−18V dc
Digital Input Voltage, Pins 2-11	+18V dc
Reference Input, Pin 17	+12V dc
Summing Junction, Pin 22	+12V dc

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, ref. in = +5V unless otherwise noted.

INPUTS	
Resolution	10 Bits
Coding, Unipolar	Straight Binary
Bipolar	Offset Binary
Input Logic Level,	
Bit ON ("1") min.[1]	+2V at 10 μA
Bit OFF ("0") max.[1]	+0.8V at 10 μA
Load Inputs	High ("1") = Hold Data Low ("0") = Transfer Data
Load Pulse Width, min.	150 nsec.
Reference Input Voltage	5V dc, ±10%
Reference Input Resistance	5 kΩ

OUTPUT	
Output Voltage Range, Unipolar	+10V dc
Bipolar	±5V dc
Output Current	5 mA
Reference Output Voltage[2]	5V ±10%
Reference Output Current, max.	3 mA

PERFORMANCE	
Linearity Error, max.	±1 LSB
Differential Linearity Error	±1 LSB
Monotonicity	Over Operating Temp. Range
Gain Error	Adjustable to Zero
Zero Error	Adjustable to Zero
Gain Tempco[3]	20 ppm/°C
Zero Tempco, Unipolar[3]	5 ppm/°C
Reference Tempco[2]	60 ppm/°C
Settling Time, 10V to 0.05%	5 μsec.
Power Supply Sensitivity, max.	±0.01% FS/%V_S

POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V dc
Power Supply Voltage Range	±11.4V dc to ±16.5V dc
Supply Current, Quiescent max.[4]	+14 mA, −15 mA
Power Dissipation, max.[4]	435 mW

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package	24 Pin Plastic Dip

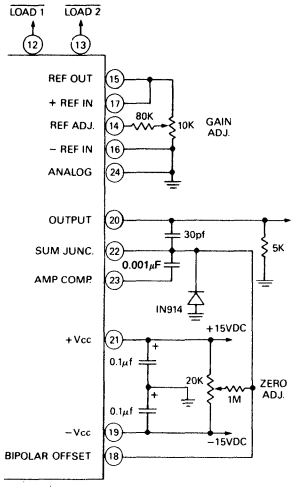
FOOTNOTES:

1. Bias circuits shown will provide the proper threshold voltage levels for various logic families. See technical note 3.
2. Ref. output current = 1 mA
3. Ref. in = +5V
4. V_S = ±15V dc, Iref = 1 mA

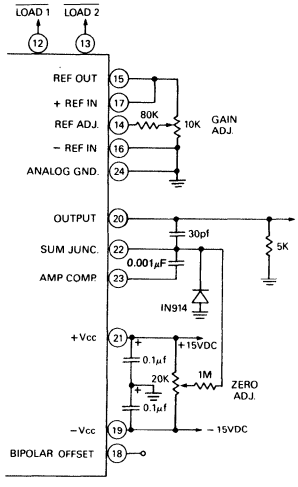
TECHNICAL NOTES

1. The Load control inputs (pins 12, 13) are level triggered inputs. The Load 2 input (pin 13) controls the two most significant bits while the Load 1 input (pin 12) controls the eight least significant bits. When the Load inputs are "Logic 1", the input registers will hold the data present, a "Logic 0", activates the registers, transferring data to the converter output.
2. A set-up time of 100 nanoseconds minimum must be allowed before the Load inputs go from low to high. In addition, a 50 nanosecond minimum Hold Time must be allowed for the input data after the Load inputs go from low to high. The minimum pulse width for the Load inputs is 150 nanoseconds. The maximum update rate is determined by the output settling time. See Timing Diagram.
3. The digital inputs of the DAC-UP10B utilize a differential logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (pin 1). Bias circuits are shown that will provide the proper threshold voltage levels for various logic families.
4. The −Ref input (pin 16) is uncommitted to allow utilization of negative polarity reference voltages. In this mode, the +Ref input (pin 17) is grounded and the negative reference is tied directly to the −Ref pin.
5. It is recommended that the ±15V power input pins both be bypassed to ground with 0.1 μF ceramic capacitors. Also, to minimize capacitance, external resistors should be mounted as close to the ref. adj. pin (pin 14) as possible. These precautions along with good layout practices will insure noise free operation.
6. The gain tempco of the DAC-UP10B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm/°C typical results for the converter. If greater temperature stability is required, a more stable external reference may be used.
7. The output amplifier incorporates output short circuit protection for both positive and negative excursions. Short circuit current is typically limited at ±15 mA.

CONNECTION AND CALIBRATION



BIPOLAR OPERATION



UNIPOLAR OPERATION

CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION TABLE.
2. Apply Logic "0" to $\overline{\text{LOAD}}$ pins (pins 12, 13).
3. Zero and Offset Adjustments
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ potentiometer for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ potentiometer for negative full scale voltage of –5.000V.
4. GAIN ADJUSTMENT
   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust GAIN ADJ potentiometer for the positive full scale voltage of +9.9902V (Unipolar) or +4.9902V (Bipolar).

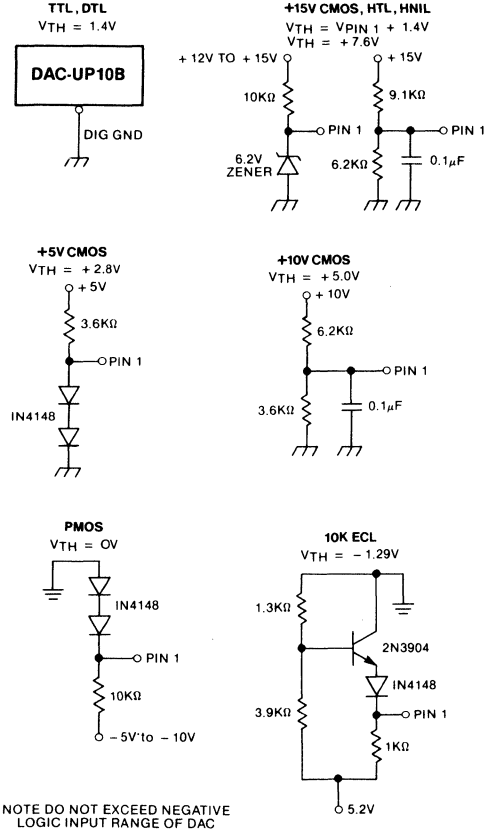
CODING TABLES

INPUT CODE			OUTPUT RANGES	
MSB		LSB	0 to +10V	±5V
1111	11	1111	+9.9902	+4.9902
1110	00	0000	+8.7500	+3.7500
1100	00	0000	+7.5000	+2.5000
1000	00	0000	+5.0000	0.0000
0100	00	0000	+2.5000	–2.5000
0010	00	0000	+1.2500	–3.7500
0000	00	0001	+0.0098	–4.9902
0000	00	0000	0.0000	–5.0000

OUTPUT RANGE SELECTION

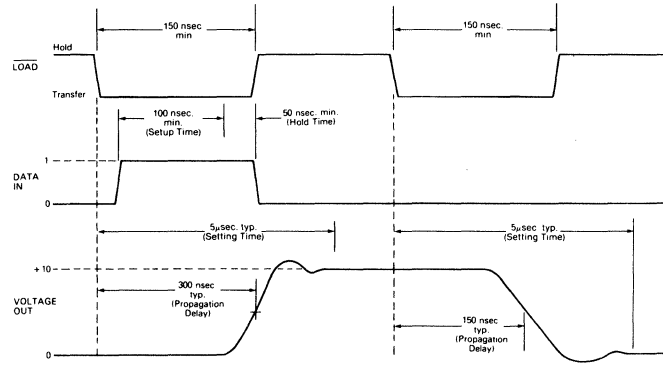
MODE	RANGE	CONNECTION
Unipolar	0 to ±10V	Pin 18 open
Bipolar	±5V	Pin 18 to Pin 20

LOGIC BIAS CIRCUITS



NOTE DO NOT EXCEED NEGATIVE LOGIC INPUT RANGE OF DAC

TIMING DIAGRAM



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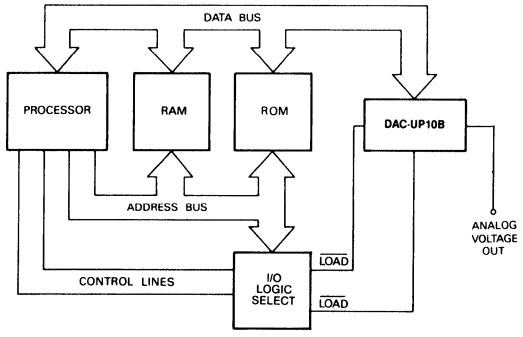
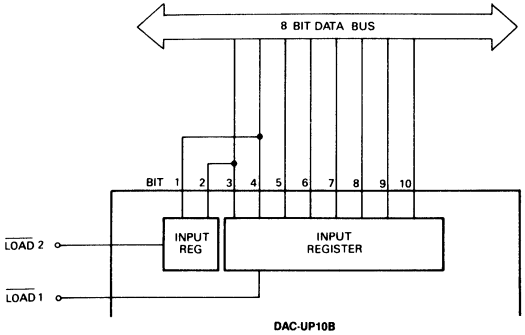
APPLICATIONS

INTERFACING TO A μPROCESSOR



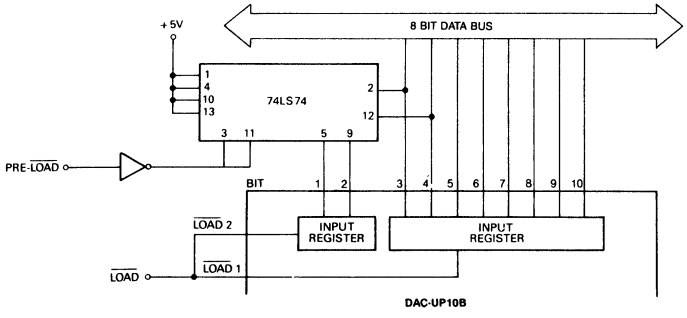
APPLICATIONS
Programmable Power Supplies
Test Equipment
Process and Control
Measurement Instruments
Computer I/O Equipment

INTERFACING TO 8 BIT DATA BUS



NOTE:
The independent $\overline{\text{LOAD}}$ lines allow the DAC-UP10B to be directly interfaced with an 8-bit data bus. Data for the two MSB's is supplied and stored when $\overline{\text{LOAD}}$ 2 is activated low and returned high according to the DAC-UP10B timing requirements. Then $\overline{\text{LOAD}}$ 1 is activated low and the remaining eight LSB's of data are transferred into the DAC-UP10B. When $\overline{\text{LOAD}}$ 1 returns high, the loading of a ten bit data word from an eight bit data bus is complete.

PRELOADING 2 MSB'S TO PROVIDE SINGLE STEP OUTPUT



NOTE:

Occasionally the analog output must change to its data value within one data address operation. This is no problem when using the DAC-UP10B with a data bus with 10 or more data bits. It can be accomplished from an 8-bit data bus by utilizing an external latch circuit to preload the two MSB data values. After preloading the external latch with the two MSB values, the DAC-UP10B $\overline{\text{LOAD}}$ inputs are activated low and the eight LSB's and two MSB's are concurrently loaded into the DAC-UP10B in one operation.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
DAC-UP10BC	0 to +70°C

ACCESSORIES Part Number	Description
TP10K, TP20K	Trimming Potentiometers

DAC-UP8B
8-Bit Monolithic D/A Converter with Input Register

DATEL

FEATURES

- **Input register**
- **Internal reference**
- **Voltage output**
- **Low cost**
- **8-Bit resolution**

GENERAL DESCRIPTION

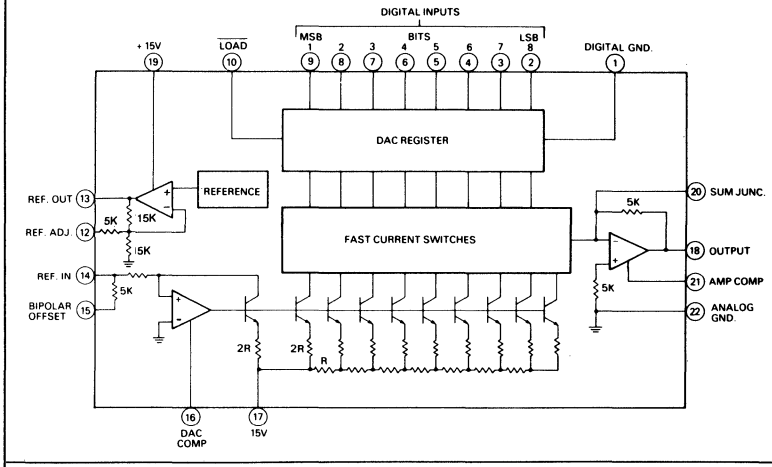
The DAC-UP8BC and DAC-UP8BM are 8-bit monolithic DAC's with internal registers. Contained in the 22-pin DIP is an 8-bit DAC, stable reference, a high-speed output amplifier and an 8-bit input latch. These microprocessor-compatible converters are ideal for low-cost applications.

The output voltage range is 0 to +10V for unipolar mode and ±5V for bipolar. Typical settling time is 2 microseconds for a full-scale change. Either the internal reference or an external reference can be used to bias the current switching network. The converter can function as a multiplying DAC by varying the reference input voltage. The reference and output amplifier are short circuit protected.

The input register is controlled by an enable line (LOAD). When low, the registers are transparent and any change on the digital input pins will be reflected on the analog output. A high state level will latch this digital information, and the data is retained until this enable line goes low. The data and latch enable input lines have low input load currents.

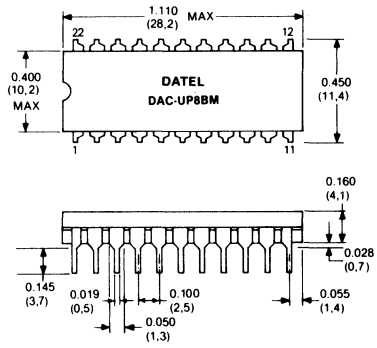
The DAC design consists of 8 fast-switching current sources, a diffused R-2R resistor ladder network and a control amplifier. The diffused resistor network gives excellent temperature tracking resulting in a gain temperature coefficient of 30 ppm/°C. This bipolar monolithic fabrication results in excellent linearity and temperature coefficient.

With an accuracy of 0.19% the device is monotonic (no missing codes) over the entire operating temperature range. Power supply requirements are ±12V to ±18V. The operating temperature range of the DAC-UP8BC is 0 to +70°C while the DAC-UP8BM operates from −55°C to +125°C.

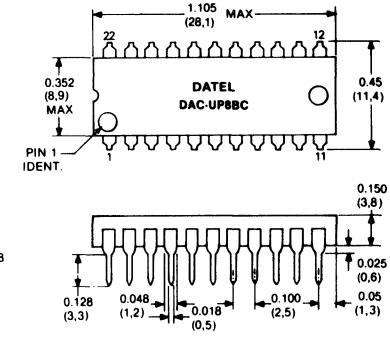


MECHANICAL DIMENSIONS
INCHES (MM)

CERAMIC PACKAGE
DAC-UP8BM



PLASTIC PACKAGE
DAC-UP8BC



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL GND	12	REF ADJ
2	BIT 8 IN (LSB)	13	REF OUT
3	BIT 7 IN	14	REF IN
4	BIT 6 IN	15	BIPOLAR OFFSET
5	BIT 5 IN	16	DAC COMP
6	BIT 4 IN	17	−15V
7	BIT 3 IN	18	OUTPUT
8	BIT 2 IN	19	+15V
9	BIT 1 IN (MSB)	20	SUM JUNCTION
10	LOAD	21	AMP COMP
11	NC	22	ANALOG GND

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ABSOLUTE MAXIMUM RATINGS

Positive Supply, pin 19	+18V
Negative Supply, pin 17	−18V
Digital Input Voltage, pins 2-10	+18V
Reference Input, pin 14	+12V
Summing Junction, pin 20	+12V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V Supply, Ref. In = +5V unless otherwise noted.

INPUTS	
Resolution	8 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary
Input Logic Level, bit ON ("1")	+2.0V to +5.5V at 10 μA
Input Logic Level, bit OFF ("0")	0V to +0.8V at −10 μA
Load Input	High ("1") = Hold Data Low ("0") = Transfer Data
Load Pulse Width[1]	150 nsec. minimum
Reference Input Voltage	+5V ±10%
Reference Input Resistance	5K
Reference Input Slew Rate	25V/μsec.
OUTPUT	
Output Voltage Range, unipolar	0 to +10V
Output Voltage Range, bipolar	±5V
Output Current	5 mA
Output Resistance	5 ohms
Reference Output Voltage	+5V ±10%
Reference Output Current	5 mA
PERFORMANCE	
Linearity Error	±½ LSB maximum
Differential Linearity Error	±½ LSB
Monotonicity	8 Bits over operating temperature range
Gain Error	Adjustable to zero
Zero Error	Adjustable to zero
Gain Tempco	20 ppm/°C
Zero Tempco, Unipolar	5 ppm/°C of FS.
Offset Tempco, Bipolar	10 ppm/°C of FS.
Reference Tempco	60 ppm/°C
Settling Time to ½ LSB[2]	2 μsec.
Power Supply Rejection	±1 mV/V
POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V dc
Power Supply Voltage Range	±12 to ±18V dc
Supply Current, quiescent	+7 mA, −10 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BC) 55°C to +125°C (BM)
Storage Temperature Range	−65°C to +150°C
Package Type	22 pin plastic (BC) 22 pin ceramic (BM)

FOOTNOTES:

1. See Timing Diagram
2. For 10V change

OUTPUT RANGE SELECTION

MODE	RANGE	CONNECTION
Unipolar	0 to +10V	Pin 15 open
Bipolar	±5V	Pin 15 to 20

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with 0.1 μf ceramic capacitors. This precaution will assure noise-free operation of the converter.
2. Both the Output (pin 18) and Reference Output (pin 13) are short circuit protected. Output short circuit current is typically 40 mA for the Output and 15 mA for the Reference Output.
3. The "LOAD" control pin is a level triggered input which causes the register to hold data with a logic "1" input state and transfer data to the DAC with a logic "0" input.
4. A Setup Time of 200 nanoseconds minimum must be allowed for the input data before the LOAD input goes from low to high. In addition, a 50 nanoseconds minimum Hold Time must be allowed for the input data after the LOAD input goes from low to high. The minimum pulse width for the LOAD input is 200 nanoseconds. The maximum update rate is determined by the output settling time. See the Timing Diagram.
5. The output settling time may be decreased somewhat by decreasing the value of the 50 pF feedback capacitor from the amplifier Output (pin 18) to the Summing Junction (pin 20). The minimum capacitance value is 10 pF.
6. The gain temperature coefficient of the DAC-UP8B without the internal reference is 20 ppm/°C. By using the internal reference, which has a tempco of 60 ppm/°C, a total tempco of 80 ppm typical results for the converter. If greater temperature stability is required, a more stable external reference should be used.
7. The data inputs (Bits 1 through 8) are high impedance inputs which give minimal logic loading. For an input low, the current that must be sinked is only 50 μA maximum, or about 1/32 of a standard TTL load. This minimizes the loading of the DAC-UP8B on a data bus.

CALIBRATION PROCEDURE

1. Select the desired output range and connect as shown in OUTPUT RANGE SELECTION table.
2. Apply a logic "0" to $\overline{\text{LOAD}}$ (pin 10).
3. **Zero and Offset Adjustments**

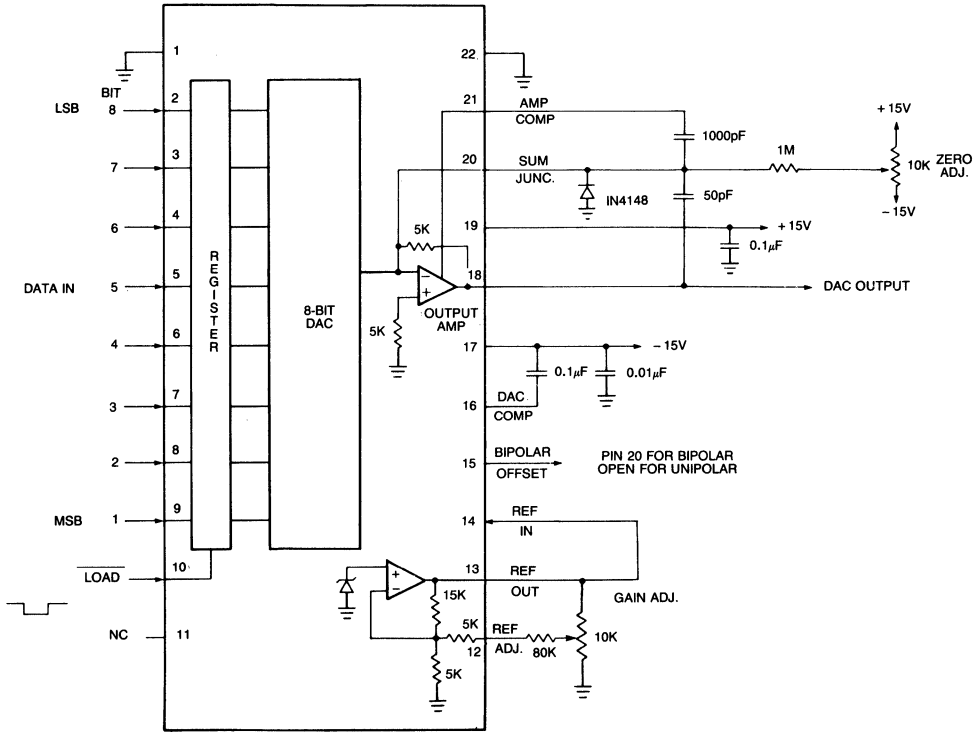
   For unipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for zero output voltage. For bipolar operation, set all digital inputs to "0" and adjust ZERO ADJ for negative full scale voltage of −5.000V.
4. **Gain Adjustment**

   For either unipolar or bipolar operation, set all digital inputs to "1" and adjust FULL SCALE ADJ for the positive full scale voltage of +9.961V (unipolar) or +4.961V (bipolar).

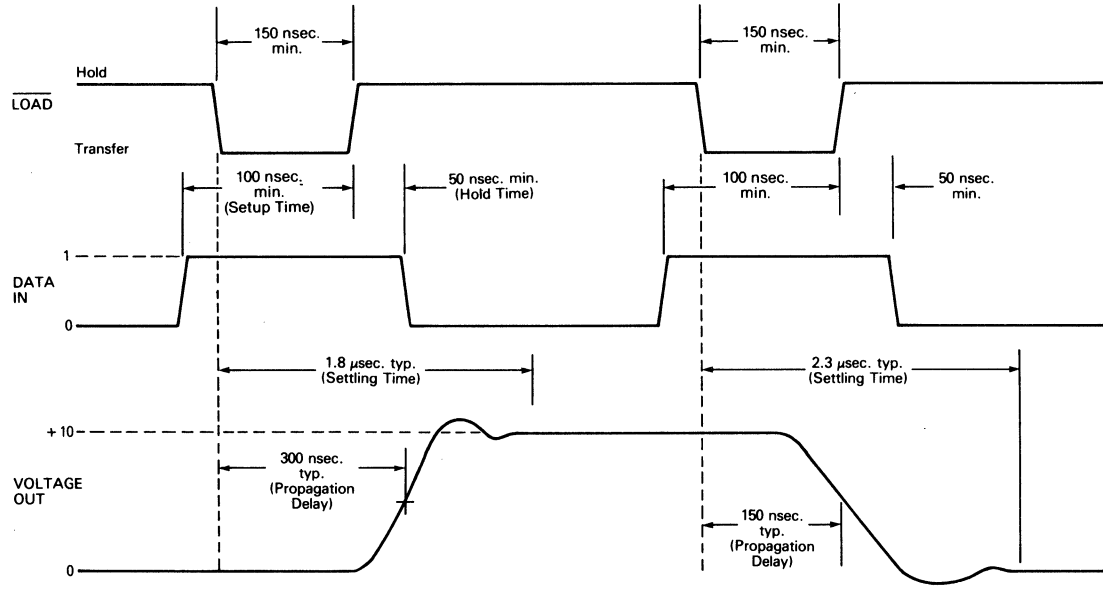
CODING TABLE

INPUT CODE MSB	INPUT CODE LSB	OUTPUT RANGES 0 to +10V	OUTPUT RANGES ±5V
1111	1111	+9.961V	+4.961V
1110	0000	+8.750	+3.750
1100	0000	+7.500	+2.500
1000	0000	+5.000	0.000
0100	0000	+2.500	−2.500
0000	0001	+0.039	−4.961
0000	0000	0.000	−5.000

CONNECTION AND CALIBRATION

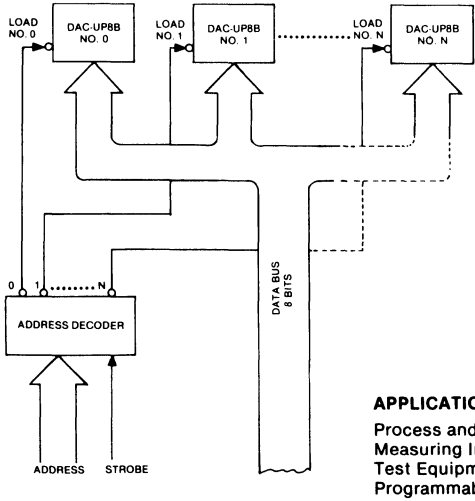


TIMING DIAGRAM



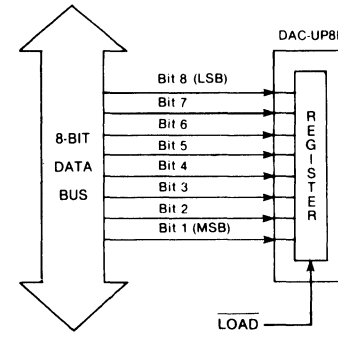
APPLICATIONS

INTERFACING TO 8 BIT DATA BUS



APPLICATIONS

Process and Control
Measuring Instruments
Test Equipment
Programmable Power Supplies
Computer I/O Equipment



This illustrates the connection for loading parallel data into the input register. The register circuit is a static latch and is controlled by the $\overline{\text{LOAD}}$, active low. When the data is stable on the data inputs (bits 1-8), it can be transferred on the positive edge of the $\overline{\text{LOAD}}$ pulse. The voltage levels on the data bus should be stable for at least 200 nsec before $\overline{\text{LOAD}}$ goes HI. The minimum pulse width of the $\overline{\text{LOAD}}$ command is 200 nsec.

2

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	CASE
DAC-UP8BC	0 to 70°C	Plastic
DAC-UP8BM	−55 to 125°C	Ceramic

ACCESSORIES

Part Number	Description
TP10K	Trimming Potentiometers

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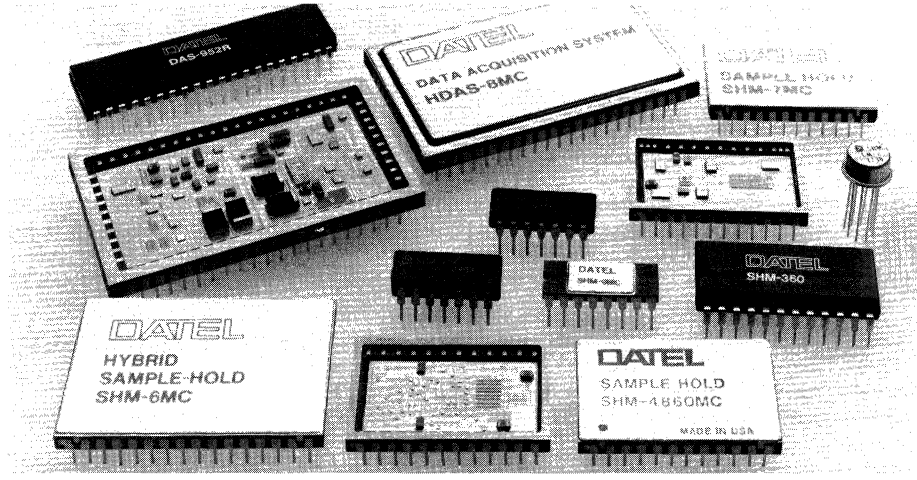
SAMPLE-AND-HOLD AMPLIFIERS



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SAMPLE/HOLD AMPLIFIERS

MODEL	LINEARITY	ACQUISITION TIME	APERTURE DELAY	INPUT RANGE	HOLD-MODE DROOP	BANDWIDTH	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
SHM-91MC	0.003%	2 µs	15 ns	±10V	5 µV/µs	1 MHz	24-pin DIP Hybrid	0 to +70	3-37
SHM-91MM								-55 to +125	
SHM-45MC	0.01%	200 ns	6 ns	±5,±10V	0.5 µV/µs	16 MHz	24-pin DIP Hybrid	0 to +70	3-15
SHM-45MM								-55 to +125	
SHM-4860MC	0.01%	200 ns	6 ns	±10V	0.5 µV/µs	16 MHz	24-pin DIP Hybrid	0 to +70	3-19
SHM-4860MM								-55 to +125	
SHM-5	0.01%	350 ns	20 ns	±10V	20 µV/µs	5 MHz	2 x 2 x 0.375in (50x50x10mm) Module	0 to +70	3-22
SHM-20C	0.01%	1 µs	30 ns	±10V	0.08 µV/µs	2 MHz	14-pin DIP Monolithic	0 to +70	3-3
SHM-IC-1	0.01%	5 µs	50 ns	±10V	50 µV/ms	2 MHz	14-pin DIP Monolithic	0 to +70	3-43
SHM-IC-1M								-55 to +125	
SHM-LM-2	0.01%	6 µs	200 ns	±10V	0.2 mV/ms	1 MHz	8-pin TO-99 Monolithic	0 to +70	3-47
SHM-6MC	0.02%	2 µs	20 ns	±10V	10µV/µs	5 MHz	32-pin DIP Hybrid	0 to +70	3-24
SHM-6MM								-55 to +100	
SHM-9MC	0.01%	6 µs	200 ns	±11.5V	0.2 mV/ms	4 MHz	16-pin DIP Hybrid	0 to +70	3-32
SHM-9MM								-55 to +125	
SHM-UH3	0.05%	30 ns	5 ns	±5V	50 µV/µs	45 MHz	2 x 2 x 0.375in (50x50x10 mm) Module	0 to +70	3-49
SHM-HUMC	0.01%	25 ns	6 ns	±2.5V	50 µV/µs	50 MHz	24-pin DIP Hybrid	0 to +70	3-41
SHM-HUMM								-55 to +100	
SHM-7MC	0.01%	40 ns	3 ns	±5V,±2.5V	100 µV/µs	40 MHz	24-pin DIP Hybrid	0 to +70	3-28
SHM-40MC	0.01%	40 ns	3 ns	±2.5V	100 µV/µs	40 MHz	24-pin DIP Hybrid	0 to +70	3-11
SHM-40MM								-55 to +125	
SHM-360	0.15%	20 ns	–	±3V	10 mV/µs	25 MHz	24-pin DIP Monolithic	-20 to +75	3-7
SHM-361		12 ns				55 MHz			
SHM-30C	0.01%	500 ns	20 ns	±10V	0.01 µV/µs	4.5 MHz	14-pin DIP Monolithic	0 to +70	—

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SHM-20
High Speed, 0.01% Monolithic Sample/Hold

FEATURES

- **Internal hold capacitor**
- **1 Microsecond acquisition time**
- **1 Nanosecond aperture uncertainty**
- **0.01% Accuracy**
- **0.08 MicroV/Microsecond droop rate**
- **Differential inputs**

GENERAL DESCRIPTION

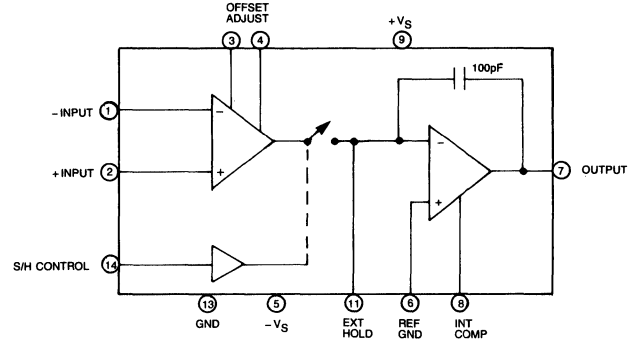
DATEL's SHM-20 is a low-cost, complete monolithic sample/hold amplifier which includes an internal 100 pF MOS hold capacitor. Primarily designed for high speed analog signal processing applications, the SHM-20 features a typical acquisition time of 1.0 microsecond for a 10V input step to 0.01%. Aperture uncertainty is typically 1 nanosecond and droop rate is as low as 0.08 μV/microsecond.

The SHM-20 consists of an input transconductance amplifier, a low leakage analog switch, an output integrating amplifier and a 100 pF MOS hold capacitor. Charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by using the offset adjust inputs. For improved droop rate, an external hold capacitor may be added at the expense of acquisition time.

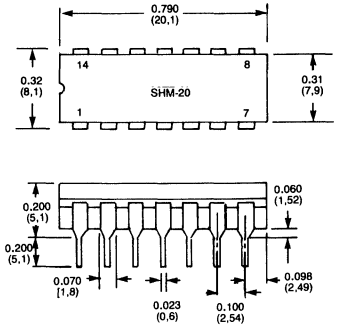
Other important features of the SHM-20 include a 30 nanosecond aperture delay time, 1 mV pedestal error, a minimum dc gain of 10^6V/V and fully differential inputs with a $\pm$10V input voltage range. Maximum input offset voltage is as low as 0.5 mV with a maximum input offset voltage drift as low as 15 μV/°C.

Its low cost and high performance make the SHM-20 an excellent choice for innumerable applications including, precision data acquisition systems, deglitching circuits, auto-zero circuits, data distribution systems and peak amplitude detectors. Power requirement is $\pm$15V dc.

The SHM-20 is available in two models for operation over the commercial, 0°C to +70°C, and military, −55°C to +125°C temperature ranges. Both models are packaged in a 14-pin ceramic DIP.



MECHANICAL DIMENSIONS INCHES (MM) MAX.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−INPUT
2	+INPUT
3	OFFSET ADJUST
4	OFFSET ADJUST
5	$-V_S$
6	REFERENCE GROUND
7	OUTPUT
8	INTEGRATOR COMPENSATION
9	$+V_S$
10	NO CONNECTION
11	EXTERNAL HOLD CAPACITOR
12	NO CONNECTION
13	SUPPLY VOLTAGE GROUND
14	S/H CONTROL

ABSOLUTE MAXIMUM RATINGS, BOTH MODELS	SHM-20C SHM-20M
Voltage between Supply Pins (Pins 9, 5)	40V
Differential Input Voltage	±24V
Digital Input Voltage, Pin 14	+8V to −15V
Output Current, Continuous[1]	±20 mA

FUNCTIONAL SPECIFICATIONS, BOTH MODELS

Typical at +25°C, ±15V dc, using internal hold capacitor, unless otherwise noted.

ANALOG INPUTS	SHM-20C	SHM-20M
Input Voltage Range,[2] minimum	±10V	
Input Impedance, minimum	1 MΩ	
Input Capacitance, maximum	3 pF	
Input Offset Voltage, maximum	1 mV	0.5 mV
Input Offset Voltage Drift, maximum	20 μV/°C	15 μV/°C
Input Bias Current, maximum	300 nA	200 nA
Input Offset Current, maximum	300 nA	100 nA
DIGITAL INPUTS[2]		
Logic Level High, Vin ("1"), minimum, Hold Mode	2.0V	
Logic Level Low, Vin ("0"), maximum, Sample Mode	0.8V	
High Level Input Current, maximum	0.1 μA	
Low Level Input Current, maximum	10 μA	
OUTPUT		
Output Voltage Range[2], minimum	±10V	
Output Current[2], minimum	±10 mA	
Output Impedance, Hold Mode[2]	1 Ω	
PERFORMANCE		
Accuracy	0.01%	
DC Gain, minimum	3×10^5 V/V	10^6 V/V
Gain Accuracy[4]	0.5×10^{-4}%FSR	
Gain Error Tempco	±0.6 ppm/°C	
Gain Bandwidth Product[5]	2 MHz	
Hold Mode Feedthrough, 10V P-P, 100 kHz[2]	2 mV	
Droop Rate	0.08 μV/μsec.	
Droop Rate[2]	1.2μV/μsec.	17 μV/μsec.
Charge Transfer[6]	0.1 pc	
Pedestal Error	1 mV	
Total Output Noise, DC to 10 MHz, maximum	200 μV RMS	
Power Supply Rejection Ratio, minimum +VS	80 dB	
−VS	65 dB	
Pedestal Error	1 mV	
DYNAMIC CHARACTERISTICS		
Acquisition Time, 10V to 0.1%	0.8 μsec.	
10V to 0.01%	1.0 μsec.	
Aperture Delay Time	30 nsec.	
Aperture Uncertainty Time	1 nsec.	
Aperture Time	25 nsec.	
Hold Mode Settling Time, 0.01%[2]	185 nsec.	
Rise Time	100 nsec.	
Overshoot	15%	
Slew Rate[7]	45 V/μsec.	
POWER REQUIREMENTS[8]		
Positive Supply, Pin 9	+15V ±0.5V at 11 mA	
Negative Supply, Pin 5	−15V ±0.5V at −11 mA	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Ranges,	
SHM-20C	0°C to +70°C
SHM-20M	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C
Package Type	14 Pin, Ceramic DIP

FOOTNOTES:

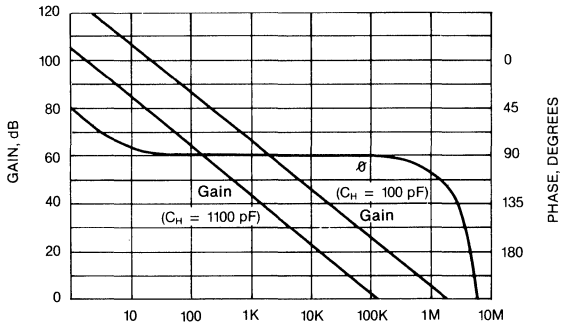
1. Internal power dissipation may limit output current below +20 mA.
2. Over full operating temperature range.
3. Cannot tolerate even a momentary short circuit to ground or either supply.
4. Voltage gain = +1
5. Voltage gain = +1, load resistance = 1 kΩ, load capacitance = 50 pF, output voltage = 100 mV P-P.
6. Input voltage = 0V, digital input voltage = 3.5V
7. Output voltage = 10V step.
8. A power supply voltage as low as ±12V may be used. However, this will cause some degradation in performance.

TECHNICAL NOTES

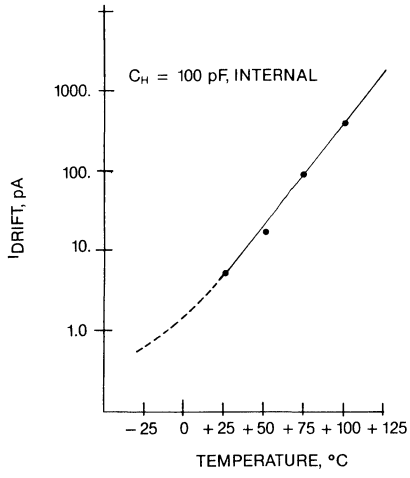
1. A printed circuit board with ground plane is recommended for best performance. The supply pins (Pins 5,9) should be bypassed to ground with a 0.01 to 0.1 μF ceramic capacitor as close to the pins as possible.
2. If an external hold capacitor (C_H) is used, 8 then a noise bandwidth capacitor with a value of 0.1 C_H (10% of the value of the external hold capacitor) should be connected from Pin 8 to ground. Exact value and type are not critical.
3. The Hold Capacitor (C_H) should have high insulation resistance and low dielectric absorption to minimize droop error. For operating temperatures up to 70°C, polystyrene dielectric is a good choice. Any PC connections to the hold capacitor terminal (Pin 11) should be kept short and "guarded" by the ground plane to avoid errors due to drift currents from nearby signal lines or power supply voltages.

TYPICAL PERFORMANCE AND DEFINITIONS

OPEN LOOP GAIN AND PHASE RESPONSE



DRIFT CURRENT VS. TEMPERATURE



SAMPLE AND HOLD DEFINITIONS:

ACQUISITION TIME: The time required, after the sample command is given, for the hold capacitor to charge to a full-scale voltage change and then remain within a specified error band around the final value.

APERTURE TIME: The time required for the Sample & Hold switch to open, independent of delays through the switch driver and input amplifier circuitry.

APERTURE DELAY TIME: The time elapsed from the hold command to the actual opening of the sampling switch.

APERTURE UNCERTAINTY TIME: The time variation, or time jitter, in the opening of the sampling switch; also the variation in aperture delay time from sample to sample.

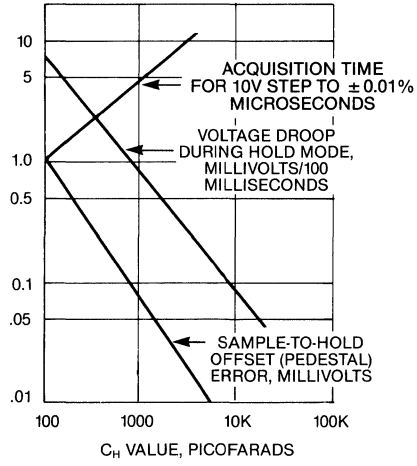
CHARGE TRANSFER: The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the hold mode. This is caused by the switch control voltage change coupling through switch capacitance to the hold capacitor. Also called charge dumping or charge injection.

DRIFT CURRENT: The net leakage current from the hold capacitor during hold mode.

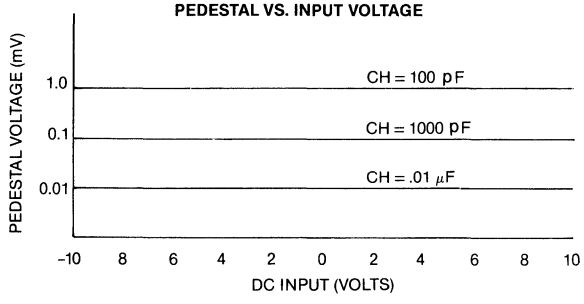
HOLD MODE DROOP: The output voltage change per unit time with the sampling switch open. Commonly expressed in V/seconds or μV/microseconds

PEDESTAL ERROR: For a sample-hold, the change in output voltage from the sample-mode to the hold-mode, with constant input voltage. This error is caused by the sampling switch transferring charge onto the hold capacitor as it opens.

TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR

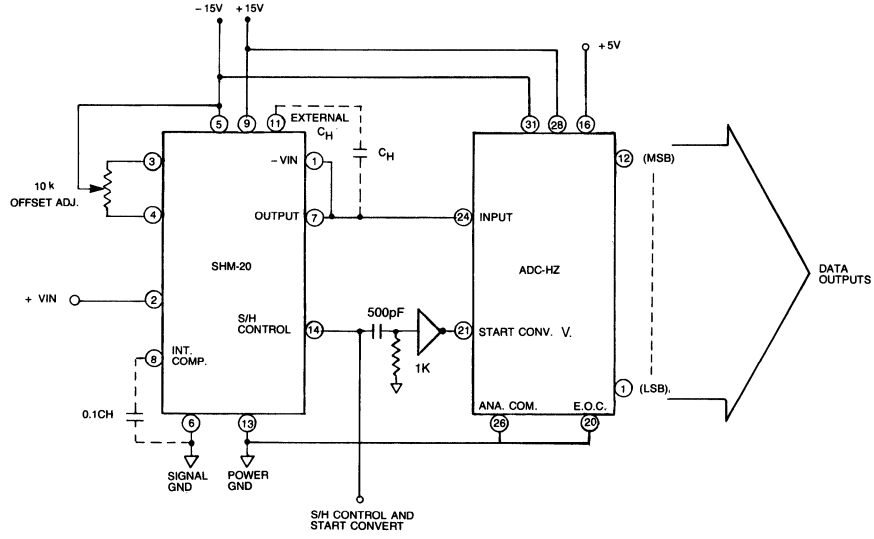


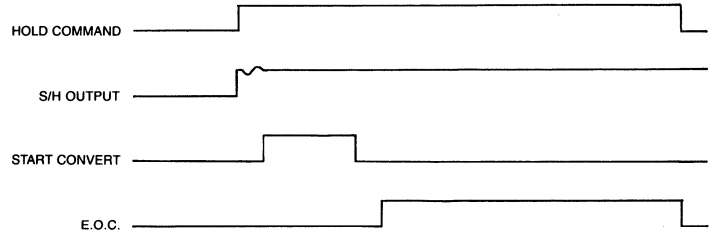
PEDESTAL VS. INPUT VOLTAGE



APPLICATION

UNITY GAIN NON-INVERTING S/H AMPLIFIER





The above diagram shows the SHM-20 connected as a unity gain non-inverting S/H amplifier, with DATEL's ADC-HZ 12-bit successive approximation A/D converter. The SHM-20's pedestal error is adjustable to zero, by the offset adjust trim pot, allowing a 12-bit accurate output from the ADC-HZ.

If an external hold capacitor (C_H) is required, it may be connected as shown between Pins 11 and 7. If an external hold capacitor is used, a capacitor, 0.1 C_H (10% of the value of the external hold capacitor) is then required from Pin 8 to ground to reduce output noise in hold mode. The RC network on Pin 14 delays the S/H Control/Start Convert pulse to allow the sample to hold transient time to settle before a conversion begins. See Timing Diagram.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-20C	0°C to +70°C
SHM-20M	-55°C to +125°C

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SHM-360, SHM-361
Video Speed Sample-Holds

FEATURES

- **8 nSec. and 12 nSec. acquisition times**
- **Sampling frequencies of 18 MHz and 35 MHz**
- **Input amplifier bandwidths of 25 MHz and 55 MHz**
- **Linearity 0.08%**
- **Low power**

GENERAL DESCRIPTION

The SHM-360 and SHM-361 are two very high speed sample/hold devices featuring separate wideband input amplifiers, and reference voltage and clock outputs. The two devices are pin-for-pin identical.

Both devices offer very fast S/H capabilities for A/D's such as the ADC-300 and ADC-303, but can be used in any application demanding very fast acquisition times.

The input amplifier has a – 3 dB bandwidth at 25 MHz or 55 MHz depending on the device used and both have offset adjustment controls.

An internal amplifier may be used to buffer a – 2V dc reference voltage output for an A/D converter.

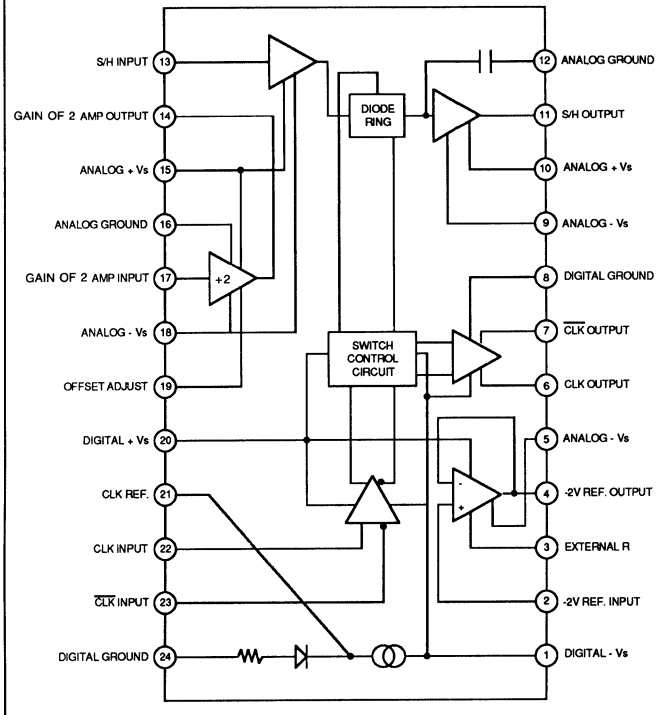
The single or 2-phase clock inputs are available as buffered outputs for use as high speed video analog-to-digital converter clock inputs.

APPLICATIONS

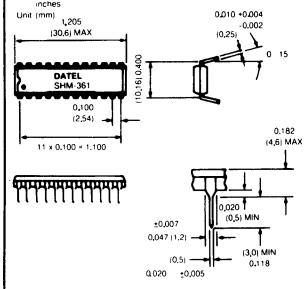
- **High speed data acquisition**
- **Radar pulse analysis**
- **TV video encoding**
- **Infrared imaging**
- **Transient analysis**
- **Medical electronics**
- **Fluid flow analysis**
- **Sonar systems**

ORDERING INFORMATION

MODEL NO.	OPERATING TEMPERATURE RANGE
SHM-360	–20°C to +75°C
SHM-361	–20°C to +75°C



MECHANICAL DIMENSIONS



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL –Vs (–5V)	24	DIGITAL GROUND
2	REF. INPUT (–2V)	23	$\overline{\text{CLOCK}}$ INPUT
3	EXTERNAL R	22	CLOCK INPUT
4	REF. OUTPUT (–2V)	21	CLOCK REF. OUTPUT
5	ANALOG –Vs (–5V)	20	DIGITAL +Vs (+5V)
6	CLOCK OUTPUT	19	OFFSET ADJUST
7	$\overline{\text{CLOCK}}$ OUTPUT	18	ANALOG –Vs (–5V)
8	DIGITAL GROUND	17	GAIN OF 2 AMP. INPUT
9	ANALOG –Vs (–5V)	16	ANALOG GROUND
10	ANALOG +Vs (+5V)	15	ANALOG +Vs (+5V)
11	S/H OUTPUT	14	GAIN OF 2 AMP. OUTPUT
12	ANALOG GROUND	13	S/H INPUT

ABSOLUTE MAXIMUM RATINGS	
Operating Voltage ±V_S	+5.5
$-V_S$	−6.0V
Operating Temperature	20°C to +75°C
Storage Temperature	−55°C to +150°C
Power Dissipation	1.2 Watts

FUNCTIONAL SPECIFICATIONS, SHM-360, SHM-361

Typical at +25°C, V_S = ±5V dc unless otherwise stated.

INPUTS	MIN.	TYP.	MAX.	UNIT
Analog Input Voltage Range	−3.0	±3.0	+3.0	V
Input Impedance	60	100	—	KΩ
Digital Input VH	−0.9	−0.80	—	V
VL	—	-1.60	-1.5	V
OUTPUTS				
Analog Range	−3.0	—	+3.0	V
Output Impedance	—	20	40	Ω
Clock (Reference)	−1.3	−1.2	−1.1	V
Reference Buffer Range	0	−2.0	−2.3	V
Clock — Amplitude	0.2	0.3	0.4	V
— Low Level	−1.2	−1.1	11.9	V
— Rise Time (Tr)	—	7	10	nSec.
— Fall Time (Tf)	—	5	8	nSec.

POWER	SHM-361			SHM-360			
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Supply Voltage +Vs	—	5.0	—	—	5.0	—	V
−Vs	—	−5.0	—	—	−5.0	—	V
Supply Current +Is	48	60	78	25	35	45	mA
−Is (No Ref)	48	60	78	25	35	45	mA
−Is (with Ref)	80	100	125	60	75	98	mA
P.S.R.R.	—	−40	—	—	−70	—	dB
PERFORMANCE	**SHM-361**			**SHM-360**			
SAMPLE/HOLD	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Acquisition Time	—	8	12	—	12	20	nSec.
Settling Time	—	25	—	—	36	—	nSec.
Linearity	—	0.08	0.15	—	0.08	0.15	%
Droop	—	2	20	—	2	10	mV/μS
Sampling Rate	5	—	35	2	—	18	MHz
Gain	0.99	1.00	1.01	0.99	1.0	1.01	
Full Power Bandwidth (−3 dB, V_{IN} = 2V p-p)	—	12	—	—	6	—	MHz
Hold Feedthrough	—	−50	−40	—	−50	−40	dB
Sample-to-hold Transient	—	10	50	—	10	50	mV
DC Offset	—	±15	±100	—	±15	±100	mV
Diff. Gain	—	0.5	1.0	—	0.5	1.0	%
Diff. Phase	—	0.5	1.0	—	0.5	1.0	Deg
Input Bias Current	—	15	30	—	9	18	μA
GAIN OF 2 AMP							
Bandwidth (−3db, V_{IN} = 1V p-p)	45	55	—	15	25	—	MHz
Input Voltage Range	−1.3	—	+0.8	−1.3	—	+0.8	V
Imput Impedance	10	20	—	10	20	—	KΩ
Output Impedance	—	4	10	—	4	10	Ω
Voltage Gain	5.1	6.0	6.9	5.1	6.0	6.9	dB
Input Bias Current	—	9	20	—	5	10	μA
CLOCK OUTPUT							
Clock Delay T1	20	28	34	36	38	45	nSec.
Clock Delay T2	14	22	28	24	26	33	nSec.
−2V REF AMP							
Voltage Gain Ratio	0.9	1.0	1.1	0.9	1.0	1.1	
Input Bias Current	—	5	10	—	5	10	μA
Output Impedance	—	2	10	—	2	10	Ω

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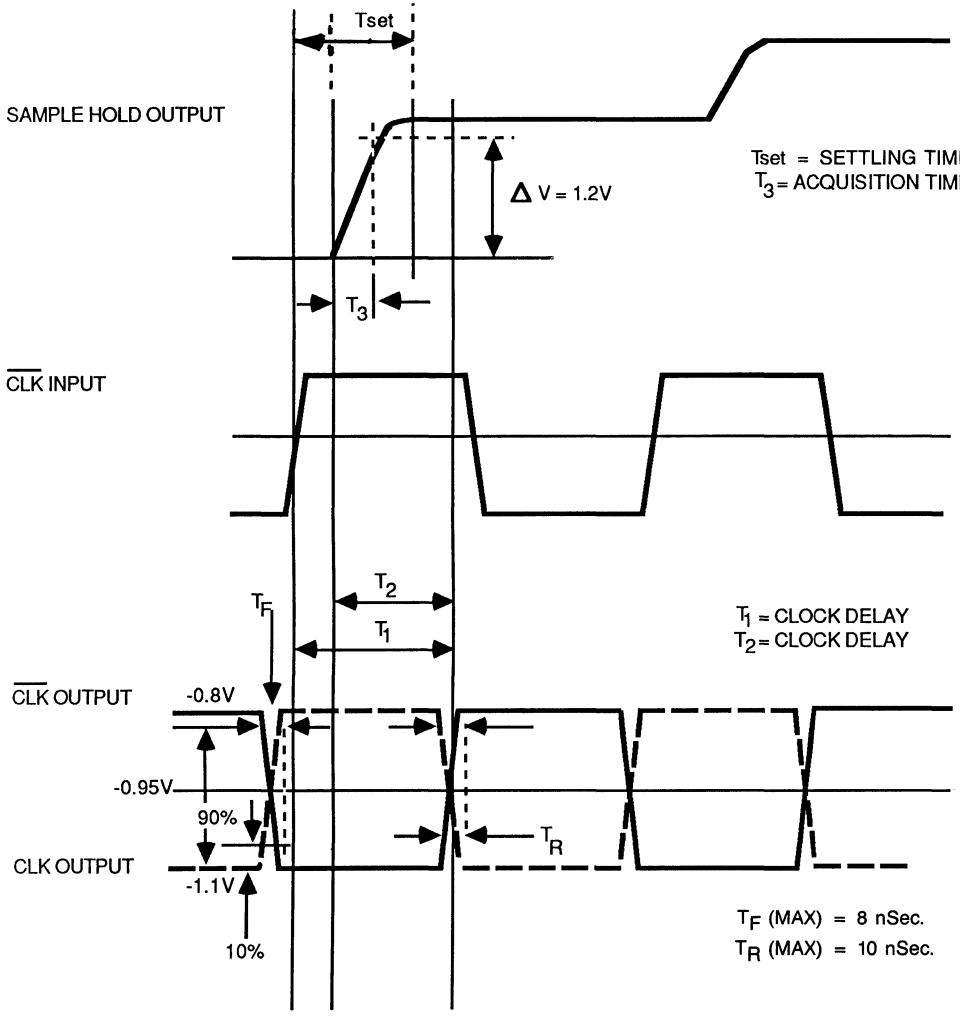
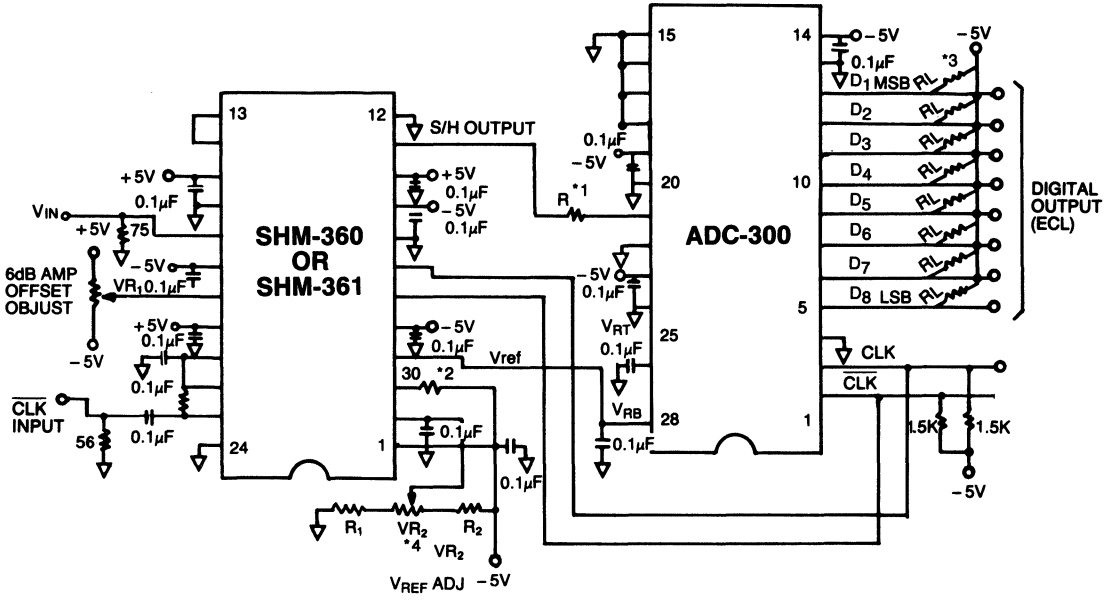
TIMING DIAGRAM (NOT DRAWN TO SCALE)



TIMING DIAGRAM NOTES

1. The hold to sample transition occurs 6 nSecs. for the SHM-361 and 12 nSecs. for the SHM-360, after positive edge of the clock input.
2. Acquisition times for the two devices are 12 nSecs. (max.) for the SHM-361 and 20 nSecs. (max.) for the SHM-360 for a change of 1.2V at the analog input.
3. Sample-to-hold transient is 50 mV (max.) for the SHM-361 and 30 mV (max.) for the SHM-360.
4. To achieve the correct timing the CLOCK and $\overline{\text{CLOCK}}$ outputs are delayed. For the SHM-361, the delay will be between 20 nSecs. and 34 nSecs. and for the SHM-360 it will be between 36 nSecs. and 45 nSecs.

CONNECTION AND APPLICATION



NOTES:

*1 R is a ringing preventing resistor. Select between 10 to 50Ω according to pattern length.
*2 Pulldown R for V_{ref}.
*3 R_L = 4.3kΩ.
*4 R1 = 2kΩ, R2 = 1kΩ, R3 = 2kΩ.

SHM-40
Video Speed Sample-Hold

FEATURES

- **40 nSec acquisition time**
- **Dual outputs**
- **10 pSec aperture uncertainty**
- **40 MHz bandwidth**
- **30 mA Output Current**

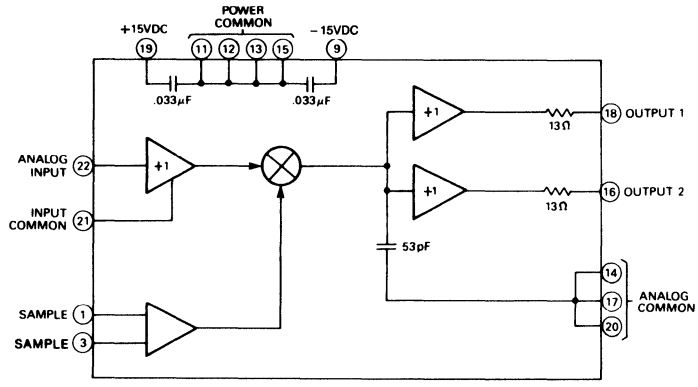
GENERAL DESCRIPTION

DATEL's SHM-40 is an ultra-fast sample and hold designed for high speed analog signal processing applications. The SHM-40 acquires a 2V input change to 0.1% in only 40 nsec and aperture uncertainty time is less than 10 psec. Sample-mode bandwidth is 40 MHz.

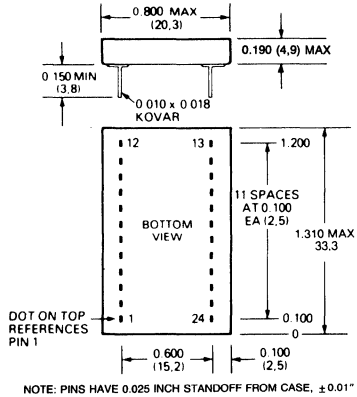
The SHM-40 is a complete Sample-Hold, containing an input buffer amplifier, a precision 53 pF MOS holding capacitor, and two output buffer amplifiers. The sampling switch is controlled by a series 10,000 complementary ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

Other features of the SHM-40 include a ±2.5V input voltage range, a fixed gain of +0.995, and a maximum gain temperature coefficient of 33 ppm/°C. The device has two outputs, each with a ±2.5V output voltage swing at 30 mA and an output impedance of only 13Ω. The outputs may be tied together for decreased output impedance and increased output current. The SHM-40 is functionally laser trimmed at the factory for offset, sample to hold offset, and gain errors, and is designed to be used without external adjustment circuits.

The SHM-40 is an ideal choice for use in ultra-high speed data acquisition systems, and video processing applications, and with its dual outputs, it is especially useful in two stage flash converter systems. Power requirement is ±15Vdc at 60 mA. Two models are available for operation over the 0°C to 70°C and −55°C to +125°C temperature ranges. All models are cased in a 24-pin, hermetically sealed, ceramic package.



MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SAMPLE	13	POWER COM.
2	N.C.	14	ANALOG COM.
3	SAMPLE	15	POWER COM.
4	N.C.	16	OUTPUT 2
5	N.C.	17	ANALOG COM.
6	N.C.	18	OUTPUT 1
7	N.C.	19	+ 15VDC
8	N.C.	20	ANALOG COM.
9	− 15VDC	21	INPUT COM.
10	N.C.	22	ANALOG INPUT
11	POWER COM.	23	N.C.
12	POWER COM.	24	N.C.

ABSOLUTE MAXIMUM RATINGS

Positive Supply	-0.5V dc to +18V dc
Negative Supply	+0.5V dc to -18V dc
Digital Input Voltage	-5.0V dc to +5.0V dc
Analog Input Voltage	-5.0V dc to +5.0V dc

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the full operating temperature range and power supply range unless otherwise specified.

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
INPUTS				
Input Voltage Range	±2.5	-	-	Vdc
Input Bias Current	-	±30	±100	μA
Input Impedance	100K	1M	-	Ω
Max Source Impedance①	-		50	Ω
Sample Control Inputs②	-	-	-	-
OUTPUTS				
Output Voltage Range	±2.5	-	-	Vdc
Output Current③	±30	±60	-	mA
Output Impedance③	8	13	20	Ω
PERFORMANCE				
Linearity	-	.1%	.2%	% of FS
Gain	+0.980	+0.993	+1.0	-
Gain Tempco	-60	-20	+20	ppm/°C
Sample to Hold Offset Error	-	±15	±50	mV
Sample Mode Offset Voltage	-	±10	±50	mV
Sample to Hold Offset Volt Drift	-	±25	±100	μV/°C
Sample Mode Offset Volt Drift	-	-	-	-
SHM-40MC	-	±143	±714	μV/°C
SHM-40MM	-	±56	±278	μV/°C
	-			
Hold Mode Feedthrough	-	-66	-60	dB
Hold Mode Droop	-	-	-	-
at 25°C	-	20	100	μV/μS
at 125°C	-	500	2500	μV/μS
	-			
DYNAMIC CHARACTERISTICS				
Acquisition Time				
2V to 0.1&	-	-	40	nS
2V to 1.0%	-	-	25	nS
4V to 0.1%	-	-	50	nS
4V to 1.0%	-	-	35	nS
Aperture Delay Time	-	3	-	nS
Aperture Uncertainty Time	-	10	-	pS
Hold Mode Settling Time	-	20	40	nS
Sample Mode Bandwidth, -3dB	25	40	-	MHz

FUNCTIONAL SPECIFICATIONS (continued)

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range ±V	±14.5	±15	±15.5	Vdc
Power Supply Rej. Ratio	-20	-30	-	dB
Current Drain				
±15V dc	-	60	80	mA
-15V dc	-	60	80	mA
Power Dissipation	-	1.8	2.4	Watts
PHYSICAL/ENVIRONMENTAL				
Thermal Resistance				
Junction to Case	-	.030	-	°C/mW
Case to Ambient	-	.035	-	°C/mW
Operating Temp. Range				
SHM-40MC	0°	+25°	+70°	°C
SHM-40MM	-55°	+25°	+125°	°C
Storage Temp.	-65°	+25°	+150°	°C
Package Type Pins	24 Pin, hermetically sealed, ceramic 0.010 x 0.018 in. kovar			

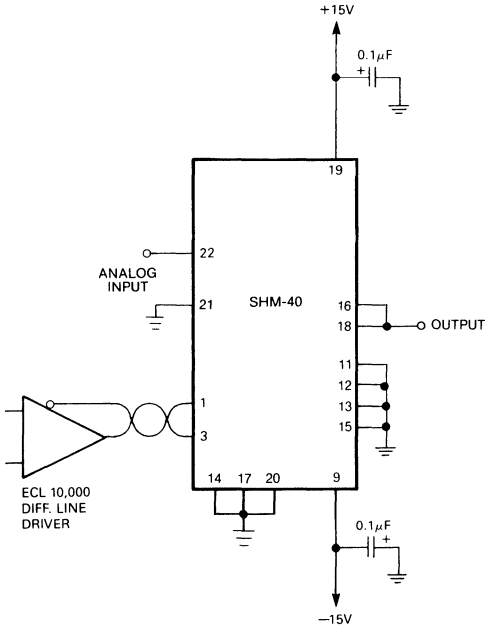
FOOTNOTES:

1. Should be purely resistive. See technical note 3.
2. Input logic voltage levels are V_{in} "0" = -1.5V to -1.4V, and V_{in} "1" = -0.7V to -1.05V. These are differential ECL 10,000.
3. Specified for each output, both outputs may be tied together for decreased output impedance and increased output current.

TECHNICAL NOTES

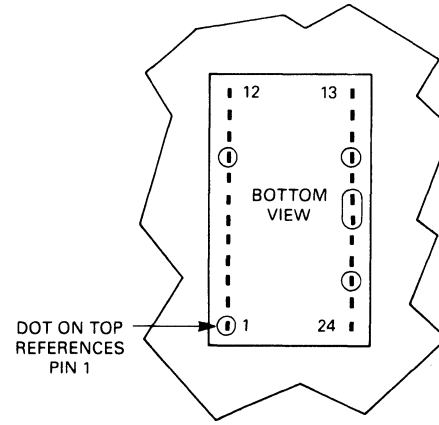
1. The use of good high frequency circuit board layout techniques is required for rated performance. The power common (Pins 11, 12, 13 and 15), analog common (Pins 14, 17 and 20), and input common (Pin 21) pins are not connected internally and therefore must be connected externally as directly as possible through a low inductance, low resistance path. The extensive use of a ground plane for all common connections is highly recommended.
2. Although they are internally bypassed with .033 μF capacitors the supply pins (Pins 19, 9) should be externally bypassed with 0.1 μF ceramic chip capacitors mounted as close to the supply pins as possible.
3. The SHM-40 inputs and outputs are sensitive to unusual loading or long lines. The analog input must be non-reactive so that leads should be short and purely resistive. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.
4. The maximum, differential, digital input voltage is ±5V. For example, if pin 3 is at a potential of -5V, pin 1 may not exceed 0V.
5. The SHM-40 has no significant acquisition time drift with temperature.
6. A positive pulse on Pin 3 and a negative pulse on Pin 1 selects the HOLD mode.

TYPICAL CONNECTION



6. Hold-Mode Droop
   The output voltage change per unit of time while in the hold mode.
7. Bandwidth
   The frequency at which the gain is down 3 dB from its dc value. It's measured in the sample-mode with a small-signal sine wave.

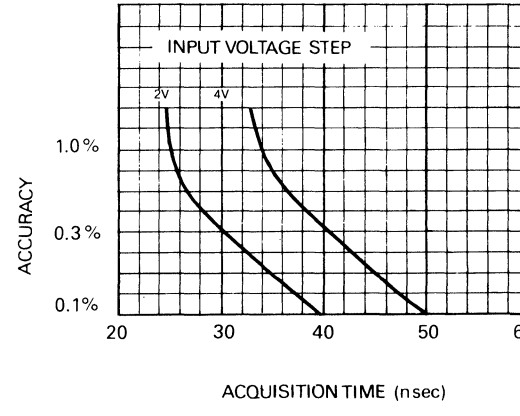
BASIC GROUND PLANE LAYOUT



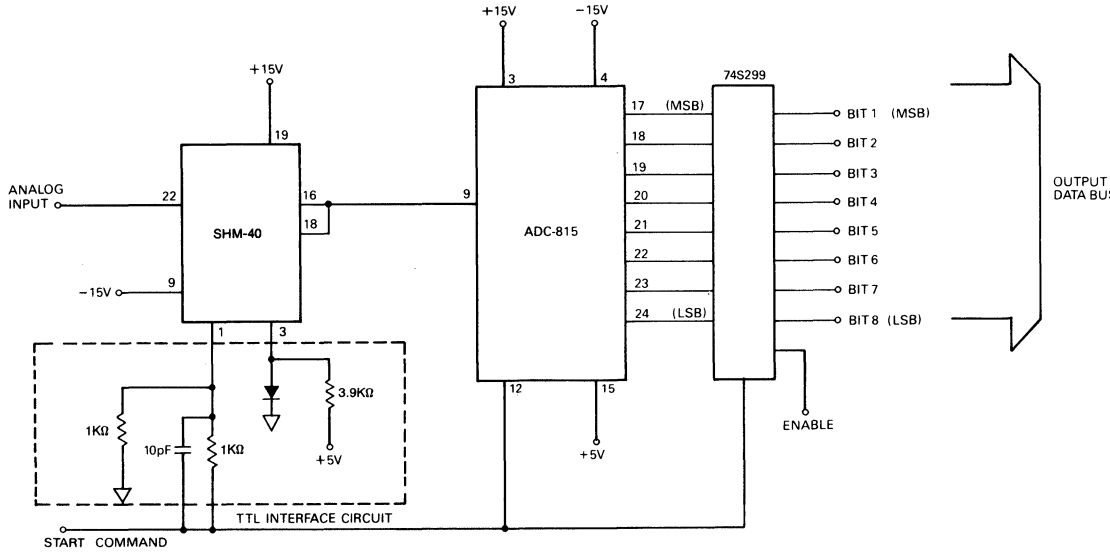
SAMPLE-HOLD DEFINITIONS

1. Acquisition Time
   Time required, after receipt of the sample command, for the hold capacitor to charge to a specified voltage change and remain within a specified error band such as 0.1%.
2. Aperture Delay Time (effective)
   The time elapsed from the hold command to the opening of the sampling switch minus the delay from the analog input to the sample switch.
3. Aperture Uncertainty Time
   Time variation, or jitter, in the opening of the sampling switch.
4. Aperture Uncertainty Error
   An amplitude uncertainty in the held value due to the change in the analog input signal during the aperture uncertainty time. This error is the product of the rate of change of the input signal and the aperture uncertainty time.
5. Hold-Mode Settling Time
   The time from the hold command transition until the output of the Sample-Hold has settled within the specified error band (0.1%). It includes aperture delay time.

ACQUISITION ACCURACY VS ACQUISITION TIME



HIGH SPEED DATA SYSTEM



This diagram represents a high speed data system using DATEL's SHM-40 and ADC-815, with an output register, to drive a data bus. The Start Command is a 60 nsec wide, TTL-compatible pulse with a maximum frequency of 1.5 MHz. Upon receipt of a start command, the SHM-40 will track the input voltage and the ADC-815 will reset. On the trailing edge of the start command, the SHM-40 will hold the input and the ADC-815 will begin its conversion. On the leading edge of the next start command, the output data will be clocked out of the output three-state register. The ADC-815 is an 8-bit, 700 nsec, analog-to-digital converter. With this system, a ±2.5V input step can be acquired to 0.1% accuracy in 40 nsec and held to within 80 μV while the A/D conversion takes place. The SHM-40 can also be used with the DATEL's ADC-816, which will yield 10 bits of resolution.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-40MC	0°C to +70°C
SHM-40MM	-55°C to +125°C

ACCESSORIES

Part Number	Description
DILS-2	Mating Socket (2 per connector)

For high reliability versions, contact Datel.

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SHM-45
HIGH-SPEED, HYBRID, PRECISION SAMPLE/HOLD

FEATURES

- **Ideally Suited for DATEL's Ultra-Fast ADC-500/505 A/D Converters**
- **200 nsec Max. Acquisition Time**
- **0.01% Accuracy**
- **100 nsec Max. Sample-Hold Settling Time**
- **74 dB Feedthrough Attenuation**
- **±50 psec Aperture Uncertainty**
- **Operable at Different Gain Settings**

GENERAL DESCRIPTION

DATEL's SHM-45 is a high-speed, high accuracy sample-hold designed for precision, high-speed analog signal processing applications. Manufactured with modern, high quality hybrid technology, the SHM-45 features excellent dynamic specifications including a maximum acquisition time of only 200 nsec for a 10V step to 0.01%. Sample-to-hold settling time to 0.01% accuracy is 100 nsec maximum with an aperture uncertainty of ±50 psec.

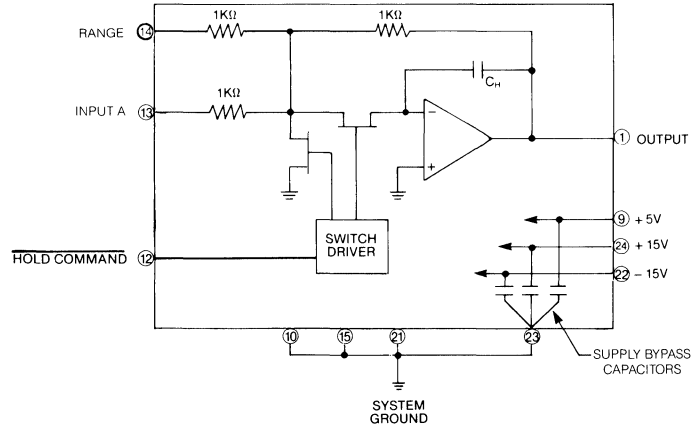
The SHM-45 is a complete sample-hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably low droop rate.

Other important features include a minimum output voltage range of ±10.25V, an aperture delay time of 6 nsec, a typical droop rate of ±0.5μV/μsec, and a sample-to-hold offset error as low as ±2.5mV. Sample-to-hold offset is constant regardless of the input/output voltage level. Output slew rate is typically 300V/μsec and small signal bandwidth (−3 dB) is 16 MHz.

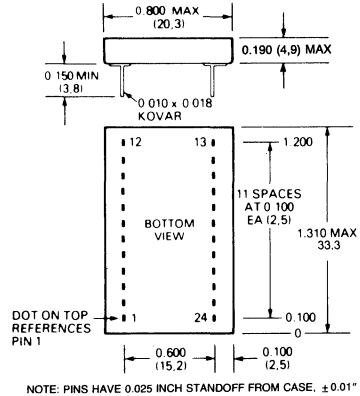
The SHM-45 has a TTL-compatible $\overline{\text{HOLD}}$ digital control input.

Applications for the SHM-45 include high-speed data acquisition and data distribution systems, peak measurement systems, fast fourier analysis, transient recorders and analog signal delay and storage.

Power requirements ±15V dc and +5V dc with a maximum power consumption of 875 mW. The SHM-45 is available in two models for operation over the commercial 0°C to +70°C and military −55°C to +125°C operating temperature ranges. All models are cased in a 24-pin, hermetically-sealed, ceramic package.



MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT	13	INPUT A
2	N/C	14	RANGE
3	N/C	15	GROUND
4	N/C	16	N/C
5	N/C	17	N/C
6	N/C	18	N/C
7	N/C	19	N/C
8	N/C	20	N/C
9	+5V SUPPLY	21	GROUND
10	GROUND	22	−15V SUPPLY
11	N/C	23	GROUND
12	$\overline{\text{HOLD COMMAND}}$	24	+15V SUPPLY

ABSOLUTE MAXIMUM RATINGS

±15V Supply Voltage (Pins 24, 22)	±18V
+5V Supply Voltage (Pin 9)	−0.5V to +7V
Analog Input (Pin 13, 14)[1]	±18V
Digital Input (Pins 11, 12)	−0.5V to +5.5V
Output Current[2]	±65 mA

FUNCTIONAL SPECIFICATIONS

Specified at +25°C, gains of −1, ±15V, and +5V power supplies unless otherwise specified.

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
ANALOG INPUTS (pin 13, 14)				
Input Volt. Range[1]	±10	—	—	V
Input Impedance	—	1K	—	ohm
LOGIC INPUTS (TTL)				
Logic "1" Voltage	+2.0	—	—	V
Logic "0" Voltage	—	—	+0.8	V
Logic "1" Current	—	—	40	μA
Logic "0" Current	—	—	−1.6	mA
ANALOG OUTPUTS (pin 1)				
Output Volt. Range	±10.25	+11.5	—	V
Output Current[2]	—	—	±40	mA
Output Impedance	—	0.1	—	ohm
Max. Capacitive Load	—	250	—	pf
PERFORMANCE				
Gain[3]	—	−1.0	—	V/V
Gain Error[3]	—	±.05	±.1	%
Gain Tempco	—	±0.5	±5	ppm/°C
Linearity Error[3]	—	±0.005	±.01	% FS
Initial Offset Voltage	—	±1	±5	mV
TRACK MODE DYNAMICS				
Frequency Response Small Signal (−3dB)	—	16	—	MHz
Slew Rate	—	300	—	V/μS
TRACK TO HOLD SWITCHING				
Aperture Delay Time	—	6	—	nS
Aperture Uncertainty (Jitter)	—	±50	—	pS
Offset Step (pedestal)[4]	—	±1	±5	mV
Settling Time 10V to ±.01% FS (±1 mV)[6]	—	60	100	nS
10V to ±.1% FS (±10 mV)	—	40	—	nS
HOLD MODE DYNAMICS				
Droop Rate at T= +25°C	—	0.5	5	μV/μS
at T= +70°C	—	15	—	μV/μS
at T= +125°C	—	1.2	—	mV/μS
Feedthrough Rejection	—	−74	—	dB
HOLD TO TRACK DYNAMICS				
Acquisition Time[5] 10V step to ±1.0mV (.01% FS)	—	160	200	nS
10V step to ±10mV (.1% FS)	—	100	170	nS
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range ±15V	—	±3%	—	
+5V	—	±5%	—	
Power Supply Rej. Ratio	—	±0.5	—	mV/V
Current Drains +15V	—	+21	+25	mA
−15V	—	−22	−25	mA
+5V	—	+17	+25	mW
Power Consumption		730	875	mW

PHYSICAL ENVIRONMENTAL	
Operating Temp. Range	
SHM-45-MC	0°C to +70°C (ambient)
SHM-45-MM	−55°C to +125°C (ambient)
Storage Temp. Range	−65°C to +150°C
Thermal Resistance	
Junction-to-Case	0.015°C/mW
Case-to-Ambient	0.035 C/mW
Package Type	24 pin ceramic
Package Dimensions	refer to Mechanical Dimensions drawing
Pins	Kovar (0.010 x 0.018)

Footnotes:

1- Input signal times gain should not exceed the output voltage range.

2- The SHM-45 output is current limited at approximately ±65 mA. The device can withstand a sustained short to ground. However, shorts to either supply will cause permanent damage. For normal operation, the load current should not exceed ±40 mA.

3- Specified at +25°C.

4- Sample-to-Hold offset error (Pedestal) is constant regardless of input/output level.

5- Acquisition time is tested with no load and is relatively unaffected by capacitive loads to 50 pF and resistive loads to 250 ohms.

6- Sample-to-Hold settling time between the point the sample-to-hold command is given and the point at which the analog output (following a transient) settles to within a specified error band around the final value.

TECHNICAL NOTES

1. All ground pins (10, 15, 21, 23) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. Care must be taken to insure that no ground potentials can exist between Pin 10 and the other ground pins.
2. Although the power supply pins (9, 22, 24) are internally bypased to ground with 0.01 μF ceramic capacitors, additional external 0.1 μF to 1μF tantalum bypass capacitors may be required in critical applications.

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3. A logic "1" on the HOLD COMMAND INPUT, Pin 12 will put the device in the sample mode. In this mode, the device acts as an inverting unity gain amplifier and its output will track its input. A logic "0" on Pin 12 will put the device in the HOLD mode, and the output will be held constant at the last input level present when the hold command was given.
4. The maximum capacitive load to avoid oscillation is typically 250 pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitances will affect both acquisition and settling time.

SHM-45 OUTPUT VOLTAGE RANGE SELECTION

The RANGE pin of the SHM-45 is usable to select different output voltage ranges. The output voltage ranges are selectable by hardware programming the SHM-45 to operate at different gains. Figure 2 shows the configuration to select different voltage ranges. In this configuration INPUT A (Pin 13) is the voltage input and RANGE (Pin 14) is used as a gain selector input. Table 1 shows the jumper selection details.

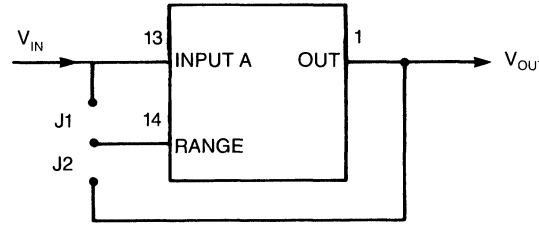


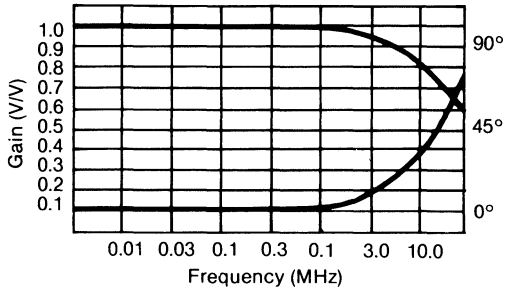
Figure 2. V_{OUT} Range Selection

Table 1. Jumper Selections for V_{OUT} Ranges

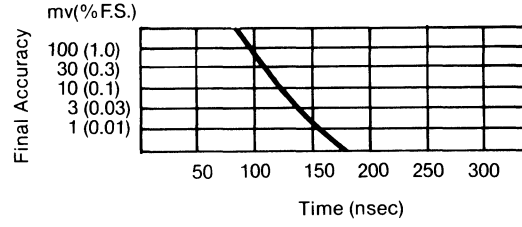
V_{IN}	V_{OUT}	Install Jumper	Operating Gain
−5 to +5	+10 to −10	J1	−2
−10 to +10	+10 to −10	—	−1
0 to −5	0 to +10	J1	−2
0 to −10	0 to +10	—	−1
−10 to +10	+5 to −5	J2	−0.5
0 to −10	0 to +5	J2	−0.5

3

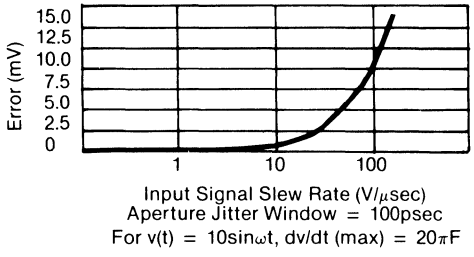
SHM-45 PERFORMANCE CHARACTERISTICS



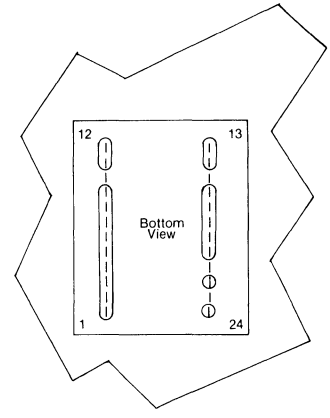
Track Mode Gain Amplitude and Phase Response



Acquisition Accuracy vs. Acquisition Time for a 10V Step



Accuracy Error Due to Aperture Uncertainty



Ground Plane Layout

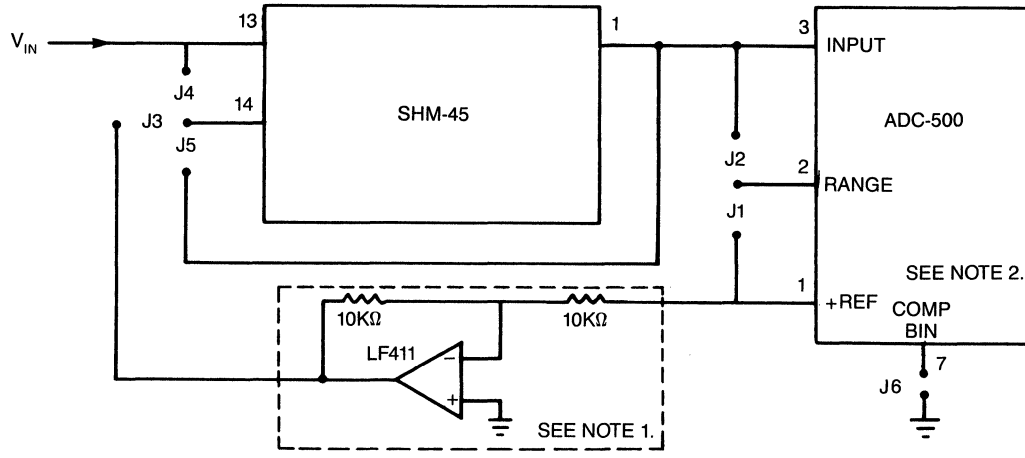
APPLICATION: Using The SHM-45 with DATEL's ADC-500/505

The SHM-45 is designed to accept different voltage ranges. However, to fully utilize the dynamic range of DATEL's ADC-500/505, the SHM-45 must be hardware programmed to provide the appropriate output voltage range. In the configuration shown in the Figure 3, RANGE functions as a gain selector. Refer to Table 2 for jumper selection details. This application configuration can sample at 1.2 MHz rate.

Table 2. Jumper Selections for V_{IN} Ranges

V_{IN} Range	Gain	Install Jumpers
0 to +10	+1*	J2, J3
0 to −10	−1	J2
−5 to +5	−2	J1, J4
−10 to +10	−1	J1
0 to −20	−0.5	J1, J5
0 to −5	−2	J2, J4

*Note: The application in this configuration operates at an overall effective gain of +1.



NOTES

1. The amplifier circuit shown is only needed if a positive unipolar signal is input to the SHM-45 (0 to +10V).
2. Positive Unipolar System Coding

V_{IN}	J6 Open	J6 Closed
0V (GND)	1111 1111 1111	0000 0000 0000
+10V (+FS)	0000 0000 0000	1111 1111 1111

Figure 3. Using SHM-45 with ADC-500/ADC-505

SHM-45 IS IDEALLY SUITED FOR USE WITH ADC-500/ADC-505

ADC-500 FEATURES

- **12-bit resolution**
- **500 nanoseconds maximum conversion time**
- **Low-power, 1.8W maximum**
- **Three-state output buffers**
- **−55°C to +125°C operation**
- **Small 32-pin DIP**

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE
SHM-45-MC	0°C to +70°C
SHM-45-MM	−55°C to +125°C

For devices compliant to MIL-STD-883, contact DATEL.

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SHM-4860
High Speed, 0.01% Hybrid Sample/Hold

FEATURES

- **200 Nanoseconds maximum acquisition time**
- **0.01% Accuracy**
- **100 Nanoseconds maximum sample-hold settling time**
- **74 dB feedthrough attenuation**
- **±50 Picoseconds aperture uncertainty**

GENERAL DESCRIPTION

DATEL's SHM-4860 is a high-speed, highly accurate sample-hold designed for precision, high-speed analog signal processing applications. Manufactured using modern, high-quality hybrid technology, the SHM-4860 features excellent dynamic specifications including a maximum acquisition time of only 200 nanoseconds for a 10V step to 0.01%. Sample-to-hold settling time, to 0.01% accuracy, is 100 nanoseconds maximum with an aperture uncertainty of ±50 picoseconds.

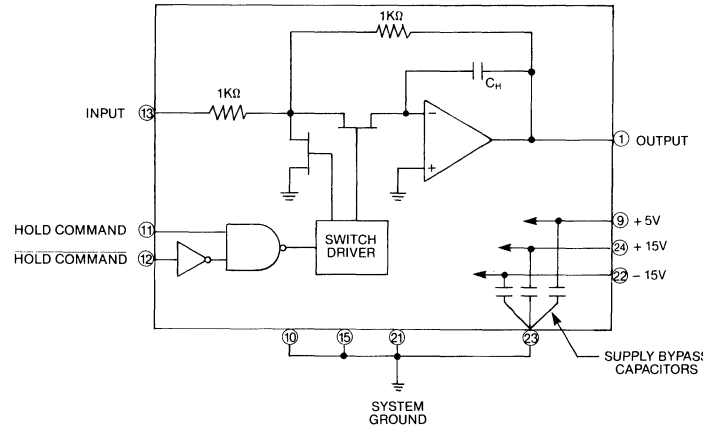
The SHM-4860 is a complete sample-hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

Other important features include a minimum input voltage range of ±10.25V, an aperture delay time of 6 nanoseconds, a typical droop rate of ±0.5 μV/μsecond, and a sample-to-hold offset error as low as ±2.5 mV. Sample-to-hold offset is constant regardless of the input/output voltage level. Output slew rate is typically 300V/microsecond and small signal bandwidth (−3 dB) is 16 MHz.

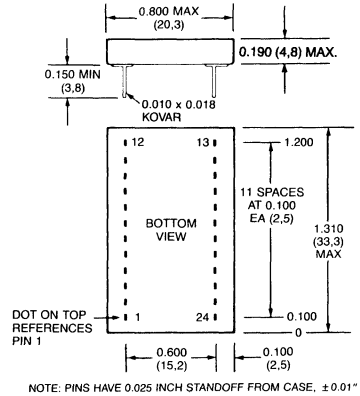
Both HOLD and $\overline{\text{HOLD}}$ digital control inputs are provided for use with either positive or negative true input commands.

Applications for the SHM-4860 include high-speed data acquisition and data distribution systems, peak measurement systems, fast fourier analysis, transient recorders, and analog signal delay and storage.

Power requirement is ±15V dc and +5V dc with a maximum power consumption of 875 mW. The SHM-4860 is available in two models for operation over the commercial 0°C to +70°C, and military, −55°C to +125°C operating temperature ranges. All models are cased in a 24-pin, hermetically sealed, ceramic package.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT	13	INPUT
2	N/C	14	N/C
3	N/C	15	GROUND
4	N/C	16	N/C
5	N/C	17	N/C
6	N/C	18	N/C
7	N/C	19	N/C
8	N/C	20	N/C
9	+5V SUPPLY	21	GROUND
10	GROUND	22	−15V SUPPLY
11	HOLD COMMAND	23	GROUND
12	$\overline{\text{HOLD COMMAND}}$	24	+15V SUPPLY

ABSOLUTE MAXIMUM RATINGS	
±15V Supply Voltage (Pins 24, 22)	±18V
+5V Supply Voltage (Pin 9)	−0.5V to +7V
Analog Input (Pin 13)[1]	±18V
Digital Input (Pins 11, 12)	−0.5V to +5.5V
Output Current[2]	±65 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

ANALOG INPUT/OUTPUT	MIN	TYP	MAX
Input/Output Voltage Range	±10.25V	±11.5V	—
Input Impedance	—	1 kΩ	—
Output Current[2]	—	—	±40 mA
Output Impedance	—	0.1 Ω	—
Maximum Capacitive Load	—	250 pF	—
DIGITAL INPUT			
Input Logic Level,[3] Logic "1"	+2.0V	—	+5.0V
Logic "0"	0V	—	+0.8V
Loading[4]	—	1 TTL Load	—
TRANSFER CHARACTERISTICS			
Gain	—	−1.0 V/V	—
Gain Accuracy	—	±0.05%	±0.1%
Gain Linearity Error[5]	—	±0.005% FS	±0.01% FS
Sample-Mode Offset Voltage	—	±0.5 mV	±5 mV
Sample-to-Hold Offset Error (Pedestal)[6]	—	±2.5 mV	±20 mV
Gain Tempco (Drift)	—	±0.5 ppm/°C	±5 ppm/°C
Sample-Mode Offset Drift[5]	—	±3 ppm of FSR/°C	±15 ppm of FSR/°C
Sample-to-Hold Offset (Pedestal) Drift[5]	—	±4 ppm of FSR/°C	—
DYNAMIC CHARACTERISTICS			
Acquisition Time;[7]			
10V to ±0.01% FS (±1 mV)	—	160 nsec.	200 nsec.
10V to ±0.1% FS (±10 mV)	—	100 nsec.	170 nsec.
10V to ±1% FS (±100 mV)	—	90 nsec.	—
1V to ±1% FS (±100 mV)	—	75 nsec.	—
Sample-to-Hold, Settling Time[8]			
10V to ±0.01% FS (±1 mV)	—	60 nsec.	100 nsec.
10V to ±0.1% FS (±10 mV)	—	40 nsec.	—
Sample-to-Hold Transient	—	180 mV P-P	—
Aperture Delay Time	—	6 nsec.	—
Aperture Uncertainty (Jitter)	—	±50 psec.	—
Output Slew Rate	—	300 V/μsec.	—
Small Signal Bandwidth (−3 dB)	—	16 MHz	—
Droop: +25°C	—	0.5 μV/μsec.	5 μV/μsec.
+70°C	—	15 μV/μsec.	—
+125°C	—	1.2 mV/μsec.	—
Feedthrough	—	74 dB	—
POWER REQUIREMENTS			
Voltage Range: ±15V	—	±3%	—
+5V	—	±5%	—
Power Supply Rejection Ratio	—	±0.5 mV/V	—
Quiescent Current Drain: +15V	—	+21 mA	+25 mA
−15V	—	−22 mA—	−25 mA
+5V	—	+17 mA—	+25 mA
Power Consumption	—	730 mW	875 mW
PHYSICAL/ENVIRONMENTAL			
Operating Temperature Ranges			
SHM-4860 MC		0°C to +70°C	
SHM-4860 MM		−55°C to +125°C	
Storage Temperature Range		−65°C to +150°C	
Package Type		24 Pin Ceramic	
Pins		Kovar (0.010 x 0.018)	

FOOTNOTES:

1. Input signal should not exceed the supply voltage.
2. The SHM-4860's output is current limited at approximately ±65 mA. The device can withstand a sustained short to ground. However, shorts from the output to either supply will cause permanent damage. For normal operation, the load current should not exceed ±40 mA.
3. See Technical Note 3.
4. One TTL load is defined as sinking 40 μA with a logic "1" input and sourcing 1.6 mA with a logic "0" input.
5. Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.
6. Sample-to-Hold offset error (Pedestal) is constant regardless of input/output level.
7. Acquisition time is tested with no load and is relatively unaffected by capacitive loads to 50 pF and resistive loads to 250Ω.
8. Sample-to-Hold settling time is the time between the point the sample-to-hold command is given and the point at which the analog output (following a transient) settles to within a specified error band around the final value.

TECHNICAL NOTES

1. All ground pins (10, 15, 21, 23) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. Care must be taken to insure that no ground potentials can exist between Pin 10 and the other ground pins.
2. Although the power supply pins (9, 22, 24) are internally bypassed to ground with 0.01 μF ceramic capacitors, additional external 0.1 μF to 1 μF tantalum bypass capacitors may be required in critical applications.
3. A logic "0" on the HOLD COMMAND INPUT, (Pin 11) (or a logic "1" on the $\overline{\text{HOLD COMMAND INPUT}}$, Pin 12) will put the device in the sample mode. In this mode, the device acts as an inverting unity gain amplifier and its output will track its input. A logic "1" on Pin 11 (logic "0" on Pin 12) will put the device in the HOLD mode, and the output will be held constant at the last input level present when the hold command was given.

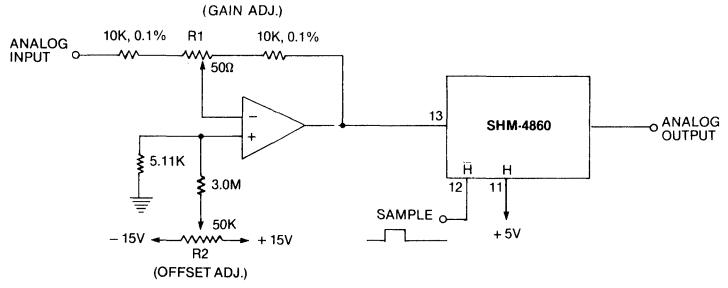
   If the HOLD COMMAND INPUT (Pin 11) is used to control the device, $\overline{\text{Pin 12}}$ must be tied to digital ground. If $\overline{\text{HOLD}}$ COMMAND INPUT (Pin 12) is used to control the device, Pin 11 must be tied to +5V.
4. The maximum capacitive load to avoid oscillation is typically 250 pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitances will affect both acquisition and settling time.

OFFSET AND GAIN ADJUSTMENTS

Critical offset adjustments may be performed utilizing this configuration. Apply zero volts (0V) to the analog input and adjust R_2 so that the output measures zero volts (0V) during the hold mode period of the SHM-4860.

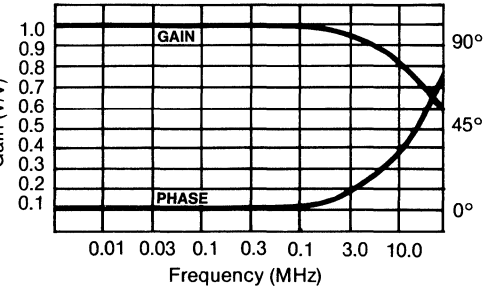
Gain may be trimmed by applying an FS voltage to the analog input and adjusting R_1 so that the output measures the same FS voltage during the hold mode period.

OFFSET AND GAIN ADJUSTMENTS

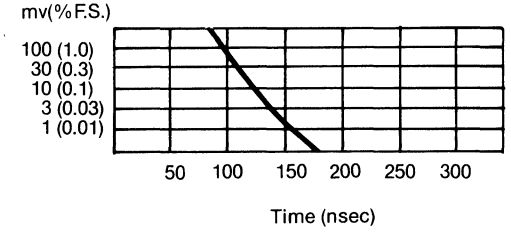


PERFORMANCE

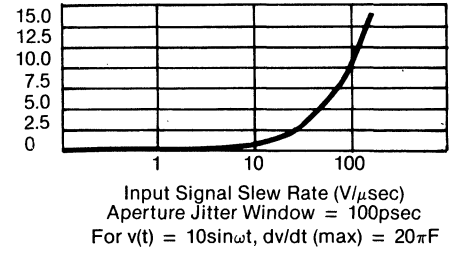
Track Mode Gain Amplitude and Phase Response



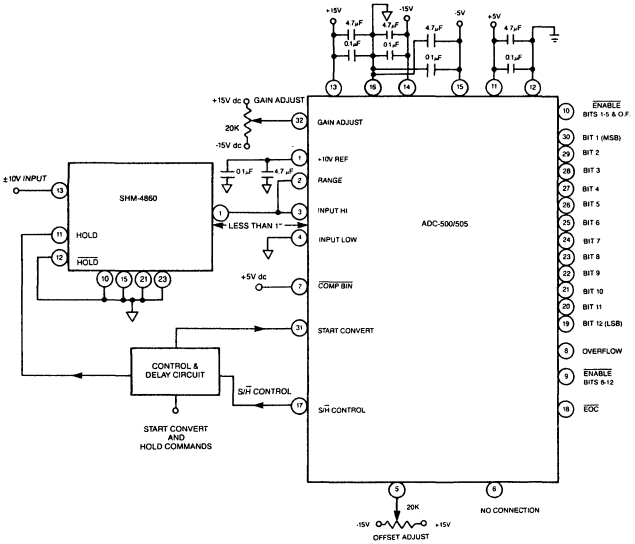
cquisition Accuracy vs. Acquisition Time for a 10V Step



Accuracy Error Due to Aperture Uncertainty



HIGH SPEED A/D USING SHM-4860



DATEL's SHM-4860, a high-speed sample/hold amplifier, is shown here coupled with DATEL's ADC-500/505. Together, they provide a high-speed analog to digital converter with sample/hold which can attain throughput rates exceeding 1.25 MHz.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-4860MC	0°C to +70°C
SHM-4860MM	–55°C to +125°C

ACCESSORIES

Part Number	Description
DILS-3	24-Pin Mating Socket

For military devices compliant to MIL-STD-883, consult the factory.

SHM-5
Ultra-Fast, 0.01% Sample-Hold

DATEL

FEATURES

- **200 Nanoseconds acquisition to 0.1%**
- **350 Nanoseconds acquisition to 0.01%**
- **5 MHz Bandwidth**
- **0.005% Linearity**
- **250 Picoseconds aperture uncertainty**

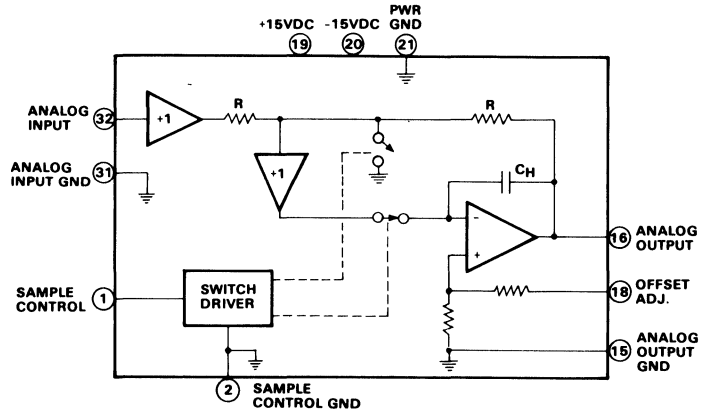
GENERAL DESCRIPTION

Model SHM-5 is a new, ultra-fast acquisition sample-hold module for use with high speed 10- and 12-bit A/D converters. When used with DATEL's model ADC-EH12B3, a 12-bit, 2 microseconds A/D, the SHM-5 permits sampling and conversion at rates up to 425 kHz. The key circuit element in the SHM-5 is an ultra-fast settling hybrid operational amplifier manufactured in DATEL's thin-film hybrid facility. This amplifier operates in the inverting mode as a hold amplifier. A fast FET sampling switch operates between two virtual ground points in order to keep switching errors small and independent of signal level. A second FET switch operates out-of-phase with the first one to minimize signal feed-through errors.

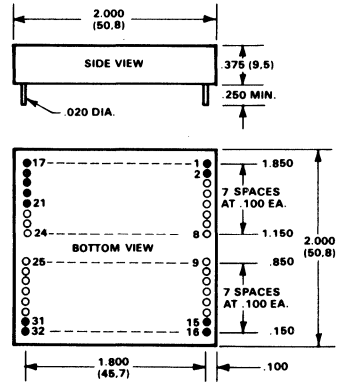
The SHM-5 is designed primarily for fast track & hold and simultaneous sampling applications with A/D converters. From the tracking mode it realizes acquisition times of 200 nanoseconds to 0.1% or 350 microseconds to 0.01% for a 10V change. When the input buffer amplifier must also make a 10V change, as in multiplexer applications, the total acquisition time is 1 microsecond to 0.01%.

The SHM-5 operates in the inverting mode with a gain of -1 and an input impedance of 10^8 ohms. Dynamic characteristics include a 5 MHz small signal bandwidth, and 25V/microseconds slew rate in the sampling (tracking) mode. When acquiring a new sample, however, the internal slew rate across the holding capacitor is 200V/microseconds. Aperture delay time is 20 nanoseconds and aperture uncertainty time is 250 picoseconds.

This device is packaged in a 2 x 2 x 0.357 inch epoxy encapsulated module. Operating temperature range is 0°C to +70°C and power requirement is ±15V dc at 75 mA maximum. The SHM-5 is pin compatible with DATEL's model SHM-UH3.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	NO CONNECTION
18	OFFSET ADJ.
19	+15V POWER
20	-15V POWER
21	POWER GND
31	ANALOG INPUT GND
32	ANALOG INPUT

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FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supply unless otherwise noted.

INPUTS	
Input Voltage Range	±10V minimum
Input Overvoltage, no damage	±15V
Input Impedance	10^8 ohms
Input Bias Current	250 nA maximum
Sample Control,	
sample mode	+2.0 to +5.5V
hold mode	0V to +0.8V
Sample Control Loading	+1 mA
Offset Adjustment Range	±300 mV
OUTPUT	
Output Voltage Range, minimum	±10V
Output Current, S.C. protected	±40 mA
Output Impedance	0.1 Ω maximum
PERFORMANCE	
Gain	−1.000 ± 0.1%
Gain Temp. Coefficient	±15 ppm/°C maximum
Output Offset Voltage,	
sample mode	±50 mV maximum
Output Offset Voltage Drift	±30 μV/°C maximum
Sample to Hold Offset Error	±5 mV maximum
Tracking Nonlinearity	±0.005% maximum
Hold Mode Droop	20 μV/μsec. maximum
Hold Mode Feedthrough,	
DC-500 kHz	0.02%
Output Offset vs Supply	1 mV/V
DYNAMIC RESPONSE	
Acquisition Time[1], 10V to 0.1%	200 nsec. maximum
Acquisition Time[1], 10V to 0.01%	350 nsec. maximum
Acquisition Time[2], 10V to 0.01%	1.0 μsec. typical 1.5 μsec. maximum
Bandwidth, tracking, −3 dB	5 MHz
Slew Rate, tracking	25V/μsec.
Aperture Delay Time	20 nsec.
Aperture Uncertainty Time	250 psec.
POWER REQUIREMENTS	
Power Supply Voltage	±15V dc ±0.5V
Quiescent Current	75 mA maximum
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	−55°C to +85°C
Relative Humidity	Up to 100% non-condensing
Case Size	2.0 x 2.0 x 0.375 in, 50,8 x 50,8 x 9,5 mm
Case Material	Black diallyl phthalate per MIL-M-14
Pins	0.020″ round, gold plated; 0.25″ long minimum
Weight	2 ounces (57 grams)

FOOTNOTES:

1. From tracking mode.
2. From input buffer.

ORDERING INFORMATION

SHM-5

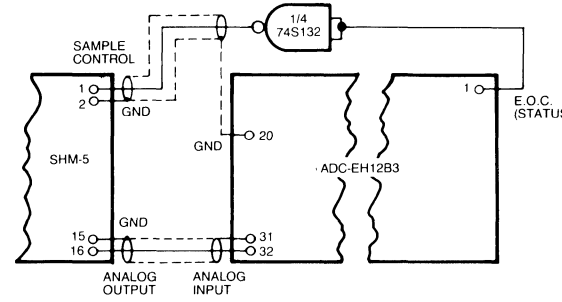
ACCESSORIES

Part Number	Description
DILS-2	Mating Sockets: (2 per module)
TP20K	Trimming Potentiometer

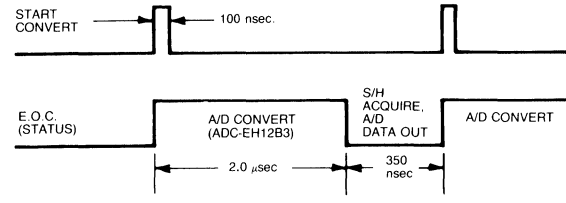
TECHNICAL NOTES

1. The SHM-5 initial gain error of ±0.1% must be adjusted out separately from the sample hold. This is most easily done by using the gain adjust of the A/D converter used with the SHM-5.
2. The maximum sample-to-hold offset error of 5 mV is constant with signal level. This error can be adjusted out in the hold mode by means of the external offset adjustment shown in the diagram. It should be noted that the SHM-5 can be adjusted for zero output offset in either the sample (tracking) mode or the hold mode, but not in both at the same time.
3. The sample control input is compatible with standard TTL levels. It is recommended that this input be driven from its own active pull-up Schottky TTL circuit, such as the 74S132. This will readily supply the +1 mA drive current required by the SHM-5.
4. The analog signal delay from the input of the SHM-5 to the sampling switch is approximately 32 nanoseconds. Aperture delay is 20 nanoseconds.
5. When the SHM-5 is switched into the hold mode, about 50 nanoseconds is required for the switch transient to settle. This time should be allowed for before the first A/D conversion is made.

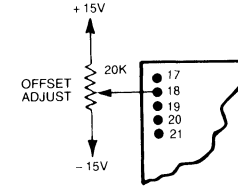
CONNECTION TO ADC-EH12B3



TIMING DIAGRAM



OFFSET ADJUSTMENT



SHM-6
0.02%, 2.0 Microseconds
Microelectronic Sample-Hold

FEATURES

- **0.02% Accuracy**
- **2.0 Microseconds acquisition time**
- **2 Nanoseconds aperture uncertainty**
- **5 MHz Bandwidth**
- **25 mA Output current**
- **Gain-programmable from ±1 to ±10**

GENERAL DESCRIPTION

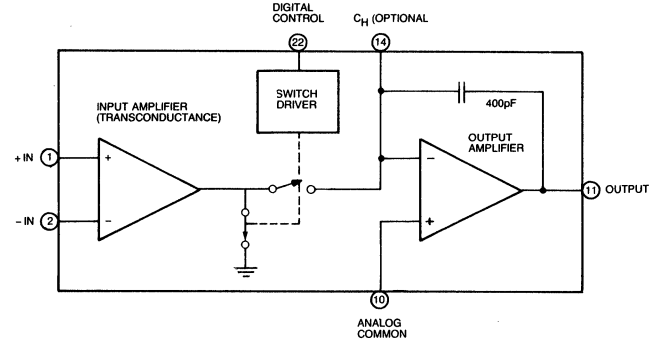
The SHM-6 is a high speed, high accuracy sample-hold circuit manufactured with thin film hybrid technology. This design offers the speed and performance of modular sample-holds with the compactness and integrity of advanced hybrid techniques. The unit's excellent high-speed characteristics include a guaranteed acquisition time of 700 nanoseconds to 0.1% accuracy and 2.0 microseconds to 0.02% for a 10 volt change.

The SHM-6 is a complete sample-hold containing a precision MOS holding capacitor. The input amplifier is an open loop transductance amplifier which can be externally connected for closed loop gains from ±1 to ±10. In addition to its speed, accuracy and selectable gain, the SHM-6 has an output capability of 25 mA. These features allow this unit to offer an unusual degree of adaptability.

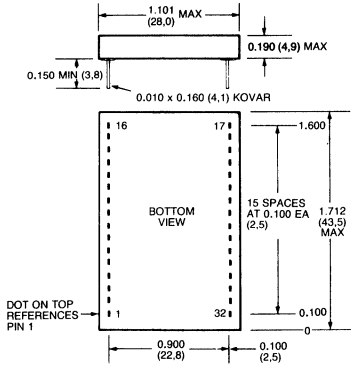
The most frequently utilized configuration of the SHM-6 is a unity gain, noninverting sample-hold. In this mode, the device has a ±10V input and output range with 10^8 Ω input resistance. Full power bandwidth is 500 KHz, and small signal tracking capability is 5 MHz. The input offset voltage and sample to hold error can be adjusted to zero with the use of two external trim pots.

The SHM-6 is a key component in fast data acquisition systems. A 100 KHz throughput rate can be accomplished using the SHM-6 in conjunction with DATEL's ADC-HZ 12-bit A/D converter (which offers 8 microseconds maximum conversion time).

The sample-hold is cased in a 32-pin ceramic package. Models are available in two operating temperature ranges: 0 to +70°C and −55 to +100°C.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+IN	17	S/H STEP ADJUST.
2	−IN	18	S/H STEP ADJUST.
3	NC	19	NC
4	OFFSET ADJUST	20	NC
5	NC	21	NC
6	OFFSET ADJ. (Wiper)	22	DIGITAL CONTROL
7	NC	23	NC
8	OFFSET ADJUST	24	+V dc
9	NC	25	NC
10	ANALOG COMMON	26	POWER GROUND
11	OUTPU	27	NC
12	NC	28	+15V dc
13	NC	29	NC
14	C.H. (OPTIONAL)	30	NC
15	NC	31	−15V dc
16	S/H ADJ. (Wiper)	32	NC

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ABSOLUTE MAXIMUM RATINGS	
Positive Supply	+18V
Negative Supply	−18V
Logic Supply	+7.0V
Digital Input Voltage	+5.5V
Analog Input Voltage	±Vs
Differential Input Voltage	±30V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUT AMPLIFIER SPECIFICATIONS	
Offset Voltage	±2 mV
Offset Voltage Tempco	±100 μV/°C
Offset Current	1 nA maximum
Offset Current vs. Temp.	Doubles every 10°C
Bias Current	10 nA maximum
Input Resistance	10^8 Ω
Common Mode Voltage Range	±10V minimum
Common Mode Rejection Ratio	74 dB minimum
Open Loop Gain	10^6V/V
Gain Bandwidth Product	5 MHz
Power Supply Rejection Ratio	0.004%/% Supply

DIGITAL INPUT CHARACTERISTICS	
Digital Control Logic	DTL, TTL
Input Logic Level, Sample Mode	0V to +0.8V at −3.2 mA
Input Logic Level, Hold Mode	+2.0V to +5.0V at +80μA

ANALOG OUTPUT CHARACTERISTICS	
Output Voltage Range	±10V minimum
Output Current	±25 mA maximum
Output Resistance	0.1 Ω maximum

SAMPLE/HOLD CHARACTERISTICS (Noninverting unity gain)	
Acquisition Time, 10V Step to 0.1%	700 nsec. maximum
Acquisition Time, 10V Step to 0.02%	1.5 μsec. typical 2 μsec. maximum
Aperture Delay Time	20 nsec.
Aperture Uncertainty Time	2 nsec.
Sample to Hold Error	Adjustable to Zero
Hold Mode Voltage Droop	10 μV/μsec. maximum
Hold Mode Feedthrough	0.02% maximum
Offset	Adjustable to Zero
Gain	±1 to ±10
Gain Error	0.01% maximum
Nonlinearity, V_{OUT} = ±10V	0.02% maximum
Full Power Bandwidth, V_{OUT} = ±10V	500 KHz
Slew Rate	40 V/μsec.

POWER REQUIREMENTS	
Positive Supply	+15V dc ±0.5V at 55 mA
Negative Supply	−15V dc ±0.5V at 60 mA
Logic Supply	+5V dc ±0.5V at 30 mA

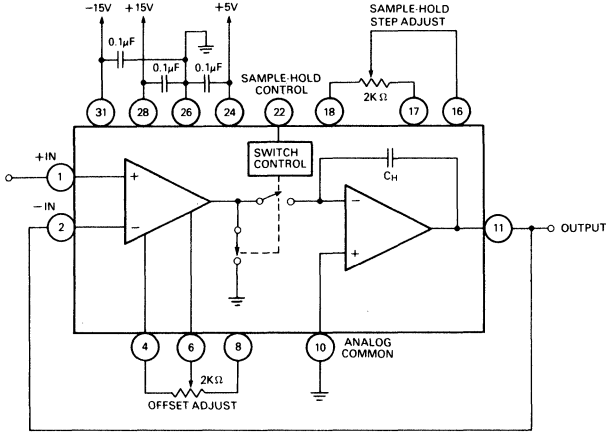
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-6MC	0°C to +70°C
SHM-6MM	−55°C to +100°C
Storage Temperature Range	−65°C to +150°C
Package Type	32 Pin Ceramic
Pins	Kovar (0.010 x 0.018)
Weight	0.5 Ounce (14 grams)

TECHNICAL NOTES

1. It is essential that the +15V, −15V and +5V supplies, pins 28, 31, and 24 respectively, each be bypassed to ground with a 0.1 μF ceramic capacitor connected as close to the pins as possible.
2. Digital Common, pin 26, and Analog Common, pin 10, are not connected together internally, therefore they must be connected externally as directly as possible. It is strongly recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 10, digital ground and +5V power ground should be run to pin 26.
3. An external holding capacitor can be added to decrease hold mode voltage droop but with consequently longer acquisition time. For temperatures up to +85°C, polystyrene capacitors are recommended; for higher temperatures, polypropylene or teflon capacitors should be used.
4. In the inverting unity gain operating mode, the feedback and input resistors should be carefully matched or trimmed to yield the desired gain of one. In general, the operating parameters are the same as the noninverting unity gain configuration, except that the sampling bandwidth is reduced by a factor of two. For applications of the SHM-6 with gain greater than one, sampling bandwidth is inversely proportional to gain.
5. Capacitive loads on the output should be limited to 100 pF to maximize acquisition time. The SHM-6 has a ±25 mA current drive capability.
6. This device dissipates approximately 2 watts of power due to the transconductance amplifier. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above +50°C, care should be taken to maintain air circulation in the vicinity of the case.
7. The adjustment procedures for the SHM-6 are as follows. Ground the input pin and connect the output to a D.V.M.; operate the offset adjustment potentiometer to yield an output of zero as read on the D.V.M. The sample-hold step adjustment is performed with the input pin grounded and the output connected to an oscilloscope set to 1 mV/cm sensitivity. The digital input pin is driven with a compatible square wave at approximately 250 KHz and the sample-hold step adjustment potentiometer is operated to produce a flat-line output on the oscilloscope.

3

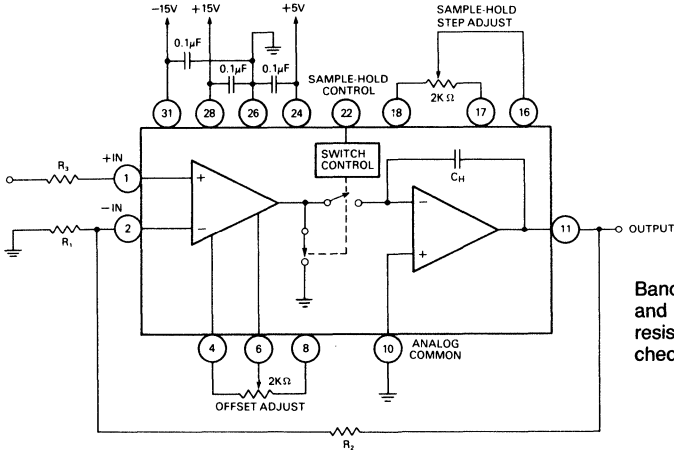
OPERATING MODES



NONINVERTING SAMPLE-HOLD

GAIN = +1

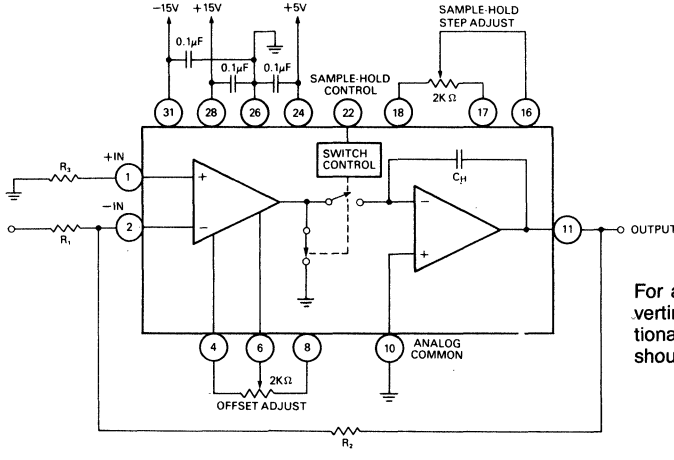
The 2KΩ offset trimming potentiometers should be of the 100PPM/°C cermet type. These are available from DATEL's as model TP2K.



NONINVERTING SAMPLE-HOLD

$$\text{GAIN} = 1 + \frac{R_2}{R_1}$$

Bandwidth decreases proportionately with gain. Resistors R_1 and R_2 should be 100PPM/°C or better, metal film type resistors. The indicated ratio between R_1 and R_2 should be matched as closely as possible and trimmed if necessary.



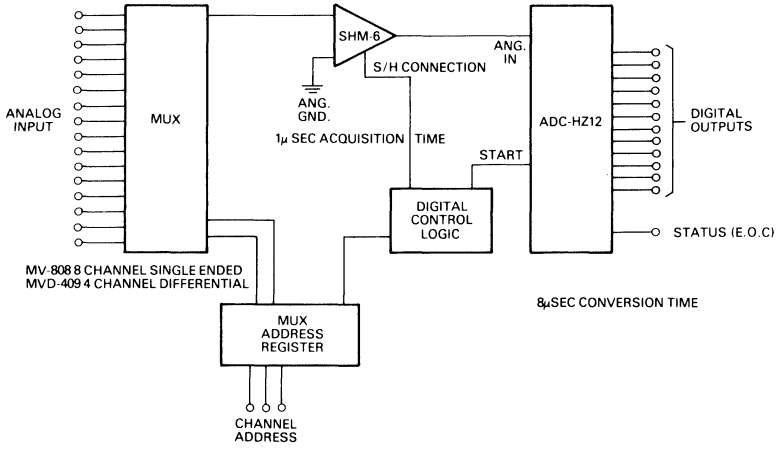
INVERTING SAMPLE-HOLD

$$\text{GAIN} = -\frac{R_2}{R_1}$$

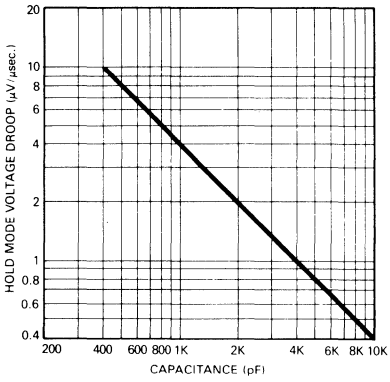
For a gain of −1 the bandwidth is one half that of the noninverting mode, for higher gains the sampling bandwidth is proportionately reduced. The above-mentioned matching procedures should be followed.

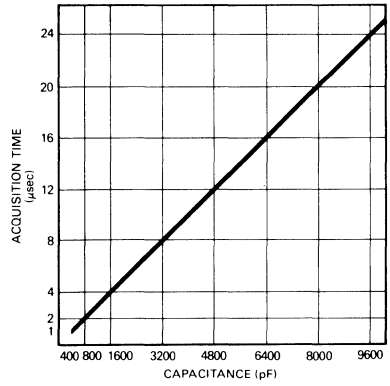
TYPICAL PERFORMANCE

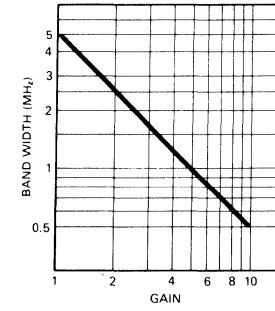
(Noninverting unity gain at 25°C, ±15V and +5V supplies unless otherwise noted)

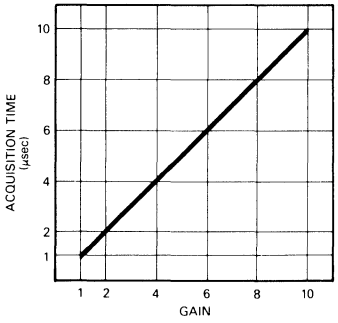


A high speed data acquisition system employing the SHM-6. This system is capable of a 110 kHz throughput rate with 12 bit resolution. In this system the SHM-6 is used with DATEL's ADC-HZ12, a high-speed hybrid 12 bit A/D converter, and DATEL's MV-808, a low cost monolithic analog multiplexer. Use of a low on-resistance MUX is recommended, so that the time constant formed by MUX on-resistance and bus capacitance does not limit the acquisition performance of the SHM-6.









ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
SHM-6MC	0°C to +70°C	Hermetic
SHM-6MM	−55°C to +100°C	Hermetic

ACCESSORIES

Part Number	Description
DILS-2	Mating Socket (2 required per SHM-6)
TP2K	Trimming Potentiometers (2 required per Sample-Hold)

For high reliability devices, contact DATEL.

SHM-7
Video Speed
Sample-Hold

DATEL

FEATURES

- **40 Nanoseconds acquisition time**
- **Dual outputs**
- **10 Picoseconds aperture uncertainty**
- **40 MHz bandwidth**
- **30 mA Output current**

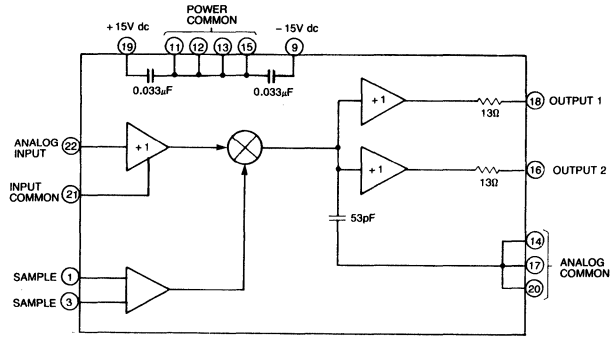
GENERAL DESCRIPTION

DATEL's SHM-7 is an ultra-fast sample and hold designed for high speed analog signal processing applications. The SHM-7 acquires a 2V dc input change to 0.1% in only 40 nanoseconds and aperture uncertainty time is less than 10 picoseconds. Sample-mode bandwidth is 40 MHz.

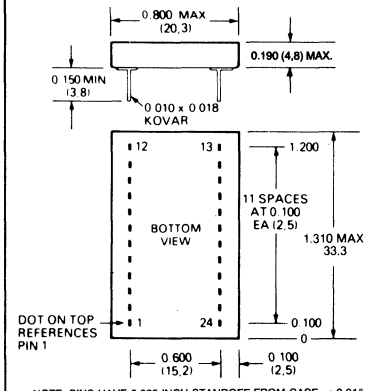
The SHM-7 is a complete Sample-Hold, containing an input buffer amplifier, a precision 53 pF MOS holding capacitor, and two output buffer amplifiers. The sampling switch is controlled by a series 10,000 complementary ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

Other features of the SHM-7 include a ±5V dc input voltage range, a fixed gain of +0.995, and a maximum gain temperature coefficient of 33 ppm/°C. The device has two outputs, each with a ±5V dc output voltage swing at 30 mA and an output impedance of only 13Ω. The outputs may be tied together for decreased output impedance and increased output current. The SHM-7 is functionally laser trimmed at the factory for offset, sample to hold offset, and gain errors, and is designed to be used without external adjustment circuits.

The SHM-7 is an ideal choice for use in ultra-high speed data acquisition systems, and video processing applications, and with its dual outputs, it is especially useful in two stage flash converter systems. Power requirement is ±15V dc at 60 mA. The SHM-7 is available for operation over the 0°C to +70°C operating temperature range and is cased in a 24 pin, hermetically sealed, ceramic package.



MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE. ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SAMPLE	13	POWER COM.
2	N.C.	14	ANALOG COM.
3	SAMPLE	15	POWER COM.
4	N.C.	16	OUTPUT 2
5	N.C.	17	ANALOG COM.
6	N.C.	18	OUTPUT 1
7	N.C.	19	+15V dc
8	N.C.	20	ANALOG COM.
9	-15V dc	21	INPUT COM.
10	N.C.	22	ANALOG INPUT
11	POWER COM.	23	N.C.
12	POWER COM.	24	N.C.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-7MC	0°C to +70°C

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ABSOLUTE MAXIMUM RATINGS	
Positive Supply	+18V dc
Negative Supply	−18V dc
Digital Input Voltage	±5V dc
Analog Input Voltage	±5V dc

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc Supplies Unless Otherwise Noted.

INPUTS	
Input Voltage Range[1], minimum	±2.5V dc
maximum	±5V dc
Input Bias Current	50 μA
Input Impedance, minimum	10 kΩ
Maximum Source Impedance[2]	50Ω
Sample Control Inputs[3]	Differential ECL 10,000 Positive Pulse on Pin 3 and Negative Pulse on Pin 1 gives Hold Mode.

OUTPUTS	
Output Voltage Range[1], minimum	±2.5V dc
maximum	±5V dc
Output Current[4]	±30 mA
Output Impedance[4]	13Ω

PERFORMANCE	
Linearity ±2.5V input volt. range	0.1%
±5V input volt. range	0.2%
Gain	+0.995
Gain Tempco, maximum	±33 ppm/°C
Sample-to-Hold Offset Error, maximum	40 mV
Sample-Mode Offset Voltage, maximum	±20 mV
Sample-to-Hold Offset Voltage Drift	75 μV/°C
Sample-Mode Offset Voltage Drift	±250 μV/°C
Hold Mode Feedthrough, maximum	−66 dB
Hold Mode Droop	100 μV/microseconds

DYNAMIC CHARACTERISTICS	
Acquisition Time, 2V to 0.1%	40 nanoseconds
2V to 1%	25 nanoseconds
4V to 0.1%	50 nanoseconds
4V to 1%	35 nanoseconds
10V to 0.1%[6]	60 nanoseconds
10V to 1%[6]	45 nanoseconds
Aperture Delay Time	3 nanoseconds
Aperture Uncertainty Time, maximum	10 picoseconds
Hold Mode Settling Time	20 nanoseconds
Sample-Mode Bandwidth; −3 dB	40 MHz
Sampling Rate[5]	17 MHz

POWER REQUIREMENTS	
Positive Supply, Pin 19	+15V dc ±0.5V dc at 60 mA
Negative Supply, Pin 9	−15V dc ±0.5V dc at 60 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-7MC	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Type	24 Pin, hermetically sealed, ceramic.
Pins	0.010 x 0.018 Inch Kovar

FOOTNOTES:

1. The SHM-7MC has a maximum input/output voltage range of ±5V.
2. Should be purely resistive. See technical note 3.
3. Input logic voltage levels are V_{in} "0" = −1.5V to −1.4V, and V_{in} "1" = −0.7V to −1.05V.
4. Specified for each output, both outputs may be tied together for decreased output impedance and increased output current.
5. For a ±2V input.
6. 10V is a step from −5V to +5V dc.

3

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for rated performance. The power common (Pins 11, 12, 13 and 15), analog common (Pins 14, 17 and 20), and input common (Pin 21) pins are not connected internally and therefore must be connected externally as directly as possible through a low inductance, low resistance path. The extensive use of a ground plane for all common connections is highly recommended.
2. Although they are internally bypassed with 0.033 μF capacitors the supply pins (Pins 19, 9) should be externally bypassed with 0.1 μF ceramic chip capacitors mounted as close to the supply pins as possible.
3. The SHM-7 inputs and outputs are sensitive to unusual loading or long lines. The analog input must be non-reactive so that leads should be short and purely resistive. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.
4. The maximum, differential, digital input voltage is ±5V. For example, if pin 3 is at a potential of −5V, pin 1 may not exceed 0V.

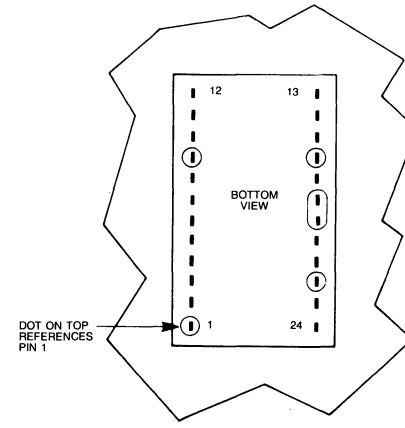
SAMPLE-HOLD DEFINITIONS

1. Acquisition Time
   Time required, after receipt of the sample command, for the hold capacitor to charge to a specified voltage change and remain within a specified error band such as 0.1%.
2. Aperture Delay Time (effective)
   The time elapsed from the hold command to the opening of the sampling switch minus the delay from the analog input to the sample switch.

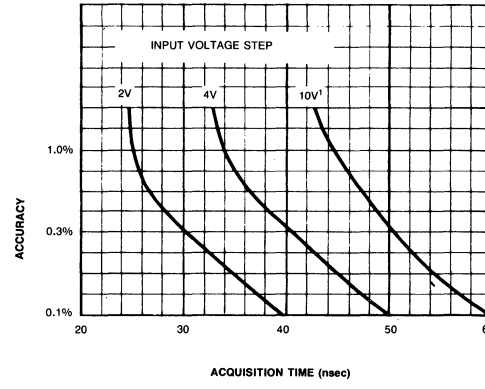
PERFORMANCE AND CONNECTION

3. Aperture Uncertainty Time
   Time variation, or jitter, in the opening of the sampling switch.
4. Aperture Uncertainty Error
   An amplitude uncertainty in the held value due to the change in the analog input signal during the aperture uncertainty time. This error is the product of the rate of change of the input signal and the aperture uncertainty time.
5. Hold-Mode Settling Time
   The time from the hold command transition until the output of the Sample-Hold has settled within the specified error band (0.1%). It includes aperture delay time.
6. Hold-Mode Droop
   The output voltage change per unit of time while in the hold mode.
7. Bandwidth
   The frequency at which the gain is down 3 dB from its dc value. It's measured in the sample-mode with a small-signal sine wave.

BASIC GROUND PLANE LAYOUT

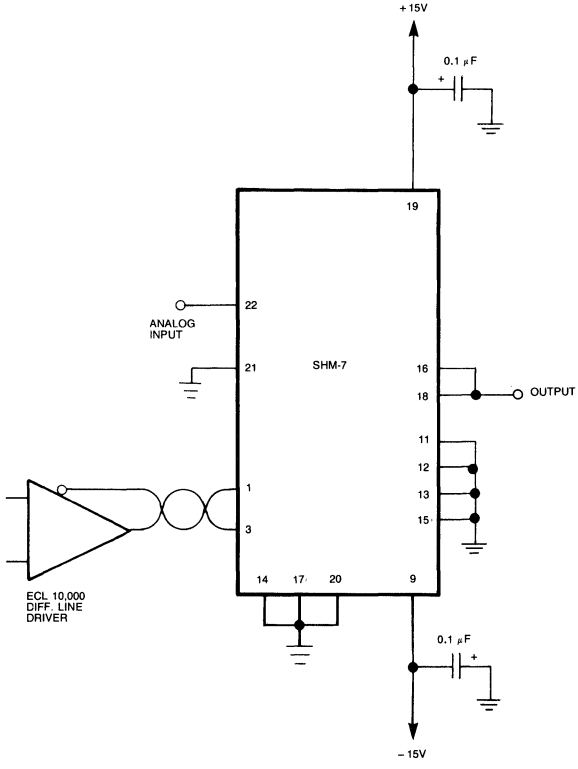


ACQUISITION TIME VS. INPUT VOLTAGE

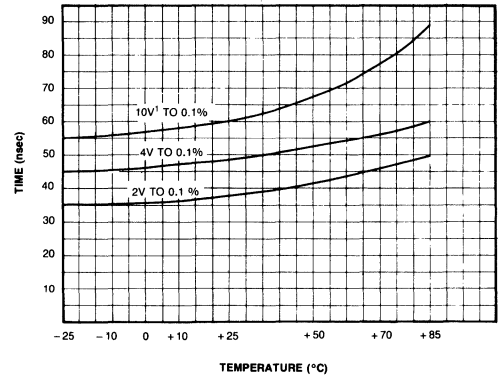


NOTE: 10 VOLTS IS A −5V TO +5V dc STEP.

TYPICAL CONNECTION



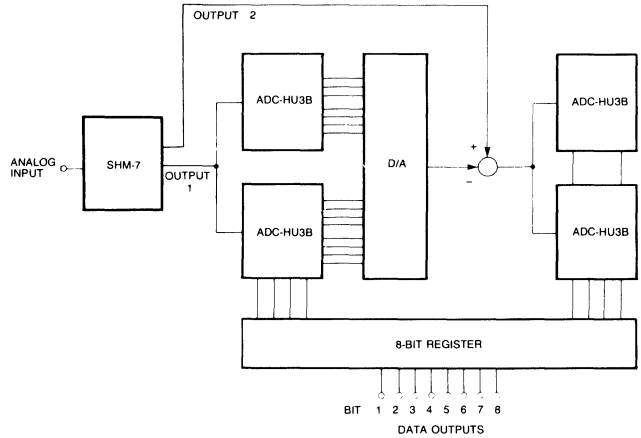
ACQUISITION TIME VS. TEMPERATURE



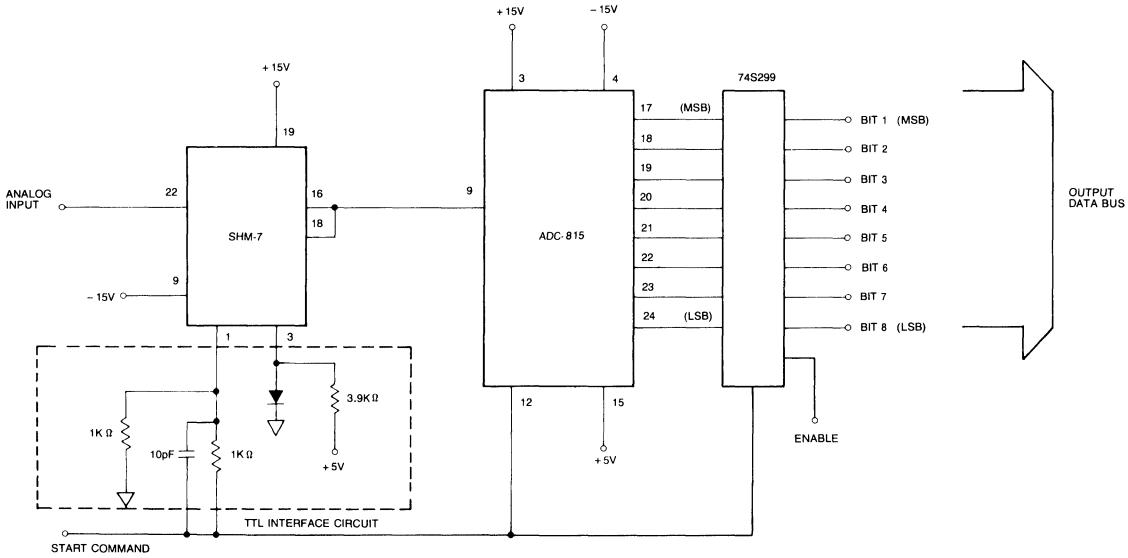
NOTE: 10 VOLTS IS A −5V TO +5V dc STEP.

TYPICAL APPLICATIONS

TWO STAGE CONVERSION SYSTEM



HIGH SPEED DATA SYSTEM



A high speed data system using DATEL's SHM-7 and ADC-815, with an output register, to drive a data bus. The Start Command is a 60 nanosecond wide, TTL-compatible, pulse with a maximum frequency of 1.5 MHz. Upon receipt of a start command, the SHM-7 will track the input voltage and the ADC-815 will reset. On the trailing edge of the start command, the SHM-7 will hold the input and the ADC-815 will begin its conversion. On the leading edge of the next start command, the output data will be clocked out of the output three-state register. The ADC-815 is an 8-bit, 700 nanosecond, analog-to-digital converter. With this system, a ± 2.5V input step can be acquired to 0.1% accuracy in 40 nanoseconds and held to within 80 μV while the A/D conversion takes place.

SHM-9
Low Cost, Fast, Sample-Hold

DATEL

FEATURES

- **Low cost**
- **0.01% Accuracy**
- **6 Microseconds acquisition time**
- **0.2 Millivolt/millisecond hold-mode droop**
- **No external adjustments needed**

GENERAL DESCRIPTION

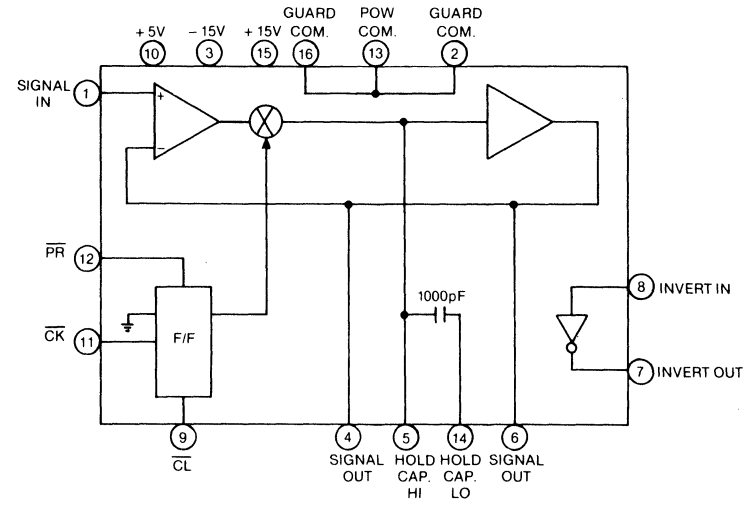
Datel's SHM-9 is a fast, hybrid sample-hold amplifier that combines high performance versatility and low cost. Acquisition time, for a 10V dc change to 0.01%, is only 6 microseconds, and aperture delay time is 200 nanoseconds. The small signal bandwidth is 4 MHz.

The SHM-9 is a complete self-contained unit, including a bipolar input amplifier, a low-leakage electronic switch, a FET output amplifier, a precision 1000 pF hold capacitor and logic control circuitry. The control circuitry allows the SHM-9 to be interfaced with virtually any A/D converter using the converter's start/convert and EOC signals. This allows the user to put the SHM-9 into the hold mode using the start/convert pulse; thus when the A/D's EOC signal goes high and conversion begins, the SHM-9 will already be providing a stable analog input signal. When the EOC goes low, signaling the end of conversion the SHM-9 is switched into the sample mode. If this is not practical, the SHM-9 can also be used with a single control signal. An external hold capacitor may be added if necessary.

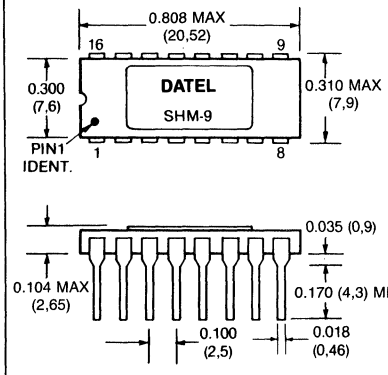
Other important features include $10^{10}\Omega$ input impedance, a hold-mode feedthrough of 0.01%, and a hold-mode droop of only 0.2 millivolts/milliseconds maximum input/output voltage range is ±11.5V dc, input bias current is 50 nA maximum, and the input offset voltage drift is 20 μV/°C. The SHM-9 is functionally laser trimmed to eliminate offset, and sample to hold offset errors, and is designed to be used without external adjustment circuits.

Its low cost, high performance and input control flexibility make the SHM-9 a good choice for unnumerable applications including sampling for A/D conversion, analog demultiplexing circuits and simultaneous sampling circuits. The small size of the SHM-9 allows it to be easily used with automatic insertion equipment.

The SHM-9 is available in two models for operation over the commercial 0°C to +70°C and military −55°C to +125°C operating temperature ranges. Power requirement is ±15V dc and ±5V dc. All models are packaged in a 16-pin, hermetically sealed, ceramic DIP.



MECHANICAL DIMENSIONS INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT	9	$\overline{CL}$
2	GUARD COMMON	10	+5VDC
3	−15VDC (V−)	11	$\overline{CK}$
4	OUTPUT	12	$\overline{PR}$
5	EXT. HOLD CAP. HI	13	POWER COMMON
6	OUTPUT	14	EXT. HOLD CAP. LO
7	INVERT OUT	15	+15VDC (V+)
8	INVERT IN	16	GUARD COMMON

NOTE: PINS HAVE 0.035 ± 0.010 INCH STANDOFF FROM CASE.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, Pin 15	+18V
Negative Supply, Pin 3	−18V
Logic Supply, Pin 10	5.5V
Analog Input Voltage	$\pm V_S$

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

ANALOG INPUT	
Input Voltage Range	±11.5V
Input Impedance	$10^{10}\Omega$
Input Offset Voltage, max.[1]	±2 mV
Input Offset Voltage Drift	20 μV/°C
Input Bias Current, max.	50 nA
DIGITAL INPUTS	
Logic Level High, V_{in} ("1"), min.	+2V
Logic Level Low, V_{in} ("0"), max.	+0.8V
High Level Input Current	60 μA
Low Level Input Current	−0.8 mA
Inverter Input Delay, max.[2]	30 nsec.
OUTPUT	
Output Voltage Range	±11.5V
Output Current, S.C. Protected	5 mA
Output Impedance	0.5Ω
PERFORMANCE	
Accuracy	0.01%
Gain	+ 1 V/V
Gain Error, max.[3]	0.01%
Sample to Hold Offset, max.[4]	2.5 mV
Hold Mode Feedthrough	0.01%
Hold Mode Droop, max.	0.2 mV/msec.
Output Noise, Hold Mode[5]	8.5 μV RMS
Power Supply Rejection Ratio min.	80 dB
DYNAMIC CHARACTERISTICS	
Acquisition Time, 10V to 0.1%	5 μsec.
10V to 0.01%	6 μsec.
20V to 0.1%	7 μsec.
20V to 0.01%	8 μsec.
Aperture Delay Time	200 nsec.
Small Signal Bandwidth, −3 dB	4 MHz
POWER REQUIREMENTS	
Analog Supply Range	±5V dc to ±18V dc
Supply Voltage, Rated Performance	±15V dc at 6.5 mA max.
Logic Supply	+5V dc ±0.25V at 9 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range: MC	0°C to +70°C
MM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package	16 pin hermetically sealed ceramic DIP

FOOTNOTES:

1. Adjustable to zero
2. This specification refers to the time delay between the invert input (Pin 8) and invert output (Pin 7).
3. R_L = 10 kΩ
4. V_{out} = OV
5. 10 Hz to 100 kHz

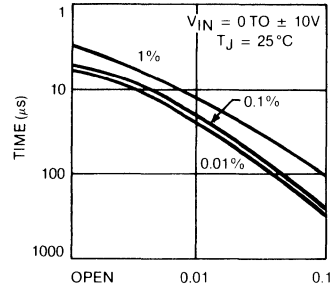
TECHNICAL NOTES

1. An external hold capacitor may be added from Pin 5 (EXT. CAP. HIGH) to Pin 14 (EXT. CAP. LOW). For best results, this should be a good quality capacitor with very high insulation resistance and low dielectric absorption; such as MOS, polystyrene or polypropylene type capacitors. Hold mode droop and sample to hold offset will decrease proportionately with the size of this capacitor, and acquisition time will increase proportionately. For lowest hold mode droop, a guard ring connected to the output should be put around EXT. CAP. HIGH Pin (Pin 5), as shown in the circuit board layout.
2. Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this, the circuit board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source.

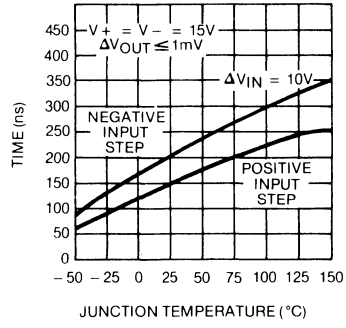
3

PERFORMANCE CURVES

ACQUISITION TIME

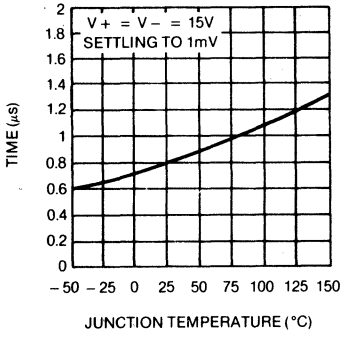


APERTURE TIME

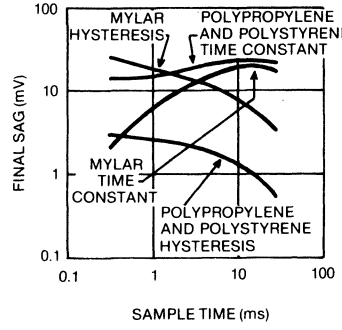


PERFORMANCE CURVES

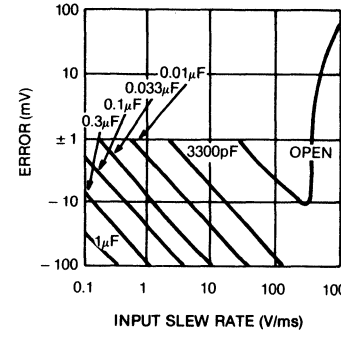
"HOLD" SETTLING TIME



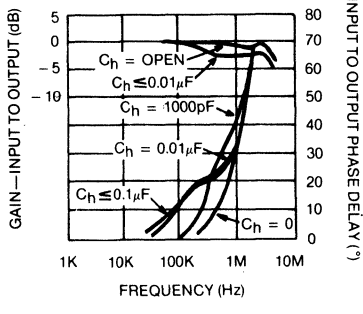
CAPACITOR HYSTERESIS



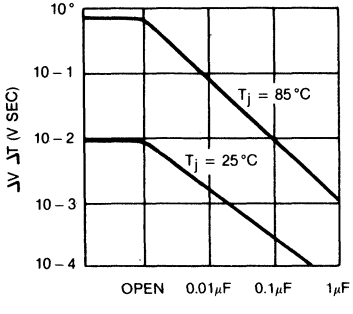
DYNAMIC SAMPLING ERROR



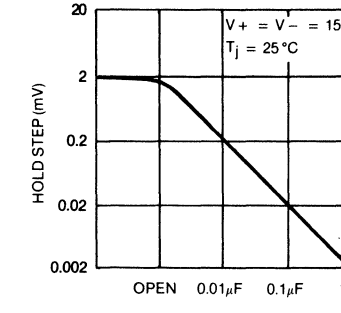
PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)



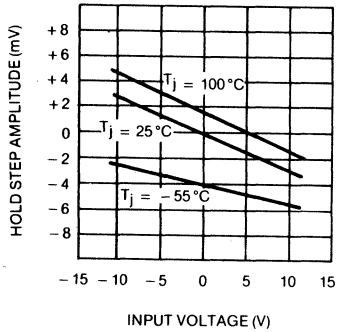
OUTPUT DROOP RATE



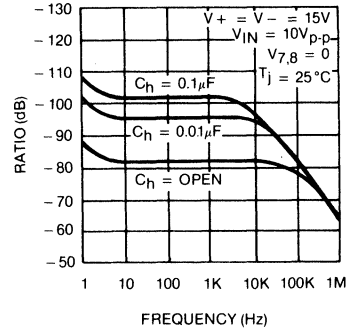
HOLD STEP



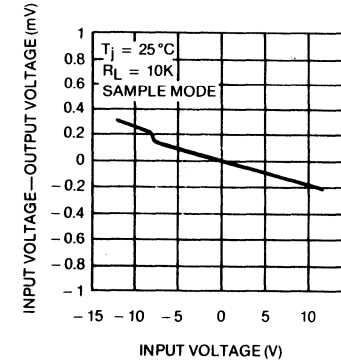
HOLD STEP INPUT VOLTAGE



FEEDTHROUGH REJECTION RATIO (HOLD MODE)

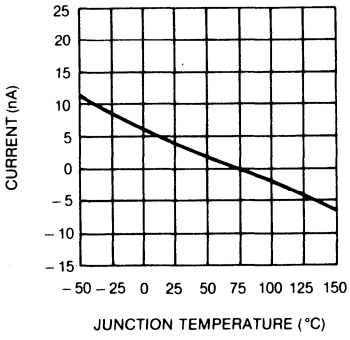


GAIN ERROR

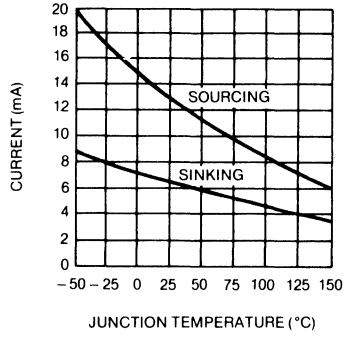


PERFORMANCE CURVES

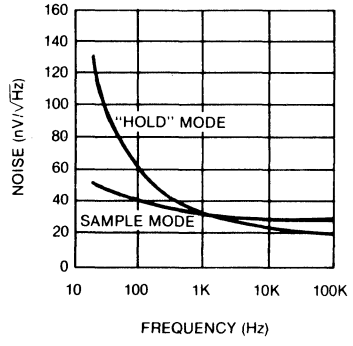
INPUT BIAS CURRENT



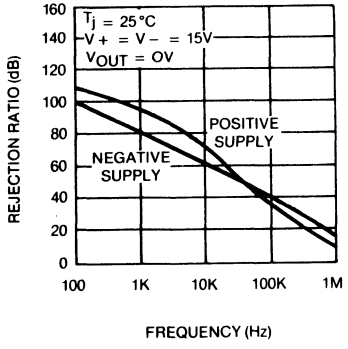
OUTPUT SHORT CIRCUIT CURRENT



OUTPUT NOISE

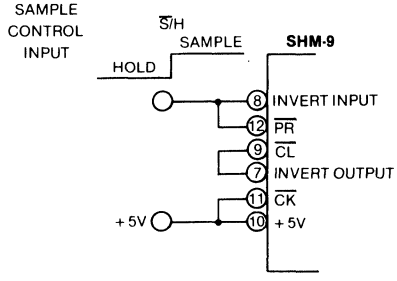


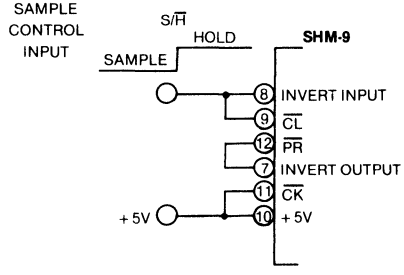
POWER SUPPLY REJECTION



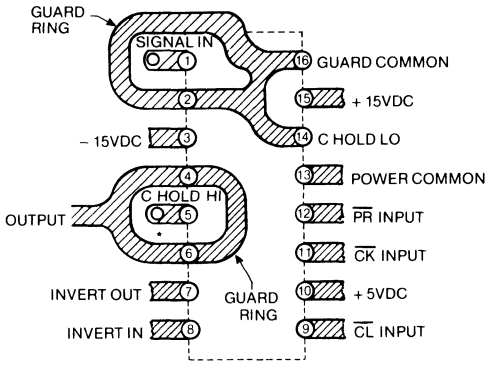
CONNECTIONS

SINGLE LINE CONTROL





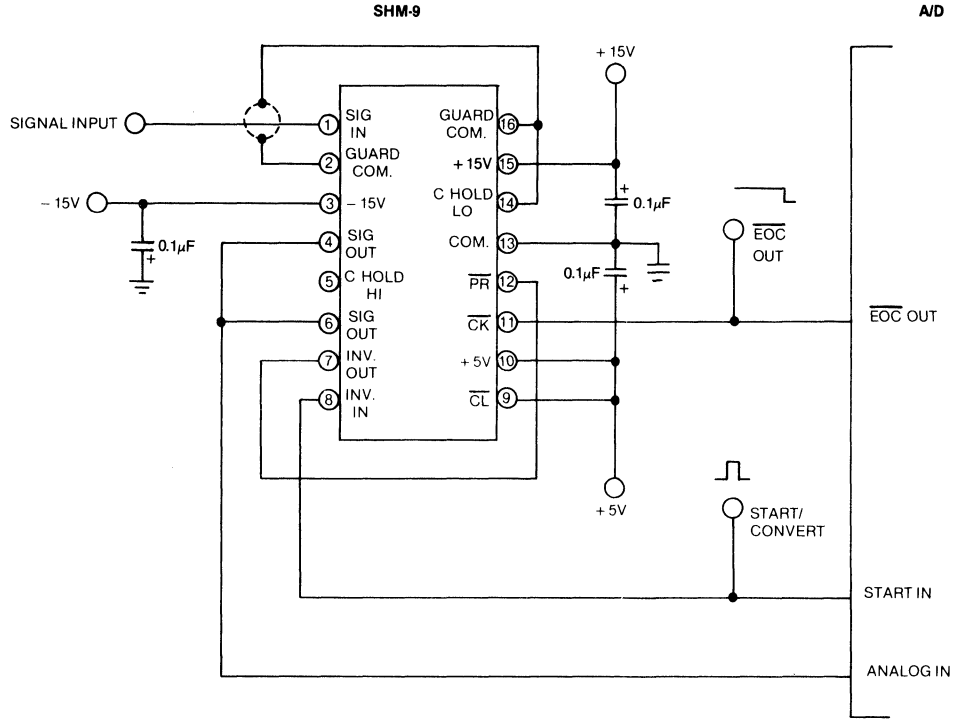
CIRCUIT BOARD LAYOUT



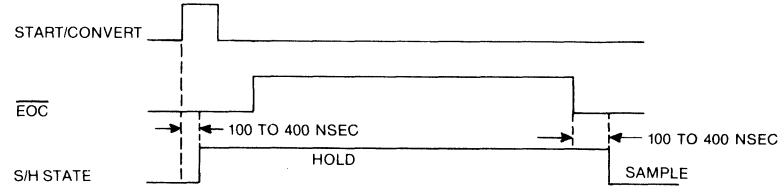
*ADDITIONAL EXTERNAL CAP, IF USED

The SHM-9 sample/hold switch can be controlled with one hold command input. The above diagrams give the circuit connection for either a Sample/Hold or a Sample/Hold control input. When using the SHM-9 with an A/D converter, the converters' E.O.C. (STATUS) output can be used to control the SHM-9.

APPLICATION
A/D INTERFACE



TIMING DIAGRAM



The SHM-9 is easily interfaced with most A/D converters. The diagram shows a typical connection in which the SHM-9 is controlled by the Start/Convert and EOC (Status) signals of the A/D converter. The Start/Convert signal puts the SHM-9 into the hold mode. The internal inverter allows the designer to use either a positive or negative Start/Convert signal. When the E.O.C. signal goes high and the A/D begins its conversion cycle, the SHM-9 is already providing a stable analog input to the A/D's comparator. When the E.O.C. goes low, signaling the end of conversion, the SHM-9 is switched back to the sample mode.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-9MC	0°C to +70°C
SHM-9MM	–55°C to +125°C

For high reliability devices, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SHM-91
PRECISION DUAL SAMPLE-AND-HOLD

FEATURES

- **Contains two precision sample/hold amplifiers**
- **Designed for use with 12- or 14-bit A/D converters**
- **Fast acquisition time (2 μSec. to ±0.002%)**
- **No external components required**
- **Wide temperature range (−55 °C to +125 °C available)**
- **24-pin dual in-line package**
- **Multiplexed inputs and outputs for application versatility**

GENERAL DESCRIPTION

DATEL's SHM-91 is a high performance/ high resolution dual sample/hold amplifier. This hybrid device is designed for multi-channel analog signal processing applications with 12- to 14-bit accuracy requirements. Typical applications for this device would demand high speed and high resolution. The SHM-91 offers both of these features at a low cost.

The SHM-91 consists of two separate sample/hold amplifiers, each independently controlled to allow flexibility when implementing a system design. Each half consists of a two-channel input multiplexer and a sample/hold amplifier. The output of each sample/hold is available directly or through a multiplexed output.

Other features of the SHM-91 include a ±10V dc input range, a fixed gain of 1, and a maximum gain temperature coefficient of 10ppm/ °C. The SHM-91 is actively laser trimmed at the factory for low initial offset and sample-to-hold offset. By design, the SHM-91 operates without external adjustment circuits.

The SHM-91 also features a maximum acquisition time of 2 microseconds for a 10V dc input step to 0.002%. Aperature uncertainty is typically 300 picoseconds and pedestal error will not exceed ±1 mV.

Power requirements is ±15V dc with a maximum power consumption of 900 mW. The SHM-91 is available in two models for operation over the commercial 0°C to +70°C and military −55°C to +125°C operating temperature ranges. All models are cased in a 24-pin, hermetically-sealed ceramic package.

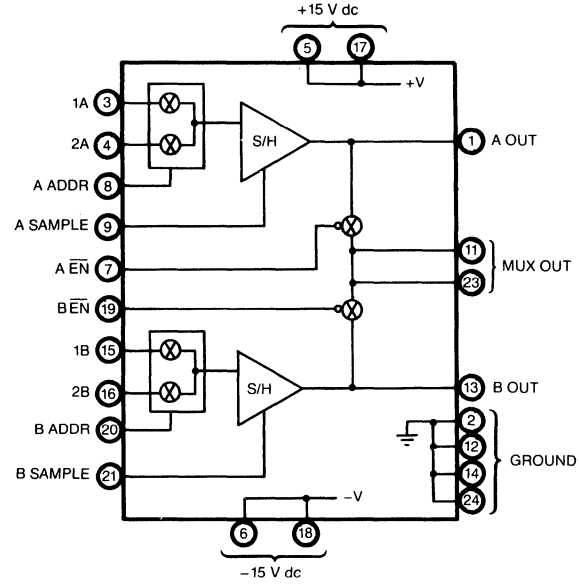
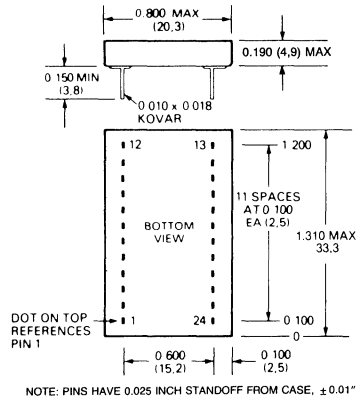


Figure 1. SHM-91 Simplified Block Diagram

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL
1	A OUT
2	GROUND
3	1A
4	2A
5	+15V dc
6	−15V dc
7	A $\overline{EN}$
8	A ADDR
9	A SAMPLE
10	NO CONNECTION
11	MUX OUT
12	GROUND
13	B OUT
14	GROUND
15	1B
16	2B
17	+15V dc
18	−15V dc
19	B $\overline{EN}$
20	B ADDR
21	B SAMPLE
22	NO CONNECTION
23	MUX OUT
24	GROUND

ABSOLUTE MAXIMUM RATINGS

Positive Supply (Pins 5, 17)	−0.5V dc to +18V dc
Negative Supply (Pins 6, 18)	+0.5V dc to −18V dc
Digital Input Voltages	
Address, Sample (Pins 8, 9, 20, 21)	−0.5V dc to +7V dc
Mux. Enable (Pins 7, 19)	−18V dc to +18V dc
Analog Input Voltage	±15V dc

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the full operating temperature range and power supply range unless otherwise specified. For test aspects, contact the factory.

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
ANALOG INPUTS				
Input Voltage Range	±10	–	–	V
Input Impedance	1M	–	–	Ohm
Input Capacitance	–	–	30	pf
Input Bias Current	–	–	1.5	μA
LOGIC INPUTS (TTL/CMOS)				
Logic 1 voltage	2.4	–	–	V
Logic 0 voltage	–	–	0.8	V
Logic 1 current	–	–	1	μA
Logic 0 current	–	–	1	μA
ANALOG OUTPUTS				
Direct Output (pins 1, 13)				
Output Voltage Range	±10	–	–	V
Output Current	10	–	–	mA
Output Impedance	–	1	2	Ohm
Mux. Output (pins 11, 23)				
Output Voltage Range	±10	–	–	V
Output Current	10	–	–	mA
Output Impedance	–	50	150	Ohms
OFF Output Leakage	–	–	1	μA
OFF Output Capacitance	–	–	20	pf
Output Switch Delay	–	–	500	nS
PERFORMANCE				
Gain (1)	–	+1	–	–
Gain Error (1)	–	–	±0.02	%
Gain Tempco	–	1	10	ppm/°C
Linearity Error (1)	–	–	0.003	% FSR
Linearity Tempco.	–	–	±1	ppm/°C
Initial Offset Voltage (2)	–	–	±1	mV
Offset Tempco., Hold Mode	–	20	50	μV/°C
Crosstalk, channel-to-channel	-90	–	–	dB
Offset Tempco. Tracking (A vs. B)	–	±10	±20	μV/°C
Gain Tracking (A vs. B)	–	–	±50	ppm
Gain Tracking Tempco.	–	–	±0.5	ppm/°C
TRACK MODE DYNAMICS				
Frequency Response Small Signal (−3dB)	–	–	1	Mhz
Slew Rate	–	45	–	V/μS

FUNCTIONAL SPECIFICATIONS (continued)

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
TRACK-TO-HOLD SWITCHING				
Aperture Delay Time	–	15	–	nS
Aperture Uncertainty (Jitter)	–	300	1,000	pS
Offset Step (2)	–	–	±1	mV
Settling Time to ±2 mV	–	–	600	nS
HOLD MODE DYNAMICS				
Droop Rate				
At +25 °C	–	–	5	μV/μS
At +85 °C	–	–	20	μV/μS
At +125 °C	–	–	100	μV/μS
Feedthrough Rejection	−90	–	–	dB
HOLD-TO-TRACK DYNAMICS				
Acquistion Time				
10 Volt Step to ±0.2 mV	–	–	2	μS
10 Volt Step to ±1 mV	–	–	1.5	μS
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range ±V	±14.5	±15	±15.5	Vdc
Power Supply Rej. Ratio	−60	–	–	dB
Current Drains				
+15V dc	–	–	30	mA
−15V dc	–	–	30	mA
Power Dissipation	–	700	900	mW
PHYSICAL/ENVIRONMENTAL				
Thermal Resistance				
Junction-to-Case	–	0.015	–	°C/mW
Case-to-Ambient	–	0.035	–	°C/mW

Operating Temperature Range (3)	
SHM-91MC	0 °C to +70 °C (ambient)
SHM-91MM	−55°C to +110°C (ambient)
Storage Temp. Range	−55°C to +125°C
Package Type	24-pin, hermetically sealed ceramic DIP
Package Dimensions	Refer to the Mechanical Dimensions

FOOTNOTES:

1- Specified at +25 °C.
2- Tested at +25 °C with input source impedance of 50 ohms.
3- Free air.

TECHNICAL NOTES

1. All ground pins (2, 12, 14, 24) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. The power supply pins (5, 6, 17, 18) should be bypassed to analog ground with .01 μF ceramic capacitors located as close to the pins as possible. In certain critical applications, additional bypass precautions using 0.1 or 1.0 μF tantalum capacitors are suggested.
2. A logic "1" on the sample pins (9, 21) will put this device in the sample mode. In this mode, the device acts as an unity gain amplifier and its output will track its input. A logic "0" on the sample pins (9, 21) will put the device in the hold mode, and the output will be held constant at the last input level present before the hold command was given.

3. Care should be taken when using the multiplexer output pins (11, 23) that the A $\overline{EN}$ (pin 7) and the B $\overline{EN}$ (pin 19) are not active (logic 0) at the same time. This condition could possibly damage the device.
4. The output of the SHM-91 should drive a high impedance receiver to minimize voltage divider losses. The receiver input impedance should be 100K ohms or greater when using the direct outputs from the amplifiers (pins 1 and 13). The receiver input impedance should be 2.5 M ohms or greater when using the multiplexer outputs (pins 11 and 23).
5. The SHM-91 should not be left in the hold mode for long periods of time. It should be left in the sample mode when long or indeterminate periods of time are involved. If left in the hold mode for several seconds, the output will continue to "droop" toward the power supply voltage. Eventually the output amplifier will saturate. The unit will require longer than the specified acquistion time to acquire a signal when the output amplifiers are saturated.
6. See charts in Figures 2b and 3b for input selection.

APPLICATIONS

Single Channel Application

Figure 2a shows how to use one of the SHM-91's sample-and-holds with multiplexed inputs. The output reflects the sampled input. The timing diagram, Figure 2b, shows that with the ADDR line low, the leading edge of the SAMPLE line pulse causes the input on 2A to be passed on to the output. The output reflects any amplitude change on 2A that occurs during the pulse width of the sample pulse. The falling edge of the sample pulse causes the output to hold the current 2A input level.

When ADDR goes high, it switches the sampled channel to 1A. On the next occurence of a sample pulse, the output will reflect any amplitude change occuring on 1A during the sampling period. The subsequent hold state signal is at whatever level the 1A input was at when the sample pulse ended.

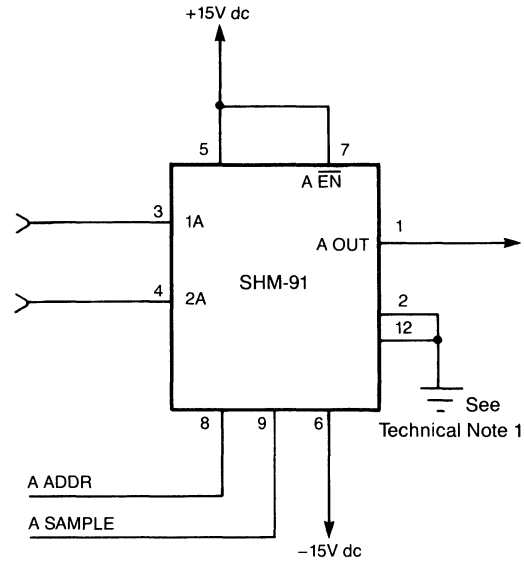
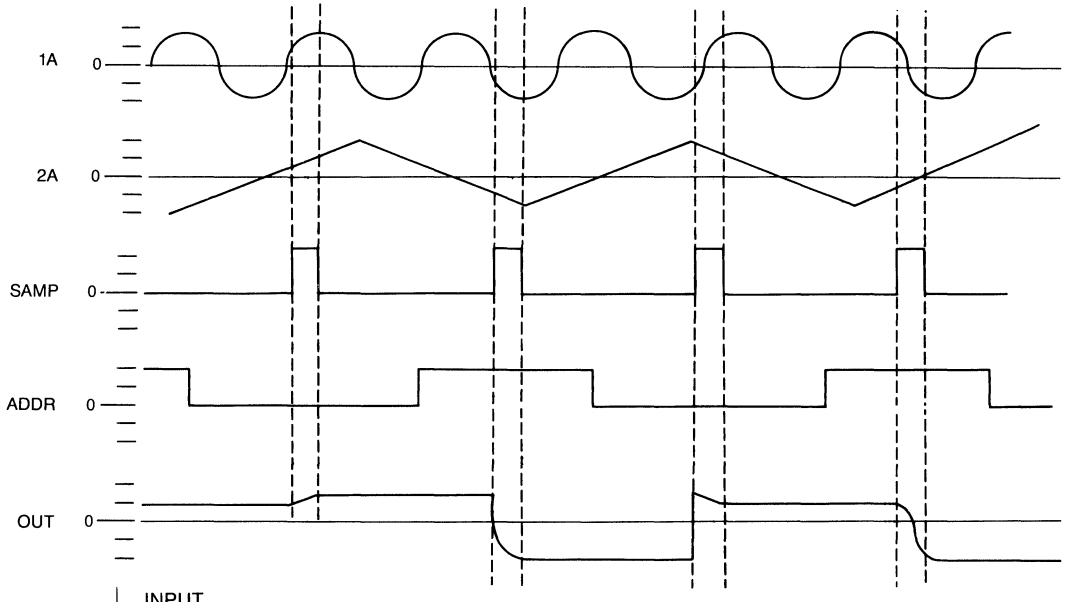
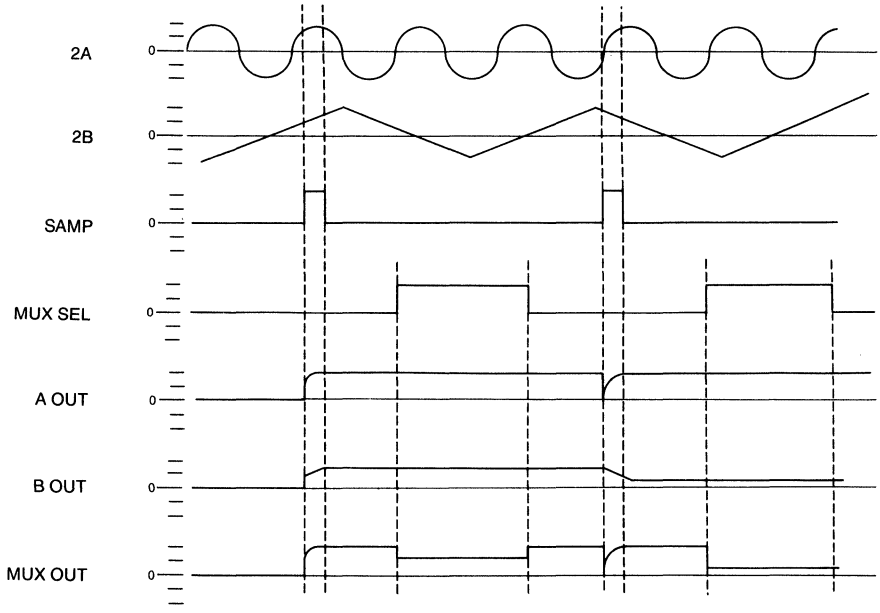


Figure 2a. SHM-91 Single Sample-and-Hold Configuration



ADDR	INPUT CHANNEL
0	2
1	1

Figure 2b. Typical Timing for Single Channel Sampling



ADDR	INPUT CHANNEL
0	2
1	1

Figure 3b. SHM-91 Simultaneous Sample-and-Hold Timing

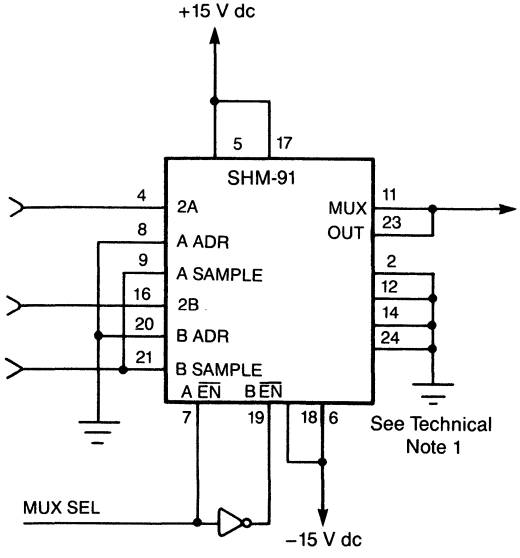


Figure 3a. SHM-91 Simultaneous Sample-and-Hold Configuration

Simultaneous Sample-and-Hold

The SHM-91 is ideally suited for simultaneous sample-and-hold applications. Figure 3a represents a typical connection diagram along with a timing diagram (Figure 3b) of the SHM-91's operation. In a simultaneous sample-and-hold application, data must be taken from all analog inputs at precisely the same time.

All SHM-91's in the application are given the hold command at the same time. The internal multiplexer then sequentially switches between sample-and-hold outputs while an A/D converter would digitize the outputs. A high-impedance buffer amplifier would be required between the multiplexer and the A/D converter.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE
SHM-91-MC	0°C to +70°C
SHM-91-MM	−55°C to +125°C

For high reliability versions of the SHM-91, contact DATEL.

SHM-HU
Ultra-Fast, 0.1% Micro-electronic Sample/Hold

FEATURES

- **25 Nanoseconds acquisition time**
- **50 MHz bandwidth**
- **10 Picoseconds aperture uncertainty**
- **Up to 8-bit accuracy**
- **±2.5V Input range**

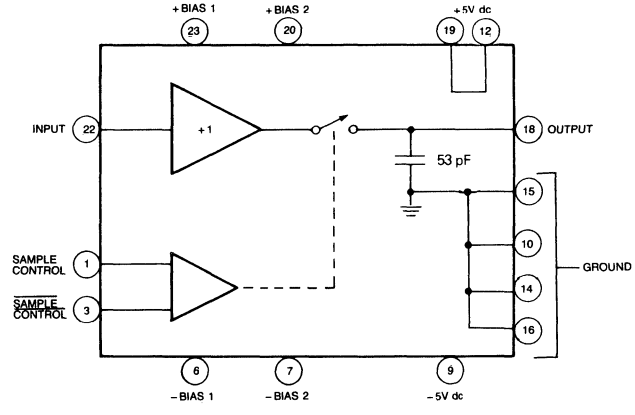
GENERAL DESCRIPTION

The SHM-HU is an ultra high speed sample-hold capable of video speed signal processing. The SHM-HU acquires a full-scale 5V input change in just 25 nanoseconds and features a 10 picoseconds aperture uncertainty time. Bandwidth is 50 MHz and the slew rate is 200 V/microseconds.

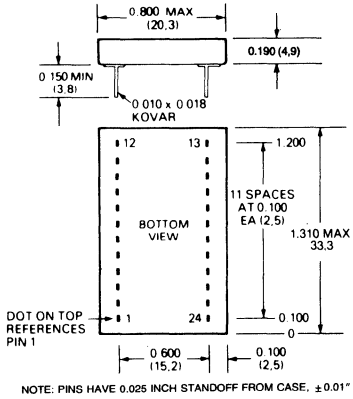
Through the use of thin film hybrid construction, this ultra high speed circuit is contained in a miniature 24-pin ceramic package. A 53 picofarad MOS hold capacitor is incorporated inside the package and provision is made for externally added capacitance when necessary. The sample-hold requires four external resistors and an LH0033 fast buffer amplifier for completion. The circuit is zeroed by adjustment of the LH0033 amplifier.

Other features of this unit include a ±2.5V input/output voltage range and a fixed gain of 0.955. The sampling switch is controlled by a complementary series 10,000 ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

Power requirements are ±15V dc at 60 mA and ±5V dc at 70 mA. There are three basic models covering two operating temperature ranges, 0 to +70° C and -55 to +100° C.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
3	SAMPLE CONTROL
6	-BIAS 1
7	-BIAS 2
9	-5V POWER
10	GROUND
12	+5V POWER
14	GROUND
15	GROUND
16	GROUND
18	OUTPUT
19	+5V POWER
20	+BIAS 2
22	INPUT
23	+BIAS 1

NOTE: ALL OTHER PINS ARE NO CONNECTION

ABSOLUTE MAXIMUM RATINGS

Power Supplies, Pins 9-19	±6V
Analog Input Voltage, Pin 22	±5V
Sample Inputs, Pins 1 & 3	±5V Differential
Current, Pins 6, 7, 20, 23,	50 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and ±5V supplies with external LH0033 Buffer Amplifier unless otherwise noted.

INPUTS	
Input Voltage Range, Min.	±2.5V
Input Bias Current	25 μA
Maximum Source Impedance	51 Ohms
Input Impedance	10^6 Ohms
Sample Control Inputs[4]	Differential ECL 10,000 Positive Pulse on Pin 1 and Negative Pulse on Pin 3 gives Sample Mode
OUTPUT[1]	
Output Voltage Range, Min.	±2.5V
Output Current	±10 mA
Output Impedance	6 Ohms
PERFORMANCE	
Accuracy	0.1%
Gain	+0.995
Output Offset Voltage[2], Sample Mode	±100 mV max.
Output Offset Voltage Drift	±100 μV/°C max.
Sample to Hold Offset Error	±100 mV max.
Hold Mode Droop	50 μV/μsec.
Hold Mode Feedthrough	0.02%
DYNAMIC RESPONSE	
Acquisition Time, 5V Step to 0.2%	25 nsec.
Bandwidth, −3 dB, Sample Mode	50 MHz
Slew Rate	200V/μsec.
Aperture Delay Time	6 nsec.
Aperture Uncertainty Time	10 psec.
POWER REQUIREMENTS[3]	
Power Supply Voltage	±15V dc ±0.75V at 60 mA ±5V dc ±0.25V at 70 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-HUMC	0 to +70°C
SHM-HUMM	−55 to +100°C
Storage Temperature Range	−65 to +150°C
Package Type	24 Pin Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

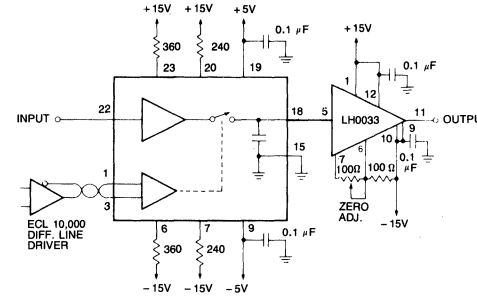
FOOTNOTES:

1. Output is from LH0033 amplifier and is not short circuit proof.
2. Output offset voltage adjustable to zero by LH0033 offset adjustment.
3. ±12V supplies can be used if the 360 ohm resistors at the Bias 1 pins are changed to 240 ohms and the 240 ohm resistors at the Bias 2 pins are changed to 160 ohms.
4. The SHM-HU can be driven by TTL logic input by biasing $\overline{\text{SAMPLE}}$ CONTROL input to +1.2V and driving the SAMPLE CONTROL with a positive pulse for sampling mode.

TECHNICAL NOTES

1. It is recommended that the ±5V supplies of the SHM-HU be bypassed with 0.1 μF ceramic capacitors as close as possible to pins 9 and 19. The ±15V supplies to the LH0033 should be bypassed with the same value capacitors.
2. It is essential that the output lead from pin 18 to pin 5 of the LH0033 be kept as short and direct as possible. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.
3. With model SHM-HUMC the LH0033C should be used, and with model SHM-HUMM, model LH0033 should be used.
4. An external hold capacitor may be added from pin 18 to pin 15. This capacitor should be an MOS or polystyrene type. Hold mode Droop and sample-to-hold offset error will decrease proportionately with the size of this capacitor and acquisition time will increase proportionately.

CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-HUMC	0 to +70°C
SHM-HUMM	−55 to +100°C

ACCESSORIES

Part Number	Description
DILS-3 (24-Pin Socket)	Mating Socket
TP100 (100 ohms)	Trimming Potentiometer

For high reliability devices, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SHM-IC-1
Monolithic Sample-Hold

Features

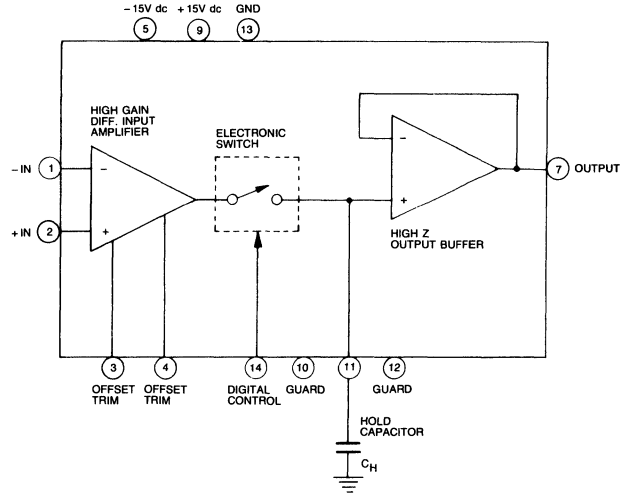
- **5 Microseconds acquisition to 0.01%**
- **50 Nanoseconds aperture**
- **Inverting or noninverting**
- **2 MHz Bandwidth**
- **0.01% Feedthrough**
- **14-pin DIP package**

GENERAL DESCRIPTION

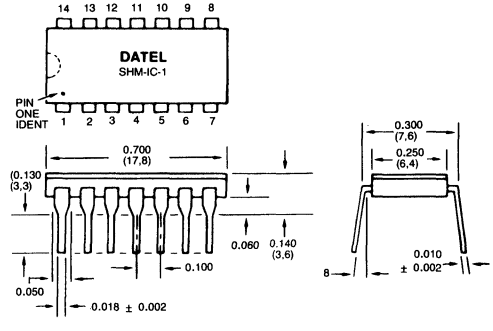
The SHM-IC-1 is a new monolithic integrated circuit sample and hold with excellent performance features. It is a self-contained device requiring only an external holding capacitor, the value of which can be chosen by the user to achieve his desired speed and accuracy requirement. The unit consists of a high gain differential input amplifier, a digitally controlled electronic switch, and a high input impedance buffer amplifier. The SHM-IC-1 operates in a closed loop configuration, either inverting or noninverting, with accuracy and speed determined by the input amplifier characteristics and the value of the holding capacitor. The electronic switch is controlled by a DTL/TTL compatible logic input.

The most common configuration for the SHM-IC-1 is a unity gain, noninverting sample and hold. In this configuration the device has a ± 10V input and output range with 10 ohms input impedance. Specifications are given for this unit with two different values of holding capacitor, 0.001 μF and 0.01 μF. The 0.001 μF capacitor gives a 4 microsecond acquisition time to 0.1% for a 10V change, a 2 MHz tracking bandwidth and 50 mV/millisecond maximum hold mode droop. The 0.01 μF capacitor gives a 10 microsecond acquisition time, 1 MHz tracking bandwidth, and 5 mV/millisecond maximum droop. Characteristics for other values of holding capacitor can be determined from graphs which are shown. The SHM-IC-1 can also be configured as either an inverting or noninverting sample and hold with gain by the use of two external resistors.

This device is housed in a 14-pin hermetically sealed dual-in-line package. Operating temperature range is 0°C to +70°C for the SHM-IC-1 and −55°C to +125°C for the SHM-IC-1M.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	−IN
2	+IN
3	OFFSET TRIM
4	OFFSET TRIM
5	−15VDC POWER
6	NO CONNECTION
7	OUTPUT
8	NO CONNECTION
9	+15VDC POWER
10	GUARD
11	HOLD CAPACITOR (C_H)
12	GUARD
13	GROUND
14	DIGITAL CONTROL

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc Supplies, unless otherwise noted.

INPUT AMPLIFIER SPECIFICATIONS	
DC Gain, volts/volt[1]	50K, 25K minimum
Bias Current	50 nA, 200 nA maximum
Offset Current	10 nA, 50 nA maximum
Offset Voltage (adjustable to zero)	3 mV, 6 mV maximum
Offset Voltage Drift	20 μV/°C
Common Mode Voltage Range	±10V minimum
Common Mode Rejection Ratio	74 dB minimum
Power Supply Rejection	±30 μV/%maximum
Gain Bandwidth Product	2 MHz
GENERAL SPECIFICATIONS, SAMPLE & HOLD, G = +1	
Input Voltage Range	±10V minimum
Input Impedance	10^6 ohms
Output Voltage Range	±10V minimum
Output Current, S.C. protected	±10 mA minimum
Output Impedance	0.2 ohm
Aperture Delay	50 nanoseconds
Aperture Uncertainty	5 nanoseconds
Gain Error, sampling mode	0.01% maximum
Hold Mode Noise	350 μV RMS
Digital Input, Sample Mode, DTL/TTL	0 to +0.8V at −0.8 mA
Hold Mode, DTL/TTL[2]	+2.0 to +5.5V at +20 μA
SAMPLE & HOLD, G = +1, C_H = 0.001 μF	
Acquisition Time, 10V to 0.1%	4 microseconds
Acquisition Time, 10V to 0.01%	5 microseconds
Bandwidth, small signal, sampling	2.0 MHz
Slew Rate	5 V/microseconds
Hold Mode Voltage Droop	50 mV/millisecond maximum
Hold Mode Feedthrough	0.01% maximum
Sample-to-Hold Offset Error, V_{IN} = 0	20 mV maximum
Sample-to-Hold Gain Error, V_{IN} = ±10V	0.05% maximum of output
Sample-to-Hold Nonlinearity Error	0.01% maximum of output
SAMPLE & HOLD, G = +1, C_H = 0.01 μF	
Acquisition Time, 10V to 0.1%	10 microseconds
Acquisition Time, 10V to 0.01%	12 microseconds
Bandwidth, small signal, sampling	1.0 MHz
Slew Rate	3 V/microseconds
Hold Mode Voltage Droop	5 mV/millisecond maximum
Hold Mode Feedthrough	0.002% maximum
Sample-to-Hold Offset Error, V_{IN} = 0	2 mV maximum
Sample-to-Hold Gain Error, V_{IN} = ±10V	0.005% maximum
Sample-to-Hold Nonlinearity Error	0.001% maximum
POWER REQUIREMENTS	
Power Supply Voltage	±15V dc at 5.5 mA maximum
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range, SHM-IC-1	0°C to 70°C
Operating Temperature Range, SHM-IC-1M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package, hermetically sealed ceramic DIP	TO-116

FOOTNOTES:

1. 40K and 20K respectively at +125°C for SHM-IC-1M.
2. +3.0 to +5.5V at −55°C for SHM-IC-1M.

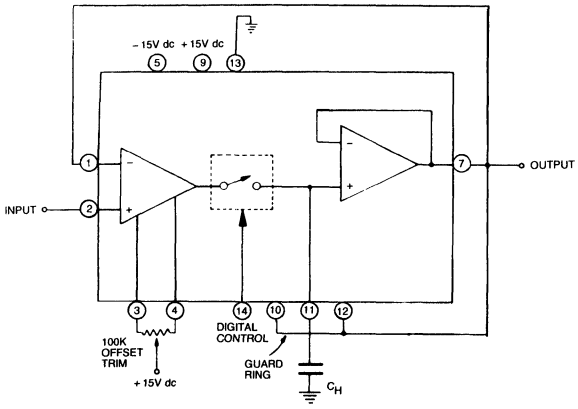
TECHNICAL NOTES

The most commonly used sample and hold configuration for the SHM-IC-1 is the noninverting unity gain circuit. This gives a high input impedance of 10^8 ohms, and the output voltage in the sample module follows the input. Specifications are given for this configuration for two values of C_H, 0.001 μF and 0.01 μF. The 0.001 μF capacitor gives excellent speed (4 microseconds acquisition) with good hold mode voltage droop (only 50 mV/millisecond maximum). For even better speed, a 100 pF capacitor may be used to give an acquisition time of only 2 microseconds. The hold mode droop, however, increases by an order of magnitude to 500 mV/millisecond, and the sample-to-hold errors also increase. For excellent accuracy a 0.01 μF capacitor should be used, giving an acquisition time of 10 microseconds, and a hold mode droop of only 5 mV/millisecond maximum. Even larger values of holding capacitor can be used with proportionate increases in accuracy but slower speed. The application graphs show the results for the different values.

For best results, C_H should be a good quality capacitor with very high insulation resistance and low dielectric absorption. For temperatures up to +85°C polystyrene type capacitors are recommended. It is also recommended for lowest hold mode droop that a guard ring be used around the C_H terminal (pin 11) in the circuit board layout as shown on the last page. This is done to prevent leakage to other conductors on the circuit board due to board leakage and contamination. If a large value polystyrene capacitor is used, such as 1 μF, hold mode droop as low as 20 μV/seconds (typical) can be achieved with an acquisition time of about 3 milliseconds.

Three error contributions are specified for sample-to-hold errors: offset error, gain error, and nonlinearity error. These sampling errors are caused by a small amount of charge being dumped to or from the holding capacitor by the sampling switch and are reduced by a larger value of C_H. It is possible to compensate for these errors by changing the gain and offset elsewhere in the external circuitry for the noninverting unity gain case. For the inverting case, the gain can be accomplished by adjusting the external resistor values and an offset can be applied to pin 2 of the input amplifier. When this external compensation is used, the output will be in error during sampling, but will be accurate in the hold mode. Only the nonlinearity error will remain of the sample-to-hold errors. The offset adjustment of the input amplifiers should be used only to zero the device in the sample mode.

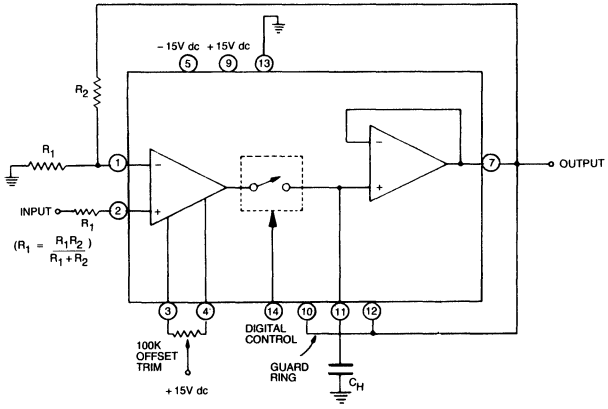
In the inverting gain of one operating mode, the feedback and input resistors should be carefully matched or trimmed to give the desired gain of one. In general, the operating parameters are the same as in the noninverting unity gain configuration except that the sampling bandwidth is reduced by a factor of two. Likewise, for higher gain configurations the sampling bandwidth is proportionately reduced.



NONINVERTING SAMPLE-HOLD, UNITY GAIN

$$GAIN = +1$$

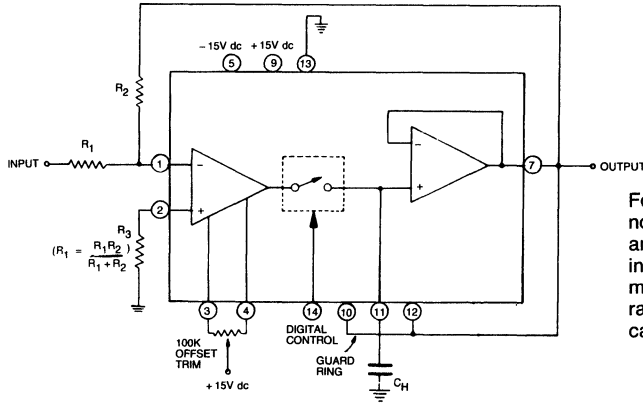
The 100K ohm offset trimming potentiometer should be a 100 ppm/°C cermet 15 turn type. These are available from DATEL. To zero, ground input (pin 2) and digital control (pin 14) and adjust 100K offset trim for zero output (pin 7).



NONINVERTING SAMPLE-HOLD

$$GAIN = 1 + \frac{R_2}{R_1}$$

Bandwidth decreases proportionately with gain. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be 100 ppm/°C metal film type resistors.

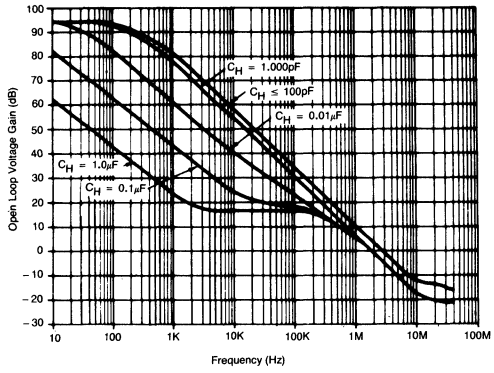


INVERTING SAMPLE-HOLD

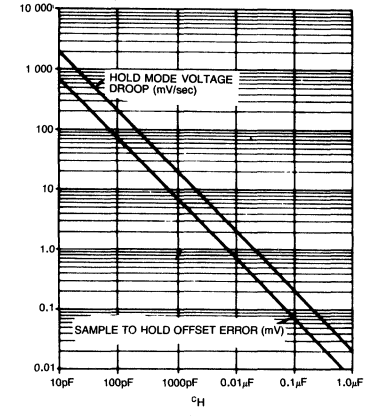
$$GAIN = -\frac{R_2}{R_1}$$

For a gain of -1 the bandwidth is one half of that given for the noninverting mode. R_3 is equal to the parallel combination of R_1 and R_2 and is used to compensate for voltage offset caused by input bias current. R_1 and R_2 should be matched 100 ppm/°C metal film type resistors for a gain of -1. For higher gains the ratio should be matched closely or trimmed with a small value carbon composition type resistor.

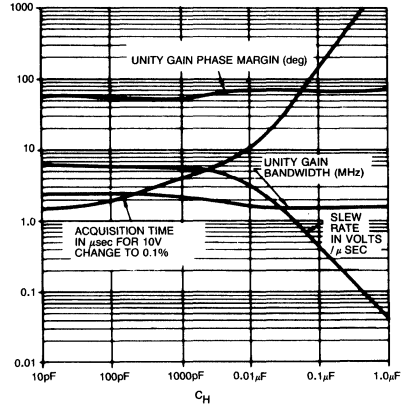
OPEN LOOP FREQUENCY RESPONSE
Typical at 25°C, ±15V Supplies



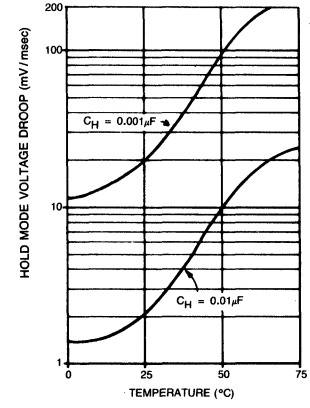
ACCURACY CHARACTERISTICS VS. C_H
Typical at 25°C, ±15V Supplies



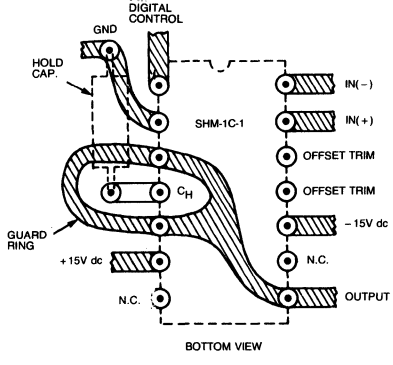
SPEED CHARACTERISTICS VS. C_H
Typical at 25°C, ±15V Supplies



HOLD MODE VOTLAGE DROOP VS. TEMPERATURE
Typical ±15V Supplies



RECOMMENDED CIRCUIT BOARD LAYOUT
USING GUARD RING



ORDERING INFORMATION

MODEL NO.

SHM-IC-1
SHM-IC-1M

ACCESSORIES

Part Number	Description
TP100K (100 KΩ)	Trimming Potentiometer

Contact Factory for Quantity Pricing

SHM-LM-2
Low Cost Monolithic Sample-Hold

FEATURES

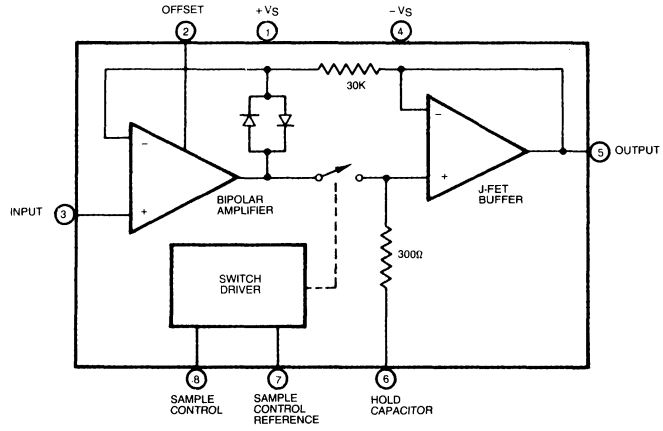
- **5 Microseconds acquisition time**
- **0.01% Gain accuracy**
- **TTL/CMOS-compatible**
- **±5V to ±18V supplies**
- **TO-99 package**
- **Low cost**

GENERAL DESCRIPTION

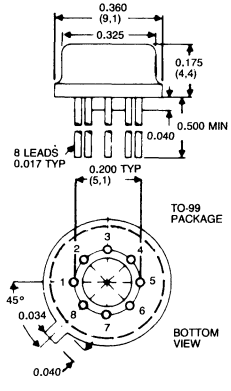
The SHM-LM-2 is a low cost monolithic sample-hold circuit with excellent performance features. It is self-contained requiring only an external hold capacitor with the value selected by the user for desired speed and accuracy characteristics. Acquisition time is 6 microseconds for a 10V change to 0.01% using a 1000 pF capacitor and 25 microseconds using a 0.01 μF capacitor. It is 5 microseconds and 20 microseconds respectively for a 10V change to 0.l%. This device is internally configured as a unity gain follower with a gain error of less than 0.01% in the sample mode.

The circuit consists of a bipolar input amplifier, a low leakage electronic switch, and an FET output amplifier. The monolithic fabrication process combines P channel junction FET's with bipolar transistors to achieve a low noise, high input impedance output amplifier. Other important specifications include 10^{10} ohms input impedance and 1 MHz bandwidth. Aperture time is less than 100 nanoseconds and hold mode feedthrough is less than 0.005%. Hold mode droop is 200 μV/mseconds maximum with a 1000 pF hold capacitor and 20 μV/mseconds maximum with a 0.01 μF capacitor. The SHM-LM-2 can operate over a power supply range of ±5V to ±18V.

Applications include sampling for A/D conversion, deglitching circuits, automatic zeroing circuits, and analog demultiplexing circuits. It is recommended that the holding capacitor (C_H) be a teflon, polystyrene, or polypropylene type for best results. Operating temperature range is 0°C to +70°C for SHM-LM-2 and −55°C to +125°C for SHM-LM-2M.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: ALL LEADS GOLD PLATED KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+POWER SUPPLY
2	OFFSET ADJUST
3	INPUT
4	−POWER INPUT
5	OUTPUT
6	HOLD CAPACITOR (C_H)
7	SAMPLE CONTROL REF.
8	SAMPLE CONTROL

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, pins 1 and 4	±18V
Input Voltage, pin 3	±Supply
Sample Control to Sample Reference, pin 8 to pin 7	+7, −30V
Hold Capacitor Short Circuit	10 seconds

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies and C_H = 0.01 µF unless otherwise stated.

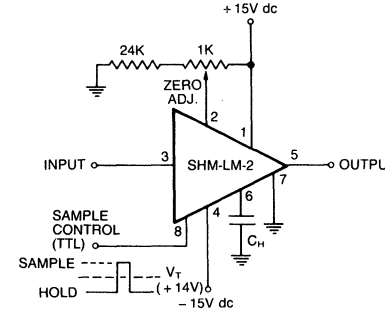
INPUTS	
Input Voltage Range	±11.5V minimum
Input Overvoltage, no damage	±Supply
Input Impedance	10^{10} ohms
Input Bias Current	10 nA typical, 50 nA maximum
Sample Control	TTL or CMOS
Sample Control Input Current[1]	10 µA maximum
OUTPUT	
Output Voltage Range	±11.5V minimum
Output Current, S.C. protected	±5 mA
Output Impedance	0.5 ohm
PERFORMANCE	
Gain	+1.000, +0, −0.01%
Output Offset Voltage, adj. to zero	±7 mV maximum
Offset Voltage Drift, SHM-LM-2	20 µV/°C
Offset Voltage Drift, SHM-LM-2M	10 µV/°C[2]
Sample to Hold Offset	2.5 mV maximum
Hold Mode Feedthrough	0.01% maximum
Power Supply Rejection Ratio	80 dB minimum
Output Noise, hold mode (10 Hz-100 kHz)	8.5 µV RMS
Hold Mode Droop, C_H = 1000 pF	200 µV/mseconds maximum
C_H = 0.01 µF	20 µV/mseconds maximum
DYNAMIC RESPONSE	
Acquisition Time	
10V Change, C_H = 1000 pF	5 microsecoonds to 0.1%
10V Change, C_H = 1000 pF	6 microseconds to 0.01%
20V Change, C_H = 1000 pF	7 microseconds to 0.1%
20V Change, C_H = 1000 pF	8 microseconds to 0.01%
10V Change, C_H = 0.01 µF	20 microseconds to 0.1%
10V Change, C_H = 0.01 µF	25 microseconds to 0.01%
Aperture Delay Time	100 nanoseconds
Hold Mode Settling Time[3]	800 nanoseconds
Bandwidth, Sample Mode, −3 dB	1 MHz
POWER REQUIREMENTS	
Voltage, rated performance	±15V dc
Voltage Range, operating	±5V to ±18V dc
Quiescent Current	6 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range, SHM-LM-2	0°C to +70°C
SHM-LM-2M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Case	8 pin TO-99

FOOTNOTES:
1. For either Sample Control or Sample Control Reference inputs
2. 28 µV/°C maximum
3. The time for the output to settle within 1 mV of final value after the logic command to switch into hold mode.

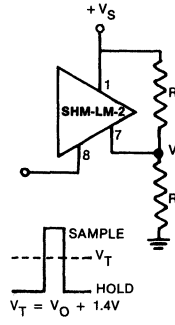
TECHNICAL NOTES

1. The sample to hold offset can be adversely affected by stray capacitive coupling from input sample control signals to the hold capacitor. It is recommended that a guard ring connected to the output be put around pin 6 in a circuit board layout in order to minimize this effect.
2. For various types of logic inputs, the logic threshold (V_T) is set by two biasing resistors as shown in the diagram. Inverted or non-inverted pulses may be used by using either pin 7 or pin 8 as the sample control input.

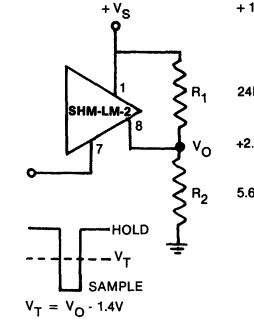
CONNECTION DIAGRAM



SAMPLE-CONTROL CONNECTIONS



FOR TTL CONNECT PIN 7 TO GROUND



FOR TTL USE VALUES SHOWN AT RIGHT

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-LM-2	0°C to 70°C
SHM-LM-2M	−55°C to +125°C

ACCESSORIES

Part Number	Description
TP1K	Trimming Potentiometer

SHM-UH Series
Ultra-High Speed
Sample-Holds

FEATURES

- **10 MHz sampling rate**
- **30 Nanoseconds acquisition time**
- **30 Picoseconds aperture uncertainty**
- **Diode bridge switch**
- **45 MHz bandwidth**

GENERAL DESCRIPTION

The SHM-UH series is comprised of two ultra-fast sample-holds specifically designed for use with ultra-fast 6-, 8- and 10-bit A/D converters. Both models in this series use an open loop design optimized for ultra-high speed operation. This design consists of an ultra-fast input buffer amplifier, a transformer driven diode bridge switch, and a high impedance output buffer amplifier.

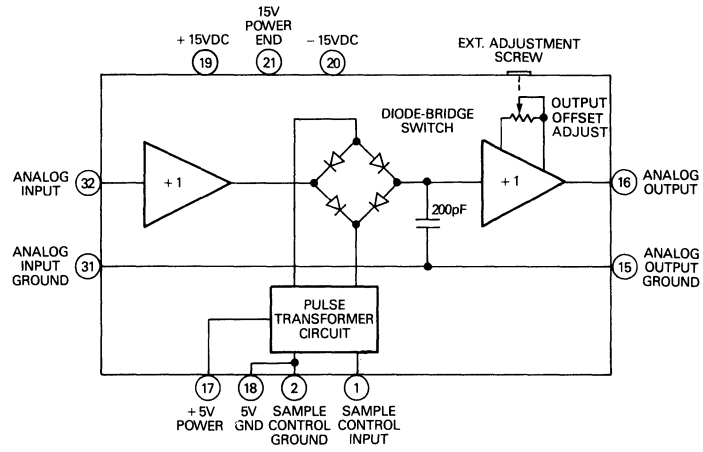
The unique pulse transformer driven diode bridge switch is a key design feature in attaining a 30 nanosecond acquisition time for a 10V signal change. This switch also holds aperture uncertainty time to less than 30 picoseconds for the SHM-UH3 and less than 200 picoseconds for the SHM-UH.

The SHM-UH3 is the newest member of this series and embodies substantial performance improvements on an already high performance design. This model is recommended for inclusion in new design applications. In addition to a 30 nanosecond acquisition time with only 30 picoseconds of aperture uncertainty, linearity is 0.05% of full scale and hold-mode feedthrough is −66 dB for inputs from dc to 10 MHz. The SHM-UH3 utilizes all hermetically sealed semiconductors in its design.

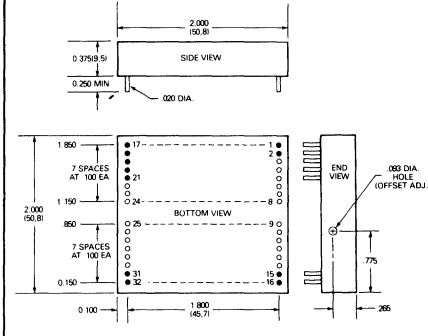
The SHM-UH is the lower cost version of the series. An acquisition time of 50 nanoseconds, aperture uncertainty of less than 200 picoseconds, and linearity of 0.25% make this model well suited to use with ultra-high speed A/D converters with up to 8 bits resolution.

Both models have sample-mode bandwidths of 45 MHz, output slew rates of 500V/microseconds and output current drive capabilities of ±30 mA. Each has an output offset adjustment accessible from the side of the module.

These sample-holds are encapsulated in 2 x 2 x 0.375 inch (51 x 51 x 5 mm) cases with dual-in-line pinning compatibility. Power requirements are ±15V dc and +5V dc. Standard versions operate over a temperature range of 0 to +70°C with extended temperature range versions also available.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL IN
2	SAMPLE CONTROL GND
15	ANALOG OUTPUT GND
16	ANALOG OUTPUT
17	+5V POWER
18	5V POWER GND
19	+15V POWER
20	−15V POWER
21	15V POWER GND
31	ANALOG INPUT GND
32	ANALOG INPUT

	SHM-UH	SHM-UH3
ABSOLUTE MAXIMUM RATINGS[1]		
Analog Input Voltage	±15V	±5.5V
Sample Control Input Voltage	+5.5V	+5.5V
Sample Pulse Width[7]	70 nsec.	100 nsec.
Analog Supply Voltage	±18V	±18V
Digital Supply Voltage	+5.5V	+5.5V

FUNCTIONAL SPECIFICATIONS,

Typical at 25°C and ±15V dc and +5V dc Supplies, unless otherwise noted.

INPUTS		
Input Voltage Range	±5V	±5V
Input Impedance	100 Meg	100k
Input Bias Current	50 pA[2]	±20 μA
Sample Control Pulse	+5V at 130 mA	+3.5 at 60 mA
Sample Control Pulse Width	40 ±10 nsec.	35 ±10 nsec.
Sample Control Input Impedance	50Ω	50Ω
Sample Pulse Rise or Fall Time	3 nsec., max.	3 nsec., max.
OUTPUTS		
Output Voltage Range, min.	±5V	±5V
Output Current, max.	±30 mA	±30 mA
Output Impedance, dc	3Ω	3Ω
Output Load[3]	500Ω	500Ω
Maximum Capacitive Load	100 pF	100 pF
PERFORMANCE		
Gain	+0.92 to +0.95	+0.95 to +0.98
Linearity Error, % of Full Scale	±0.25%, max.[9]	±0.05%, max.
Output Offset Voltage, Hold Mode	Adj. to Zero	Adj. to Zero
Output Offset Voltage Drift	±50 μV/°C	±50 μV/°C
Hold Mode Droop	50 μV/μsec.	50 μV/μsec.
Hold Mode Feedthrough[4]	−50 dB at 10 MHz	−66 dB, dc to 10 MHz
Analog Supply Rejection	6 mV/V	25 mV/V
DYNAMIC RESPONSE		
Acquisition Time	50 nsec.[5]	30 nsec.
Acquisition to Output Time[11]	70 nsec.	50 nsec.
Hold Mode Settling Time	20 nsec.	20 nsec.
Bandwidth, Sample Mode	45 MHz	45 MHz
Output Slew Rate	500V/μsec.	500V/μsec.
Aperture Delay Time	12 nsec.[6]	12 nsec.[8]
Aperture Uncertainty Time	200 psec.	30 psec.
Sampling Rate, max.	10 MHz[10]	10 MHz[10]
POWER REQUIREMENTS		
Analog Power Supply	±15V dc ±0.2V dc at 100 mA	
Digital Power Supply	+5V dc ±0.25V dc at 100 mA	

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	−55°C to +85°C
Relative Humidity	Up to 100% Non-condensing
Case Size	2 x 2 x 0.375 inches (50,8 x 50,8 x 9,5 mm)
Case Material	Black Diallyl Phthalate, per MIL-M-14
Pins	0.020″ Dia, Gold Plated 0.25″ Long, min.
Weight	3 ounces (85 grams)

FOOTNOTES:

1. Maximum ratings represent the limits of device operation without damage. The devices should not be operated at these limits.
2. 150 pA maximum at 25°C. Doubles every 10°C (SHM-UH Only).
3. For full scale signal outputs. For small signal outputs (±1V), output load resistance may be decreased to 100Ω.
4. See Feedthrough Attenuation Graph.
5. Model SHM-UH requires three sampling pulses to acquire a full scale signal change.
6. For the SHM-UH this will vary by ±2 nanoseconds maximum with temperature.
7. See Technical Note 10.
8. This may vary between units by 3 nanoseconds.
9. For input signal changes of ±1.25V maximum, larger input signal changes require additional sample pulses and settling time. See Technical Note 9.
10. 30 nanoseconds sampling pulses with 70 nanoseconds between pulses.
11. See Technical Note 4.

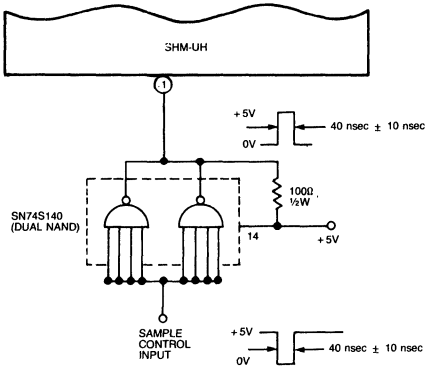
TECHNICAL NOTES

1. These devices are true sample-holds, rather than track and holds, in that they take an "instantaneous" sample of the input signal rather than continuously track it and hold on command. The extremely high speed available with this series allows a close approximation to sampling period of the ideal zero-order hold. Design considerations necessary to attain this level of performance place a limit on long-term holding ability. A/D converters used with these sample-holds should be selected for compatible speed and accuracy.
2. Aperture uncertainty time is a measurement of the time uncertainty or jitter of the actual point in time of the switch change to the off state. It is an indication of the repeatability of the switch characteristics. This time should not be confused with the aperture delay time which is a fixed delay and can be compensated for.
3. Acquisition time is the time required, after the sampling switch is closed, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band around the final value.
4. Acquisition to output time is defined as the period from the receipt of the sample command until the output of the sample-hold has settled to within a specified error band of its final value. This is the operating period of the sample-hold, including all internal delays and settling time, and consequently defines the total time required for a single sample-hold operation.
5. Digital and analog grounds are not connected internally. When using these sample-holds with A/D converters, good design practice dictates the connection of analog and digital grounds from both devices at one point, preferably at the A/D converter to avoid ground loops. Use of a ground plane is recommended for best performance.

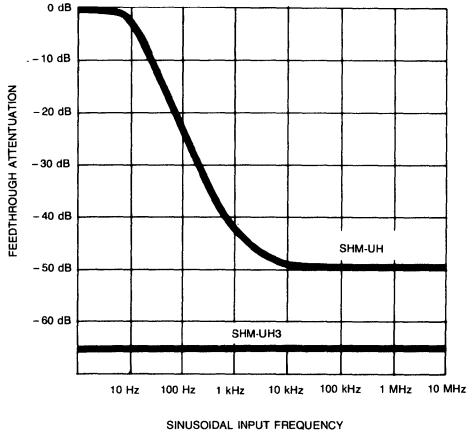
6. For Model SHM-UH only, hold mode droop is from the held value of the analog input signal toward the signal level at the input. The droop experienced is also dependent on input signal characteristics and is related to the feedthrough attenuation characteristics. The combination of these factors may cause the observed hold mode voltage droop to be significantly less than 50 μV/microseconds for some applications, e.g., droop is zero for a constant input signal. In the case of Model SHM-UH3, droop is independent of feedthrough.
7. For both the SHM-UH and the SHM-UH3 input sources should be purely resistive.
8. Input overvoltage protection may be added to the SHM-UH3 by connecting diodes from the analog input and the analog input ground to the +5V and −5V supplies.
9. To acquire full-scale input signal changes, the SHM-UH requires three sampling pulses with a 100 nanoseconds settling time allowed between each to acquire full-scale input changes to rated linearity.
10. Sample pulse widths greater than those specified under MAXIMUM RATINGS will give unsatisfactory performance due to drive transformer saturation. For Model SHM-UH3, excessive pulse widths will result in the sample-hold returning to the hold mode before the sample control input is taken low. Model SHM-UH may be damaged by exceeding sample pulse width limits.

APPLICATION

SAMPLE CONTROL INTERFACE SHM-UH

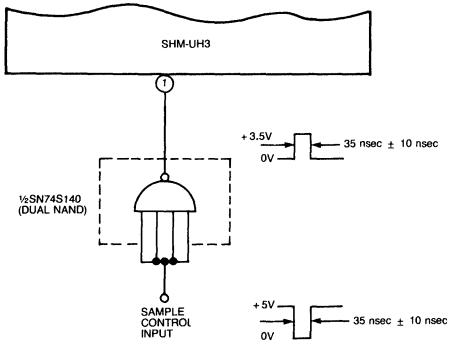


HOLD MODE FEEDTHROUGH ATTENUATION



HOLD-MODE FEEDTHROUGH IS A PHENOMENA THAT OCCURS AFTER THE SWITCH HAS BEEN OPENED AND THE SIGNAL IS BEING HELD. A SMALL PART OF THE SIGNAL ON THE INPUT WILL BE COUPLED TO THE OUTPUT.

SAMPLE CONTROL INTERFACE SHM-UH3



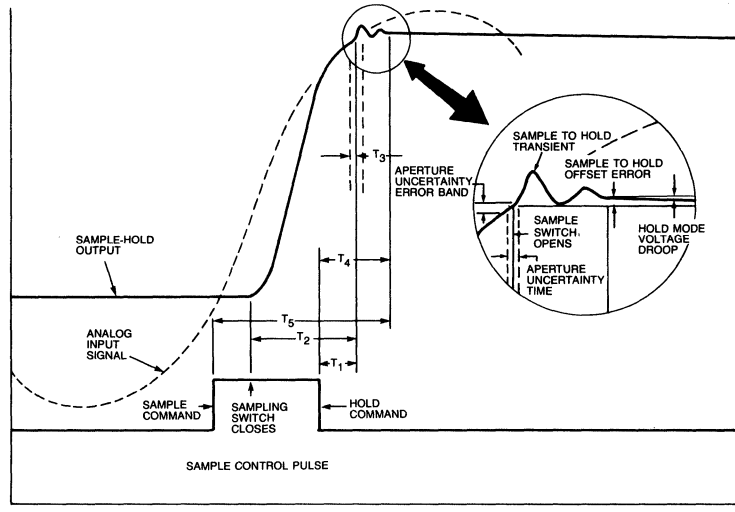
ADJUSTMENT PROCEDURE

1. Connect the Analog Input (pin 32) to the Analog Input Ground (pin 31).
2. Connect a precision pulse generator with negative going output pulses via a terminated coaxial cable to the Sample Control Input (pin 1) and the Sample Control Ground (pin 2). Use the sample control interface shown in the applicable diagram.
3. Pulse Repetition Rate 50 kHz
   Pulse Width 40 nsec
   Pulse Amplitude +5V

   Note: Sample Control Input Impedance is 50 Ohms.
4. Connect a precision digital voltmeter to the Analog Output (pin 16) and the Analog Output Ground (pin 15).
5. Adjust the Offset Adjust Potentiometer (accessible through side of case) until the digital voltmeter reads 0.0000V.

APPLICATION

SAMPLE-HOLD DEFINITIONS



APERTURE DELAY TIME, T_1
The period between the receipt of the hold command and opening of the sampling switch. Due to sampling switch characteristics, the measurement of this period contains a small amount of uncertainty, i.e., the actual point in time of the opening of the sampling switch will vary by a small amount with each operation. This variance falls within a narrow time range which is specified as the aperture uncertainty time (see definition below).

ACQUISITION TIME, T_2
The time required, after the closing of the sampling switch, for the hold capacitor to charge to a full scale voltage change and then remain within a specified error band around the final value.

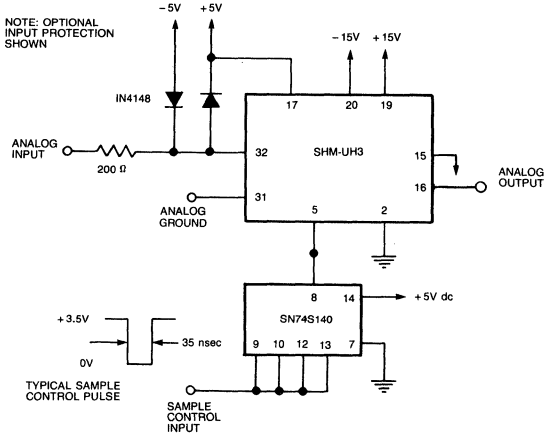
APERTURE UNCERTAINTY TIME, T_3
The time variation, or jitter, in the opening of the sample switch.

HOLD MODE SETTLING TIME, T_4
The time from the hold command transition until the output has settled within a specified error band around the final value.

ACQUISITION TO OUTPUT TIME, T_5
The time from the receipt of the sample command until the output of the sample-hold has settled within a specified error band around the final value.

APERTURE UNCERTAINTY ERROR
An amplitude uncertainty in the held value due to the change in the analog input signal during the aperture uncertainty time. This error is the product of the rate of change of the input signal and the aperture uncertainty time. Therefore, small values of aperture uncertainty time yield small values of aperture uncertainty error.

SHM-UH3



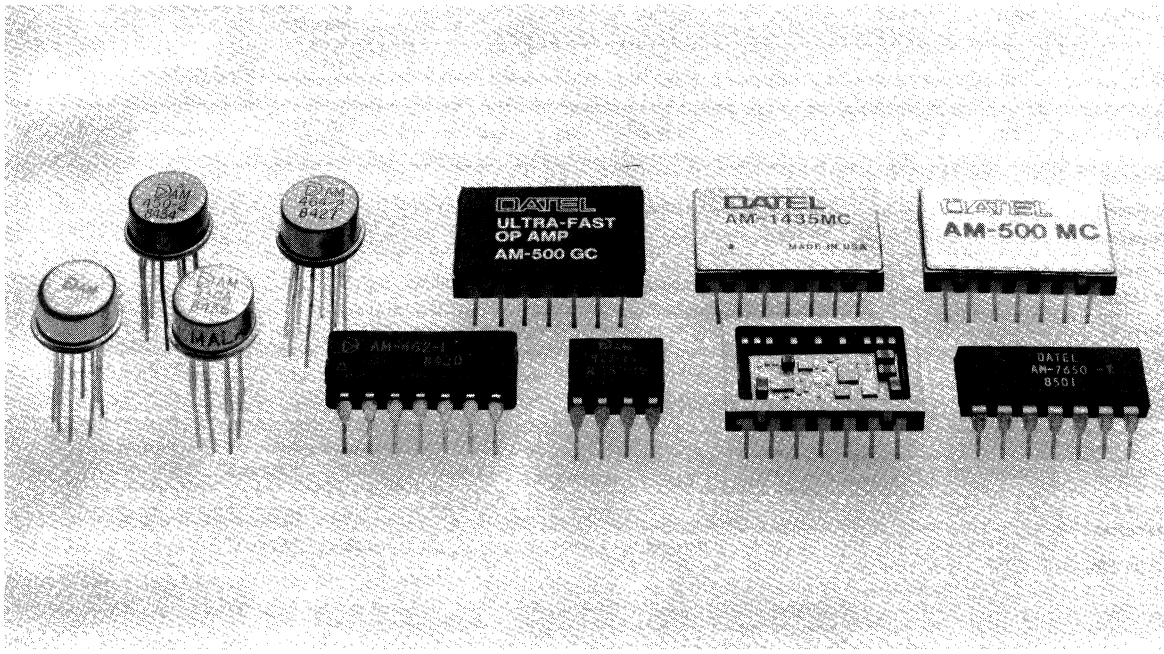
ORDERING INFORMATION

MODEL NO.	DESCRIPTION
SHM-UH	50 nanoseconds, 0.25%
SHM-UH3	30 nanoseconds, 0.05%

ACCESSORIES

Part Number	Description
DILS-2	Mating Socket, 2 required/Module

AMPLIFIERS


DATEL
ULTRA-FAST
OP AMP
AM-500 GC
DATEL
AM-1435MC
MADE IN USA
DATEL
AM-500 MC
DATEL
AM-7650
8501

OPERATIONAL AMPLIFIERS

MODEL	DC OPEN LOOP GAIN (V/V)	SETTLING TIME 10V to 0.1%	SLEW RATE (V/μSec)	GAIN BANDWIDTH	OFFSET DRIFT (μV/°C)	OUTPUT	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
AM-427-1A	6.3×10^5	—	1.7	5 MHz	1.8	±11V/±18 mA	8-pin DIP Monolithic	0 to +70	4-11
AM-427-1B	10^6				0.6				
AM-427-2A	6.3×10^5	—	1.7	5 MHz	1.8	±11V/±18 mA	8-pin TO-99 Monolithic	0 to +70	4-11
AM-427-2B	10^6				0.6				
AM-430A	100K	11 μs	0.5	2.5 MHz	1.3	±10V/±25 mA	8-pin TO-99 Monolithic	0 to +70	4-15
AM-430B					0.6				
AM-450-2	25K	330 ns	30	12 MHz	20	±10V/±10 mA	8-pin TO-99 Monolithic	0 to +70	4-19
AM-450-2M								-55 to +125	
AM-452-2	15K	200 ns	120	20 MHz	30	±10V/±10 mA	8-pin TO-99 Monolithic	0 to +70	4-17
AM-452-2M								-55 to +125	
AM-453-2C	100K	—	13	10 MHz	30	±12V/±20 mA	8-pin TO-99 Monolithic	0 to +70	4-17
AM-453-2M								-55 to +125	
AM-460-2C	150K	1.5 μs	7	12 MHz	10	±10V/±10 mA	8-pin TO-99 Monolithic	0 to +70	4-19
AM-462-2	150K	1.0 μs	35	100 MHz	15	±10v/±10 mA	8-pin TO-99 Monolithic	0 to +70	4-19
AM-464-2	100K	—	5	4 MHz	15	±35V/±10 mA	8-pin TO-99 Monolithic	0 to +70	4-23
AM-500GC	10^6	200 ns to 0.01%	1000	100 MHz	5	±10V/±50 mA	14-pin DIP Hybrid	0 to +70	4-25
AM-500MC					7			0 to +70	
AM-500MM					10			-55 to +125	
AM-1435MC	10^5	70 ns to 0.01%	300	1000 MHz	5	±7V/±14 mA	14-pin DIP Hybrid	0 to +70	4-3
AM-1435MM								-55 to +125	
AM-7650-1	10^6	—	2.5	2 MHz	0.05	±4.7V	14-pin DIP 8-pin TO-99	0 to +70	4-35
AM-7650-2									

INSTRUMENTATION AMPLIFIERS

MODEL	DESCRIPTION	GAIN RANGE	GAIN NON-LINEARITY	SETTLING TIME	INPUT IMPEDANCE	OUTPUT	COMMON MODE REJECTION	PACKAGE	OPERATING TEMPERATURE RANGE (°C)	PAGE
AM-542MC	High Performance Hybrid Digitally Selectable Gain Ranges	1 to 1024	0.005%	150 μsec.	$10^9\Omega$	±10.5V at ± 5 mA	86 dB	24-pin DIP	0 to +70	4-27
AM-542MM									-55 to +125	
AM-543MC		1 to 128	0.01%	6 μsec.	$10^{12}\Omega$	±11V at ±1 mA	86 dB	24-pin DIP	0 to +70	4-27
AM-551MC	Low Cost, High Performance Hybrid	1 to 1000	0.01%	2 μsec.	$10^{12}\Omega$	±11V at ±5 mA	100 dB	16-pin DIP	0 to +70	4-31
AM-551MM									-55 to +125	

SIGNAL CONDITIONING AND ISOLATION AMPLIFIERS

MODEL	DESCRIPTION	ISOLATION VOLTAGE	GAIN RANGE	GAIN NON-LINEARITY	INPUT RESIST-ANCE	COMMON MODE REJECTION	INPUT OFFSET VOLTAGE	OUTPUT	OPERATING TEMPERATURE RANGE (°C)	PAGE
AM-227	Low-cost Precision Isolation Amplifier	±1000V dc	10 to 1000	±0.005%	100 MΩ	176 dB	±150 μV	±10V at ±5 mA	0 to +70	4-7
SCM-100A	Low-Cost, Four Channel Isolation Amplifier	±1000V dc	1 to 1000	±0.03%	100 MΩ	156 dB	±20 μV	±5V at ±5 mA	0 to +70	4-41
SCM-100B				±0.02%		145 dB	±50 μV			
SCM-101										
SCM-103	4-chan Strain gage cond.	None	166.6 V/V or 50 V/V	±0.01%	100 MΩ	94 dB	±150 μV	±5V at ±5 mA	0 to +70	4-45

AM-1435
Ultra-High Speed Wideband Operational Amplifier

FEATURES

- **70 Nanoseconds settling to 0.01%**
- **1 GHz Gain bandwidth product**
- **100 dB Open loop gain**
- **80 dB Minimum CMRR**
- **−55°C to +125°C Operation**

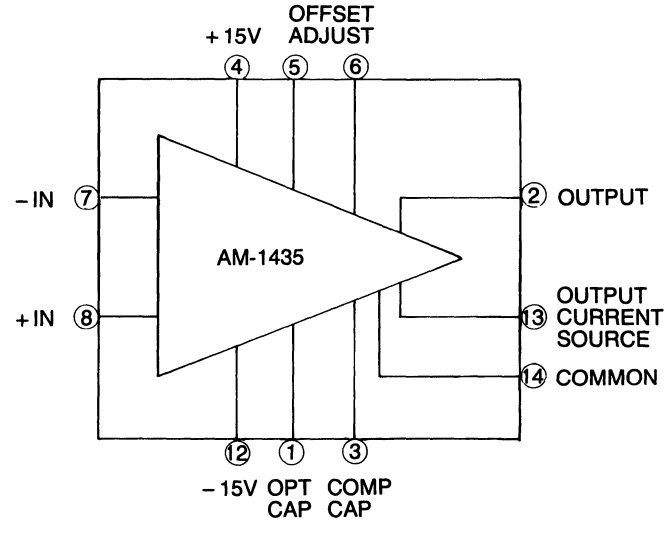
GENERAL DESCRIPTION

DATEL's AM-1435 is an ultrafast settling, wide-band operational amplifier. Utilizing precision thin-film hybrid construction and differential input operational amplifier design techniques, the AM-1435 achieves a settling time of only 70 nanoseconds for a 10 volt step to 0.01% accuracy. High speed performance is optimized with high open-loop gain, flat frequency response beyond 10 kHz and a roll-off of 6 dB/octave to beyond 100 MHz. Typically, gain bandwidth product is 1 GHz and slew rate is 300 V/microsecond.

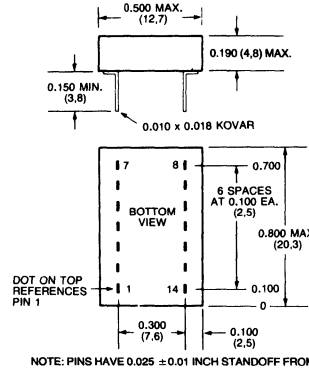
AM-1435 dc characteristics include a dc open loop gain of 100 dB, 1 MΩ input impedance, and an initial input offset voltage of only ±2 mV. Input offset voltage drift is typically ±5 μV/°C. Also featured is a minimum common mode rejection ratio of 80 dB and full power frequency of 8 MHz.

The AM-1435 is designed specifically for applications requiring high accuracy in the amplification of complex wide-band waveforms. Such applications would include radar and sonar signal processing, video instrumentation and ultra-fast, A/D, D/A converters and sample-hold amplifiers.

Power supply requirement is ±15V dc at 30 mA maximum quiescent current. Models are specified for operation over the commercial 0°C to +70°C, and military -55°C to +125°C operating temperature ranges. The device package is a 14-pin, hermetically sealed, ceramic case.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 ±0.01 INCH STANDOFF FROM CASE

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OPTIONAL CAP
2	OUTPUT
3	COMPENSATION CAP.
4	+15V SUPPLY (+Vs)
5	OFFSET ADJUST
6	OFFSET ADJUST
7	− INPUT
8	+ INPUT
9	N.C.
10	N.C.
11	N.C.
12	−15V SUPPLY (−Vs)
13	OUTPUT CURRENT SOURCE
14	COMMON

4

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS	MINIMUM	TYPICAL	MAXIMUM
Differential between inputs	—	—	±4V
Common Mode Voltage Range	±7V	±8.5V	—
Common Mode Rejection Ratio;			
dc	80 dB	—	—
1 MHz	70 dB	—	—
Input Impedance;			
common mode	1 MΩ ‖ 2 pF	—	—
differential mode	2.5 kΩ ‖ 2 pF	—	—
Input Offset Voltage[2]	—	±2 mV	±5 mV
Input Bias Current	—	10 μA	20 μA
Input Offset Current	—	0.3 μA	—
OUTPUT CHARACTERISTICS			
Output Voltage[3]	±5V	±7V	—
Output Current[3]	±10 mA	±14 mA	—
Stable Capacitive Load[4]	—	1000 pF	—
PERFORMANCE			
dc Open Loop Gain[3]	90 dB	100 dB	—
Input Offset Voltage Drift	—	±5 μV/°C	±25 μV/°C
Input Bias Current Drift	—	50 nA/°C	100 nA/°C
Input Offset Current Drift	—	2 nA/°C	—
Input Voltage Noise,			
0.01 Hz to 10 Hz	—	15 μV P-P	—
100 Hz to 10 kHz	—	1.6 μV RMS	—
10 Hz to 1 MHz	—	5.2 μV RMS	—
Input Current Noise[5],			
0.01 Hz to 10 Hz	—	2.5 nA P-P	—
100 Hz to 10 kHz	—	2.5 nA RMS	—
10 Hz to 1 MHz	—	3.5 nA RMS	—
Power Supply Rejection Ratio	—	0.15 mV/V ΔV_S	—
DYNAMIC CHARACTERISTICS			
Gain Bandwidth Product	700 MHz	1000 MHz	—
Unity Gain Bandwidth	—	150 MHz	—
Full Power Frequency[6]	8 MHz	10 MHz	—
Settling Time, 10V to 0.025%[7]	—	60 nsec.	75 nsec.
10V to 0.01%	—	70 nsec.[8]	—
5V to 1.0%	—	25 nsec.	—
5V to 0.1%	—	40 nsec.	60 nsec.
1V to 1.0%	—	10 nsec.	—
1V to 0.1%	—	20 nsec.	—
Slew Rate	250 V/μsec.[6]	300 V/μsec.	
Overshoot	—	—	1%
Propagation Delay	—	5 nsec.	—
Rise Time, 10V Step	—	40 nsec.	—
Overload Recovery Time	—	50 nsec.	—
POWER REQUIREMENTS			
Rated Supply Voltage	±12V	±15V	±16V
Quiescent Current[8]	—	—	±30 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range:	
AM-1435MC	0°C to +70°C
AM-1435MM[9]	−55°C to +125°C
Storage Temp. Range	−65°C to +150°C
Package	14-pin, hermetically sealed ceramic DIP

FOOTNOTES:

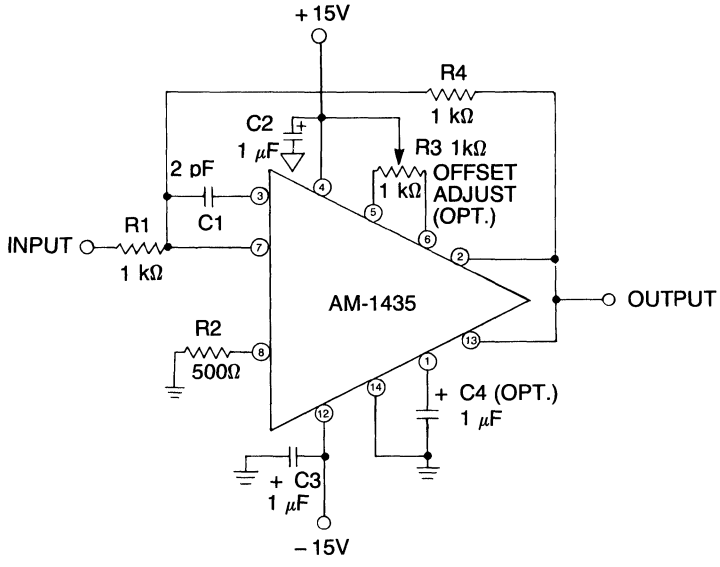
1. Specified for dc linear operation. Common mode voltage range prior to fault condition is ±10V dc maximum.
2. Adjustable to zero.
3. R_L = 500Ω.
4. C_1 = 3 pF.
5. Referred to input.
6. C_1 = 0.5 pF.
7. C_f = 1 pF.
8. $\pm V_S$ = ±15V dc.
9. With 18°C/watt heat sink.

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for rated performance. The extensive use of a ground plane for all common connections is recommended. Lead length should be kept to a minimum with point-to-point connections wired directly to the amplifier pins. 1 μF tantalum bypass capacitors should be used at the $+V_S$ and $-V_S$ pins.
2. Operation of the AM-1435MM over the +85°C to +125°C temperature range requires additional thermal dissipation to achieve rated performance. Use of an 18°C/W heat sink is recommended.
3. No input protection is provided so as to maximize frequency response. As a result, several precautions must be observed: Do not apply positive supply voltage before the negative supply. Do not apply power to either input prior to power-up. If frequency response is not critical, installation of an external input protection circuit is recommended.
4. A 1 μF bypass capacitor connected from Pin 1 to common (Pin 14) may be required to inhibit output oscillation when driving capacitive loads.
5. To ensure stable operation when the noise gain is less than 10, a 2 pF compensation capacitor must be connected between pins 3 and 7. The value of the compensation capacitor may be application sensitive.
6. The AM-1435 is a prime choice as a current to voltage converter due to its excellent E_{OS} and I_{OS} temperature coefficient ratings. Input bias currents are easily compensated by adding a resistor from pin 8 to ground, which is equal to the parallel combination of the feedback resistor and input impedance.

TYPICAL CONNECTION AND PERFORMANCE

TYPICAL CONNECTION DIAGRAM



TYPICAL CONNECTION AND COMPENSATION

The typical connection diagram (above) shows the AM-1435 in a unity gain inverting configuration. Operational in any conventional operational-amplifier circuitry, the AM-1435 as a non-inverting amplifier requires a noise gain of at least two (NOISE GAIN = 1 + R_4/R_1).

The 2 pF compensation capacitor at C_1 is required for stable operation when the noise gain is less than 10. Compensation for bias current is provided by R_2 and its value determined by the formula

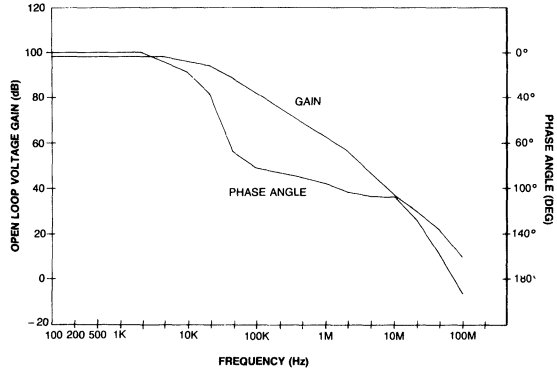
$$R_2 = \frac{(R_1) \times (R_4)}{R_1 + R_4}$$

The offset adjust potentiometer at R_3 and the compensation capacitor at C_4 are optional. Note however, C_4 should be implemented when driving capacitive loads to prevent oscillation of the output stage.

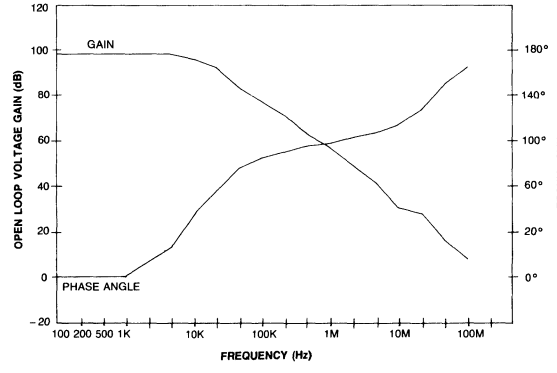
Operation of the AM-1435 at low impedances requires careful attention to include the feedback resistor as a part of the total output load.

The use of good, high frequency circuit board layout techniques is required for rated performance. The amplifier should be mounted on a ground plane using minimum lead length and point to point wiring directly to the amplifier pins.

GAIN AND PHASE VS. FREQUENCY (UNCOMPENSATED)

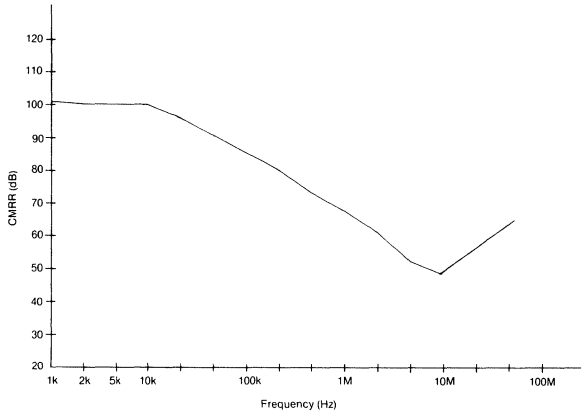


GAIN AND PHASE VS. FREQUENCY (COMPENSATED 2 pF)

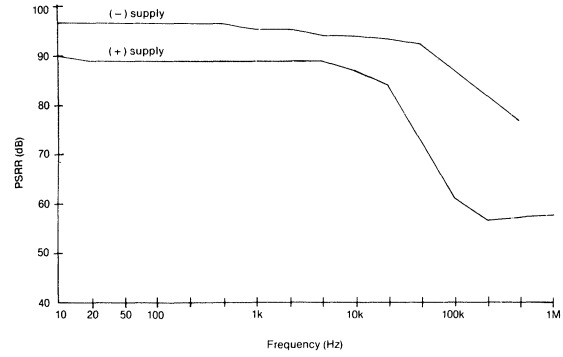


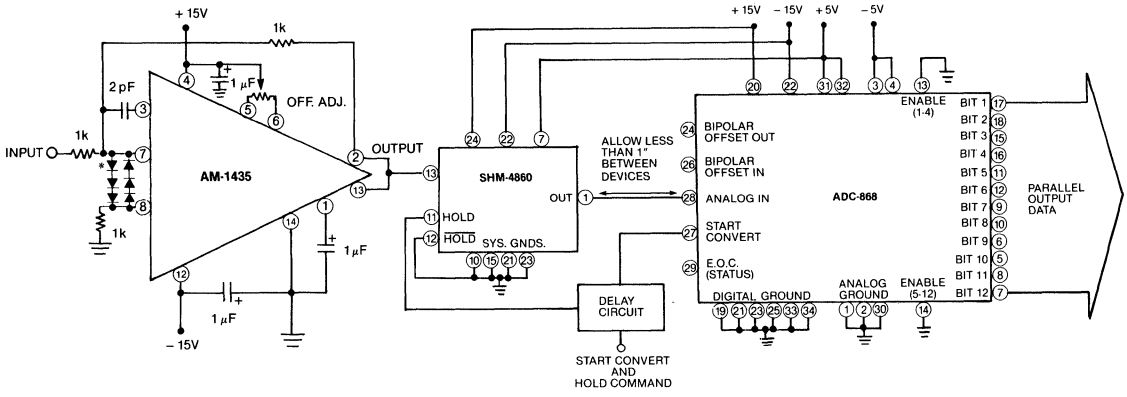
PERFORMANCE AND APPLICATION

CMRR VS FREQUENCY



PSRR VS FREQUENCY





The AM-1435, an ultra high speed, wideband operational amplifier is shown here with DATEL's SHM-4860, an ultra fast 0.01% sample-hold amplifier and ADC-868, a 500 nsec. 12-bit A/D converter. This configuration provides high speed analog to digital conversion at throughput rates exceeding 1 MHz.

*Input protection circuit utilizing six HP2811 Schottky diodes. Series configuration reduces effect of diode capacitance on circuit response.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
AM-1435MC	0°C to + 70°C
AM-1435MM	−55°C to +125°C

ACCESSORIES

Part Number	Description
TP1K	Trimming Potentiometer

For military devices compliant to MIL-STD-883, Contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

AM-227
Low Cost, Ultra-Stable Isolation Amplifier

FEATURES

- **1000V dc Isolation**
- **0.005% Nonlinearity**
- **166 dB Minimum, CMRR**
- **0.2 Microvolt/°C offset drift**
- **10 to 1000 Gain range**

GENERAL DESCRIPTION

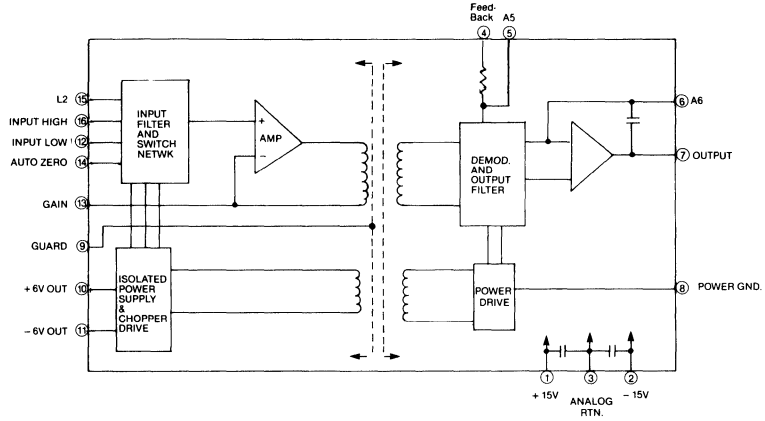
DATEL's AM-227 is a low-cost, precision modular isolation amplifier designed specifically for applications involving the amplification of low-level, low frequency signals in the presence of high common mode interference. The ultra-low drift, high accuracy, and high CMRR make it possible to accurately amplify microvolt-level signals with a user selectable gain range of 10 to 1000. Gain nonlinearity is specified as low as ±0.005% FSR maximum with gain selection accomplished through the addition of one external resistor.

The AM-227 offers excellent dc input characteristics including an unadjusted offset voltage of ±150 microvolts, common mode rejection ratio of 166 dB minimum and common mode isolation voltage of 1000V dc. Offset voltage drift is 0.5 microvolt/°C maximum and long term stability is typically as low as 2 microvolts/year.

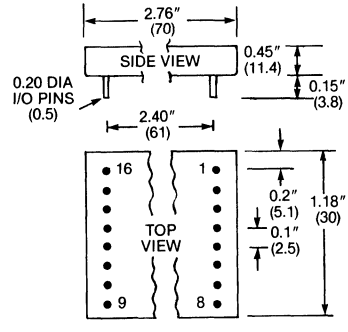
The AM-227 includes a chopper-stabilized input amplifier, power oscillator, demodulator, and 3-pole 60 dB/decade filtering. An output buffer amplifier provides ±10V dc at ±5 mA. The isolated ±6V power outputs can be used in a simple open input indication network.

Its combination of high performance, low cost and small size make the AM-227 an excellent choice for applications involving thermocouple temperature measurements, remote data acquisition systems, strain gauge measurements, and precision telemetry systems.

Power requirement is ±15V dc. The AM-227 is packaged in a compact 2.8 x 1.2 x 0.45 inch, shielded steel case. Operation is specified over the industrial 0°C to +70°C temperature range.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V POWER IN	9	GUARD
2	−15V POWER IN	10	+6V OUT
3	ANALOG RTN	11	−6V OUT
4	FEEDBACK	12	INPUT LO
5	A5	13	GAIN
6	A6	14	AUT. ZER. RTN.
7	OUTPUT	15	L2
8	POWER GND	16	INPUT HIGH

FUNCTIONAL SPECIFICATIONS, AM-227

Typical at +25°C, ±15V dc supplies unless otherwise noted.

INPUT CHARACTERISTICS	
Linear Differential Input Voltage Range[1]	±10 mV to ±1V full-scale
Offset Voltage, RTI[2], G = 100	±600 μV
G = 1000	±150 μV
Input Bias Current, max.	2 nA (0.5 nA typ.)
Input Resistance, Differential Mode	100 MΩ
Input Impedance, Common Mode	10^{10} ‖ for 80 pF
Differential Mode	100 MΩ shunted by 22 kΩ in Series with 1.5 μF
Overload Input Impedance	22 kΩ
Common Mode Rejection Ratio, min.[3]	166 dB (176 dB typ.)
Common Mode Isolation Voltage, max.	1000V dc, 750V RMS
OUTPUT CHARACTERISTICS	
Output Voltage Range	±10V
Output Impedance, DC	0.1Ω
Output Load, max.	±5 mA and 500 pF
Ouput Short-Circuit Protection	Continuous to Ground
Output Chopper Noise[4]	1 mV peak-to-peak at approximately 10 kHz
PERFORMANCE	
Gain Range[5]	10 to 1000
Gain Equation[6]	$G = 10^4/R_G$
Gain Nonlinearity, max., G = 10	±0.05% FSR
G = 50–500	±0.005% FSR
G = 1000	±0.01% FSR
Gain Tempco, max., G = 10–500	±20 ppm FSR/°C(±10 ppm FSR/°C typ.)
G = 1000	±30 ppm FSR/°C(±20 ppm FSR/°C typ.)
Input Offset Temp. Drift, RTI, max.	±0.5 μV/°C(0.2 μV/°C typ.)
Input Bias Current Temp. Drift	50 pA/°C
Warm-Up Drift[7], RTI	<2 μV
Long Term Drift, RTI	1 μV/month, non-cumulative, 2 μV/year
Small Signal Bandwidth[8]	5 Hz
Power Supply Sensitivity	±2 μV/% change in V_S
ISOLATED POWER SUPPLY OUTPUT	
Voltage, with respect to Input Low	±6V dc nominal
Current, Full Load	±3 mA
Regulation, No Load to Full Load	6%
Ripple	20 mV peak-to-peak at 10 kHz
INPUT POWER REQUIREMENTS	
Positive Supply, No Load	+15V ±3% at +5 mA
Negative Supply, No Load	−15V ±3% at −3 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range[9]	0°C to +70°C
Storage Temperature Range	−55°C to +85°C
Relative Humidity	0 to 85%, non-condensing to +40°C
Package Size	1.2 x 2.8 x 0.5 in (30 x 70 x 12 mm)

FOOTNOTES:

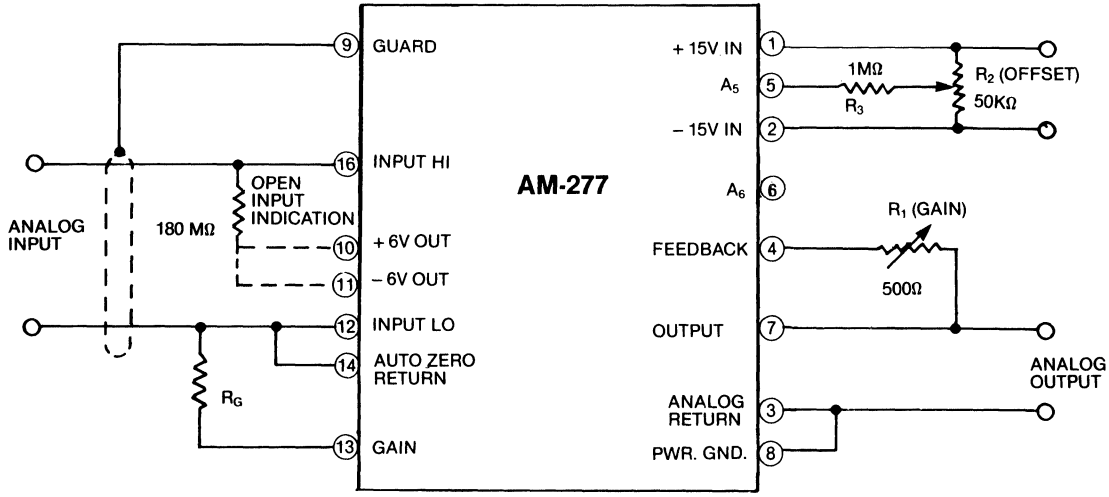
1. Absolute maximum safe differential input voltage is: 120V RMS, continuous.
2. Untrimmed, referred to input (RTI). Adjustable to zero.
3. At dc and from 50 to 800 Hz. G = 50 to 1000 with a 1 kΩ source imbalance.
4. 1 MHz bandwidth.
5. Non-inverting. Optimized for gains of 50 to 500.
6. See Technical Note 1.
7. 5 minutes.
8. 6 dB down at 5 Hz. See Technical Note 2 for information on the AM-227's internal filters.
9. It is possible to operate the AM-227 over the −25°C to +85°C temperature range with some degradation of performance.

TECHNICAL NOTES

1. The AM-227 gain may be set to any value from 10 to 1000 by connecting an external resistor (R_G) between the gain pin (Pin 13) and the input low pin (Pin 12). The gain is equal to $G = 10^4/R_G$ and untrimmed will be within ±3% of the calculated value. An RN55E resistor is recommended for temperature stability.
2. The AM-227 contains both input and output filters. The input filter is a one-pole RC (3 dB cut-off at 5 Hz) and the output filter is a two-pole Butterworth (3 dB cut-off at 5 Hz). Overall filtering is three-pole, 60 dB/decade roll-off (−60 dB at 50 Hz).
3. For normal operation of the AM-227, connect the auto-zero pin (Pin 14) to the input low pin (Pin 12). A stable voltage source may be connected to the auto zero pin for applications requiring an input offset that exceeds the range of the offset adjust. Signals present on the input high pin (Pin 16) and auto zero pin (if used) are measured with respect to the input low pin. For optimum linearity, each signal must be within ±1V of input low.

CONNECTION AND CALIBRATION

TYPICAL CONNECTION DIAGRAM



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GAIN SELECTION

The AM-227 gain can be set to any value from 10 to 1000 by simply connecting an external resistor (R_G) between the gain pin (Pin 13) and the Input Lo pin (Pin 12) as shown in the typical connection diagram. The selected gain is equal to $10^4/R_G$.

Absolute gain, unadjusted, will be within ±3% of the calculated value. For temperature stability, an RN55E resistor is recommended.

OFFSET ADJUSTMENT

To externally zero the offset of the AM-227, connect the resistors R_2 (R_2 can be a 25 kΩ or 50 kΩ potentiometer) and R_3 as shown in the typical connection diagram. Metal film resistors with a TCR of ±100 ppm/°C or less should be used.

To adjust the offset, short the Input High (Pin 16), Input Low (Pin 12), and Auto Zero Return (Pin 14) pins to the Analog Return Pin (Pin 3). With the input momentarily connected to ground, set R_2 for zero volts at the output (Pin 7).

GAIN ADJUSTMENT

The gain of the AM-227 may be fine trimmed externally by connecting a 500Ω potentiometer (R_1) as shown in the typical connection diagram. A metal film resistor with a TCR of ±100 ppm/°C or less is recommended.

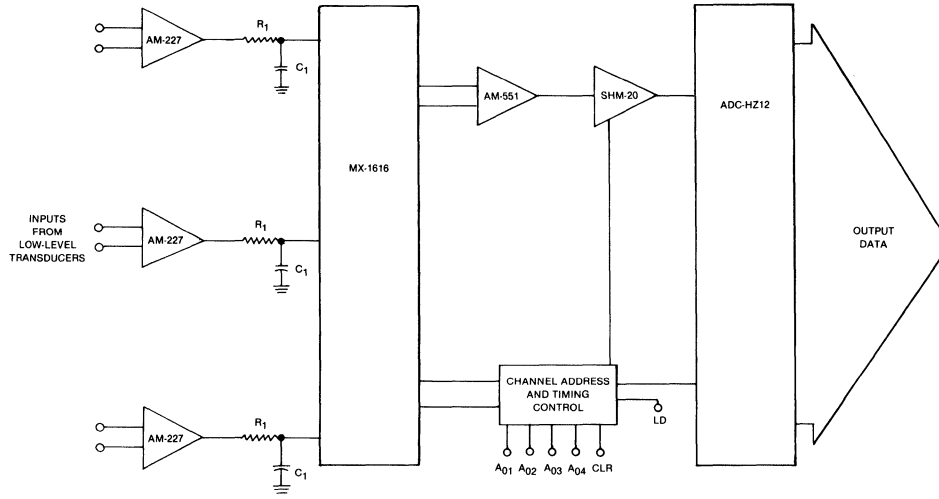
This adjustment is used to compensate for the tolerance of R_G and for unit-to-unit gain variability (3%) between multiple AM-227's. In applications where cost is of primary importance, a fixed resistor may be used.

OPEN INPUT INDICATION

The ±6V isolated power supply (Pins 10 & 11) outputs may be used for an open input indication network. This simple network consists of a resistor of approximately 180 MΩ connected between the input high pin (Pin 16) and either the +6V out pin (Pin 10) or the −6V out pin (Pin 11). This produces a bleeder current of approximately 20 nA through the input source circuitry. If the source is opened, this bleeder current will drive the AM-227 output into saturation.

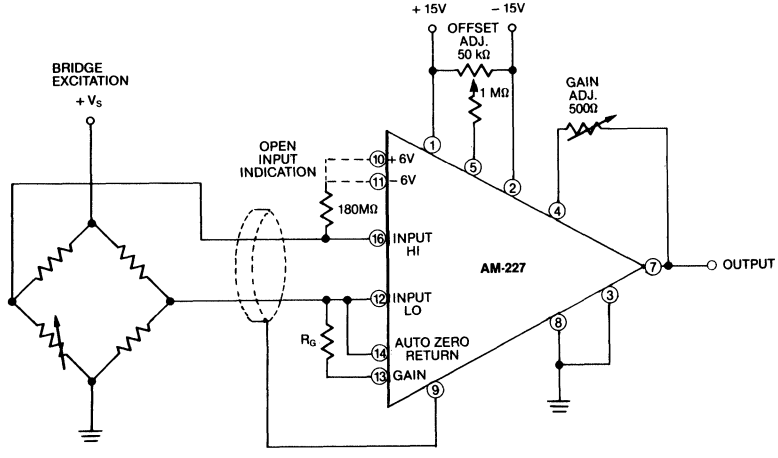
APPLICATION

MULTI-CHANNEL DATA ACQUISITION SYSTEM



For multichannel applications, the outputs of multiple AM-227 may be multiplexed to a common analog line. The single-pole filter (R_1, C_1) at the AM-227 output is used to eliminate errors due to dumped charge. Typical values for R_1 would be 50Ω–270Ω with a corresponding range for C_1 of 10,000 pF to 1,000 pF. This filter must be included for all high resolution (> 12-bits) applications of the AM-227.

BRIDGE TRANSDUCER INTERFACE



The AM-227 is designed to interface with low-level signal transducers such as thermocouples and strain gages. Because the transducers are often situated in noisy industrial environments and the output signal produced is extremely small, they are often connected in a bridge circuit. The AM-227 provides the user with the high input impedance, high common mode rejection, isolation (for ground loop elimination) and gain required for bridge interfacing.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
AM-227	0°C to +70°C

AM-427
Ultra Low-Noise Operational Amplifier

FEATURES

- **5.5 nV/$\sqrt{Hz}$ Maximum noise density**
- **0.08 Microvolt peak-to-peak low frequency noise**
- **25 Microvolt maximum input offset voltage**
- **$\pm$40 nA Maximum input offset current**
- **0.6 Microvolt/°C maximum offset voltage drift**

GENERAL DESCRIPTION

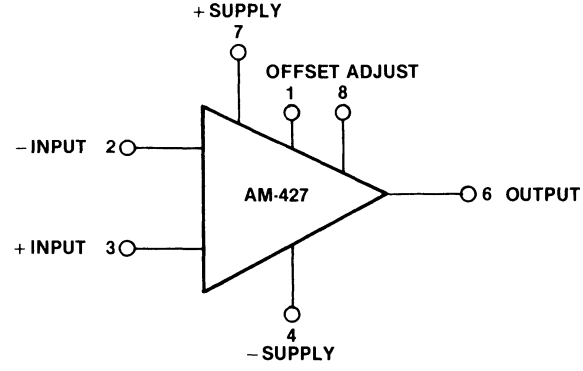
The AM-427 is a low cost monolithic instrumentation grade amplifier that combines ultra-low noise operation with exceptional dc performance. Input noise voltage density is typically 3.5 nV/$\sqrt{Hz}$ at 10 Hz while input noise current density is as low as 0.4 pA/$\sqrt{Hz}$.

Other significant features include a maximum input offset voltage of 25 microvolts, eliminating the need for external zeroing in most applications. Maximum input offset voltage drift is only 0.6 microvolt/°C. The AM-427 is internally compensated to provide a phase margin of 70° in the unity gain mode which eliminates peaking and ringing in low gain feedback applications. Output voltage is typically $\pm$13.5V at $\pm$6.75 mA load current with a short circuit protected output.

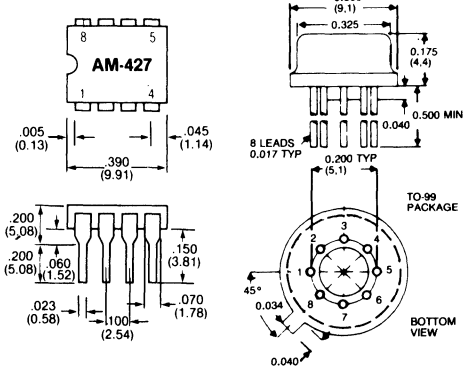
Dynamic characteristics include an 8 MHz gain bandwidth product and 2.8V/microseconds slew rate. Power supply rejection ratio and common mode rejection ratio are both in excess of 120 dB.

The AM-427 is an ideal choice for applications requiring high accuracy, low drift and low noise performance such as the amplification of low level transducer signals.

The AM-427 is available for operation over the industrial −25°C to +85°C temperature ranges. Models are packaged in either an 8-pin, hermetically sealed TO-99 case or an 8-pin ceramic DIP.



MECHANICAL DIMENSIONS INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET VOLTAGE ADJ.
2	− INPUT
3	+ INPUT
4	− SUPPLY VOLTAGE
5	N.C.
6	OUTPUT
7	+ SUPPLY VOLTAGE
8	OFFSET VOLTAGE ADJ.

ABSOLUTE MAXIMUM RATINGS	A MODELS	B MODELS
Power Supply Voltage		±22V
Input Voltage		±22V
Differential Input Voltage		±0.7V
Power Dissipation		658 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS		
Input Voltage Range, minimum		±11V
Input Resistance, diff. mode, minimum	0.8 MΩ	1.5 MΩ
Input Offset Voltage, maximum	100 μV	25 μV
Input Bias Current, maximum	±80 nA	±40 nA
Input Offset Current, maximum	75 nA	35 nA
OUTPUT CHARACTERISTICS		
Output Voltage, minimum[1]		±11V
Output Current, S.C. protected, minimum		±18 mA
Output Resistance, open loop[2]		70Ω
PERFORMANCE		
DC Open Loop Gain, minimum[3]	116 dB	120 dB
Input Offset Voltage Drift, maximum[4]	1.8 μV/°C	0.6 μV/°C
Long Term Stability	2 μV/mo	1 μV/mo
Input Bias Current Drift, maximum	±700 pA/°C	±200 pA/°C
Input Offset Current Drift maximum	600 pA/°C	150 pA/°C
Common Mode Rejection Ratio, minimum[5]	100 dB	114 dB
Input Noise Voltage, maximum, 0.1 to 10 Hz	0.25 μV peak-to-peak	0.18 μV peak-to-peak
Input Noise Voltage Density, maximum, 10 Hz	8 nV/√Hz	5.5 nV/√Hz
Input Noise Current Density, maximum, 1 kHz	0.6 pA/√Hz	0.6 pA/√Hz
Power Supply Rejection Ratio, minimum	94 dB	100 dB
Gain Bandwidth Product, minimum		5.0 MHz
Slew Rate, minimum		1.7V/microsecond
POWER REQUIREMENTS		
Voltage, Rated Performance		±15V dc
Quiescent Current, maximum	±5.7 mA	±4.7 mA
Power Dissipation	170 mW	140 mW
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range: AM-427A,B		−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Package, AM-427-1		8-Pin Ceramic DIP
AM-427-2		8-Pin Hermetically Sealed TO-99

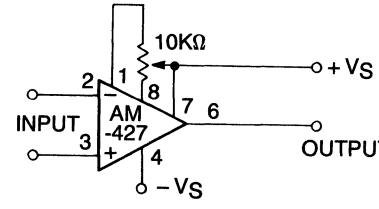
FOOTNOTES:

1. RL = 600Ω
2. Output Voltage = 0, output current = 0.
3. R_L = 2K ohm, V_{OUTPUT} = ±10V.
4. Guaranteed unnulled or when nulled with an 8 kΩ to 20 kΩ potentiometer.
5. Common mode voltage = ±11V.
6. V_S = ±4V to ±18V.

TECHNICAL NOTES

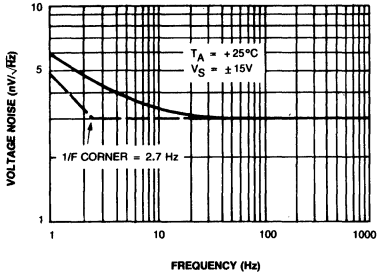
1. In order to maintain the specified drift performance, both input pins should be maintained at the same relative temperature. This is to avoid stray thermoelectric voltages which are generated by the dissimilar metals at the contacts of the input terminals.
2. To obtain the best possible linearity, circuit design should call for the minimum output current required by the application to assure high gain performance and excellent linearity, the output current range should be held to a maximum of ±10 mA.
3. The AM-427 provides stable operation with load, capacitance of up to 2000 pF and ±10 volt swings. Larger capacitances should be decoupled with a 50Ω decoupling resistor. To avoid additional phase shifting and phase margin, a 20 pF capacitor should be used in parallel with the feedback resistor when the value of the feedback resistor is greater than 2K ohm.
4. If adjustment of offset voltage is required, a 10 kΩ trimpot can be used without degrading the offset voltage drift specifications. A 1K ohm to 1 MΩ trimpot can be used, however, a 0.1 to 0.2 μV/°C degradation may occur. Trimming to a value other than zero will create a drift of (offset voltage/300) μV/°C. A 10K ohm offset trimpot will yield an adjustment range of ±4 mV. A smaller trimpot in conjunction with fixed resistors can be used to obtain a smaller adjustment range with higher sensitivity and resolution.

TYPICAL CONNECTION DIAGRAM

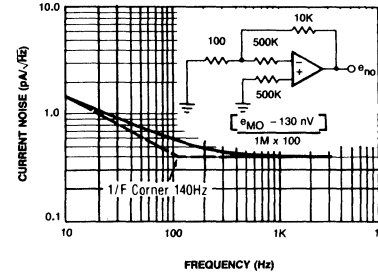


TYPICAL PERFORMANCE

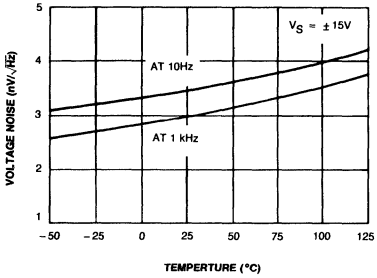
VOLTAGE NOISE VS. FREQUENCY



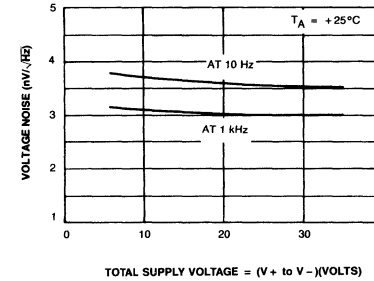
CURRENT NOISE VS. FREQUENCY



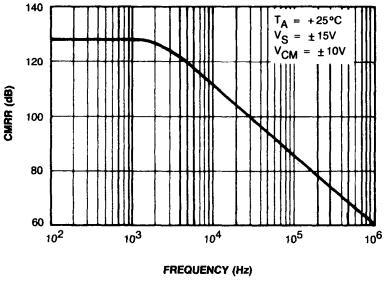
VOLTAGE NOISE VS. TEMPERATURE



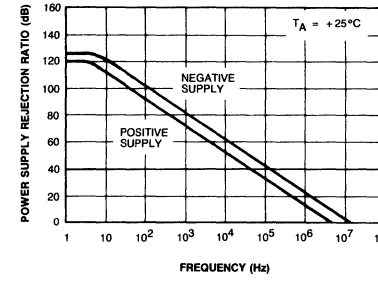
VOLTAGE NOISE VS. SUPPLY VOLTAGE



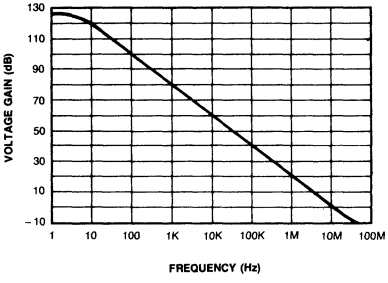
CMRR VS. FREQUENCY



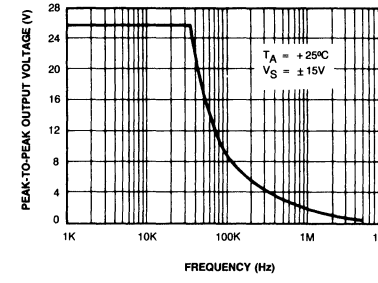
PSRR VS. FREQUENCY



OPEN LOOP GAIN VS. FREQUENCY

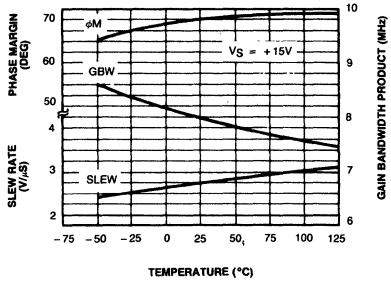


MAXIMUM UNDISTORTED OUTPUT VS. FREQUENCY

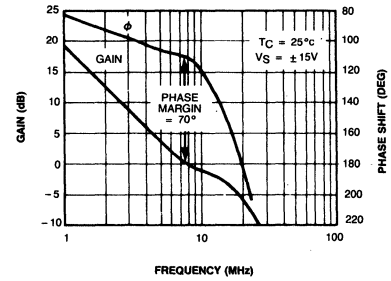


TYPICAL PERFORMANCE AND APPLICATIONS

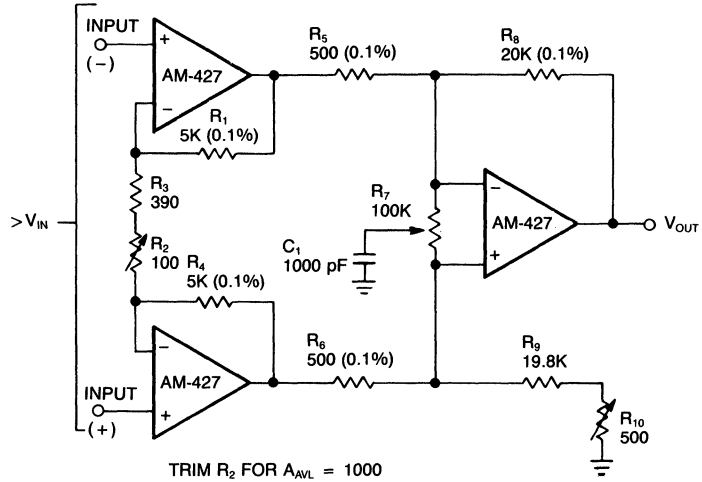
SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN VS. TEMPERATURE



GAIN, PHASE SHIFT VS. FREQUENCY



INSTRUMENTATION AMPLIFIER



TRIM R_2 FOR A_{AVL} = 1000
TRIM R_{10} FOR DC CMRR
TRIM R_7 FOR MINIMUM V_{OUT} AT V_{CM} = 20Vp-p, 10kHz

The AM-427 is particularly useful in instrumentation applications. In a single difference amplifier configuration, the AM-427 exhibits excellent common mode rejection and spot noise voltage so low, it is dominated by the resistor Johnson noise.

The three amplifier configuration shown avoids the low input impedance characteristics of difference amplifiers. Because of the additional amplifiers used, the spectral noise voltage will increase from a typical of 3 nV/√Hz to approximately 4.9 nV/√Hz. The overall gain of the circuit is set at 1000, and with balanced source resistors, a CMRR of 100 dB is achieved.

ORDERING INFORMATION

MODEL NO.	PACKAGE
AM-427-1A	8-Pin Ceramic DIP
AM-427-1B	8-Pin Ceramic DIP
AM-427-2A	8-Pin TO-99
AM-427-2B	8-Pin TO-99

AM-430
Ultra-Low Drift, Monolithic Operational Amplifier

FEATURES

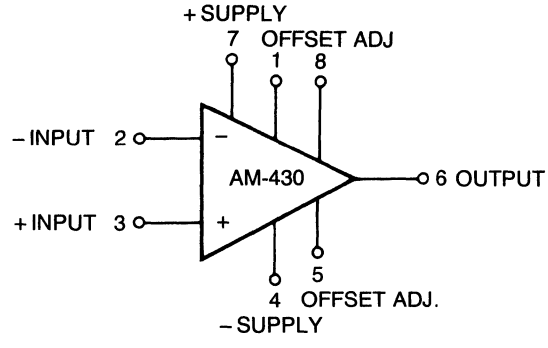
- **0.6 Microvolts/°C maximum drift**
- **25 Microvolts maximum input offset voltage.**
- **2.5 MHz Bandwidth**
- **10^7 Open loop gain**
- **9 nV/$\sqrt{Hz}$ Voltage noise**
- **$\pm$4 nA Maximum bias**

GENERAL DESCRIPTION

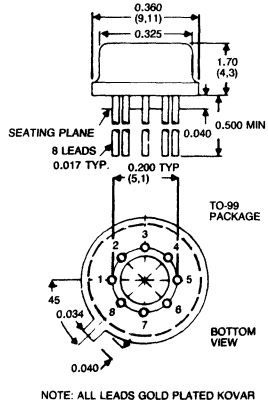
The AM-430 is a chopperless, ultra-low drift monolithic operational amplifier. Excellent input characteristics in conjunction with 2.5 MHz unity gain bandwidth make this amplifier extremely useful for precision integrator, biomedical, and low level signal amplification applications. This amplifier features 25 microvolts maximum input offset voltage, eliminating the need for external zeroing in most applications, and a maximum input offset voltage drift of only 0.6 microvolts/°C; specifications that rival those of more expensive chopper stabilized amplifiers.

Other significant features include 10^7 open loop voltage gain, 100 dB minimum common mode rejection ratio, and $\pm$4 nA maximum bias current. The AM-430 also has low input noise characteristics of 9 nV/$\sqrt{Hz}$ voltage noise density and 0.2 pA/$\sqrt{Hz}$ current noise density. Output voltage range is $\pm$10V minimum at $\pm$25 mA load current with a short circuit protected output.

Dynamic characteristics include a settling time of 11 microseconds to 0.1%, and a minimum slew rate of 0.5V/microsecond. Its unique combination of specifications make the AM-430 ideal for transducer amplification, threshold detector applications, low drift active filters and precision D/A converter output amplifiers.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: ALL LEADS GOLD PLATED KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OFFSET ADJ.
2	– INPUT
3	+ INPUT
4	– SUPPLY VOLTAGE
5	OFFSET ADJ.*
6	OUTPUT
7	+ SUPPLY VOLTAGE
8	OFFSET ADJ.*

*PINS 5 AND 8 ARE INTERNALLY CONNECTED.

4

ABSOLUTE MAXIMUM RATINGS[1]	AM-430A	AM-430B
Power Supply Voltage		±20V
Differential Input Voltage		±15V
Power Dissipation[2]		300 mW

FUNCTIONAL SPECIFICATIONS

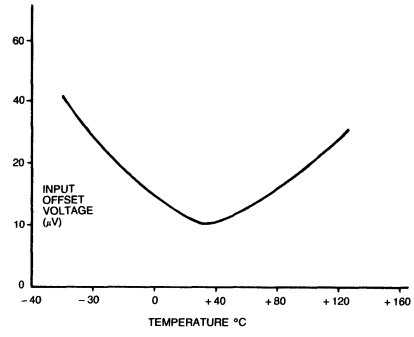
Typical at +25°C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS		
Common Mode Voltage Range, minimum[3]		±12V
Input Resistance, diff. mode		30 MΩ
Input Offset Voltage, maximum	75 μV	25 μV
Input Bias Current, maximum	±4 nA	±2 nA
Input Offset Current, maximum	4 nA	2 nA
OUTPUT CHARACTERISTICS		
Output Voltage, minimum[4]		±10V
Output Current, S.C. protected, minimum		±15 mA
Output Resistance, open loop[5]		45Ω
PERFORMANCE		
DC Open Loop Gain, minimum[6]		120 dB
Input Offset Voltage Drift, maximum	1.3 μV/°C	0.6 μV/°C
Input Bias Current Drift, maximum		40 pA/°C
Input Offset Current Drift, maximum		40 pA/°C
Common Mode Rejection Ratio, minimum		100 dB
Input Noise Voltage Density, 1 kHz		9 nV/√Hz
Input Noise Current Density, 1 kHz		0.2 pA/√Hz
Power Supply Rejection Ratio, minimum[7]		94 dB
DYNAMIC CHARACTERISTICS		
Unity Gain Bandwidth		2.5 MHz
Full Power Frequency		10 kHz
Slew Rate, minimum		0.5V/μsec.
Settling Time, 10V to 0.1%[8]		11 μsec.
Rise Time		340 nsec.
POWER REQUIREMENTS		
Voltage, Rated Performance		±15V dc
Quiescent Current, maximum[9]		1.3 mA
PHYSICAL/ENVIRONMENTAL		
Operating Temperature Range: AM-430A,B		0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Package, Hermetically Sealed		TO-99

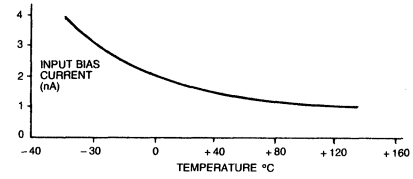
FOOTNOTES:

1. Maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at temperatures above +75°C.
3. Specified at full operating temperature.
4. R_L = 600Ω.
5. Measured under open loop conditions, f = 100 Hz.
6. Vout = ±10V, R_L = 2 kΩ.
7. Vsupp = ±5V dc to ±20V dc. Specified at full operating temperature.
8. G = −1.
9. Specified at full operating temperature.

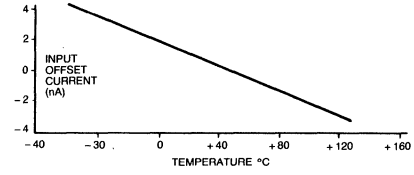
TYPICAL INPUT OFFSET VOLTAGE VS. TEMP



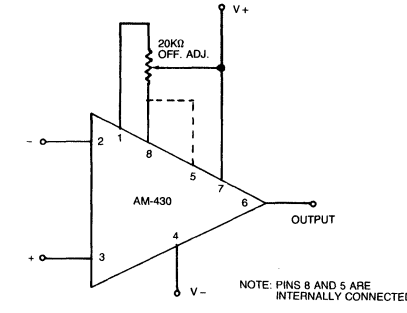
TYPICAL INPUT BIAS CURRENT VS. TEMP.



TYPICAL INPUT OFFSET CURRENT VS. TEMP.



CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL	INPUT OFFSET VOLTAGE DRIFT
AM-430A	1.3 μV/°C maximum
AM-430B	0.6 μV/°C maximum

AM-453-2
Low-Noise, Wideband Monolithic Operational Amplifier

FEATURES

- **4 nV/$\sqrt{Hz}$ Wideband noise voltage**
- **0.6 pA/$\sqrt{Hz}$ Wideband noise current**
- **13V/Microsecond slew rate**
- **20 mA Output current**
- **±3V dc to ±20V dc Supply range**

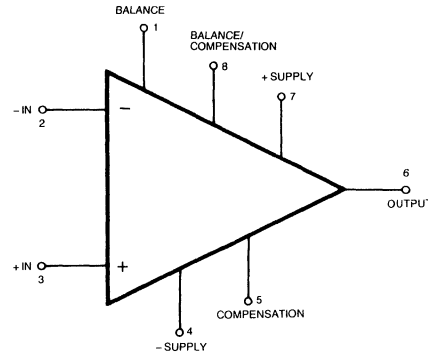
GENERAL DESCRIPTION

The AM-453-2 is a high performance, low noise monolithic operational amplifier. It offers better noise characteristics, improved output drive capability and extended small signal and power bandwidths when compared with standard operational amplifiers.

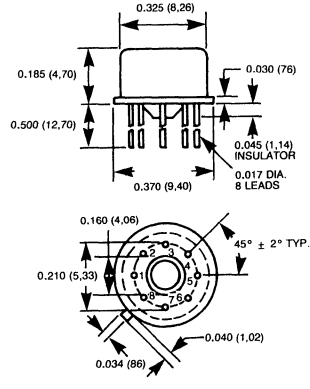
Typical input noise voltage is less than 7 nV/$\sqrt{Hz}$ at 30 Hz and drops to 4 nV/$\sqrt{Hz}$ for frequencies greater than 200 Hz. Input noise current is typically 2.5 pA/$\sqrt{Hz}$ at 30 Hz falling to only 0.6 pA/$\sqrt{Hz}$ frequencies above 1 kHz. Along with low noise performance, the AM-453-2 has a gain bandwidth product of 10 MHz and a full power frequency response that typically extends to 200 kHz for an output swing of ±10V. In addition, the amplifier has the capability to drive 600Ω at 10V (RMS) when supplied by ±18V. The AM-453-2 is internally compensated for a gain of three or greater while frequency response may be optimized for various applications by the addition of an external compensation capacitor. Other features include a minimum common mode rejection ratio of 80 dB, 13V/microsecond slew rate, input overvoltage protection by diodes and a large supply voltage range extending from ±3V to ±20V.

Its low noise, wideband, extended output characteristics make the AM-453-2 exceptionally well-suited to applications in instrumentation and control circuits, data acquisition circuits, wideband transducer amplification and audio frequency analog signal processing including active filters.

Packaged in an 8 lead hermetically sealed TO-99 case, the AM-453-2 is available in two operating temperature ranges, 0°C to +70°C or −55°C to +125°C.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	BALANCE
2	-INPUT
3	+INPUT
4	-SUPPLY
5	COMPENSATION
6	OUTPUT
7	+SUPPLY
8	BAL./COMP.

4

ABSOLUTE MAXIMUM RATINGS

Max. Supply Voltage	±22V
Max. Common Mode Voltage Range	±V Supply
Max. Differential Input Voltage[1]	±0.5V
Max. Power Dissipation	680 mW

FUNCTIONAL SPECIFICATIONS

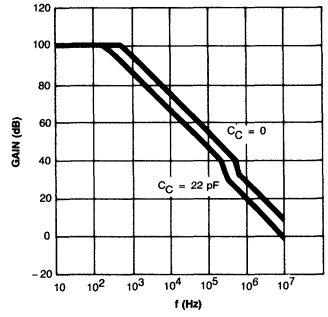
Typical at 25°C, ±15V supply unless otherwise noted.

INPUT CHARACTERISTICS	
Input Offset Voltage	0.5 mV typ., 4 mV max.
Input Offset Current	20 nA typ., 300 nA max.
Input Bias Current	500 nA typ., 1.5 μA max.
Input Resistance	100 KΩ
Common Mode Voltage Range	±12V min.
OUTPUT CHARACTERISTICS	
Output Voltage	±12V min.
Output Current, Short Circuit Protected	±20 mA
Output Resistance	0.3Ω
PERFORMANCE	
Input Offset Voltage Drift[2]	30μV/°C
Input Noise Voltage, 30 Hz	7 nV/√Hz
Input Noise Voltage, 200 Hz – 100 kHz	4 nV/√Hz
Input Noise Current, 30 Hz	2.5 pA/√Hz
Input Noise Current, 1 kHz – 100 kHz	0.6 pA/√Hz
Common Mode Rejection Ratio	100 dB typ., 80 dB min.
Power Supply Sensitivity	10 μV/V
DC Open Loop Gain	100,000 V/V
Full Power Frequency, ±10V Output	200 kHz
Unity Gain Bandwidth	10 MHz
Slew Rate	13V/μsec.
POWER REQUIREMENTS	
Supply Voltage Rated Performance	±15V
Supply Voltage Range	±3V to ±20V
Supply Current	4 mA typ., 8 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
AM-453-C	0°C to +70°C
AM-453-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package, Hermetically Sealed	TO-99

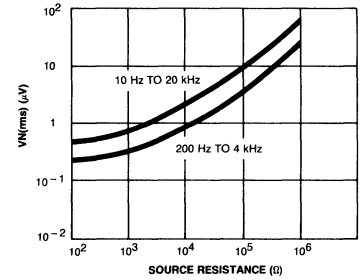
FOOTNOTES:

1. Since the inputs are protected against overvoltage by diodes, differential input exceeding 0.6V will cause large current flows unless current limiting resistors are used. Maximum current should be limited to ±10 mA.
2. 30μV/°C typ. for C models only, 30μV/°C max. for M models.

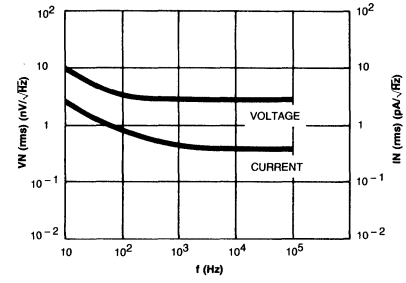
OPEN LOOP FREQUENCY RESPONSE



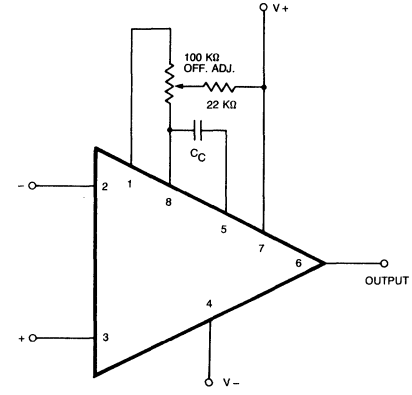
BROADBAND INPUT NOISE VOLTAGE



INPUT NOISE VOLTAGE AND CURRENT VS. FREQUENCY



FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
AM-453-2C	0°C to +70°C
AM-453-2M	−55°C to +125°C

ACCESSORIES

Part Number	Description
TP100K	Trimming Potentiometer Cermet, 100 ppm/°C

AM-450, AM-460 Series Wide Bandwidth, Fast-Settling Monolithic Operational Amplifiers

FEATURES

- **120V/Microsecond slew rate**
- **100 MHz Gain bandwidth**
- **200 Nanoseconds settling to 0.1%**
- **300 Megohm input impedance**
- **Bipolar differential inputs**
- **5 nA Input offset current**

GENERAL DESCRIPTION

DATEL's AM-450 and AM-460 series bipolar input operational amplifiers provide a wide spectrum of capabilities required for high-speed, wide bandwidth signal processing applications. Features available within these two high-performance families include a 100 MHz gain-bandwidth-product (AM-462), a 120V/microsecond slew rate (AM-452), 300 megohm input impedance (AM-460 and AM-462) and 200 nanoseconds settling time to 0.1% of full scale (AM-452).

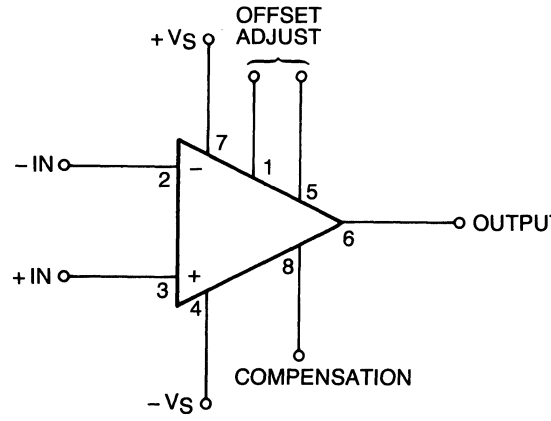
All models provide a full ± 10V output at 10 mA and may be operated in non-inverting as well as inverting modes. Other features common to these units are low input offset currents and low input offset voltages as well as common mode rejection ratios typically greater than 90 dB.

The AM-460 devices are bipolar operational amplifiers with very high impedance differential inputs, making them particularly well suited to applications as high speed comparators, wideband active filters and low distortion oscillators.

Both AM-450 and the AM-460 series units find many applications as fast acquisition sample and hold amplifiers, D/A output amplifiers, A/D input buffer amplifiers, pulse amplifiers, and fast integrators.

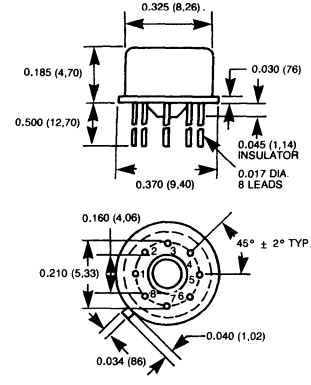
All models are packaged in an 8-lead, hermetically sealed TO-99 package with standard pin out, allowing them to be used easily as pin-for-pin replacements for general purpose IC operational amplifiers.

All models are available in 0°C to +70°C operating temperature range or in −55°C to +125°C for suffix M models.



MECHANICAL DIMENSIONS
INCHES (MM)

TO-99



ABSOLUTE MAXIMUM RATINGS	AM-450	AM-452	AM-460	AM-462
Power Supply Voltage	±20V	±20V	±22.5V	±22.5V
Differential Input Voltage	±15V	±15V	±12V	±12V
Peak Output Current	50 mA	50 mA	Short Circuit Protected	Short Circuit Protected

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, R_L = 2K, unless otherwise noted.

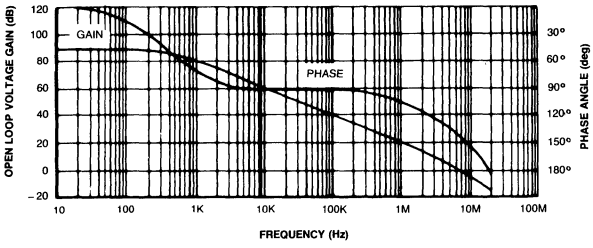
INPUT CHARACTERISTICS	AM-450	AM-452	AM-460	AM-462
Common Mode Voltage Range[1], minimum	±10V	±10V	±11V	±11V
Input Resistance	50 Meg	100 Meg	300 Meg	300 Meg
Input Resistance, minimum	20 Meg	20 Meg	40 Meg	40 Meg
Input Offset Voltage	±4 mV	±5 mV	±3 mV	±3 mV
Input Offset Current, typical	20 nA	20 nA	5 nA	5 nA
maximum	50 nA	50 nA	25 nA	25 nA
Input Bias Current, typical	125 nA	125 nA	5 nA[6]	5 nA
maximum	250 nA	250 nA	25 nA	25 nA
OUTPUT CHARACTERISTICS				
Output Voltage, minimum	±10V	±10V	±10V	±10V
Output Current, minimum[7]	±10 mA	±10 mA	±10 mA	±10 mA
PERFORMANCE				
DC Open Loop Gain[2]	25k V/V	15k V/V	150k V/V	150k V/V
Full Power Bandwidth[2]	500 kHz	1600 kHz	75 kHz	600 kHz
Gain Bandwidth Product	12 MHz	20 MHz	12 MHz	100 MHz
Slew Rate	30V/μsec.	120V/μsec.	7V/μsec.	35V/μsec.
Settling Time, 10V to 0.1%	330 nsec.[3]	200 nsec.[3]	1.5 μsec.[4]	1.0 μsec.
Common Mode Rejection Ratio[5], typical	90 dB	90 dB	100 dB	100 dB
maximum	74 dB	74 dB	74 dB	74 dB
Input Offset Voltage Drift	20 μV/°C	30 μV/°C	10 μV/°C	15 μV/°C
External Compensation Required	None	Gains <3	Gains <3	Gains <5
Power Supply Rejection Ratio	90 dB	90 dB	90 dB	90 dB
POWER REQUIREMENTS				
Voltage, Rated Performance	±15V dc	±15V dc	±15V dc	±15V dc
Operating Voltage Range, minimum	±10V	±10V	±5V	±5V
maximum	±20V	±20V	±22.5V	±22.5V
Supply Current, maximum	6 mA	6 mA	4 mA	4 mA
PHYSICAL/ENVIRONMENTAL				
Oper. Temp. Range, −2 Models			0° to +70°C	
−2M Models			−55°C to +125°C	
Storage Temp. Range			−65°C to +150°C	
Package Type, −2 & −2M Models			TO-99	

FOOTNOTES:

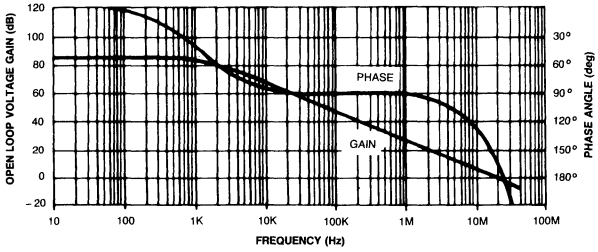
1. At Full Temperature
2. V_{out} = ±10V
3. C_L = 50 pF
4. C_L = 100 pF
5. For ±5V Common Mode Range
6. 15 nA typical for AM-460-2M only
7. AM-460 and AM-462 outputs are short circuit protected

TYPICAL OPEN LOOP FREQUENCY AND PHASE RESPONSE

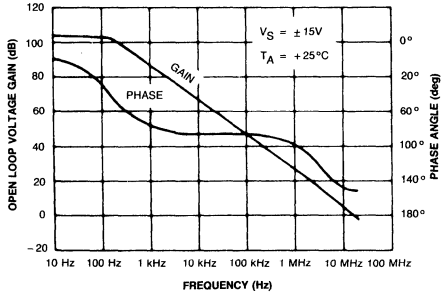
AM-450



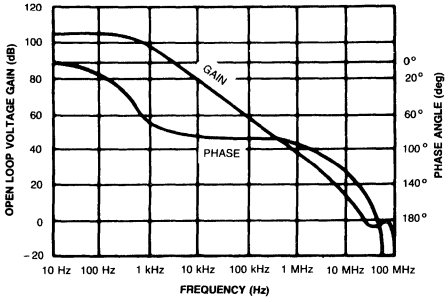
AM-452



AM-460



AM-462



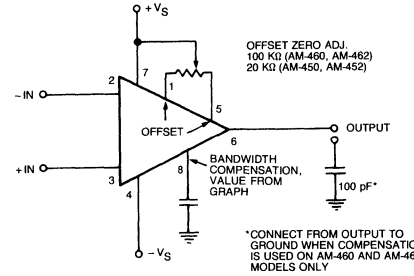
CONNECTIONS

INPUT/OUTPUT CONNECTIONS

ALL -2 AND -2M MODELS

PIN	FUNCTION
1	OFFSET ADJUST
2	-INPUT
3	+INPUT
4	-Vs
5	OFFSET ADJUST
6	OUTPUT
7	+Vs
8	BANDWIDTH CONTROL
ON AM-460, AM-462 THE CASE IS CONNECTED TO-SUPPLY	

EXTERNAL OFFSET ADJUSTMENT AND BANDWIDTH COMPENSATION (ALL MODELS)

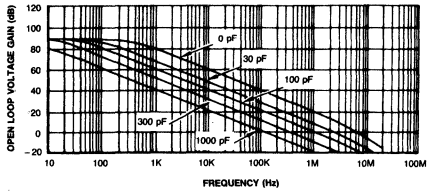


NOTE: PINS SHOWN FOR TO-99 CASE

TYPICAL PERFORMANCE CURVES

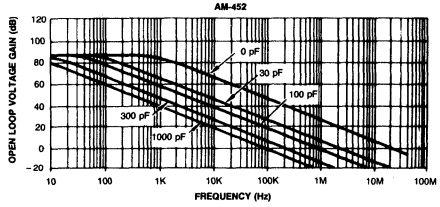
OPEN LOOP FREQUENCY RESPONSE AND EXTERNAL BANDWIDTH COMPENSATION

AM-450



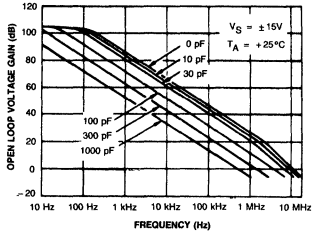
NOTE: EXTERNAL COMPENSATION COMPONENTS ARE NOT REQUIRED FOR STABILITY, BUT MAY BE ADDED TO REDUCE BANDWIDTH IF DESIRED.

AM-452



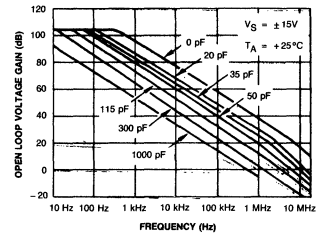
NOTE: EXTERNAL COMPENSATION IS REQUIRED FOR CLOSED LOOP GAIN <3.

AM-460



NOTE: EXTERNAL COMPENSATION COMPONENTS ARE NOT REQUIRED FOR STABILITY, BUT MAY BE ADDED TO REDUCE BANDWIDTH IF DESIRED. IF EXTERNAL COMPENSATION IS USED, ALSO CONNECT 100 pF CAPACITOR FROM OUTPUT TO GROUND.

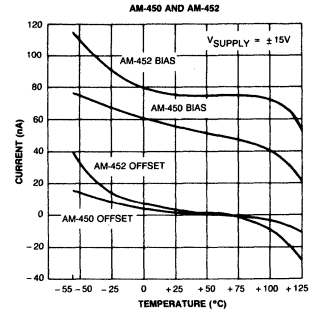
AM-462



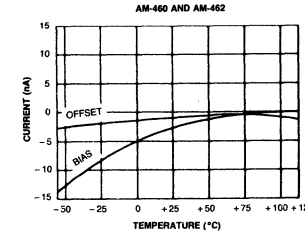
NOTE: EXTERNAL COMPENSATION IS REQUIRED FOR CLOSED LOOP GAIN <5. IF EXTERNAL COMPENSATION IS USED, ALSO CONNECT 100 pF CAPACITOR FROM OUTPUT TO GROUND.

INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

AM-450 AND AM-452

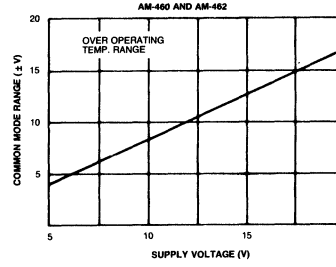


AM-460 AND AM-462



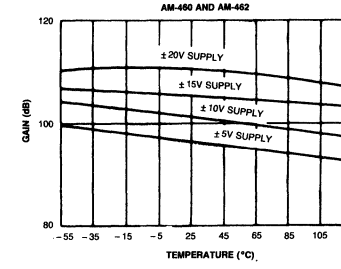
COMMON MODE VOLTAGE RANGE VS. SUPPLY VOLTAGE

AM-460 AND AM-462



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

AM-460 AND AM-462



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
AM-450-2	0°C to +70°C
AM-450-2M	−55°C to +125°C
AM-452-2	0°C to +70°C
AM-452-2M	−55°C to +125°C
AM-460-2	0°C to +70°C
AM-460-2M	−55°C to +125°C
AM-462-2	0°C to +70°C
AM-462-2M	−55°C to +125°C

ACCESSORIES

Part Number	Description
TP100K, TP20K	Trimming Potentiometers

AM-464-2
High Voltage, Monolithic Operational Amplifier

FEATURES

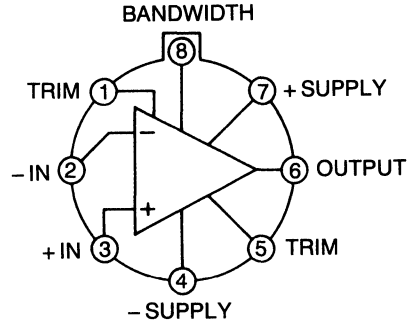
- ±35V Output swing
- ±10V dc to ±40V dc supply
- 4 MHz Gain bandwidth
- 5 V/Microsecond slew rate
- 74 dB Minimum CMRR

GENERAL DESCRIPTION

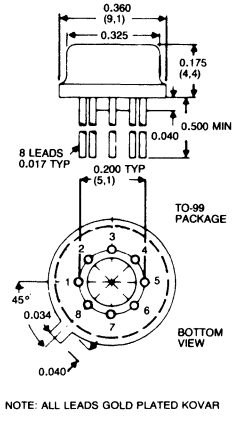
The AM-464-2 is a monolithic IC operational amplifier with an input common mode voltage range of ±35V dc and an output voltage swing of ±35V dc when operated from a ±40V dc supply. Along with high voltage performance, this amplifier has a 4 MHz gain bandwidth product and a 5 V/microsecond output slew rate. It is particularly useful in data conversion circuits and other signal processing applications where higher than normal common mode voltage and output voltage swings are required. The AM-464-2 is internally compensated for all gains and has an on-chip temperature sensing, output current-limiting circuit for absolute output short-circuit protection.

Other features of this amplifier include: common mode rejection of 74 dB minimum, input bias current of 30 nA maximum, and open loop voltage gain of 100,000 minimum. The output slew rate of 5 volts per microsecond gives a 70 volt peak-to-peak sinusoidal output voltage at up to 23 kHz. The power supply voltage can range from ±10V dc to ±40V dc to give output swings from ±5V to ±35V. Power supply quiescent current is only 3.2 mA typical.

The AM-464-2 is packaged in an 8-lead, hermetically sealed TO-99 case and may be used as a pin-for-pin replacement for general purpose IC operational amplifiers such as 741, 101, and 108 for higher voltage applications. Operating temperature range is 0°C to +70°C for the AM-464-2.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: ALL LEADS GOLD PLATED KOVAR

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	TRIM
2	-IN
3	+IN
4	-SUPPLY
5	TRIM
6	OUTPUT
7	+SUPPLY
8	BANDWIDTH (C_B)

ABSOLUTE MAXIMUM RATINGS	
Input Overvoltage	±37V max.
Supply Voltage	±50V max.
Internal Power Dissipation	680 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±40V dc supply, unless otherwise noted.

INPUT CHARACTERISTICS	
Common Mode Voltage Range	±35V min.
Input Impedance, AM-464-2	200 MegΩ
Input Offset Voltage, AM-464-2	±6 mV max.
Input Bias Current, AM-464-2	30 nA max.
Input Offset Current, AM-464-2	30 nA max.
OUTPUT CHARACTERISTICS	
Output Voltage	±35V min.
Output Current[1], AM-464-2	±10 mA min.
Output Resistance	500 ohms
Stable Capacitive Load	100 pF
PERFORMANCE	
DC Gain, 5 KΩ Load	100K V/V min.
Common Mode Rejection[2], AM-464-2	74 dB min.
Input Offset Voltage Drift	15 μV/°C
Input Offset Current[3], AM-464-2	50 nA max.
Input Noise Voltage, 10 Hz-10 kHz	3 μV RMS
DYNAMIC CHARACTERISTICS	
Unity Gain Bandwidth	4 MHz
Slew Rate	5 V/μsec.
Full Power Frequency, 70V peak-to-peak	23 kHz
POWER REQUIREMENTS	
Voltage, Rated Performance	±40V dc
Power Supply Voltage Range	±10 to ±40V dc
Quiescent Current, AM-464-2	4.5 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range, AM-464-2	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package, Hermetically Sealed	TO-99

FOOTNOTES:

1. Overload protected by current limiting and temperature sensing.
2. For common mode voltage = ±30V.
3. At maximum operating temperature.

ORDERING INFORMATION

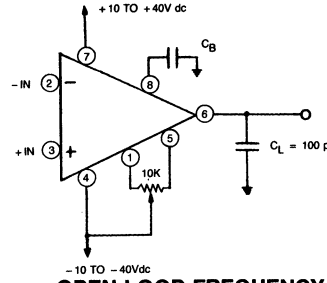
MODEL	OPERATING TEMP. RANGE
AM-464-2	0°C to +70°C

ACCESSORIES

Part Number	Description
TP10K	Trimming Potentiometer

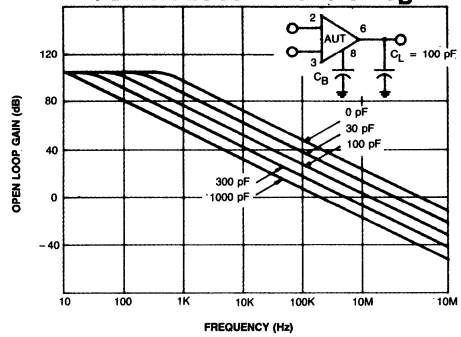
PERFORMANCE PARAMETERS

OFFSET TRIMMING AND BANDWIDTH REDUCTION

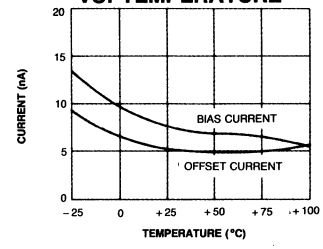


NOTES:
C_B is not required for stability since amplifier is internally compensated. It may be used to reduce bandwidth, however. C_L = 100 pF may be required for stability if external C_B is used.

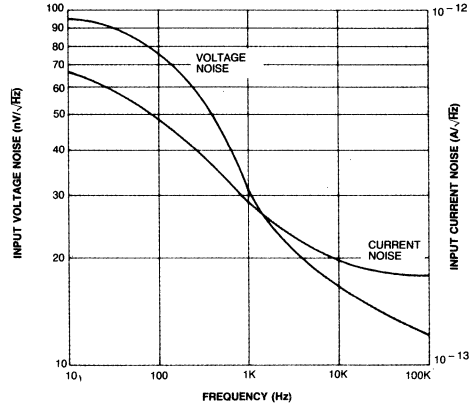
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF C_B



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



INPUT NOISE CHARACTERISTICS



 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

AM-500 Series
Ultra-Fast
Operational Amplifier

FEATURES

- **200 Nanoseconds settling to 0.01%**
- **100V/Microsecond slew rate**
- **100 MHz Minimum gain-bandwidth**
- **10^6 Open loop gain**
- **1 Microvolt/°C drift**
- **±50 mA Output current**

GENERAL DESCRIPTION

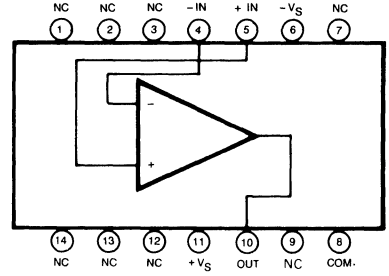
The AM-500 series amplifiers are ultra-fast settling operational amplifiers for use in inverting applications. A unique feedforward amplifier design combines the characteristics of a low drift dc amplifier with those of a very fast AC amplifier. For optimum fast settling performance, this amplifier has an open loop gain roll-off of 6 dB per octave to beyond 100 MHz. Miniature thin-film hybrid construction permits an optimum combination of semiconductor devices and minimum lead lengths to realize the amplifier circuitry. Applications for the AM-500 Series include fast integrators, sample-holds, fast waveform drivers, and fast D/A converter output amplifiers.

Output settling time is 200 nanoseconds maximum to 0.01% for a 10 dc volt step change. Slew rate is 1000V/microsecond for positive output transitions and 1800V/microsecond for negative transitions. This high slew rate permits undistorted reproduction of a full load, 20V peak-to-peak sinewave out to 16 MHz. Gain bandwidth product is 100 MHz minimum.

AM-500 series dc characteristics include a dc open loop gain of 10^6, 30 megohm input impedance, and 1 nanoampere bias current. Input offset voltage is ±0.5 mV and input offset voltage drift is 1 microvolt/°C. Although these amplifiers do not operate differentially, a dc offset voltage in the range of ±5V dc can be applied to the positive input terminal.

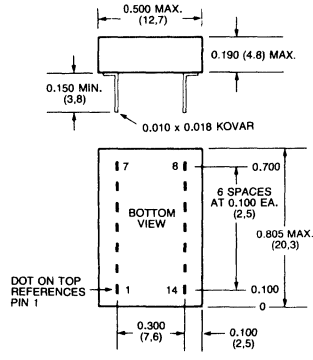
Power supply requirements is ±15 V dc at 22 mA quiescent current. The amplifiers will operate over a supply range of ±10V to ±18V dc. Output current capability is ±50 mA with output short circuit protection. Three basic versions are available: AM-500GC and AM-500MC for 0°C to +70°C, and AM-500MM for −55°C to +125°C. The device package is a 14-pin ceramic DIP.

INPUT/OUTPUT CONNECTIONS



PIN	FUNCTION
1	N.C.
2	N.C.
3	N.C.
4	-INPUT
5	+INPUT
6	-SUPPLY
7	N.C.
8	COMMON
9	N.C.
10	OUTPUT
11	+SUPPLY
12	N.C.
13	N.C.
14	N.C.

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE ±0.01 INCH STANDOFF FROM CASE

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
AM-500GC	0°C to +70°C	Epoxy
AM-500MC	0°C to +70°C	Herm.
AM-500MM	−55°C to +125°C	Herm.

For military devices compliant to MIL-STD-883, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS, AM-500 SERIES

Typical at 25°C, ±15V dc supply, unless otherwise noted.

INPUT CHARACTERISTICS	
Input Common Mode Voltage Range[1]	±5V
Maximum Input Voltage, no damage	±18V
Differential Input Impedance	30 Meg. typical, 3 Meg. min.
Input Bias Current	1 nA typical, 4 nA max.
Input Offset Current	0.5 nA typ., 8 nA max.
Input Offset Voltage	0.5 mV typ., 3 mV max.
OUTPUT CHARACTERISTICS	
Output Voltage	±10V min.
Output Current, S.C. protected	±50 mA typ., ±25 mA min.
Stable Capacitive Load	100 pF
Output Impedance	25Ω
PERFORMANCE	
DC Open Loop Gain	10^6 volts/volt
Input Offset Voltage Drift,	
0°C to +70°C	1 μV/°C typ., 5 μV/°C max.
−55°C to +125°C	5 μV/°C typ., 10 μV/°C max.
Input Bias Current Drift,	
−55°C to +70°C	−20 pA/°C
+70°C to +125°C	doubles every 10°C
Input Voltage Noise,[2]	
0.01 Hz to 1 Hz	5 μV peak-to-peak typ., 25 μV peak-to-peak max.
100 Hz to 10 kHz	1 μV RMS typ., 5 μV max.
1 Hz to 10 MHz	20 μV RMS typ., 100 μV max.
Power Supply Rejection Ratio	80 dB min.
DYNAMIC CHARACTERISTICS	
Gain Bandwidth Product	130 MHz typ., 100 MHz min.
Slew Rate, positive going	1000V/μsec.
Slew Rate, negative going	1800V/μsec.
Full Power Frequency (20V peak-to-peak)	16 MHz
Settling Time,	
10V step to 1%[3]	70 nsec.
10V step to 0.1%[3]	100 nsec.
10V step to 0.01%[3]	200 nsec. max.
Overload Recovery Time	10 μsec.
POWER REQUIREMENTS	
Voltage, rated performance	±15V dc
Voltage, operating	±10V dc to ±18V dc
Quiescent Current	22 mA typ., 33 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
AM-500GC	0°C to +70°C
AM-500MC	0°C to +70°C
AM-500MM	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Package Type	14 pin ceramic
Pins	0.010x0.018″ Kovar
Weight	0.09 ounces (2.5 grams)

FOOTNOTES:

1. dc only
2. −3 dB Single-pole bandwidth
3. 1k Input and feedback resistors, 2.4 pF feedback capacitor

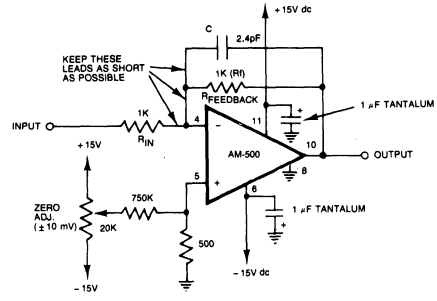
TECHNICAL NOTES

1. The circuit design shows the connection of the AM-500 series for fast settling operation with a closed loop gain of −1. It can be used for fast settling at closed loop gains up to −10. The equivalent resistance seen by the summing junction should be 500 ohms or less. For gains larger than −1 use an input resistor of 500 ohms and pick a feedback resistor for the required closed loop gain (1k for −2, 1.5k for −3, etc.).
2. A small feedback capacitor should be used across the feedback resistor. Determine C in nanofarads from the following formula:

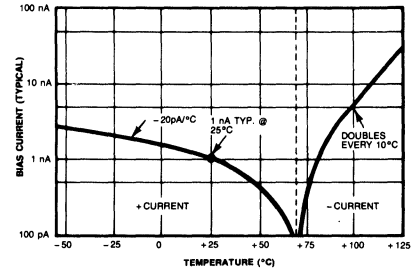
$$C = \frac{1 + |G|}{0.816Rf}$$

   where G is closed loop gain and Rf is in kilohms.
3. Summing point leads must be kept as short as possible. Input and feedback resistors should be soldered close to the body of the resistor directly to the summing point (pin 4). Summing point capacitance to ground must be kept very low.
4. Low output impedance power supplies should be used with 1 μF tantalum bypassing capacitors at the amplifier supply terminals. There are internal 0.03 μF ceramic capacitors in the amplifier.
5. Although these amplifiers are inverting mode only, a dc voltage in the range of ±5V may be applied to the positive input terminal for offsetting the amplifier.
6. For interrupted power applications, apply power to the AM-500 three (3) seconds before operating the device.

CONNECTION FOR FAST SETTLING WITH GAIN OF −1



INPUT BIAS CURRENT VS. TEMPERATURE



AM-542, AM-543
Programmable Gain Instrumentation Amplifiers

FEATURES

- **1 to 1024 Gains**
- **Digital gain selection**
- **10^9 Ω Input impedance**
- **6 Microseconds settling time, AM-543**
- **1 Microvolt/°C offset drift, AM-542**
- **±3 to ±18V dc Analog supply range, AM-542**
- **6 mV Peak-to-peak output voltage noise, AM-543**

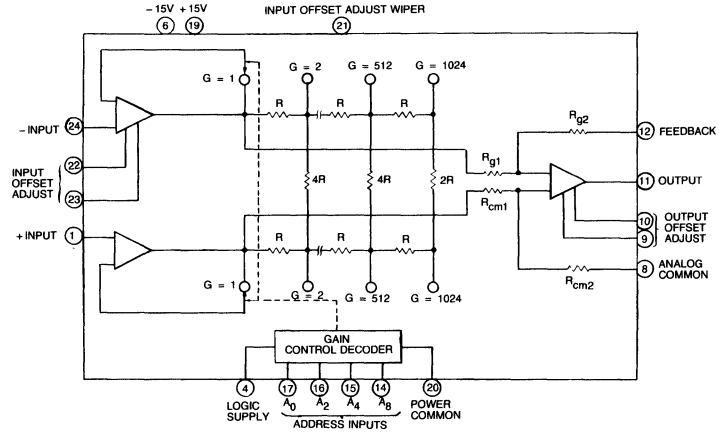
GENERAL DESCRIPTION

The AM-542 and AM-543 are high performance, digitally controlled, Progammable Gain Instrumentation Amplifiers. The AM-542 permits selection of gains from 1 to 1024 in 11 binary weighted steps, while the AM-543 permits selection of gains from 1 to 128 in 8 binary weighted steps. Gain selection is accomplished by the input of a 4-bit word. One version is optimized for low drift with extremely low noise and the other is optimized for fast settling. Use of these devices in data acquisition applications yields a system with wide dynamic range and high resolution.

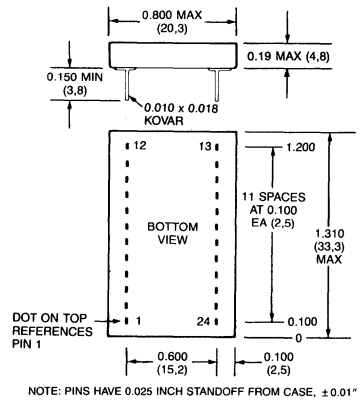
The AM-542 is optimized for low drift performance, having an input offset voltage drift specified at only 1 microvolt/°C, while the gain temperature coefficient is a maximum of only ±5 ppm/°C. Other specifications include an input impedance of 10^9 Ω, Common Mode Rejection of 90 dB minimum, and an output voltage range of ±10.5V dc minimum at 5 mA. The AM-542 operates from analog supply voltages from ±3V dc to ±18V dc with very low power dissipation.

The AM-543 is tailored for high speed applications; a 20V dc step settles to 0.01% in only 6 microseconds maximum at unity gain. These devices also feature a slew rate of 13V/microseconds, an input impedance of 10^{12}Ω, Common Mode Rejection of 80 dB minimum, and a gain temperature coefficient of ±10 ppm/°C maximum. The AM-543 operates with analog supply voltages from ±10V dc to ±16V dc.

Both devices are packaged in a compact, hermetically sealed 24-pin ceramic DIP and are available for operation over the 0°C to +70°C, −25°C to +85°C, and −55°C to +125°C temperature ranges.



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	+INPUT
2	NC
3	NC
4	LOGIC SUPPLY
5	NC
6	−15V dc
7	NC
8	ANALOG COMMON
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	FEEDBACK
13	NC
14	A_8
15	A_4
16	A_2
17	A_0
18	NC
19	+15V dc
20	POWER COMMON
21	INPUT OFF. ADJ. WIPER
22	INPUT OFFSET ADJUST
23	INPUT OFFSET ADJUST
24	−INPUT

4

ABSOLUTE MAXIMUM RATINGS	AM-542	AM-543
Positive Supply, Pin 19	+22V dc	+16V dc
Negative Supply, Pin 6	−22V dc	−16V dc
Input Voltage Range	±20V dc	±20V dc
No Damage	±VCC	±VCC

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS	AM-542	AM-543
Input Offset Voltage, adjust to zero	±200 μV dc, max.	±200 μV dc
Input Bias Current, max.		
MC models	±50 nA	±50 pA
MR/MM models	±14 nA	±50 pA
Input Offset Current, max.		
MC models	±50 nA	±50 pA
MR/MM models	±14 nA	±50 pA
Input Impedance, Diff. Mode	$10^9\Omega$	$10^{12}\Omega$
Com. Mode	2 x $10^9\Omega$	$10^{12}\Omega$
Common Mode Volt. Range min.[1]	±11V dc	±10.25V dc
Digital Inputs, Logic 1, min.[2]	+2.4V dc at 2 μA	+2.4V dc at 2 μA
Digital Inputs, Logic 0, max.	+0.8V dc at 50 μA	+0.8V dc at 50 μA
OUTPUT CHARACTERISTICS		
Output Voltage Range, min.[3]	±10.5V dc	±11V dc
Output Current, min.	±5 mA	±1 mA
Output Offset Voltage, max.[4]	±1 mV dc	±12 mV dc
Output Voltage Noise, dc to 1 MHz, max.[5]	6 mV dc (P-P)	7 mV (P-P)
PERFORMANCE		
Gain Range	1 to 1024	1 to 128
Gain Accuracy, max.	±0.02%	±0.05%
Gain Nonlinearity, max.	0.005%	0.01%
Gain Temp. Coefficient, max.	±5 ppm/°C	±10 ppm/°C
Input Offset Temp. Drift,		
0 to +70°C	1 μV dc/°C	30 μV dc/G +30 μV dc/°C
+70°C to +85°C	5 μV dc/°C	35 μV dc/G +30 μV dc/°C
+85°C to +125°C	10 μV dc/°C	40 μV dc/G +30 μV dc/°C
Power Supply Reject. Ratio, min.	80 dB	80 dB
Input Current Noise, max.[8]	90 pA (P-P)	270 pA (P-P)
Common Mode Rejection Ratio,		
60 Hz, min.[9]	86 dB	86 dB
DC, min.[9]	90 dB	80 dB
Small Signal Bandwidth, (−3 dB)		
G = 1	500 kHz	7 MHz
G = 1024	500 Hz	—
Slew Rate	0.14V dc/μsec.	13V dc/μsec.
Settling Time, 20V dc to 0.01%, max.		
G = 1	150 μsec.	6 μsec.
G = 16	200 μsec.	10 μsec.
G = 64	400 μsec.	40 μsec.
G = 128	400 μsec.	100 μsec.
G = 256	700 μsec.	—
G = 512	1.4 msec.	—
G = 1024	2.8 msec.	—
POWER REQUIREMENTS		
Analog Supply, Rated Value	±15V dc at 20 mA, max.	±15V dc at 40 mA, max.
Analog Supply Range	±3V dc to ±18V dc	±10V dc to ±16V dc
Logic Supply	+3V dc to +18V dc at 5 nA max.	+3V dc to +18V dc at 5 nA max.

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
MC	0 to +70°C
MM[10]	−55 to +125°C
Storage Temperature Range	−65 to +150°C
Package Type	Hermetically sealed 24-Pin DIP

FOOTNOTES:

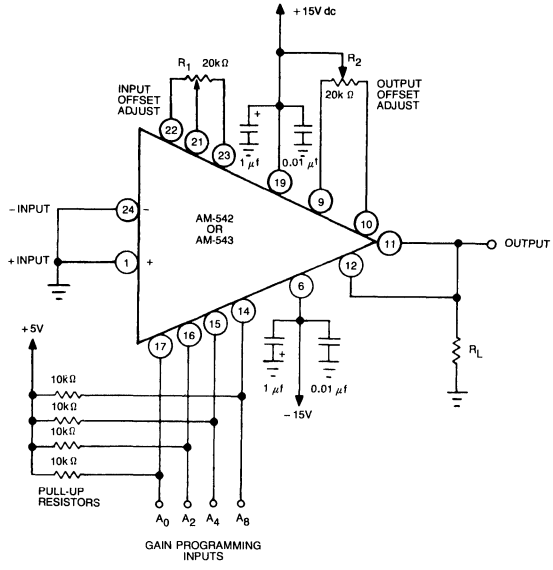
1. As with any three amplifier instrumentation amplifier configuration, the voltage at either input ±½ the output voltage must not exceed ±12V dc (±11V dc — AM543) for linear operation.
2. Requires pull up resistor for TTL logic. Please refer to technical note 3.
3. AM-542, R_L = 2kΩ. AM-543, R_L = 10KΩ.
4. G = 1, adjustable to zero.
5. AM-542, R_S = 5kΩ, G = 1024. AM-543, R_S = 5kΩ, G = 128.
6. Maximum for AM-542MM/MR. Maximum for AM-542MC is ±0.05%.
7. Maximum for AM-542MM/MR. Maximum for AM-542MC is 0.01%.
8. DC to 1 kHz.
9. 1KΩ source imbalance, G = 2.
10. AM-542 only.

TECHNICAL NOTES

1. The AM-542 and AM-543 have an offset adjustment capability for each stage, input and output. The output trim should be sufficient to zero out offset errors on the lower gain ranges, adjustment should be made with a gain of 1 selected. For the higher gain ranges, the input offset zeroing circuit should be used to optimize accuracy. Adjustment of the input offset should be made with a gain of 1024 selected on the AM-542, and a gain of 128 selected for the AM-543.
2. Power supply inputs to the AM-542 and AM-543 are bypassed internally. However, for best performance both power supplies should be bypassed with 1 microfarad electrolytics in parallel with 0.01 microfarad ceramic capacitors as close as possible to the ± supply pins.
3. The digital inputs of the AM-542/543 are TTL/CMOS-compatible. However, when interfacing with TTL logic, it is recommended that 10 kΩ pull-up resistors be used. When interfacing with CMOS logic, the logic supply pin (pin 4) should be connected to the system logic supply.

CONNECTION AND APPLICATION

OFFSET ADJUSTMENT



The AM-542/543 are functionally laser trimmed to reduce initial offset voltage and offset voltage change due to gain change to a minimum level. However, for critical applications where zero offset is required, the following procedure can be followed to externally zero the offset.

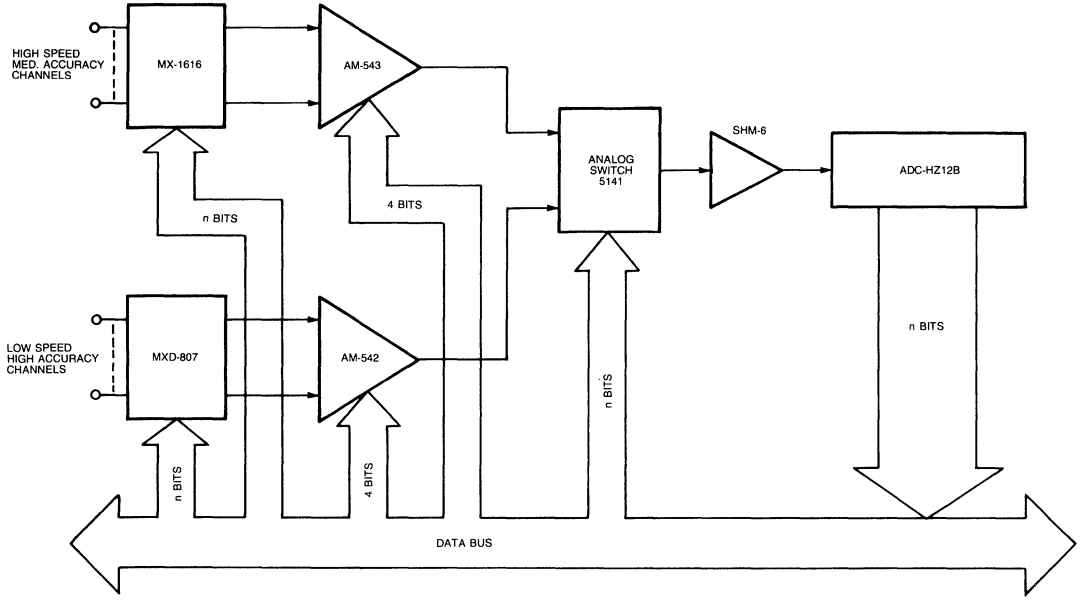
1. Allow the Amplifier to reach operating temperature.
2. Set R_1 and R_2 to mid-range.
3. Set gain to 1 V/V.
4. Adjust R_2 for zero output.
5. Set gain to 1024 (128-AM-543) V/V
6. Adjust R_1 for zero output.

This technique minimizes the offset voltage change over the maximum change in gain. Trimming may cause input offset temperature drift to increase slightly.

GAIN STATE TRUTH TABLE

DIGITAL INPUTS				GAIN	
A_3(PIN 14)	A_1(PIN 15)	A_2(PIN 16)	A_0(PIN 17)	AM-542	AM-543
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	4	4
0	0	1	1	8	8
0	1	0	0	16	16
0	1	0	1	32	32
0	1	1	0	64	64
0	1	1	1	128	128
1	0	0	0	256	—
1	0	0	1	512	—
1	0	1	0	1024	—

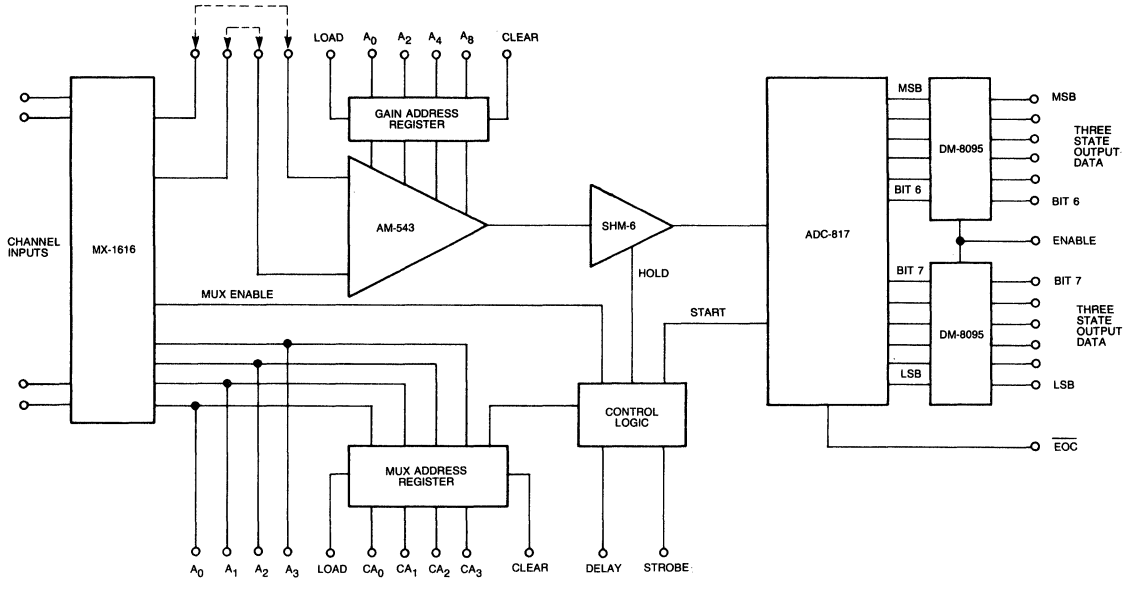
HIGH ACCURACY/HIGH SPEED DATA ACQUISITION SYSTEM



This diagram shows a system that uses the AM-542 with high gain, high accuracy, low-to-moderate speed transducers and the AM-543 with moderate gain, moderate-to-high speed transducers.

TYPICAL APPLICATIONS

HIGH SPEED DATA ACQUISITION SYSTEM

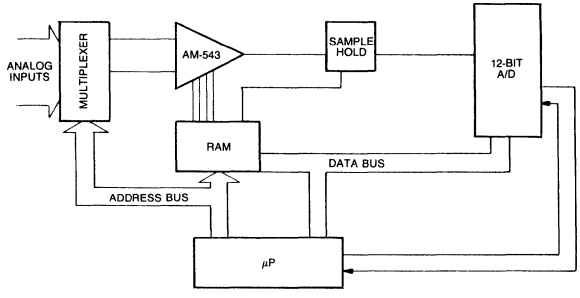


This diagram shows a high-speed data acquisition system with 8 differential inputs and 12-bit resolution using the AM-543. If the control logic is timed so that the Sample-Hold-ADC section is converting one analog value while the mux-amplifier section is allowed to settle to the next input value, throughput rates greater than 156 KHz can be achieved. The AM-543 is used with Datel's ADC-817, a 12-bit hybrid A/D with a 2 μsec conversion rate, the SHM-6, a 0.01%, 1 μsec hybrid Sample-Hold, and the MX-1616, a low cost, high-speed, monolithic analog multiplexer.

The system works as follows:

The μP selects a channel and initiates a conversion at G = 1 and then looks at the MSB of the conversion result. If the MSB = 1, the μP will store the value. If the MSB = 0, the μP will select G = 2. The μP will repeat the cycle of gain incrementing, comparison, and analog-to-digital conversion until the MSB = 1. The μP will then test for an output of all 1's, as this is the full-scale output of the A/D. If the output is all 1's, the μP will decrement the gain by 1 step and perform the final conversion.

MICROPROCESSOR BASED DATA ACQUISITION SYSTEM



A typical application of the AM-542/543 is in a microprocessor controlled data acquisition system. The microprocessor loads the RAM with the desired gain coding. This coding relates the selected gain ranges to a specific address. When the processor instructs the multiplexer to multiplex a particular analog input channel, this instruction is also received by the RAM, which puts out the appropriate gain code to the AM-542/543. This system allows acquisition of signals over a wide dynamic range at high resolution.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
AM-542MC	0°C to +70°C
AM-542MM	−55°C to +125°C
AM-543MC	0°C to +70°C

For military devices compliant to MIL-STD-883, consult DATEL.

AM-551
Low Cost, Programmable Gain Instrumentation Amplifier

FEATURES

- **1 to 1000 Gain range**
- **±0.01% Maximum nonlinearity**
- **2 Microseconds settling time**
- **100 dB CMRR**
- **Low cost**

GENERAL DESCRIPTION

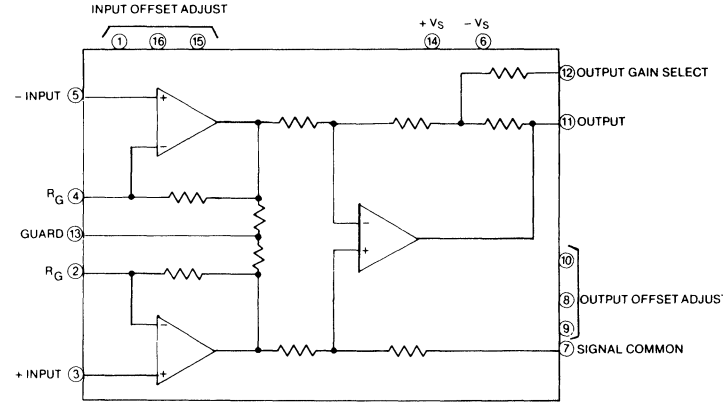
DATEL's AM-551 is a low cost, high performance, programmable gain instrumentation amplifier manufactured with hybrid thin-film technology. Gain is adjustable over a range of 1 to 1000 by the addition of a single external resistor and a simple user-selectable pin-strapping option. Maximum gain nonlinearity is ±0.01%.

The AM-551 dynamic characteristics include a settling time of 2 microseconds for a 20V dc output step to 0.01% accuracy. Slew rate is 23V dc/microsecond and small signal bandwidth is 400 kHz. Other specifications include a common mode rejection ratio of 100 dB, a $10^{12}\Omega$ input impedance and a minimum output voltage swing of ±11V dc. Maximum offset voltage drift is ±15 microvolts/°C.

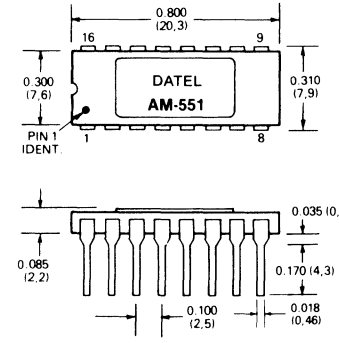
The AM-551 is a self-contained, functionally complete device, containing a high impedance variable gain voltage follower input stage followed by a differential output stage with user selectable gains of 1 or 10. High accuracy, ultra-low drift thin-film technology is used in the fabrication of all interconnected resistor networks.

The combination of high accuracy, speed, low cost, and rugged hybrid construction make the AM-551 an ideal choice for applications involving the remote amplification of low-level signals produced by thermocouples, strain gages and RTD's, high performance data acquisition systems and remote instrumentation systems.

Power requirement is ±15V dc and all devices are cased in miniature, hermetically sealed, 16-pin ceramic packages. Models are available for operation over the commercial, 0°C to +70°C industrial, −25°C to +85°C, and military, −55°C to +125°C operating temperature ranges.



MECHANICAL DIMENSIONS INCHES (MM)



16-PIN CERAMIC DIP

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	INPUT OFFSET ADJUST
2	R_G (Gain Resistor)
3	+ INPUT
4	RG (Gain Resistor)
5	− INPUT
6	$-V_S$
7	SIGNAL COMMON
8	OUTPUT OFFSET ADJ. WIPER
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	OUTPUT GAIN SELECT
13	GUARD
14	$+V_S$
15	INPUT OFFSET ADJUST
16	INPUT OFFSET ADJ. WIPER

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, Pin 14	+18V
Negative Supply, Pin 6	−18V
Input Voltage Range	±18V
Differential Input Voltage Range	±30V
Output Short Circuit	Continuous
Power Dissipation	810 mW

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS	
Input Offset Voltage, unadjusted[1], max.	±1 mV x gain
Input Bias Current, max.	±100 pA
Input Offset Current, max.	±20 pA
Input Impedance, Diff. or Com. Mode	$10^{12}\Omega$
Common Mode Voltage Range, min.	±11V
OUTPUT CHARACTERISTICS	
Output Voltage Range, min.[2]	±11V
Output Current, min.	±5 mA
Output Impedance[3]	0.5Ω
Output Offset Voltage, unadjusted[1], max.	±1 mV x gain
PERFORMANCE	
Gain Range[4]	1 to 1000 V/V
Gain Equation[7]	$G = (1 + 20k/R_G)G_2$
Gain Accuracy, max.	±0.04%
Gain Nonlinearity, max.	±0.01%
Gain Tempco, max.[5]	50 ppm/°C
Offset Voltage Drift, max.	15 µV/°C
Input Bias Current Drift	Doubles for every 10°C
Input Voltage Noise, dc to 100 Hz	20 nV/√Hz
Power Supply Rejection Ratio, min.	82 dB
Common Mode Rejection Ratio[6]	
1 kHz	96 dB
100 Hz	98 dB
dc	100 dB
Slew Rate	23 V/µsec.
Small Signal Response, (−3 dB)	
G = 1	400 kHz
G = 10	150 kHz
G = 100	100 kHz
G = 1000	40 kHz
Settling Time, 20V to 0.01%	
G = 1	2.0 µsec.
G = 10	4.6 µsec.
G = 100	20 µsec.
G = 1000	200 µsec.
POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V dc
Supply Current, max.	±27 mA
Power Supply Range	±5V to ±18V
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
MC	0°C to +70°C
MM	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Package Type	16-Pin Ceramic DIP

FOOTNOTES:

1. Adjustable to zero.
2. R_L = 2 kΩ
3. At 1 kHz, for all gain ranges.
4. To 0.01% accuracy. Higher gains are achievable, however, performance will degrade.
5. Tempco of R_G = ±0 ppm/°C. For R_G = ∞, Gain Tempco = 5 ppm/°C
6. 1 kΩ Source Imbalance.
7. G_2 is the gain of the second stage of the AM-551. Connecting output gain select (Pin 12) to the output (Pin 11) sets the second stage gain at 1. Connecting output gain select (Pin 12) to signal common (Pin 7) sets the second stage gain at 10. R_G is the gain resistor for the first stage and is connected to R_G (Pins 2, 4).

TECHNICAL NOTES

1. A 25 kΩ trimpot may be used for both input and output offset adjusts. The trimpot is connected across the input offset adjust pins (Pins 1, 15) and the wiper is connected to Pin 16.

   For output offset adjust, the trimpot is connected across the output offset adjust pins (Pins 10, 9) with the wiper connected to Pin 8.

2. For unity gain, R_G is left open and the output gain select pin (Pin 12) is tied to the output pin (Pin 11). To avoid oscillation in the unity gain configuration, the connection between the output gain select pin and the output pin should be kept as short as possible.

3. Gain selection is accomplished in two stages. The input stage gain (G_1) is selected by an external gain resistor (R_G) connected across the (R_G) pins, (Pins 2, 4) and is expressed as follows:

$$G_1 = 1 + \frac{20k}{R_G}$$

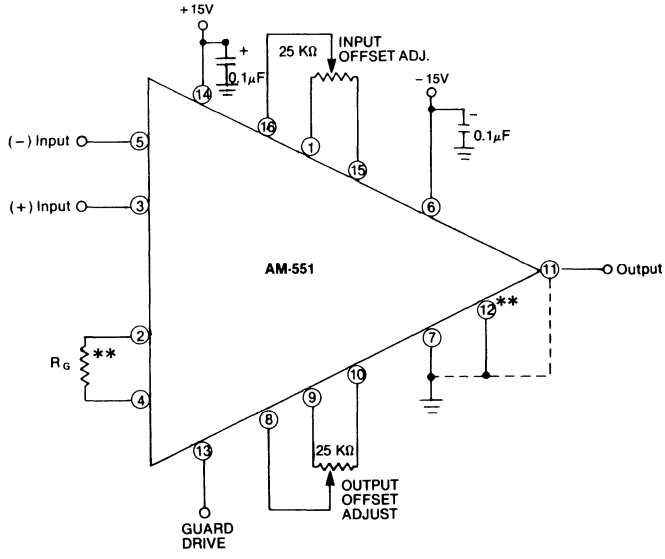
   The output stage gain (G_2) is selected by external pin-strapping: For G_2 = 1, connect the gain select pin (Pin 12) to the output pin (Pin 11). For G_2 = 10, connect the gain select pin (Pin 12) to the signal common pin (Pin 7).

   The total gain of the amplifier is as follows:

$$G_t = G_1 \times G_2 = \left(1 + \frac{20k}{R_G}\right) G_2$$

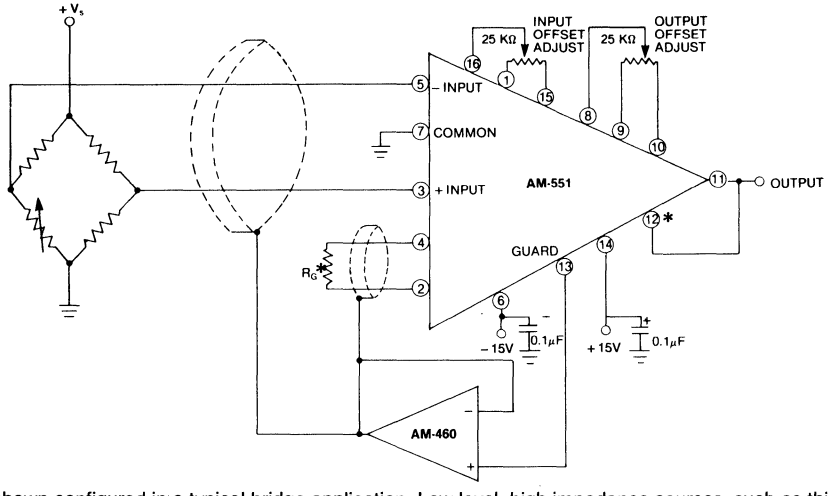
4. Both power supplies should be bypassed to ground with 0.1 microfarad electrolytic capacitors.

TYPICAL CONNECTION DIAGRAM



** See application note #3

TYPICAL BRIDGE TRANSDUCER INTERFACE



The AM-551 is shown configured in a typical bridge application. Low level, high impedance sources, such as this, require proper shielding and grounding, particularly in noisy environments. Shielding of the input leads as well as the gain resistor will minimize induced noise.

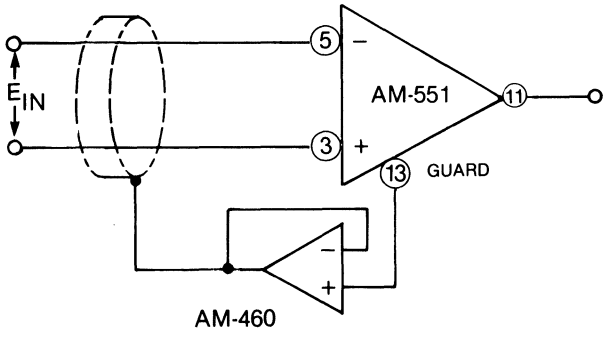
The AM-551 provides a guard output to drive the input cable shield at the input common mode voltage, greatly reducing noise pick-up and system bandwidth degradation as well as improving AC CMRR.

*Connect Pin 12 to Pin 11 for a gain selection of $G = \left(1 + \frac{20K}{R_G}\right)$

Connect Pin 12 to Pin 7 for a gain selection of $G = \left(1 + \frac{20K}{R_G}\right)10$

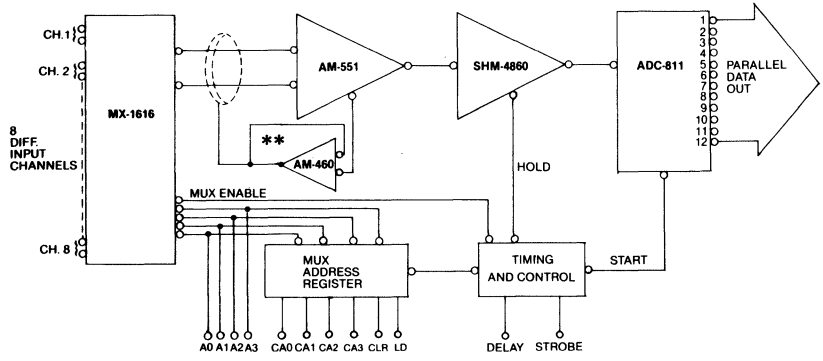
Refer to Technical Note #3 for more information.

GUARD DRIVE CONNECTION



A guard (pin 13) is provided to improve AC common mode rejection by compensating for unbalanced capacitance due to long input leads. Use of the guard function is recommended where input leads are longer than a few inches. In cases where the input leads are very long or where system bandwidth is very high, the addition of a buffer amplifier is recommended. The diagram shows a typical guard drive connection to the AM-551 using DATEL's AM-460.

HIGH SPEED DATA ACQUISITION SYSTEM



This diagram shows a high speed data acquisition system employing the AM-551. This system is capable of a 130 kHz throughput rate with 12-bit resolution. In this system, the AM-551 is coupled with DATEL's MX-1616, a 0.01% high speed multiplexer, SHM-4860, a 0.01% high speed sample/hold and ADC-811, a 12-bit, 4 microseconds hybrid analog to digital converter. Although shown with a differential front end, 16 single input channels can also be used.

**The guard drive circuit (AM-460) is only necessary when using long lead lengths between the MUX and the AM-551.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
AM-551MC	0°C to + 70°C
AM-551MM	−55°C to +125°C

ACCESSORIES

Parts Number	Description
TP25K	Trimming Potentiometer

For military devices compliant to MIL-STD-883, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

AM-7650
Low Cost Chopper-Stabilized Operational Amplifier

FEATURES

- ±5 Microvolt maximum input offset
- 0.05 Microvolt/°C maximum offset drift
- Low cost
- 110 dB Minimum CMRR
- 10 pA Maximum input bias

GENERAL DESCRIPTION

The AM-7650 is a low cost, monolithic chopper-stabilized operational amplifier fabricated using CMOS technology. The amplifier consists of a main dc amplifier, nulling amplifier, output clamp, compensation circuit, and switches controlled by a two-phase oscillator. The extremely low offset voltage drift, 0.05 microvolt/°C maximum, and the initial input offset voltage of only ±5 microvolt maximum eliminate the requirement for external zero adjustment in most applications.

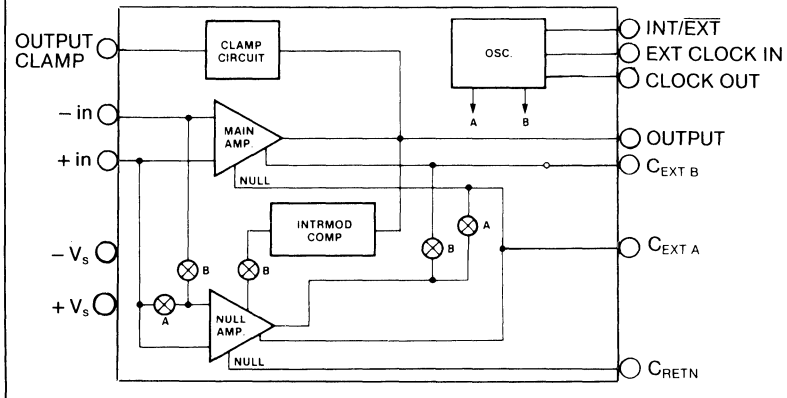
The amplifier achieves its low offset by comparing the input voltages to a nulling amplifier that spends alternate clock phases nulling itself and the main amplifier. Two external capacitors, the only external components necessary, are required to store the correcting potentials on the two amplifier nulling inputs. The compensation circuit minimizes the intermodulation between the applied signal and the chopping frequency. The output clamp circuit reduces the over-load recovery time of the amplifier.

Besides providing virtually glitch-free output and very fast recovery from overloads, the AM-7650 offers differential inputs, maximum input bias current of 10 pA, input noise voltage of only 2 microvolt peak-to-peak, and an input resistance of $10^{12}\Omega$. Unity gain bandwidth product is 2 MHz, CMRR is 110 dB minimum and the open loop gain is a minimum of 120 dB. Long term stability is typically 100 nV/ $\sqrt{\text{mnth}}$.

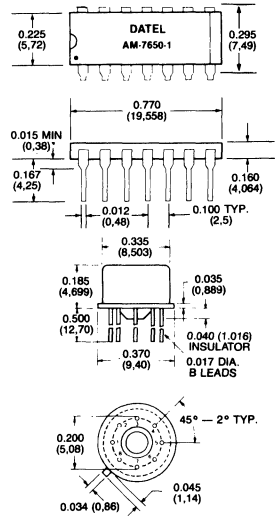
The clock oscillator and all the other circuitry is entirely self-contained, however, the AM-7650-1 includes a provision for the use of an external clock, if required for a particular application. In addition, the AM-7650 is internally compensated for unity gain operation.

Any application where system performance can be significantly improved by a reduction in input offset voltage and bias current is right for the AM-7650. These applications would include inverting or non-inverting amplifier configurations, strain gauge pre-amplifiers, nulling amplifiers, and low offset comparator circuits.

The AM-7650-1 is packaged in a 14-pin DIP and the AM-7650-2 is packaged in an 8-lead, hermetically sealed TO-99 case. Models are available in the 0 to +70°C operating temperature range.



MECHANICAL DIMENSIONS
inches (mm)



INPUT/OUTPUT CONNECTIONS

AM-7650-1

PIN	FUNCTION	PIN	FUNCTION
1	C EXT B	8	C RETURN
2	C EXT A	9	OUTPUT CLAMP
3	NC (GUARD)	10	OUTPUT
4	– IN	11	+ Vs
5	+ IN	12	INT CLOCK OUT
6	NC (GUARD)	13	EXT CLOCK IN
7	– Vs	14	INT/EXT

AM-7650-2

PIN	FUNCTION	PIN	FUNCTION
1	C EXT A	5	OUTPUT CLAMP
2	– IN	6	OUTPUT
3	+ IN	7	+ Vs
4	– Vs	8	C EXT B

ABSOLUTE MAXIMUM RATINGS	AM-7650-1	AM-7650-2
Power Supply Voltage ($+V_S$ to $-V_S$)	18V	
Input Voltage	($+V_S$ +0.3) to ($-V_S$ −0.3)	
Lead Temperature (soldering, 10 seconds)	300°C	
Oscillator Control Voltage (Pins, 12, 14)[1]	$\pm V_S$	
Current into any Pin	10 mA	
Current into any Pin while operating[2]	100 μA	
Total Power Dissipation	375 mW	250 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V supplies unless otherwise noted.

INPUT CHARACTERISTICS	
Input Resistance	$10^{12}\Omega$
Input Offset Voltage, maximum[3]	±5 μV
Input Bias Current, maximum[4]	10 pA
Input Offset Current	8 pA
OUTPUT CHARACTERISTICS	
Output Voltage Swing, minimum[5]	±4.7V
Output Short Circuit Duration	Indefinite
PERFORMANCE	
Large Signal Voltage Gain, minimum[6]	10^6V/V
Input Offset Voltage Drift, maximum	0.05 μV/°C
Long Term Stability	100 nV/√month
Common Mode Voltage Range, minimum	−5.0V
maximum	+3.5V
Common Mode Rejection Ratio, minimum	120 dB
Power Supply Rejection Ratio, minimum	120 dB
Input Noise Voltage[7]	2 μV peak-to-peak
Input Noise Current, 10 Hz	0.01 pA/Hz
Unity Gain Bandwidth	2.0 MHz
Slew Rate[8]	2.5V/μsec
Rise Time	0.2 μsec
Overshoot	20%
Internal Chopping frequency,[9] minimum	120 Hz
maximum	375 Hz
Clamp ON Current[10], minimum	25 μA
Clamp OFF Current[10]	1 pA
POWER REQUIREMENTS	
Power Supply Range ($+V_S$ to $-V_S$), minimum	4.5V
maximum	16V
Power Supply Current (no load), maximum	3.2 mA

PHYSICAL/ENVIRONMENTAL		
Operating Temperature Range	0°C to +70°C	
Storage Temperature Range	−55°C to +150°C	
Package	14 Pin Plastic DIP	8 Pin TO-99

FOOTNOTES:

1. AM-7650-1 only. Voltage on EXT CLOCK IN = ($+V_S$ +0.3V) to (V_S −6.0V)
2. Limiting input current to 100 μA is recommended to avoid latch-up problems. Typically 1 mA is safe, however, it is not guaranteed.
3. Specified at 25°C. Typically ±1.0 microvolts over temperature (0°C to +70°C).
4. Specified at 25°C. Typically 35 pA over temperature (0°C to +70°C). Doubles every 10°C.
5. OUTPUT CLAMP not connected. R_L = 10 kΩ. With R_L = 100 kΩ, the output voltage swing is typically ±4.95V.
6. R_L = 10 kΩ.
7. R_S = 100Ω. 0 to 10 Hz.
8. C_L = 50 pF, R_L = 10 kΩ.
9. Pins 12 and 14 open (DIP).
10. See Technical Note 2.

TECHNICAL NOTES

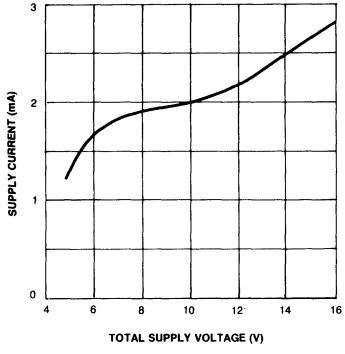
1. Null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (for the AM-7650-1) or the $-V_S$ pin (for the AM-7650-2). This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} (or $-V_S$ for TO-99). C_{EXTA} and C_{EXTB} have optimum values which depend on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. If an external clock is used, the value of C_{EXTA} and C_{EXTB} should be scaled approximately in proportion in order to maintain the same relationship between the chopping freqency and the nulling time constant. A high quality film-type capacitor such as mylar is preferred, however, a ceramic or other lower-grade capacitor may be suitable for many applications. For the quickest settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) are recommended.
2. To reduce overload recovery time which is inherent with chopper-stabilized amplifiers, tie the OUTPUT CLAMP to the inverting input pin or summing junction. A current path between this point and the output pin occurs just before the device output saturates. Thus, uncontrolled differential inputs are avoided, along with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.
3. To avoid latch-up, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latch-up, even under fault conditions.
4. All of the AM-7650's inputs are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided as this can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

5. The open loop gain of this amplifier will be 17 dB 8 lower with a 1 kΩ load than with a 10 kΩ load. If the device is used strictly for dc applications, the lower gain is of little consequence since the dc gain of this device is greater than 120 dB with loads down to 1 kΩ. For wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or greater. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.
6. Due to thermo-electric or Peltier effects arising in the thermocouple junctions of dissimilar metals, alloys, silicon, etc., special precautions should be made to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High impedance loads are preferable, and good separation from surrounding head-dissipation elements is recommended.
7. Care must be taken in the assembly of printed circuit boards to take full advantage of the AM-7650's low input currents. The boards should be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination. Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and the adjacent metal runs. Input guarding of the 8-pin TO-99 package can be accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when the device is inserted into the board. The guard which is a conductive ring surrounding the inputs, is connected to a low impedance point that is approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard. The pin configuration of the 14-pin DIP version is designed to facilitate guarding since the pins adjacent to the inputs are not used.

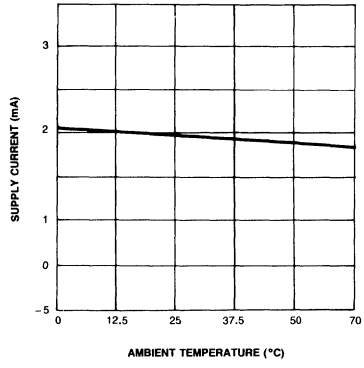
4

PERFORMANCE

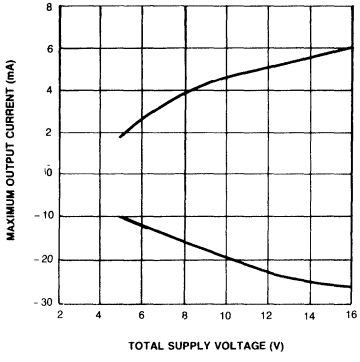
SUPPLY CURRENT VS. SUPPLY VOLTAGE



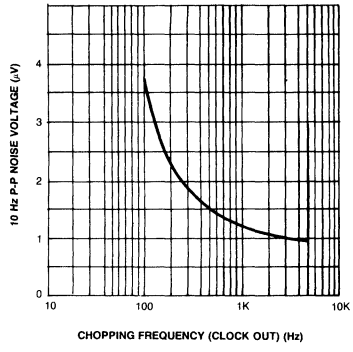
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



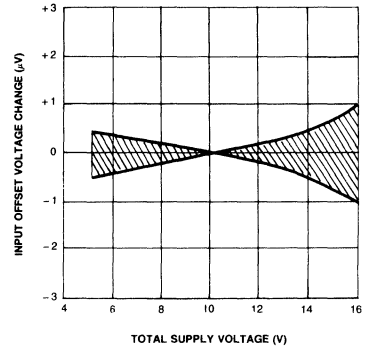
MAXIMUM OUTPUT CURRENT VS. SUPPLY VOLTAGE



10 Hz P-P NOISE VOLTAGE VS. CHOPPING FREQUENCY

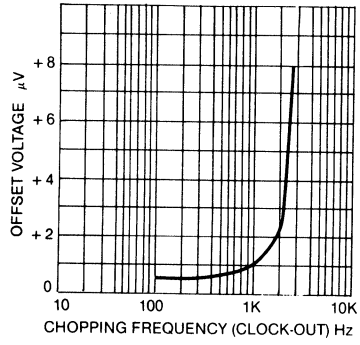


INPUT OFFSET VOLTAGE CHANGE VS. SUPPLY VOLTAGE

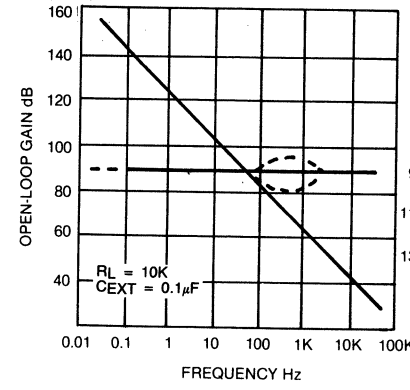


PERFORMANCE

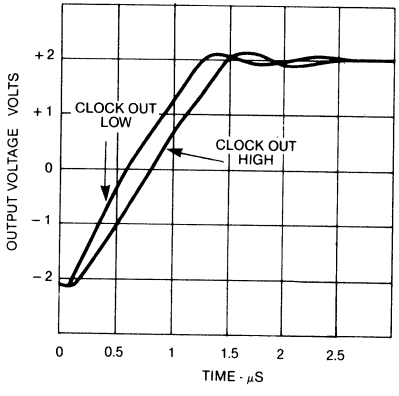
INPUT OFFSET VOLTAGE
vs. CHOPPING FREQUENCY



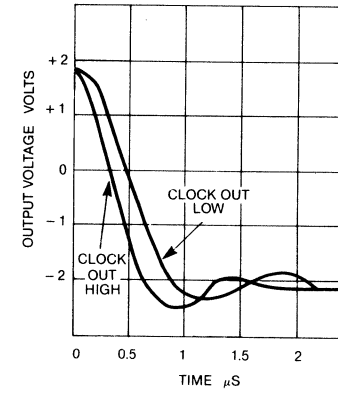
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE

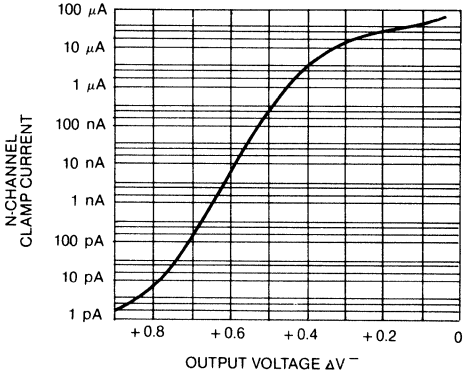


VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE

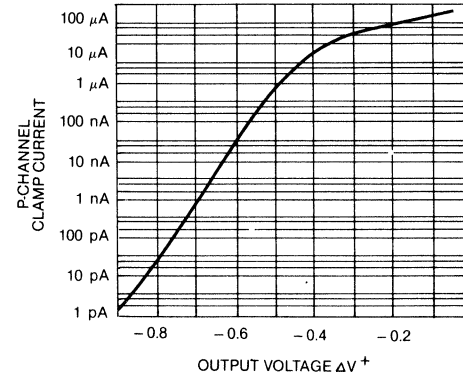


THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK

N-CHANNEL CLAMP CURRENT
vs. OUTPUT VOLTAGE



P-CHANNEL CLAMP CURRENT
vs. OUTPUT VOLTAGE

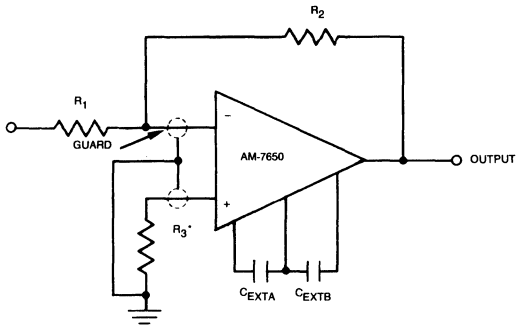


DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

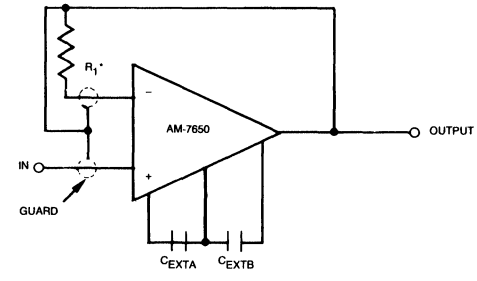
CONNECTION

INPUT GUARD CONNECTION

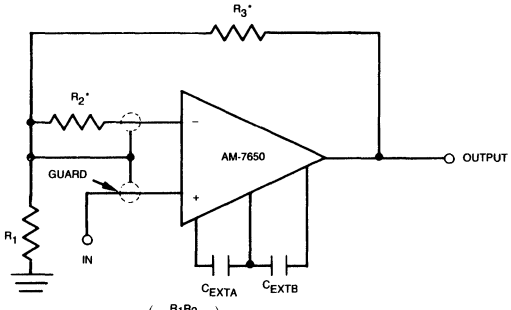
INVERTING AMPLIFIER



VOLTAGE FOLLOWER



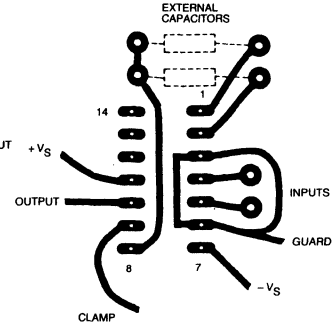
NON-INVERTING AMPLIFIER



R_1/R_2 COMBINATION $\left(\frac{R_1R_2}{R_1+R_2}\right)$ MUST BE LOW IMPEDANCE

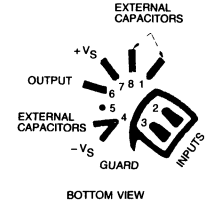
*COMPENSATES FOR LARGE SOURCE RESISTANCE

SUGGESTED BOARD LAYOUT AM-7650-1



BOTTOM VIEW

SUGGESTED BOARD LAYOUT AM-7650-2

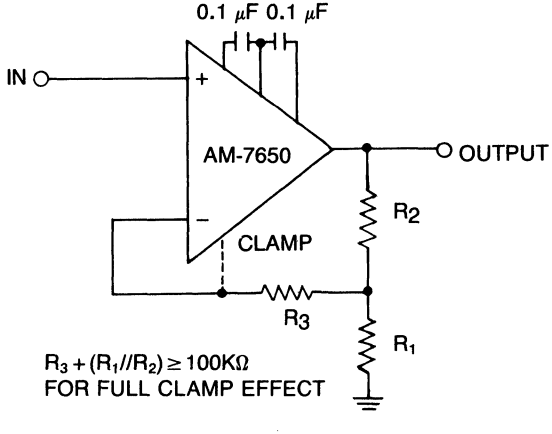


BOTTOM VIEW

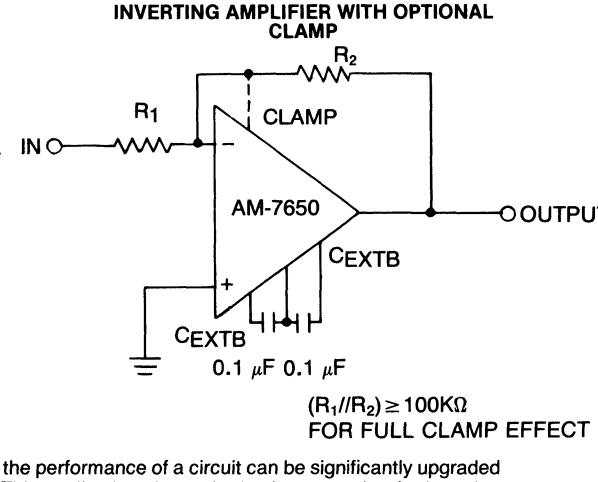
THIS LAYOUT REQUIRES A 10-PIN LEAD CIRCLE.

TYPICAL CONNECTION

NON-INVERTING AMPLIFIER WITH OPTIONAL CLAMP

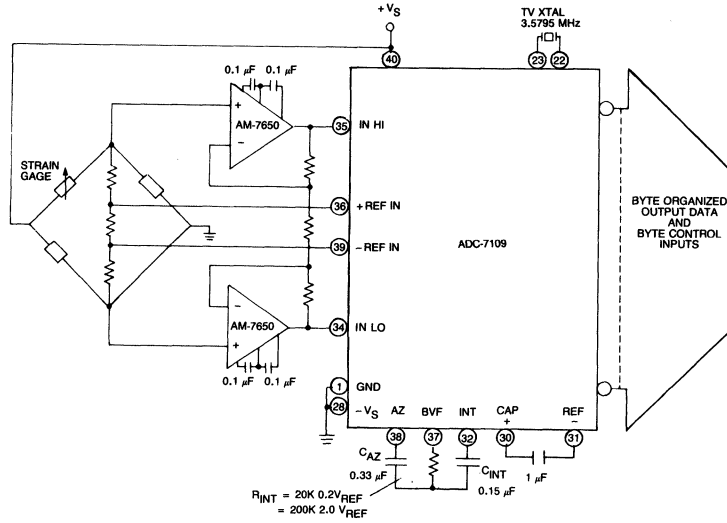


INVERTING AMPLIFIER WITH OPTIONAL CLAMP



The AM-7650 can be used in any application where the performance of a circuit can be significantly upgraded by improved input offset voltage and bias current. This application shows the basic connection for inverting and non-inverting configurations of the AM-7650. The "Output Clamp" function is used to improve the overload recovery performance.

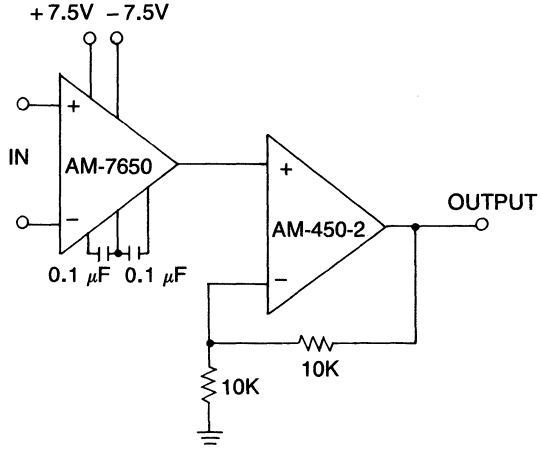
APPLICATION
DIFFERENTIAL PRE-AMP FOR ADC-7109



Two AM-7650s may be used with Datel's ADC-7109, 12-bit integrating A/D converter to construct a preamplifier for signals from bridge type transducers such as strain gages. The circuit will maintain high differential gain without any common-mode gain.

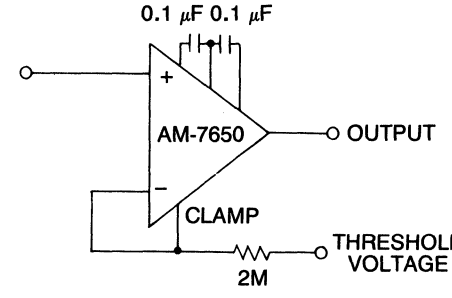
This circuit also works well with thermocouples in noisy environments where shielding is grounded at the sensing end.

BOOSTING OUTPUT DRIVE CAPABILITY



The AM-7650 is an ideal replacement for any operational amplifier with the only limitations being the supply voltage (±8V max) and the output drive capability, (10 kΩ load for a full output swing). These limitations can be overcome by using a booster amplifier as shown.

LOW OFFSET COMPARATOR



The AM-7650 will operate well as a low offset comparator. Other chopper amplifiers perform poorly under overload conditions. However, the optional overload avoidance feature (output clamp) allows the AM-7650 to be used in many of these applications.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	PACKAGE
AM-7650-1	0 to +70°C	Plastic DIP
AM-7650-2	0 to +70°C	TO-99

SCM-100, SCM-101
Four-Channel, Isolated Signal Conditioning Modules

FEATURES

- **Wide input span range**
- **4-Channel operation**
- **±1000 Volts peak isolation voltage**
- **156 dB CMR**
- ***±0.02% Maximum nonlinearity***
- **±1 Microvolt/°C input offset drift**
- **Low cost**

GENERAL DESCRIPTION

The SCM-100 and SCM-101 are low-cost, high performance signal conditioning modules designed to interface with low-level thermocouple and high-level analog input signals respectively. Each module is a functionally complete unit, consisting of four individually isolated input channels multiplexed into a single output amplifier. Common Mode isolation is ±1000 volts peak.

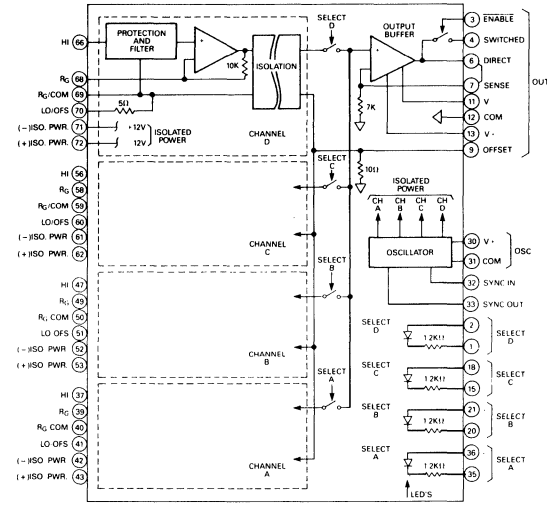
The SCM-100 is optimized for low level signal conditioning. An input span range of ±5 mV to ±100 mV and common mode rejection ratio of 156 dB minimum make this module an ideal choice for interfacing with thermocouples or strain gages, where low level signals require amplification in the presence of high common mode voltages. The SCM-100B features a maximum gain temperature coefficient of ±25 ppm/°C and an input offset temperature drift of only ±1 microvolt/°C maximum.

The SCM-101 is optimized for ±50 mV to ±5V or 4-to-20 mA input signals. Other specifications include a minimum common mode rejection ratio of 145 dB, a maximum gain temperature coefficient of ±25 ppm of FS/°C and a maximum input offset voltage drift of ±5 microvolt/°C.

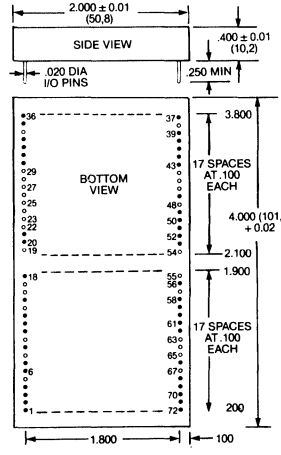
All models feature a minimum channel scanning rate of 400 channels/second. Long term stability is specified at 1.5 microvolts/month and gain nonlinearity as low as ±0.02% maximum. Their combination of functionally complete design, wide input range, high noise rejection, small size, and low cost make these devices an ideal choice for applications involving multi-channel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation.

Each device is packaged in a compact 2″ x 4″ x 0.4″ encapsulated module.

SCM-100, SCM-101



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	– CHAN. D. SELECT	40	CHAN A RG/COMMON
2	+ CHAN D. SELECT	41	CHAN A LO/OFFSET
3	SWT. OUTPUT ENABLE	42	CHAN A (–) ISO. POWER
4	SWITCHED OUTPUT	43	CHAN A (+) ISO. POWER
6	DIRECT OUTPUT	47	CHAN B HI INPUT
7	OUTPUT SENSE	49	CHAN B RG
9	OUTPUT OFF ADJ	50	CHAN B RG/COMMON
11	OUTPUT POWER, –15V	51	CHAN B LO/OFFSET
12	OUTPUT POWER, COMMON	52	CHAN B (–) ISO. POWER
13	OUTPUT POWER, +15V	53	CHAN B (+) ISO. POWER
15	– CHAN C SELECT	56	CHAN C HI INPUT
18	+ CHAN C SELECT	58	CHAN RG
20	– CHAN B SELECT	59	CHAN C RG/COMMON
21	+ CHAN B SELECT	60	CHAN C LO/OFFSET
30	OSCILLATOR POWER, + Vs	61	CHAN C (–) ISO. POWER
31	OSCILLATOR POWER, COMMON	62	CHAN C (+) ISO. POWER
32	SYNC IN	66	CHAN D HI INPUT
33	SYNC OUT	68	CHAN D RG
35	– CHAN A SELECT	69	CHAN D RG/COMMON
36	+ CHAN A SELECT	70	CHAN D LO/OFFSET
37	CHAN A HI INPUT	71	CHAN D (–) ISO. POWER
39	CHAN A RG	72	CHAN D (+) ISO. POWER

4

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS	SCM-100A	SCM-100B	SCM-101
Number of Channels	4	4	4
Input Span Range	±5 mV to ±100 mV	±5 mV to ±100 mV	±50 mV to ±5V
Input Offset Voltage, max.[1]	±20 μV	±20 μV	±50 μV
Input Noise Voltage[2]	0.6 μV P-P	0.6 μV P-P	0.6 μV P-P
Input Bias Current, max.	+8 nA	+8 nA	+8 nA
Input Resistance			
Power On	100 MΩ	100 MΩ	100 MΩ
Power Off, min.	35KΩ	35KΩ	74KΩ
Common Mode Voltage Range[2],			
ac, 60 Hz	750V RMS	750V RMS	750V RMS
ac or dc, max.	±1000 V pk	±1000 V pk	±1000 V pk
Common Mode Rejection Ratio[4],			
min., G = 1000	156 dB	156 dB	
G = 50	128 dB	128 dB	
G = 100			145 dB
G = 1			110 dB
Normal Mode Input Without Damage 60 Hz	130V RMS	130V RMS	130V RMS
Normal Mode Rejection,			
min., G = 1000	55 dB	55 dB	
G = 100			55 dB
Open Input Detection Time[5]			
G = 1000	6 sec.	6 sec.	
G = 100	120 sec.	120 sec.	
OUTPUT CHARACTERISTICS			
Output Voltage Swing[6]	±5V at ±5 mA	±5V at ±5 mA	±5V at ±5 mA
Output Offset Voltage, max.[1]	±12 mV	±12 mV	±12 mV
Output Noise, dc to 100 kHz	0.8 mV P-P	0.8 mV P-P	0.8 mV P-P
Output Resistance			
Direct Output	0.1Ω	0.1Ω	0.1Ω
Switched Output	35Ω	35Ω	35Ω
PERFORMANCE			
Gain Equation	G = 1 + 10kΩ/R_G	G = 1 + 10kΩ/R_G	G = 1 + 10KΩ/R_G
Gain Nonlinearity[7], max., G = 1 to 100[8]			−0.2% min. to −0.55% max.
G = 50 to 300	±0.03%	0.02%	
Typical, G = 1000	±0.03%	±0.03%	
Gain Temp. Coef., max.	±35 ppm/°C	±25 ppm/°C	±25 ppm/°C
Input Offset Temp. Drift, max.	±2.5 μV/°C	±1 μV/°C	±5 μV/°C
Input Offset Drift vs Time	±1.5 μV/month	±1.5 μV/month	±1.5 μV/month
Output Offset Temp. Drift, max.	±50 μV/°C	±50 μV/°C	±50 μV/°C
Total Offset Drift, RTI, max.	±(2.5 +50/G) μV/°C	±(1 + 50/G) μV/°C	±(5 +50/G) μV/°C
Channel Selection Time[9], max.	2.5 msec.	2.5 msec.	2.5 msec.
Channel Scanning Speed, min.	400 channels/sec.	400 channels/sec.	400 channels/sec.
Channel Select Input Reverse Voltage Rating, max.	3V	3V	3V
POWER REQUIREMENTS			
Analog Supply, rated value	±15V dc ±10%		
Analog Supply Range, max.	±12V dc to ±18V dc		
Analog Supply Current, max. ±V_s = 15V dc	±4 mA		
Oscillator Supply, rated value	+13.5V dc to +24V dc		
Oscillator Supply, absolute value max.	+26V dc		
Oscillator Supply Current, max. +V_{OS} = +15V	40 mA		
Power Supply Sensitivity, RTI			
Analog Supply	1 μV/V		
Oscillator Supply	1 μV/V		

PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0°C to +70°C
Storage Temp. Range	−55°C to +85°C
Relative Humidity[9]	0 to 85%
Case Size	2″ x 4″ x 0.4″ (50,8 x 101,6 x 10,2 mm)

FOOTNOTES:

1. Adjustable to zero.
2. R_S = 1KΩ, 0.01 Hz to 100 Hz.
3. Channel to channel or channel to ground.
4. $R_S \leq 100\Omega$, f ≥ 50 Hz.
5. Response time can be reduced by addition of external resistors.
6. Short circuit protected.
7. Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line.
8. A negative gain error is purposely introduced to allow all channels to be matched at G = >1 by trimming the input gain. The gain is then set by the output gain adjustment.
9. To +0.01% full scale.

TECHNICAL NOTES

1. To minimize coupling between input and output, keep all leads associated with signals on the input as far as possible from leads associated with output signals. The use of a guard track on both sides of the board (see typical connection) may be helpful. The power supplies should be decoupled with tantalum capacitors mounted as close to the device as possible.
2. For lowest noise, the grounding scheme shown in the typical connection diagram should be used. To prevent power supply currents from flowing in the low lead of the signal output, the output signal common should be tied directly to the output power common pin (pin 12), with the power supply returns brought separately to pin 12.
3. When using an unregulated power source for the oscillator, a 0.1 μf capacitor should be connected directly from the output power common (pin 12) to the oscillator power common (pin 31). Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A one or two volt potential difference between the two power supply commons will not affect operation.
4. Channel selection is determined by the select inputs. Each select input consists of an LED in series with a resistor. Turning the LED on (± ≥2.5 mA) turns the channel on, and turning the LED off (± ≤50 μA) turns the channel off. The easiest way to use the select inputs is to

tie all the Select (+) inputs (pins 2, 18, 21 and 36) to +5V and drive the Select (–) inputs (pins 1, 15, 20 and 35) from TTL logic. Open-collector or totempole outputs can be used.

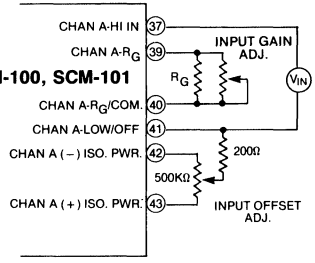
With a +15V logic supply, a standard CMOS decoder or gate can supply enough current to drive the select inputs. At higher CMOS supply voltages, more current than the required 2.5 mA will flow into the select inputs. While this will not affect operation, it can be brought back to the minimum value if desired by putting a resistor in series with the decoder or gate output and the select (–) input. For 10V dc operation, a 2KΩ resistor should be used and at 15V dc, a 2.9KΩ.

5. The maximum reverse voltage applied to any select input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25 mA. Select inputs are isolated from all other circuits in the module and may be operated at up to ±50V with respect to output and power ground. Channels may be selected in any order with no restrictions on rate or duty cycle — except the 2.5 nanoseconds settling time for channel access. However, selecting two or more channels simultaneously for more than a few microseconds will result in very long settling times.
6. Output filtering is not required in most applications, since the affect of the small carrier-related noise spikes on the output (<1 =mV peak-to-peak, 100 kHz B.W.) drops off rapidly as bandwidth decreases. To eliminate the carrier noise, a simple R-C filter (for example — 1KΩ, 0.0047 μf) may be used at the output. Only one filter is required, even when using multiple modules. However, if the load to be driven has an input resistance of less than 10 MΩ, a buffer will be needed.
7. Output errors caused by differences in individual oscillator frequencies may occur in applications where multiple SCM-100/101's are used in close proximity or when system clock signals are present near the isolator. To eliminate these errors, multiple units may be synchronized by connecting the Sync Output (pin 33) of one module to the Sync Input (pin 32) of the adjacent module. The first module of a group may be synchronized to an external source via the SYNC IN (Pin 32). Sync wiring should be separated from analog signal runs to keep noise pickup at a minimum. (See External Synchronization.) The frequency of the external Sync Source (if used) will have a slight effect on the gain and output offset of the device. Thus, any adjustments should be made with the modules synchronized.

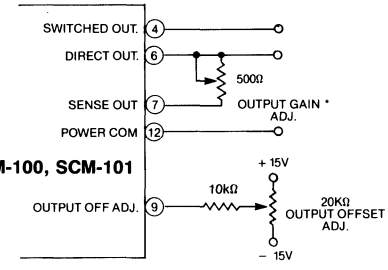
4

TYPICAL CONNECTION AND CALIBRATION

INPUT OFFSET AND GAIN ADJUST



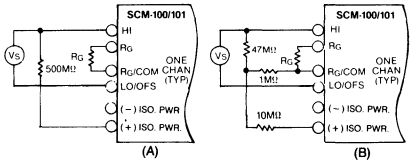
OUTPUT OFFSET AND GAIN ADJUST



TRIM POTS ARE 10 TURN.

GAIN ADJUST RANGE SHOULD NOT EXCEED 10% TO MAINTAIN GAIN STABILITY

OPEN INPUT DETECTION



GAIN ADJUST — The gain of each channel is independently adjusted by an external gain resistor (R_G). A trimpot may be connected in parallel with R_G to trim out R_G's tolerance and the modules gain error. R_G should be chosen to give an untrimmed gain slightly less than the desired trimmed gain.

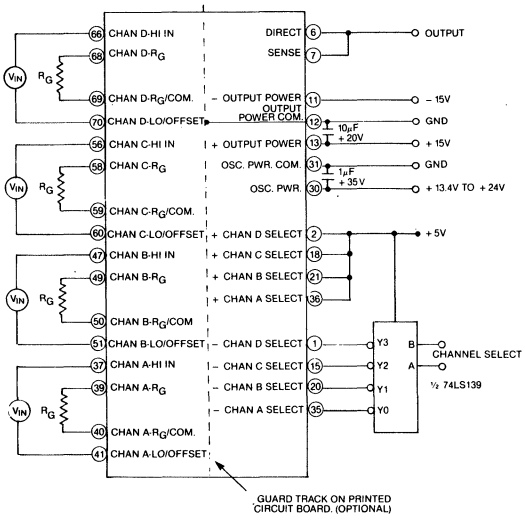
OFFSET ADJUST (optional) — The input offset of each channel may be fine adjusted with an external trimpot if required. This fine adjust has a limited range of ±250 μV and can be used to adjust each channel for zero offset while operating at the desired gain. Since the range of this adjustment is so limited, it is recommended that the output offset be adjusted first. Output Offset Adjustment should be made as follows:

1. Select the desired channel.
2. Apply zero volts in and set for unity gain. (This can be done by disconnecting R_G.)
3. Set the OUTPUT OFFSET ADJUST for an output of 0V.

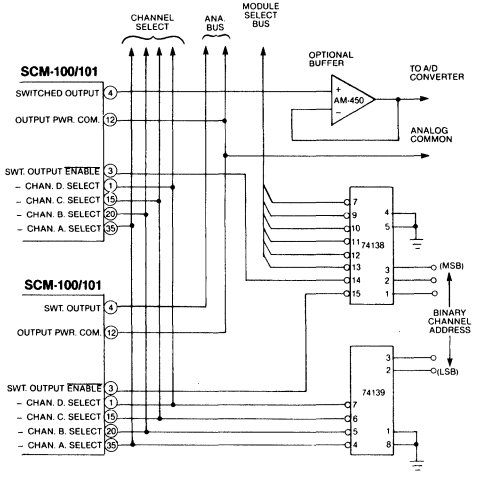
Since only a few nA of input bias current is available to charge the input filter, the response time for open input detection can be in the tens of seconds. Shorter response times and a positive overscale if required may be achieved with one of the above circuits which will augment or reverse the input bias current. Either circuit will supply a bias current of approximately 20 nA which may be used to aid or oppose the 3 nA supplied from the module. Circuit A has the advantage of simplicity, however, the high value resistor may not be readily available. Circuit B solves the problem at the expense of complexity. The component values may be varied to give an optimum trade of bias current for response time as required. The values shown will give a typical response time of 2 to 5 seconds.

TYPICAL CONNECTION

SCM-100, SCM-101



EXPANSION TO 32 CHANNELS



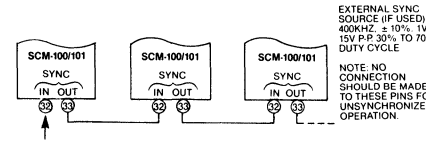
The SCM-100/101 are mainly used in Data Acquisition systems to maintain high system accuracy in electrically noisy industrial environments.

It is possible to operate up to sixteen modules in parallel giving 64 input channels. However, it will be necessary to divide the select inputs into several groups to avoid overloading the decoder.

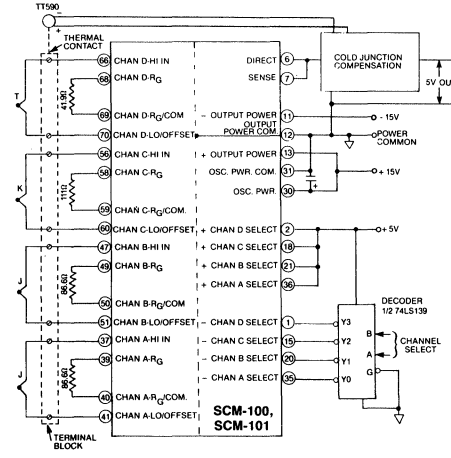
The above diagram shows the SCM-100/101 expanded to 32 channels. The CHANNEL SELECT inputs are driven in parallel from a single 74139 decoder. Module selection is achieved by driving the enable inputs with a 74138 decoder. All + channel select pins are tied to +5V.

EXTERNAL SYNCHRONIZATION

(see Tech Note 7)



THERMOCOUPLE TEMPERATURE MEASUREMENT



In this application, the SCM-100 is set up as a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the module. Various thermocouple types are used, and the gain adjust pots on each channel have been selected to take the standard ANSI range for each thermocouple to a 5V output span. A universal cold junction compensator is used to compensate for the temperature of the reference junction which is formed where the thermocouple leads are terminated.

ORDERING INFORMATION

MODEL

SCM-100A
SCM-100B
SCM-101

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SCM-103
Strain Gage Signal Conditioning Module

FEATURES

- **4-Channel operation**
- **±1 Microvolt/°C input offset drift**
- **±0.01% Maximum nonlinearity**
- **3000 Channels/second scanning speed**
- **Low cost**

GENERAL DESCRIPTION

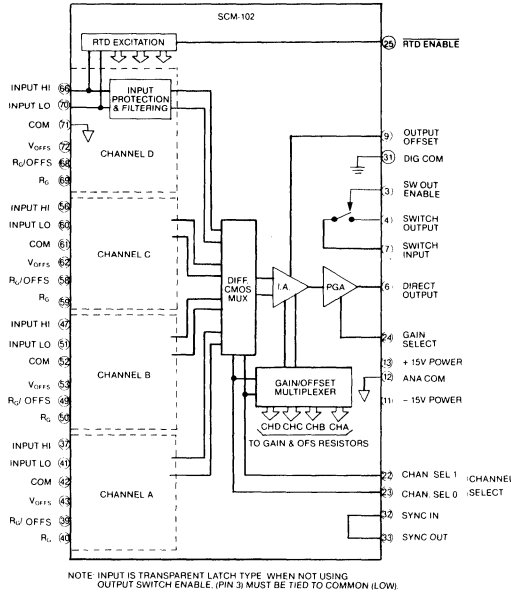
DATEL's SCM-103 is a low-cost, high performance signal conditioning module specifically designed to interface with strain gage sensors. The module is a functionally complete unit consisting of four individual input channels multiplexed into a single low-drift instrumentation amplifier which is followed by a digitally controlled, programmable gain amplifier output stage. Each channel includes an input protection and filtering circuit to preserve signal integrity in the presence of series mode 50/60 Hz noise.

The SCM-103 is designed to interface with strain gage sensors, and features an input span range of ±30 mV to ±100 mV and a minimum common mode rejection ratio of 94 dB.

The SCM-103 features a minimum channel scanning speed of 3000 channels/second, 100 MΩ input resistance and ±0.01% maximum nonlinearity. Total offset drift is ±1 microvolt/°C, output voltage swing is ±5V dc and the gain temperature coefficient is ±25 ppm/°C. Gain and channel selection is accomplished by applying the proper binary code to the gain or channel select inputs. User-selectable switched or direct outputs allow for the interconnection of multiple units when more than four channels are required.

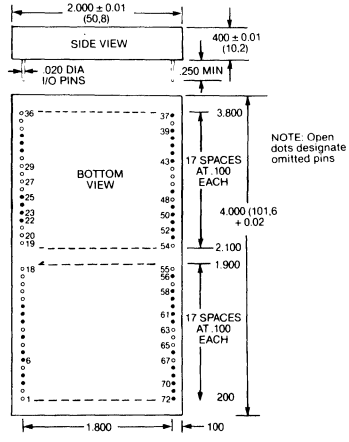
The low-cost, functionally complete multi-channel design makes it an ideal choice for applications involving multi-channel data acquisition systems, computer interface systems and industrial process measurement and control.

The device is packaged in a compact 2″ ×4″×0.4″ encapsulated module and operates over the industrial −25°C to +85°C temperature range.



NOTE: INPUT IS TRANSPARENT LATCH TYPE. WHEN NOT USING OUTPUT SWITCH ENABLE, (PIN 3) MUST BE TIED TO COMMON (LOW).

MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
3	SW D. OUTPUT ENABLE	43	CHAN A — Volt (+10V)
4	SWITCHED OUTPUT	47	CHAN B — INPUT HI
6	DIRECT OUTPUT	49	CHAN B — R_G/OFFSET
7	SWITCHED INPUT	50	CHAN B — R_G
9	OUTPUT OFFSET	51	CHAN B — INPUT LO
11	−15V POWER	52	CHAN B — COMMON
12	ANALOG COMMON	53	CHAN B — Volt (+10V)
13	+15V POWER	56	CHAN C — INPUT HI
22	CHANNEL SELECT 1	58	CHAN C — R_G/OFFSET
23	CHANNEL SELECT 0	59	CHAN C — R_G
24	GAIN SELECT	60	CHAN C — INPUT LO
25	RTD ENABLE	61	CHAN C — COMMON
31	DIGITAL COMMON	62	CHAN C — Volt (+10V)
32	SYNC IN	66	CHAN D — INPUT HI
33	SYNC OUT	68	CHAN D — R_G/OFFSET
37	CHAN A — INPUT HI	69	CHAN D — R_G
39	CHAN A — R_G/OFFSET	70	CHAN D — INPUT LO
40	CHAN A — R_G	71	CHAN D — COMMON
41	CHAN A — INPUT LO	72	CHAN D — Volt (+10V)
42	CHAN A — COMMON		

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc Supplies, unless otherwise noted.

INPUT CHARACTERISTICS	SCM-103
Number of Channels	4
Input Span Range	±30 mV and ±100 mV
Input Offset Voltage, Adj. to Zero	±150 μV
Channel-to-Channel Offset	±25 μV
Input Bias Current, max.	10 nA
Input Noise Voltage, 0.01 Hz to 100 Hz[1]	1.5 μV peak-to-peak
Common Mode Voltage Range	±6V
Common Mode Rejection Ratio, min.[2]	94 dB
Normal Mode Rejection, 60 Hz	24 dB
Max. Safe Differential Input	130V RMS
Input Resistance	>100 MΩ
Lead Resistance Effect	
OUTPUT CHARACTERISTICS	
Output Voltage Swing	±5V dc at 5 mA
Output Resistance;	
Direct Output	0.1Ω
Switched Output	35Ω, +0.5%/°C
Max. Switched Voltage	±10V dc[3]
PERFORMANCE	
Gain Range[5], R_G = 945Ω	166.6 V/V or 50 V/V
Gain Error, max., G = 50	±0.6%
G = 166.6	±0.8%
Gain Nonlinearity, max.	±0.01% of Span
Transfer Function	
Gain Tempco[6]	±25 ppm/°C
Input Offset Temp. Drift	±1 μV/°C
Total Offset Temp. Drift, RTI	±1 μV/°C
Channel Selection Time, max.[7]	300 μsec.
Channel Scanning Speed, min.	>3000 chan/sec.
Input Settling Time, to ±0.01% Full-Scale	0.4 sec.
Bandwidth	4 Hz
Sensor Excitation Level[8]	
Sensor Excitation Level Tempco	
Power Supply Rejection	±0.003%/%V_S
POWER REQUIREMENTS	
Analog Supply, Rated Value	±15V dc ±5%
Analog Supply Current, max.,	
+15V	+35 mA
−15V	−15 mA
PHYSICAL/ENVIRONMENTAL	
Specified Temperature Range	0°C to +70°C
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−55°C to +85°C
Case Size	2″ x 4″ x 0.4″ (50.8 x 101.6 x 10.2 mm)

FOOTNOTES:

1. R_S = 1 kΩ
2. R_S = 1 kΩ, f = 60 Hz
3. R_L = 2 kΩ
4. No load
5. Gain range may be expanded by use of an external amplifier. Expanded gain range for SCM-103 is 50 V/V to 1000 V/V.
6. Does not include effects of sensor excitation drift.
7. To 0.01% Full Scale.
8. Per channel.

1. Channel selection for the SCM-103 is accomplished by applying the proper binary code to the channel select inputs (Pins 22 and 23). Channels may be selected in any order, the only restriction being the 300 microsecond channel selection settling time.

Channel Select 1 (Pin 22)	Channel Select 0 (Pin 23)	Channel
0	0	A
0	1	B
1	0	C
1	1	D

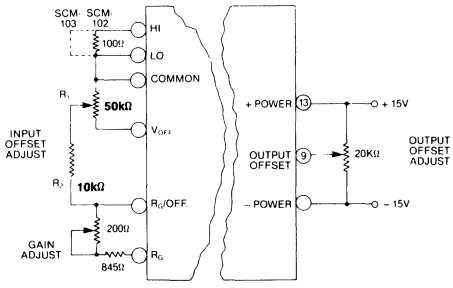
2. The SCM-103 is precalibrated to provide gains of 50 V/V and 166.6 V/V. Gain selection is accomplished by applying the appropriate binary code to the gain select input (Pin 24). A logic high applied to Pin 24 gives a gain of 50 V/V while a logic low gives a gain of 166.6 V/V. A 200Ω potentiometer connected in series with an 845Ω resistor across the R_G pins of each channel will provide ±3% full-scale span adjustment.

Gain Select (Pin 24)	Gain
0	166.6
1	50

3. The gain range of the SCM-103 may be expanded by the use of an external amplifier. A low-drift amplifier, such as DATEL's AM-427 should be used to maintain signal integrity.
4. All unused inputs should be shorted to common.

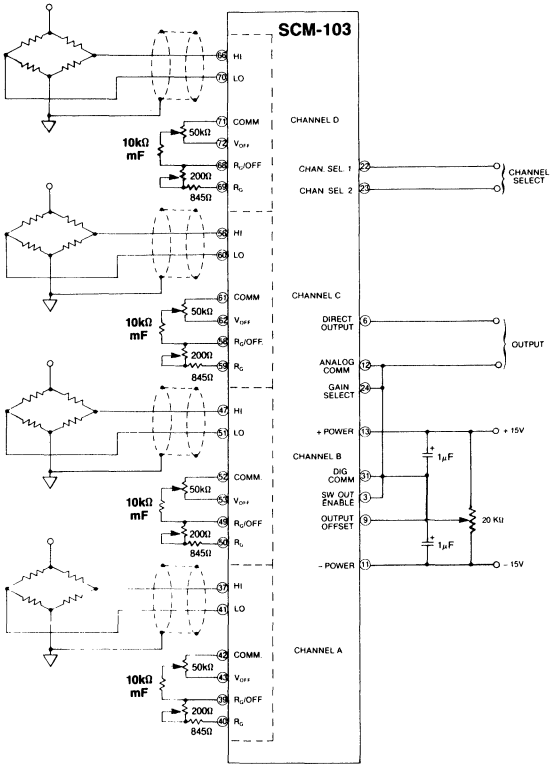
CONNECTION AND APPLICATION

SCM-103



For calibration of the SCM-103 these values should be changed as follows:

R_1–50kΩ } Resistors are metal film
R_2–10kΩ mF}



NOTE: 10kΩ resistors are metal film.

TYPICAL CONNECTION — SCM-103

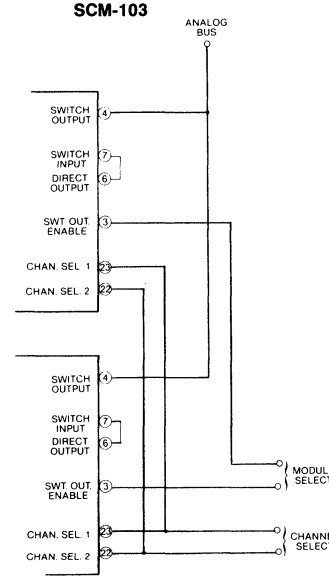
The SCM-103 is designed to interface with strain gage transducers. This diagram shows a four-channel strain gage input system with provision made for eliminating input offset and gain errors.

CALIBRATION

Each channel of the SCM-103 has a typical input offset (RTI) specification of only ±150 μV. While this is adequate for most applications, provision has been made for fine adjustment of the input offset (RTI) of each channel as well as the output offset (RTO) of the entire module.

To adjust the SCM-103, short the channel inputs (Pins 37, and 41 for channel A) to common and center the input offset potentiometer. The output offset is then adjusted for a null at the selected gain. The input offset adjustments of other channels may then be used to eliminate errors on subsequent channels that are selected.

SCM-103



CHANNEL EXPANSION

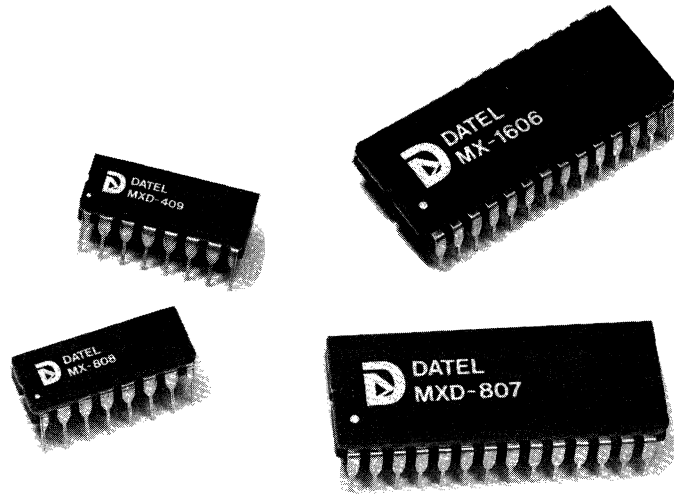
For applications where more than four channels ae required, multiple SCM-103's may be interconnected as shown. Channel address and $\overline{\text{ENABLE}}$ inputs (active low) are CMOS/TTL compatible with an input current of 100 μA each.

ORDERING INFORMATION

MODEL NO.	INPUT
SCM-103	Strain Gage

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ANALOG MULTIPLEXERS



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ANALOG MULTIPLEXERS

MODEL	CHANNELS	SETTLING TIME 20V to 0.01%	ACCESS TIME	INPUT VOLTAGE RANGE	PACKAGE	TEMPERATURE RANGE (°C)	FEATURES	PAGE
MV-808	8 Single Ended	2.8 µs	350 ns	±15V	16-pin DIP Monolithic	0 to +70	Low ON Resistance Dielectrically Isolated CMOS	5-3
MV-1606	16 Single Ended	2.4 µs	300 ns	±15V	28-pin DIP Monolithic	0 to +70		5-3
MV-1606M						-55 to +125		
MVD-409	4 Differential	2.8 µs	350 ns	±15V	16-pin DIP Monolithic	0 to +70		5-3
MVD-807	8 Differential	2.4 µs	300 ns	±15V	28-pin DIP Monolithic	0 to +70		5-3
MX-808	8 Single Ended	3 µs	500 ns	±15V	16-pin DIP Monolithic	0 to +70	Overvoltage Protected	5-11
MX-818C	8 Single Ended or 4 Differential	800 ns	125 ns	±15V	18-pin DIP Monolithic	0 to +70	High Speed	5-11
MX-818M						-55 to +125		
MX-1606	16 Single Ended	3 µs	500 ns	±15V	28-pin DIP Monolithic	0 to +70	Overvoltage Protected	5-11
MX-1606M						-55 to +125		
MX-1616C	16 Single Ended or 8 Differential	800 ns	150 ns	±15V	28-pin DIP Monolithic	0 to +70	High Speed	5-11
MX-1616MC						-55 to +125		
MXD-409	4 Differential	3 µs	500 ns	±15V	16-pin DIP Monolithic	0 to +70	Overvoltage Protected	5-7
MXD-807	8 Differential	3 µs	500 ns	±15V	28-pin DIP Monolithic	0 to +70		5-7

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

MV Series
Low ON-Resistance
CMOS Analog Multiplexers

FEATURES

- **Low "ON" resistance**
- **Break-before-make switching**
- **Dielectrically isolated CMOS**
- **Single-ended or differential**
- **Fast settling time**
- **DTL/TTL/CMOS-compatible**

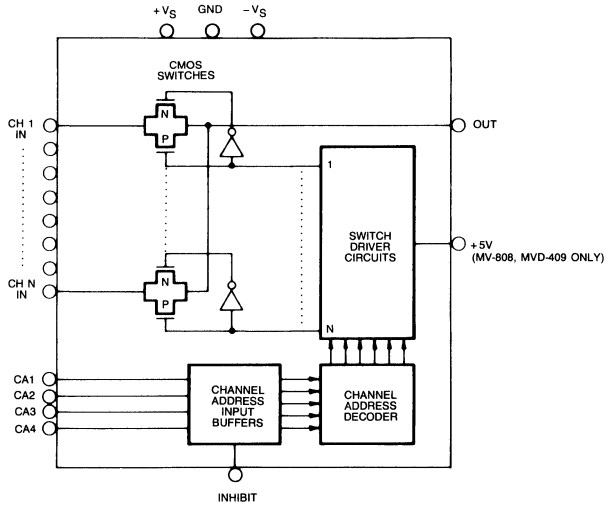
GENERAL DESCRIPTION

The MV series analog multiplexers are 4-, 8-, and 16-channel monolithic devices featuring a low ON resistance of 270 ohms. These units are manufactured with CMOS technology using a dielectric isolation process. There are 8- and 16-channel single-ended models and 4- and 8-channel differential models in this series. Channel addressing is done by a 2-, 3-, or 4-bit binary code; an inhibit input enables or disables the entire device to permit expansion of the number of channels by using several devices together. Another important feature is break-before-make switching, which insures that no two channels are ever momentarily shorted together.

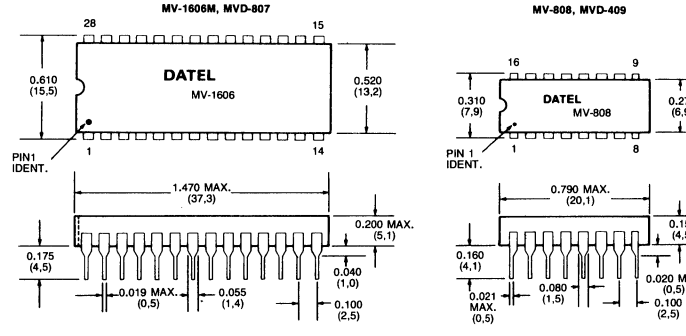
With a high impedance load, transfer accuracies of 0.01% can be achieved at channel sampling rates up to 350 kHz. These multiplexers are ideal for multichannel data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. The channel ON resistance is less than 500 ohms over full operating temperature range.

These multiplexers are packaged in 16-pin and 28-pin ceramic DIP's. Standard versions operate over 0 to +70°C while the MV-1606M operates from −55°C to +125°C. The MV series is similar in specification to DATEL's MX series multiplexers. The MX series is recommended where input over-voltage protection to 20 volts above supply voltage is required and where higher channel ON resistance can be tolerated.

CAUTION:
These multiplexers are CMOS devices and should be handled with anti-static precautions until installed in a circuit with leakage return paths.



MECHANICAL DIMENSIONS INCHES (MM)



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ABSOLUTE MAXIMUM RATINGS	MV-808 MV-808M	MV-1606 MV-1606M	MVD-409 MVD-409M	MVD-807 MVD-807M
Power Supply, analog	±20V	±20V	±20V	±20V
Power Supply, digital	+30V	—	+30V	—
Analog Input Voltage	±|Vs+2V|	±|Vs+2V|	±|Vs+2V|	±|Vs+2V|
Digital Input Voltage	±Vs	±|Vs+4V|	±Vs	±|Vs+4V|
Package Dissipation, maximum	780mW	1200mW	780mW	1200mW

FUNCTIONAL SPECIFICATIONS

Typical at +15V supplies (and +5V supply for MV-808 & MVD-409), unless otherwise noted.

ANALOG INPUTS				
Number of Channels	8	16	4	8
Type	Single Ended	Single Ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance[1]	250Ω	270Ω	250Ω	270Ω
Channel ON Resistance[2], maximum over temp.	500Ω	500Ω	500Ω	500Ω
Channel OFF Input Leakage	20 pA	30 pA	20 pA	30 pA
Channel OFF Output Leakage	100 pA	1.0 nA	50 pA	1.0 nA
Channel ON Leakage	100 pA	1.0 nA	50 pA	1.0 nA
Channel OFF Input Capacitance	4 pF	4 pF	4 pF	4 pF
Channel Off Output Capacitance	20 pF	44 pF	10 pF	22 pF
DIGITAL INPUTS[3]				
Logic "0" Threshold, maximum	+0.4V	+0.8V	+0.4V	+0.8V
Logic "1" Threshold,[4] minimum	+4.0V	+2.4V	+4.0V	+2.4V
Input Current, maximum, High or Low	1μA	5μA	1μA	5μA
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, all channels OFF	Logic "1"	Logic "0"	Logic "1"	Logic "0"
PERFORMANCE				
Transfer Error, maximum	0.01%	0.01%	0.01%	0.01%
Crosstalk, 10kHz	−86 dB	−86 dB	−86 dB	−86 dB
Common Mode Rejection	—	—	120 dB	120 dB
Settling Time, 20V to 0.1%	1.1 μsec.	1.2 μsec.	1.1 μsec.	1.2 μsec.
Settling Time, 20V to 0.01%	2.8 μsec.	2.4 μsec.	2.8 μsec.	2.4 μsec.
Turn ON Time	350 nsec.	300 nsec.	350 nsec.	300 nsec.
Turn OFF Time	250 nsec.	220 nsec.	250 nsec.	220 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break-Before-Make Delay	100 nsec.	80 nsec.	100 nsec.	80 nsec.
POWER REQUIREMENTS				
Power Supply Voltage	±15V dc	±15V dc	±15V dc	±15V dc
Power Supply Current,[5] maximum	+1, −2 mA	+5, −2 mA	+1, −2 mA	+5, −2 mA
Digital Supply Voltage	+5V dc	—	+5V dc	—
Digital Supply Current, maximum	2 mA	—	2 mA	—
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, standard version	0 to +70°C	0 to +70°C	0 to +70°C	0 to +70°C
Operating Temperature Range, military, version		−55° to +125°C		
Storage Temperature Range	−65° to +150°C	−65° to +150°C	−65° to +150°C	−65° to +150°C
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP

FOOTNOTES:

1. For MV-1606M typical value is 170 ohms.
2. For MV-1606M maximum value is 400 ohms.
3. Channel address and inhibit inputs.
4. For MV-808 and MVD-409; to drive from DTL/TTL logic 1K pull-up resistors to +5V should be used.
5. For MV-1606M maximum current is +3, −1 mA.

CONNECTION AND APPLICATION

CHANNEL ADDRESSING

MV-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MV-808, MVD-807

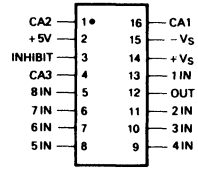
4	2	1	MVD-807 INHIB.	MV-808 INHIB.	ON CHANNEL
X	X	X	0	1	NONE
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8

MVD-409

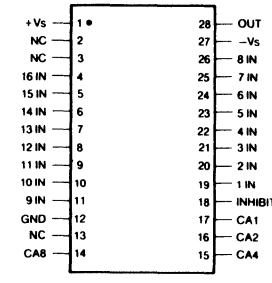
2	1	INHIB.	ON CHANNEL
X	X	1	NONE
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

PIN CONNECTIONS

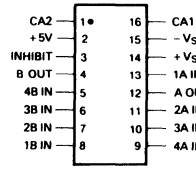
MV-808



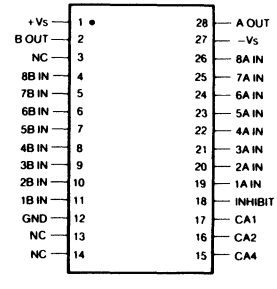
MV-1606



MVD-409



MVD-807



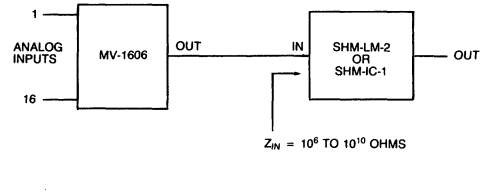
NOTES:
CA = CHANNEL ADDRESS
Vs = SUPPLY VOLTAGE
NC = NO CONNECTIONS

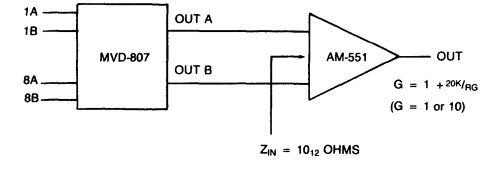
TOP VIEW SHOWN

TECHNICAL NOTES

1. The transfer accuracy of the MV series multiplexers depends on both the source resistance and load resistance. For example, with zero source resistance and assuming 500 ohms maximum channel ON resistance, the load impedance must be at least 5 megohms to achieve 0.01% accuracy. In practice it is recommended that a load impedance of 10^8 ohms or more be used. This is a typical input impedance value for most IC operational amplifiers connected in the follower mode (see DATEL's AM-400 series) or for IC sample-holds (see DATEL's SHM-1C-1, SHM-LM-2, or SHM-20). Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 250 ohms is recommended.
2. For differential operation, either two unity gain buffers or an instrumentation amplifier (such as DATEL's AM-551) is recommended as the output load. To maintain high CMR, source impedance unbalance must be kept to a minimum, and amplifiers with high CMR should be used.
3. The maximum analog input overvoltage for the MV series is $\pm|Vs+2V|$. The maximum digital input voltage is $\pm Vs$. It should be noted that the logic (channel address) inputs are protected with resistors and clamp diodes but the analog inputs are not. Because the analog inputs are not protected, the low ON resistance is achieved.
4. Channel expansion is accomplished by use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.
5. For the MV-808 and MVD-409 it is recommended that 1K pull-up resistors to the +5V logic supply be used when the logic inputs are driven from DTL or TTL circuits. Only these two models require a +5V logic supply.

CIRCUIT CONNECTIONS





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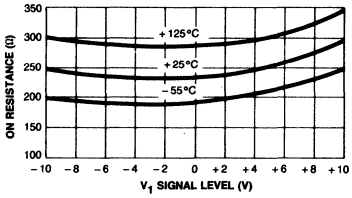
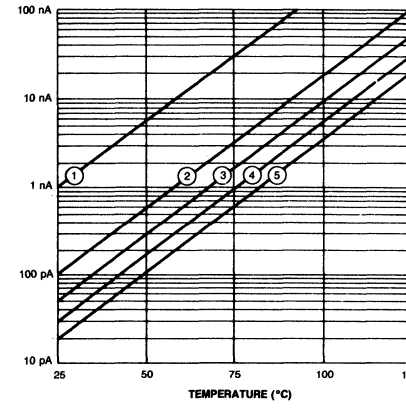
PERFORMANCE GRAPHS

ON RESISTANCE VS. TEMPERATURE

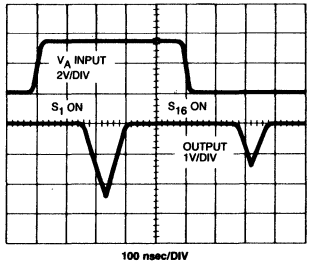


LEAKAGE CURRENT VS. TEMPERATURE

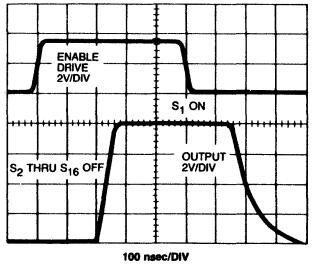


① MV-1606, MVD-807 CHANNEL OFF OUTPUT LEAKAGE
② MV-808 CHANNEL OFF OUTPUT LEAKAGE
③ MVD-409 CHANNEL OFF INPUT LEAKAGE
④ MV-1606, MVD-807 CHANNEL OFF INPUT LEAKAGE
⑤ MV-808, MVD-409 CHANNEL OFF INPUT LEAKAGE

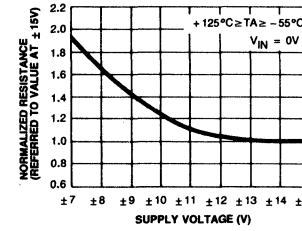
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



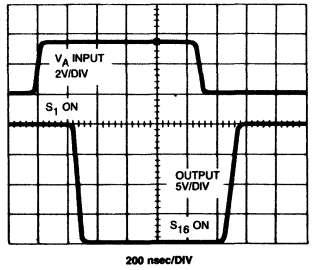
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



ACCESS TIME



ORDERING INFORMATION

MODEL NO.	CHANNELS	OPERATING TEMP. RANGE
MV-808	8 S.E.	0 to 70°C
MV-1606	16 S.E.	0 to 70°C
MV-1606M	16 S.E.	–55 to +125°C
MVD-409	4 Diff.	0 to 70°C
MVD-807	8 Diff.	0 to 70°C

MX Series
4-, 8-, and 16-Channel CMOS Multiplexers

FEATURES

- **Dielectrically isolated CMOS**
- **Break-before-make switching**
- **Single-ended and differential**
- **Overvoltage protection**
- **DTL/TTL/CMOS-compatible**
- **7.5 mW Standby power**

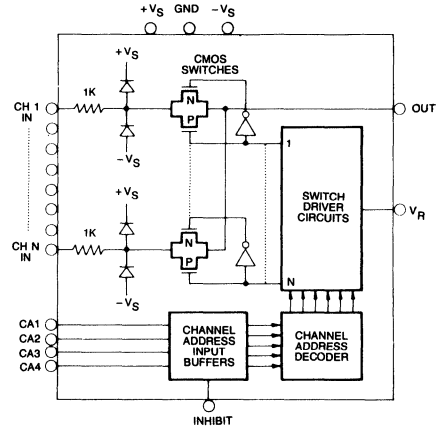
GENERAL DESCRIPTION

The MX series analog multiplexers are 4-, 8-, and 16-channel monolithic devices manufactured with a dielectrically isolated complementary MOS process. The circuits incorporate analog and digital input protection which protects the units from both overvoltage and loss of power. The digital inputs are DTL/TTL/CMOS compatible and address the proper channel by means of a 2-, 3-, or 4-bit binary code. An inhibit input enables or disables the entire device and thus permits expansion of the number of channels by using several devices together. Another important feature of these multiplexers is the use of break-before-make switching to insure that no two channels are ever momentarily shorted together.

Transfer accuracies of 0.01% can be achieved at channel sampling rates up to 200 kHz and over ±10V signal ranges. These multiplexers are ideal for multichannel data acquisition systems where the multiplexer operates into a high-impedance load such as a sample-hold, buffer amplifier, or instrumentation amplifier. Channel ON resistance is typically 1.5K at +25°C and is less than 2K over the operating temperature range.

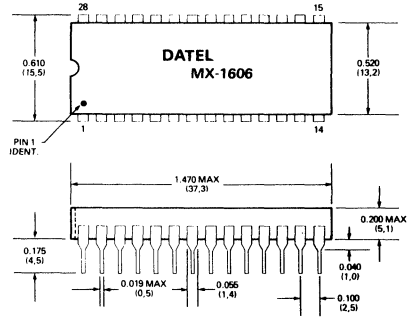
Power consumption is only 7.5 mW at standby and 15 mW at 100 kHz switching rate. Power supply range is ±5V to ±20V. The devices are packaged in 16 pin or 28 pin DIP's and operate over the 0°C to +70°C temperature range.

CAUTION: These are CMOS devices and may be damaged by static discharge. Standard anti-static precautions should be taken to prevent possible damage.

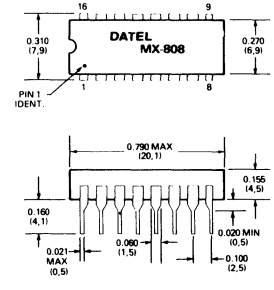


MECHANICAL DIMENSIONS — INCHES (MM)

MX-1606, MXD-807



MX-808, MXD-409



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ABSOLUTE MAXIMUM RATINGS	MX-808	MX-1606	MXD-409	MXD-807
Voltage Between Supply Pins	40V	40V	40V	40V
V_{REF} to Ground, V+ to Ground	+20V	+20V	+20V	+20V
Digital Input Overvoltage	±[V_S +4V]	±[V_S +4V]	±[V_S +4V]	±[V_S +4V]
Analog Input Overvoltage	±[V_S +20V]	±[V_S +20V]	±[V_S +20V]	±[V_S +20V]
Package Dissipation, maximum	725 mW	1200 mW	725 mW	1200 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies, R source <1K, unless otherwise noted.

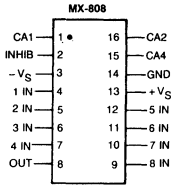
ANALOG INPUTS	MX-808	MX-1606	MXD-409	MXD-807
Number/Type of Channels	8 Single-ended	16 Single-ended	4 Differential	8 Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance	1.5 KΩ	1.5 KΩ	1.5 KΩ	1.5 KΩ
Channel ON Resistance, Over Temp	2.0 KΩ, maximum	2.0 KΩ, maximum	2.0 KΩ, maximum	2.0 KΩ, maximum
Channel OFF Input Leakage	30 pA	30 pA	30 pA	30 pA
Channel OFF Output Leakage	1.0 nA	1.0 nA	1.0 nA	1.0 nA
Channel ON Leakage	100 pA	100 pA	100 pA	100 pA
Channel OFF Input Capacitance	5 pF	5 pF	5 pF	5 pF
Channel OFF Output Capacitance	25 pF	50 pF	12 pF	25 pF
DIGITAL INPUTS[1]				
Logic "0" Threshold	+0.8V, maximum	+0.8V, maximum	+0.8V, maximum	+0.8V, maximum
Logic "1" Threshold, (TTL)[2]	+4.0V, minimum	+4.0V, minimum	+4.0V, minimum	+4.0V, minimum
Logic "1" Threshold, (CMOS)[3]	+6.0V, minimum	+6.0V, minimum	—	—
Input Current, High or Low	5 μA, maximum	5 μA, maximum	5 μA, maximum	5 μA, maximum
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, All Channels OFF	Logic "0"	Logic "0"	Logic "0"	Logic "0"
PERFORMANCE				
Transfer Error, maximum	0.01%	0.01%	0.01%	0.01%
Crosstalk, 1 kHz	0.005%	0.005%	0.005%	0.005%
Common Mode Rejection	—	—	120 dB	120 dB
Settling Time[4], 20V step to 0.1%	2 μsec.	2 μsec.	2 μsec.	2 μsec.
Settling Time[4], 20V step to 0.01%	3 μsec.	3 μsec.	3 μsec.	3 μsec.
Turn ON Time	500 nsec.	500 nsec.	500 nsec.	500 nsec.
Turn OFF Time	300 nsec.	300 nsec.	300 nsec.	300 nsec.
Break Before Make Delay	80 nsec.	80 nsec.	80 nsec.	80 nsec.
Inhibit/Enable Delay	300 nsec.	300 nsec.	300 nsec.	300 nsec.
POWER REQUIREMENTS				
Rated Power Supply Voltage	±15V dc	±15V dc	±15V dc	15V dc
Power Supply Voltage Range	±5V to ±20V	±5V to ±20V	±5V to ±20V	±5V to ±20V
Quiescent Current, maximum	+5, −2 mA	+5, −2 mA	+5, −2 mA	+5, −2 mA
Power Consumption, 10 kHz Sampling	7.5 mW	7.5 mW	7.5 mW	7.5 mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Standard Models	0°C to +70°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Package	16 Pin DIP	28 Pin DIP	16 Pin DIP	28 Pin DIP

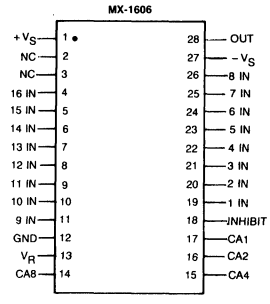
FOOTNOTES:

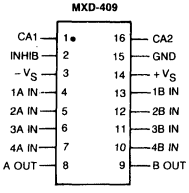
1. The digital inputs are the channel address inputs and the inhibit input.
2. To drive from DTL/TTL circuits, 1K pull-resistors to +5V are recommended. With models MX-1606 and MXD-807, pin 13 should be left open.
3. For a +6.0V threshold with models MX-1606 and MXD-807, pin 13 is connected to +10V.
4. With a load impedance of >100 megohms in parallel with 2 pF.

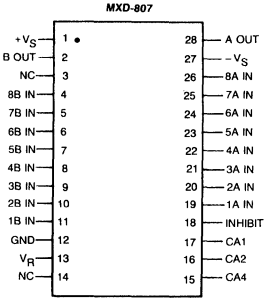
CONNECTION & APPLICATION

PIN CONNECTIONS









NOTES:

NOTES:
CA CHANNEL ADDRESS
VS SUPPLY VOLTAGE
VR REFERENCE VOLTAGE
NC NO CONNECTIONS

CHANNEL ADDRESSING

MX-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MX-808, MXD-807

4	2	1	INHIB.	ON CHANNEL
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

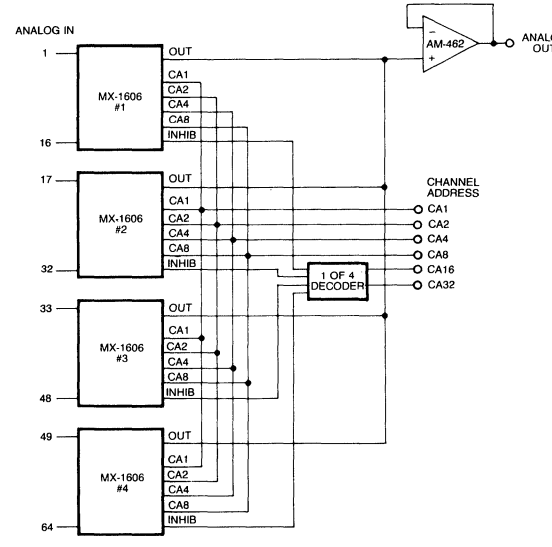
MXD-409

2	1	INHIB.	ON CHANNEL
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

TECHNICAL NOTES

1. The transfer accuracy of these multiplexers depends on both the source resistance and the load resistance. With zero source resistance, and assuming 2K ohms maximum channel ON resistance, the load impedance should be at least 20 megohms to achieve 0.01% accuracy. In practice, it is recommended that a load impedance of at least 100 megohms be used to minimize errors. This can be done by using a good high-gain, high-CMR operational amplifier as a buffer (such as DATEL's AM-462). Source resistance should be kept as low as possible so that accuracy is not affected; less than 1K ohms is recommended. Higher source resistance, in addition to affecting accuracy, will degrade the settling time of the multiplexer.
2. For differential operation, two buffer amplifiers or a good quality instrumentation amplifier (such as DATEL's AM-201) should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used, and an amplifier with high CMR should be chosen.
3. The maximum analog input overvoltage for these models is ±[Vs +20V]. Maximum logic input overvoltage is ±[Vs +4V].
4. Channel expansion is accomplished using the inhibit input of the multiplexer. A logic "0" on this input disables the multiplexer. The expansion technique shown in the diagram applies to all of the multiplexer models.
5. The reference terminal (V_R) sets the noise immunity level of the input logic for models MX-1606 and MXD-807. In most cases this terminal is left open (TTL inputs). For higher level inputs (+6V minimum), this terminal should be connected to +10V dc. When addressing from DTL/TTL logic, use 1K ohm pull-up resistors to the +5V dc supply.

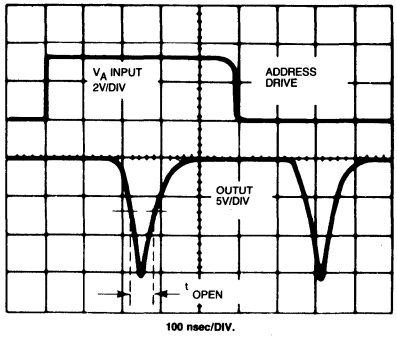
EXPANSION TO 64 CHANNELS



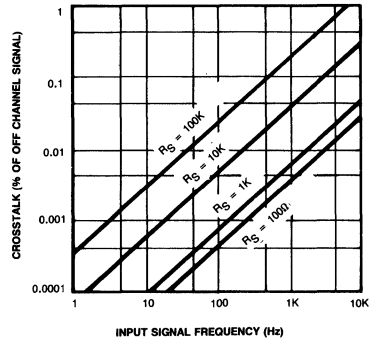
5

PERFORMANCE GRAPHS

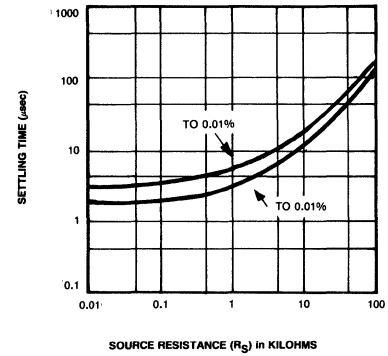
BREAK-BEFORE-MAKE DELAY (t OPEN)



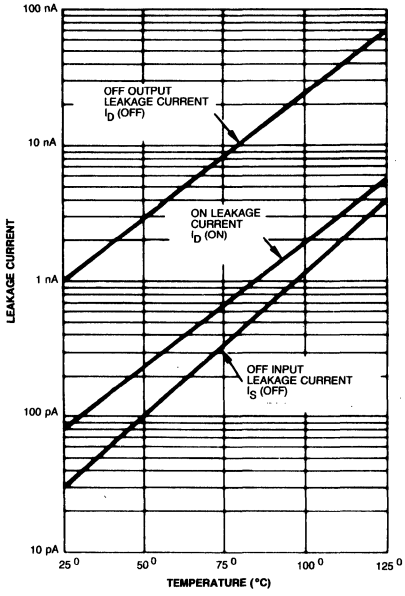
CROSSTALK VS. FREQUENCY OF INPUT SIGNAL



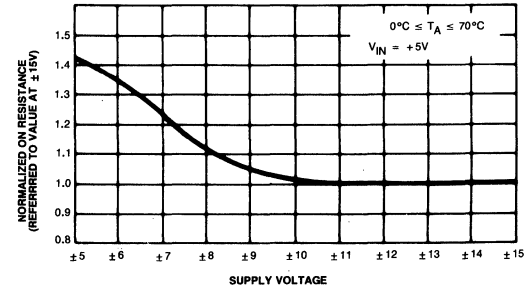
SETTLING TIME VS. SOURCE RESISTANCE (20V STEP)



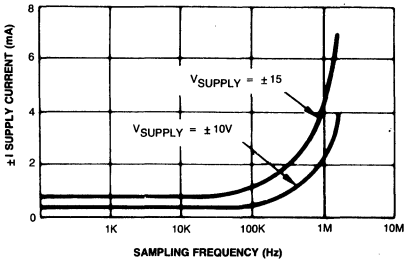
LEAKAGE CURRENT VS. TEMP.



NORMALIZED ON RESISTANCE VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. SAMPLING FREQUENCY



ORDERING INFORMATION

MODEL NO.	CHANNELS	OPERATING TEMP. RANGE
MX-808	8 S.E.	0°C to +70°C
MX-1606	16 S.E.	0°C to +70°C
MXD-409	4 Diff.	0°C to +70°C
MXD-807	8 Diff.	0°C to +70°C

MX-1616, MX-818
High-Speed CMOS
Analog Multiplexers

FEATURES

- **800 Nanoseconds settling time**
- **Programmable input mode**
- **Break-before-make switching**
- **Dielectrically isolated CMOS**
- **TTL/CMOS-compatible**

GENERAL DESCRIPTION

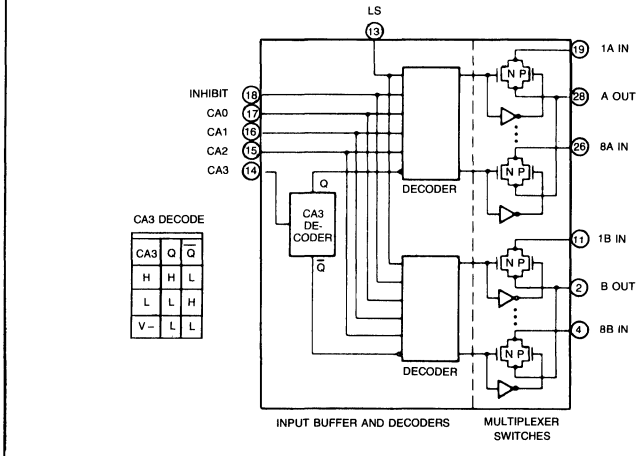
The MX-1616 and MX-818 are high-speed, high performance analog multiplexers manufactured with a dielectrically isolated CMOS process. Both devices achieve transfer accuracies of 0.01% at channel sampling rates of up to 1.25 MHz over ±10V signal ranges. These multiplexers are ideal for high-speed, multi-channel, data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier or instrumentation amplifier. Channel ON resistance is 750Ω maximum at +25°C and only 1KΩ maximum over the full operating temperature range. The channel OFF Output Leakage current is typically only 35 pA for the MX-1616 and 100 pA for the MX-818.

A unique feature of these circuits is the ability of the user to program their inputs for either single-ended or differential operation. The MX-1616 is user programmable either as a single ended 16-channel or as a differential 8-channel multiplexer while the MX-818 is user programmable either as a single-ended 8-channel or as a differential 4-channel multiplexer.

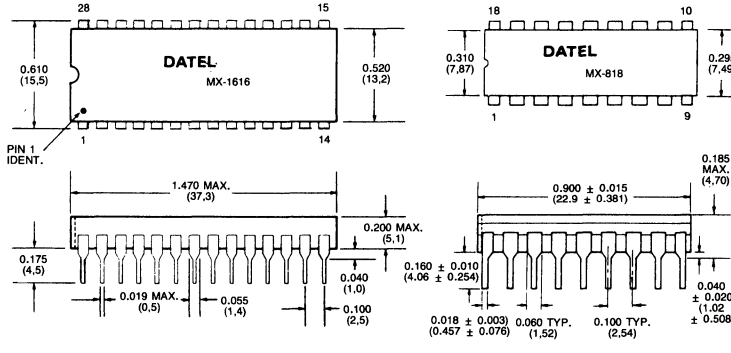
Digital inputs are user selectable for either TTL or CMOS compatibility. The proper channel is addressed by means of a 3- or 4-bit binary word. An inhibit function enables or disables the entire device, permitting expansion of the number of channels by using several devices together. Another important feature of these devices is the use of break-before-make switching to insure that no two channels are ever momentarily shorted together.

These multiplexers are packaged in 18-pin and 28-pin ceramic DIP's. Commercial versions operate over the 0°C to +70°C operating temperature range.

CAUTION: These multiplexers are CMOS devices and should be handled with anti-static precautions until installed in a circuit with anti-static return paths.



MECHANICAL DIMENSIONS
INCHES (MM)



5

ABSOLUTE MAXIMUM RATINGS	MX-1616	MX-818
Voltage Between Supply Pins	33V	*
Analog Input Voltage	$\pm(V_S + 2V)$	*
Digital Input Voltage:		
TTL[1]	CA3 = $(-V_S - 2V)$ < Logic "1" < +6V	CA2 = $(-V_S - 2V)$
CMOS[2]	$+V_S + 2V$	*
	GRND −2V	*
Package Dissipation, maximum	1200 mW	725 mW

PHYSICAL/ENVIRONMENTAL	MX-1616	MX-818
Operating Temp. Range:		
C Suffix	0°C to +70°C	*
		*
Storage Temperature Range	−65°C to +155°C	*
Package	28-Pin DIP	18 Pin DIP

* Same specification as column 1.

FOOTNOTES:

1. For TTL compatibility, the Logic Select pin (MX-1616 Pin 13, MX-818 Pin 8) is grounded or left open.
2. For CMOS compatibility, the Logic Select Pin (MX-1616 Pin 13, MX-818 Pin 8) is tied to the system Logic Supply.
3. Vin = ±10V, Iout = −100 µA.
4. 200 nseconds maximum at full rated operating temperature.
5. 150 nseconds maximum at full rated operating temperature.

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, unless otherwise noted.

ANALOG INPUTS	MX-1616	MX-818
No. of Channels	16 Single-Ended 8 Differential	8 Single-Ended 4 Differential
Input Voltage Range	±15V	*
Channel ON Resistance, maximum[3]	750Ω	*
Channel ON Res. over Temp., maximum[3]	1 KΩ	*
Channel OFF Input Leakage	10 pA	50 pA
Channel OFF Output Leakage	35 pA	100 pA
Channel ON Leakage	40 pA	100 pA
Channel OFF Input Capacitance	2.5 pF	1.9 pF
Channel OFF Output Capacitance	18 pF	10 pF
DIGITAL INPUTS		
Logic "0" Threshold, maximum: TTL	+0.8V	*
CMOS	+0.3V	*
Logic "1" Threshold, minimum: TTL	+2.4V	*
CMOS	0.7 (Logic sup.)	*
Input Leakage Current, maximum: High	1 µA	*
Low	25 µA	20 µA
Channel Address Coding	4 Bits	3 Bits
Channel Inhibit, All Channels OFF	Logic "0"	*
PERFORMANCE		
Transfer Error, maximum	0.01%	*
Settling Time, 10V step to 0.1%	250 nsec.	*
10V step to 0.01%	800 nsec.	*
Access Time, maximum	150 nsec.[4]	125 nsec.[5]
Enable Delay "ON", maximum	150 nsec.	*
Enable Delay "OFF", maximum	125 nsec.	*
Break Before Make Delay	20 nsec.	*
POWER REQUIREMENTS		
Rated Power Supply Voltage	±15V	*
Quiescent Current maximum	±30 mA	±18 mA
Power Dissipation, maximum	900 mW	540 mW

TECHNICAL NOTES

1. The transfer accuracy of the MX-1616 and MX-818 depends upon both the source and the load resistance. With zero source resistance and assuming 1 KΩ maximum channel on resistance the load impedance must be at least 10MΩ to achieve 0.01% accuracy. This can be done by using a good high gain, high CMR operational amplifier as a buffer (such as DATEL's AM-410). Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 500Ω is recommended.
2. For differential operation, two buffer amplifiers or a good instrumentation amplifier (such as DATEL's AM-551) should be used. To maintain high CMR, source impedance unbalance should be kept to a minimum, the highest possible load impedance should be used and an amplifier with high CMR should be chosen.
3. These devices have the added feature of being programmable for single-ended or differential operation. The MX-1616 is user programmed for single-ended 16-channel operation by connecting A out (Pin 28) to B out (Pin 2) and using CA3 (Pin 14) as a digital address input. To program the MX-1616 for differential 8-channel operation, CA3 (Pin 14) is simply connected to $-V_S$ (Pin 27). The MX-818 may be programmed as a single-ended 8-channel multiplexer by connecting Aout (Pin 18) to Bout (Pin 2) and using CA2 (Pin 9) as a digital input address, or as a differential 4-channel multiplexer by connecting CA2 (Pin 9) to $-V_S$ (Pin 17). Refer to the truth tables for channel addressing information.
4. Both devices are selectable for either TTL or CMOS compatibility. For TTL compatibility, the Logic Select Pin (MX-1616 Pin 13, MX-818 Pin 8) is left open or grounded. For CMOS compatibility, the Logic Select Pin should be connected to the system Logic Supply.
5. Channel expansion is accomplished by the use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

CONNECTION & APPLICATION

MX-1616 - USED AS 16 CHANNEL MULTIPLEXER

USE CA3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
3	2	1	0	INHIB.	OUPUT A	OUTPUT B
X	X	X	X	0	NONE	NONE
0	0	0	0	1	1A	____
0	0	0	1	1	2A	____
0	0	1	0	1	3A	____
0	0	1	1	1	4A	____
0	1	0	0	1	5A	____
0	1	0	1	1	6A	____
0	1	1	0	1	7A	____
0	1	1	1	1	8A	____
1	0	0	0	1	____	1B
1	0	0	1	1	____	2B
1	0	1	0	1	____	3B
1	0	1	1	1	____	4B
1	1	0	0	1	____	5B
1	1	0	1	1	____	6B
1	1	1	0	1	____	7B
1	1	1	1	1	____	8B

MX-1616 - USED AS DUAL 8 CHANNEL MULTIPLEXER

CONNECT CA3 TO −V SUPPLY				ON CHANNEL TO	
2	1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	X	0	NONE	NONE
0	0	0	1	1A	1B
0	0	1	1	2A	2B
0	1	0	1	3A	3B
0	1	1	1	4A	4B
1	0	0	1	5A	5B
1	0	1	1	6A	6B
1	1	0	1	7A	7B
1	1	1	1	8A	8B

MX-818 - USED AS 8 CHANNEL MULTIPLEXER

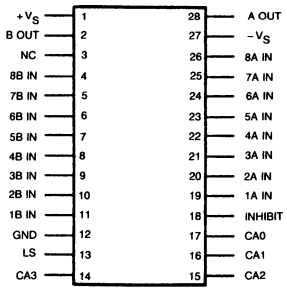
USE CA2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
2	1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	X	0	NONE	NONE
0	0	0	1	1A	____
0	0	1	1	2A	____
0	1	0	1	3A	____
0	1	1	1	4A	____
1	0	0	1	____	1 B
1	0	1	1	____	2 B
1	1	0	1	____	3 B
1	1	1	1	____	4 B

MX-818 - USED AS DUAL 4 CHANNEL MULTIPLEXER

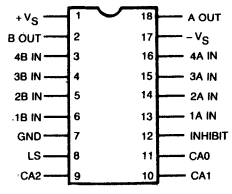
CONNECT CA2 TO −V SUPPLY			ON CHANNEL TO	
1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	0	NONE	NONE
0	0	1	1	1B
0	1	1	2	2B
1	0	1	3	3B
1	1	1	4	4B

PIN CONNECTIONS

MX-1616

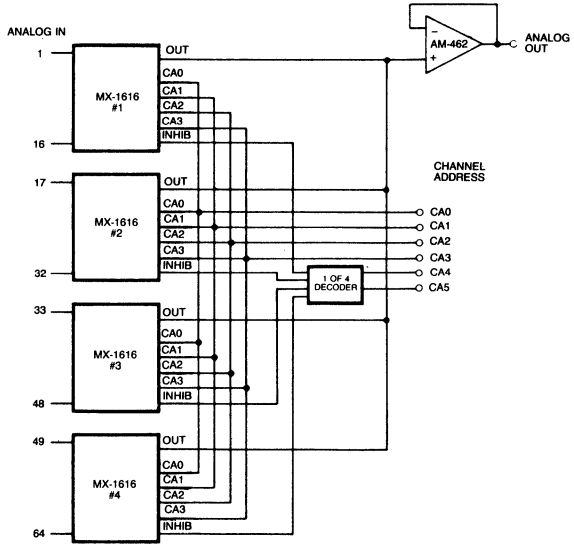


MX-818

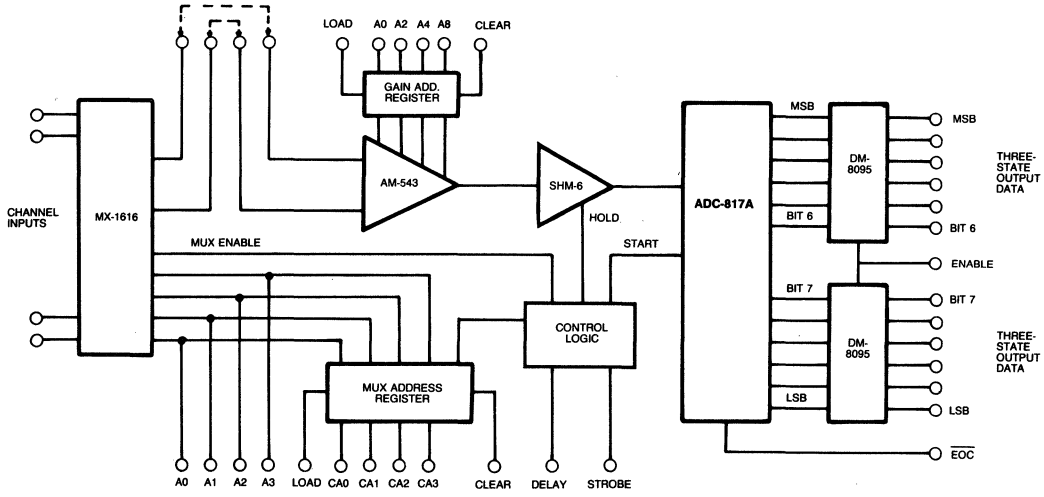


NOTES:
CA CHANNEL ADDRESS
VS SUPPLY VOLTAGE
LS LOGIC SELECT
NC NO CONNECTION

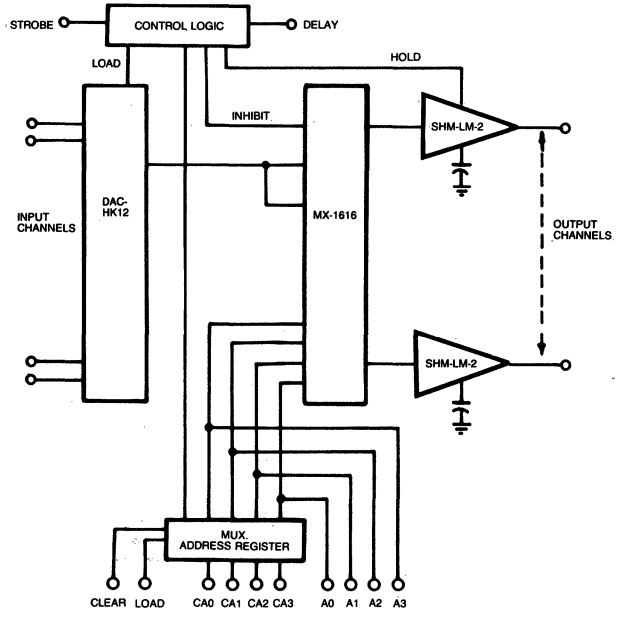
EXPANSION TO 64 CHANNELS



APPLICATION



NOTE: This application diagram shows a high-speed data acquisition system with 8 differential inputs and 12-bit resolution that utilizes the MX-1616. If the control logic is timed so that the sample-hold-A/D section is converting one analog value while the mux-amplifier section is allowed to settle to the next input value, throughput rates greater than 156 KHz can be achieved. The MX-1616 is used with Datel's AM-543, a high speed digitally programmable gain amplifier, the ADC-817A, a 12-bit hybrid A/D with a 2 microsecond conversion rate, and the SHM-6, a 0.01%, 1 microsecond hybrid sample-hold.

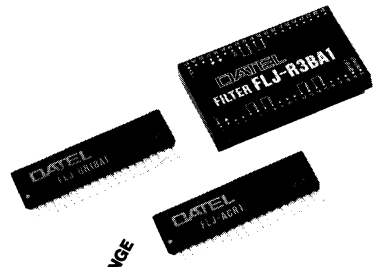


NOTE: The switches in a CMOS multiplexer will conduct equally well in either direction, making it feasible to use them as single input-selected multiple output switches. The circuit shown is capable of sample rates of 78 KHz for inputs of ±10V. The MX-1616 is used with Datel's DAC-HK12, a 12 bit hybrid D/A with input registers and the SHM-LM-2, a low cost monolithic sample-hold.

ORDERING INFORMATION

MODEL NO.	CHANNELS	OPERATING TEMP. RANGE
MX-818C	8 S.E. or 4 Diff.	0 to +70°C
MX-1616C	16 S.E. or 8 Diff.	0 to +70°C

ACTIVE FILTERS



MODEL	NO. OF POLES	BUTTERWORTH	BESSEL	ELLIPTICAL	LOW PASS	HIGH PASS	BAND PASS	BAND REJECT	RESISTOR TUNING	DIGITAL TUNING	VOLTAGE TUNING	ACCURACY	FREQUENCY RANGE	PAGE
FLJ-DC	2	•	•	•	•	•	•			•		0.1%	Note 1	6-11
FLJ-D1	2	•			•	•	•			•		0.1%	1–1.6 kHz	6-11
FLJ-D2	2	•			•	•	•			•		0.1%	100–160 kHz	6-11
FLJ-D5LA1	5			•	•					•		3%	10 Hz–2 kHz	6-23
FLJ-D5LA2	5			•		•				•		3%	100 Hz–20 kHz	6-23
FLJ-D6LA1	6			•	•					•		3%	10 Hz–2 kHz	6-23
FLJ-D6LA2	6			•		•				•		3%	100 Hz–20 kHz	6-23
FLJ-R3BA1	3					•			•			2	10 Hz–2 kHz	6-25
FLJ-R3BA2	3					•			•			2	100 Hz–20 kHz	6-25
FLJ-R8LA1	8			•	•				•			2	10 Hz–2 kHz	6-25
FLJ-R8LA2	8			•	•				•			2	100 Hz–20 kHz	6-25
FLJ-R8LB1	8			•					•			2	10 Hz–2 kHz	6-25
FLJ-R8LB2	8			•					•			2	100 Hz–20 kHz	6-25
FLJ-UR1BA1	1	•					•		•			3	40 Hz– 1.6 kHz	6-27
FLJ-UR1BA2	1	•					•		•			3	400 Hz–10 kHz	6-27
FLJ-UR2BA1	2	•					•		•			3	40 Hz–1.6 kHz	6-27
FLJ-UR2BA2	2	•					•		•			3	400 Hz–10 kHz	6-27
FLJ-UR2EA1	2	•						•	•			3	40 Hz–1.6 kHz	6-27
FLJ-UR2EA2	2	•						•	•			3	400 Hz–10 kHz	6-27
FLJ-UR2LH1	2	•			•	•			•			3	40 Hz–1.6 kHz	6-27
FLJ-UR2LH2	2	•			•	•			•			3	400 Hz–20 kHz	6-27
FLJ-UR4HA1	4	•				•			•			3	40 Hz–1.6 kHz	6-27
FLJ-UR4HA2	4	•				•			•			3	400 Hz–5 kHz	6-27
FLJ-UR4HB1	4			•		•			•			3	40 Hz–1.6 kHz	6-27
FLJ-UR4HB2	4			•		•			•			3	400 Hz–20 kHz	6-27
FLJ-UR4LA1	4	•			•				•			3	40 Hz–1.6 kHz	6-27
FLJ-UR4LA2	4	•			•				•			3	400 Hz–20 kHz	6-27
FLJ-UR4LB1	4	•			•				•			3	40 Hz–1.6 kHz	6-27
FLJ-UR4LB2	4	•			•				•			3	400 Hz–20 kHz	6-27
FLJ-VB	2	•					•				•	±3	200 Hz–20 kHz	6-37
FLJ-VH	4	•				•					•	±3	20 Hz–20 kHz	6-37
FLJ-VL	4	•			•						•	±3	100 Hz–100 kHz	6-37
FLT-U2	2	•			•	•	•		•			±5	0.001Hz–200 kHz	6-41
FLT-C1	7			•	•					•		±0.5	78 Hz-20 kHz	—

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DATEL

PRODUCT DATA SHEET

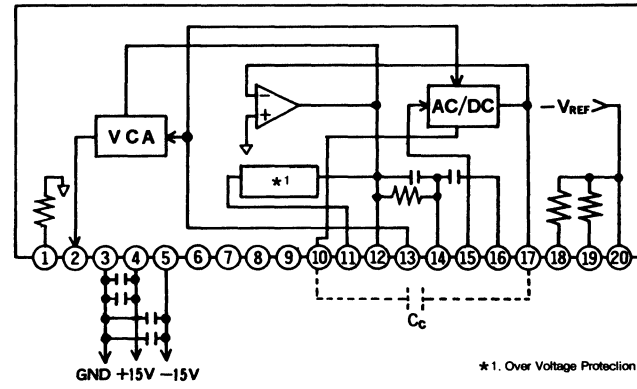
FLJ-ACO1
Oscillator Adaptor for FLJ-D Series

FEATURES

- **Output 2.5Vrms ±0.5% accuracy**
- **500mV~20Vp-p wide amplitude range**
- **Single inline Hybrid package**

GENERAL DESCRIPTION

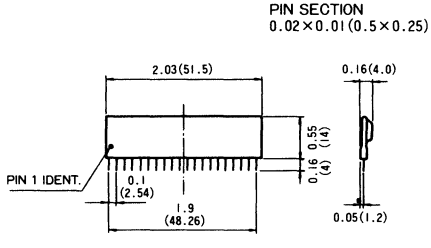
FLJ-ACO1 is an accessory of FLJ-D1, D2 and DC to build a digital programmable oscillator which is controlled with 3 digits of BCD logic input. The setting method, set frequency accuracy and TC depend on FLJ-D1, D2 and DC which are to be used with this FLJ-ACO1, but the specifications related to output voltage such as output voltage accuracy, stability and amplitude TC are determined with the FLJ-ACO1. The output voltage is trimmed internally to provide 2.5Vrms ±0.5% output. With connections of the pins so assigned, 20Vp-p (≦50kHz) output is available. Other intermediate output amplitude is also available by adding external resistors. Oscillation frequency range is 100Hz to 100 kHz. This range is widened toward lower and higher frequency ranges once a few external components are used.



BLOCK DIAGRAM (Fig. 1)

6

MECHANICAL DIMENSIONS INCHES (mm)



PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Rq	11	OUTPUT PROTECTION
2	LOOP OUTPUT	12	COMPENSATION 1
3	GND	13	SUB (-90°) OUTPUT
4	+15V Supply	14	COMPENSATION 3
5	−15V Supply	15	MAIN OUTPUT
6	NC	16	−Vref IN
7	NC	17	COMPENSATION 2
8	NC	18	OUTPUT RANGE 1
9	NC	19	OUTPUT RANGE 2
10	Cext	20	−Vref OUT

DO NOT CONNECT NC PINS TO ANY.
PIN 14 SHOULD BE LEFT OPEN NORMALLY.

SPECIFICATIONS

Typical at 25°C, with ±15V power supplies unless otherwise specified.

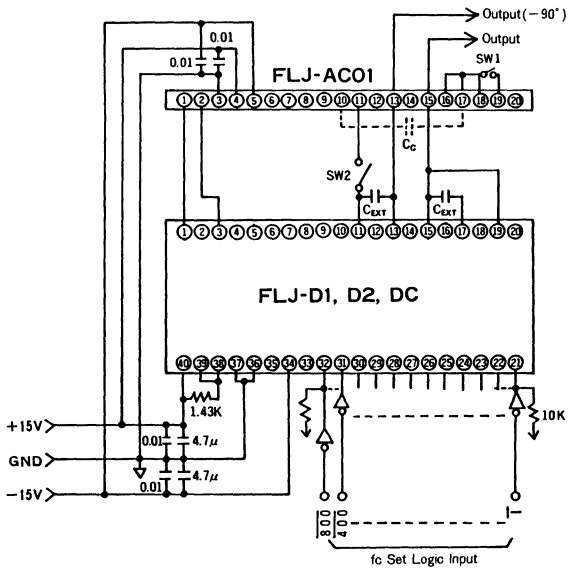
ABSOLUTE RATINGS	
Power Supply Voltage (±Vs)	±18V
Signal Input (Pin 13)	±Vs
Detector Input (Pin 15)	±Vs
OUTPUT	
Output Voltage	2.5Vrms normal *1
Voltage Range ≦100kHz	500mVrms to 2.5Vrms
≦ 50kHz	500mVrms to 20Vp-p
Voltage Set Accuracy	±0.5% max.
Amplitude TC	100 ppm/°C
Output Resistance	5Ω max.
Distortion	0.01%@10kHz
Sub Output	−90°phase of Main Output
FREQUENCY	
Frequency Range	100Hz to 100kHz *2
Frequency Set Error	±0.1%
Setting Method	BCD 3 digits
POWER SUPPLIES & ENVIRONMENT	
Supply Voltage	±15V ±10%
Supply Current	+14mA, −24mA
Operating Temperature Range	−20°C to 70°C
Storage Temperature Range	−30°C to 80°C
Operating/Storage Humidity	10% to 95%/80% RH

*1. 20Vp-p with pin connections, other voltage output ranges are available with the use of external components.
*2. Expandable to wider range with the use of external components.

TECHNICAL NOTES

1. Oscillation frequency range varies depending on the Digital Tuneable Filter to be used with FLJ-ACO1.
   FLJ-D1 1Hz ~ 1.599kHz
   FLJ-D2 100Hz ~ 159.9kHz
   FLJ-DC Determined by external capacitors
   Any model can be used being connected as shown in Figure 3 to get the performance that meets the values shown on the specifications at the frequency range of 100Hz to 100kHz for 2.5Vrms output amplitude and 100Hz to 50kHz for 20Vp-p output.
2. FLJ-DC needs two external capacitors. The relationship between capacitance and oscillation frequency fc is:
   $fc = \frac{N}{20 \cdot Cext}$ fc: Hz, Cext: μF N: Digital Number
   For example, once Cext of 0.005μF and N of 1000 are given, fc shall be 10kHz. Therefore, with N of 1 to 1599, fc can be set at any frequency of 10Hz to 15.99kHz range with BCD logic inputs.
3. Expansion to higher frequency range:
   The maximum frequency is 50kHz for 20Vp-p output even if FLJ-D2 is used. Connect Pin 11 of both FLJ-DC and FLJ-ACO1 together to expand the oscillation frequency range to higher levels. Up to 100kHz of frequency range is obtained for 20 Vp-p amplitude even though distortion ratio is slightly derated as the protection circuit in FLJ-ACO1 works. Up to 159.9kHz of oscillation shall be available for 2.5Vrms output with the same connection.
4. Expansion to lower frequency range:
   Distortion at lower frequency range shall be improved with the addition of a few external components. See Figs. 7, 8 and 9.
   a. With FLJ-D1 (1Hz to 1.599kHz): Connect as shown in Fig. 4. As little as 0.01% distortion can be attained at 4Hz oscillation. See Fig. 7.
   b. With FLJ-DC, Cext=5000pF: Figure 5 shows the circuit with which 10Hz to 15.99Hz oscillation range can be achieved. Distortion at 10Hz shall be improved to 0.005%. See Fig. 8.
5. Adjustment of output voltage:
   Normal 2.5Vrms output voltage is obtained with SW1 of Fig. 3 open and 20Vp-p is obtained with SW1 closed. For other output voltage, follow Fig. 6 and the following equation.
   $R = \frac{1111}{Vo(rms)}$ (kΩ)
   The range of Vo is 0.5Vrms to 20 Vp-p.

TYPICAL CONNECTION (Fig. 3)



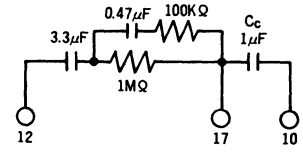
Note 1. Open SW1 and SW2 for 2.5 VrmS output. Close SW1 and SW2 for 20Vp-p output.
2. Two Cext are required for FLJ-DC.

LOGIC INPUT FOR FLJ-D

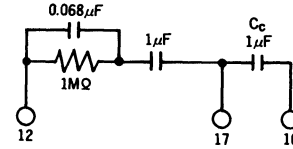
Logic Input		Oscillation F (Hz)		
MSD LSD	Dec.	FLJ−D1	FLJ−D2	FLJ−DC
0000 0000 0001	1	1	100	10
0000 0000 0010	2	2	200	20
0000 0000 0100	4	4	400	40
0000 0000 1000	8	8	800	80
0000 0001 0000	10	10	1 k	100
0000 0010 0000	20	20	2 k	200
0000 0100 0000	40	40	4 k	400
0000 1000 0000	80	80	8 k	800
0001 0000 0000	100	100	10 k	1 k
0010 0000 0000	200	200	20 k	2 k
0100 0000 0000	400	400	40 k	4 k
1000 0000 0000	800	800	80 k	8 k
1001 0000 0000	900	900	90 k	9 k
1010 0000 0000	1000	1000	100 k	10 k
1100 0000 0000	1200	1200	120 k	12 k
1110 0000 0000	1400	1400	140 k	14 k
1111 0000 0000	1500	1500	150 k	15 k
1111 1001 1001	1599	1599	159.9 k	15.99 k

Note1. Only MSD is hexadecimal.
2. Logic 1 : +5V, 0 : GND or OPEN
3. Cext=5000pF used with FLJ-DC

FLJ-D1 FOR LOWER FREQUENCY (Fig. 4)

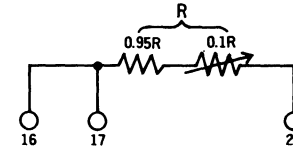


FLJ-DC FOR LOWER FREQUENCY (Fig. 5)



Note: FLJ-D1 or FLJ-DC with 5000pF of Cext for lower than 10Hz oscillation, use one of these circuits.

OUTPUT VOLTAGE ADJUSTMENT (Fig. 6)



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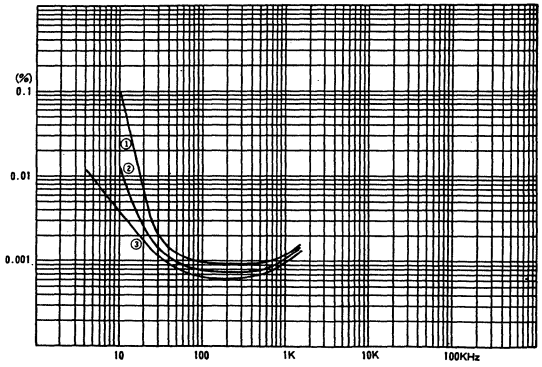
DISTORTION vs. FREQUENCY (Fig. 7)

With FLJ-D1, 2.5Vrms output, technical note 4a.

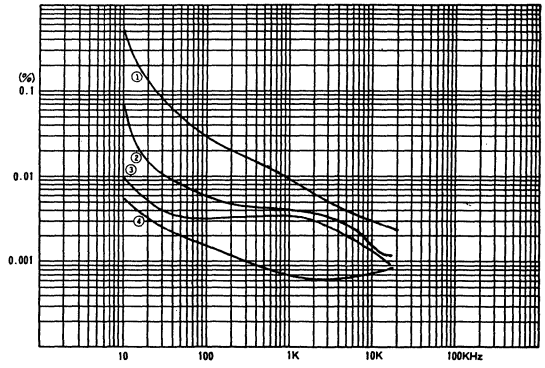
①No external component ②Cc=1μF only ③with all componets of Fig. 4



DISTORTION vs. FREQUENCY (Fig. 8)

With FLJ-DC, Cext=5000pF, technical note 4b.

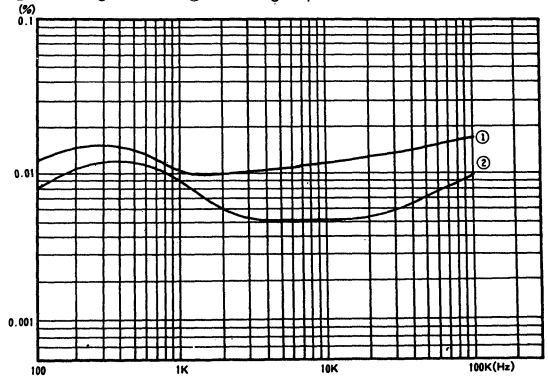
①20Vp-p, no external component ②2.5Vrms, no external components
③2.5Vrms, Cc=1μF only ④2.5Vrms, with all components of Fig. 5



DISTORTION vs. FREQUENCY (Fig. 9)

With FLJ-DC, Cext=500pF, 2.5Vrms, no external component

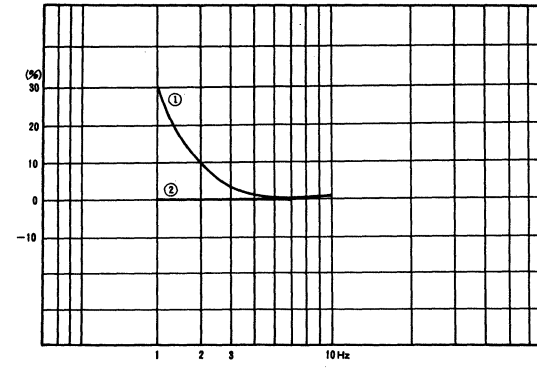
①SW_2 of Fig. 3 closed ②SW_2 of Fig. 3 open



DISTORTION AT LOWER FREQUENCY (Fig. 10)

With FLJ-D1

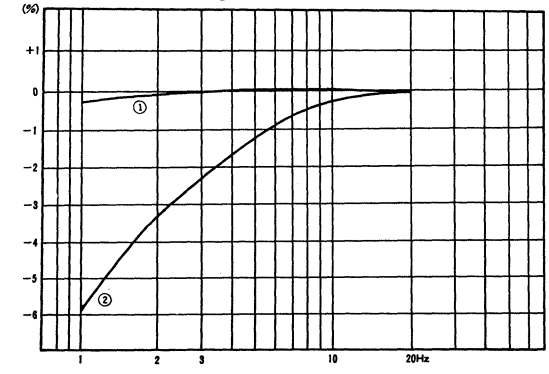
①No external component ②With all components of Fig. 4



fc ACCURACY AT LOWER FREQUENCY (Fig. 11)

With FLJ-D1

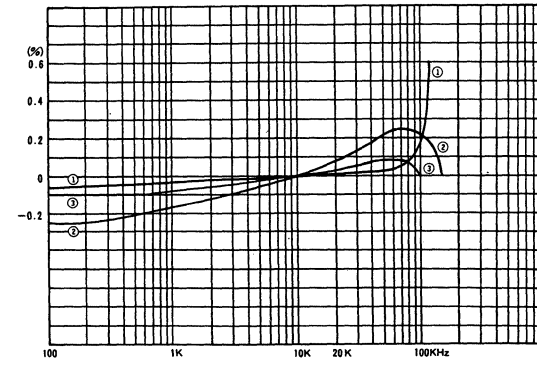
①With all components of Fig. 4 ②No external component



OUTPUT VOLTAGE VARIANCE vs. FREQUENCY (Fig. 12)

With FLJ-D2, 10kHz base

①20Vp-p ②1Vrms ③2.5Vrms



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LOGIC CONTROLLED RESISTOR NETWORK FLJ-ACR1,2

FEATURES

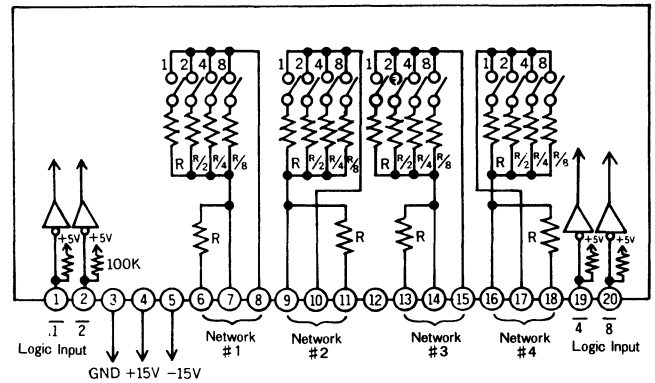
- **Cutoff frequency of resistor tuneable filters can be set with BCD logic.**
- **Single Inline Hybrid.**
- **Small Size, Low Cost.**

GENERAL DESCRIPTION

FLJ-ACR series are logic controlled resistor networks. They are designed to be used with resistor tuneable filters such as FLJ-UR series.

Four separate resistor networks are included in one package. One network consists of four resistors such as R, R/2, R/4 and R/8. The value of R in FLJ-ACR1 is 1.59MΩ while that of FLJ-ACR2 is 159kΩ.

A combination of an FLJ-ACR and an FLJ-UR makes it possible to make a filter whose cutoff frequency or center frequency is set with BCD logic. It is also possible to use this resistor network in the negative feedback loop of an amplifier circuit and control the gain with BCD logic.



R=1.59MΩ (FLJ-ACR1)
R= 159kΩ (FLJ-ACR2)

BLOCK DIAGRAM (Fig. 1)

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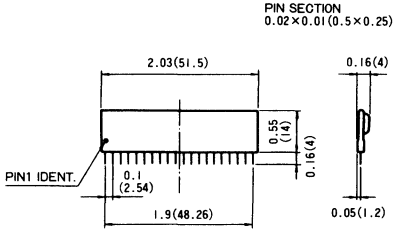
MECHANICAL DIMENSIONS (Fig. 2)
INCHES (mm)



FLJ-UR Series List

Model No.	fc Range	No. of Pole	Type
FLJ-UR4LA1	40Hz ~ 1.6KHz	4	LP, Butt.
FLJ-UR4LB1		4	LP, Cheb.
FLJ-UR4HA1		4	HP, Butt.
FLJ-UR4HB1		4	HP, Cheb.
FLJ-UR2LH1		2	LP/HP, Butt.
FLJ-UR1BA1		1 pair	BP, Butt.
FLJ-UR2BA1		2 pair	BP, Butt.
FLJ-UR2EA1		2 pair	BE, Butt.
FLJ-UR4LA2	400Hz ~ 20KHz	4	LP, Butt.
FLJ-UR4LB2		4	LP, Cheb.
FLJ-UR4HA2		4	HP, Butt.
FLJ-UR4HB2		4	HP, Cheb.
FLJ-UR2LH2		2	LP/HP, Butt.
FLJ-UR1BA2		1 pair	BP, Butt.
FLJ-UR2BA2		2 pair	BP, Butt.
FLJ-UR2EA2		2 pair	BE, Butt.

LP: Lowpass
HP: Highpass
BP: Bandpass
BE: Bandelimination
Butt.: Butterworth
Cheb.: Chebychev

SPECIFICATIONS

Typical at 25°C, ±15VDC power supplies unless otherwise specified.

ABSOLUTE RATINGS

Power Supply Voltage (±Vs) ..... ±18V
Input Signal Voltage ..... ±Vs
Control Logic Voltage ..... +5.5Vmax., -0.5V min.

FREQUENCY SET MODE

BCD 1 Digit ..... 0 to 15
BCD 1 Digit +1 ..... 1 to 16

FREQUENCY SET RANGE (WITH FLJ-UR) Unit: Hz

a. FLJ-ACR1 OR ACR2 SINGLE USE

FLJ-UR Suffix		-1 (Low Range)		-2 (High Range)	
Frequency Set Mode		BCD	BCD+1	BCD	BCD+1
FLJ-ACR1	From	0*	10	0*	100
	To	150	160	1.5k	1.6k
	Resolution	10	10	100	100
FLJ-ACR2	From	0*	100	0*	1k
	To	1.5k	1.6k	15k	16k
	Resolution	100	100	1k	1k

b. FLJ-ACR1 AND ACR2 PARALLEL USE

FLJ-UR Suffix		-1 (Low Range)			-2 (High Range)		
Frequency	-ACR2	BCD	BCD	BCD+1	BCD	BCD	BCD+1
Set Mode	-ACR1	BCD	BCD+1	BCD	BCD	BCD+1	BCD
From		0*	10	100	0*	100	1k
To		1.59k	1.60k	1.69k	15.9k	16.0k	16.9k
Resolution		10	10	10	100	100	100

*Output saturates at 11VDC with zero logic code input.

PERFORMANCE

Frequency Set Error ..... ±1% or less

CONTROL CHARACTERISTICS Logic Code ..... BCD 1 digit (1, 2, 4, 8)
Logic and Level ..... 0V: ON
+5V or Open: OFF

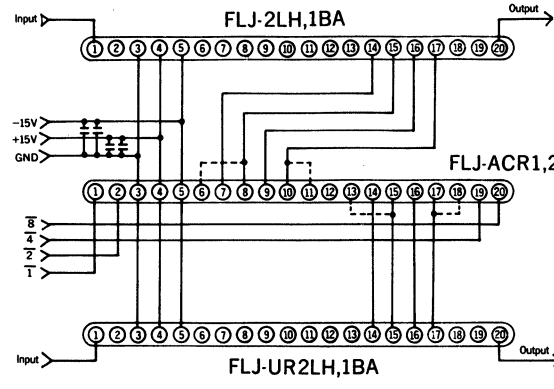
POWER SUPPLIES AND ENVIRONMENT

Power Supply (Operating Range) ..... ±15V (±5V to ±18V)
Current ..... +6.2mA, -1.2mA
Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... -30°C to 80°C
Operating Humidity Range ..... 10% to 95% RH
Storage Temperature Range ..... 10% to 80% RH

TECHNICAL NOTES

1. FLJ-ACR1 and FLJ-ACR2 contain four separate resistor networks which are controlled by common logic inputs. There are two types of FLJ-UR's (resistor tuneable filters) which are to be connected with FLJ-ACR's to build BCD Logic Programmable Filters. One type such as FLJ-UR2LH or FLJ-UR1BA requires two external resistors while all other FLJ-UR's require four external resistors to set a cutoff frequency. Therefore, one FLJ-ACR can control two FLJ-UR2LH's or FLJ-UR1BA's. See Fig. 3.
2. Typical examples of connection are shown in Figs. 4a, 4b, 5a and 5b. Such connections shown in Figs. 4a and 4b generate a problem at the time when an input logic code "0000" is given because no resistor is selected as an external resistor of FLJ-UR's. The filter output is saturated at approximately 11VDC with zero logic code input. The merit of these modes of connection is that the digital code corresponds to the value of fc directly.
   Figs. 5a and 5b illustrate BCD+1 mode of connections. The lowest end frequency is obtained with the input code of "0000" and no output saturation takes place even with zero code logic input. See Table 1.
3. Figs. 6a, 6b and 6c illustrate the connections how to program fc in two digits range. See Table 2.
4. FLJ-ACR1, -ACR2 are designed as accessories of FLJ-UR series resistor tuneable filters. FLJ-ACR can be used as external resistors of operational amplifier circuits to build a programmable gain amplifier.

TYPICAL CONNECTION (Fig. 3)



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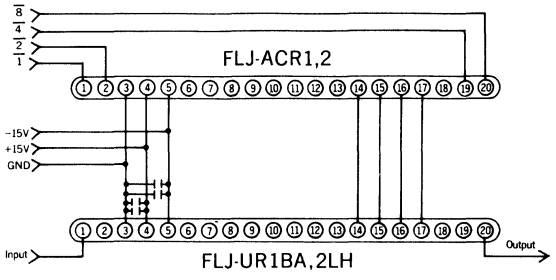
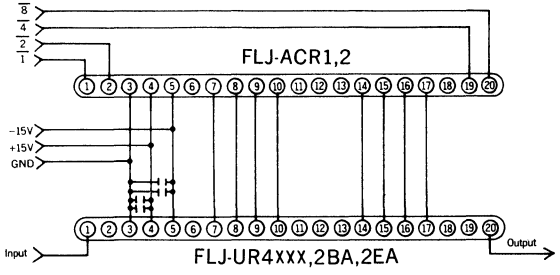
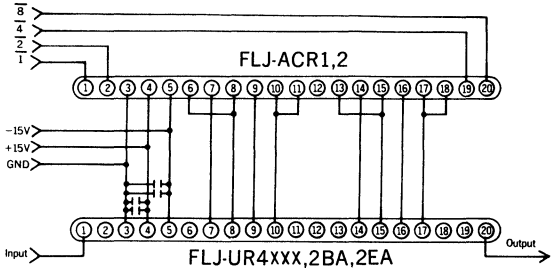
BCD MODE CONNECTION (Fig. 4a)



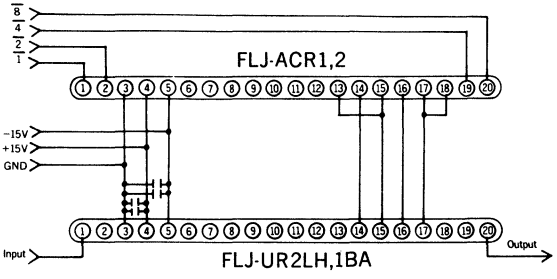
BCD MODE CONNECTION (Fig. 4b)



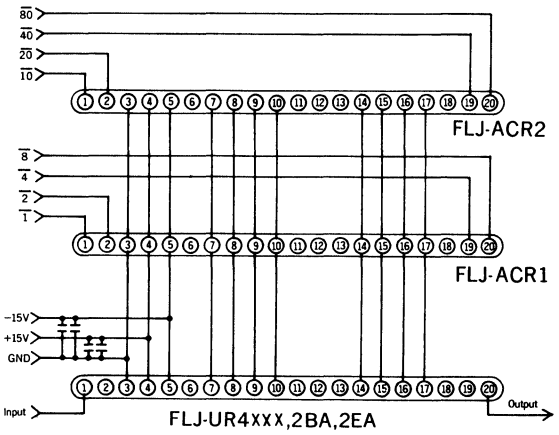
BCD+1 MODE CONNECTION (Fig. 5a)



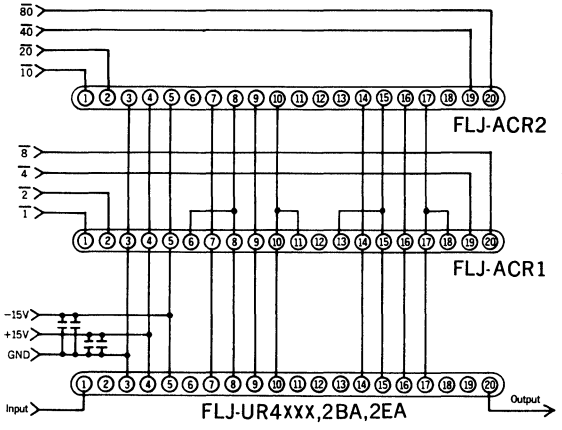
BCD+1 MODE CONNECTION (Fig. 5b)



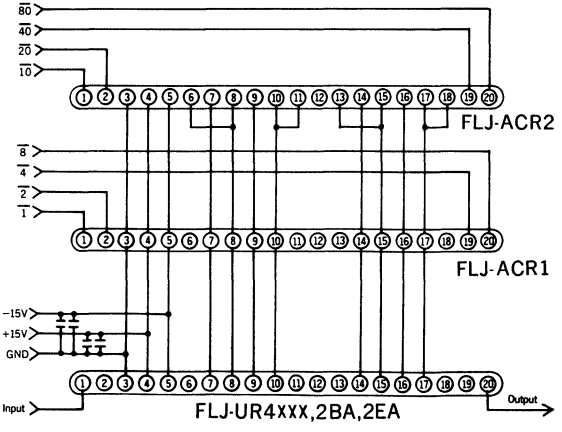
BCD & BCD MODE CONNECTION (Fig. 6a)



BCD & BCD + 1 MODE CONNECTION (Fig. 6b)



BCD + 1 & BCD MODE CONNECTION (Fig. 6c)



6

FLJ-ACR1 OR ACR2 SINGLE USE, SET FREQUENCY (Table 1)

		FLJ−ACR1				FLJ−ACR2			
FLJ-UR Suffix		−1		−2		−1		−2	
Input Logic		fc(Unit:Hz)							
Dec.	BCD	Fig.4	Fig.5	Fig.4	Fig.5	Fig.4	Fig.5	Fig.4	Fig.5
0	0000	−	10	−	100	−	100	−	1 k
1	0001	10	20	100	200	100	200	1 k	2 k
2	0010	20	30	200	300	200	300	2 k	3 k
3	0011	30	40	300	400	300	400	3 k	4 k
4	0100	40	50	400	500	400	500	4 k	5 k
5	0101	50	60	500	600	500	600	5 k	6 k
6	0110	60	70	600	700	600	700	6 k	7 k
7	0111	70	80	700	800	700	800	7 k	8 k
8	1000	80	90	800	900	800	900	8 k	9 k
9	1001	90	100	900	1 k	900	1 k	9 k	10 k
10	1010	100	110	1 k	1.1 k	1 k	1.1 k	10 k	11 k
11	1011	110	120	1.1 k	1.2 k	1.1 k	1.2 k	11 k	12 k
12	1100	120	130	1.2 k	1.3 k	1.2 k	1.3 k	12 k	13 k
13	1101	130	140	1.3 k	1.4 k	1.3 k	1.4 k	13 k	14 k
14	1110	140	150	1.4 k	1.5 k	1.4 k	1.5 k	14 k	15 k
15	1111	150	160	1.5 k	1.6 k	1.5 k	1.6 k	15 k	16 k

FLJ-ACR1 & ACR2 PARALLEL USE, SET FREQUENCY (Table 2)

FLJ-UR Suffix		−1			−2		
Input Logic		fc(Unit:Hz)					
Dec.	BCD	Fig.6a	Fig.6b	Fig.6c	Fig.6a	Fig.6b	Fig.6c
0	0000 0000	−	10	100	−	100	1 k
1	0000 0001	10	20	110	100	200	1.1 k
2	0000 0010	20	30	120	200	300	1.2 k
4	0000 0100	40	50	140	400	500	1.4 k
8	0000 1000	80	90	180	800	900	1.8 k
9	0000 1001	90	100	190	900	1 k	1.9 k
10	0001 0000	100	110	200	1 k	1.1 k	2.0 k
20	0010 0000	200	210	300	2 k	2.1 k	3.0 k
40	0100 0000	400	410	500	4 k	4.1 k	5.0 k
80	1000 0000	800	810	900	8 k	8.1 k	9.0 k
90	1001 0000	900	910	1000	9 k	9.1 k	10.0 k
100	1010 0000	1000	1010	1100	10 k	10.1 k	11.0 k
110	1011 0000	1100	1110	1200	11 k	11.1 k	12.0 k
120	1100 0000	1200	1210	1300	12 k	12.1 k	13.0 k
130	1101 0000	1300	1310	1400	13 k	13.1 k	14.0 k
140	1110 0000	1400	1410	1500	14 k	14.1 k	15.0 k
150	1111 0000	1500	1510	1600	15 k	15.1 k	16.0 k
159	1111 1001	1590	1600	1690	15.9k	16.0 k	16.9 k

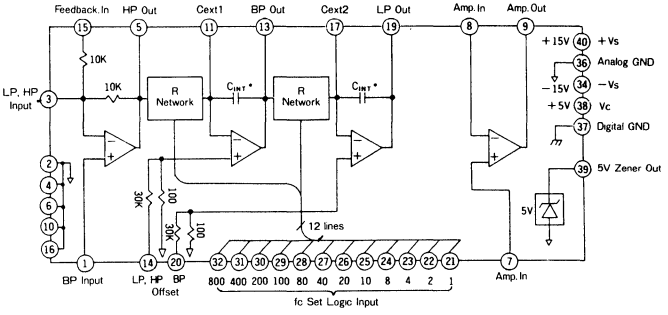
FLJ-D1,D2,DC
DIGITAL PROGRAMMABLE FILTER

FEATURES

- **Cutoff frequency is set by logic inputs.**
- **Lowpass, Highpass and Bandpass output functions are available simultaneously.**
- **Gain and Q are set by external components.**
- **High accuracy, high stability**

GENERAL DESCRIPTION

FLJ-D1, -D2 and -DC are digital programmable filters which can set the cutoff frequency and center frequency with 3 digit BCD inputs.
Two-pole lowpass, bandpass and highpass output functions are available simultaneously from three different outputs and notch function is available by combining these outputs to the uncommitted op amp.
To realize higher order filters, several filters can be cascaded. And to obtain higher performance of higher order filters, both Gain and Q are designed to be set with external components.

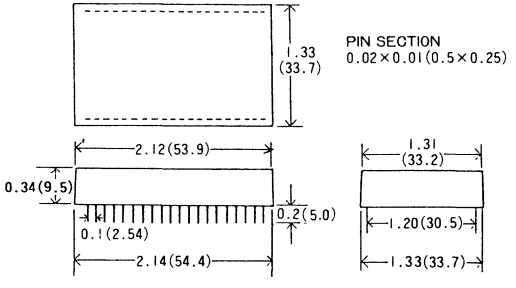


*C_{INT} FLJ-D1 50,000pF
FLJ-D2 500pF
FLJ-DC None. Need Cext.

BLOCK DIAGRAM (Fig. 1)

6

MECHANICAL DIMENSIONS (Fig. 2)
INCHES(mm)



PIN CONNECTIONS (Table 1)

FUNCTION	PIN		FUNCTION
INPUT (BP)	1	40	+Vs (+15V)
ANALOG GND	2	39	5V ZENER OUTPUT
INPUT (HP, LP)	3	38	Vc(+5V)
ANALOG GND	4	37	DIGITAL GND
OUTPUT (HP)	5	36	ANALOG GND
ANALOG GND	6	35	NC
AMP. (+) INPUT	7	34	-Vs(-15V)
AMP. (−) INPUT	8	33	NC
AMP. OUTPUT	9	32	LOGIC 800
ANALOG GND	10	31	LOGIC 400
Cext 1.	11	30	LOGIC 200
NC	12	29	LOGIC 100
OUTPUT (BP)	13	28	LOGIC 80
ZERO ADJ. (HP, LP)	14	27	LOGIC 40
NEG. FEEDBACK IN	15	26	LOGIC 20
ANALOG GND	16	25	LOGIC 10
Cext 2.	17	24	LOGIC 8
NC	18	23	LOGIC 4
OUTPUT (LP)	19	22	LOGIC 2
ZERO ADJ. (BP)	20	21	LOGIC 1

DO NOT CONNECT NC PINS TO OTHERS.

SPECIFICATIONS (Table 2)

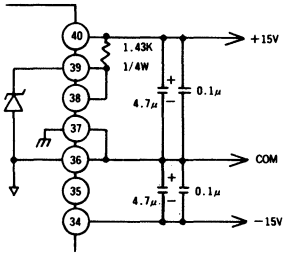
Typical at 25°C, ±15V and +5V supplies, gain of -1, $Q = \sqrt{2}/2$ unless otherwise specified.

ABSOLUTE RATINGS

Power Supplies ..... ±Vs : ±20V, Vc : +5.5V
Control Logic Input ..... Vc+0.5V
Analog Input ..... ±Vs

FILTER CHARACTERISTICS	
Frequency Program Range : FLJ-D1 ...	1Hz ~ 1.599KHz
FLJ-D2 ...	100Hz ~ 159.9KHz
FLJ-DC ...	Determined by external capacitors
Frequency Program	BCD 3 digits, MSD is hexa-decimal (0~15)
Frequency Program Accuracy	±0.1%
Q Range	$1/3 \leqq Q \leqq 1 \times 10^6 / fc$
Rolloff	12dB/oct (LP, HP), 6dB/octBW (BP)
Number of poles	2pole (1 pole pair)
Voltage Gain	1 ~ 10
Pass Band Gain Variance	Depends on external resistors
Resonant Frequency T.C.	0.01%/°C
Gain T.C.	0.2dB Full Temperature Range
Distortion	0.002%
Noise	35μVrms (LP), 100μVrms (HP), 30μVrms (BP)
Load Resistance	2KΩ
AMPLIFIER CHARACTERISTICS	
Input Voltage Range	±10V min.
Input Impedance	300KΩ
Input Offset Voltage	0.5mV
Input Bias Current	200nA
Input Offset Drift	5μV/°C
Output Voltage/Current	±10V/5mA min.
Output Impedance	5Ω max.
Output Short Circuit Current	38mA
Small Signal Frequency Bandwidth ...	10MHz
Slew Rate	8V/μSec
POWER SUPPLIES AND ENVIRONMENT	
Supply Voltages	±Vs : ±15V ±10%, Vc : +5V ±10%
Supply Current	+15mA, -18mA +2.2mA
Operating Temperature Range	-20°C ~ +70°C
Operating Humidity Range	10% ~ 95% RH
Storage Temperature Range	-30°C ~ +80°C
Storage Humidity Range	10% ~ 80% RH

ZENER OUTPUT (Fig. 3)



TECHNICAL NOTES

1. The cutoff frequency of lowpass and highpass, and the center frequency of bandpass filters can be set with three digit BCD, TTL compatible logic inputs. The MSD is hexadecimal. See table 1.
2. The cutoff frequency is shown as either one equation of the following:

$$fc = \frac{N}{20 \cdot C} \text{ Hz}, \quad C : \mu F, \ N : \text{Digital Number}$$

$$fc = \frac{N}{2\pi \cdot C \cdot Rf} \text{ Hz}, \ C : F, \ Rf : \Omega, \ N : \text{Digital Number}$$

C = 50,000pF is contained in FLJ-D1 and C = 500pF is contained in FLJ-D2 respectively, while no capacitor is contained in FLJ-DC.
The fc's of each model are:

$$\text{FLJ-D1} : fc = N \text{ or } fc = \frac{N}{2\pi \cdot 5 \times 10^{-8} \cdot Rf}$$

$$\text{FLJ-D2} : fc = 100N \text{ or } fc = \frac{N}{2\pi \cdot 5 \times 10^{-10} \cdot Rf}$$

$$\text{FLJ-DC} : fc = \frac{N}{20 \cdot C} \text{ or } fc = \frac{N}{2\pi \cdot Cext \cdot Rf}$$

The value of Rf is 3.183KΩ for the programmed fc logic is 1,000.
The value of Cext is calculated taking these factors into consideration.

3. Each logic input is connected to CMOS4000 series internally. Then each input is pulled down with 100KΩ resistors. The use of 10KΩ pull-up resistors to +5V is recommended when filters are programmed with TTL logic.
4. An independent +5V zener diode is contained in the filter. The output voltage range of this diode is +4.87V ~ +5.12V. The connection shown in Figure 3 is recommended if a filter is driven by ±15V supplies only.
5. Analog GND (Pin36) and logic GND (Pin37) are separated to be useful for universal applications. Connect grounds of ±15V and +5V externally. No return current of the digital power supply should flow through the analog ground.
6. The use of 4.7μF and 0.1μF bypass capacitors for both ±15V and +5V lines close to the module is highly recommended.

LOGIC INPUT CODING TABLE (Table 3)

Logic Input *1 (MSD)			(LSD)	Decimal Number	fc (Cutoff Frequency)		
					FLJ-D1	FLJ-D2	FLJ-DC*2
0 0 0 0	0 0 0 0	0 0 0 1		1	1Hz	100Hz	0.1Hz
0 0 0 0	0 0 0 0	0 0 1 0		2	2	200	0.2
0 0 0 0	0 0 0 0	0 1 0 0		4	4	400	0.4
0 0 0 0	0 0 0 0	1 0 0 0		8	8	800	0.8
0 0 0 0	0 0 0 1	0 0 0 0		10	10	1KHz	1
0 0 0 0	0 0 1 0	0 0 0 0		20	20	2	2
0 0 0 0	0 1 0 0	0 0 0 0		40	40	4	4
0 0 0 0	1 0 0 0	0 0 0 0		80	80	8	8
0 0 0 1	0 0 0 0	0 0 0 0		100	100	10	10
0 0 1 0	0 0 0 0	0 0 0 0		200	200	20	20
0 1 0 0	0 0 0 0	0 0 0 0		400	400	40	40
1 0 0 0	0 0 0 0	0 0 0 0		800	800	80	80
1 0 0 1	0 0 0 0	0 0 0 0		900	900	90	90
1 0 1 0	0 0 0 0	0 0 0 0		1000	1000	100	100
1 1 0 0	0 0 0 0	0 0 0 0		1200	1200	120	120
1 1 1 0	0 0 0 0	0 0 0 0		1400	1400	140	140
1 1 1 1	0 0 0 0	0 0 0 0		1500	1500	150	150
1 1 1 1	1 0 0 1	1 0 0 1		1599	1599Hz	159.9KHz	159.9Hz

Note: *1. Logic 1 = +5V
Logic 0 = GND or OPEN
*2. FLJ-DC needs external capacitors.
These values are ones when two 0.5μF are used as external capacitors.

GAIN AND Q

The gain and Q of this filter are set with the following equations.

1. Lowpass and highpass filters

Gain: $G = \frac{-1}{Rg} \times 10^4$ (Rg : Ω)

Q: $Q = \frac{Rg \cdot (Rq + 10^4)}{Rq \cdot (2Rg + 10^4)}$

Rg = 10KΩ when G = -1. Then, $Rq = \frac{10^4}{3Q-1}$

Then, the following values are obtained:

	Q	Rq
Butterworth	0.70711	8.918KΩ
Bessel	0.57735	13.66KΩ

See Figure 4 and 5 for "Amplitude/Phase vs. Frequency" characteristics.

2. Bandpass filter

Gain: $G = \frac{-1}{Rg} \times 10^4$ (Rg : Ω)

Q: $Q = \frac{1 + (1/Rg + 1/Rq) \cdot 10^4}{2}$

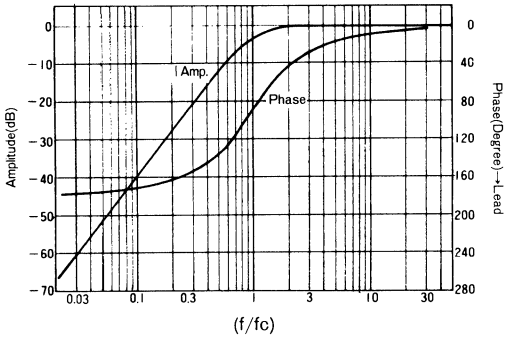
Rg = 10KΩ when G = -1. Then, $Rq = \frac{10^4}{2(Q-1)}$

Then, the following values are obtained:

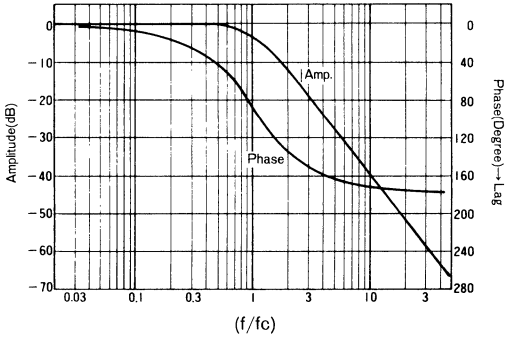
Q	Rq
2	5.00KΩ
5	1.25KΩ
10	556Ω

See Figure 6 for reference.

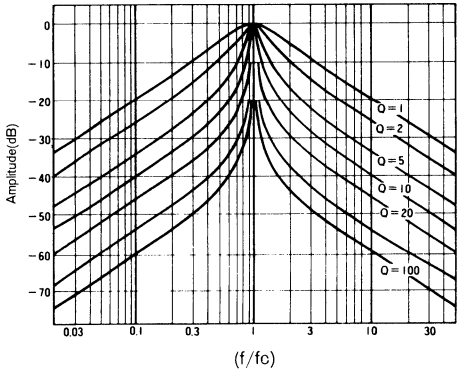
BUTTERWORTH HIGHPASS (Fig. 4)



BUTTERWORTH LOWPASS (Fig. 5)



BANDPASS (Fig. 6)



6

APPLICATIONS

I. HIGHER ORDER LOWPASS AND HIGHPASS FILTERS

Several units of FLJ-D Series filters can be cascaded to realize higher order filters. Any model can be used to make Butterworth filters as the cutoff frequency of each stage is equal.

The use of FLJ-DC is recommended for other type of filters such as Chebyshev and Bessel because the cutoff frequency of each stage is different.

The value of external components are different at each stage. The Tables 7 and 8 show the values of fn and Qn at each stage.

= Design Example 1. =

- Higher Order Lowpass Filter/Basic Theory

Following points should be understood referring to the Figure 9.

a. Connections are the same either for Butterworth, Bessel or Chebyshev.
b. Each module is used as a two-pole filter in case of even order.
c. The first module is used as a one-pole filter and the rest are used as two-pole in case of odd order.
d. Even order filter : Input is given to Input #2 of Fig. 9. Output is either Output #3, #4 or #5 depending on the number of order.
In case of sixth order filter, for example, 3 pieces of FLJ-D are used, input and output are Input #2 and Output #4 respectively.
Proper values of Rg1 ~ Rg4, Rq1 ~ Rq4 and Cext1 ~ Cext 4 are to be selected depending on filter type. See Table 4, 5, 6.
e. Odd order filter : Input is given to Input #1 of Fig. 9. Output is either Output #2, #3, #4. In case of fifth order filter, 3 pieces of FLJ-D are used, input is given to Input #1, Output #1 and Input #2 are connected, output is taken from Output #3.
f. The fc program logic lines are connected to each other of filter in equal ways.

- Higher Order Lowpass Filter/Calculation Example

To build 8th order, 0.05dB ripple, Chebyshev filter using four FLJ-DC's.
Here, gain=+1, the cutoff frequency should be programmed between 10Hz and 15.99KHz.

a. Use 4 pieces of FLJ-DC.
b. Output is inverted at every 2nd order. Output becomes in phase with input at the final stage, in this case.
c. The relationship between the cutoff frequency and the external capacitors of FLJ-DC is shown in the following equation.

$fc = \frac{N}{20\ Cext}$ N: Digital Number (1~1,599) Cext: μF, fc:Hz

If digital range of 10Hz ~ 15.99KHz is desired, fc is equal to 10N.

$10N = \frac{N}{20\ Cext}$ then, Cext = 0.005μF = 5000pF

d. Gain of each stage is -1, then $G=-1/Rgx10^4$, then Rg=10KΩ.
e. Refer to Table 7 and find out fn=0.42170 and Qn=0.57503 at the crossing point of "8 Poles, 1st stage" and "Chebyshev, 0.05dB ripple".
These figures mean that the cutoff frequency of the 1st stage should be 0.42170 times of the total cutoff frequency, and that the Q of 1st stage should be 0.57503 respectively.

$0.42170fc = \frac{N}{20Cext}$ here substitute fc=10N

then, $4.2170N = \frac{N}{20Cext}$ therefore, Cext = 0.011857μF = 11857pF

$Rq = \frac{10^4}{3Q-1}$ here Q = 0.57503, therefore, Rq1=13.7KΩ.

f. Rqn and Cextn of 2nd, 3rd and 4th stages are calculated in similar ways. The Table 6 shows the results of the calculations.

= Design Example 2 =

- Higher Order Highpass Filter/Calculation Example

To build 8th order Butterworth highpass filter using FLJ-DC.
Gain should be +1, the cutoff frequency range should be 10Hz ~ 15.99KHz.

a. Use 4 pieces of FLJ-DC. Gain of each stage is -1 and it becomes +1 at the final stage.

$G = \frac{-1}{Rg} \times 10^4$, therefore, Rg = 10KΩ.

b. See table 4 and obtain values of fn and Qn of each stage under 8th Butterworth.

$fc = \frac{N}{20Cext}$ N: Digital Number (1 ~ 1,599) Cext: μF fc:Hz

The fn of each stage is 1.

Therefore, $10N = \frac{N}{20Cext}$ then, Cext = 5000pF

c. Gain is -1 at each stage.

$Rq = \frac{10^4}{3Q-1}$ substitute values of Qn to obtain Rq of each stage.

The results are shown in Table 9. See Table 10 for Chebyshev highpass filter.

II. BANDPASS FILTER

One-pole pair, two-pole pair and three-pole pair connections are shown in Figure 11. The values of external components are shown in Table 11.

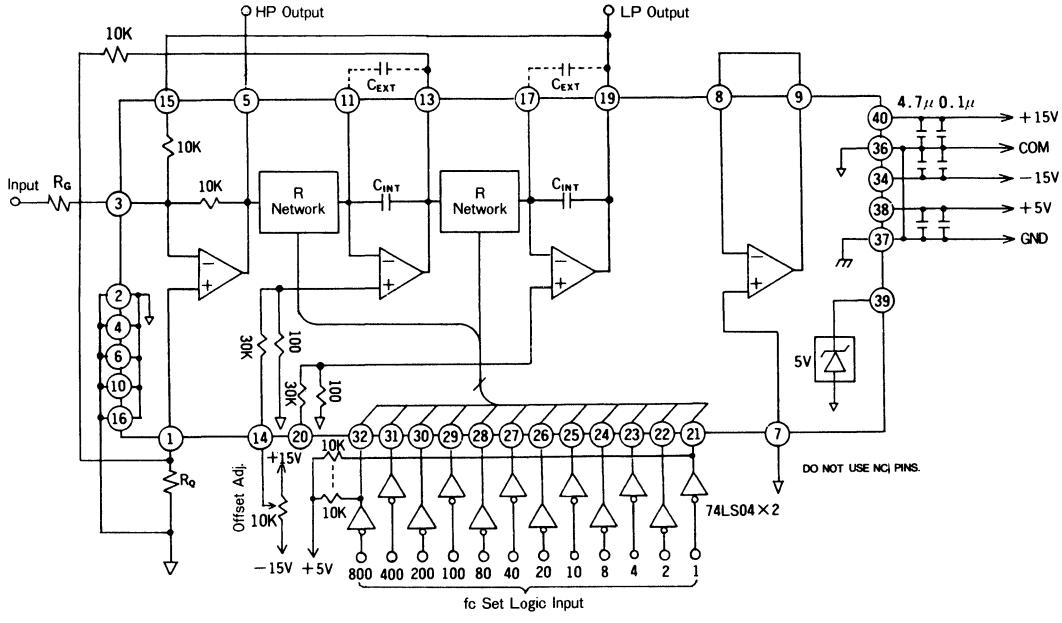
III. BAND ELIMINATION FILTER

A band elimination (=notch) filter can be made using FLJ-D Series filters.

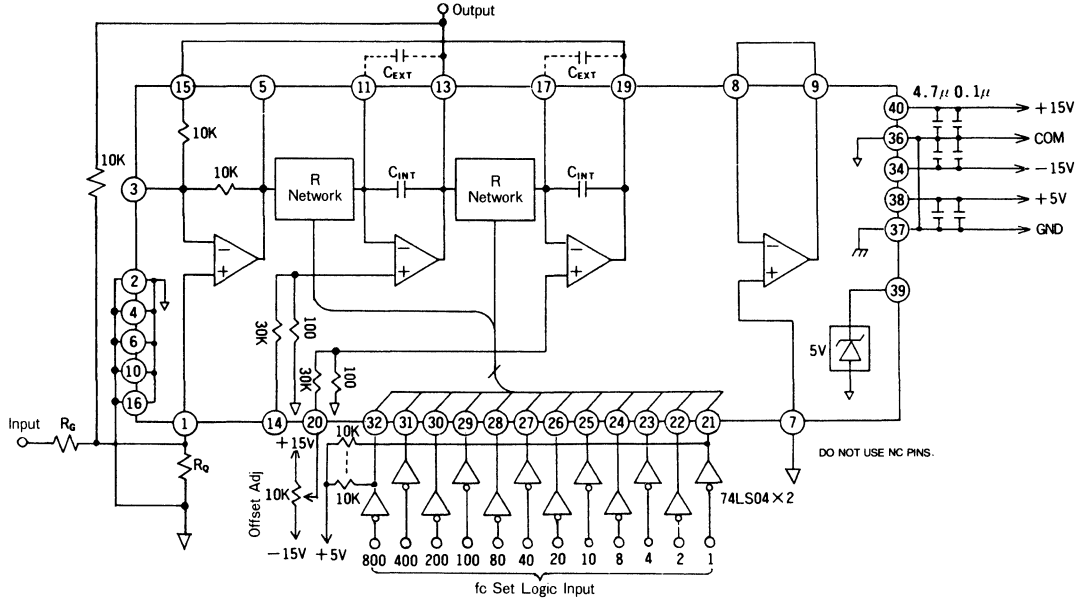
A non-inverting type which employs LP + HP method is shown in Figure 12.

An inverting type which employs 1-BP method is shown in Figure 13. It is recommended to use a non-inverting type for $Q \leqq 1$ and inverting type for $Q \geqq 1$ applications. A bandpass filter of higher order is shown in Figure 14.

LOWPASS & HIGHPASS CONNECTIONS (Fig. 7)



BANDPASS FILTER CONNECTIONS (Fig.8)



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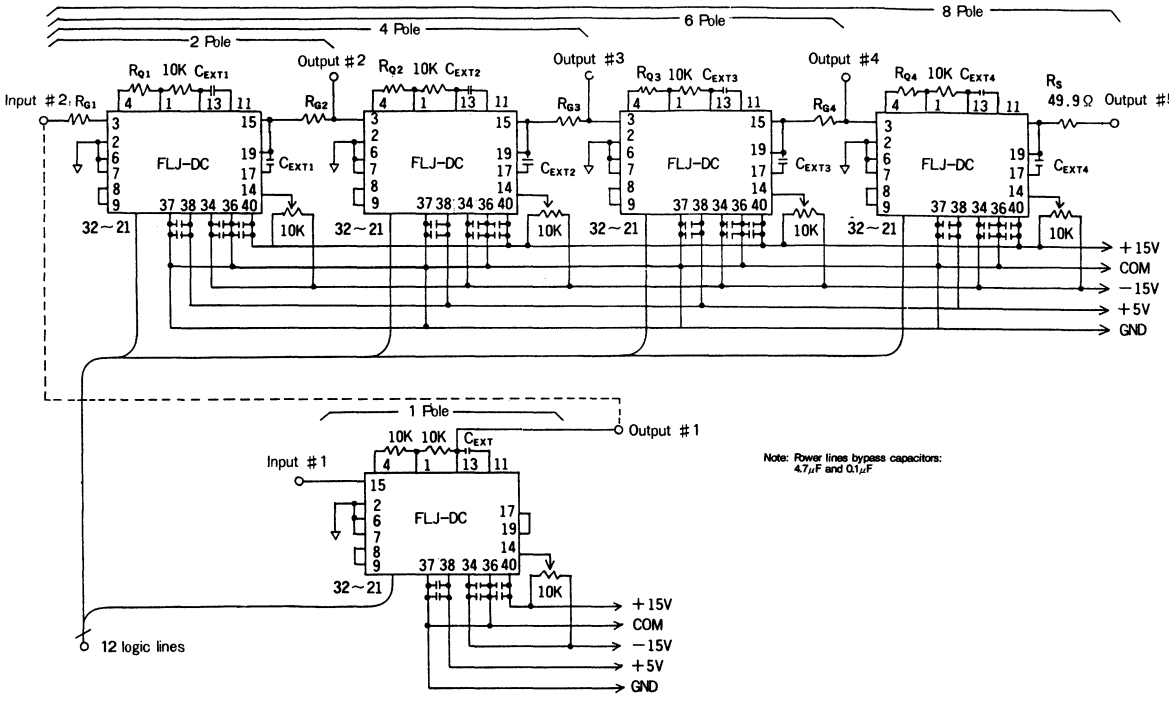
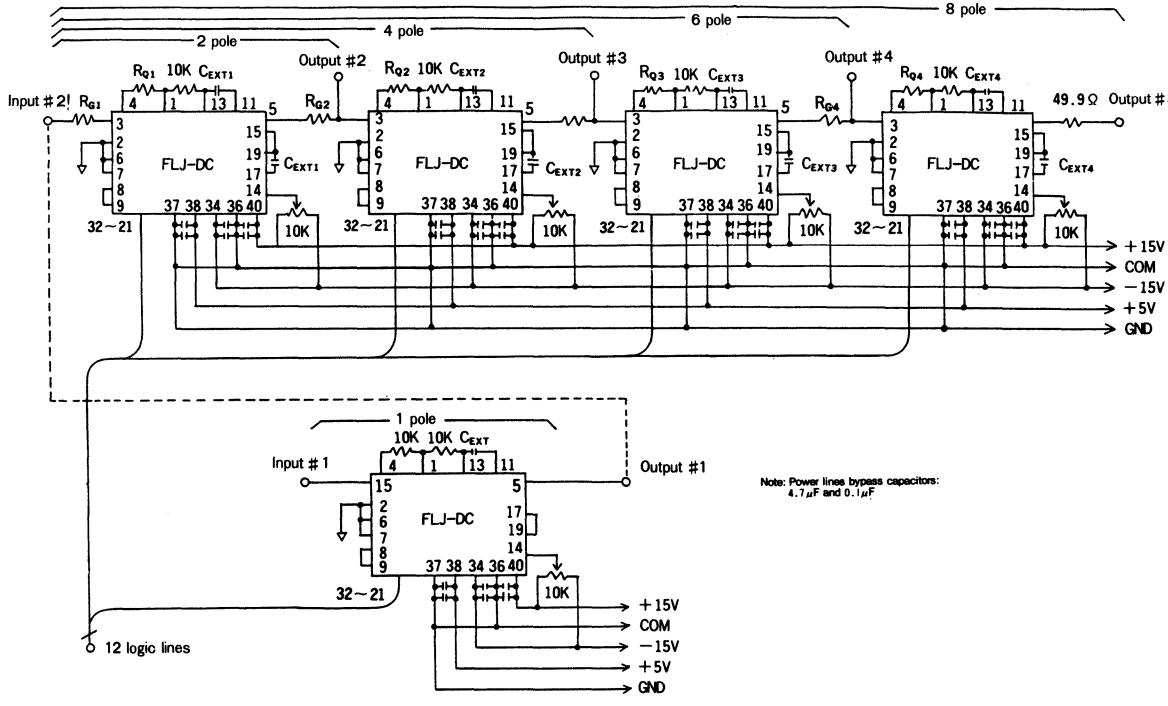
HIGHER ORDER LOWPASS FILTER (Fig. 9)



HIGHER ORDER HIGHPASS FILTER (Fig. 10)



BUTTERWORTH, LOWPASS EXTERNAL COMPONENTS (Table 4)

(FLJ-DC, fc:10Hz~15.99KHz, IGI=1) (See Fig. 9)

	2 pole	3 pole	4 pole	5 pole	6 pole	7 pole	8 pole
C_{EXT}		5000pF		5000pF		5000pF	
C_{EXT1}	5000pF	5000pF	5000pF	5000pF	5000pF	5000pF	5000pF
C_{EXT2}			5000pF	5000pF	5000pF	5000pF	5000pF
C_{EXT3}					5000pF	5000pF	5000pF
C_{EXT4}							5000pF
R_{G1}	10KΩ	10KΩ	10KΩ	10KΩ	10 KΩ	10KΩ	10KΩ
R_{G2}	Rs	Rs	10KΩ	10KΩ	10 KΩ	10KΩ	10KΩ
R_{G3}			Rs	Rs	10 KΩ	10KΩ	10KΩ
R_{G4}					Rs	Rs	10KΩ
R_{Q1}	8.87KΩ	4.99K	16.2KΩ	11.8KΩ	18.2KΩ	15KΩ	18.7KΩ
R_{Q2}			3.4KΩ	2.61KΩ	8.87KΩ	6.98KΩ	12.4KΩ
R_{Q3}					2.10KΩ	1.74KΩ	5.90KΩ
R_{Q4}							1.50KΩ
Input	#2	#1	#2	#1	#2	#1	#2
Output	#2	#2	#3	#3	#4	#4	#5

Rs=49.9Ω

BESSEL, LOWPASS EXTERNAL COMPONENTS (Table 5)

(FLJ-DC, fc:10Hz~15.99KHz, IGI=1) (See Fig.9)

	2 pole	3 pole	4 pole	5 pole	6 pole	7 pole	8 pole
C_{EXT}		3774pF		3323pF		2964pF	
C_{EXT1}	3924pF	3448pF	3491pF	3208pF	3112pF	2908pF	2807pF
C_{EXT2}			3113pF	2844pF	2955pF	2739pF	2725pF
C_{EXT3}					2621pF	2436pF	2556pF
C_{EXT4}							2281pF
R_{G1}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G2}	Rs	Rs	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G3}			Rs	Rs	10KΩ	10KΩ	10KΩ
R_{G4}					Rs	Rs	10KΩ
R_{Q1}	13.7KΩ	9.31KΩ	17.8KΩ	14.3KΩ	18.7KΩ	16.9KΩ	19.1KΩ
R_{Q2}			6.98KΩ	5.76KΩ	12.1KΩ	10.2KΩ	14.7KΩ
R_{Q3}					4.87KΩ	4.22KΩ	8.87KΩ
R_{Q4}							3.74KΩ
Input	#2	#1	#2	#1	#2	#1	#2
Output	#2	#2	#3	#3	#4	#4	#5

Rs=49.9Ω

CHEBYSHEV, LOWPASS EXTERNAL COMPONENTS (Table 6)

(FLJ-DC, fc:10Hz~15.99KHz, IGI=1) (See Fig.9) ( ):Ripple

	4pole(0.5dB)	5pole(0.5dB)	6pole(0.1dB)	7pole(0.1dB)	8pole(0.05dB)
C_{EXT}		13800pF		13270pF	
C_{EXT1}	8375pF	7241pF	9743pF	8701pF	11857pF
C_{EXT2}	4848pF	4913pF	5992pF	5761pF	7467pF
C_{EXT3}			4705pF	4784pF	5485pF
C_{EXT4}					4764pF
R_{G1}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G2}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G3}	Rs	Rs	10KΩ	10KΩ	10KΩ
R_{G4}			Rs	Rs	10KΩ
R_{Q1}	8.87KΩ	3.92KΩ	12.4KΩ	6.49KΩ	13.7KΩ
R_{Q2}	1.27KΩ	787Ω	3.32KΩ	2.21KΩ	4.54KΩ
R_{Q3}			768Ω	562Ω	1.78KΩ
R_{Q4}					487Ω
Input	#2	#1	#2	#1	#2
Output	#3	#3	#4	#4	#5

BUTTERWORTH, HIGHPASS (Table 9)

(FLJ-DC, fc:10Hz~15.99KHz, IGI=1) (See Fig.10)

	2pole	3pole	4pole	5pole	6pole	7pole	8pole
C_{EXT}		5000pF		5000pF		5000pF	
C_{EXT1}	5000pF	5000pF	5000pF	5000pF	5000pF	5000pF	5000pF
C_{EXT2}			5000pF	5000pF	5000pF	5000pF	5000pF
C_{EXT3}					5000pF	5000pF	5000pF
C_{EXT4}							5000pF
R_{G1}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G2}	49.9Ω	49.9Ω	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G3}			49.9Ω	49.9Ω	10KΩ	10KΩ	10KΩ
R_{G4}					49.9Ω	49.9Ω	10KΩ
R_{Q1}	8.87KΩ	4.99KΩ	16.2KΩ	11.8KΩ	18.2KΩ	15.0KΩ	18.7KΩ
R_{Q2}			3.4KΩ	2.61KΩ	8.87KΩ	7.15KΩ	12.4KΩ
R_{Q3}					2.10KΩ	1.74KΩ	5.9KΩ
R_{Q4}							1.50KΩ
Input	#2	#1	#2	#1	#2	#1	#2
Output	#2	#2	#3	#3	#4	#4	#5

CHEBYSHEV, HIGPASS (Table 10)

(FLJ-DC, fc:10Hz~15.99KHz, IGI=1) (See Fig.10)

	4pole(0.5dB)	5pole(0.5dB)	6pole(0.1dB)	7pole(0.1dB)	8pole(0.05dB)
C_{EXT}		1812pF		1884pF	
C_{EXT1}	2985pF	3452pF	2566pF	2873pF	2109pF
C_{EXT2}	5156pF	5089pF	4172pF	4339pF	3348pF
C_{EXT3}			5314pF	5226pF	4558pF
C_{EXT4}					5248pF
R_{G1}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G2}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G3}	49.9Ω	49.9Ω	10KΩ	10KΩ	10KΩ
R_{G4}			49.9Ω	49.9Ω	10KΩ
R_{Q1}	8.87KΩ	3.92KΩ	12.4KΩ	6.49KΩ	13.7KΩ
R_{Q2}	1.27KΩ	787Ω	3.32KΩ	2.21KΩ	4.53KΩ
R_{Q3}			768Ω	562Ω	1.78KΩ
R_{Q4}					487Ω
Input	#2	#1	#2	#1	#2
Output	#3	#3	#4	#4	#5

Rs=49.9Ω

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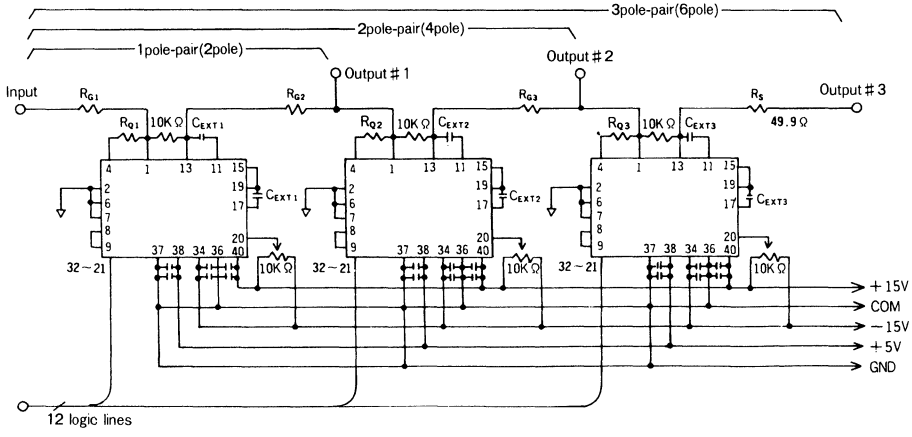
HIGHER ORDER BUTTERWORTH(LP, HP), BESSEL(LP), CHEBYSHEV(LP)···fn, Qn Table (Table 7)

No. of Pole		Butterworth		Bessel(LP)		Chebyshev(LP)											
						0.05dB(Ripple)		0.1dB		0.2dB		0.25dB		0.3dB		0.5dB	
		fn	Qn	fn	Qn	fn	Qn	fn	Qn	fn	Qn	fn	Qn	fn	Qn	fn	Qn
2		1.0	0.707107	1.2742	0.57735												
3	1st	1.0	0.5	1.32475	0.5												
	2nd	1.0	1.000000	1.44993	0.69104												
4	1st	1.0	0.541196	1.43241	0.52193	0.88526	0.60017	0.78926	0.61880	0.70111	0.64590	0.67442	0.65725	0.65324	0.66778	0.59700	0.70511
	2nd	1.0	1.306563	1.60594	0.80554	1.22098	1.99842	1.15327	2.18293	1.09483	2.43501	1.07794	2.53611	1.06482	2.62790	1.03127	2.94055
5	1st	1.0	0.5	1.50470	0.5	0.61901	0.5	0.53891	0.5	0.46141	0.5	0.43695	0.5	0.41713	0.5	0.36232	0.5
	2nd	1.0	0.618034	1.55876	0.56354	0.85362	0.85227	0.79745	0.91452	0.74726	1.00091	0.73241	1.03593	0.72076	1.06790	0.69048	1.17781
	3rd	1.0	1.618034	1.75812	0.91652	1.13476	2.96615	1.09313	3.28201	1.05708	3.70686	1.04663	3.87568	1.03851	4.02836	1.01773	4.54496
6	1st	1.0	0.517638	1.60653	0.51032	0.56933	0.58116	0.51319	0.59946	0.46032	0.62595	0.44406	0.63703	0.43103	0.64729	0.39623	0.68364
	2nd	1.0	0.707107	1.69186	0.61120	0.87014	1.21335	0.83449	1.33157	0.80306	1.49172	0.79385	1.55565	0.78666	1.61360	0.76812	1.81038
	3rd	1.0	1.931852	1.90782	1.0233	1.09094	4.15611	1.06273	4.63290	1.03823	5.26890	1.03112	5.52042	1.02560	5.74741	1.01145	6.51285
7	1st	1.0	0.5	1.68713	0.5	0.43017	0.5	0.37678	0.5	0.32431	0.5	0.30760	0.5	0.29400	0.5	0.25617	0.5
	2nd	1.0	0.554958	1.71911	0.53235	0.61098	0.78823	0.57464	0.84640	0.54170	0.92694	0.53186	0.95956	0.52411	0.98931	0.50386	1.09155
	3rd	1.0	0.801938	1.82539	0.66083	0.89236	1.66357	0.86788	1.84721	0.84643	2.09299	0.84017	2.19039	0.83528	2.27837	0.82273	2.57555
	4th	1.0	2.246980	2.05279	1.1263	1.06561	5.56621	1.04520	6.23324	1.02745	7.11866	1.02230	7.46782	1.01829	7.78256	1.00802	8.84180
8	1st	1.0	0.509796	1.78143	0.50599	0.42170	0.57503	0.38159	0.59318	0.34344	0.61944	0.33164	0.63041	0.32219	0.64058	0.29674	0.67657
	2nd	1.0	0.601345	1.83514	0.55961	0.66965	1.07710	0.64514	1.18296	0.62334	1.32615	0.61692	1.38326	0.61189	1.43501	0.59887	1.61068
	3rd	1.0	0.899976	1.95645	0.71085	0.91166	2.19456	0.89381	2.45282	0.87820	2.79620	0.87365	2.93174	0.87011	3.05398	0.86101	3.46567
	4th	1.0	2.562915	2.19237	1.2257	1.04963	7.19539	1.03416	8.08190	1.02070	9.25500	1.01679	9.71678	1.01375	10.1327	1.00595	11.5308

HIGH ORDER CHEBYSHEV(HP)···fn, Qn Table (Table 8)

No. of Pole		Chebyshev(HP)											
		0.05dB(Ripple)		0.1dB		0.2dB		0.25dB		0.3dB		0.5dB	
		fn	Qn	fn	Qn	fn	Qn	fn	Qn	fn	Qn	fn	Qn
4	1st	1.129612	1.99842	1.267010	2.18293	1.426310	2.43501	1.482756	2.53611	1.530831	2.62790	1.675042	2.94055
	2nd	0.819014	0.60017	0.867100	0.61880	0.913384	0.64590	0.927695	0.65725	0.939126	0.66778	0.969678	0.70511
5	1st	1.615483	2.96615	1.855597	3.28201	2.167270	3.70686	2.28859	3.87568	2.397334	4.02836	2.759991	4.54496
	2nd	1.171481	0.85227	1.253997	0.91452	1.338222	1.00091	1.365355	1.03593	1.387424	1.06790	1.448268	1.17781
	3rd	0.881244	0.5	0.914804	0.5	0.946002	0.5	0.955447	0.5	0.962918	0.5	0.982579	0.5
6	1st	1.756451	4.15611	1.948596	4.63290	2.172402	5.26890	2.25195	5.52042	2.320024	5.74741	2.523787	6.51285
	2nd	1.149240	1.21335	1.198337	1.33157	1.245237	1.49172	1.259684	1.55565	1.271197	1.61360	1.301880	1.81038
	3rd	0.916641	0.58116	0.940973	0.59946	0.963178	0.62595	0.969819	0.63703	0.975039	0.64729	0.98868	0.68364
7	1st	2.324662	5.56621	2.654069	6.23324	3.083470	7.11866	3.25098	7.46782	3.401361	7.78256	3.903658	8.84180
	2nd	1.636715	1.66357	1.740220	1.84721	1.846040	2.09299	1.880194	2.19039	1.907996	2.27837	1.984678	2.57555
	3rd	1.120624	0.78823	1.152233	0.84640	1.181433	0.92694	1.19024	0.95956	1.197203	0.98931	1.215466	1.09155
	4th	0.938430	0.5	0.956755	0.5	0.973283	0.5	0.97819	0.5	0.982039	0.5	0.992044	0.5
8	1st	2.371354	7.19539	2.620614	8.08190	2.911717	9.25500	3.015318	9.71678	3.103759	10.1327	3.369953	11.5308
	2nd	1.483317	2.19456	1.550051	2.45282	1.604261	2.79620	1.620956	2.93174	1.634281	3.05398	1.669811	3.46567
	3rd	1.096900	1.07710	1.118806	1.18296	1.138693	1.32615	1.144623	1.38326	1.149280	1.43501	1.161427	1.61068
	4th	0.952717	0.57503	0.966968	0.59318	0.97972	0.61944	0.98349	0.63041	0.986436	0.64058	0.994085	0.67657

HIGHER ORDER BANDPASS FILTER (Fig. 11)



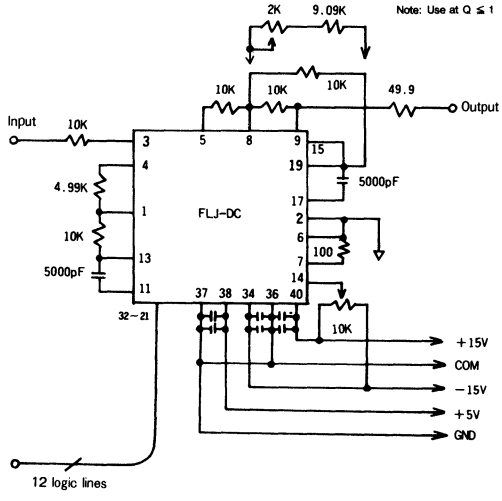
BANDPASS FILTER (1 POLE-PAIR, 2 POLE-PAIR, 3 POLE-PAIR) (Table 11)

(Total $|G|=1$, $Q=2, 5, 4.32, 10$ $fo=10\sim15.99$KHz) (See Fig. 11)

	1 pole-pair, Inverting			2 pole-pair, Non-Inverting			3 pole-pair, Inverting			
Q	2	5	10	2	5	10	2	4.32 (1/3oct)	5	10
C_{EXT1}	5000pF	5000pF	5000pF	4182pF	4658pF	4826pF	4027pF	4523pF	4585pF	4788pF
C_{EXT2}				5978pF	5367pF	5180pF	5000pF	5000pF	5000pF	5000pF
C_{EXT3}							6208pF	5527pF	5452pF	5221pF
R_{G1}	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G2}	49.9Ω	49.9Ω	49.9Ω	4.87KΩ	4.99KΩ	4.99KΩ	10KΩ	10KΩ	10KΩ	10KΩ
R_{G3}				49.9Ω	49.9Ω	49.9Ω	2.37KΩ	2.49KΩ	2.49KΩ	2.49KΩ
R_{Q1}	4.99KΩ	1.24KΩ	562Ω	2.67KΩ	825Ω	383Ω	1.62KΩ	649Ω	549Ω	261Ω
R_{Q2}				3.74KΩ	887Ω	392Ω	4.99KΩ	1.5KΩ	1.24KΩ	549Ω
R_{Q3}							3.40KΩ	806Ω	665Ω	287Ω
f_1	1.0	1.0	1.0	1.19550	1.07340	1.03600	1.24166	1.10547	1.09046	1.04425
f_2				0.83647	0.93162	0.965251	1.0	1.0	1.0	1.0
f_3							0.80537	0.90459	0.91704	0.95763
Q_1	2.0	5.0	10.0	2.87	7.09	14.15	4.094	8.68040	10.04	20.01
Q_2				2.87	7.09	14.15	2.00000	4.31847	5.0000	10.000
Q_3							4.094	8.68040	10.04	20.01
Gain				6.30dB	6.06dB	6.03dB	12.45dB	12.13dB	12.11dB	12.06dB

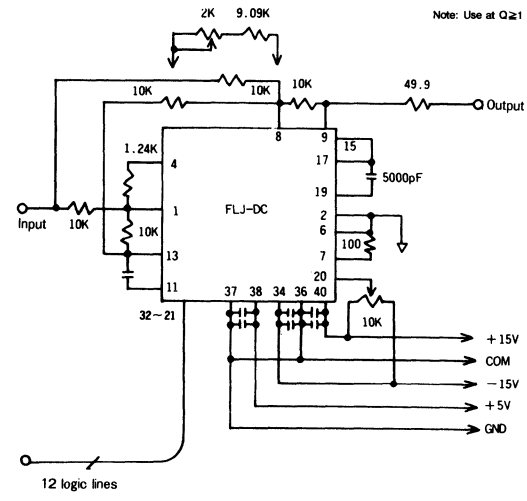
1POLE-PAIR(2 POLE)BAND ELIMINATION FILTER (Fig. 12)

Non-Inverting (LP + HP, fc: 10Hz ~ 15.99KHz)



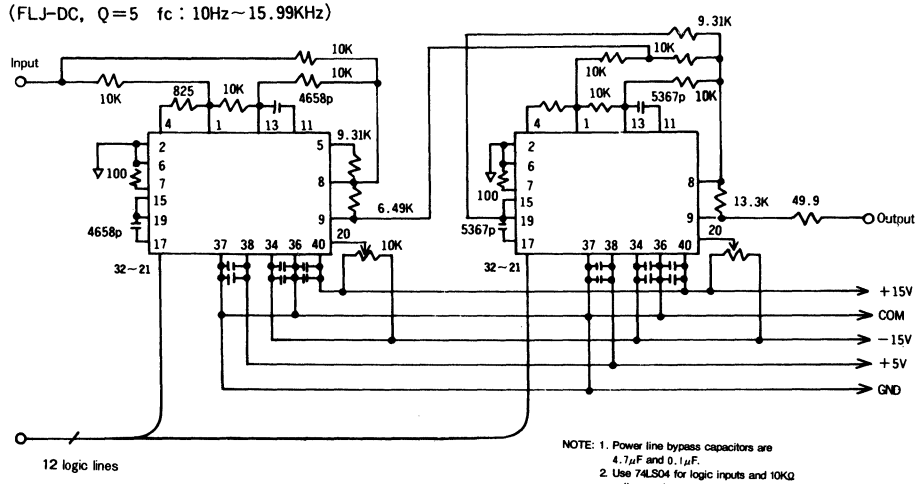
1POLE-PAIR(2 POLE)BAND ELIMINATION FILTER (Fig. 13)

Inverting (I-BP, fc: 10Hz ~ 15.99KHz) Q = 5



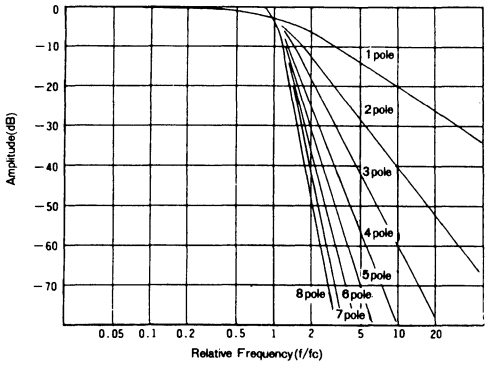
2POLE-PAIR(4 POLE)BAND ELIMINATION FILTER (Fig. 14)

(FLJ-DC, Q = 5 fc : 10Hz ~ 15.99KHz)

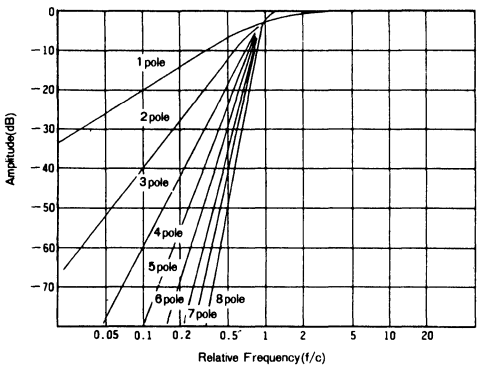


NOTE: 1. Power line bypass capacitors are 4.7μF and 0.1μF.
2. Use 74LS04 for logic inputs and 10KΩ pull-up resistors to +5V.

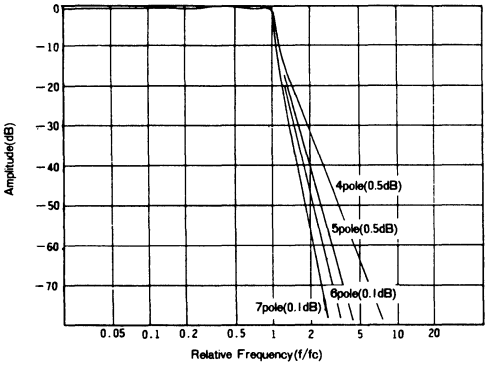
LOWPASS, BUTTERWORTH (Fig. 15)



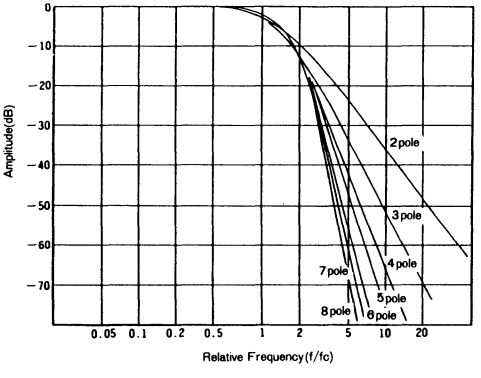
HIGHPASS, BUTTERWORTH (Fig. 16)



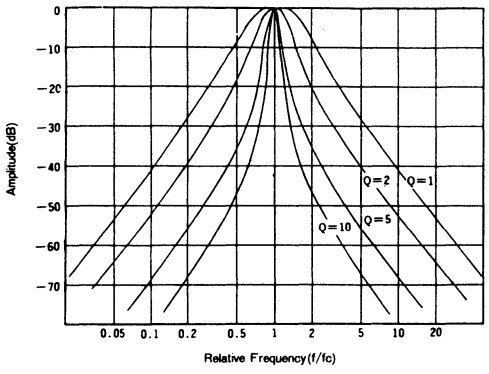
LOWPASS, CHEBYSHEV (Fig. 17)



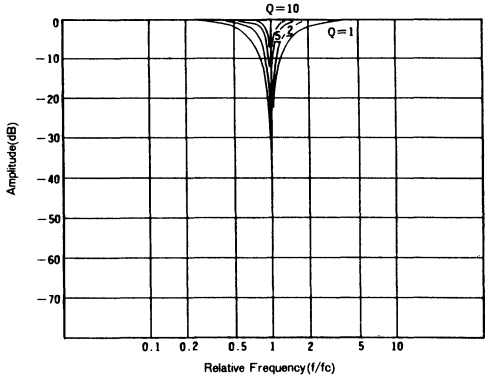
LOWPASS, BESSEL (Fig. 18)



BANDPASS, 2 POLE-PAIR(4 POLE) (Fig. 19)

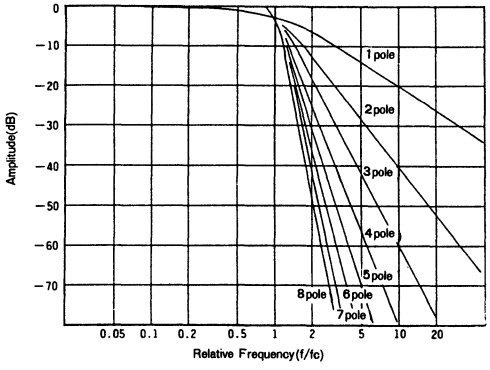


BAND ELIMINATION, 1 POLE-PAIR(2 POLE) (Fig. 20)

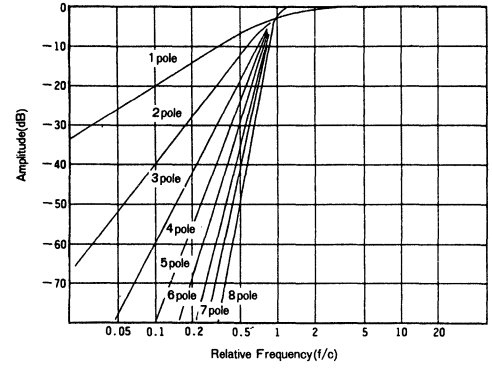


6

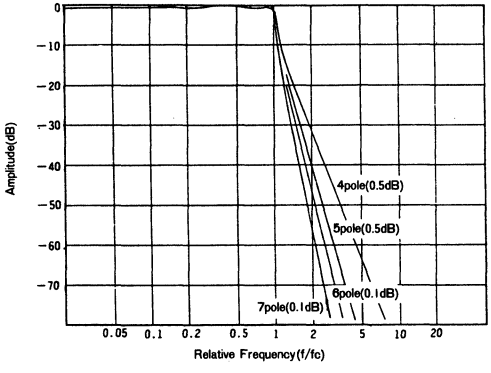
LOWPASS, BUTTERWORTH (Fig. 15)



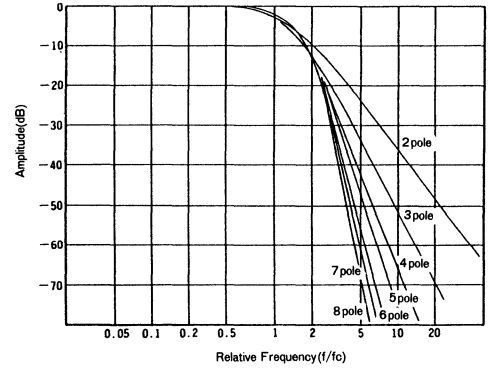
HIGHPASS, BUTTERWORTH (Fig. 16)



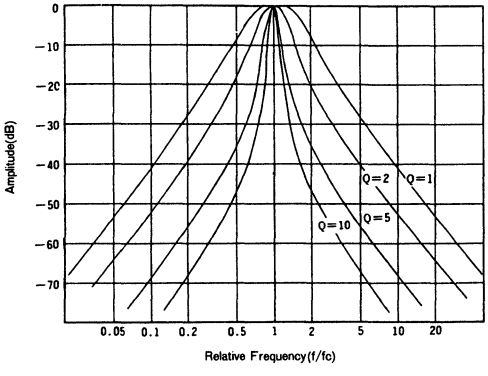
LOWPASS, CHEBYSHEV (Fig. 17)



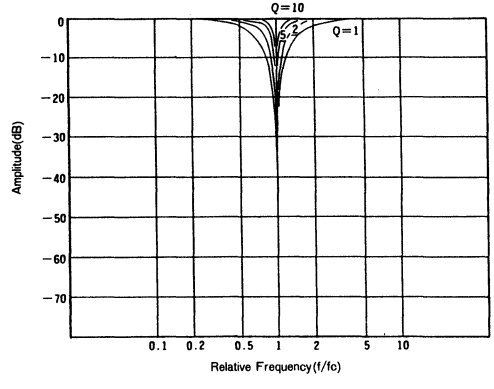
LOWPASS, BESSEL (Fig. 18)



BANDPASS, 2 POLE-PAIR(4 POLE) (Fig. 19)



BAND ELIMINATION, 1 POLE-PAIR(2 POLE) (Fig. 20)



FLJ-D5,D6
DIGITAL-PROGRAMMABLE, HIGH-ORDER LOWPASS FILTER

FEATURES

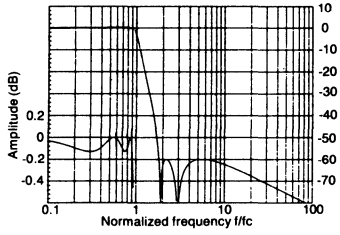
- **60dB, 80dB/octave rolloff lowpass filter**
- **Cutoff frequency programmed by logic at 8 points**
- **Compact, lightweight, hybrid IC construction**

GENERAL DESCRIPTION

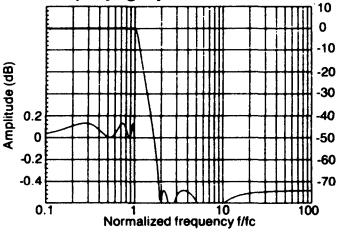
The FLJ-D5 and -D6 series are lowpass filters that although are compact, have higher order and high attenuation performance. They are Chebyshev type filters. The FLJ-D5LA is a 5-pole filter which has a rolloff of 60 dB/oct and the FLJ-D6LA is a 6-pole filter with a rolloff of 80 dB/oct. The cutoff frequency is programmed with 3-bit, TTL-compatible digital logic and the settings can be changed to 8 different levels. Cutoff frequency range of the lower range type which has suffix 1 is 10Hz-2kHz, and the higher range type has suffix 2 is 100Hz-20KHz.

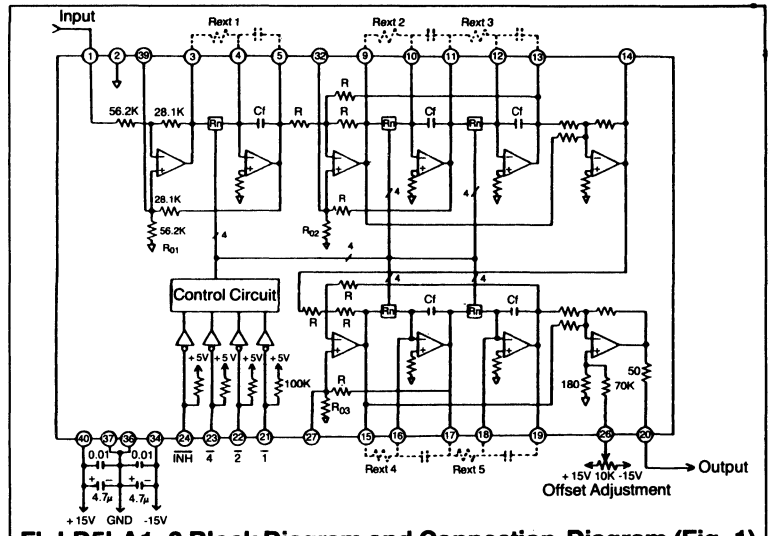
Ripple within the pass band is minimal at 0.13dBp-p and the distortion rate is held extremely low at 0.05%. These filters are optimal as anti-aliasing filters in A/D conversion circuits of data acquisition systems.

FLJ-D5LA1, 2 (Fig. 4)



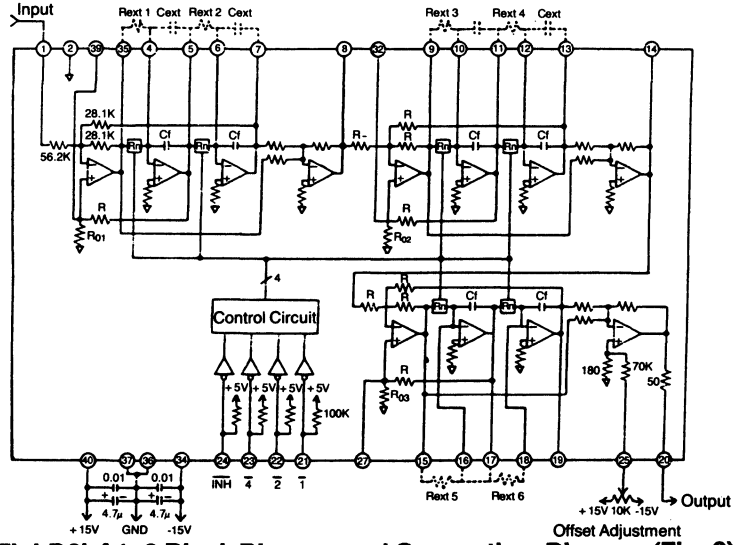
FLJ-D6LA1, 2 (Fig. 5)





FLJ-D5LA1, 2 Block Diagram and Connection Diagram (Fig. 1)

Cf in the diagram is 10000pF for the Suffix 1 model and 1000pF for the Suffix 2 model.



FLJ-D6LA1, 2 Block Diagram and Connection Diagram (Fig. 2)

Cf in the diagram is 10000pF for.the Suffix 1 model and 1000pF for the Suffix 2 model.

ORDERING INFORMATION

Low Cutoff Frequency Type (10Hz-2KHz)

FLJ-D5LA1: 60dB/oct., 5-pole lowpass, Chebyshev

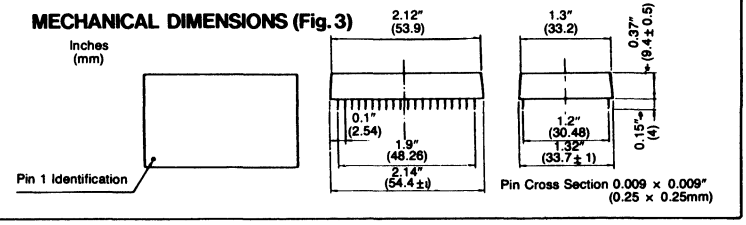
FLJ-D6LA1: 80dB/oct., 6-pole lowpass, Chebyshev

High Cutoff Frequency Type (100Hz-20KHz)

FLJ-D5LA2: 60dB/oct., 5-pole lowpass, Chebyshev

FLJ-D6LA2: 80dB/oct., 6-pole lowpass, Chebyshev

MECHANICAL DIMENSIONS (Fig. 3)



SPECIFICATIONS (Table 1)

Typical at 25°C and ±15V supply voltage unless otherwise specified.

ABSOLUTE RATINGS

Supply voltage (±Vs) ..... ±16V
Input voltage ..... ±Vs
Logic input voltage ..... +5.5V

FILTER CHARACTERISTICS, CUTOFF FREQUENCY

Low Range (10, 20, 50, 100, 200, 500, 1K, 2KHz, 8 points programmable, at -3dB)
FLJ-D5LA1 ..... 5-pole Chebyshev
FLJ-D6LA1 ..... 6-pole Chebyshev
High Range (100, 200, 500, 1K, 2K, 5K, 10K, 20KHz, 8 points programmable, at 0dB)
FLJ-D5LA2 ..... 5-pole Chebyshev
FLJ-D6LA2 ..... 6-pole Chebyshev
Setting of Cutoff Frequency ... 3-bit binary, TTL-compatible

Model 1	Model 2	Control $\overline{INH}$	$\overline{4}$	$\overline{2}$	$\overline{1}$
10Hz	100Hz	0	0	0	0
20	200	0	0	0	1
50	500	0	0	1	0
100	1KHz	0	0	1	1
200	2K	0	1	0	0
500	5K	0	1	0	1
1K	10K	0	1	1	0
2K	20K	0	1	1	1

"0": +5V or OPEN
"1": 0V

Accuracy of setting of cutoff frequency ..... ±3%max.

PASS BAND CHARACTERISTICS

Gain	0dB±0.3dBmax. (0.05fc)
Ripple	0.13dBp-p (central designed value)
Distortion rate	0.05%

ROLLOFF CHARACTERISTICS

	FLJ-D5LA1,2	FLJ-D6LA1,2
Rolloff	60dB/oct	80dB/oct
Attenuation volume	60dB (1.82fc)	74dB (1.9fc)
Minimum attenuation	60dB	74dB
Attenuation at 10fc-1MHz	55dBmin.	60dBmin.

INPUT CHARACTERISTICS

Input impedance	50KΩmin.
Maximum input voltage	±10Vmin.

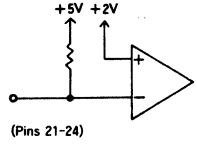
OUTPUT CHARACTERISTICS

Output impedance	100Ωmax.
Maximum output voltage	±10Vmin.
Noise (input shorted)	140μVrms max. (BW10Hz-500KHz)
Offset voltage	10mV adjustable

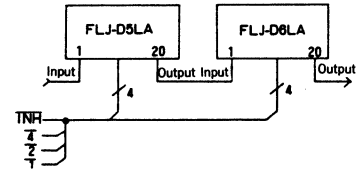
POWER SUPPLY AND ENVIRONMENTAL CONDITIONS

Supply voltage	±15V ±1Vmax.
Power consumption current	±28mA (FLJ-D5), ±33mA (FLJ-D6)
Operating temperature/ Humidity range	-20°C to +70°C, 10%-95%RH
Storage temperature/ Humidity range	-30°C to +80°C, 10%-80%RH

LOGIC INPUT PINS (Fig. 6)



CASCADE WIRING DIAGRAM (Fig. 7)



TECHNICAL NOTES

1. Use a series-type power supply for the FLJ-D5 and -D6, because a switching-type power supply is not recommended. Install 0.01μF multilayer ceramic and 4.7μF tantalum bypass capacitors in parallel as close to the filter as possible.
2. Each logic input (Pins 21-24) which programs the cutoff frequency has an internal analog comparator as shown in Fig. 6. External logic signals are TTL-compatible.
3. The fc setting input logic is negative true. Terminal open or +5V represents logic "0", while GND level is logic "1". The $\overline{INH}$ terminal is used normally open. Once $\overline{INH}$ is given logic "1", all $\overline{4}$, $\overline{2}$ and $\overline{1}$ logic inputs are inhibited and all internal resistor network switches are opened. The fc setting with external resistors becomes available with logic "1" at this $\overline{INH}$ terminal. The relationship between fc and the external resistors in this case is as follows:

FLJ-D5LA1 (Low Range Type)

$$Rext1 = \frac{31.423 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext2 = Rext3 = \frac{21.399 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext4 = Rext5 = \frac{16.358 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

FLJ-D6LA1 (Low Range Type)

$$Rext1 = Rext2 = \frac{29.622 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext3 = Rext4 = \frac{18.633 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext5 = Rext6 = \frac{15.215 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

FLJ-D5LA2 (High Range Type)

$$Rext1 = \frac{314.23 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext2 = Rext3 = \frac{213.99 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext4 = Rext5 = \frac{163.58 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

FLJ-D6LA2 (High Range Type)

$$Rext1 = Rext2 = \frac{296.22 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext3 = Rext4 = \frac{186.33 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext5 = Rext6 = \frac{152.15 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

4. An 11-pole ultra-high attenuation filter is available once cascaded as shown in Fig. 7. As can be seen from the curves (Figs. 4,5), the amplitude of the ripple in the pass band is reversed between FLJ-D5LA and FLJ-D6LA. As a result, when connected in a cascade, the pass band ripple amplitude is greatly reduced, and moreover, the rolloff becomes steeper.
5. For filters that have been constructed like those in this series, it is not recommended to change the fc setting range with external capacitors. This is because trimming of the internal constants is performed with pairs of internal resistors and capacitors. Although shifting to a lower fc setting range is possible through the addition of external capacitors, in this case a change will result in ripple amplitude.

FLJ-R SERIES HIGHER ORDER, RESISTOR-TUNEABLE FILTER

FEATURES

- **135dB, 100dB/octave high order, lowpass filter**
- **1/3 octave bandwith (Q = 4.32) bandpass filter**
- **Can set cutoff (fc) frequency with 6 or 8 external resistors**
- **Ultra-compact size, high-function hybrid construction**

GENERAL DESCRIPTION

The FLJ-R series filters are of the highest order and have the highest attenuation characteristics among the entire group of DATEL filter products. Through the use of hybrid techniques, even though compact in size, the FLJ-R series filters have complete 8-pole lowpass and 3-pole pair bandpass filter functions. The cutoff (central) frequency can be set with only 8 or 16 external resistors.

Bandpass ripple in the lowpass filter is 0.1dB and boasts outstanding performance with the distortion ratio for all models being a mere 0.005%. Each model is composed of the Suffix 1 and Suffix 2 types and varies according to cutoff frequency setting range. The Suffix 1 model has a range from 10Hz-2KHz and the Suffix 2 model has a range from 100 Hz-20KHz. The FLJ-R series filters are optimum as anti-aliasing filters in A/D conversion circuits of data acquisition systems.

The FLJ-R3BA1,2 are 1/3 octave, bandpass filters that meet IEC-225 Standard requirements.

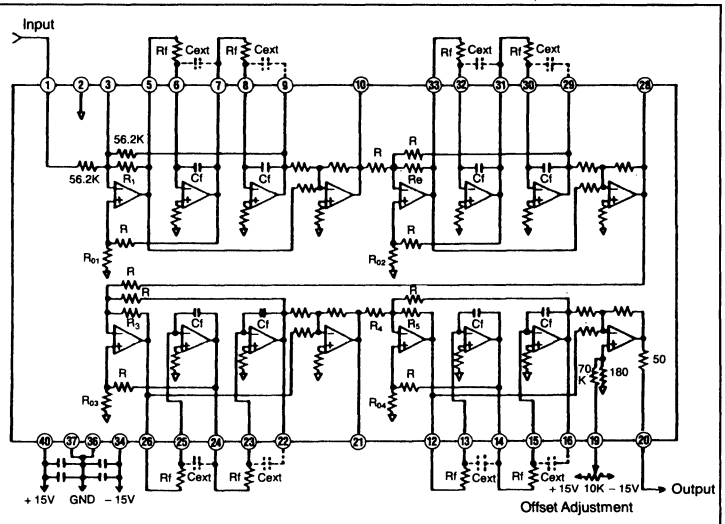
ORDERING INFORMATION

Low Cutoff Frequency Type (10Hz-2KHz)

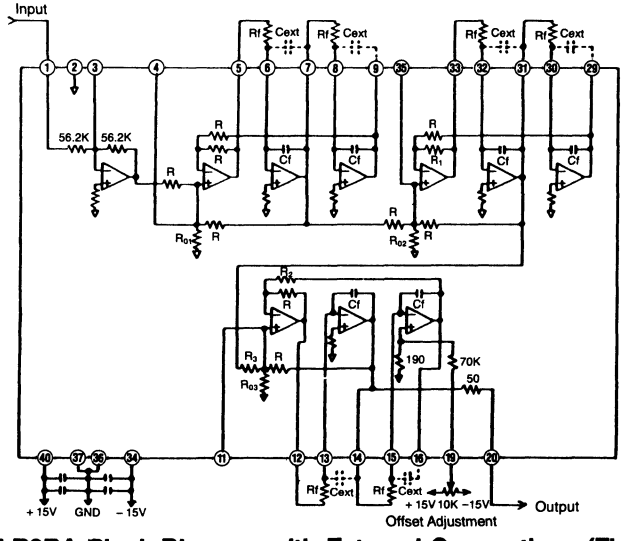
FLJ-R8LA1: 135dB/oct., 8-pole lowpass, Chebyshev
FLJ-R8LB1: 100dB/oct., 8-pole lowpass, Chebyshev
FLJ-R3BA1: 3-pole pair bandpass

High Cutoff Frequency Type (100Hz-20KHz)

FLJ-R8LA2: 135dB/oct., 8-pole lowpass, Chebyshev
FLJ-R8LB2: 100dB/oct., 8-pole lowpass, Chebyshev
FLJ-R3BA2: 3-pole pair bandpass

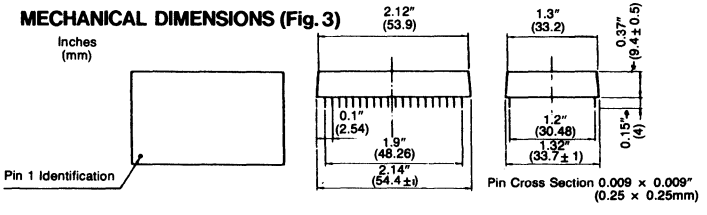


FLJ-R8LA, B Block Diagram with External Connections (Fig. 1)



FLJ-R3BA Block Diagram with External Connections (Fig. 2)

MECHANICAL DIMENSIONS (Fig. 3)



SPECIFICATIONS

Typical at 25°C and ±15V supply voltage unless otherwise specified.

ABSOLUTE RATINGS

Supply voltage (±Vs) ..... ±18V
Input voltage ..... ±Vs

FILTER CHARACTERISTICS	
fc setting range	Suffix 1: 10Hz-2KHz Suffix 2: 100Hz-20KHz
fc setting	8 equivalent lowpass or 6 equivalent bandpass external resistors
fc setting accuracy	±2%max.

PASS BAND CHARACTERISTICS	FLJ-R8LA,B	FLJ-R3BA
Gain	0dB±0.1dBmax.	0dB±1dBmax.
Gain after Rf adjustment	—	0dB±
Ripple p-p	0.15dB	—
Ripple ≦0.9fc	0.3dBmax.	—
Ripple after Rf adjust	0.1dB	—
Distortion ratio	0.005%@1KHz	*Same as left

ROLLOFF CHARACTERISTICS	FLJ-R8LA	FLJ-R8LB	FLJ-R3BA
Attenuation rolloff	135dB/oct	100dB/oct	—
Q	—	—	4.32(BW1/3oct)
Attenuation volume	86dB@1.56fc	92dB@2.0fc	18dB/octBW
Minimum attenuation	86dB	106dB	—
Attenuation at 10fc-1MHz	80dBmin.	86dBmin.	80dBmin.

INPUT CHARACTERISTICS	
Input impedance	50KΩmin.
Maximum input voltage	±10Vmin.

OUTPUT CHARACTERISTICS	
Output impedance	100Ωmax.
Maximum output voltage	±10Vmin.
Noise (input shorted)	140μVrms max. (BW10-500KHz)
Offset voltage	±10mV zero adjustable

POWER SUPPLY AND ENVIRONMENTAL CONDITIONS	
Supply voltage (operating range)	±15V (±5V-±18V)
Power consumption current	40mA (FLJ-R8), 25mA (FLJ-R3)
Operating temperature/ Humidity range	-20°C to +70°C, 10%-95%RH
Storage temperature/ Humidity range	-30°C to +80°C, 10%-80%RH

TECHNICAL NOTES

1. Setting the cutoff (central) frequency is accomplished with 8 external resistors which are equal in value for lowpass filters and 6 external resistors which are equal in value for bandpass filters. The relationship between the resistance Rf of the external resistors and the cutoff frequency fc is as follows:

Suffix 1 model (10Hz-2KHz) $Rf = \frac{15.9 \times 10^3}{fc} (K\Omega)$ *Suffix 2 model (100Hz-20KHz)* $Rf = \frac{159 \times 10^3}{fc} (K\Omega)$

where fc is measured in Hz.

The FC setting range can be shifted to a lower band by adding external capacitors Cext. The equation shown below should be used for reference.

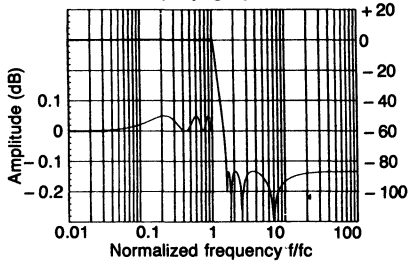
Suffix 1 model $Cext = \frac{159}{(Cext + 0.01) \times fc} (K\Omega)$ *Suffix 2 model* $Cext = \frac{159}{(Cext + 0.001) \times fc} (K\Omega)$

where Cext is measured in μF and fc in Hz.

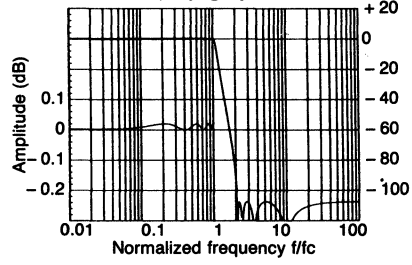
In this case, the external capacitors should have high dielectric characteristics. It is recommended to use multilayer ceramic capacitors. Further, tolerance of these capacitors should be within ±0.25%. For filters such as these of higher order and with high attenuation characteristics, the uniformity of the tolerance of external resistors and capacitors has an effect not only on the accuracy of the setting range, but also on the size of pass band ripple.

2. Use series type power supplies for the ±15V power supplies because switching-type power supplies are not recommended. Install 4.7μF tantalum and 0.01μF multilayer ceramic bypass capacitors. It is recommended that these be installed in parallel, and as close to the filter as possible, between the ±15V power supplies and ground.
3. Use metal film resistors with a tolerance better than 1% for the 6 or 8 fc setting resistors.

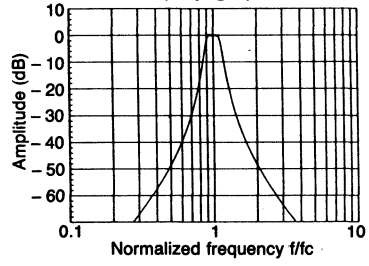
FLJ-R8LA1, 2 (Fig. 4)



FLJ-R8LB1, 2 (Fig. 5)



FLJ-R3BA1, 2 (Fig. 6)



DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

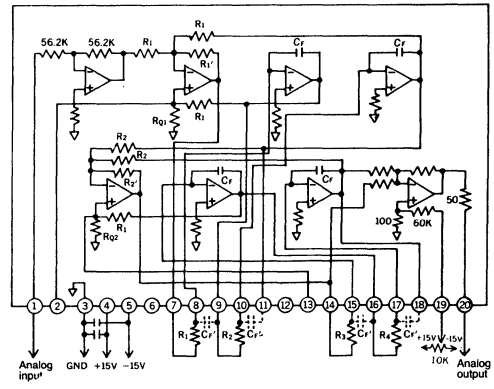
FLJ-UR Series
Single In-line Hybrid
Resistor Tuneable Filter

FEATURES

- **Small and thin size**
- **A variety of families**
- **Cutoff frequency fc is set by only two or four resistors**
- **Light weight, low cost**

GENERAL DESCRIPTION

The FLJ-UR series filters are single in-line package resistor tuneable filters. They are small in size and can reduce installation space on the printed circuit board. The cutoff frequency can be easily set by only two or four external resistors. The series have a variety of products, allowing system designers to make a wide-ranging selection to suit the applications.



FLJ-UR4LB1/2 Block Diagram (Fig. 1)

6

LOW CUTOFF FREQUENCY TYPE (40 Hz~1.6 kHz)

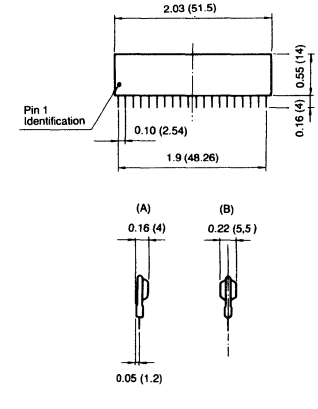
FLJ-UR4LA1: 4-pole lowpass, Butterworth
FLJ-UR4LB1: 4-pole lowpass, Chebyshev
FLJ-UR4HA1: 4-pole highpass, Butterworth
FLJ-UR4HB1: 4-pole highpass, Chebyshev
FLJ-UR2LH1: 2-pole lowpass/highpass, Butterworth
FLJ-UR1BA1: 1-pole pair bandpass, Butterworth
FLJ-UR2BA1: 2-pole pair bandpass, Butterworth
FLJ-UR2EA1: 2-pole pair band elimination, Butterworth

HIGH CUTOFF FREQUENCY TYPE (400 Hz~5 k/10 k/20 kHz)

FLJ-UR4LA2: 4-pole lowpass, Butterworth
FLJ-UR4LB2: 4-pole lowpass, Chebyshev
FLJ-UR4HA2: 4-pole highpass, Butterworth
FLJ-UR4HB2: 4-pole highpass, Chebyshev
FLJ-UR2LH2: 2-pole highpass/lowpass, Butterworth
FLJ-UR1BA2: 1-pole pair bandpass, Butterworth
FLJ-UR2BA2: 2-pole pair bandpass, Butterworth
FLJ-UR2EA2: 2-pole pair band elimination, Butterworth

MECHANICAL DIMENSIONS (Fig. 2)

INCHES (mm)



SPECIFICATIONS

Typical at R=31.8 kΩ, 25°C and ±15V supply voltage unless otherwise specified.

COMMON SPECIFICATIONS TO ALL MODELS

ABSOLUTE RATINGS

Supply voltage (±Vs) ....±18V
Input voltage.....±Vs

FREQUENCY CHARACTERISTICS

fc accuracy.....±3% max.
(with 0 dB gain at the frequency given in Note *2)

INPUT CHARACTERISTICS

Input Impedance.....50 kΩ min.
Maximum Input Voltage ±10V

OUTPUT CHARACTERISTICS

Output Impedance .....100Ω max.
Maximum Output Voltage ...±10V min.
Load Resistance.....10 kΩ min.
Noise (10~500 kHz).....140 μV max.
Offset Voltage .....±30 mV max. zero adjustable

POWER SUPPLY AND ENVIRONMENTS

Supply Voltage.....±15V
Supply Voltage,
Operating Range.....±5V~±18V
Operating Temerature/
Humidity Range .....−20°C~70°C, 10~95%RH
Storage Temperature/
Humidity Range .....−30°C~80°C, 10~80%RH

SPECIFICATIONS 1 (4 POLE MODELS)

No. of poles/characteristics		4-pole lowpass	4-pole lowpass	4-pole highpass	4-pole highpass
Type		Butterworth	Chebyshev	Butterworth	Chebyshev
Model		FLJ-UR4LA	FLJ-UR4LB	FLJ-UR4HA	FLJ-UR4HB
fc (−3 dB) characteristics					
Range*1	Suffix 1 model	40 Hz~1.6 kHz	*Same as left	*Same as left	*Same as left
	Suffix 2 model	400 Hz~20 kHz	•	400 Hz~5 kHz	•
Setting		by 4 external resistors	•	•	•
Pass band characteristics					
Gain*2		0 dB±0.3 dB	•	0 dB±1 dB	•
Ripple		—	0.28 dBp-p	—	0.28 dBp-p
Upper-limit frequency (small signal)		—	—	50 kHz±1 dB max.*3	•
Rolloff characteristics					
Rolloff		24 dB/oct	42 dB/oct or equivalent	24 dB/oct	42 dB/oct or equivalent
Attenuation volume (1/2 fc or 2 fc)		24 dB	55 dB	24 dB	55 dB
Minimum attenuation		—	46 dB	—	46 dB
Attenuation at 1 MHz		70 dB min.	•	—	—
Output characteristics					
Offset drift		30 μV/°C	•	15 μV/°C	•
Distortion rate*2		0.01%	•	0.1%	•
Slew rate		—	—	2V/μsec	•
Quiescent current/package					
Quiescent current (@±15V)		±12 mA	±16 mA	±8 mA	±16 mA
Package		20 pins SIP (A)	•	•	•

SPECIFICATIONS 2 (2 POLE AND 1 POLE PAIR MODELS)

No. of poles/characteristics		2-pole high lowpass	1-pole pair bandpass	2-pole pair bandpass	2-pole pair band elimination
Type		Butterworth	Butterworth	Butterworth	Butterworth
Model		FLJ-UR2LH	FLJ-UR1BA	FLJ-UR2BA	FLJ-UR2EA
fc (−3 dB) characteristics					
Range*1	Suffix 1 model	40 Hz~1.6 kHz	*Same as left	*Same as left	*Same as left
	Suffix 2 model	400 Hz~20 kHz	400 Hz~10 kHz	•	•
Setting		by 2 external resistors	•	by 4 external resistors	•
Pass band characteristics					
Gain*2		0 dB±0.3 dB	0 dB±1 dB	•	0 dB±0.3 dB
Upper-limit frequency (small signal)*3		100 kHz±1 dB HPF	—	—	50 kHz±1 dB max.
Rolloff characteristics					
Rolloff		12 dB/oct	—	—	—
Q		—	5 *4	5	5
Attenuation volume (1/2 fc or 2 fc)		12 dB	17.5 dB	35 dB	—
Attenuation at 1 MHz		−70 dB min. LPF	•	•	—
Maximum attenuation (f_0)		—	—	—	60 dB
Output characteristics					
Offset drift		15 μV/°C	•	•	30 μV/°C
Distortion rate*2		0.1%	0.01%	•	•
Slew rate		2V/μsec HPF	—	—	2V/μsec
Quiescent current/package					
Quiescent current (@±15V)		±8 mA	•	±12 mA	±20 mA
Package		20 pins SIP (A)	•	•	20 pins SIP (B)

*1: Addition of 2 or 4 external capacitors allow extension to lower band.
*2: FLJ-UR4LA, 4LB; fc/10, FLJ-UR4HA; 3.3 fc, FLJ-UR4HB; 10 fc (fc≦3 kHz), 3.3 fc (fc>3 kHz)
FLJ-UR2LH; fc/10 (LPF), 10 fc (HPF)
*3: Gain of 0 dB at above stated frequencies. (See *2)
*4: Connection of a specified pin to GND allow 10, 20, 30, 40 and 50. External resistors allow a range of 1.81≦Q≦50.

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TECHNICAL NOTES

1. Do not use a switching regulator but use a well regulated ±15V power supply. Install 0.01 μF bypass capacitors as close to the filter as possible.
2. Use metal film resistors of 1% tolerance for fc setting. When making a higher-order filter, use more accurate resistors.
3. Connect external resistors with short leads as close to the filter as possible.
4. Use external capacitors with good stability and high dielectric resistance. It is recommended to use multilayer ceramic capacitors or plastic film capacitors.
5. Regulate output offset voltage by using an external trimmer (10 kΩ to 50 kΩ).
6. The FLJ-UR series filters are packaged in single inline and are compact in size. Installation at high-density may cause temperature rises between elements. Installation with 0.8" or more of space between filters can eliminate the problem.
7. Relation between fc and external resistor/capacitor
   With the FLJ-UR series, a cutoff or center frequency can be set by 2 or 4 external resistors. The values of R of 2 or 4 external resistors for normal use can be calculated as;

$$R = \frac{15.9\times10^6}{fc\ (Hz)}\ (\Omega) \quad \text{Suffix 1 model}$$

$$R = \frac{159\times10^6}{fc\ (Hz)}\ (\Omega) \quad \text{Suffix 2 model}$$

   In the applications given later, the resistance of each of 2 or 4 resistors may be changed. R_1 to R_4 shown in the block diagrams are the external resistors explained here. In the standard use, the fc can be set to a minimum of 40 Hz. This is because the values of R have to be increased to about 400K according to the relation between R and fc. The fc setting range can be expanded to lower band by adding 2 or 4 external capacitors.

$$R = \frac{159\times10^3}{(Cext+0.01)\ fc}\ (\Omega) \quad \text{Suffix 1 model}$$

$$R = \frac{159\times10^3}{(Cext+0.001)\ fc}\ (\Omega) \quad \text{Suffix 2 model}$$

   where Cext is measured in μF and Fc in Hz.

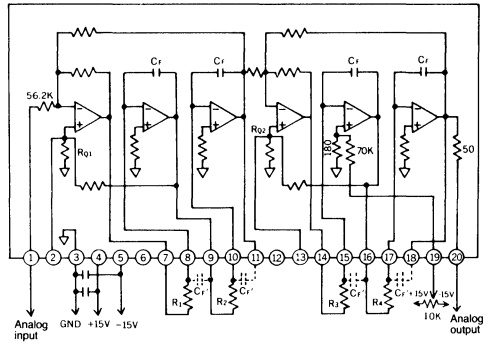
   In the applications in which the output offset, time drift, or output noise must be minimal, use the above external capacitors if the values of external resistors exceed 100 kΩ each.

8. How to tune fc
   As shown in the specifications, the fc setting accuracy is 3% depending on the accuracy of elements used. There is no practical problem in tuning when they are used as lowpass or highpass filters. However, bandpass filters and band elimination filters may require sharp tuning. Such filters can be tuned with external trimmers as shown in Fig. 10. R_1, R_2 and VR_1 are not used with the FLJ-UR1BA1/2.

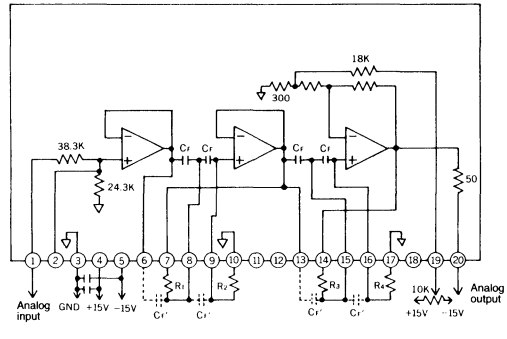
   a. FLJ-UR1BA1/2
   - An input signal of oscillating frequency fc is given.
   - I/O signals are monitored with a phase measuring instrument such as an oscilloscope.
   - Tune VR_2 until the phase difference between I/O signals can be reduced to 0°.

   b. FLJ-UR2BA1/2
   - An input frequency of 1.0734×fc is provided.
   - Tune VR_1 until the phase difference between the input signal and the output signal at pin 9 reaches at 180° looking at a phase measuring instrument such as an oscilloscope.
   - An input signal of frequency fc is given.
   - Tune VR_2 until the phase difference between the input signal and the output signal at pin 20 set to 0°

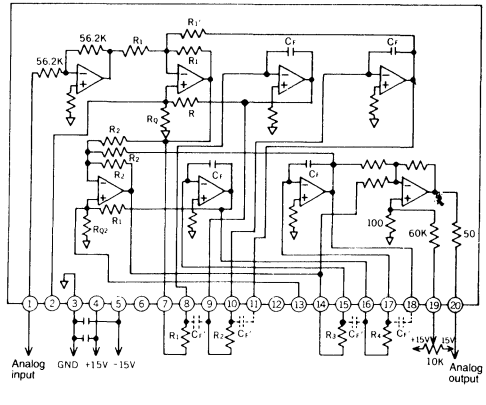
FLJ-UR4LA1/2 Block Diagram (Fig. 3)



FLJ-UR4HA1/2 Block Diagram (Fig. 4)

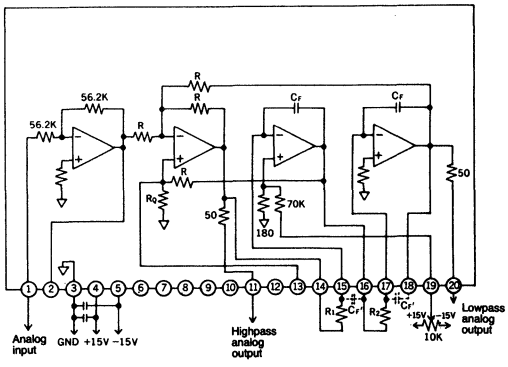


FLJ-UR4HB1/2 Block Diagram (Fig. 5)

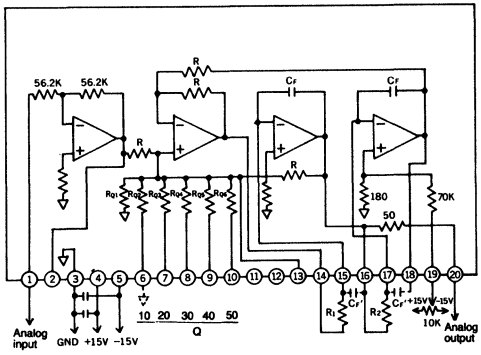


Cf in each figure is 10000 pF for suffix 1 model and 1000 pF for suffix 2 model.

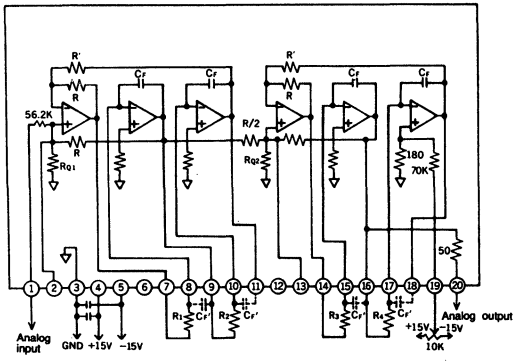
FLJ-UR2LH1/2 Block Diagram (Fig. 6)



FLJ-UR1BA1/2 Block Diagram (Fig. 7)



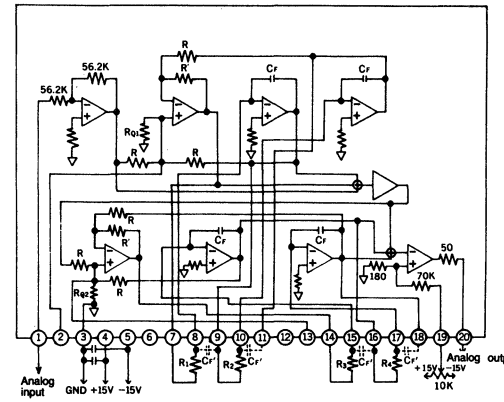
FLJ-UR2BA1/2 Block Diagram (Fig. 8)



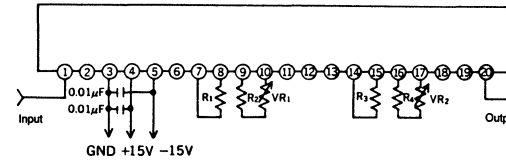
Cf in each figure is 10000 pF for suffix 1 model and 1000 pF for suffix 2 model.

20Cext

FLJ-UR2EA1/2 Block Diagram (Fig. 9)



fc tuning method (Fig. 10)



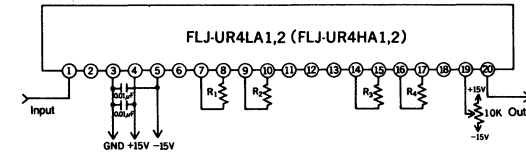
APPLICATIONS

This section illustrates configuration examples of filters with various characteristics in which external resistors are changed or 2 filters are used. Each application is provided with a circuit diagram and a table of resistor values. The first example explains how to look up the table of resistor values in detail. This can be applied to the others.

1. A 4-pole Bessel or Chebyshev filter (pass band ripple of 0.5 dB) modified from FLJ-UR4LA1/2

   The circuit diagram is shown in Fig. 11.

(Fig. 11)



Install external resistors with the resistance obtained from Table 1 in the procedure given below. In the standard application of FLJ-UR4LA1/2, the relation between fc and R (external resistor) is:

$$R = \frac{15.9\times10^6}{fc\ (Hz)}\ (\Omega);\ \text{FLJ-UR4LA1}$$

$$R = \frac{159\times10^6}{fc\ (Hz)}\ (\Omega);\ \text{FLJ-UR4LA2}$$

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Obtain R that corresponds to the desired fc from the above equation first. (In a standard application, the R calculated here serves as R_1, R_2, R_3 or R_4 shown in Fig. 11.)

Based on the R calculated here, obtain external resistance R_1, R_2, R_3 and R_4 referring to Table 1. For example, a Bessel lowpass filter has:

$R_1 = 0.673 \times R$
$R_2 = 0.712 \times R$
$R_3 = 0.384 \times R$
$R_4 = 1.014 \times R$

Design Example

A Chebyshev lowpass filter (pass band ripple of 0.5 dB) with fc = 4 kHz using FLJ-UR4LA2

From $R = \dfrac{159 \times 10^6}{fc\ (Hz)}$

$$R = \frac{159 \times 10^6}{4 \times 10^3} = 39.75\ k\Omega$$

From Table 1,

$R_1 = 2.182R = 2.182 \times 39.75\ k\Omega = 86.73\ k\Omega$
$R_2 = 1.286R = 1.286 \times 39.75\ k\Omega = 51.12\ k\Omega$
$R_3 = 2.178R = 2.178 \times 39.75\ k\Omega = 86.57\ k\Omega$
$R_4 = 0.432R = 0.432 \times 39.75\ k\Omega = 17.17\ k\Omega$

4-pole lowpass filter resistance table (Table 1)

	Bessel	Chebyshev (0.5 dB ripple)
R_1	0.673R	2.182R
R_2	0.712R	1.286R
R_3	0.384R	2.178R
R_4	1.014R	0.432R

4-pole highpass filter resistance table (Table 2)

	Chebyshev (0.5 dB ripple)
R_1	0.726R
R_2	0.491R
R_3	0.386R
R_4	2.757R

2. A 4-pole Chebyshev highpass filter modified from FLJ-UR4HA1/2 (normal band ripple of 0.5 dB).

   The circuit diagram is shown in Fig. 11.
   Obtain external resistance R_1 to R_4 from Table 2.

3. Application of FLJ-UR1BA1/2

   Q=5 band elimination filter

   A band elimination filter can be made using an external operational amplifier as shown in Fig. 12.

   a. Cutoff frequency fc is set by R. Adjust VR_1 to tune the fc accurately.
   b. Then, adjust VR_2 to control volume of attenuation.
   c. Fig. 12 shows Q=5. For Q=10 or 20, connect one of pins 6 to 10 to ground.

   How to set operational Q

   The FLJ-UR1BA1/2 pin connection allows selection of Q=5, 10, 20, 30, 40 or 50. For other than the above, set Q as follows: where the range of Q is $1.81 \leqq Q \leqq 50$

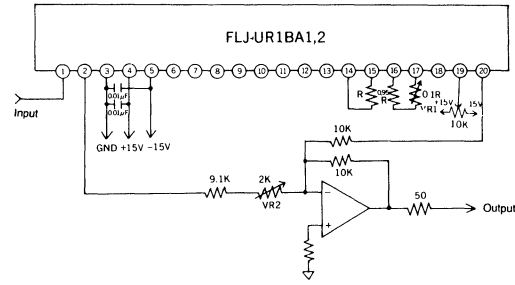
   a. Setting of Q at the range of $1.81 \leqq Q < 5$
      Connect pins as shown in Fig. 13. Obtain Rg from the equation given below.

      $$Rq = \frac{10(Q-1) \times 10^3}{5-Q}\ (\Omega)$$

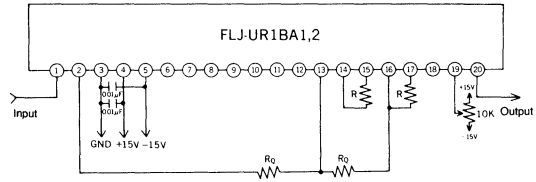
   b. Setting of Q at the range of $5 < Q < 50$
      Connect pins as shown in Fig. 14. Obtain Rq from the equation given below.

      $$Rq = \frac{5 \times 10^3}{Q-5}\ (\Omega)$$

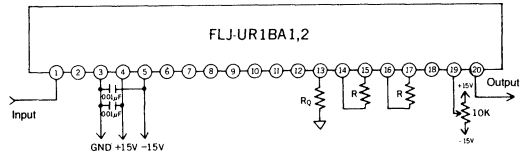
(Fig. 12)



(Fig. 13)



(Fig. 14)



4. How to change Q of FLJ-UR2BA1/2
   The Q of FLJ-UR2BA1/2 is set 5 at the time of shipment. This can be changed from 5 to 10.

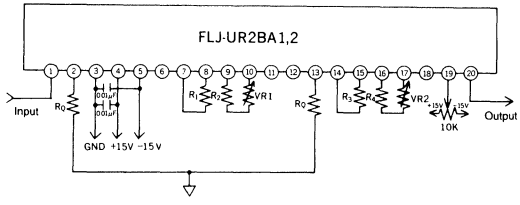
   a. Connect pins as shown in Fig. 15.
   b. Rq, R_1, R_2, R_3 and R_4 are to be changed.

      Calculations are:

      Rq = 3.92 kΩ
      Resistances for setting fc are:

      $R_1 = 1.0355R$ $\quad R_4 = 0.95R_3$
      $R_2 = 0.95R_1$ $\quad VR_1 \geqq 0.1R_1$
      $R_3 = 0.9657R$ $\quad VR_2 \geqq 0.1R_2$.

(Fig. 15)



6

R given here is the fc setting resistance in the standard use as mentioned above and obtained from the following equation:

$$R = \frac{15.9\times10^6}{fc\ (Hz)}\ (\Omega);\ \text{FLJ-UR2BA1}$$

$$R = \frac{159\times10^6}{fc\ (Hz)}\ (\Omega);\ \text{FLJ-UR2BA2}$$

Unlike the FLJ-UR1BA1/2, FLJ-UR2BA1/2 requires fine adjustments.

c. Adjustment procedure

1. Set the input signal frequency to 1.036×fc.
2. Adjust VR_1 to obtain a phase difference of 180° between the input signal and the output signal at pin 9.
3. Set the input signal frequency to fc.
4. Adjust VR_2 to obtain a phase difference of 0° between the input signal and the output signal (pin 20).

5. A 2-pole Bessel lowpass filter modifying FLJ-UR2LH1/2, FLJ-UR2LH1/2 is a 2-pole Butterworth lowpass/highpass simultaneous output filter. A 2-pole Bessel lowpass filter is implemented just by changing fc setting resistances R_1 and R_2. The output is obtained at pin 20. Calculate R_1 and R_2 as shown below.

$R_1 = 0.6408R$
$R_2 = 0.9612R$

6. A 6-pole lowpass/highpass filter example FLJ-UR2LH1/2, FLJ-UR4LA1/2 and FLJ-UR4HA1/2 can be combined to make 6-pole lowpass/highpass filters.

a. Lowpass filter

Fig. 16 shows the circuit diagram for the 6-pole lowpass filter configuration. Table 3 is the external resistance table. The combination of FLJ-UR2LH1 and FLJ-UR4LA1 or FLJ-UR2LH2 and FLJ-UR4LA2 depends on the fc setting range.

Design Example

Example of 6-pole Butterworth lowpass filter with fc = 6 kHz.
Assume the desired cutoff frequency is 6 kHz. The combination of FLJ-UR2LH2 and FLJ-UR4LA2 should be selected because of the fc desired.

According to the relation between fc and external resistance R, external resistance values R_{11} to R_{24} are as follows:

$$R = \frac{159\times6^6}{6\times10^3} = 26.5\ k\Omega$$

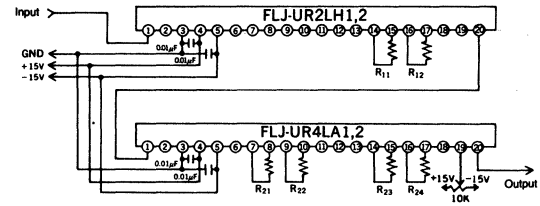
From the Butterworth resistance values in Table 3,

$R_{11}=0.7303R=0.7303\times26.5=19.35\ k\Omega$
$R_{12}=1.3694R=1.3694\times26.5=36.29\ k\Omega$
$R_{21}=0.9540R=0.9540\times26.5=25.28\ k\Omega$
$R_{22}=1.0482R=1.0482\times26.5=27.78\ k\Omega$
$R_{23}=1.4786R=1.4786\times26.5=39.18\ k\Omega$
$R_{24}=0.6763R=0.6763\times26.5=17.92\ k\Omega$

b. Highpass filter

Fig. 17 shows the circuit diagram for a 6-pole highpass filter configuration. Table 4 is the external resistance table. External resistance values can be determined in the same way as the 6-pole lowpass filter configuration.

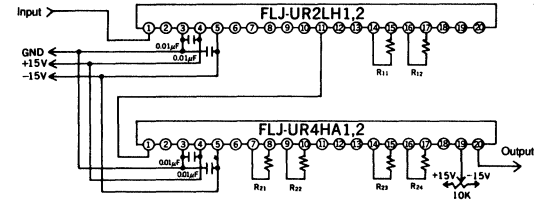
(Fig. 16)



6-pole lowpass filter resistance table (Table 3)

	Bessel	Butterworth	Chebyshev (0.1 dB)
R_{11}	0.4492R	0.7303R	1.6520R
R_{12}	0.8625R	1.3694R	2.2985R
R_{21}	0.6675R	0.9540R	2.9484R
R_{22}	0.5234R	1.0482R	0.4871R
R_{23}	0.4105R	1.4786R	3.3366R
R_{24}	0.6693R	0.6763R	0.2654R

(Fig. 17)



6-pole highpass filter resistance table (Table 4)

	Butterworth	Chebyshev (0.1 dB)
R_{11}	0.732R	0.435R
R_{12}	1.366R	0.605R
R_{21}	1.215R	0.831R
R_{22}	0.823R	0.838R
R_{23}	0.434R	0.356R
R_{24}	2.303R	3.172R

7. A 8-pole lowpass/highpass filter example

a. Fig. 18 shows the circuit diagram for a lowpass/highpass filter configuration. Two FLJ-UR4LA1's or FLJ-UR4LA4's can be used in a lowpass filter configuration, and two FLJ-UR4HA1's or FLJ-UR4HA2's in a highpass filter configuration. Table 5 gives the resistances for the lowpass filter, and Table 6 for the highpass filter configuration.

b. A 8-pole Butterworth lowpass filter

Fig. 19 shows another example of 8-pole Butterworth lowpass filter. Two FLJ-UR4LA1's or FLJ-UR4LA2's are used in the same manner as in Fig. 18. Same resistances are employed for eight resistors (R_{11} to R_{24}) but R_Q values are varied at 2 poles each internally. Four more external resistors are used, but the advantage is that the eight resistances are the same. R is obtained from the equation given below.

$$R = \frac{15.9}{fc\ (Hz)} \times 10^6\ (\Omega);\ \text{FLJ-UR4LA1}$$

$$R = \frac{159}{fc\ (Hz)} \times 10^6\ (\Omega);\ \text{FLJ-UR4LA2}$$

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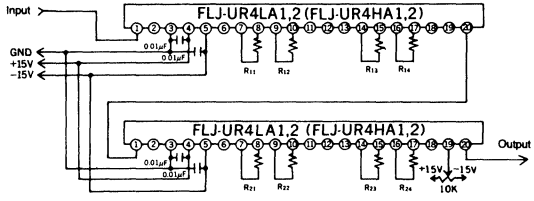
(Fig. 18)



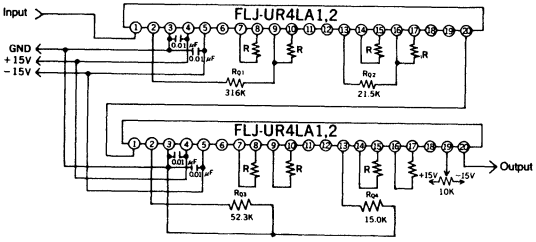
8-pole lowpass filter resistance table (Table 5)

	Bessel	Butterworth	Chebyshev (0.05 dB)
R_{11}	0.525R	0.942R	2.520R
R_{12}	0.600R	1.062R	2.232R
R_{13}	0.233R	0.689R	1.842R
R_{14}	1.272R	1.452R	0.653R
R_{21}	0.671R	1.111R	2.986R
R_{22}	0.389R	0.900R	0.750R
R_{23}	0.428R	1.962R	5.248R
R_{24}	0.486R	0.501R	0.173R

8-pole highpass filter resistance table (Table 6)

	Butterworth	Chebyshev (0.05 dB)
R_{11}	1.416R	0.5619R
R_{12}	0.706R	0.3165R
R_{13}	0.915R	0.3762R
R_{14}	1.093R	2.2090R
R_{21}	1.111R	0.7039R
R_{22}	0.900R	0.6371R
R_{23}	0.391R	0.3287R
R_{24}	2.561R	3.3520R

(Fig. 19)



8. 72 dB/oct high rolloff lowpass filter

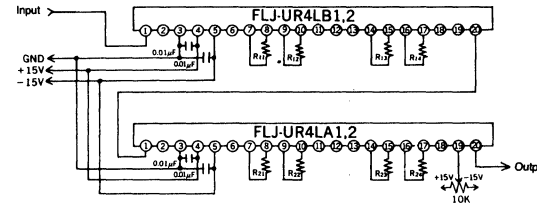
   Fig. 20 shows an example of a Chebyshev lowpass filter with high rolloff of 72 dB/oct achieved by combining FLJ-UR4LB1/2 and FLJ-UR4LA1/2. Resistances R_{11} to R_{24} are as follows:

   $R_{11} = R_{12} = R_{13} = R_{14} = R$
   $R_{21} = 1.801R$
   $R_{22} = 1.221R$
   $R_{23} = 1.797R$
   $R_{24} = 0.4788R$

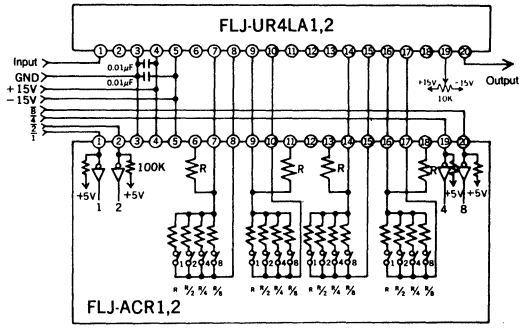
9. Example of a digital tuneable filter

   The FLJ-ACR1/2 is provided as FLJ-UR series accessory. FLJ-ACR1/2 is composed of resistance networks and analog switches. Combined use of those instead of external resistors provides a digital tuneable filter in which fc can be set by digital (BCD) codes (See Fig. 21).

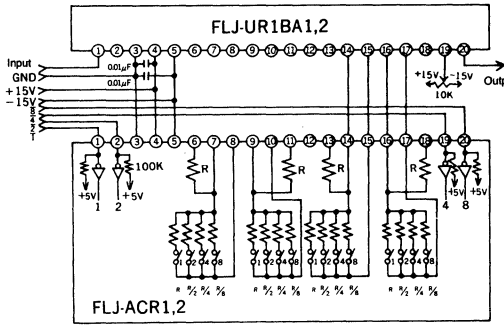
(Fig. 20)



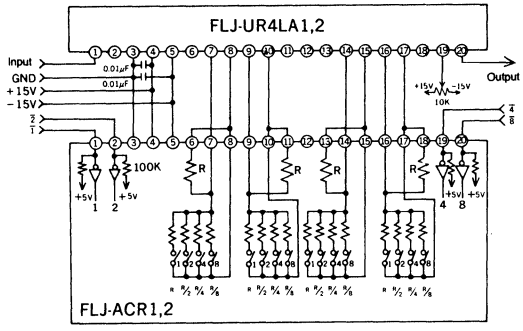
(Fig. 21) R shown here is 1.59 MΩ for FLJ-ACR1 and 159 kΩ for FLJ-ACR2.



(Fig. 22)

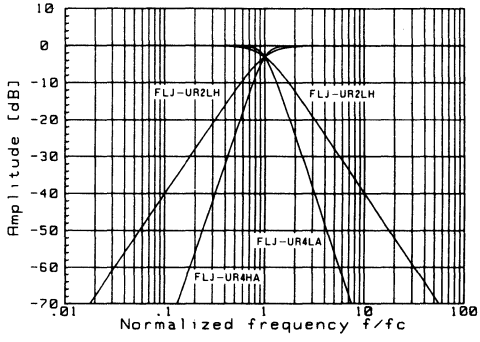


(Fig. 23)

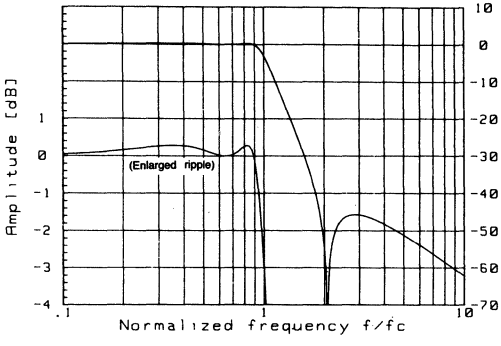


A model such as FLJ-UR1BA1/2 that requires two external resistors is shown in Fig. 22. A model that requires 4 resistors is shown in Fig. 21. In the examples shown in Figs. 21 and 22, when all digitals are 0 (when no filter external resistor is installed), no filter function is expected. The wiring shown in Fig. 23 is also possible. See FLJ-ACR data sheets.

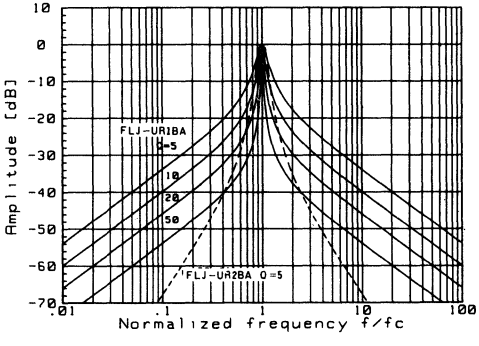
FLJ-UR4LA, 4HA, 2LH Frequency Response (Fig. 24)



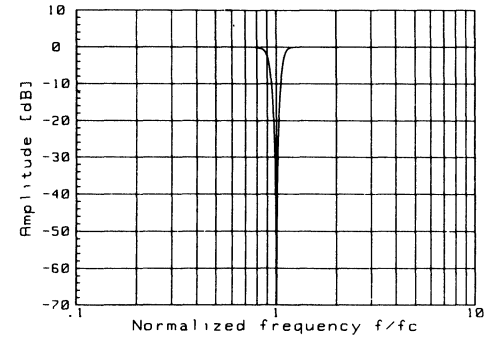
FLJ-UR4LB Frequency Response (Fig. 26)



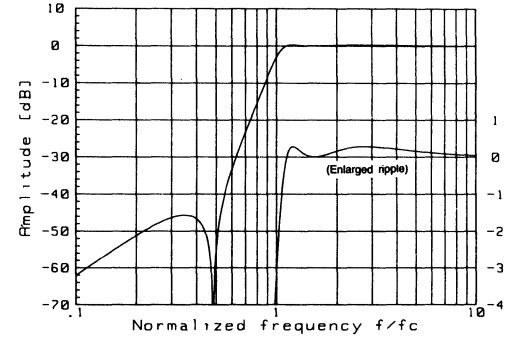
FLJ-UR1BA, 2BA Frequency Response (Fig. 28)



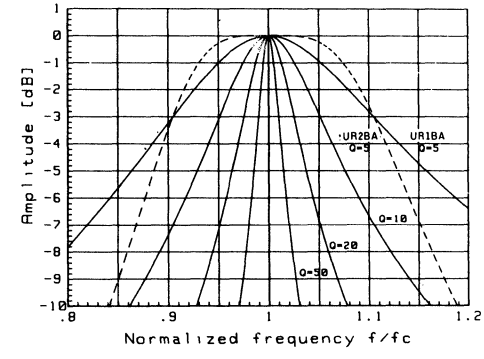
FLJ-UR2EA Frequency Response (Fig. 25)



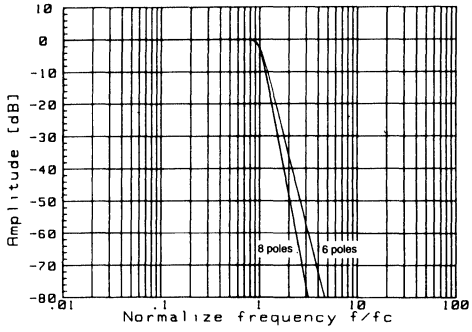
FLJ-UR4HB Frequency Response (Fig. 27)



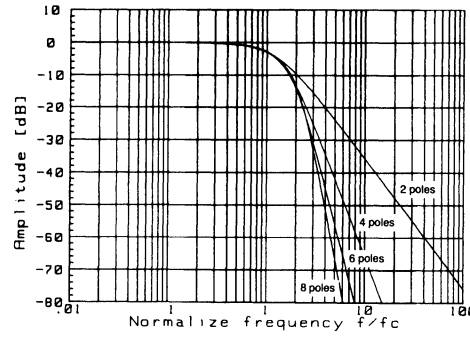
FLJ-UR1BA, 2BA Frequency Response Enlarged Diagram (Fig. 29)



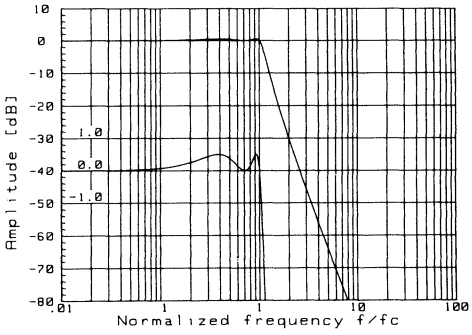
Higher Order Butterworth Lowpass Filter Frequency Response (Fig. 30)



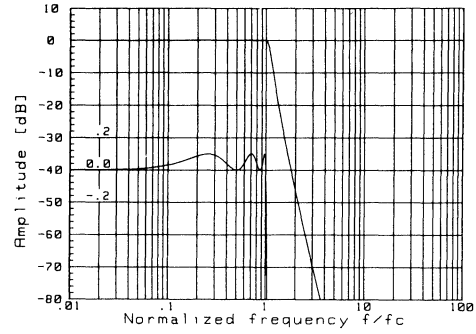
Higher Order Bessel Lowpass Filter Frequency Response (Fig. 31)



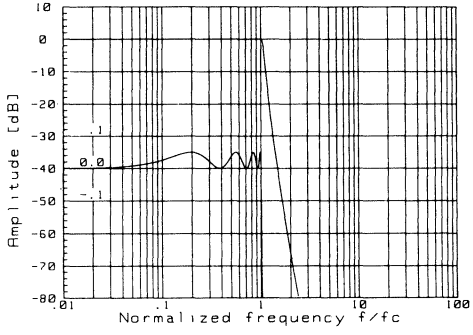
4-pole Chebyshev Lowpass Filter Frequency Response (Fig. 32)
Ripple 0.5 dB (The center shows the enlarged ripple.)



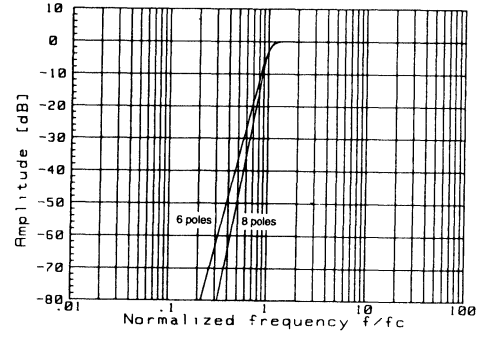
6-pole Chebyshev Lowpass Filter Frequency Response (Fig. 33)
Ripple 0.1 dB (The center shows the enlarged ripple.)



8-pole Chebyshev Lowpass Filter Frequency Response (Fig. 34)
Ripple 0.05 dB (The center shows the enlarged ripple.)

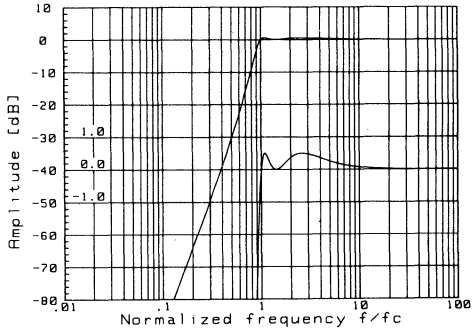


Higher Order Butterworth Highpass Filter Frequency Response (Fig. 35)

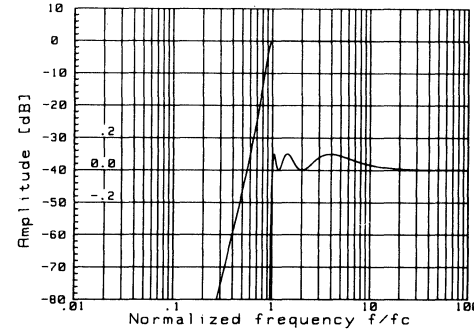


6

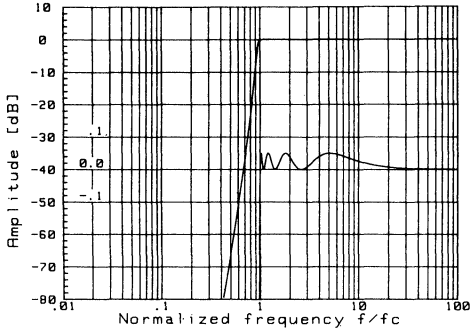
4-pole Chebyshev Highpass Filter Frequency Response (Fig. 36)
Ripple 0.5 dB (The center shows the enlarged ripple.)



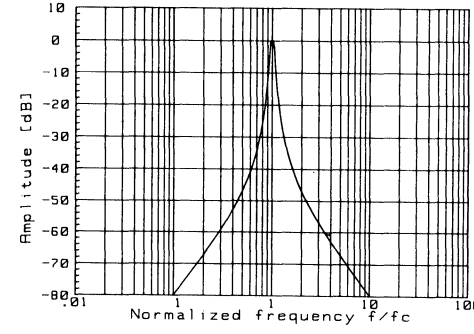
6-pole Chebyshev Highpass Filter Frequency Response (Fig. 37)
Ripple 0.1 dB (The center shows the enlarged ripple.)



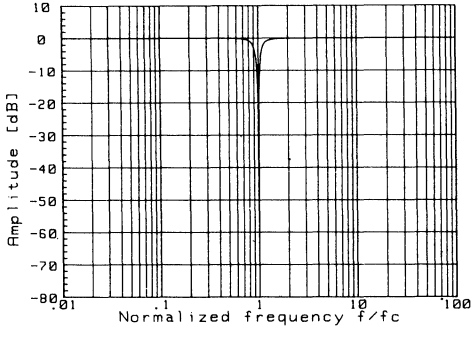
8-pole Chebyshev Highpass Filter Frequency Response (Fig. 38)
Ripple 0.05 dB (The center shows the enlarged ripple.)



FLJ-UR2BA1/2 Bandpass Filter Frequency Response Q = 10 (Fig. 39)



Band Elimination Filter Frequency Response (Fig. 40)
FLJ-UR1BA1/2+External amplifier (Refer to Application 3, Q = 5)



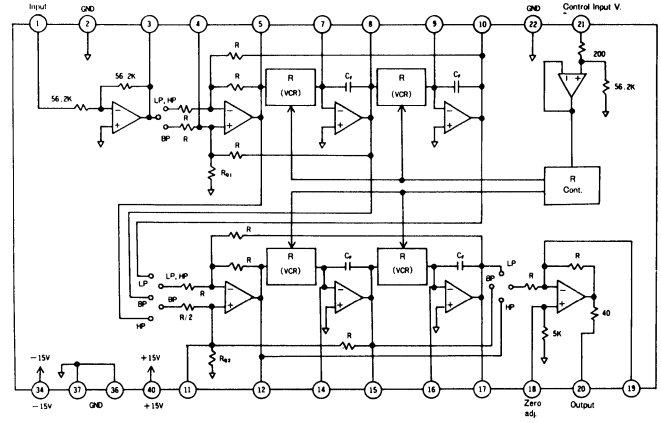
FLJ-VL,VH,VB VOLTAGE TUNEABLE FILTER

FEATURES

- **Cuttoff frequency tuned by external voltage.**
- **Wide range of control frequency.**
- **Small hydrid.**

GENERAL DESCRIPTION

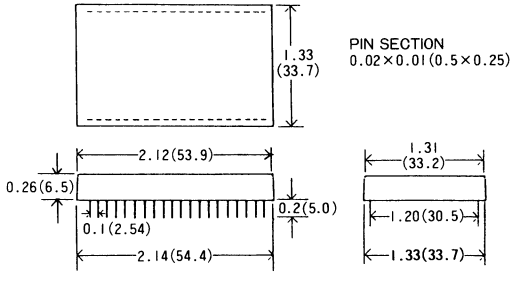
FLJ-V Series are filters whose cutoff frequency or center frequency can be set with an external control voltage.
Hybrid construction has made it possible to build highly reliable, high performance filters in small size at low cost.
FLJ-VL is a lowpass filter and FLJ-VH is a highpass filter. Both filters have 24dB/octave rolloff characteristics. FLJ-VB is a bandpass filter which has 12dB/octBW at Q = 5 characteristic.



BLOCK DIAGRAM (Fig. 1)

6

MECHANICAL DIMENSIONS (Fig. 2) INCHES (mm)



PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT	21	CONTROL V. INPUT
2	GND	22	GND
4	Rq1	34	-Vcc (-15V)
7	Cext1-1	36	GND
8	Rq1, Cext1-1	37	GND
9	Cext1-2	40	+Vcc (+15V)
10	Cext1-2		
11	Rq2		
14	Cext2-1		
15	Rq2, Cext2-1		
16	Cext2-2		
17	Cext2-2		
18	ZERO ADJ.		
20	OUTPUT		

DO NOT CONNECT UNUSED PINS TO OTHERS.

SPECIFICATIONS

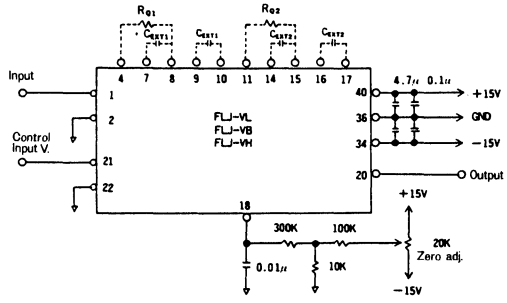
Typical values at 25°C with ±15V supply, 10V control voltage, ±1V rated input unless otherwise specified.

	FLJ-VL (Lowpass Filter)	FLJ-VB (Bandpass Filter)	FLJ-VH (Highpass Filter)
ABSOLUTE MAXIMUM			
Power Supply Voltage	±18V	* "Same as FLJ-VL"	* "Same as FLJ-VL"
Input Voltage	±Vcc	* "Same as FLJ-VL"	* "Same as FLJ-VL"
Control Input Voltage	±Vcc	* "Same as FLJ-VL"	* "Same as FLJ-VL"
FILTER CHARACTERISTICS			
Frequency Set Range	100Hz ~ 100KHz	200Hz ~ 20KHz	20Hz ~ 20KHz
Frequency Set Accuracy	± (3%+0.01% F.S.) max.	*	*
Control Input Voltage Range	+10mV ~ +10V	+100mV ~ +10V	+10mV ~ +10V
Control Input Impedance	50 Kohm min.	*	*
Characteristic	4 pole Butterworth	2 pole pair Butterworth	4 pole Butterworth
Rolloff	24dB/oct	12dB/oct BW(Q=5)	24dB/oct
Pass Gain vs. Control Input V.	±0.5dB	±1dB	±0.5dB
Distortion	0.1% max.	*	*
Frequency Set T.C.	±0.03%/°C	*	*
AMPLIFIER CHARACTERISTICS			
Input Voltage	±10V min.	±2V min.	±10V min.
Rated Input Voltage	±1V	*	*
Input Impedance	50 Kohm min.	*	*
Offset Voltage	±10mV Zero Adjustable	*	*
Offset V. Variance vs. Control V.	±20mV max.	*	*
Temperature Drift	300μV/°C	*	*
Noise	800μVrms max. @10Hz ~ 300KHz	*	*
Output Voltage/Current	±10V/5mA min.	±2V/5mA min.	±10V/5mA min.
Output Impedance	50ohm max.	*	*
Load Resistance	10Kohm min.	*	*
Small Signal BW	DC ~ fc	-	fc ~ 300KHz
POWER REQUIREMENTS & ENVIRONMENT			
Power Supply Voltage	±15V, +10%, -5%	*	*
Current	±36mA	*	*
Operating Temperature Range	-20°C ~ +70°C	*	*
Operating Humidity Range	10% ~ 95%RH	*	*
Storage Temperature Range	-30°C ~ +80°C	*	*
Storage Humidity Range	10% ~ 80%RH	*	*

TECHNICAL NOTES

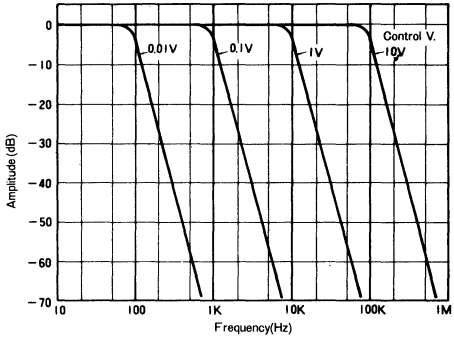
1. The rated input voltage is ±1V. The maximum performance is obtained if input voltage does not exceed this range.
2. These filters are 4pole Butterworth (2pole pair) filters. Cutoff frequency is controlled by external voltage. The relationship between control voltage and cutoff frequency is linear (=proportional). Cutoff frequency ranges can be shifted toward lower frequency region if four external capacitors are added. See Figure 3.
   FLJ-VL:
   $$Cext1, Cext\ 2 = \frac{1}{fc(max) \times 2\pi \times 6.36 \times 10^3} - 250 \times 10^{-12}$$
   FLJ-VB, VH:
   $$Cext1, Cext\ 2 = \frac{1}{fc(max) \times 2\pi \times 6.36 \times 10^3} - 1250 \times 10^{-12}$$
   Cext1, Cext 2 : F (Farad)
   fc(max) : -3dB frequency at 10V control voltage.
3. Zero offset adjustment range is approximately ±50mV.
4. Control input voltage signal has approximately 10KHz of frequency response. However, it takes long time before the output DC offset (=approx. 10mV) settles under the new fc set. It is not recommended to use alternating signals for the control input, depending on applications. The cutoff frequency shall be affected by unstable control voltage if it is small signal, even if it is DC.
5. FLJ-VL can be used as Bessel filter. Connect Rq1 = 95.3KΩ and Rq2 = 9.53KΩ as shown Figure 3. External capacitors should be:
   $$Cext1 = 250\left(\frac{100}{fc(max)\ (KHz) \times 1.43241} - 1\right)$$
   $$Cext2 = 250\left(\frac{100}{fc(max)\ (KHz) \times 1.60594} - 1\right)$$
   fc(max) ≦ 62.2KHz, -3dB frequency at 10V control input voltage.
   Cext1, Cext2 : pF (pico Farad)

TYPICAL CONNECTION (Fig. 3)

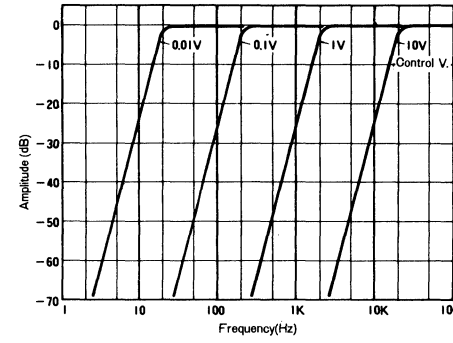


AMPLITUDE VS. FREQUENCY (Fig. 4)

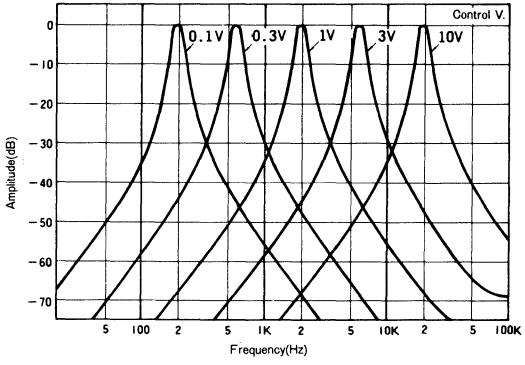
FLJ-VL (Fig. 4-1)



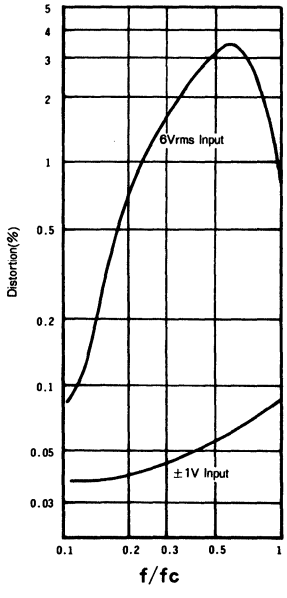
FLJ-VH (Fig. 4-2)



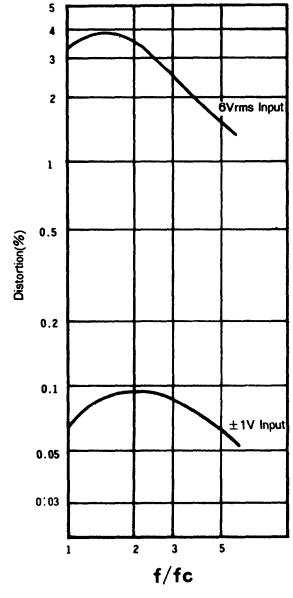
FLJ-VB (Fig. 4-3)



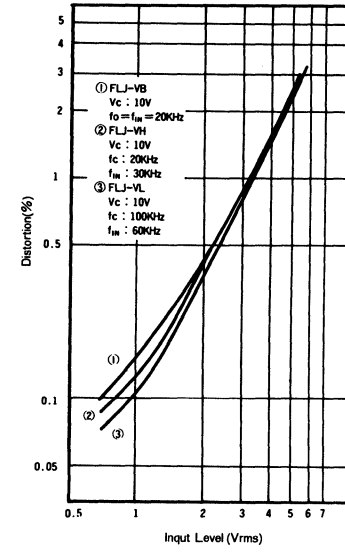
FLJ-VL DISTORTION VS. f/fc (Fig. 5-1)



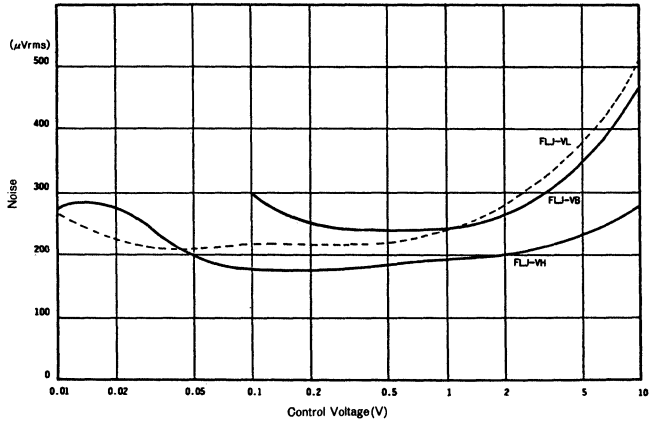
FLJ-VH DISTORTION VS. f/fc (Fig. 5-2)



DISTORTION VS. INPUT LEVEL (Fig. 6)



NOISE VS. CONTROL VOLTAGE (Fig. 7)



FLT-U2
Microelectronic
Universal Active Filter

FEATURES

- **State variable filter**
- **LP, BP, or HP functions**
- **2-Pole response**
- **Low-noise operational amplifiers**
- **−55°C to +125°C Operation**
- **Low cost**

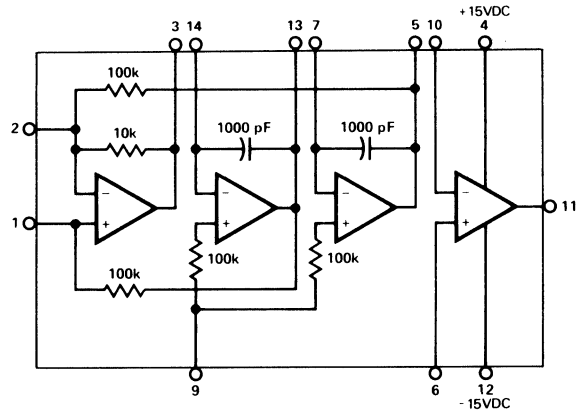
GENERAL DESCRIPTION

The FLT-U2 is a universal active filter manufactured with thick-film hybrid technology. It uses the state variable active filter principle to implement a second order transfer function. Three committed operational amplifiers are used for the second order function while a fourth uncommitted operational amplifier can be used as a gain stage, summing amplifier, buffer amplifier, or to add another independent real pole.

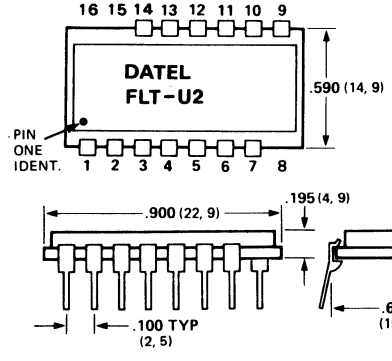
Two-pole lowpass, bandpass, and highpass output functions are available simultaneously from three different outputs, and notch and allpass functions are available by combining these outputs in the uncommitted operational amplifier. To realize higher order filters, several FLT-U2's can be cascaded. Q range is from 0.1 to 1,000 and resonant frequency range is 0.001 Hz to 200 kHz. Frequency stability is 0.01%/°C and resonant frequency accuracy is within ±5% of calculated values. Frequency tuning is done by two external resistors and Q tuning by a third external resistor. For resonant frequencies below 50 Hz, two external tuning capacitors must be added. Exact tuning of the resonant frequency is done by varying one of the resistors around its calculated value.

The internal operational amplifiers in the FLT-U2 have 3 MHz gain bandwidth products and a wideband input noise specification of only 10 nV/√Hz. This results in considerably improved operation over most other competitive active filters which employ lower performance amplifiers. By proper selection of external components any of the popular filter types such as Butterworth, Bessel, Chebyshev, or Elliptic may be designed. Applications include audio, tone signalling, sonar, data acquisition, and feedback control systems.

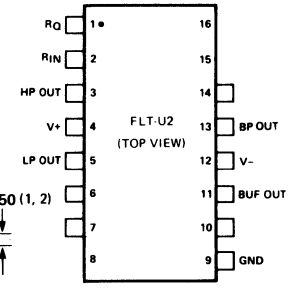
Two models are available for operation over the commercial, 0°C to +70°C, and military, −55°C to +125°C, temperature ranges.



MECHANICAL DIMENSIONS INCHES (MM)



CONNECTIONS DIAGRAM



6

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies, unless otherwise stated.

FILTER CHARACTERISTICS	
Frequency Range[14]	0.001 Hz to 200 kHz
Q Range[1]	0.1 to 1.000
f_0 Accuracy	±5%
f_0 Temperature Coefficient	0.01%/°C
Voltage Gain[1]	0.1 to 1.000
AMPLIFIER CHARACTERISTICS	
Input Offset Voltage	0.5 mV typ., 6 mV max.
Input Bias Current	40 nA typ., 500 nA max.
Input Offset Current	5 nA typ., 200 nA max.
Input Impedance	5 Megohms
Input Com. Mode Voltage Range	±12V min.
Input Voltage Noise, wideband	10 nV/√Hz
Output Voltage Range	±10V min.
Output Current	±5 mA min.
Open Loop Voltage Gain	300,000
Common Mode Rejection Ratio	100 dB
Power Supply Rejection	10 μV/V
Unity Gain Bandwidth	3 MHz
Slew Rate	1 V/μsec.
POWER SUPPLY REQUIREMENTS	
Voltage, rated performance	±15V dc
Voltage Range, operating	±5V to ±18V
Quiescent Current	11.5 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
FLT-U2	0°C to +70°C
FLT-U2M	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Case	Ceramic 16-pin DIP (double-spaced)

FOOTNOTE:

1. $f_0Q \leq 5 \times 10^5$ optimally

TECHNICAL NOTES

1. The FLT-U2 has simultaneous lowpass, bandpass, and highpass output functions. The chosen output for a particular function will be at unity gain based on Tables II and III. This means that the other two unused outputs will be at other gain levels. The gain of the lowpass output is always 10 dB higher than the gain of the bandpass output and 20 dB higher than the gain of the highpass output.
2. When tuning the filter and checking it over its frequency range, the outputs should be checked with a scope to make sure there is no waveform clipping present, as this will affect the operation of the filter. In particular the lowpass output should be checked since its gain is the highest.
3. Check f_1, the center frequency for bandpass and the cutoff frequency for lowpass or highpass, at the bandpass output. Here the peaking frequency can easily be determined for high Q filters and the 0° or 180° phase frequency can easily be determined for low Q filters (depending on whether inverting or noninverting).
4. Tuning resistors should be 1% metal film resistors with 100 ppm/°C temperature stability or better for best performance. Likewise external tuning capacitors should be NPO ceramic or other stable capacitor types.

THEORY OF OPERATION

The FLT-U2 block diagram is shown in Figure 1. This is a second order state-variable filter using three operational amplifiers. Lowpass, bandpass, and highpass transfer functions are simultaneously produced at its three output terminals. These three transfer functions are characterized by the following second order equations:

$$H(s) = \frac{K_1}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{LOWPASS}$$

$$H(s) = \frac{K_2 S}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{BANDPASS}$$

$$H(s) = \frac{K_3 S^2}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{HIGHPASS}$$

where K_1, K_2, and K_3 are arbitrary gain constants.

A second order system is characterized by the location of its poles in the s-plane as shown in Figure 2. The natural radian frequency of this system is ω_0. In Hertz this is $f_0 = \frac{\omega_0}{2\pi}$.

The resonant radian frequency of the circuit is different from the natural radian frequency and is:

$$\omega_1 = \omega_0 \sin \phi = \sqrt{\omega_0^2 - \sigma_1^2}$$

The damping factor d determines the amount of peaking in the filter frequency response and is defined as:

$$d = \cos \phi$$

The point at which the peaking becomes zero is called critical damping and is $d = \sqrt{2}/2$.

Q is found from d and is a measure of the sharpness of the resonance of the peaking:

$$Q = \frac{1}{2d}$$

$$\text{Also, } Q = \frac{f_0}{-3 \text{ dB Bandwidth}} = \frac{\omega_0}{2\sigma_1}$$

For high Q filters the natural frequency and resonant frequency are approximately equal.

$$\omega_1 \simeq \omega_0 \text{ or } f_1 \simeq f_0$$

This is true since $\omega_1 = \omega_0 \sin \phi$ and $\sin \phi \simeq 1$ as the poles move close to the $j\omega$ axis in the s-plane.

For high Qs ($Q > 1$) we therefore have for the second order filter:

$f_0 \simeq$ Bandpass center frequency
$\simeq$ Lowpass corner frequency
$\simeq$ Highpass corner frequency

In the simplified tuning procedure which follows, the tuning is accomplished by independently setting the natural frequency and Q of the filter. This is done most simply by assuming unity gain for the output of the desired filter function. Unity gain means a gain of one (±) at dc for lowpass, at center frequency for bandpass, and at high frequency ($f >> f_0$) for highpass. Unity gain does not apply to all outputs simultaneously but only to the chosen output based on the component values given in the tables. Figure 3 shows the relative gains of the three simultaneous outputs assuming the bandpass gain is set to unity. Note that lowpass gain is always 10 dB higher than bandpass gain and highpass gain is always 10 dB lower than bandpass gain.

SIMPLIFIED TUNING PROCEDURE

1. Select the desired transfer function (lowpass, bandpass, or highpass) and inverted or noninverted output. From this determine the filter configuration (inverting or noninverting) using Table I.

TABLE I FILTER CONFIGURATION

	LP	BP	HP
INVERTING INPUT	INV	NON-INV	INV
NONINVERTING INPUT	NON-INV	INV	NON-INV

2. Starting with the desired natural frequency and Q (determined from the filter transfer function or s-plane diagram), compute f_0Q. For $f_0Q > 10^4$ the actual realized Q will exceed the calculated value. At $f_0Q = 10^4$ the increase is about 1% and at $f_0Q = 10^5$ it is about 20%.

3. **Inverting Configuration.** Using the value of Q from Step 2 find R_1 and R_3 from Table II. R_2 is open, or infinite.

TABLE II INVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	100K	OPEN	$\frac{100K}{3.80\ Q-1}$
BANDPASS	Q X 31.6K	OPEN	$\frac{100K}{3.48\ Q}$
HIGHPASS	10K	OPEN	$\frac{100K}{6.64\ Q-1}$

4. **Noninverting Configuration.** Using the value of Q from Step 2 find R_2 and R_3 from Table III. R_1 is open, or infinite.

TABLE III NONINVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	OPEN	$\frac{316K}{Q}$	$\frac{100K}{3.16\ Q-1}$
BANDPASS	OPEN	100k	$\frac{100K}{3.48\ Q-1}$
HIGHPASS	OPEN	$\frac{31.6K}{Q}$	$\frac{100K}{0.316\ Q-1}$

5. Using the value of f_0 from Step 2, set the natural frequency of the filter by finding R_4 and R_5 from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{f_0}$$

where R_4 and R_5 are in ohms and f_0 is in Hertz. The natural frequency varies as $\sqrt{R_4R_5}$ and therefore one value may be increased and the other decreased and the natural frequency will be constant if the geometric mean is constant. To maintain constant bandwidth at the bandpass output while varying center frequency, fix R_4 and vary R_5.

6. For $f_0 < 50$ Hz the internal 1000 pF capacitors should be shunted with external capacitors across pins 5 & 7 and 13 & 14. If equal value capacitors are used, R_4 and R_5 are then computed from:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0 C} \text{ (C in pF)}$$

For unequal value capacitors this becomes:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0\sqrt{C_1C_2}} \text{ (C_1C_2 in pF)}$$

In both cases the capacitance is the sum of the external values and the internal 1000 pF values.

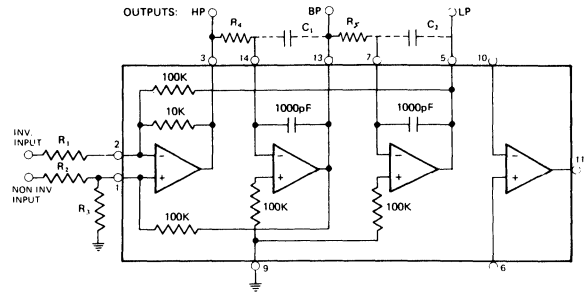


Figure 1.
FLT-U2 Block Diagram

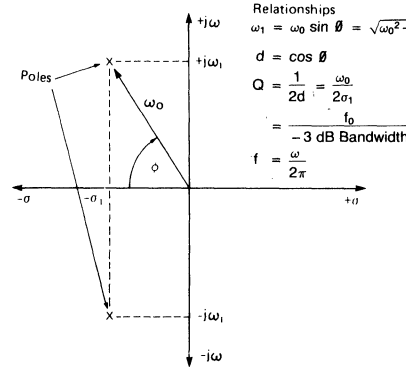


Figure 2.
S-Plane Diagram

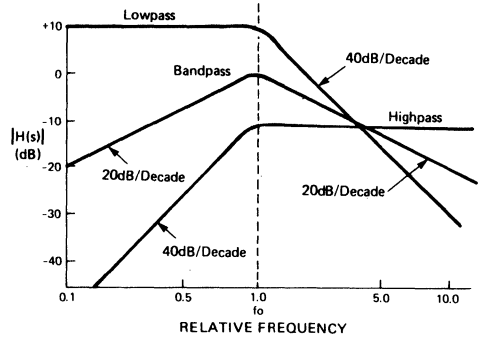


Figure 3.
Relative Gains of Simultaneous Outputs, Q=1

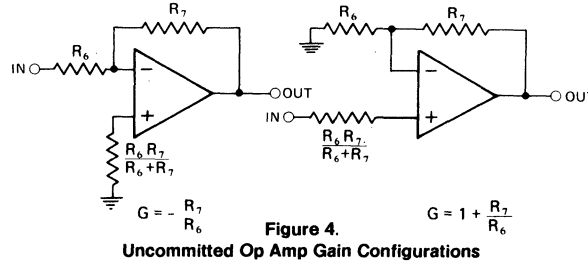


Figure 4.
Uncommitted Op Amp Gain Configurations

SIMPLIFIED TUNING PROCEDURE, (Cont'd)

7. This procedure is based on unity gain output for the desired function. For additional gain, the fourth uncommitted operational amplifier should be used as an inverting or noninverting gain stage following the selected output. See Figure 4. A third pole on the real axis of the s-plane may also be added to the transfer function by adding a capacitor to the gain stage as shown in Figure 5.

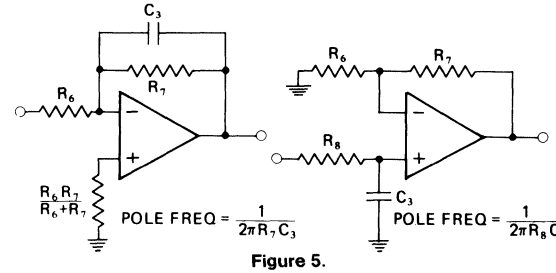


Figure 5.
Using the Uncommitted Op Amp to Add a Real Axis Pole

FILTER DESIGN EXAMPLES

Bandpass Filter With 1 kHz Center Frequency Q = 10 and Inverted Output

1. From Table I the noninverting configuration is chosen to realize an inverted bandpass output $f_0Q = 10^4$ which means the realized Q will be about 1% higher than calculated.
2. From Table III, using Q = 10, we find:

$$R_1 = \text{open}$$
$$R_2 = 100\text{K ohms}$$
$$R_3 = \frac{100K}{3.48\ Q\text{-}1} = \frac{100K}{33.8} = 2.96\text{K ohms}$$

3. Using f_0 of 1 kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{1000} = 50.3\text{K ohms}$$

4. This completes the filter design which is shown in Figure 6. To choose the nearest 1% standard value resistors either 49.9K or 51.1K ohms could be used; likewise one value of 49.9K and one of 51.1K could be used giving the geometric mean of $\sqrt{R_4R_5} = \sqrt{49.9K} \times 51.1K = 50.5K$ which is even closer. But due to the filter ±5% frequency tolerance it may be better to hold R_4 constant while varying R_5 to tune it exactly.

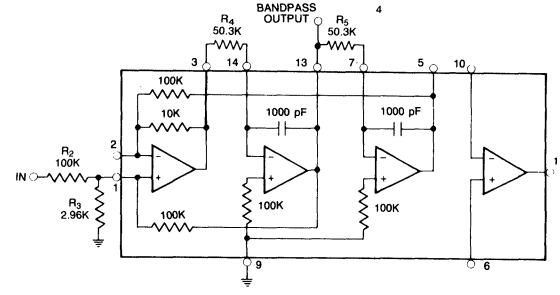


Figure 6.
Bandpass Filter Example

Three-Pole Noninverting Butterworth Low Pass Filter With dc Gain of 10 and Cutoff Frequency of 5 kHz.

The s-plane diagram of the 3-pole Butterworth filter is shown in Figure 7. We will use a second order filter to realize the two complex conjugate poles and the uncommitted operational amplifier to provide the third real axis pole and a dc gain of 10.

1. From Table I, the noninverting filter configuration would normally be used to give a noninverting low pass output. In this case, however, we choose an inverting uncommitted op amp with a gain of 10 and therefore we use the inverting configuration for the filter. By comparing the second order portion of the Butterworth function $S^2 + \omega_0S + \omega_0^2$ to the standard second order function $S^2 + \omega_0S + \omega_0^2$ we find Q = 1 f_0Q is then 5×10^3 so that Q will not exceed its specified value.
2. From Table II, using Q = 1, we find:

$$R_1 = 100\text{K ohms}$$
$$R_2 = \text{open}$$
$$R_3 = \frac{100K}{3.80\ Q\text{-}1} = 35.7\text{K ohms}$$

3. Using f_0 of 5 kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{5000} = 10.1\text{K ohms}$$

4. For the uncommitted output amplifier, a gain of −10 is required. This defines $R_7/R_6 = 10$ and we arbitrarily choose R_6 = 2K, R_7 = 20K ohms.

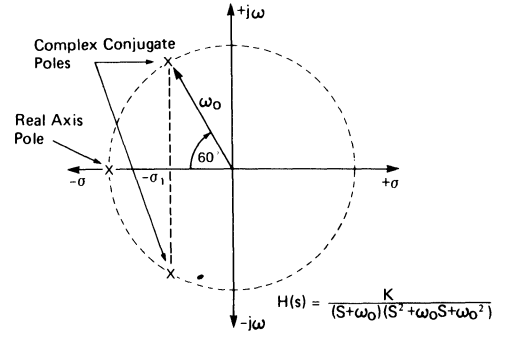


Figure 7.
S-Plane Diagram of 3-Pole Butterworth Lowpass Filter

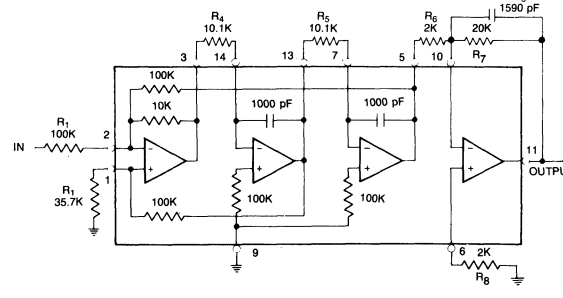


Figure 8.
Three Pole Butterworth Low Pass Filter Example

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FILTER DESIGN EXAMPLES, (Cont'd)

5. The final step is to realize the real axis pole of the Butterworth filter. This pole is at 5 kHz and is set by using capacitor C_3 across the feedback resistor R_7:

$$C_3 = \frac{1}{2\pi f R_7} = \frac{1}{6.28 \times 5 \times 10^3 \times 20 \times 10^3} = 1590 \text{ pF}$$

6. This completes the 3-pole Butterworth filter which is shown in Figure 8.

Highpass Filter with Gain of −1, 20 kHz Cutoff Frequency, and Critical Damping

1. From Table I the inverting configuration must be used to realize a highpass gain of −1. An s-plane diagram of this function is shown in Figure 9. Critical damping requires the pole positions to be on a line 45° with respect to the real axis and this results in no frequency peaking. The damping factor d is:

$$d = \cos\phi = \cos 45° = 0.707$$

and

$$Q = \frac{1}{2d} = \frac{1}{2(0.707)} = 0.707$$

Because this is a low Q system the natural frequency will not be the same as the highpass cutoff frequency f_1. From Figure 9:

$$f_0 = \frac{f_1}{\cos\phi} = \frac{20 \text{ kHz}}{0.707} = 28.3 \text{ kHz}$$

Then $f_0Q = 0.707 \times 28.3 \times 10^3 = 2 \times 10^4$ and the Q will exceed its desired value by slightly over 1%.

2. From Table II, using Q = 0.707 we find:

R_1 = 10K ohms
R_2 = open

$$R_3 = \frac{100K}{6.64\,Q-1} = \frac{100K}{3.69} = 27.1K \text{ ohms}$$

3. Using f_0 = 28.3 kHz, R_4 and R_5 are found from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{28.3 \times 10^3} = 1.78K \text{ ohms}$$

4. This completes the highpass filter design which is shown in Figure 10. When using this filter, care should be exercised so that clipping does not occur in the filter due to excessive input levels. If clipping occurs, the filter will not operate properly. Clipping will first occur at the lowpass output around f_0 since its gain is 20 dB higher than the highpass output. The signal level should be reduced so that clipping does not occur anywhere in the frequency range used. If higher signal level is required, the highpass output should be amplified by a gain stage using the uncommitted operational amplifier.

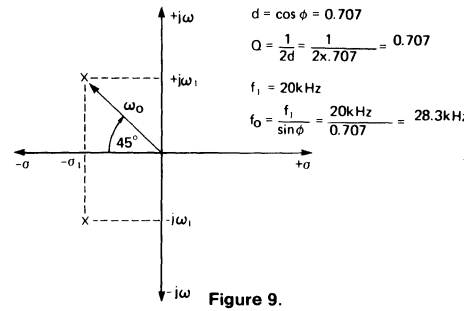


Figure 9.
S-Plane Diagram of Highpass Filter with Critical Damping

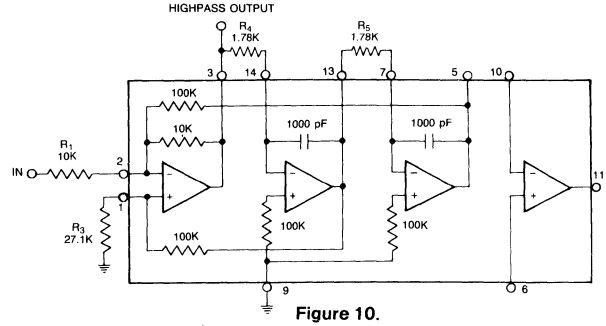


Figure 10.
Highpass Filter Example

6

ADVANCED FILTERS

All of the common filter types can be realized by using cascaded FLT-U2 stages. This includes multi-pole Butterworth, Bessel, Chebyshev, and Elliptic types. The basic procedure is to implement each pole pair with a single FLT-U2 and cascade enough units to realize all poles. A real axis pole is implemented by an uncommitted operational amplifier stage. Each stage should be separately tuned with an oscillator and scope and then the stages connected together and checked. See Figure 11.

A notch filter can be constructed in several ways. The first way is to use the FLT-U2 as an inverting bandpass filter and sum the output of the filter with the input signal by means of the uncommitted operational amplifier. This produces a net subtraction at the center frequency of the bandpass which produces a null at the output of the amplifier. (See Figure 12.) Likewise lowpass and highpass outputs (which are always in phase) can be subtracted from each other with an external operational amplifier. The highpass output must have some gain added to it, however, so that its gain is equal to that of the lowpass output. A third method is to use two separate FLT-U2's, one as a two-pole lowpass filter and the other as a two-pole highpass filter. Again the outputs are subtracted in an operational amplifier. This method permits independent tuning of the two sections to get the best null response.

Further discussion of filter designs is beyond the scope of this data sheet and the user is referred to the various texts on filter design, some of which are listed below.

Estep, G.J., *The State Variable Active Filter Configuration Handbook,* 2nd Edition, Agoura, Ca., 1974.

Reference Data for Radio Engineers, Howard W. Sams & Co. Inc., 5th Edition.

Christian, E., and Eisenmann, E., *Filter Design Tables and Graphs,* McGraw-Hill Book Co., 1974.

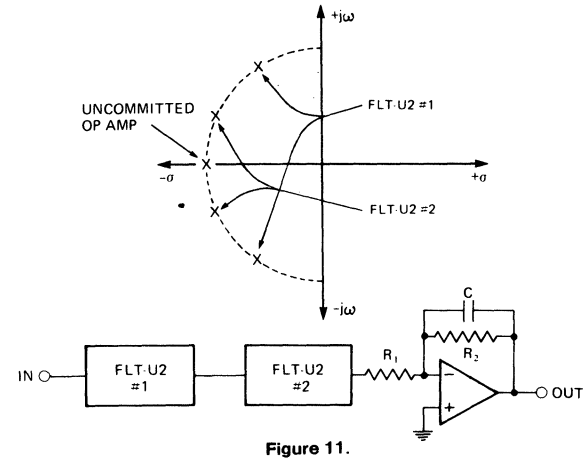


Figure 11.
Realization of a Complex Multipole Filter

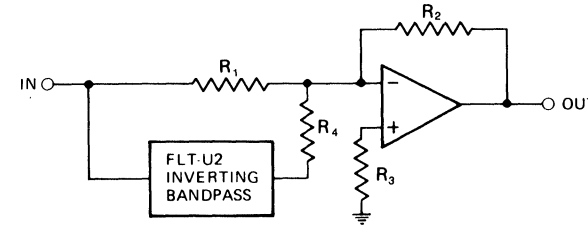


Figure 12.
Realization of Notch Filter

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
FLT-U2	0°C to +70°C
FLT-U2M	−55°C to +125°C

DATEL

PRODUCT DATA SHEET

ROJ-20,1K RESISTOR TUNEABLE OSCILLATOR

FEATURES

- **Oscillation frequency is set by two external resistors.**
- **Ultra-low distortion . . . 0.0018% typical.**
- **Stable.**
- **Small hybrid package.**

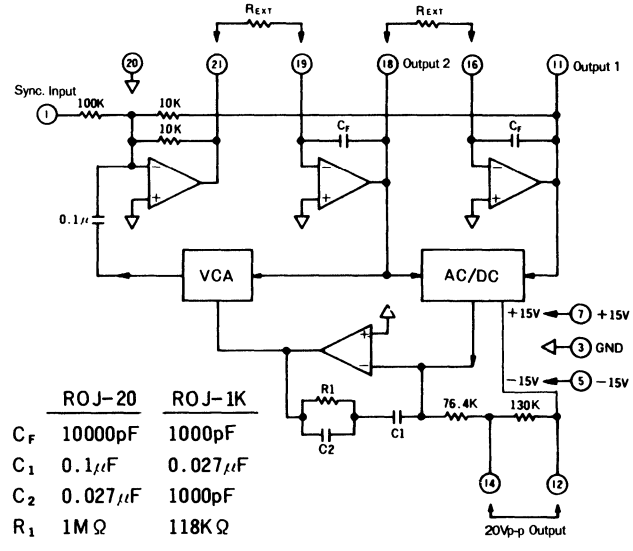
GENERAL DESCRIPTION

ROJ-20 and ROJ-1K are resistor tuneable osciliators whose oscillation frequency is set with two external resistors.

Output frequency range of the ROJ-20 is 20Hz to 20KHz while that of the ROJ-1K is 1KHz to 100KHz. Output distortion is as low as 0.0018% typical at 1KHz frequency range. Output voltage temperature coefficient is also as low as 50ppm/°C.

Output voltage amplitude is internally trimmed at 2.5 Vrms ±0.5% and this amplitude is adjusted to the range from 500 mV to 20 Vp-p with external resistors. Sine and cosine waves are generated from two output terminals. A synchronization input terminal is provided in order to fine tune the relationship of these two outputs.

Hybrid construction has made it possible to build highly stable oscillators in small size at low cost.

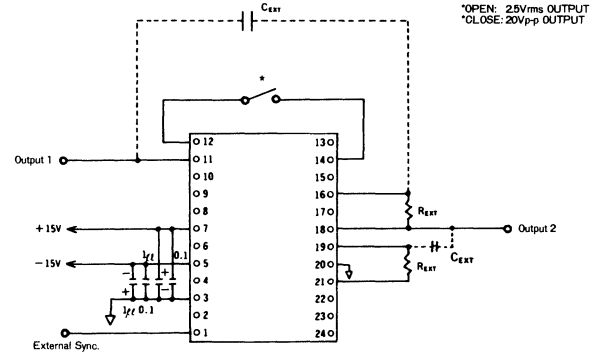


	ROJ-20	ROJ-1K
C_F	10000pF	1000pF
C_1	0.1μF	0.027μF
C_2	0.027μF	1000pF
R_1	1MΩ	118KΩ

BLOCK DIAGRAM (Fig. 1)

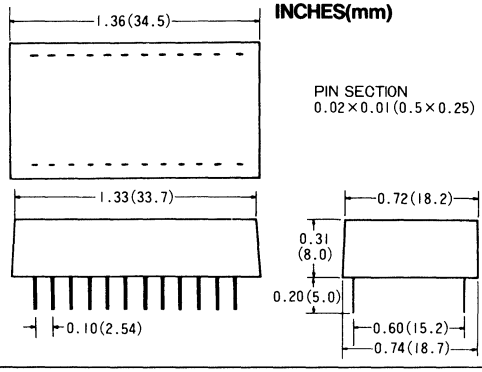
TECHNICAL NOTES

1. Typical connections are shown in Figure 3. Do not connect unused pins to any points. The external synchronization pin (Pin 1) is left open normally.
2. Output voltage level is 20Vp-p when the pins 12 and 14 are connected, 2.5Vrms when these pins are disconnected.
   Any output voltage level can be set using external resistors RV1 and RV2 as shown Figure 4-a and 5-a.
   The curves 4-b and 5-b show approximate values. The use of potentiometers



TYPICAL CONNECTIONS (Fig. 3)

MECHANICAL DIMENSIONS INCHES(mm)



PIN CONNECTIONS

PIN	FUNCTION
1	SYNCHRONIZATION INPUT
3	GND
5	−15V POWER SUPPLY
7	+15V POWER SUPPLY
11	OUTPUT 1
12	20Vp-p
14	20Vp-p
16	REXT
18	OUTPUT 2 (-90°)
19	REXT
20	GND
21	REXT

DO NOT CONNECT UNUSED PINS TO ANY.

SPECIFICATIONS

Typical value at 25°C with ±15VDC supplies unless otherwise specified.

	ROJ-20	ROJ-1K
OSCILLATED FREQUENCY		
Frequency Range (Note 1)	20Hz - 20KHz	1KHz - 100KHz
Accuracy, Calculated Frequency	0.5% @1KHz	0.5% @10KHz
Wave Shape	Sin, Cosin	* Same as left
OUTPUT CHARACTERISTICS		
Output Voltage/Current	±10V/5mA	*
Voltage Level Accuracy (Note 2)	2.5Vrms ±0.5%max.	*
" (20Vp-p, Note 3)	0.05% (<10KHz)	0.1% (<50KHz)
Distortion	0.0018% typ	*
	0.005% max. (70Hz - 10KHz)	* (2KHz - 50KHz) 0.01% max. (>50KHz)
Output Impedance	50 ohm max.	*
Load	2 Kohm min. 100pF max.	*
Voltage Level Tracking Error	0.4% (Rext1=Rext2)	*
Output Voltage TC	50ppm/°C	*
Frequency TC	15ppm/°C	25ppm/°C
POWER REQUIREMENTS & ENVIRONMENT		
Power Supply Voltage	±15V±10%	*
Power Supply Current	+14mA, -21mA	*
Operating Temperature Range	-20°C to +70°C	*
Storage Temperature Range	-30°C to +80°C	*
Relative Humidity	10% to 95% Non Condensing	*

Note 1. Two external resistors are:

ROJ-20 $Rext = \frac{15.9}{fo\ (KHz)}$ (Kohm)

ROJ-1K $Rext = \frac{159}{fo\ (KHz)}$ (Kohm)

Note 2. Pins 12 and 14 OPEN.

Note 3. Pins 12 and 14 CONNECTED.

are recommended when an accurate level of output is desired.

3. Output frequency can be slightly shifted toward lower frequency range if two Cext are added. See Figure 3. Relationship among Rext, Cext and fo are:

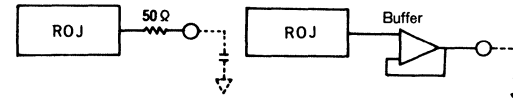
ROJ-20 $Rext = \frac{159}{(Cext + 0.01) \times fo}$ (Kohm)

Cext : μF fo : Hz

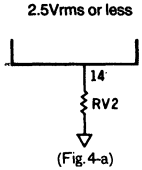
ROJ-1K $Rext = \frac{159}{(Cext + 0.001) \times fo}$ (Kohm)

4. Output frequency could become unstable if the capacitive load exceeds 100pF. The use of 50ohm resistor or an output buffer amplifier is recommended. See Figure 6.
5. Output frequency can be synchronized with the input from the pin 1. First, oscillate at nearly equal frequency to the one desired to be synchronized. Then, apply synchronization frequency to pin 1 at several Vrms level. Phase difference between synchronization input and output frequency vs. the frequency ratio is shown in Fig. 7.

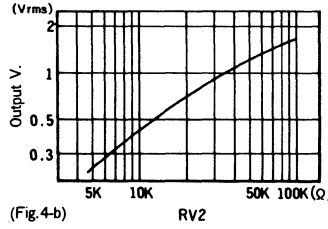
LARGE CAPACITIVE LOAD (Fig. 6) (Technical Note 4)



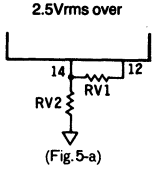
OUTPUT LEVEL ADJUSTMENT (Technical Note 2)



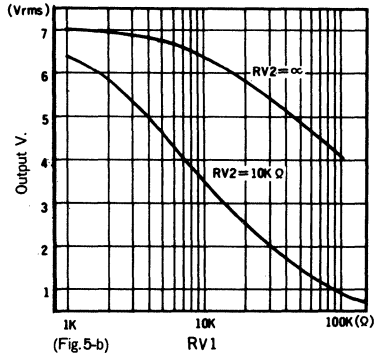
(Fig. 4-a)



(Fig. 4-b)

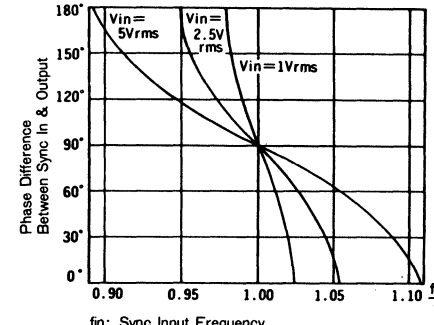


(Fig. 5-a)



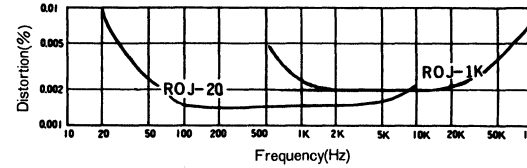
(Fig. 5-b)

PHASE DIFFERENCE BETWEEN SYNC INPUT AND OUTPUT (Fig. 7) (Technical Note 5)



fin: Sync Input Frequency
fo: Frequency when no Sync In is given.

DISTORTION vs. FREQUENCY (Fig. 8)



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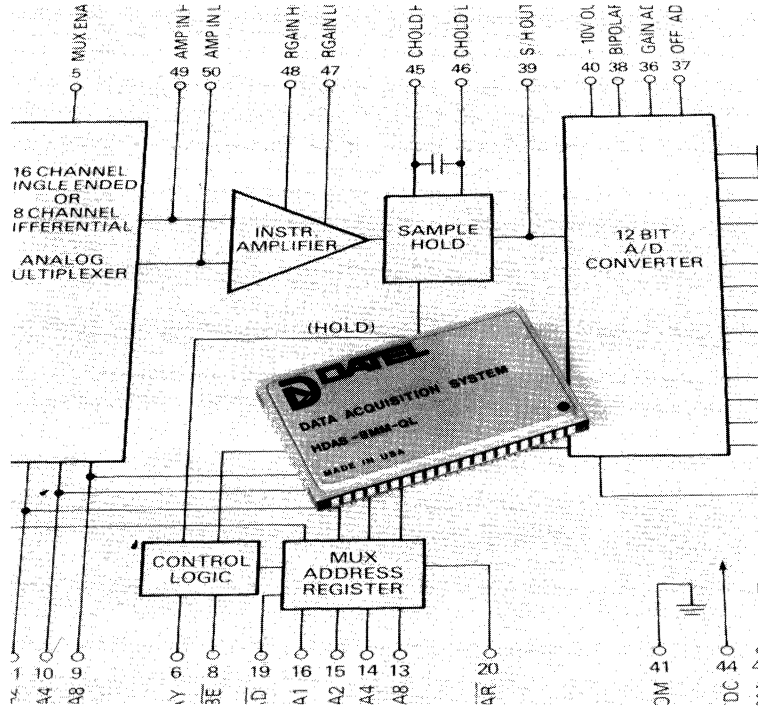
DATA ACQUISITION SUBSYSTEMS



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DATA ACQUISITION SUBSYSTEMS

MODEL	RESOLUTION	CHANNELS	THROUGH-PUT RATE	LINEARITY (MAX)	GAIN RANGE	INPUT RANGE	PACKAGE	TEMPERATURE RANGE (°C)	PAGE
DAS-952R	8 Bits	16 Single Ended	17 kHz	±1/2 LSB	—	0 to +5V	40-pin DIP Monolithic	-25 to +85	7-3
HDAS-8MC / **HDAS-8MM**	12 Bits	8 Diff.	50 kHz	±3/4 LSB	1 to 200	0 to +50 mV 0 to +10V ±50 mV to ±10V	62-pin Hybrid	0 to +70 / -55 to +125	7-9
HDAS-16MC / **HDAS-16MM**	12 Bits	16 Single Ended	50 kHz	±3/4 LSB	1 to 200	0 to +50 mV 0 to +10V ±50 mV to ±10V	62-pin Hybrid	0 to +70 / -55 to +125	7-9
MDAS-8D	12 Bits	8 Diff.	50 kHz	±1 LSB	—	0 to +5V 0 to +10V ±2.5V, ±5V, ±10V	Module	0 to +70	7-17
MDAS-16	12 Bits	16 Single Ended	50 kHz	±1 LSB	—	0 to +5V 0 to +10V ±2.5V, ±5V, ±10V	Module	0 to +70	7-17
MDAS-940D	12 Bits	8 Diff.	33 kHz	±1/2 LSB	1, 2, 4, 8	0 to +5V 0 to +10V ±5V, ±10V	Module	0 to +70	7-23
MDAS-940S	12 Bits	16 Single Ended	33 kHz	±1/2 LSB	1, 2, 4, 8	0 to +5V 0 to +10V ±5V, ±10V	Module	0 to +70	7-23

Output logic for all devices is three-state TTL.

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DAS-952R
16 Channel, 8-Bit Monolithic Data Acquisition System

FEATURES

- **16 Single-ended channels**
- **8-Bit resolution**
- **Monolithic CMOS construction**
- **Three-state outputs**
- **Ratiometric operation**
- **Low cost**

GENERAL DESCRIPTION

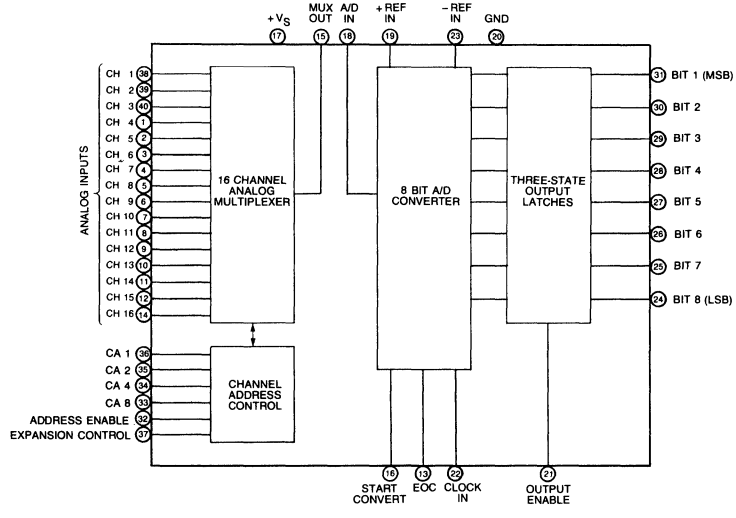
The DAS-952R is a single-chip, 16-channel, 8-bit data acquisition system. Using monolithic CMOS technology, this single DIP product includes a 16-channel multiplexer, an 8-bit successive approximation A/D converter, and microprocessor-compatible control logic.

The design of this system emphasizes high accuracy, excellent repeatability, low power consumption, and a minimum of adjustments (no full scale or zero adjustment required). Latched and decoded address inputs and latched TTL three-state outputs allow easy interfacing to microprocessors.

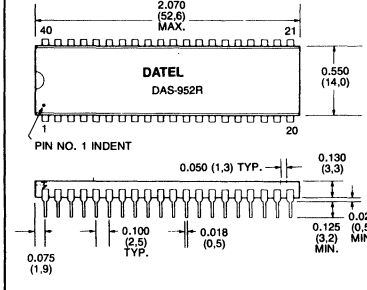
The input multiplexer allows random access to any one of 16 single-ended analog input channels and provides necessary logic for additional channel expansion. Connection of the multiplexer output to the converter input is by external pin connection. This permits easy signal conditioning such as amplification, linearization, or the use of a sample and hold.

The 8-bit A/D converter uses a 256R ladder network, successive approximation register, and a chopper-stabilized comparator to implement the successive approximation conversion technique with a switching tree. Using a 256R ladder network ensures monotonicity while the chopper-stabilizer comparator makes the converter highly resistant to thermal effects and long term drift. In ratiometric conversion, the converter expresses the analog value being measured as a percentage of reference input. Full-scale range may be selected within limits, to adjust the sensitivity of the converter to the desired application or to refer the output to a secondary standard.

Accuracy, speed, flexibility, excellent performance over a wide temperature range (−25°C to +85°C) and low cost make the DAS-952R an easy and practical answer to many data acquisition needs.



MECHANICAL DIMENSIONS (INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 4 IN	21	OUTPUT ENABLE
2	CH 5 IN	22	CLOCK INPUT
3	CH 6 IN	23	−REF. IN
4	CH 7 IN	24	BIT 8 OUT (LSB)
5	CH 8 IN	25	BIT 7 OUT
6	CH 9 IN	26	BIT 6 OUT
7	CH 10 IN	27	BIT 5 OUT
8	CH 11 IN	28	BIT 4 OUT
9	CH 12 IN	29	BIT 3 OUT
10	CH 13 IN	30	BIT 2 OUT
11	CH 14 IN	31	BIT 1 OUT (MSB)
12	CH 15 IN	32	ADDRESS ENABLE
13	E.O.C.	33	CA 8 INPUT
14	CH 16 IN	34	CA 4 INPUT
15	MULTIPLEXER OUTPUT	35	CA 2 INPUT
16	START CONVERT	36	CA 1 INPUT
17	+VS	37	EXPANSION CONTROL
18	A/D IN	38	CH 1 INPUT
19	+REF. IN	39	CH 2 INPUT
20	GROUND	40	CH 3 INPUT

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ABSOLUTE MAXIMUM RATINGS	
Voltage at Any Pin (Except Digital and REF inputs)	−0.3V to V_S +0.3V
Voltage at Digital Inputs	−0.3V to +15V
$+V_S$	+6.5V
+REF	V_S +0.1V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, $+V_{SUPPLY} = +V_{REF}$, $-V_{REF} = G_{ND}$, clock = 640 kHz unless otherwise noted.

ANALOG INPUTS	
Number of Channels	16 Single Ended[1]
Input Voltage Range	0 to +5.25V max.
Channel ON-Resistance	1.5KΩ typ., 3KΩ max.[2]
Channel ON-Resistance, 85°C	6KΩ max.
Channel OFF Leakage Current, V_{IN} = +5V	10 nA typ., 200 nA max.
Channel OFF Leakage Current, V_{IN} = 0V	−10 nA typ., −200 nA min.
Channel Input Capacitance	5 pF type., 7.5 pF max.
REF Input Resistance	1KΩ min., 4.5KΩ typ.[3]
REF Input Voltage	+0.512V to +5.25V[3]
A/D Converter Input Current[4]	±0.5 μA

DIGITAL INPUTS	
Logic high ("1") Threshold, min.	V_S −1.5V
Logic low ("0") Threshold, max.	+1.5V
Input Current, Max. high or low	1.0 μA
Input Capacitance	7.5 pF max.
Clock Frequency	10 kHz min., 1.2 MHz max.

DIGITAL OUTPUTS	
Logic high ("1") OUT, I_{OUT} = +360 μA	V_S −0.4V min.
Logic low ("0") OUT, I_{OUT} = −1.6 mA	+0.45V max.
EOC Logic low OUT, I_{OUT} = −1.2 mA	+0.45V max.
3-State Output Current, V_{OUT} = +5V	+3 μA max.
3-State Output Current, V_{OUT} = 0V	−3 μA max.
3-State Output Capacitance	10 pF
Output Coding	Straight Binary, Positive True

CONVERTER PERFORMANCE	
Resolution	8 Bits
Linearity Error	±½ LSB, max.
Zero Error	±½ LSB, max.
Full Scale Error	±½ LSB, max.
Total Unadjusted Error	±½ LSB, max.[5]
Power Supply Rejection	±0.15%/V max.[6]

DYNAMIC PERFORMANCE	
Conversion Time	100 μsec. typ., 116 μsec. max.[7]
MUX Delay, from ADDRESS ENABLE	1 μsec. typ., 2.5 μsec. max.
3-State Turn-ON Delay	250 nsec. max.

POWER REQUIREMENTS	
Supply Voltage, rated performance	+5V ±0.25V
Supply Voltage, operating range	+4.5V to +6V
Supply Current	300 μA typ., 3.0 mA max.

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package	40 Pin Plastic DIP

FOOTNOTES:

1. Logic is provided for expanding the number of channels externally.
2. Channel ON-resistances matched to within 75Ω maximum difference between any two channels.
3. Measured from +REF input to −REF input.
4. This is the comparator input current, a bias current into or out of the chopper stabilized comparator. It varies directly with clock frequency and is relatively independent of temperature.
5. Total unadjusted error is the sum of linearity, zero, and full-scale errors at any point on the transfer function.
6. V_S = +REF = +5V ±0.25V.
7. For clock frequency of 640 kHz. See technical note 4.

TECHNICAL NOTES

1. The analog input voltage is expressed as a percentage of full-scale voltage range. Full-scale voltage range may be varied from +0.512V to +5.25V. The system uses an 8-bit converter with the full-scale range divided into 256 steps (one step = 1 LSB). The ability to select the full-scale range by means of the reference voltage allows selection of the size of the LSB, thereby allowing selection of the converter's sensitivity. The center of the full-scale voltage range must be held within ±0.1V of the center of the supply range because the analog switch tree changes from N-channel switches to P-channel switches at this point. Failure to maintain the symmetry of these ranges may result in erratic switch operation. This condition is automatically satisfied in configurations where +REF = $+V_S$ and −REF = GND. For configurations where +REF < $+V_S$, −REF must be greater than GND by an equal amount. +REF can never exceed $+V_S$ and −REF can never be less than GND.
2. The system requires less than 1 mA of supply current. For applications where full scale range is selected between +4.75V and +5.25V, the reference can be used to generate the supply.
3. To preserve the accuracy of the system over its full operating temperature range, the reference source should have a temperature coefficient of 20 ppm/°C or less. For ambient temperature changes less than 75°C, a reference temperature coefficient of 30 ppm/°C is sufficient to maintain accuracy.
4. Conversion time and throughput rate for the DAS-952R is dependent on external clock frequency. The clock may be varied from 10 kHz to 1.2 MHz (see comparator input current graph).

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DESCRIPTION OF OPERATION

Any one of 16 single-ended analog inputs may be selected by using the address decoder. The multiplexer input selection table shows the channel address input states required to select each channel. Channel address input states are latched into the address decoder on the low-to-high transition of the ADDRESS ENABLE input. Channel address inputs are required to be stable for 50 nanoseconds before and after the ADDRESS ENABLE low-to-high transition. Additional channel expansion is accomplished by disabling the internal multiplexer (all channels are off when EXPANSION CONTROL input is low) and connecting the additional signals directly to the converter input.

The converter input may also be used to introduce various signal conditioning devices into the analog signal path. The analog signal at the multiplexer input selected is available to the comparator after a maximum delay time of 2.5 microseconds. The converter's successive approximation register is reset on the positive going edge of 200 nanoseconds start conversion pulse, and conversion is initiated on the falling edge of the pulse.

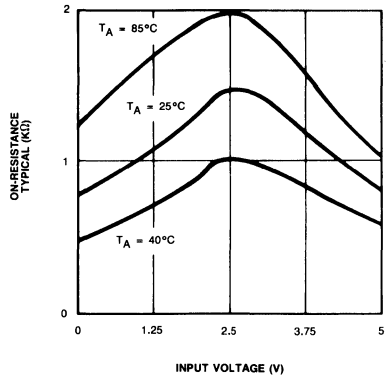
A conversion in progress may be interrupted by a new start conversion pulse. The EOC output goes low in 1 to 8 clock periods after the rising edge of the start conversion pulse. For continuous conversions the EOC output can be tied to the start conversion input and an initial external start conversion pulse applied after power up.

The 8-bit A/D converter requires 64 clock periods to resolve the analog signal voltage level. The converter employs a chopper-stabilized comparator for extreme resistance to input offset drift errors. The 256R ladder network ensures monotonicity and does not cause load variations on the reference voltage. The values of the top and bottom resistors are different from the rest of the ladder so that the first output transition occurs when the analog voltage level reaches +½ LSB and each succeeding output transition occurs at intervals of 1 LSB up to full scale.

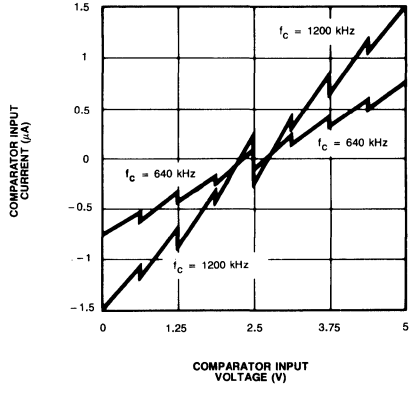
The 8-bit, straight binary, positive true result appears at the three-state output latches, which are enabled when the OUTPUT ENABLE control is high.

TYPICAL PERFORMANCE

MULTIPLEXER ON RESISTANCE



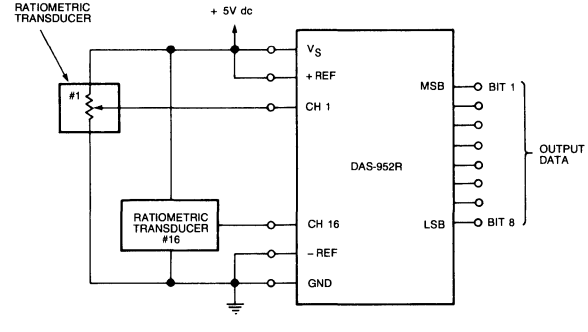
COMPARATOR INPUT CURRENT



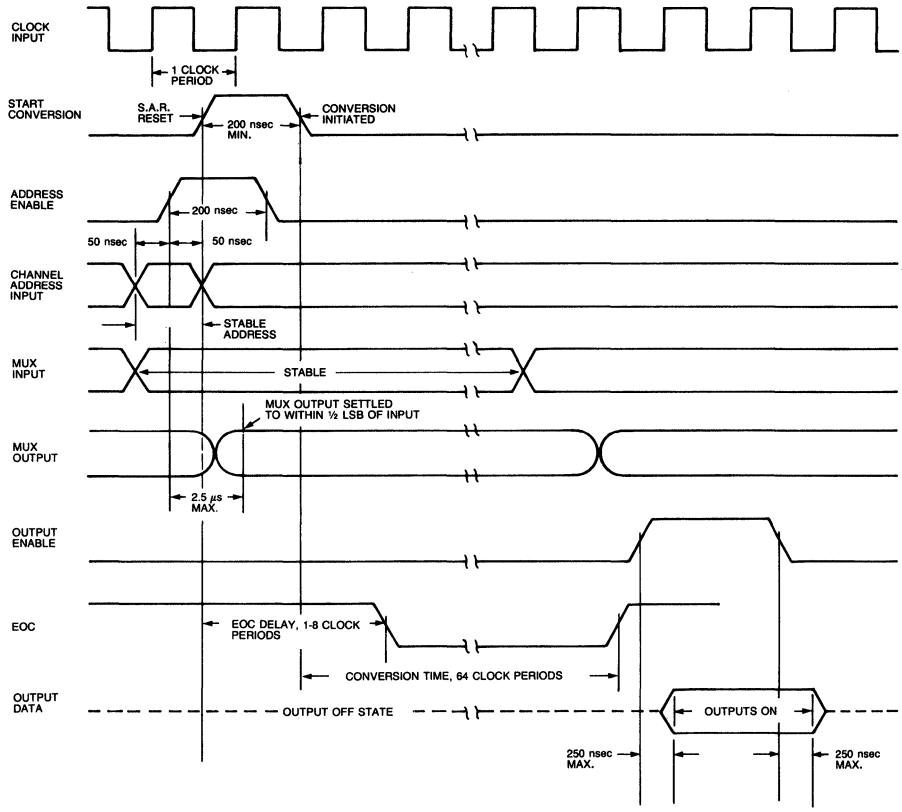
CHANNEL ADDRESS TABLE

CHANNEL ADDRESS INPUT 8	4	2	1	INHIBIT CONTROL	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

RATIOMETRIC CONVERSION SYSTEM

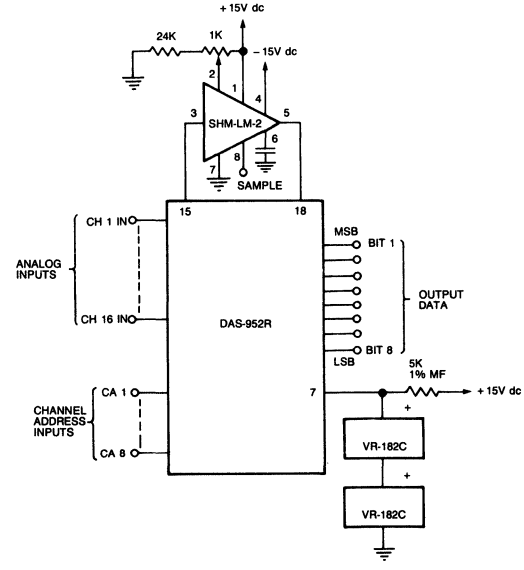


TIMING DIAGRAM



DATA ACQUISITION SYSTEM WITH SAMPLE-HOLD

For applications where a sample-hold is required, connections are made as shown in the accompanying diagram. The sample-hold may be put in the sample mode after the multiplexer output settles (see timing diagram). The start conversion input can be taken high as shown in the timing diagram but should not be taken low until the sample-hold has acquired the input voltage. The acquisition time of the sample-hold is dependent on the value of the hold capacitance. This value must be selected for the acquisition time and hold-mode voltage droop required by the converter speed and accuracy, respectively. Optimal values of hold capacitance may be selected after throughput rate is determined. See SHM-LM-2 data sheet.



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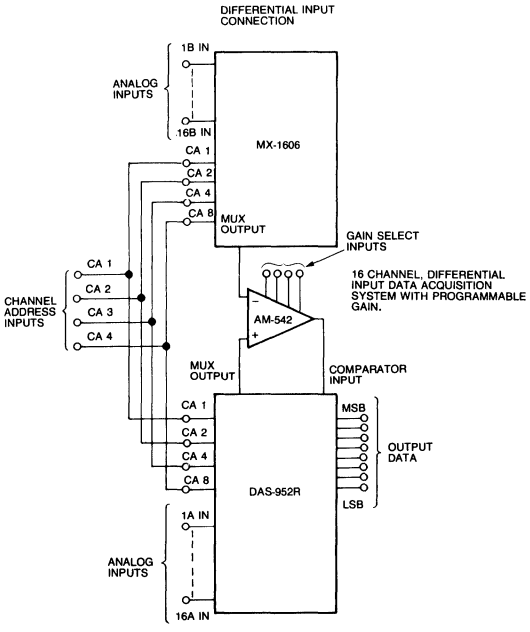
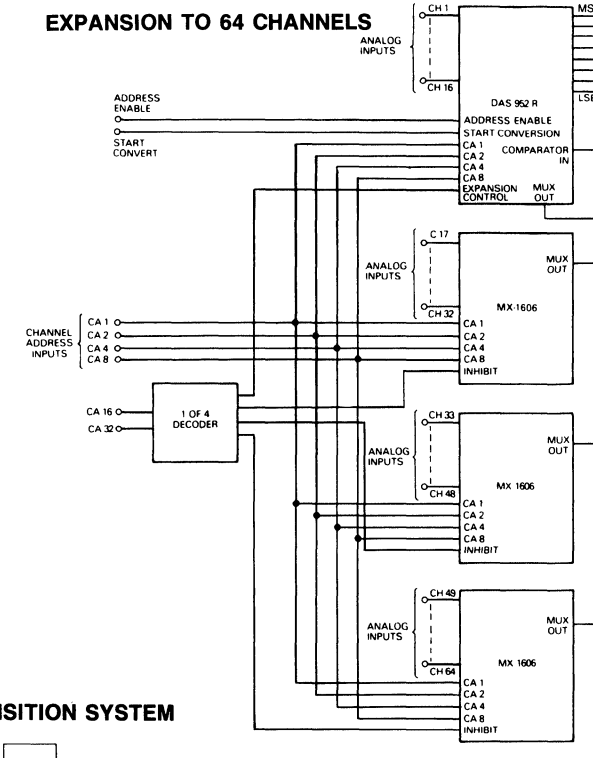
APPLICATIONS

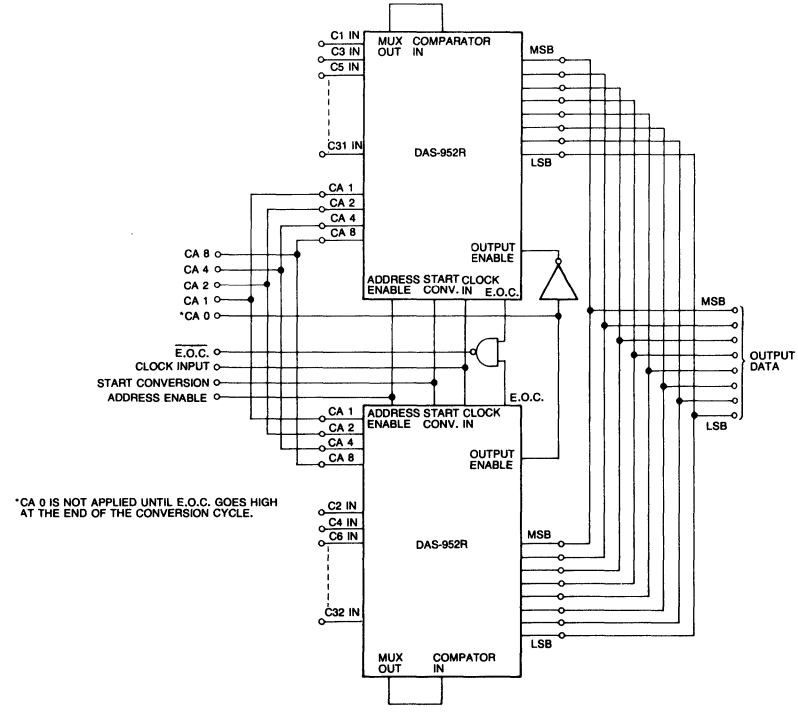
DIFFERENTIAL INPUT CONNECTION



EXPANSION TO 64 CHANNELS



32 CHANNEL, 35 kHz DATA ACQUISITION SYSTEM



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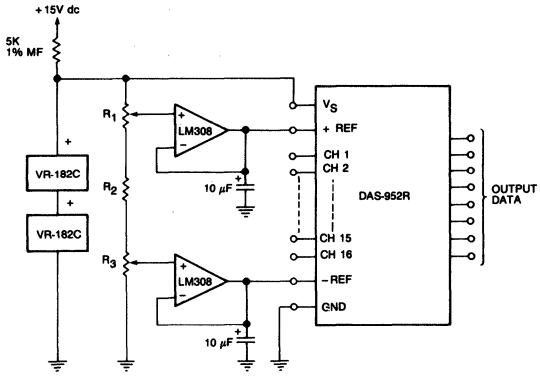
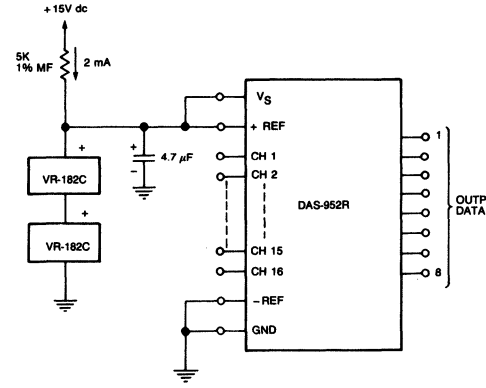
REFERENCE AND SUPPLY CIRCUITS

DUAL ADJUSTABLE REFERENCE

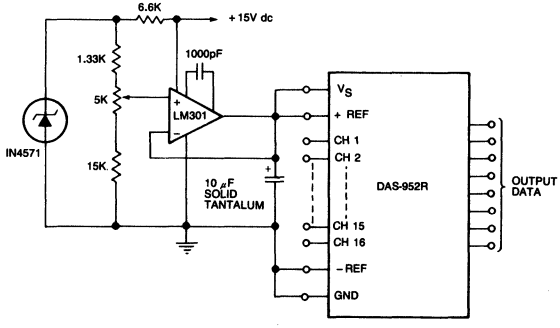


NOTE: VALUES OF R_1, R_2 AND R_3 ARE SELECTED TO YIELD THE DESIRED FULL SCALE CONVERSION RANGE. SEE TECHNICAL NOTE 1.

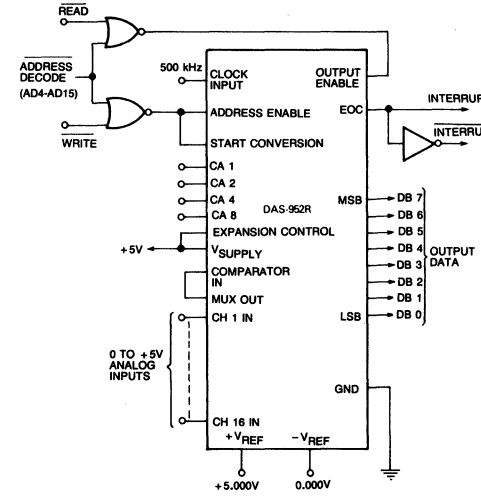
30 PPM/°C REFERENCE AND SUPPLY



ADJUSTABLE REFERENCE AND SUPPLY



TYPICAL MICROPROCESSOR INTERFACE



ORDERING INFORMATION

MODEL	DESCRIPTION
DOS-952R	16 Channel, 8-Bit Monolithic Data Acquisition System

HDAS-16, HDAS-8
12-Bit Microelectronic Data Acquisition Systems

FEATURES

- **Miniature 62-pin hermetic package**
- **12-Bit resolution, 50 KHz**
- **Full-scale gain range of 50 mV to 10V**
- **Three-state outputs**
- **16 Channels single-ended or 8 channels differential**
- **Auto-sequencing channel addressing**
- **MIL-STD-883 versions**

GENERAL DESCRIPTION

Using thin-and thick-film hybrid technology, DATEL offers complete low-cost data acquisition systems with superior performance and reliability.

The HDAS-8 (with 8 differential input channels), and the HDAS-16 (with 16 single-ended input channels), are complete high performance 12-bit data acquisition systems in 62-pin packages. Each HDAS may expand to 32 single-ended or 16 or more differential channels by adding external multiplexers.

Combined acquisition and A/D conversion time is 20 microseconds maximum, giving a minimum throughput rate of 50 KHz. The 12-bit binary data may be transferred out in three 4-bit bytes using the three-state data bus drivers. Output coding is straight binary in unipolar operation, and offset binary in bipolar operation.

Internal HDAS circuitry includes:

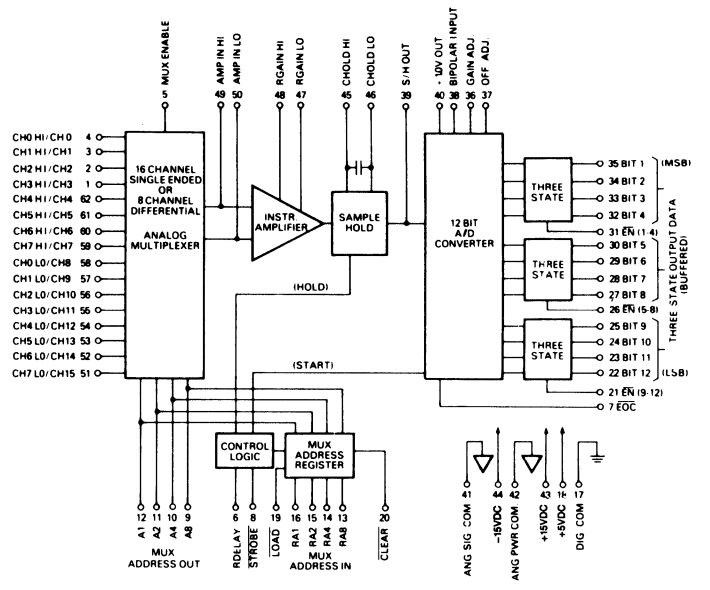
- Analog signal multiplexer
- Resistor programmable gain instrumentation amplifier
- A sample-and-hold circuit, complete with MOS hold capacitor
- a 10 volt buffered reference
- A 12-bit A/D converter with three-state outputs and control logic.

All that is required to power the HDAS devices are external +5V and ±15V dc supplies.

Internal channel address sequencing is automatic after each conversion, or the user may supply external channel addresses.

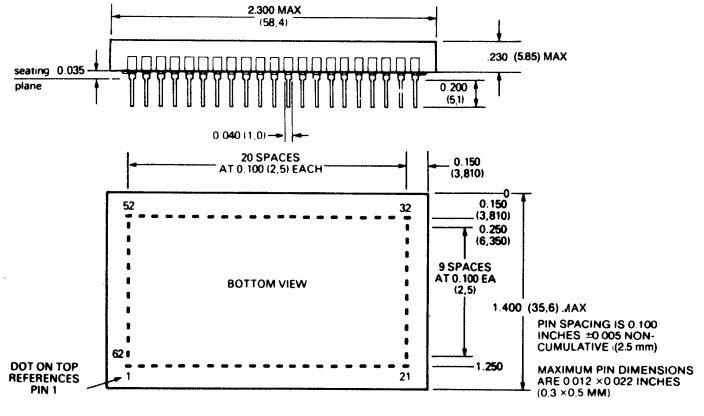
The internal instrumentation amplifiers are supplied with a gain of 1 and a 10 volt full-scale range. An external resistor may be added to achieve gains of up to 200, corresponding to a 50 mV full-scale input range. This key feature is useful in low-level signal applications involving bridge amplifiers, transducers, strain gauge and thermocouple interfaces.

The HDAS devices are cased in a 62-pin hermetic package measuring 1.4″ W × 2.3″ L × 0.23″ H. Models are available in two temperature ranges: 0 °C to +70 °C and −55 °C to +125 °C.



HDAS-16/HDAS-8 Simplified Block Diagram

MECHANICAL DIMENSIONS — INCHES (MM)



ABSOLUTE MAXIMUM RATINGS			
Parameters	**Min.**	**Max.**	**Units**
+15V Supply (Pin 43)	−0.5	+18	Volts dc
−15V Supply (Pin 44)	+0.5	−18	Volts dc
+5V Supply (Pin 18)	−0.5	+7	Volts dc
Analog Inputs (Note 1)	−35	+35	Volts
Digital Inputs	−0.5	+7	Volts
Thermal Resistance			
Junction-Case		13	°C/Watt
Case-Ambient		17	°C/Watt
Junction-Ambient		30	°C/Watt
Power Dissipation		1.75	Watts
Lead Temp. (10 Sec.)		300	°C

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Signal Range				
Unipolar				
Gain = 1	0	—	+10	Volts
Gain = 200	0	—	+50	mV
Bipolar				
Gain = 1	−10	—	+10	Volts
Gain = 200	−50	—	+50	mV
Input Gain Equation (Note 2)	Gain = 1 ± (20K Ohm/RGAIN)			
Gain Equation Error	—	—	±0.1	%
Instrumentation Amp.				
Input Impedance	10^8	10^{12}	—	Ohms
Input Bias Current:				
0°C to +70°C	—	—	±250	pA
−55°C to +125°C	Doubles every 10°C above 70°C			
Input Offset Current:				
0°C to +70°C	—	—	±1	nA
−55°C to +125°C	Doubles every 10°C above 70°C			
Multiplexer				
Channel ON Resistance	—	—	2.0	K Ohms
Channel OFF Input Leakage	—	30	—	pA
Channel OFF Output Leakage	—	1.0	—	nA
Channel ON Leakage	—	100	—	pA
Input Capacitance				
HDAS-16, Channel On	—	100	—	pF
HDAS-8, Channel On	—	50	—	pF
+25°C, Channel Off	—	5	—	pF
Input Offset Voltage				
Gain = 1 to 200, +25°C	—	—	±2	mV
−55°C to +125°C	± (30ppm/°C × Gain) ppm/°C (max)		±20	
Common Mode Range	±11	—	—	Volts
CMRR, Gain = 1, at 60 Hz	−70	−82	—	dB
Input Voltage Noise (Referred to Input)				
Gain = 1	—	150	200	µV RMS
Channel Crosstalk	−80	—	—	dB
PERFORMANCE				
Resolution	12	—	—	Bits
Integral Nonlinearity:				
+25°C	—	—	±¾	LSB
0°C to 70°C	—	—	±1	LSB
−55°C to +125°C	—	—	±1	LSB

PERFORMANCE (cont.)	MIN.	TYP.	MAX.	UNITS
Differential Nonlinearity:				
+25°C	—	—	±¾	LSB
0°C to 70°C	—	—	±1	LSB
−55°C to +125°C	—	—	±1	LSB
Differential Nonlinearity Tempco	—	—	±2	ppm/°C
Unipolar Zero Error				
+25°C (Note 3)	—	—	±0.1	%FSR
−55°C to +125°C	—	—	±0.3	%FSR
Unipolar Zero Tempco	—	—	±20	ppm/°C
Bipolar Zero Error				
±25°C (Note 3)	—	—	+0.1	%FSR
−55°C to +125°C	—	—	±0.3	%FSR
Bipolar Zero Tempco	—	—	±35	ppm/°C
Bipolar Offset Error				
+25°C (Note 3)	—	—	0.1	%FSR
−55°C to +125°C	—	—	0.3	%FSR
Bipolar Offset Tempco	—	—	±35	ppm/°C
Gain Error				
+25°C (Note 3)	—	—	±0.2	%FSR
−55°C to +125°C	—	—	±0.3	%FSR
Gain Error Tempco	—	—	±30	ppm/°C
No Missing Codes	Over the operating temperature range			
DYNAMIC CHARACTERISTICS				
Acquisition Time,				
At Gain = 1, +25°C	—	9	10	µSec.
−55°C to +125°C	—	—	15	µSec.
At Gain = 10, +25°C	—	9	—	µSec.
At Gain = 50, +25°C	—	16	—	µSec.
At Gain = 200, +25°C	—	60	—	µSec.
Aperture Delay Time	—	100	500	nSec.
Aperture Uncertainty	—	—	1	nSec.
S/H Droop Rate	—	—	800	mV/Sec.
Feedthrough Accuracy	—	—	±0.01	%
A/D Conversion Time:				
+25°C	—	9	10	µSec.
−55°C to +125°C	—	—	15	µSec.
Throughput Rate				
+25°C	50	55	—	KHz
−55°C to +125°C	33	—	—	KHz
DIGITAL INPUTS				
Logic Levels: (Pins 5, 8, 13, 14, 15, 16, 19, and 20)				
Logic 1	2.0	—	5.5	Volts
Logic 0	0	—	0.8	Volts
(Pins 21,26, 31)				
Logic 1	2.0	—	5.5	Volts
Logic 0	0	—	0.7	Volts
Logic Loading: (Pins 5, 8, 13, 14, 15, 16, 19, and 20)				
Logic 1	—	—	1	µA
Logic 0	—	—	−280	µA
(Pins 21, 26, 31)				
Logic 1	—	—	20	µA
Logic 0	—	—	−0.40	µA
Multiplexer Address Set-up Time	20	—	—	nSec.
Enable to Data Valid Delay	—	20	30	nSec.
$\overline{\text{STROBE}}$ (Note 4)	40	—	—	nSec.

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OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels:				
(Pin 7 & Output Data)				
Logic 1	2.4	—	—	Volts
Logic 0	—	—	0.4	Volts
(Pins 9, 10, 11, and 12)				
Logic 1	4.4	—	—	Volts
Logic 0	—	—	0.1	Volts
Logic Loading:				
Logic 1	—	—	400	µA
Logic 0	—	—	4	mA
Internal Reference:				
Voltage, +25°C	+9.99	+10.00	+10.01	Volts dc
Drift	—	—	±20	ppm/°C
External current	—	—	1	mA
Data Output Coding	Straight binary (unipolar) or offset binary (bipolar)			
POWER REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.5	+15.0	+15.5	Volts dc
−15V dc Supply	−14.5	−15.0	−15.5	Volts dc
+5 dc Supply	+4.75	+5.0	+5.25	Volts dc
Supply Current:				
+15V Supply	—	—	+40	mA
−15V Supply	—	—	−45	mA
+5V Supply	—	—	+95	mA
Power Dissipation	—	1.45	1.75	Watts
PHYSICAL — ENVIRONMENTAL				
Operating Temperature Range:				
MC Models	0	—	+70	deg. C
MM Models	−55	—	+125	deg. C
Storage Temperature Range:	−65	—	+150	deg. C
Weight		1.4(39.7)		oz. (gram)
Package Type	62-pin hermetically sealed Ceramic DIP			
Pin Type	Kovar			

SPECIFICATION NOTES

1. Analog inputs will withstand ±35 volts with power on. If the power is off, the maximum safe input (no damage) is ±20 volts.
2. The gain equation error is guaranteed before external trimming and applies at gains under 50. This error increases at gains over 50.
3. Adjustable to zero.
4. $\overline{\text{STROBE}}$ pulse width must be smaller than $\overline{\text{EOC}}$ period to achieve maximum throughput rate.

TECHNICAL NOTES

1. Input channels are protected to 20 volts beyond the power supplies. All digital output pins have one second short circuit protection; CHOLD has a ten second short circuit protection.
2. To retain high system throughput rate while digitizing low level signals, apply external high-gain amplifiers for each channel. Datel's AM-551 is suggested for such amplifier-per-channel applications.
3. The HDAS devices have self-starting circuits for free-running sequential operation. If, however, in a power-up condition the supply voltage slew rate is less than 3V per microsecond, the free running state might not be initialized. Apply a negative pulse to the $\overline{\text{STROBE}}$, to eliminate this condition.
4. For unipolar operation, connect BIPOLAR INPUT (pin 38) to S/H OUT (pin 39). For bipolar operation, connect BIPOLAR INPUT (pin 38) to +10V REFERENCE OUT (pin 40).
5. RDELAY may be a standard value 5% carbon composition or film type resistor.
6. RGAIN must be very accurate with low temperature coefficients. If necessary, fabricate the gain resistor from a precision metal film type in series with a low value trim resistor or potentiometer. The total resistor temperature coefficient must be no greater than ± 10 ppm/°C.

PIN CONNECTIONS

PIN NO.	HDAS-16	HDAS-8
1	CH3 IN	CH3 HIGH IN
2	CH2 IN	CH2 HIGH IN
3	CH1 IN	CH1 HIGH IN
4	CH0 IN	CH0 HIGH IN
5	MUX ENABLE	*
6	R DELAY	*
7	$\overline{\text{EOC}}$	*
8	$\overline{\text{STROBE}}$	*
9	A8 MULTIPLEXER	*
10	A4 ADDRESS	*
11	A2 OUT	*
12	A1	*
13	RA8 MULTIPLEXER	*
14	RA4 ADDRESS	*
15	RA2 IN	*
16	RA1	*
17	DIGITAL COMMON	*
18	+5V dc	*
19	$\overline{\text{LOAD ENABLE}}$	*
20	$\overline{\text{CLEAR ENABLE}}$	*
21	$\overline{\text{ENABLE}}$ (Bits 9–12)	*
22	BIT 12 OUT (LSB)	*
23	BIT 11 OUT	*
24	BIT 10 OUT	*
25	BIT 9 OUT	*
26	$\overline{\text{ENABLE}}$ (Bits 5–8)	*
27	BIT 8 OUT	*
28	BIT 7 OUT	*
29	BIT 6 OUT	*
30	BIT 5 OUT	*
31	$\overline{\text{ENABLE}}$ (Bits 1–4)	*
32	BIT 4 OUT	*
33	BIT 3 OUT	*
34	BIT 2 OUT	*
35	BIT 1 OUT (MSB)	*
36	GAIN ADJUST	*
37	OFFSET ADJUST	*
38	BIPOLAR INPUT	*
39	SAMPLE/HOLD OUT	*
40	+10V OUT	*
41	ANALOG SIGNAL COMMON	*
42	ANALOG POWER COMMON	*
43	+15V dc	*
44	−15V dc	*
45	C HOLD HIGH	*
46	C HOLD LOW	*
47	R GAIN LOW	*
48	R GAIN HIGH	*
49	AMP. IN HIGH[1]	*
50	AMP. IN LOW[1]	*
51	CH15 IN	CH7 LOW IN
52	CH14 IN	CH6 LOW IN
53	CH13 IN	CH5 LOW IN
54	CH12 IN	CH4 LOW IN
55	CH11 IN	CH3 LOW IN
56	CH10 IN	CH2 LOW IN
57	CH9 IN	CH1 LOW IN
58	CH8 IN	CH0 LOW IN
59	CH7 IN	CH7 HIGH IN
60	CH6 IN	CH6 HIGH IN
61	CH5 IN	CH5 HIGH IN
62	CH4 IN	CH4 HIGH IN

* Same as HDAS-16

1. Caution: pins 49 and 50 do not have overvoltage protection; therefore, protected multiplexers, such as DATEL's MX-1606 an MX-808 are recommended. See the channel expansion description.

7

Table 1. Description of Pin Functions

FUNCTION	LOGIC STATE	DESCRIPTION
DIGITAL INPUTS		
$\overline{\text{STROBE}}$	1 to 0	Initiates acquisition and conversion of analog signal
$\overline{\text{LOAD}}$	0	Random Address Mode Initiated on falling edge of $\overline{\text{STROBE}}$
	1	Sequential Address Mode
$\overline{\text{CLEAR}}$	0	Allows next $\overline{\text{STROBE}}$ pulse to reset MULTIPLEXER ADDRESS to CH0 overriding $\overline{\text{LOAD}}$ COMMAND
MULTIPLEXER ENABLE	0	Disables internal MULTIPLEXER
	1	Enables internal MULTIPLEXER
MULTIPLEXER ADDRESS IN		Selects channel for Random Address Mode 8, 4, 2, and 1 natural binary coding
DIGITAL OUTPUTS		
$\overline{\text{EOC}}$		End of Conversion (STATUS)
	0	Conversion complete
	1	Conversion in process
$\overline{\text{ENABLE}}$ (1-4)	0	Enables three-state outputs bits 1-4
	1	Disables three-state outputs bits 1-4
$\overline{\text{ENABLE}}$ (5-8)	0	Enables three-state outputs bits 5-8
	1	Disables three-state outputs bits 5-8
$\overline{\text{ENABLE}}$ (9-12)	0	Enables three-state outputs bits 9-12
	1	Disables three-state outputs bits 9-12
MULTIPLEXER ADDRESS OUT		Output of MULTIPLEXER Address Register 8, 4, 2, 1 natural binary coding
ANALOG INPUTS		
Channel Inputs		Limit voltage to ±20V beyond power supplies.
Bipolar Input		For unipolar operation, connect to pin 39 (S/H OUT) For biploar operation, connect to pin 40 (+10V OUT)
AMP. IN HIGH AMP. IN LOW		These pins are direct inputs to the instrumentation amplifier for external channel expansion beyond 16SE or 8D channels.
ANALOG OUTPUTS		
S/H OUT		Sample/Hold Output
+10V OUT		Buffered +10V reference output
ADJUSTMENT PINS		
ANALOG SIGNAL COMMON		Low level analog signal return
GAIN ADJUSTMENT		External gain adjustment, see calibration instructions.
OFFSET ADJUSTMENT		External offset adjustment. See calibration instructions.
R GAIN		Optional gain selection point. Factory adjusted for G = 1 when left open.
C HOLD		Optional hold capacitor connection.
R DELAY		Optional acquisition time adjustment when connected to +5V, factory adjusted for 9 μSec. Must be connected to +5V either directly or through a resistor.

Table 2. Calibration Table

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

CALIBRATION PROCEDURES

1. Offset and gain adjustments are made by connecting two 20K trim potentiometers as shown in Figure 1.
2. Connect a precision voltage source to pin 4 (CH0 IN). If the HDAS-8 is used, connect pin 58 (CH0 LOW IN) to analog ground. Ground pin 20 ($\overline{\text{CLEAR}}$) and momentarily short pin 8 ($\overline{\text{STROBE}}$). Trigger the A/D by connecting pin 7 ($\overline{\text{EOC}}$) to pin 8 ($\overline{\text{STROBE}}$). Select proper value for RGAIN and RDELAY by referring to Table 3.
3. Adjust the precision voltage source to the value shown in Table 2 for the unipolar zero adjustment (ZERO + ½ LSB) or the bipolar offset adjustment (−FS + ½ LSB). Adjust the offset trim potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
4. Change the output of the precision voltage source to the value shown in Table 2 for the unipolar or bipolar gain adjustment (+FS − 1½ LSB). Adjust the gain trim potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

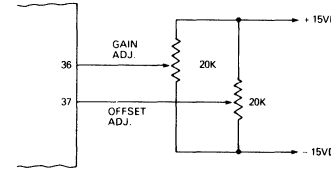


Figure 1. External Adjustment

THEORY OF OPERATION

The HDAS devices accept either 16 single-ended or 8 differential input signals. For single-ended circuits, the AMP IN LO (pin 50) input to the instrumentation amplifier must terminate at ANALOG SIGNAL COMMON (pin 41). For differential circuits, both the HI and LO signal inputs must terminate externally for each channel. Tie unused channels to the ANALOG SIGNAL COMMON (pin 41). Obtain additional channels by connecting external multiplexers to the AMP IN HI (pin 49) and the AMP IN LO (pin 50), (See Figures 5 and 6).

The acquisition time is the amount of time the multiplexer, instrumentation amplifier, and Sample/Hold require to settle within a specified range of accuracy after $\overline{\text{STROBE}}$ (pin 8) goes low. The acquisition time period can be observed by measuring how long $\overline{\text{EOC}}$ is low after the falling edge of $\overline{\text{STROBE}}$ (See Figure 2.) For higher gains increase the acquisition time. Do this by connecting a resistor from RDELAY (pin 6) to +5V (pin 18). An external resistor, RGAIN, can be added to increase the gain value. The gain

Table 3. Input Range Parameters (Typical)

INPUT RANGE	GAIN	RGAIN (Ω)	ACQUISITION AND SETTLING DELAY	RDELAY (Ω)	THROUGHPUT	SYSTEM ACCURACY (%of FSR)
±10V	1	OPEN	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±5V	2	20.0K	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±2.5V	4	6.667K	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±1V	10	2.222K	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±200 mV	50	408.2	16 μSec.	7K	40.0 KHz	0.010%
±100 mV	100	202.0	30 μSec.	21K	25.6 KHz	0.011%
±50 mV	200	100.5	60 μSec.	51K	14.5 KHz	0.016%

NOTES

$$RGAIN\ (\Omega) = \frac{20{,}000}{(GAIN-1)} \qquad RDELAY\ (\Omega) = \frac{(Delay\ \mu sec. \times 1000)}{} - 9000$$

1. For gains between 1 and 10, RDELAY (pin 6) must be shorted to +5V (pin 18).
2. Throughput period equals Acquisition and Settling Delay, plus A/D conversion period (10 microseconds maximum).
3. The analog input range to the A/D converter is 0 to +10V for unipolar signals, and −10.0V to +10.0V for bipolar signals.
4. Full-scale can be accommodated for analog signal ranges of ±50mv to ±10V.

is equal to 1 without an RGAIN resistor. Table 3 refers to the appropriate RDELAY and RGAIN resistors required for various gains.

The HDAS devices enter the hold mode and are ready for conversion as soon as the one-shot (controlling acquisition time) times out. An internal clock is gated ON, and a start-convert pulse is sent to the 12-bit A/D converter, driving the EOC output high.

The HDAS devices can be configured for either bipolar or unipolar operation. (See Table 2). The conversion is complete within a maximum of 10 microseconds. The EOC now returns low, the data is valid and sent to the three-state output buffers. The sample/hold amplifier is now ready to acquire new data. The next falling edge of the STROBE pulse repeats the process for the next conversion.

Table 4. Output Coding

	UNIPOLAR		STRAIGHT BINARY
	0 to +10V	0 to +5V	
+FS − 1 LSB	+9.9976	+4.9988	1111 1111 1111
+½FS	+5.0000	+2.5000	1000 0000 0000
+1 LSB	+0.0024	+0.0012	0000 0000 0001
ZERO	0.0000	0.0000	0000 0000 0000

	BIPOLAR		OFFSET BINARY*
	±10 V	±5V	
+FS − 1 LSB	+9.9951	+4.9976	1111 1111 1111
+½FS	+5.0000	+2.5000	1100 0000 0000
+1 LSB	+0.0049	+0.0024	1000 0000 0001
ZERO	0.0000	0.0000	1000 0000 0000
−FS + 1 LSB	−9.9951	−4.9976	0000 0000 0001
−FS	−10.000	−5.0000	0000 0000 0000

*For 2's complement — add inverter to MSB line.

MULTIPLEXER ADDRESSING

The HDAS devices can be configured in either random or sequential addressing modes. Refer to Table 5 and the subsequent descriptions. The number of channels sequentially addressed can be truncated using the MUX ADDRESS OUT (pins 9, 10, 11 and 12) and appropriate decoding circuitry for the highest channel desired. The decoding circuit can drive the CLEAR (pin 20) function low to reset the addressing to channel 0.

RANDOM ADDRESS

Set pin 19 (LOAD) to logic 0. The next falling edge of STROBE will load the MUX CHANNEL ADDRESS present on pin 13 to pin 16. Digital address inputs must be stable 20 nanoseconds before and after falling edge of STROBE pulse.

FREE RUNNING SEQUENTIAL ADDRESS

Set pin 19 (LOAD) and pin 20 (CLEAR) to logic 1 or leave open. Connect pin 7 (EOC) to pin 8 (STROBE). The falling edge of EOC will increment channel address. This means that when the EOC is low, the digital output data is valid for the previous channel (CHn −1) than the channel indicated on MUX ADDRESS OUTPUT. The HDAS will continually scan all channels.

Example:

CH4 has been addressed and a conversion takes place. The EOC goes low. That channel's data becomes valid, but MUX ADDRESS CODE is now CH5.

TRIGGERED SEQUENTIAL ADDRESS

Set pin 19 (LOAD) and pin 20 (CLEAR) to logic 1 or leave open. Apply a falling edge trigger pulse to pin 8 (STROBE). This negative transition causes the contents of the address counter to be incremented by one, followed by an A/D conversion in 9 microseconds.

DIFFERENTIAL OR SINGLE-ENDED INPUTS

The location of the analog signals being digitized dictates whether to use single-ended or differential inputs. Problems arise when the ground of the internal A/D converter is at a potential difference far from the ground of the analog signal. This results in a common mode voltage.

Table 5. Mux Channel Addressing

← MUX ADDRESS → PIN 9 RA8	PIN 10 RA4	PIN 11 RA2	PIN 12 RA1	PIN 5 MUX ENAB.	ON CHANNEL	
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	HDAS-8 (3-BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	HDAS-16 (4-BIT ADDRESS)
1	1	1	1	1	15	

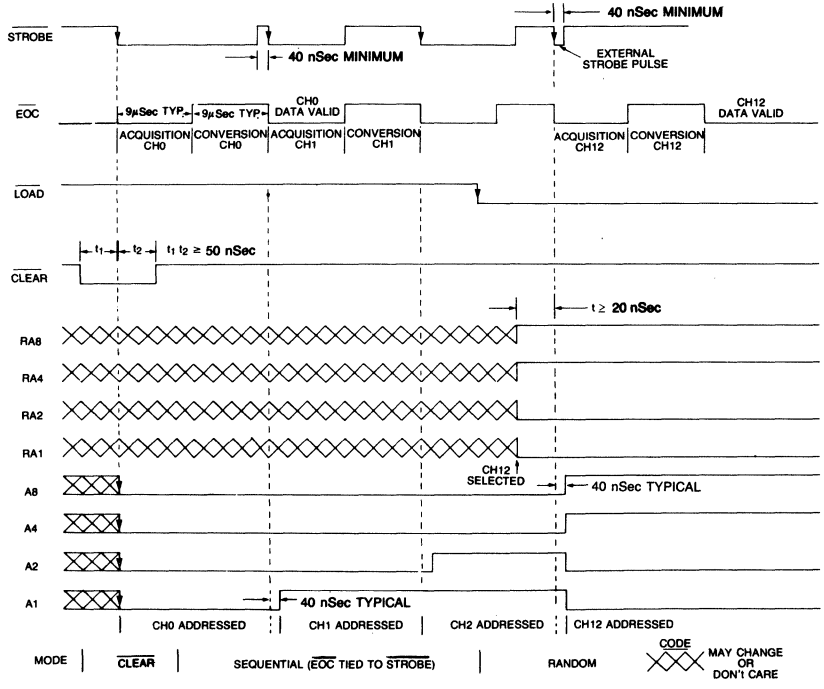


Figure 2. HDAS Timing Diagram

This common mode voltage occurs often when analog signals are taken from different locations away from the A/D converter. If signal sources are monitored from various locations, a differential type input is needed.

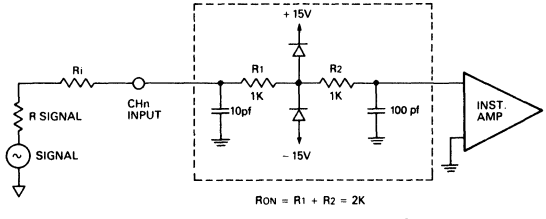


Figure 3. Multiplexer Equivalent Circuit

Location of signal sources close to the HDAS devices (essentially on the same chassis) eliminates the common mode voltage. A single-ended hook-up can then be used, reducing the cost per channel.

The single-ended mode can still be used, even when the signal sources are far from the HDAS, if all the signal sources are returned to the same point. In effect, the analog signals are remote from the HDAS, but in one location. The instrumentation amplifiers' LO (pin 50) input would then be tied to this common return point of the signal sources.

ANALOG SIGNAL COMMON, POWER COMMON, and DIGITAL COMMON are connected internally. Avoid ground-related problems by connecting the commons to one point . . . the ground plane beneath the converter when the above special grounding considerations do not apply.

INPUT VOLTAGE PROTECTION

As shown in Figure 3, the multiplexer has reversed biased diodes which protect the input channels from being damaged by overvoltage signals. The HDAS input channels are protected up to 20V beyond the supplies and can be increased by adding series resistors (Ri) to each channel. The input resistor must limit the current flowing through the protection diodes to 10 mA.

The value of Ri for a specific voltage protection range (Vp) can be calculated by the following formula:

$$Vp = (R\ signal + Ri + Ron)\ (10\ mA)$$

where $R_{ON} = 2K$

NOTE: Increased input series resistance will increase multiplexer settling time significantly.

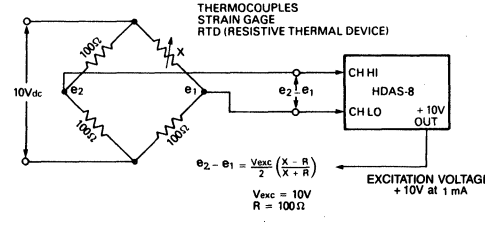


Figure 4. Low-Level Inputs

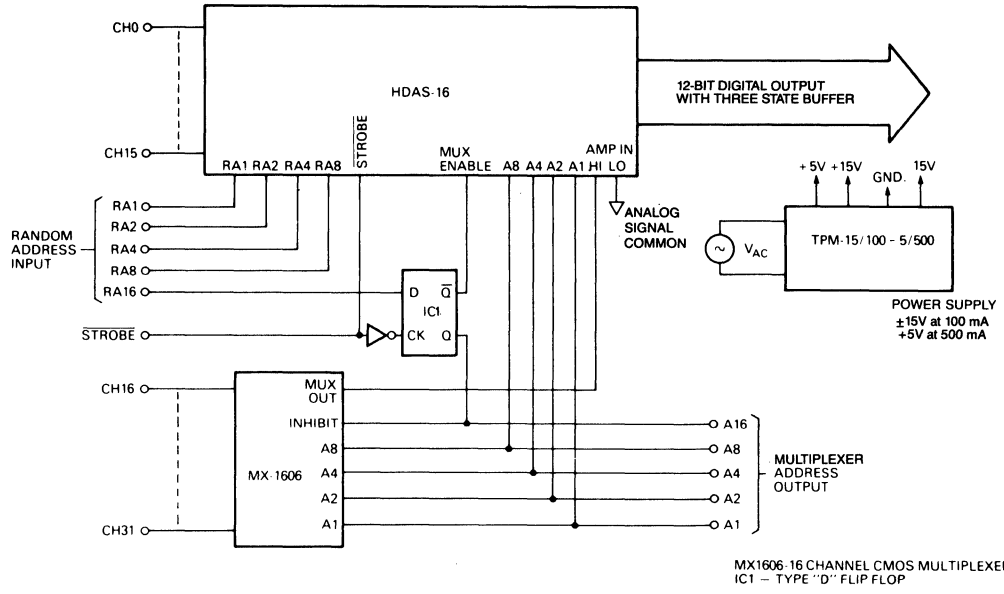


Figure 5. 32-Channel, Single-Ended Data Acquistion System

Remote monitoring of low level signals can be difficult, especially when analog signals pass through an environment with high levels of electrical noise. One solution is to use an instrumentation amplifier to extract the common mode voltage and amplify the voltage difference. The HDAS-8, an eight channel differential input system, can reject common-mode noise and allow amplification up to a gain of 200. Direct connections to thermocouples, transducers, strain gages and RTD can be made through shielded twisted pairs. A differential RC filter may be used to attenuate normal mode noise.

MULTIPLEXER EXPANSION

Figure 5 shows an interconnection scheme for expanding the multiplexer channel capacity of the HDAS-16 from 16 channels single-ended to 32 channels. Figure 6 shows a similar scheme to expand the HDAS-16 to 16 differential channels.

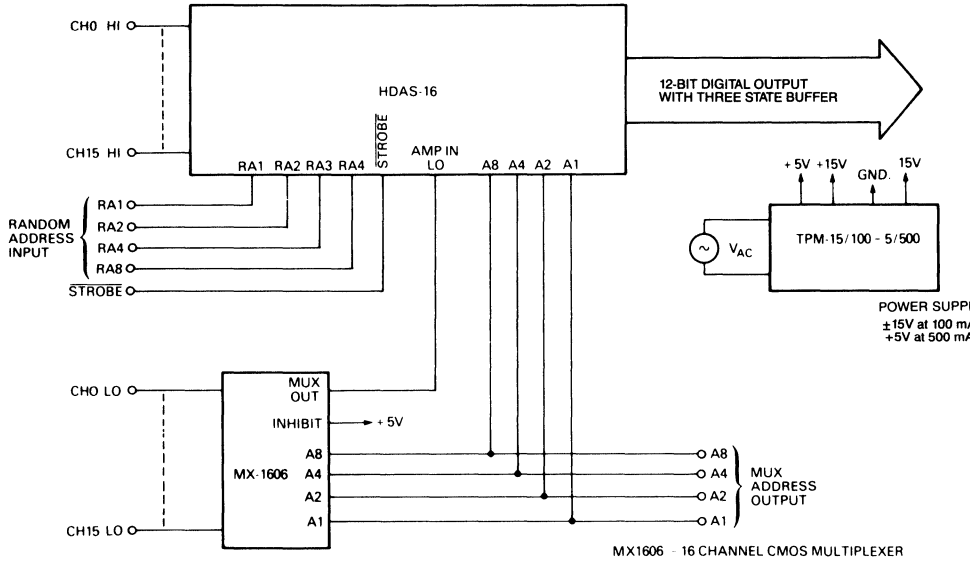


Figure 6. 16-Channel Differential Data Acquistion System

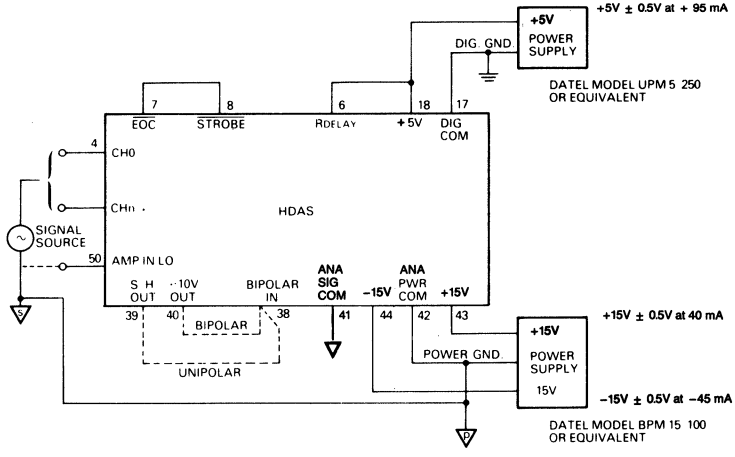


Figure 7. Simple Connection Diagram

NOTES:

1. For HDAS-16, tie pin 50 to a "signal source common" if possible. Otherwise tie pin 50 to pin 41 (ANA SIG COM).
2. BIPOLAR connection yields ±10V range. UNIPOLAR connection yields 0 to +10V range. Other ranges are created by selecting appropriate value for R_{GAIN}
3. DIG COM, ANA PWR COM, and ANA SIG COM are internally connected.

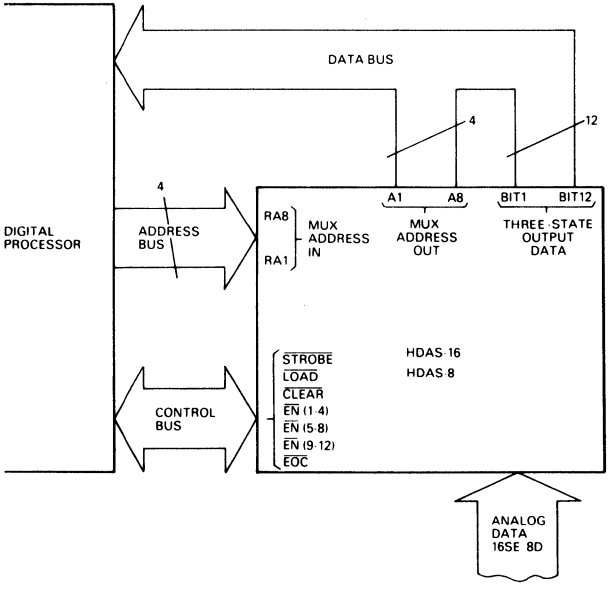


Figure 8. Processor Interface

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
HDAS-16MC	0°C to + 70°C
HDAS-16MM	−55°C to + 125°C
HDAS-16/883B	−55°C to + 125°C
HDAS-8MC	0°C to + 70°C
HDAS-8MM	−55°C to + 125°C
HDAS-8/883B	−55°C to + 125°C

ACCESSORIES

Part Number	Description
58-6322-1	Evaluation Socket
TP20K (20 K ohms)	Trimming Potentiometer

Receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-4 (component lead spring socket) 62 required.

Each includes PC board with offset and gain potentiometers, bifurcated terminals for electrical connections.

/883B Models are fully compliant to MIL-STD-883.

MDAS-16, MDAS-8D Modular Data Acquisition System

FEATURES

- **16 Channels single ended or 8 channels differential**
- **12-Bit resolution**
- **50 kHz Throughput rate**
- **Three-state outputs**
- **Low cost**

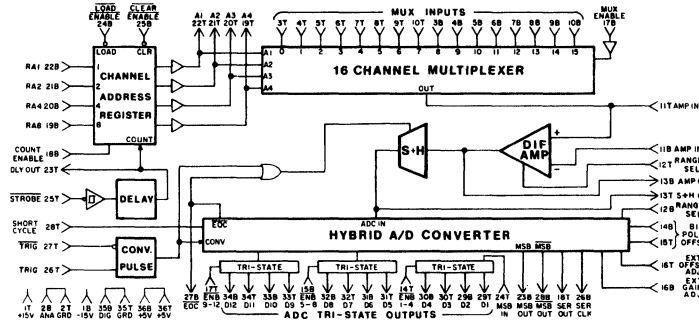
DESCRIPTION

The MDAS-16 and MDAS-8D data acquisition modules are complete, self-contained systems featuring 16-channel single-ended or 8-channel differential operation respectively. Resolution is 12 bits and throughput rate is 50 kHz. Output data is buffered three-state for interfacing to mini- or microcomputer data buses. Output data can be transferred in three 4-bit bytes. Output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation.

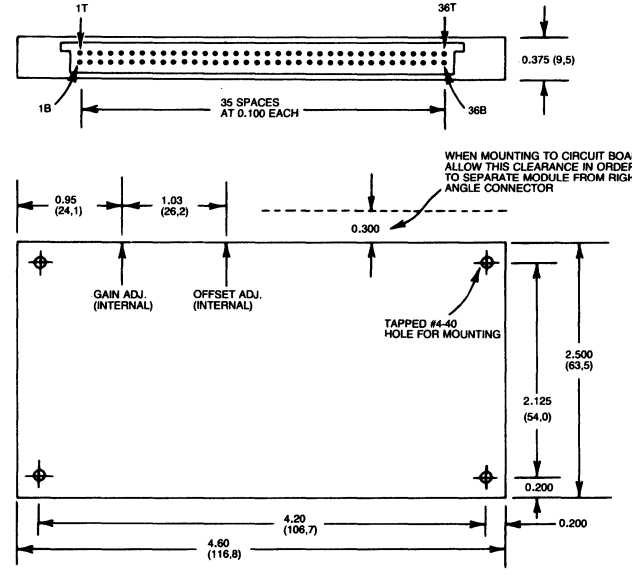
The 4.6 x 2.5 x 0.375 inch size of these modules is ½ inch narrower than other competitive models. The small size and low cost are made possible by extensive use of hybrid and monolithic circuits to reduce parts count and increase reliability. Both models use DATEL's ADC-HZ12BGC 12-bit hybrid A/D converter along with a monolithic sample-hold and analog multiplexer.

The MDAS-16 and MDAS-8D feature a high degree of user flexibility with pin-programmable input ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V dc. The systems may be operated in either random or sequential channel addressing modes. For applications where lower than 12-bit resolution can be used, the A/D converter can be short-cycled to achieve a faster conversion rate. Output data is also available in serial form with a gated clock output.

The modules are housed in a shielded steel case. Input-output connections are made using a 72-pin connector.



MECHANICAL DIMENSIONS INCHES (MM)



7

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise indicated.

ANALOG INPUTS

Number of Channels ..... 16 Single Ended (MDAS-16)
8 Differential (MDAS-8D)
Input Voltage Ranges
unipolar ..... 0 to +5V 0 to +10V
bipolar ..... ±2.5V, ±5V, ±10V
Common Mode Range, min. ..... ±10V
Max. Input Voltage,
no damage ..... ±15V
Input Impedance ..... 100 megohms
Input Bias Current ..... 3 nA, 10 nA max. 0 to 70°C
Input Capacitance
OFF channel ..... 10 pF
ON channel ..... 100 pF

ACCURACY

Resolution ..... 12 Bits
Error, max. 50 kHz sampling ..... ±0.025% of FSR
Nonlinearity, max. ..... ±1 LSB
Diff. Nonlinearity, max. ..... ±1 LSB
Gain Error ..... Adj. to zero
Offset Error ..... Adj. to zero
Temp. Coeff. of Gain, max. ..... ±30 ppm/°C
Temp. Coeff. of Offset, max. ..... ±7 ppm/°C of FS
Diff. Linearity Tempco, max. ..... ±3 ppm/°C of FS
Common Mode Rejec., min. ..... 70 dB at 1 kHz
Monotonicity ..... 0°C to 70°C
Power Supply Rejection ..... 0.01%/% Supply

DYNAMIC CHARACTERISTICS

Throughput Rate, max. ..... 50 kHz
Acquisition Time ..... 6 μsec.
Conversion Time ..... 14 μsec.
Aperture Time, max. ..... 100 nsec.
Sample-Hold Droop, max. ..... 200 μV/msec.
Feedthrough, max. 0.01%
Channel Crosstalk (Mux.) ..... −80 dB at 1 kHz

DIGITAL OUTPUTS

Parallel Data Out ..... 12 parallel lines of buffered three-state output data. Drives 12 TTL loads.
Coding ..... Straight binary, offset binary, and two's complement.
Serial Out ..... Output data in MSB first, NRZ format. Straight binary and offset binary coding. Drives 5 TTL loads.
Mux Address Out ..... Buffered output of address register. Drives 20 TTL loads.
Delay Out ..... Drives 5 TTL loads.
Clock Out ..... Drives 5 TTL loads.
$\overline{\text{EOC}}$ (Status) ..... Drives 4 TTL loads.
$\overline{\text{MSB}}$ Out ..... Drives 5 TTL loads.
MSB Out ..... Drives 5 TTL loads.

DIGITAL INPUTS

$\overline{\text{Enable}}$ ..... Three separate inputs which enable three-state outputs in 4 bit bytes. 1 TTL load
Mux Address In ..... 3 bit (MDAS-8D) or 4 bit (MDAS-16) binary address 1 LS TTL load
$\overline{\text{Strobe}}$ ..... 1 LS TTL load with 10K pull-up resistor
A/D Trigger ..... 1 LS TTL load with 10K pull-up resistor
$\overline{\text{A/D Trigger}}$ ..... 1 LS TTL load
Mux Enable ..... 1 TTL load with 10K pull-up resistor
Count Enable ..... 1 LS TTL load with 10K pull-up resistor
$\overline{\text{Load Enable}}$ ..... 1 LS TTL load with 10K pull-up resistor
$\overline{\text{Clear Enable}}$ ..... 1 LS TTL load with 10K pull-up resistor
MSB In ..... 1 TTL load
Short Cycle ..... 1 TTL load with 10K pull-up resistor

POWER REQUIREMENTS

Power Supply Voltage ..... +15V dc ±0.5V at 65 mA
−15V dc ±0.5V at 60 mA
+5V dc ±0.25V at 200 mA

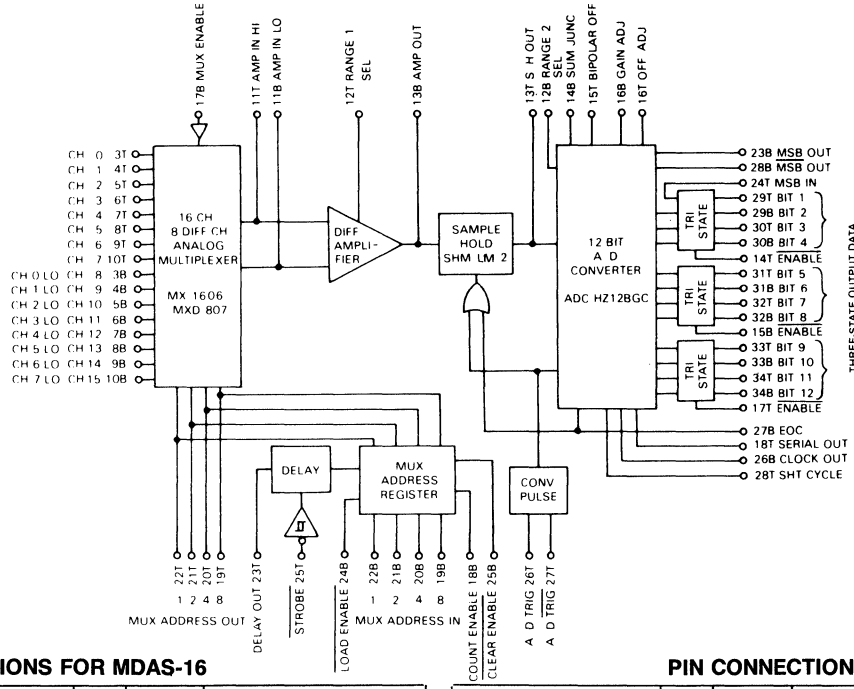
PHYSICAL/ENVIRONMENTAL

Operating Temp. Range ..... 0°C to +70°C
Storage Temperature Range ..... −25°C to +85°C
Package Size ..... 4.6 x 2.5 x 0.375 inches (116,8 x 63,5 x 9,5 mm)
Package Type ..... Steel, shielded on 5 sides
Weight ..... 6 ounces (170 grams)

FOOTNOTES:

1. All outputs are Vout ("0") ≤ +0.4V, Vout ("1") ≥ +2.4V
2. All inputs are Vin ("0") ≤ +0.8V, Vin ("1") ≥ +2.0V

BLOCK DIAGRAM MDAS-16, MDAS-8D



PIN CONNECTIONS FOR MDAS-16

	Top	Bottom	
+15V dc	1T	1B	−15V dc
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 In	3T	3B	Ch. 8 In
Ch. 1 In	4T	4B	Ch. 9 In
Ch. 2 In	5T	5B	Ch. 10 In
Ch. 3 In	6T	6B	Ch. 11 In
Ch. 4 In	7T	7B	Ch. 12 In
Ch. 5 In	8T	8B	Ch. 13 In
Ch. 6 In	9T	9B	Ch. 14 In
Ch. 7 In	10T	10B	Ch. 15 In
Amplifier in high	11T	11B	Amplifier in low
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1–4 Out)	14T	14B	Sum. Junc. (Bipolar Off.)
Bipolar Offset	15T	15B	Enable (Bits 5–8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9–12)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out / 4 Out / 2 Out / 1 Out — Mux Address Lines	19T	19B	8 In / 4 In / 2 In / 1 In — Mux Address Lines
	20T	20B	
	21T	21B	
	22T	22B	
Delay Out	23T	23B	MSB Out (TTL)
MSB in (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5V dc	36T	36B	+5V dc

*Three-State Outputs

PIN CONNECTIONS FOR MDAS-8D

	Top	Bottom	
+15V dc	1T	1B	−15V dc
Analog Gnd.	2T	2B	Analog Gnd.
Ch. 0 high In	3T	3B	Ch. 0 low In
Ch. 1 high In	4T	4B	Ch. 1 low In
Ch. 2 high In	5T	5B	Ch. 2 low In
Ch. 3 high In	6T	6B	Ch. 3 low In
Ch. 4 high In	7T	7B	Ch. 4 low In
Ch. 5 high In	8T	8B	Ch. 5 low In
Ch. 6 high In	9T	9B	Ch. 6 low In
Ch. 7 high In	10T	10B	Ch. 7 low In
Amplifier in high	11T	11B	Amplifier In low
Range 1 Select	12T	12B	Range 2 Select
Sample Hold Out	13T	13B	Amplifier Out
Enable (Bits 1–4 Out)	14T	14B	Sum. Junc. (Bipolar Off.)
Bipolar Offset	15T	15B	Enable (Bits 5–8 Out)
Ext. Offset Adjust	16T	16B	Ext. Gain Adjust
Enable (Bits 9–12 Out)	17T	17B	Mux Enable
Serial Out	18T	18B	Count Enable
8 Out / 4 Out / 2 Out / 1 Out — Mux Address Lines	19T	19B	8 In / 4 In / 2 In / 1 In — Mux Address Lines
	20T	20B	
	21T	21B	
	22T	22B	
Delay Out	23T	23B	MSB Out (TTL)
MSB In (TTL)	24T	24B	Load Enable
Strobe	25T	25B	Clear Enable
A/D Trigger	26T	26B	Clock Out
A/D Trigger	27T	27B	EOC (status)
Short Cycle	28T	28B	MSB Out (TTL)
Bit 1 Out* (MSB)	29T	29B	Bit 2 Out*
Bit 3 Out*	30T	30B	Bit 4 Out*
Bit 5 Out*	31T	31B	Bit 6 Out*
Bit 7 Out*	32T	32B	Bit 8 Out*
Bit 9 Out*	33T	33B	Bit 10 Out*
Bit 11 Out*	34T	34B	Bit 12 Out* (LSB)
Digital Gnd.	35T	35B	Digital Gnd.
+5V dc	36T	36B	+5V dc

*Three-State Outputs

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TABLE 1 DESCRIPTION OF CONTROL PIN FUNCTIONS

FUNCTION	PIN	DESCRIPTION
Amplifier In Low	11B	Analog monitoring point for MDAS-8D. For the MDAS-16 this pin must be grounded.
Amplifier In High	11T	Analog monitoring point.
Range 2 Select Range 1 Select	12B 12T	These pins program analog input voltage range. See Table 2.
Amplifier Out	13B	Analog monitoring point.
Sample Hold Out	13T	Analog monitoring point.
Summing Junction	14B	Used to program analog input voltage range and bipolar offset. See Table 2.
$\overline{\text{Enable}}$	14T	Input low enables tri-state outputs for bits 1-4. Input high inhibits outputs.
$\overline{\text{Enable}}$	15B	Input low enables tri-state outputs for bits 5-8. Input high inhibits outputs.
Bipolar Offset	15T	Connects to 14B for bipolar operation and to analog ground for unipolar operation. See Table 2.
Ext. Gain Adjust	16B	Used to adjust out gain error. Operates independently of the internal adjustment. See External Adjustments diagram.
Ext. Offset Adjust	16T	Used to adjust out offset error. Operates independently of the internal adjustment. See External Adjustments diagram.
Mux Enable	17B	Input high enables multiplexer. Input low inhibits analog multiplexer.
$\overline{\text{Enable}}$	17T	Input low enables three-state outputs for bits 9-12. Input high inhibits outputs.
Count Enable	18B	Input high enables Mux Address Register. Input low inhibits Mux Address Register.
Mux Address In	19B, 20B, 21B, 22B	Digital inputs for channel address selection in random addressing mode. Straight binary coding. See Table 3.
Mux Address Out	19T, 20T, 21T, 22T	Straight binary coded output of Mux Address Register.
MSB Out	23B	Bit 1 TTL output A/D converter. Connect to pin 24T for straight binary or offset binary output coding.
Delay Output	23T	An output delay pulse for 6 microseconds to allow for multiplexer and amplifier settling time and sample hold acquisition time. This pin is normally connected to A/D $\overline{\text{Trigger}}$ (pin 27T) to initiate A/D conversion.
$\overline{\text{Load Enable}}$	24B	Input high for sequential addressing. Input low for random addressing.
MSB In	24T	Bit 1 input to three-state output buffers. Connect to either pin 23B (MSB Out) or pin 28B ($\overline{\text{MSB}}$ Out).
$\overline{\text{Clear Enable}}$	25B	Input low and a negative transition on pin 25T resets Mux address counter to zero.
$\overline{\text{Strobe}}$	25T	Negative input transition initiates channel scanning sequence in sequential mode or a conversion in the random mode. A Schmidt trigger input adds hysteresis for good noise rejection.
Clock Output	26B	A/D converter clock pulses for synchronization of serial data. Negative going pulses of approximately 100 nseconds duration.
A/D Trigger	26T	A positive logic transition on this input initiates A/D conversion.
$\overline{\text{EOC}}$ (status)	27B	End of conversion (status) output. Output high during conversion and low when conversion is complete.
A/D $\overline{\text{Trigger}}$	27T	A negative logic transition on this input initiates A/D conversion. This pin is normally connected to pin 23T (Delay Output).
$\overline{\text{MSB}}$ Out	28B	Complemented bit 1 TTL output of A/D converter. Connect to pin 24T for two's complement output coding.
Short Cycle	28T	For 12-bit resolution connect this pin to ground. To short cycle A/D converter for lower resolution, connect this pin to output bit n + 1 for a resolution of n bits. Short cycling of the A/D converter can only be done with the $\overline{\text{Enable}}$ inputs (pins 14T, 15B and 17T) low.

CONNECTION DIAGRAMS AND TABLES

TABLE 2 INPUT RANGE SELECTION

INPUT RANGE	CONNECT THESE PINS TOGETHER		
	RANGE 1 PIN 12T	RANGE 2 PIN 12B	BIPOLAR OFF. PIN 15T
0 to +5V	13B	13T	2B OR 2T
0 to +10V	2B OR 2T	13T	2B OR 2T
±2.5V	13B	13T	14B
± 5V	2B OR 2T	13T	14B
±10V	2B OR 2T	OPEN	14B

TABLE 4 THROUGHPUT RATES VS. NO. BITS FOR SHORT-CYCLED A/D CONVERTER

NO. BITS	THROUGHPUT RATE
12	50 kHz
10	53 kHz
8	57 kHz
4	67 kHz

TABLE 3 MUX CHANNEL ADDRESSING

← MUX ADDRESS → PIN 19B	20B	21B	22B	17B	ON CHANNEL	
8	4	2	1	MUX ENAB.		
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	MDAS-8D (3 BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	MDAS-16 (4 BIT ADDRESS)
1	1	1	1	1	15	

TABLE 5 CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 to +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 to +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

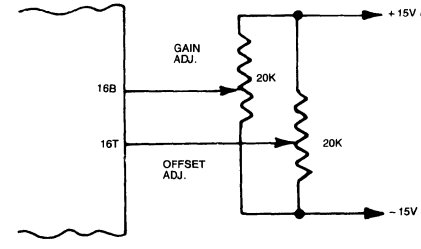


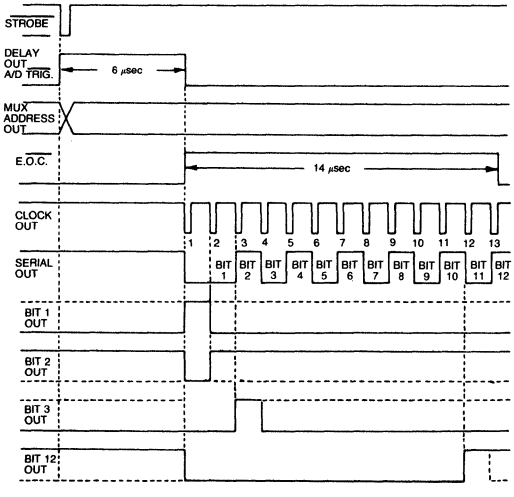
FIG 1 EXTERNAL ADJUSTMENTS

SET-UP AND CALIBRATION INSTRUCTIONS

1. Select input voltage range desired and connect pins 12B, 12T, and 15T in accordance with Table 2. If the MDAS-16 is used, ground pin 11B. Ground all analog channel inputs which are not to be used. Leave pin 17B open.
2. Determine resolution to be used. For full 12 bits, ground pin 28T. For lower resolution requirements, connect pin 28T to bit output n + 1 for n bit resolution. For example: for 8-bit resolution, connect pin 28T to pin 33T (Bit 9 Out). To operate the A/D converter in this short cycled mode, the Enable inputs (pins 14T, 15B, and 17T) must be connected to ground, thereby enabling the three-state outputs. For 12-bit resolution the three-state outputs can be either enabled or disabled.
3. Select the output coding desired. For straight binary (unipolar) or offset binary (bipolar) connect pin 23B (MSB Out) to pin 24T (MSB In). For two's complement (bipolar) connect pin 28B (MSB Out) to pin 24T.
4. Select desired multiplexer mode. Connect pin 23T (Delay Out) to pin 27T (A/D Trigger).
   A. **Free Running Sequential Addressing**
   Connect pin 27B (EOC) to pin 25T (Strobe). Leave pins 24B (Load Enable) and 25B (Clear Enable) open. Sequencing is initiated by a positive logic transition applied to pin 26T (A/D Trigger). Pin 26T must remain high during free running sequential addressing. Sequencing is stopped by a low applied to pin 26T.
   B. **Triggered Sequential Addressing**
   Leave pins 24B (Load Enable) and 25B (Clear Enable) open. Apply a falling edge trigger to pin 25T (Strobe). The negative transition of the strobe will cause the contents of the address counter to be incremented by one.
   C. Random Addressing Ground pin 24B (Load Enable). Leave pin 25B (Clear Enable) open. Each negative transition applied to pin 25T (Strobe) will cause the data at pins 19B, 20B, 21B and 22B (Mux Address In) to be loaded into the Address Register. Address inputs must be stable for at least 300 nanoseconds after negative transition of Strobe.
5. Calibration Procedure
   A. Offset and gain adjustments may be made either internally or externally. Self-contained trimming potentiometers are provided for the internal adjustments. For external adjustments, 20K trimming potentiometers must be used with pins 16B and 16T. Connect as shown in Figure 1.
   B. Connect power supplies to the module and a precision voltage source to pin 3T (Channel 0 In). If the MDAS-8D is used, connect pin 3B (Channel 0 low) to analog ground. Ground pin 25B (Clear Enable) and momentarily short pin 25T (Strobe) to ground. Use an oscilloscope to monitor the serial output code at pin 18T. Trigger the A/D converter with 50 kHz positive going pulses applied to pin 26T (A/D Trigger).
   C. Adjust the precision voltage source to the value shown in Table 5 for the unipolar zero adjustment (zero + ½ LSB) or the bipolar offset adjustment (– FS + ½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
   D. Change the output of the precision voltage source to the value shown in Table 5 for the unipolar or bipolar gain adjustment (+ FS – 1½ LSB). Adjust the gain trimming potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

MDAS-16, MDAS-8D TIMING DIAGRAM

OUTPUT CODE 010101010101



ORDERING INFORMATION

MDAS-16
MDAS-8D

Included with each module is a mating right-angle 72 pin connector. (AMP 3-86063-2). Order additional connectors using the following number: 58-2083010.

MDAS-940
12-Bit Programmable Gain Data Acquisition Subsystem

FEATURES

- **16 channels single-ended or 8 channels differential**
- **12-Bit resolution**
- **2-Bit gain programming**
- **33 kHz throughput rate**
- **Resistor-Programmed low level inputs**
- **Three-state bussable outputs**

GENERAL DESCRIPTION

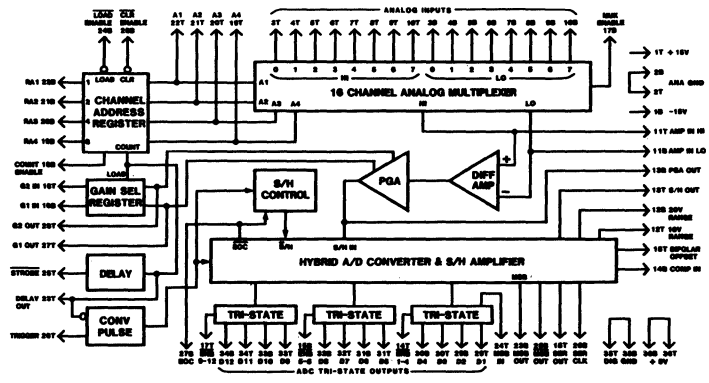
DATEL's MDAS-940S and MDAS-940D are complete, self-contained data acquisition subsystems featuring 16 channel single-ended or 8 channel differential A/D inputs respectively. Resolution is 12 binary bits with accuracy of ±0.025% at a throughput rate of 33 kHz. Both models contain a Programmable Gain Amplifier with digitally selectable gain ranges of 1, 2, 4 and 8. Gain selection is accomplished through the input of a 2-bit word.

Output data is buffered three-state with 3 separate enable lines brought out for easy interfacing to 4-, 8-, or 16-bit data busses. Data is also available in serial form with a gated clock output. Output coding is straight binary for unipolar operation and offset binary or two's complement for bipolar operation.

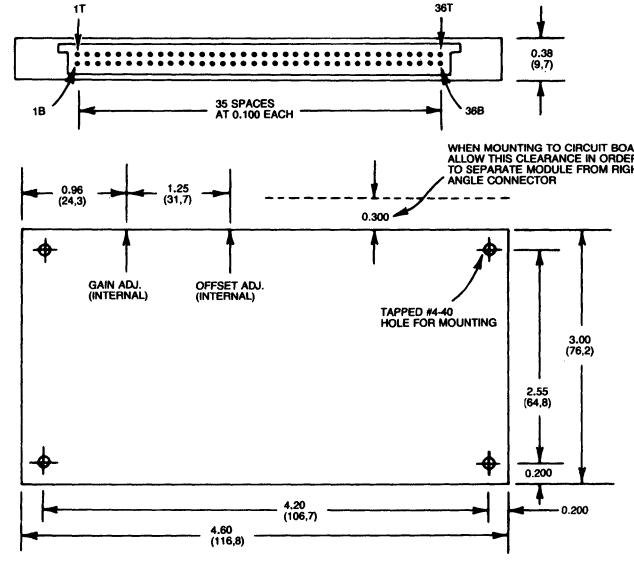
These modules also feature pin-programmable input ranges of 0 to +5V, 0 to +10V, ±5V, and ±10V, which allows for analog measurements with an effective full-scale range of 0.625V when the PGA is selected for a gain of 8. Thus, inputs from strain gages, and other low level signal sensors may be accepted without external signal conditioning. The systems may be operated in either random or sequential channel addressing modes.

The extensive use of hybrid and monolithic circuits reduces the parts count, increases reliability, and makes possible the small size and low cost of these modules. Both models use DATEL's ADC-HS12BGC hybrid A/D converter with internal sample-hold along with a monolithic analog multiplexer.

The modules are housed in a 4.6 x 3.0 x 0.38 inch shielded steel case. Input-output connections are made by means of a 72-pin connector.



MECHANICAL DIMENSIONS
INCHES (MM)



7

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, G = 1, ±10V Input Range, unless otherwise noted.

ANALOG INPUTS

Number of Channels,	
MDAS-940S	16 Single Ended
MDAS-940D	8 Differential
Input Voltage Range,	
unipolar	0 to +5v, 0 to +10V
bipolar	±5V, ±10V
Input Voltage, No Damage, max.	±35V
Common Mode Range, min.	±10V
Input Impedance	100 MΩ
Input Bias Current, max.[1]	8 nA
Input Capacitance,	
OFF Channel to Ground	10 pF
ON Channel to Ground	100 pF

PERFORMANCE

Resolution	12 Binary Bits
Accuracy, G = 1	±0.025% of FSR
Nonlinearity, max.	±½ LSB
Diff. Nonlinearity, max.	±½ LSB
Gain Range	1, 2, 4, 8
Gain Error	Adj. to Zero
Offset Error	Adj. to Zero
Temp. Coeff. of Gain, max.	±30 ppm of FSR[3]/°C
Temp. Coeff. of Offset, max.	±7 ppm of FSR[3]/°C
Diff. Linearity Tempco, max.	±3 ppm of FSR[3]/°C
Common Mode Rejection, min.	70 dB
Monotonicity	0°C to +70°C
Power Supply Rejection	0.01%/%

DYNAMIC CHARACTERISTICS

Throughput Rate, min.	33 kHz
Conversion Time	10 μsec.
Acquisition Time	20 μsec.
Aperture Delay Time	100 nsec.
Output Enable Delay, max.	30 nsec.
Hold Mode Droop, max.	200 nV/μsec.
Feedthrough, max.	0.01%
Channel Crosstalk (Mux.), 1 kHz	−80 dB

DIGITAL OUTPUTS

Parallel Output Data (Pins 29T-34T, 29B-34B)	12 Parallel data lines. Data is arranged as three 4-bit, gateable three-state outputs. Drives 12 TTL loads.
High Level Output Current (IOH)	−15 mA
Low Level Output Current (IOL)	24 mA
Off State Output Current (IOZH), max.	20 μA
Output Logic Level, high ("1"), min.[4]	≥ 2.4V
Output Logic Level, low ("0"), max.[4]	≤ 0.5V
Output Coding	Straight Binary, Offset Binary, and Two's Complement.
Serial Output Data (Pin 18T)	NRZ successive decision pulses out, MSB first. Straight binary and offset binary coding. Drives 15 TTL loads.
Clock Out (Pin 26B)	Train of negative going −5V, 100 nsec. pulses at 1.5 MHz rate. Drives 15 TTL loads.
Delay Output (Pin 25T)	Output Delay pulse set for 20 μsec. Drives 5 TTL loads.
$\overline{\text{EOC}}$ (Status) (Pin 27B)	Conversion status signal. Drives 4 TTL loads.
Mux. Address Out (19T-22T)	Binary-coded output of Mux. Address Register. Drives 4 TTL loads.
Gain Select Out (1 & 2) 27T, 28T	Binary-coded gain stored in Gain Select Register. Drives 5 TTL loads.
MSB Out (Pin 23B)	Bit 1 output of A/D converter. Drives 15 TTL loads.
$\overline{\text{MSB}}$ Out (Pin 28B)	Complemented Bit 1 output of A/D converter. Drives 14 TTL loads.

DIGITAL INPUTS[5]

$\overline{\text{Output}}$ Enable[6] (Pins 14T, 15B, 17T)	Three separate inputs which enable three-state output data in 4 bit bytes. Loading: 1 LS TTL load.
$\overline{\text{Strobe}}$ (Pin 25T)	Increments channel address register and enables gain code update in sequential mode or starts a conversion when in random mode. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
Trigger (Pin 26T)	Positive pulse with 100 nsec. duration min. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
Mux Address In (Pins 19B-22B)	3-bit MDAS-940D or 4-bit (MDAS-940S) binary address input for channel address selection. Loading: 1 LS TTL load.
$\overline{\text{Load Enable}}$ (Pin 24B)	Input high for sequential addressing. Input low for random addressing. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
$\overline{\text{Clear Enable}}$ (Pin 25B)	Input low and a negative transition on $\overline{\text{STROBE}}$ (Pin 25T) resets mux. address register to zero. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
Count Enable (Pin 18B)	Input high enables mux address register sequencing. Input low inhibits Mux Address Register Sequencing. Enable delay is 20 nsec. Loading: 1 LS TTL load with 10 kΩ pull-up resistor.
Mux Enable (Pin 17B)	Input high enables analog multiplexer. Input low disconnects analog multiplexer for external channel expansion.
Gain Select In (Pins 16T, 16B)	2-bit binary address to select gain of internal PGA. Loading: 1 LS TTL load.
MSB In (Pin 24T)	Bit 1 input to three-state output buffers. Loading: 1 TTL load.

POWER REQUIREMENTS

Analog Supply	+ 15V dc ±0.5V at 110 mA regulated − 15V dc ±0.5V at 100 mA regulated
Logic Supply	+ 5V dc ±0.25V at 275 mA regulated

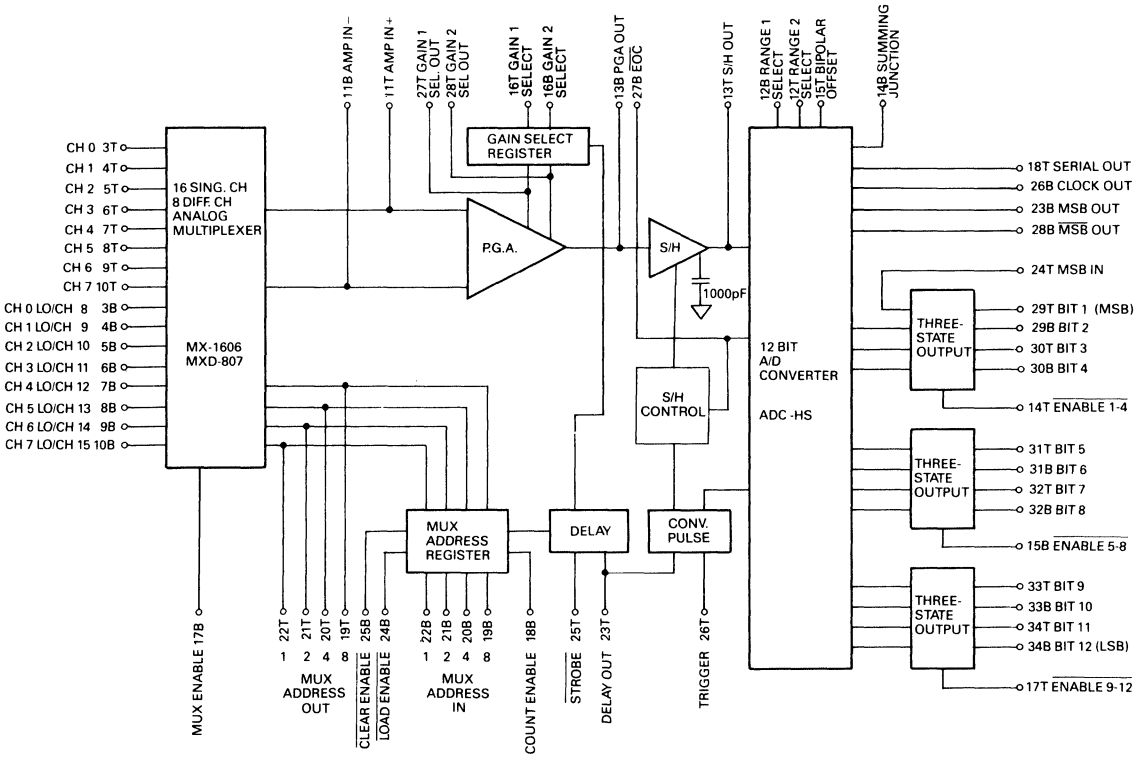
PHYSICAL/ENVIRONMENTAL

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +85°C
Package Size	4.6 x 3.0 x 0.38 inches (116,8 x 76,2 x 9,7 mm)
Package Type	Steel, shielded on 5 sides
Weight	5 ounces

FOOTNOTES:

1. Specification is for full temperature range of 0°C to +70°C.
2. A factory option allows the gain range to be incremented upwards (for example: 10, 20, 40 and 80) for OEM orders. To retain 12 bit linearity, the P.G.A. gain must not exceed 100. For more information contact your nearest DATEL sales office.
3. FSR is Full Scale Range.
4. Logic levels of all other digital outputs are Vout ("1") ≥ +2.4V and Vout ("0") ≤ +0.4V.
5. All digital input logic levels are V_{IN}("1") ≥ +2.0V and V_{IN}("0") ≤ +0.8V.
6. The OUTPUT ENABLE specification refers to three inputs; ENABLE 1-4 (Pin 14T), ENABLE 5-8 (Pin 15B), and ENABLE 9-12 (Pin 17T).

BLOCK DIAGRAM MDAS-940



PIN CONNECTIONS FOR MDAS-940

Signal	Bottom	Top	Signal
–15V dc	1B	1T	+15V dc
Analog Gnd.	2B	2T	Analog Gnd.
Ch. 8 In/Ch. 0 Low In	3B	3T	Ch. 0 In/Ch. 0 High In
Ch. 9 In/Ch. 1 Low In	4B	4T	Ch. 1 In/Ch. 1 High In
Ch. 10 In/Ch. 2 Low In	5B	5T	Ch. 2 In/Ch. 2 High In
Ch. 11 In/Ch. 3 Low In	6B	6T	Ch. 3 In/Ch. 3 High In
Ch. 12 In/Ch. 4 Low In	7B	7T	Ch. 4 In/Ch. 4 High In
Ch. 13 In/Ch. 5 Low In	8B	8T	Ch. 5 In/Ch. 5 High In
Ch. 14 In/Ch. 6 Low In	9B	9T	Ch. 6 In/Ch. 6 High In
Ch. 15 In/Ch. 7 Low In	10B	10T	Ch. 7 In/Ch. 7 High In
Amplifier In	11B	11T	Amplifier In +
Range 1 Select	12B	12T	Range 2 Select
P.G.A. Out	13B	13T	Sample Hold Out
Sum. Junc.	14B	14T	$\overline{\text{Enable}}$ (Bits 1-4 Out)
$\overline{\text{Enable}}$ (Bits 5-8 Out)	15B	15T	Bipolar Offset
Gain 2 Select In	16B	16T	Gain 1 Select In
Mux Enable	17B	17T	$\overline{\text{Enable}}$ (Bits 9-12)
Count Enable	18B	18T	Serial Out
8 In / 4 In / 2 In / 1 In — Mux Address Lines	19B	19T	8 Out / 4 Out / 2 Out / 1 Out — Mux Address Lines
	20B	20T	
	21B	21T	
	22B	22T	
$\overline{\text{MSB OUT}}$ (TTL)	23B	23T	Delay Out
$\overline{\text{Load Enable}}$	24B	24T	$\overline{\text{MSB}}$ In (TTL)
$\overline{\text{Clear Enable}}$	25B	25T	$\overline{\text{Strobe}}$
Clock Out	26B	26T	Trigger
$\overline{\text{EOC}}$ (status)	27B	27T	Gain 1 Select Out
$\overline{\text{MSB}}$ Out (TTL)	28B	28T	Gain 2 Select Out
Bit 2 Out*	29B	29T	Bit 1 Out* (MSB)
Bit 4 Out*	30B	30T	Bit 3 Out*
Bit 6 Out*	31B	31T	Bit 5 Out*
Bit 8 Out*	32B	32T	Bit 7 Out*
Bit 10 Out*	33B	33T	Bit 9 Out*
Bit 12 Out*	34B	34T	Bit 11 Out*
Digital Gnd.	35B	35T	Digital Gnd.
+5V dc	36B	36T	+5V dc

*Three-State Outputs

PIN DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1T	+15V dc	Positive analog supply voltage. +15V dc at 65 mA typical.
1B	–15V dc	Negative analog supply voltage. –15V dc at 60 mA typical.
2T/2B	Analog Gnd.	Analog common. Analog common and digital common (Pins 35T/35B) are connected within the module and should not be connected externally.
3T/3B through 10T/10B	Channel In	Analog inputs to multiplexer. MDAS-940S has 16 single-ended inputs. The MDAS-940D has 8 differential inputs.
11T	Amplifier In +	Analog monitoring point for the positive input of the internal Programmable Gain Amplifier.
11B	Amplifier In –	Analog monitoring point for the negative input of the internal Programmable Gain Amplifier. For normal operation on the MDAS-940S this pin must be grounded.
12T	Range 1 Select	A/D converter input resistor. Should be grounded when not being used. See Input Range Selection Chart.
12B	Range 2 Select	A/D converter input resistor. Should be grounded when not being used. See Input Range Selection Chart.
13T	Sample-Hold Output	Sample-Hold output. Connect to desired range select pin for normal operation. See Input Range Selection Chart.

7

PIN	MNEMONIC	DESCRIPTION
13B	P.G.A. Out	Analog monitoring point for the output of the internal Programmable Gain Amplifier.
14T	Enable 1-4	Enable line for three-state output, bits 1-4. Input low enables output, input high inhibits output. Max. enable delay is 30 nsec.
14B	Summing Junction	Comparator input for A/D converter, used in range selection. See Input Range Selection Chart. Make no other external connections to prevent performance degradation.
15T	Bipolar Offset	A/D Converter Bipolar Offset. Connnect to Summing Junction (Pin 14B) for bipolar operation, or to analog common (Pins 2T/2B) for unipolar operation. See Input Range Selection Chart.
15B	Enable 5-8	Enable Line for three-state outputs, bits 5-8. Input low enables output, input high inhibits output. Max. enable delay is 30 nsec.
16T/16B	Gain Select IN 1 & 2	Address lines that select gain 8 of Internal Programmable Gain Amplifier. Gains of 1, 2, 4, or 8 may be selected. See Gain Selection Chart.
17T	Enable 9-12	Enable line for three-state outputs, bits 9-12. Input low enables output, input high inhibits output. Max. enable delay is 30 nsec.
17B	Mux. Enable	Enable line for analog multiplexer. Input high enables multiplexer, Input low disconnects multiplexer for external channel expansion.
18T	Serial Out	Serial Output data in NRZ format, MSB first. Data is synchronous with Clock Out (Pin 26B), use negative edge of clock to strobe each bit.
18B	Count Enable	Enable line for Mux. Address Register Sequencing. Input high enables register sequencing, Input low inhibits register sequencing. Enable delay is 20 nsec.
19T through 22T	Mux. Address Out	Binary coded output of Mux. Address Register. Should be buffered externally if long etch runs or cables are to be driven.
19B through 22B	Mux. Address In	Address lines that select one out of 16 (8-MDAS-940D) input channels when operating in the random addressing mode. Straight binary coding.
23T	Delay Out	20 μsec. pulse used to delay start of A/D conversion to allow settling of the multiplexer, amplifier, and sample-hold. Negative going edge initiates A/D conversion.
23B	MSB Out	Bit 1 output of A/D converter. Connected to MSB In (Pin 24T) for straight binary or offset binary coding.
24T	MSB In	Bit 1 input to three-state output buffer. Connect to MSB Out (Pin 23B) for straight or offset binary coding. Connect to MSB Out (Pin 28B) for Two's Complement coding.
24B	Load Enable	Input high for sequential addressing. Input low for random addressing. Loads address code for random addressing on high to low transition of STROBE.
25T	Strobe	Negative input transition initiates channel sequencing and gain selection in sequential mode, A/D conversion when in random mode.
25B	Clear Enable	Input low in conjunction with a negative transition on Strobe (Pin 25T) will reset the mux address register to zero.
26T	Trigger	Logic low to high transition resets A/D converter and initiates next conversion.
26B	Clock Out	A/D converter clock output. Used as shift clock for serial output data.
27T	Gain 1 Select Out	Output 1 of Gain Select Register.
27B	EOC	Conversion status signal. Output high during conversion, low when conversion is complete.
28T	Gain 2 Select OUT	Output 2 of Gain Select Register.
28B	MSB out	Complimented Bit-1 output of A/D converter. Connected to MSB in (Pin 24T) for two's complement coding.
29T/29B through 34T/34B	Data Outputs	Three-state digital outputs.
35T/35B	Digital Ground	Digital common. Digital Common and Analog Common (Pins 2T/2B) are connected within the module and should not be connected externally.
36T/36B	Logic Supply	+5V dc at 200 mA typical.

CONNECTION AND CALIBRATION

1. Select input voltage range desired and connect pins 12B, 12T, and 15T in accordance with Table II. If the MDAS- 940S is used, ground pin 11B. Ground all analog channel inputs which are not to be used. Leave pin 17B open.
2. Select the output coding desired. For straight binary (unipolar) or offset binary (bipolar) connect pin 23B (MSB Out) to pin 24T (MSB In). For two's complement (bipolar), connect pin 28B (MSB Out) to pin 24T.
3. Select desired multiplexer mode.
   A. Free Running Sequential Addressing
   Connect pin 27B (EOC) to pin 25T (Strobe). Leave pins 24B (Load Enable) and 25B (Clear Enable) open. Sequencing is initiated by a positive logic transition applied to pin 26T (Trigger). Pin 26T must remain high during free running sequential addressing. Sequencing is stopped by a low applied to pin 26T.

   B. Triggered Sequential Addressing
   Leave pins 24B (Load Enable) and 25B (Clear Enable) open. Apply a falling edge trigger to pin 25T (Strobe). The negative transition of the strobe will cause the contents of the address counter to be incremented by one.
4. CALIBRATION
   A. Connect power supplies to module and ground all analog channel inputs. Monitor PGA Out pin (Pin 13B) and adjust P.G.A. Null adjustment for 0.0000V.
   B. Connect a precision voltage source to pin 3T (Chan 0 In). If the MDAS-940D is used, connect pin 3B (Chan 0 low) to analog ground. Ground pin 25B (Clear Enable) and momentarily short pin 25T (Strobe) to ground. Use an oscilloscope to monitor the serial output code at pin 18T. Trigger the A/D converter with 50 kHz positive going pulses applied to pin 26T (Trigger).

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C. Adjust the precision voltage source to the value shown in the Calibration Table for the unipolar zero adjustment (zero + ½ LSB) or the bipolar offset adjustment (−FS +½ LSB). Adjust the offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

D. Change the output of the precision voltage source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+ FS −1½ LSB). Adjust the gain trimming potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO GAIN	+0.6 mV +4.9982V
0 TO +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

GAIN SELECTION CHART

GAIN SELECT	GAIN SELECT	PGA GAIN[1]
0	0	1
0	1	2
1	0	4
1	1	8

[1]A factory option allows the gain range to be incremented upwards (for example: 10, 20, 40 and 80) for OEM orders. To retain 12-bit linearity, the P.G.A. gain must not exceed 100. For more information contact your nearest DATEL sales office.

MUX CHANNEL ADDRESSING

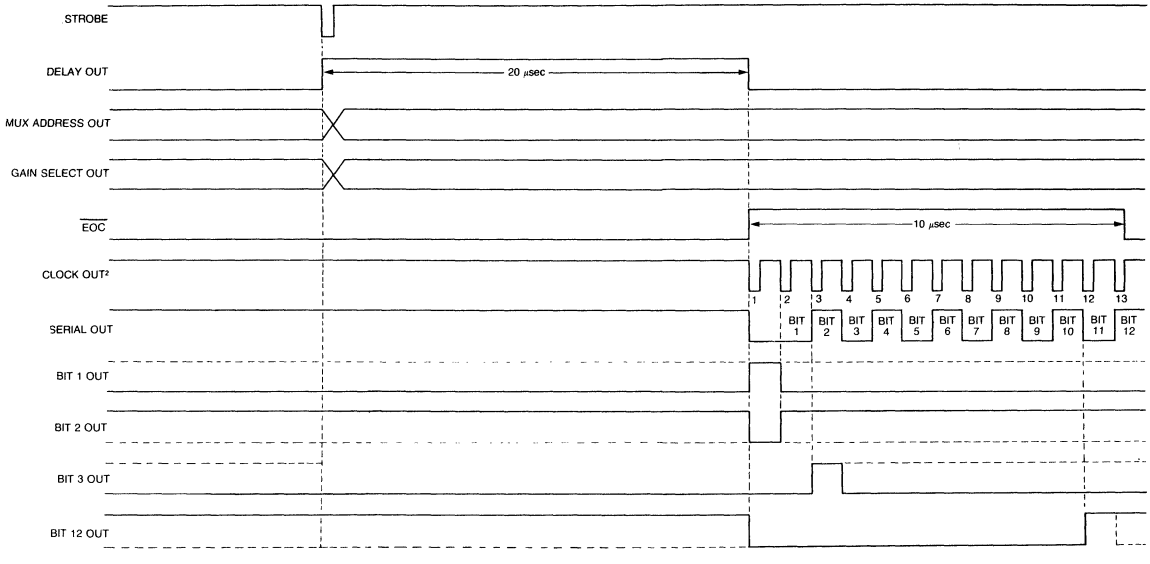
MUX ADDRESS PIN 19B	20B	21B	22B	17B	ON CHANNEL	
8	4	2	1	MUX ENAB.	MDAS 940S	MDAS 940D
X	X	X	X	0	—	—
0	0	0	0	1	1	1
0	0	0	1	1	2	2
0	0	1	0	1	3	3
0	0	1	1	1	4	4
0	1	0	0	1	5	5
0	1	0	1	1	6	6
0	1	1	0	1	7	7
0	1	1	1	1	8	8
1	0	0	0	1	9	—
1	0	0	1	1	10	—
1	0	1	0	1	11	—
1	0	1	1	1	12	—
1	1	0	0	1	13	—
1	1	0	1	1	14	—
1	1	1	0	1	15	—
1	1	1	1	1	16	—

Data must be present for 70 nsec. min. after the high to low transition of STROBE.

INPUT RANGE SELECTION

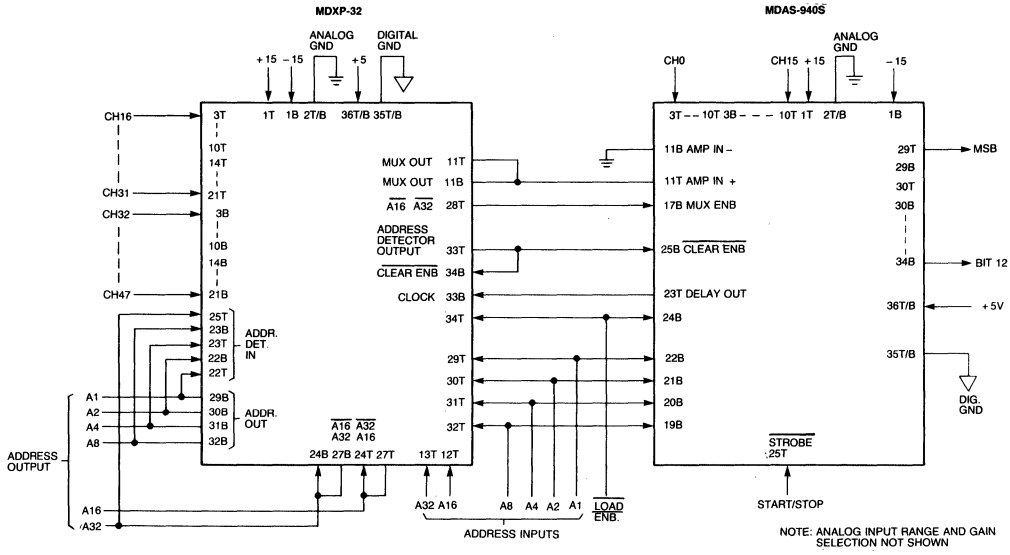
INPUT RANGE	CONNECT THESE PINS TOGETHER RANGE 2 PIN 12T	RANGE 1 PIN 12B	BIPOLAR OFF. PIN 15T
0 TO +5V	13T	14B	2T or 2B
0 TO +10V	13T	—	2T or 2B
±5V	13T	—	14B
±10V	—	13T	14B

TIMING DIAGRAM OUTPUT CODE: 010101010101



1. Negative going edge of Delay pulse initiates conversion if Trigger (Pin-26T) is open or high. Allows for multiplexer and amplifier settling time and sample-hold acquisition time.
2. Train of negative going −5V, 100 nsec. pulses at 1.5 MHz rate.

CHANNEL EXPANSION WITH MDXP-32 AND MDXP-32-1
SINGLE LEVEL MULTIPLEXING FOR 48 SINGLE-ENDED CHANNELS



DATEL's MDX-P-32 and MDXP-32-1 are input channel expansion modules that are compatible with MDAS-940. Both models contain 32 analog multiplex channels which permit expanding the MDAS-940S up to 48 single-ended channels and the MDAS-940D up to 24 differential channels. With double level multiplexing, up to 256 single-ended channels or 128 differential channels can be achieved using 1 MDXP-32 and 7 MDXP-32-1's. Both modules are contained in a 4.6 x 2.5 x 0.375 in. shielded steel case and operate over the 0°C to +70°C temperature range.

ORDERING INFORMATION

MODEL	INPUT CHANNEL SELECTION
MDAS-940D	8 Chan. Differential
MDAS-940S	16 Chan. Single Ended

Included with each module is a mating right-angle 72-pin connector. (AMP 3-86063-2). Use the following number to order additional connectors: 58-2083010.

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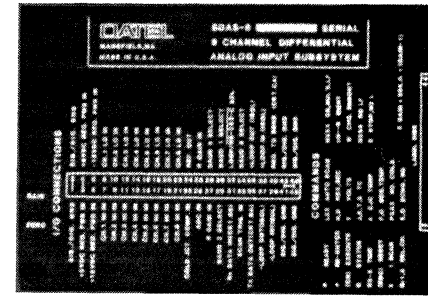
SDAS-8 Analog Input 8 Channel Differential Serial Microsystem

SDAS-8 FEATURES

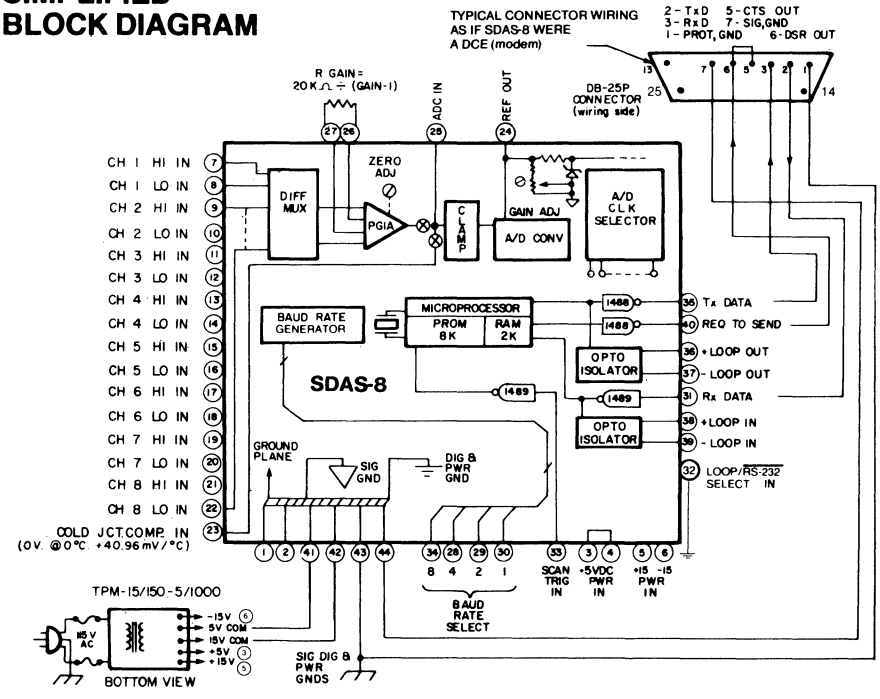
- 8 Differential Analog Input Channels, ±4.095Vdc full scale.
- Serial RS-232-C full duplex data link, 75-9600 baud.
- Simple ASCII commands.
- Direct thermocouple input (J, K, S, T) and linearization.
- Resistor-selected gain ×1 to ×200.
- Includes crystal time-of-day clock (23:59:59).
- Output is command-selected as ASCII hexadecimal or decimal, volts, °F or °C.
- A/D resolution is 12 bit binary and polarity (13 bits)
- Choice of 50 to 60 Hz normal mode AC rejection.
- Also includes optoisolated (2500Vpk) 20mA serial loop I/O
- 3 scan transmit start methods
  1. Local 10 μS TTL trigger input.
  2. Polled by host ASCII command.
  3. Auto-start using internal timer, 1 second to 17:59:59 hours intervals.
- 4″ × 6″ × 0.4″ steel-cased module, for direct PC-board mounting or standoffs.
- Uses regulated +5Vdc @ 500mA, ±15Vdc @ 50mA power.
- Easily interfaces to popular RS-232-C terminals, microcomputers and serial-port personal computers.
- May be positioned many hundreds of feet from host.
- Multidrop up to 4 stations (32 differential channels) using the 20mA serial I/O.
- Extensive editing, formatting and ident. header controls.



APPLICATIONS

- Simple A/D input to any RS-232-C terminal.
- Remote data logging to any host computer.
- Direct data acquisition mode with clock for any printer from local TTL trigger scan transmit.
- Diagnostic instruments, analytical systems, multichannel computer-controlled test equipment.

SIMPLIFIED BLOCK DIAGRAM



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INTRODUCTION

Designed to simplify the connection of analog input signals to digital computers, the SDAS-8 is an 8-channel differential input A/D smart microsystem combined with a full-serial, full duplex terminal I/O port operated by an internal microprocessor. The serial port accepts input commands from the user's host computer or terminal and transmits ASCII analog data and status from dc or slowly varying transducer signals. The SDAS-8 is housed in a steel-cased modular package measuring only 4" × 6" × 0.4" for printed circuit board or standoff mounting. Using standard RS-232-C serial interfacing levels and simple ASCII commands, the SDAS-8 connects to all popular computers including personal computers with a programmable serial port.

The normal application for SDAS-8 is as a remote analog data input to a computer. The user's host computer would take the SDAS-8 data strings under program control and would process this data for arithmetic manipulation (peak detection, averaging, scaling and offset), display formatting (columnizing data with engineering unit labels), data storage to disk or tape or data retransmission.

SPECIAL FEATURES

SDAS-8 includes two onboard crystal-stabilized clocks, both of which are controlled and displayed with simple user commands. A settable 24-hour (23:59:59) time of day clock may be optionally tagged with each returned data scan transmission. A selectable independent interval timer causes automatic scan transmissions from 1 second to 17:59:59 hours intervals. Direct thermocouple inputs are available using the gain-selected, resistor-programmed instrumentation amplifier and a separate cold-junction compensation input channel. Under serial ASCII command, SDAS will directly linearize type J, K, T and S thermocouples with software correction for the local TC-to-copper cold junction EMF error using an external connector temperature sensor. Other ASCII commands produce direct data output in degrees Celsius or Fahrenheit from thermocouple inputs.

SDAS-8 includes both RS-232-C (non-isolated) and 20mA loop (isolated) serial ports. Using the loop ports, up to 4 SDAS-8 stations (32 Differential channels) may be multi-dropped in series on input and output loops (4 wires).

Individual channels may then be polled under host computer command many hundreds of feet away.

Requiring regulated +5V and ±15V dc power, SDAS-8 readily adapts to existing computers. Remote 2-wire data acquisition to any distance requires the addition of standard RS-232-C auto-dial, auto-answer telephone modems at both ends.

The standard SDAS-8 analog input range is ±4.095Vdc full scale at a gain of one. Analog signals are converted to a 12-bit binary representation plus polarity for bipolar signals, yielding a resolution of one part in 8192. For programming convenience, channel data is transmitted either as ASCII decimal or as ASCII hexadecimal under serial command. To simplify program number conversion, bit weighting in hex is 1 millivolt per count at gain = 1. All data is tagged with a hexadecimal checksum which may be compared for data link integrity.

The differential instrumentation amplifier is gain programmable with an external, user-supplied precision resistor for practical gains up to X200. For J and K thermocouples, SDAS-8 is calibrated for a gain of X80. S and T thermocouples require a gain of X160. The gain resistor is omitted for the gain-of-one ±4.095Vdc range.

The dual-slope, sign/magnitude A/D converter used in SDAS-8 continually overwrites a local random access semiconductor memory (RAM) buffer at 15 samples per second (12.5Hz for 50Hz NMR). Depending on baud rate, protocol overhead and formatting, per channel bandwidth is typically 1Hz.

A/D scan transmissions may be started by the remote host computer in polled mode or after host initialization of the SDAS-8 autostart timer. Scan starts may also occur using a local TTL start trigger input. In this mode, no host computer is needed. SDAS-8 will directly transmit to a serial input printer such as Datel's MPP-20 or APP-48 series.

A wealth of formatting controls are included for manual set-up, evaluation and calibration. Line length may be command-selected from 20 to 132 characters per line. Editing features include two types of rubout format, similar to micro-computer monitor programs. Line feed characters may be suppressed and filler NUL's may be command-selected for slow printers. Syntax errors which won't execute are echoed with a "#."

A status message indicates system state at any time. Half duplex operation may be invoked by suppressing the character echo and the string transmission can be throttled for host input buffer management using the XON/XOFF commands. A selectable (20 character) identification message may precede all data to tag the location, date, scale factors, etc. Line formatting prevents skewing or slicing of data for any one channel over two lines.

Careful selection of A/D integration periods offers rejection of 50 or 60Hz input noise.

SDAS-8 input/output connections are made through a dual-row right-angle connector whose mating pins may be PC board mounted or adapted to a flat cable header.

ST-705: A COMPLETE SDAS-8 SINGLE BOARD SUBSYSTEM

SDAS-8 is also available on the Model ST-705 single-board system which includes an AC power supply, screw-terminal analog input connections and a standard 25-pin RS-232-C DB-25P connector for direct plug-in to the user's terminal or computer. The ST-705 also includes the local thermocouple cold-junction compensation amplifier and connector temperature sensor. For local triggered scan starts, a TTL one-shot circuit accepts a switch input. Extra PC board pads are included for user-installed input voltage dividers (higher voltage ranges), current shunts (direct 4-20mA measurement, etc.) overvoltage protection clamp zeners or RC hash filters. Barrier screw terminals are installed to connect an AC line cord and pads are included for user-installed gain resistors.

The ST-705 is configured on a Multibus format PC board for mounting convenience in Multibus stand-alone card cages or in the user's host Multibus computer. The ST-705 may also be mounted in a separate chassis on standoffs. Although the ST-705 does not connect to the Multibus computer signals, pads are included to use +5V and ±15Vdc power from the host computer, thereby eliminating the ST-705 AC power supply. Using a combination of the transformer-isolated AC supply and the opto-isolated 20mA loop serial port, full isolation of the analog inputs is achieved on the ST-705.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SPECIFICATIONS

(Typical at +25°C, rated power unless otherwise noted)

ANALOG INPUT

Number of channels — 8 Differential plus single-ended CJC input*

*V_{CJC} IN = (Connector Temp. −0°C) × 40.96mV

Configuration — High impedance, non-isolated, voltage input, true balanced differential.

Full Scale Input Range — ±4.095 Volts dc (standard), gain = 1. The full scale input range may be reduced up to gains of X200 using an external user-supplied gain programming resistor.

Full Scale Temperature Ranges (using calibrated thermocouples and external cold junction compensation).

J Type	−165° C to +760°C
K Type	−165°C to +1232°C
S Type	0°C to +1768°C
T Type	−200°C to +400°C

Common Mode Voltage Range — ±11V max. referred to signal common (user's external input circuit must prevent exceeding CMV range).

Common Mode Rejection — 70 dB min., dc to 60 Hz, 1 kilohm unbalance, GAIN = 1

Input Overvoltage — ±14V max. referred to signal common (no damage)

Normal mode rejection — at 50Hz (SDAS-8E) 40 dB min., at 60Hz (SDAS-8A) 40 dB min.

Input Offset Voltage — ±200 microvolts max.

Input Bias current — ±80nA max.
(The user's external circuit must bias the input to remain within the CMV range. The input is not isolated.)

Input Impedance — 800 kilohms, min. either input to signal common.

Resolution — 1 millivolt per count (GAIN = 1)

Analog to Digital Conversion — 12 binary bits and polarity (1 part in 8192) dual-slope conversion with auto-zeroing in the A/D converter.

PERFORMANCE

A/D Sampling Rate — Continuous transfer of all 8 channels to local memory at 15 samples/second (60 hz NMR version, SDAS-8A) or 12.5 samples/second (50Hz NMR version, SDAS-8E), jumper selected.

Highest Bandwidth — Approximately 1Hz (9600 baud, suppress clock and ident. header strings, select only one channel, polled mode). More rapid polling will re-transmit previously sent A/D samples.

Input Offset Voltage Temperature Coefficient — ±3.6 microvolts/°C max., referred to input.

Gain Temperature Coefficient — (GAIN = 1) [voltage mode only, no TC linearization]
±20 ppm of FSR/°C typ.,
±50 ppm of FSR/°C max.
(external R GAIN resistor TC will add to these figures)

Accuracy (repeatability and non-linearity relative to calibration source) — ±0.02% of full scale range, ±1 count @ +25°C

Temperature Mode Accuracy (not including CJC and thermocouple calibration accuracy).

J Type	±2°C
K Type	±2°C
T Type	±2°C
S Type	±4°C

Rollover Error (Input polarity inversion, not including accuracy) ±1 Count

Calibration Control — 2 multiturn, external access potentiometers (zero and full scale gain) at edge of module, opposite connector. Recalibration is suggested every 90 days in non-hostile environments.

Internal Time of Day Clock — 23:59:59 hours:minutes:seconds (1 second resolution), ±0.05% max., ±0.01% typ. accuracy, crystal-controlled.

Cold Junction Compensation input range ..... ±99°C

COMMUNICATIONS

Data Encoding — Full Serial ASCII characters per ANSI × 3.4-1977 coding.

Baud Rates — 75, 150, 300, 600, 1200, 2400, 4800, 9600 (pin selected, see Baud rate table). Baud coding is acquired at power-up. Turn off power to reset if baud rate is changed.

Signal Levels

1. EIA RS-232-C (−3 to −15V = "1" MARK, +3 to +15V = "0" SPACE), non-isolated.
2. 20mA loop (20mA = "1" MARK, 0mA = "0" SPACE) isolated, ±2500V pk, 100 megohms*

*Current loop external excitation is required. Receiver drop: 1.6V in series with 75 ohms. Transmitter "1" drop, approx. 1.2V.

Mode — Full Duplex asynchronous, 4 wire.

Character Format — 1 Start bit (= "1"), 8 Data Bits (LSB first), no parity, 1 stop bit (= "0"), non-return to zero, compatible with terminals.

Handshake host buffer control protocol — Software only, received by SDAS-8:

XOFF = DC3 = 13 HEX = Control S
Stop SDAS-8 transmission immediate

XON = DC1 = 11HEX = Control Q
Resume SDAS-8 transmission

Hardware DSR or RTS Input to SDAS-8 is not implemented.

Distance (assuming low electrical noise environments, twisted pair or coaxial cabling):

RS-232-C	50 feet (15m)
20mA isoloop	10,000 feet (3050m)

Multidrop — Up to 4 polled stations (32D channels) may be connected in serial using two separate transmit and receive 20mA loops with external excitation (Not implemented for RS-232-C). Station selection is by station number (1 thru 4) command prefix. Auto-start or trigger start modes are not allowed.

CONTROL FEATURES

(Refer to command menu table. All commands are upper case ASCII characters plus controls)

Command Types (Input through receiver port)

1. Display formatting (line length 20, 40, 48, 72, 80, 132 char.)
2. Editing
3. A/D Channel Selection
4. A/D Data type (hex/dec radix, temperature)
5. Time-of-Day clock controls
6. Data link controls
7. Identification Header (20 characters max.)
8. Scan transmit start controls
9. Resets

Error checksum — All data strings are tagged with the hexadecimal 2's complement binary sum of the preceding data and control character string. Adding the hex values of all characters + checksum in a data string should equal zero. (This includes delimiters, syntax and controls).

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Specifications, Continued

Scan Start Methods

1. Local 10 microsecond TTL trigger input
2. Polled by ASCII command
3. Auto-start using internal timer, 1 second to 17:59:59 hours interval, command selected.

POWER REQUIREMENTS

+5Vdc regulated ±5% @ 500mA max., 400mA typ.
±15Vdc regulated ±5% @ 50mA max., 30mA typ.

INPUT/OUTPUT CONNECTIONS

Pins 1, 2, 41-44 — Common logic, data and analog grounds

Pins 3, 4 + 5Vdc reg. power in.

Pin 5 + 15Vdc reg. power in.

Pin 6 − 15Vdc reg. power in.

Pins 7-22 — 8 Differential Analog inputs

Pin 23 — Single-ended cold junction compensation input. V_{CJC} IN = (Connector temp −0°C) × 40.96mV (see typical circuit) or use CJC module. Leave pin 23 open for non-thermocouple inputs.

Tie pin 23 to ground for external CJC.

Pin 24 — Reference out, +2.048Vdc. May be used in external ratiometric circuits to develop a common, TC-tracking system reference. An external high impedance follower would be required.

Pin 25 — A/D converter input after PGIA and multiplexer (see block diagram)

Pins 26, 27 — External resistor (mount close to connector) to increase gain up to X200. R GAIN = 20Kiloms ÷ (GAIN-1). Use a low drift precision resistor and add resistor TC to overall drift. Leave pins 26, 27 open for GAIN = 1 (FSR = ±4.095V).

Pins 28, 29, 30, 34 — Baud rate select, see chart

Pin 31 — Received Data In, RS-232-C input. Input to type 1489 circuit.

Pin 32 — Loop /RS-232-C Select input, compatible to TTL or RS-232-C levels, 2.7 kilohm pullup to +5V, type 1489 circuit.

PIN 32	20mA loop input	RS-232-C
OPEN	ENABLED	DISABLED, LEAVE OPEN
GROUND	DISABLED, INPUT = DON'T CARE	ENABLED

Pin 33 — Scan Trigger In. A local 10 microsecond positive pulse will initiate a scan transmission per the pre-selected format. Input is a 1489 circuit, compatible to TTL or RS-232-C levels. Trigger pulses sent during scan transmission will be ignored and will not be saved. Do not send trigger pulses during command inputs.

PIN 35 — Transmitted Data Out, RS-232-C output. Output from type 1488 circuit.

Pin 36-39 — 20mA serial data loop I/O. Optoisolation: 2500V pk, 100 megohms. Both ports require external excitation currents. Receiver drop 1.6V in series with 75 ohms. Transmitter "1" drop, approx. 1.2V.

Pin 40 — Request to Send Out. When the SDAS-8 emulates a modem, RTS is asserted whenever power is on. RTS should also be jumpered on the DSR and CTS lines to enable most terminals. (see block diagram).

MECHANICAL, PHYSICAL, ENVIRONMENTAL

Case Fabrication — Fully enclosed (6 sided) 2-piece steel housing.

Outline dimensions — 4" × 6" × 0.4" (101,6 × 152,4 × 10,2mm)

Mounting Method — Via 4 corner standoff holes, 4-40 threads on user's printed circuit board or 4 standoffs.

Connector — Dual in-line right angle connector, two rows of 22 square .025" pins, 0.100" spacing (row and pin — pin). Mating connector type: AMP 1-86063-8 or ITT/Cannon UBS 4-044-1D (Datel Model 60-12284-1). SDAS-8 may be adapted to flat cable headers, 3M model 609 - 4400M or equal.

Operating Temperature Range — 0 to +60°C

Storage Temperature Range — −25°C to +85°C

Weight — 10 ounces (284 grams)

ORDERING GUIDE

MODEL NUMBERING:

SDAS-8

AC NORMAL MODE REJECTION AND A/D SAMPLING RATE	STATION NUMBER
A = 60 Hz (15 samples/second) E = 50 Hz (12.5 samples/second)	1 = CHANNELS 1-8 (MASTER, ECHOS ALL COMMANDS) 2 = SLAVE, CHANNELS 9-16 3 = SLAVE, CHANNELS 17-24 4 = SLAVE, CHANNELS 25-32 USE STATIONS 2, 3, 4 ONLY IN 20mA MULTIDROP WITH STATION 1 MASTER

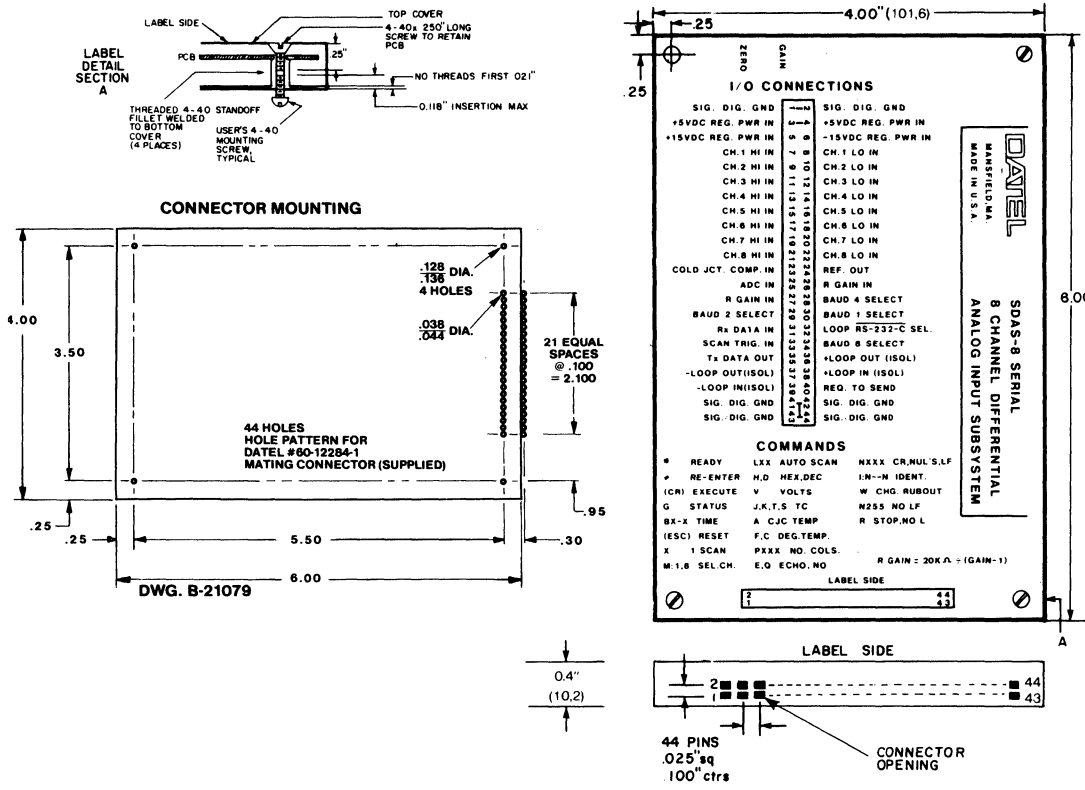
Example:
SDAS-8A1
60 Hz NMR, Master station 1, channels 1-8

A right-angle, PCB mating connector is included.
Contact Datel for quantity discounts.

ACCESSORIES/RELATED PRODUCTS

MODEL	DESCRIPTION
60-12284-1	Spare mating connector (one is included with SDAS-8)
TPM-15/150-5/1000 (115 VAC input) TPM-15/150-5/1000E (230 VAC input) TPM-15/150-5/1000J (100 VAC input)	Modular AC power supply, 5 Vdc regulator @ 1A and ± 15 Vdc reg. @ 150 mA
58-2079260	DB-25P solder tab RS-232-C connector
ST-705A (115 VAC/60 Hz) ST-705E (230 VAC/50 Hz) ST-705J (100 VAC/50 Hz)	Complete SDAS-8 subsystem, AC power supply, screw terminal inputs, CJC amplisensor, DB-25 connector
MPP-20, 48 Printers	Request Brochures

Mechanical Dimensions — Inches (mm)



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A/D CODING TABLE

Input Volts (R GAIN = ∞) (no connection)	Hexadecimal Display*	Decimal Display
+4.096 V	+++++	+++++
+4.095 V	ØFFFH	+4.095
+2.048 V	Ø800H	+2.048
+1.024 V	Ø400H	+1.024
+0.256 V	Ø100H	+0.256
+0.002	Ø010H	+0.002
+0.001	Ø001H	+0.001
0.000	0000H	+0.000
−0.001	FFFFH	−0.001
−0.002	FFFEH	−0.002
−0.256 V	FF00H	−0.256
−1.024 V	FC00H	−1.024
−2.048 V	F800H	−2.048
−4.095 V	F001H	−4.095
−4.096 V	-----	-----

*In hex, the polarity bit 12 has been extended to the top 3 MSB's (Bits 13, 14, 15)

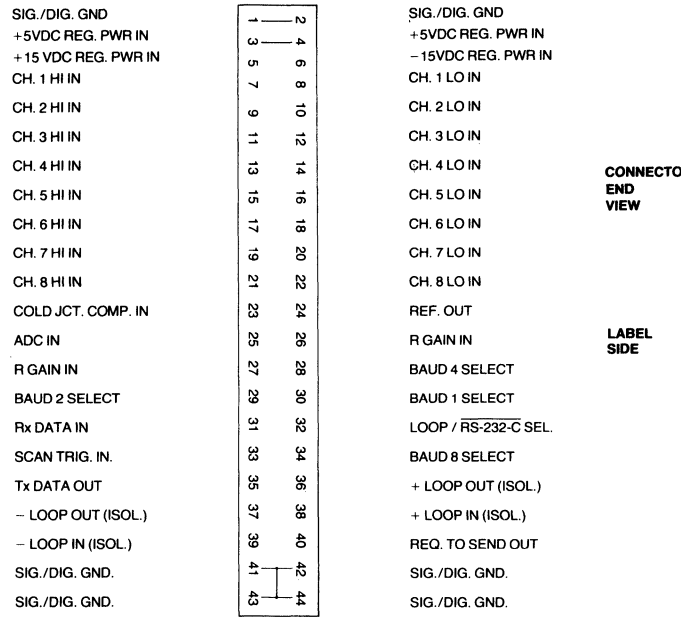
BAUD RATE SELECTION TABLE

Where Baud Rate = 1 ÷ Bit Period (in seconds) and logic "1" = +5V or open; "0" = ground or zero volts

BAUD RATE	BAUD SEL. 8 (pin 34)	BAUD SEL. 4 (pin 28)	BAUD SEL. 2 (pin 29)	BAUD SEL. 1 (pin 30)
75	1	0	0	1
150	1	0	0	0
300	0	1	1	1
600	0	1	1	0
1200	0	1	0	1
2400	0	1	0	0
4800	0	0	1	1
9600	0	0	1	0

INPUT/OUTPUT CONNECTIONS

R GAIN = 20KΩ ÷ (GAIN-1)



DATA LINK HANDSHAKING

SDAS-8 uses a minimal subset of the EIA RS-232-C I/O line designation (refer to the block diagram), consisting of Transmitted Data, Received Data, Signal Ground and Protective Ground. SDAS-8 also supplies an RS-232-C level Request-to-Send output which is always asserted when power is applied. Users may also need to assert the Data Set Ready input to the terminal or computer.

Otherwise, it is assumed that SDAS-8 will be used full duplex and all handshaking is data-encoded. Users who must operate half-duplex may suppress normal character echo from SDAS-8 back to the display by using the Q (CR) command. Users would normally write their computer program to change a half-duplex line from transmit to receive after the X (CR) scan command is sent with the echo suppressed. After a polled (X command) A/D scan was received, the host should turn the line around to transmit to be ready for the next command.

SDAS-8 also interprets the XOFF/XON protocol (control S or DC3/control Q or DC1) to intermittently halt the SDAS-8 transmitter in mid-string. This is used with computers which have a limited input string buffer length to prevent buffer overflow.

Send Escape first when operating SDAS-8 from a terminal

User's who wish to operate SDAS-8 manually from a CRT or printer terminal or from a microcomputer which is emulating an ASCII terminal should first send an Escape character to remove SDAS-8 from the power-up printer mode. This mode is intended for direct connection to Datel's APP-20 and APP-48 miniature thermal printers using the triggered scan start. These printers require suppression of Line Feed and 216 NUL characters following the Carriage Return to allow time to print each line. Sending an Escape after power-up reinstates the Line Feed following Carriage Return and cancels the filler NUL's.

ERROR DETECTION

All data is tagged with a 4-character hexadecimal checksum. The 16-bit (4 ASCII hex character) checksum is a 2's complement sum of all the previous data and control characters sent in the string before the checksum characters (the MSB bit 7 in each previous character is set to zero). By adding the checksum to the string sum, a zero result will indicate no data errors. Normally a user's program should perform this addition and CALL an error-flagging subroutine if the algebraic result is not zero. If the data link reliability is high, or occasional data errors are tolerable, this procedure is not required.

DISPLAY FORMATTING

For highest data efficiency, data is packed with a minimum of formatting characters. Normally, for data logging or display applications, the user would format the data (arrange it in tabular columns), apply labels ("gallons per hour," "RPM," "pump No. 4" etc.) and apply offset and span scaling arithmetic to the data. This is best done in the user's computer, probably using high-level language such as BASIC or FORTRAN which have display/printout formatting syntax.

Using SDAS-8 with Datel's MPP-20 and APP-48A2 Printers

When SDAS-8 is first powered up, either of these full serial RS-232-C printers may be directly connected and operated in the triggered scan mode with a TTL start pulse to SDAS-8 pin 33. The 216 NUL filler characters following CR allow adequate time for the 750mS print cycle *provided that 2400 BAUD or lower is selected.* In addition, the printer connector jumpering and DIP switches must also match the SDAS-8 word format (8 data, no parity, 1 stop).

SERIAL COMMAND SUMMARY

LEGEND:

1. XXX — X are characters entered and displayed on the terminal.
2. ( ) are blind control characters (such as carriage return or escape) which do not appear on the terminal.
3. [ ] are notes on the command. They are not entered or displayed.
4. Carriage return (CR) requests the SDAS-8 to execute the command consisting of the previous character string.
5. The asterisk (*) confirms that the command was executed, and is ready for the next command.
6. The pound sign (#) indicates that the returned character string is not executable. Re-enter a corrected string.

COMMAND CHARACTERS

G (CR) — Display status message
B (CR) — Display time (HR: MIN: SEC)
B 23:59:59 (CR) — Set time in 24 hour format
(Escape) — Reset all controls to power-up status except clock
(Backspace) — Delete previous character
(Control S or DC3 or XOFF) — [13 HEX] Stop transmission immediate and wait
(Control Q or DC1 or XON) — [11 HEX] Start transmission immediate, mid-string
R — Stop output transmission from SDAS-8.
Stop L mode auto-start timer. (CR) not required. Revert to trigger or polled-start mode.

A/D CONTROLS

X (CR) — Display one scan
M:2 (CR) — Set up to display channel 2 only
M:1, 8 (CR) — Set up to display channels 1-8
LO2 (CR) — Start automatic scan transmissions every 2 seconds. R or (ESC) are the only way to stop L mod.
L59:59 (CR) — Start automatic scan transmissions every 59 minutes :59 seconds
L17:59:59 (CR) — Start automatic scan transmissions every 17:59:59 hours: minutes / seconds (max).
H (CR) — Format A/D data as hexadecimal ASCII
D (CR) — Format A/D data as decimal ASCII (cancel hex)
V (CR) — Format A/D data as DC volts, (cancel thermocouple)
J (CR) —Format A/D data linearized to selected thermocouple
K (CR)
S (CR)
T (CR)

* — Power-up prompt. Previous command executed; ready for next command.
\# — Echoed string not executable; try again.

A (CR) — Transmit A/D data from CJC channel, equivalent ambient temperature. Range ±99°C
F (CR) — Format A/D data as Fahrenheit.
C (CR) — Format A/D data as Celsius.

TERMINAL CONTROLS

W (CR) — Toggles between rubout echo as BS-SP-BS or /X where X is the last character.
P80 (CR) — Set column width to 20, 40, 48, 72, 80 or 132 (20 = power up state)
E (CR) — Echo all printables (power up state) for full duplex
Q (CR) — Don't echo printables (for half duplex)
N nnn (CR) — Insert nnn nulls between, CR, NULL's, LF
N255 (CR) — Suppress line feed. End all scans with CR, (NULL's), no line feed, N255 (CR) is a toggle, which cycles on and off with each application. Confirm the line feed status bit using the G status.

IDENT STRING

I : nnn — n (CR) — Start all A/D scans with the Ident character string nnn — n (20 characters max)
All lower case printables — Echo if selected. Not acted upon.
All non-specified controls — Echo if selected. Not acted upon.
BN (CR) — Delete, time and station
BY (CR) — Resume, time and station

POWER UP MODE

Station 1
20 characters per line
Trigger/polled scan start
8 channels, 1-8
Echo on

Elapsed time from power-on
The line terminator sequence at power up is:
<CR, NUL, NUL, -- (216 NUL's), no LF>
For CRT's, send ESCAPE to cancel the NUL's and restore LF.

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DATA OUTPUT FORMAT

The following message samples were prepared on an SDAS-8 directly connected to an RS-232-C Datel APP-48A2 thermal printer and a CRT terminal. These data printouts indicate the degree of formatting control, channel selection, editing and message readability offered by SDAS-8. Note throughout these samples the visual format consistency even when changing line length. Each data point uses a constant 9 characters and is tagged with a hex checksum for optional error detection. Hexadecimal samples always include an "H" in the data with optional C or F temperature tags trailing the H. The suppressable clock line includes the station number and an optional 20-character ident/header message is returned with each sample (4 headers may be used with 4 multidrop stations).

While some computer programs may re-format returned data strings, many will simply reflect the string out to a printer or other ASCII device. SDAS-8 data will preserve the consistent readability of this output.

ASCII Controls which are blind (CR, LF, NUL's, DEL, ESCAPE, etc.) of course are not displayed but their effects can be seen in the editing and non-executable command strings.

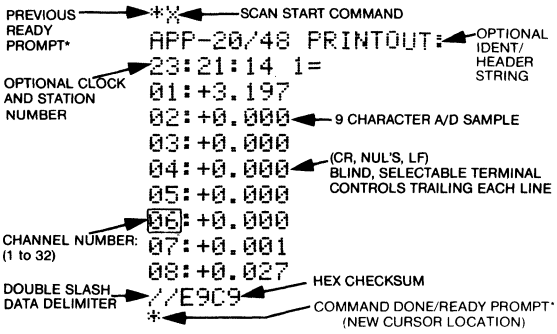
LOADING AN IDENT/HEADER STRING:

```
*I:APP-20/48 PRINTOUT:
```

SETTING AND DISPLAYING THE CLOCK:

```
*B23:00:00
*B
23:00:02
```

20-COLUMN OUTPUT:



40-COLUMN OUTPUT USING THE IDENT/HEADER AS A DATE STAMP WITH FAHRENHEIT THERMOCOUPLE PRESENTATION:

```
*X
10/17/83 BATCH 9
23:15:56 1=
01:+1824F/02:  +83F/03:  +83F
04:  +83F/05:  +83F/06:  +83F
07:  +83F/08:  +97F//EAB9
```

STATUS MESSAGE:

```
*G
B80481/ HEX STATUS
STATION 1 ONLINE
TIME 23:07:15
40 CHARS PER LINE
START CHAN. IS 1
FINAL CHAN. IS 8
TYPE J THERMOCOUPLE
ECHO IS ON
OUTPUT IS HEX. DEG F
DEL ECHOED /LAST CHR
NO LF AFTER CR
```

AMBIENT CJC CELSIUS DECIMAL OUTPUT:

```
*A
SDAS-8 IDENT STRING
23:10:13 1=
CJC:  +27C//F9B3
```

RESPONSE TO NON-EXECUTABLE COMMAND STRING:

```
*BAD COMMAND SAMPLE
BAD COMMAND SAMPLE#
```

RESPONSE TO PRINTER-COMPATIBLE BACKSPACE FUNCTION:

```
*DEL/L/E/D
```

48-COLUMN CELSIUS THERMOCOUPLE OUTPUT:

Note: Terminate each line entered from the keyboard with carriage return.

```
*X
IBM PC SDASLOGGER
23:22:00 1=
01: +736C/02:  +29C/03:  +29C/04:  +29C
05:  +29C/06:  +29C/07:  +29C/08:  +35C
//E949
```

HEXADECIMAL CELSIUS OUTPUT AFTER SELECTING CHANNELS 1-3:

```
*M:1,3
*X
LO PRESS TURBO TEMP
00:30:12 1=
01:02E0HC/02:001CHC/03:001CHC//F1DF
```

HEX VOLTS OUTPUT, CHANNELS 1-3:

```
*X
MANIFOLD GAL/HR
00:30:20 1=
01: 0C7EH/02: 0000H/03: 0000H//F259
```

STATUS MESSAGE FORMAT

In response to a G (CR) command (or 2G, 3G, 4G for Multidrop stations), SDAS-8 will transmit a status message in 20 column format. The status message contains two parts: an encoded hexa-decimal header and a plain-English body. The header may be read by the user's host computer (after being intercepted by a string-capture parsing program)

The status message indicates the contents of 3 status bytes (24 bits) which SDAS-8 assembles when status is requested. The 3 bytes are represented by 6 ASCII hex characters such that the least significant 4-bit hex nybble of each ASCII hex character comprise the upper and lower nybbles of each of the 3 bytes.

Two of the status bytes indicate various formatting parameters and the third byte indicates A/D channel selection for that station.

The encoded hex status is placed at the beginning of the message to simplify the task of the user's parsing program (to avoid searching the entire message string for status information).

At power-up, the status defaults to the state shown including 216 filler NUL's after CR and suppression of line feed. An Escape command sent anytime thereafter reverts to this default state *except* that the NUL's are deleted and LF is inserted after CR.

Status Message format (□ = variable)

[FFFFF]/HEX STATUS <CR, NULS, LF>
STATION [1] ON LINE <CR, NULS, LF>
[20] CHARS. PER LINE <CR, NULS, LF>
[TRIGGER] SCAN START <CR, NULS, LF>
[TIMER]
START CHAN. = [1] <CR, NULS, LF>
FINAL CHAN. = [8] <CR, NULS, LF>
TYPE [J] THERMOCOUPLE <CR, NULS, LF>: not listed on default
ECHO IS [ON / OFF] <CR, NULS, LF>
OUTPUT = [DEC. / HEX.] VOLTS <CR, NULS, LF>
DEG. C
BS = [/ LAST CHAR. / BS-SP-BS] <CR, NULS, LF>
[LF ADDED AFTER CR <CR, NULS, LF> / NO LF AFTER CR]

Encoded HEX Status:

FFFFFF/HEX STATUS <CR, NULS, LF>
- CHAN. SELECT BYTE (HI CHAN., LO CHAN.)
- 2ND STATUS BYTE
- 1ST STATUS BYTE

Power up default state will be: 000081

1st Status Byte

7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	— DEFAULT STATE

BITS 1 + 0 — 00 For J type thermocouples (default state)
— 01 For K type thermocouples
— 10 For S type thermocouples
— 11 For T type thermocouples
BIT 2 — 0 = ECHO ON (default state)
— 1 = ECHO OFF
BIT 3 — 0 = Output in volts [default] [overrides bits 0+1+5]
— 1 = Output in temperature
BIT 4 — 0 = Output in Decimal (default state)
— 1 = Output in Hexadecimal
BIT 5 — 0 = Output in Celcius (default)
— 1 = Output in Fahrenheit
BIT 6 — 0 = Rubout or Backspace as / last char.(default)
— 1 = Rubout as BS-SP-BS sequence
BIT 7 — 0 = LF enabled after fill characters
— 1 = LF disabled after CR (default)

2nd Status Byte

7	6	5	4	3	2	1	0	
0	X	0	0	0	0	0	0	— DEFAULT STATE

BITS 1+0 — 00 = Communicating with station 1 (default)
— 01 = Communicating with station 2
— 10 = Communicating with station 3
— 11 = Communicating with station 4
BITS 4+3+2 — 000 = 20 Characters per line (default)
— 001 = 40 Characters per line
— 010 = 48 Characters per line
— 011 = 72 Characters per line
— 100 = 80 Characters per line
— 101 = 132 Characters per line
BIT 5 — 0 = Trigger or polled start mode (default)
— 1 = Timer start mode
BIT 6 — Don't care
BIT 7 — 0 = XON SET (default)
— 1 = XOFF SET

3rd Channel Selection Byte

7	6	5	4	3	2	1	0	
1	0	0	0	0	0	0	1	— DEFAULT STATE

BITS 0+1+2+3 — Low channel scan selection
BITS 4+5+6+7 — High channel scan selection

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DUMB TERMINAL SESSION

A typical application for SDAS-8 is a remote A/D data transmitter controlled by a host computer which continually logs A/D scans. However, SDAS-8 may also be controlled manually from a dumb terminal.

For demonstration purposes, a typical session with a dumb terminal will be described. The dumb terminal consists of a keyboard input device and a data output device consisting of a printer or a CRT display.

All conversations use ASCII characters (ANSI x3.4-1977) sent over EIA RS-232-C digital data lines. A minimum of 4 wires (RxD, TxD, signal ground and chassis ground) carry all information. SDAS emulates an on-line data base by echoing all printable characters it receives. The user's dumb terminal would normally be configured in full duplex so that the keyboard characters appear on the display as SDAS-8 echoes them.

Power to the terminal is first turned on. Then SDAS-8 is turned on and after several seconds of self-test, it transmits an asterisk (*) prompt indicating that it is ready for a command. For a dumb terminal, the user must send ESCAPE to cancel the power-up printer mode. To see a plain-language status message, the user then presses G and carriage return (CR). SDAS-8 responds by transmitting a status message terminated by an asterisk. The carriage return tells SDAS-8 to interpret the G (status) command and execute it.

The returned asterisk indicates that SDAS-8 successfully completed the command and is ready for a new command. In this way, SDAS-8 operates similarly to a microcomputer monitor program.

The user may then send any of the commands, most of which are a few characters long. Sending an X(CR) will immediately send a full analog scan in decimal volts format. The scan will begin with the elapsed time from power on, the analog channel data and ends with a 4-character hexadecimal checksum. This checksum is used by a host data logging computer to continually verify the integrity of the data link.

Repeated X (CR) commands will send subsequent analog scans. This is the normal polled mode that a host computer would use.

SDAS-8 can also initiate its own scans by commanding it into the timer auto-start mode. By pressing L03 (CR) for example, SDAS-8 will automatically send scans every 3 seconds and a wide range of other timer intervals may be commanded, from 1 second to 17:59:59 hours.

A full menu of other commands may be invoked at any time during operation since SDAS-8 continually listens to its serial input except during scan transmission.

These commands alter the data format, printout format, and other controls. Data may be sent as decimal or in 2's complement hexadecimal, either as DC volts or linearized to J, K, S, or T thermocouples in degrees Fahrenheit or Celsius. The local connector temperature may also be sent to invoke cold junction compensation.

Power-up display width is initiated for 20 columns but may be selected up to 132 columns. Therefore, all popular printers may be employed.

Editing controls include 2 popular rubout formats, and a pound sign (#) acknowledgement of an unintelligible (non-executable) command string.

The 24 hour clock may be set and read for actual time or it may be suppressed in returned scan strings to reduce transmission time. Popular XON/XOFF transmitter controls are accepted by SDAS-8 to accommodate host computers which need to avoid overflowing their input buffers. This is a common time-share/modem control.

Users who prefer to use local half-duplex display of their keyboards may suppress the echo feature.

A selectable number of NULL characters may be inserted between Carriage Return and Line Feed to accommodate certain printers. Line feed may be suppressed so that carriage return alone acts like a print command or NEWLINE/ENTER.

The polled scan transmission mode will also accept a local SDAS-8 TTL trigger start pulse. For example, a simple data logger requiring no keyboard may be built using a 74123 one-shot trigger generator and Datel's miniature MPP-20 thermal printer.

SDAS-8 CALIBRATION PROCEDURE

This calibration is performed by alternately connecting the input terminals for channel 1 to ground (zero volts) and +/− 4.000 Vdc (nearly full scale). Adjustments are made to the calibration potentiometers until the instrument performs properly.

1. Make the normal external connections from SDAS-8 to a DC power supply and a separate video RS-232-C CRT terminal. A microcomputer executing a dumb terminal emulator program may also be used instead as well as a printing terminal. If a keyboard input device is not available, SDAS-8 scans may be seen on a printer only using the local scan trigger input repeatedly pulsed at pin 33. Strap the baud rate pins to as high a baud rate as possible. Set the input PGIA gain equal to one by making no connection to pins 26 and 27. The complete ST-705 is recommended to simplify connections.
2. Assuming the use of a video terminal or emulator, first turn on the terminal power.
3. Turn on the SDAS-8 power supply. An asterisk (*) prompt will appear on the terminal after power up self-test. Because of the power-up printer mode, the asterisk may take many seconds at low baud rates.
4. Cancel the printer mode by sending an ESCAPE character to SDAS-8.
5. Delete the clock line by sending BN(CR)
6. Delete the ident line by sending I:<CR>
7. Select channel 1 by sending M:1<CR>
8. Select decimal volts display by sending D<CR> and V<CR>.
9. Cancel filler NUL's by sending Nϕ<CR>
10. SDAS-8 should now be ready for operation. Sending a G<CR> status request will confirm the previous parameters. A single analog scan may be seen by sending X<CR>
11. Start SDAS-8 sampling once per second by sending Lϕ1<CR>. This may be terminated with an R<no CR> command.
12. Connect a precision DC voltage source of known accuracy (such as Datel's DVC-8500 or DVC-350 DC voltage calibrators) to pins 7, 8 and 1. Connect the calibrator HI (positive) output to pin 7 and the LO (negative or ground) output to pins 8 and 1 connected together. All 3 pins must be connected.
13. Set the calibrator output to zero output. SDAS-8 should display zero or within a few counts of zero. An identical reading should be seen if the calibrator is disconnected and pins 7 and 8 are both grounded to pin 1.
14. Adjust any small offset error to a reading of 0.000 by

CALIBRATION, CONTINUED

rotating the "ZERO" potentiometer at the end of the SDAS-8 case using a small slotted screwdriver.

15. Select an output of +4.000 Vdc on the calibrator.
16. Adjust the SDAS-8 displayed output on the terminal to read +4.000 by rotating the "GAIN" potentiometer on the SDAS-8 case, adjacent to the "ZERO" pot.
17. The "ZERO" and "GAIN" adjustments interact somewhat, therefore repeat steps 14 through 16 until no further improvement can be achieved.
18. A rollover test can be made by reversing the positive and negative calibrator output leads (sometimes this is available using a polarity inversion switch). The SDAS-8 displayed output should be within −3.998 to −4.002 volts. If the application will use predominantly negative inputs, the user may wish to readjust the "GAIN" pot.
19. This completes the calibration for a gain of one. The user may now proceed to higher gain and thermocouple input calibration if desired.
20. Programmable Gain Instrumentation Amplifier Calibration: If the user is increasing the system amplification by adding an external gain resistor connected adjacent to pins 26 and 27, calculate the desired resistance using the gain equation (RGAIN=20KΩ÷(GAIN-1)).
21. Connect the gain resistor and repeat the calibration steps using proportionately lower calibrator output voltages (a precision attenuator may be desirable).
22. Two important exceptions should be noted: PGIA gain should be adjusted by trimming the external gain resistor, not by adjusting the SDAS-8 "GAIN". This is to avoid offset interaction.
23. Similarly, higher gain offset corrections should be made externally in the user's circuit with small offset adjustment circuits.

If both external PGIA offset and gain adjustments are impractical, the SDAS-8 pots may be used but will no longer be calibrated at a gain of one.

> The guiding rule is to recalibrate if gain changes are made.

24. SDAS-8 is internally resistor-trimmed before shipment for common mode rejection errors. To prevent PGIA settling time difficulties, the channel multiplexing is inhibited and the PGIA is continuously connected to Channel 1 by sending the command Y:E$\phi\phi$2<CR>. SDAS-8 must be powered down to reset this command. The PGIA analog output then appears continuously on pin 25 and A/D scans are terminated. The CMR should not normally need adjustment. Contact Datel if you need assistance.
25. Temperature Measurements are a complex interaction between the calibration accuracy of the selected thermocouple, the PGIA gain resistor, the CJC sensor, any CJC gradient error and previous SDAS-8 "GAIN" and "ZERO" pot adjustments.

    A suggested procedure is to make two calibrated temperature sources available (an ice bath and a calibrated oven), and a reference-grade thermocouple. Since this may be impractical, an attenuated voltage calibrator developing equivalent millivolt temperature outputs may be used which track the published ANSI and NBS thermocouple tables. Using the calibrator method, ground the CJC input (connect pin 23 to pin 2).

    Select the appropriate linearization using the J,K,T, or S <CR> commands and degrees Celcius using C<CR>. Calibrate as before, using the PGIA resistor if possible for the high calibration temperature. Use the ice bath and the SDAS-8 "ZERO" pot for 0°Celsius. Null out any interaction with the "ZERO" and "GAIN" pots after initial PGIA resistor adjustment.

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DETAILED COMMAND DESCRIPTION (SEE NEXT PAGE)

Command descriptions: The tables on the next page list ASCII character commands sent by the host computer or user's terminal and then acted upon by SDAS-8. All commands are upper case capitals only. Lower case letters sent to SDAS-8 are echoed back to the host or terminal but are not acted upon.

Command Sequence — As each character is sent from the host or terminal, it is immediately retransmitted (echoed) so that it may be displayed on the terminal (in full duplex mode) to aid in typing or for the host to confirm proper transmission. Execution of the command by SDAS-8 does not begin until the host or terminal sends ASCII Carriage Return (CR). Until CR is sent, typing or transmission errors may be fixed by sending ASCII backspace or delete characters. After SDAS-8 performs the command, it indicates completion by sending as asterisk(*). The next command may begin immediately after the asterisk and host software should test for errors if the asterisk is not sent when expected. The only mode which appears to withhold asterisk acknowledgements is the auto-scan L mode. During the L mode, no other commands can be accepted (true to the asterisk convention) except the R or Escape command to terminate the L command, at which time an asterisk is sent.

These tables list the command character, its hexadecimal byte equivalent code, and its keyboard input equivalent using the "control" (↑) key. Other keyboard forms are also shown.

All control characters are "blind" (do not remain displayed) and are designated by parenthesis ( ).The parenthesis should not be sent.

Although command characters sent *to* SDAS-8 are terminated with a single (CR), output character strings returned *from* SDAS-8 are terminated with a selectable (CR, NUL's, LF) format to suit differing terminals and printers.

These tables also include (where applicable) the command(s) to alter the command which is listed.

Most printable characters may be optionally echoed (full duplex) or non-echoed (half-duplex). Control characters vary and this is shown in the "echo" column.

The command formats listed below are for a single SDAS-8, channels 1-8, station 1. For *multidrop* applications, most commands require a station number prefix (1, 2, 3, or 4) for channels 9-16, 17-24, and 25-32 respectively. Some commands (such as the L mode) are not allowed in multidrop. The "Multidrop Usage" column lists these variations.

During locally-triggered scans (trigger input to pin 33), SDAS-8 ignores inport serial characters but stores a single character in its UART buffer.

INPUT ASCII CHARACTERS	EQUIVALENT CONTROL (↑) CHAR. OR HEX	MULTIDROP USAGE	FUNCTION	NOTES: ECHOABLE? HOW TO ALTER? OUTPUT RESPONSE, ETC.
			FILL CHARACTERS AND LINE FEED SUPPRESSION	
Nnnn<CR>		Acted upon by all stations simultaneously. Only Sta. 1 acknowledges.	Insert nnn NULL's (ØØH) after CR to allow buffering delay for printers. nnn may be a 1, 2, or 3 digit digit number with a range of Ø to 254 nulls.	The power up state of the SDAS-8 is 216 NUL's after CR and no LF for Datel APP-20/48 printer usage with locally-triggered scans. Example: N3<CR> causes all SDAS-8 transmissions to end with <CR NUL NUL NUL LF>
N255<CR>		Acted upon by all stations simultaneously. Only Sta. 1 acknowledges.	N255<CR> alternately toggles Line Feed (LF) suppression on and off after the CR, NUL's sequence sent from SDAS-8. LF suppression state may be checked with the G (status) command.	
			ECHO COMMANDS FOR HALF OR FULL DUPLEX	
E <CR>		Acted upon by ALL stations. NO PREFIX. Only Sta. 1 acknowledges.	Echo all characters as sent except: CR echoes as selectable <CR , NULS, LF> *(see description) Escape echoes as <CR, NUL's, LF> * (see description). Rubout or Delete (see W description).	Alter with Q <CR>
Q <CR>		Acted upon by ALL stations. NO PREFIX. Only Sta. 1 acknowledges.	Stop echo on all commands including the next E <CR> until echo is restored. Normal X and L scans occur at all times.	Alter with E <CR> or Escape.
			COMMANDS	
<CR>	ØD hex. Also designated "↵" or "ENTER" or "NEWLINE" or "RETURN" on some keyboards.	ALL STATIONS NO PREFIX	Execute the previously sent character string, if intelligible. If execution is successful, SDAS-8 responds with an asterisk (*) prompt. If the string is not executable, SDAS-8 echoes the string, terminated with a pound (#) sign <CR, NUL,s LF> and a new * prompt. The line terminator sequence <CR, NUL's LF> always includes the CR, and user-optional filler NUL's (ASCII ØØH) and user-optional Line Feed. Successful L command execution delays the prompt until R or Escape <CR> clears the command buffer.	Output responses: 1) If executable: <CR, NUL's LF> [execution interval] * 2) If not executable: <CR, NUL's LF> [unintelligible string] # <CR, NUL's LF> * An empty string (CR) alone is not executable and is returned as: <CR, NUL's, LF> # <CR, NUL's, LF> *
			TERMINAL EDITING CONTROLS	
Rubout or Delete or Backspace	7FH 08H or Control H.	Echoed by selected station only.	Delete echoes as one of two formats depending on the last state of the W command toggle. For printer usage, delete echoes as slash, last character (this is the power-up default mode). Example: ABC (an unintelligible command string) prints ABC/C/B/A if 3 deletes are sent. For video display terminal usage, delete echoes as backspace-space-backspace, moving the cursor backwards on the display and erasing previously sent characters.	Deletes always echoes unless no previous characters were sent after the last * prompt.
W<CR>		Echoed by selected station only.	W alternately toggles delete or backspace characters sent to SDAS-8 as either slash, last character or BS-space-BS (see delete). Delete usage (W state) may be checked using the G (status) command.	W<CR> is selectable echo
			HOST BUFFER OVERFLOW HANDSHAKES	
XOFF	DC3, Control S or 13 HEX	ALL STATIONS	Halt transmission immediately in mid-string (a character in progress will be completed). Send only XON or Escape after sending XOFF.	Restored by XON XON/XOFF do not echo. XOFF/XON may be sent several times during transmission without losing characters.
XON	DC1, Control Q or 11 HEX.	ALL STATIONS	Resume transmission in mid-string. XON/XOFF are commonly used for flow control of computers and printers with limited buffer size.	Do not set XOFF within a command string before sending CR.
			LINE LENGTH CONTROLS	
Pnnn <CR>		ALL STATIONS, no prefix.	Pnnn <CR> establishes the maximum number of characters sent per line before the <CR, NULS, LF> line terminator. SDAS-8 supports line lengths from 20 characters per line (power-up default value) to 132 character/line. Channel samples will be spaced for easiest viewing and vertical tabular alignment to avoid skewing a data sample over 2 lines. nnn may be 20, 40, 48, 72, 80, 132 characters per line.	Example: P80 <CR> will adjust SDAS-8 output not to exceed 80 char./line. The G status message is always 20 char./line. Pnnn <CR> is selectable echo.
			A/D CONTROLS	
D<CR> H<CR>		Use station prefix, example: 3D <CR> for station 3 (Ch. 17-24) only.	Radix controls: D <CR> formats output A/D data as ASCII bipolar (sign/magnitude) decimal. H <CR> formats output as sign-extended, 2's complement binary transmitted as ASCII hexadecimal.	D and H are selectable echo, Refer to the coding table for information. Power-up default is Decimal. HEX data is always tagged with an "H" last character.
M:n,m <CR>		Use station prefix, example: 3M:17, 18 <CR>	Number of channels: The M command selects the channels to be sent. M:5 <CR> sends channel 5 only. 4M:25, 29 <CR> sends channel 25 through 29 whenever station 4 is polled.	M:n,m <CR> is selectable echo. Only one sequential interval is allowed per station. Power-up default mode enables all channels.

INPUT ASCII CHARACTERS	EQUIVALENT CONTROL (↑) CHAR. OR HEX	MULTIDROP USAGE	FUNCTION	NOTES: ECHOABLE? HOW TO ALTER? OUTPUT RESPONSE, ETC.
			SCAN TRANSMISSION STARTS:	
X<CR>		Use station prefix, example: X<CR> scans station 1. 4X<CR> scans channels 25-32.	X<CR> starts a single scan transmission and is the normal polled mode from a host computer.	X<CR> is selectable echo.
Ln--n<CR>		Not allowed in multi-drop.	L mode is an auto-start scan transmission automatically sent from SDAS-8 using the timer interval specified in the L mode command string.	Disable L mode with R <no CR> or Escape <no CR>. All other commands except XON/XOFF are ignored. L mode is not allowed in multi-drop to avoid data collisions. An * acknowledgement is not sent until R or Escape.
		Use for station 1 only.	L mode timer range is 01 second to 17:59:59 hours: minutes: seconds. Examples: L01 <CR> is 1 second. L05: 00 <CR> is 5 minutes. L08: 30: 00 <CR> is 8½ hours. L20: <CR> not allowed. L2: 00 <CR> not allowed. L: 30 <CR> not allowed.	
			IDENTIFICATION/HEADER STRING	
I:n--n<CR>		Use station prefix for separate station. Example: 3I: Ident. <CR>	I: <CR> is a general purpose user-loaded message line which will accept 96-character ASCII printables of upper or lower case letters, numbers and punctuation. The character string will truncate at 20 columns and is returned with each scan as a first optional line before the clock and station line.	Delete the ident. string by sending I: <CR>, the empty string which is the power-up default state. Do not send controls except CR, DEL, LF, BS, Escape.
			SYSTEM RESETS	
Escape <no CR>	1B HEX, control [	ALL STATIONS	Master reset, accepted at any time. Cancels transmission in progress. Clears command buffer. Does not reset clock registers.	Echoes as <CR, NUL's, LF> *. Video terminals must send ESC first to reset printer mode.
R <no CR>		ALL STATIONS	Used to stop L mode or any transmission in progress without changing other parameters. Cancelled strings are lost.	Echoes as R <CR, NUL's, LF> * unless echo is off.
			TIME-OF-DAY CLOCK CONTROLS	
B<CR> Bhh: mm: ss <CR> BN <CR> BY <CR>		Use station prefix for separate stations. Example: 3B <CR> (no prefix) B--- sets all clocks simultaneously.	Sends clock string in 24 hour (23:59:59 Hours: Minutes: Seconds) format. Sets clock. Example: B16:00:00 <CR> sets 4 PM. B00:00:00 <CR> is midnight. BN Inhibits clock characters in scan transmission, to reduce transmission time. BY Enables clock/station line	Clock powers up at 00:00:00 with clock and station number line enabled. Clock is not reset by Escape. Echo is selectable.
			MISCELLANEOUS	
All non-specified controls		ALL STATIONS	All controls not listed will have echo if selected but will have no effect on SDAS-8. This allows standard terminal control functions.	
All non-upper case printables		ALL STATIONS	Will echo if selected but will have no effect and will return a non-executable # with <CR> unless cleared by Escape or Deletes. Ident strings (see I: command) will accept all printables.	
O, U, Y, Z		ALL STATIONS	Reserved, do not use.	For calibration purposes only, the command Y:E002 <CR> stops A/D scanning and continuously switches the analog mux to channel 1 and the PGIA output appears on pin 25. Power down to reset.
			STATUS MESSAGE	
G<CR>		Use station prefix for separate stations. Example: 2G <CR>	The G command causes SDAS-8 to transmit a status message consisting of a hexa-decimal status code followed by a plain-language translation, in 20-column format. See the status message example. Status includes station number, time, char./line, start/final channels, echo, decimal/hex, volts/thermocouple, delete usage and LF suppression.	May be terminated by R or Escape.
			THERMOCOUPLE TEMPERATURE MEASUREMENT CONTROLS	
J <CR> K <CR> S <CR> T <CR>		Use station prefix for separate stations.	Linearize the A/D data using ANSI/NBS J, K, S or T thermocouple tables and correct for ambient temperature input voltage (cold junction compensation) to pin 23. Data will be in decimal or hex format depending on the last state of the H or D commands, and Celsius or Fahrenheit conversions.	External PGA gain resistors (J, K use gain = X80.; S, T use gain = X160) and a CJC sensor circuit are required. Cancel TC linearization using V (volts) command.
C <CR> F <CR>		Use station prefix for separate stations.	C and F format temperature data to Celsius or Fahrenheit respectively.	Escape or power-up defaults to Celsius decimal format.
A<CR>		Use station prefix for separate stations.	The A command returns the ambient temperature measured through the CJC sensor circuit connected to pin 23. Data may be formatted in decimal/hex, Celsius/Fahrenheit. In 20-column line length, the CJC output will be 3 lines (times/station, CJC temp., checksum). Example: 00:39:35 1= CJC 26C //FB1E. By suppressing the clock (BN <CR> command) and requesting more than 20 characters per line (Example: P40 <CR>,) the CJC and checksum will form on one line Example: CJC: +26C//FD82	The local SDAS-8 temperature may be accessed anytime a CJC sensor circuit is installed, even if thermocouples are not used. In fact, this fixed-gain (X100) ninth channel may be used for any purpose but is only sent with the A command. The maximum CJC range is ±99° C (±4.095Vdc) and resolves 1° C.

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MULTIDROP APPLICATIONS

This application shows up to four multidrop SDAS-8 stations sharing common transmit and receive 20mA serial data loops. Because each T/R serial port is optically isolated, the internal analog channels may have several hundred volts of isolation from station to station (*within* a single station however, analog inputs must remain within the ±11V common mode voltage range). By using the current loop mode, stations may be separated thousands of feet in low noise environments. The two current loops require a source of excitation and a typical circuit and external power supply is shown. Some host computers and terminals include their own excitation supplies. Users should carefully test such remote systems because low data errors are a complex result of shielding, noise protection, wire type, baud rate, and link ringing suppression.

Multidrop SDAS-8 stations are addressed with a station number prefix before each command (Example: "3M:2(CR)" configures station 3 (channels 17-24) to respond with only channel 18 in returned data strings). Ommission of the station number prefix always implies station 1 (channels 1-8), which responds with or without the 1 prefix.

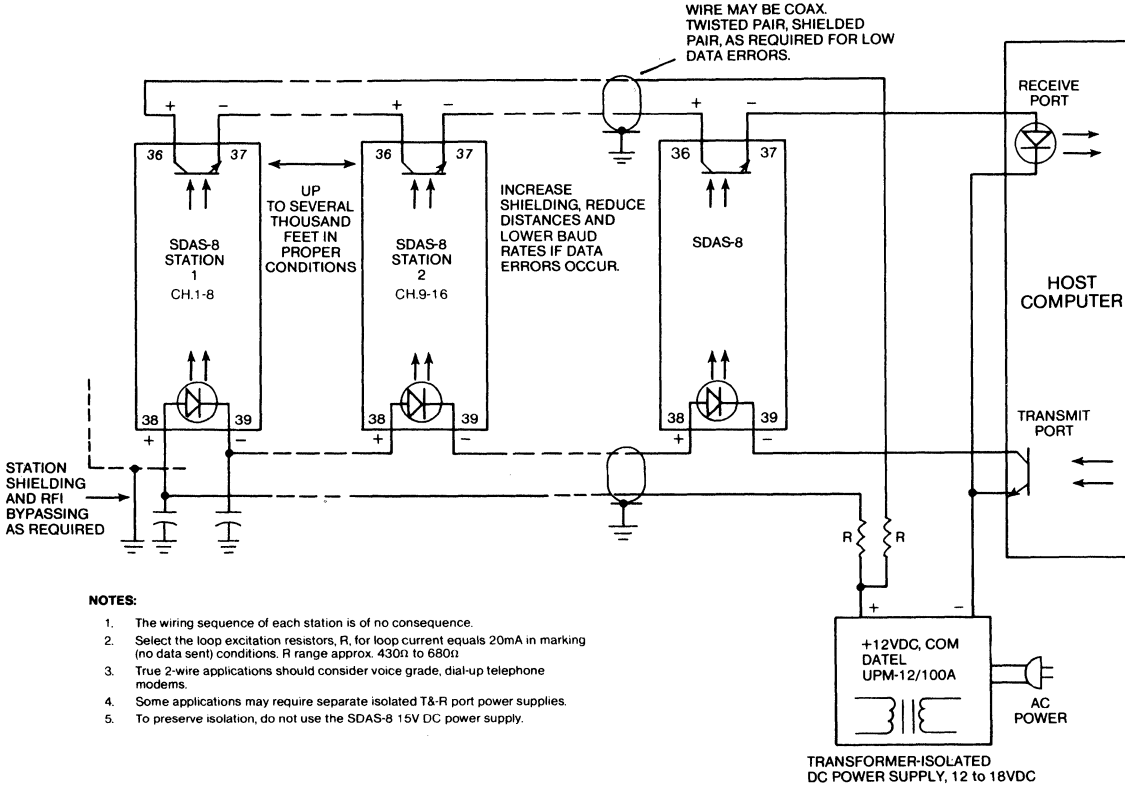
In multidrop applications, separate stations may have differing identification header strings and the station number is always included at the end of the clock line.

Self start auto scans (L mode) are not allowed in multidrop applications, to avoid data collisions on the host computer's receive port. Locally triggered scan starts are also not advisable in multidrop. Normal multidrop applications should use a polled mode, "4X(CR)" for each station.

Multidrop allows a mix of different gains and transducer types from station to station. Longer distance applications or those demanding only two wires or applications where installing more wires is unsuitable should consider using auto-answer RS-232-C modems and either telephone or radio links.

The serial loop port circuits shown for each SDAS-8 station have been simplified for this drawing. The actual circuits contain some additional protection not shown for miswiring abuse (reverse polarity clamps, current limiters, etc.).

TYPICAL 20mA ISOLATED SERIAL LOOP MULTIDROP WIRING, 4 CONDUCTOR



NOTES:

1. The wiring sequence of each station is of no consequence.
2. Select the loop excitation resistors, R, for loop current equals 20mA in marking (no data sent) conditions. R range approx. 430Ω to 680Ω
3. True 2-wire applications should consider voice grade, dial-up telephone modems.
4. Some applications may require separate isolated T&R port power supplies.
5. To preserve isolation, do not use the SDAS-8 15V DC power supply.

MISCELLANEOUS APPLICATION NOTES

1. The baud rate code is internally stored in the SDAS-8 memory at power-up. To change the baud rate, turn off power first to reload the baud rate code.
2. Since SDAS-8 is a software-based subsystem, excessive electrical noise can introduce data errors or can disable SDAS-8, requiring power down to reset. Use power supplies with larger bypass capacitors to maintain continuous voltage in the presence of power dropouts. This is particularly important for the +5V supply powering the microprocessor and memory. In cases of severe, unavoidable power supply problems, use an external means (relay, microprocessor reset pin, etc.) to remotely reset SDAS-8 by momentarily powering down.

   Similarly, excessive serial data link noise could send characters which affect data integrity. Periodic G status code tests by the host computer may be recommended.

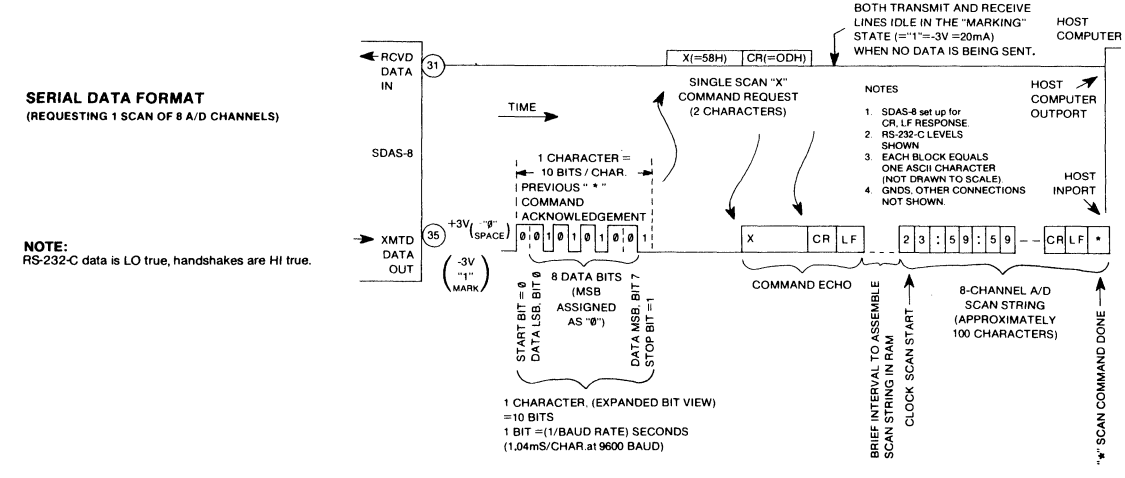
   Sources of high radiation should be avoided to prevent errors in command/control bits. PROM checksum errors will print a warning on power up if they occur.
3. For video terminals, send ESCAPE first after power up to disable the 216 NUL's and reinstate LF's. At low baud rates, ESCAPE is not acknowledged until the * asterisk appears on power-up after many seconds of initial NUL's.
4. Be aware that the analog signal inputs are high impedance differential but are not isolated. Therefore the common mode voltage range can be exceeded. Even with a transformer-isolated AC power supply, the RS-232-C ports are not isolated from the analog section. Use the 20mA isoloop ports if required. Or, external isolation amplifiers such as Datel's AM-227 may be used. Telephone modems also provide some isolation methods.
5. When connecting SDAS-8 to a host computer, the host must have a spare programmable auxiliary RS-232-C serial port which is not connected to the host console device. On some personal computers, the "console" is an internal connection to the keyboard and display. Therefore, the RS-232-C port is truly a spare which is assignable to SDAS-8.

   On some older microcomputers, the RS-232-C port in the CPU is for an external terminal used as a console. An additional RS-232-C port board and driver programs may be required.

   This port must be programmable, either using a terminal emulator program for the computer or as a port with known internal addresses and register formats. The port baud rate and word format may need to be altered and this is usually done with jumpers or switches or with control data loaded into registers or memory addresses.
6. SDAS-8 is intended for DC or slowly-varying inputs such as from transducers. A limited amount of increased data rate may be obtained by suppressing the clock/station and header lines, increasing the baud rate, and requesting only one channel. The A/D converter however continuously overwrites all 8 channels into RAM buffer at 15 samples per second on interrupt basis.
7. Except for the L-mode autoscan, users should write their host control programs to inhibit sending new commands until the previous asterisk (*) command acknowledgement is received.
8. Miscellaneous uses for the Ident/Header string include:
   A. Separation of adjacent records by loading 1 space character in the Ident.

   B. Self-sorting of data from multidrop SDAS-8 clusters on several serial ports to multiple mass storage/disk files. The header string would contain the drive number and file name. For temporary buffering, the header could contain a hex memory location or displacement which could be dynamically incremented with each scan block.

   C. Operator names (locally entered from hand-held terminals), dates, locations, job numbers, batch numbers, reflected (G) status hex codes, calibration data results from previous host computations, system revision levels, driver program information.



SDAS-8 THERMOCOUPLE INPUT

Direct thermocouple inputs may be accepted by SDAS-8 for J, K, S, and T ANSI thermocouple types. Thermocouple measurement requires several data manipulation and signal conditioning factors which are automatically provided by SDAS-8 and some external circuits. Thermocouples require substantial gain since they are millivolt level outputs. The internal SDAS-8 resistor-programmable gain amplifier (PGA) should be selected for a gain of X80 for J, K thermocouples and X160 for S, T thermocouples. These gains require low-drift precision gain resistors listed below which must be mounted close to SDAS-8 to avoid noise errors:

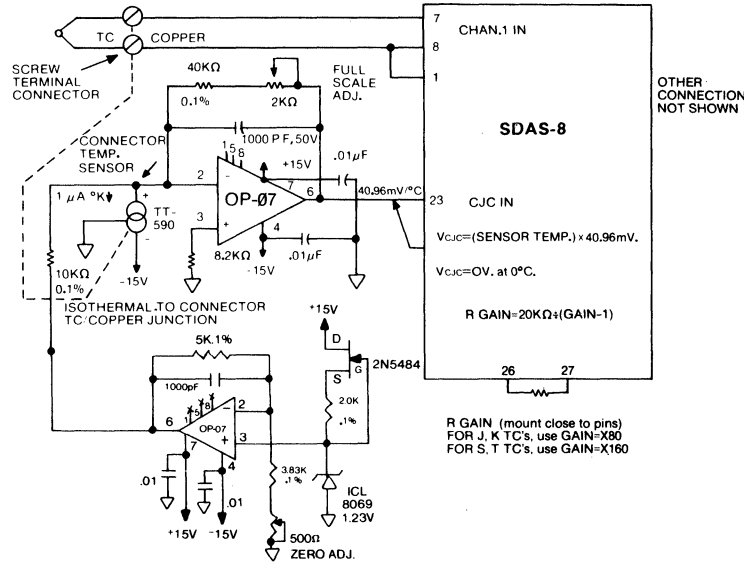
TC	Gain	Gain Resistor*	Temp. Range
J	X80	253.16Ω	−165°C/+760°C
K	X80	253.16Ω	−165°C/+1232°C
S	X160	125.79Ω	0°C/+1768°C
T	X160	125.79Ω	−200°C/+400°C

* The PGA gain resistor is normally developed using a higher value precision metal film or wirewound resistor which is adjusted to final value with a parallel trim resistor.

Thermocouples are nonlinear devices which require linearization correction. In SDAS-8, this is automatically performed in software using a look-up table and linear interpolation algorithm. This function is invoked by sending a J, K, S, or T command first (example: 3K (CR) for station 3, channels 17-24) to SDAS-8. All subsequent analog scans will be linearized to the selected thermocouple. The user may subsequently request offset and scaling to degrees Celcius or Fahrenheit and data formatting to ASCII decimal or ASCII hexadecimal (These are all automatically performed in software by SDAS-8). The thermocouple linearization mode is negated by sending the V (CR) command to revert to dc volts.

Thermocouple connections also require correction for the EMF voltage error which is developed by the two junctions at the screwterminal input connector. On this connector, two thermocouple-to-copper junctions are formed. Since the two thermocouple wires are dissimilar, the EMF voltages developed at the connector are different and this voltage difference changes over temperature. Over a small temperature range, this function is essentially linear. SDAS-8 automatically performs a software correction for this voltage difference error which is called cold junction compensation (CJC). To make this correction however requires temperature measurement of the screw terminal connector. This temperature is converted to a voltage input to a 9th SDAS-8 single-ended channel input (pin 23). The conversion function for this CJC input is V_{CJC} = (Temp. − 0°C) X40.96mV. Simple external circuits and a semiconductor temperature sensor will perform this conversion. This entire CJC function is offered on Datel's ST-705 complete SDAS-8 single-board subsystem. A sample circuit is shown in this brochure. The user may access this CJC channel at any time by sending the A (CR) command (ambient temperature). For non-thermocouple applications, this channel may also be used to measure local equipment temperature as long as a CJC sensor and circuit are connected. In volts mode (V command), a normal scan (X command) ignores any input on the CJC channel.

TYPICAL SDAS-8 COLD JUNCTION COMPENSATION (CJC) EXTERNAL SENSOR CIRCUIT (Included on ST-705)



VFQ-1, VFQ-2, VFQ-3
Low Cost, Monolithic V/F Converters

FEATURES

- **10 kHz to 100 kHz FS**
- **0.01% Maximum linearity at 10 kHz (VFQ-2)**
- **Single- or dual-supply operation**
- **Open collector output**
- **Pulse and square wave outputs**
- **Operates as V/F or F/V**

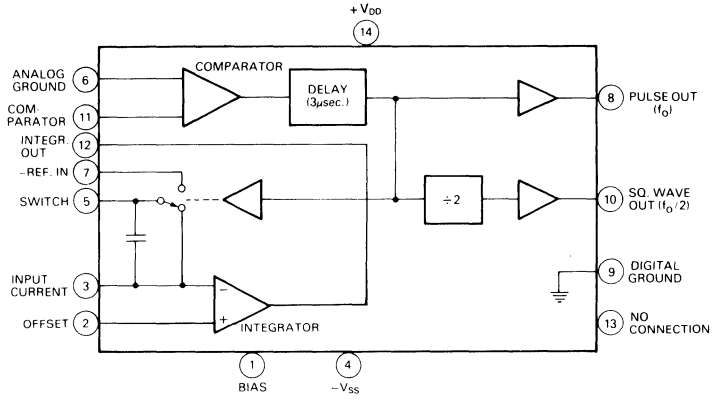
GENERAL DESCRIPTION

DATEL's VFQ series is a family of low-cost, monolithic voltage-to-frequency converters combining bipolar and CMOS technologies. These devices accept a positive analog input current and produce an output pulse train with a frequency linearly proportional to an input current. The full-scale output pulse rate can be set from 10 kHz to 100 kHz by means of two external capacitors.

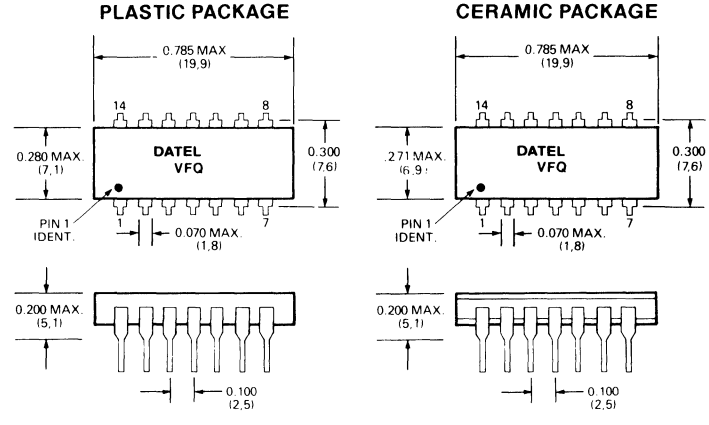
Linearities are specified for both 10 kHz and 100 kHz full-scale outputs. The maximum linearity, at 10 kHz, of the VFQ-1 is 0.05%, while the VFQ-2 has a maximum of 0.01%, and the VFQ-3 has a 0.25% maximum. The linearity holds over the full output range of zero to full scale.

The internal circuitry of these converters includes an operational integrator, a comparator, digital delay circuit, single-pole double-throw electronic switch, a start circuit, a divide by two circuit, and two output driver circuits. Operation is based on the well-known charge balancing integrator principle. The two outputs are open collector NPN which can sink up to 10 mA and give a logical high output up to +18 volts. In normal operation these devices require only five external components and a reference. If the zeroing adjustment is used, a trimming potentiometer and two more resistors are required. The VFQ series can be operated from dual ±4 to ±7.5V supplies or from a single +10V to +15V supply. They may also be operated as frequency-to-voltage converters.

Each model is available in a 14-pin Plastic DIP for 0°C to +70°C operation, with the VFQ-1 also available in a 14-pin Ceramic DIP for −25°C to +85°C operation.



MECHANICAL DIMENSIONS
INCHES (MM)



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ABSOLUTE MAXIMUM RATINGS	VFQ-1	VFQ-2	VFQ-3
Supply Voltage, pin 4 to pin 14	18 Volts	*	*
Input Current, pin 3	±10 mA	*	*
Output Voltage, pins 8 to 10	+25 Volts	*	*
Reference (pin 7) to $-V_{SS}$	±1.5 Volts	*	*

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V supplies, −5V ref., unless otherwise noted.

INPUTS			
Input Current Range	0 to 10 µA	*	*
Input Current Overrange, max.	+50 µA	*	*
Input Offset Voltage, max.[1]	±50 mV	±50 mV	±100 mV
Reference Input	Negative Voltage Within ±1.5V of negative supply		
OUTPUTS			
Type Outputs	Open Collector NPN		
Pulse Output, pin 8	Negative Going, 3 µsec. pulses at f_o		
Square Wave Output, pin 10	Square Wave at $f_o/2$		
Output Logic Levels	V_{OUT} ("0") ≤ +0.4V at −10 mA V_{OUT} ("1") = $+V_{DD}$		
PERFORMANCE			
Linearity, 10 kHz Full-Scale, max.	0.05%	0.01%	0.25%
Linearity, 100 kHz Full-Scale, max.	0.25%	0.08%	0.5%
Gain Tempco, max.	40 ppm/°C	40 ppm/°C	100 ppm/°C
Zero Tempco, max.	50 µV/°C	50 µV/°C	100 µV/°C
Full Scale Accuracy, before trim	±10%	*	*
Output Settling Time, 0.01%	2 Pulses of New Frequency		
SPECIFICATIONS AS F/V			
Nonlinearity, max.[2]	0.05%	0.02%	0.25%
Input Frequency Range	10 Hz to 100 kHz	*	*
Input Voltage, min.	±0.4V	*	*
Input Voltage, max.	−2V to $+V_{DD}$	*	*
Input Pulse Width, Negative pulse, min.	0.5 µsec.	*	*
Input Pulse Width, Positive pulse, min.	5.0 µsec.	*	*
Output Voltage Range[3]	0V to $(+V_{DD}-1)$	*	*
Output Load, min.	2 kΩ		
POWER REQUIREMENTS			
Positive Supply (pin 14)	+4.0V to +7.5V		
Negative Supply (pin 4)	−4.0V to −7.5V		
Quiescent Current, max.[4] VFQ-1C, 2C	±4 mA		
VFQ-1R	±6 mA		
VFQ-3C	±10 mA		
PHYSICAL/ENVIRONMENTAL			
Operating Temperature Range:			
Suffix C	0 °C to +70°C		
Suffix R	−25°C to +85°C		
Storage Temperature Range	−65°C to +150°C		
Package, C Suffix	14 pin Plastic DIP		
Package, R Suffix	14 pin Ceramic DIP		

*Specifications same as VFQ-1.

FOOTNOTES:

1. Before Trimming, $I_{IN} = 0$.
2. 10 Hz to 100 kHz
3. $R_L \geq 2$ kΩ
4. $V_{IN} = -0.1V$

TECHNICAL NOTES

1. To calibrate the VFQ as a V/F converter, connect as shown in the diagrams. Connect a precision voltage source (such as DATEL DVC-8500) to the input resistor. Connect a 5 digit counter, with time base set to one second, to the output (pin 8).

   Zero. Set the voltage reference to +0.01V and adjust the zero adjust potentiometer for an output frequency of 10 Hz (for 10 kHz FS) or 100 Hz (for 100 kHz FS).

   Gain. Assuming the 10V FS input, set the voltage reference to +10.000V and trim the value of R1 to give an output frequency of 10,000 Hz (for 10 kHz FS) or 100,000 Hz (for 100 kHz FS).

2. The two outputs (pins 8 and 10) are open collector NPN transistors for easy interfacing to a variety of standard logic circuits. A pull-up resistor must be used as shown in the diagrams. The resistor may be tied to any voltage up to +18V, which can be separate from +Vdd.

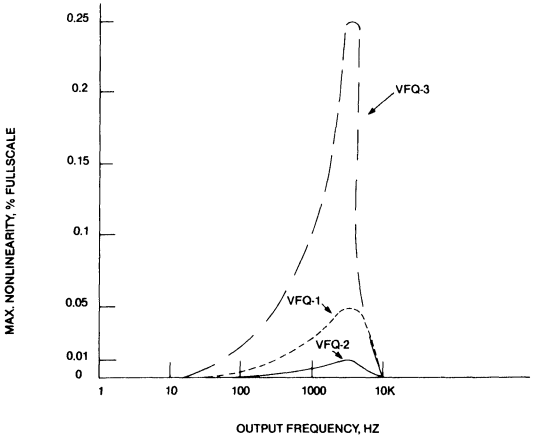
3. Note that the negative reference voltage must be within ±1.5V of the negative supply ($-V_{SS}$). For a given full-scale output frequency the value of C_2 is dependent on the negative reference voltage.

4. Note the minimum-maximum waveform requirements for the input when using the VFQ as a frequency-to-voltage converter. See "Input Waveform Limits" diagram. The minimum ±0.4V must be observed as well as the minimum widths for both positive and negative going portions of the waveform. If the input waveform exceeds the maximum amplitude limits, an input resistor and back-to-back clamping diodes should be used as shown in the connection diagram.

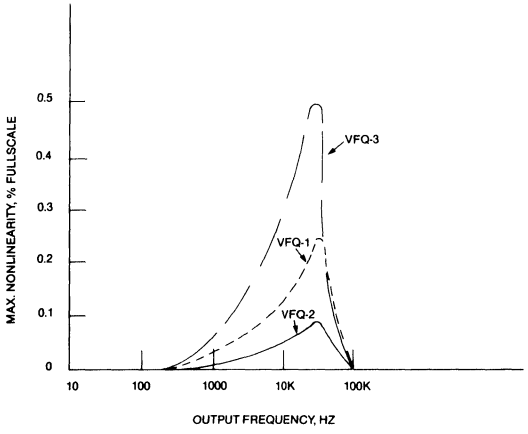
5. For F/V operation, the input signal must cross through zero in order to trip the comparator. In order to overcome the hysteresis the amplitude must be greater than ±200 mV. If only a unipolar input signal (F_{in}) is available, it is recommended that either an offset circuit using resistors be used or that the signal be coupled in via a capacitor.

PERFORMANCE CHARACTERISTICS

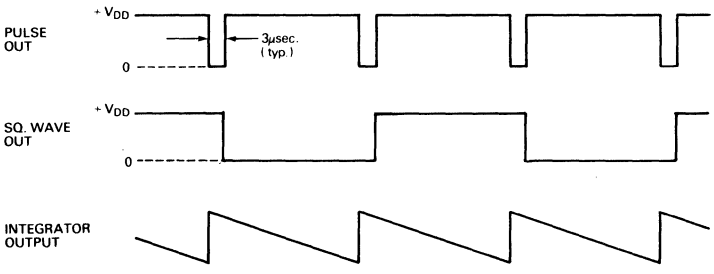
MAX. NONLINEARITY - 10 KHZ FULLSCALE

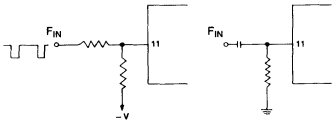


MAX. NONLINEARITY - 100 KHZ FULLSCALE



OUTPUT WAVEFORMS





NOTE:
For F/V operation, if only a unipolar input signal is available, an offset circuit using resistors should be used or the signal should be capacitor coupled.

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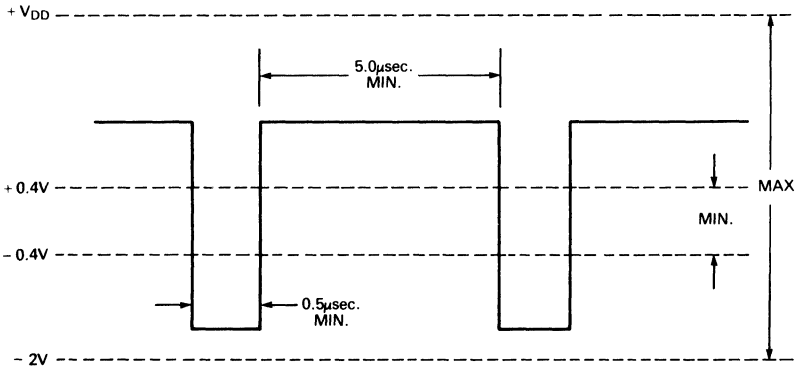
INPUT WAVEFORM LIMITS (F/V CONVERTER)



VFQ FORMULAS

$$f_{OUT} = \frac{V_{IN}}{R_1} \times \frac{1}{V_{REF}\ C_2}$$

$$R_1 = \frac{V_{IN}\ (max.)}{10\mu A}$$

$82K \leq R_2 \leq 120K$

$3C_2 \leq C_1 \leq 10\ C_2$

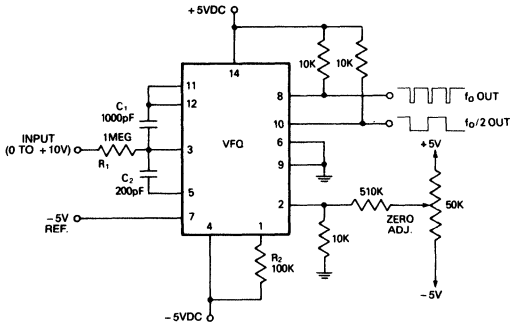
C_1 (optimum) $= 4\ C_2$

F/V CONVERTER
$V_{OUT} = F_{IN}(V_{REF} \times C_2 \times R_1)$

OUTPUT TIME CONSTANT:
$T = R_1\ C_1$

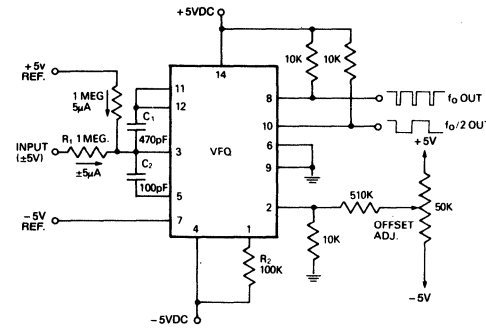
APPLICATION DIAGRAMS

NORMAL CONNECTION—10 kHz FULL SCALE

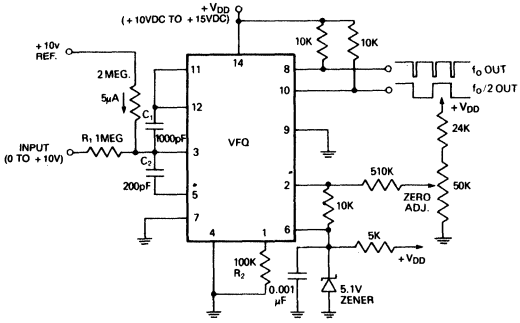


NOTE: FOR 100kHz FULL SCALE, C_1 = 100pF AND C_2 = 20 pF

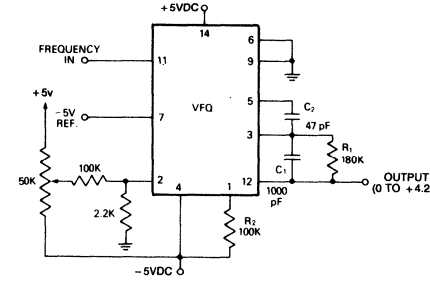
BIPOLAR OPERATION (0 to 20 kHz)



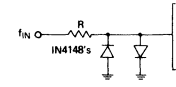
SINGLE SUPPLY OPERATION



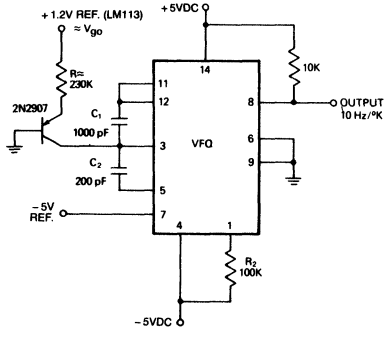
FREQUENCY TO VOLTAGE CONVERTER (0 to 100 kHz INPUT)



NOTE: IF THE AMPLITUDE OF THE INPUT WAVEFORM EXCEEDS THE SPECIFIED MAXIMUM, THE FOLLOWING INPUT CIRCUIT SHOULD BE ADDED



TEMPERATURE TO FREQUENCY CONVERTER



NOTES:

1. V_{go} IS THE EXTRAPOLATED ENERGY-BAND-GAP VOLTAGE FOR SILICON AT 0°K.
2. R IS A STABLE METAL FILM RESISTOR (50 PPM/°C OR BETTER) ITS EXACT VALUE SHOULD BE FOUND BY ADJUSTING IT TO GIVE AN OUTPUT FREQUENCY OF 10 X °K IN HZ FOR A KNOWN TEMPERATURE SUCH AS 300°K. IT WILL THEN BE CORRECTLY CALIBRATED FOR ALL OTHER TEMPERATURES.
3. WHEN PROPERLY IMPLEMENTED THIS CONVERTER IS ACCURATE TO 1°K.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	LINEARITY
VFQ-1C	0°C to +70°C	0.05%
VFQ-1R	−25°C to +85°C	0.05%
VFQ-2C	0°C to +70°C	0.01%
VFQ-3C	0°C to +70°C	0.25%

ACCESSORIES

Part Number	Description
TP50K	Trimming Potentiometer

POWER PRODUCTS

DATEL manufactures a wide range of power supplies for data conversion and general purpose applications. We offer quality products, competitive pricing, and fast delivery. Power Supplies are a major part of DATEL business, not just a convenient sideline.

DATEL's comprehensive line of dc-to-dc converters feature:

1-, 3-, 4.5-, 5-, 10-, and 15-Watt devices
Single, Dual, and Triple Output versions
High Efficiency
Miniature Size
Wide Input Voltage Range Models

DATEL also offers compact modular AC line-operated supplies for circuit board and chassis mounting. Single, Dual, and Triple output versions are available. Included in this line are switching supplies and plug-in power adapters.

Single Output Line Operated Power Modules

SPECIFICATIONS, 25°C	UPM-5/250	UPM-5/500	UPM-5/1000	UPM-5/1000B
Output Voltage	5V dc	5V dc	5V dc	5V dc
Output Voltage Accuracy	±1%	±1%	±1%	±2%
Rated Output Current	250 mA	500 mA	1.0A	1.0A
Line Regulation, max.	0.05%	0.05%	0.05%	0.25%
Load Regulation, max.	0.1%	0.1%	0.1%	0.25%
Temp. Coefficient, max.	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
Output Ripple, RMS max.	1 mV	1 mV	1 mV	1 mV
Output Impedance, max.	0.05Ω	0.05Ω	0.01Ω	0.01Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
Isolation Capacitance, max.	250 pF	250 pF	250 pF	250 pF
Breakdown Voltage, min.	1500 VAC	1500 VAC	1500 VAC	1500 VAC
Operating Temp. Range	−25°C to +71°C (No Derating)			
Storage Temp. Range	−25°C to +85°C			
Case Material	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, Inches	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.25
Module Size, Millimeters	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2	88,9 x 63,5 x 31,8	88,9 x 63,5 x 31,8
Module Weight	14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	18 oz. (510g)
Case/Pin Configuration	C1	C1	C2	C2
Mating Socket	MS-7	MS-7	MS-7	MS-7

FOOTNOTES:

1. For UPM-5/2000 operating temperature range should be restricted for a maximum case temperature of 80°C in use.

This line of single output voltage regulated dc power supplies features five 5 volt output models with output currents from 250 mA to 2 amperes. In addition, there are 4 other models with 6V to 15V outputs. All outputs have current limiting short circuit protection. Temperature coefficients are 0.02%/°C and output ripple voltage is 1 to 2 millivolts RMS.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification:
115 VAC ± 10% at 60–440 Hz

UPM-5/2000	UPM-6/150A	UPM-9/100A	UPM-12/100A	UPM-15/100A
5V dc	6V dc	9V dc	12V dc	15V dc
±1%	±1%	±1%	±1%	±1%
2.0A	150 mA	100 mA	100 mA	100 mA
0.05%	0.05%	0.05%	0.02%	0.02%
0.1%	0.1%	0.1%	0.05%	0.05%
0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
1 mV	1 mV	2 mV	2 mV	2 mV
0.005Ω	0.05Ω	0.01Ω	0.01Ω	0.01Ω
50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
100 Meg.	100 Meg.	100 Meg.	100 Meg.	100 Meg.
250 pF	250 pF	250 pF	250 pF	250 pF
1500 VAC	1500 VAC	1500 VAC	1500 VAC	1500 VAC
①		−25°C to +71°C (No Derating)		
		−25°C to +85°C		
Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
3.5 x 2.5 x 1.56	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875
88,9 x 63,5 x 39,6	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2
24 oz. (680g)	14 oz. (397g)	14 oz. (397g)	14 oz. (397g)	14 oz. (397g)
C3	C1	C1	C1	C1
MS-7	MS-7	MS-7	MS-7	MS-7

Dual Output Line Operated Power Modules

SPECIFICATIONS, 25°C	BPM-5/250	BPM-5/500	BPM-12/60	BPM-12/100
Output Voltage	±5V dc	±5V dc	±12V dc	±12V dc
Output Voltage Accuracy	±1%	±1%	±1%	±2%
Rated Output Current	±250 mA	±500 mA	±60 mA	±100 mA
Line Regulation, max.	0.05%	0.05%	0.02%	0.02%
Load Regulation, max.	0.1%	0.1%	0.05%	0.05%
Temp. Coefficient, max.	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
Output Ripple, RMS max.	1 mV	1 mV	2 mV	2 mV
Output Impedance, max.	0.05Ω	0.03Ω	0.2Ω	0.1Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 MΩ	100 MΩ	100 MΩ	100 MΩ
Isolation Capacitance, max.	250 pF	250 pF	250 pF	250 pF
Breakdown Voltage, min.	1500 VAC	1500 VAC	1500 VAC	1500 VAC
Operating Temp. Range	−25°C to +71°C (No Derating)			
Storage Temp. Range	−25°C to +85°C			
Case Material	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, Inches	3.5 x 2.5 x 0.875	3.5 x 2.5 x 1.25	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875
Module Size, Millimeters	88,9 x 63,5 x 22,2	88,9 x 63,5 x 31,8	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2
Module Weight	14 oz. (397g)	18 oz. (510g)	14 oz. (397g)	14 oz. (397g)
Case/Pin Configuration	C1	C2	C1	C1
Mating Socket	MS-7	MS-7	MS-7	MS-7

FOOTNOTES:

1. For BPM-12/300 and BPM-15/300, operating temperature range should be restricted for maximum case temperature of 80°C in use.

This broad line of dual output, voltage regulated dc Power supplies features 10 different models with a wide choice of output voltages and currents. Output voltages are ±5, ±12, and ±15V dc with ±1% accuracy. Rated output currents range from ±60 to ±500 mA with output short circuit protection.

Temperature coefficient is 0.02%/°C and output ripple voltage is 1 to 2 millivolts RMS.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification:
115 VAC ± 10% at 60–440 Hz

BPM-12/200	BPM-12/300	BPM-15/60	BPM-15/100	BPM-15/200	BPM-15/300
±12V dc	±12V dc	±15V dc	±15V dc	±15V dc	±15V dc
±1%	±1%	±1%	±1%	±1%	±1%
±200 mA	±300 mA	±60 mA	±100 mA	±200 mA	±300 mA
0.02%	0.02%	0.02%	0.02%	0.02%	0.02%
0.05%	0.05%	0.05%	0.05%	0.05%	0.05%
0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
2 mV	2 mV	2 mV	2 mV	2 mV	2 mV
0.05Ω	0.05Ω	0.2Ω	0.1Ω	0.05Ω	0.03Ω
50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
100 MΩ	100 MΩ	100 MΩ	100 MΩ	100 MΩ	100 MΩ
250 pF	250 pF	250 pF	250 pF	250 pF	250 pF
1500 VAC	1500 VAC	1500 VAC	1500 VAC	1500 VAC	1500 VAC
①		−25°C to +71°C (No Derating)			①
		−25°C to +85°C			
Phenolic	Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.56	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.56
88,9 x 63,5 x 31,8	88,9 x 63,5 x 39,6	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2	88,9 x 63,5 x 31,8	88,9 x 63,5 x 39.6
18 oz. (510g)	24 oz. (680g)	14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	24 oz. (680g)
C2	C3	C1	C1	C2	C3
MS-7	MS-7	MS-7	MS-7	MS-7	MS-7

Chassis Mounting Modules

SPECIFICATIONS, 25°C	UCM-5/250	UCM-5/500	UCM-5/1000	UCM-5/1000B
Output Voltage	5V dc	5V dc	5V dc	5V dc
Output Voltage Accuracy	±1%	±1%	±1%	±2%
Rated Output Current	250 mA	500 mA	1.0A	1.0A
Line Regulation, max.	0.05%	0.05%	0.05%	0.25%
Load Regulation, max.	0.1%	0.1%	0.1%	0.025%
Temp. Coefficient, max.	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
Output Ripple, RMS max.	1 mV	1 mV	1 mV	1 mV
Output Impedance, max.	0.05Ω	0.05Ω	0.01Ω	0.01Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 MΩ	100 MΩ	100 MΩ	100 MΩ
Isolation Capacitance, max.	250 pF	250 pF	250 pF	250 pF
Breakdown Voltage, min.	1500 VAC	1500 VAC	1500 VAC	1500 VAC
Operating Temp. Range	−25°C to +71°C (No Derating)			
Storage Temp. Range	−25°C to +85°C			
Case Material	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, Inches	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.25
Module Size, Millimeters	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2	88,9 x 63,5 x 31,8	88,9 x 63,5 x 31,8
Module Weight	14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	18 oz. (510g)
Case/Pin Configuration	D1	D1	D2	D2

FOOTNOTES:

1. For UCM-5/2000 and BCM-15/300, operating temperature range should be restricted for a maximum case temperature of 80°C in use.

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This line of popular power supplies has input-output connections made to a terminal strip on top of the modules. These supplies are useful in applications where it is impractical or undesirable to use printed circuit cards or sockets. For simple mounting to a metal chassis, screw inserts are provided on the bottom of the modules.

All outputs have current limiting short circuit protection.

INPUT VOLTAGE SPECIFICATIONS

Standard input specification:
115 VAC ± 10% at 60–440 Hz

UCM-5/2000	BCM-15/60	BCM-15/100	BCM-15/200	BCM-15/300
5V dc	± 15V dc	± 15V dc	± 15V dc	± 15V dc
± 1%	± 1%	± 1%	± 1%	± 1%
2.0A	± 60 mA	± 100 mA	± 200 mA	± 300 mA
0.05%	0.02%	0.02%	0.02%	0.02%
0.1%	0.05%	0.05%	0.05%	0.05%
0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
1 mV	2 mV	2 mV	2 mV	2 mV
0.005Ω	0.2Ω	0.1Ω	0.05Ω	0.05Ω
50 μsec.	50 μsec.	50 μsec.	50 μsec.	50 μsec.
100 MΩ	100 MΩ	100 MΩ	100 MΩ	100 MΩ
250 pF	250 pF	250 pF	250 pF	250 pF
1500 VAC	1500 VAC	1500 VAC	1500 VAC	1500 VAC
See Footnote 1		–25°C to +71°C (No Derating)		See Footnote 1
		–25°C to +85°C		
Phenolic	Phenolic	Phenolic	Phenolic	Phenolic
3.5 x 2.5 x 1.56	3.5 x 2.5 x 0.875	3.5 x 2.5 x 0.875	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.56
88,9 x 63,5 x 39,6	88,9 x 63,5 x 22,2	88,9 x 63,5 x 22,2	88,9 x 63,5 x 31,8	88,9 x 63,5 x 39,6
24 oz. (680g)	14 oz. (397g)	14 oz. (397g)	18 oz. (510g)	24 oz. (680g)
D3	D1	D1	D2	D3

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Triple Output Modules

These power modules are specially designed for operation with data conversion and other circuits where both a dual analog supply and a 5V logic supply are required. Using a triple output supply to power these circuits can be more economical than using two separate equivalent supplies.

All outputs have current limiting short circuit protection.

INPUT VOLTAGE SPECIFICATIONS

Standard input specifications:
115 VAC ± 10% at 60–440 Hz

SPECIFICATIONS, 25°C	TPM-15/100–5/500 TPM-12/100–5/500	TPM-15/200–5/500 TPM-12/200–5/500	TPM-15/150–5/1000 TPM-12/150–5/1000
Output Voltages, Dual 15V	±15V dc/5V dc	±15V dc/5V dc	±15V dc/5V dc
Output Voltages, Dual 12V	±12V dc/5V dc	±12V dc/5V dc	±12V dc/5Vdc
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current	±100 mA/500 mA	±200 mA/500 mA	±150 mA/1000 mA
Line Regulation, max.	0.02%/0.05%	0.02%/0.05%	0.02%/0.05%
Load Regulation, max.	0.05%/0.1%	0.05%/0.1%	0.05%/0.1%
Temp. Coefficient, max.	0.02%/°C	0.02%/°C	0.02%/°C
Output Ripple, RMS max.	2 mV/1 mV	2 mV/1 mV	2 mV/1 mV
Output Impedance, max.	0.1/0.05Ω	0.1/0.05Ω	0.1/0.05Ω
Trans. Recovery Time, typ.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 MΩ	100 MΩ	100 MΩ
Isolation Capacitance, typ.	250 pF	250 pF	250 pF
Breakdown Voltage	1500 VAC	1500 VAC	1500 VAC
Operating Temp. Range	−25°C to +71°C	−25°C to +71°C	−25°C to +71°C
Storage Temp. Range	−25°C to +85°C	−25°C to +85°C	−25°C to +85°C
Case Material	Phenolic	Phenolic	Phenolic
Module Size, Inches	3.5 x 2.5 x 1.56	3.5 x 2.5 x 1.56	3.5 x 2.5 x 1.56
Module Size, Millimeters	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6
Module Weight	24 oz. (681g)	24 oz. (681g)	24 oz. (681g)
Case/Pin Configuration	E3	E3	E3
Mating Socket	MS-13	MS-13	MS-13

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Modular Switching Supplies

This series of single output, line operated switching power supplies features four different compact modules. Two models are for PC mounting and two models are for chassis mounting. These 5 volt supplies are available in 3 or 5 amp versions with overvoltage protection set at 6.5 volts and are also short circuit protected.

INPUT VOLTAGE SPECIFICATIONS

Standard input specifications:
90 to 130 VAC at 47 to 450 Hz

SPECIFICATIONS, 25°C	USM-5/3	USC-5/3	USM-5/5	USC-5/5
Output Voltage	5V dc	5V dc	5V dc	
Output Voltage Accuracy	±1%	±1%	±1%	±1%
Rated Output Current	3 Amps	3 Amps	5 Amps	5 Amps
Efficiency, typical	80%	80%	80%	80%
Line Regulation, max.	0.05%	0.05%	0.05%	0.05%
Load Regulation, max.	0.1%	0.1%	0.1%	0.1%
Temp. Coefficient, max.	0.02%/°C	0.02%/°C	0.02%/°C	0.02%/°C
Output Ripple, P-P max.	50 mV	50 mV	50 mV	50 mV
Output Impedance, max.	0.001Ω	0.001Ω	0.002Ω	0.002Ω
Trans. Recovery Time, max.	300 μsec.	300 μsec.	300 μsec.	300 μsec.
Isolation Resistance, min.	50 MΩ	50 MΩ	50 MΩ	50 MΩ
Isolation Capacitance, max.	100 pF	100 pF	100 pF	100 pF
Breakdown Voltage, min.	1000 VAC	1000 VAC	1000 VAC	1000 VAC
Operating Temp. Range		−25°C to +71°C		
Storage Temp. Range		−25°C to +85°C		
Case Material	Phenolic	Phenolic	Phenolic	Phenolic
Module Size, Inches	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.25	3.5 x 2.5 x 1.25
Module Size, Millimeters	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6
Module Weight	24 oz. (680g)	24 oz. (680g)	24 oz. (680g)	24 oz. (680g)
Case/Pin Configuration	C2	H	C2	H
Mating Socket	MS-7	—	MS-7	—

FOOTNOTE:
For the USC/USM-5/5 only — derate 60 mA/°C from 50°C to 71°C

DATEL

High Voltage Modules

This series of dual high voltage supplies is specially designed for use with high voltage operational amplifiers such as DATEL's AM-300 series. The 3 supplies in this series offer output voltages of ±120, ±150, and ±180 volts with excellent regulation, stability, and low output ripple. All outputs have current limiting short circuit protection.

INPUT VOLTAGE SPECIFICATIONS

Standard input specifications:
115 VAC ±10% at 60–550 Hz.

SPECIFICATIONS, 25°C	BPM-120/25	BPM-150/20	BPM-180/16
Output Voltage	±120V dc	±150V dc	±180V dc
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current	20 mA	20 mA	16 mA
Line Regulation, max.	0.05%	0.05%	0.05%
Load Regulation, max.	0.2%	0.2%	0.2%
Temp. Coefficient, max.	0.02%/°C	0.02%/°C	0.02%/°C
Output Ripple, RMS max.	10 mV	10 mV	10 mV
Output Impedance, max.	5Ω	5Ω	5Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.
Isolation Resistance, min.	100 MΩ	100 MΩ	100 MΩ
Isolation Capacitance, max.	250 pF	250 pF	250 pF
Breakdown Voltage, min.	1500 VAC	1500 VAC	1500 VAC
Operating Temp. Range	−25°C to +71°C (No Derating)		
Storage Temp. Range	−25°C to +85°C		
Case Material	Phenolic	Phenolic	Phenolic
Module Size, Inches	3.5 x 2.5 x 1.56	3.5 x 2.5 x 1.56	3.5 x 2.5 x 1.56
Module Size, Millimeters	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6	88,9 x 63,5 x 39,6
Module Weight	24 oz. (681g)	24 oz. (681g)	24 oz. (681g)
Case/Pin Configuration	C3	C3	C3
Mating Socket	MS-7	MS-7	MS-7

Plug-In Power Adapters

This series of plug-in power adapters consists of 2 different single output regulated supplies. 5V dc at 500 mA, and 12V dc at 200 mA. Both models are packaged in a flame-retardant 2.06 x 2.18 x 1.71 inch compact molded case. These adapters are a direct plug-in to any available AC outlet and offer isolated low-voltage operation. These light-weight miniature modules operate with minimal heat dissipation and use screw-type terminals for the DC output. All adapters are current limited short circuit protected.

SPECIFICATIONS, 25°C	UPA-5/500	UPA-12/200
Input Voltage	115 VAC ±10%	115 VAC ±10%
Input Frequency	60 Hz	60 Hz
Output Voltage	+4.8 to +5.3V dc	+11.5 to +12.5
Rated Output Current	500 mA	200 mA
Line Regulation, max.	0.3% Typical	0.3% Typical
Load Regulation, max.	0.3% Typical	0.3% Typical
Output Ripple, RMS max.	8 mV	8 mV
Breakdown Voltage, min.	1500 VAC	1500 VAC
Operating Temp. Range	-25°C to +71°C	
Storage Temp. Range	-25°C to +85°C	

4.5 Watt dc-to-dc Converters

These miniature, aluminum cased dc-to-dc converters are ideal for applications where mounting space is tight, yet highly regulated ±15V dc is required at up to 150 mA output current. Specifications include voltage accuracy of ±1%, line regulation of 0.05% maximum, load regulation of 0.05% maximum, and tempco of 0.005%/°C. For convenient heat sinking, two 2-56 studs are provided on the bottom of the case. All models have output current limiting protection.

OTHER SPECIFICATIONS

Isolation Resistance, minimum	100 MΩ
Isolation Capacitance, maximum	100 pF
Breakdown Voltage, minimum	300V dc
Operating Temperature Range	−25°C to +71°C
Storage Temperature Range	−55°C to +85°C

SPECIFICATIONS, 25°C	BPM-15/150-D5	BPM-15/150-D24	BPM-15/150-D28
Output Voltage	±15V dc	±15V dc	±15V dc
Output Voltage Accuracy	±1%	±1%	±1%
Rated Output Current[1]	±150 mA	±150 mA	±150 mA
Input Voltage	5V dc	24V dc	28V dc
Input Voltage Tolerance	±0.25V	±3.5V	±4V
Maximum Input Current	1.75A	0.35A	0.3A
Efficiency, Full Load	51%	54%	54%
Line Regulation, max.	0.05%	0.05%	0.05%
Load Regulation, max.	0.05%	0.05%	0.05%
Temp. Coefficient, max.	0.005%/°C	0.005%/°C	0.005%/°C
Output Ripple, RMS max.	1 mV	1 mV	1 mV
Output Impedance, max.	0.05Ω	0.05Ω	0.05Ω
Trans. Recovery Time, max.	50 μsec.	50 μsec.	50 μsec.
Case Material	Aluminum	Aluminum	Aluminum
Module Size, Inches	2.0 x 2.0 x 0.4	2.0 x 2.0 x 0.4	2.0 x 2.0 x 0.4
Module Size, Millimeters	50,8 x 50,8 x 10,2	50,8 x 50,8 x 10,2	50,8 x 50,8 x 10,2
Module Weight	3.0 oz. (85g)	3.0 oz. (85g)	3.0 oz. (85g)
Case/Pin Configuration	B	B	B
Mating Socket	MS-6	MS-6	MS-6

THESE POWER SUPPLIES ARE COVERED BY GSA CONTRACT

FOOTNOTE:

1. Above 35°C (95°F) mounting surface temperature, derate 1.3 mA/°C.

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WIDE INPUT RANGE DC/DC CONVERTERS

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. RANGE	NO LOAD INPUT CURRENT MAX.
SINGLE OUTPUT					
UPS-5/3000-D12	+5V	+3000 mA	12V	9-18V	30 mA
UPS-5/3000-D24	+5V	+3000 mA	24V	18-36V	20 mA
UPS-5/5000-D12	+5V	+5000 mA	12V	9-18V	30 mA
UPS-5/5000-D24	+5V	+5000 mA	24V	18-36V	20 mA
UPS-12/1250-D12	+12V	+1250 mA	12V	9-18V	30 mA
UPS-12/1250-D24	+12V	+1250 mA	24V	18-36V	20 mA
UPS-12/2500-D12	+12V	+2500 mA	12V	9-18V	30 mA
UPS-12/2500-D24	+12V	+2500 mA	24V	18-36V	20 mA
UPS-15/1000-D12	+15V	+1000 mA	12V	9-18V	30 mA
UPS-15/1000-D24	+15V	+1000 mA	24V	18-36V	20 mA
UPS-15/2000-D12	+15V	+2000 mA	12V	9-18V	30 mA
UPS-15/2000-D24	+15V	+2000 mA	24V	18-36V	20 mA
DUAL OUTPUT					
BPS-12/625-D12	±12V	±625 mA	12V	9-18V	25 mA
BPS-12/625-D24	±12V	±625 mA	24V	18-36V	25 mA
BPS-12/1250-D12	±12V	±1250 mA	12V	9-18V	25 mA
BPS-12/1250-D24	±12V	±1250 mA	24V	18-36V	25 mA
BPS-15/500-D12	±15V	±500 mA	12V	9-18V	25 mA
BPS-15/500-D24	±15V	±500 mA	24V	18-36V	25 mA
BPS-15/1000-D12	±15V	±1000 mA	12V	9-18V	25 mA
BPS-15/1000-D24	±15V	±1000 mA	24V	18-36V	25 mA
TRIPLE OUTPUT					
TPS-5/1500-12/310-D12	+5 ±12V	+1500 ±310 mA	12V	9-18V	50 mA
TPS-5/1500-12/310-D24	+5 ±12V	+1500 ±310 mA	24V	18-36V	40 mA
TPS-5/1500-15/250-D12	+5 ±15V	+1500 ±250 mA	12V	9-18V	50 mA
TPS-5/1500-15/250-D24	+5 ±15V	+1500 ±250 mA	24V	18-36V	40 mA
TPS-5/310-5/1500-D12	+12 ±5V	+310 ±1500 mA	12V	9-18V	50 mA
TPS-5/310-5/1500-D24	+12 ±5V	+310 ±1500 mA	24V	18-36V	40 mA

MINIATURE DC/DC CONVERTERS

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT
UPS-12/80-D5	+12V	+80 mA	5V	±10%	90 mA
UPS-15/65-D5	+15V	+65 mA	5V	±10%	90 mA
BPS-12/40-D5	±12V	±40 mA	5V	±10%	90 mA
BPS-15/33-D5	±15V	±33 mA	5V	±10%	90 mA

FULL LOAD INPUT CURRENT MAX.	LINE REG. MAX.	LOAD REG. MAX.	TEMP. COEF.	CASE CONFIG.	CASE SIZE (H x W x L, INCHES/MM)
1700 mA	±0.2%	±1%	0.02%/°C	X	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
810 mA	±0.2%	±1%	0.02%/°C	X	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
2800 mA	±0.2%	±1%	0.02%/°C	Z	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1350 mA	±0.2%	±1%	0.02%/°C	Z	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1600 mA	±0.2%	±1%	0.02%/°C	X	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
780 mA	±0.2%	±1%	0.02%/°C	X	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
3200 mA	±0.2%	±1%	0.02%/°C	Z	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1550 mA	±0.2%	±1%	0.02%/°C	Z	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1600 mA	±0.2%	±1%	0.02%/°C	X	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
780 mA	±0.2%	±1%	0.02%/°C	X	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
3200 mA	±0.2%	±1%	0.02%/°C	Z	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1550 mA	±0.2%	±1%	0.02%/°C	Z	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1520 mA	±0.2%	±1%	0.02%/°C	X1	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
750 mA	±0.2%	±1%	0.02%/°C	X1	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
3050 mA	±0.2%	±1%	0.02%/°C	Z1	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1500 mA	±0.2%	±1%	0.02%/°C	Z1	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1520 mA	±0.2%	±1%	0.02%/°C	X1	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
750 mA	±0.2%	±1%	0.02%/°C	X1	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
3050 mA	±0.2%	±1%	0.02%/°C	Z1	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1500 mA	±0.2%	±1%	0.02%/°C	Z1	0.83 x 2.56 x 4.56 (21.1 x 66.0 x 115.8)
1600 mA	±1%	±5%	0.05%/°C	T	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
780 mA	±1%	±5%	0.05%/°C	T	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
1600 mA	±1%	±5%	0.05%/°C	T	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
780 mA	±1%	±5%	0.05%/°C	T	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
1470 mA	±1%	±5%	0.05%/°C	T	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)
715 mA	±1%	±5%	0.05%/°C	T	0.83 x 2.56 x 3.00 (21.1 x 66.0 x 76.2)

FULL LOAD INPUT CURRENT	LINE REG.	LOAD REG.	TEMP. COEF.	CASE CONFIG.	CASE SIZE (H x W x L, INCHES/MM)
380 mA	±0.3%	±0.4%	0.1%/°C	24 pin DIP	0.40 x 0.80 x 1.25 (10.2 x 20.3 x 31.8)
380 mA	±0.3%	±0.4%	0.1%/°C	24 pin DIP	0.40 x 0.80 x 1.25 (10.2 x 20.3 x 31.8)
380 mA	±0.3%	±0.4%	0.1%/°C	24 pin DIP	0.40 x 0.80 x 1.25 (10.2 x 20.3 x 31.8)
380 mA	±0.3%	±0.4%	0.1%/°C	24 pin DIP	0.40 x 0.80 x 1.25 (10.2 x 20.3 x 31.8)

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1 Watt dc-to-dc Converters

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT MAX.	FULL LOAD INPUT CURRENT MAX.
UPM-5/200-D5	5V	200 mA	5V dc	± 10%	95 mA	400 mA
UPM-5/200-D12	5V	200 mA	12V dc	± 10%	100 mA	220 mA
UPM-5/200-D28	5V	200 mA	28V dc	± 10%	40 mA	100 mA
UPM-12/80-D5	12V	80 mA	5V dc	± 10%	220 mA	500 mA
UPM-12/80-D28	12V	80 mA	28V dc	± 10%	50 mA	100 mA
UPM-24/40-D5	24V	40 mA	5V dc	± 10%	220 mA	500 mA
UPM-24/40-D12	24V	40 mA	12V dc	± 10%	95 mA	210 mA
UPM-28/25-D5	28V	25 mA	5V dc	± 10%	160 mA	400 mA
UPM-28/25-D12	28V	25 mA	12V dc	± 10%	80 mA	180 mA
BPM-12/25-D5	± 12V	25 mA	5V dc	± 10%	150 mA	350 mA
BPM-12/25-D12	± 12V	25 mA	12V dc	± 10%	80 mA	165 mA
BPM-12/25-D28	± 12V	25 mA	28V dc	± 10%	30 mA	65 mA
BPM-15/25-D5	± 15V	25 mA	5V dc	± 10%	160 mA	400 mA
BPM-15/25-D12	± 15V	25 mA	12V dc	± 10%	80 mA	180 mA
BPM-15/25-D28	± 15V	25 mA	28V dc	± 10%	30 mA	80 mA

DATEL

This broad line of dc-to-dc converters features 14 one watt models with single and dual output voltages. Input voltages are 5, 12, and 28V with single outputs of 5, 12, 24, and 28V, and dual outputs of ±12 and ±15V. Output voltage accuracies are ±1% with 0.02%/ °C temperature coefficient. Other features include low output ripple, 100 megohm isolation, and output current limiting.

GENERAL SPECIFICATIONS – ALL MODELS

Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	20 mV pk-pk (2 mV RMS)
Back Ripple Current, max.	5% (3% typ.) of I_{IN}
Capacitive Coupling, max.	50 pF
Breakdown Voltage, min.	300V dc
Transient Recovery Time, max.	50 microseconds
Operating Temperature Range	-20 °C to +71 °C
Storage Temperature Range	-55 °C to +85 °C
Case Material	Diallyl Phthalate
Weight	1.5 ounce (43 grams)

The 1 watt series uses 2 DILS-1 or DILS-2 terminal strips for sockets.

LINE REG. MAX.	LOAD REG. MAX.	TEMP. COEF.	OUTPUT IMPEDANCE	CASE CONFIG.	CASE SIZE (H x W x L, INCHES/MM)
0.05%	0.1%	0.02%/°C	0.07Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.1%	0.02%/°C	0.07Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.1%	0.02%/°C	0.07Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5
0.05%	0.05%	0.02%/°C	0.02Ω	F	1.5 x 2.0 x 0.375/38,1 x 50,8 x 9,5

9

3 Watt dc-to-dc Converters

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT
UPS-5/600-D5	5V	600 mA	5V dc	±10%	125 mA	935 mA
UPS-5/600-D12	5V	600 mA	12V dc	±10%	50 mA	364 mA
UPS-5/600-D28	5V	600 mA	28V dc	±10%	20 mA	135 mA
UPS-12/250-D5	12V	250 mA	5V dc	±10%	140 mA	863 mA
UPS-12/250-D28	12V	250 mA	28V dc	±10%	25 mA	125 mA
UPM-24/125-D12	24V	125 mA	12V dc	±10%	125 mA	530 mA
UPM-28/100-D5	28V	100 mA	5V dc	±10%	300 mA	1350 mA
UPM-28/100-D12	28V	100 mA	12V dc	±10%	125 mA	500 mA
BPS-12/125-D5	±12V	125 mA	5V dc	±10%	130 mA	965 mA
BPS-12/125-D12	±12V	125 mA	12V dc	±10%	55 mA	380 mA
BPS-12/125-D28	±12V	125 mA	28V dc	±10%	25 mA	145 mA
BPS-15/100-D5	±15V	100 mA	5V dc	±10%	135 mA	955 mA
BPS-15/100-D12	±15V	100 mA	12V dc	±10%	55 mA	376 mA
BPS-15/100-D28	±15V	100 mA	28V dc	±10%	25 mA	143 mA

This broad line of dc-to-dc converters features 14 three watt models with single and dual output voltages. Input voltages are 5, 12, and 28V with single outputs of 5, 12, 24, and 28V, and dual outputs of ±12 and ±15V. Output voltage accuracies are ±1% with 0.01%/ °C temperature coeffiecient. Other features include low output ripple and output current limiting.

GENERAL SPECIFICATIONS - ALL MODELS

Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	20 mV pk-pk (2 mV RMS)
Breakdown Voltage, min.	300V dc
Operating Temperature Range	-25 °C to +71 °C
Storage Temperature Range	-55 °C to +85 °C
Case Material	Diallyl Phthalate

The 3 watt series uses 2 DILS-1 or DILS-2 terminal strips for sockets.

LINE REG.	LOAD REG.	TEMP. COEF.	BREAKDOWN VOLTAGE	REFLECTED RIPPLE CURRENT	CASE CONFIG.	CASE SIZE (H x W x L, INCHES/MM)
0.02%	0.04%	0.02%/ °C	500V dc	32 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.04%	0.02%/ °C	500V dc	24 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.04%	0.02%/ °C	500V dc	21 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.04%	0.02%/ °C	500V dc	31 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.04%	0.02%/ °C	500V dc	21 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.05%	0.05%	0.02%/ °C	300V dc	16 mA pk-pk	G1	2.0 x 2.0 x 0.432/50,8 x 50,8 x 11,0
0.05%	0.05%	0.02%/ °C	300V dc	40 mA pk-pk	G1	2.0 x 2.0 x 0.432/50,8 x 50,8 x 11,0
0.05%	0.05%	0.02%/ °C	300V dc	15 mA pk-pk	G1	2.0 x 2.0 x 0.432/50,8 x 50,8 x 11,0
0.02%	0.02%	0.01%/ °C	500V dc	34 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.02%	0.01%/ °C	500V dc	23 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.02%	0.01%/ °C	500V dc	21 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.02%	0.01%/ °C	500V dc	33 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.02%	0.01%/ °C	500V dc	24 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2
0.02%	0.02%	0.01%/ °C	500V dc	21 mA pk-pk	G1	2.0 x 2.0 x 0.40/50,8 x 50,8 x 10,2

5 Watt dc-to-dc Converters

This comprehensive line of higher power dc-to-dc converters features 16 different models with both single and dual outputs. Input voltages are 5, 12, 24, 28, and 48V with single output voltages of 5, 12, 15, 24, and 28V, and dual outputs of ±12 and ±15 volts. Output voltage accuracies are ±1% with 0.02%/°C temperature coefficientsl Other features include low output ripple, 100 megohm isolation, and output current limiting protection.

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT	FULL LOAD INPUT CURRENT MAX.
UPS-5/1000-D12	5V	1000 mA	12V dc	±10%	50 mA	640 mA
UPS-5/1000-D24	5V	1000 mA	24V dc	±10%	25 mA	320 mA
UPS-5/1000-D28	5V	1000 mA	28V dc	±10%	20 mA	275 mA
UPS-12/470-D5	12V	470 mA	5V dc	±10%	500 mA	2000 mA
UPS-12/470-D24	12V	470 mA	24Vdc	±10%	120 mA	415 mA
UPM-24/210-D5	24V	210 mA	5V dc	±10%	500 mA	2000 mA
UPM-24/210-D12	24V	210 mA	12V dc	±10%	200 mA	830 mA
BPS-12/230-D5	±12V	±230	5V dc	±10%	130 mA	1650 mA
BPS-12/230-D12	±12V	±230	12V dc	±10%	55 mA	690 mA
BPS-12/230-D24	±12V	±230	24V dc	±10%	25 mA	340 mA
BPS-12/230-D28	±12V	±230	28V dc	±10%	25 mA	300 mA
BPS-15/190-D5	±15V	±190	5V dc	±10%	135 mA	1700 mA
BPS-15/190-D12	±15V	±190	12V dc	±10%	55 mA	710 mA
BPS-15/190-D24	±15V	±190	24V dc	±10%	30 mA	350 mA
BPS-15/190-D28	±15V	±190	28V dc	±10%	25 mA	300 mA
BPS-15/190-D48	±15V	±190	48V dc	±10%	14 mA	180 mA

GENERAL SPECIFICATIONS – ALL MODELS

Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	50 mV pk-pk (5 mV RMS), 35 mV pk-pk for dual output
Operating Temperature Range	-25 °C to +71 °C
Storage Temperature Range	-55 °C to +85 °C
Case Material	Diallyl Phthalate

The 5 watt series uses 2 DILS-1 or DILS-2 terminal strips for sockets.

LINE REG.	LOAD REG.	TEMP. COEF.	BREAKDOWN VOLTAGE, MIN.	REFLECTED RIPPLE CURRENT, MAX.	CASE CONFIG.	CASE SIZE (H X W X L, INCHES/MM)
0.02%	0.04%	0.02%/ °C	500V dc	54 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.04%	0.02%/ °C	500V dc	22 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.04%	0.02%/ °C	500V dc	22 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.04%	0.02%/ °C	500V dc	61 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.04%	0.02%/ °C	500V dc	25 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.05%	0.1%	0.02%/ °C	300V dc	100 mA pk-pk	G2	2.0 x 2.0 x 0.750/50,8 x 50,8 x 19,1
0.05%	0.1%	0.02%/ °C	300V dc	42 mA pk-pk	G2	2.0 x 2.0 x 0.750/50,8 x 50,8 x 19,1
0.02%	0.02%	0.01%/ °C	500V dc	58 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	24 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	24 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	23 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	60 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	25 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	25 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	24 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2
0.02%	0.02%	0.01%/ °C	500V dc	25 mA pk-pk	G3	2.0 x 2.0 x 0.40/50,8 x 50,8 x10,2

10 Watt dc-to-dc Converters

MODEL	OUTPUT VOLTAGE	OUTPUT CURRENT	INPUT VOLTAGE	INPUT VOLT. TOLERANCE	NO LOAD INPUT CURRENT MAX.	FULL LOAD INPUT CURRENT MAX.
UPS-5/2000-D24	5V	2000 mA	24V dc	22.32 – 26.4V	45 mA	640 mA
UPS-5/2000-D28	5V	2000 mA	28V dc	26.04 – 30.8V	40 mA	550 mA
UPS-5/2000-D48	5V	2000 mA	48V dc	44.64 – 52.8V	20 mA	320 mA
BPM-12/420-D5	±12V	420 mA	5V dc	4.5 – 5.5V	980 mA	4000 mA
BPM-12/420-D12	±12V	420 mA	12V dc	10.8 – 13.2V	340 mA	1530 mA
BPM-12/420-D24	±12V	420 mA	24V dc	21.6 – 26.4V	175 mA	760 mA
BPM-12/420-D28	±12V	420 mA	28V dc	25.2 – 30.8V	130 mA	650 mA
BPM-12/420-D48	±12V	420 mA	48V dc	42 – 54V	120 mA	415 mA
BPS-15/412-D5	±15V	412 mA	5V dc	4.65 – 5.5V	260 mA	3700 mA
BPS-15/412-D12	±15V	412 mA	12V dc	11.16 – 13.2V	110 mA	1590 mA
BPS-15/412-D24	±15V	412 mA	24V dc	21.6 – 26.4V	55 mA	770 mA
BPS-15/412-D28	±15V	412 mA	28V dc	44.64 – 52.8V	45 mA	660 mA

This comprehensive line of higher power dc-to-dc converters features 12 different models with both single and dual outputs. Input voltages are 5, 12, 24, 28, and 48V with single output voltages of 5, 12, 15, 24, and 28V, and dual outputs of ±12 and ±15V. Output voltage accuracies are ±1% with 0.2%/ °C temperature coefficients. Other features include low output ripple, and output current limiting protection.

GENERAL SPECIFICATIONS – ALL MODELS

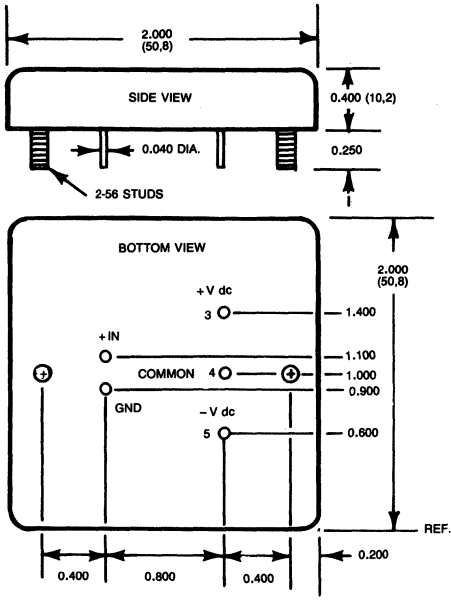
Output Voltage Accuracy	±1%
Output Noise and Ripple, max.	50 mV pk-pk (5 mV RMS)
Operating Temp. Range	-25 °C to +71 °C
Storage Temp. Range	-55 °C to +85 °C
Case Material	Phenolic

The 10 watt series uses the MS-7 socket.

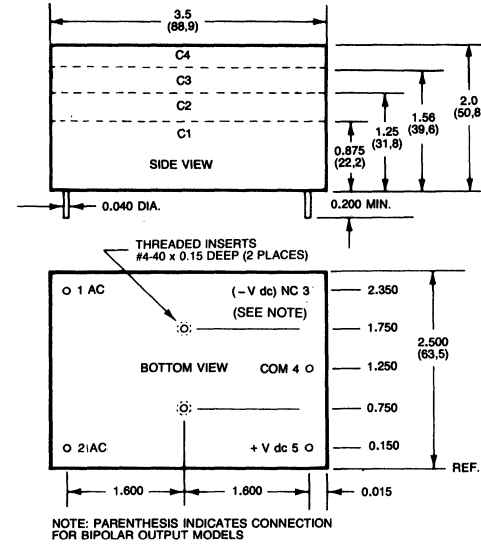
LINE REG. MAX.	LOAD REG. MAX.	TEMP. COEF.	BREAKDOWN VOLTAGE, MIN.	REFLECTED RIPPLE CURRENT	CASE CONFIG.	CASE SIZE (H x W x L, INCHES/MM)
0.02%	0.05%	0.02%/ °C	500V dc	32 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.02%	0.05%	0.02%/ °C	500V dc	33 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.02%	0.05%	0.02%/ °C	500V dc	32 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.05%	0.05%	0.02%/ °C	300V dc	120 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.05%	0.05%	0.02%/ °C	300V dc	46 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.05%	0.05%	0.02%/ °C	300V dc	23 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.05%	0.05%	0.02%/ °C	300V dc	20 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.05%	0.05%	0.02%/ °C	300V dc	13 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.02%	0.02%	0.01%/ °C	500V dc	130 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.02%	0.02%	0.01%/ °C	500V dc	54 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.02%	0.02%	0.01%/ °C	500V dc	38 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2
0.02%	0.02%	0.01%/ °C	500V dc	39 mA pk-pk	CB	3.5 x 2.5 0.875/88,9 x 63,5 x 22,2

Case/Pin Configurations and Sockets

CASE B

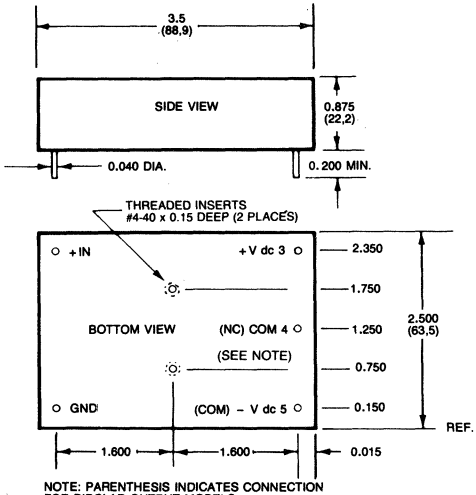


CASE C



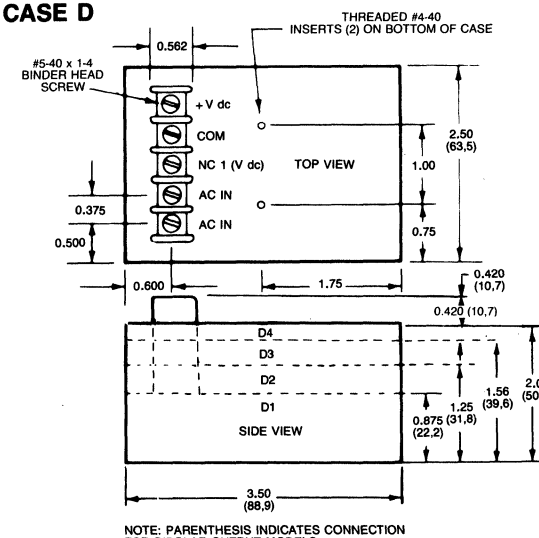
NOTE: PARENTHESIS INDICATES CONNECTION FOR BIPOLAR OUTPUT MODELS

CASE CB



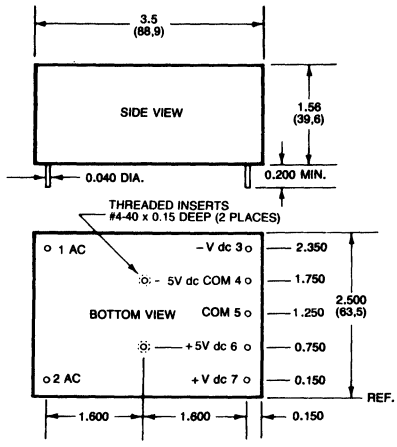
NOTE: PARENTHESIS INDICATES CONNECTION FOR BIPOLAR OUTPUT MODELS

CASE D

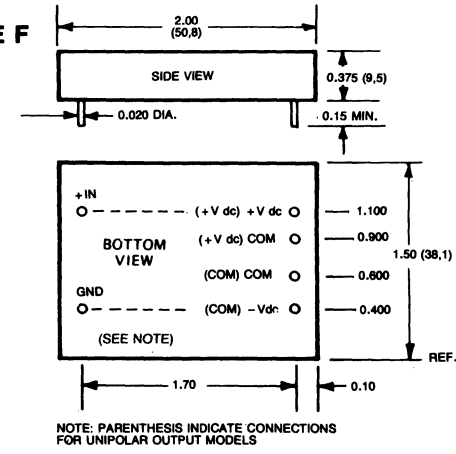


NOTE: PARENTHESIS INDICATES CONNECTION FOR BIPOLAR OUTPUT MODELS

CASE E3

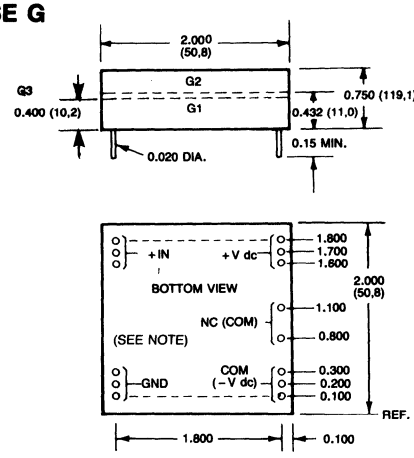


CASE F



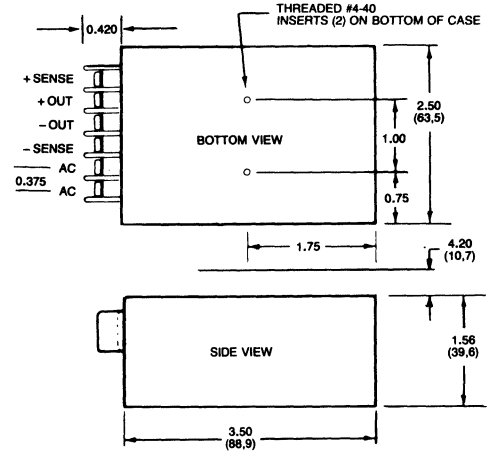
NOTE: PARENTHESIS INDICATE CONNECTIONS FOR UNIPOLAR OUTPUT MODELS

CASE G



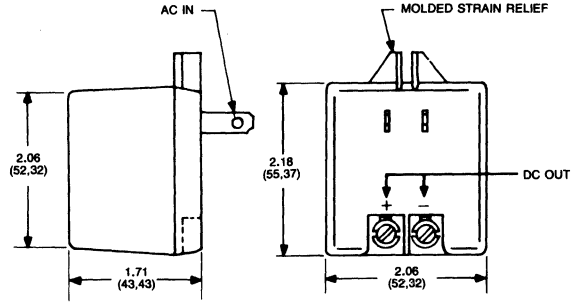
NOTE: PARENTHESIS INDICATE CONNECTIONS FOR BIPOLAR OUTPUT

CASE H

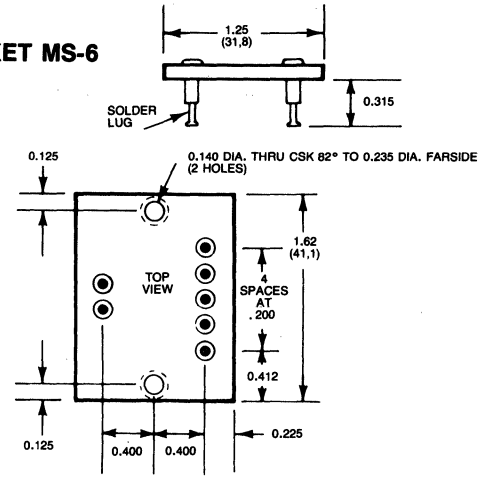


9

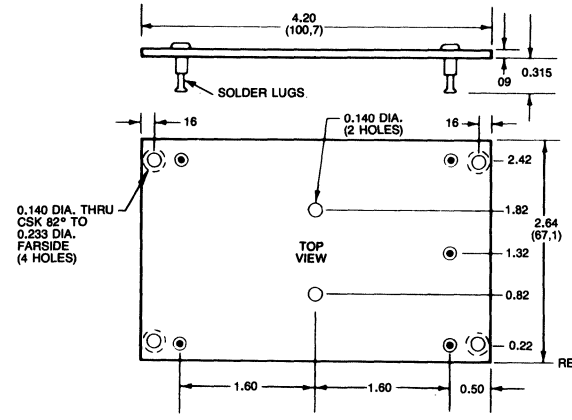
PLUG-IN POWER ADAPTER



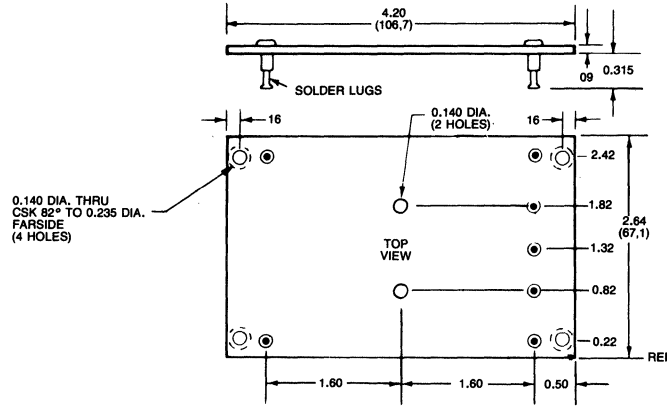
SOCKET MS-6



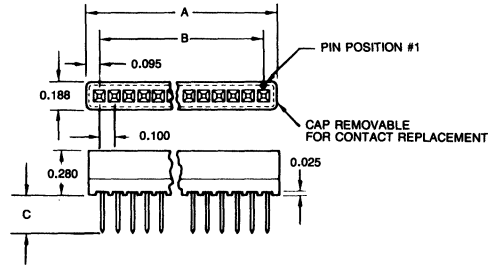
SOCKET MS-7



SOCKET MS-13



SOCKETS DILS-1, DILS-2



Model	No. of Contacts	A	B	C	
DILS-1	20	2.090	1.900	.645	WIRE-WRAP
DILS-2	20	2.090	1.900	.145	SOLDER PIN

Model VI-7660
Monolithic Voltage Converter

FEATURES

- **Easy +5V dc supply conversion to ±5V supplies**
- **Simple voltage multiplication ($V_{OUT} = (-)nV_{IN}$)**
- **99.9% Typical voltage conversion efficiency (RL = ∞)**
- **98% Typical power efficiency**
- **Wide operating voltage range of 1.5V dc to 10.0V dc**
- **Requires only 2 non-critical passive components**

GENERAL DESCRIPTION

The VI-7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The VI-7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V dc to +10.0V dc, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only two non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for $V_{SUPPLY} > 6.5V$ dc.

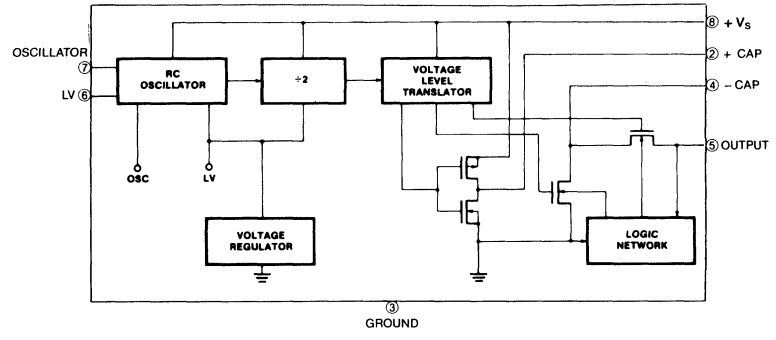
Contained on chip are a series dc power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the OSC terminal, or the oscillator may be overdriven by an external clock.

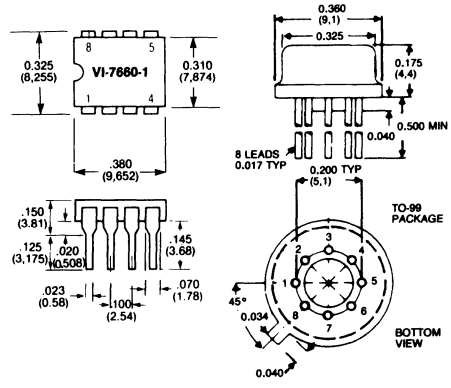
The LV terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latch-up.

Typical applications for the VI-7660 will be data acquisition and microprocessor based systems where there is a +5V dc supply available for the digital functions and an additional −5V dc supply is required for the analog functions. The VI-7660 is also ideally suited for providing low current, −5V dc body bias supply for dynamic RAMs.

The VI-7660 operates over the commercial 0°C to +70°C temperature range. It is available packaged in either an 8-pin TO-99 can or an 8-pin plastic DIP.



MECHANICAL DIMENSIONS INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	N.C.
2	+CAP
3	GROUND
4	−CAP
5	OUTPUT
6	LV
7	OSCILLATOR
8	+Vs (Input)

9

ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltage	10.5V
Input Voltage[1] LV, OSC (Pins 6, 7)	
$V_s > 5.5V$	$-0.3V$ to $(V_s + 0.3V)$
$V_s < 5.5V$	$(+V_s - 5.5V)$ to $(+V_s + 0.3V)$
Input Current LV (Pin 6)	20 μA
Output Short Circuit Duration[2]	Continuous
Power Dissipation: VI-7660-1[3]	300 mW
VI-7660-2	500 mW

FUNCTIONAL SPECIFICATIONS

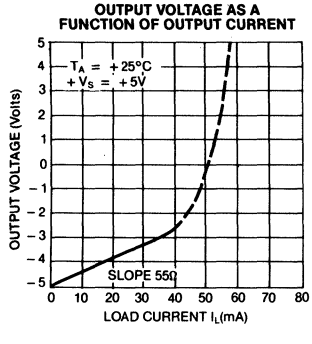
Typical at 25°C, +5V Supply, Cosc = 0, unless otherwise noted.

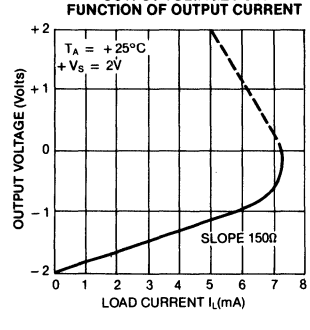
INPUT CHARACTERISTICS	
Supply Current, Max[4]	500 μA
Supply Voltage Range High, min.[5]	3.0V
max.	6.5V
Supply Voltage Range Low, min.[6]	1.5V
max.	3.5V
Supply Voltage Range High, min.[6]	3.0V
max.	10.0V
Supply Voltage Range Low, min.[7]	1.5V
max.	3.5V
PERFORMANCE	
Output Source Resistance, max.[8]	100 Ω
Oscillator Frequency	10 kHz
Voltage Conversion Efficiency, min.	97%
Power Efficiency, min.[9]	95%
Oscillator Impedance, $+V_s = 2V$	1 MΩ
$+V_s = 5V$	100 kΩ
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Soldering Temperature, (10 sec)	300°C

FOOTNOTES:

1. Do not connect any terminal to voltages greater than $+V_s$ or less than ground or destructive latch-up may occur. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the device.
2. For $+V_s$ greater than or equal to 5.5V.
3. Derate linearly above 50°C by 5.5 mW/°C.
4. $R_L = \infty$
5. 0°C to +70°C, R_L = 10 kΩ, LV open and D_x out of circuit.
6. 0°C to +70°C, R_L = 10 kΩ, LV open and D_x in circuit.
7. 0°C to +70°C, R_L = 10 kΩ, LV to ground, D_x in circuit.
8. 0°C to +70°C, R_L = 10 kΩ, LV to ground, D_x out of circuit.
9. Iout = 20 mA. T_A = 25°C. 120Ω max., over 0°C to +70°C. 400Ω max over 0°C to +70°C, $+V_s$ = 2V, Iout = 3 mA, LV to ground.
10. R_L = 5 kΩ.

PERFORMANCE





TECHNICAL NOTES

1. For improved low voltage operation, the "LV" terminal (Pin 6) should be connected to ground (this disables the regulator). For supply voltages greater than 3.5V, the "LV" terminal must be left open to insure latch-up proof operation. Never exceed the maximum rated supply voltage ($+V_S$).
2. The output (Pin 5) should not be shorted to the supply voltage pin (Pin 8) for supply voltages above 5.5V for extended periods of time. However, transient conditions, including start-up are acceptable.
3. If using polarized capacitors for charge pumping and charge reservoir functions, the positive terminal of C1 must be connected to Pin 2 of the VI-7660 and the positive terminal of C2 must be connected to ground. (See typical connection diagrams, page 4.)
4. To operate with voltages up to 10V over temperature without the danger of latch-up, a general purpose diode (D_x) must be added in series with the devices output. The affect of the diode (D_x) is the reduction of output voltage by one diode drop (0.6V).

   D_x must be used in high-voltage elevated temperature applications. The device will function properly in the specified temperature range with only the 2 external capacitors, provided the supply voltage does not exceed 6.5V at 70°C. Exceeding this maximum could result in destructive latch-up of the device. (Refer to the OPERATING VOLTAGE VS TEMPERATURE graph and the typical connection diagrams.)
5. The oscillator operates (unloaded) at a nominal frequency of 10 kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the OSCILLATOR terminal (Pin 7) or the oscillator may be overdriven by an external clock. For large values of the OSCILLATOR CAPACITOR, (>1000 pF), C_1 and C_2 should be increased to 100 μF.

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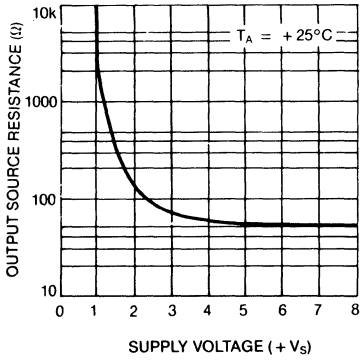
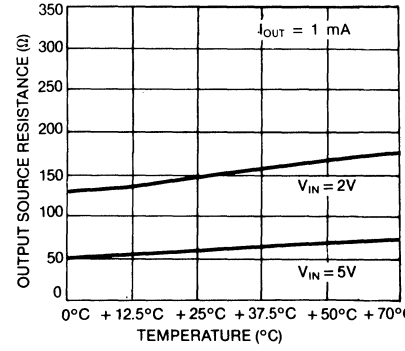
PERFORMANCE

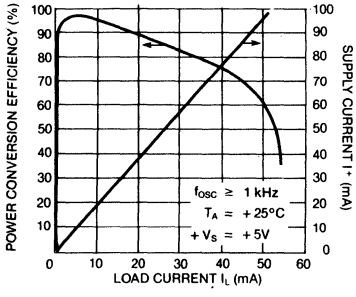
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



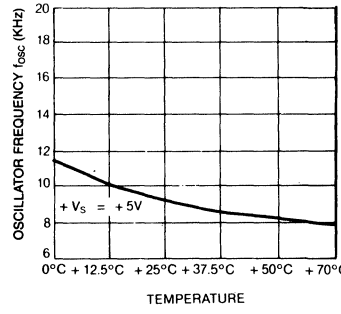
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



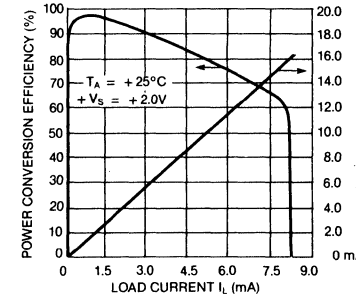
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

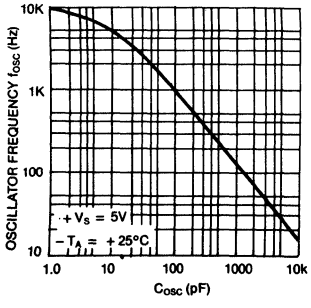


SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

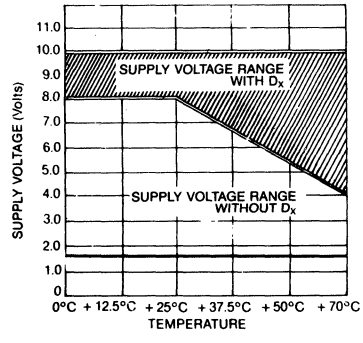


9

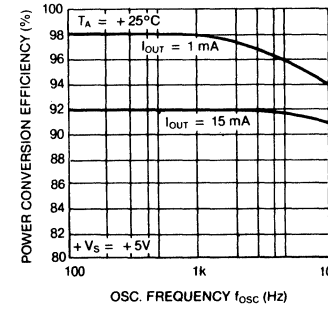
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

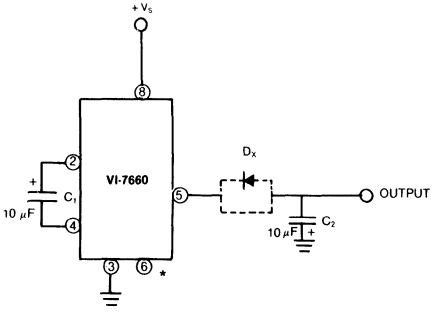


POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



TYPICAL CONNECTION AND APPLICATION

NEGATIVE VOLTAGE CONVERTER



D_x must be included for proper operation at high voltages (>6.5V) and/or elevated temperatures.
*Ground if $+V_S < 3.5V$

This application shows the typical connections to provide a negative supply where a positive supply is available. The output characteristics of this circuit are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of −10 mA and a supply voltage of +5V, the output voltage will be −4.3V. The output equations are as follows:

V_{OUT} without D_x

$$V_{OUT} = -V_S \text{ for } +V_S = 1.5V \text{ to } 6.5V$$

V_{OUT} with D_x

$$V_{OUT} = -V_S + V_{FDX} \text{ for } +V_S = 6.5V \text{ to } 10.0V$$

Where: V_{FDX} = Forward Voltage across D_x

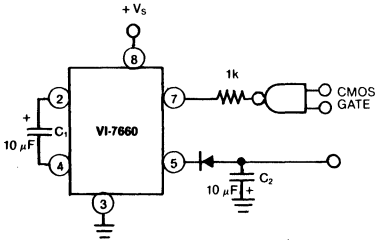
The dynamic output impedance due to the capacitor impedance is approximately $1/\omega C$ where:

$$C = C_1 = C_2$$

Giving $$\frac{1}{\omega C} = \frac{1}{2\Pi f_{osc} \times 10^{-5}} = 3\Omega$$

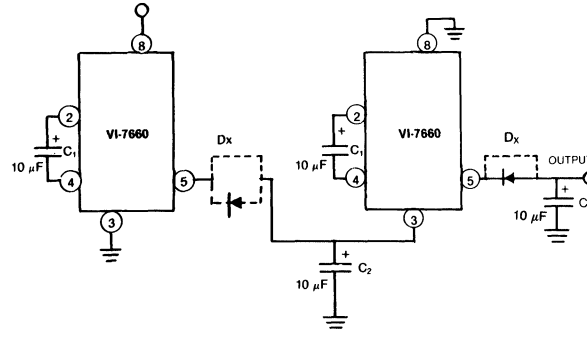
For C = 10 μF and f_{osc} = 5 kHz (½ of oscillator frequency)

EXTERNAL CLOCKING



The oscillator frequency may be increased by overdriving the oscillator from an external clock. The 1 kΩ resistor is used to prevent latch-up when using CMOS logic. If TTL is used to over drive the oscillator, a 10 kΩ pullup resistor to $+V_S$ is required.

CASCADING VI-7660's (ARITHMETIC CASCADING)

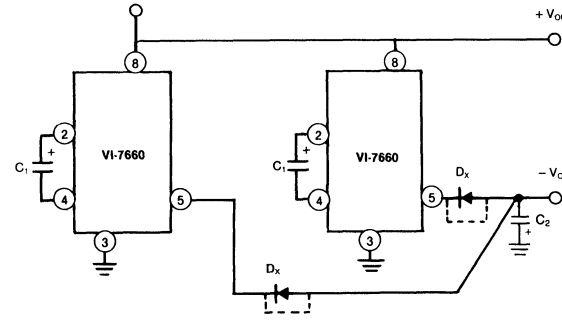


VI-7660's may be cascaded for increased output voltage. The practical limit is 10 devices for light loads due to the finite efficiency of each device. The output equation is as follows:

$$V_{OUT} = -n\,(V_S)$$

where "n" is the number of devices cascaded. The output resistance is the sum of each VI-7660's R_{OUT}.

PARALLELING VI-7660's



VI-7660's may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices; however, each device requires its own pump capacitor (C_1).

$$\text{Output Resistance} = \frac{R_{OUT} \text{ (of VI-7660)}}{\text{n (number of devices)}}$$

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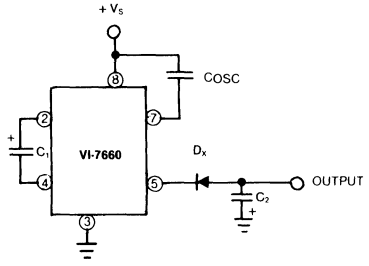
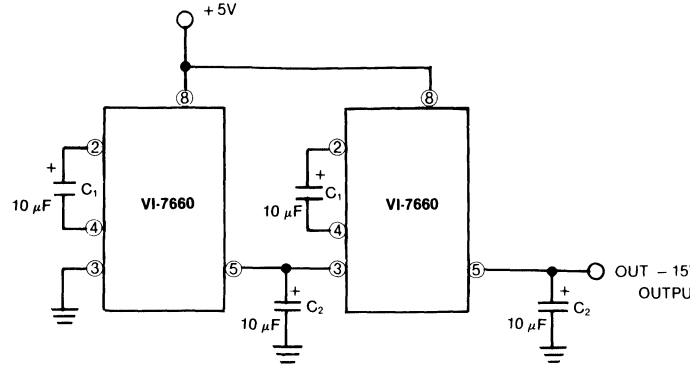
APPLICATIONS

DECREASING OSCILLATOR FREQUENCY



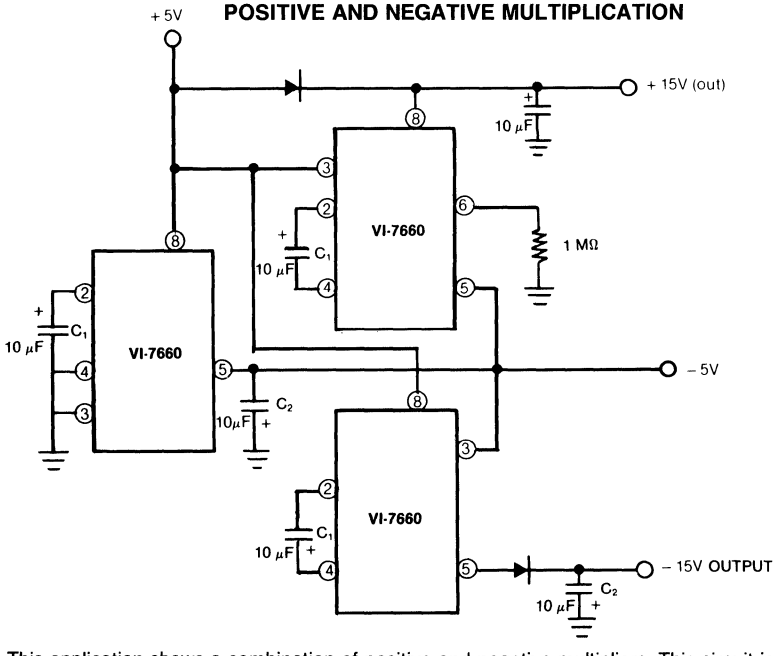
Conversion efficiency can be maximized by lowering the oscillator frequency. This is achieved by connecting an additional capacitor C_{OSC} as shown. Lowering the frequency will cause an increase in the impedance of C_1 and C_2. This can be overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been decreased.

POSITIVE MULTIPLICATION



This circuit will generate –15V dc from +5V dc using two VI-7660's. The two devices are connected in cascade fashion with Pin 3 of device #2 connected to V_{IN} rather than ground. The geometric increase performed by this circuit is good until the input voltage limit is reached, at which point, arithmetic cascading should be utilized. Cascading is recommended for use in light load applications.

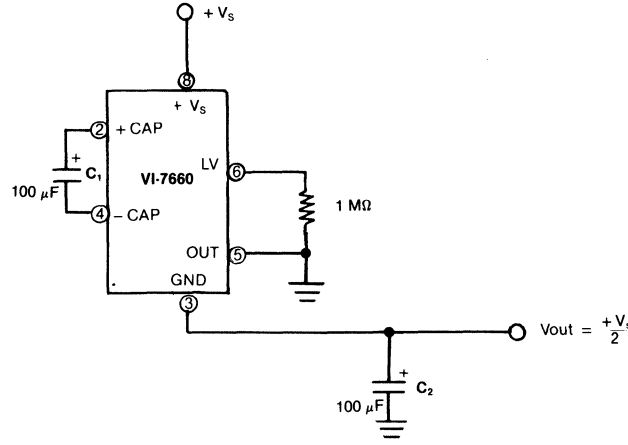
POSITIVE AND NEGATIVE MULTIPLICATION



This application shows a combination of positive and negative multipliers. This circuit is an extension of the above application providing ±15V dc supplies from a +5V dc input. The 1 MΩ resistor on Pin 6 of device number 1 is used to avoid startup problems by forcing the internal regulator on.

9

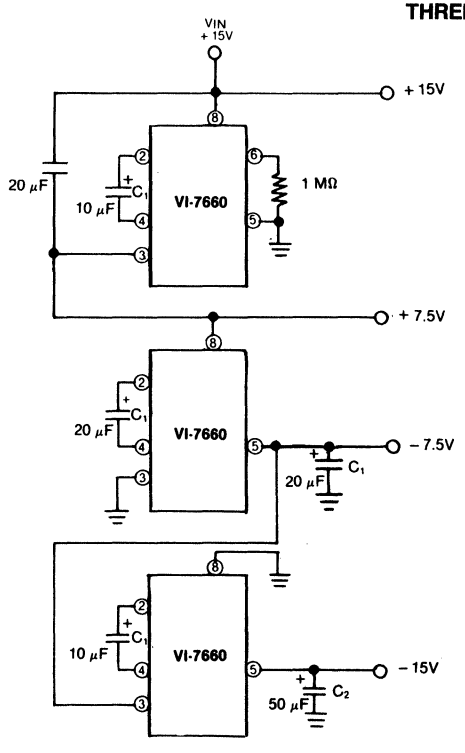
EFFICIENT SUPPLY SPLITTING



In this application, the VI-7660 is connected as a voltage splitter. Note the "normal" output pin is connected to ground and the "normal" ground pin is used as the output. (The switches that allow the charge pumping are bidirectional; therefore, charge transfer can be performed in reverse as well as forward). The 1 MΩ resistor is used to avoid start-up problems by forcing the internal regulator on.

An application for this circuit would be driving low voltage (± 7.5V dc) circuits from ± 15V dc supplies, or low voltage logic from 9V to 12V batteries.

THREE-STAGE +15V TO –15V CONVERSION



The circuit shown here will convert + 15V dc to – 15V dc using three VI-7660's. Device number 1 acts as a voltage splitter. Device number 2 is a voltage converter and device number 3 is configured as a voltage doubler. The output impedance of this circuit is approximately 250Ω.

ORDERING INFORMATION

MODEL NO.	PACKAGE
VI-7660-1	8-PIN PLASTIC DIP
VI-7660-2	8-PIN TO-99

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

VR-182 Series
Precision Bandgap
Voltage References

FEATURES

- **2.455V dc Output**
- **Tempcos to 30 ppm/°C**
- **2-to-120 mA Reference current**
- **±1.4% Tolerance**
- **Two terminals**
- **Low cost**

GENERAL DESCRIPTION

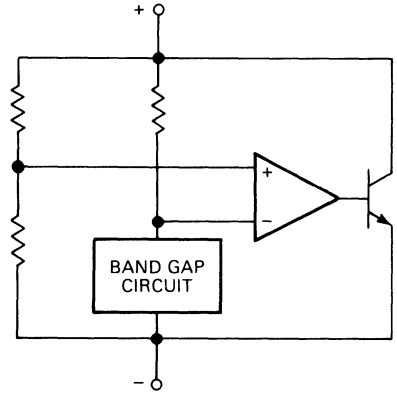
The VR-182 series precision references are two-terminal monolithic bandgap devices which feature 2.455 volts output with tight tolerance and low tempcos. Temperature coefficients are 100, 50, and 30 ppm/°C respectively for Models VR-182A, VR-182B, and VR-182C.

An active regulator around the bandgap circuit results in 0.1 ohm typical dynamic impedance with a wide 2-to-120 mA reference current range. Furthermore, the dynamic impedance is flat to 4 kHz rising to only 1.2 ohms at 50 kHz. Other specifications include ±1.43% voltage tolerance, 10 μV RMS output voltage noise, and 10 ppm per 1000 hours long term stability.

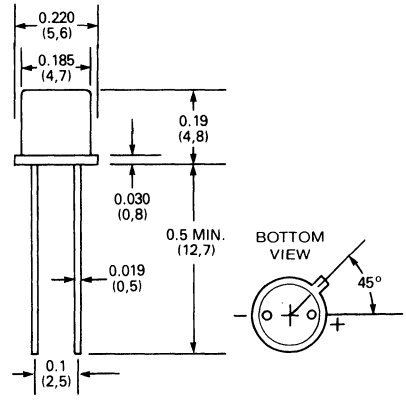
These low cost references are easy to use and are ideal for use with monolithic A/D and D/A converters which do not have internal references. They are also useful in voltage regulator circuits, switching power supplies, comparator circuits, and other analog signal processing applications.

The low 2.455 reference voltage allows these references to be used with 5V dc logic supplies and other power supply voltages as low as 3.5V dc. In many cases they give improved performance over higher priced Zener diode references which require higher supply voltages and have much higher dynamic impedances.

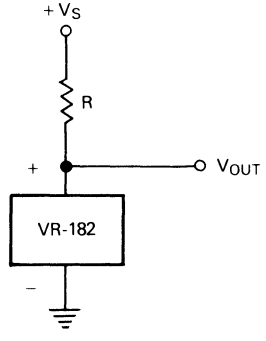
The VR-182 devices are supplied in a two-lead hermetically sealed TO-18 package and operate over the 0°C to +70°C temperature range.



MECHANICAL DIMENSIONS
INCHES (MM)



CONNECTION



9

ABSOLUTE MAXIMUM RATINGS	
Reference Current	120 mA*
Dissipation	300 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, I_{REF} = 2 mA unless otherwise noted.

OUTPUT	
Output Voltage	2.455V
Output Voltage Tolerance, %	±1.43%
Output Voltage Tolerance, mV	±35 mV
PERFORMANCE	
Reference Current Range	2 to 120 mA*
Temperature Coefficient, ppm/°C	
VR-182A	60 typ., 100 max.
VR-182B	35 typ., 50 max.
VR-182C	23 typ., 30 max.
Dynamic Impedance, DC	0.1 typ., 0.2 ohm max.
Dynamic Impedance, 50 kHz	1.2 ohms
Noise Voltage, 1 Hz to 10 Hz	10 μV RMS
Long Term Stability	±10 ppm/1000 hours
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Package Type	2-lead TO-18

*Derate the 120 mA by 1 mA/°C above 25°C

APPLICATION

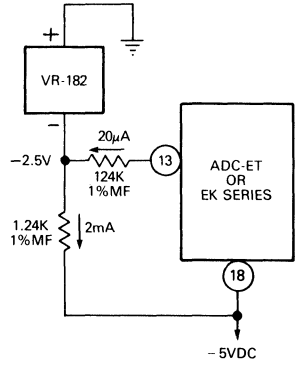
VR-182 series voltage references are recommended for use with the following DATEL products:

A/D Converters	D/A Converters
ADC-EK Series	DAC-08B
ADC-ET Series	DAC-IC8B
	DAC-IC10B

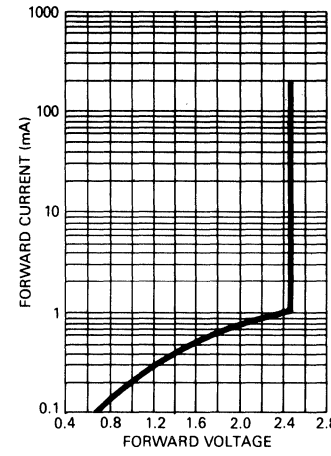
Application Equation: $R = \frac{V_S - 2.455}{I_L + I_R}$

V_S = Supply Voltage
I_R = Reference Current
I_L = Load Current

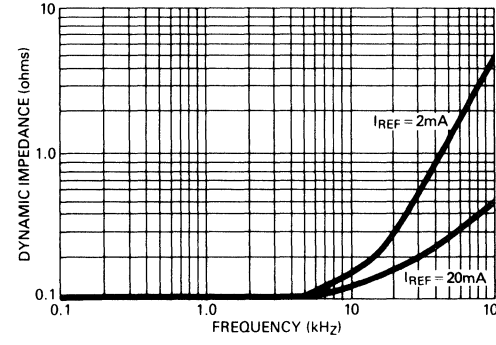
CONNECTION TO DATEL ADC-EK OR ADC-ET SERIES A/D CONVERTERS



FORWARD CHARACTERISTIC



DYNAMIC IMPEDANCE



ORDERING INFORMATION

MODEL	TEMPCO/MAXIMUM
VR-182A	100 ppm/°C
VR-182B	50 ppm/°C
VR-182C	30 ppm/°C

INSTRUMENT PRODUCTS

PANEL MOUNT THERMAL PRINTERS

MODEL	COLUMNS	INPUT INTERFACE	POWER (Note 1)	CHARACTER SET	CASE	SPECIAL FEATURES	PAGE
DPP-Q7	7	BCD	115/230 VAC	Numeric (decimal or hex) plus sign	A	Simple interface to DATEL DPMS	10-32
APP-20A1	20	Parallel	115/230 VAC	96 char ASCII	A	Inverted, tall character options	10-5
APP-20D1	20	Parallel	+12 Vdc	96 char ASCII	A	Inverted, tall character options	10-5
APP-20A21	20	RS-232/20 mA loop	115/230 VAC	96 char ASCII	A	Inverted, tall, condensed character options	10-8
APP-20D21	20	RS-232/20 mA loop	+12 Vdc	96 char ASCII	A	Inverted, tall, condensed character options	10-8
APP-20A3	20	IEEE-488	115/230 VAC	96 char ASCII	A	Inverted, tall character options	10-12
APP-20D3	20	IEEE-488	+12 Vdc	96 char ASCII	A	Inverted, tall character options	10-12
MPP-20A	20	RS-232/Parallel	115 VAC	127 char ASCII	A	Inverted, tall, enhanced character options	10-36
MPP-20D	20	RS-232/Parallel	+12 Vdc	127 char ASCII	A	Inverted, tall, enhanced character options	10-36
MPP-20E	20	RS-232/Parallel	230 VAC	127 char ASCII	A	Inverted, tall, enhanced character options	10-36
APP-48A1	48	Parallel	115 VAC	192 char ASCII	B	Inverted character option	10-15
APP-48D1	48	Parallel	+12 Vdc	192 char ASCII	B	Inverted character option	10-15
APP-48A2	48	RS-232	115/230 VAC	192 char ASCII	B	Inverted character option	10-18
APP-48D2	48	RS-232	+12 Vdc	192 char ASCII	B	Inverted character option	10-18
APP-48A3	48	IEEE-488	115/230 VAC	192 char ASCII	B	Inverted character option	10-22
APP-48D3	48	IEEE-488	+12 Vdc	192 char ASCII	B	Inverted character option	10-22
APP-48A4	48	RS-232	115/230 VAC	192 char ASCII	B	132-character buffer for continuous throughput	10-18
APP-48D4	48	RS-232	+12 Vdc	192 char ASCII	B	132-character buffer for continuous throughput	10-18
APP-M20A1	20	Parallel	115/230 VAC	96 char ASCII	C	Hardened for shock, vibration and humidity (mobile)	10-26
APP-M20D1	20	Parallel	+12 Vdc	96 char ASCII	C		10-26
APP-M20A21	20	RS-232	115/230 VAC	96 char ASCII	C		10-26
APP-M20D21	20	RS-232	+12 Vdc	96 char ASCII	C		10-26
APP-M20A3	20	IEEE-488	115/230 VAC	96 char ASCII	C		10-26
APP-M20D3	20	IEEE-488	+12 Vdc	96 char ASCII	C		10-26
APP-M48D1	48	Parallel	+12 Vdc	192 char ASCII	D		10-28
APP-M48D2	48	RS-232	+12 Vdc	192 char ASCII	D		10-28
APP-M48D3	48	IEEE-488	+12 Vdc	192 char ASCII	D		10-28
APP-M48D4	48	RS-232	+12 Vdc	192 char ASCII	D	Hardened; 132-character buffer for continuous throughput	10-28

NOTE 1: 100 VAC versions available for most models ("J" version); European line cords also available ("E" version). Consult factory.

CASES:

A = 4.44" W x 2.76" H x 8.00" D

B = 8.20" W x 2.84" H x 8.14" D

C = 5.36" W x 3.47" H x 8.00" D (including mobile-mount brackets)

D = 9.25" W x 3.25" H x 10.44" D (including mobile-mount brackets)

PANEL MOUNT DIGITAL PANEL METERS

MODEL	DIGITS	DISLAY	POWER	CASE	DATA I/O	FEATURES	PAGE
DM-500	3 1/2	LED	+5V dc	D	_	Low cost	10-86
DM-3100L	3 1/2	LED	+5V dc	B	_		10-53
DM-3100MIL	3 1/2	LED	+5V dc	B	_	MIL-STD-202 for shock, vibration	10-55
DM-3100N	3 1/2	LED	+5V dc	A	_	Provisions for 4 - 20 mA input	10-57
DM-3101	3 1/2	LED	+5V dc	A	_	High-intensity display	10-57
DM-3103	3 1/2	LED	+5V dc	B	_	High-intensity display	10-53
DM-9100	3 1/2	LED	+5V dc	C	_	Meets NEMA 12 vibration standards	10-89
DM-3100U1	3 1/2	LCD	+5 or +9V dc	A	_	Units display; battery powered operation	10-59
DM-3100X	3 1/2	LCD	+5 or +9V dc	B	_	Battery powered operation	10-63
DM-9150	3 1/2	LCD	+5V dc	C	_	Meets NEMA 12 vibration standards	10-89
DM-3100B	3 1/2	LED	115/230 VAC	B	_		10-51
DM-3100U2	3 1/2	LCD	115 VAC	A	_	Units display	10-61
DM-3100U3	3 1/2	LCD	230 VAC	A	_	Units display	10-61
DM-3104	3 1/2	LED	115/230 VAC	B	_		10-51
DM-9115	3 1/2	LED	115/230 VAC	C	_	Meets NEMA 12 vibration standard	10-89
DM-9165	3 1/2	LCD	115/230 VAC	C	_	Meets NEMA 12 vibration standard	10-89
DM-LX3	3 1/2	LCD	+5V dc	uncased	_	Uncased; battery powered operation	10-95
DM-31	3 1/2	LED	+5V dc	uncased	_	Uncased	10-49
DM-4101N	4 1/2	LED	+5V dc	A	_	High-intensity display	10-76
DM-9200	4 1/2	LED	+5V dc	C	_	Meets NEMA 12 vibration standards	10-89
DM-9250	4 1/2	LCD	+5V dc	C	_	Meets NEMA 12 vibration standards	10-89
DM-9215	4 1/2	LED	115/230 VAC	C	_	Meets NEMA 12 vibration standards	10-89
DM-9265	4 1/2	LCD	115/230 VAC	C	_	Meets NEMA 12 vibration standards	10-89
DM-3102A	3 1/2	LCD	+5V dc	A	Serial BCD out	Autoranging 200 mV to 200V; units display	10-65
DM-3102B	3 1/2	LCD	+5V dc	A	Serial BCD out	Autoranging 2V to 1000V; units display	10-65
DM-4100D	4 1/2	LED	+5V dc	A	Serial/parallel BCD out	High-speed sampling mode	10-68
DM-4101D	4 1/2	LED	+5V dc	A	Serial/parallel BCD out	High-intensity display	10-71
DM-4101L	4 1/2	LED	+5V dc	B	Serial BCD out		10-74
DM-4105	4 1/2	LCD	+5V dc	A	Serial BCD out	Battery powered operation	10-82
DM-4200	4 1/2	LED	+5V dc	A	Serial BCD out		10-84
DM-4102	4 1/2	LED	+5V dc	A	Serial BCD in	Display-only slave meter	10-78
DM-4103	4 1/2	LED	+5V dc	B	Serial BCD in	Display-only slave meter	10-78
DM-4104	4 1/2	LED	+5V dc	A	Parallel/Serial BCD in	Display-only slave meter	10-80
DM-4106	4 1/2	LCD	+5V dc	A	Serial BCD in	Display-only slave meter	10-78
DBM-20	_	LED	+5V dc	A	TTL out	20-segment analog bar graph display	10-47
PC-6	6	LED	+5V dc	B		10 megahertz counter/event timer	10-106

CASES:

A = 2.53"W x 3.34"D x 0.94" (64 x 85 x 24mm)
B = 3.00"W x 2.15"D x 1.76" (76 x 55 x 45mm)
C = 3.60"W x 3.57"D x 1.67" (91 x 91 x 42mm)
D = 1.89"W x 1.22"D x 0.94" (48 x 31 x 24mm)

PROCESS MONITORS

PM-50 _0-1 _ _ 0 _

INPUTS

- 5 — Thermocouple types J, K, T, S, B, E, N R
- 6 — RTD/Thermistor
- 7 — Strain Gage
- 8 — Voltage/Current

COMMUNICATIONS MODE

- 0 — RS-232-C (Standard)
- 1 — RS-422/485

ANALOG OUTPUT

- 0 — None
- 1 — One output (0-10V/4-20mA)

POWER

- A — 115 VAC
- E — 230 VAC
- J — 100 VAC
- D — ±5V dc

10

VOLTAGE CALIBRATORS

MODEL	OUTPUT RANGE	SETTABLE INCREMENTS	ACCURACY	SOURCE/SINK CURRENT	DISPLAY	POWER	CASE/ MOUNTING	PAGE
DVC-350A	±1.2000 or ±12.000	100 µV or 1 mV	0.015%	20 mA	4 1/2 DIGIT LCD	9V Battery or 115 VAC Adaptor (optional)	5.75 X 3.60 X 1.29 in (146 X 91 X 33 mm) HAND HELD	10-135
DVC-8500	±19.999	1mV	0.005%	25 mA	4 1/2 DIGIT MECHANICAL	100 VAC (J) 115 VAC (A) 230 VAC (E)	5.59 X 2.11 X 5.78 (142 X 54 X 147 mm)	10-142

APP-20A1, D1, E1, J1
Parallel Input 20 Column Thermal Printers

FEATURES

- **Minature 20-column, parallel input, alphanumeric thermal printer includes all interface electronics and power supply**
- **Full 96-character ASCII set, TALL character mode, inverted printing option**
- **Fast 1.1 lines/second; 66 lines/minute**
- **Quiet, inkless, virtually maintenance-free**
- **Light-weight and compact; only 4.25 lbs (AC version), 2.2 lbs (DC version)**
- **Selectable positive/negative true data inputs**
- **Available with dual 115/230 VAC, 100 VAC, or +12V dc power supply**

For a ruggedized version of the APP-20, suitable for mobile applications, see the APP-M20.

GENERAL DESCRIPTION

The APP-20 prints the full ASCII character set of upper and lower case letters, numerals, punctuation, etc. in 20 columns across, 2 5/16" wide (58,6 mm) thermal paper. A dot-line thermal printhead forms 5 x 7 matrix characters which are 0.11 inches (2,8 mm) high. The printing rate is 1.1 lines per second regardless of the number of characters printed and a 150 foot roll of thermal paper prints almost 9,000 lines of data (180,000 characters max.) at 5 lines per inch (2 lines/cm) spacing.

The internal control microprocessor of the APP-20 offers special OEM programming features which would be impossible with a standard mechanical printer. Perhaps the most striking feature is the inverted text printout mode. In this mode, printing appears upside down from the front panel. However, when the paper is torn off and inverted, the last line printed is at the botton as normal text would be. In fact the APP-20 may be mounted with its front panel horizontal (facing upward) for text printing applications. In these applications the APP-20 is a text printer , like a teletypewriter. In the normal front-panel application, the APP-20 prints the last line at the top (Lister mode). This mode is commonly used in printing data logger applications. Since the Text and Lister Modes are pin-selected, users may combine inverted text with normal listings on the same printout.

Other programming features are either data-coded or pin-selected (see specifications). These include double-height characters, single-character printing, form feed, horizontal tab, backspace, delete, and selected data polarity.

Extended-height characters are used for emphasis and may be intermixed on one line with regular height characters. Characters are normally entered as 8-bit TTL parallel asynchronous data to a 20-character line bufffer. However, single characters may be printed one at a time to echo a keyboard.

A form feed (FF) character advances the paper 11 lines to separate adjacent records and a horizontal tab (HT) command indexes input data to print in columns 4, 5, and 15 for tabular data. All data inputs may be selected as positive or negative true logic coding.

The AC power supply used in the APP-20A1 and APP-20E1 is a dual-voltage type (115/230 VAC) so that OEMs need to stock only one version (USA or European line cords are supplied). Power consumption is 5 W at idle and averages 17 W while printing, with an occasional 24 W peak. Also available are 100 VAC and +12V dc versions (J1 and D1).

The APP-20 may be operated at -20°C to +50°C and may be stored at -45°C to +85°C (the paper will begin to darken after several days exposure to temperatures exceeding +60°C).

ORDERING GUIDE

MODEL	DESCRIPTION
APP-20A1	115 VAC Power (jumper-selectable for 230 VAC), USA plug
APP-20E1	230 VAC Power (jumper-selectable for 115 VAC), European plug
APP-20J1	100 VAC Power, USA plug
APP-20D1	+12V dc Power at 1 Amp
APP-TR2A	Automatic take-up reel/Rewind accessory, 115 VAC powered
APP-TR2E	Automatic take-up reel/Rewind accessory, 230 VAC powered
APP-TR2D	Automatic take-up reel/Rewind accessory, +12V dc powered
32-2242572	Box of 10 rolls black image paper
33-8193200	Printer Stand Kit

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless noted)

PRINTOUT

Number of Columns 20

Characters Printed
All upper and lower case ASCII letters, numbers, punctuation and special symbols shown in the ANSI X3.4-1977 specification.

Printing Format 5 columns x 7 row matrix

Character Spacing (Horizontal)
Approx. 9 characters per inch

Line Spacing
Approx. 0.2 inches (5,1 mm). 5 lines per inch (4 dot widths spaced between lines)

Character Size Normal: 0.11"H x 0.07"W
Tall: 0.165"H x 0.07"W

Printing Method
Dot-line, thick-film non-impact ceramic thermal printhead.

Paper Motion
Stepping Motor, Friction Roller, and gear reduction. Paper advance (4 dot widths) occurs automatically after printing. A line may be viewed immediately after printing.

Printing Rate (Max.)
1.1 lines per second regardless of number of printed characters per line.

Data Transfer Rate
2.2 KHz max. for loading one line of 20 characters

Printing Paper
Thermal paper 2.31 inches wide (58,6 mm) with active surface facing away from roll center. Supplied on rolls of 150 feet length (45 m). Approx. 140 feet usable (42 m). Supplied in boxes of 10 rolls, DATEL model number 32-2242572.

Printout Color
Black characters on white paper.

Data Capacity
Approximately 8,400 lines (168,000 characters max.) per 140 feet of paper roll.

Printhead Life
30 million lines typical (random character distribution and usage with DATEL-supplied paper and unmodified printers).

Mechanism Life
5000 hours, typical

Maintenance
Periodic cleaning with isopropyl alcohol of mechanism, printhead and roller is suggested for dirt accumulation depending on operating conditions. Printhead design is self-cleaning.

FRONT PANEL

Power On
Red Light-emitting diode illuminates when power is applied.

Feed
2 position momentary toggle switch. Actuating either up or down advances paper continuously at 2.9 lines/second or 0.6 inches/second (1,5 cm/sec).

End-of-Paper Indicator
Red LED illuminates when approximately one inch of paper remains (printing automatically stops). DATEL thermal paper features a red "paper low" warning stripe on the last six feet of paper.

Housing Latch
Rotating "UNLOCK" knob 1/4 turn counter-clockwise frees mechanism from housing and electronics. Knob is pulled out to replace paper roll. This disconnects power to the mechanism and stops printing.

POWER SUPPLY

Supply Voltage

APP-20A1:	105 to 130 VAC (jumper selectable* for 210 to 260 VAC)
APP-20E1:	210 to 260 VAC (jumper selectable* for 105 to 130 VAC)
APP-20J1:	85 to 105 VAC (jumper selectable* for 170 to 210 VAC)
APP-20D1:	+10.5 to +15V dc

*Jumpers are located in the printer housing and are accessible when the print module assembly is removed

Frequency 47 to 440 Hz

Power Consumption

AC models:	5 W idling, 17 W average while printing
DC models:	200 mA idling, 1 A average while printing

Line Cords
Captive 3-wire line cords approximately 6 feet (2 m) long supplied with grounding plugs for US (A and J models) or European (E models, 2 prong and gnd. shell). D models supplied with line cord terminating in spade lug connectors.

Fuses

A and J models:	1/2 Amp SLO-BLO
E models:	1/4 Amp SLO-BLO
D models:	2 Amp SLO-BLO
Dimensions:	0.25" dia x 1.25" long

3AG type accessible on rear panel

PHYSICAL/ENVIRONMENTAL

Operating Temperature Range
0°C to +50°C

Storage Temperature Range
-25°C to +85°C (Paper darkens above +60°C)

Altitude
0 to 10,000 feet (3000 meters)

Relative humidity
0% to 90% (no condensation)

Acceleration (Non-operating)
±5G, 3 axes, 0 to 50 Hz

Weight

AC models:	4.25 pounds (with paper roll), 1,93 kg
DC models:	2.2 pounds, 1 kg

MECHANICAL

Housing Outline Dimensions
4.44"W x 2.76"H x 8.75"D
(113 x 70 x 222 mm)
Allow an additional 1.5" for connector hood and cable clearance.

Bezel Dimensions
5.25"W x 2.82"H x 0.78"D
(134 mm x 72 mm x 20 mm)

Front Panel Mounting Cutout
4.50"W x 2.78"H
(115 mm x 71 mm)

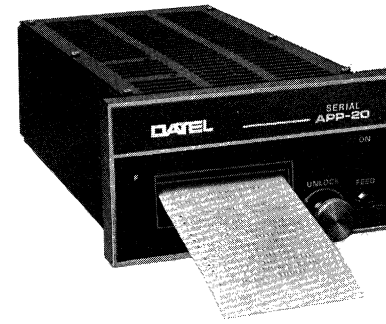
Mounting Method
Using four sets of 4-40 hardware (not supplied) in housing mounting flanges. Mounting bolts are concealed by slideout front panel bezel.

APP-20A21,D21,E21,J21 Serial Input 20-Column Thermal Printers

DATEL

FEATURES

- **Miniature, 20-column serial input alphanumeric thermal printer inlcudes all interface electronics and power supply**
- **RS-232-C and 20 mA current loop compatible**
- **20 mA current loop input is optoisolated to 300 VRMS, 100 Megohms to eliminate ground loop noise; the APP-20 can be located hundreds of feet from the computer**
- **Selectable 75 to 9600 Baud Rates with 9/10/11-bit character lengths**
- **Prints full 96-character ASCII set with TALL and condensed printing modes.**
- **Jumper or logic selectable inverted (TEXT) printing or normal (LISTER) printing**
- **Available with dual 115/230 VAC, 100 VAC, or +12V dc power supply**
- **4.25 LB feather weight (DC version only 2.2 LB). 1.2 lines per second (72 lines per minute) in "Paper Saver" mode**
- **Quiet, inkless, virtually maintenance-free**



For a ruggedized version of the APP-20, suitable for mobile applications, see the APP-M20

GENERAL DESCRIPTION

The APP-20 prints the full ASCII character set of 96 upper and lower case letters, numerals, punctuation, etc. in 20 columns across 2-15/16" (58,6 mm) wide thermal paper. A dot-line thermal print head forms 5 x 7 dot matrix characters which are 0.11 inches (2,8 mm) high. The print rate in "Paper Save" mode is 1.2 lines per second (1/2 height characters continously) regardless of the number of characters printed per line. A 130 foot roll of thermal paper allows almost 16,850 lines to be printed at 10.8 lines per inch (4,2 lines/cm) spacing (in PAPER SAVER MODE).

The internal control microprocessor of the APP-20 offers special printout features which would be impossible with a conventional mechanical printer. One of the most striking features is the inverted text printout mode. In this mode, the printout appears to be upside down with respect to the front panel. However, when the paper is torn off and inverted, the last line printed is at the botton as normal text would be. In fact, the APP-20 may be mounted with its front panel facing upwards for text printing applications. In these applications, the APP-20 is a text printer, like a teleteypewriter. In normal applications, the APP-20 prints the last line at the top (Lister Mode). This mode is commonly used in printing data logger applications. Since the Text and Lister Modes are pin selectable, users may combine inverted text with normal listings on the same printout.

Other programming features are either data-coded or pin selected. These include extended or reduced height characters, form feed, horizontal tab, and backspace.

Extended and reduced height characters are standard. There are four character heights available. They are: Normal (0.115"H x 0.08"W), TALL (0.165"H x 0.08"W), Paper Saver (0.065"H x 0.08"W) and Extended Paper Saver (0.090"H x 0.08"W). Normal and TALL characters can be mixed on the same line, with the TALL characters being used to accent words, phrases or numbers. Paper Saver and Extended Paper Saver character heights can be mixed together on a single lne in the same manner as the TALL and Normal character size combination and achieve the same effect, but because of their reduced height, substantially less paper is used. An additional benefit to reduced character height printing is a slight increase in the print rate and the optical density of the printout. This is particularly useful in printing data logger applications where the printer is left unattended for extended periods of time and running out of paper would be a serious problem.

A form feed (FF) character advances the paper 11 character lines to separate adjacent records, and a horizontal tab (HT) command indexes input data to print in columns 1, 4, 9 and 15 for tabular data.

The AC power supply used in the APP-20A21 and APP-20E21 is a dual-voltage type (115/230 VAC) so that OEM's need to stock only one model (either U.S.A. or European line cords are supplied). Jumper plugs, located internally, select either 115 or 230 VAC, 47 - 400 Hz. They can be accessed when the print module assembly is pulled out of the housing as in the paper loading procedure. Also available are 100 VAC (J21) and +12V dc (D21) versions.

Power consumption is 5 watts at idle and averages 17 watts while printing with an occasional 24 watt peak.

The APP-20 may be operated at -20°C to +50°C and may be stored at -45°C to +85°C. (The paper will begin to darken after several days of exposure to temperatures exceeding +60°C.

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FUNCTIONAL SPECIFICATIONS
(Typical at +25°C unless noted)

PRINTOUT

Number of Columns 20

Characters Printed
All upper and lower case ASCII letters, numbers, punctuation, and special symbols shown in the ANSI X3.4-1977 specification.

Printing Format 5 columns x 7 row dot matrix.

Character Size

Tall	0.165"H x 0.08"W (4,2 x 2 mm)
Normal	0.115"H x 0.08"W (2,9 x 2 mm)
Extended Paper Saver	0.090"H x 0.08"W (2,3 mm x 2 mm)
Paper Saver	0.065"H x 0.08"W (1,7 mm x 2 mm)

Character Spacing (Horizontal)
Approximately 9 characters/in (3,5/cm)

Line Spacing

Tall	0.236" (6 mm) 4.2 lines/inch (1,7 per cm)
Normal	0.185" (4,7 mm) 5.4 lines/inch (2,1 per cm)
Extended Paper Saver	0.118" (3 mm) 8.5 lines/inch (3,3 per cm)
Paper Saver	0.092" (2,4 mm) 10.8 lines/inch (4,25 per cm)

Printing Method
Dot-line, non-impact thermal printhead.

Paper Motion
Stepping Motor, Friction Roller, and Gear Reduction. Paper advance (4 dot lines) occurs automatically after printing. A line is visible immediately after printing.

Print Rates

Tall	0.90 lines/sec. 54 lines/min.
Normal	1.05 lines/sec. 63 lines/min.
Extended Paper Saver	1.00 lines/sec. 60 lines/min.
Paper Saver	1.20 lines/sec. 72 lines/min.

Line Feed Cycle Times

Tall	680 mS
Normal	370 mS
Extended Paper Saver	340 mS
Paper Saver	250 mS

Printing Paper
Thermal paper 2.31 in. (58,6 mm) wide with active surface facing away from roll center. Supplied on rolls 130 feet long (approximately) in boxes of 10 rolls (Datel PIN 32-2242572)

Printout Color
Black printout on white paper.

Data Capacity
Based on a roll length of 130 feet, the approximate data capacities/character size are:

Tall	6,550 lines/130' roll
Normal	8,425 lines/130' roll
Extended Paper Saver	13,260 lines/130' roll
Paper Saver	16,850 lines/130' roll

Note: These figures represent the maximum number of lines/roll for each character size. The mixing of character sizes either on the same line or on a line by line basis will affect the accuracy of these figures.

Printhead Life
30 million lines (random character distribution and usage with DATEL-supplied paper and unmodified printers).

Mechanism Life
5000 hours of actual use minimum.

Maintenance
Periodic cleaning with clinical grade isopropyl alcohol of the printhead and roller is recommended for dirt accumulation depending on operating conditions.

FRONT PANEL CONTROLS AND INDICATORS

Power ON
Yellow light-emitting diode illuminates when power is applied.

End Of Paper
A red light-emitting diode illuminates when the paper supply has one inch remaining, and the printing has stopped. Datel thermal paper features a red "paper low" warning stripe on the last six feet of paper.

Paper Feed/Self-Test Switch
A two position momentary action toggle switch.
To activate the Paper Feed Function, lift the switch lever to the up position and hold it until the desired amount of paper is fed – then release it.
To activate the Self-Test function, depress the switch lever to the down position and release it. The printer will begin printing the full 96 ASCII character set. This will continue until the Self-Test mode is manually cancelled by lifting the toggle switch to the Paper Feed position and holding it there until a blank paper feed occurs, then release it. If Self-Test is invoked again without first removing power from the printer (which will reset the pattern back to the beginning), the pattern displayed will be continued from where it left off previously.

Housing Latch
Rotating "UNLOCK" knob 1/4 counter clockwise frees mechanism from housing and electronics.

POWER SUPPLY

Supply Voltages

APP-20A21:..... 105 to 130 VAC (jumper selectable* for 210-260 VAC)
APP-20E21:..... 210 to 260 VAC (jumper selectable* for 105-130 VAC)
APP-20J21:..... 85 to 105 VAC (jumper selectable* for 170-210 VAC)
APP-20D21:..... +10.5 to +15V dc

*Jumpers are located in the printer housing and are accessible when the print module assembly is removed.

Input Frequency Range 47 to 440 Hz

Power Consumption

AC models..... 5 watts at idle, 17 watts avg. during printing.
DC models..... 360 mA at idle, 1.2 Avg. while printing.

Note: The APP-20D21 (and APP-M20D21) will operate off a typical 3 A (min.) linear regulated general purpose power supply having transient tolerance of 10 A for 10 mS. If the supply is not exclusively for use with the APP-20, a larger unit is required because line disturbances may occur.

Line Cords

AC models..... Captive 3-wire line cord approximately 6 feet (2m) long supplied with grounding plug for US (A and J models) or two prongs and ground shell for European (E and V models).
DC models..... MOLEX® 03-09-1094 housing with MOLEX® 02-09-1118 crimp-on female terminals (sockets).

Fuse

AJ models.....1/2 amp SLO-BLO
E models.....1/4 amp SLO-BLO
D models.....2 amp SLO-BLO
3AG type, dimensions.....0.25" dia. x 1.25" long, mounted on printer housing rear panel.

PHYSICAL/ENVIRONMENTAL

Operating Temperature Range -20°C to +50°C

Storage Temperature Range
-45°C to +85°C (Warning: The paper will begin to darken after several days of exposure to temperatures exceeding +60°C).

Altitude 0 to 10,000 feet (3048 meters)

Relative Humidity 0% to 90% (no condensation)

Acceleration (Non-Operating) +5G, 3 axes, 0 to 50 Hz

Weight

AC models:..... 4.25 lbs (1.9 kg), paper included
DC models:..... 2.2 lbs (1 kg), paper included

Housing Outline Dimensions
4.44"W x 2.76"H x 8.75"D* (113 x 70 x 222 mm)
*Allow an additional 1.5" for connector hood and cable clearance.

Bezel Dimensions
5.25"W x 2.82"H x 0.78"D (134 x 72 x 20 mm)

Front Panel Mounting Cutout
4.50"W x 2.78"H x (115 x 71 mm)

Mounting Method
Using 4 sets of 4-40 hardware in printer housing mounting flanges. Mounting bolts are concealed be the bezel attached to the slide out print module assembly.

Interface Type
Serial asynchronous 20 mA current loop or RS-232-C compatible.

Input Data Rates
The following data rates, which are selectable at the rear connector by either jumpers or TTL logic levels, are supported: 75, 110, 150, 300, 600, 1200, 2400, 4800, 9600.

Word Length
Automatic word length recognition is standard. Word lengths of 9, 10 and 11 bits consisting of the following are supported:

A. 1 Start bit always
B. 7 or 8 data bits
C. Parity or no parity (parity adds 1 bit, no parity adds 0 bits)
D. 1 or 2 stop bits

Note: 8 data and one parity are not allowed.

Data Coding Levels

"1" (MARK)	Current Loop: 20 mA nominal (15 to 25 mA)
	RS-232-C: -3 to -15V
"0" (SPACE)	Current Loop: 0 mA nominal (0 to 0.5 mA) , 2.6 to 2.8V, drop to "1" Isolation: 300 Vrms, 100 Megoms
	RS-232-C: +3 to +15V (refer to EIA spec. for further information)

Input Logic Levels
All connections are compatible with DTL/TTL and TTL-LS levels. CMOS 4049 buffers may also be used. Outputs can drive 2 TTL loads, min.
All logic inputs include internal pullup resistors and may be floated for the positive level, and tied to signal GND (pin 7) for low level. All inputs are level sensitive; risetime is not critical.

Exceptions: Tall character control (pin 8) floats to ground via a 2K ohm resistor. Tall character control (pin 9) has a 1K ohm pullup and may not be driven by type 4049 CMOS.

ORDERING GUIDE

MODEL	DESCRIPTION
APP-20A21	115 VAC powered, (jumper-selectable for 230 VAC) USA type power cord and plug included.
APP-20D21	+10.5 to +15V dc powered, MOLEX® connector and pins included.
APP-20E21	230 /VAC powered, (jumper-selectable for 115 VAC) European power cord included.
APP-20J21	100 VAC powered, USA type power cord included.
APP-M20D21	+10.5 to +15V dc ruggedized mobile printer, including mounting bracket, power cable and printout illuinating lamps.
APP-TR2A	Automatic take-up reel/rewind accessory, 115 VAC powered
APP-TR2E	Automatic take-up reel/rewind accessory, 230 VAC powered
APP-TR2D	Automatic take-up reel/rewind accessory, +12V dc powered
32-2242572	20 column thermal printer paper (10 130' rolls)
33-8193200	Printer stand kit for bench top applications.

APP-20A3,E3,J3,D3
IEEE-488 Bus Compatible 20-Column Thermal Printer

FEATURES

- **Complete 20-column panel-mount printer with IEEE-488 interface and power supply built in**
- **Full 96-character ASCII set, TALL character mode, inverted printing option**
- **Fast 1.1 lines/second**
- **Quiet, inkless, virtually maintenance-free**
- **Light-weight and compact; only 4.25 lbs (AC version), 2.2 lbs (dc version)**
- **Available with dual 115/230 VAC, 100 VAC, or +12V dc power supply**

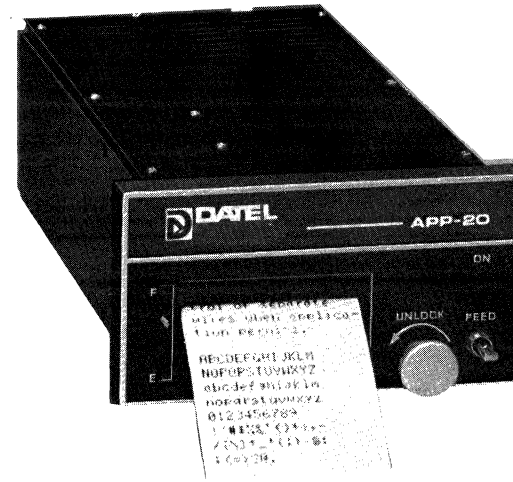
GENERAL DESCRIPTION

The APP-20A3/E3/J3/D3 is a miniature 20-column panel-mount alpha-numeric thermal printer with complete power supply and interface electronics to accept data using the IEE-488 Standard General Purpose Instrument Bus (GPIB). The APP-20 functions as a Listen Only device with its own user-selectable 5-bit My Listen Address (MLA). While sharing a party-line 488 Instrument Bus, unique addressed messages can be sent to only the selected APP-20 or to groupes of remotely-addressed APP-20's.

The APP-20 prints the full ASCII character set of upper and lower case letters, numerals, punctuation, etc. in 20 columns across 2 5/16" wide (58,6 mm) thermal paper. A dot-line thermal printhead forms 5 x 7 matrix characters which are 0.11 inches (2,8 mm) high. The printing rate is 1.1 lines per second regardless of the number of characters printed and a 150 foot roll of thermal paper prints almost 9,000 lines of data (180,000 characters max.) at 5 lines per inch (2 lines/cm) spacing.

The internal control microprocessor of the APP-20 offers special OEM programming features which would be impossible with a conventional mechanical printer. Perhaps the most striking feature is the inverted text printout mode. In this mode, printing appears upside down from the front panel. However, when the paper is torn off and inverted, the last line printed is at the bottom as normal text would be. In fact, the APP-20 may be mounted with its front panel horizontal (facing upward) for text printing applications. In these applications, the APP-20 is a text printer, like a teletypewriter. In the normal front-panel application, the APP-20 prints the last line at the top (Lister mode). This mode is commonly used in printing data logger applications. Since the Text and Lister Modes are pin-selected, users may combine inverted text with normal listings in the same printout.

Other programming features are either data-coded or pin-selected (see specifications). These include double-height characters, single-character printing, form feed, horizontal tab, backspace, delete, and selected data polarity.



Extended-height characters are used for emphasis and may be intermixed on one line with regular height characters.

A form feed (FF) character advances the paper 11 lines to separate adjacent records and a horizontal tab (HT) command indexes input data to print in columns 4, 9, and 15 for tabular data. The AC power supply used in the APP-20A3 and APP-20E3 is a dual voltage type (115/230 VAC) so that OEMs need to stock only one version. Power consumption is 5 watts at idle and averages 17 watts while printing. Also available are 100 VAC and +12V dc models (J3, D3)

The printer may be operated at +10°C to +40°C.

For a ruggedized version of the APP-20, suitable for mobile applications, see the APP-M20.

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FUNCTIONAL SPECIFICATIONS
(Typical at +25°C unless noted)

GENERAL
Function..... The APP-20 prints alphanumeric information on internal roll paper from externally supplied ASCII character codes.

PRINTOUT
Number of Columns....20
Characters Printed.... All upper and lower case ASCII letters, numbers, punctuation and special symbols shown in the ANSI X3. 4-1977 specification.
Printing Format..... 5 columns x 7 row matrix
Character Spacing (Horizontal)..... Approx. 9 characters per inch
Line Spacing..... Approx. 0.2 inches (5,1 mm). 5 lines per inch (4 dot widths spaced between lines)
Character Size
Normal..... 0.11"H x 0.07"W
Tall..... 0.165"H x 0.07"W
Printing Method..... Dot-line, thick-film non-impact ceramic thermal printhead
Paper Motion..... Stepping Motor, Friction Roller, and gear reduction. Paper advance (4 dot widths) occurs automatically after printing. A line may be viewed immediately after printing.
Printing Rate (Max.)..... 1.1 lines per second regardless of number of printed characters per line.
Data Byte Throughput Period
1. All printable characters, 400 microseconds/character max.
2. CR print command or LF, 0.9 seconds typical., 1 second max.
3. FF character, 5 seconds max.

Printing Paper..... Thermal paper 2.31 inches wide (58,6 mm) with active surface facing away from roll center. Supplied on rolls of 150 feet length (45 m). Approx. 140 feet usable (42 m). Supplied in boxes of 10 rolls, DATEL model number 32-2242572
Printout Color..... Black characters on white paper
Data Capacity..... Approximately 8,400 lines (168,000 characters max.) per 140 feet of paper roll
Printhead Life..... 30 million lines typ (random character distribution and usage with DATEL-supplied paper and unmodified printers)
Mechanism Life..... 5,000 hours, typical
Maintenance..... Periodic cleaning with isopropyl alcohol of mechanism, printhead and roller is suggested for dirt accumulation depending on operating conditions. Printhead design is self-cleaning.

FRONT PANEL
Power On..... Red Light-emitting diode illuminates when power is applied
Feed..... 2 position momentary toggle switch. Actuating either up or down advances paper continuously at 2.9 lines/second or 0.6 inches/second (1,5 cm/sec).
End of Paper Indicator..... A red light emitting diode illuminates when the paper supply has one inch remaining. DATEL thermal paper features a red "paper low" warning stripe on the last six feet of paper.
Housing Latch..... Rotating "UNLOCK" knob 1/4 turn counter-clockwise frees mechanism from housing and electronics. Knob is pulled out to replace paper roll. This disconnects power to the mechanism and stops printing.

POWER SUPPLY
Supply Voltage
APP-20A3..... 105 to 130 VAC (jumper selectable* for 210-260 VAC)
APP-20E3..... 210 to 260 VAC (jumper selectable* for 105-130 VAC)
APP-20J3..... 85 to 105 VAC (jumper selectable* for 170-210 VAC)
APP-20D3..... +10.5 to +15V dc
*Jumpers are located in the printer housing and are accessible when the print module assembly is removed
Frequency..... 47 to 440 Hz
Power Consumption
AC models:..... 5 W idling, 17 W average while printing
DC models:..... 200 mA idling, 1 A average while printing
Line Cords..... Captive 3-wire line cords approximately 6 feet (2 m) long supplied with grounding plugs for US (A and J models) or European (E models, 2 prong and ground shell)
Fuses
A and J models:..... 1/2 Amp SLO-BLO
E models: ..... 1/4 Amp SLO-BLO
D models:..... 2 Amp SLO-BLO

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PHYSICAL-ENVIRONMENTAL-MECHANICAL

Operating Temperature Range..... +10°C to +40°C
Storage Temperature Range..... -25°C to +85°C (Paper darkens above +60°C)
Altitude..... 0 to 10,000 feet (3,000 meters)
Relative Humidity..... 0% to 90% (no condensation)
Acceleration (Non-operating)..... ±5G, 3 axes, 0 to 50 Hz
Weight
AC models:.....4.25 lbs (with paper roll), 1,93 kg
DC models:.....2.2 lbs, 1 kg
Dimensions:..... 0.25" dia x 1.25" long 3AG type accessible on rear panel
Housing Outline Dimensions.....4.44"W x 2.76"H x 8.75"D (113 x 70 x 222 mm) Allow an additional 1.5" for connector hood and cable clearance.
Bezel Dimensions..... 5.25"W x 2.82"H x 0.78"D (134 x 72 x 20 mm)
Front Panel Mounting Cutout..... 4.50"W x 2.78"H (115 x 71 mm)
Mounting Method..... Using four sets of 4-40 hardware (not supplied) in housing mounting flanges. Mounting bolts are concealed by slide-out front panel bezel.

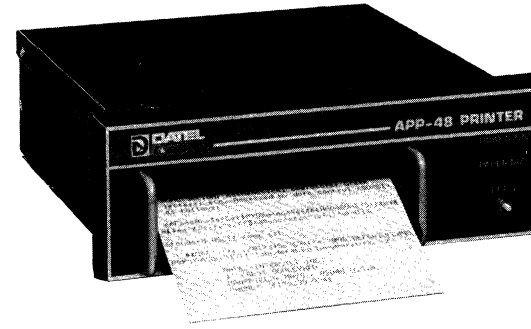
INPUT/OUTPUT CONNECTIONS

Type.....Byte-parallel IEEE-488-1978 General Purpose Instrument Bus
List of Allowable Subsets (see IEEE-488-1978, Appendix C).....SHØ, AH1, TØ, TEØ, L1, LEØ, SRØ, RL2, PPØ, DC1, DTØ, CØ
Drivers.....E1 (open collector)

ORDERING GUIDE

MODEL	DESCRIPTION
APP-20A3	20-column thermal printer, IEEE-488 Interface, 115/230 VAC transformer wired as 115, USA line cord.
APP-20E3	20-column thermal printer, IEEE-488 Interface, 115/230 VAC transformer wired as 230, 2-prong and ground shell line cord.
APP-20J3	20-column thermal printer, IEEE-488 Interface, 100 VAC, USA line cord.
APP-20D3	20-column thermal printer, IEEE-488 Interface, +12V dc power at 1A typ., 6A max. 20 mS.
32-2242572	Box of 10 paper rolls, black image
33-8193200	Printer stand kit for bench-top applications
APP-TR2A	Automatic take-up reel/Rewind accessory, 115 VAC powered
APP-TR2E	Automatic take-up reel/Rewind accessory, 230 VAC powered
APP-TR2D	Automatic take-up reel/Rewind accessory, +5V dc powered

APP-48A1, E1, J1, D1
Byte-Parallel Input 48 Column Thermal Printer



FEATURES

- **Complete 48-column panel-mount printer with byte-parallel Centronics-compatible data electronics and power supply built-in.**
- **Prints full 96-character, upper and lower case ASCII alphanumerics. Includes 2nd 96-character set of special figures, currency symbols, mathematical operators.**
- **Thermal printhead, 5 X 7 dot matrix, few moving parts for OEM reliability. No ink, no ribbons, no hammers, no mess!**
- **Prints inverted text (like a TTY) under data-coded control. Last line printed at bottom of text.**
- **Internal microprocessor includes 1-line, 48-column data register.**
- **6 pound mini–lightweight.**
- **Prints up to 72 lines per minute.**
- **Choice of 100/115/230 VAC or 12V dc power supplies.**

GENERAL DESCRIPTION

The APP-48 A1, E1, D1, J1 series is a miniature, panel-mounting 48-column alphanumeric printer with quiet, inkless thermal printing and complete, internal byte-parallel data electronics and power supply. The 8-bit parallel data signals are directly compatible with the universally-accepted Centronics Interface standard which uses an asynchronous 3-wire handshake.

This interface is ideal for connection to popular microprocessors through Peripheral Interface (PIA/PIO) parallel port LSI integrated circuits. A conventional 25-pin D-connector is mounted on the APP-48 A1's rear panel for connection to a host computer data source.

The APP-48 is designed as a miniature, panel-mounting printing RO data terminal for applications in test and measurement, instrumentation, analytical instruments, diagnostic test systems, custom automatic test equipment and microcomputer development systems.

Besides the 8-bit parallel interface, the APP-48 is also available with full serial RS-232-C/20 mA loop interfaces and a byte-parallel IEEE-488 GPIB interface BUS. DATEL also manufactures a 20-column APP-20 mini-thermal printer with choice of parallel, serial or IEE-488 interfaces. A seven-column numeric full-parallel BCD thermal printer is also available as model DPP-Q7.

The printing technology on the APP-48 uses a quiet OEM-rugged thermal 5 X 7 dot matrix method with no ink ribbons, platens, hammers or ink mess. Only two moving parts are used to provide very long life and high reliability.

For a ruggedized version of the APP-48, suitable for mobile applications, see the APP-M48.

The internal microprocessor controls the data electronics, printhead and motor drivers. Data-coded control characters (STX/ETX) allow inverted printout for text applications so that the last line will appear either at the top or bottom of the printout. Normal data entry uses standard 96-character ASCII-encoded alphanumerics. SO/SI data-coded control characters map the input ASCII coding into a second set of 96 characters stored in a type 2716 Programmable Memory.

The lightweight 6 pound (2,7 kg) APP-48 mounts through a 8.40"W X 2.92"H (213, 4 X 74,2 mm) front panel cutout with four screws. A choice of power supplies are available: 100VAC, 115VAC, 230VAC, or 12V dc. For AC units, power consumption is 40 watts printing, 12 w idle; DC units average 1.5A while printing, 0.7A idle. The operating temperature range is 0 to +50°C.

ORDERING GUIDE

MODEL	DESCRIPTION
APP-48A1	Printer with 115/230 VAC (XfmR, USA line cord, 115V wired.
APP-48-E1	Printer with 115/230 VAC XfmR, European line cord, 230V wired.
APP-48J1	Printer with 100 BAC XfmR, USA line cord.
APP-48D1	Printer with +12VDC Power.
32-2242568	Box of 10 paper rolls, black image.
33-8193205	Printer Stand Kit.
APP-TR5A	Take-up Reel/Rewind Accessory, 115 VAC powered.
APP-TR5E	Take-up Reel/Rewind Accessory, 230 VAC powered.
APP-TR5D	Take-up Reel/Rewind Accessory, +12V dc powered.
58-2079130	Spare Mating DB-25S Connector (1 supplied)

FUNCTIONAL SPECIFICATIONS
(Typical at +25°C unless noted)

PRINTOUT

Number of Columns 48

Characters Printed
96-character set per ANSI X3.4-1977 specification. A second 96-character is accessed by SO/SI control.

Printing Inversion Selectable using STX/ETX control characters (may not be intermixed on the same line)

Printing Format 5 dot columns x 7 dot row matrix per character.

Line Spacing
0.164 inch (4,2 mm) line to line. Approximately 6 lines per inch.

Printout Width (48 columns)
4.77 inches (121,2 mm)

Character Size
0.070"W x 0.110"H (1,8 X 2,8 mm)

Printing Rate
1.2 lines/second maximum. Depends on data loading period and printing period. Data Loading Period equals 110 µS minute per character. Printing period equals 750 mS minute per line.

Printing Paper
Thermal paper 5 inches (127 mm) wide by 150 foot (45 m) rolls. A red stripe appears when approximately 10 feet of paper remain. User-supplied paper must detach from the roll.

Data Capacity
Approximately 11,000 lines in 150 feet usable per roll.

Printhead Life
30 million characters with random data and DATEL-supplied paper.

Mechanism Life
5000 hours in non-hostile applications.

DATA CODED FUNCTIONS

Character	Meaning	Hex Code
Nul	Null, ignored	ØØ
BS	Backspace, delete previous character, decrement column address counter toward the left	Ø8
SO	Map input data to 2nd 96-character set, mixable within a line.	ØE
SI	Reset to normal ASCII character set, mixable within a line.	ØF
STX	Change to inverted (text) printing. Not mixable within a line.	Ø2
ETX	Change to non-inverted (lister) printing. Not mixable within a line.	Ø3
HT	Tab successively to columns 9, 17, 25, 33.	Ø9
LF	Feed one line, no print, no data register change.	ØA
FF	Advance 11 lines, no register change.	ØC
CR	Print register contents, advanceone line, clear register. Requires 750 mS during which input data may not be loaded. LF is not required LF will be ignored in the sequence CR, LF. Loading of 48 characters and/or spaces will automatically start printing.	ØD
DEL	Decrement column address to the left, clear that data register, load a rubout obliteration pattern and increment column address to the right.	7F

NOTE: Data is loaded starting at the left margin.

POWER SUPPLY

Required Power

APP-48A1..... 105 to 130 VAC @ 47 to 440 Hz, jumper-selectable* for 210 to 250 VAC. Includes USA-style power cord.

APP-48E1..... 210 to 250 VAC @ 47 to 440 Hz, jumper-selectable* for 105 to 130 VAC. Includes European-style power cord.

APP-48J1..... 100 VAC @ 47 to 440 Hz. Includes USA-style power cord.

APP-48D1..... +10.5 to 15V dc. Line cord with spade lugs included (black = +12V dc, white = 12V dc return, green = ground).

* Jumpers are located at the top rear of the power regulator board.

CONSUMPTION

AD models
40 watts max printing, 12 watts max idling

DC model
1.5A printing (average), 0.7 amps idling

FUSES

A1, J1 Models..... 1 amp

E1 Model..... 1/2 amp

D1 Model..... 3 AG 5A SLO-BLO

PHYSICAL

Operating Temperature Range
0 to +50°C

Storage Temperature Range
-30°C to +85°C without paper. Warning: The paper darkens after long exposure above +60°C.

Humidity
10% to 90%, non-condensing

Weight
6 pounds (no paper) 2,7kg)

Paper Roll
0.7 lb (0.3 kg)

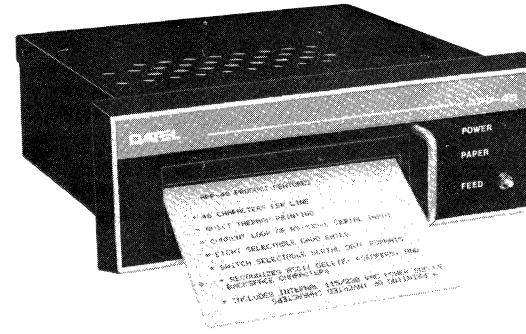
Outline Dimensions
8.20"W X 3.25"H X 8.14"D
(208,3 X 72,1 X 206,8 mm)

Bezel Dimensions
9.25"W X 3.25"H X 0.75" Thick
(235,0 X 82,6 X 19,1 mm)

Front Panel Mounting Cutout
8.40"W X 2.92"H 213,4 X 74,2 mm)
requiring 4 #8 mounting bolts.

Connector Type
DB-25P mounted on rear panel (25 pint D connector). Mates to a supplied DB-25S connector (DATEL P/N 58-2079130).

APP-48A2, E2, J2, D2
Serial Input 48-Column Thermal Printers



For a ruggedized version of the APP-48, suitable for mobile applications, see the APP-M48

FEATURES

- **Complete 48-column panel-mount printer with full serial data electronics and power supply built in.**
- **Accepts standard RS-232-C input at 110 to 9600 baud; also provides optoisolated 20 mA current loop input for operation hundreds of feet from the data source.**
- **Prints full 96-character, upper and lower case ASCII alphanumerics. Includes a second 96-character set of special figures, currency symbols, European punctuation, mathematical operators, Greek letters.**
- **Dot-line thermal printhead, few moving parts for OEM reliability.**
- **Prints inverted text like a TTY under software control. Last printed line is at bottom of text.**
- **Internal microprocessor includes 1-line, 48-column data buffer. Optional 132 character buffer (APP-48_4) permits continous data input.**
- **Prints up to 72 lines per minute.**
- **6-pound (2.7 kg) mini-lightweight.**
- **Choice of 100/115/230 VAC or +12V dc power supplies.**

GENERAL DESCRIPTION

Datel APP-48 panel-mount alphanumeric thermal printer highlights half a decade of thermal printer experience and leadership. Beginning in 1975 Datel pioneered the concept of including *all* data and power supply electronics *inside* the miniature housing.

The non-moving thermal printhead technology employed today in the APP-48 obsoletes ink printers with their twirling printwheels banging hammers and internal mess due to ink ribbons or platens.

The APP-48 accepts full serial input which has been formatted into 10 or 11-bit packed ASCII characters and is driven to either 20 mA loop or RS-232-C data levels. One printable line (up to 48 columns) of input data is stored in an internal input register. Data input is then halted briefly (750 mS) while the APP-48 drives the thermal printhead elements and advances to the next line after printing. The character is formed in a 5 column by 7 row dot matrix on specially-coated, thermally sensitive paper measuring 5 inches (127 mm) wide. Input data may be accepted at switch-selected data rates from110 to 9600 baud. Commonly used with teletypewriters, computer serial I/O ports and data terminals.

With the optional 132-character FIFO buffer installed (APP-48_4), the printer wil accept continuous full serial input at 110 baud (11-bit word length) or 300 baud (10-bit word length).

The 20 mA current loop data input is optoisolated so that common mode noise is rejected. Also the APP-48 may be operated at lower baud rates many hundreds of feet from the data source using only voice grade telephone wire.

The RS-232-C inputs include Request-To-Send and Data-Terminal- Ready standard control signals to synchronize start-stop data transfer from a remote source. A rear-panel DIP switch set selects the data baud rate, input format and other parameters.

The APP-48 prints the full 96-character set of standard ASCII characters. A second 96-character alphanumeric data set is stored in internal memory. This set may be accessed by transmitting the shift out control code (SO) before loading the next character. Shift in (SI) restores the normal 96-character ASCII set. The second set includes special figures, currency symbols, mathematical operators, European punctuation, Greek letters, etc.

The STX/ETX control codes change the mode to inverted printing where the last record is at the bottom of the text when viewed normally. In this mode the APP-48 may be mounted with its panel horizontal with printout feeding upwards like a teletypewriter. Under software control, lines may be alternated between lister (normal) and text (inverted) print modes.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

The print mechanism of the APP-48 consists of a stationary dot-line thermal printhead, Software-controlled stepping motor and cogged belt/print roller drive. The lightweight 6 pound (2.7 kg) APP-48 mounts through a 8.40"W X 2.92"H (213.4 X 74.2 mm) front panel cutout with four screws. A 3-pronged line plug is captive to the internal AC power supply which is available as 115, 230, or 100 VAC, 47 to 440 Hz Power consumption is 40 watts maximum during printing and 12 watts while idling or accepting data. The printer is also available with a +12V dc power supply. The dc version draws 1.5 amps while printing, 0.7 amps idling. The overall dimensions of the APP-48 are 8.12"W X 2.84"H X 8.32"D (206,3 X 72,2 X 211,3 mm). The operating temperature range is 0 to +50°C and the front bezel measures 9.25"W X 3.25"H X 0.75" thick (235,0 X 82,6 X 19,1 mm)

SPECIFICATIONS,

(Typical at +25°C unless noted)

PRINTOUT

Numbers of Columns 48

Characters Printed

96-character set upper and lower case ASCII letters, numbers, punctuation per ANSE X3.4-1977 Specification. A second 96-character set is accessible by transmitting the ASCII Shift Out (SO) character. This second set consists of European characters, mathematical symbols, Greek letters, some graphics symbols, monetary symbols, and others. The original ANSI X3.4 set is restored using the Shift In (SI) control character.

Printout Inversion. Character-lines may be printed out inverted with STX and ETX control characters. (Note: Normal and Inverted Text may not be intermixed on the same line)

Printout Format... 5 dot columns by 7 dot row matrix per character.

Printout Color..... Black characters on white paper.

Line Spacing..... 0.164 inch (4,2 mm) line to line. Approximatelyu 6 lines per inch.

Vertical Spacing Between Characters 0.1 inch (2.5 mm)

Printout Width (48 columns)..... 4.77 inches (121,2)

Character Size..... 0.070"WX0.110 H (1,8 X 2.8 mm)

Printing Method.... Dot-line, non- impact inkless ceramic thermal printhead.

Printing Rate..... Up to 72 lines per minute. (1.2 lines per second) at highest 9600 baud rate, regardless of the number of characters printed per line. The time required to print each line is:

$$\left[\frac{\text{char line \# bits char}}{\text{Baud Rate}} + 0.75\right] \text{ Seconds}$$

Printing Paper..... Thermal paper 5 inches (127 mm) wide X 150 foot (45 m) rolls. Supplied only in boxes of 10 rolls. Reorder part no. 33-22422568. A red warning strip is displayed on the paper when approximately 10 feet of paper remain*.

Data Capacity..... Approx. 11,00 lines in 150 feet usable per roll.

Printhead Life..... 30 million characters typical with random characters and Datel 33-2242568 paper rolls.

Mechanism Life.... 5,000 hours, typical in non-hostile environments.

*For users fabricating their own paper rolls, the end of the paper must detach from the core when paper is exhausted.

INTERFACE

Interface Type..... Full serial asynchronous either with or without data loading handshake controls.

Input Data Rate.... A rear panel DIP switch set selects one of the following data baud rates:

110	1200
150	2400
300	4800
600	9600

Note: The external data source must either halt or pad nulls during the 750 mS print and advance cycle. Continuous data input at 110 or 300 baud is possible when the 132 character FIFO buffer option is installed (OAPP-48_4).

Data Format..... Selectable 10 or 11 bits per character. 7 or 8 data bits, odd, even or no parity. 1 or 2 stop bits.

Electrical Data Inputs

Two inputs, EIA RS-232-C or 20 mA corrent loop on separate pin sets on the rear panel DB-25P data connector. A Request to Send output (RS-232-C circuit CA, pin 4) and Data Terminal Ready output (RS-232-C circuit CD, pin 20) are provided. (Note: The logic polarity of Requst to Send is Switch Selectable)

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CD, pin 20) are provided. (Note: the logic polarity of Request to Send is switch selectable)

Self Test.....An internal rotating 96-character ASCII set may be printed using two external jumpers from pin 25 to pin 7 (ground) and from pin 2 to 3.

Data Coding Levels

	Current Loop*	RS-232-C
"1" (Mark)	20 mA nom	-3 to -15V
"0" (Space)	0 mA nom	+3 to +15V

*10^5 Megohms resistance, 1500V dc isolation.

DATA-CODED FUNCTIONS

Character	meaning	Hex.	Octal
NUL	Null, ignored	00	000
BS	Backspace delete previous character	08	010
	Shift Out. Maps input data into the 2nd 96-character (non-standard set)	0E	016
SI	Shift In. Reset into ASCII data set	0F	017

Note1 SO and SI may be transmitted before each character. If SO or SI are not sent, printer will remain in last character set status. Power-on reset selects the ASCII character set.

Note 2 Backspace decrements the column address counter loads a space character, and leaves column counter, decremented The recommended procedure to clear a line of any length before printing is to load 48 backspaces.

Character	Meaning	Hex.	Octal.
STX	Changes to inverted printing (text) mode	02	002
ETX	Changed to normal, non-inverted (lister) printing mode.	03	003

Note: STX and ETX must be transmitted before each line and cannot be accepted within a line. If STX and ETX are not sent, the other printer will remain in the last mode status. Power-on reset may be DIP switch selected to automatically start in either the text or lister mode.

Character	Meaning	Hex.	Octal.
HT	Horizontal tab. Successively indexes to columns 9, 17, 25 and 33 for data logging or tabular aplications.	09	011
LF	Line Feed. Advances one line, no print, no change of input register.	0A	012
FF	Form Feed. Advances 11 lines, no register change.		
CR	Carriage Return is used to print register contents, clear the register and advance one line. CR requires 750 mS, during which input data cannot be accepted. LF is not required to advance the line. If the sequence CR LF is sent, LF is ignored*	0D	015
DEL	Delete. Clear previous character column, load rubout obliteration pattern, and advance column counter to original address. It is not possible to backspace and obliterate previously printed characters	7F	177

* A full input register will also automatically start the printing cycle

FRONT PANEL

Power On..... Yellow Light Emitting Diode (LED) iluminates when power is applied. Note: Since most users will connect the APP-48 through a master system power on-off switch. There is not spearate power on-off switch on the APP-48.

Feed..... Momentary pushbutton switch (Note 1) advances paper as long as it is depressed. (Note 2)

End of Paper..... Red LED illuminates when approx. one inch of paper is remaining and disables further printing until paper is renewed. A red warning stripe appears on paper before the LED illuminates. (Note 2)

Note: 1 A line will finish printing if Feed is depressed while executing the print and advance cycle.

Note: 2 Feed and End of Paper functions cause Request to Send to go false to inhibit the data transmitter.

POWER SUPPLY

Required Power

APP-48A2..... 105 to 30VAC @ 47 to 440 Hz, jumper-selectable * for 210 to 250 VAC. Includes USA-style power cord.

APP-48E2..... 210 to 250 VAC @ 47 to 440 Hz, jumper-selectable* for 105 to 130 VAC. Includes European-style power cord.

APP-48J2..... 100 VAC 47 to 440 Hz. Includes USA-style power cord.

APP-48D2..... +10.5 to 15V dc. Line cord with space lugs included (black = +12V dc, white = 12V dc return, green = green).

*Jumpers are located at the top rear of the power regulator board.

Consumption

AC Model..... 40 watts max printing, 12 watts max idling.

DC Model..... 1.5A printing (avg), 0.7 amps idling.

Fuses

AC Models..... 115 and 100 VAC, 1 amp
230 VAC, 1/2 amp

DC Model..... 3 AG, 5A SLO-BLO

PHYSICAL

Operating Temperature Range..... 0 to +50°C

Storage Temperature Range..... -30°C to +85 without paper. Warning: The paper begins to darken after long exposure to +60°C and above.

Weight..... 6 pounds (no paper) (2.7 kg)

Paper Roll..... 0.7 lbs. (0.3 kg)

Outline Dimension. 8,12"W X 2.84"H X 8.32"D (206,25 X 72,14 X 211.33 mm)

Bezel Dimensions. 9.25"W X 3.25"H X 0.75"Thick. (235,0 X 82,6 X 19,1 mm).

Mounting Method. Through a front panel cutout measuring 8.40"W X 2.92"H (213.4 X 74.2 mm) 4 #8 mounting bolts and hardware are required.

Mounting Position Horizontal (Panel Mount) or Vertical (with panel facing upwards)

Acceleration (non-operating).... Within ±5G 0 to 50 Hz,3 Axes

Relative Humidity. 0 to 90% non-condensing

Altitude..... 0 to 10,000 feet (3048 m)

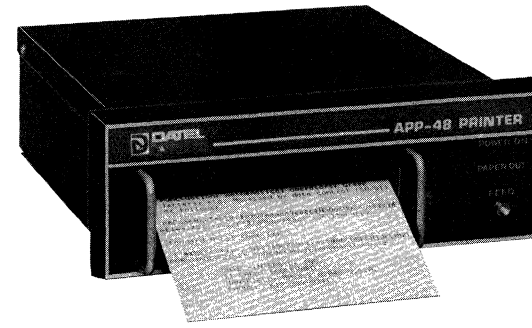
ORDERING INFORMATION

MODEL	DESCRIPTION
APP-48A2	Printer, 115/230 VAC (115 VAC wired), 47-440 Hz, USA Plug
APP-48E2	Printer, 115/230 VAC (230 VAC wired), 47-440 Hz, European Plug
APP-48J2	Printer, 100 VAC, 47-440 Hz, USA Plug
APP-48D2	Printer, +12V dc Power
APP-48_4	Printer with optional 132-character data buffer (specify desired power supply).
33-2242568	Box of 10 thermal paper rolls (150 feet per roll)
58-2079130	Spare Mating DB-25S Data Connector (1 supplied)
33-8193205	Printer stand kit (for bench-top applications)
APP-TR5A	Take-up reel/rewind accessory, 115 VAC powered
APP-TR5E	Take-up reel/rewind accessory, 230 VAC powered
APP-TR5D	Take-up reel/rewind accessory, ±12V dc powered.

APP-48A3, E3, J3, D3
IEEE-488 Bus Compatible 48-Column Thermal Printers

FEATURES

- **Complete 48-column panel-mount printer with IEEE-488 interface and built-in power supply**
- **Prints full 96-character, upper and lower case ASCII alphanumerics. Includes second 96-character set of special figures, currency symbols, European punctuation, mathematical operators, etc.**
- **Dot-line thermal printhead, few moving parts for OEM reliability. No ink, no hammers, no mess!**
- **Prints inverted text (like a TTY) under software control**
- **Internal microprocessor includes one line, 48-column data buffer**
- **Prints up to 72 lines per minute**
- **6 pound (2.7 kg) mini-light weight**
- **Choice of 100/115/230 VAC or +12V dc power supplies**



GENERAL DESCRIPTION

The APP-48A3/E3/J3/D3 is a miniature 48-column panel-mount/table top alphanumeric thermal printer. It comes complete with power supply and GPIB compatible interface electronics to provide hard copy output via the IEEE-488 General Purpose Interface Bus (GPIB). The APP-48 operates as a "Listen Only" device using a unique user-selectable 5-bit "My Listen Address" (MLA).

The IEEE-488 IB compatible devices which can send data messages to the APP-48 include computers, programmable calculators, digital voltmeters and spectrum analyzers. In addition, by using readily available GPIB interface boards, most popular mini and microcomputers can easily make use of the APP-48.

The APP-48 is fully IEEE Std. 488-1978 GPIB (General Purpose Interface Bus) compatible. The GPIB compatible APP-48 communicates with the controller using standard open collector drives. One printable line (up to 48 columns) of input data is stored in an internal data buffer register. The data input is then halted for 750 mS while the APP-48 activates the thermal printhead elements to ouput the alphanumeric characters, after which the paper is advanced to the next line. Each character is formed by a 5 column by 7 row dot matrix on specially coated, heat sensitive paper which measures 5 inches (127 mm) wide. There are no baud rate switches or jumpers to worry about as print rate is a direct function of the GPIB handshake protocol.

The APP-48 GPIB data format is 8 parallel, bi-directional lines, normally 7 data bits and 1 parity bit with 3 handshake lines:
A. DAV (Data Valid)
B. NRFD (Not Ready for Data)
C. NDAC (Not Data Accepted)

The APP-48 prints the full 96-character set of standard ASCII characters. A second 96 alphanumeric character set is stored in an internal memory. This set may be accessed by transmitting the shift out control code (SO) before loading the next character. Shift in (SI) restores the normal 96-character ASCII set. The second set includes special figures, currency symbols, mathematical operators, European punctuation, Greek letters, etc.

The STX/ETX control codes change the mode to inverted printing where the last record is at the bottom of the text when viewed normally. In this mode, the APP-48 may be mounted with its panel horizontal with printout feeding upwards like a teletypewriter. Under software control, lines may be alternated between lister (normal) and text (inverted) print modes.

The print mechanism of the APP-48 consists of a stationary dot-line thermal printhead, software-controlled stepping motor and cogged belt/print roller drive. The lightweight 6 pound (2.7 kg) APP-48 mounts through a 8.40"W x 2.92"H (213,4 x 74,2 mm) front panel cutout with four screws. A 3-prong line plug is captive to the internal AC power supply which is available as 115, 230 or 100 VAC, 47 to 440 Hz. Power consumption is 40 watts, maximum during printing and 12 watts while idling or accepting data. The printer is also available with a +12V dc power supply. The dc version draws 1.5 Amps while printing, 0.7mA idling. The overall dimensions of the APP-48 are 8.12"W x 2.84"H x 8.32"D (206,3 x 72,2 x 211,3 mm). The operating temperature range is 0 to +50°C and the front bezel measures 9.25"W x 3.25"H x 0.75" thick (235,0 x 82,6 x 19,1 mm).

For a ruggedized version of the APP-48, suitable for mobile applications, see the APP-M48

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FUNCTIONAL SPECIFICATIONS

(Typical at +25°C unless noted)

PRINTOUT

Numbers of Columns.. 48

Characters Printed.... 96-character set, upper and lower case ASCII letters, numbers, punctuation per ANSI X3.4-1977 Specification. A second 96-character set is accessible by transmitting the ASCII Shift Out (SO) character. This second set consists of European characters, mathematical symbols, Greek letters, some graphics symbols, monetary symbols and others. The original ANSI X3.4 set is restored using the Shift In (SI) control characters.

Printout Inversion..... Character-lines may be printed out inverted with the STX and ETX control characters. When switch nine at the rear of the printer is OFF (switched left), the unit comes up in List mode, when it is ON (switched right), the unit comes up in Text (inverted) mode. STX = Text Mode. ETX = Lister Mode. (Note: Normal and inverted text may not be intermixed on the same line)

Printout Format..... 5 dot columns by 7 dot row matrix per character.

Printout Color..... Black characters on white paper.

Line Spacing..... 0.164 inch (4,2 mm) line to line. Approximately 6 lines per inch.

Vertical Spacing Between Characters..... 0.1 inch (2,5 mm)

Printout Width (48 Columns)..... 4.77 inches (121,2 mm)

Character Size..... 0.070"W x 0.110"H (1,8 x 2,8 mm)

Printing Method..... Dot-line, non-impact, inkless ceramic thermal printhead.

Printing Rate..... Up to 72 lines per minute, 1.2 lines per second max. regardless of the number of characters to be printed per line.

Printing Paper..... Thermal paper 5 inches (127 mm) wide x 150 foot (45 m) rolls. Supplied only in boxes of 10 rolls. Reorder part no. 33-2242568. A red warning stripe is displayed on the paper when approximately 10 feet of paper remain.

Data Capacity..... Approx. 11,000 lines in 150 feet usable per roll.

Printhead Life..... 30 million characters typical with random characters and DATEL 33-2242568 paper rolls.

Mechanism Life..... 5000 hours, typical in non-hostile environments.

INTERFACE

Interface Type..... IEEE 488 STD (1978) compatible.

Data Format..... 8 parallel, bi-directional data lines, normally 7 data bits and 1 parity bit. 3 handshake lines: A) DAV (data valid) B) NRFD (not ready for data) C) NDAC (not data accepted).

Electrical Data Inputs..... IEEE 488 STD (1978) Inter face Bus compatible.

Self Test..... An internal rotating 96 character ACII set printed when the bottom switch (SWØ) is switched left. The switch is accesable at the rear panel. NOTE: The unit must be powered down for 2 sec. min. after changing any switch position for the change to become effective.

Data Coding Levels...

Logic Level	Voltage Level
0 (False)	≥2.0V (High)
1(True)	≥+0.8V(Low)

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DATA-CODED FUNCTIONS

Character	Meaning	Hex	Octal
NUL	Null, ignored	00	000
BS	Backspace, delete previous character	08	010
SO	Shift Out, Maps input data into the 2nd 96-character (non-standard set)	0E	016
SI	Shift In, Reset into standard ASCII data set	0F	017
STX	Changes to inverted printing (text) mode	02	002
ETX	Changes to normal, non-inverted (lister) printing mode	03	003
HT	Horizontal tab successively indexes to columns 9, 17, 25 and 33 for data logging or tabular applications.	09	011
LF	Line Feed advances one line, no print, no change of input register.	0A	012
FF	Form Feed advances 11 lines, no register change.	0C	014
CR	Carriage Return is used to print register and advances one line. CR requires 750 mS, during which input data cannot be accepted. LF is not required to advance the line. If the sequence CR, LF is sent, LF is ignored.*	0D	015
DEL	Delete. Clear previous character column, load rubout obliteration pattern, and advance column counter to original address. It is not possible to backspace and obliterate previously-printed characters.	7F	177

*A full input register will also automatically start the printing cycle.

FRONT PANEL

Power On..... Yellow Light Emitting Diode (LED) illuminates when power is applied. NOTE: Since most users will connect the APP-48 through a master system power on-off switch, there is no separate power on-off switch on the APP-48.

Feed..... Momentary pushbuttom switch (Note 1) advances paper as long as it is depressed. (Note 2)

End of Paper..... Red LED illuminates when approximately one inch of paper is remaining and disables further printing until paper is renewed. A red warning stripe appeares on paper before the LED illuminates (Note 2)

Note 1: A line will finish printing if Feed is depressed while executing the print and advance cycle.

Note 2: Feed and End of paper functions inhibit data transmission from the controller to the printer.

POWER SUPPLY

Required power

APP-48A3.....105 to 130 VAC at 47 to 440 Hz, jumper-selectable* for 210 to 250 VAC. Includes USA-style power cord.

APP-48E3.....210 to 250 VAC at 47 to 440 Hz, jumper-selectable* for 105 to 130 VAC. Includes European-style power cord.

APP-48J3..... 100 VAC at 47 to 440 Hz. Includes USA-style power cord.

APP-48D3.....+10.5 to 15V dc. Line cord with spade lugs included (Black = +12V dc, White = 12V dc return, Green = ground)

*Jumpers are located at the top rear of the power regulator board.

Consumption

AC models..... 40 watts max printing, 12 watts max idling

DC models..... 1.5 A printing (avg), 0.7 Amps idling

Fuses

AC models.....115 and 100 VAC, 1 Amp
230 VAC, 1/2 Amp

DC models..... 3 AG 5A SLO-BLO

PHYSICAL/ENVIRONMENTAL

Operating Temperature Range..... 0 to +50°C

Storage Temperature Range..... -30°C to +85°C without paper. The paper begins to darken after long exposure to +60°C and above.

Weight..... 6 pounds (no paper) (2,7kg)

Paper Roll..... 0.7 lbs (0,3 kg)

Outline Dimensions... 8.12"W x 2.84"H x 3.32"D (206,25 x 74,2 x 221,33 mm)

Bezel Dimensions..... 9.25"W x 3.25"H x 0.75" thick (213,4 x 74,2 mm)

Mounting Method..... Through a front panel cutout measuring 8.40"W x 2.92"H (213,4 x 74,2 mm) 4 #8 mounting bolts and hardware are required.

Mounting Position..... Horizontal (Panel Mount) or Vertical (with panel facing upwards)

Acceleration (Non-operating)..... Within ±5G, 0 to 50 Hz, 3 Axes

Relative Humidity..... 0 to 90%, non-condensing

Altitude..... 0 to 10,000 feet (3048 m)

ORDERING GUIDE

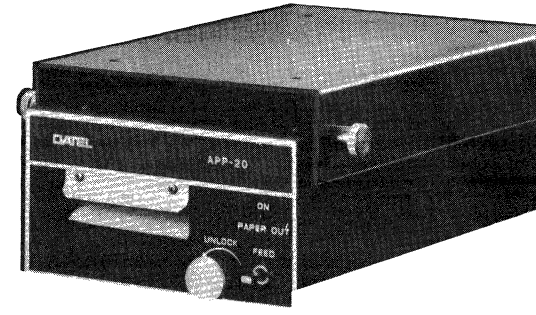
MODEL	DESCRIPTION
APP-48A3	Printer, 115/230 VAC, 47-440 Hz, USA Plug (115 VAC wired)
APP-48E3	Printer, 115/230 VAC, 47-440 Hz, European Plug (230 VAC wired)
APP-48J3	Printer, 100 VAC, 47-440 Hz, USA Plug
APP-48D3	Printer, +12V dc Power
33-2242568	Box of 10 black image paper rolls
58-2079130	Spare Mating DB-25S Data Connector (1 supplied)
APP-TR5A	Takeup/Rewind Accessory, 115 VAC
APP-TR5E	Takeup/Rewind Accessory, 230 VAC
APP-TR5D	Takeup/Rewind Accessory, +12V dc

APP-M20
Rugged Mobile 20-Column Thermal Printer

DATEL

FEATURES

- **Ruggedized construction - designed to comply with MIL-STD-202E and 810C for shock, humidity, and vibration**
- **+12V dc powered, for use with standard vehicle battery; AC models also available**
- **Low power consumption - 1.2 A printing, 360 mA standby**
- **Illuminated printout, extra TALL character printing and paper advance features for easy viewing day or night**
- **20 column output with the full 96 ASCII character set available**
- **Quiet non-distracting thermal printing**
- **Compact - smaller than a CB radio**
- **Slide mounted for easy removal**
- **Available in Serial, Parallel or IEEE-488 compatible versions**



APPLICATIONS

- **Radio communications system with many varied applications**
- **Portable personal computers**
- **Test and measurement equipment for field use**
- **Hard copy output for medical and analytical instrumentation**
- **Diagnostic test equipment**
- **Remote data loggers and factory automation productivity systems**

GENERAL DESCRIPTION

The APP-M20 is a 20 column thermal printer specifically designed for use in harsh evironments. With its slide mount and illuminated printout, the APP-M20 is particularly well suited for use in mobile applications. The mechanical specifications (except for the mounting bracket) and electrical specifications correspond exactly to those of the popular panel mount models (APP-20D1, APP-20D21, APP-20D3).

The APP-M20 user will benefit from the microprocessor controlled interface, compact size (smaller than a CB radio) and quiet, inkless thermal printing. The TALL character height printing capability, Form Feed (paper advance) and illuminated paper output slot make reading the printer output at a glance extremely easy, both day and night. In addition, the APP-M20 offers a special "inverted text" option, where the last line printed is at the bottom of the printout. The APP-M20 thermal printing mechanism requires virtually no maintenance outside of an occasional printhead cleaning. No replacement printheads or ribbons need to be carried. The APP-M20 can be ordered with the bracket installed either on the top, on the bottom (by special order), or in a panel mount configuration making it installable virtually anywhere.

Much effort has been put into the hardware design to ensure that the printers will stand up the the rigors of mobile operation. The APP-M20 has passed testing by an independent laboratory for shock, vibration and humidity, conforming to MIL-STD-202E and MIL-STD-810C. Copies of these test results are available from DATEL upon request.

The APP-M20 voltage input requirements are +10.5 to +14.5 V dc at 1.2 A while printing and 360 mA during standby. No special powerline conditioning is required.

The APP-M20 prints the full 96 ASCII character set across 2-15/16" (58,6 mm) wide thermal paper. A single dot line, thick film, thermal printhead forms 5 x 7 dot matrix characters which are 0.11" (2,8 mm) high at a rate of 63 lines of 20 characters per minute. A standard 130' roll of paper will display 8,400 lines of alphanumerics at 5 lines per inch (2 lines per cm) spacing.

The operating temperature range is from -20°C to +50°C. The printer can withstand up to 95% relative humidity.

A mounting bracket and slides are shipped with each printer for easy installation.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C unless noted)

(For complete specifications, refer to the standard parallel, serial, or IEEE-488 model brochures: APP-20D1, APP-20D21, APP-20D3).

INTERFACE TYPES (3)

8-bit parallel (APP-M20D1)
Serial RS-232-C or 20 mA current loop (APP-M20D21)
IEEE-488 (APP-M20D3)

PRINT CHARACTERISTICS

Printing Rate..... 63 lines/minute
Number of Columns..... 20
Characters Available..... 96 Standard ASCII
Character Height..... 0.11" (127 mm)

PHYSICAL AND ENVIRONMENTAL

Dimensions
- Overall Clearance..... 6.16"W x 3.57"H x 11.52"D (156,46 x 90,68 x 292,60 mm)
- Housing..... 5.36"W x 2.76"H x 8.00"D (136,14 x 70,10 x 203,20 mm)
- Mounting Hood..... 5.36"W x 0.75"H x 8.0"D (135,14 x 19,0 x 203,20 mm)
- Bezel..... 5.25"W x 2.82"H x 0.78"D (133,87 x 71,91 x 19,89 mm)

Weight..... 2.5 lbs (1,14 kg)
Operating Temp Range... -20°C to +50°C
Storage Temp Range..... -45°C to +85°C (Caution: the paper will begin to darken after several days of exposure to temperatures in excess of +60°C)
Relative Humidity..... 0% to 95% non-condensing
Shock..... 10 g at 10 to 500 Hz

POWER

Power Requirement..... +10.5 to 14.4V dc
Current Draw..... 1.2 A printing; 360 mA standby
Connector..... MOLEX receptacle with crimp-on female terminals

ORDERING GUIDE

MODEL	DESCRIPTION
APP-MS0D1	Parallel input 20-column ruggedized printer
APP-M20D21	Serial input 20-column ruggedized printer
APP-M20D3	IEEE-488 input 20-column ruggedized printer
APP-TRD	Automatic, panel-mount take-up reel (+12V powered)
32-2242572	20-column thermal printer paper (10 130' rolls)

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APP-M48
Rugged Mobile 48-Column Thermal Printer

DATEL

FEATURES

- **Ruggedized construction — designed to comply with MIL-STD-202E and 810C for shock, humidity, and vibration**
- **+12V dc powered, for use with standard auto battery**
- **Low power consumption — 2.3A printing, 1A standby**
- **Illuminated printout, inverted text option and paper advance features for easy viewing — day or night**
- **48 column output with the full 96 ASCII character set, plus second 96-character set of special symbols**
- **Quiet, non-distracting thermal printing; virtually maintenance free**
- **Compact size, slide-mounted for easy removal**
- **Available in Serial, Parallel or IEEE-488 compatible versions (APP-M48D1, APP-M48D2, APP-M48D3)**

APPLICATIONS

- **Radio communications systems**
- **Portable personal computers**
- **Test and measurement equipment for field use**
- **Hard copy output for medical and analytical instrumentation**
- **Remote data loggers**

GENERAL DESCRIPTION

The APP-M48 is a 48 column thermal printer specifically designed for use in harsh environments. With its slide mount and illuminated printout, the APP-M48 is particularly well suited for mobile applications. The mechanical specifications (except for the mounting bracket) and electrical specifications correspond exactly to those of the popular panel mount models (APP-48D1, 2, 3).

The APP-M48 user will benefit from the microprocessor controlled interface, compact size, and quiet, inkless thermal printing. The inverted text option (last line printed is at the bottom of the printout), Form Feed (paper advance) and illuminated paper output slot make reading the printer output at a glance extremely easy, both day and night. In addition, the APP-M48 thermal printing mechanism requires virtually no maintenance. No replacement printheads of ribbons need to be carried. The APP-M48 can be ordered with the bracket installed either on the top, on the bottom (on special order) or in a panel mount configuration making it installable virtually anywhere.

Much effort has been put into the hardwhere design to ensure that the printers will stand up to the rigors of mobile operation. The APP-M48 has passed testing by an independent laboratory for shock, vibration and humidity, conforming to MIL-STD-202E and MIL-STD-810C. Copies of these test results are available from DATEL upon request.

The APP-M48 voltage input requirements are +10.5 to +14.5V dc at 2.3 A average while printing and 1 mA during standby. No special powerline conditioning is required.

The APP-M48 prints the full 96 ASCII character set across 5" (127 mm) wide thermal paper. A second 96-character set includes special characters such as currency symbols, European punctuation, mathematical operators, Greek letters, etc. A single dot line, thick film, thermal printhead forms 5x7 dot matrix characters which are 0.11" (2,8 mm) high at a rate of 1.2 lines per second.

The operating temperature range is from -20°C to +50°C. The printer can withstand up to 95% relative humidity.

A mounting bracket and slides are shipped with each printer for easy installation.

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FUNCTIONAL SPECIFICATIONS
(Typical at 25°C unless noted)

(For complete specifications, refer to the standard parallel, serial, or IEEE-488 model brochures: APP-48D1, APP-48D2, APP-48D3)

INTERFACE TYPES (4)
8-bit parallel (APP-M48D1)
Serial RS-232-C or 20 mA current loop (APP-M48D2)
RS-232-C/20 mA loop with 132 byte buffer (APP-M48D4)
IEEE-488 (APP-M48D3)

PRINT CHARACTERISTICS
Printing Rate..... 72 lines/minute
Number of Columns..... 48
Characters Available..... 96 Standard ASCII plus 96 special characters
Character Height..... 0.11" (127 mm)

PHYSICAL ENVIRONMENT
Dimensions
Overall Clearance..... 9.25"W x 4.00"H x 10.44"D (234,95 x 101,6 x 265,18 mm)
Housing..... 8.20"W x 2.84"H x 8.14"D (208,28 x 72,14 x 206,76 mm)
Mounting Hood..... 5.36"W x 0.75"H x 8.0"D (135,14 x 19,0 x 203,20 mm)
Printer Beze..... l9.25"W x 3.25"H x 0.75"D (234,95 x 82,55 x 19,1 mm)
Weight..... 6 lbs. (2.7 kg)
Operating Temp Range... -20°C to +50°C
Storage Temp Range..... -45°C to +85°C (Caution: the paper will begin to darken after several days of exposure to temperatures in excess of +60°C)
Relative Humidity..... 0% to 95% non-condensing
Shock..... 10g at 10 to 500Hz

POWER
Power Requirement..... +10.5 to +14.4 V dc
Current Draw..... 2.3A printing; 1.0A standby
Connection..... 5' long power cord

ORDERING GUIDE

MODEL	DESCRIPTION
APP-M48D1	Parallel input 48 column ruggedized printer
APP-M48D2	Serial input 48 column ruggedized printer
APP-M48D3	IEEE-488 input 48 column ruggedized printer
APP-48D4	Same as APP-M48D2 but includes 132 character input buffer for continuous throughput
APP-TR5D	Automatic, panel-mount take-up reel (+12V powered)
32-2242572	48 column thermal printer paper (10 130' rolls)

10

APP-TR1,2,5
Take-Up/Rewind Reels for Panel Printers

DATEL

FEATURES

- **Automatically takes up printout from all DATEL thermal printers and many other brands of panel mount printers**
- **Allows manual paper withdrawl for easy viewing while powered ON**
- **Very fast rewind**
- **Easy-to-install panel mounting**
- **AC and DC powered models available**
- **+12 VDC model is ideal for vehicular/mobile applications**
- **Low cost - dependable**

DESCRIPTION

The APP-TR Series Take-up/Rewind Accessories automatically take up the printout as it is generated by DATEL panel-mount thermal printers. The APP-TR is also compatible with other brands of panel-mount printers which use similar width paper. The APP-TR is a completely self-contained unit, designed for panel mounting.

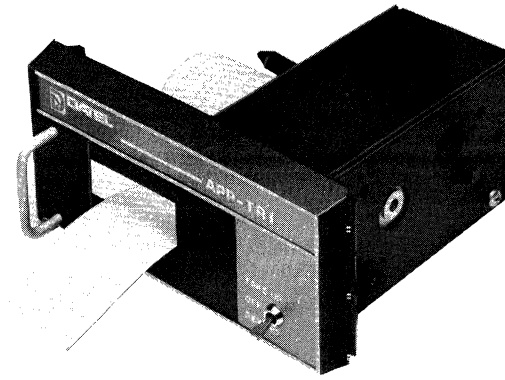
The front bezels of the APP-TR1, APP-TR2, and APP-TR5 match the bezels of DATEL's DPP-Q7, APP-20, and APP-48 thermal printers respectively. The APP-TR2 is also compatible with DATEL's low-cost MPP-20 printer.

The APP-TR bezels mount on hinges which allow the user to swing open the unit for easy access to the paper rollers. The paper is taken up by a slotted take-up shaft which does not require the use of spools or axles which are easily lost. Also, the APP-TR take-up mechanisms have been designed so that the paper can be pulled out and read while the power is on; when the paper is released it is automatically rewound.

A front panel mounted three-position switch (TAKE UP/OFF/REWIND) is the only operator control on the unit. The "TAKE UP" position is the normal position, while the "REWIND" positions allows the paper to be quickly rewound to its original state (first line printed is at the outside of the roll).

The APP-TR is available with several power supply options: 90 - 130VAC (for American and Japanese line power), 210 - 260VAC (European), and a +12V dc version ideal for mobile applications.

All of the necessary mounting hardware is provided for mounting the APP-TR in a standard 1/8" thick panel. The APP-TR must be mounted directly below and in line with the companion printer; the paper printout exiting from the printer must travel straight down to enter into the take up reel properly. The distance between the printer and the APP-TR depends on how much usable panel space is available, and how much of the printout the user wishes to display.



ORDERING GUIDE

APP-TR1A	DPP-Q7 compatible (1.75" paper), 115VAC powered
APP-TR2A	APP-20/MPP-20 compatible (2.31" paper), 115VAC powered
APP-TR5A	APP-48 compatible (5.0' paper), 115VAC powered
APP-TR1E	DPP-Q7 compatible (1.75 " paper), 230VAC powered
APP-TR2E	APP-20/MPP-20 compatible (2.31" paper), 230VAC powered
APP-TR5E	APP-48 compatible (5.0" paper), 230VAC powered
APP-TR1D	DPP-Q7 compatible (1.75" paper), +12V dc powered.
APP-TR2D	APP-20/MPP-20 compatible (2.31" paper), +12V dc powered
APP-TR5D	APP-48 compatible (5.0" paper), +12V dc powered

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FUNCTIONAL SPECIFICATIONS (Typical @ 25°C unless otherwise noted)

COMPATIBILITY

APP-TR1A, E, D:	DATEL's DPP-Q7 Panel-mount Thermal Printer or any printer using 1.75" - wide (max.) paper.
APP-TR2A, E, D:	DATEL's APP-20 and MPP-20 Panel-mount Thermal Printers or any printer using 2.31" - wide (max.) paper.
APP-TR5A, E, D:	DATEL's APP-48 Panel-mount Thermal Printer, or any printer using 5.00" - wide (max.) paper.

POWER

Requirements

APP-TR1A/
APP-TR2A: 90 to 130VAC, 0.18A, 10W, 47 to 440Hz
APP-TR5A: 90 to 130VAC, 0.3A, 16W, 47 to 440HZ

APP-TR1E/
APP-TR2E: 210 to 250VAC, 0.09A, 10W, 47 to 440Hz
APP-TR5E: 210 to 260VAC, 0.15A, 16W, 47 to 440Hz

APP-TR1D/
APP-TR2D: +10 to +14V dc, 0.9A, 10W
APP-TR5D: +12 to +14V dc, 1.5A, 16W

Fuses

APP-TR1/TR2A 1/2 Amp. SLO BLO
APP-TR1A/APP-TR2A: 1/2 Amp, SLO BLO
APP-TR5A: 1 Amp, SLO BLO

APP-TR1E/APP-TR2E: 1/4 Amp, SLO BLO
APP-TR5E: 1/2 Amp, SLO BLO

APP-TR1D/
APP-TR2D/
APP-TR5D: 2 Amp, SLO BLO

Power Cords

"A" models: 6', USA-style line cord
"E" models: 6', European-style line cord (2 prongs and ground shell)
"D" models: 6' line cord which spade lug termination (3):
BLACK = +12V
WHITE = 12V return
GREEN = Chassis ground

PERFORMANCE

Paper roll capacity:	150' (all models)
Paper tension:	2 oz. min, 12 oz. max
Paper rewind time:	45 seconds for 150' roll

PHYSICAL/EVIRONMENTAL

Case Dimensions

APP-TR1/
APP-TR2: 6.56"W x 3.25"H x 5.75"D (166,62 x 82,55 x 146,05mm)
APP-TR5: 9.25"W x 3.25"H x 5.75"D (234,95 x 82,55 x 146,05mm)

Panel Cutout Dimensions

APP-TR1/
APP-TR2: 5.944"W x 3.040"H (150,977 x 77,21mm)
APP-TR5: 8.634"W x 3.040"H (219,30 x 77,21mm)

(Mounting hardware supplied for all models)

Weight

APP-TR1/
APP-TR2: 1.05 lbs
APP-TR5; 1.25 lbs

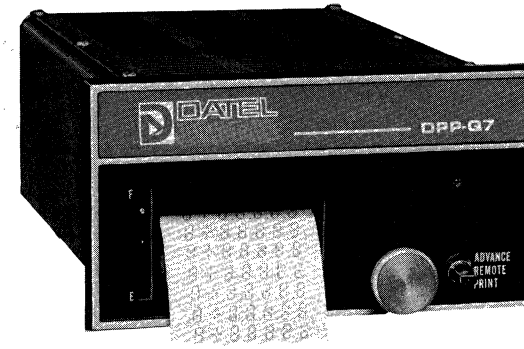
Case Construction: Aluminum case, plastic front bezel

Operating Temperature Range: 0 to + 50°C

DPP-Q7
BCD Input, 7-Column Thermal Printer

DATEL

FEATURES
- **6 Numeric columns and sign**
- **4 Lines/second OEM-reliable thermal printer**
- **Includes all electronics for parallel BCD input Selectable leading zero blanking**
- **Positive or negative true TTL/DTL inputs**
- **Available in 100, 110, 230 VAC versions**
- **4.4 Pound panel-mount featherweight**
- **No ink, ribbons or hammers; virtually maintenance free**



GENERAL DESCRIPTION

Imagine a low cost 7-column panel-mounting printer just slightly larger than most digital panel meters. Imagine this lightwight, high-reliability digital panel printer installed in your instrument or system front panel. And imagine an inkless, non-impact thermal printing method with only two moving parts which will last for years.

This is DATEL's miniature 4 line per second DPP-Q7 thermal panel printer. A no-nonsense, simple to apply, OEM-designed digital output device that weighs in at only 4.4 pounds (2.0 Kg). OEM features are designed into the DPP-Q7 such as selectable leading zero blanking, selectable positive or negative true coding inputs and choice of 100 to 230 VAC line power. Full parallel TTL input BCD electronics are included as standard.

Other OEM design features include a selection of printout formats, manual print and advance front panel switch, and a low paper switch output. A unique mounting technique uses an aluminum housing which attaches directly through a front panel cutout. This housing permanenty holds the electronics, although the mechanical assembly can be completely removed for paper replacement using a single front panel thumbscrew.

As the mechanical assembly is removed, it disconnects from the internal electronics PC board connectors, so that no lethal power voltages are exposed during paper reloading. However, the external PC board connectors at the rear of the case remain connected to the signal inputs. The housing supports the weight of the mechanical assembly and is mounted on a front panel through a 4.50" x 2.78" cutout and secured by four screws. Three DPP-Q7 panel printers can conviently be mounted across a 19" x 3 1/2" high rack-mount panel.

OEM pricing makes the DPP-Q7 ideal for instrument products. Comparable impact parallel printers with BCD decoding and drive electronics usually list for more than the DPP-Q7.

Standard 1 3/4" wide thermographic papers are used in handy 130 foots rolls giving about 7,800 lines per roll with 5 lines per inch. The 7-segment digits are .155" high with left-of-digit decimal points selectable at each digit. Seven column printing formats include sign, and six digits or 2-channel (ident) digits, sign and 4 data digits. Other 7-column decimal formats, as well as hexidecimal formats, are also available.

The DPP-Q7 Digital Panel Printer extends back 8.62" from the front surface of the mounting panel, including space allowance for the two 30-conductor PC board connectors and AC fuses.

Three universal AC line voltages (100,115, and 230 VAC) will power the DPP-Q7 Printer at approximately 20 watts.

The DPP-Q7 is ruggedly built, using a simple, but sophisticated mechanical design which is optimized for heavy duty OEM applications. A proprietary printhead character coating allows the head to be conservatively rated at 3 million lines, minimum.

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FUNCTIONAL SPECIFICATIONS
(Typical at +25°C unless noted)

GENERAL

Number of columns 7-Column formats available:
a) Leading ± sign and 6 decimal digits
b) 2 Leading ident or channel digits, ± sign and 4 data digits

Decimal digit format:
7-segment 0 to 9 digits .155" (4mm) high with 10° slant and selectable left decimal point.

Printing method:
Thick film thermal print head, black characters on white paper (using DATEL 32-2242570 paper)

Printer paper:
1.75" wide x 130 feet long, (44,5 x 39,62 m), thermal paper with the thermal surface facing away from the center of the roll (DATEL P/N 32-2242570)

Paper advance:
Via stepper motor

PERFORMANCE

Max. printing rate: 4 lines per second
Print and paper advance cycle: 250 milliseconds

Line spacing: 0.2 inch (5mm)
Line density: 5 lines per inch
Line capacity per paper roll: approx. 7,800 lines
Minimum print head life: 3 million lines

INPUTS

DTL/TTL compatible, selectable positive or negative true, level sensitive, TTLLS low power Schottky logic used on all inputs.

Logic Levels:

Positive true: +2.0V ≤ "1" ≤ +5.0V
0V ≤ "0" ≤ +0.5V

Negative true: 0V ≤ "1" ≤ +0.5V
+2.0V ≤ "0"≤ +5.0V

Note: Pullup resistors to +5V may be optionally removed on all inputs and output.

Data: (24 lines)
Full parallel BCD (1-2-4-8), selectable positive or negative-true, 1 TTLLS load plus 10 K Ohm pullup to +5V. May be used with Form A (normally open) or Form B (normally closed) switch closure inputs. Level sensitive (rise-time non-critical). Data is stored.

Change Data Polarity: (Pin C1-B11)
Selects input polarity of data, decimal points and ± sign simultaneously.
LOW = positive true coding
HIGH = negative true coding

6 TTLS loads, plus 1K Ohm pullup to +5V, level sensitive

Print and Advance Command: (Pind C1-B14)
Level sensitive for Form A or Form B contact closure selectable positive or negative true.
1 TTLLS load plus 10K Ohm pullup to +5V.

Pulse Width: 1 microsecond to 200mSec (data must be valid 1 µsec after leading edge and 500 n Sec. before the print command).

Maximum print command rate: 3 per second
Paper advance automatically occurs after digit printing. Holding print command TRUE longer than the busy output is true (200 to 250 mSec. typ) causes continuous 4 lines/sec printing.

Change Print Polarity: (Pin C1-B7)
HIGH = negative true coding
LOW = positive true coding
1 TTLLS load, plus 10 K Ohm pullup to +5V, level sensitive.

Leading Zero Suppress: (Pin C1-B4)
blanks all leading zero's to the left of decimal point except a zero just left of the decimal point.
HIGH = Leading 0's blanked
LOW = full print (no suppression)
2 Low Power TTL loads, plus 10 K Ohm pullup to +5V, level sensitive.

Minus Sign: (Pin C1-B1)
Selectable positive or negative true using data level select input.
1 TTLS load plus 10 K Ohm pullup to +5V, level sensitive.

Plus Sign: (Pin C1-A5)
(Selectable positive or negative true using change data polarity input). (Minus sign must also be printed since it is used as the horizontal portion of the plus sign).
1 TTLS load plus 10 K Ohm pullup to +5V, level sensitive.
Note: Printing "plus" sign only results in vertical portion of plus sign. See above. Usable as 100% over-range digit.

Blanked Character:
Created by loading 1-1-1-1 in a given column. Can be hard-wired.

Decimal Points: (6 lines)
1 TTLS load plus 10 K Ohm pullup to +5V, level sensitive.
(Selectable positive or negative true using change data polarity inputs).

No-Print Paper Advance: (Pin C1-A3)
Ground this line .5µS to .1 sec. minimum to advance one line. Hold to ground for continuous advance at 6.7 lines per second.

No Print Paper Advance:
May also be created by loading the illegal BCD character 1-1-1-1 in all decimal locations, and disabling all decimal points and ± signs, then initiating a print/advance command.

Test: (Pin C2-B6)
LOW = ± .8 .8 .8 .8 .8 .8 printout when print/advance command is given.
1 TTLS load plus 10 K Ohm pullup to +5V, level sensitive (2 minutes max, this test, DPP-7)

Change Busy Polarity: (Pin C1-A2)
HIGH = positive true busy out
LOW = negative true busy out
1 TTLLS load, plus 10 K Ohm pullup to +5V, level sensitive.

10

OUTPUTS

DTL/TTL compatible

Positive true: 0V ≤ "0" ≤ +0.4V
+2.4 ≤ "1" ≤ +5.0V

Negative true: +2.4V ≤ "0" ≤ +5.0v
0V ≤ "1" ≤ +0.4V

Busy: (Pin C2-B12) Open collector TTL 7438 with 1 k ohm pullup to +5V)

Remains TRUE during print and advance cycle (approximately 200 to 250 milliseconds). Data inputs may be change 500 nanoseconds after transition to TRUE. Next print command can be enabled when busy goes FALSE. Selectable positive or negative true. 10 TTL loads.

Out of Paper: (Pin C2-B4)
The switch opens when approx. 6' (2m) of paper are left on roll. Paper roll visually indicates "low paper" within 10 to 15 feet (3 to 4.5m) of end of roll using red stripe on roll. Switch is in series with PC board contacts which disconnect if printer mechanism is not completely seated in case. Open switch contact or print mechanism removed will disable both local and remote print command. Pin C2-B4 has an internal 1 K ohm pullup to +5V normally grounded by switch before paper is low.

FRONT PANEL

Power On
Red light emitting diode illuminates when power is applied.

End of Paper
Yellow light emitting diode illuminates when the paper supply has 2" remaining at which time the printer stops printing.

Paper Roll Replacement:
By sliding out front panel printer assembly. PC board interlock automatically disconnects all power to printer assembly and power supply with electronics remain with housing case. Removal by a single front panel 1/4 turn thumbscrew.

Print/Remote/Advance
Front panel 3 position toggle switch, stable in center position (REMOTE), must be held in top (ADVANCE) or bottom (PRINT) positions.

ADVANCE:
When switch is held up, the printer continuously advances paper without printing at a 6.7 line per second rate.

REMOTE:
Center position enables all external inputs.

PRINT:
When switch is pushed down, printer prints one line and stops. After print and advance, external input is accepted even if the switch is held down.

TEMPERATURE RANGES

Operating: 0 to + 40°C (to +50°C at derated speed)
Storage: -25°C to +85°C (Paper darkens above +60°C)

Active printhead temperature sensor is employed to adjust drive energy to the existing head temperatures.

HEXADECIMAL PRINTOUT

Users requiring full alphanumeric printout (upper and lower case letters, numerals, punctuation and special characters should select Datel's model APP-20 thermal printer using a 5 X 7 dot matrix character format: The DPP-Q7 is also available as an extended numeric printout called hexadecimal which includes 6 extra letters (A through F) beyond the 10 numerals. Hexadecimal code is ideal for machine microprocessor systems. Because of the 7-segment format, the b and d must be lower case. Also, the 1-1-1-1 code will no longer blank a column, although leading zero suppression may be selected. The type 4 printout (.9.9.9 .9.9.9 decimal or .F.F.F .F.F.F hexadecimal) with a blanked center column is available for two data points printed on the same line.

Hexadecimal Coding

Input	Printout	Input	Printout
0000	0	1000	8
0001	1	1001	9
0010	2	1010	A
0011	3	1011	b
0100	4	1100	C
0101	5	1101	d
0110	6	1101	E
0111	7	1111	F

POWER SUPLY

DPP-Q7A:
105-125 VAC, 47-440 Hz @ 40 watts max (10 watts, typ standby) U.S.A. grounding line cord. Jumper-selectable* for 230 VAC.

DPP-Q7E:
205-240 VAC, 47-440 Hz @ 40 watts max (10 watts, typ standby). 2 prong with 8 gnd. shell line cord. Jumper-selectable* for 115 VAC.

DPP-Q7J:
90-110 VAC, 47-440 Hz @ 40 watts max (10 watts, typ standby)

AC Fuse:
DPP-Q7A/J: .25" x 1.25" Buss MDL or equivalent 1/2A SLO-BLO
DPP-Q7E: 1/4A SLO-BLO

Notes:
1. Case is grounded to AC power ground
2. +5V, 200mA max. logic power out available

*Jumpers are located in the printer housing and are accessable when the print module is removed.

CONNECTORS

Data and Controls:
(2)30-conductor (15 per side)
Double-sided PC board connectors.
0.1" centers. Datel #58-2073083 (included)

AC Power
Supplied captive line cord with European or U.S.A. plug.

WEIGHT (with housing and full paper roll)
4.4 lbs. (2,0 kg)

DIMENSIONS

Front panel mounting cutout:
4.50" W x 2.72" H (115 mm x 69 mm)

Front panel Bezel dimensions:
5.25" W x 2.82" H (134 mm x 72 mm)

Depth behind front surface of mounting panel including clearance for rear PC connectors and fuses:
8.7" (221 mm)

MODEL NUMBER

DPP-Q7 ____ ____ ____

Power Supply

A = 115 VAC*
B = 230 VAC*
J = 100 VAC

Printout Format

1 = ±.9.9.9.9.9.9
2 = .9.9±.9.9.9.9
3 = .9±.9.9.9.9.9
4 = .9.9.9 .9.9.9
5 = .9.9.9.9 .9.9
6 = .9.9.9.9.9 .9

Characters

Leave Blank } = Decimal Digits

H = Hexadecimal Digits

DPP-Q7A, E, or J

OEM Versions available (same prices)
DDP-Q7-9554.....no panel belt
DPP-Q7-9555.....no connectors
DPP-Q7-9556.....no label, no connectors

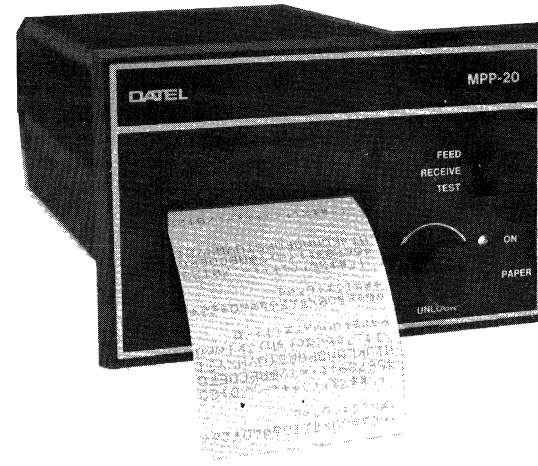
*Include jumper-selectable dual voltage 115/230V transformers

DPP-Q7 Printer stand for bench-top applications.....33-8193200

APP-TR1A Automatic take-up reel/Rewind accessory, 115 VAC powered.
APP-TR1E Automatic take-up reel/Rewind accessory, 230 VAC powered.

MPP-20
Low-Cost Serial/Parallel Input 20-Column Thermal Printer

DATEL



FEATURES

- **Two communications modes:**
  - **RS-232-C serial**
  - **Centronics® -compatible parallel**
- **No external interface logic required**
- **Two character sizes, 20-characters per line**
- **Prints full 96-character ASCII set with 31 additional special characters**
- **Enhanced and inverted character output formats via data-encoded commands**
- **Front panel SELF-TEST and FEED controls**
- **SUPERTORQUE mode for operation in sub-zero temperatures**
- **AC- or dc-powered models**
- **Rugged, lightweight 4.2 pounds design**
- **Low cost**
- **Very high OEM reliability**
- **Quiet, virtually maintenance-free operation**

The MPP-20 Thermal Printer is the newest addition to DATEL's proven line of OEM-reliable thermal printers. Able to communicate in both serial and parallel modes, the low-cost MPP-20 thermal printer's rugged construction, variable output styles, and ease of application make it the choice of OEM's and end-users alike.

GENERAL DESCRIPTION

Able to use the full set of 96 ASCII characters and 31 special characters, the device prints output characters on 2-5/16 inch wide (58,6mm) thermal printer (see Figure 1). The printout has 20 columns of characters with the print rate varying as a function of the print format selected. Whether operating in the serial or parallel mode, all signals interface with the device via a single connector which attaches to the rear of the enclosure. The user accomplishes all unit wiring using a 30-pin card-edge connector (included).

The MPP-20 uses microprocessor-driven logic for timing character generation, printhead drive, and motor stepping. This technology accounts for the small size of the MPP-20 printer, at the same time making it easy to install and maintain.

The serial mode of operation uses straightforward two-, three-, or four-wire cabling schemes. One line carries serial transmissions of data to the MPP-20. Two other lines provide handshaking and status monitoring while the fourth is a system ground. The host queries the MPP-20 to detect when it is ready to accept data.

When ready, the MPP-20 loads one printable line of characters (20 columns wide) into an internal data buffer. The MPP-20 then halts any data input for a short period of time while it prints the line and advances the paper one line.

Parallel data operations are designed to be compatible with the Centronics® data bus configuration. This configuration has become an accepted de-facto standard for simple data transmission. The data is present on the data bus in the form of an eight-bit word. The MPP-20 loads and interprets the data word upon receipt of a strobe signal from the host. The MPP-20 issues a negative going acknowledge pulse upon storage of each character.

In either mode, the MPP-20 interprets the received ASCII code into a printable character via a look-up table resident in the microprocessor's memory. The character is then fed to the print control logic for storage in a print buffer. After storing 20 consecutive characters (or spaces, punctuation, etc.), the print head burns an image of the characters onto the termperature-sensitive paper. The print drive logic controls a stepper motor which in turn drives the paper roll. The speed at which the motor turns is directly a function of the various output attributes selected (see Table 1). Selection of some attributes, such as ENHANCED feature, require longer burning time thus affecting the overall throughput rate. For instance, selecting the SUPERTORQUE attribute, used to drive the motor slowly in colder environments, would also add to the total throughput.

ORDERING GUIDE

MODEL	DESCRIPTION
MPP-20A	115 VAC-powered, USA-type power cord and plug included
MPP-20D	+10.5 to +15V dc-powered, Molex connector and pins included
MPP-20E	230 VAC-powered, European-type power cord and plug included
MPP-20J	100 VAC-powered, USA-type power cord and plug included
32-2242572	Black printout paper, 10 rolls
58-2073083	Connector, input/output, dual 15 pin 0.100 inches on center, cardedge type (one included with each printer)
APP-TR2A/E/D/J	Take-up/Rewind Reel

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS
(Typical at 25°C)

Parameter	Min.	Typ.	Max.	Units
PRINTOUT				
Print Rate (1)				
Normal Size	-	90	-	lines/ minute
Tall	-	50	-	lines/ minute
Line Density				
Normal Size	-	7	-	lines/inch
	-	3	-	lines/inch
Tall	-	3.8	-	lines/inch
	-	1.2	-	lines/inch
Line-to-Line Spacing				
Normal Size	-	0.14	-	inches
	-	3.6	-	mm
Tall	-	0.26	-	inches
	-	6.5	-	mm
Character Size				
Height, Normal	-	0.10	-	inches
		2.5	-	mm
Height, Tall	-	0.20	-	inches
	-	5.1	-	mm
Character Format	-	5 X 7	-	dot matrix
Character				
Horizontal Spacing	-	2.8	-	mm
	-	0.11	-	inches
Line Feed Cycle Time			see	
Normal	-	370	table	ms
Tall	-	680	1	m
POWER CONSUMPTION				
AC Models	-	-	5.8	watts, idling
	-	-	17	watts, printing
DC Models	-	-	400	mA, idling
	-	-	1.6	amps, printing
POWER REQUIREMENTS				
MPP-20A	105	115	130	Voltts
MPP-20E	200	220	250	Volts
Frequency Range	47	-	440	Hertz
MPP-20J	90	100	110	Volts
Frequency	47	-	440	Hertz
MPP-20D	+10.5	+12	+15	Volts, dc regulated

VOLTAGE LEVELS
(TTL- and TTLS- compatible)

Parameter	Min.	Typ.	Max.	Units
Input Logic				
Low	0	-	+0.8	Volts dc (logic 0, or False)
High	+24	-	+5.0	Volts dc (logic 1, or True)
Outputs				
Low	0	-	+0.4	Volts dc (logic 0, or False)
High	+24	-	+5.0	Volts dc (logic 1, or True)
PRINT MECHANISM				
Printhead Life	30×10^6	-	-	character life
Mechanism Life	5000	-	-	hours
ENVIRONMENT				
Temperature Range(2,4)				
Operating	-20	+25	+50	Degrees Celcius
Storage	-45	-	+85	Degrees Celcius
Relative Humidity no condensation	0	-	90	Percent
PAPER				
Data Capacity (3)				
Normal Size	-	-	10,600	Lines
Tall	- 2.31 inches by 140 foot			
Size	Black on white, DATEL number			
Type	32-2242572			

NOTES
1. Transmission at 9600 baud.
2. Paper darkens after 48 hours of exposure to temperatures exceeding +60 degrees Celcius.
3. Capacity dependent upon the mix of normal and tall characters.
4. +50 degrees Celcius operation is for continuous operation. Derated throughput is usable up to +55 degrees Celcius.

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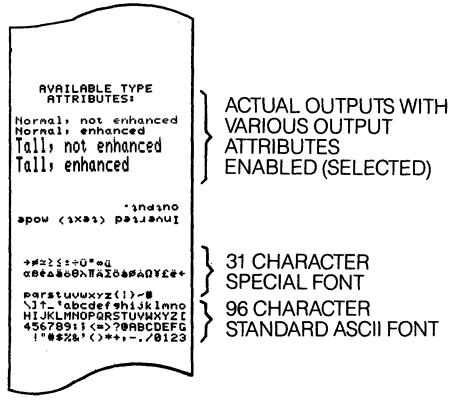

Figure 1. MPP-20 Sample Printouts

Table 1. Throughput Rate Variations

Output Character Attribute	Normal Size: Millisecs added to basic cycle	Normal Size: Equiv. through-put lines/sec.	Tall Size: Millisecs added to basic cycle	Tall Size: Equiv. through-put lines/sec.	Notes
Std Size	0	1.5	-	-	-
Tall Size	-	-	543	.86	1,3,4
Enhanced	560	.85	1081	.45	4
Supertorque	116	1.35	240	.71	5
Special Font	91	1.4	180	.74	2,3

NOTES

1. Figure given is worst case, i.e., full line of tall characters. Minor variations occur with fewer tall characters per line.
2. Same speed reduction occurs regardless of proportion of standard and special characters.
3. All figures are for full lines of printable characters.
4. Two burns take place for each dot of character formation. Between burns in a pair, the paper makes a half increment so as to fill in the gaps with redundant marks. When enhancement is added to tall characters, quadruple burns are generated at each character-mapping point.
5. Supertorque is state of lowered step motor frequency. It executes by trebling the time delay in the paper motion subroutines.

The basic print cycle at 9600 Baud lasts 667 milliseconds. This serial mode print cycle reflects a 640 ms-long busy state and a 27 ms-long ready state.

Internal power supplies provide the various voltages used by the logic stepping motor and printhead. These supplies also provide an external +5 volts dc at 100 mA for user needs.

TTL Compatiblity

All input/output signals, whether data or control, are designed to be fully TTL compatible. Table 2 lists the signals and their nominal current levels.

Table 2. TTL Signal Levels

MPP-20 SIGNAL	Input Current Low (mA)
TEXT/$\overline{\text{LIST}}$	0.5
$\overline{\text{EOP}}$	1.6
NEG/POS TRUE	0.7
$\overline{\text{DATASTROBE}}$	5
TALL CHARACTER	0.5
DATA BITS	0.5
BAUD RATE PINS	−0.7
CR/$\overline{\text{CRLF}}$	0.5
$\overline{\text{SO SUPPRESS}}$	0.5

Interface Specifications

$\overline{\text{RS}}$-232-C RDY/$\overline{\text{BSY}}$ (Pin A2):

Voltage Output (High)	+4.5 volts dc with 3K ohm terminator +4.75 volts dc open circuit, 330 ohms source resistance
Voltage Output (Low)	−5.5 volts dc with 3K ohm terminator −12 volts dc open circuit, 3K ohms source resistance
ACTIVE PRINTING (Pin B9):	
(High)	+5.0 volts dc (from 2K ohms source)
(Low)	0 to +0.5 volts dc
Current Output (Low)	10 mA at 0.45 V dc

$\overline{\text{ACK}}$ (Pin B3):

Voltage Output (High)	+5.0 volts dc (from 500 ohms source)
Voltage Output (Low)	+0.4 volts dc (sinking 20 mA)
Voltage Output (Low)	+0.9 volts dc (sinking 80 mA)
BUSY (Pin A9):	Signal levels same as $\overline{\text{ACK}}$ (Pin B3)

OPERATIONAL DESCRIPTION

Pin Functions:

Outputs

$\overline{\text{EOP}}$ (Pin B6): This pin switches to logic ground when the paper (End Of Paper) supply is nearly exhausted, providing a 0.5 volt dc source at 50 mA for external alarming. This signal is not available after withdrawing the print module for paper renewal. In systems where this is an inconvenience, the circuit shown in Figure 3 may be added at the MPP-20 user connector.

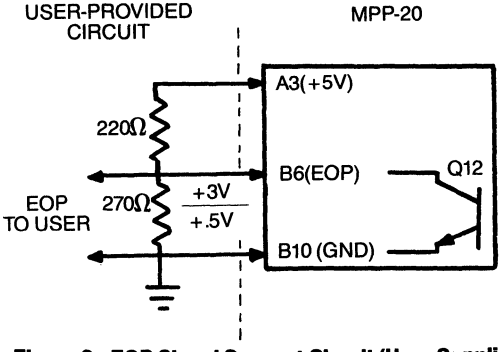

Figure 3. EOP Signal Support Circuit (User-Supplied)

With this circuit in place and the print module present but out of paper, the EOP state supports approximately 15 TTL loads (24 mA). Removing the print module assembly results in pins A3, B6, and B10 being disconnected. The circuit shown in Figure 3 supports approximately 1 TTL load (1.6mA).

XON/XOFF (Pin A7): The MPP-20 uses this serial control line to notify the user of its status. Three basic conditions trigger activity on this line:

1) At completion of any lengthy operation, such as printing, the MPP-20 issues an XON control character to the user.
2) Upon receipt of an XON control character from the user device, the MPP-20 echoes a single XON, indicating that the printer is ready to receive.
3) The MPP-20 issues a single XOFF whenever the MPP-20 enters the busy state for reasons uncontrolled by user software. Typically, TEST, FEED, and EOP conditions trigger this state.

Inputs

$\overline{\text{SUPERTORQ}}$ (Pin B7): Grounding this pin lowers the paper feed stepper motor frequency, providing extra torque in cold environments if necessary. Printer throughput is somewhat reduced. This pin is normally at a TTL high level (+5 Volts dc.) See Table 1.

$\overline{\text{ENHANCE}}$ (Pin B8): If this pin is logically low when the print cycle begins, the line prints bold by performing a double burn of each dot.

TEXT/$\overline{\text{LIST}}$ (Pin B2): A logic low on this pin puts the printer in LISTER mode, which causes the characters to appear right side up when viewed from the front panel. The most recent line printed appears at the top of the printout while the first line appears at the bottom.

Floating the pin (no connection = high) puts the printer in the TEXT mode. In this mode, the characters appear upside down when viewed from the front panel. Removing the paper from the printer and inverting it so that the characters are right side up, the printout appears as normal text. Definition of the print direction must be established before starting the print cycle.

NEG/$\overline{\text{POS}}$ TRUE: (Pin A8) Parallel data may be sent either positive or negative true. Parallel data may be inverted, for Centronics-compatibility (positive-true data operation), by tying this pin to logic ground.

$\overline{\text{SO SUPPRESS}}$: (Pin A15) A logic low on this pin prevents SO characters from taking effect. Does not affect the tall character select line, pin B11.

TALL CHARACTER: (Pin B11) The TTL signal on this pin identifies characters as tall or normal (high for tall) as an alternative to SO/SI codes. This line also functions during serial operation and overrides the SI control character (but not the SO). With the NEG/POS TRUE pin A8 floated (high), tall characters are not available, and SO/SI therefore takes control. Centronics-compatibility requires that this pin be grounded whenever positive true data is selected (pin A8 grounded).

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Control Characters

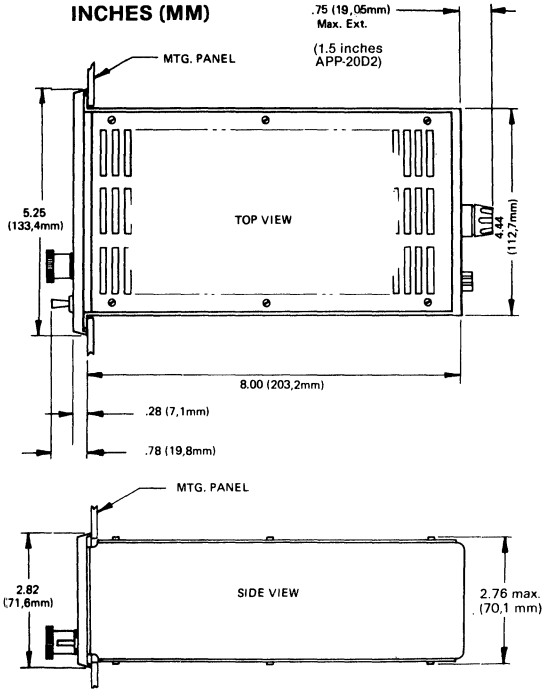
The MPP-20 responds to a set of 15 specific control characters, each causing the printer to perform a specific function. These functions, their mnemonics, and hexidecimal codes appear in Table 3.

Table 3. MPP-20 Responses to Control Characters

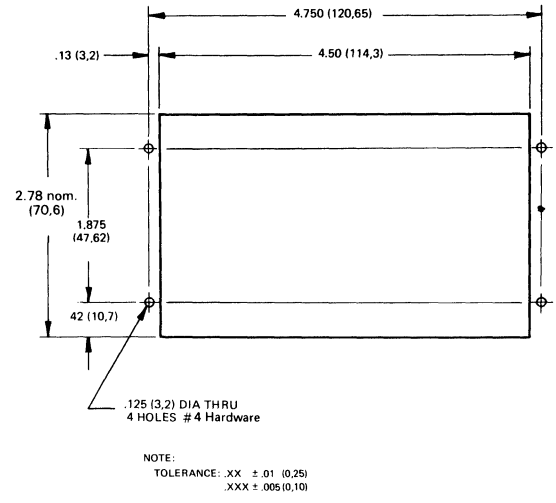
MNEMONIC	HEX CODE	NAME	ACTION PRODUCED
NUL	00	Null	None
BS	08	Backspace	Moves the column pointer back one position, deleting one character. On reaching column 1, the printer ignores subsequent BS commands.
HT	09	Horizontal Tab	Successively indexes the column pointer to positions 1, 4, 9, 15, and 20. Upon reaching position 20, the printer no longer responds to HT.
LF	0A	Linefeed	Advances the paper by one line. The amount of paper fed increases if tall characters have been requested by either invoking the SO state or if a logical "1" is the MSB of the parallel data input (bit 7, pin B11.) LF clears the line buffer without printing and resets the character column pointer to column 1.
VT	0B	Vertical Tab	Causes the printer to skip 5 lines. Does not print the data in the buffer; therefore, it is lost unless first printed as a result of receiving a CR. Upon receipt, cancels any existing SO, DC2, and SUB flags in the flag register. The column pointer resets to position 1. Head of form sensor will interrupt VT.
FF	0C	Form Feed	Same as VT except skips 11 lines. Head of form sense interrupts FF.
CR	0D	Carriage Return	Initiates printout of characters in line buffer and causes a line feed.
SO	0E	Shift Out	Sets the tall character mode. Cancel lable either by SI, VT, FF, or RS. Using the SO/SI control characters allows mixing tall and normal sized characters on the same line. Grounding pin A15 (SO SUPPRESS) at the user connector suppresses the tall character selection option. The SO state can be locked on (in both serial and parallel modes) by holding parallel data bit 7 at logic 0 at the user connector, pin B11.
SI	0F	Shift In	Cancels SO state. Unit powers up in SI state.
DC1	11	Device Control 1	Causes the printer to return an XON in the serial mode one time if idle.
		(XON)	Useful in systems that cannot monitor the RS-232 signal input line.
DC2	12	Enhanced Print Request	Prints an entire line bold if this character is received any time before CR. Self-clearing after each line.
DC4	14	Cancel Enhance Request	Cancels the enhanced mode.
SUB	1A	Substitute	Shifts to the alternate set of 31 special characters, if not disabled by solder-gap SG2 closure.
CAN	1B	Cancel	Shifts back to the standard set of ASCII characters. This is the power-up default condition.
RS	1E	Paper Feed	Causes a paper feed. Cancels DC2, SO, and SUB flags in the flag register. Feed ends after: 1) 84 lines (12") are fed, or 2) A head of form sensor returns a "stop" before 84 lines, or 3) 2 lines are fed with a "stop" signal strapped low.

APP-20 Series

OUTLINE DIMENSIONS
INCHES (MM)

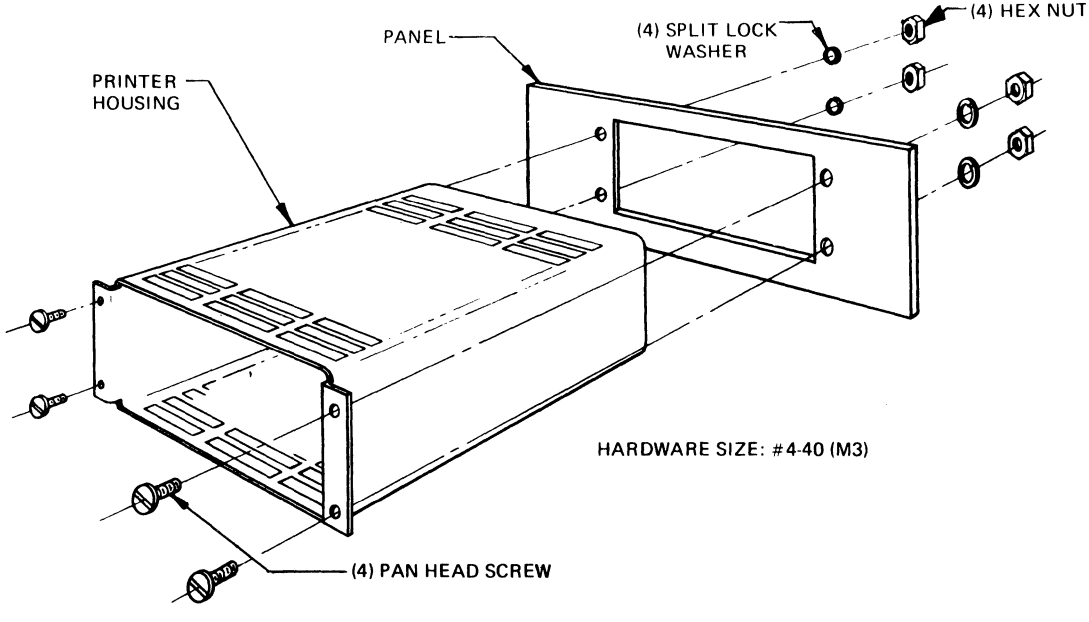


PANEL CUTOUT



NOTE:
TOLERANCE: .XX ±.01 (0,25)
.XXX ±.005 (0,10)

MOUNTING DETAILS



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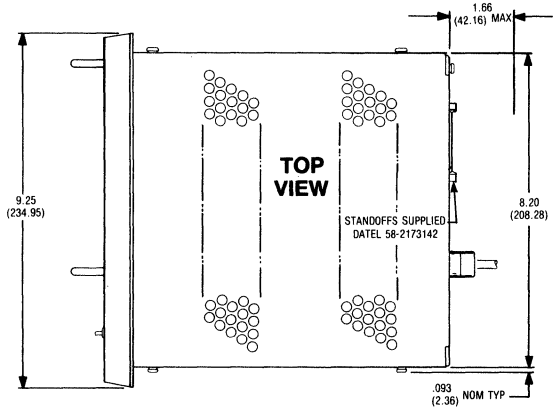
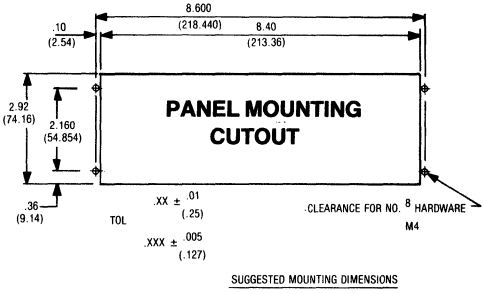
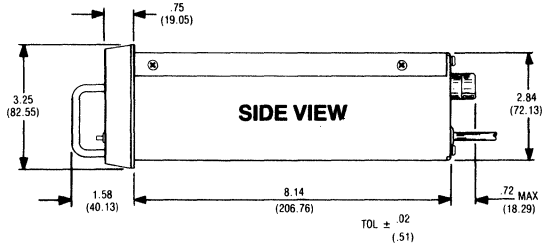
APP-48 Series

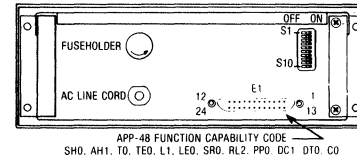
MECHANICAL DIMENSIONS — INCHES (MM)



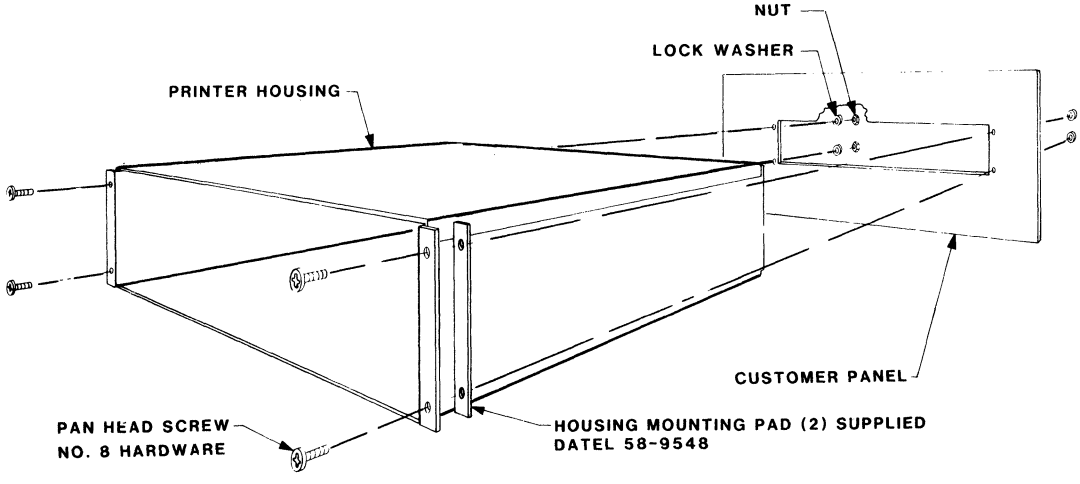




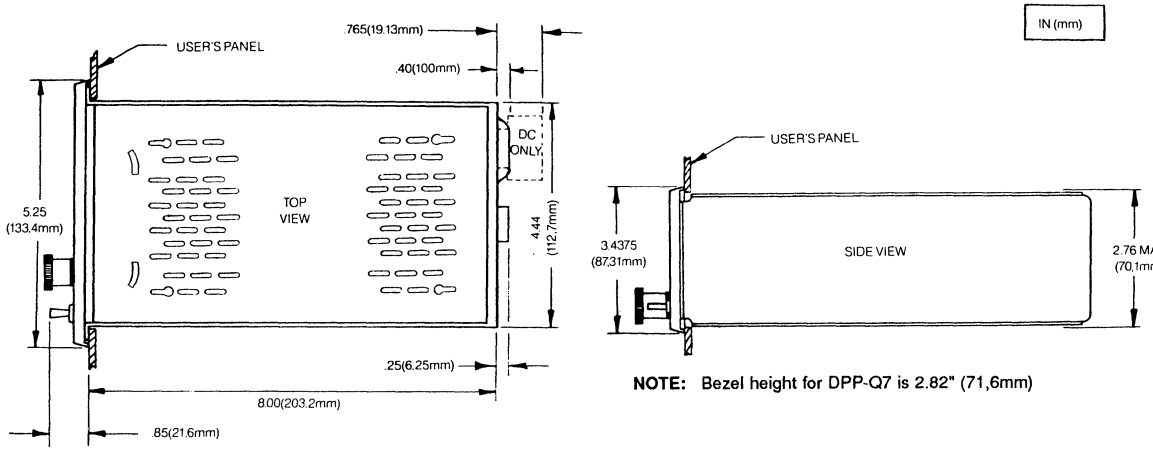
PRINTER REAR VIEW



MOUNTING DETAILS



Physical Dimensions



NOTE: Bezel height for DPP-Q7 is 2.82" (71,6mm)

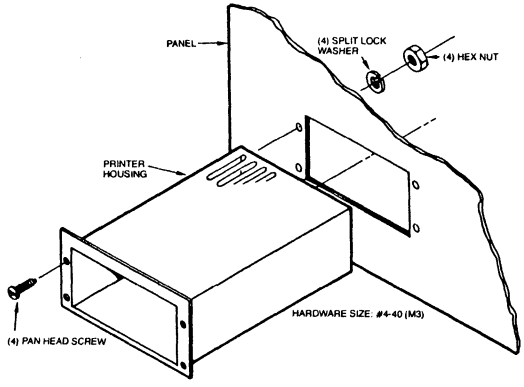
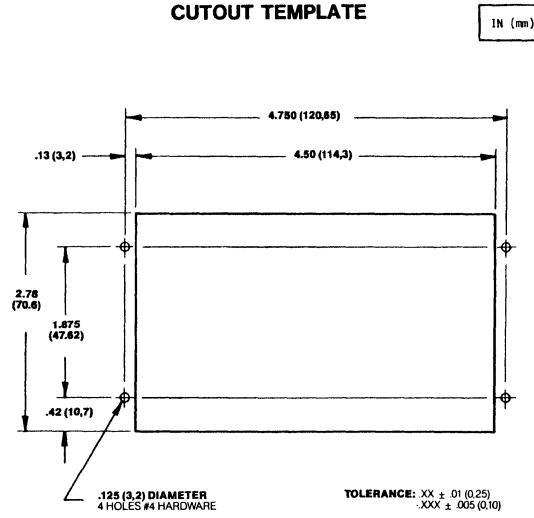


Figure 11. MPP-20 Mounting Details

CUTOUT TEMPLATE



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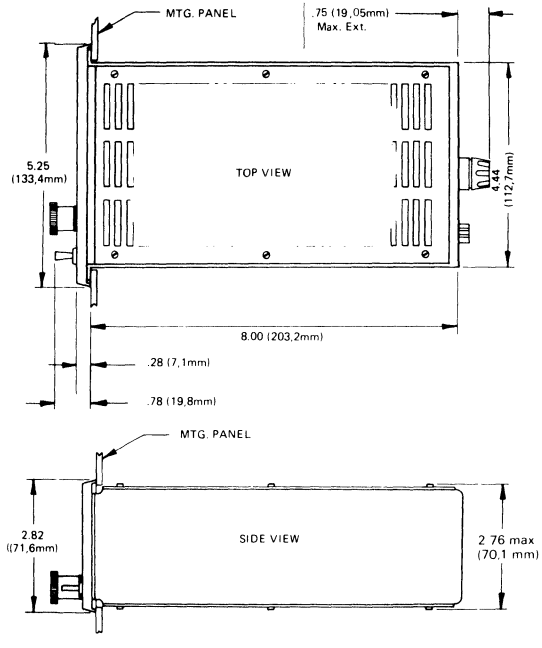
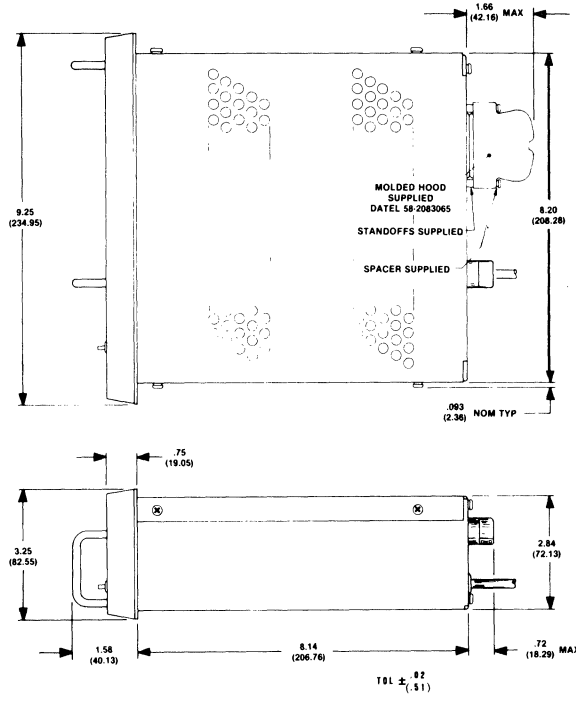
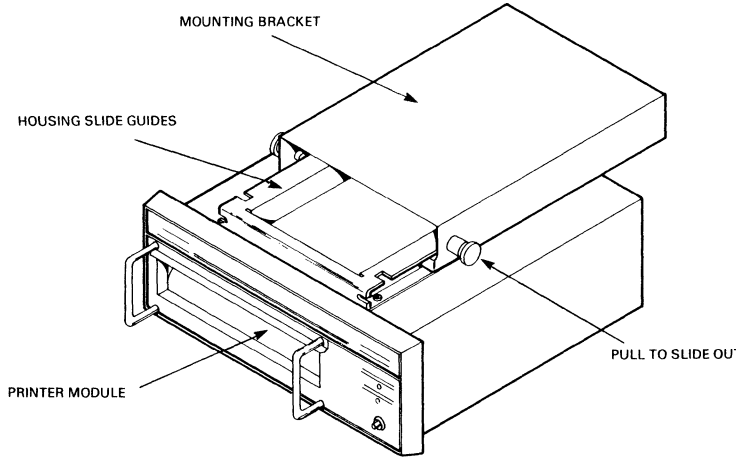
APP-M20 Series



APP-M48 Series

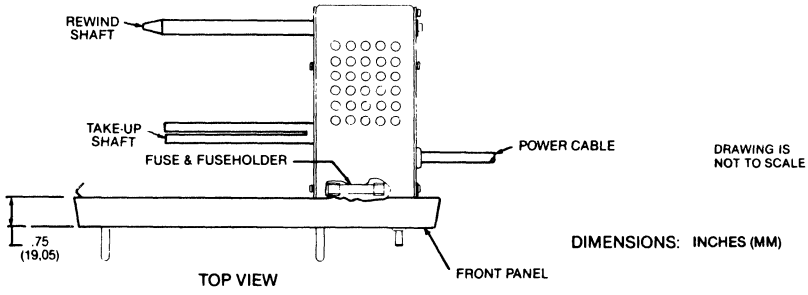


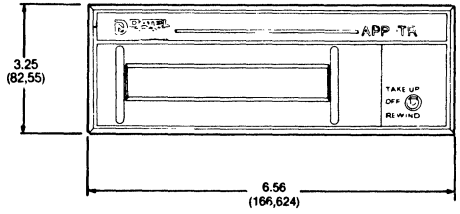
MOUNTING BRACKET

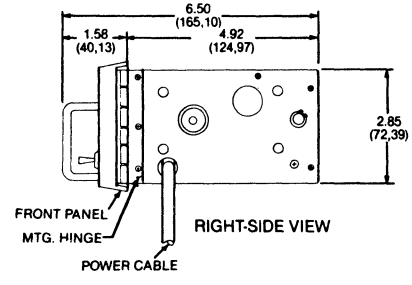


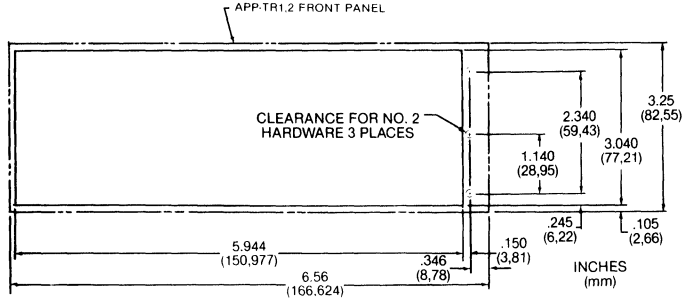
APP-TR1,-TR2

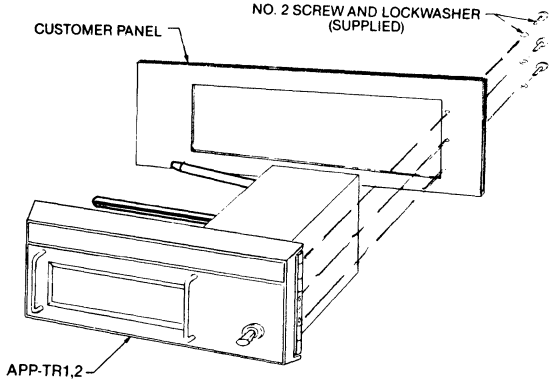
OUTLINE DIMENSIONS-INCHES (MM)











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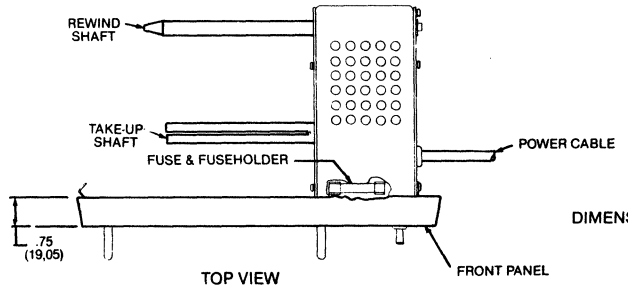
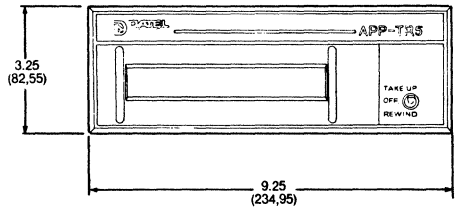
APP-TR5

OUTLINE DIMENSIONS-INCHES (MM)

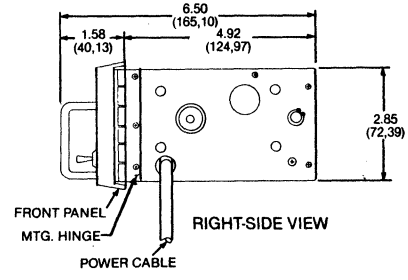


TOP VIEW

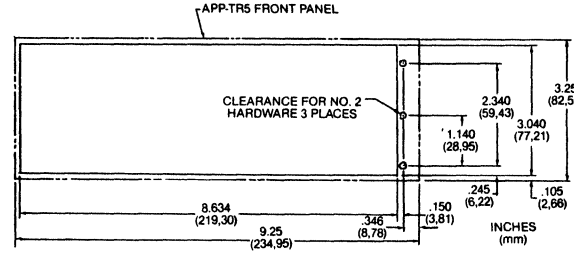
DIMENSIONS: INCHES (MM)

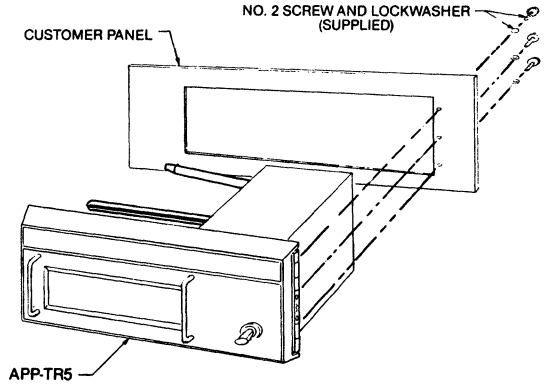


FRONT VIEW



RIGHT-SIDE VIEW

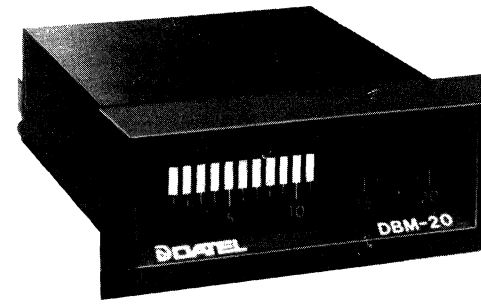




DBM-20
20 Segment LED Bar Meter with TTL Outputs

FEATURES

- **20-segment, high-intensity analog bar graph display**
- **TTL outputs for process control or alarm circuits**
- **Adjustable input range from +0.1 to +2.4V dc full-scale. Higher voltage and current ranges (including 4–20 mA) with user-installed options**
- **Instant response with no overshoot**



DESCRIPTION

The DBM-20 Bar Meter is a panel-mounted, self-illuminated 20-segment red LED (Light Emitting Diode) bar display. It accepts a dc or slowly varying input signal, converts that signal to digital form and displays it in the form of a progression of lighted LED segments arranged to shape a single bar graph.

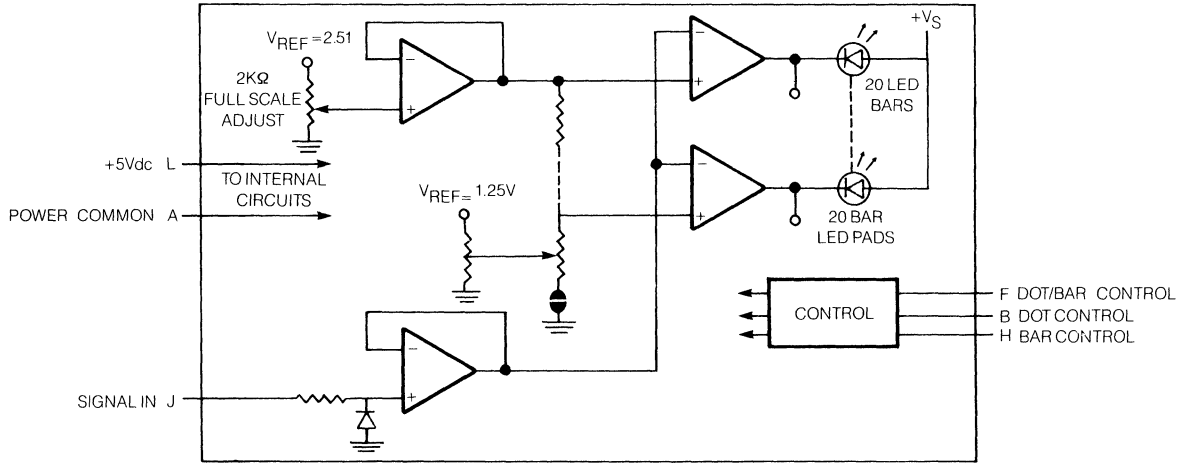
The DBM-20 is particularly well-suited for trend measurement, where relative changes in the measured variable must be easily recognized. Applications of this type include measurement of belt speed, noise level, pollution effluent and the like.

The DBM-20 contains 20 TTL driver pads corresponding to the 20 bar graph LED segments. TTL outputs can be wired from the pads to any of the four unused finger connectors. These outputs can be used as setpoint trips in simple control loops, or to control alarm circuits. The meter also provides internal pads for the installation of additional logic circuitry, such as TTL comparitors, DIP relays, and driver ICs, to be used in conjunction with the TTL outputs.

The DBM-20 features an adjustable input range from +0.1 to +2.4V dc full scale. Other voltage and current ranges (including 4–20 mA) are easily obtained by installing resistors/potentiometer on the provided locations. The inputs provide high input impedance (100 KΩ, minimum) and a low input bias current (10 nA, typical). The DBM-20's input configuration is single-ended unipolar.

The meter displays an instant response with no overshoot. The user has a choice of either a Bar mode display or Dot mode display. In the Bar mode, all LED's will light up from the left of the display up to the high end of the input signal. In the Dot mode, only the LED at the high end of the input signal will light.

A red optical display filter has 20-unit graduation markings in white. The filter may be changed by opening the housing from the rear. The low-profile housing is a rugged, black polycarbonate case that is impact and solvent resistent. Its dimensions are 2.53"W x 3.34"D x 0.94"H. Panel mounting cutout dimensions are 2.56"W x 0.97"H.



Simplified Block Diagram of DBM-20

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FUNCTIONAL SPECIFICATIONS
(Typical at +25°C unless noted)

INPUT CHARACTERISTICS
Input Voltage Range..... Adjustable +100 mV dc to +2.4V dc Full Scale, Unipolar (R3 at rear of instrument sets the Full Scale). Higher voltage and current inputs (including 4–20 mA) are easily configured with user-installed options. Factory-installed range changes available in OEM quantities.
Input Impedance..... 100 KΩ min.
Input Bias Current..... 10 nA typ, 50 nA max.
Input Configuration..... Single-ended
Input Offset Voltage..... Solder-gapped to signal ground. May be adjustable 0 to +1.25V dc with addition of a 1 KΩ user-installed pot.
LED Trip Point Nonlinearity..... 0.5% typ, 2% max.
Input Overvoltage..... ±35V max.
Temperature Coefficient..... 1% of Full Scale, 0 to +50°C

DISPLAY
Type..... 20 self-illuminated red light-emtiing diodes (LED). Segment size 0.20"H x 0.07"W.
Modes
Bar:..... All LED's light starting from the display left side, according to the input voltage (Connect pin L, F and H).
Dot:..... Only one LED lights starting from the left side according to the input voltage (Connect pins B and F).

INPUT/OUTPUT CONNECTIONS
Pin A..... Power and Signal Common.
Pin F..... Dot/Bar Control.
Dot mode..... Connect pins B and F.
Bar mode..... Connect pins F, L and H.
Pin J..... Signal Input.
Pin L..... +5 V dc Power Input.
Pins B, C, D, E, H, K..... Connected to drilled internal PCB pads for user circuits.

PHYSICAL/ENVIRONMENTAL
Input/Output Connector..... Edgeboard PC type using bottom side only. 10-pins, 0.156" centers, DATEL model 58-2073082 or equivalent (included).
Case Material..... Black polycarbonate plastic, impact and solvent resistant.
Case Outline Dimensions (Less Bezel)..... 2.53"W x 3.34"D x 0.94"H (64,3 x 84,8 x 23,8 mm)
Front Panel Mounting Cutout..... 2.56"W x 0.97"H min. (65,1 x 24,6 mm). Thickness range 0.062" to 0.625" (1,6 to 15,9 mm).
Bezel Dimensions..... 1.32"H x 2.92"W x 0.157"D (33,5 x 74,2 x 4 mm)
User Circuits..... 4 Internal uncommitted 14-pin DIP pads are drilled for user circuits such as DIP relays and a driver IC (to be used in conjunction with the 20 TTL outputs).
Power required..... +5V dc ±0.25V dc at 250 mA typ, regulated (unregulated power supplies cannot be used because of display switching currents).
Operating Temperature Range..... 0 to +50°C.
Storage Temperature Range..... -25°C to +85°C.

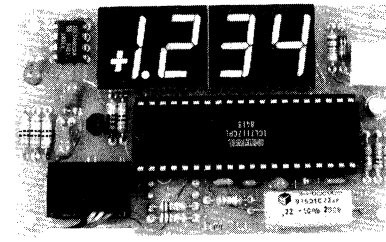
ORDERING GUIDE

MODEL	DESCRIPTION
DBM-20	20-segment LED bar meter (includes one connector)
UPA-5/500	115 VAC to +5V dc power adapter (not included)
58-2073082	Edgeboard connector, 10 pins

DM-31
Single Board, 3½ Digit LED Panel Meter

FEATURES

- **Compact single board design**
- **0.56" bright red 3½ digit display**
- **Fits into most panel cutouts**
- **80 dB CMRR**
- **True balanced high-impedance inputs**
- **Logic powered (+5V dc @ 280mA)**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**



GENERAL DESCRIPTION

The DM-31 is a low-cost single board DPM. The DPM adapts easily into most test instruments and data acquisition systems.

Its compact dimensions (2" x 3.5" x 0.5") let the DPM be easily installed into most panel cutouts. The DM-31 has provisions for modifying the voltage and current ranges.

APPLICATIONS

The DM-31 may be used for any application where a physical or electrical parameter needs to be measured and can be converted with user-supplied external circuits into the basic dc voltage, current or resistance ranges which the DM-31 accepts and displays. Such parameters include temperature, pressure, flow rate, RPM, noise, weight, velocity, frequency and many others. The DM-31 is intended for applications in analytical instruments, test and measurement equipment, data acquisition systems, research and development instrumentation, laboratory analyzers and other devices. Industries using the DM-31 include petrochemical, power utilities, batch and continuous processing, telecommunications, paper, glass, metals and chemical manufacturing, photographic, automotive and medical services.

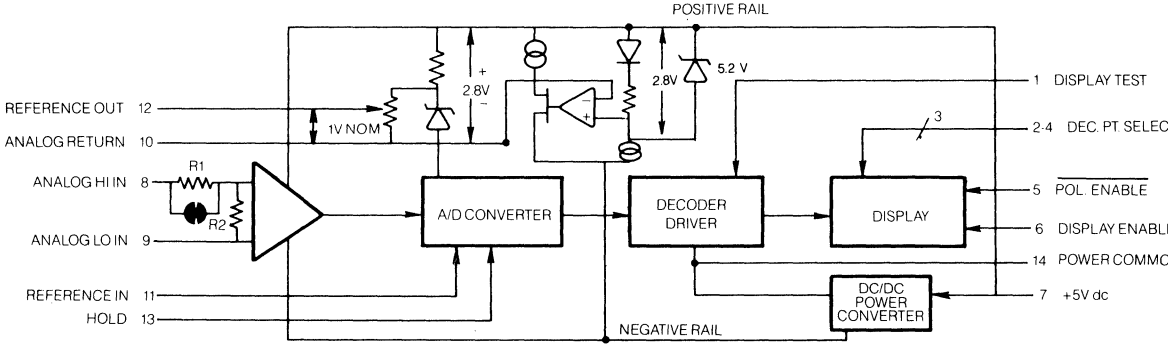
ORDERING INFORMATION

DM-31 - 1

Model	Description
DM-31-1	Single-Board Digital Panel Meter (including plug connector)

ACCESSORIES

Part Number	Description
39-2106705	14-pin dip connector
UPA-5/500	115V AC to +5V dc power adaptor
39-8194910	DM-31 mounting accessory kit



Simplified Block Diagram of a DM-31

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.

Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical) 50 pA (maximum)

Input Overvoltage ..... ±250V dc, l75V RMS continuous (maximum) ±300V intermittent (maximum)

External Reference Range ..... ±100 mV to ±2V referred to -Vs

Common-Mode Rejection ..... 80 dB (typical), from dc to 60 Hz, with a 1 Kilohm unbalanced input

Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.

Resolution ..... 1 mV

Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count

Temperature Drift of Zero ..... Autozeroed ±1 count over a 0° to +50°C temperature range

Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)

Sampling Time ..... 83.3 mS (nominal)

Sampling Rate ..... 3 conversions per second. May be rewired for up to 20 conversions per second

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)

Decimal Points ..... Selectable using decimal point select signal lines.

Display Type ..... LED (red, high efficiency)

Display Height ..... 0.56" (14,2 mm)

Overscale ..... Inputs exceeding the full-scale range display a "+1" MSD with other digits blanked.

Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

Power Consumption .... +5V dc nominal, -1, +2V regulated required. Logic spikes must not exceed 50 mV. Use an external bypass capacitor or other means to attenuate noise. Current at 5V is 280 mA average, 450 mA maximum. Current varies rapidly as digits switch so that unregulated supplies cannot be used. Current is approximately 5 mA with displays blanked.

PHYSICAL

External Dimensions
3.5"W x 2"H x 0.5"D (88,9 x 50,8 x 12,7 mm)

Panel Cutout Dimensions (For Optional Bezel/Filter)
1.156"H x 2.375"W (29,36 x 60,33 mm) Bezel/Panel thickness 0.040" to 0.062" (1,0 to 1,6 mm) (snug fit at 0.062")

Optional Snap-In Bezel/Filter Dimensions
Outside dimensions: 1.343"H x 2.531"W (34,1 x 64,3 mm) Display opening: 0.812"H x 2.0"W (20,6 x 50,8 mm) Front panel bezel relief height: 0.062" (1,6 mm)

Mounting Kit
Optional, includes bezel/filter, DIP connector, standoffs, and hardware. See Ordering Information.

Weight
1.2 ounces (35g)

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0° to 50°C)

Storage Temperature Range
-13°F to +185°F (-25°C to 85°C)

Relative Humidity
10% to 90% non-condensing

DM-3100B/DM-3104
AC powered, 3½ Digit LED Panel Meters

FEATURES

- **3½ Digit red LED (DM-3100B) and high brightness red LED (DM-3104) models**
- **Selectable 115/230VAC powered**
- **Balanced high-impedance differential inputs**
- **80 dB CMRR**
- **Autozeroing capability**
- **Allows ratiometric reference for drift correction**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**

GENERAL DESCRIPTION

The DM-3100B and the DM-3104 are 3½ digit LED display devices. The DPM's are dual AC-powered DPM's, easily configurable for a variety of applications. The versatility is due to logic power outputs (+5V dc and -5V dc) provided by the DPM.

The DM-3100B and the DM-3104 use 0.56" and 0.6" display respectively. The displays are clearly visible from many feet away in normal or dim light.

Inputs to the DPM's are balanced differential (80 dB Common Mode Rejection). The meter accurately displays small signals even in electrically noisy industrial environments. CMOS circuitry results in an extremely high input impedance (1000 Megohms, typically) and a very low bias current (5 picoamps). Inputs with a source impedance as high as 100 kilohms can be displayed accurately. The input circuitry safely tolerates overvoltages up to ±250V dc (155V RMS). Inputs are sampled and displayed about four times per second.

The DPM's are designed for installations where existing dc supplies are noisy, inaccessible, or overloaded. The meters may be used wherever a voltage, or a unit which can be made proportional to voltage, must be displayed with accuracy and clarity.

The DPM's are supplied in DATEL's standard short depth black polycarbonate case.

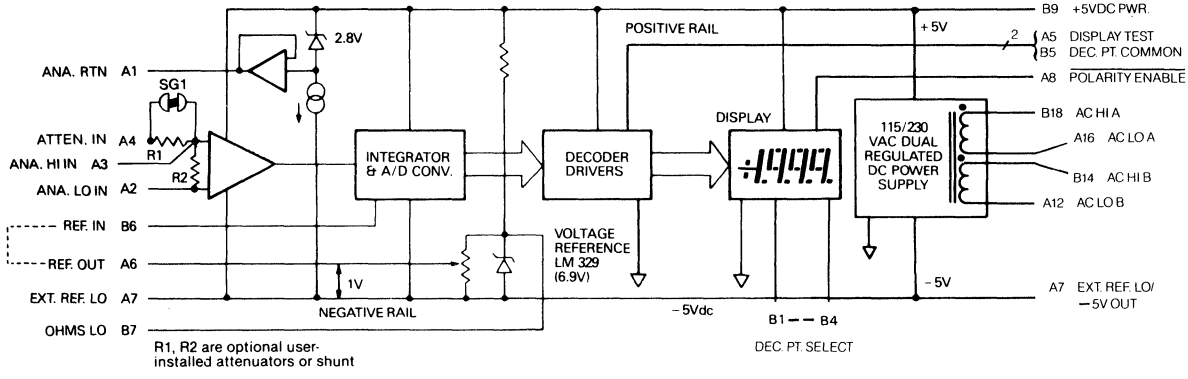
ORDERING INFORMATION

DM-3100B - 1
DM-3104-1

Model	Description
DM-3100B-1	3 1/2 Digit, LED, 115/230 V AC powered (includes one connector
DM-3104-1	3 1/2 Digit, LED high brightness, 115/230 V AC powered (includes one connector)

ACCESSORIES

Part Number	Description
58-2075010	Connector, dual 18-pin, 0.1" centers
UPA-5/500	115V AC to ±5V dc (@ 500 mA) power adaptor



Simplified Block Diagram of DM-3104 and DM-3100B

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.

Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical) 50pA (maximum)

Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V intermittent (maximum)

External Reference Range ..... ±100 mV to ±2V referred to -Vs (EXT. REF LO)

Common-Mode Rejection ..... 80 dB (typical), from dc to 60 Hz, with a 1 Kilohm unbalanced input

Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.

Resolution ..... 1 mV

Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count

Temperature Drift of Zero ..... Autozeroed ±1 count over a 0° to +50 C temperature range

Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)

Warm-Up Time ..... 10 minutes (typical)

Sampling Time ..... 83.3 mS (nominal)

Sampling Rate ..... 3 conversions per second. May be rewired for up to 20 conversions per second

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)

Brightness ..... 2400 min, 4800 typ microcandelas per display segment (seven segments per digit)

Decimal Points ..... Selectable using decimal point select signal lines.

Display Type ..... DM-3100B, red LED DM-3104, High brightness red LED

Display Height ..... DM-3100B, 0.56" (14,2 mm) DM-3104, 0.6" (15,2)

Overscale ..... The inputs exceeding the full-scale range display a "1" MSD and sign with other digits blanked.

Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

POWER REQUIREMENTS

AC Power

115 or 230 VAC, ±10%, 47 to 440 Hz, 4 watts typical

dc Power

+5V ±0.25Vdc @ 250 mA typical, 400 mA maximum and -5V dc @ 5 mA typical, 25 mA maximum. Logic spikes must be less than 50 mV. Bypass supplies externally if necessary.

(Users will normally power from AC-only; dc-only power is optional.)

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

PHYSICAL

External Dimensions

Short-Depth Case 3.0"W x 2.15"D x 1.76"H (76,2 x 54,6 x 44,7 mm)

Panel Cutout Dimensions

1.812"H x 3.062"W (46,0 x 77,7 mm)

Weight

5 ounces (142g) approximately

ENVIRONMENTAL

Altitude

0 to 15,000 feet (4900m)

Operating Temperature Range

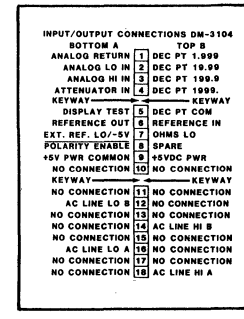
32°F to 122°F (0° to 50°C)

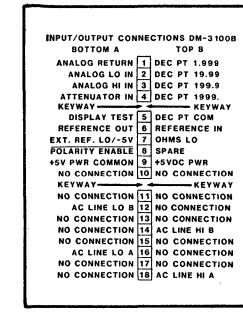
Storage Temperature Range

-13°F to +185°F (-25°C to 85°C)

Relative Humidity

20% to 80% non-condensing





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DM-3100L/DM-3103
Low-Cost, 3½ Digit LED Panel Meters

FEATURES

- **Balanced differential inputs**
- **1000 MΩ CMOS high-impedance inputs**
- **3½ Digit 0.56" red LED (DM-3100L) and 0.6" high brightness red LED Models (DM-3103).**
- **Logic Power (+5V dc)**
- **Compact Short-Depth cases**
- **80 dB CMRR**
- **Autozeroing Capability**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**
  1. **Accepts shunts for ±20 μA to ±2A FS ranges**
  2. **Accepts attenuators for ±2V to ±200V FS ranges**
  3. **Digital ohmmeter, 2KΩ to 10MΩ FSR**

GENERAL DESCRIPTION

The DM-3100L and DM-3103 are 3½ digit Short-Depth versions of the DM-3100N and DM-3101 respectively. The DPM's have bright red LED displays making them easily readable from many feet away. The short-depth cases used are ideally suited for shallow panels. The DPM's are easily field-modifiable for different input voltage and current ranges.

The DPM's accept a DC or slowly-varying input voltage and display that input on front panel numerical indicators. They employ conventional dual-slope A/D converters plus 7 segment display decoder-drivers all in one LSI microcircuit. Since the microcircuits require approximately 10V to power the A/D section, the internal DC/DC converters generate -5V from +5V power input to form bipolar supplies.

The DM-3100L and DM-3103 employ balanced differential inputs. When used with a bridge or transducer input, the DPM's offer high noise immunity. In such configurations the DPM's can accurately measure very small signals in the presence of much larger common mode signals.

The high impedance (1000 megohms) inputs will not load down sensitive input circuits.

The meters can be operated ratiometrically. That is, the DPM's internal circuits automatically compensate for reference drifts in the supplies of balanced bridge or transducer sensors.

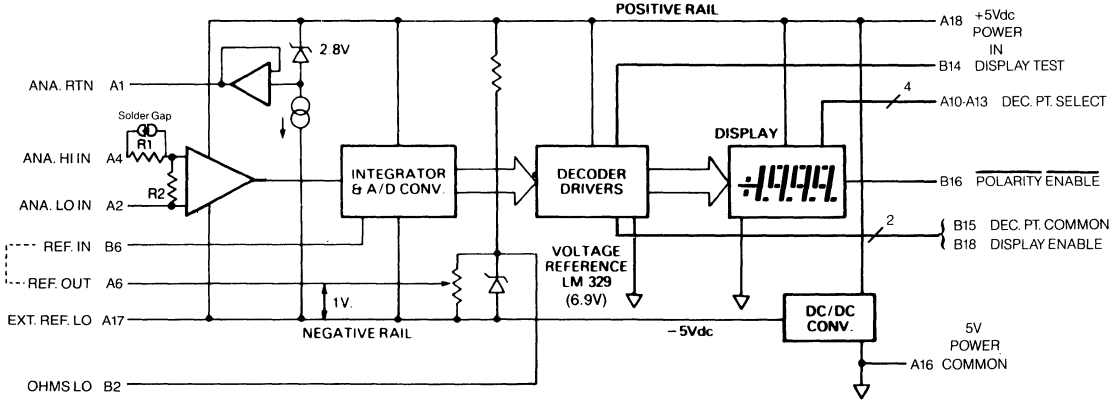
The DPM's find use in analytical instruments, industrial process controllers, portable diagnostic instruments, automatic test equipment, medical instruments, airborne, marine and ground vehicles and data acquisition/data logging systems.

ORDERING INFORMATION
DM-3100L - 1/DM-3103 - 1

Model	Description
DM-3100L-1	3 1/2-digit LED DPM in short depth case (includes one connector)
DM-3103-1	High-brightness version of DM-3100L (includes one connector)

ACCESSORIES

Part Number	Description
58-2075010	Connector, dual 18-pin, 0.1" centers
UPA-5/500	115V AC to ± 5V dc (@ 500 mA) power adaptor



Simplified Block Diagram of DM-3100L and DM-3103

10

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.

Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical) 50 pA (maximum)

Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V intermittent (maximum)

External Reference Range ..... ±100 mV to ±2V referred to -Vs (EXT. REF LO)

Common-Mode Rejection ..... 80 dB (typical, from dc to 60 Hz, with a 1 Kilohm unbalanced input

Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below +5V dc supply and 1.0V dc above -5V dc supply.

Resolution ..... 1 mV

Display Accuracy ..... @Adjustable to ±0.1% of reading, ±1 count

Temperature Drift of Zero ..... Autozeroed ±1 count over 0 to +50°C temperature range

Temperature Drift of Gain ..... ± 50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)

Warm-Up Time ..... 10 minutes (typical)

Sampling Time ..... 83.3 mS (nominal)

Sampling Rate ..... 3 conversions per second. May be rewired for up to 20 conversions per second

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)

Decimal Points ..... Selectable using decimal point select signal lines.

Display Type ..... DM-3100L, red LED DM-3103, High brightness red LED

Display Height ..... DM-3100L 0.56" (14,2 mm) DM-3103 0.6" (15,2 mm)

Brightness (DM-3103) ..... 2400 minimum, 4800 typical microcandelas per display segment (7 segments per digit)

Overscale ..... The inputs exceeding the full-scale range blank the display leaving a "1" MSD and sign.

Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

POWER REQUIREMENTS

External +5, ±0.25V dc regulated required at 280 mA typical, 450 mA maximum. Logic spikes must not exceed 50 mV. Power current varies rapidly so that unregulated supplies cannot be used.

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

PHYSICAL

External Dimensions Short-Depth Case
3.0"W x 2.15"D x 1.76"H (76,2 x 54,6 x 44,7 mm)

Panel Cutout
1.812"H x 3.062"W (46,0 x 77,7 mm)

Weight
5 ounce (142g) approximately

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0° to 50°C)

Storage Temperature Range
-13°F to +185°F (-25°C to 85°C)

Relative Humidity
20% to 80% non-condensing

INPUT/OUTPUT CONNECTION DM-3100L

BOTTOM A		TOP B
ANALOG RETURN	1	NO CONNECTION
ANALOG LO INPUT	2	OHMS LO
NO CONNECTION	3	NO CONNECTION
ANALOG HI INPUT	4	NO CONNECTION
NO CONNECTION	5	NO CONNECTION
REFERENCE OUT	6	REFERENCE IN
NO CONNECTION	7	NO CONNECTION
NO CONNECTION	8	NO CONNECTION
NO CONNECTION	9	NO CONNECTION
DEC PT 1.999	10	NO CONNECTION
DEC PT 19.99	11	NO CONNECTION
DEC PT 199.9	12	NO CONNECTION
DEC PT 1999.	13	NO CONNECTION
NO CONNECTION	14	DISPLAY TEST
NO CONNECTION	15	DEC PT COM
PWR COMMON	16	POLARITY ENABLE
EXT. REF. LO	17	NO CONNECTION
+5VDC PWR IN	18	DISPLAY ENABLE

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL (EXT. REF. LO).

INPUT/OUTPUT CONNECTION DM-3103

BOTTOM A		TOP B
ANALOG RETURN	1	NO CONNECTION
ANALOG LO INPUT	2	OHMS LO
NO CONNECTION	3	NO CONNECTION
ANALOG HI INPUT	4	NO CONNECTION
NO CONNECTION	5	NO CONNECTION
REFERENCE OUT	6	REFERENCE IN
NO CONNECTION	7	NO CONNECTION
NO CONNECTION	8	NO CONNECTION
NO CONNECTION	9	NO CONNECTION
DEC PT 1.999	10	NO CONNECTION
DEC PT 19.99	11	NO CONNECTION
DEC PT 199.9	12	NO CONNECTION
DEC PT 1999.	13	NO CONNECTION
NO CONNECTION	14	DISPLAY TEST
NO CONNECTION	15	DEC PT COM
PWR COMMON	16	POLARITY ENABLE
EXT. REF. LO	17	NO CONNECTION
+5VDC PWR IN	18	DISPLAY ENABLE

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL (EXT. REF. LO).

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DM-3100MIL
Ruggedized, 3½ Digit LED Panel Meter

FEATURES

- **3½ Digits LED display, +5V dc-powered**
- **Extended Operating Temperature Range (−46°C to +49°C)**
- **Designed to meet Military Standards:**
  - **Vibration Testing per MIL-STD-202**
  - **Humidity Testing per MIL-STD-202**
  - **Inspected per MIL-STD-105**
- **Balanced Different Inputs**
- **Withstands 3 shocks @ 25 g's for 11ms Vertical Axis**
- **Standard ±1.999 Vdc input range;**

GENERAL DESCRIPTION

The DM-3100MIL is a 3½ Digit, LED Display, +5V dc-powered digital panel meter. The DPM is designed to operate over an extended temperature range of -46°C to +49°C and conform to military standards. The DM-3100MIL meets and exceeds vibration and humidity testing per MIL-STd-202. It will also withstand shock testing (3 shocks @ 25 g's for 11ms vertical axis). The DPM successfully meets and exceeds the military specifications by using all hermetically sealed components and conformally coating the circuit boards. Its compact design lets this DPM fit into a short-depth case. The design and rigorous testing permits using the DM-3100MIL in portable test equipment for field use, ground vehicles, submerged vessels and aircraft. The DM-3100MIL offers a standard +/-1.999 Vdc input range; a +/-199.9 mV range is available to OEM quantity customers.

Overall, the DM-3100MIL is a highly reliable DPM designed for the rugged military environment.

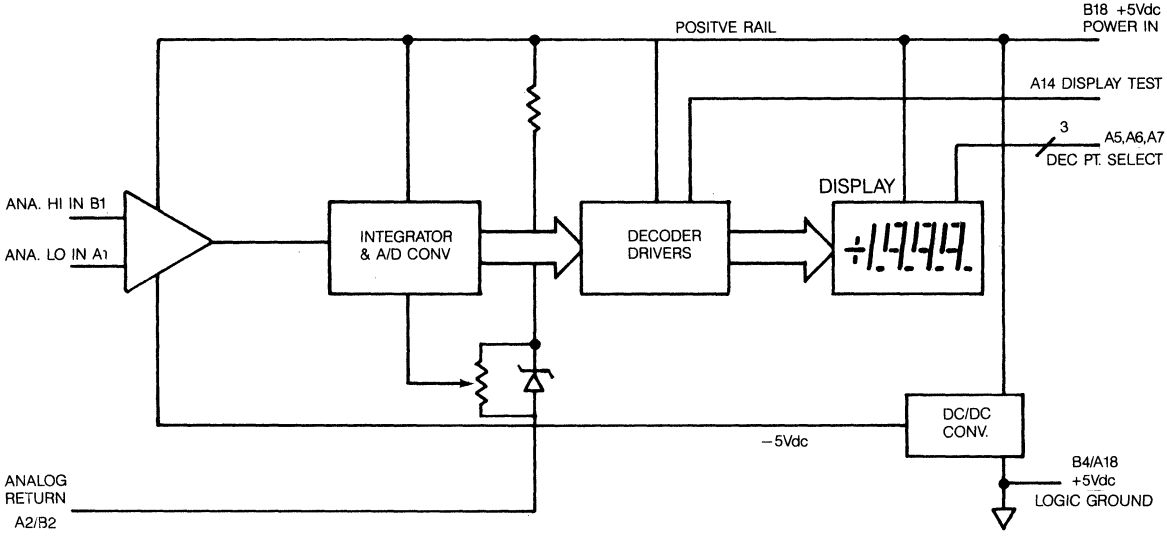
ORDERING INFORMATION

DM-3100MIL-1

Model	Description
DM-3100MIL-1	Ruggedized, 3½ digit meter

ACCESSORIES

Part Number	Description
58-2075010	Connector, dual 18-pin, 0.1" centers (one included with each meter)
UPA-5/500	115V AC to +5V dc (@ 500 mA) adaptor



Simplified Block Diagram of DM-3100MIL

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FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES"

Input Impedance ..... 100 Megohms (minimum)
1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical)
50 pA (maximum)

Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum). ±300V intermittent (maximum).

Common-Mode Rejection ..... 80 dB (typical), from dc to 60 Hz, with a 1 Kilohm unbalanced input.

Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.

Resolution ..... 1 mV

Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count.

Temperature Drift of Zero ..... Autozeroed ±1 count over -46° to +49°C temperature range.

Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical).
±100 ppm of reading/°C (maximum).

Warm-Up Time ..... 10 minutes (typical)

Sampling Time ..... 83.3 mS (nominal)

Sampling Rate ..... 3 conversions per second. May be rewired up to 20 conversions per second.

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits).

Decimal Points ..... Selectable using decimal point select signal lines.

Display Type ..... Red LED

Display Height ..... .3"

Overscale ..... Inputs exceeding the full-scale range blank the display leaving a "1" MSD and sign.

Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

POWER REQUIREMENTS

External +5 dc, ±0.25V dc regulated required at 280 mA typical, 450 mA maximum. Logic spikes must not exceed 50 mV. Power current varies rapidly so that unregulated supplies cannot be used.

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

PHYSICAL

External Dimensions
Short-Depth Case
3.0"W x 2.15"D x 1.76"H (76,2 x 54,6 x 44,7 mm)

Panel Cutout Dimensions
1.812"H x 3.062"W (46,0 x 77,7 mm)

Weight
5 ounces (142g) approximately

ENVIRONMENTAL

Altitude
0 to 50,000 feet

Operating Temperature Range
-51°F to 88°F (-46°C to 49°C)

Storage Temperature Range
-124°F to +185°F (-69°C to +85°C)

Relative Humidity
MIL-STd-202, Method 106D (98% relative humidity)

Vibration
MIL-STd-202, Method 204C
Section 2.2, (Condition A) (10G at 10 to 500Hz)

Shock
3 shocks @ 25 g's for 11ms Vertical Axis

Marking
MIL-STd-130

Marking Permanency
MIL-STd-202, Method 215

Inspection
MIL-STd-105

INPUT/OUTPUT CONNECTIONS DM-3100MIL

BOTTOM A		TOP B
INPUT SIGNAL LO	1	INPUT SIGNAL HI
ANALOG RETURN	2	ANALOG RETURN
NC	3	NC
NC	4	PWR COMMON
DEC PT 100	5	NC
DEC PT 10	6	NC
DEC PT 1	7	NC
NC	8	NC
NC	9	NC
NC	10	NC
NC	11	NC
NC	12	NC
NC	13	NC
DISPLAY TEST	14	NC
NC	15	NC
NC	16	NC
NC	17	NC
PWR COMMON	18	+5V DC INPUT

DM-3100N/DM-3101
Low-Cost, 3½ Digit LED Panel Meters

FEATURES

- **Balanced differential inputs**
- **1000 MΩ CMOS high-impedance inputs**
- **Compact low-profile case**
- **Logic powered (+5V dc)**
- **Internal provision for an offset pot for various applications**
- **80 dB CMRR**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**
- **Autozeroing capability**

GENERAL DESCRIPTION

The DM-3100N and its high-brightness equivalent, the DM3101 are 3½ digit Solid State devices using red LED displays. The bright red LED displays make them easily readable from many feet away. Packaged in compact low profile cases, these DPM's have provisions for user-installed resitors and offset potentiometers.

The autozeroing capability further enhances the versatility of the meter. A pot can be internally installed so that an offset can be obtained with a zero input to the meter, or a zero reading with an offset input.

The DPM's accept a DC or slowly-varying input voltage and display that input on front panel numerical indicators. They employ conventional dual-slope A/D converters plus 7 segment display decoder-drivers all in one LSI microcircuit. Since the microcircuits require approximately 10V to power the A/D section, the internal DC/DC converters generate -5V from +5V power input to form bipolar supplies.

Another feature of these DPM's is that a balanced differential input is used. When used with bridge or transducer inputs, it offers high noise immunity and can accurately measure very small signals in the presence of much larger common mode signals.

A very noteworthy feature of the meters is that they can be operated ratiometrically. This means that internal circuits in the DPM's automatically compensate for reference drifts in the supplies of balanced bridge or transducer sensors.

These DPM's find use in analytical instruments, industrial process controllers, portable diagnostic instruments, automatic test equipment, medical and patient monitoring instruments, airborne, marine and ground vehicles and data acquisition/data logging systems.

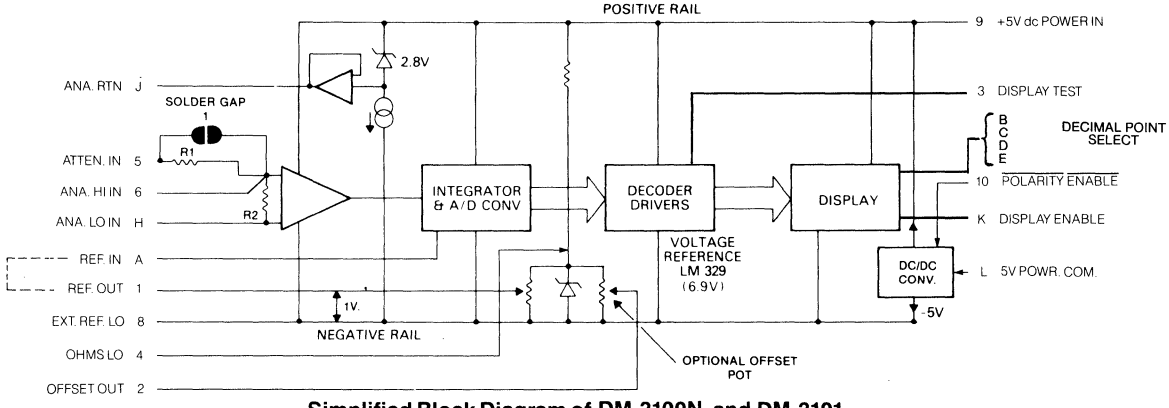
ORDERING INFORMATION

DM-3100N - 1/DM-3101 - 1

Model	Description
DM-3100N-1	3 1/2 Digit LED DPM in low-profile case (includes one connector)
DM-3101-1	High-brightness version of DM-3100N (includes one connector)

ACCESSORIES

Part Number	Description
58-2073082	Dual 10-pin, 0.156" centers connector
TP-50K	Offset pot
UPA-5/500	115V AC to ±5V dc (@ 500 mA) power adaptor



Simplified Block Diagram of DM-3100N and DM-3101

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.

Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical) 50 pA (maximum)

Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V intermittent (maximum)

External Reference Range ..... ±100 mV to ±2V referred to -Vs (EXT. REF LO)

Common-Mode Rejection ..... 80 dB (typical), from dc to 60 Hz, with 1 Kilohm unbalance

Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below +5V dc supply and 1.0V dc above -5V dc supply

Resolution ..... 1 mV

Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count

Temperature Drift ..... Autozeroed ±1 count over 0 to +50°C temperature range

Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)

Warm-Up Time ..... 10 minute (typical)

Sampling Time ..... 83.3 mS (nominal)

Sampling Rate ..... 3 conversions per second. May be required up to 20 conversions per second.

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)

Decimal Points ..... Selectable using decimal point select signal lines.

Display Type ..... DM-3100N, Red LED DM-3101, High brightness Red LED

Display Height ..... DM-3100N, 0.56" (14,2 mm) DM-3101, 0.6" (15,2 mm)

Overscale ..... The inputs exceeding the full-scale range blank the display leaving a "1" MSD and sign.

Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

POWER REQUIREMENTS

External +5, ±0.25V dc regulated required at 280 mA typical, 450 mA max. Logic spikes must not exceed 50 mV. Power current varies rapidly so that unregulated supplies cannot be used.

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

PHYSICAL

External Dimensions
Low-Profile Case 2.53"W x 3.34"D x 0.94"H (64,3 x 84,8 x 23,8 mm)

Panel Cutout Dimensions
2.56"W x 0.97"H (minimum) (65,1 x 24,6 mm)

Mounting Method
Refer to end of this section.

Weight
5 ounces (142g) approximately

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0° to 50°C)

Storage Temperature Range
-13°F to +185°F (-25°C to 85°C)

Relative Humidity
20% to 80% non-condensing

INPUT/OUTPUT CONNECTIONS DM-3100N

BOTTOM			TOP
REFERENCE IN	A	1	REFERENCE OUT
DEC PT 1999.	B	2	OFFSET OUT (OPT)
DEC PT 199.9	C	3	DISPLAY TEST
DEC PT 19.99	D	4	OHMS LO (OPT)
DEC PT 1.999	E	5	ATTENUATOR IN (OPT)
DEC PT COM	F	6	ANALOG HI IN
ANALOG LO IN	H	7	NO CONNECTION
ANALOG RETURN	J	8	EXT REF LO
DISPLAY ENABLE	K	9	+5VDC PWR IN
PWR COM	L	10	POLARITY ENABLE

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL (EXT. REF. LO)

INPUT/OUTPUT CONNECTIONS DM-3101

BOTTOM			TOP
REFERENCE IN	A	1	REFERENCE OUT
DEC PT 1999.	B	2	OFFSET OUT (OPT)
DEC PT 199.9	C	3	DISPLAY TEST
DEC PT 19.99	D	4	OHMS LO (OPT)
DEC PT 1.999	E	5	ATTENUATOR IN (OPT)
DEC PT COM	F	6	ANALOG HI IN
ANALOG LO IN	H	7	NO CONNECTION
ANALOG RETURN	J	8	EXT REF LO
DISPLAY ENABLE	K	9	+5VDC PWR IN
PWR COM	L	10	POLARITY ENABLE

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL (EXT. REF. LO)

DM-3100U1
Micropowered 3½ Digit LCD Panel Meters

FEATURES

- **Ultra-low power consumption**
- **.5" high 3½ digits LCD readout**
- **5V or 9 to 15V dc-powered**
- **Internal ratiometric reference for drift correction**
- **Selectable unit descriptors: A, mA, V, mV, Ω, KΩ, AC, or DC**
- **Balanced differential inputs with 5 pA bias currents**
- **Autozeroing with 80 db CMR noise rejection**
- **User-configurable to accept 4 to 20 mA inputs**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**
  1. **Offset pot for 4-20 mA and other applications**
  2. **Accepts shunts for ±20 μA to ±2A FS ranges**
  3. **Accepts attenuators for ±2V to ±200V FS ranges**
  4. **Digital ohmmeter, 2KΩ to 10MΩ FSR**

GENERAL DESCRIPTION

The DM-3100U1 is a 3½ digit, LCD-type DPM that uses very little power and can be powered by +4V to +15V dc sources. The 0.5" high numeric display is visible under ambient room light from many feet away. This device is packaged in a low-profile case, allowing a higher packing density on the final product's panel. Besides measuring dc voltages and current, unit descriptors (A, mA, V, mV, Ω, KΩ, AC, and DC) indicate what is being measured.

The versatility of this meter is further enhanced by its autozeroing capabilities. If the customer desires, an offset pot can be internally installed so that a desired reading can be obtained with a zero output to the meter.

This DPM accepts a dc or slowly varying input voltage and displays that input on front panel numerical indicators. It employs a conventional dual-slope A/D converter plus 7 segment display decoders/drivers all in one LSI microcircuit. Since this microcircuit requires approximately 9V to power the A/D section, an internal dc/dc converter generates -5V from +5V power input. Together these two voltage sources form a bipolar power supply to power the A/D converter. The DM-3100U1 may also be powered directly from a single 9V battery @ 3 mA without using the dc/dc converter.

Another feature of the DM-3100U1 is that it employs a balanced differential input. When used with a bridge or transducer input, it offers high noise immunity and can accurately measure very small signals in the presence of much larger common mode noise. Another characteristic of this balanced differential input is that it will not load down sensitive input circuits due to its high input impedance of 1000 megohms, and low 5 pA bias current.

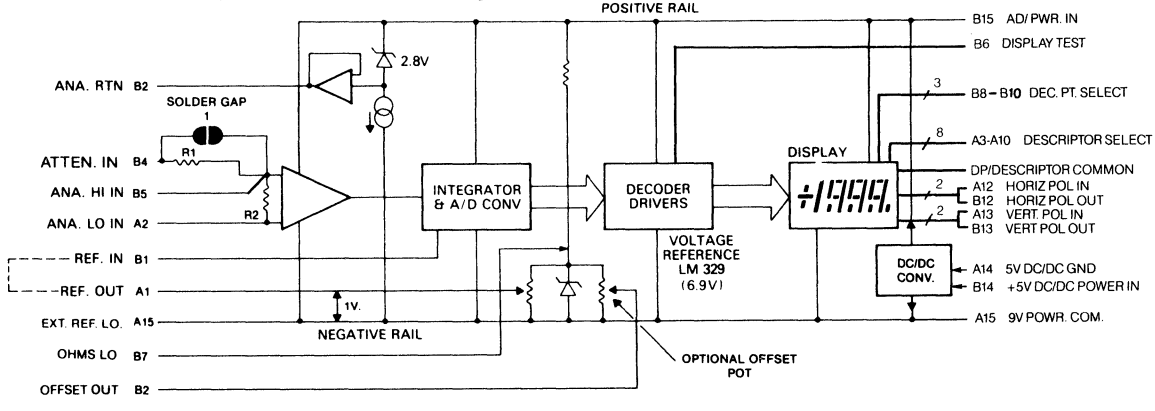
A very noteworthy feature of this meter is that it can be operated ratiometrically. This means that it has internal circuits that can automatically compensate for reference drifts in the supplies of balanced bridge or transducer sensors and still give accurate readings.

ORDERING INFORMATION
DM-3100U1 - 1

Model	Description
DM-3100U1-1	3 1/2-digit micropowered LCD DPM with descriptors (Includes one connector)

ACCESSORIES

Part Number	Description
58-2073083	Connector, dual 15-pin, 0.1" centers
TP-50K	Offset pot
UPA-5/500	Power Supply



Simplified Block Diagram of DM-3100U1

10

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full Scale Input .....-1.999V dc to +1.999V dc
Range Input pad area will accept user-installed range change
Input Impedance .....100 Megohms, minimum
Input Bias Current.....5 pA typical, 50 pA maximum
Input Overvoltage .....±250 volts dc 175 VRMS continuous max.
±300 Volts intermittent max.
External Ref. Range ....+100 mV to +2V, referred to -Vs
Common Mode .....80 dB, dc to
Rejection 60 Hz, 1 Kilohm unbalance
Common Mode .....Within +Vs-0.5V to -Vs+1.0V,
Voltage Range where +Vs is the positive rail (Pin B15) and -Vs is the negative rail (Pin A15) -Vs is approximately equal to -5V below PWR. COM.
Resolution 1mV
Displayed
Accuracy..... Adjustable to ± of reading, ± count
Temperature Drift .....Autozeroed ±1 count over
of Zero 0 to +50°C
Temperature Drift .....±50 ppm of Reading/°C typ.
of Gain ±100 ppm of Reading/°C max
Ramp-up Time .....(integration Period) 83.3 mS
Sampling Rate .....Factory set at 3 conversions per second. May be rewired up to 20 conversions/second

DISPLAY

Number of Digits.....3 decimal digits and most significant "1" digit (3½ digits)
Decimal Points.....Selectable decimal points are included for scale multipliers
Display Type.....Field effect liquid crystal displays (LCD) requiring room light for viewing. Black digits against a light background
Display Height .....0.5 inches (12.7 mm)
Overscale.....Inputs exceeding the full scale range blank the display, leaving a "1" MSD and sign
Autopolarity .....A minus sign is automatically displayed for negative inputs, and may also be blanked
Descriptors .....K, Ω, mA, mV, AC, and DC This field of function labels is positioned to the right of the decimal digits. Individual unit descriptors may be selected for display.

POWER CONNECTIONS

A/D Power In (Pin B15)
Connect +9 to +15V dc source to this pin, referred to 9V dc Power Common)PIN A15). When using a +5V dc power source, connect this pin to pin B14.
+5V dc Power In (PIN B14)
Connect this pin to the +5V dc power source, referred to +5V dc Power Ground (PIN A14)

POWER REQUIREMENTS

5V between B14/B15 and A14; 12mA typ., 15mA max. OR 9 to 15 V dc between B15 and A15; 9V, 9 mA; 15V, 20 mA. max

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration is 90 days.

PHYSICAL-ENVIRONMENTAL

Outline Dimensions
2.53"W x 3.25"D x 0.94"H (64.3 x 82.5 x 23.8 mm)
Cutout Dimensions
2.56:W x 0.97"H min. (65.1 x 24.6 mm)
Mounting Method
See Mounting Section
Weight
Approximately 5 ounces (142g)

TEMPERATURE RANGE

Operating
0 to +50°C
Storage
0°C to +55°C
Altitude
0 to 15,000 feet (4900m)
Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features:

Reference In/Out (Pins B1/A1)
Normally, REF. IN and REF. OUT should be jumpered together. An external floating source referred to EXT.REF. LO (Pin A15) may be substituted for ratiometric operations.
Vertical Polarity In (Pin A13)
Vertical Polarity Out (Pin B13)
For reverse sensing applications, VERT. POL. OUT may be jumpered to HORIZ. POL. IN (no other connections). This will display a minus sign with positive inputs and no sign (implied positive) with negative inputs.
See Backplane Out
Backplane Out (Pin A11)
Connect all unused Polarity, Decimal Points and Descriptors to Backplane Out.

INPUT/OUTPUT CONNECTIONS DM-3100U1

BOTTOM A		TOP B
REFERENCE OUT	1	REFERENCE IN
ANALOG LO IN	2	ANALOG RETURN
mA DSCRPTR IN	3	OFFSET OUT (OPT)
KΩ DSCRPTR IN	4	ATTENUATOR HI IN (OPT)
KΩ DSCRPTR IN	5	ANALOG HI IN
mA DSCRPTR IN	6	DISPLAY TEST
mV DSCRPTR IN	7	OHMS LO
DC DSCRPTR IN	8	DEC PT 199.9
AC DSCRPTR IN	9	DEC PT 19.99
mV DSCRPTR IN	10	DEC PT 1.999
BACKPLANE OUT	11	DP/DSCRPTR COM
HORIZ POL IN	12	HORIZ POL OUT
VERT POL IN	13	VERT POL OUT
+5V DC DC GND.	14	+5V DC/DC PWR IN
+9V PWR COM/EXT.REF.LO	15	A/D PWR IN

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL(EXT. REF. LO).

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DM-3100U2,-U3
AC/dc-powered 3½ Digit LCD Panel Meters

FEATURES

- **Dual powered: +9 to +15V dc/115VAC (DM-3100U2), +9 to 15V dc/230VAC (DM-3100U3)**
- **Selectable unit descriptors: A, mA, V, mA, Ω, kΩ AC or dc**
- **Balanced high-impedance differential inputs**
- **80dB CMRR**
- **Autozeroing capability**
- **Internal provision for an offset potentiometer for various applications**
- **Standard ±1.9999V dc input range; user-installed options set other voltage or current ranges.**
  1. **Offset pot for 4-20 mA and other applications**
  2. **Accepts shunts for ±20 μA to ±2A FS ranges**
  3. **Accepts attenuators for ±2V to ±200V FS ranges**
  4. **Digital ohmmeter, 2KΩ to 10MΩ FSR**

GENERAL DESCRIPTION

The DM-3100U2 and DM-3100U3 are 3½ digit LCD display devices. The DPM's operate with either AC or +9 to +15V dc voltages. The DM-3100U2 uses 115V AC at 47 to 440Hz. The DM-3100U3 uses 230V AC at 47 to 440Hz. The input voltage and current ranges are easily field-modifiable.

Both models use DATEL's low profile DPM case. The input section is balanced differential for excellent noise rejection and uses a high-impedance (1000 MΩ) CMOS front end with low 5 pA bias currents.

Both meters are autozeroed and accept external ratiometric reference inputs to reduce drift errors in instrumentation systems.

The LCD display on both meters contains unit descriptors (A, mA, V, mV, Ω, KΩ, AC, dc) which are pin-programmable for dedicated VOM and DVM applications.

The AC supply in both meters produces an additional filtered dc output of approximately +12V dc @ 5 mA for customer use. A suggested application is to charge standby NiCad batteries. Since this power output pin is also used for power input when dc-powered, the NiCads may be left continuously connected so the meter will continue operating if there is an AC power failure.

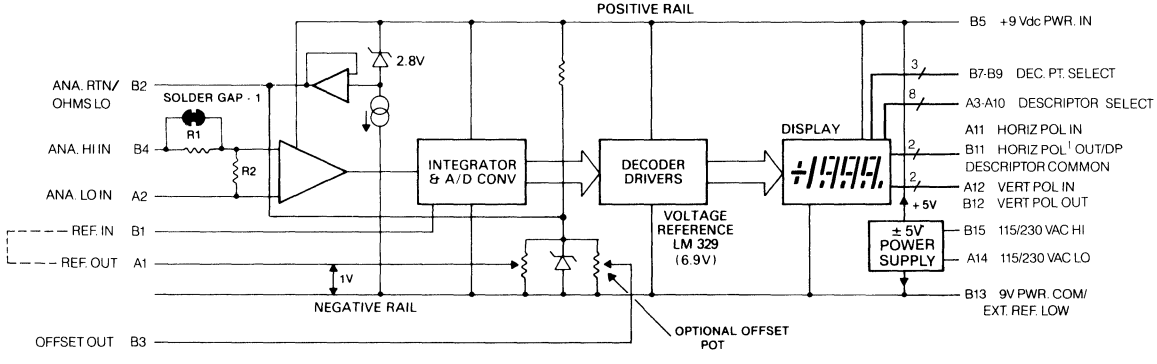
ORDERING INFORMATION

DM-3100U2 - 1/DM-3100U3 - 1

Model	Description
DM-3100U2-1	3 1/2-Digit, LCD Digital panel meter, 115V AC or +9 to +15V dc powered (one connector included)
DM-3100U3-1	3 1/2-Digit, LCD Digital panel meter, 230V AC or +9 to +15V dc powered (one connector included)

ACCESSORIES

Part Number	Description
58-2073083	Connector dual 15-pin, 0.1" centers
TP-50K	Offset pot



Simplified Block Diagram of DM-3100U2 and DM-3100U3

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS both models
(Typical at +25°C, unless noted)

ANALOG INPUT

Full-Scale Input ..... Refer to "FEATURES"
Range Ranges field-modifiable.
Input Impedance ..... 100 Megohms (minimum)
1000 Megohms (typical)
Input Bias Current ..... 5 pA (typical) 50 pA (maximum)
Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum)
±300V dc intermittent (maximum)
External Reference ..... ±100 mV to ±2V referred
Range to -Vs
Common-Mode ..... 80 dB (typical),
Rejection from dc to 60 Hz, with a 1 Kilohm unbalanced input
Common-Mode ..... Both the inputs must
Voltage Range remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.
Resolution ..... 1 mV
Display Accuracy ..... Adjustable to ±0.1% of reading, +/-1 count
Temperature Drift ..... Autozeroed ±1 count
of Zero over a 0°C to +50°C temperature range
Temperature Drift ..... ±50 ppm of reading/°C
of Gain (typical) ±100 ppm of reading/°C (maximum)
Sampling Time ..... 83.3 mS (nominal)
Sampling Rate ..... 3 conversions per second

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)
Decimal Points ..... Selectable using decimal point select signal lines.
Display Type ..... Field-effect liquid crystal display (LCD)
Display Height ..... 0.5" (12,7mm)
Overscale ..... Inputs exceeding the full-scale range display "+1" MSD with zeroes blanked.
Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity.
Descriptors ..... Ω, kΩ, mA, mV, AC, dc, A, V. This field of function labels is positioned to the right of the decimal digits. Individual unit descriptors may be selected for display.

POWER REQUIREMENTS

AC
¼ watt, maximum, 115 or 230V AC.

dc
+9 to +15V dc, filtered @ 9 mA typical, 20 mA maximum. Logic spikes must be less than 50 mV.

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

PHYSICAL

External Dimensions
2.53"W x 3.25"D x 0.94"H (64,3 x 82,5 x 23,8mm)

Panel Cutout Dimensions
2.56"W x 0.97"H (65,1 x 24,mm)

Mounting Method
Refer to end of this section.

Weight
5 ounces (142g) approximately

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
+32°F to 122°F (0° to 50°C)

Storage Temperature Range
+32°F to 131°F (0° to 55°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

Horizontal Polarity In (Pin A11)
Horizontal Polarity Out (Pin B11)
Normally these inputs are jumpered together to continuously display the horizontal portion of the polarity sign.

Vertical Polarity In (Pin A12)
Vertical Polarity Out (Pin B12)
Jumper these inputs when HORIZ. POL. is jumpered for automatic sign display with bipolar inputs. For reverse sensing applications VERT. POL. OUT may be jumpered to HORIZ. POL. IN (no other connections). This will display a minus sign with positive inputs and no sign (implied positive) with negative inputs. See BACKPLANE OUT.

Backplane Out (Pin B10)
Connect all unused polarity, decimal points and descriptor pins to BACKPLANE OUT.

Descriptors
Electrical units are displayed by connecting their respective pins to DESCRIPTOR COMMON Pin B11.

INPUT/OUTPUT CONNECTIONS DM-3100U2

BOTTOM A		TOP B
REFERENCE OUT	1	REFERENCE IN
ANALOG LO IN	2	OHMS LO
mA DSCRPTR IN	3	OFFSET OUT (OPT.)
KΩ DSCRPTR IN	4	ANALOG HI IN
KΩ DSCRPTR IN	5	+9VDC PWR IN
mA DSCRPTR IN	6	DISPLAY TEST
mV DSCRPTR IN	7	DEC PT 199.9
DC DSCRPTR IN	8	DEC PT 19.99
AC DSCRPTR IN	9	DEC PT 1.999
mV DSCRPTR IN	10	BACKPLANE OUT
HORIZ POL IN	11	HRZ. POL OUT/DP. COM
VERT POL IN	12	VERT POL OUT
NO CONNECTION	13	+9V PWR COM/EXT REF LO
115 VAC LO	14	NO CONNECTION
NO CONNECTION	15	115 VAC HI

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL(PIN B13)

INPUT/OUTPUT CONNECTIONS DM-3100U3

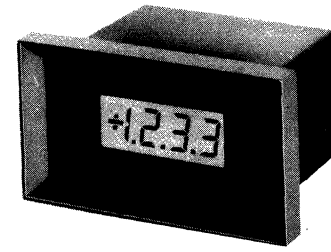
BOTTOM A		TOP B
REFERENCE OUT	1	REFERENCE IN
ANALOG LO IN	2	OHMS LO
mA DSCRPTR IN	3	OFFSET OUT (OPT.)
KΩ DSCRPTR IN	4	ANALOG HI IN
KΩ DSCRPTR IN	5	+9VDC PWR IN
mA DSCRPTR IN	6	DISPLAY TEST
mV DSCRPTR IN	7	DEC PT 199.9
DC DSCRPTR IN	8	DEC PT 19.99
AC DSCRPTR IN	9	DEC PT 1.999
mV DSCRPTR IN	10	BACKPLANE OUT
HORIZ POL IN	11	HRZ. POL OUT/DP. COM
VERT POL IN	12	VERT POL OUT
NO CONNECTION	13	+9V PWR COM/EXT REF LO
230 VAC LO	14	NO CONNECTION
NO CONNECTION	15	230 VAC HI

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL(PIN B13)

DM-3100X
Micropowered 3½ Digit LCD Panel Meter

FEATURES

- **Consumes very low power**
- **Dual dc-voltage power in (+5V dc or +9 to +15V dc)**
- **Balanced high-impedance differential inputs**
- **80 dB CMRR**
- **Autozeroing capability**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**
  1. **Accepts shunts for ±20 μA to ±2A FS ranges**
  2. **Accepts attenuators for ±2V to ±200V FS ranges**
  3. **Digital ohmmeter, 200Ω to 10MΩ FSR**



GENERAL DESCRIPTION

The DM-3100X is a 3½ digit LCD display device. The DPM consumes typically less than 0.03 watts. Powered by a range of +4V dc to +l5V dc the DM-3100X may be configured to measure different voltage, current and resistance ranges. The DPM is contained in a short-depth case.

The versatility of this meter is further enhanced by its autozeroing circuits which eliminate zero drift.

This DPM accepts a dc or slowly varying input voltage and displays that input on front panel numerical indicators. It employs a conventional dual-slope A/D converter plus 7 segment display decoder-drivers all in one LSI microcircuit. Since this microcircuit requires approximately 9V to power the A/D section, an internal dc/dc converter generates -5V from +5V power input. Together these two voltage sources form a bipolar power supply to power the A/D converter. The DM-3l00X may also be powered directly from a single 9V battery @ 3 mA without using the dc/dc converter.

The DM-3100X employs a balanced differential input. When used with a bridge or transducer input, it offers high noise immunity and can accurately measure very small signals in the presence of much larger common mode noise. The DPM's high-impedance input circuits will not load down the sensitive input circuits.

The meter can be operated ratiometrically. That is, the DPM's internal circuits automatically compensate for references drifts in the supplies of balanced bridge or transducer sensors and still give accurate readings.

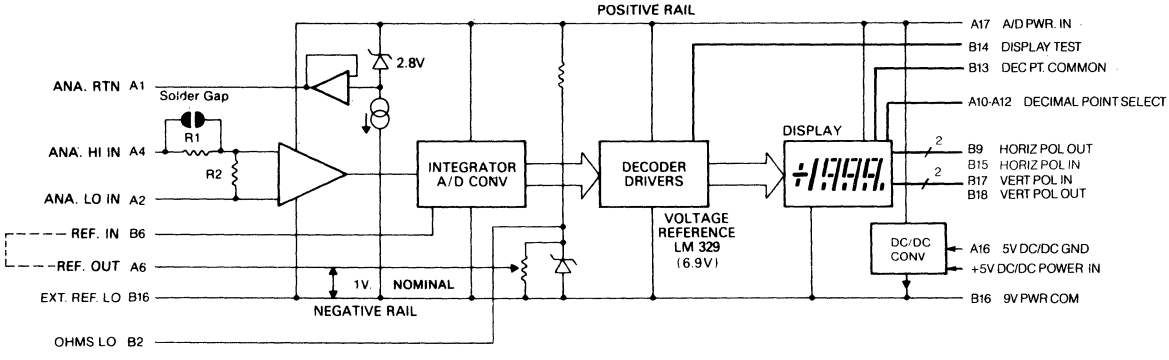
The DM-3100X finds use in analytical instruments, industrial process controllers, portable diagnostic instruments, automatic test equipment, medical instruments, airborne, marine, and ground vehicles, and data acquisition/data logging systems.

ORDERING INFORMATION
DM-3100X - 1

Model	Description
DM-3100X-1	3 1/2-digit LCD DPM (Includes one connector)

ACCESSORIES

Part Number	Description
58-2075010	Connector, dual 18-pin, 0.1" centers
UPA-5/500	115V AC to ±5V dc (@ 500 mA) power adaptor



Simplified Block Diagram of a DM-3100X

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C,2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.
Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)
Input Bias Current ..... 5 pA (typical) 50 pA (maximum)
Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V dc intermittent (maximum)
External Reference Range ..... ±100 mV to ±2V referred to -Vs
Common-Mode Rejection ..... 80 dB (typical), from dc to 60Hz, with 1 Kilohm unbalance
Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below +5V dc supply and 1.0V dc above -5V dc supply
Resolution ..... 1 mV
Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count
Temperature Drift of Zero ..... Autozeroed ± count over 0°C to +50°C temperature range
Temperature Drive of Gain ..... ±50 ppm of reading/°C (typical) ± 100 ppm of reading/°C (maximum)
Sampling Time ..... 83.3 mS (nominal)
Sampling Rate ..... 3 conversions per second

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)
Decimal Points ..... Selectable using decimal point select signal lines
Display Type ..... Field effect liquid crystal display (LCD)
Display Height ..... 0.5" (12,7mm)
Overscale ..... The inputs exceeding the full-scale range display "+1" MSD with zeroes blanked.
Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "–" sign for negative inputs. The user may blank the polarity.

POWER CONSUMPTION

The DPM requires 5V dc regulated at 12 mA typical and 15 mA maximum, or 12V dc regulated, at 12 mA typical and 15 mA maximum or 15V dc regulated at 18 mA typical and 20 mA maximum. The logic spikes must not exceed 50 mV.

PHYSICAL

External Dimensions
Short-Depth Case 3.0"W x 2.15"D x 1.76"H (76,2 x 54,6 x 44,7mm)

Panel Cutout Dimensions
3.062"W x 1.812"H (46,0 x 77,7mm)

Mounting Method
Refer to end of this section.

Weight
5 ounce (142g) Approximately

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
+32°F to 122°F (0°C to 50°C)

Storage Temperature Range
+32°F to 131°F (0°C to 55°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

Decimal Points
Connect selected pin to DECIMAL POINT COMMON (Pin B13). See Backplane Out.

Horizontal Polarity In (Pin B15)
Horizontal Polarity Out (Pin B9)
Normally these inputs are jumpered together to continuously display the horizontal portion of the polarity sign. Omit the jumper for applications not requiring sign display. See Backplane Out.

Vertical Polarity In (Pin B17)
Vertical Polarity Out (Pin B18)
Jumper these inputs when HORIZ.POL. is jumpered for automatic sign display with bipolar inputs. For reverse sensing applications, VERT.POL. OUT may be jumpered to HORIZ.POL. IN (no other connections). This will display a minus sign with positive inputs and no sign (implied positive) with negative inputs. See Backplane Out.

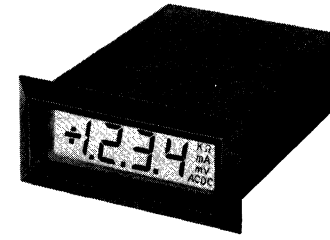
Backplane Out (Pin A13)
Connect all unused Polarity, and Decimal Points to Backplane Out. For VOM or DVM applications, a 470 kΩ resistor may be used for each Decimal Point. A rotary switch pole to Bl3 will then select the desired Decimal Point.

INPUT/OUTPUT CONNECTIONS DM-3100X

BOTTOM A		TOP B
ANALOG RETURN	1	NO CONNECTION
ANALOG LO INPUT	2	OHMS LO
NO CONNECTION	3	NO CONNECTION
ANALOG HI INPUT	4	NO CONNECTION
NO CONNECTION	5	NO CONNECTION
REFERENCE OUT	6	REFERENCE IN
NO CONNECTION	7	NO CONNECTION
NO CONNECTION	8	NO CONNECTION
NO CONNECTION	9	HORIZ POL OUT
DEC PT 199.9	10	NO CONNECTION
DEC PT 19.99	11	NO CONNECTION
DEC PT 1.999	12	NO CONNECTION
BACKPLANE OUT	13	DEC PT COM
NO CONNECTION	14	DISPLAY TEST
NO CONNECTION	15	HORIZ POL IN
+5V DC/DC PWR COM	16	+9V PWR COM
A/D PWR IN	17	VERT POL IN
+5V DC/DC PWR IN	18	VERT POL OUT

NOTE: REFERENCE IS BIASED AGAINST NEGATIVE RAIL (EXT. REF. LO).

DM-3102A, DM-3102B AUTORANGING 3 1/2 DIGIT PANEL METERS



FEATURES

- **Two Model Ranges**
  - **—Model DM-3102A: 200 mV, 2V, 20V, and 200V dc full scale autoranges**
  - **—Model DM-3102B: 2V, 20V, 200V, and 1000V dc full scale autoranges**
- **Accuracy Adjustable to ±0.1% or ±1 count over any full scale range**
- **3½ Digit LCD displays .5" high (12,7mm)**
- **Low power consumption, 5V dc at 30 mA typical**
- **Multiplexed BCD data outputs to drive a slave display**
- **-5V dc power output at 15 mA for external low power circuitry**
- **Seven unit descriptors: K, Ω, m, DC, AC, V, A**
- **Balanced differential inputs with 9 megohms nominal input impedance**

GENERAL DESCRIPTION

The DM-3102 is a 3½ digit, four decade, autoranging digital panel meter (DPM) with true balanced differential analog inputs. The low profile DPM is available in two model configurations. Model DM-3102A has 4 full-scale ranges of 200 mV, 2V, 20V, and 200V dc while Model DM-3102B has 4 full-scale ranges of 2V, 20V, 200V and l000V dc.

Both models are powered from a +5V dc power source, typically drawing 15mA. Output power of -5V dc at 15mA is available to the user for powering low power external circuitry. The multiplexed BCD data outputs allow interfacing the DPM to micro-processors or UART'S. They may also drive an additional slave display meter. This is made easier with the presence of the STROBE, RUN/HOLD and BUSY/DONE signal lines. A RUN/HOLD signal freezes the display and stops A/D conversions. Based on a single chip CMOS A/D converter, the DM-3102A/B autoranging meter has an accuracy of ±1 count in 20,000 counts, or .1% of any full scale range.

Typical conversion cycle time of the A/D converter is 300 milliseconds. (Worst-case autoranging time interval would be 900 milliseconds maximum.) Analog input signals enter through a .1% matched resistor network and typical signal input impedance is 9 megohms.

INTERFACING

To reduce the amount of wiring required to implement a slave display, four-wire BCD data is multiplexed using four digit drive outputs. Each digit drive sequentially turns on its respective signal when the drive signal is high. The digit is blanked when the drive line is low. The DM-3102A/B minimizes the wiring to a remote display, UART, or microprocessor since only 14 wires are needed to transfer the data which include 4 BCD data lines, 4 digit strobes, 4 range indications, polarity, and BUSY/DONE.

DISPLAY DESCRIPTOR SELECTION

The DM-3102A/B display allows enabling optional unit descriptors by jumpering pins on the converter PWA. Polarity and overrange indicators, as well as the unit descriptors, are driven by logic on the converter PWA.

PIN							
A3	B5	A2	A1	B1	B2	B3	B4
DESCRIPTORS							
'm [V]'	m [A]	AC	DC	'[m] V'	'[m] A'	Ω	K

To activate the desired unit descriptor, the corresponding pin must be connected to pin B6 B.P. (display common). Connect any unused unit descriptors to pin B12 (B.P.)

ORDERING INFORMATION

Model	Description
DM-3102A	Digital panel meter autoranging 200mV, 2V, 20V, 200V full scale ranges. (Includes two connectors)
DM-3102B	Digital panel meter autoranging 2V, 20V, 200V, 1000V full scale ranges. (Includes two connectors)

ACCESSORIES

Part Number	Description
58-2073083	Dual 15-pin, 0.100" centers PC edge board connector (Not included — order two with DPM).
UPA-5/500	AC to +5V dc power adapter.
DM-4106	Low-profile Slave Display (No description)

10

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, 2V range unless otherwise noted)

ANALOG INPUT

Configuration ..... True balanced differential bipolar inputs If single-ended inputs are preferred, close SG4 solder gap.

Full Scale Input Range
DM-3102A ..... ±200V dc
DM-3102B ..... ±1000V dc

Input Bias Current..... 1 pA typical, 10 pA maximum.

Display Accuracy..... Adjustable to ±0.1% of reading, +/-1 count.

Warm-Up Time..... 5 minutes.

Resolution ..... 100 uV in last digit (200mV range only).

Temperature Drift of Zero ..... Autozeroed, ±1 count over 0°C to +50°C temperature range.

Temperature Drift of Gain ..... ±50ppm of reading/°C typical — ±100ppm of reading/°C maximum.

Input Impedance ..... 9 Megohms, nominal.

Input Overvoltage ..... ±300 volts dc intermittent maximum, 175 VRMS continuous maximum on the 200V range, model A.

±350 volts dc intermittent maximum, 1500 VRMS continuous maximum on the 1000V range, model B.

Reference ..... Internal, referred to Analog Common, (between pins A13/B13). An external, user-supplied reference referenced to pin B15 is optional for ratiometric operation.

External Reference Range ..... +90mV to +200mV dc referenced to Analog Common, pin B15.

Common-Mode Voltage Range ..... Both inputs must remain within ±3V dc of Power Common. The user must provide external circuitry to keep the inputs within the common-mode range.

DISPLAY

Number of Digits..... 3 decimal digits and most significant "1" digit (3½ digits).

Display Type..... Black digits on white Liquid Crystal Display (LCD). Requires external illumination under low ambient light conditions.

Display Height ..... 0.5 inches (12,7 mm).

Overrange ..... Inputs exceeding the full scale range cause the 'OR' symbol in the upper left corner to flash (A Model only).

Autopolarity ..... A plus or minus sign is automatically displayed for positive or negative voltage inputs. The polarity display may be disabled by opening solder gap SG1.

Sampling Rate ..... Approximately 3 conversions per second.

Decimal Points ..... Automatically shifted by auto-ranging logic.

POWER REQUIREMENTS

External

+5V dc unregulated is required at 15mA typical, 30mA maximum. Logic spikes must not exceed 50mV. [Note: Any current consumed by external devices using the -5V output (pin A15) must be added to +5V power consumption to yield total meter power consumption.]

Power Output

-5V dc unregulated is available to the user by closing solder gap SG2 (normally open). The solder gap is located on the bottom of the converter/display board.

PIN DETAILS

PIN# SIGNAL DESCRIPTION

Analog HI Input (PINS A/B12)
Analog LO Input (PINS A/B9)

Differential input signals are applied to pins A/B12 and A/B9. A single-ended input configuration is available by closing solder gap SG4. This effectively ties the ANALOG LO to input (pins A/B9) to ANALOG COMMON (pins A/B15).

Reference IN/Out (Pins A13/B13)

The instrument is calibrated when a +0.1V dc drop exists between pins B13 (+) and B15 (-). An internal reference voltage circuit, adjustable by potentiometer R3, provides this reference voltage. To use this internal reference, the user joins pins A13 and B13 at the connector. If the user wishes to generate an external reference voltage, pin A13 is used as the input, biased against pin B15.

Busy/Done Out (Pin A11)

This output is High during A/D conversions. The falling edge indicates that a new valid digit Strobe output will appear in 1.3 milliseconds. The high Busy level may be used by automatic equipment to prevent changing the input voltage during conversion.

Digit Strobe Out (Pin B7, B8, B9, B10)

Strobe consists of 4 positive pulses per conversion of approximately 4 microseconds width and approximately 1.6 milliseconds apart issued after an A/D conversion. They indicate that valid multiplexed data is available on the BCD data output lines, starting with the Most Significant Digit (MSD). The Polarity of the BCD data is not multiplexed out with the BCD data. A fifth line (Polarity Out, Pin A12 must be polled to determine the sign.

Run/Hold IN (Pin B11)

For normal operation, leave this pin open. Grounding Pin B11 halts A/D conversions and displays the last valid sample until the pin returns to a high state.

Polarity Out (Pin A12)

A high on this line indicates a positive input; a low indicates a negative input. This output is valid even for a zero reading. In other words, a display of +0000 means that the signal is positive but less than the LSB.

-5V Power Out (Pin A15)

Up to 15mA of -5V dc power may be taken to power external user-supplied circuits such as signal conditioners.

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PHYSICAL-ENVIRONMENTAL

Outline Dimensions
2.53"W X 3.34"D X 0.94"H (64,3 X 85 X 23,8mm).

Cutout Dimensions
2.562"W X 0.97"H min. (65,1 X 24,6mm)

Weight
Approximately 5 ounces (142g).

Connector
Two dual 15-pin, 0.100" centers, Datel Part #58-2073083 (two included with meter).

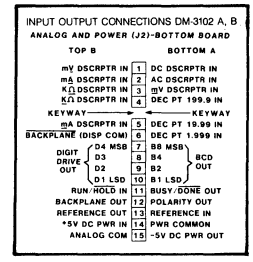
Mounting Position
Limited by readability of LCD's (typical viewing angle of 70%).

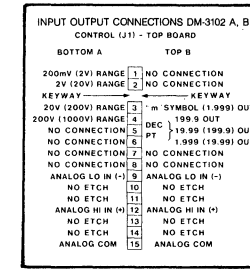
Operating Temperature Range
32°F to 122°F (0°C to +50°C)

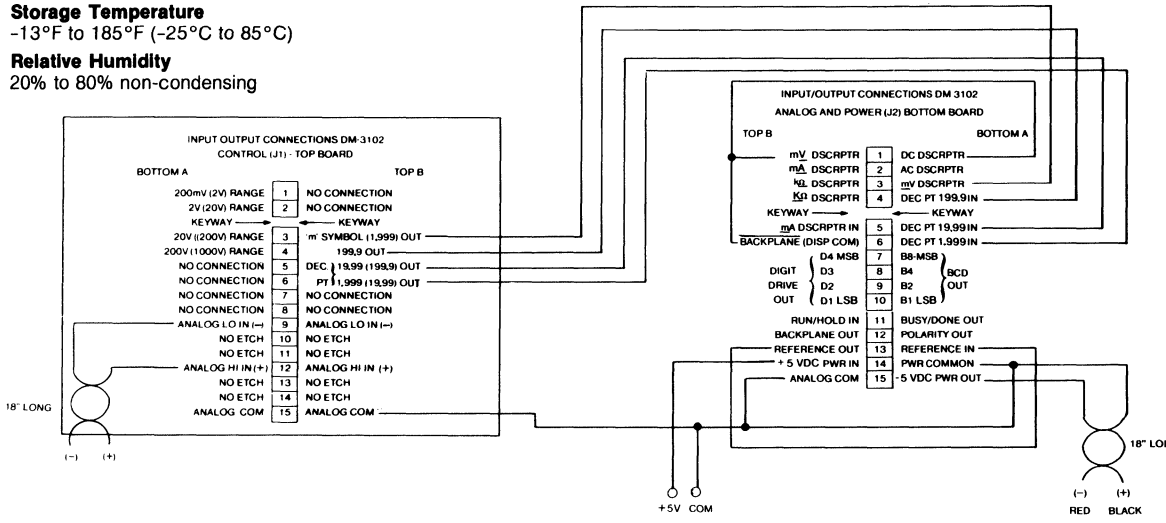
Altitude
0 to 15,000 feet (4,900m)

Storage Temperature
-13°F to 185°F (-25°C to 85°C)

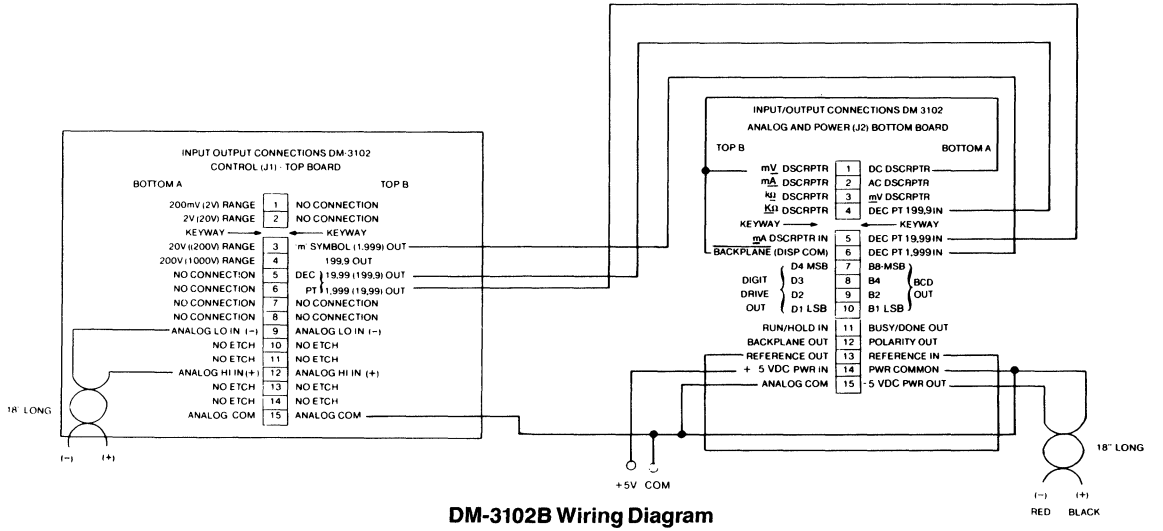
Relative Humidity
20% to 80% non-condensing







DM-3102A Wiring Diagram



DM-3102B Wiring Diagram

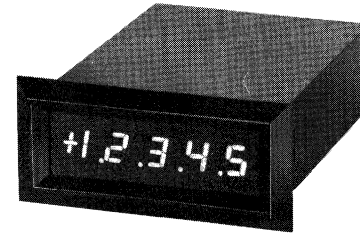
10

DM-4100D
4½ Digit Panel Meter with Tri-State Data Outputs

DATEL

FEATURES

- **Tri-state BCD data outputs**
- **Data outputs gated for use with 4-, 8-, 12- or 16-bit bus structures**
- **Standard ±1.9999V dc input range; user-installed options set other voltage or current ranges.**
- **High-impedance differential inputs with low 5 pA bias currents**
- **Autozeroing, ratiometric for drift-free operation**
- **Low power consumption: +5V dc at 500 mA**
- **Provides ±13.5V dc outputs at 20 mA for external circuits**
- **Up to 30 conversions per second possible**
- **Designed for single-ended, bipolar inputs**



GENERAL DESCRIPTION

The DM-4100D provides full 4½ digit DPM capabilities with tri-state BCD outputs. Built-in ability to provide 3½ digit displays with 10 times the normal sampling rate. Designed for single-ended inputs, this meter has all the features found in DATEL's DPM product line plus voltage and data outputs. The unit is accurate to within .02% FSR (±2 counts). Input circuitry is autozeroed on each conversion cycle to reduce zero drift. All this performance has been packed into a low-profile black polycarbonate case only 2.53" wide x 3.34" deep x 0.94" high (64,3 x 85 x 23,8mm).

The DM-4100D's 3-state BCD outputs take it beyond many so-called "microprocessor-compatible" DPM's. The 3-state outputs mean that the meter can be connected directly to a microcomputer's data bus. They also permit multiple DM-4100D's to be daisy-chained to a single set of computer or printer input connections — the computer inputs "see" only those meter outputs which have been enabled. And, since each 4-bit group (corresponding to a single BCD-encoded numeral) may be gated separately, a single rear-panel change makes the DM-4100D compatible with processors using 4-, 8-, 12-, or

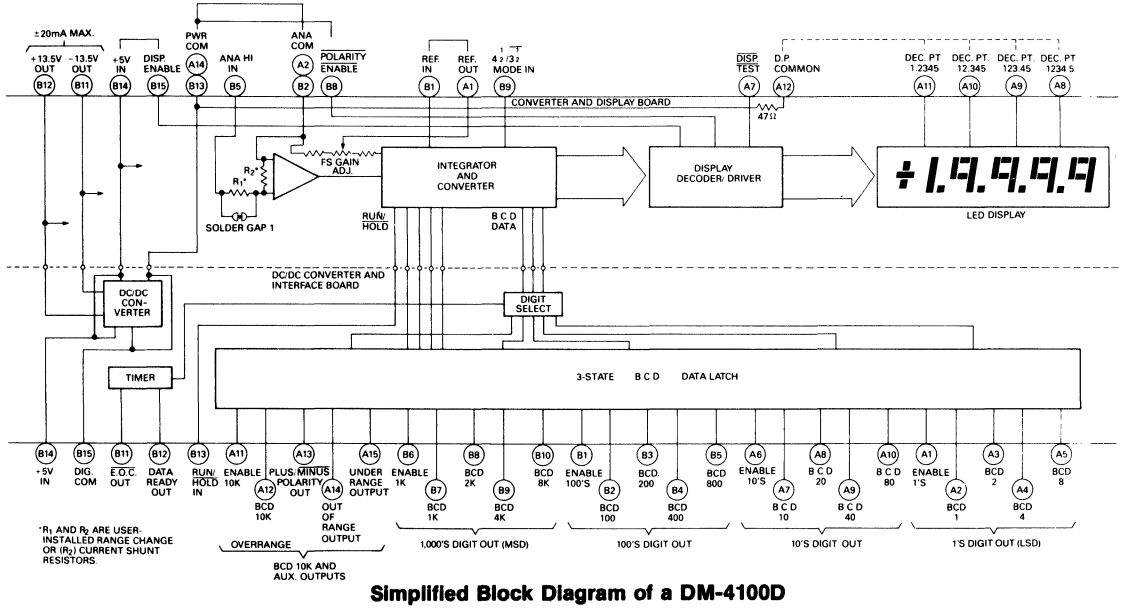
ORDERING INFORMATION

DM-4100D - 1

Model	Description
DM-4100D-1	Micro-bussable 4 1/2-Digit, single-ended input DPM (includes 2 connectors)

ACCESSORIES

Part Number	Description
58-2073083	Dual 15-pin edge connector, 0.1" centers
UPA-5/500	115V AC to 5V dc power adaptor



Simplified Block Diagram of a DM-4100D

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

16-bit data words. Digital outputs for the Display Polarity, Underrange, Out of Range, E.O.C., "Data Ready" (a 10 μsecond pulse occurring 10 μseconds after the digital data is valid), and meter Run/Hold status make microcomputer control of the meter possible with minimal external hardware. Sufficient control circuitry is already built into the DM-4100D so that it can directly interface with DATEL's DPP-Q7 thermal printer (or a similar printer) to become a functional data logger.

The DM-4100D's input CMOS circuitry can safely handle overvoltages to ±250V dc. The meter's converter board contains blank circuit pads to accept input attenuation resistors or current shunts. Temperature drift of the autozeroed input amplifier is ±1 count from 0° to +50°C. Temperature drift of gain measures ±50 ppm of FSR/°C (typical) and ±100 ppm of FSR/°C maximum.

The DM-4100D uses a dual slope integrating converter which provides normal mode rejection of AC power line noise. It provides an input-to-output conversion linearity to within ±.02% of reading, or ±2 counts. The standard sampling rate is 3 conversions per second, but a rear pin connector may be used to disable the least significant digit. In the 3½ digit mode, the DM-4100D provides 30 conversions/second.

Power to the meter is +5V dc @ 380 mA typical (500 mA maximum), and may be supplied directly from a microcomputer bus. A built-in dc-dc converter (to power the meter's analog input circuitry) provides ±13.5V dc ±5% (@ ±20 mA max.) to power user-supplied circuitry. The ±13.5V output was specifically intended to power an external instrumentation or CAZ amp, providing the DM-4100D with a differential analog input. DATEL's UPA-5/500, 5V @ 500mA power supply is available as an accessory.

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.
Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)
Input Bias Current ..... 5 pA (typical) 50 pA (maximum)
Input Overvoltage ..... ±250V dc, 155V RMS continuous (maximum) ±300V intermittent (maximum)
External Reference Range ..... +100 mV to +2V referred to Analog Common
Common-Mode Rejection Range ..... 80 dB (typical), from dc to 60 Hz, with 1 Kilohm unbalance
Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.
Resolution ..... 1 mV (least significant digit)
Display Accuracy ..... Adjustable to ±0.02% of reading, ±2 counts
Temperature Drift of Zero ..... Autozeroed ±1 count over 0 to +50°C temperature range
Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)
Sampling Time ..... 83.3 mS (nominal)
Sampling Rate ..... 3 conversions per second. May be rewired for up to 20 conversions per second

NOTE: The DM-4100D's display is not latched; the display may not track the meter's BCD data out.

DISPLAY

Number of Digits ..... 4 decimal digits and most significant "1" digit (4½ digits)
Decimal Points ..... Selectable using decimal point select signal lines.
Display Type ..... Red LED's
Display Height ..... 0.3" (7,6 mm)
Overscale ..... The display flashes when inputs exceed the full-scale range.
Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

CALIBRATION

A multiturn screwdriver pot (rear-panel mounted) adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

POWER CONSUMPTION

The DPM requires +5V dc regulated (±5%) at 380 mA typical and 500 mA maximum. Logic spikes must not exceed 50 mV. Any current taken from the ±13V dc outputs must be added to the above specifications to yield the total meter power consumption.

PHYSICAL

External Dimensions
2.53"W x 3.34"D x 0.95"H (64,3 x 85 x 23,8mm)

Panel Cutout Dimensions
2.562"W x 0.97"H (65,1 x 24,6mm)

Weight
Approximately 4.1 ounces (116 grams)

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0° to 50°C)

Storage Temperature Range
-13°F to +195°F (-25°C to +85°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

J2 ANALOG CONNECTOR (LOWER)

-13V, +13V dc Power Out (Pins B11, B12)
Up to 20mA of unregulated + and -13.5V dc power may be taken directly from the meter to power external user-supplied circuits such as signal conditioners.

Analog H1 Input (Pin B5)
Signal input normal voltage range is -1.9999 to +1.9999V dc.

3½/4½ Mode Input (Pin B9)
Leave open or high for 4½ digit mode. Logic low (connected to POWER COMMON) causes Least Significant Digit to read permanent zero, and causes meter to operate in 3½ digit mode. Conversions in 3½ digit mode occur at 10 times usual speed, i.e., 30 conversions per second.

+5V In (Pin B14)
Power input to the meter; connections made between +5V IN and POWER COMMON (pins A14 and B13); requires regulated supply (±5%), capable of supplying 500 mA maximum.

J1 DATA CONNECTOR (UPPER)

Digit Enable Input
These are active high, and operate on data in groups of 4 bits (e.g., Enable 10's controls BCD 10, 20, 40 and 80; Enable 10,000's controls BCD 10,000 (overrange), PLUS/MINUS, OUT OF RANGE, and UNDERRANGE.

Enable 1's (Pin A1)
Enable 10's (Pin A6)
Enable 100's (Pin B1)
Enable 1,000's (Pin B6)
Enable 10,000's (Pin A11)

BCD Data Outputs
1, 2, 4, 8 (and 10, 20, 40, 80, etc) BCD data is fully latched. Outputs are 3-state and controlled in groups of 4. Outputs are DTL/TTL compatible, positive true, and sink 4.0 mA @ 0.4V (2½ TTL loads).

BCD 1 (Pin A2), 2 (Pin A3), 4 (Pin A4), 8 (Pin A5)
BCD 10 (Pin A7), 20 (Pin A8), 40 (Pin A9), 80 (Pin A10)
BCD 100 (Pin B2), 200 (Pin B3), 400 (Pin B4), 800 (Pin B5)
BCD 1000 (Pin B7), 2000 (Pin B8), 4000 (Pin B9), 8000 (Pin B10)
BCD 10,000 (Pin A12)

Plus/Minus Polarity Out (Pin A13)
This is true for positive input. 3-state latch enabled by pin A11.

BCD OUTPUT

Format
BCD outputs 3-state, gatable in 4-bit groups, full parallel output available.

Fanout
2½ TTL loads.

Logic Controls
E.O.C. pulse, "Data Ready" (Print Pulse), Overrange, Underrange, Out of Range, PLUS/MINUS Polarity OUT, and RUN/HOLD.

D.C. Power In
+5V dc, regulated (±5%), @ 380 mA typical, 500 mA maximum.

D.C. Power Out
±13.5V dc, ±5%, @ ±20 mA, unregulated, for external signal conditioning.

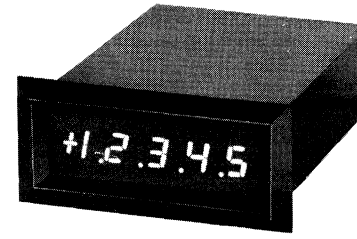
INPUT/OUTPUT CONNECTIONS DM-4100D
ANALOG AND POWER (J2)-BOTTOM BOARD

BOTTOM A		TOP B
REFERENCE OUT	1	REFERENCE IN
ANALOG COM	2	ANALOG COM
NO CONNECTION	3	NO CONNECTION
NO CONNECTION	4	NO CONNECTION
KEYWAY →		← KEYWAY
NO CONNECTION	5	ANALOG HI IN
NO CONNECTION	6	NO CONNECTION
DISPLAY TEST	7	NO CONNECTION
D.P. 1234.5	8	POLARITY ENABLE
D.P. 123.45	9	4 1/2 3 1/2 MODE
D.P. 12.345	10	NO CONNECTION
D.P. 1.2345	11	-13.5V OUT (20mA)
D.P. COM	12	+13.5V OUT (20mA)
NO CONNECTION	13	PWR COMMON
PWR COMMON	14	+5V IN
NO CONNECTION	15	DISPLAY ENABLE

INPUT/OUTPUT CONNECTIONS DM-4100D
DIGITAL INTERFACE (J1)-TOP BOARD

BOTTOM A		TOP B
ENABLE 1's	1	ENABLE 100's
BCD 1	2	BCD 100
KEYWAY →		← KEYWAY
BCD 2	3	BCD 200
BCD 4	4	BCD 400
BCD 8	5	BCD 800
ENABLE 10	6	ENABLE 1K
BCD 10	7	BCD 1K
BCD 20	8	BCD 2K
BCD 40	9	BCD 4K
BCD 80	10	BCD 8K
ENABLE 10K	11	E.C.O.
BCD 10K	12	DATA READY
PLUS/MINUS OUT	13	RUN/HOLD
OUT OF RANGE	14	+5V IN
UNDERRANGE	15	DIGITAL COMMON

DM-4101D
4½ Digit LED Panel Meter with Tri-State Data Outputs



FEATURES

- **Tri-state BCD data outputs**
- **Data outputs gated for use with 4-, 8-, 12- or 16-bit bus structures**
- **Standard ±1.9999V dc input range; user-installed options set other voltage or current ranges.**
- **High-impedance differential inputs with low 5 pA bias currents**
- **Autozeroing, ratiometric for drift-free operation**
- **Low power consumption: +5V dc at 450 mA**
- **Provides ±5V dc outputs at 15 mA for external circuits**
- **Designed for differential, bipolar inputs**

GENERAL DESCRIPTION

The DM-4101D provides full 4½ digit DPM capabilities along with tri-state BCD outputs. Designed for differential bipolar inputs, this device provides an ideal display function without loading down sensitive input signals. The unit is accurate to within .02% FSR (±2 counts). Input circuitry is autozeroed on each conversion cycle to reduce zero drift. All this performance has been packed into a low-profile black polycarbonate case only 2.53" wide x 3.34" deep x 0.94" high (64,3 x 84,8 x 23,8mm).

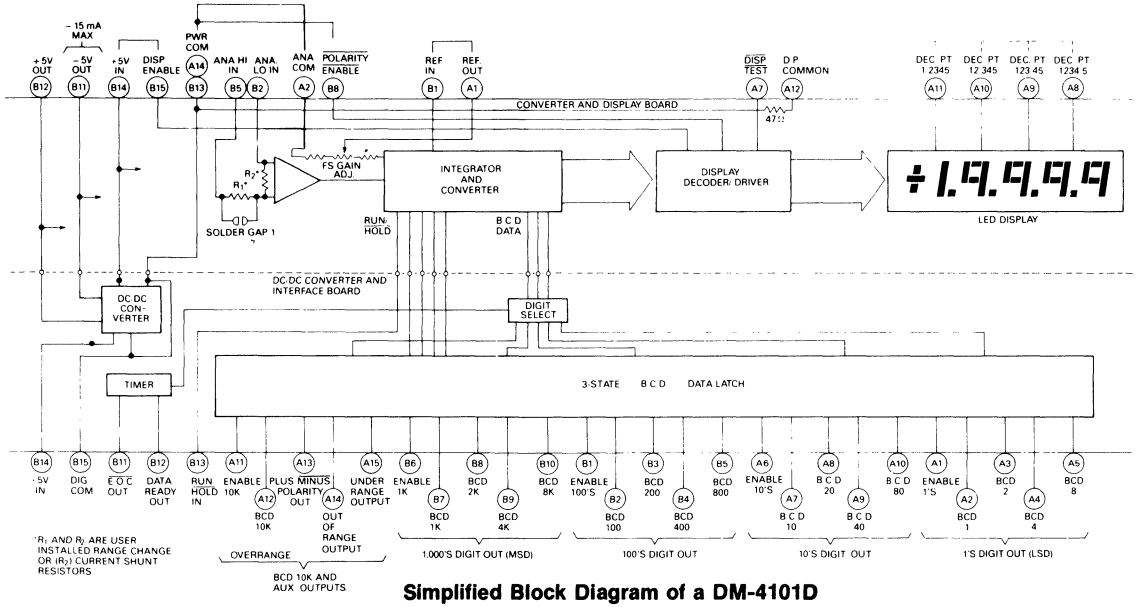
The DM-4101D's 3-state BCD outputs take it beyond many so-called "microprocessor compatible" DPM's. Tri-state outputs mean that the meter can be connected directly to a microcomputer's data bus. They also permit multiple DM-4101D's to be daisy-chained to a single set of computer or printer input connections — the computer inputs "see" only those meter outputs which have been enabled. And, since each 4-bit group (corresponding to a single BCD-encoded numeral) may be gated separately, a single rear-panel change makes the DM-4101D compatible with processors using 4-, 8-, 12-, or 16-bit data words. Digital outputs for the Display Polarity, Underrange, Out of Range, E.O.C., "Data Ready" (a 10 microsecond pulse occurring 10 microseconds after the digital data is valid), and meter Run/Hold status make microcomputer control of the meter possible with minimal external hardware. Sufficient control circuitry is already built into the DM-4101D so that it can directly interface with DATEL's DPP-Q7 thermal printer (or a similar printer) to become a functional data logger.

ORDERING INFORMATION
DM-4101D - 1

Model	Description
DM-4101D-1	Micro-bussable 4 1/2 Digit DPM (includes 2 connectors)

ACCESSORIES

Part Number	Description
58-2073083	Dual 15-pin edge connector
UPA-5/500	115V AC to 5V dc power adaptor



Simplified Block Diagram of a DM-4101D

The DM-4101D's input CMOS circuitry can safely handle overvoltages to ±250V dc. The meter's converter board contains blank circuit pads to accept input attenuation resistors or current shunts. Temperature drift of the autozeroed input amplifier is ±1 count from 0 to +50°C. Temperature drift of gain measures ±50 ppm of FSR/°C (typical) and ±100 ppm of FSR/°C maximum.

The DM-4101D uses a dual slope integrating converter which provides normal mode rejection of AC power line noise. It provides an input-to-output conversion linearity to within ±.02% of reading ±2 counts. The standard sampling rate is 3 conversions per second.

Power to the meter is +5V dc @ 380 mA typical (450 mA maximum), and may be supplied directly from a microcomputer bus. A built-in dc-dc converter (to power the meter's analog input circuitry) provides ±5V dc ±5% (@ ±15 mA maximum) to power user-supplied circuitry. The ±5V output was specifically intended to power an external instrumentation or CAZ amp, providing the DM-4101D with a differential analog input. DATEL's UPA-5/500, 5V @ .5A AC power supply is available as an accessory.

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... See "FEATURES" range field modifiable

Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical) 50 pA (maximum)

Input Overvoltage ..... ±250V dc, 155V RMS continuous (maximum) ±300V intermittent (maximum)

External Reference Range ..... +100 mV to +2V dc referred to Analog Common

Common-Mode Rejection Range ..... 80 dB (typical), from dc to 60 Hz, with a 1 Kilohm unbalanced input

Common-Mode Voltage Range ..... Both the inputs must remain within ±2V dc maximum of power ground

Resolution ..... 1 mV (least significant digit)

Display Accuracy ..... Adjustable to ±0.2% of reading, ±2 counts

Temperature Drift of Zero ..... Autozeroed ±1 count over 0 to +50°C temperature range

Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)

Sampling Time ..... 83.3 mS (nominal)

Sampling Rate ..... 3 conversions per second.

DISPLAY

Number of Digits ..... 4 decimal digits and most significant "1" digit (4½ digits)

Decimal Points ..... Selectable using decimal point select signal lines.

Display Type ..... Red LED's

Display Height ..... 0.39" (9,9 mm)

Overscale ..... The display flashes when inputs exceed the full-scale range.

Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

NOTE: The DM-4101D's display is not latched; therefore, the display may not track the meter's BCD data output.

POWER CONSUMPTION

The DPM requires +5 dc regulated (±5%) at 380 mA typical and 500 mA maximum. Logic spikes must not exceed 50 mV. Any current taken from the ±5V dc outputs must be added to the above specifications to yield the total meter power consumption.

PHYSICAL

External Dimensions
2.53"W x 3.34"D x 0.95"H (64,3 x 85 x 23,8mm)

Panel Cutout Dimensions
2.562"W x 0.97"H (65,1 x 24,6mm)

Weight
Approximately 4.1 ounces (116 grams)

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0° to 50°C)

Storage Temperature Range
-13°F to +195°F (-252°C to +85°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

J2 ANALOG CONNECTOR (LOWER)

+5V Out (Pin B12)
-5V Out (Pin B11)
These voltage outputs provide +1A and -15 mA respectively to power user-supplied external circuitry. May be used to power an instrumentation or C.A.Z. amplifier.

J1 DATA CONNECTOR (UPPER)

Digit Enable Input

These are active high, and operate on data in groups of 4 bits (e.g., Enable 10's controls BCD 10, 20, 40 and 80; Enable 10,000 controls BCD 10,000 (overrange), PLUS/MINUS, OUT OF RANGE, and UNDERRANGE.

Enable 1's (Pin A1)
Enable 10's (Pin A6)
Enable 100's (Pin B1)
Enable 1,000's (Pin B6)
Enable 10,000's (Pin A11)

BCD Data Outputs

1, 2, 4, 8 (and 10, 20, 40, 80, etc) BCD data is fully latched. Outputs are 3-state and controlled in groups of 4. Outputs are DTL/TTL compatible, positive true, and sink 4.0 mA @ 0.4V (2½ TTL loads).

BCD 1 (Pin A2), 2 (Pin A3), 4 (Pin A4), 8 (Pin A5)
BCD 10 (Pin A7), 20 (Pin A8), 40 (Pin A9), 80 (Pin A10)
BCD 100 (Pin B2), 200 (Pin B3), 400 (Pin B4), 800 (Pin B5)
BCD 1000 (Pin B7), 2000 (Pin B8), 4000 (Pin B9), 8000 (Pin B10)
BCD 10,000 (Pin A12)
Plus/Minus Polarity Out (Pin A13)
This is true for positive input. 3-state latch enabled by pin A11.

BCD OUTPUT

Format

BCD outputs 3-state, gatable in 4-bit groups, full parallel output available.

Fanout

2½ TTL loads.

Logic Controls

E.O.C. pulse, "Data Ready" (Print Pulse), Overrange, Underrange, Out of Range, PLUS/MINUS Polarity OUT, and RUN/HOLD.

CALIBRATION

A multiturn screwdriver pot (rear-panel mounted) adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration in stable conditions is 90 days.

POWER CONNECTIONS

+5V In (Pin B14)

Power input to the meter; connections made between +5V IN and POWER COMMON (pins J1-A14 and B13 and J2-B14); requires a regulated supply (±5%), capable of supplying 450 mA max.

INPUT OUTPUT CONNECTIONS DM-4101D
ANALOG AND POWER (J2)-BOTTOM BOARD

BOTTOM A		TOP B
REFERENCE OUT	1	REFERENCE IN
ANALOG COM	2	ANALOG LO IN
NO CONNECTION	3	NO CONNECTION
NO CONNECTION	4	NO CONNECTION
KEYWAY →		← KEYWAY
NO CONNECTION	5	ANALOG HI IN
NO CONNECTION	6	NO CONNECTION
DISPLAY TEST	7	NO CONNECTION
D.P. 1234.5	8	POLARITY ENABLE
D.P. 123.45	9	NO CONNECTION
D.P. 12.345	10	NO CONNECTION
D.P. 1.2345	11	-5V OUT (15 mA)
D.P. COM	12	+5V OUT
NO CONNECTION	13	PWR COMMON
PWR COMMON	14	+5V IN
DISPLAY BLANK	15	DISPLAY ENABLE

INPUT/OUTPUT CONNECTIONS DM-4101D
DIGITAL INTERFACE (J1)-TOP BOARD

BOTTOM A		TOP B
ENABLE 1's	1	ENABLE 100's
BCD 1	2	BCD 100
KEYWAY →		← KEYWAY
BCD 2	3	BCD 200
BCD 4	4	BCD 400
BCD 8	5	BCD 800
ENABLE 10'S	6	ENABLE 1K'S
BCD 10	7	BCD 1K
BCD 20	8	BCD 2K
BCD 40	9	BCD 4K
BCD 80	10	BCD 8K
ENABLE 10K	11	E.C.O.
BCD 10K	12	DATA READY OUT
PLUS/MINUS OUT	13	RUN/HOLD IN
OVERRANGE OUT	14	+5V IN
UNDERRANGE OUT	15	DIGITAL COMMON

10

DM-4101L
4½ Digit LED Panel Meter with Data Outputs

DATEL

FEATURES

- **Large .56" digits**
- **Replaces the DM-4100L with improved driver circuit for 20% brighter LED display**
- **±5V dc outputs at 15 mA for user's circuits**
- **Balanced differential inputs with 5 pA bias currents**
- **Internal ratiometric reference for drift correction**
- **Autozeroing with 86dB CMR noise rejection**
- **Standard ±1.9999V dc input range; user-installed options set other voltage or current ranges.**
- **BCD Outputs available to drive DM-4103 slave displays**

GENERAL DESCRIPTION

The DM-4101L replaces DATEL's older DM-4100L DPM, offering higher performance at an even lower price. The improved display driver circuitry gives a 20% brighter output from the .56" high LED's. Besides offering DATEL's standard input features, this device provides multiplexed BCD outputs. These outputs can drive a remote display, such as the DM-4103, or be used by an external microprocessor. This DPM is housed in a short-depth case, a feature appreciated by many OEM's.

The quality performance features of the DM-4100L have been retained. CMOS circuitry provides an extremely high input impedance (1000 Megohms), and extremely low input bias current (5 picoamps). The meter's dual slope converter autozeroes the input in each conversion cycle for a true zero reading. And a reference in/out loop permits use of the DM-4101L in ratiometric and bridge-type circuits.

Additional features include a Busy/Done Output which indicates when an A/D conversion is complete. Overscale and Underscale outputs can be used with external circuitry for autoranging. A Run/Hold line permits a reading to be held for several seconds while an operator copies down the reading. And an externally-accessible Display Enable line can blank the display to minimize power consumption, while the A/D converter and BCD outputs are running to drive an external slave display. BCD outputs, used in conjunction with a strobe line from the DM-4101L's A/D converter, can drive a remote slave display (Model DM-4103), or provide A/D data conversion for a microprocessor.

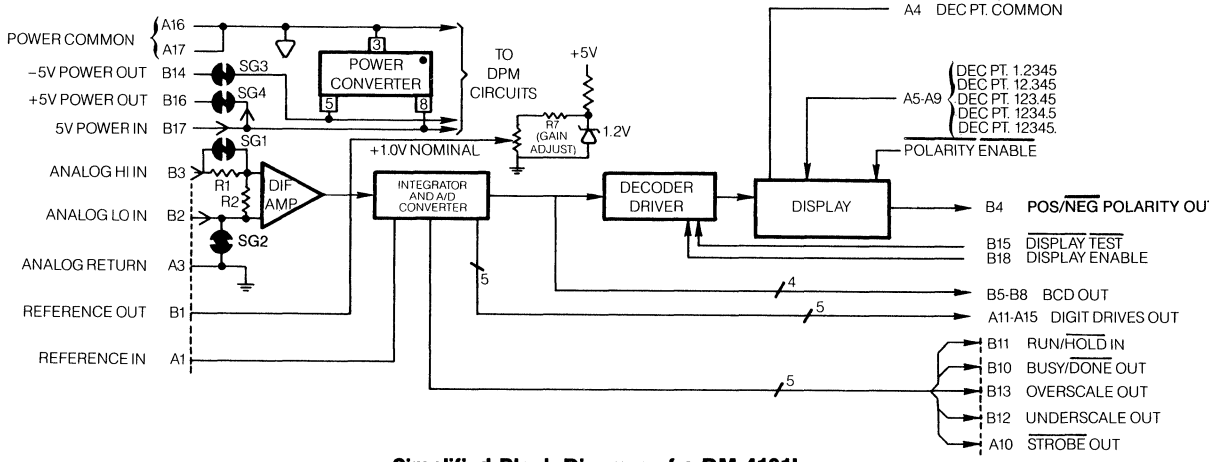
Power to the meter is +5V dc at 350 mA maximum. A dc-to-dc converter in the DM-4101L provides a -5V dc output (at 15 mA maximum) to power user circuitry.

ORDERING INFORMATION
DM-4101L - 1

Model	Description
DM-4101L-1	4 1/2-digit DPM with BCD outputs (Includes one connector)
DM-4103	MUX'D BCD Slave Display

ACCESSORIES

Part Number	Description
58-2075010	Dual 18-pin, 0.1" centers PC edgeboard connector
UPA-5/500	115V AC to 5V dc power adaptor



Simplified Block Diagram of a DM-4101L

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FUNCTIONAL SPECIFICATIONS
(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... As specified in "FEATURES"

Input Impedance ..... 100 Megohms (minimum)
1000 Megohms (typical)

Input Bias Current ..... 5 pA (typical) 50 pA (maximum)

Input Overvoltage ..... ±250V dc, 175 VRMS continuous (maximum)
±300V intermittent (maximum)

External Reference Range ..... +100 mV to +2V referred to Analog Return

Common-Mode Rejection ..... 86 dB typical to Analog Return

Common-Mode Voltage Range ..... Both inputs must remain within ±4V of Power Common

Resolution ..... 100 μV in last digit

Displayed Accuracy ..... Adjustable to ±0.2% of reading, ±2 counts

Temperature Drift of Zero ..... Autozeroed ±1 count over 0° to +50° C

Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical), ±100 ppm of Reading/°C (maximum)

Ramp-up Time (Integration Period) ..... 83.3 mS

Sampling Rate ..... Approximately 3 conversions per second.

DISPLAY

Number of Digits ..... 4 decimal digits and most significant "1" digit (4½ digits)

Decimal Points ..... Right-of-digit selectable decimal points are included for scale multipliers

Display Type ..... Red, light-emitting diode (LED), self-illuminated

Display Height ..... 0.56 inches (14,2 mm)

Overscale ..... Inputs exceeding the full-scale range cause the display to blink

Autopolarity ..... A "+" is displayed for positive inputs, a "-" for negative inputs. Polarity may be disabled.

Sampling Rate ..... Approximately 3 conversions per second.

POWER REQUIREMENTS

External +5V, ±0.25V dc regulated required at 350 mA maximum, 250 mA typical. Logic spikes must not exceed 50 mV. (+5V OUT and -5V OUT current must be added to the +5V power requirements for total meter consumption.

PHYSICAL

External Dimensions
Short-Depth Case 3.0"W x 2.15"D x 1.76"H (76,2 x 54,6 x 44,7 mm)

Panel Cutout Dimensions
1.812"H x 3.062"W (46,0 x 77,7 mm)

Mounting Method
Refer to end of this section.

Weight
5 ounces (142g) approximately

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0° to 50°C)

Storage Temperature Range
-13°F to +185°F (-25°C to 85°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

Reference Output (Pin B1)
Reference Input (Pin A1)
Normally Pins A1 and B1 are jumpered together. The instrument is calibrated when a + 1.0V dc drop exists between Pins A1 (+) and A3 (-). An external reference input to Pin A1 which is biased against Pin A3 may be used by disconnecting Pin B1. Ratiometric drift-correcting action may then be achieved over the reference input range of +0.1V dc to +2.0V dc.

-5V Power Out (Pin B14)
Up to 15 mA of -5V dc power may be taken to power external user-supplied circuits such as signal conditioners.

+5V Power Out (Pin B16)
is an additional +5V power source.

INPUT/OUTPUT CONNECTIONS DM-4101L

BOTTOM A		TOP B
REFERENCE IN	1	REFERENCE OUT
ANALOG GND	2	ANALOG LO IN (-)
ANALOG GND	3	ANALOG HI IN (+)
DEC PT COM	4	POLARITY OUT
DEC PT 1.9999	5	B1 LSB (BCD)
DEC PT 19.999	6	B2 (BCD)
DEC PT 199.99	7	B4 (BCD)
DEC PT 1999.9	8	B8 MSB (BCD)
DEC PT 19999.	9	NO CONNECTION
STROBE OUT	10	BUSY/DONE OUT
DIGIT DRIVE OUT D1 LSB	11	RUN/HOLD IN
DIGIT DRIVE OUT D2	12	UNDERSCALE OUT
DIGIT DRIVE OUT D3	13	OVERSCALE OUT
DIGIT DRIVE OUT D4	14	-5VDC PWR OUT
DIGIT DRIVE OUT D5 MSD	15	DISPLAY TEST IN
PWR COMMON	16	+5VDC PWR OUT
PWR COMMON	17	+5VDC PWR IN
POLARITY ENABLE	18	DISPLAY ENABLE

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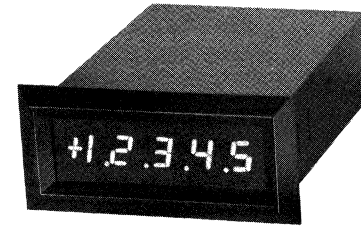
DM-4101N
4½ Digit Differential Input LED Panel Meter

DATEL

FEATURES

- **Improved replacement for the DM-4100N**
- **Improved driver circuit for 20% brighter LED display**
- **Balanced, high-impedance differential inputs with 5 pA bias currents**
- **Internal ratiometric reference for drift correction**
- **± 5V dc outputs at 15 mA for user's circuits**
- **Displayed digits are .3" high**
- **Standard ±1.9999V dc input range; user-installed options set other voltage or current ranges.**



GENERAL DESCRIPTION

The DM-4101N replaces DATEL's older DM-4100N DPM, offering higher performance at an even lower price. Improved display driver circuitry yields a 20% brighter output from the .3" high LED's while requiring a maximum of 350 mA current. This device is packaged in a low-profile case, allowing a higher packing density on the final product's panel.

The DM-4101N offers such high performance features as ultra-high impedance analog signal inputs (1000 MΩ, typically) which require extremely low input bias currents (5 pA typical). Inputs are bipolar and autozeroed.

Other features include Overrange and Underrange Outputs which can be used in external autoranging circuits; a Hold input which permits display of a given value indefinitely; and a Busy/Done line which goes low at the end of a conversion cycle. The DM-4101N's display may be disabled to reduce power consumption, while keeping the A/D converter cycling. A Reference In/Out line can accept an external reference for use in ratiometric and bridge-type applications.

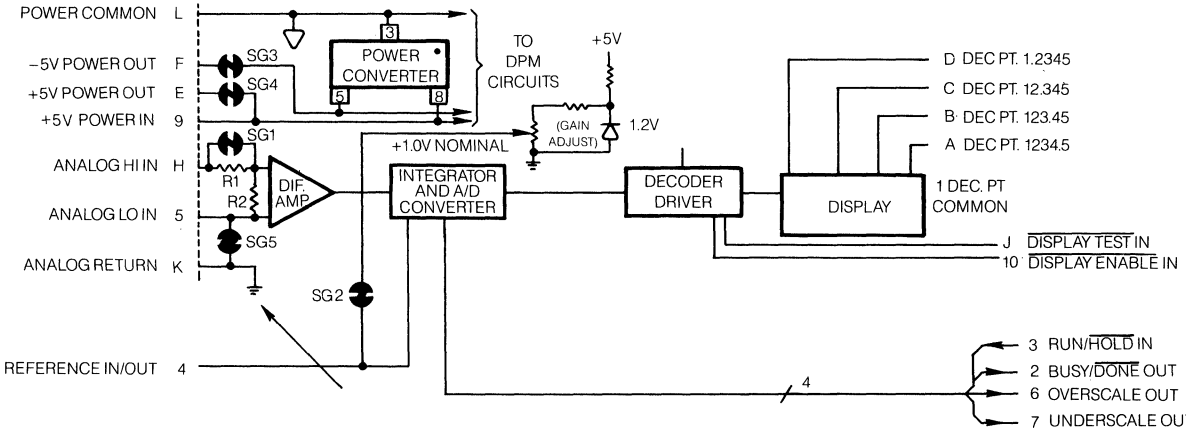
Power to the meter is +5V dc @ 250 mA max. -5V Out @ 15 mA is available to power user circuits.

ORDERING INFORMATION
DM-4101N - 1

Model	Description
DM-4101N-1	4 1/2-digit panel motor (includes one connector)

ACCESSORIES

Part Number	Description
58-2073082	Dual 10-pin 0.156" centers, PC edgeboard connector (not included with DPM)
UPA-5/500	115V AC to 5V dc power adaptor



Simplified Block Diagram of a DM-4101N

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.

Input Bias Current ..... 5 pA (typical) 50pA (maximum)

Displayed Accuracy .... Adjustable to ±0.2% of reading, ±2 counts

Resolution ..... 100 μV in last digit

Temperature Drift of Zero ..... Autozeroed ±1 count over 0°C to +50°C

Temperature Drift of Gain ..... +50 ppm of reading/°C typical, ±100 ppm of reading/°C maximum

Input Impedance ..... 100 Megohms, minimum; 1000 Megohms, typical

Input Overvoltage

ANALOG LO IN ..... ±5V dc maximum continuous referred to Power Common

ANALOG HI IN ..... ±100V dc maximum continuous or ±250V dc for 5 seconds referred to Power Common

External Reference Range ..... +100 mV to +2V referred to Analog Return

Common Mode Rejection ..... 86 dB typical to Analog Return at dc

Common Mode Voltage Range ..... Both inputs must remain within ±4.0V dc of Power Common

DISPLAY

Number of Digits ..... Four decimal digits and most significant "1" digit

Display Type ..... Red, light-emitting diode (LED)

Display Height ..... 0.3 inches (7,6mm)

Overscale ..... Inputs exceeding the full scale range cause the display to blink.

Autopolarity ..... A minus sign is automatically displayed for negative voltage inputs and may be blanked.

Sampling Rate ..... 3 Conversions per second

POWER REQUIREMENTS

External +5, ±0.25V dc regulated required at 250 mA typical, 350 mA maximum. Logic spikes must not exceed 50 mV. +5V OUT and -5V OUT currents must be added to the +5V IN power requirements.

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration is 90 days.

PHYSICAL

External Dimensions
2.53"W x 3.25"D x 0.94"H (64,3 x 82,5 x 23,8mm)

Panel Cutout Dimensions
2.56"W x 0.97"H (65,1 x 24,mm)

Mounting Method
Refer to end of this section.

Weight
5 ounces (142g) approximately

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperture Range
+32°F to 122°F (0° to 50°C)

Storage Temperature Range
+32°F to 131°F (0° to 55°C)

Relative Humidity
20% to 80% non-condensing

INPUT/OUTPUT CONNECTIONS DM-4101N

BOTTOM			TOP
DEC PT 1999.9	A	1	DEC PT COM
DEC PT 199.99	B	2	BUSY/$\overline{\text{DONE}}$ OUT
DEC PT 19.999	C	3	RUN/$\overline{\text{HOLD}}$ IN
DEC PT 1.9999	D	4	REF IN/OUT
+5VDC PWR OUT	E	5	ANALOG LO IN(-)
-5VDC PWR OUT	F	6	OVERSCALE OUT
ANALOG HI IN(+)	H	7	UNDERSCALE OUT
$\overline{\text{DISPLAY TEST}}$ IN	J	8	DISPLAY ENABLE
ANALOG GND	K	9	+5VDC PWR IN
PWR COMMON	L	10	POLARITY ENABLE

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DM-4102, DM-4103, DM-4106
4½ Digit Multiplexed BCD Input LED Slave Displays

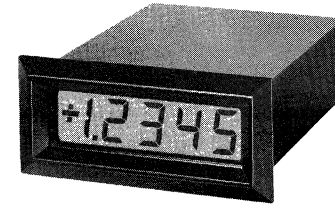
DATEL

FEATURES

- **Remote slave displays for DATEL digital panel meters**
- **Data repeater for second operator station up to 25 feet away**
- **Simple 12-wire interface, ideal for ribbon cable**
- **Operates with any 3 to 4½ digit DPM with multiplexed BCD data outputs**

DM-4102

DM-4103



DM-4106

GENERAL DESCRIPTION

The slave display meters function as repeaters for decimal data from a master data source. Data sources include DATEL's DPM's and a variety of microprocessor peripheral interface circuits. Depending on the model, the multiplexed BCD data is displayed using either LED or LCD display technology. The DM-4102 (LED) and the DM-4106 (LCD) are packaged in a low profile case, while the DM-4103 (LED) is packaged in a short depth case. The DM-4106 may use a battery source and is suitable for digital thermometer repeater applications.

Any of these slave displays may be used interchangeably with the multiplexed BCD output DPM's by rewiring the connector.

CIRCUIT OPERATION

To reduce the amount of wiring required to implement a slave display, 4-wire BCD data is multiplexed using 5 digit drive outputs which direct the BCD data to the proper digit. Using the DM-4200, -4101L and -4105 master DPM's as BCD data sources, these slave displays rely on the persistence of vision of the human eye to store an image of the displayed digit. This multiplexing technique is commonly used with DPM's and DVM's. Each digit drive has the effect of sequentially turning on its respective digit when the drive signal is high. The digit is blanked when the drive is low.

Digits are scanned in this manner in the DM-4101L, -4200, and -4105 approximately 150 times per second. The BCD data is updated with every A/D conversion which is approximately 3 times per second. For applications from other multiplexed data sources, digits must be updated at least 30 times a second (30 scans/sec) to avoid annoying display flicker.

Full parallel input data will require a multiplexer and possibly a storage register.

These display slaves may be connected to popular microprocessors by using peripheral interface circuits and a suitable rotating stack (FIFO) driver program.

ORDERING INFORMATION

Model	Description
DM-4102	4½ digit, LED, low-profile slave
DM-4103	4½ digit, LED, short-depth slave
DM-4106	4½ digit, LCD, low-profile slave

To Order, Specify Model Number.

ACCESSORIES

Part Number	Description
58-2073083	15-pin edge connector for DM-4102 and DM-4106 (one included with each order)
58-2075013	18-pin edge connector for DM-4103 (one included with each display)

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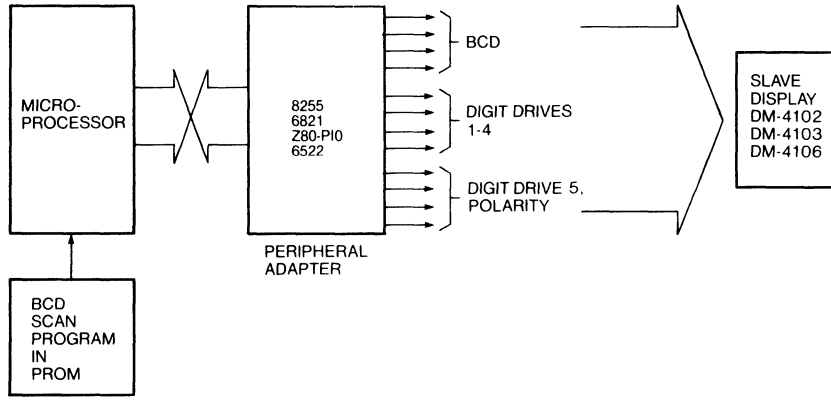

Microprocessor Output To Slave Display

FUNCTIONAL SPECIFICATIONS

Data Input ..... Multiplexed 1-2-4-8 binary coded decimal (BCD) data and polarity, TTL logic levels ("0" ≤ 0.08V, "1" ≥ 2.0V), 1 TTL load. Multiplex rate 30 scans/second minimum.

Display ..... 4½ digits (±19999 counts).

Power Required ..... +5V dc regulated, wired from master DPM. DM-4102 5V @ 250 mA max. DM-4103 5V @ 350 mA max. DM-4106 5V @ 10 mA max.

Operating Temperature Range . 32°F to 122°F (0° to +50°C)

Storage Temperature Range .... -13°F to +131°F -25°C to +55°C.

Case Material ..... Polycarbonate Plastic.

Mounting Method ..... Refer to end of this section.

Decimal Points ..... Jumper-selected 1.2.3.4.5, on rear connector.

INPUT/OUTPUT CONNECTIONS DM-4102

BOTTOM A		TOP B
DEC PT 19.999	1	DEC PT 1999.9
DEC PT 1.9999	2	DEC PT 199.99
POLARITY INPUT	3	NO CONNECTION
NO CONNECTION	4	NO CONNECTION
NO CONNECTION	5	DISPLAY TEST
NO CONNECTION	6	B1 LSB
NO CONNECTION	7	B2 (BCD INPUTS)
NO CONNECTION	8	B4 (BCD INPUTS)
D1 LSD	9	B8 MSB (BCD INPUTS)
DIGIT DRIVE INPUTS D2	10	DISPLAY ENABLE
DIGIT DRIVE INPUTS D3	11	DEC PT COM
DIGIT DRIVE INPUTS D4	12	NO CONNECTION
DIGIT DRIVE INPUTS D5 MSD	13	OVERSCALE INPUT
PWR COMMON	14	+5VDC PWR IN
NO CONNECTION	15	+5VDC PWR OUT

INPUT/OUTPUT CONNECTIONS DM-4103

BOTTOM A		TOP B
NO CONNECTION	1	NO CONNECTION
NO CONNECTION	2	NO CONNECTION
NO CONNECTION	3	NO CONNECTION
DEC PT COM	4	POLARITY INPUT
DEC PT 1.9999	5	B1 LSB (BCD INPUTS)
DEC PT 19.999	6	B2 (BCD INPUTS)
DEC PT 199.99	7	B4 (BCD INPUTS)
DEC PT 1999.9	8	B8 MSB (BCD INPUTS)
DEC PT 19999.	9	NO CONNECTION
NO CONNECTION	10	NO CONNECTION
D1 LSD	11	NO CONNECTION
DIGIT DRIVE INPUTS D2	12	NO CONNECTION
DIGIT DRIVE INPUTS D3	13	OVERSCALE INPUT
DIGIT DRIVE INPUTS D4	14	NO CONNECTION
D5 MSD	15	DISPLAY TEST IN
PWR COMMON	16	+5VDC PWR OUT
PWR COMMON	17	+5VDC PWR IN
POLARITY ENABLE	18	DISPLAY ENABLE

INPUT/OUTPUT CONNECTIONS DM-4106

BOTTOM A		TOP B
DEC PT 19.999	1	DEC PT 1999.9
DEC PT 1.9999	2	DEC PT 199.99
POLARITY INPUT	3	NO CONNECTION
NO CONNECTION	4	NO CONNECTION
NO CONNECTION	5	DEGREE SIGN IN
NO CONNECTION	6	B1 LSB (BCD INPUTS)
NO CONNECTION	7	B2 (BCD INPUTS)
NO CONNECTION	8	B4 (BCD INPUTS)
D1 LSD	9	B8 MSB (BCD INPUTS)
DIGIT DRIVE INPUTS D2	10	B.P. INPUT/OUTPUT
DIGIT DRIVE INPUTS D3	11	B.P. INPUT (DISP COM)
DIGIT DRIVE INPUTS D4	12	UNDERSCALE INPUT
D5 MSD	13	OVERSCALE INPUT
PWR COMMON	14	+5VDC PWR IN
NO CONNECTION	15	+5VDC PWR OUT

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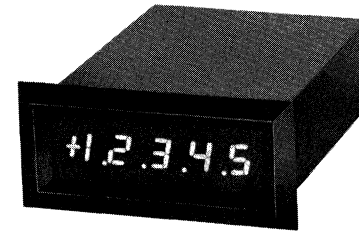
DM-4104
4½ Digit Parallel Input LED Slave Display

DATEL



FEATURES

- **Bright 0.3" high LED display**
- **Operates with 2½ to 4½ digit DPM's**
- **Latches BCD data in 4-bit nibbles**
- **Interfaces directly to a 4-, 8-, 12-, or 16-Bit data bus or to a full parallel 18-bit data bus**
- **Remote flashing alarm function**
- **Logic powered**

GENERAL DESCRIPTION

The DM-4104 slave display meter interfaces directly to a parallel 18-bit or to a multiplexed BCD (Binary Coded Decimal) master unit. This type of master unit includes DATEL's DPM's and a variety of microprocessor-based systems. The DM-4104 is packaged in a compact low-profile case.

Master digital panel meters accept a dc or slowly varying input voltage and display that input on front panel numerical indicators. In addition to dc voltages, DPM's can be adapted to measure practically any physical parameter which can be converted to electrical units. If the DPM provides parallel or multiplexed BCD outputs, the inputs of the DM-4104 Slaved Digital Panel Display can be electrically connected to these outputs to display the same information shown on the master DPM. There are several uses for slaved displays, among them being a remote workstation situation that requires the same up-to-the-instant information as the master unit. Other uses may be distributed networks, such as medical monitoring stations, industrial process control stations or linked data acquisition/data logging systems. The DM-4104 is not dependent exclusively on master DPM's. Any device that can convert physical parameters into bussable BCD outputs, such as a parallel microcomputer port, can control the DM-4104.

The DM-4104 interfaces directly to 4, 8, 12 or 16-bit data busses or full parallel 18-bit data busses. The BCD data inputs are latchable (enables data to be stored on electrical command) and bussable in 4-bit NIBBLES. A display blank may be used as a flashing alarm, blinking the display off and on using an external control. Right-of-digit selectable decimal points are included as well as a minus sign. The DM-4104 doesn't accept analog inputs.

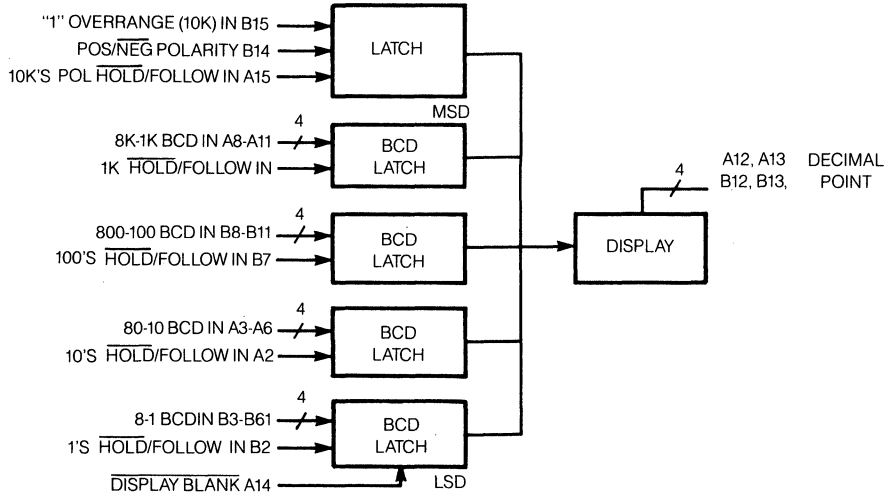
Power requirements of the DM-4104 Slaved Digital Panel Display is an external +5, ±0.25V dc, regulated at 450 mA typical (550 mA maximum). Power current varies rapidly — unregulated power supplies cannot be used. DATEL's UPM-5/1000 Single Output Power Supply is the recommended power supply for the DM-4104.

ORDERING INFORMATION
DM-4104

Model	Description
DM-4104-1	4½ Digit Slave Digital Panel Display (includes one connector)

ACCESSORIES

Part Number	Description
58-2073083	15-pin edge connector
UPM-5/1000	Power Supply



Simplified Block Diagram of a DM-4104

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS
(Typical at 25°C, 2V range unless noted)

Input configuration ..... Full parallel BCD, internally latchable in 4-bit nybbles.
Number of Digits ..... 4 decimal digits and most significant "1" digit (4½ digits)
Display Type ..... Red, light emitting diode (LED), self-illuminated
Display Height ..... 0.3 inches (7,6mm)
Decimal Points ..... Right-of-digit selectable decimal points are selected by rear connector pins.
Power Requirement .... External +5V, ±0.25V dc regulated required at 450 mA typical, 550 mA maximum. Logic spikes must not exceed 50 mV. Power current varies rapidly so that unregulated supplies cannot be used.
Connector ..... Dual 15-pin, 0.100" centers, DATEL #58-2073083 (one included with meter)

Low-Profile Case Dimensions ..... 2.53"W x 3.34"D x 0.94"H (64,3 x 82,5 x 23,8mm)
Cutout Dimensions ..... 2.562"W x 0.97"H (minimum) (65,1 x 24,6mm)
Mounting Method ..... See end of this section.
Mounting Position ..... See end of this section.
Weight ..... 3 ounces (15,9g)
Operating Temperature Range ..... (0°C to +50°C 32°F to 122°F)
Storage Temperature Range ..... (-25°C to +85°C -13°F to 185°F)
Altitude ..... 0 to 15,000 feet (4900m)
Relative Humidity ..... 10% to 90%, non-condensing

INPUT/OUTPUT CONNECTIONS DM-4104

BOTTOM A		TOP B
POWER/LOGIC COMMON	1	+5V DC POWER IN
10'S $\overline{\text{HOLD}}$ / FOLLOW IN	2	1'S $\overline{\text{HOLD}}$/FOLLOW IN
80 BCD IN	3	8 BCD IN
40 BCD IN	4	4 BCD IN
20 BCD IN	5	2 BCD IN
10 BCD IN	6	1 BCD IN
1K'S $\overline{\text{HOLD}}$/FOLLOW IN	7	100'S $\overline{\text{HOLD}}$/FOLLOW IN
8K BCD IN	8	800 BCD IN
4K BCD IN	9	400 BCD IN
2K BCD IN	10	200 BCD IN
1K BCD IN	11	100 BCD IN
DEC.PT.19.999 IN	12	DEC.PT.1999.9 IN
DEC.PT.1.9999 IN	13	DEC.PT.199.99 IN
$\overline{\text{DISPLAY BLANK}}$ IN	14	POS/$\overline{\text{NEG}}$ POL.IN
10K/POL. $\overline{\text{HOLD}}$/FOLLOW IN	15	"1" OVERRANGE (10K) IN

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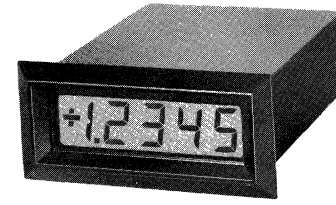
DM-4105
Micro-powered LCD Panel Meter with Data Outputs

FEATURES

- **Ultra-low power consumption**
- **.5" high 4½ digits LCD readout**
- **Draws only 3 mA from a 5V dc power source**
- **Balanced differential inputs with 5 pA bias currents**
- **Autozeroing with ratiometric reference for drift correction**
- **Right-most digit may be °C or °F descriptor for 3½ digit thermometer applications**
- **BCD outputs available to drive DM-4106 remote slave displays**
- **Standard ±1.999V dc input range; user-installed options set other voltage or current ranges.**



GENERAL DESCRIPTION

The DM-4105 is a 4½ digit, LCD-type DPM that uses very little power and produces outputs usable by other devices. The 0.5" high numeric display is visible under ambient room light from many feet away. Digit-serial BCD outputs are available to pass the digitized input signal on to microcomputers, data loggers, or printers.

The DM-4105 provides excellent electrical performance in a compact panel-mounting package. Analog inputs have a very high input impedances (1000 Megohm typical) with very low bias currents of 5 pA (typical). Common Mode Rejection Ratio (CMRR) is 86 dB. The meter is autozeroed on each conversion cycle to minimize drift of zero. A Reference In-Out loop can be used to correct drift in externally excited ratiometric circuits.

A variety of designed-in features makes it easy to use the DM-4105 in many applications. Blank circuit pads will accept user-supplied current shunts, voltage dividers, and ohmmeter components. Overrange and Underrange outputs can be used to trigger external autoranging circuitry (the DM-4105 display has Overrange and Underrange descriptors which may be set by the user). In 3½ digit thermometer applications, a degree sign can be enabled on the display, while the right-most digit (LSD) can be solder-gap programmed as "C" for Celsius readings or "F" for Fahrenheit readings.

The DM-4105 is powered from +5V dc at 3 mA typical (5 mA maximum.). It may be powered using 4 "AA" alkaline cells. A -5V output (at up to 15 mA output) is provided to power external circuits. The meter's low-profile polycarbonate case is 2.53"W x 3.25"D x 0.94"H (64,3 x 82,5 x 23,8mm).

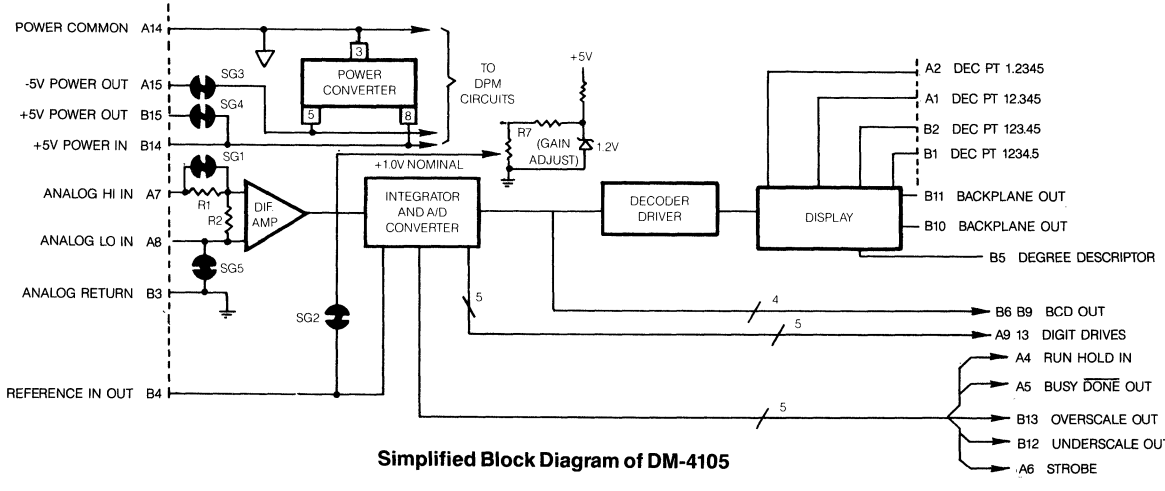
ORDERING INFORMATION

DM-4105 - 1

Model	Description
DM-4105-1	4 1/2-digit micro-powered DPM with data output (one connector included)

ACCESSORIES

Part Number	Description
58-2073083	15-pin edge connector
UPA-5/500	115V AC to 5V dc power adaptor
DM-4106	Low-profile slave display



Simplified Block Diagram of DM-4105

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.
Input Impedance ..... 100 Megohms (minimum) 1000 Megohms (typical)
Input Bias Current ..... 5 pA (typical) 50 pA (maximum)
Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V intermittent (maximum)
External Reference Range ..... ±100 mV to ±2V referred to -Vs
Common-Mode Rejection ..... 86 dB (typical), from dc to 60 Hz, with 1 Kilohm unbalanced
Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below +5V dc supply and 1.0V dc above -5V dc supply.
Resolution ..... 1 mV
Display Accuracy ..... Adjustable to ±0.2% of reading, ±2 counts
Temperature Drift of Zero ..... Autozeroed ±1 count over 0°C to +50°C temperature range
Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)
Sampling Rate ..... 3 conversions per second

DISPLAY

Number of Digits ..... 4 decimal digits and most significant "1" digit (4½ digits)
Decimal Points ..... Selectable using decimal point select signal lines.
Display Type ..... Liquid Crystal Display (LCD)
Display Height ..... 0.5 inches (12,7mm)
Overscale ..... An indicator flashes when inputs exceed the fullscale range.
Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity display.

POWER CONSUMPTION

The DPM requires +5 to +6V dc regulated at 3mA typical and 5mA maximum. Logic spikes must not exceed 50 mV. Any current taken from the -5V dc output must be added to the above specifications to yield the total meter power consumption. These figures exclude use of the +5V dc output.

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

Degree Symbol(°) In (Pin B5)
The temperature degree symbol may be displayed between the 1's and 10's digit by tying pin B5 to B11. To blank the degree symbol, tie B5 to B10. The 1's digit may be dedicated an F (Fahrenheit) or C (Celsius) unit abbreviation by modifying internal solder gaps. This modification provides a 3½ digit (1.9.9.9.°C) instrument.

-5V dc Power Out
Up to 15mA of unregulated -5V dc power may be taken directly from the meter to power external user-supplied circuits such as signal conditioners.

+5V dc Power Out
A separate pin on the I/O connector lets the user take +5V dc indirectly from the input power source. The amount of current taken is limited only by the power source.

PHYSICAL

External Dimensions
2.53"W x 3.34"D x 0.95"H (64,3 x 85 x 23,8mm)

Panel Cutout Dimensions
2.562"W x 0.97"H (65,1 x 24,6mm)

Mounting Method
Refer to end of this section.

Weight
Approximately 5 ounces (142g)

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0°C to 50°C)

Storage Temperature Range
32°F to 131°F (0°C to 55°C)

Relative Humidity
20% to 80% non-condensing

INPUT/OUTPUT CONNECTIONS DM-4105

BOTTOM A		TOP B	
DEC PT 19.999	1	DEC PT 1999.9	
DEC PT 1.9999	2	DEC PT 199.99	
POLARITY OUT	3	ANALOG GND	
RUN/$\overline{\text{HOLD}}$ IN	4	REF IN/OUT	
BUSY/$\overline{\text{DONE}}$ OUT	5	DEGREE SIGN IN	
$\overline{\text{STROBE}}$ OUT	6	B1 LSB	BCD OUT
ANALOG HI IN(+)	7	B2	
ANALOG LO IN (-)	8	B4	
D1 LSD	9	B8 MSB	
DIGIT DRIVE OUT D2	10	B.P. OUT	
D3	11	$\overline{\text{B.P.}}$ OUT (DISP COM)	
D4	12	UNDERSCALE OUT	
D5 MSD	13	OVERSCALE OUT	
PWR COMMON	14	+5VDC PWR IN	
-5VDC PWR OUT	15	+5VDC PWR OUT	

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DM-4200
4½ Digit LED Panel Meter with Data Outputs

DATEL

FEATURES

- **BCD outputs to drive DM-4102 remote slave displays**
- **±5V dc outputs for user's circuits**
- **Balanced differential inputs with 5 pA bias currents**
- **Internal ratiometric reference for drift correction**
- **High-brightness .3" high LED display**
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**

GENERAL DESCRIPTION

The DM-4200 is a 4½ digit DPM using high-brightness LED's and housed in DATEL's low-profile enclosure. Besides offering DATEL's standard input features, this device provides mutliplexed BCD outputs. These outputs can drive a remote display, such as the DM-4102, or can be used by an external microprocessor.

A dual slope A/D converter changes the signal inputs to a BCD digital code. Decoder drivers cause the input voltage to be displayed on .3" high LED numerals. The BCD-encoded numerals (digit serial) are also output to a rear-panel connector where they may be used to drive a slave display, or become A/D inputs to a printer or microcomputer.

The DM-4200 is housed in a compact, low profile polycarbonate case only .94" high. The DM-4200 can be used in process control panels, OEM products, and medical instrumentation to provide a clear, unambiguous display of dc voltages.

CMOS input circuitry gives the DM-4200 very high input impedance (1000 MΩ typical, 100 MΩ minimum), and a very low input bias current (5 pA typical, 50 pA maximum). The meter's input amplifier is autozeroed to minimize zero drift. The reference voltage is brought out on a rear panel pin (Reference Out), where it can correct drift in external ratiometric bridge circuits.

BCD outputs, multiplexed by digit, are available. The outputs are 1 TTL load, and can be used to drive a remote display.

Overscale and Underscale outputs can be used with external circuits to autorange the meter. A Run/Hold output can be tied low to stop the meter's A/D conversions, and to continuously display the last reading. A Busy/Done output goes low to indicate the end of an A/D conversion.

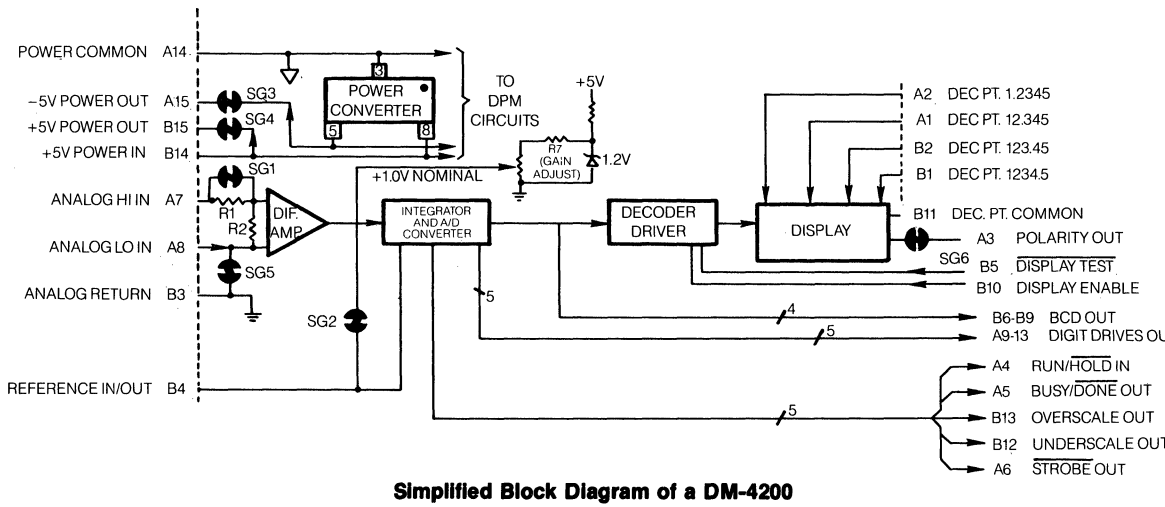
A built-in dc-to-dc converter provides -5V Out (at 15 mA maximum) to power user circuits. Power input is +5V dc (±.25V) regulated at 200 mA typical and 250 mA maximum.

ORDERING INFORMATION
DM-4200 - 1

Model	Description
DM-4200-1	4 1/2-Digit DPM with BCD outputs (includes connector)

ACCESSORIES

Part Number	Description
DM-4102	Mux'd BCD Slave Display
58-2073083	Dual 15-pin, 0.1" centers, P.C. edgeboard connector
UPA-5/500	115V AC to 5V dc power adaptor



Simplified Block Diagram of a DM-4200

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FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input Range ..... Refer to "FEATURES" Ranges field-modifiable.
Input Impedance ..... 100 Megohms (minimum)
Input Bias Current ..... 5 pA (typical) 50 pA (maximum)
Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V intermittent (maximum)
External Reference Range ..... ±100 mV to ±2V referred to -Vs
Common-Mode Rejection ..... 80 dB (typical), from dc to 60 Hz, with a 1 Kilohm unbalanced input
Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.
Resolution ..... 1 mV
Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count
Temperature Drift of Zero ..... Autozeroed ± count over a 0° to +50°C temperature range
Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical) ±100 ppm of reading/°C (maximum)
Sampling Time ..... 83.3 mS (nominal)
Sampling Rate ..... 3 conversions per second.

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)
Decimal Points ..... Selectable using decimal point select signal lines.
Display Type ..... LED (red, high efficiency)
Display Height ..... 0.3 inches high (7,6 mm)
Overscale ..... The display indicates inputs exceeding the full-scale range.
Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

POWER CONSUMPTION

The DPM requires +5 to +6V dc regulated at 3mA typical and 5mA maximum. Logic spikes must not exceed 50 mV. Any current taken from the -5V dc output must be added to the above specifications to yield the total meter power consumption. These figures exclude use of the +5V dc output.

PHYSICAL

External Dimensions
2.53"W x 3.34"D x 0.95"H (64,3 x 85 x 23,8mm)

Panel Cutout Dimensions
2.562"W x 0.97"H (65,1 x 24,6mm)

Mounting Method
Refer to end of this section.

Weight
Approximately 5 ounces(142g)

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
32°F to 122°F (0°C to 50°C)

Storage Temperature Range
32°F to +131°F (0°C to 55°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features.

-5V dc Power Out
Up to 15mA of unregulated -5V dc power may be taken directly from the meter to power external user-supplied circuits such as signal conditioners.

+5V dc Power Out
A separate pin on the I/O connector lets the user take +5V dc indirectly from the input power source. The amount of current taken is limited only by the power source.

Data Outputs
4-wire Binary Coded Decimal (BCD 1-2-4-8) per digit, multiplexed. Polarity display may be disabled. This would be used for unsigned reverse sensing (implied positive) applications with negative inputs.

INPUT/OUTPUT CONNECTIONS DM-4200

BOTTOM A		TOP B		
DEC PT 19.999	1	DEC PT 1999.9		
DEC PT 1.9999	2	DEC PT 199.99		
POLARITY OUT	3	ANALOG GND		
RUN/$\overline{\text{HOLD}}$ IN	4	REF IN/OUT		
BUSY/$\overline{\text{DONE}}$ OUT	5	$\overline{\text{DISPLAY TEST}}$		
$\overline{\text{STROBE}}$ OUT	6	B1 LSB		
ANALOG HI IN(+)	7	B2	BCD	
ANALOG LO IN(−)	8	B4	OUT	
D1 LSB	9	B8 MSB		
DIGIT D2	10	DISPLAY ENABLE		
DRIVE D3	11	DEC PT COM		
OUT D4	12	UNDERSCALE OUT		
D5 MSD	13	OVERSCALE OUT		
PWR COMMON	14	+5VDC PWR IN		
-5VDC PWR OUT	15	+5VDC PWR OUT		

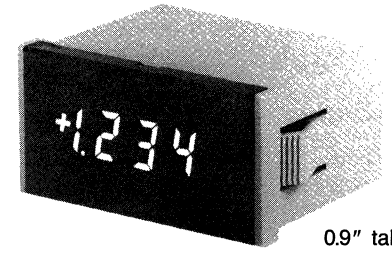
10

DM-500
Low-Cost, 3½ Digit, LED Mini Panel Meter

DATEL

FEATURES

- **Ultra-small size (0.89"H x 1.80"W x 1.89"D)**
- **DIN case and panel cutout**
- **3½ Digit, bright LED (0.3" character) display**
- **+5V dc-powered**
- **Low power consumption, 60 mA typical**
- **Single-ended and differential inputs**
- **Dual-slope A/D conversion**
- **Standard 1.999 Vdc input range; easily modified with external circuits.**
- **200 Hour burn-in and 1 year warranty**
- **Low cost**



0.9" tall

Photo Depicts Actual Size

Visibility, compact DIN size, and power efficiency combine to make this ultra-small panel meter ideal for applications such as portable instruments where low power consumption is critical.

GENERAL DESCRIPTION

The DM-500 is a low cost, ultra-small 3½ digit, 5V dc-powered digital panel meter (DPM). This panel meter uses a seven-segment light emitting diode (LED) display with 0.3" (8.0mm) tall characters. These high-efficiency, brilliant red LED characters provide high visibility for distant and angular viewing even under bright ambient light conditions. This DPM is contained in a lightweight, compact, easily-mounted DIN case suited for portable instruments while also allowing for higher packing density on test panel faces.

The DM-500 operates in either single-ended or differential modes. DATEL ships each unit ready for single-ended operation, with differential operation easily user-selectable. In either mode, the DM-500's provide high noise immunity. In the differential mode, the DM-500 accurately measures very small signals in the presence of much larger common-mode voltages. The high input impedance (typically 1000 Mohms) will not load down sensitive input circuits. The DM-500 panel meters employ conventional dual-slope A/D conversion techniques, with autozeroing further enhancing this versatile meter.

Standard units are configured for +/-1.999 Vdc input. Other voltage ranges (up to +/-1.999 Vdc) and current ranges (up to 199.9 mA) are easily obtained by using simple external circuits.

Overrange measurement conditions will blank the displays. As shown in Figure 1, the DM-500 accepts a hold signal from the user, inhibiting continuous sampling. When powered up, the DM-500 displays the last data sampled, acting as a temporary signal sample storage and display device. Other display functions include autopolarity, selectable decimal point, and display blanking.

Mounting the DM-500 mini panel meter is extremely easy. The housing it is contained in incorporates locking mechanisms as part of its construction. Once the proper-sized hole has been created, simply sliding the DM-500 into the hole engages the locking mechanisms.

The DM-500 will properly flush-mount onto panels up to ⅛" in thickness.

The DM-500 is a compact, high-quality panel meter fully tested for 200 hours before leaving the factory and fully warranted for one year.

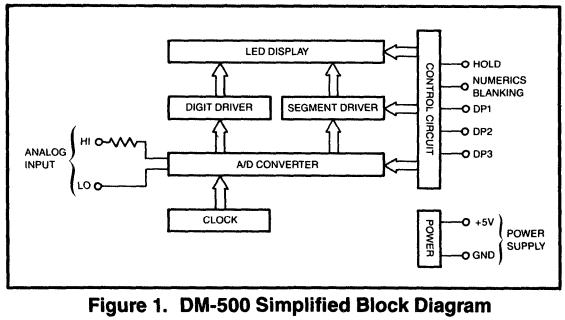


Figure 1. DM-500 Simplified Block Diagram

Pin Connections

1	Input LO
2	Input HI
3	Hold
4	Blanking Numericals
5	Decimal Point 1
6	Decimal Point 2
7	Decimal Point 3
8	+5V dc Power
9	GND

Note: Input LO (Pin 1) and Power GND (Pin 9) are internally connected.

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FUNCTIONAL SPECIFICATIONS

(Typical at +25 degrees Celsius, unless otherwise noted)

Common Specifications:

Input Range ..... ±1.999V; user-configurable for other voltage and current ranges
Input Overvoltage ..... ±100V max
Accuracy ..... ±0.1% of reading +1 digit
A/D Conversion ..... Dual-slope with autozeroing circuit
Sampling Rate ..... 2.5 samples/second
Input Configuration .... Single-ended. Differential input can be applied after cutting etch.
Gain Temperature Coefficiency ... Less than +100 ppm/°C
Zero Temperature Coefficiency .. Autozeroed ±1 count over 0 to +50°C
Input Impedance..... 1000 MΩ
Bias Current ..... 20 pA typical
Common Mode Rejection Ratio ..... 50dB typical
Common Mode Voltage Range ... ±0.5V, ±1V dc maximum
Noise Rejection ..... NMR 40dB typical at 50/60 Hz
External Controls ..... Hold and numerical blanking capabilities

Display ..... Red, 7-segment LED, 0.3 inch (8.0 mm) tall characters
Displayed Characters ..... ±1999
Decimal point location .... Switched under external control
Polarity Signs ..... + and − signs automatically displayed
Polarity Disable (blanking) ..... Available by cutting a part of the etch
Overrange . All digits blank (+ or − sign stays on depending on overrange polarity)

Power Supply ..... +5V dc, ±5%, 60 mA typical, 80 mA maximum. +7V dc supply maximum

Cutout Dimensions .... 0.89″(22,7mm)H x 1.80″(45,7mm)W x 1.89″(48mm)D
Weight ..... 1.22 ounces (35 grams)
Operating Temperature Range ..... 0°C to +50°C
Operating Humidity ..... Less than 85%
Storage Temperature Range ..... −20°C to +70°C

OPERATING INSTRUCTIONS

Power Supply

Use a well regulated power source. When using a battery, tie a 100μF to 1000μF capacitor between the power terminals. Maximum supply voltage is +7V dc.

Inputs

Single-ended inputs—Apply the input voltage (or current) between pins 1 (Input LO) and 2 (Input HI). Pin 1 is internally tied to Pin 9 (GND). In electrically noisy environments, use a shielded cable for inputs, tying the shield to Pin 1.

Differential inputs—Cut the etch shown in Figure 2a, applying the input signal as shown in Figure 2b.

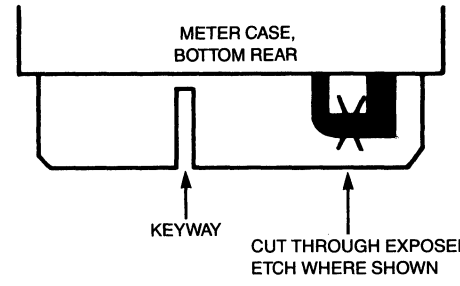


Figure 2a. Location of Etch

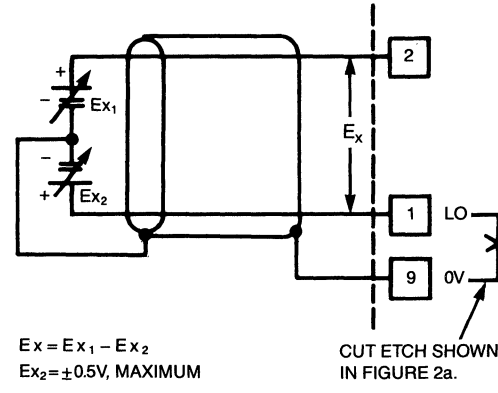


Figure 2b. Typical Differential Input Configuration

Decimal Point Location

XXX.X Connect Pins 5 and 8
XX.XX Connect Pins 6 and 8
X.XXX Connect Pins 7 and 8

Hold Function

A display remains constantly on when Pin 3 (Hold) is connected to Pin 9 (GND).

Numerical Blanking

To blank the numbers on the display, tie Pin 4 (Blanking Numericals) to Pin 9.

Polarity Sign Blanking

Remove the front panel and cut the + or − jumper wires to disable displaying the polarity of the input signal (see Figure 3).

10

CALIBRATION

Calibration is suggested once every six months. See Figure 3.

Procedure:

1. Allow the DM-500 to warm up for at least five minutes.
2. Ensure that the meter's environment is +23°C, humidity at less than 84%.
3. Apply a voltage or current to the input close to positive full scale.
4. Adjust the full scale adjustment potentiometer for a reading identical to that of the voltage source.

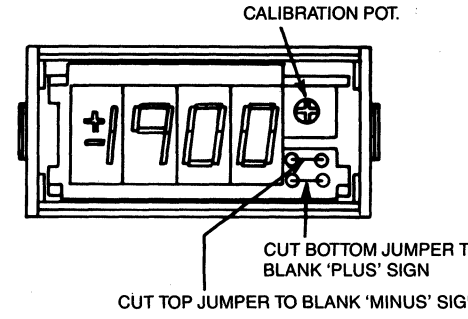
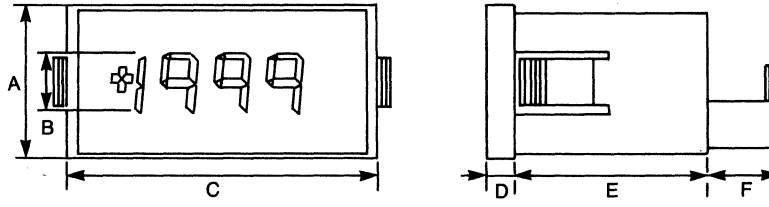


Figure 3. Location of Polarity and Jumpers and Calibration Potentiometer

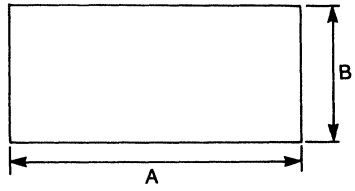
MECHANICAL DIMENSIONS INCHES (mm)



A: 0.94 (24)
B: 0.31 (8.0)
C: 1.89 (48)

D: 0.20 (5)
E: 1.22 (31)
F: 0.47 (12)

PANEL CUTOUT DIMENSIONS



INCHES	mm
A: 1.80 (+0.01, −0)	45.7 (+0.3, −0)
B: 0.89 (+0.01, −0)	22.7 (+0.3, −0)

ORDERING INFORMATION

DM-500 - 1

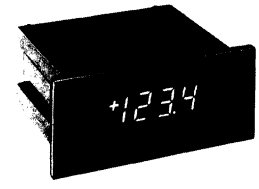
Connector included with meter.

*Standard configuration is DM-500-1; other configurations available.

DM-9000 SERIES DIN/NEMA Size Panel Meters

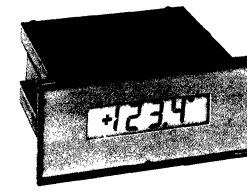
FEATURES

- **Fit into industry standard DIN/NEMA size panel cutouts**
- **Meets NEMA vibration standards**
- **3½ or 4½ digit display**
- **Bright 0.56" light emitting diode (LED) and 0.5" liquid crystal display (LCD)**
- **Powered by AC or dc sources**
- **Overvoltage protection ±250V dc**
- **High resolution**
  0.001V (3½ digit DPM's)
  0.0001V (4½ digit DPM's)
- **Balanced high-impedance differential inputs**
- **Autozeroing capability**
- **80 dB CMRR**
- **Standard ±1.9999V dc input range; user-installed options set other voltage or current ranges.**



DM-9100
DM-9115

DM-9200
DM-9215



DM-9150
DM-9165

DM-9250
DM-9265

GENERAL DESCRIPTION

The DM-9000 Series DPM's offer the user 3½ or 4½ digits of display, using either AC or dc power sources. This panel meter line offers two types of displays. The high-efficiency red LED's provide excellent readability from up to 23 feet (7 meters) away, even under bright ambient light. The high contrast LCD's have viewing angles of up to 75 degrees from normal and are ideally suited for low power applications.

These DPM's may be operated in Differential, Single-Ended or Ratiometric modes. In differential mode, the balanced inputs of the DM-9000 Series provide high noise immunity and accurately measure very small signals in the presence of much larger common-mode voltages. The high impedance (100 megohms) will not load down sensitive input circuits. The single-ended mode in the DM-9000 Series DPM's is solder gap selectable and is easy to use for simple applications.

For ratiometric measurements, the DPM's reference the input voltages to the user-supplied voltage using the REF IN/OUT pin (Pin 4). The ratiometric mode of operation corrects for input errors created by drift in transducer excitation sources, i.e., bridge type applications.

The 4½ digit panel meters (DM-92XX models) have OVERRANGE and UNDERRANGE outputs, usable in auto-ranging circuits and a BUSY/DONE output which goes low at the end of each analog-to-digital conversion cycle.

All models accept a HOLD (or RUN/HOLD) signal from the user, inhibiting continuous sampling. The units display the last data sampled, acting as temporary single sample storage and display devices.

ORDERING INFORMATION

Model
DM-9000 Series **DM-9 _ _ _ 1**
To Order, Specify:
Features
3 1/2 Digits 1
4 1/2 Digits 2

LED, dc Power 00
LED, AC Power 15
LCD, dc Power 50
LCD, AC Power 65

ACCESSORIES

Part Number	Description
39-21025	Screw Terminal Block Connector
58-2073078	Dual 15-pin edge connector (one included with each meter)
UPA-5/500	115V AC to 5V dc Power adapter

10

Functionally, a DPM is made up of four parts; the integrator and A/D converter, decoder driver, display, and power supply (see Figure 1).

All AC models accept 100, 117, 220 or 240 VAC sources. Refer to Table 1 for power supply pin connections

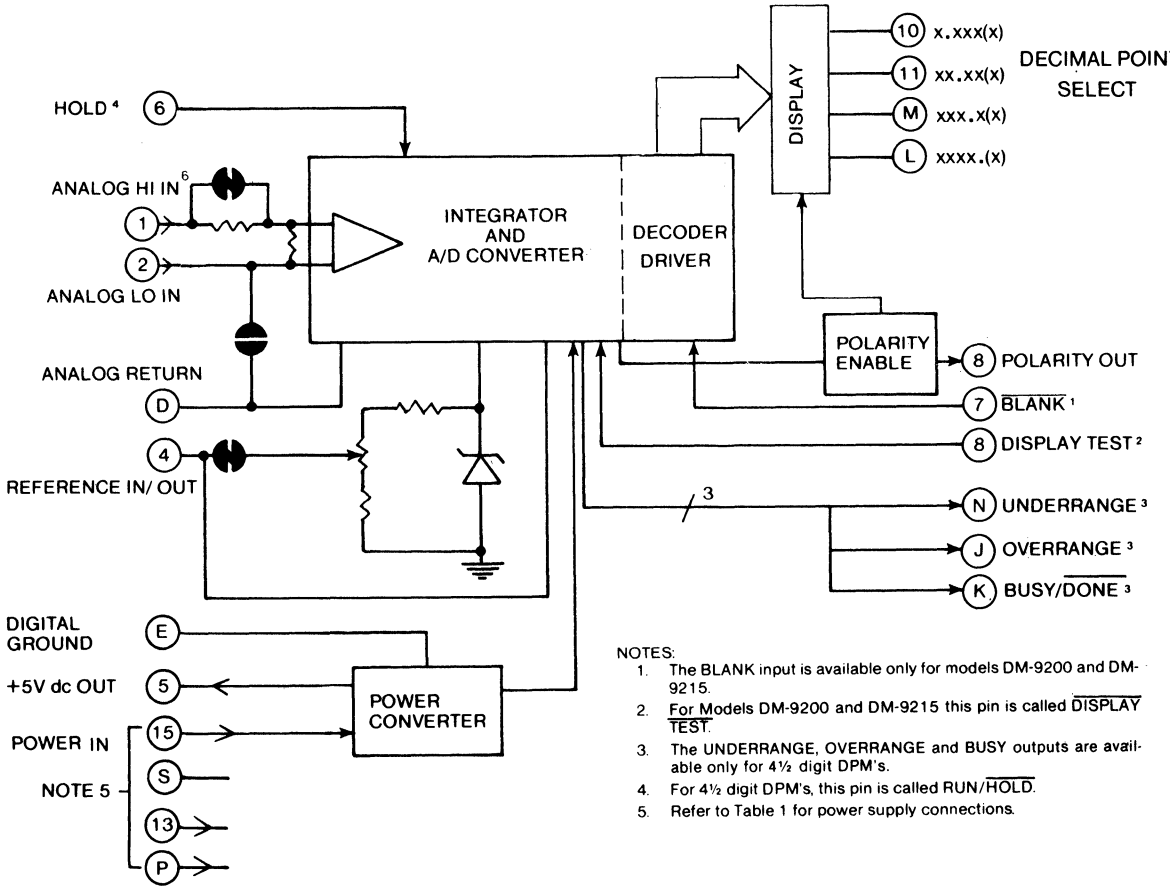


Figure 1. Simplified Block Diagram

Table 1. Power Supply Connections

PIN NUMBER / INPUT VOLTAGE	15	13	S	P
5V dc			1	
115 VAC				
220 VAC				
240 VAC				
100 VAC				

NOTE

The DM-9000 Series DPM's uses pins P, 13, 15, and S for power connections. Use of these pins is different for dc and AC models. AC models use different combinations of these pins for different power inputs. It is therefore important to check the information presented here for correct power applications.

Note 1: Pin S is POWER COMMON for dc models.

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FUNCTIONAL SPECIFICATIONS
(Typical @ 25°C, 2V range unless noted)

ANALOG INPUT

Full Scale Input ..... Refer to "FEATURES"

Range ..... Ranges field-modifiable
Input Impedence ..... 100 Megohms (minimum)
Input Bias Current ..... 5 pA (typical)
50 pA (maximum)
Input Overvoltage
ANALOG LO IN }
ANALOG HI IN } ..... ±100V dc continuous, referenced to POWER COMMON. ±250V dc (5 seconds maximum) referenced to POWER COMMON.
External Ref. Range .... +100 mV to +2V dc referenced to ANALOG RETURN.
Common-Mode Rejection ..... 80 dB (typical from dc to 60 Hz, with a 1 Kilohm unbalanced input
Common-Mode Voltage Range ..... Both the inputs must remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply
Resolution ..... 1 mV, 3½ digit DPM's
100 μV, 4½ digit DPM's
Accuracy ..... Adjustable to ±0.02% of reading (maximum), ±2 counts
Temperature Drift of Zero ..... Autozeroed ±1 count over a 0 to +50°C temperature range
Temperature Drift of Gain ..... ±50 ppm of reading/°C (typical)
±100 ppm of reading/°C (maximum)
Warm-Up Time ..... 5 minutes (typical)

	3½ digit DPM's	4½ digit DPM's
Sampling Time (nominal)	83.3 ms	74 ms
Conversion Time (nominal)	333 ms	296 ms

DISPLAY SPECIFICATIONS

Number of Digits ..... 3½ and 4½ digits
Decimal Points ..... Selectable
Display Type ..... LED (Red, high efficiency)
LCD (Liquid crystal with high contrast ratio, high temperature fluid)
Display Height ..... LED 0.56" (14,22 mm)
LCD 0.5" (12,70 mm)
Auto Polarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign is for negative inputs. The user may blank the polarity using solder gap options.
Over Scale ..... The display indicates inputs exceeding the full-scale range. Refer to the table below.

Model Number	Overscale Display
DM-9100, DM-9115, DM-9150, DM-9165	Blanks the display leaving a "1" MSD and sign.
DM-9200, 9215	Blanks "1" MSD and displays all other digits as zeroes and flashes.
DM-9250, DM-9265	Blanks "1" MSD, displays all other digits as zeros and flashes error sign (▲in the top left corner).

POWER CONSIDERATIONS

Power Consumption with no external load

MODEL	Typical	Maximum
DM-9100	0.9 W	1.1W
DM-9115	2.6W	3.2W
DM-9150	0.02W	0.025W
DM-9165	0.9W	1.1W
DM-9200	0.9W	1.1W
DM-9215	2.6W	3.2W
DM-9250	0.02W	0.025W
DM-9265	0.9W	1.1W

Power output for AC models: +5V dc @ 100mA (maximum)
Power output for dc models: Limited by user's dc source

CALIBRATION

A screwdriver pot allows adjusting the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration period under normal operating conditions is 90 days.

PHYSICAL-ENVIRONMENTAL

External Dimensions
3.6"W x 3.57"D x 1.67"H (91,44 mm x 90,68 mm x 42,42 mm)

Panel Cutout Dimensions
NEMA Standard: 3.924" x 1.682" (99,67 mm x 42,72 mm) DIN Standard: 3.622" x 1.772" (92 mm x 45 mm)

Weight
AC models: 11 Ounces (311,8 grams) dc models: 6 Ounces (170,1 grams)

Altitude
0 to 15,000 feet (4900 m)

10

TEMPERATURE RANGES

Operating
0° to 50° Celsius

Storage
-25° to +85° Celsius

Relative Humidity
10% to 90%, non-condensing (for LED models) 0 to 90% (non-condensing) from -25° to +35°C derated linearly to 25% at +50°C (for LCD models)

PIN DETAILS

Figure 2 shows the pin connections for the different models in the DM-9000 Series.

INTERNAL GROUNDING CONNECTIONS:

The internal connections for ANALOG RETURN (Pin D), DIGITAL GROUND (Pin E) and POWER COMMON (Pin S) differ based on the DPM model. For 3½ digit DPM's DIGITAL GROUND and POWER COMMON are internally connected. For 4½ digit DPM's ANALOG RETURN, DIGITAL GROUND and POWER COMMON are internally connected. Depending on the application and input configuration, the user may have to make the grounding connections. POWER COMMON is internal for AC models and is not user accessible.

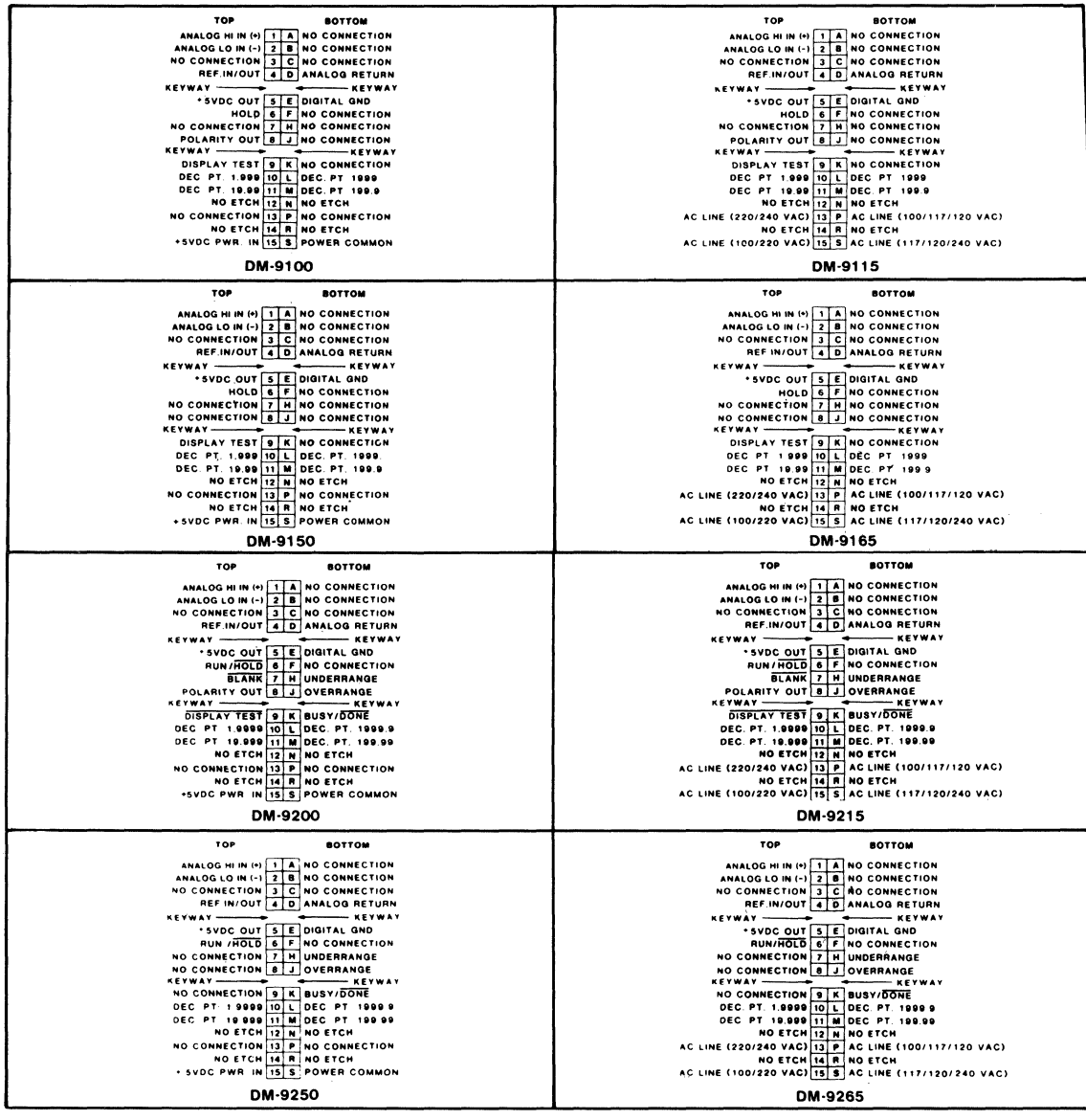

Figure 2. Pin Details of DM-9000 Series DPM's

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Table 2 lists the voltage and current levels on the DM-9000 Series DPM's input/output pins.

Table 2. Logic Levels for Input/Output Pins

Model Number	Pin Number	Pin	Parameter	Minimum	Typical	Maximum	Units
9100 9115	6	HOLD IN	V_{IL} V_{IH}	-- 3.5	-- --	1.5 --	Volts Volts
	8	POLARITY OUT	Positive Inputs Negative Inputs	2.5 --	-- --	-- 0.5	Volts Volts
9150 9165	6	HOLD IN	V_{IL} V_{IH}	-- 3.5	-- --	1.5 --	Volts Volts
9200 9215 9250 9265	6	RUN/$\overline{\text{HOLD}}$ IN	V_{IH} V_{IL} I_{IL} (@V = 0V) I_{IH} (@V = 5V)	2.8 -- -- --	2.2 1.6 0.02 0.1	-- 0.8 0.1 10	Volts Volts milli-amperes milli-amperes
	K 8 H J	BUSY/$\overline{\text{DONE}}$ POLARITY OUT OVERRANGE OUT UNDERRANGE OUT	V_{OL} (@I = 1.6mA) V_{OH} (@I = −1mA) V_{OH}(@I = −10μA)	-- 2.4 4.9	0.25 4.2 4.99	0.4 -- --	Volts Volts Volts
9200 9215	7	$\overline{\text{BLANK}}$ IN	V_{IL}	--	--	0.8	Volts

PIN#	SIGNAL	DESCRIPTION
1 2	ANALOG HI IN ANALOG LO IN	Differential input voltages connect to these inputs. A bias current path to POWER COMMON (if + 5V dc powered) or ANALOG RETURN from both these inputs must be externally provided. External circuits must restrict these inputs to be within the common-mode voltage range.
4	REF IN/OUT	The instrument is calibrated when a + 1.0V dc drop exists between this pin and ANALOG RETURN (Pin D). The DPM's are provided with a solder gap option to allow an external ratiometric reference. The external source must be biased against ANALOG RETURN (Pin D).

PIN#	SIGNAL	DESCRIPTION
5	+ 5V dc OUT	This pin delivers + 5V dc (@ 100mA maximum for AC models) for user circuits. The dc model output is limited to the user's dc source limit.
6	RUN/$\overline{\text{HOLD}}$ IN (low = $\overline{\text{HOLD}}$)	For models DM-9200, DM-9215, DM-9250, and DM-9265 a TTL high (or open) on this pin enables continuous sampling. A TTL low (or ground) will hold and display the last sample for temporary single sample storage. For models DM-9100, DM-9115, DM-9150, and DM-9165 a TTL low (or open) on this pin enables continuous sampling. A TTL high holds the display.

10

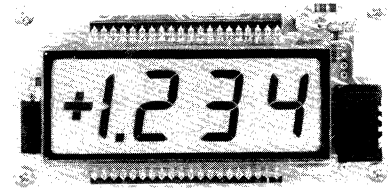
PIN#	SIGNAL	DESCRIPTION
7	$\overline{\text{BLANK IN}}$ (active low)	This pin's function is available only on models DM-9200 and DM-9215. A TTL low (or ground) on this pin blanks the display, excluding the selected decimal points and the polarity sign. Data remains valid even with the display blanked.
8	POLARITY OUT	This pin goes low when the DPM receives a negative input signal. It is valid even for a zero reading. A display of +0000 means the signal is positive but less than the least significant digit.
9	DISPLAY TEST IN	To test the display, apply + 5V dc to this pin for models DM-9100, DM-9115, DM-9150, and DM-9165 or ground this pin for models DM-9200 and DM-9215. The display will read 1.888(8). This pin is not available in models DM-9250 and DM-9265.
10	DECIMAL POINT SELECT (active low) x.xxx(x)	Connect the selected decimal point to Pin E, Digital Ground.
11	DECIMAL POINT SELECT (active low) xx.xx(x)	
M	DECIMAL POINT SELECT (active low) xxx.x(x)	
L	DECIMAL POINT SELECT (active low) xxxx.(x)	

PIN#	SIGNAL	DESCRIPTION
D	ANALOG RETURN IN	This pin may be used as a reference for some floating inputs. If not possible, inputs may be referenced to POWER COMMON (if + 5V dc powered). ANALOG RETURN is approximately − 2.8V below + Vs and can sink 30 mA to − Vs.
H	UNDERRANGE OUT (active high)	This pin goes high if the previous input displays + 1800 counts or less. The pin remains high until the beginning of signal integration in the next measurement cycle.
J	OVERRANGE OUT (active high)	This pin is high if the previous input signal exceeds the A/D converter range of + 19999 counts. The pin remains high until the beginning of reference integration in the next measurement cycle. UNDERRANGE and OVERRANGE are normally used as up/down ranging gain selection controls for an auto-ranging input selection.
K	BUSY/$\overline{\text{DONE}}$ OUT (low=$\overline{\text{DONE}}$).	This pin goes high during A/D conversions. The pin remains high until the conversion is complete or until the end of a measurement in the case of an OVERRANGE. The pin may be used to prevent the input voltage from changing during conversions.

DM-LX3
Single Board, 3½ Digit LCD Panel Meter

FEATURES

- **Compact, single board design**
- **3½ digit LCD display**
- **Balanced high-impedance differential inputs**
- **80dB CMRR**
- **Low power consumption**
- **Fits easily into most panel cutouts**
- **Autozeroing capability**
- ***Ratiometer reference for drift correction***
- **Standard ± 1.999V dc input range; user-installed options set other voltage or current ranges.**



GENERAL DESCRIPTION

The DM-LX3 is a compact, uncased, single board digital panel meter (DPM). The DPM displays a range of input voltages and currents on a 0.75" LCD display. The DM-LX3 operates on logic power (+5V dc) or 4 "AA" alkaline batteries.

Despite its small size and low cost, the DM-LX3 offers very high instrument performance. CMOS circuitry provides 1000 Megohm input impedance and 5 picoamp input bias current; the meter will not "load down" sensitive input signals. Analog inputs to the meter are balanced differential, and offer 80 dB Common Mode Rejection. Overvoltages to ±250V dc (175 VRMS) are handled without damage.

A significant feature is an externally-accessible Reference In-Out loop which sets the meter's gain. This permits the DM-LX3 to be used in ratiometric applications such as a digital ohmmeter. Here, an external reference voltage, derived from a bridge-type input circuit, causes the meter's gain to compensate for voltage drift in the bridge excitation source.

Other circuit features include autopolarity, a display hold circuit, and a selectable display test. Autozeroing holds the meter's zero drift to ±1 count maximum over the 0°C to 50°C operating range. Temperature drift of gain is typically within ±50 ppm of reading/°C. The meter's on-board dc-to-dc converter can also be used to supply -5V out at 20 mA maximum to power user-supplied signal conditioning components.

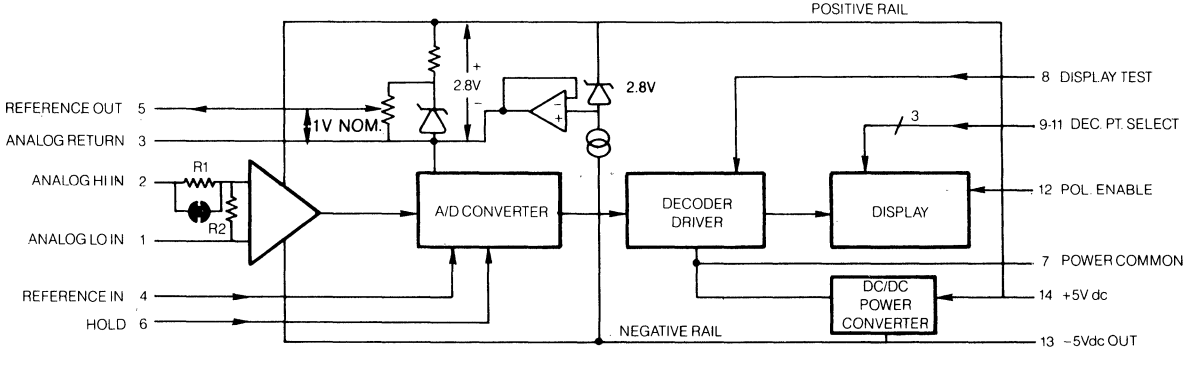
ORDERING INFORMATION

DM-LX3-1

Model	Description
DM-LX3-1	3 1/2 Digit single board DPM with Liquid Crystal Display (includes one P1 connector)

ACCESSORIES

Part Number	Description
39-2106705	P1 connector for J1 jack; 14-pin DIP connector and cover
UPA-5/500	115V AC in, +5V dc (@ 500 mA) out, power adaptor



Simplified Block Diagram of a DM-LX3

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical at 25° C, 2V range unless noted)

ANALOG INPUT

Full-Scale Input ..... Refer to "FEATURES"
Range Ranges field-modifiable.
Input Impedance ..... 100 Megohms (minimum)
1000 Megohms (typical)
Input Bias Current ..... 5 pA (typical) 50 pA (maximum)
Input Overvoltage ..... ±250V dc, 175V RMS continuous (maximum) ±300V intermittent (maximum)
External Reference ..... ±100 mV to ±2V
Range referred to -Vs
Common-Mode ..... 80 dB (typical),
Rejection from dc to 60 Hz, with a 1 Kilohm unbalanced input
Common-Mode ..... Both the inputs must
Voltage Range remain within 0.5V dc below the +5V dc supply and 1.0V dc above the -5V dc supply.
Resolution ..... 1 mV
Display Accuracy ..... Adjustable to ±0.1% of reading, ±1 count
Temperature Drift ..... Autozeroed ±1 count
of Zero over a 0° to +50°C temperature range
Temperature Drift ..... ±50 ppm of
of Gain reading/°C (typical) ±100 ppm of reading/°C (maximum)
Sampling Time ..... 83.3 mS (nominal)
Sampling Rate ..... 3 conversions per second.

DISPLAY

Number of Digits ..... 3 decimal digits and most significant "1" digit (3½ digits)
Decimal Points ..... Selectable using decimal point select signal lines.
Display Type ..... LCD
Display Height ..... 0.75" (19mm)
Overscale ..... The inputs exceeding the full-scale range display "+1" MSD with zeroes blanked.
Underscale ..... The inputs below the 1800 counts display "-1" MSD with zeroes blanked.
Autopolarity ..... A "+" sign is automatically displayed for positive inputs and a "-" sign for negative inputs. The user may blank the polarity using the POLARITY ENABLE line.

CALIBRATION

A multiturn screwdriver pot adjusts the full scale reading (gain). Zero is automatic (autozeroing). Suggested recalibration is 90 days.

PHYSICAL

External Dimensions
4.0"W x 2.0"H x 0.56"D (102 x 51 x 14 mm)

Panel Cutout Dimensions
2.88" x 1.13" (72 x 29 mm) (Requires a 0.125" (3,2 mm) diameter hole for gain adjust pot)

Weight
1.8 ounces (52g)

ENVIRONMENTAL

Altitude
0 to 15,000 feet (4900m)

Operating Temperature Range
+32°F to 122°F (0° to 50°C)

Storage Temperature Range
+32°F to +131°F (0°C to 55°C)

Relative Humidity
20% to 80% non-condensing

I/O SIGNAL FEATURES

Besides the common I/O Signals defined elsewhere, this device also has some important I/O features:

-5V dc OUT (Pin 13)
A voltage output may be used from the internal dc-to-dc converter to power user-supplied external circuitry.

POWER CONSUMPTION

+5V dc POWER IN
+5V dc (3.5 to 7.0V dc) at 3.5mA nominal. May be supplied from four "AA" alkaline batteries in series, or a regulated (+/-5%) power supply (DATEL UPA-5/500).

dc POWER OUT
-5V dc (-3.5V to -7.0V dc, depending on input) @ 20 mA maximum.
Any current taken at -5V dc out must be added to +5V power to yield total meter power.

DIGITAL PANEL METER CASE MOUNTING CONFIGURATIONS

DATEL DPM cases are designed to meet different industry-standard specifications. Table 6-1 shows the different case dimensions and the DPM models. A user may select a DPM depending on the front panel requirements: low profile, short depth, DIN, or NEMA dimensions. Some DPM models also meet NEMA vibration specifications. Figures 6-1 through 6-4 show different DPM case dimensions and panel installation methods.

Table 10-1: DPM Case Dimensions

Case Type	Dimensions W x D x H	DPM Model Number
Low-Profile	2.53" x 3.34" x 0.94" (64,3 x 84,8 x 23,8 mm)	DM-3100N DM-3100U1 DM-3100U2 DM-3100U3 DM-3102 DM-4100D DM-4101D DM-4101N DM-4102 DM-4104 DM-4105 DM-4106 DBM-20
Short-Depth	3.00" x 2.15" x 1.76" (76,2 x 54,6 x 44,7 mm)	DM-3100B DM-3100L DM-3100X DM-4101L DM-4103 PC-6
	1.89 x 1.4 x 0.94 (48 x 34,3 x 24)	DM-500
DIN/NEMA	3.6" x 3.57" x 1.67" (91,44 x 90,68 x 42,42 mm)	DM-9100 DM-9115 DM-9150 DM-9165 DM-9200 DM-9215 DM-9250 DM-9265
Uncased	4.0" x 2.0" x 0.56" (102 x 51 x 14 mm)	DM-LX-3
	3.5" x 2.0" x 0.5" (88,9 x 50,8 x 12,7 mm)	DM-31

Inches (MM)

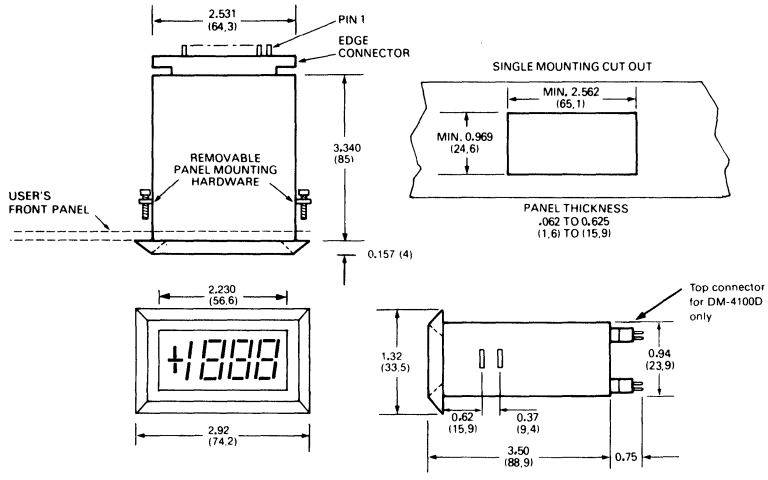


Figure 10-1a: Mechanical and Panel Cutout Dimensions for a Low-Profile DPM Case

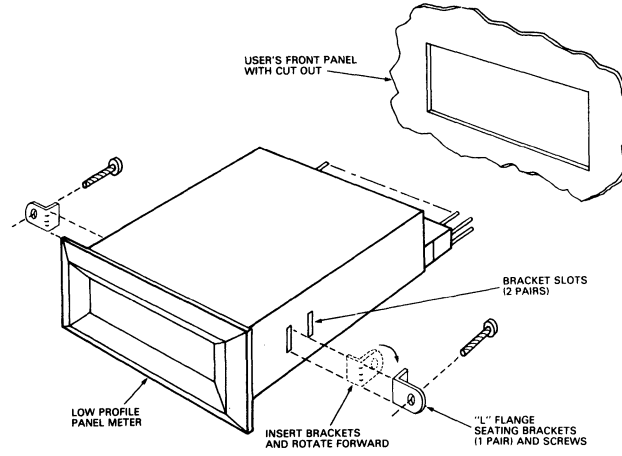


Figure 10-1b: Panel Installation of a Low-Profile DPM Case

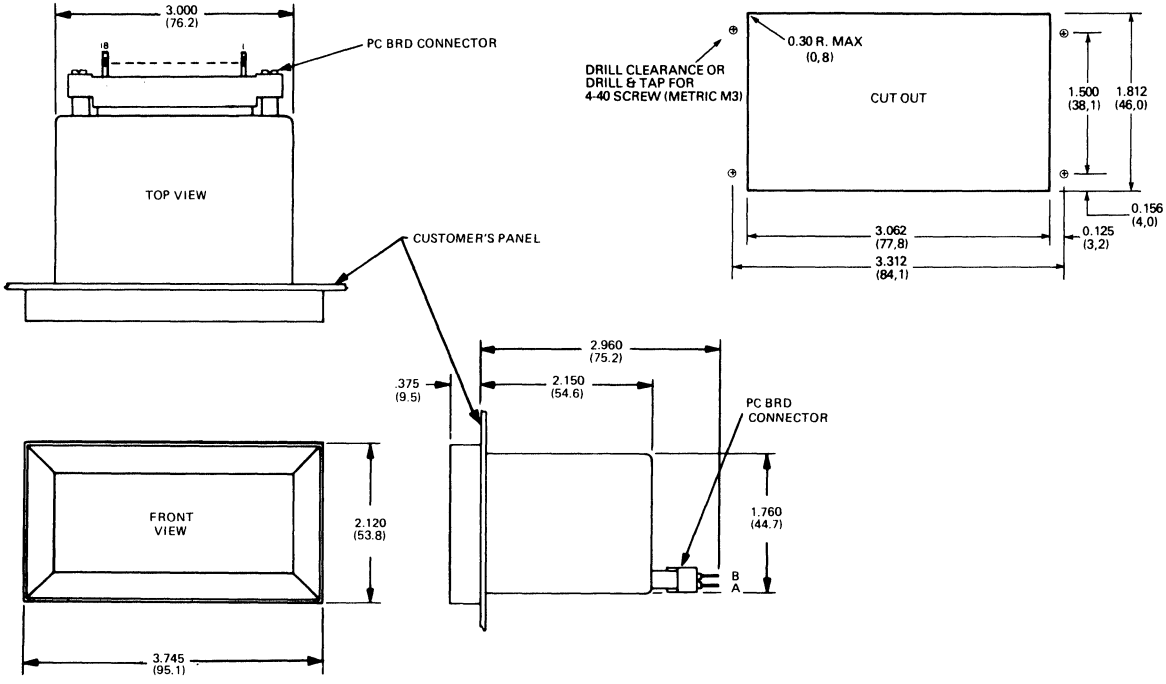


Figure 10-2a: Mechanical and Panel Cutout Dimensions of a Short-Depth DPM Case

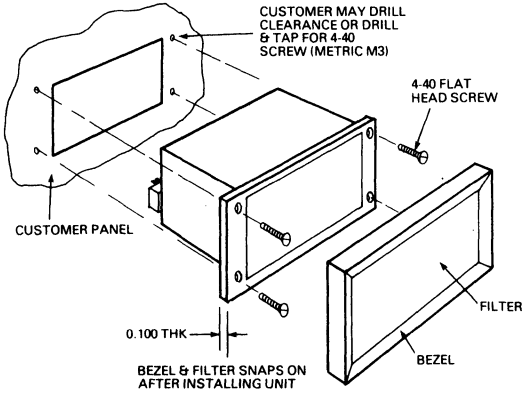
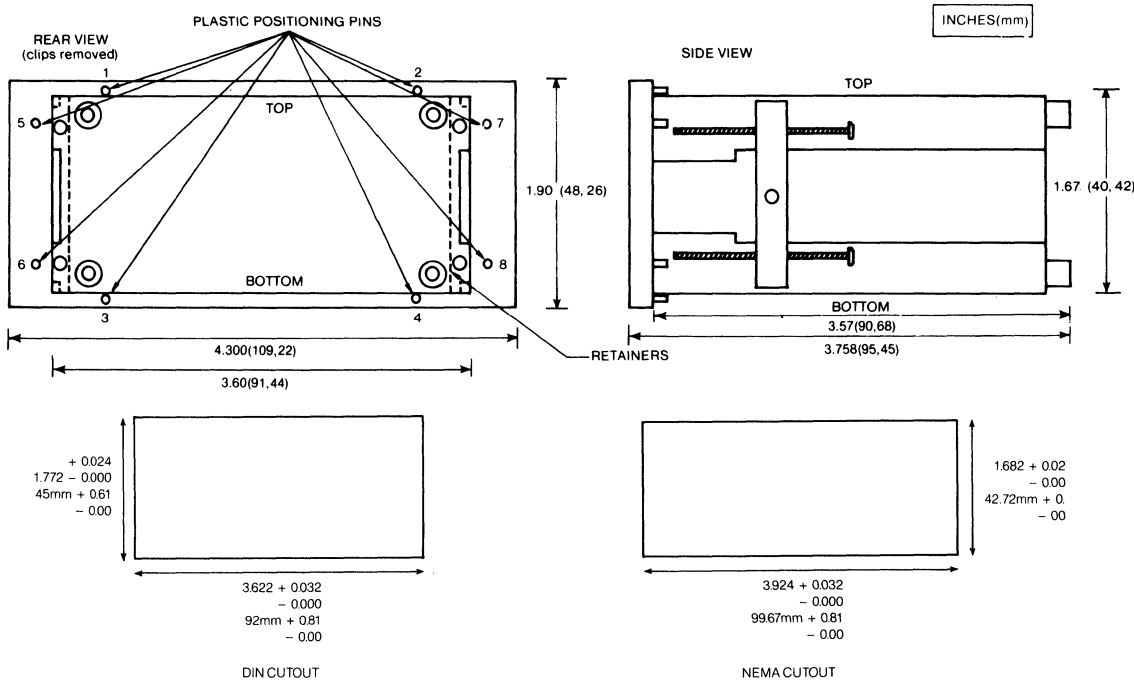


Figure 10-2b: Panel Installations of a Short-Depth DPM Case

10



Note: The DM-9000 Series DPM Case is designed to fit into industry standard DIN or NEMA size panel cutouts. Remove the plastic positioning pins 1, 2, 3 and 4 to fit the DPM into NEMA size panel cutout, or, pins 5, 6, 7, and 8 to fit the DPM into a Din size panel cutout.

Figure 10-3a: Mechanical and Panel Cutout Dimensions of a DIN/NEMA DPM Case

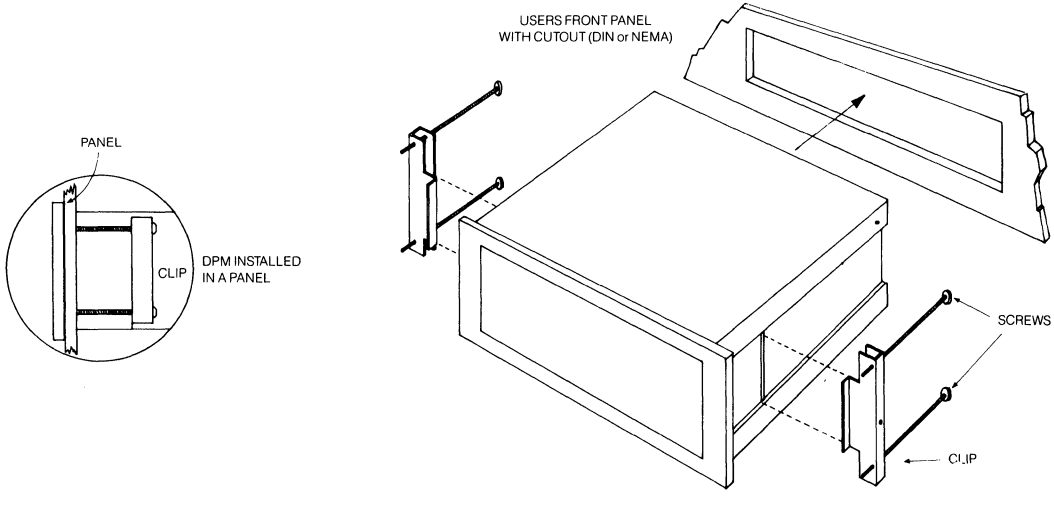
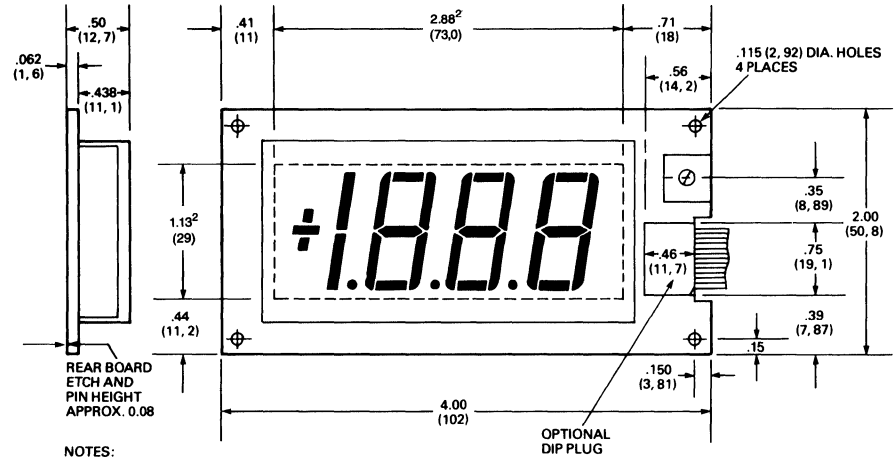
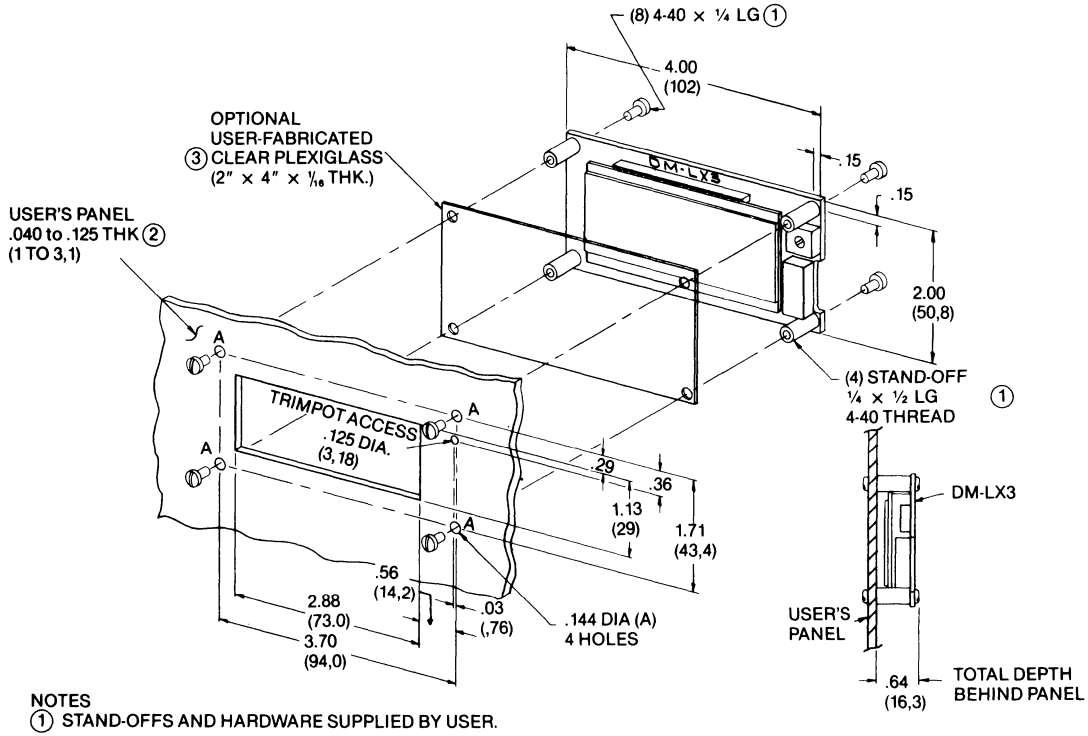


Figure 10-3b: Panel Installation of a DIN/NEMA DPM Case



NOTES:
1. USE ¼" x ½" LG STAND-OFFS (NOT SUPPLIED WITH METER) TO REAR MOUNT DM-LX3.
2. THESE ARE NOT OUTLINE DIMENSIONS FOR THE DISPLAY. THEY ARE PANEL CUTOUT DIMENSIONS USED WHEN REAR MOUNTING THE METER.

Figure 10-4a: DM-LX3 Mechanical Dimensions



NOTES
① STAND-OFFS AND HARDWARE SUPPLIED BY USER.
② PANEL THICKNESS OF ABOUT 1/8" MAY REQUIRE 4-40 x 5/16 LG. SCREWS FROM THE FRONT.
③ A CLEAR FILTER IS RECOMMENDED TO PROTECT THE DM-LX3 DISPLAY. IF USED, INCREASE LENGTH OF FRONT SCREWS BY 1/16"

Figure 10-4b: DM-LX3 Panel Mounting

10

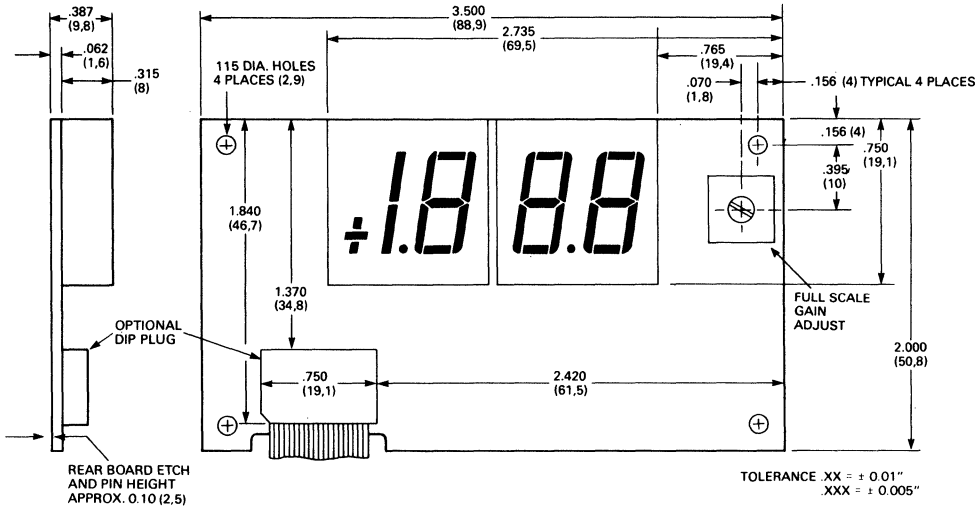


Figure 10-5a: DM-31 Mechanical Dimensions

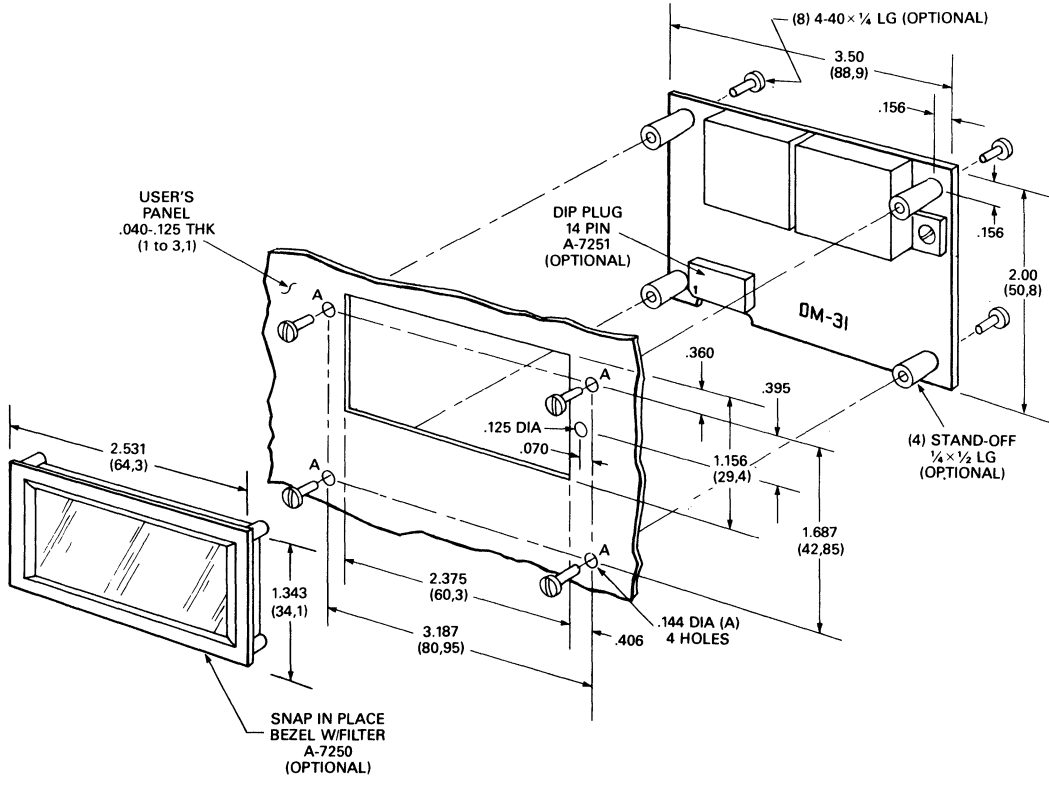
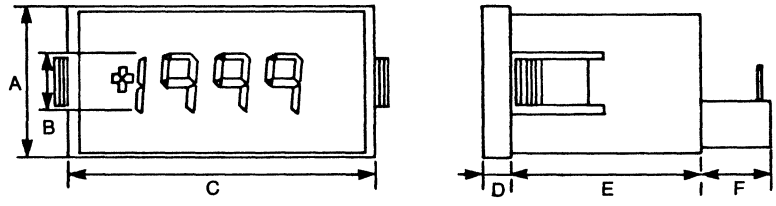


Figure 10-5b: DM-31 Panel Mounting with Optional Bezel/Filter

MECHANICAL DIMENSIONS INCHES (mm)

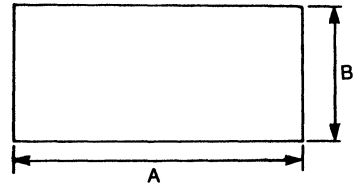


A: 0.94 (24)
B: 0.31 (8.0)
C: 1.89 (48)

D: 0.20 (5)
E: 1.22 (31)
F: 0.47 (12)

Figure 10-6a: DM-500 Mechanical Dimensions

PANEL CUTOUT DIMENSIONS



INCHES	mm
A: 1.80 (+0.01, −0)	45.7 (+0.3, −0)
B: 0.89 (+0.01, −0)	22.7 (+0.3, −0)

Figure 10-6b: DM-500 Panel Mounting

FUNCTIONAL PINOUT DESCRIPTION

ANALOG HI IN
ANALOG LO IN

Differential input voltages connect to these inputs. A bias current path to POWER COMMON or ANALOG RETURN from both these inputs must be externally provided. External circuits must restrict these inputs to be within the common-mode voltage range.

ANALOG RETURN IN

This signal line may be used as a reference for some floating inputs. If not possible, inputs may be referenced to POWER COMMON. ANALOG RETURN is approximately -2.8V below +Vs and can sink 30 mA to -Vs.

ATTENUATOR IN

This signal line is used as ANALOG HI IN line for higher voltage and current ranges. Install the attenuator and shunt resistors prior to using this signal line.

BLANK IN

Activating this signal line blanks the display, excluding the selected decimal points and the polarity sign. Data remains valid even with the display blanked.

BUSY/DONE OUT

This signal line is active during A/D conversions. The signal line remains active until the conversion is complete or until the end of measurement in the case of an OVERRANGE. This signal line may be used to prevent the input voltage from changing during conversions.

BCD OUT

Depending on the DPM model, these signal lines are digit serial outputs or 3-state outputs. Refer to the data sheets for details on these signal lines.

DATA READY OUT

This signal is a short pulse (10 microseconds) which is produced 10 microseconds after the data is valid in the DPM latches. This signal line may be used to trigger an external microprocessor-based device.

DECIMAL POINT SELECT IN

The decimal points are selectable depending upon the application and range of operation. To select a decimal point on the display, connect the decimal point signal line to ground or DECIMAL POINT COMMON.

DESCRIPTORS IN

Some DPM models are equipped with descriptors to display electrical units. The descriptors function as labels only. They do not select functions.

DIGIT DRIVES OUT

These signal lines multiplex the BCD data and direct the BCD to the proper digit. These signal lines scan the five displays approximately 150 times per second (1.3 Milliseconds per digit). DIGIT DRIVES may be used for driving remote slave displays.

DISPLAY ENABLE IN

This signal line must be active for normal operation. Not activating this signal line blanks the display, but keeps the A/D converter sampling to reduce display turn-on drift.

DISPLAY TEST IN

Activating this signal line displays 1888 on the DPM.

EOC OUT

This signal line goes high during A/D conversions. This may be used to prevent the input voltage from changing during conversions.

EXT REF LO IN

The reference input from an external source must be referred to this signal line.

HOLD IN

Activating this signal line will hold and displays the last sample storage.

HORIZONTAL POLARITY Activating this signal line displays the horizontal portion of the polarity sign.

OFFSET OUT This signal line provides a 0 to 6.9V dc output referred to the negative rail. Using this signal line requires installing optional offset potentiometer.

OHMS LO OUT This signal line is used in the ohmmeter configuration only. This signal line is 6.9V dc above the DPM's -5V dc negative rail.

OVERRANGE OUT This signal line is high if the previous input signal exceeds the A/D converter range of +19999 counts. The signal line remains high until the beginning of reference integration in the next measurement cycle. UNDERRANGE and OVERRANGE are normally used as up/down ranging gain selection controls for an auto-ranging input selection.

OUT OF RANGE OUT See OVERRANGE.

OVERSCALE OUT See OVERRANGE.

POLARITY ENABLE IN Activating this signal line causes a '+' sign to be displayed for positive inputs and a '-' sign for negative inputs.

POLARITY OUT This signal line is active when the DPM receives a negative input signal. It is valid even for a zero reading. A display of +0000 means the signal is positive but less than the least significant digit.

POWER COMMON IN The common of the external dc power source must be connected to this signal line. This signal line may also be used as a bias current return path for signal inputs.

REFERENCE IN Normally the DPM is calibrated when a +1V dc drop exists between the signal line and ANALOG RETURN. For ratiometric operation, an external reference is biased against ANALOG RETURN, on EXT REF LO.

REFERENCE OUT This signal line is normally jumpered to the REFERENCE IN LINE. This signal line is approximately +1V dc above ANALOG RETURN.

REF IN/OUT The DPM is calibrated when a +1V dc drop exists between the signal line and ANALOG RETURN. The DPM's are provided with an option to allow external ratiometric reference. The external source must be biased against ANALOG RETURN, on EXT REF LO.

RUN/HOLD IN See HOLD.

STROBE OUT After every A/D conversion, five negative pulses of approximately 6.7 microseconds width and approximately 1.3 milliseconds apart are issued on this line. The STROBE signal indicates that valid multiplexed data is available on the BCD data output lines. The data starts with the most significant digit.

UNDERRANGE OUT This signal line is active if the previous input displays 1800 counts or less. The signal line remains high until the beginning of signal integration in the next measurement cycle.

UNDERSCALE OUT See UNDERRANGE.

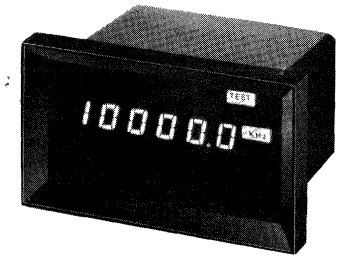
VERTICAL POLARITY This signal line must be used with the HORIZONTAL POLARITY line for automatic sign display of bipolar inputs.

PC-6
Programmable 10 MHz Counter-Timer

DATEL

FEATURES

- **Performs five functions: unit counter, frequency counter, sub-second period counter, frequency ratio counter, and sub-second interval timer**
- **Offers four full-scale ranges to measure frequency and time (period and interval)**
- **All functions, ranges, and input slopes programmable using TTL-compatible inputs or front-access command switches**
- **6-digit LED display with descriptors**



GENERAL DESCRIPTION

The DATEL PC-6 is a low cost, ultra-compact, programmable 10 MHz Universal Counter-Timer. Frequency and time measurements are displayed on a 6-digit, .3" high Light Emitting Diode (LED) display. The counter is housed in a panel-mount polycarbonate short depth case.

Frequency measurements to 10 MHz can be made using an internal crystal timebase (Frequency Counter function, with the measured Frequency display in kHz), or with an external timebase (Frequency Ratio Counter where FA/FB is displayed). The PC-6 can also function as a Unit Counter, a Sub-Second Period Timer (single input, measuring the period of a single waveform), or a Sub-Second Interval Timer (dual input, measuring the time period from a start pulse on Input A to a stop pulse on Input B). Four ranges for each function permit resolution on frequency measurements to .1 Hz and resolution on time measurements to 100 pS.

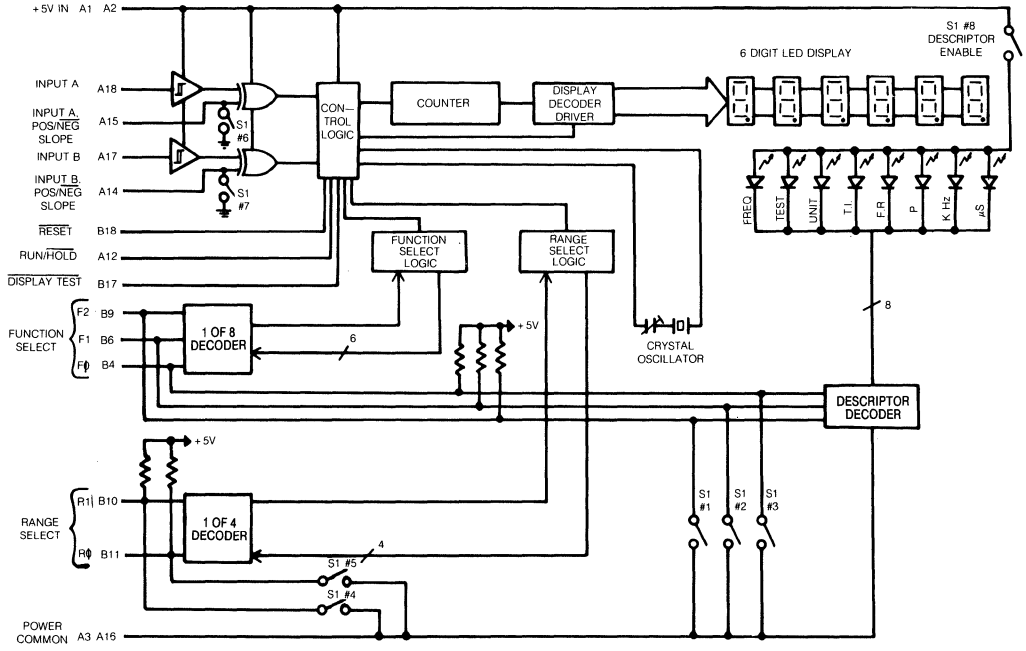
The PC-6 differs from many available Universal counter-timers in being programmable. Counter function, range, and input slope are selected by a binary code. The code is input either electrically on rear-panel, TTL-compatible digital inputs; or manually by setting a front-access Command DIP Switch.

ORDERING INFORMATION

To Order, Specify: PC-6

ACCESSORIES

Part Number	Description
58-2075010	Dual 18-pin edge connector
UPA-5/500	115V AC in, +5V dc (@ 500mA) out power adaptor



Simplified Block Diagram of a PC-6

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SPECIFICATIONS

(Typical at +25°C unless noted)

FUNCTIONS

Unit (Event) Counter
Event counter dosplays total number of low-to-high transitions (or high-to-low, see Input Slope Selection Chart). Clears by RESET (Pin B-18).

Measurement Range ....999,999 counts occuring at up to 10 MHz rate.

Frequency Counter
Measurement Range ....10 MHz max. with 50 nS min. pulse width.
Full Scale Ranges .....10000.0 kHz, 9999.99 kHz, 999.999 kHz, 99.9999 kHz.
Gate Times .....User-selectable: 10mS, 100mS, 1S, 10S.
Timebase .....Internal.
Displayed Unit .....kHz.

Sub-Second Period Timer (Single Input)
Measurement Range ....500 nS to .999999S.
Full Scale Ranges .....99999.9 μS, 9999.99 μS, 999.999 μS, 99.9999 μS.
Cycles Measured .....User-selectable: 1, 10, 100, 1000.
Displayed Unit .....μS.

Frequency Ratio Counter
Frequency Ratio Counter measures a frequency at Input A referenced to another frequency at Input B, and displays the unitless ratio FA/FB.

Full Scale Ranges .....99999.9:1, 9999.99:1, 999.999:1, 99.9999:1.
Frequency Range, Input A .....10 MHz maximum with 50% duty cycle square waves
Frequency Range, Input B .....2.0 MHz maximum
Cycles Measured .....User-selectable: 1, 10, 100, 1000.
Displayed Unit .....Pure ratio, FA/FB.

Sub-Second Interval Timer (Dual Input)
Time Interval Timer measures time period from a start pulse at Input A to a stop pulse at Input B.

Measurement Range ....500 nS to .999999S.
Full Scale Ranges .....99999.9 μS, 9999.99 μS, 999.999 μS, 99.9999 μS.
Cycles Measured .....User-selectable: 1, 10, 100, 1000.
Displayed Unit .....μS.

Test
Test measures the PC-6 internal oscillator frequency (10 MHz nominally).
Resolution .....100 Hz, 10 Hz, 1 Hz, .1 Hz.
Gate Times .....User-selectable: 10 mS, 100 mS, 1S, 10S

Overall Accuracy
±1 count

Crystal Accuracy
10 ppm accuracy, total (typical) over full temperature range.

Display
Six self-illuminated red LED digits, .3" (7,6mm) high.

Decimal Point
A decimal point is automatically positioned to set display for units shown

Descriptors
Set of 8 LED lamps, which illuminate lenses to indicate Function and Displayed Unit. consists of: FREQ, TEST, UNIT, T.I. (Time Interval), F.R. (Frequency Ratio), P (Period), kHz, and μS. Descriptors are automatically selected with Function and Range Selection, or may be disabled by opening Command Switch #8.

Overrange
"Over" lamp on front panel lights: counting on displayed digits continues

Front-Access Control
Command Switch S1 can be used to select Function, Range, Input Slope, and to enable or disable Descriptors

Time Between Measurement Cycles
200mS, all Functions, all Ranges.

I/O SIGNAL FEATURES

+5V IN (Pins A-1, A-2)
POWER COMMON (Pins A-3, A-16)
Power to PC-6 is input here: +5V (regulated) @ 350 mA required. All logic inputs may be tied to +5V IN for Logic Hi; all inputs may be tied to POWER COMMON for Logic Lo. All inputs are returned at POWER COMMON.

INPUT A (Pin A-18)
INPUT B (Pin A-17)
Signals to be measured are input here (return at POWER COMMON). INPUT A is used for all functions except Test. INPUT B is used only in Frequency Ratio and Time Interval functions.

INPUT A: POS/$\overline{\text{NEG}}$ SLOPE IN (Pin A-15)
INPUT B: POS/$\overline{\text{NEG}}$ SLOPE IN (Pin A-14)
These logic inputs select positive or negative slopes for INPUT A and INPUT B (see "Input Slope Selection" Chart).
Connecting either input to POWER COMMON sets that input for a negative slope; connecting either to +5V IN selects a posibite slope.

F2 (Pin B-9) FUNCTION
F1 (Pin B-6) INPUT
F0 (Pin B-4) CODE
R1 (Pin B-10) RANGE
R0 (Pin B-11) INPUT CODE
These five pins select all Functions and Ranges on the PC-6. See "PC-6 Function and Range Selection Chart" for details. Inputs are CMOS with 10kΩ pull-ups to +5V for compatibility with open collector logic.
1 = Logic HI (+3.5V < VH < +5V).
0 = Logic LO (0V < VL < +1.5V).

RESET INPUT (Pin B-18)

Connecting this pin to POWER COMMON stops any measurement in progress, resets the main counter, and displays all zeros. Tie to +5V IN for normal operation. Input is to a Schmitt Trigger (negative-going threshold = 1.5V typ; positive-going threshold is +0.8V typ).

POWER REQUIREMENTS

+5V IN regulated at 350 mA typical between pins A1/A2 (+5V IN) and A3/A16 (POWER COMMON). Logic spikes must not exceed 50 mV. Current varies rapidly as digits switch so that unregulated supplies cannot be used.

PHYSICAL-ENVIRONMENTAL

Outline Dimensions Short-Depth Case, 3.00"W x 2.15"D x 1.76"H (76,2 x 54,6 x 47,7 mm)

Cutout Dimensions
1.812"H x 3.062"W (46,0 x 77,7 mm)

Mounting Method
See end of this section.

Weight
Approximately 7.4 ounces (210 g)

Operating Temperature Range
0° to +50°C (32° to 122°F)

Storage Temperature Range
-25°C to +85°C (-13° to +185°F)

Altitude
0 to 15,000 feet (4900m)

Relative Humidity
10% to 90% non-condensing

INPUT OUTPUT CONNECTIONS PC-6

BOTTOM A		TOP B
+5V PWR IN	1	NO CONNECTION
	2	NO CONNECTION
PWR COMMON	3	NO CONNECTION
NO CONNECTION	4	FUNCTION FØ
KEYWAY →		← KEYWAY
NO CONNECTION	5	NO CONNECTION
NO CONNECTION	6	FUNCTION F1
NO CONNECTION	7	NO CONNECTION
NO CONNECTION	8	NO CONNECTION
NO CONNECTION	9	FUNCTION F2
NO CONNECTION	10	RANGE R1
NO CONNECTION	11	RANGE RO
RUN/HOLD	12	NO CONNECTION
NO CONNECTION	13	NO CONNECTION
B SLOPE	14	NO CONNECTION
A SLOPE	15	NO CONNECTION
PWR COMMON	16	NO CONNECTION
INPUT B	17	DISPLAY TEST
INPUT A	18	RESET

THE WAVEFORMS BELOW INDICATE THE MINIMUM TIMES AN INPUT MUST BE HIGH OR LOW TO INCREMENT THE COUNTER CIRCUITRY IN THE PC-6.

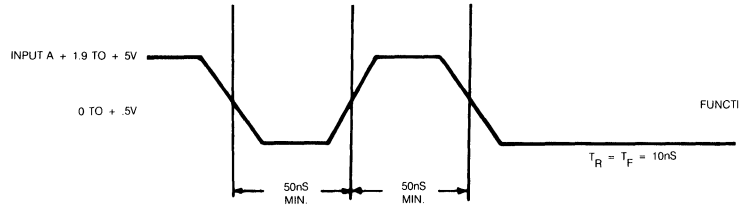


FIGURE 1
FUNCTION = FREQUENCY, FREQUENCY RATIO, UNIT COUNTER

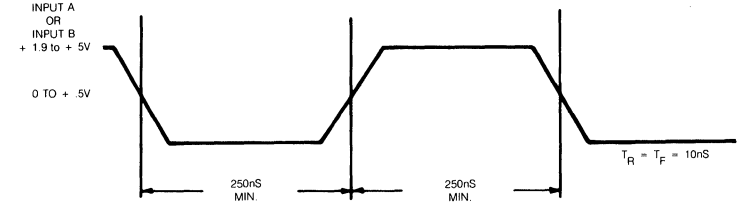


FIGURE 2
FUNCTION = PERIOD, TIME INTERVAL

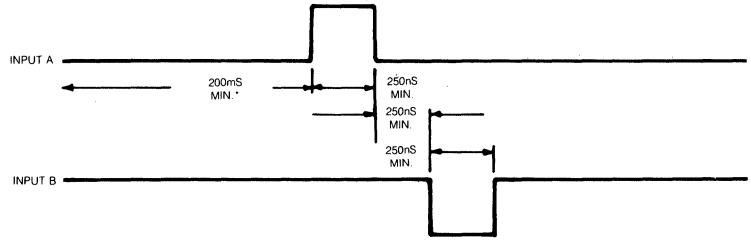


FIGURE 3
FUNCTION = TIME INTERVAL

* 200ms REQUIRED BETWEEN MEASUREMENTS FOR INTERNAL CIRCUITRY TO UPDATE.

PC-6 Input Waveforms

PC-6 FUNCTION AND RANGE SELECTION CHART

FUNCTION (8)	FULL SCALE DISPLAY RANGES	GATING TIMES/ CYCLES MEASURED	FUNCTION/RANGE SELECTION: S1 DIP SWITCH	Rear-Panel Logic Input (1) B9	B6	B4	B10	B11	TYPICAL INPUT WAVEFORM	SIGNAL (4) INPUT PIN(S)
UNIT (EVENT) COUNTER	999999 counts	N/A	OPEN 1 2 3 (2)	ϕ	1	1	-	-		A-18
FREQUENCY COUNTER (Internal Time-base)	10000.0 kHz	.01S	OPEN 1 2 3 4 5 (2)	ϕ	ϕ	ϕ	ϕ	ϕ		A-18 (7)
	9999.99 kHz	.1S	OPEN 1 2 3 4 5	ϕ	ϕ	ϕ	ϕ	1		
	999.999 kHz	1S	OPEN 1 2 3 4 5	ϕ	ϕ	ϕ	1	ϕ		
	99.9999 kHz	10S	OPEN 1 2 3 4 5	ϕ	ϕ	ϕ	1	1		
SUB-SECOND PERIOD TIMER (single input)	99999.9 μS	1	OPEN 1 2 3 4 5	1	1	ϕ	ϕ	ϕ	T_A	A-18 (7)
	9999.99 μS	10	OPEN 1 2 3 4 5	1	1	ϕ	ϕ	1		
	999.999 μS	100	OPEN 1 2 3 4 5	1	1	ϕ	1	ϕ		
	99.9999 μS	1000	OPEN 1 2 3 4 5	1	1	ϕ	1	1		
FREQUENCY RATIO COUNTER (External Time-base)	99999.9:1	1	OPEN 1 2 3 4 5	1	ϕ	1	ϕ	ϕ	INPUT A	A-18 (INPUT A)
	9999.99:1	10	OPEN 1 2 3 4 5	1	ϕ	1	ϕ	1		
	999.999:1	100	OPEN 1 2 3 4 5	1	ϕ	1	1	ϕ	INPUT B	A-17 (INPUT B)
	99.9999:1	1000	OPEN 1 2 3 4 5	1	ϕ	1	1	1		
SUB-SECOND INTERVAL TIMER (dual input)	99999.9 μS	1 (6)	OPEN 1 2 3 4 5	1	ϕ	ϕ	ϕ	ϕ	$T_{A \to B}$	A-18 (INPUT A)
	9999.99 μS	10	OPEN 1 2 3 4 5	1	ϕ	ϕ	ϕ	1		
	999.999 μS	100	OPEN 1 2 3 4 5	1	ϕ	ϕ	1	ϕ		A-17 (INPUT B)
	99.9999 μS	1000	OPEN 1 2 3 4 5	1	ϕ	ϕ	1	1		
TEST	10000.0 kHz (3)	.01S	OPEN 1 2 3 4 5	ϕ	1	ϕ	ϕ	ϕ	N/A	N/A
	0000.00 kHz (3)	.1S	OPEN 1 2 3 4 5	ϕ	1	ϕ	ϕ	1		
	000.000 kHz (3)	1S	OPEN 1 2 3 4 5	ϕ	1	ϕ	1	ϕ		
	00.0000 kHz (3)	10S	OPEN 1 2 3 4 5	ϕ	1	ϕ	1	1		

NOTES:

1) ϕ = Logic Low (0V< V_L <+1.5V)
   1 = Logic High (+3.5V< V_H <+5.0V)
   - = Don't care.

2) FREQUENCY COUNTER may identically be selected by:

		B9	B6	B4
OPEN	1 2 3	ϕ	ϕ	1
OPEN	1 2 3	1	1	1

Range Selection codes are those given in the above chart for ϕϕϕ Function Code.

3) TEST measures the internal oscillator frequency of the PC-6. This is nominally 10.0MHz (10000kHz). In the lower three ranges on TEST, the 10.0MHz frequency will be over-scale (Overrange light will turn on). The least significant digits on these ranges are accurately displayed to permit more accurate calibration of the PC-6.

4) All input signals are returned at A-16, POWER COMMON.

5) On the PC-6, Gating Times or Number of Cycles Measured is selected automatically with the Full Scale Display Range.

6) To measure a single cycle in the INTERVAL TIMER function, the PC-6 must be "primed," first by a single cycle preceding that to be measured. The first cycle sets the counter circuitry; the second cycle is measured.

7) In FREQUENCY and PERIOD functions, tie INPUT B (pin A-17) to POWER COMMON (pin A-16).

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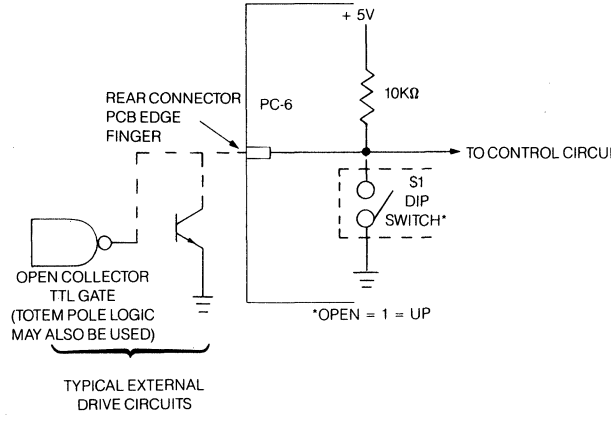
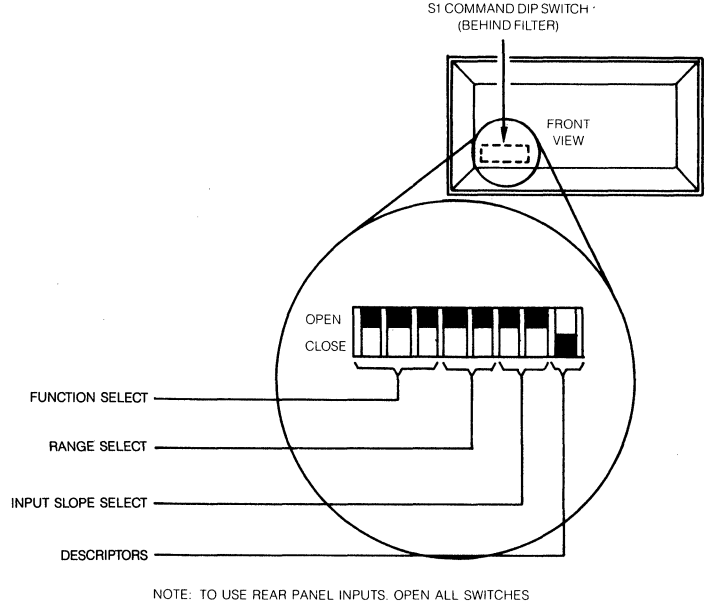
APPLICATION NOTES

The PC-6 is designed to fit into automatic test equipment. In most applications, the tester's built-in logic circuitry can program the PC-6's functions, ranges and input slopes. The PC-6 with external circuits (switches, power supply and connectors) may be configured as a full, self-contained benchtop counter for test and repair applications.



PC-6 Typical Programmable Function Input



NOTE: TO USE REAR PANEL INPUTS, OPEN ALL SWITCHES

PC-6 Command Switch Location

PM-5050
THERMOCOUPLE INPUT INTELLIGENT PROCESS MONITOR/CONTROLLER

FEATURES

- **Microprocessor-based, with all operating parameters set/recalled using the front panel or via the RS-232-C serial communications port.**
- **Totally menu-driven monitor configuration including:**
  1. **J, K, T, S, B, E, N, or R type thermocouple measurement.**
  2. **Cold junction compensation (CJC) enable/disable option.**
  3. **Celsius or Fahrenheit display option with 0.1, 1.0 degree resolution.**
  4. **Up to 4 setpoint entries, with up to 25 degrees hysterisis.**
  5. **Serial communications options for baud rate, parity, stop bits.**
- **Automatic display of open thermocouple conditions. Automatic gain and offset calibration.**
- **Total signal-to-logic and line-to-logic isolation (1400V).**
- **Over 50 simple ASCII commands usable via the serial port for data acquisition and control.**
- **Four MOSFET setpoint outputs (300V, 100mA load) are individually programmable for absolute, relative, high-, or low-going temperatures.**
- **Six character (five digits), 14-segment, alphanumeric 0.4" high fluorescent blue-green display with six custom annunciators.**

- **Security feature to prevent front panel tampering.**
- **All parameter values saved in EEPROM.**
- **Optional analog output (0 to 10V dc or 4-to-20 mA). User-programmable temperature range for scaling.**
- **Screw-terminal connectors for easy power and input connections.**
- **Compact ⅛ DIN case, standard DIN panel mount cutout.**
- **Interfaces directly to Datel's thermal printers.**
- **Optional RS-485 interface for 32-point multi-drop applications.**

DATEL'S PM-5050 INTELLIGENT PROCESS MONITOR AND DISPLAY IS SPECIFICALLY DESIGNED FOR REAL-TIME THERMOCOUPLE DATA ACQUISITION AND CONTROL APPLICATIONS. THE HIGH-ISOLATION INPUT AND FOUR SETPOINT OUTPUTS ARE TOTALLY CONTROLLABLE FROM THE EASY-TO-USE RS-232-C ASYNCHRONOUS COMMUNICATIONS PORT. ENGINEERED FOR RUGGED INDUSTRIAL ENVIRONMENTS, THE PM-5050 OFFERS UP TO 1400V ISOLATION, 128dB CMRR, AND A HIGH RFI AND EMI IMMUNITY.

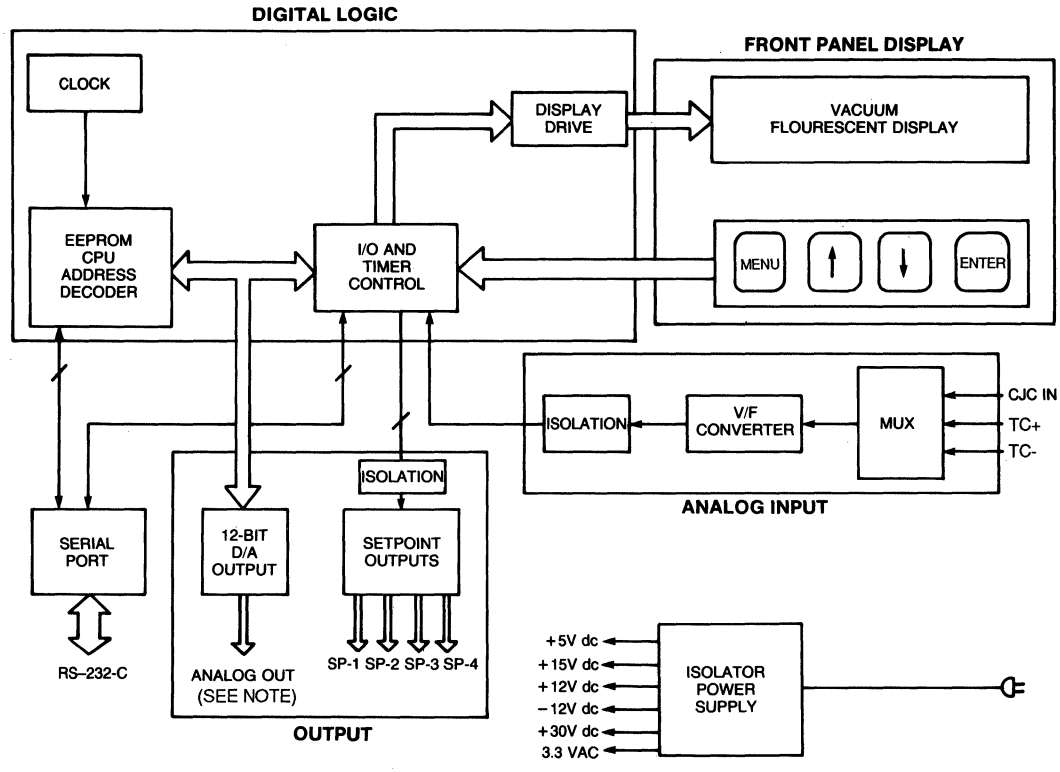
FUNCTIONAL DESCRIPTION

The functionality built into the PM-5050 allows high-precision process monitoring with real-time display of process parameters. The monitor supports eight thermocouple types: J, K, T, S, B, E, N, and R. Functionally, the PM-5050 has five sections: isolated analog input section, microprocessor and control logic, front panel key board and display, serial communications port, and setpoint outputs. (See the Block Diagram in Figure 1.)

The isolated analog input section consists of thermocouple input circuitry, signal conditioning pre-amplifiers, cold junction compensation (CJC) circuits, and a voltage-to-frequency converter. The analog input section is isolated up to 1400V RMS from the control logic and power lines. The 128dB CMRR ensures accurate readings by rejecting unwanted common mode voltages sometimes introduced by ground loops. The CJC input is located in the screw terminal connector, thus offering a true cold junction compensation reference.

The microprocessor and control logic linearizes the input signal depending on the thermocouple type used. This section also processes commands received from both the front panel keypad and the RS-232-C serial communications port. The monitor supports over 50 ASCII commands for operation via the serial communications port. The command structure uses simple command/reply message protocols. All control parameters set on the monitor are saved in an EEPROM and are automatically retrieved on power up.

A significant feature of the monitor is the easy-to-use front panel keypad. All meter functions are user-selectable by a few simple keystrokes. The display is completely menu-driven with selectable parameters appearing directly on the display. The vacuum fluorescent display has six custom annunciators, four for indicating setpoint status, and two for calibration parameters (full-scale, and zero). The PM-5050 displays five digits, such as 3001.6, providing a tenth of a degree of resolution.



NOTE: The optional analog output is user-configurable for 4-to-20 mA or 0 to +10V dc.

Figure 1. PM-5050 Block Diagram

The PM-5050's serial port is configurable to perform as either a DTE or DCE device, depending on how the communication cable is wired. The monitor supports simple ASCII commands to exercise the functions. In addition to the commands that read, set, and invoke control parameters, the software in the monitor also supports diagnostic commands. The PM-5050 is configurable for baud rates from 110 to 9600 baud.

The PM-5050 provides the user four opto-isolated setpoint outputs (SP-1 through SP-4) to respond to four front panel-selectable preset temperatures. The annunciators on the vacuum fluorescent display indicate the setpoint status.

The setpoint outputs are isolated from power lines, logic, and input to up to 1500 volts. The setpoints are individually programmable for high- or low-going, absolute, or relative temperatures. For relative setpoint operation, setpoints SP-2, SP-3, and SP-4 are active relative to setpoint SP-1. The setpoints may be set in degrees C or degrees F with user-selectable hysterisis bands up to 25 degrees.

The setpoint outputs are solid state MOSFET relays able to drive up to 100 mA, 300V loads. The setpoint outputs are usable as alarm outputs or to control heater circuits in temperature control applications. The alarm status is displayed through the display annunciators.

Table 1 shows the various types of thermocouple input ranges available.

Table 1. Thermocouple Input Ranges, Accuracy and Drift, (maximum)

Thermocouple Type	Temperature Range (°C)	Accuracy	Temperature Drift (°C/°C)
J	−210 to −100 −100 to +760	+0.2°C +0.1°C	0.1
K	−212 to −100 −100 to 0 0 to +1371	+0.3°C +0.1°C +0.2°C	0.15
S	0 to 300 +300 to 1768	+0.7°C +0.5 C	0.3
T	−270 to −200 −200 to +400	+1.0°C +0.5°C	0.1
B	+210 to +750 +750 to +1820	+1.0 C +0.6°C	0.3
E	−270 to −200 −200 to −100 −100 to +900	+0.7 C +0.2°C +0.1°C	0.15
R	−50 to 0 0 to +850 +850 to +1768	+1.2°C +0.4°C +0.5°C	0.3
N	−200 to 0 0 to +400	+0.4°C +0.2°C	0.3

FUNCTIONAL SPECIFICATIONS
(Typical at 25 degrees C, unless noted)

ANALOG INPUT

Analog-to-digital conversion	Voltage-to-frequency converter, microprocessor controlled
Conversion time	300 mSec, maximum
Resolution (User-selectable)	0.1 degree or 1 degree
Range Tempco	+25 ppm/°C, typical +50 ppm/°C, maximum
CJC error 0 to 60°C	+0.5°C, maximum
Stability	Automatic gain and offset calibration every 1.8 seconds
Configuration	Differential (Isolated)
Range	−10mV to +70mV dc
Impedance	100 Megohms, minimum
Common mode voltage	1400V (peak AC or dc)
Differential input overvoltage protection	115 VAC, continuous
(Short to or across AC line without damage.)	230 VAC, 5 seconds
Normal mode rejection ratio, at 50/60 Hz	80 dB, minimum
Common mode rejection ratio, dc to 60 Hz	128 dB, minimum 140 dB, typical

DISPLAY SPECIFICATIONS

Type	14-segment, alphanumeric, blue-green vacuum fluorescent
Number of characters	6 alphanumeric characters
Annunciators	SP-1, SP-2, SP-3, SP-4, ZERO, F.S.

SETPOINT OUTPUT SPECIFICATIONS

Number of setpoint outputs	4
Setpoint control	User-programmable for high or low-going, absolute or relative temperatures. For relative operation, SP-2, SP-3, and SP-4 are active relative to SP-1
Output type	Opto-isolated MOSFET's
Isolation	1000V minimum, 1500V typical
Output rating (maximum)	300V at 100 mA resistive load
Hysteresis range	User-selectable; 25 degrees, maximum

POWER REQUIREMENTS

Operating Voltage	100, 115, 230 VAC +5V dc, or +9 to +36V dc (optional)
Power Consumption	
AC Models	2.5W typical, 4W max.
DC Models	385 mA @ 5V dc

SERIAL COMMUNICATION SPECIFICATIONS
(RS-232-C standard)

Baud rate	110 to 9600 baud
Format	
Data bits	7 or 8
Parity	Even, odd, or none
Stop bits	1 or 2

ANALOG OUTPUT SPECIFICATIONS (OPTION)

Types	Voltage or current, user-selectable
VOLTAGE	0 to 10V dc, at 2A maximum
Resolution	12 bits
Non-linearity	±0.1%
Gain Tempco	±50 ppm/degree C
Offset Tempco	±0.1 mV/degree C
Span	Programmable using front panel keys.
CURRENT	4-to-20 mA
Compatibility	ISA type U
Excitation	Internal
Accuracy	0.1% full-scale range
Load Resistance	100 ohms, minimum 1000 ohms, maximum
Span and Offset	Programmable using front panel keys

PHYSICAL SPECIFICATIONS

Case quality	High-impact, flame retardant polycarbonate
Case dimensions	3.622″W × 1.771″H × 5.47″L (92 W x 45 H x 139 L) mm
Length including terminals	6″ (152 mm)
Bezel dimensions	3.97″ W × 2.08″ H x 0.35″D (101 W x 53 H x 9 D) mm
Panel cutout	⅛ DIN standard 3.622″W × 1.772″H (92W x 45H) mm
Front panel control	Membrane keypad with 4 key switches
Weight	1 pound 4 ounces

ENVIRONMENTAL SPECIFICATIONS

Operating temperature range (see note)	0 to +60°C (+32 F to +140°F)
Storage temperature range	−40°C to +85°C (−40°F to +185°F)
Relative humidity	0 to 90%, non-condensing

NOTE: The monitor will operate from −10°C to +70°C at a reduced accuracy.

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ANALOG OUTPUT

The PM-5050 has an optional analog output which outputs a voltage or current in proportion (or inverse proportion) to the temperature reading. The output is suitable for simple control applications (e.g., heater control) or to drive external measuring devices such as strip chart recorders.

An on-board 12-bit D/A converter provides a 0 to 10V dc or 4 to 20 mA output. The temperature range for the output is programmable from either the front panel or the serial communications port. The on-board microprocessor performs the required D/A output scaling.

PM-5050 MENU DESCRIPTION

The PM-5050 is operable from both the front panel key pad and the serial communications port. The front panel keypad consists of four keys: MENU SELECT, UP ARROW, DOWN ARROW, and ENTER. The menus are interactive, with the process parameter appearing directly on the display. The MENU select key scrolls through the menus available at each level and the ARROW keys scroll through options available for each parameter selected. The ENTER key sets the value for the selected parameter. Table 2 shows the parameter values.

The serial communications menu also allows enabling a data output mode. In this mode, the PM-5050 continuously outputs a data message to a printer at a user-selectable rate. The data message consists of information on the monitor configuration, status of setpoints, and thermocouple data.

Table 2. PM-5050 Front Panel Menu Options

Menu	Menu Selection Choice	Parameter Selection Choices
Security Code	See Notes	Enable/Disable
Input	TC type	J, K, T, S, B, E, N, and R
	Unit	Degree C of Degree F
	Resolution	0.1°C or 1.0°C
	CJC	On or Off
Setpoint	1 to 4	User-selectable
	Hysterisis	Up to 25 degrees
Serial Communications	Baud rate	110, 300, 600, 1200, 2400, 4800 and 9600
	Parity	Odd, Even, or None
	Stop bits	1 or 2
	ID number	0 through 99
Self-test	Diagnostics	
Calibration		A/D, CJC, and D/A
D/A output		Zero and full-scale

NOTES

The PM-5050 uses three different security codes for the following:

1. Enable the security to prevent front panel tampering.
2. Enabling the calibration mode to calibrate the meter.
3. Disabling the security to change monitor settings.

PM-5050 SERIAL COMMUNICATIONS

A standard feature included in the PM-5050 is an RS-232-C serial communications port. The PM-5050 may operate as a DTE or DCE device depending on the connection scheme used from the J1 connector to a typical D-type connector.

The monitor receives configuration information and process parameters via the serial port, using conventional ASCII message formats. The monitor is configurable for different baud rates, parity, stop bits and ID number using the front panel keys. The monitor supports over 50 simple ASCII commands usable via the serial port for data acquisition and control.

The host may issue three types of commands to the monitor: configuration commands, data acquisition commands, and diagnostic commands.

Configuration commands: These commands set the PM-5050 to the user-selected operating mode. The monitor responds to the commands either with an acknowledge character or by echoing the command message back to the source.

Data acquisition commands: These commands read and log in temperature data and the status of the monitor. The monitor responds with a fixed-format ASCII message. The reply message consists of an ASCII string containing the monitor's ID number, thermocouple data and status, the status of the monitor configuration, and checksum. The data acquisition commands also operate in a continuous mode. In this mode the PM-5050 sends data, status, and checksum to the host system at a user-selectable rate.

Diagnostic commands: These commands test the PM-5050 display, perform calibration, read RAM locations, read reference voltage values, and check the result of built-in self test routines. Table 3 lists some command descriptions.

Table 3. PM-5050 Command Descriptions (partial list)

Configuration Commands	Set thermocouple type Set temperature unit (°C or °F) Set resolution (0.1 or 1.0) Set/Read setpoints values Set/Read hysteresis value Set/Read D/A scaling values Transmit data in decimal or hex format Transmit to host temperature measured Transmit to host CJC temperature
Data Acquisition Commands	Transmit to host last 64 data samples with status Transmit to host the PM-5050 status Enable/Disable command echo Enable/Disable terminal emulation mode Enable/Disable reply messages on set-point conditions Set reply message format Send thermocouple data to host Output digital data to D/A section
Diagnostics Command	Test display segments Perform calibration Read internal reference values Read raw temperature value Read CJC value Perform self-test

APPLICATION: MONITORING AND CONTROLLING PROCESS TEMPERATURE

The PM-5050 has built-in features applicable to controlling process temperature. Figure 2 shows a typical PM-5050 application configuration.

The setpoint outputs provide the on/off control to a process and an alarm at preset temperatures. These setpoints may be absolute, or relative to a certain process temperature. The optional analog output is a linear controlling voltage (0 to +10V dc) that is usable to control a heater coil.

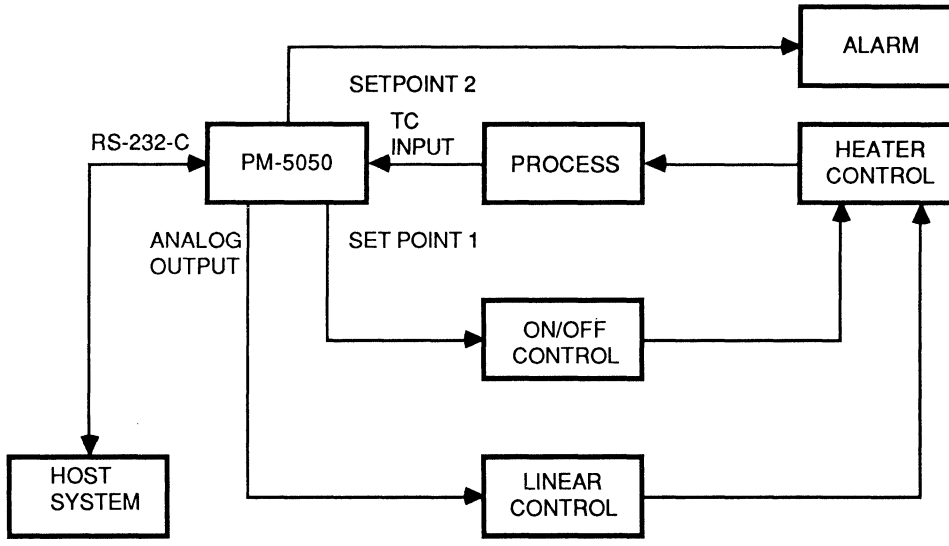


Figure 2. Temperature Control By A Host System Using the PM-5050

The PM-5050 automatically scales the analog output to a user-programmed temperature range. All process parameters may be set from the front panel or via the serial communications port. Users may also operate the PM-5050 from an intelligent host system using simple ASCII commands to acquire data and control the process.

PM-5050 INPUT/OUTPUT CONNECTIONS

The PM-5050 uses terminal blocks TB1 and TB2 for thermocouple inputs and power connections respectively. The setpoint outputs and serial communications are provided on the J1 connector. Tables 4 through 6 show pinouts for I/O connections.

Table 4a. Setpoint Output Connections (J1)

Setpoint	Connections
SP-1	B1 B2
SP-2	A1 A2
SP-3	B4 B5
SP-4	A4 A5

Table 4b. RS-232-C Connections (J1)

Signal	Connection
TXD	B21
RXD	B20
CTS	B18
RTS	B19
DTR	A16
GND	B16
+5V dc	A6

Table 5. Thermocouple Input Connections (TB1)

Signal	Connection
TC +	TB1-2
TC –	TB1-4

Table 6: AC Power Supply Connections (TB2)

Signal	Connection
GROUND	TB2-1
115/230/100 VAC Hot	TB2-2
110/230/100 VAC Neutral	TB2-3

PM-5050 MECHANICAL DIMENSIONS

The PM-5050 fits into standard 1/8 DIN panel cutouts. Mounting procedures involve tightening two screws through a metal bracket (supplied) against the front panel. Figure 3 shows the mechanical dimensions of the monitor.

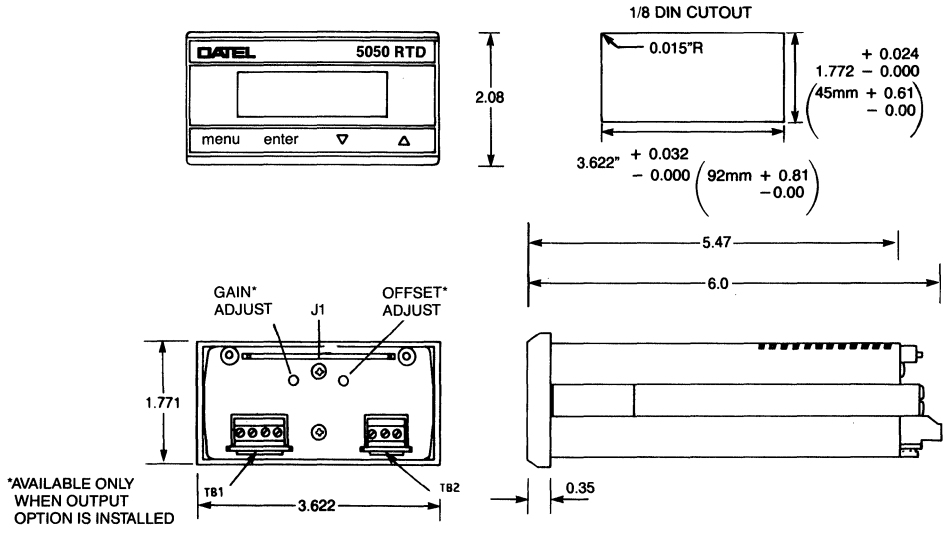
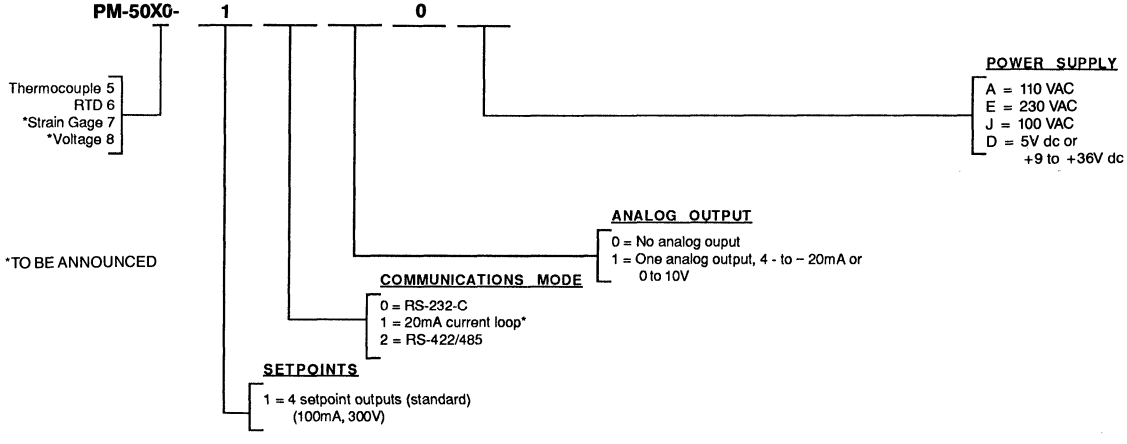


Figure 3. PM-5050 Mechanical Dimensions

ORDERING INFORMATION



PM-5060
RTD/THERMISTOR INPUT INTELLIGENT PROCESS MONITOR/CONTROLLER

FEATURES

- **Microprocessor-based, with all operating parameters set/recalled using the front panel or via the RS-232-C serial communications port.**
- **Totally menu-driven monitor configuration allows:**
  1) **Measuring inputs from**
     a) **100Ω RTD's, types:**
        American (Alpha = 0.00391)
        European (Alpha = 0.00385, DIN 43760)
     b) **Thermistors, types:**
        2252Ω, 3000Ω, 5000Ω, 10000Ω
  2) **Two-, three-, or four-wire operation**
  3) **Celsius or Fahrenheit display option with 0.1, 1.0° resolution.**
  4) **Up to 4 setpoint entries, with up to 25° hysteresis.**
  5) **Serial communications options for baud rate, parity, stop bits.**
- **Automatic display of open RTD input conditions. Automatic gain and offset calibration.**
- **Total signal-to-logic and line-to-logic isolation.**
- **Over 50 simple ASCII commands usable via the serial port for data acquisition and control.**
- **Four MOSFET setpoint outputs (300V, 100 mA load) are individually programmable for absolute, relative, high-, or low-going temperatures.**
- **Interfaces directly to IBM PC or compatibles.**
- **1400V input isolation for transient protection.**

- **Interfaces directly to DATEL's printers: APP-20_21, MPP-20, APP-48_2**
- **Six character (five digits), 14-segment, alphanumeric 0.4" high fluorescent blue-green display with six custom annunciators.**
- **Security feature to prevent front panel tampering.**
- **All parameter values saved in EEPROM.**
- **Optional analog output (0 to 10V dc or 4-to-20 mA). User-programmable temperature range for scaling.**
- **Screw-terminal connectors for easy power and input connections.**
- **Compact 1/8 DIN case, standard DIN panel mount cutout.**
- **Optional RS-485 interface for 32-point multi-drop applications.**

DATEL's PM-5060 Intelligent Process Monitor and Display is specifically designed for high-accuracy, real-time RTD and thermistor data acquisition and control applications. The high-isolation input and four setpoint outputs are totally controllable from the easy-to-use front panel or the RS-232-C asynchronous communications port. Engineered for rugged industrial environments, the PM-5060 offers up to 1400V isolation, 128 dB CMRR, and a high RFI and EMI immunity.

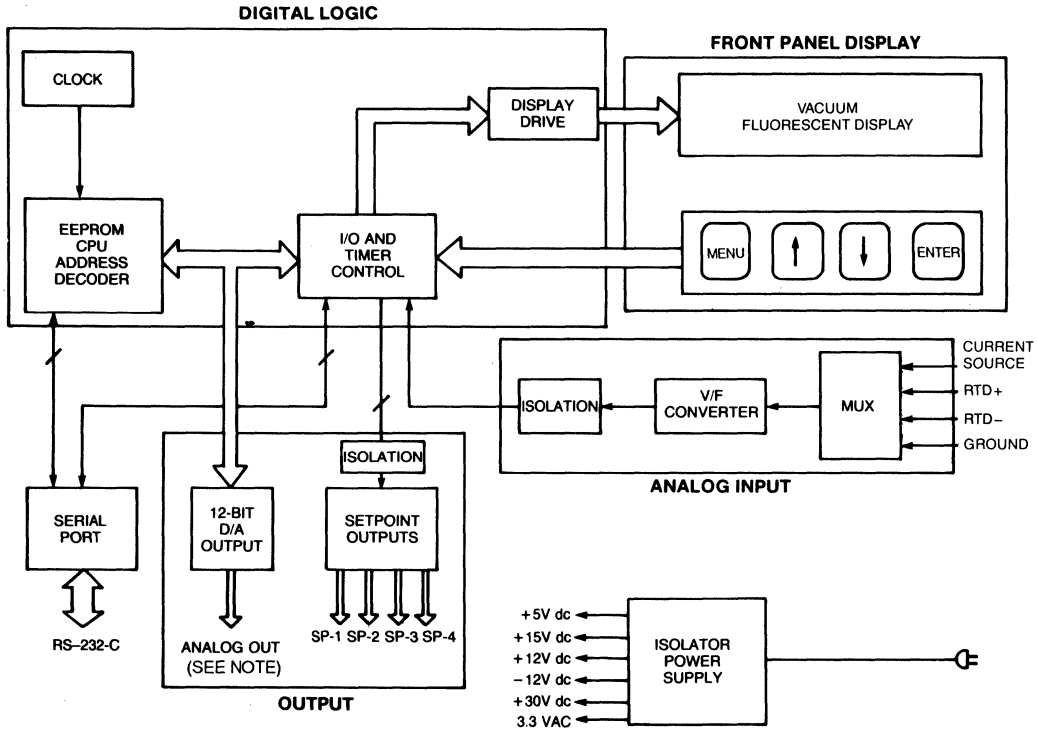
GENERAL DESCRIPTION

The PM-5060 is an ideal choice for applications requiring highly accurate high-resolution temperature measurement and display. The functionality built into the PM-5060 allows high-precision process monitoring with real-time display of process parameters. The monitor supports 100Ω platinum RTD types DIN 43760 (with Alpha = 0.00385) and American (with Alpha = 0.00391). The device also supports inputs from 2,252Ω, 3,000Ω, 5,000Ω, and 10,000Ω thermistors. The PM-5060 is usable with two-, three-, or four-wire inputs.

Functionally, the PM-5060 has five sections: an isolated analog input section, microprocessor and control logic, front panel keyboard and display, serial communications port and setpoint outputs. (See the Block Diagram in Figure 1).

The isolated analog input section consists of RTD/thermistor input circuitry, signal conditioning pre-amplifiers, and a voltage-to-frequency converter. The analog input section is isolated up to 1400V RMS from the control logic and power lines. The 128 dB CMRR ensures accurate readings by rejecting unwanted common mode voltages sometimes introduced by ground loops.

The microprocessor and control logic linearize the input signal depending on the RTD/thermistor type used. This section also processes commands received from both the front panel keypad and the RS-232-C serial communications port. The monitor supports over 50 ASCII commands for operation via the serial communications port. The command structure uses simple command/reply message protocols. All control parameters set on the monitor are saved in an EEPROM and are automatically retrieved on power up.



NOTE: The optional analog output is user-configurable for 4-to-20 mA or 0 to +10V dc.

Figure 1. PM-5060 Block Diagram

A significant feature of the monitor is the easy-to-use front panel keypad. All meter functions are user-selectable by a few simple keystrokes. The display is completely menu-driven with selectable parameters appearing directly on the display. The vacuum fluorescent display has six custom annunciators, four for indicating setpoint status, and two for indicating calibration parameters (full-scale, and zero). The PM-5060 displays five digits, such as 1472.3, providing a tenth of a degree of resolution.

The PM-5060's serial port is configurable to perform as either a DTE or DCE device, depending on how the communication cable is wired. The monitor supports simple ASCII commands to exercise the functions. In addition to the commands that read, set, and invoke control parameters, the software in the monitor also supports diagnostic commands. The PM-5060 is configurable for baud rates from 110 to 9600 baud.

The PM-5060 provides the user four opto-isolated setpoint outputs (SP-1 through SP-4) to respond to four front panel-selectable preset temperatures. The annunciators on the vacuum fluorescent display indicate the setpoint status.

The setpoint outputs are isolated to power lines, logic, and input to up to 1400V. The setpoints are individually programmable for high- or low-going, absolute, or relative temperatures. For relative setpoint operation, setpoints SP-2, SP-3, and SP-4 are active relative to setpoint SP-1. The setpoints may be set in degrees C or degrees F with user-selectable hysterisis bands up to 25°.

The setpoint outputs are solid-state MOSFET relays able to drive up to 100 mA, 300V loads. The setpoint outputs are usable as alarm outputs or to control heater circuits in temperature control applications. The alarm status is displayed through the display annunciators. Table 1 lists the input ranges of common input devices and their accuracy.

Table 1. Input Ranges and Accuracy

Input Type	Range	Accuracy	
		Typical	Maximum
100Ω Platinum RTD Alpha = 0.00391	–200 to +850°C	±0.1°C	±0.5°C
100Ω Platinum RTD Alpha = 0.00385 (DIN 43760)	–200 to +850°C	±0.2°C	±0.5°C
2252Ω Thermistors	–50 to 0°C 0 to +150°C	±2°C ±0.2°C	— —
3000Ω Thermistors	–50 to 0°C 0 to +150°C	±3°C ±0.2°C	— —
5000Ω Thermistors	0 to +150°C	±0.2°C	—
10000Ω Thermistors	0 to +150°C	±0.3°C	—

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, unless noted)

ANALOG INPUTS

Analog-to-digital ..... Voltage-to-frequency conversion converter, microprocessor controlled

Conversion Time ..... 300 mSec., maximum

Resolution (User-selectable) ..... 0.1° or 1°

Range Tempco ..... +25 ppm/°C, typical +50 ppm/°C, maximum

Stability ..... Automatic gain and offset calibration every 1.8 Sec.

Configuration ..... Differential (Isolated)

Range ..... −10 mV to +70 mV dc

Impedance ..... 100 Megohms, minimum

Common mode voltage ... 1400V (peak AC or DC)

Differential Input overvoltage protection Short to (or across) AC line without damage. .... 115 VAC, continuous 230 VAC, 5 Sec.

Normal mode rejection ratio, dc to 60 Hz .... 80 dB, minimum

Input bias current ..... 8 nA, maximum

DISPLAY SPECIFICATIONS

Type ..... 14-segment, alphanumeric, blue-green vacuum fluorescent

Number of characters ..... 6 alphanumeric characters

Annunciators ..... SP-1, SP-2, SP-3, SP-4, ZERO, F.S.

SETPOINT OUTPUT SPECIFICATIONS

Number of setpoint outputs 4

Setpoint control ..... User-programmable for high or low-going, absolute or relative temperatures.

For relative operation, SP-2, SP-3, and SP-4 are active relative to SP-1.

Output type ..... Opto-isolated MOSFET's

Output rating (maximum) ..... 300V at 100 mA resistive load

Hysteresis range ..... User-selectable; 25° max.

SERIAL COMMUNICATION SPECIFICATIONS

(Standard RS-232-C)

Baud rate ..... 110 to 9600 baud

Format

Data bits ..... 7 or 8

Parity ..... even, odd, or none

Stop bits ..... 1 or 2

ANALOG OUTPUT SPECIFICATIONS (OPTION)

Types ..... Voltage or current, user-selectable

VOLTAGE ..... 0 to 10V dc, at 2 mA max.

Resolution ..... 12 bits

Non-linearity ..... ±0.1%

Gain Tempco ..... ±50 ppm/°C

Offset Tempco ..... ±0.1 mV/°C

Span ..... Programmable using front panel keys.

CURRENT ..... 4-to-20 mA

Compatibility ..... ISA type U

Excitation ..... Internal

Accuracy ..... 0.1% full-scale range

Load Resistance ..... 100Ω, minimum 1000Ω, maximum

Span and Offset ..... Programmable using front panel keys

PHYSICAL SPECIFICATIONS

Case quality ..... High-impact, flame retardant polycarbonate

Case dimensions ..... 3.622″W × 1.771″H × 5.47″L (92 W × 45 H × 139 L) mm

Length, including terminals ..... 6″ (152 mm)

Bezel dimensions ..... 3.97″ W × 2.08″ H × 0.35″D (101 W × 53 H × 9 D) mm

Panel cutout ..... 1/8 DIN standard 3.622″W × 1.772″H (92W × 45H) mm

Front panel control ..... Membrane keypad with 4 key switches

Weight ..... 1 pound, 4 ounces

ENVIRONMENTAL SPECIFICATIONS

(The monitor will operate from −10°C to +70°C at a reduced accuracy.)

Operating temperature range .... 0 to +60°C (+32°F to +140°F)

Storage temperature range ..... −40°C to +85°C (−40°F to +185°F)

Relative humidity ..... 0 to 90%, non-condensing

POWER REQUIREMENTS

Operating Voltage (See Ordering Information) ..... 115, 230, 100 VAC +5V, or +9 to +36V dc (optional)

Power Consumption

AC Models ..... 2.5 W typical, 4 W max.

DC Models ..... 385 mA @ 5V dc

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ANALOG OUTPUT

The PM-5060 has an optional analog output which outputs a voltage or current in proportion (or inverse proportion) to the temperature reading. The output is suitable for simple control applications (e.g., heater control) or to drive external measuring devices such as strip chart recorders.

An on-board 12-bit D/A converter provides a 0 to 10V dc or 4 to 20 mA output. The temperature range for the output is programmable from either the front panel or the serial communications port. The on-board microprocessor performs the required D/A output scaling.

PM-5060 MENU DESCRIPTION

The PM-5060 is operable from the both the front panel keypad and the serial communications port. The front panel keypad consists of four keys: MENU SELECT, UP ARROW, DOWN ARROW, and ENTER. Table 2 shows the menu structures. The menus are interactive, with the process parameter appearing directly on the display. The MENU select key scrolls through the menus available at each level and the ARROW keys scroll through options available for each parameter selected. The ENTER key locks the value for the selected parameter.

The serial communications menu also allows enabling a data output mode. In this mode, the PM-5060 continuously outputs a data message to a printer at a user-selectable rate. The data message consists of information on the monitor configuration, status of setpoints, and input data.

Table 2. PM-5060 Front Panel Menu Options

Menu	Menu Selection Choice	Parameter Selection Choices
Security Code	See Notes	Enable/Disable
Input	RTD, American RTD, European	Alpha = 0.00391 Alpha = 0.00385
	Thermistor	2252Ω 3000Ω 5000Ω 10000Ω
	Unit	Degree C or Degree F
	Resolution	0.1°C or 1.0°C
Setpoint	1 — 4	User-selectable
	Hysteresis	Up to 25°
Serial Communications	Baud rate	110, 300, 600, 1200, 2400, 4800 and 9600
	Parity	Odd, Even, or None
	Stop bits	1 or 2
	ID number	0 through 99
	Set data output rate	Multiples of 0.6 Sec.
Self-test	Diagnostics	
Calibration		A/D and D/A
D/A output		Zero and Full-scale

NOTES: The PM-5060 uses three different security codes for the following:
1. Enabling the security to prevent front panel tampering.
2. Enabling the calibration mode to calibrate the meter.
3. Disabling the security to change monitor settings.

PM-5060 SERIAL COMMUNICATIONS

A standard feature included in the PM-5060 is an RS-232-C serial communications port. The PM-5060 may operate as a DTE or DCE device, depending on the connection scheme used from the J1 connector to a typical D-type connector.

The monitor receives configuration information and process parameters via the serial port, using conventional ASCII message formats. The monitor is configurable for different baud rates, parity, stop bits and ID number using the front panel keys. The monitor supports over 50 simple ASCII commands usable via the serial port for data acquisition and control.

The host may issue three types of commands to the monitor: configuration commands, data acquisition commands, and diagnostic commands.

Configuration commands: These commands set the PM-5060 to the user-selected operating mode. The monitor responds to the commands either with an acknowledge character or by echoing the command message back to the source.

Data acquisition commands: These commands read and log in temperature data and the status of the monitor. The monitor responds with a fixed format ASCII message. The reply message consists of an ASCII string containing the monitor's ID number, RTD/thermistor data and status, the status of the monitor configuration, and checksum. The data acquisition commands also operate in a continuous mode. In this mode the PM-5060 sends data, status, and checksum to the host system at a user-selectable rate.

Diagnostic commands: These commands test the PM-5060 display, perform calibration, read RAM locations, read reference voltage values, and check the result of built-in self test routines. Table 3 lists some command descriptions.

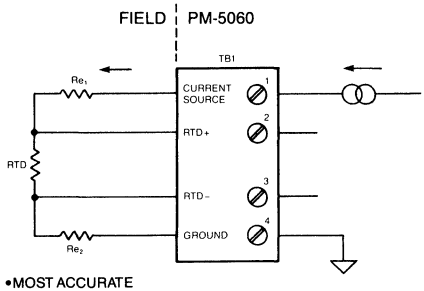
Table 3. PM-5060 Command Descriptions (partial list)

Command Type	Description
Configuration Commands	Set input type Set temperature unit (°C or °F) Set resolution (0.1 or 1.0) Set/Read setpoints' values Set/Read hysteresis value Set/Read D/A scaling values Transmit data in decimal or hex format Transmit to host temperature measured
Data Acquisition Commands	Transmit to host last 50 data samples with status Transmit to host the PM-5060 status Enable/Disable command echo Enable/Disable terminal emulation mode Enable/Disable reply messages on setpoint conditions Set reply message format Send temperature data to host Output digital data to D/A section
Diagnostics Command	Test display segments Perform calibration Read internal reference values Read raw temperature value Perform self test

TWO-, THREE-, and FOUR-WIRE RTD CONFIGURATIONS

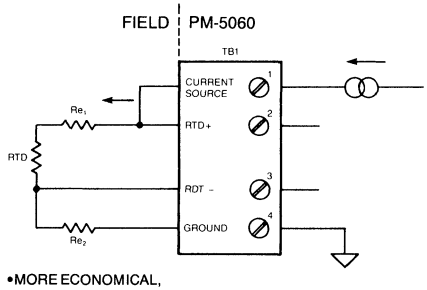
The PM-5060 accepts inputs from a variety of commercial RTD's and thermistors. The device operates with varying degrees of efficiency based upon the way the input signal is brought into the monitor. Figure 2 shows how inputs may be connected using two-, three-, or four-wire schemes. Each scheme has its advantages; the user must weigh accuracy versus economy when designing their configuration.

NOTE: When using a thermistor sensor, a 400Ω resistor must be installed externally across the RTD+ and RTD− inputs.



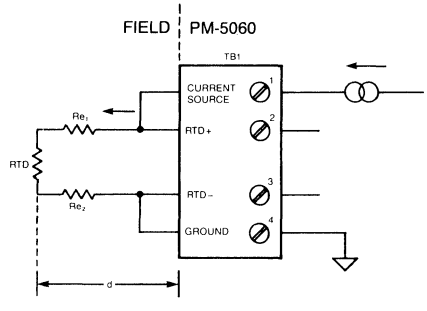
•MOST ACCURATE

Figure 2a. Four-wire Input Configuration



•MORE ECONOMICAL,
ASSUMES THAT $Re_1 = Re_2$

Figure 2b. Three-wire Input Configuration



•MOST ECONOMICAL
•LEAST ACCURATE
•ERROR PROPORTIONAL TO DISTANCE d
•SIMILAR TO 4-WIRE CONFIGURATION, BUT Re_1 AND Re_2 NOT FACTORED OUT.

Figure 2c. Two-wire Input Configuration

PM-5060 INPUT/OUTPUT CONNECTIONS

The PM-5060 uses terminal blocks TB1 and TB2 for RTD/thermistor inputs and power connections respectively. The setpoint outputs and serial communications are provided on the J1 connector. Tables 4 through 7 show pinouts for I/O and power connections.

Table 4a. Setpoint Output Connections (J1):

Setpoint	Connections
SP-1	B1 B2
SP-2	A1 A2
SP-3	B4 B5
SP-4	A4 A5

Table 4b. RS-232-C Connections (J1)

Signal	Connection
TXD	B21
RXD	B20
CTS	B18
RTS	B19
DTR	A16
GND	B16
+5V dc	A6

Table 5. AC Power Supply Connections (TB2)

Signal	Connection
GROUND	TB2-1
115/230/100V AC Hot	TB2-2
110/230/100V AC Neutral	TB2-3

Table 6. DC Power Connections (TB2)

Signal	Connection
+5V dc	TB1-1
+9 to +36V dc	TB2-2
GROUND	TB2-3

Table 7. Input Connections (TB1)

Signal	Connection
CURRENT SOURCE	TB1-1
RTD +	TB1-2
RTD −	TB1-3
GROUND	TB1-4

10

PM-5060 MECHANICAL DIMENSIONS

The PM-5060 fits into standard 1/8 DIN panel cutouts. Mounting procedures involve tightening two screws through a metal bracket against the front panel. Figure 3 shows the mechanical dimensions of the monitor.

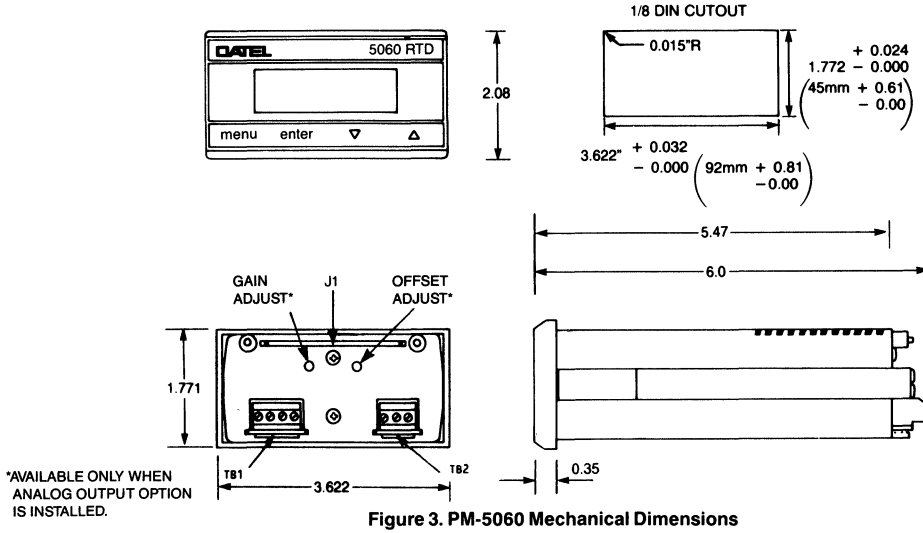


Figure 3. PM-5060 Mechanical Dimensions

ORDERING INFORMATION

PM-50X0- 1 ___ ___ 0 ___

Thermocouple 5
RTD/Thermistor 6
*Strain Gage 7
Voltage/Current 8

POWER SUPPLY
A = 110 VAC
E = 230 VAC
J = 100 VAC
D = 5V dc or +9 to +36V dc

ANALOG OUTPUT
0 = No analog ouput
1 = One analog output, 4 - to - 20mA or 0 to 10V

COMMUNICATIONS MODE
0 = RS-232-C
1 = 20mA current loop*
2 = RS-422/485*

SETPOINTS
1 = 4 setpoint outputs (standard) (100mA, 300V)

*TO BE ANNOUNCED

PM-5070
STRAIN GAGE INPUT INTELLIGENT PROCESS MONITOR/CONTROLLER

FEATURES

- **Two bipolar signal inputs plus a precision excitation output for strain gage and other bridge-type applications**
- **Four MOFSET setpoint outputs (300V/100 mA load) and optional analog output for control applications**
- **72 Commands to set control schemes, transmit data, perform bridge calibration and scaling, set communications protocol, and initiate diagnostic routines**
- **Microprocessor-based, with all operating parameters set through the front panel (or remote host) and stored internally in non-volatile EEPROM memory**
- **Easy-to-use scaling function converts bridge output to engineering units for display**
- **Two powerful math functions permit sophisticated input manipulation and advanced control algorithms**
- **Cyclical 5-digit display of up to eight system variables, including input PEAKS and VALLEYS**
- **Displays standard or user-defined engineering units**
- **Stand-alone, or operation via standard RS-232-C communication interface (RS-485 optional)**

- **Interfaces easily with serial-input printers, or logs data directly to computer disk via the serial communications port**
- **Adjustable sample rate with optional averaging**
- **Security feature prevents front panel tampering**
- **Screw terminal connectors for easy power and signal connections**
- **Menu-driven calibration procedure requires no potentiometer adjustments; continuous automatic gain and offset calibration**
- **Compact 1/8 DIN case fits standard panel cutouts**

DATEL's PM-5070 provides all the functions necessary for precision bridge measurement, including excitation output, input scaling, and the toughness to withstand harsh industrial enviroments. The PM-5070 goes beyond simple measurement. With two signal inputs, four setpoint outputs, optional analog output, and two powerful math functions, the PM-5070 is equipped to handle even demanding control applications. When combined with a host computer the PM-5070 forms a full-function operator station for real-time process monitoring and control, data archiving, and statistical analysis--all at a fraction of the cost of large dedicated systems.

GENERAL DESCRIPTION

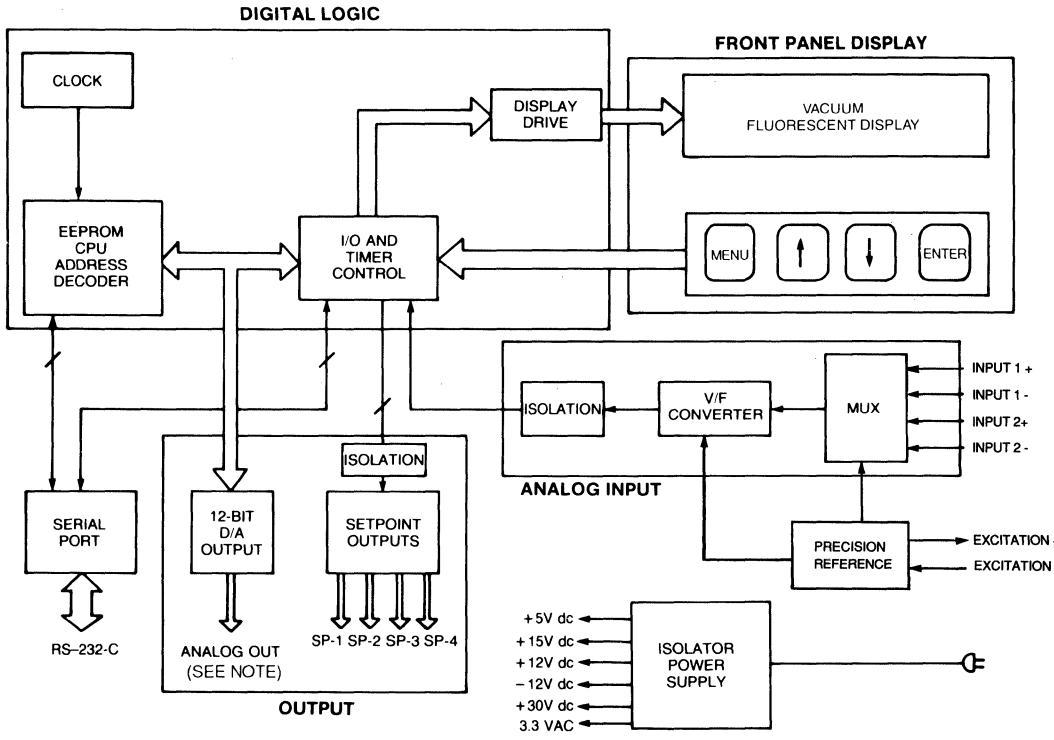
The PM-5070 consists of six functional sections: an isolated analog input section excitation circuit, microprocessor and control logic, front panel keyboard and display, serial communciations port, and setpoint outputs. A seventh section, analog output, is optional. Figure 1 is the block diagram of the PM-5070.

The isolated analog input section consists of multiplexing circuitry, signal conditioning pre-amplifiers, and a voltage-to-frequency converter. The multiplexing circuitry arbitrates between the two signal inputs. Both input channels are true differential, with INPUT 1 offering a ±50 mV full-scale range and INPUT 2 providing ±10 V. Typically, INPUT 1 is used for the bridge input, while INPUT 2, operating ratiometrically, is used as the excitation reference input. For applications requiring only a single input, multiplexing may be disabled and faster sample rates obtained. The single channel sample rate can be set to 100 ms, 200 ms, 300 ms, or 400 ms; multiplexed rates are 200 ms, 400 ms, 600 ms, or 800 ms.

The analog input section is isolated up to 1500V RMS from the control logic and power lines. A common mode rejection ratio of 140 dB ensures accurate readings in the presence of environmental noise and ground loops. Typical accuracy is 0.01% over the full-scale range.

The excitation circuit utilizes a precision reference coupled with an amplifier to generate a +10 V excitation output. The output can drive up to a 30 mA, more than enough for bridge excitation or to power other types of external sensor circuitry.

The microprocessor and control logic provide the system timing used to convert the V/F output to an equivalent digital value. This section also processes commands received via both the front panel and the RS-232 serial communication port. The microprocessor accesses operating software contained in PROM memory, while user-defined operating parameters are stored in EEPROM and are automatically retrieved on power-up.



NOTE: The optional analog output is user-configurable for 4-to-20 mA or 0 to +10V dc.

Figure 1. PM-5070 Block Diagram

A major feature of the PM-5070 is the easy-to-use front panel keypad. During set-up and parameter selection, the MENU and ENTER keys are used to traverse a hierarchical menu structure which prompts the user for operating parameter values. The two arrow keys are used to scroll through the choices for a particular parameter, or in some cases, to ramp a numeric value to the required setting. If desired, the keypad can be disabled and operating parameters entered through the serial port using simple ASCII commands.

During set-up, the six-character alphanumeric display presents menu choices and parameters using easy to remember mnemonics. During operation, the readout displays up to five digits of numeric data plus engineering units. The display also features six annunciators: four for indicating setpoint status and two for calibration parameters (full-scale and zero). Another unique feature is the ability to alternately display up to eight system variables. When used in this mode, each of the selected variables displays for approximately two seconds.

The PM-5070's RS-232-C communication port connects directly to any host computer with similar interface (e.g. IBM PC/XT/AT or compatible). Commands and parameters can be read/set at the host computer. In addition, data can be sent from the PM-5070 to the host for storage and analysis. The port is full duplex with handshake, and can be configured as DTE or DCE. The port supports baud rates ranging from 110 to 9,600 baud, one or two stop bits, and odd, even, or no parity.

The PM-5070 provides four opto-isolated setpoint outputs which respond to user-defined setpoint limits. A setpoint can be associated with any of the eight system variables (INPUT 1, INPUT 2, PEAK 1, PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, or FUNCTION 2). Further, each setpoint is assigned a trip direction (high-or low-going) and a hysterisis (deadband) value. The setpoint outputs are fully isolated MOSFET relays able to drive 100 mA/ 300V loads. The outputs can be used in to trip alarm systems or in discrete control applications .

The PM-5070's optional analog output section consists of a precision 12-bit D/A converter which is user-configured to output either 0-10V or 4-20 mA. The output value can be set through the serial port or controlled proportionally by either INPUT 1, INPUT 2, FUNCTION 1, or FUNCTION 2. Controlling the output with a function allows implementing sophisticated control algorithms such as PI and PD.

FUNCTIONAL SPECIFICATIONS
(Typical at 25 °C, 300ms conversion rate unless noted)

ANALOG INPUTS

Conversion Technique.... Voltage-to-Frequency
V/F Resolution..... 30,000 counts
Input 1 Range..... ±50 mV
Input 2 Range..... ±10V
Input 1 Accuracy..... 0.01% of full-scale
Input 2 Accuracy..... 0.01% of full-scale
Conversion Time..... User-selectable: 100 ms,200 ms, 300 ms, 400 ms (single channel)
Range Tempco..... ± 20 ppm/ °C typical
± 50 ppm/ °C maximum
Stability..... Automatic gain and offset calibration every minute
Input 1 Impedance..... 100 M ohms
Input 2 Impedance..... 100 K ohms
Common Mode Voltage... 1400 VAC peak @ 50 - 60 Hz
Common Mode Rejection 140 dB to 100 Hz
Normal Mode Rejection... 80 dB min @ 50 - 60 Hz
Over Voltage Protection 130V RMS maximum

EXCITATION

Voltage..... +10V dc
Load Current..... 30 mA max
Accuracy..... ±1.0%

DISPLAY

Type..... 14-segment, alphanumeric, blue-green vacuum flourescent
Number of Characters.... 6 alphanumeric (5 digits plus engineering units)
Character Height..... 0.38"
Annunciators..... 4 setpoint status indicators; zero and full-scale indicators
Variables Displayed..... 1 to 8 variables displayed alternately at 2 second intervals (INPUT 1, INPUT 2, PEAK 1, PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, FUNCTION 2)

SETPOINT OUTPUTS

Number..... 4
Control Source..... INPUT 1, INPUT 2, PEAK 1, PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, FUNCTION 2, or serial port
Trip Direction..... User-programmed as high- or low-going
Hysterisis Range..... 0 - 100%
Output Type..... Opto-isolated MOSFET
Isolation..... 1500VRMS
ON Resistance..... 25 Ohm
Output Rating..... 300V, 100 mA continuous

SERIAL COMMUNICATIONS

Protocol..... RS-232-C, full duplex (standard)RS-485/422 (optional)
Baud Rate..... User-programmable: 110 - 9600 Baud
Data Bits..... 7 or 8
Stop Bits..... 1 or 2
Parity..... Even, odd, or none

ANALOG OUTPUT (OPTION)

Control Source..... INPUT 1, INPUT 2, FUNCTION 1, FUNCTION 2, or serial port
Mode..... User-configured: voltage or current

Voltage:
Range..... 0 - 10V (2 mA max)
D/A Resolution..... 12 bits
Non-linearity..... ±0.1%
Gain Tempco..... 0.1 mV/ °C
Offset Tempco..... 20 ppm/ °C

Current:
Range..... 4 - 20 mA
Compatibility..... ISA type U
Excitation..... Internal or external
Accuracy ..... 0.1% of full-scale range
Load Resistance..... 100 Ohm, minimum; 1000 Ohm, maximum

PHYSICAL

Case Material..... High-impact, flame retardant polycarbonate
Case Dimensions..... 1/8 DIN cutout:
Width: 3.622" (92 mm)
Height: 1.772" (45 mm)
Depth: 5.47" (138 mm) w/o terminals
6.00" (148mm) w/terminals
Bezel Dimensions..... Depth: 0.35" (9 mm)
Width: 3.96" (101 mm)
Height: 2.08" (53 mm)
Front Panel Keypad..... Membrane with 4 key switches
Weight..... 1.32 lb (0.6 Kg)
Power..... 90 - 110 VAC, 50 Hz (PM-5070-1XX0J)
104 - 126 VAC, 60 Hz (PM-5070-1XX0A)
207 - 253 VAC, 50 Hz (PM-5070-1XX0E)
2.5 Watts typical, 4 Watts maximum

ENVIRONMENTAL

Operating Temperature Range
Rated Accuracy..... 32 to 140 °F (0 to +60 °C)
Reduced Accuracy.. 5 to 158 °F (-15 to +70 °C)
Storage Temp. Range..... -91 to 185 °F (-40 to +85 °C)
Relative Humidity..... 0 to 90% non-condensing

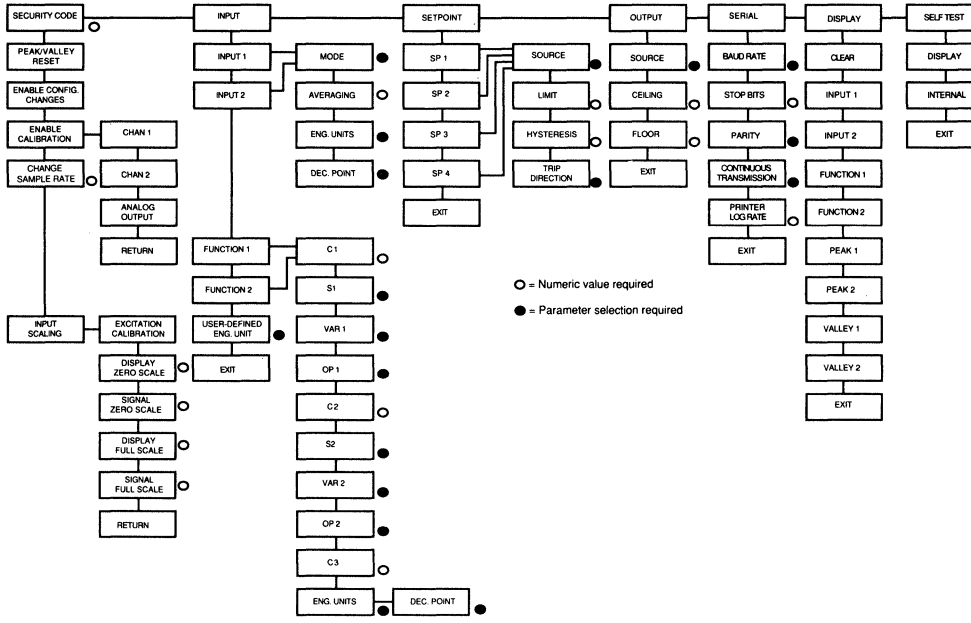


Figure 2: PM-5070 Menu Flow Chart

PM-5070 MENU

The PM-5070's powerful software provides capabilities and flexibility unmatched by conventional panel instruments. The 72 built-in software commands:

- Specify data acquisition and display parameters
- Define input scaling
- Define setpoint and analog output characteristics
- Create custom math functions
- Configure the serial communication protocol
- Specify data transmission parameters
- Let the user calibrate and diagnose the unit

Commands are issued and parameters entered in one of two ways: either directly at the monitor using the four front-panel buttons, or at a host computer connected to the meter through the serial communications port.

When configuring the PM-5070 from the front panel, the MENU and ENTER keys are used to scan a hierarchical menu structure. Menu items display as easy-to-understand mnemonics (or entire words) on the alphanumeric readout. At the uppermost menu level there are seven menu items: SECURITY CODE, INPUT, SETPOINT, OUTPUT (if the analog output option is installed), SERIAL, DISPLAY, and SELFTEST. Each major menu contains submenus, and each submenu presents the parameters needed to complete the configuration. Figure 2 depicts the menu structure.

Security Code Menu
Upon entering this menu the user is immediately prompted to enter one of five security codes. The codes, when correctly entered, allow the user to:

- Reset peak, valley, and math function variables
- Change operating parameters
- Calibrate the meter
- Set the sampling rate
- Specify input scaling parameters

Input Menu
Using this menu, the user identifies the nature of each input signal and defines how the value of the signal will appear. Specified parameters include:

- Input is enabled/disabled
- Input is scaled/used ratiometrically
- Sample averaging (1 to 10)
- Engineering units displayed
- Decimal point location

The INPUT menu also gives the user the opportunity to define one or two custom math functions to manipulate system variables for display or control output.

Setpoint Menu
This menu allows the user to define, in turn, each of the four available setpoint outputs. For each setpoint the user specifies:

- The source which controls the output (INPUT 1, INPUT 2 PEAK 1, PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, or FUNCTION 2)
- Setpoint limit
- Hysterisis
- Trip direction

Output Menu
This menu is only available when the analog output option is installed. When available, the menu allows the user to define:

- The source which controls the output (either INPUT 1, INPUT 2, FUNCTION 1, or FUNCTION 2)
- The zero and full-scale limits of the controlling source

Serial Menu
Using this menu the user defines the protocol used in communications through the serial port. Parameters specified include:

- Baud rate (110 to 9,600)
- Number of stop bits
- Odd, even, or no parity
- Meter ID number (required for multidrop applications)
- Transmission rate for logging data to a printer

Display Menu
With this menu the user specifies which of the eight system variables are to be displayed alternately at two second intervals.

Selftest Menu
This menu provides access to a series of diagnostic tests which verify the integrity of the display segments and the meter's internal circuitry.

MATH FUNCTIONS

One of the most powerful features of the PM-5070 are the two user-configurable math functions. The two functions have the generalized form:

[[(C1 x S1) x VAR1] OP1 [(C2 x S2) x VAR2]] OP2 (C3)

Where:
C1, C2, C3 = numeric constants
S1, S2 = scaling factors
VAR1, VAR2 = any one of the eight system variables
OP1, OP2 = an arithmetic operator: +, -,x, /

The constants, scale factors, variables, and operators constituting the function are specified either from the front panel (within the INPUT menu), or from a host computer connected through the serial port.

During operation, the value of a function is calculated at the monitor's sample rate. This value can be displayed and/or used to control setpoint or analog outputs. Because of their flexibility, the two functions may be used in a variety of ways: for engineering units scaling, as control algorithms, or for combining inputs to calculate other physical process variables.

SERIAL COMMUNICATIONS

A standard feature of the PM-5070 is an RS-232-C serial communications port. Using this port, the PM-5070 can be connected to a host computer or PLC having a similar interface. Any configuration parameter which can be set using the meter's front panel can alternatively be set by issuing a simple ASCII command from the host computer. Additionally, the host can read the current meter status, log data, and directly control the setpoint and analog outputs.

PM-5070 commands all conform to a simple ASCII format and can be incorporated into any structured language program. As an example, the command to change the trip limit of setpoint number 4 to 500 is: WSP 4,500

TYPICAL STRAIN GAGE INTERFACE

Figure 3 illustrates a typical strain gage interface. The bridge output is connected to the PM-5070's INPUT 1 connections, while INPUT 2 is used to measure the excitation voltage. In this configuration INPUT 2 is used ratiometrically, meaning that the monitor will adjust the INPUT 1 reading to compensate for any variations in the excitation source. Ratiometric operation is specified through the front panel or with a serial port command.

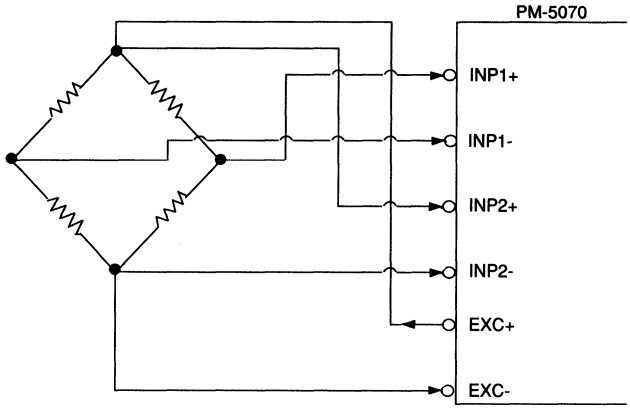
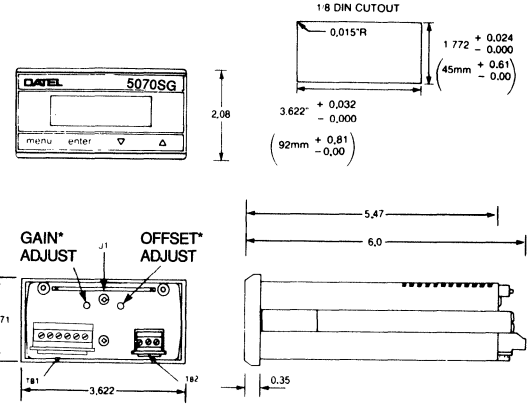
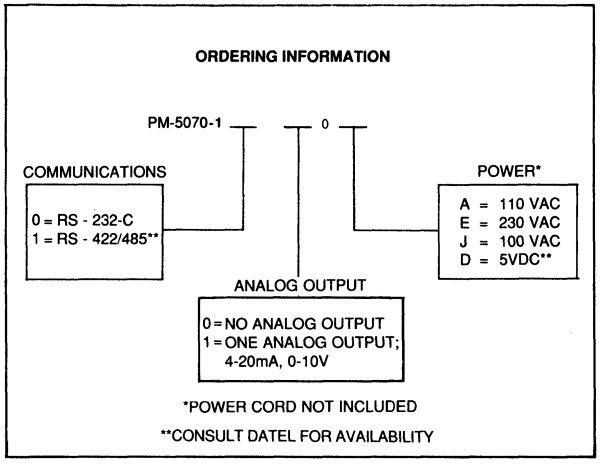


Figure 3. Strain Gage Interface



NOTE: GAIN AND OFFSET ADJUSTMENT POTENTIOMETERS ARE AVAILABLE ONLY ON MODELS HAVING THE ANALOG OUTPUT OPTION.

Figure 4. Mechanical Dimensions



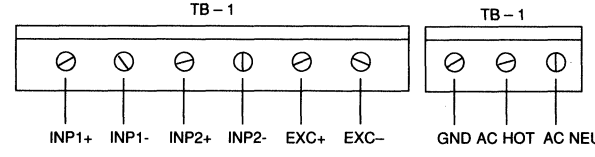


Figure 5: Signal/Power Connections

WARRANTY

DATEL warrants this product to be free from defects in material and workmanship under normal use and service for a period of one year from the date of shipment. DATEL's obligations under this warranty are limited to replacing or repairing the unit, at its option, at its factory or facility, when the unit is returned to DATEL's facility, transportation charges prepaid, and which is after examination disclosed to the satisfaction of DATEL to be thus defective. This warranty shall not apply to any such equipment which shall have been repaired or altered except by DATEL or which shall have been subjected to misuse, negligence, or accident. In no case shall DATEL's liability exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by DATEL.

NOTE: Equipment sold by DATEL, Inc. is not intended to be used, nor shall it be used, as a "Basic Component" under 10 CFR 21 (NRC).

Should this equipment be used in or with any nuclear installation or activity, the Purchaser will indemnify Datel, Inc. and hold Datel, Inc. harmless from any liability or damage whatsoever arising out of the use of the equipment in such a manner.

PM-5080
VOLTAGE/CURRENT INPUT INTELLIGENT PROCESS MONITOR/CONTROLLER

FEATURES

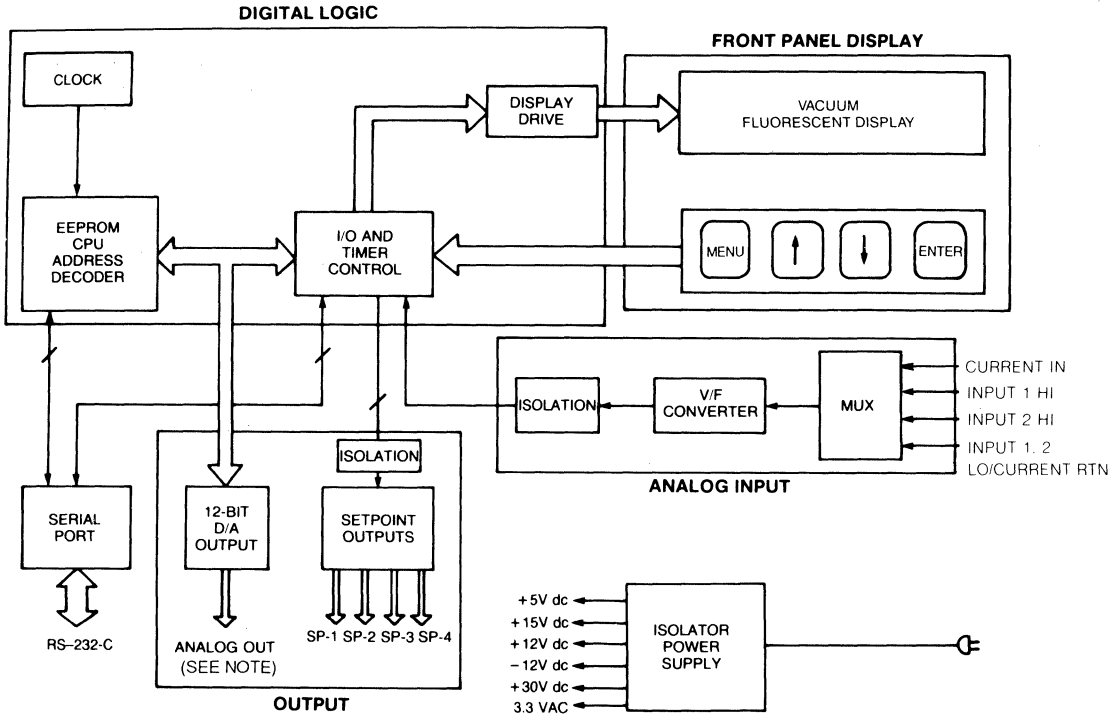
- **Two signal inputs, four MOSFET setpoint outputs (300V/100 mA load) and one analog output for control applications (optional)**
- **72 Commands to set control schemes, transmit data, perform calibration and scaling, set communications protocol, and initiate diagnostic routines**
- **Microprocessor-based, with all operating parameters set through the front panel (or remote host) and stored internally in non-volatile EEPROM memory**
- **Easy-to-use input scaling function**
- **Two powerful math functions permit sophisticated input manipulation and advanced control algorithms**
- **Cyclical 5-digit display of up to eight system variables, including input PEAKS and VALLEYS**
- **Displays standard or user-defined engineering units**
- **Stand-alone, or operation via standard RS-232-C communication interface (RS-485 optional)**
- **Interfaces easily with serial-input printers, or logs data directly to computer disk via the communications port**
- **Adjustable sample rate with optional averaging**
- **Security feature prevents front panel tampering**
- **Screw terminal connectors for easy power and signal connections**
- **Menu-driven calibration procedure requires no potentiometer adjustments; continuous automatic gain and offset calibration**
- **Compact 1/8 DIN case fits standard panel cutout**

DATEL's PM-5080 Intelligent Process Monitor represents a new generation of microprocessor-based, panel-mounted instrumentation. The PM-5080 offers two voltage/current signal inputs, four programmable setpoint outputs, and an optional analog output. Powerful user-defined math functions make the PM-5080 easily adapted to a wide variety of process monitoring and control applications. When combined with a host computer, the PM-5080 forms a full-function operator station for real-time process monitoring and control, data archiving, and statistical analysis — all at a fraction of the cost of large dedicated systems.

GENERAL DESCRIPTION

The PM-5080 consists of five functional sections: an isolated analog input section, microprocessor and control logic, front panel keyboard and display, serial communciations port, and setpoint outputs. A sixth section, analog output, is optional. Figure 1 is the block diagram of the PM-5080.

The isolated analog input section consists of multiplexing circuitry, signal conditioning pre-amplifiers, and a voltage-to-frequency converter. The multiplexing circuitry gives the user a choice of two input pair combinations: one 0-100 mV input and one 0-10V input, or one 0-20 mA current input and one 0-10V input. For applications requiring only a single input, multiplexing may be disabled and faster sample rates obtained. The single channel sample rate can be set to 100 ms, 200 ms, 300 ms, or 400 ms; multiplexed rates are 200 ms, 400 ms, 600 ms, or 800 ms.



NOTE: The optional analog output is user-configurable for 4-to-20 mA or 0 to +10V dc.

Figure 1. PM-5080 Block Diagram

The analog input section is isolated up to 1500V RMS from the control logic and power lines. A common mode rejection ratio of 140dB ensures accurate readings in the presence of environmental noise and ground loops.

The microprocessor and control logic provide the system timing used to convert the V/F output to an equivalent via both the front panel and the RS-232-C serial communication port. The microprocessor accesses operating software contained in PROM memory, while user-defined operating parameters are stored in EEPROM and are automatically retrieved on powerup.

A major feature of the PM-5080 is the easy-to-use front panel keypad. During set-up and parameter selection, the MENU and ENTER keys are used to traverse a hierarchical menu structure which prompts the user for operating parameter values. The two arrow keys are used to scroll through the choices for a particular parameter, or in some cases, to ramp a numeric value to the required setting. If desired, the keypad can be disabled and operating parameters entered through the serial port using simple ASCII commands.

During set-up, the six-character alphanumeric display presents menu choices and parameters using easy-to-remember mnemonics. During operation, the readout displays up to five digits of numeric data plus engineering units. The display also features six annunciators: four for indicating setpoint status and two for calibration parameters (full-scale and zero). Another unique feature is the ability to alternately display up to eight system variables. When used in this mode, each of the selected variables displays for approximately two seconds.

The PM-5080's RS-232-C communication port connects directly to any host computer with similar interface (e.g. IBM PC/XT/AT or compatible). Commands and parameters can be read/set at the host computer. In addition, data can be sent from the PM-5080 to the host for storage and analysis. The port is full duplex with handshake, and can be configured as DTE or DCE. The port supports baud rates ranging from 110 to 9,600 baud, one or twostop bits, and odd, even, or no parity.

The PM-5080 provides four opto-isolated setpoint outputs which respond to user-defined setpoint limits. A setpoint can be associated with any of the eight system variables (INPUT 1, INPUT 2, PEAK 1, PEAK 2, VALLEY 1, VALLEY 2 FUNCTION 1 or FUNCTION 2). Further each setpoint is assigned a trip direction (high or low going) and a hysterisis (deadband) value. The setpoint outputs are fully isolated MOSFET relays able to drive 100mA/300V loads. The outputs can be used to trip alarm systems or in discrete control applications.

The PM-5080's optional analog output section consists of a precision 12-bit D/A converter which is user-configured to output either 0-10V or 4-20 mA. The output value can be set through the serial port or controlled proportionally by either INPUT 1, INPUT 2, FUNCTION 1, or FUNCTION 2. Controlling the output with a function allows implementing sophisticated control algorithms such as PI and PD.

FUNCTIONAL SPECIFICATIONS
(Typical at 25 °C, 300 mS conversion rate unless noted)

ANALOG INPUTS

Conversion Technique..... Voltage-to-Frequency
V/F Resolution..... 30,000 counts
Input 1 Range..... 0 - 100 mV or 0 - 20 mA
Input 2 Range..... 0 - 10V
Input 1 Accuracy (V)..... 0.01% of full-scale
Input 1 Accuracy (I)..... 0.05% of full-scale
Input 2 Accuracy..... 0.01% of full-scale
Conversion Time..... User-selectable: 100 ms, 200 ms, 300 ms, 400 ms
Range Tempco..... ± 20 ppm/ °C typical
± 50 ppm/ °C maximum
Stability..... Automatic gain and offset calibration every minute
Input 1 Impedance..... 100 M Ohms
Input 2 Impedance..... 1 M Ohms
Common Mode Voltage..... 1400 VAC peak @ 50 - 60 Hz
Common Mode Rejection.... 140 dB to 100 Hz
Normal Mode Rejection..... 80 dB min @ 50 - 60 Hz
Over Voltage Protection.... 130V RMS maximum

DISPLAY

Type..... 14-segment, alpha numeric, blue-green vacuum flouresecent
Number of Characters..... 6 alphanumeric (5 digits plus engineering units)
Character Height..... 0.38"
Annunciators..... 4 setpoint status indicators; zero and full-scale indicators
Variables Displayed..... 1 to 8 variables displayed alternately at 2 second intervals (INPUT 1, INPUT 2, PEAK 1, PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, FUNCTION 2)

SETPOINT OUTPUTS

Number..... 4
Control Source..... INPUT 1, INPUT 2, PEAK 1 PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, FUNCTION 2, or serial port
Trip Direction..... User-programmed as high- or low-going
Hysterisis Range..... 0 - 100%
Output Type..... Opto-isolated MOSFET
Isolation..... 1500VRMS
On Resistance..... 25 Ohm
Output Rating..... 300V, 100 mA continuous

SERIAL COMMUNICATIONS

Protocol..... RS-232-C, full duplex (standard)
RS-485/422 (optional)
Baud Rate..... User-programmable: 110-9600 Baud
Data Bits..... 7 or 8
Stop Bits..... 1 or 2
Parity..... Even, odd, or none

ANALOG OUTPUT (OPTION)

Control Source..... INPUT 1, INPUT 2, FUNCTION 1, FUNCTION 2, or serial port
Mode..... User-configured: voltage, current

Voltage:
Range..... 0 - 10V (2 mA max)
D/A Resolution..... 12 bits
Non-linearity..... ±0.1%
Gain Tempco..... 0.1 mV/ °C
Offset Tempco..... 20 ppm/ °C

Current:
Range..... 4 - 20 mA
Compatibility..... ISA type U
Excitation..... Internal or external
Accuracy ..... 0.1% of full-scale range
Load Resistance..... 100 Ohm, minimum; 1000 Ohm, maximum

PHYSICAL

Case Material..... High-impact, flame retardant polycarbonate
Case Dimensions..... 1/8 DIN cutout:
Width: 3.622" (92 mm)
Height: 1.772" (45 mm)
Depth: 5.47" (138 mm) w/o terminals; 6.00" (148mm) w/terminals
Bezel Dimensions..... Depth: 0.35" (9 mm)
Width: 3.96" (101 mm)
Height: 2.08" (53 mm)
Front Panel Keypad..... Membrane with 4 key switches
Weight..... 1.32 lb (0.6 Kg)
Power..... 90 - 110 VAC, 50 Hz (PM-5080-1XX0J)
104 - 126 VAC, 60 Hz (PM-5080-1XX0A)
207 - 253 VAC, 50 Hz (PM-5080-1XX0E)
2.5 Watts typical, 4 Watts maximum

ENVIRONMENTAL

Operating Temperature Range
Rated Accuracy..... 32 to 140 °F (0 to +60 °C)
Reduced Accuracy..... 5 to 158 °F (-15 to +70 °C)
Storage Temp. Range..... -91 to 185 °F (-40 to +85 °C)
Relative Humidity..... 0 to 90% non-condensing

10

PM-5080 MENU

The PM-5080's powerful software provides capabilities and flexibility unmatched by conventional panel instruments. The 72 built-in software commands:

- Specify data acquisition and display parameters
- Define setpoint and analog output characteristics
- Create custom math functions
- Configure the serial communication protocol
- Let the user calibrate and diagnose the unit

Commands are issued and parameters entered in one of two ways: either directly at the monitor using the four front-panel buttons, or at a host computer connected to the meter through the serial communication port.

When configuring the PM-5080 from the front panel, the MENU and ENTER keys are used to scan a hierarchical menu structure. Menu items display as easy-to-understand mnemonics (or entire words) on the alphanumeric readout.

At the uppermost menu level there are seven menu items: SECURITY CODE, INPUT, SETPOINT, OUTPUT, (if the analog output option is installed), SERIAL, DISPLAY, and SELF-TEST. Each major menu contains submenus, and each submenu presents the parameters needed to complete the configuration. Figure 2 depicts the menu structure.

Security Code Menu

Upon entering this menu the user is immediately prompted to enter one of five security codes. The codes, when correctly entered, allow the user to:

- Reset peak, valley, and math function variables
- Change operating parameters
- Calibrate the meter
- Set the sampling rate
- Specify input scaling parameters

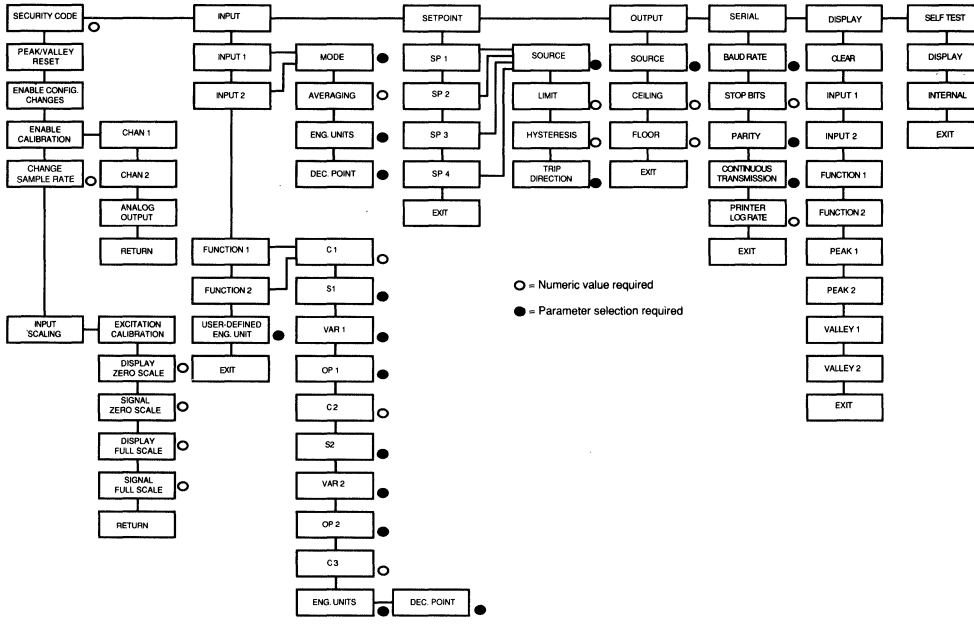


Figure 2. PM-5080 Menu Structure

Input Menu
Using this menu, the user identifies the nature of each input signal and defines how the value of the signal will appear. Specified parameters include:

- Input is enabled/disabled/scaled
- Input is voltage or current
- Sample averaging (1 to 10)
- Engineering units displayed
- Decimal point location

The INPUT menu also gives the user the opportunity to define one or two custom math functions to manipulate system variables for display or control output.

Setpoint Menu
This menu allows the user to define, in turn, each of the four available setpoint outputs. For each setpoint the user specifies:

- The source which controls the output (INPUT 1, INPUT 2 PEAK 1, PEAK 2, VALLEY 1, VALLEY 2, FUNCTION 1, or FUNCTION 2)
- Setpoint limit
- Hysterisis
- Trip direction

Output Menu
This menu is only available when the analog output option is installed. When available, the menu allows the user to define:

- The source which controls the output (either INPUT 1, INPUT 2, FUNCTION 1, or FUNCTION 2)
- The zero and full-scale limits of the controlling source

Serial Menu
Using this menu the user defines the protocol used in communications through the serial port. Parameters specified include:

- Baud rate (110 to 9,600)
- Number of stop bits
- Odd, even, or no parity
- Meter ID number (required for multidrop applications)
- Transmission rate for logging data to a printer

Display Menu
With this menu the user specifies which of the eight system variables are to be displayed alternately at two second intervals.

Selftest Menu
This menu provides access to a series of diagnostic tests which verify the integrity of the display segments and the meter's internal circuitry.

MATH FUNCTIONS

One of the most powerful features of the PM-5080 are the two user-configurable math functions. The two functions have the generalized form:

[[(C1 x S1) x VAR1] OP1 [(C2 x S2) x VAR2]] OP2 (C3)

Where:
C1, C2, C3 = numeric constants
S1, S2 = scaling factors
VAR1, VAR2 = any one of the eight system variables
OP1, OP2 = an arithmetic operator: +, -,x, /

The constants, scale factors, variables, and operators constituting the function are specified either from the front panel (within the INPUT menu), or from a host computer connected through the serial port.

During operation, the value of a function is calculated at the monitor's sample rate. This value can be displayed and/or used to control setpoint or analog outputs. Because of their flexibility, the two functions may be used in a variety of ways: for engineering units scaling, as control algorithms, or for combining inputs to calculate other physical process variables. One use of the math functions is illustrated in the application example given below.

SERIAL COMMUNICATIONS

A standard feature of the PM-5080 is an RS-232-C serial communications port. Using this port, the PM-5080 can be connected to a host computer or PLC having a similar interface. Any configuration parameter which can be set using the meter's front panel can alternatively be set by issuing a simple ASCII command from the host computer. Additionally, the host can read the meter status, log data, and directly control the setpoint and analog outputs.

PM-5080 commands all conform to a simple ASCII format and can be incorporated into any structured language program. As an example, the command to change the trip limit of setpoint number 4 to 500 is: WSP 4,500.

APPLICATION EXAMPLE

A coal burning power plant is required to monitor the amount of carbon monoxide (CO) expelled into the atmosphere. To do this, the PM-5080's dual inputs are employed. One input is connected to a flow sensor which tracks the total flow of gas through the discharge flue; the second input is connected to an in-line analyzer which measures the amount of CO in the discharge gas.

Using the PM-5080's scaling function, the flow meter's 4-20mA output is converted to 0-300 cubic feet/minute for display. One of the monitor's math functions is used to compute and display the rate at which CO is expelled into the atmosphere:

CO Discharge Rate=Total Discharge Rate x %CO in flow

FUNCTION 1 = INPUT1 x (INPUT2 x 0.1)

Formatting to the general form of the equation and scaling for display:

FUNCTION 1 = [(C1 x S1 x VAR1) OP1 (C2 x S2 x VAR2)] OP2(C3)
= [(1 x 0.1 x INPUT1) x (1 x 0.01 x INPUT2)] / 100

In this example, the function is also used to control two setpoint outputs: one setpoint trips an alarm system should the CO discharge rate rise above a preset level; the second setpoint initiates an emergency plant shutdown if the discharge level reaches an even higher preset level. If desired, the function could also be used to drive an analog output which would control the plant's burners such that CO discharge is kept below a selected setpoint limit.

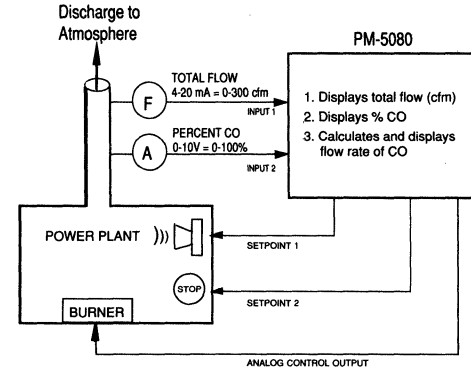
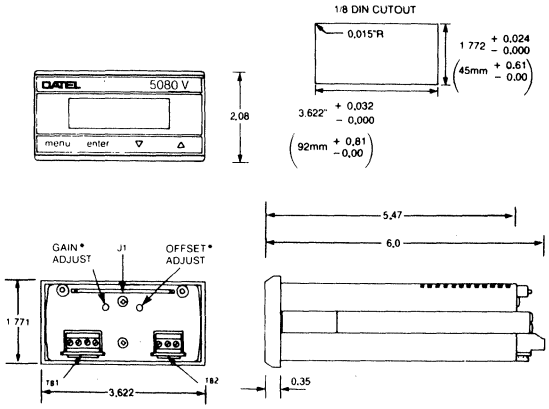


Figure 3. Application Example



NOTE: GAIN AND OFFSET ADJUSTMENT POTENTIOMETERS ARE AVAILABLE ONLY ON MODELS HAVING THE ANALOG OUTPUT OPTION.

Figure 4. Mechanical Dimensions

ORDERING INFORMATION

PM-5080-1 — 0

COMMUNICATIONS
0 = RS - 232-C
1 = RS - 422/485**

POWER*
A = 110 VAC
E = 230 VAC
J = 100 VAC
D = 5VDC**

ANALOG OUTPUT
0 = NO ANALOG OUTPUT
1 = ONE ANALOG OUTPUT; 4-20mA, 0-10V

*POWER CORD NOT INCLUDED

**CONSULT DATEL FOR AVAILABILITY

WARRANTY

DATEL warrants this product to be free from defects in material and workmanship under normal use and service for a period of one year from the date of shipment. DATEL's obligations under this warranty are limited to replacing or repairing the unit, at its option, at its factory or facility, when the unit is returned to DATEL's facility, transportation charges prepaid, and which is after examination disclosed to the satisfaction of DATEL to be thus defective. This warranty shall not apply to any such equipment which shall have been repaired or altered except by DATEL or which shall have been subjected to misuse, negligence, or accident. In no case shall DATEL's liability exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by DATEL.

NOTE: Equipment sold by DATEL, Inc. is not intended to be used, nor shall it be used as a "Basic Component" under 10 CFR 21 (NRC).

Should this equipment be used in or with any nuclear installation or activity, the Purchaser will indemnify DATEL, Inc. and hold DATEL, Inc. harmless from any liability or damage whatsoever arising out of the use of the equipment in such manner.

DVC-350A
Hand-Held, Battery-Powered Voltage Calibrator

FEATURES

- **Hand-held, lightweight 11 ounces (342 grams)**
- **Laboratory accuracy of ±0.015% of FSR at +25°C, traceable to the National Bureau of Standards**
- **4½ Digit LCD display**
- **100 μV increments**
- **Two output voltage ranges:**
  Decimal: ±1.2V dc, ±12V dc
  Hexadecimal: ±1V dc, ±10V dc
- **Up to 20 mA source or sink current capability**
- **Rated accuracy down to 6.5V dc battery level using rechargeable 7.2V battery or conventional 9V battery**
- **Right and left binary shift for hexadecimal calibration of A/D or D/A converters**
- **Convenient, easy-to-use membrane keyboard with audible feedback**
- **Finger-touch cursor control with automatic voltage increment or decrement**
- **Dual voltage output capability: absolute 0 volts (with current limiting) and entered value**
- **Automatic current limiting and low battery indication**
- **AC adapter/charger operation optional**

THE DVC-350A'S ACCURACY AND PORTABILITY MAKES IT THE CALIBRATOR-OF-CHOICE FOR PRECISE ADJUSTMENT OF ANALYZERS, RECORDERS, CONTROLLERS, DATA ACQUISITION SYSTEM COMPUTERS, AND MANY OTHER LAB AND FIELD APPLICATIONS.

INTRODUCTION

DATEL's Model DVC-350A hand-held, microprocessor-based voltage calibrator provides the user with two entry modes of operation and four output voltage ranges. The outputs have an unprecedented 0.015% accuracy, commonly found only in laboratory-type calibrators.

Complementing the DVC-350A's portability and flexibility is an outstanding array of features and the large 4½ digit LCD display. Mode of entry is switch-selectable as either decimal or hexadecimal. Decimal mode output ranges are ±1.2V dc in 100 μV increments and ±12V dc in 1 mV increments. Hexadecimal mode offers output voltage ranges of ±1V dc in 244 μV increments and ±10V dc in 2.44 mV increments.

The hexadecimal mode is notably useful for computer-oriented calibration of digital panel meters, A/D's, and data acquisition systems. It eliminates the need for tedious hexadecimal-to-decimal number conversion; the DVC-350A does it all automatically. The DVC-350A accepts and converts hexadecimal numbers up to FFF hex.

APPLICATIONS

The DVC-350A is a universal field and laboratory voltage calibrator with accuracy and stability traceable to the National Bureau of Standards.

In the lab, the DVC-350A is an ideal voltage source for engineering prototypes, breadboards, and test setups without competing with other instruments for space and AC outlets.

Size and portability, however, make the DVC-350A an outstanding field instrument. It easily fits into a coat pocket or attache case. It makes remote site calibration easy and accurate. The DVC-350A is extremely effective for calibrating A/D converters, V/F converters, DPM's and transducers (load cells, strain gages, LVDT'S, etc.).

DESCRIPTION

The DVC-350A owes its accuracy to the precision and stability of the power supply, the analog output circuitry, and its high performance, 14-bit CMOS digital-to-analog converter, characterized by its precision and lower power consumption. As shown in Figure 1, the 14-bit digital input to the DAC is routed by the 8-bit CMOS microprocessor which also takes the entered data from the keyboard and updates the 4½ digit LCD display.

The DVC-350A uses an extremely stable switching power supply. The power supply circuitry incorporates the latest power supply technology, operating with battery potentials from 20V dc down to 6.5V dc without degrading performance. The low battery indicator on the display turns on at a 6.7V dc battery potential.

The DVC-350A uses one standard 9V alkaline battery or a rechargeable Nickel-Cadmium battery. The calibrator may also operate using an optional AC adaptor/charger when a Ni-Cd battery is installed. When using an alkaline battery, remove the battery before using the adapter.

The low output impedance amplifier of the DVC-350A will source or sink up to 20 mA over the specified output voltage ranges without compromising its performance and accuracy.

The device begins current limiting at 22 mA, turning on an overload symbol on the display. At higher current loading, the calibrator's accuracy will be somewhat degraded until such time as its short-circuit protection circuit shuts down the output at 33 mA. The overload circuitry protects the calibrator from external loads lower than 480 ohms on the 12V scale or 48 ohms on the 1.2V scale.

FUNCTIONAL SPECIFICATIONS

(Typical at +25° C unless otherwise noted)

VOLTAGE OUTPUT

Ranges
Decimal . . . . . 0 to ±1.2V dc, 0 to ±12V dc
Hexadecimal . . . . . 0 to ±0.99975V dc, 0 to ±9.9975V dc (HEX = FFF)

Zero Volts Output Error . . . . +100 μV

Output Type . . . . . Low-impedance dc voltage, current limited.

Current Capability . . . . . Output will sink or source 20 mA maximum over the full scale ranges.

Output Overload . . . . . Greater than +20 mA current will turn on the overload indicator and output accuracy will degrade.

Output Impedance . . . . . 30 milliohms.

Capacitive Load . . . . . No limitation.

Output Connector Type . . . . Two banana-type jacks, 0.75″ spacing on centers.

OUTPUT PROTECTION

Current . . . . . 33 mA short circuit-proof (Will shut down at this point)

Voltage . . . . . 15V (dc or AC peak-to-peak) maximum (Damage to output circuitry might result when exceeding this value).

Output Settling Time . . . . . 5 seconds to rated accuracy, 2 seconds to 99% of final output.

PERFORMANCE

Accuracy . . . . . Within ±0.015% of full scale

Resolution . . . . . 12V scale; 1 mV increment
1.2V scale; 100 μV increment
10V scale; 2.44 mV increment
1V scale; 244 μV increment

Temperature Drift of Zero
(12V scale) . . . . . within ±10 μV/°C
(1.2V scale) . . . . . within ±1 μV/°C

Temperature Drift of Calibration
(+15°C to +35°C) . . . . . ±10ppm of setting/°C
(0°C to +50°C) . . . . . ±15ppm of setting/°C

Operating Temperature Range . . . . . 0°C to +50°C

Storage Temperature Range . . . . . −25°C to +85°C

Output Noise . . . . . 150 μV peak-to-peak, wideband (12V dc scale)

POWER REQUIREMENTS

Supply Battery Voltage Range . . . . 20V dc to 6.5V dc (no effect on performance)

Supply Current . . . . . 20mA (no load) at +9V dc

Battery Type . . . . . 9V alkaline or Ni-Cd

Battery Life (GC9B NiCd) (before requiring recharging)	Min.*	Typ.	Units
	1.0	4	hours

* 12V at 20 mA output would require an input current of 55 mA at 9V.

PHYSICAL DIMENSIONS

Size . . . . . 5.75″L × 3.6″W × 1.29″H
146 × 91 × 33mm

Weight . . . . . 11 ounces (342 grams)

Case . . . . . ABS plastic

Keyboard Life . . . . . 10 million cycles per switch (minimum)

Key Operating Force . . . . . 4 to 8 ounces, 124 to 248 grams

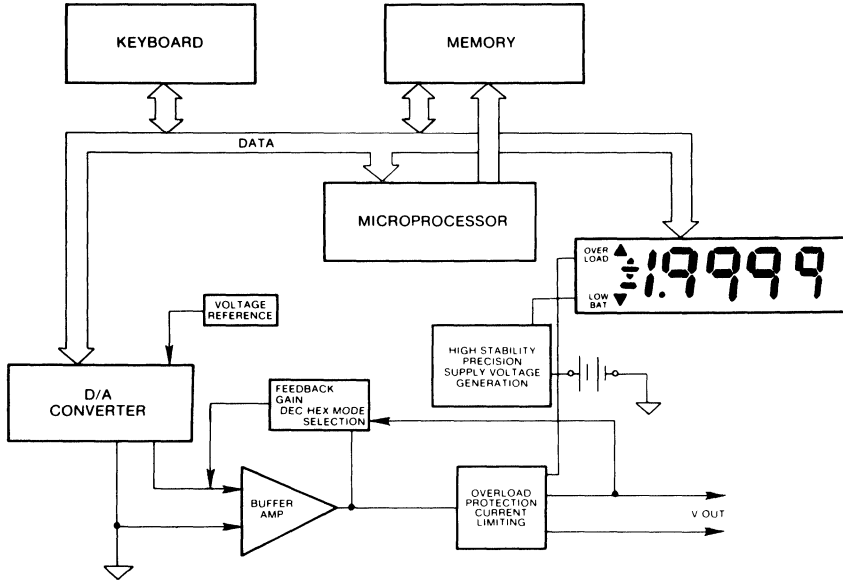


Figure 1. DVC-350A Block Diagram

SWITCHES AND INDICATORS
(Refer to Figure 2)

Power, output polarity, range, and decimal/hexadecimal mode switches are located above the keypad; each is clearly labeled. Decimal and hexadecimal mode selection is switch-selectable.

The three-position polarity switch on the keyboard allows "+" or "−" polarity output selection as well as 0V dc output indicated by the alternately flashing "+" and "−" sign.

An oscillating polarity sign (between + and −) indicates that the calibrator is producing a 0 volt output. In this mode, the display still reads the last keyboard entry which becomes an output when the switch moves from the center position to the left (−) or right (+).

KEYBOARD
(Refer to Figure 2)

The DVC-350A's touch-sensitive membrane keyboard consists of 24 decimal, hexadecimal, and function keys. A minimum force of 4 ounces activates the keys. An internal buzzer provides audible feedback for all keypad entries (except the increment and decrement key).

Cursor left/right keys
The cursor keys move the cursor left and right to select the desired digit to be incremented or decremented by the increment/decrement keys. The cursor is not visible on the display and the user must use the increment/decrement keys to find the cursor position. The device provides an audible feedback when using the cursor left/right keys until the cursor position is at either end of the display.

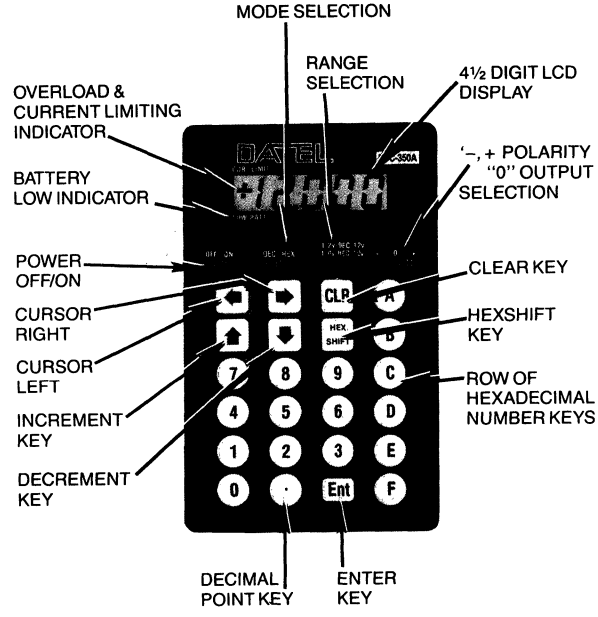


Figure 2. Keys, Indicators, Switches

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Increment/decrement keys

These keys allow the user to increase or decrease the value in a display position by one unit. The change is immediately present on the output. These keys are always active.

Alpha keys

The A, B, C, D, E, F keys are only used in the hexadecimal mode and are combined with numeric keys to create a valid hexadecimal entry. Figures 3 and 4 clarify how the device converts decimal numbers to hexadecimal numbers while Table 1 lists equivalent voltage outputs for displayed hexadecimal values.

Numeric keys

The numeric keys allow entering decimal values within the decimal and hexadecimal ranges. Out-of-range values result in a 'bad entry' indication.

Decimal point key

This key is used to enter a decimal point when in decimal mode.

Clear entry key

Pressing this key while in the decimal and hexadecimal modes clears the keyboard entry and the display.

Enter key

Pressing the ENTER key permits the newly-entered decimal value to appear at the output connectors of the calibrator. This key must be used when entering a decimal number from the keyboard. The ENTER key does not need to be pressed when using the increment and decrement keys, since the output of the calibrator changes automatically with the use of these keys.

Hex shift key

Pressing the HEX SHIFT key changes the function of the increment/decrement keys. After enabling this function, the increment key multiplies the displayed hexadecimal value by 2 and the decrement key divides the entered hexadecimal value by 2. A second depression of the HEX SHIFT key disables the function. The display shows 4 decimal points to indicate that the HEX SHIFT function is active. This key is only valid in the hex operation mode.

DISPLAY

The DVC-350A uses a 4½ digit liquid crystal display with indication of current limit and low battery conditions. Sourcing or draining more than 22 mA turns on the current limit indicator in the upper left corner, indicating an automatic current limiting and overload condition.

When battery potential is lower than 6.5V dc, the low battery indicator in the lower left corner turns on.

Invalid entries, in both modes, turn on the "bAdE" (bad entry) message, displaying it for about 3 seconds before returning to the last valid entry.

When in Hexadecimal mode with HEX SHIFT enabled, attempting to multiply a zero display by 2 results in a display of '1' in the LSB position since the microprocessor automatically shifts left. This action is graphically shown in Figure 5.

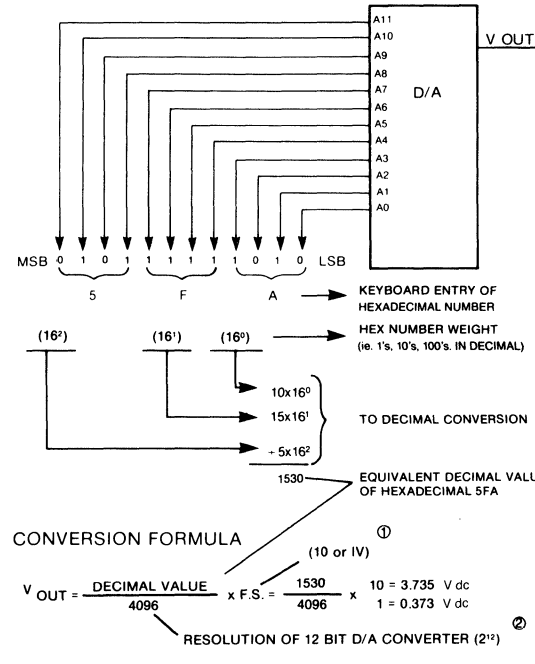
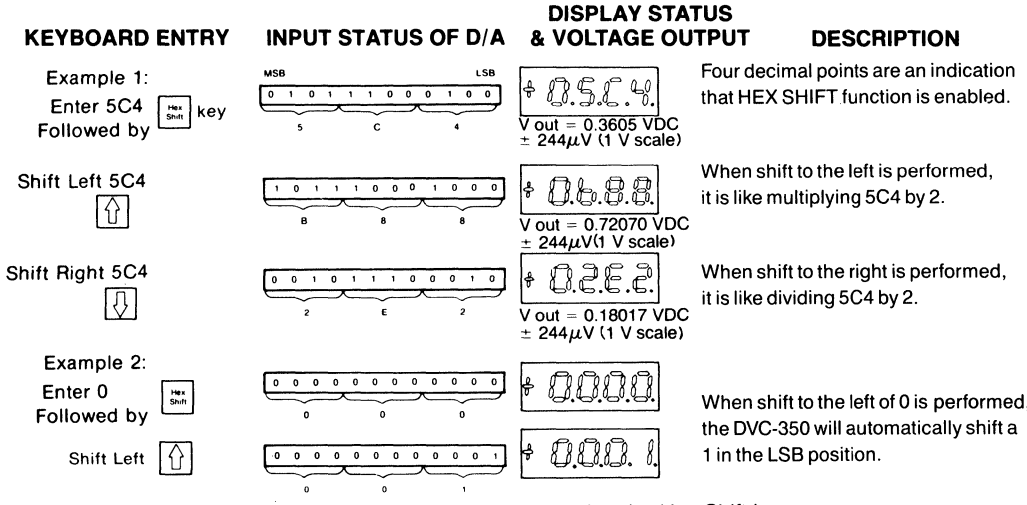


Figure 3. Hexadecimal Mode Operation

DECIMAL	BINARY	HEXADECIMAL
0	0 0 0 0	0
1	0 0 0 1	1
2	0 0 1 0	2
3	0 0 1 1	3
4	0 1 0 0	4
5	0 1 0 1	5
6	0 1 1 0	6
7	0 1 1 1	7
8	1 0 0 0	8
9	1 0 0 1	9
10	1 0 1 0	A
11	1 0 1 1	B
12	1 1 0 0	C
13	1 1 0 1	D
14	1 1 1 0	E
15	1 1 1 1	F

Note: In hexadecimal, B and D are displayed as lower case, b and d respectively. Note the difference between letter (b) and the numeral (6).

Figure 4. Decimal, Binary, Hexadecimal Chart



Hex Shift function is activated by pressing the Hex Shift key.
When Hex Shift key is pressed the 2nd time the user is out of the Hex Shift Mode.

Figure 5. HEX SHIFT Key Operation

Table 1. DVC-350A Coding Table

DISPLAYED HEXADECIMAL VALUES	DECIMAL VOLTAGE OUTPUT EQUIVALENT	
	10 VDC SCALE	1 VDC SCALE
FFF	9.9975	.99975
•		
•		
•		
800	5.0000	.50000
•		
•		
•		
400	2.5000	.25000
•		
•		
•		
100	0.6250	.06250
•		
•		
•		
010	0.0390	.00390
•		
•		
•		
002	0.00488	.00048
001	0.00244	.00024
000	0.00000	.00000

EXAMPLES OF DVC-350A ENTRY

Decimal Mode

Power: On
Mode: DEC (decimal)
Range: 12V dc,
Polarity: +
Enter: 9.354

Press the decimal number and decimal point keys, reading from left to right, followed by the ENTER key. The display will indicate a value of +9.354 and an analog voltage of +9.354V dc will be present at the output of the unit.

Hexadecimal Mode

Power: On
Mode: HEX (hexadecimal)
Range: 10V dc
Polarity: +
Enter: 1FA

Follow the same procedure described in the earlier example with the addition of using the hexadecimal ALPHA keys. After pressing the ENTER key, the display will read 1FA with a corresponding output voltage of +1.235V dc. The DVC-350A automatically converts the hexadecimal number entry into a decimal equivalent voltage output (see the conversion formula presented in Figure 3).

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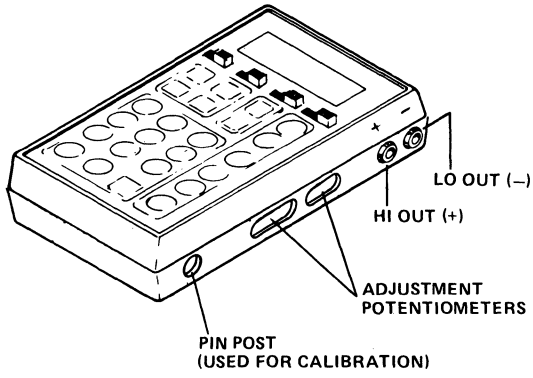

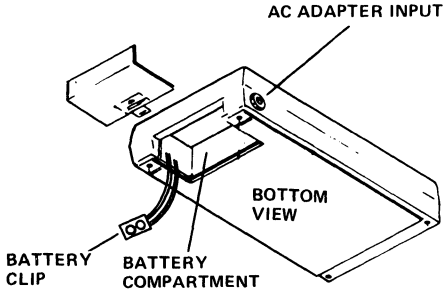

Figure 6. Terminals and Battery Locations

HOUSING AND MECHANICAL DIMENSIONS

The ABS plastic housing has access holes for adjustment potentiometers. Procedures for adjustment are covered in the DVC-350A User Manual. Figure 6 shows the locations of the battery compartment and voltage connectors.

The mechanical dimensions of the DVC-350A appear in Figure 7.

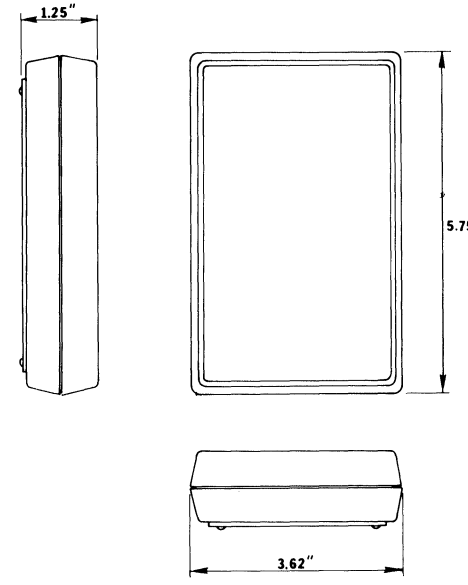

Figure 7. DVC-350A Mechanical Dimensions

ORDERING GUIDE

DVC-350A

Includes:

Calibrator

Water resistant carrying case (inside pocket for test leads and spare batteries).

Test Leads Set
Two 3 foot, 20 AWG, leads, stackable banana plugs (with retracting hook clips)

Certificate of NBS Traceability
Operations Manual

Accessory Kit MODEL 39-7267690

Includes:
AC Adapter/Charger, UL/CSA approved

7.2V Rechargeable Ni-Cd battery

1. DVC-350A
2. Case
3. AC Adapter
4. 7.2V Rechargeable Battery
5. Test Leads

WARRANTY

DATEL warrants this product to be free of defects in material and workmanship for a period of one year from the date of shipment, under normal use and service. DATEL's obligations under this warranty are limited to replacing or repairing the product, at its option, at its factory or facility. The defective product must be shipped to DATEL's facility for repair or replacement within the warranty period, transportation and charges prepaid. This warranty shall not apply to a product which has been repaired or altered, except by DATEL, or which has been subjected to misuse, negligence, or accident. In no case shall DATEL's liability exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of this product which has either been repaired or replaced by DATEL.

DVC-8500
Miniature High-Precision Voltage Calibrator

FEATURES

- **±19.999 Volts full-scale output range, attenuation kits available for ±1.9999V FSR and ±199.99 mV FSR**
- **Millivolt settability with accuracy of ±25 ppm of setting ±1/2 LSB (0.005% of Full-scale Range)**
- **Output range set from quick-select front panel lever switches**
- **Continuous front panel ±1.5 mV vernier control**
- **Rated accuracy up to 25 mA output**
- **Current from short-circuit-proof output transformer-isolated ±300 Volts to AC line**
- **Miniature aluminum case includes bench-top stande or can be panel mounted**
- **Choice of 100, 115, or 230 VAC power supplies**
- **Low cost**

GENERAL DESCRIPTION

DATEL's low-cost miniature Digital Voltage Calibrator, model DVC-8500, is a 4 1/2 digit voltage reference source with a full-scale output range of -19.999 Volts to +19.999 Volts in 1 millivolt steps. An active buffered output amplifier provides very low output impedence and up to 25 milliamps output current at the rated accuracy of ±25 ppm of setting, ±500 µV. This short-circuit proof output is selected by unique front-panel lever switches. These switches provide rapid, positive contact adjustment, far superior to traditional thumbwheel switches. Voltage outputs may be continuously varied within ±1.5 millivolts of selected readings by using the front panel vernier control. The DVC-8500 output is available from both front panel banana jacks and a rear panel 36-pin gold-plated PC connector fitted with lug terminals.

The DVC-8500 Digital Voltage Calibrator is small enough for bench-top use or panel mounting. It fulfills many laboratory needs such as calibrating A/D and D/A Converters, Digital Panel Meters, Operational and Instrumentation Amplifiers, Voltage/Frequency Converters and Digital Voltmeters. The small size and light-weight design of the DVC-8500 make it an ideal portable instrument for a technician's repair kit. When mounted on its bench-top tilt stand, the DVC-8500 uses very little space and can be positioned close to test circuits.

The miniature calibrator features high performance for such a small, low-cost instrument. An oven-stabilized zener diode internal reference provides an overall accuracy of ±500 µV and ±25 ppm of the setting with zero drift of ±5 µV/°C and full-scale drift of 4 ppm/°C max.

Rear connector sense feedback inputs to reduce errors caused by cable resistance. A front panel LED overload lamp lights if the output exceeds 25 mA and current limiting occurs at 70 mA output. The output circuit can accept up to ±25 mA source or sink current at rated accuracy. The rear connector also includes a low-Z output of the +10 Volt reference source with 5 mA maximum drive for external reference tracking. Wideband output noise is 25 microvolts, pk-pk max.

Powered by a choice of 100, 115 or 230 VAC ±10%, and 47 to 440 Hz at 10 watts, the DVC-8500 offers transformer isolation up to ±300 VDC. Output line rejection is within ±50 microvolts of zero and within ±25 ppm of full-scale range. The black-anodized extruded aluminum housing provides excellent shielding to electrical noise.

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FUNCTIONAL SPECIFICATIONS

(Typical between 0°C and +50°C at steady ambient temperature after 5 minute warm-up)

VOLTAGE OUTPUT

Output Type..... Shielded transformer isolated, active low impedence DC voltage output, current limited.

Output Voltage Range..... 0 to +19.999 Volts DC or 0 to -19.999 Volts DC, lever switch selected, 1 mV steps (Range ±20.0005 Volts using vernier control).

Output Current Range..... 0 to 25 mA (source current) to rated voltage output accuracy.

Output Overload..... Greater than 25 mA (source current) will illuminate front panel LED overload lamp. Output is current limited (continuous short-circuit proof) to 70 mA (source current) at any voltage up to ±20V dc.

Output Impedance..... Less than 10 milliohms.

Capacitive Load..... no limitation

PERFORMANCE

Accuracy @ +25°C with Vernier Control at Zero..... Within ±25 ppm of setting, ±500 µV when calibrated (0.005% of Full-scale range).

Resolution..... Set within ±1 mV increments. A front panel vernier control provides ±1.5 mV continuous offset with 100 µV graduations.

Temperature Drift of Zero..... Within ±5 µV/°C

Temperature Drift of Calibration..... Within ±4 ppm of setting/°C

Operating Temperature Range..... 0°C to +50°C

Storage Temperature Range..... -25°C to +85°C

Warm-Up Time..... 5 minutes to rated accuracy

Output Noise..... 25 µV pk-pk, wideband (no cap load)

Reference Source..... 6.4V oven-stabilized low TC zener reference diode

AC Line Voltage Rejection..... Zero: ±50 µV over full line range
Calibration: ±25 ppm of setting over full line range

Power Transformer Isolation..... 1000 Megohms. Transformer primary has a grounded shield for capacitive isolation.

Breakdown..... 300 VRMS, min.

FRONT PANEL

Output Selector Switches..... Six lever-operated detented switches are set in millivolts (±19999 mV range)

Polarity..... 2 positions, + or -

Leading Digit..... 2 positions, 0 or 1

4 Digits..... 10 positions, 0 thru 9

Output Vernier..... Rotary potentiometer, range ±1.5 mV of selected output. Graduated in 100 µV divisions. Clockwise rotation labeled "INCR" (increase) will increase the absolute value of the selected output. "INCR" will make a negative output more negative or positive output more positive. Counterclockwise rotation labeled "DECR" (decrease).

Overload Light..... Red LED lamp illuminates if output exceeds ±25 mA.

Power Switch..... Toggle switch, AC power on or off.

Power Light..... Red LED lamp illuminates when AC power is on.

INPUT/OUTPUT CONNECTORS

Front Panel..... Voltage output (blue) and output comon (black) available from two (2) gold plated brass banana jacks, 0.166" (4,22 mm) i.d., 0.56" (14,2 mm) deep, 0.75" (19,05 mm) between centers. (Order DATEL test leads, model 38-8193902)

Rear Connections:

Voltage Output..... Parallel connection with front panel jack.

Output and Reference Common..... Parallel connection with front panel jack. Transformer isolated ±300V from case ground.

Reference Output.. Low impedance ±10 Volt DC output from +6.4V ref. diode. Drain must not exceed ±5 mA maximum. Ref. output is opposite polarity of calibrator output.

Sense Input..... Connect to remote load to compensate for cable resistance voltage drops. See diagram. This input must be tied to voltage output if not used.

Sense Common..... Return for sense inputs. Tie to output common if sense is not used.

Rear connections are arranged as dual 36-pin PC edge-board connections on 0.1" centers. Individual connections consist of 4 gold-plated fingers on a common pad area in

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parallel with the 4-finger pad on the bottom. Each dual-pad (8 fingers total) is drilled and plated through for optional lug connection using 4-40 hardware. Shorting bars and 4-40 hardware are included to short sense and common connections if not used.

For rear connections, use a Viking#3VH36/1JN-5 or equivalent PC connector.

ADJUSTMENTS

Calibration adjustment trim pots are accessible by partially removing circuit board from case.

POWER SUPPLY

Requirement:

DVC-8500A..... 115 VAC, ±10%, @ 47-440 Hz, 10 watts (includes US-style, 3-prong line cord)

DVC-8500E..... 230 VAC, ±10%, @ 47-440 Hz, 10 watts (includes US-style, 3-prong line cord)

DVC-8500J..... 100 VAC, ±10%, @ 47-440 Hz, 10 watts (includes US-style, 3-prong line cord)

Grounding..... Ground wire to case, but transformer-isolated ±300 VRMS from output common.

Fuses:

DVC-8500A..... 0.15 A AGC SLO-BLO

DVC-8500E..... 0.1 A AGC SLO-BLO

DVC-8500J..... 0.15 A AGC SLO-BLO

MECHANICAL DIMENSIONS

Case..... 5.59"W x 2.11"H x 5.78"D (142,0 x 53,6 x 146,8 mm) (Bench-top stand retracted)

Bezel..... 5.86"W x 2.25"H x 0.50"THK (148,7 x 57,0 x 12,7 mm)

Servicing..... Bezel, front panel and mother board are removable from front while unit remains secured in panel. Bezel is lifted off by removing the two 0.050-inch (4-40) Allen hex key set screws on the bottom side edges. PC boards may be removed by loosening the PC board guide track retaining screws on the lowest position of the panel mounting seats.

Weight..... 2.25 pounds (1,0 Kg)

Cutout..... 5.62" x 2.16" (142,7 x 54,8 mm)

MOUNTING

Choice of bench-top mounting or panel mounting through a cutout measuring 2.16"H x 5.62"W (54,8 x 142,7 mm) and secured by 2 U-Straps. See ordering guide for optional panel-mount kit.

ORDERING GUIDE

Accessories:

DVC-8500A..... Calibrator, 115 VAC

DVC-8500E..... Calibrator, 230 VAC

DVC-8500J..... Calibrator, 100 VAC

Panel-Mount Kit, P/N 38-8193022..... Consists of (2) U-Straps, rear PC board connector and hardware

Test Lead Set, 38-8193902..... Consists of (2) 3-foot, 20 gauge leads, red and black. Stackable banana plugs and retracting hook clips

10:1 Attenuator, 38-8193900..... For ±1.9999V output range

100:1 Attenuator, 38-8193901..... For ±199.99 mV output range

DATA ACQUISITION BOARDS

VMEbus I/O BOARD CHART

COMPUTER BUS	FUNCTIONS	A/D CHANNELS	RESOLUTION	A/D CONVERTER RATE	D/A CHANNELS	NOTES	MODEL	PAGE
VMEbus 16 data 16 addr Slave	A/D	32S/16D expandable to 256D	12, 14 16 Bits	50 kHz (611A) 250 kHz (611B) 28.5 kHz (611C) 2.5 Hz (611D)	Not included, See DVME-612	VMEbus slave, expandable to 256D channels using DVME-64X series MUX.	**DVME-611**	11-23
VMEbus 16 data 16 addr Slave	A/D & D/A combination	32S/16D expandable to 256D	12, 14 16 Bits	50 kHz (612A) 250 kHz (612B) 28.5 kHz (612C) 2.5 Hz (612D)	2 D/A 12 bits, 10µS	VMEbus slave, analog input expandable to 256D channels using DVME-64X series MUX.	**DVME-612**	11-23
VMEbus 16 data 16 addr Slave	A/D thermocouple RTD, high-level, strain gage, and voltage options	4 Differential 1000V pk isolated	12 Bits plus sign	12.5 to 30 Hz, selectable	N/A	VMEbus slave, smart thermocouple processor with 1000V pk isolated inputs. Optional strain gauge, RTD, and high-level-signal conditioning modules available.	**DVME-602**	11-11
VMEbus 16 data 16 addr Slave	D/A Isolated	N/A	12 Bits	N/A	4 Isolated 30 µS setting (-624C1, V1) 6 µS setting (-624C2, V2)	VMEbus slave, 300 VRMS output isolated channel-to-channel and channel-to-bus.	**DVME-624**	11-31
VMEbus 16 data 16 addr Slave	D/A, Non-isolated	N/A	12 Bits	N/A	8-Channel 12 bits, 6 µS setting time	VMEbus slave.	**DVME-628**	11-39
VMEbus except data/ addr	A/D mux., Non-isolated	32S/16D channel expander for DVME-611/ 612	N/A	N/A	N/A	32S/16D channel slave. Analog multiplier can expand DVME-611/612/ 601 inputs to 256D channels.	**DVME-641**	11-43
VMEbus except data/ addr	A/D mux., Isolated	8 differential channel expander for DVME-611/ 612	N/A	N/A	N/A	8-Channel isolated analog multiplexer with thermocouple, RTD, strain gauge, or high-level signal conditioning. Can expand DVME-611/ 612/601 inputs to 256D channels.	**DVME-643**	11-45
VMEbus except data/ addr	A/D mux.	32S/16D simultaneous sample/hold. Channel expander for DVME-611/ 612	N/A	N/A	N/A	32S/16D channel slave analog simultaneous samlpe/hold multiplexer. Can expand DVME-611/ 612/601 inputs to 256D channels.	**DVME-645**	11-47
VMEbus 16 data 16 addr Slave	Digital I/O Non-isolated	N/A	N/A	N/A	N/A	48-Line digital I/O with timer.	**DVME-660**	11-49
VMEbus 16 data 24 addr Slave	Intelligent A/D plus local 68010, RS-232, 5 TTL I/O	16S/8D plus channel expand to 256 Chans.	12,14 16 Bits	50 kHz (601A) 250 kHz (601B) 28.5 kHz (601C) 2.5 Hz (601D) 500 kHz (601E)	N/A	Smart A/D local 68010, 64K dual port RAM, 64/ 128K EPROM w/ monitor/Exec, 3 timers.	**DVME-601**	11-3

NOTE: All models include AC/DC converter

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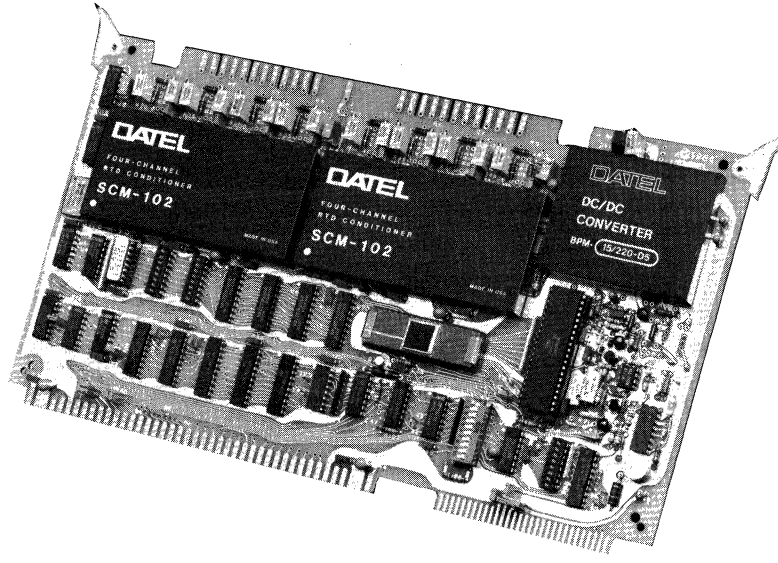


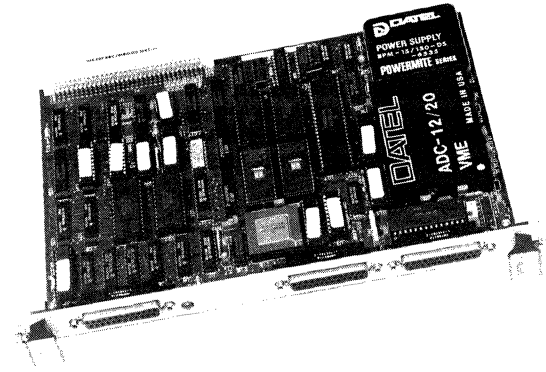
MULTIBUS I/O BOARD CHART

COMPUTER BUS	FUNCTIONS	A/D CHANNELS	RESOLUTION	A/D CONVERTER RATE	D/A CHANNELS	NOTES	MODEL	PAGE
MULTIBUS 8/16 data 20/24 addr	A/D & 3 Digital I/O lines	32S/16D Up to 144D	12, 14 16 Bits	Up to 132 kHz; selectable converters	N/A	Intelligent A/D data preprocessor with 4K dualported RAM and on-board executive interpreter.	**ST-701**	11-67
MULTIBUS 8/16 data 20/24 addr	A/D Thermocouple RTD, strain gage, voltage options	8 Differential 1000V isolated	12 Bits plus sign	12.5 to 30 Hz, selectable converters	N/A	Smart thermocouple processor with 1000 Vpk isolated inputs. Option for RTD, strain gage & voltage.	**ST-702**	11-75
MULTIBUS 8/16 data 20/24 addr	Isolated D/A	N/A	12 Bits	N/A	4 Isolated 30 µS (ST-703A) 6µS (ST-703B)	300 VRMS output isolation from channel-to-channel and channel-to-bus.	**ST-703**	11-83
R-232C or Isolated 20 mA	Remote A/D, Multi-drop	8 Differential	12 Bits plus sign	12.5 to 30 Hz, selectable converters	N/A	Smart, remote thermocouple or voltage measurement subsystem with RS-232/ 20 mA common. port.	**ST-705**	11-91
MULTIBUS 8 data 20/24 addr	A/D, Non-isolated	32S/16D	12 Bits	50 kHz	See ST-732	Industry-standard replacement for ISBC-711.	**ST-711**	11-103
MULTIBUS 8 data 20/24 addr	A/D & D/A combination	32S/16D	12 Bits	50 kHz	2 D/A with 4-20 mA, 12 bits, 3 µS	Industry-standard replacement for ISBC-732.	**ST-732**	11-103
MULTIBUS 8/16 data 20/24 addr	D/A, Non-isolated	N/A	12 Bits	N/A	4- or 8-Channel 12 bits, 5 µS	Replaces ISBC-724 with increased channel capacity.	**ST-728**	11-125
MULTIBUS 8/16 data 20/24 addr	D/A, Non-isolated	N/A	16 Bits	N/A	4- or 8-Channel 14 bits, 15 µS	Higher resolution, higher accuracy (14 bits) D/A.	**ST-716**	11-111
MULTIBUS 8/16 data 20/24 addr	Digital I/O and Interrupt	N/A	N/A	N/A	N/A	72-Line digital I/O card with interrupt capability (industry standard).	**ST-519**	11-61

NOTE: All models include AC/DC converter

DVME-601
16S or 8D-Channel 68010-based VME A/D Coprocessor Board

FEATURES



- **Local 8 MHz 68010 CPU plus:**
  - **— 64 Kb Private RAM**
  - **— 64/128 Kb EPROM**
  - **— 64 Kb Dual-ported RAM**
- **Various analog-to-digital front ends:**
  - **— 12 Bits, 4 μSec.**
  - **— 16 Bits, 35 μSec.**
  - **— 16 Bits, 400 ms**
  - **— 12 Bits, 2 μSec.**
- **16 Single-ended or 8 differential on-board analog input channels expandable to 256 channels using DATEL's slave MUX boards.**
- **Simultaneous A/D scanning and host transfer of previous scans. Ideal for DSP, FFT, ATE, graphics.**
- **Monitor/Executive firmware to run in "no program mode" or from user programs.**
- **RS-232-C serial port to debug optional user software. Programs may be downloaded through dual-port RAM or serial port and reprogrammed in EPROM.**
- **Programmable Peripheral I/O (68901):**
  - **— RS-232-C serial port USART.**
  - **— Three timer outputs which are software-programmable as interrupts, A/D start triggers, or pulses.**
  - **— Two 8-bit counter inputs.**
  - **— Five TTL I/O bits or interrupts.**
- **On-board +5V dc-to-dc power converter**
- **Users may integrate the programmable VMEbus interrupt with a real-time operating system.**
- **A/D Start by external trigger, timer or program.**
- **Sample-to-memory transfers at up to 170 kHz**
- **Easily integrates with popular host multitasking Real Time Operating Systems such as VERSAdos, PDOS, OS-9, and VRTX.**

Today's VME environment requires that busy host processors run real-time operating systems, seriously affecting the host system's processing speed. DATEL'S DVME-601 coprocessor board integrates high-performance A/D data acquisition with a local 68010-based microcomputer. This unique single-board design lets the host handle other tasks while the DVME-601 smart A/D board simultaneously collects analog data.

GENERAL DESCRIPTION

Unlike dumb A/D boards, the DVME-601 coprocessor board automatically collects scanned data without delaying other host tasks. When A/D data is ready, the DVME-601 coprocessor board can interrupt the VME host. The host can then transfer data from previous scans to memory without halting collection of the next scan's data.

Typical applications for the DVME-601 include high-speed process control loops, analytical instruments, vehicular data recorders, ATE equipment and communications testers. The block-oriented, interrupt-controlled memory transfers of A/D scans to the host are particularly suited to digital signal processing applications. Such applications include acoustics, sonar, high-speed mapping, seismology, medical imaging, graphics, array processing, FFT's, and waveform analysis. Using the single-channel fast-throughput mode and the 4 μSec., 12-bit converter yields true speeds of up to 170,000 samples per second to memory (single channel, gain = 1).

As shown in Figure 1, the data acquisition section includes an analog input multiplexer with 16S/8D local channels expandable up to 256 total channels using DATEL's slave multiplexer boards. The board includes an instrumentation amplifier which may be resistor-programmed by the user for gains of up to 1000. A choice of pluggable A/D converter modules is offered on four different models. Resolution from 12 to 16 bits is available with 12-bit conversion speeds down to 2 μSec.

New!! DVME-601E: over 200kHz (single-channel, gain = 1, PGA bypassed)

(VERSAdos is a Motorola trademark. PDOS is an Eyring Research Institute trademark. OS-9 is Microware trademark. VRTX is a Hunter and Ready trademark.)

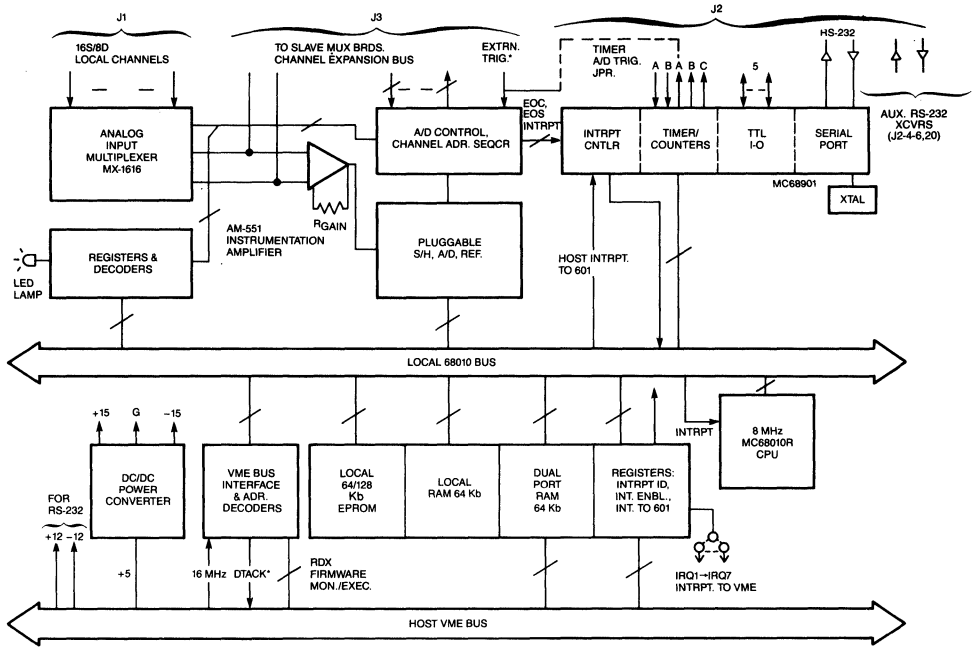


Figure 1. DVME-601 Coprocessor Board Simplified Block Diagram

External triggers, the internal programmable timer, local programs, or host commands may initiate A/D conversions. On-board EPROM firmware manages all of these start modes. A dc-to-dc converter supplies low-noise, regulated power to the data acquisition section.

The primary interface between the DVME-601 and its VME host is a 64 Kb dual-ported random access memory (DPR). The DPR is used for commands, subroutines and parameters, control/status bits, A/D data blocks, optional downloads of user programs, and bidirectional interrupts between the DVME-601 and the host. The maskable interrupt to the VMEbus normally occurs after A/D scanning, but may also be issued by a local user program.

Executive firmware included in the EPROM offers many ways to manage the DPR including swapped buffer ("ping-ponged") A/D scan transfers while the host reads the alternate buffer. The user may run the DVME-601 either in the "no-programming" mode or may load and execute their own programs. The no-program mode uses fast A/D routines supplied in the EPROM. The firmware also includes a serial port monitor program for developing optional user programs.

The DVME-601's full power and flexibility is realized with user-written software. As a high-performance, general-purpose microcomputer, the DVME-601 is ideal for automatic A/D data collection and arithmetic pre-processing of A/D data before sending it to the host. Transferring pre-processed results rather than raw data enhances total system performance while the host continues with disk, display, or control activities. Programs may be developed in the host, saved on disk, then downloaded to local RAM via the DPR or serial port. The pluggable EPROM may be reprogrammed by the user or by DATEL under special order. Any language may be used such as Assembly, BASIC, FORTRAN or C if it can be compiled to 68010 code.

The local microcomputer consists of an 8 MHz MC68010 microprocessor, 64 Kb of pluggable EPROM (socketed to 128 Kb), 64 Kb of DPR and 64 Kb of private RAM. Total local storage of A/D data may approach 62,000 samples using the DPR plus private RAM if no other program is using RAM space.

A programmable 68901 I/O peripheral controller is also included as part of the board design. This device offers an interrupt controller, an RS-232-C serial port, four timer/counters, and five I/O bits. Some of the timers and the serial port are used by the monitor/executive firmware but may be reprogrammed by the user to include external interrupts. A second RS-232-C serial port is available using a software UART and the I/O bits. A green front panel LED lamp lights to confirm power-up self-test and may be programmed by the user for alarms, etc.

Using only the serial port, a 16 MHz clock, and a +5V dc power supply, it is even possible to operate the DVME-601 in stand-alone mode, not connected to the VMEbus. Commands and A/D data pass through the port at rates of up to 19.2 Kb.

The board uses +5V dc at 2.8 A and ±12V dc at 2 mA (typical) from the VMEbus. Connections are made only to P1 (P2 is not used to assure compatibility with most hosts). Data transfer is 16 bits wide. The DVME-601 is a D16 A24 slave board using 24 address lines and 6 address modifier lines. The board occupies 64 Kb of host memory. A single interrupt to the host asserts a programmable interrupt vector. Three front panel D-type connectors provide physical interfacing for local analog inputs, analog slave-mux channel expansion, and for the serial/parallel/timer I/O.

The DVME-601 is a 9.19″W × 6.3″D × 0.6″H (233,5 × 160 × 15,2 mm) 6U board. It includes a comprehensive user's manual with programming information. Access to the EPROM source code in several formats is available to customers upon special request.

FUNCTIONAL SPECIFICATIONS
(Typical at +25°C, Gain=1, unless noted.)

DATA ACQUISITION SECTION

Number of On-board Channels ....16 single-ended or 8 differential

Number of Off-board Channels ...Up to 240 single-ended or 248 differential using DATEL's external channel multiplexer boards. (10 MUX brds max.)

Total Addressable Channels .....Up to 256 single-ended or differential

Input Voltage Range .... ±10 Volts full scale. (± 5V, 0 to +10V, and 0 to +5V may be jumpered or special-ordered)

Common Mode Voltage Range ..... ± 10V, maximum, non-isolated

Common Mode Rejection (dc to 60 Hz, CMV = ±10V) .....80 dB, gain=1 with 1 KΩ source unbalance

Input Bias Current ..... ±200 pA

Overvoltage Protection . ±30V dc, maximum sustained

Input Impedance .....Power on: 1000 MΩ, differential or to ground. Power off: 1.5 KΩ

A/D Output Coding (All models) .....Bipolar 2's complement, or bipolar offset binary. The DVME-601A is jumperable for unipolar straight binary.

Instrumentation Amplifier Type and Gain Range .....AM-551, supplied as gain = 1. May be resistor-programmed by user up to gain=1000 with increased settling delay.

Instrumentation Amplifier Settling Delay (gain = 1) .....3 μSec. to 0.01% of FSR

Adjustments .....Instrumentation Amplifier offset, A/D offset and A/D gain.

LOCAL MICROCOMPUTER

CPU Type and Clock Speed ... MC68010R8, 8 MHz (requires VMEbus SYSCLK)

Local Data Bus Width ...16 Bits

Local Read/Write Memory .....64 Kilobytes static RAM (no VMEbus access)

Local Read-only Memory .....UV-erasable EPROM, 64 Kb supplied as two 27C256's but is socketed for two 27C512's totaling 128 Kb.

Dual-ported Read/Write Memory .....64 Kb (VMEbus and local access)

Front Panel LED Lamp . . Green LED lamp is lit if local CPU power-up self-test succeeds. User software may use the lamp for alarms, etc.

A/D-S/H RESOLUTION AND CONVERSION PERIOD OPTIONS
(See Technical Note 1)

Model	Resolution (Bits)	Convert Time	Throughput to RAM
DVME-601A	12	20 μSec.	40 kHz
DVME-601B	12	4 μSec.	114 kHz
DVME-601C	16	35 μSec.	25 kHz
DVME-601D	16	400 mSec.	2.5 Hz
DVME-601E	12	2 μSec.	see notes

SYSTEM PERFORMANCE

Specification	A/D Type				
	12 bit, 20 μSec.	12 bit, 4 μSec.	16 bit, 35 μSec.	16 bit, 400 mSec.	12 bit, 2 μSec.
Accuracy, minimum	±0.025% of FSR	±.05% of FSR	±0.01% of FSR	±0.0063% of FSR	±0.025% of FSR
Nonlinearity, maximum	±½ LSB	±½ LSB	±2 LSB	±2 LSB	±½ LSB
Zero tempco, maximum	±20 ppm/°C	±20 ppm/°C	±20 ppm/°C	±10 ppm/°C	±20 ppm/°C
Gain tempco, maximum	±20 ppm/°C	±20 ppm/°C	±20 ppm/°C	±10 ppm/°C	±20 ppm/°C

External A/D Start Trigger .....Negative-going TTL input with 4.7 KΩ pullup to +5V. Pulse width is 100 nSec. minimum, 2 μSec. max.

Local Pacer Clock .....Software-programmable to cause either an A/D scan start or a single conversion.

Pacer Clock Interval Range (supported in firmware) ....3.255 μSec. to 41.667 mSec. using one timer. Up to 3.03 hours using 3 cascaded timers.

PERIPHERAL I/O CONTROLLER

Controller Type .....MC68901 multifunction peripheral, crystal-controlled, 2.4576 MHz, user-programmed.

Interrupts

Local Hardware Interrupts to 68010 CPU (Maskable) .....A/D End of Conversion, A/D End of Scan, VMEbus host command request

Local Software Interrupts (Programmable) .....Any timer count reached or I/O bits 0 through 4.

Digital I/O

Number of I/O Lines . .5 lines, individually programmable as inputs, outputs, or interrupts.

Logic Levels .....TTL levels, 1 load maximum with 10 KΩ pullups to +5V.

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PERIPHERAL I/O CONTROLLER (cont.)

Timer/Counters

Number of Timers .....4 8-bit timers with pre-scale up to divide-by-200.

Timer Outputs .....3 outputs, (Timers A,B,C), 1 TTL load maximum. Timer D is the USART baud clock but may be reprogrammed.

Timer/Counter Inputs...2 inputs, TTL levels with 10 KΩ pullups to +5V.

Serial Port (See Technical Note 2)

Number of Serial Ports..1 USART, full duplex, RS-232-C levels, DTE pinout.

RS-232-C Handshakes ..DTR, DSR, RTS, CTS programmed by the user. (See J2 pinout).

Modes .....Synchronous or asynchronous.

Number of Stop Bits....0, 1, 1.5, or 2

Number of Data Bits....5, 6, 7, or 8

Parity.....Odd, even, none for receiver. Transmitter is user-coded.

Baud Rates .....Up to 19.2 Kilobaud.

VMEbus INTERFACE

Standards Compliance..IEEE P1014/D1.0

Data Bus Width.....16 Bits

Address Bus .....A24 D16 slave, 24 address lines (A23-A01) plus 6 address modifiers, jumper selected.

Address Modifier Codes .....39 hex or 3D hex, jumperable.

Architecture (See memory map) .....Dual-ported 64 Kb block mapped on 64 Kb boundaries.

VME Bus Interrupter (See Note 3)....1 line, jumper-selectable IRQ1* through IRQ7*.

Data Transfer.....16 bits using P1. Generates DTACK* derived from 16 MHz bus clock.

CONNECTORS

VMEbus, P1.....96-pin male DIN connector. P2 connector not used.

Local Analog Input, J1 ..25-pin DB-25S female on front panel.

Multifunction I/O Peripheral (68901), J2.....25-pin DB-25S female on front panel.

Analog Input Channel Expansion Bus, J3...25-pin DB-25S female on front panel, compatible to DATEL DVME-64X series multiplexer boards.

MISCELLANEOUS

Power Required .....+5 Vdc ±5% at 3.0 A max. (DVME-601A,B) or 3.1 A max. (DVME-601C,D) and ±12 Vdc at 10 mA max. from VMEbus for serial port. A local ± 15V dc-to-dc converter is included for linear circuits.

Operating Temperature.....0 to +60°C

Storage Temperature ...−20°C to +80°C

Relative Humidity.....10% to 90%, non-condensing.

Outline Dimensions ....Double-height VME, 6U outline. 9.19″ W × 6.3″ D × 0.6″ H, (233,5 × 160 × 15,24 mm).

Weight.....17 ounces (482 grams)

TECHNICAL NOTES

1. The typical throughput rate is an aggregate time within a multichannel scan and does not include setup time. The rate includes times for channel sequencing, multiplexing, as well as delays from the instrumentation amplifier, S/H acquisition/settling, A/D conversion, and 68010 software times. The polled-EOC STSNSC subroutine is used, triggering A/D conversion on each data read. Higher single-channel speed is available using the "fast-throughput" mode (delayed DTACK*). The DVME-601E offers over 200kHz in a long-burst to local RAM (single channel, gain = 1, PGA bypassed).
2. EPROM Monitor firmware uses Timer D and the serial port. Communications format is 9600 baud, 8 data bits, no parity, and 1 stop bit. A 4800-baud software UART is formed with I/O bit 0 for optional serial S record downloads. Firmware also uses Timer A as an A/D start clock. The user may re-program all functions.
3. Asserts one interrupt ID code which is programmable from the host. A DVME-601 local register generates the interrupt. The host may mask this interrupt by writing to a DVME-601 DPR register.

DVME-601 FIRMWARE OVERVIEW

Memory Mapping

Table 1 shows the relationship between the local DVME-601 memory and the host DPR window. Arbitration circuits prevent simultaneous access to the DPR by delaying either the local DVME-601 DTACK* or the VMEbus DTACK*. Three addresses in the DPR are hardware-mapped from the host. They enable interrupts to the host, select the interrupt ID vector that is asserted and force a local 68010 interrupt to execute a Function Block Command or local subroutine.

A portion of the top of Read/Write DPR is reserved for control/status bits defined by the DVME-601 firmware. A portion of the local RAM is reserved for the DVME-601 system control, vectors and stacks. Data acquisition and 68901 registers, as well as a register to interrupt the host from a local program, are hardware-mapped in local memory.

Table 1. DVME-601 Memory Map

Local Memory		Host Memory	
$000000- $01FFFF	64/128 Kb Local EPROM (READ only)		
$020000- $02FFFF	64 Kb Local RAM (READ/WRITE)		
$040000- $04FFF7	64 Kb Shared Dual Port RAM (READ/WRITE)	Base + $0000- Base + $FFF7 [$FFF0-FFF7 are soft-mapped R/W cmd/stat. See manual.]	Shared 64 Kb DPR (RD/WR)
$04FFF8 $04FFF9	Not used Not used	Base + $FFF8 Base + $FFF9	Enable interrupt to VMEbus (RD/WR) (Bit 7)
$04FFFA $04FFFB	Not used Not used	Base + $FFFA Base + $FFFB	Host interrupt ID Vector (RD/WR)
$04FFFC $04FFFD	Not used Not used	Base + $FFFC Base + $FFFD	Force command interrupt to DVME-601 (WR-only word from host)
$04FFFE $04FFFF	Not used Not used	Base + $FFFE Base + $FFFF	Not used Not used
$06XXXX	A/D Start Channel Address Reg. (WR)	Notes:	
$08XXXX	A/D Final Channel Address Reg. (WR)	1. Unlisted addresses are redundant or not defined. All addresses are in hexadecimal. "XXXX" bytes are not decoded and are don't care. Factory-jumpered base addressing is $FA0000.	
$0AXXXX	Command/Status Reg. (R/W) [EOC,EOS, LED, A/D, etc.]	2. Hardware registers from $6XXXX to $10XXXX require MOVE.W instructions. Local RAM from about $20000-21000 is reserved. 68901 registers require MOVE.B instructions or Read-Modify-Write.	
$0CXXXX	Start A/D Convert (WRITE only)		
$0EXXXX	Force interrupt to VMEbus Host (WR)	3. BASE + $FFFC is write-only from VMEbus and should be located beyond power-up memory testing.	
$10XXXX	A/D Data Register (READ only)		
$120000- $12002F	68901 Intrpt/Timers/ USART/Parallel Port (READ/WRITE)		

A/D Converter Command Modes

Location $0AXXXX in the DVME-601's local memory map contains a command register. The settings of individual bits in this register determine:

- A/D converter triggering,
- modes of channel sequencing, and
- how the converter transfers data.

Executive firmware manages this register; however, it may be directly controlled by user-written programs as well. The addresses below refer to the local 68010 memory map (see Table 1). The command register controls the following hardware functions:

1. A/D conversion starts with a short settling delay before the actual conversion. Three events can trigger the delay:
   A. An external TTL trigger or timer input arrives. (The logic enables the trigger and waits for the falling edge.)
   B. The local CPU reads the A/D data register ($10XXXX).
   C. A write to location $0CXXXX occurs.

These modes may be partially combined. All modes must test the End of Conversion (EOC) bit to confirm that data is ready.

2. The start pulse may start either a single conversion or a scan of N channels as defined by the start and final channel address registers ($06XXXX and $08XXXX). If the start defines a SCAN, then individual samples must still be started by reading the A/D data register.
3. A "fast throughput" mode is offered where the A/D converter logic holds off the local DTACK* input to the 68010 until the End of Conversion output. This mode offers higher speeds by eliminating EOC polling. When used with a block move instruction loop which auto-increments the destination pointer, this acts like a DMA transfer. During DMA transfers, the instruction remains in the 68010's queue and requires no opcode fetch cycle.
4. A "re-scan mode" is offered which automatically reloads the start channel register when the End of Scan is reached. This mode yields higher speeds for repeated scans by eliminating the address register write.
5. The channel address sequencer may be inhibited from incrementing after each sample. This would be used for very high-speed single channel applications and is similar to loading the same address in both the start and final addresses registers.
6. The A/D start logic may be inhibited by local 68010 command. This would be used to ignore external triggers until ready or for other usage.

NOTE

EOC/EOS interrupts are always sent to the local 68901 interrupt controller but are normally masked off by programming the 68901 registers.

EPROM Firmware

The 64 Kb EPROM includes Monitor and Executive software. The Monitor helps in developing and debugging optional user-written programs and is available only via the RS-232-C serial port. This port is on the DVME-601's front panel J2 connector. The user simply connects a "dumb" terminal to this connector.

The Monitor is not required if the user chooses to control the DVME-601 only from the DPR using the Executive. After successful power-up testing, the LED is lit and the DVME-601 automatically enters the Monitor. This LED illuminates to indicate successful memory and I/O tests. The DVME-601 attempts to run the Monitor even if self-test fails. The Executive will be off, insuring that the DVME-601 will ignore any power-up bus activity in the DPR. The user switches the board from the Monitor to the Executive state via either the serial port or the DPR.

The Executive accepts function blocks loaded from the DPR by the host. The blocks may contain reserved command words, local subroutine addresses, and optional input or output parameters. The host tells the DVME-601 to execute a previously loaded command by writing to a reserved location in the DPR. This forces a local 68010 interrupt to branch to the command or routine.

A typical subroutine would set the start and final analog channel address registers. It would include these addresses as long-word parameters in a sequential list after the subroutine memory address. Another subroutine would start A/D scanning. Its "output parameter" would be blocks of digitized A/D data transferred to the DPR.

Subroutine addresses may also include the addresses of user-written code which was previously downloaded into local memory or reprogrammed in the EPROM. A function command is reserved to perform the DPR download of S records. Since the S records contain destination addresses and may be of any length, the code may be sent anywhere in usable local RAM. It can overlay previous code and can be repeated indefinitely at high speed. It can include tables as well as executable binary image since it is not executed as part of the download.

All of this activity is controlled by VMEbus commands via the Executive. While a subroutine runs, a reserved control/status area of DPR indicates when command execution is in progress

and when a command block is done. Any subroutine (including a long multiple A/D scan) may be interrupted to return to the command level or execute a different routine. Thus, the user has an extremely powerful, general purpose means of controlling the DVME-601.

Monitor Commands

A conventional hexadecimal firmware Monitor allows full access to the 68010 CPU registers, data acquisition registers, the 68901 peripheral, and to memory locations (including the DPR). Programs may be run under breakpoint and/or trace control. The Monitor also includes several A/D diagnostic commands to aid in calibration or hardware troubleshooting. A list of monitor command functions appears in Table 2.

Table 2. Summary of Monitor Command Functions

Monitor Commands
Read/Write CPU or memory registers.
Display memory block in hexadecimal and ASCII.
Fill memory block with a constant.
Set or display breakpoint.
Trace one or more instructions.
Start execution until optional breakpoint.
Turn Executive ON or OFF (enable/disable DPR commands).
Transition to/from Executive or Monitor.
Auxiliary serial port download.
Start A/D sampling to serial port.

Executive Commands

The Executive accepts commands and optional parameters through the DPR. A major benefit of the Executive is a uniform sequential list method of passing subroutine parameters. User programs may also use this syntax or may develop their own parameter-passing method in another part of the DPR. If the user's serial port terminal is connected, the execution of Executive Function Blocks may be analyzed at the Monitor level. The Executive also traps non-executable subroutine addresses by performing a soft reset.

Executive Commands
Select the memory destination address of A/D scans as either local RAM, single DPR or swapped DPR buffers.
Select the source of A/D start triggers as external TTL, local timer, last A/D read or host command.
Select A/D triggering per conversion or per scan.
Select channel address sequencer to increment or not after each conversion.
Select start/final sequential channel addresses.
Select timer channel, period and control.
Transfer A/D scans from local RAM to DPR (after data pre-processing by a user-downloaded program).
Define whether scan transfers will wait for host Ready status or transfer without waiting.
Select how scanning will stop (N samples, N scans, buffer full, stop by host).
Download S records via DPR or auxiliary serial port and flag checksum errors but do not start execution.
Load subroutine addresses or function command block with optional parameter list and await execution.
Execute previously loaded commands or subroutine(s).
Memory block transfer.

The Executive allows for repeating or alternating blocks of sequential subroutines. They may be selected once, N number of times, or until stopped by the host. The DPR Download is one of the Executive commands. Most of the subroutines available through the Executive manage the data acquisition section. Table 3 lists the functions of executive commands available.

Speed by Architecture

The primary difference between the DVME-601 smart A/D board and "dumb" A/D boards is the increased total system throughput achieved by offloading the host. This is a result of simultaneous A/D scanning and concurrent host processing, plus using the DPR as a programmable buffer. Even greater system bandwidth may be possible by having the DVME-601 do arithmetic pre-processing of A/D blocks, delivering final results rather than raw input data.

Figure 2 shows the wasted idle times in the host for dumb A/D boards because an interrupt, polling, or DTACK* delay must occur with each sample.

The interrupt processing takes many microseconds to save stacks and registers and arbitrate with the Real Time Operating System. To realize the full speed of a dumb board, the host must be fully dedicated to data acquisition, leaving no time for non-A/D tasks. With fast converters and high bandwidth inputs, the short sample intervals make it inefficient to run the host in an interrupt mode, thereby locking out other host software tasks during data acquisition. The typical lack of memory on dumb boards for sample storage also means that the last sample is saved in the A/D converter and new sampling cannot start until the old sample is read.

The DVME-601 efficiently runs long blocks of thousands of samples, allowing ample time for host disk and display activity between blocks.

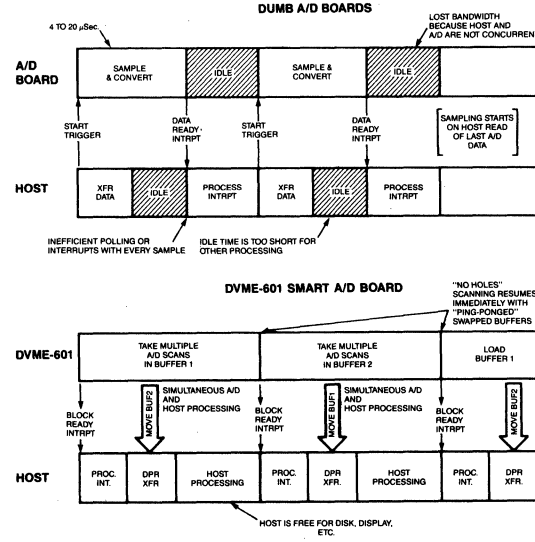

Figure 2. Speed by Architecture

I/O SIGNALS AND CONNECTIONS

A/D Channel Expansion Bus

(Please refer to the Channel Address Map, Table 4)

The DVME-601's J3 front panel connector accepts a flat cable assembly, such as DATEL Part Numbers DVME-C-01 or DVME-C-02, to form a channel expansion bus. The cable assembly plugs into DATEL's slave multiplexer boards installed in slots adjacent to the DVME-601 or in a nearby VME chassis. Available DATEL channel expansion boards include:

- DVME-641 A 32 Single-ended/16 Differential channel high-speed MUX;
- DVME-643 An 8 Differential channel low-level isolated MUX (for sensors such as thermocouples, RTD's, 4-20 mA loops, etc.); and,
- DVME-645 A 16 Single-ended/8 Differential channel simultaneous sample/hold MUX.

The DVME-645 is especially suited to array processing and DSP applications. This channel expansion bus allows the DVME-601 to directly control each slave MUX board and carries three classes of signals. They are:

1. Eight-bit channel address outputs from the DVME-601's address register, offering up to 256 total channels. This autosequencing register is software-controlled by the user's host program or DVME-601 firmware.
2. Buffered high-level switched differential analog signals into the DVME-601's instrumentation amplifier.
3. Control and handshake lines, an external A/D start trigger, and grounds.

Channel addresses are distributed to all MUX boards along the bus. The first 8 or 16 addresses are for local DVME-601 channels. Address selection logic and base address switches on each MUX board allows it to respond to a range of addresses. All other de-selected boards disconnect their analog outputs from the bus until addressed. For diagnostics, each MUX board has a LED lamp which turns on when that board is addressed. DATEL offers 2- and 3-connector cables to connect one or two slave MUX boards and users may fabricate flat cables for connecting up to 10 boards.

One of the control lines on the expansion bus is a TTL-compatible, open-collector A/D trigger. This lets the DVME-601's A/D start input be initiated from the trigger input on any multiplexer board. A single external event hardware trigger will start either one A/D sample and host interrupt or a scan of channels and interrupt on one or more boards. Alternatively, automatic channel sequencing and A/D conversion may be started from a DVME-601 timer by jumpering the timer output to the trigger input on the J3 connector. Software commands from the host will also start the A/D conversion process.

A settling delay control line output from each MUX board will delay the actual A/D conversion to synchronize settling times of low-level pre-amplifiers on the MUX slave boards. Through appropriate host A/D software, board addressing and input range selection, it is even possible to mix high- and low-level expansion input boards on the same bus.

Figure 3 shows how a DVME-601 Coprocessor board physically links to DATEL's slave multiplexer boards and field equipment.

Table 4. Analog Channel Expansion Address Map

Unused addresses	($FFh)
Expansion MUX Board N ⋮ Expansion MUX Board 2	
Expansion MUX Board 1	($0Fh or $07h)
DVME-601 16S/8D Channels	($00)

Input/Output Connections

Figures 4, 5, and 6 show the signals present on the DVME-601's J1, J2, and J3 connectors respectively. The connectors are dedicated as follows:

J1 Local Analog Inputs
J2 Multifunction Peripheral I/O Signals
J3 Analog Channel Expansion Bus

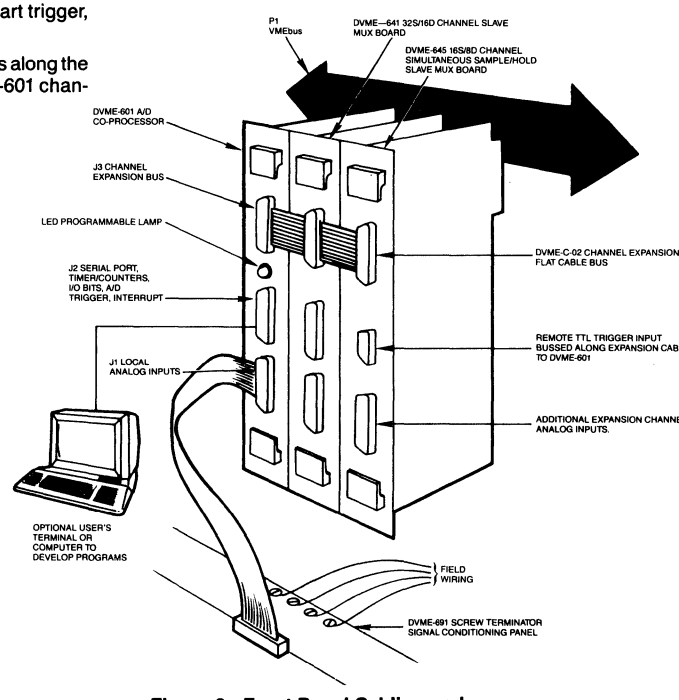

Figure 3. Front Panel Cabling and Wiring Connections

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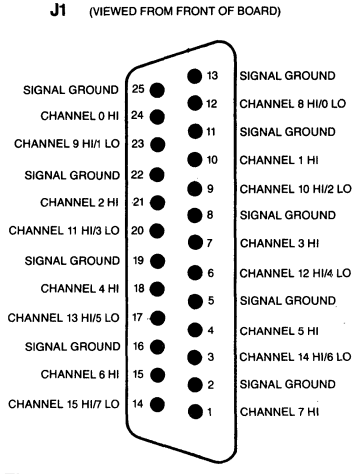


Figure 4. Local Analog Input Connector Analog (J1)

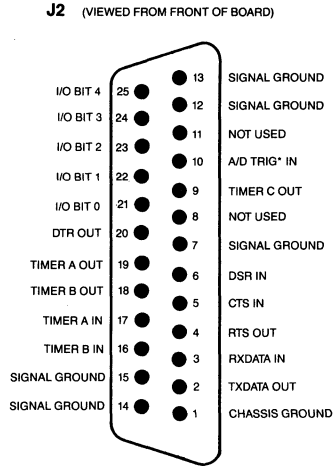


Figure 5. Multifunction Peripheral I/O Connector (J2)

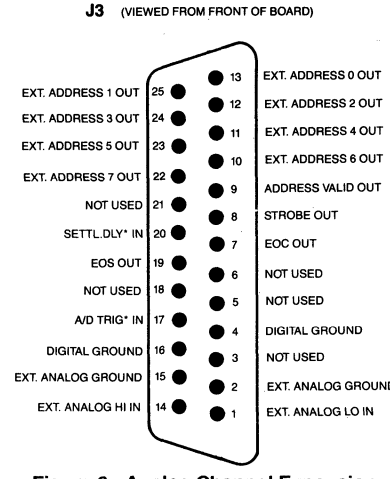


Figure 6. Analog Channel Expansion Bus Connector (J3)

ORDERING GUIDE

Model Number	A/D Bits, Conversion Speed, and Input Configuration
DVME-601A	12 Bits, 20 μSec., unipolar or bipolar
DVME-601B	12 Bits, 4 μSec., bipolar
DVME-601C	16 Bits, 35 μSec., bipolar
DVME-601D	16 Bits, 400 ms, bipolar
DVME-601E	12 Bits, 2 μSec., bipolar

Unipolar models DVME-601B-U and DVME-601C-U are available under special order.

All models include a 64 Kb EPROM with Monitor/Executive firmware, and a User's Manual. A substantial amount of unused EPROM is available to the user. DATEL will review custom software requirements under special order.

HARDWARE ACCESSORIES

Part Number	Description
DVME-691A	Rack-mount screw terminator panel with signal conditioning pads for 32S/16D input channels. Includes flat signal cables compatible with the DVME-601.
DVME-C-01	Channel expansion flat cable with 2 DB-25P connectors for use with one slave MUX board.
DVME-C-02	Channel expansion flat cable with 3 DB-25P connectors for use with two slave MUX boards.

CHANNEL EXPANSION SLAVE MUX BOARDS

Part Number	Description
DVME-641	32S/16D Channel high speed, high-level non-isolated MUX board.
DVME-643	8D Channel low-level, isolated MUX board.
DVME-645	16S/8D Channel simultaneous sampling MUX board.

Contact DATEL for DVME-601 software on disk.

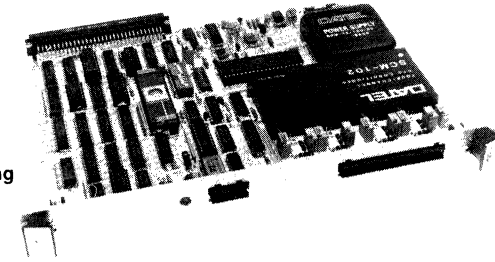
D/A OUTPUT AND DISCRETE I/O BOARDS

Part Number	Description
DVME-624	4 Channel isolated 12-bit D/A board, plus 4-to-20 mA passive loops.
DVME-626	6 Channel 14/16-bit D/A board.
DVME-628	4 or 8 Channel 12-bit D/A board, plus 4-to-20 mA passive loops.
DVME-660	48-line TTL I/O and timer/interrupt board.

DVME-602R
VMEbus 4-CHANNEL
RTD INPUT A/D BOARD

FEATURES

- **4 A/D channels for RTD temperature measurements**
- **Fully hardware-compatible with VMEbus architecture**
- **On-board CPU for temperature calculations**
- **Open RTD detection circuitry**
- **Internal RTD excitation, linearization and signal conditioning**
- **Output in degrees Celsius or Fahrenheit**
- **12-Bit plus sign resolution**



THE DVME-602R IS AN INTELLIGENT VMEbus A/D BOARD SPECIFICALLY DESIGNED FOR RTD INPUT MEASUREMENTS. CONDITIONING SIGNALS FROM UP TO 4 CHANNELS, THE DVME-602R PROVIDES LINEARIZED DATA TO VMEbus-BASED HOST SYSTEMS. THE DVME-602R IS PROGRAMMABLE TO PROVIDE OUTPUTS IN DEGREES C OR F. DESIGNED FOR HOSTILE ENVIRONMENTS, THE BOARD IS IDEAL FOR MOST REAL-TIME DATA ACQUISITION AND PROCESS CONTROL APPLICATIONS.

GENERAL DESCRIPTION

The Model DVME-602R measures direct RTD transducer inputs. This intelligent A/D board provides signal conditioning for up to four analog input channels. The microprocessor on the DVME-602R performs functions relating to linearization of 100 ohm platinum RTD's with Alphas of 0.00385 European and 0.00392 American. The output data is available as either a Celsius or Fahrenheit temperature range value. On-board switches let the user conveniently select the RTD type and the output unit of measurement.

The DVME-602R hardware consists of four sections: VMEbus interface, microprocessor control, A/D converter and the input signal conditioning (with RTD excitation). An internal data bus links the control/data registers, A/D converter and the microprocessor. The board also detects open RTD's. Figure 1 shows the DVME-602R functional block diagram.

The DVME-602R A/D board comes complete with a user's manual. The manual describes the installation and calibration procedures for different applications and presents a theory of operation of the board. The user's manual also has a detailed section on troubleshooting. The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted using VERSAdos (PDOS format also available). Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

VME Interface

The DVME-602R interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to the address modifier codes 29H and 2DH for data output purposes. The DVME-602R generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes the VMEbus WRITE*, DS0*, DS1*, and SYSRESET* control lines to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-602R uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

VMEbus Interrupt Logic

The on-board microprocessor, at the end of linearization, generates an interrupt request on one of the VMEbus interrupt lines (IRQ1* through IRQ7*). The interrupt line is jumper-selectable. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-602R interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number on to the VMEbus (low byte). The interrupt ID number is programmable by the host system. If the interrupt level on the address line does not match the board's interrupt level, the board generates the daisy chain IACKOUT* signal.

ORDERING INFORMATION

DVME-602

- R = RTD inputs
- T = Thermocouple and low-level isolated inputs *
- H = High-level voltage and current loop isolated inputs *
- S = Strain gage inputs (Consult factory for availability.)

* Refer to the DVME-602T Data Sheet for specifications.

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FUNCTIONAL SPECIFICATIONS

(Typical at 25° C, unless otherwise noted.)

INTERFACE SPECIFICATIONS

Data Bus ..... 16 Bits

Address Bus ..... Short I/O Space 16 address lines

Address Modifier Codes .... Uses codes 29H and 2DH

Interrupts ..... 1 line, jumper-selectable.

Memory Mapping ..... Short I/O space, user or supervisor 256 words allocated per board.

Data Transfer ..... DTACK* signal line. Notifies the VMEbus host that data has been placed or accepted from the VMEbus data lines.

The VMEbus SYSCLK signal is required.

CONNECTOR SPECIFICATIONS

VMEbus P1 connector ..... 96-pin male DIN connector.

J1 Analog Input Connector ..... Connects to a 12-pin terminal block. Use Phoenix Contacts MSTB 1.5/12-ST or equivalent

J2 Digital Output Connector ..... Connects to a 4-pin terminal block. Use Phoenix Contacts MSTB 1.5/4-ST or equivalent.

ANALOG INPUT SPECIFICATIONS

Analog Input channels 4

Input Configuration ..... Differential

Input Type ..... RTD (Refer to Table 1)

Input Impedance ..... <100 Megohms, minimum

Input Bias Current ..... 10 nanoamps, maximum

Common Mode Rejection Ratio, minimum, Rs ≤ 1k, f=0.01 to 100 Hz ... 94 dB, minimum

Maximum Safe Differential Voltage without damage (Over-voltage protection) ... 130V RMS

Normal Mode Rejection at 50/60 Hz ..... 55 dB, minimum

Input Lead Resistance Effects ..... ±0.03/Ohm

Voltage Range Gain Drift, ... 45 ppm/°C, maximum

RTD Excitation Level ..... 0.4 mA

Gain Non-linearity ..... ± 0.01% of span

Gain Tempco ..... ± 25 ppm/°C

Digital Output ..... Degrees C or Degrees F

Digital Output Coding ..... 2's complement or sign and magnitude

Resolution ..... 12 bits plus sign and overrange

Conversion rate (Switch selectable) ..... 12.5 conversions/second at 50Hz NMR
15 conversions/second at 60Hz NMR
25 conversions/second at 50Hz NMR
30 conversions/second at 60 Hz NMR

Power Supply Requirements

With internal dc-to-dc Converter ..... +5V dc ±0.5% at 1.6 A
2.5 Amps maximum

Physical Characteristics

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight ..... 14.5 Oz (411 grams)

Operating Temperature Range .... 0 to + 60° C (+32 to +140° F)

Storage Temperature Range ..... -20 to +80° C (-4 to 176° F)

Relative Humidity non-condensing ..... 0 to 80%

Altitude ..... 0 to 15000 feet (4572 meters)

Table 1. RTD Functional Specifications

RTD TYPE	RANGE (°C)	NOTES
European Alpha of 0.00385	-200 to +850	Equivalent resistance of 18.49 to 390.26 Ohms
System Accuracy	-200 to 0 0 to +850	± 3 Degrees Celsius ± 1 Degree Celsius
American Alpha of 0.00392	-200 to +630	Equivalent resistance of 17.14 to 327.02 Ohms
System Accuracy	-200 to 0 0 to +630	± 3 Degrees Celsius ± 1 Degree Celsuis

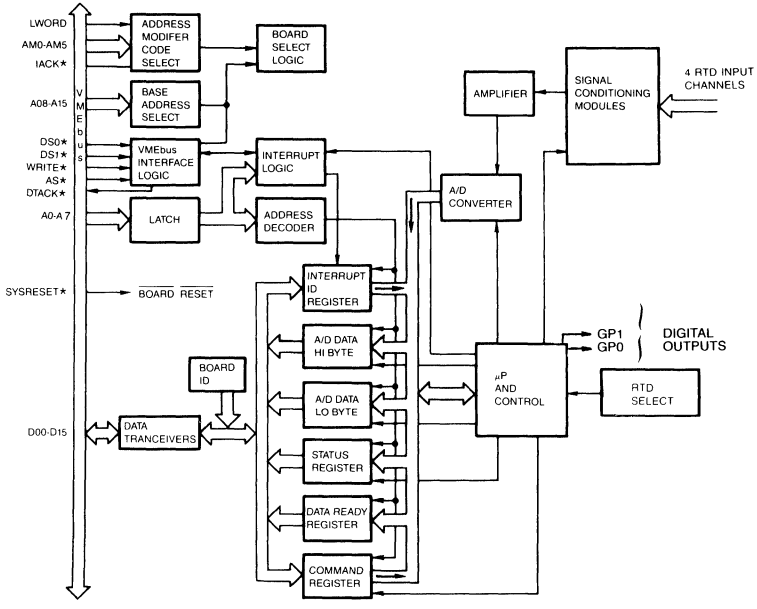

Figure 1. DVME-602R Functional Block Diagram

DVME-602R PROGRAMMING INFORMATION

The DVME-602R maps onto 256 consecutive bytes in the host system's address space. The address space essentially consists of the board ID number and registers. The registers are the command register, the status register, the A/D data register, the interrupt vector register, and the interrupt enable register. Table 2 lists the contents of the DVME-602R address space.

Table 2. DVME-602R Hardware registers

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 144	Write	Command register
Base + 144	Read	Status register
Base + 146	Read	A/D data register
Base + 148	Read/ Write	Interrupt vector register
Base + 150	Write	Interrupt enable register

Command Register

Programming this register selects the mode of scanning, mode of operation, output format, and PGA gain. Bits 0 and 7 of the status register monitor successful completion of the command. After entering the calibration mode, the gain and offset potentiometers may be adjusted on a per-channel basis. Figure 2 shows the command register format.

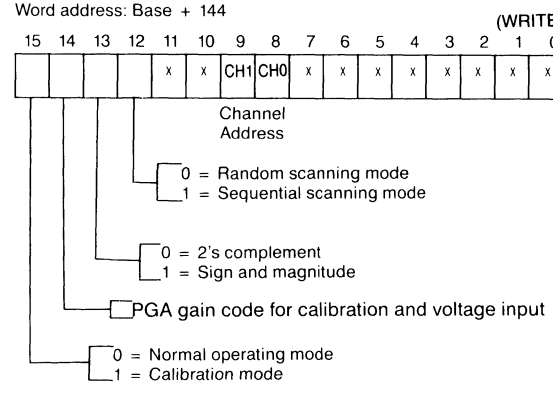

Figure 2. DVME-602R Command Register Format

Status Register

The contents of the status register indicate the channel selected, unit of temperature, and status of the A/D data and command registers. The bits 12 through 15 of this register indicate error conditions concerning open inputs, data out of range, and possible DVME-602R hardware failures. If the DVME-602R fails the self-test at power-up, the status bits indicate RAM or ROM failure and the BOARD OK lamp turns OFF. Figure 3 shows the format of the status register and Table 3 lists the error status conditions.

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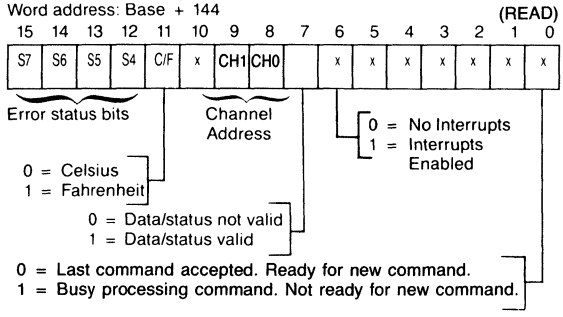


Figure 3. DVME-602R Status Register Format

Table 3. Error Status Conditions

Error Number S7	S6	S5	S4	Error
0	0	0	0	No error
1	0	0	0	Calibration mode
1	0	0	1	Data out of range
1	0	1	0	Open wire detection
1	0	1	1	Board not ready
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Memory or board failure

A/D Data Register

This register contains the binary data received from the selected channel after successful completion of a command. Bit 7 of the status register indicates the validity of the data. Depending the mode of operation, the data may be a raw reading from the A/D converter or the linearized data from a thermocouple input. Data in this register can exist in two formats, as defined by bit 13 of the command register. This bit sets up the data word as either a 16-bit 2's complement or a 15-bit number plus sign.

As a 2's complement word, 12 bits of data occupy bit locations 0 through 11. The sign bit (MSB) occupies bit location 12 and the sign is extended to fill the 16-bit register. Figure 4 shows the format of the A/D data register.

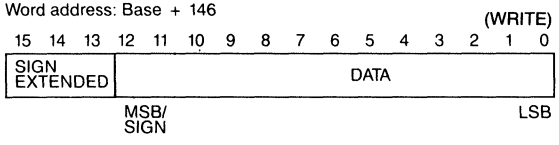


Figure 4. DVME-602R A/D Data Register 2's Complement

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines.

If the DVME-602R interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number onto the VMEbus (low byte). Figure 5 shows the format of the interrupt ID register.

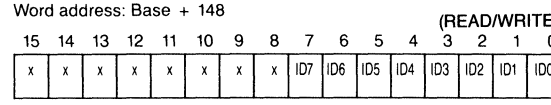


Figure 5. DVME-602R Interrupt ID Register Format

Interrupt Enable Register

The host system may program bit 6 of the interrupt enable register to enable the on-board interrupt. If this bit is set, the DVME-602R interrupts the host system when the A/D data is ready. The status of this bit is indicated in bit 6 of the status register. Bits 0 and 1 of the interrupt enable register are programmable to function as digital outputs. These outputs are provided on the digital output connector. Figure 6 shows the format of the interrupt enable register.

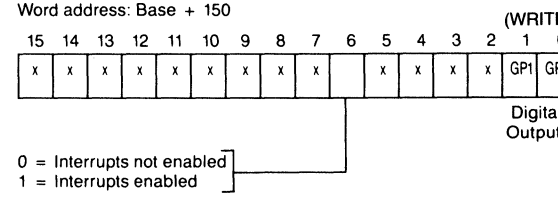


Figure 6. DVME-602R Interrupt Enable Register

I/O CONNECTIONS

The DVME-602R uses TB1 for analog input (J1) connections and TB2 for digital output (J2) connections. Table 4 lists input signals on the TB1 connector while Table 5 lists those on the TB2 connector.

Table 4. J1 Connector Signals (TB1)

Pin #	Signal	Pin #	Signal
1	N.C.	2	CHANNEL 3 LO IN
3	CHANNEL 3 HI IN	4	N.C.
5	CHANNEL 2 LO IN	6	CHANNEL 2 HI IN
7	N.C.	8	CHANNEL 1 LO IN
9	CHANNEL 1HI IN	10	N.C.
11	CHANNEL 0 LO IN	12	CHANNEL 0 HI IN

Table 5. J2 Connector Signals (TB2)

Pin #	Signal
1	DIGITAL GROUND
2	DIGITAL GROUND
3	DIGITAL OUTPUT 1
4	DIGITAL OUTPUT 0

RTD Input Range Selection

The DVME-620R board lets the user select between American and European Alpha coefficients for the type of RTD used in the application. Selection of the proper Alpha, and selection of the output temperature unit, is simple. A DIP switch on the board, S2, allows the user to select these options. Table 6 lists the proper S2 settings to implement these options.

Table 6. RTD Input Range/Output Range Selection

CHANNELS 0 THROUGH 3	S2-3	S2-4	S2-5	S2-10
American Alpha (0.00392)	OFF	OFF	ON	NA
European Alpha (0.00385)	ON	ON	ON	NA
Degrees Fahrenheit	NA	NA	NA	ON
Degrees Celsius	NA	NA	NA	OFF

NOTES

DVME-602R Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	0	
+ 1F	2	

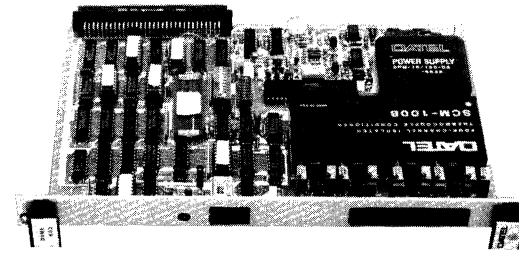
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611	DVME-611: 32 single-ended/ 16 differential channel A/D board
	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
	DVME-624	DVME-624: 4-channel isolated D/A board
	DVME-626	DVME-626: 6-channel, 16-bit D/A board
	DVME-628	DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-602T
ISOLATED THERMOCOUPLE 4-CHANNEL VMEbus A/D BOARD

FEATURES

- **4 A/D channels with high isolation (1000V peak).**
- **Fully hardware-compatible with VMEbus architecture**
- **Two models to measure a choice of inputs: DVME-602T for thermocouples and low-level inputs. DVME-602H for high-level and 4-to-20 mA inputs.**
- **On-board CPU for temperature calculations**
- **On-board linearization for J, K, T, S, B, E, and R type thermocouples**
- **On-board cold junction compensation**
- **Output in degrees Celcius or Fahrenheit**
- **13-bit resolution**



THE DVME-602T/602H ARE DATEL's HIGH-END A/D BOARDS SPECIFICALLY DESIGNED FOR THERMOCOUPLE AND HIGH-LEVEL INPUT MEASUREMENTS. BOTH BOARDS CONDITION SIGNALS FROM UP TO 4 CHANNELS AND PROVIDE LINEARIZED BINARY DATA TO A VMEbus-BASED HOST SYSTEM. THE DVME-602T MODEL IS PROGRAMMABLE TO PROVIDE OUTPUTS IN °C OR °F. DESIGNED FOR HOSTILE ENVIRONMENTS REQUIRING HIGH-ISOLATION, THESE BOARDS ARE IDEAL FOR MOST REAL-TIME DATA ACQUISITION AND CONTROL APPLICATIONS.

GENERAL DESCRIPTION

DATEL offers the DVME-602 A/D boards in two models. The model DVME-602T measures thermocouple and low-level inputs and the model DVME-602H measures high-level inputs. The intelligent A/D boards provide signal conditioning for up to four analog input channels. The microprocessor on the DVME-602T performs functions relating to linearization for J, K, T, S, B, E, and R type thermocouples. The output data is available as either a celcius or fahrenheit temperature range value. On-board switches let the user select the thermocouple type and the output unit of measurement.

Features include isolation, 50/60Hz rejection, and a 120 dB Common Mode Rejection Ratio. The on-board signal conditioning modules provide a minimum of 750V RMS isolation from channel-to-channel and channel-to-VMEbus. The high isolation protects the host system from high voltage damages if a thermocouple accidentally contacts a high voltage line. The boards' 120 dB CMRR allow thermocouple measurements even in the presence of high common mode voltages.

The DVME-602T also measures low-level ±25.6, ±51.2 and ±102.4 mV dc full-scale range analog signals from sources other than thermocouples, providing the raw, unlinearized A/D data to the host system.

An on-board cold junction compensation (CJC) circuit eliminates errors caused by temperature variations of the cold junction. The CJC is effective over a range of 0 to +60 °C. The DVME-602H offer ±5V dc and current loop signal input capability. The board is provided with an attenuation circuit for higher input voltage ranges.

The DVME-602T/602H hardware consists essentially of five sections: VMEbus interface section, microprocessor control section, A/D converter section, input signal conditioning section and the CJC section. An internal data bus links the control/data registers, A/D converter and the microprocessor. Figure 1 shows the DVME-602 functional block diagram.

The DVME-602 A/D boards will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the A/D boards. The user's manual also contains information on troubleshooting the boards.

The boards are shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted using VERSAdos (PDOS format also available). Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

NOTE:

References to the DVME-602 in this Data Sheet apply to both the DVME-602T and the DVME-602H.

ORDERING INFORMATION

DVME-602 —

- T = Thermocouple and low-level isolated inputs.
  Types J, K, T, S, B, E, and R.
  Low-level ranges: ±25.6 mV, ±51.2 mV and ±102.4 mV dc
- H = High-level voltage and current loop isolated inputs
  High-level voltage ranges: ±5V dc
  Current loop inputs: 4-to-20 mA
- R = RTD inputs**
- S = Strain gage inputs*
  (Consult factory for availability)

*See page 4

** Refer to the DVME-602R Data Sheet for specifications.

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VME Interface

The DVME-602 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to the address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-602 generates the data acknowledge (DTACK★) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK★ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes the VMEbus control lines WRITE★, DS0★, DS1★, and AS★ to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-602 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

VMEbus Interrupt Logic

The on-board microprocessor, at the end of linearization, generates an interrupt request on one of the VMEbus interrupt lines (IRQ1★ through IRQ7★). The interrupt line is jumper-selectable. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK★ and the daisy chain IACKIN★ signal lines. If the DVME-602 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number on to the VMEbus (low byte). The interrupt ID number is programmable by the host system. If the interrupt level on the address lines do not match, the board generates the daisy chain IACKOUT★ signal.

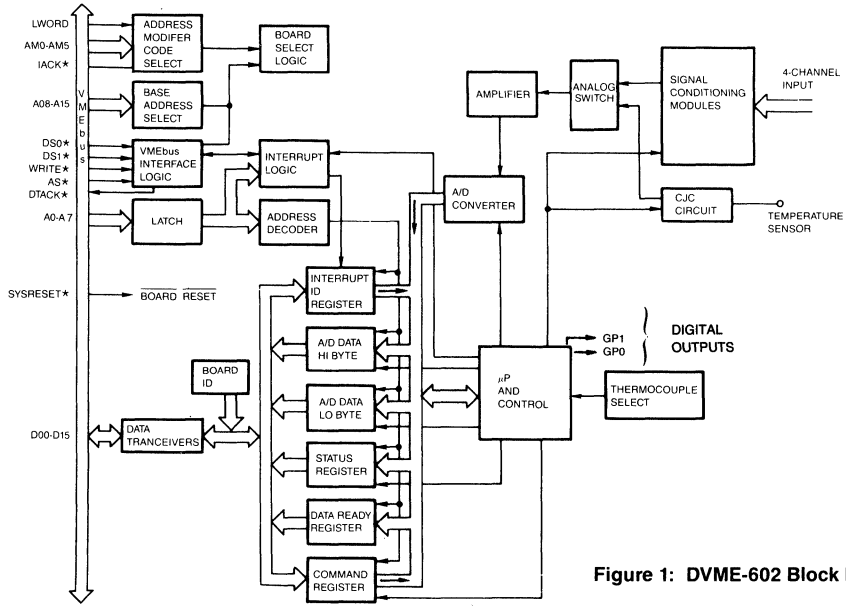

Figure 1: DVME-602 Block Diagram

FUNCTIONAL SPECIFICATION

(Typical at + 25 degrees Celcius, unless otherwise noted)

Interface specifications

Data Bus . . . . . 16 Bits

Address Bus . . . . . Short I/O Space 16 address lines

Address Modifier Codes . . . . . Codes used 29H, 2DH, 39H, and 3DH

Interrupts . . . . . 1 line, jumper-selectable.

Memory Mapping . . . . . Short I/O space, user or supervisor 256 words allocated per board.

Data Transfer . . . . . DTACK★ signal line. Notifies the VMEbus host that data has been placed or accepted from the VMEbus data lines.

The VMEbus SYSCLK signal is required.

CONNECTOR SPECIFICATIONS

VMEbus P1 connector . . . . . 96-pin male DIN connector.

J1 Analog Input Connector . . . . . Connects to a 12-pin terminal block. Use Phoenix Contacts MSTB 1.5/12-ST or equivalent.*

J2 Digital Output Connector . . . . . Connects to a 4-pin terminal block. Use Phoenix Contacts MSTB 1.5/4-ST or equivalent.*

*One mating connector supplied with each board.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

DVME-602 PROGRAMMING INFORMATION

The DVME-602 maps onto 256 consecutive bytes in the host system's address space. The address space essentially consists of the board ID number and registers. The registers are the command register, the status register, the A/D data register, the interrupt ID register and the interrupt enable register. Table 1 lists the contents of the DVME-602 address space.

Table 1: DVME-602 Hardware Registers

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 144	Write	Command register
Base + 144	Read	Status register
Base + 146	Read	A/D data register
Base + 148	Read/ Write	Interrupt ID register
Base + 150	Write	Interrupt enable register

Command Register

Programming this register selects the mode of scanning, mode of operation, coding, PGA gain code and CJC. The bits 0 and 7 of the status register monitor successful completion of the command. Figure 2 shows the command register format.

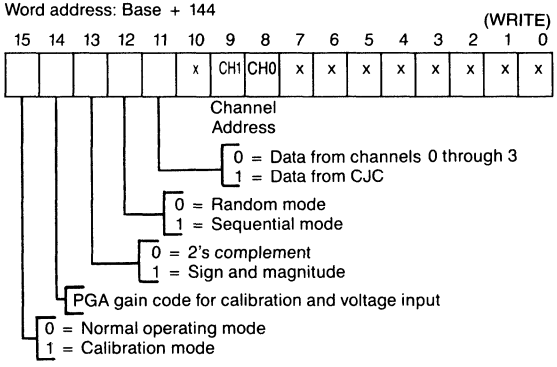

Figure 2: DVME-602 Command Register Format

Status Register

The contents of the status register indicate the channel selected, unit of temperature, and status of the A/D data and command registers. Bits 12 through 15 of this register indicate error conditions concerning open inputs, CJC and data out of range, and possible DVME-602 hardware failures. If the DVME-602 fails the self-test at power-up, the status bits indicate RAM or ROM failure and the BOARD OK lamp turns off. Figure 3 shows the format of the status register and Table 2 lists the error status conditions.

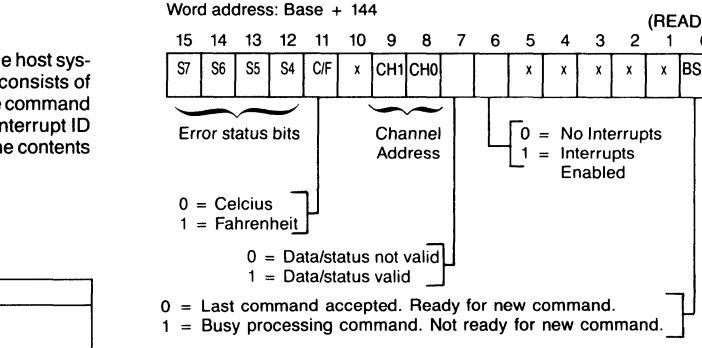

Figure 3: DVME-602 Status Register Format

Table 2: Error Status Conditions

Error Number S7	S6	S5	S4	Error
0	0	0	0	No error
1	0	0	0	Calibration mode
1	0	0	1	Data out of range
1	0	1	0	Open wire detection
1	0	1	1	Board not ready
1	1	0	0	CJC out of range
1	1	0	1	CJC and data out of range
1	1	1	0	CJC and open wire
1	1	1	1	Memory or board failure

A/D Data Register

This register contains the binary data received from the selected channel after successful completion of a command. Bit 7 of the status register indicates the validity of the data. Depending on the mode of operation, the data may be a raw reading from the A/D converter or the linearized data from a thermocouple input. Data in this register can exist in two formats, as defined by bit 13 of the command register. This bit sets up the data word in either a 2's complement of sign plus magnitude format. As a 2's complement word, 12 bits of data occupy bit locations 0 through 11. The sign bit (MSB) occupies bit location 12 and the sign is extended to fill the 16-bit register. Figure 4 shows the 2's complement format of the A/D data register.

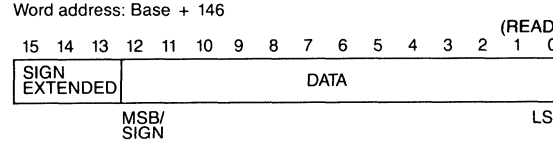

Figure 4: DVME-602 A/D Data Register 2's Complement Format

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Interrupt ID register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-602 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number onto the VMEbus (low byte). Figure 5 shows the format of the interrupt ID register.

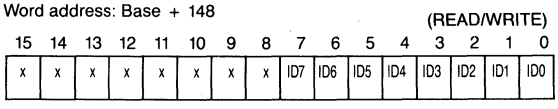

Figure 5: DVME-602 Interrupt ID Register Format

Interrupt Enable Register

The host system may program bit 6 of the interrupt enable register to enable the on-board interrupt. If this bit is set, the DVME-602 interrupts the host system when the A/D data is ready. The status of this bit is indicated in bit 6 of the status register. Bits 0 and 1 of the interrupt enable register are programmable to function as digital outputs. These outputs are provided on the digital output connector. Figure 6 shows the format of the interrupt enable register.

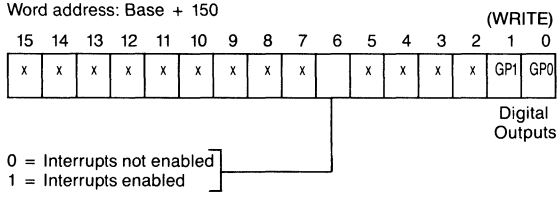

Figure 6: DVME-602 Interrupt Enable Register

I/O CONNECTIONS

The DVME-602 uses TB1 for analog input (J1) connections and TB2 for digital output (J2) connections. Table 3 lists input signals on the TB1 connector.

Table 3: J1 Connector Listing

Pin #	Signal	Pin #	Signal
1	-12V dc	2	CHANNEL 3 LO IN
3	CHANNEL 3 HI IN	4	-12V dc
5	CHANNEL 2 LO IN	6	CHANNEL 2 HI IN
7	-12V dc	8	CHANNEL 1 LO IN
9	CHANNEL 1 HI IN	10	-12V dc
11	CHANNEL 0 LO IN	12	CHANNEL 0 HI IN

Table 4: J2 Connector Listing

Pin #	Signal
1	DIGITAL GROUND
2	DIGITAL GROUND
3	DIGITAL OUTPUT 1
4	DIGITAL OUTPUT 0

FEATURES FOR RTD and STRAIN GAGE MODELS

DVME-602R

- 4 A/D channels
- RTD inputs
  A. 25 to 175Ω
  B. 0 to 350Ω
- Fully compatible with VMEbus hardware
- On-board signal conditioning
- On-board constant current excitation
- On-board source and lead wire compensation
- 130V maximum safe differential input voltage

DVME-602S

- 4 A/D channels
- Strain gage inputs
  A. ±30 mV dc
  B. ±100 mV dc
- Fully hardware-compatible with VMEbus hardware
- On-board signal conditioning
- 94 dB minimum CMRR
- ±0.02% maximum nonlinearity
- 130V maximum safe differential input voltage

ANALOG INPUT SPECIFICATIONS

Analog Input channels.....4

Input configuration.....Differential

Input types.....Thermocouples, low-level, High-level and 4-to-20 mA current loops

Isolation, channel-to-channel and channel-to-bus, AC or dc.....1000V, Peak maximum

Input Impedance.....100 Megohms, minimum

Input Bias Current.....8 nanoamps, maximum

Common Mode Voltage Range, channel-to-channel and channel-to-VMEbus AC, 50 or 60 Hz.....750V RMS, minimum 1000V peak, maximum

Common Mode Rejection Ratio, minimum (Rs = 1k, f=0.01 to 100 Hz)

DVME-602T.....120 dB, minimum
DVME-602H.....110 dB, minimum

Maximum Safe Differential Voltage without damage (Overvoltage protection)...130V RMS

Normal Mode Rejection at 50/60 Hz...55 dB, minimum

Input Lead Resistance Effects.....None

Voltage Input Ranges

DVME-602T..... ±25.6mV dc
±51.2mV dc
±102.4mV dc

DVME-602H..... ±5.12V dc

Voltage Range Accuracy

DVME-602T.....0.03% FSR, minimum
DVME-602H.....0.1% FSR, minimum

Voltage Range Gain Drift,....45 ppm/ °C, maximum

Input Voltage Range Offset Drift

Model Number	Input Range	Offset Drift
DVME-602T	±25.6mV dc	3μV/ °C
	±51.2mV dc	3μV/ °C
	±102.4mV dc	3.5μV/ °C
DVME-602H	±5.12V dc	70μV/ °C

Time and Temperature Related Drift

Thermocouple Type	Time related drift (°C/6 months)	Temperature related drift (°C/°C)
J	± 0.2	± 0.1
K	± 0.25	± 0.15
S	± 1.0	± 0.3
T	± 0.25	± 0.1
E	± 0.2	± 0.15
R	± 0.8	± 0.3
B	± 1.0	± 0.3

Digital Output.....Degrees C or degrees F

Digital Output Coding.....2's complement or sign and magnitude

Resolution..... 12 bits plus sign and overrange

Conversion rate (Switch-selectable).....12.5 conversions/second at 50Hz NMR
15 conversions/second at 60Hz NMR
25 conversions/second at 50Hz NMR
30 conversions/second at 60Hz NMR

CJC Error
Room temperature.....±0.5 °C
Full temperature range....±1.5 °C

Power Supply Requirements

With internal dc-to-dc Converter.....+5V dc ±0.5% at 1.6 A

Thermocouple Input Ranges and Accuracy (Maximum)

Thermocouple Type	Temperature Range (°C)	Input Voltage Range (mV)	Accuracy (°C)
J	−200 to 0	−7.890 to −4.632	±3
	0 to +760	−4.632 to +42.922	±1
K	−200 to −100	−5.891 to −3.553	±3
	−100 to +1232	−3.553 to +49.988	±1
S	0 to +300	0.000 to +2.323	±6
	+300 to +1768	+2.323 to +18.698	±3
T	−200 to 0	−5.603 to 0.000	±3
	0 to +400	0.000 to +20.869	±1
E	−270 to −200	−9.835 to −8.824	±10
	−200 to 0	−8.824 to 0.000	±3
	0 to +1000	0.000 to +76.358	±1
R	0 to +300	0.000 to +2.400	±4
	+300 to +1768	+2.400 to +21.108	±2
B	+300 to +500	+0.431 to +1.241	±5
	+500 to +1000	+1.241 to +4.833	±3
	+1000 to +1820	+4.833 to +13.814	±2

Physical Characteristics

Outline Dimensions.....9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight.....14.5 Oz. (411 grams)

Operating Temperature Range.....0 to +60 °C

Storage Temperature Range. −20 to +80 °C

Relative Humidity non-condensing.....0 to 80%

Altitude.....0 to 15000 feet (4572 meters)

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DVME-602T Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	0	
+ 1F	2	

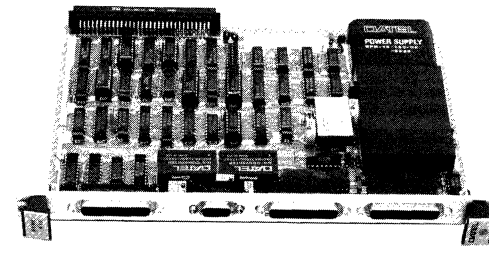
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611	DVME-611: 32 single-ended/ 16 differential channel A/D board
	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
	DVME-624	DVME-624: 4-channel isolated D/A board
	DVME-626	DVME-626: 6-channel, 16-bit D/A board
	DVME-628	DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-611/612
32S/16D-CHANNEL
VME A/D-D/A BOARDS

FEATURES:

- **Two models of VMEbus-based boards:**
  DVME-611: 32 single-ended/16 differential A/D channels
  DVME-612: 32 single-ended/16 differential A/D channels and 2 D/A channels
- **Five levels of resolutions available:**
  A. 12-bit/20 μS
  B. 12-bit/4 μS
  C. 16-bit/35 μS
  D. 16-bit/400 mS
  E. 12-bit/2 μS
- **Four input voltage ranges available: ±10V, ±5V, 0 to 5V, and 0 to 10V dc**
- **Three types of output coding:**
  A. Bipolar 2's complement
  B. Bipolar offset binary
  C. Unipolar straight binary
- **Up to 160,000 conversions per second throughput.**
- **Fast throughput mode for high-speed data transfers**
- **On-board interrupt vector register for host system's service routines.**
- **Up to 0.0063% full-scale range accuracy**
- **±1/2 LSB linearity error**
- **80 dB CMRR at gain of 128**



- **Eight-stage programmable gain amplifier (PGA)**
- **±0.05% full-scale range accuracy for D/A channels**
- **Channel expansion boards for up to 256 channels:**
  DVME-641: Non-isolated, high-level inputs
  DVME-643: Isolated, thermocouple, RTD, high-level, 4-to-20mA inputs
  DVME-645: Simultaneous sample/hold inputs
- **Two TTL digital outputs**

DATEL's DVME-611/612 ARE HIGH-PERFORMANCE A/D BOARDS OFFERING SAMPLING RATES OF UP TO 160kHz SAMPLING. DESIGNED FOR VMEbus SYSTEMS, THE PRODUCT LINE INCLUDES MODELS WITH DIFFERENT A/D CONVERTER RESOLUTIONS. WITH HIGH-SPEED REAL-TIME DATA ACQUISITION APPLICATIONS IN MIND, THE DVME-611/612 BOARDS ARE IDEAL CHOICES FOR PROCESS CONTROL, TEST AND MEASUREMENT AND OTHER RELATED INDUSTRIAL APPLICATIONS.

GENERAL DESCRIPTION

The DVME-611/612 are DATEL's VMEbus based high-end A/D conversion boards. The A/D boards provide up to 16-bit binary data from up to 32 single-ended or 16 differential analog input channels. DATEL offers optional expansion boards for up to 256 single-ended or differential analog input channels. The DVME-612 is also equipped with two D/A channels, operable in four output voltage ranges.

The on-board hardware essentially consists of multiplexers, a PGA, an A/D converter and registers. The PGA is programmable for gains from 1 to 128 in binary increments. Both the DVME-611 and the DVME-612 are available in four models depending upon the A/D converter module used. The A/D converter modules are easily field-replaceable. All models except the DVME-611D and the DVME-612D contain a sample/hold amplifier.

The host programmable command register controls the A/D conversion process. Depending upon the contents of the command register, an external trigger may also initiate the A/D conversion process. The host system may obtain the information pertaining to the A/D conversion and control selections using the status register.

For an intelligent A/D board (local 68010, dual-port RAM, RS-232, etc.), see model DVME-601)

ORDERING INFORMATION

DVME-611	A — 12-bit/20 μS ADC B — 12 bit/4 μS ADC
DVME-612	C — 16-bit/35 μS ADC D — 16-bit/400 mS E — 12-bit/2 μS ADC

Optional Multiplexer Expansion Boards (See Page 4)

DVME-641 — 32S/16D-Channel high-level non-isolated inputs.

DVME-643 — 8D-Channel isolated inputs.

DVME-645 — 16S/8D-Channel simultaneous sample/hold high-level non-isolated inputs.

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

Contact DATEL for unipolar models DVME-611/612B-U or 611/612C-U under special order.

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The channel and control information from the channel select logic section is brought out to the J4 expansion connector. The control lines include End of Conversion (EOC), End of Scan (EOS), settling time delay and external trigger signals. These control signals on the expansion connector are also usable with externally multiplexed input channels. The start and final channels for A/D scanning process are selected by the host system.

On-board jumpers allow coding the digital output data in bipolar 2's complement, offset binary, or unipolar straight binary format. The analog output section on the DVME-612 offers ±1/2 LSB differential non-linearity and operates at ±0.05% of full-scale range accuracy.

Functionally, the analog signal from the input channels is amplified and converted into binary data. The resolution depends on the A/D converter module used. Figure 1 shows the functional block diagram of the DVME-611/612 A/D boards. Data from the A/D converter module is coded into straight binary, offset binary, or 2's complement coding. The binary A/D data is transferred to the host system through the VMEbus transceivers.

For applications requiring fast data transfers, the DVME-611/612 A/D boards can operate in fast throughput mode. This mode is selectable using the command register. The fast throughput mode guarantees transfer of A/D data on to the VMEbus without having to test the conversion status. This mode delays the host CPU DTACK* while EOC = 0 when A/D data is read.

The DVME-611/612 A/D boards come with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the A/D boards. The user's manual also contains information on troubleshooting the boards.

The boards are shipped with an example 68010 assembly language using VERSAdos. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats. The diagnostic program is also available in hard copy from DATEL. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

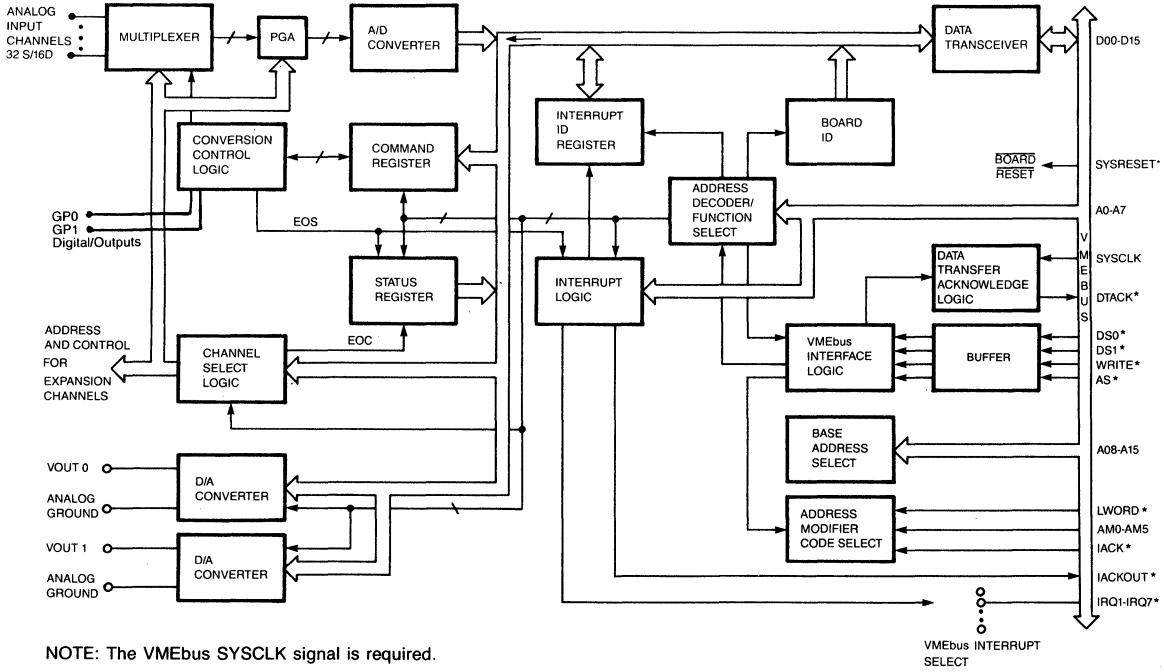
VME Interface

The DVME-611/612 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-611/612 generates the data acknowledge (DTACK★) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK★ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE★, DS0★, DS1★, and AS★) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-611/612 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

VMEbus Interrupt Logic

The interrupt logic section senses an EOC or EOS condition and generates an interrupt request on one of the VMEbus interrupt lines (IRQ1★ through IRQ7★). The interrupt line is jumper-selectable. The interrupt logic accepts IACK★ and IACKIN★ signals from the host system as interrupt acknowledge and daisy chain input signals. Depending upon the interrupt level, the on-board logic loads the interrupt ID number on to the VMEbus or generates the daisy chain IACKOUT★ signal.



NOTE: The VMEbus SYSCLK signal is required.

Figure 1: DVME-611/612 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

Interface specifications

Data Bus	16 Bits. (A16:D16 slave)
Address Bus	Short I/O Space 16 address lines
Address Modifier Codes	Codes used 29H, 2DH, 39H, and 3DH
Interrupts	1 line, jumper-selectable 2 interrupt ID's for EOC and EOS Software programmable
Memory Mapping	Short I/O space, user or supervisor 256 words allocated per board
Data Transfer	DTACK* signal line Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines.

CONNECTOR SPECIFICATIONS

VMEbus P1 connector	96-pin male DIN connector
J1 and J2 Analog Input Connectors	25-pin D-type female connectors
J3 Analog Output Connector	9-pin D-type female connector
J4 Analog Expansion Connector	25-pin D-type female connector

ANALOG SPECIFICATIONS

ANALOG INPUT

Number of Channels	32 single-ended or 16 differential
Channel Expansion	256 single-ended or differential; requires external multiplexing. Use DATEL's DVME-641, DVME-643, or DVME-645 mux boards.
Input Configuration	Single-ended or differential.
Input Ranges	±10V, ±5V, 0 to 5V, or 0 to 10V, jumper-selectable.
Digital Output Coding	
DVME-611/612A	Unipolar and Bipolar (jumperable).
DVME-611/612B **DVME-611/612C** **DVME-611/612D** **DVME-611E/612E**	Bipolar (For Unipolar coding consult the factory)

Resolution and Throughput

	Resolution in bits	Conversion time	Throughput conversions/sec.
DVME-611A/DVME-612A	12	20 μS	40,320
DVME-611B/DVME-612B	12	4 μS	160,000*
DVME-611C/DVME-612C	16	35 μS	18,667
DVME-611D/DVME-612D	16	400 mS	2.5
DVME-611E/612E	12	2 μS	see notes

External Trigger	TTL compatible, negative going edge. Minimum pulse width=100 nS Maximum pulse width=2 μS
Programmable Gain Amplifier	Uses an AM-543MC for gains of X1, X2, X4, X8, X16, X32, X64, X128
Common Mode Voltage	±10V dc, maximum, non-isolated
Input Bias Current	8 nA, maximum
Over Voltage Protection	±35V dc, maximum
Input Impedance Differential to ground	10 megohms, minimum
Common Mode Rejection for ±10V input signal at 60Hz, minimum	75 dB at a gain of 2 80 dB at a gain of 128

Full-Scale Range Accuracy, minimum

DVME-611A/DVME-612A **DVME-611E/612E**	.025% at a gain of 1 .20% at a gain of 128
DVME-611B/DVME-612B	.05% at a gain of 1 .20% at a gain of 128
DVME-611C/DVME-612C	.010% at a gain of 1 .20% at a gain of 128
DVME-611D/DVME-612D	.0063% at a gain of 1 .20% at a gain of 128

Temperature Drift and Linearity

	Gain Temperature Coefficient (ppm/°C)	Zero Temperature Drift, (ppm/°C)	Linearity Error, maximum
DVME-611A/612A	+/−20	20	½ LSB
DVME-611B/612B	+/−20	20	1 LSB
DVME-611C/612C	+/−20	20	½ LSB
DVME-611D/612D	+/−10	10	2 LSB
DVME-611E/612E	±20	±20	½ LSB

PGA plus MUX Settling Time, maximum

8 μS at a gain of 1
12 μS at a gain of 16
40 μS at a gain of 64
100 μS at a gain of 128

Minimum conversion time required for step input at rated accuracy, typical

DVME-611A/DVME-612A	20 μS at a gain of 1 110 μS at a gain of 128
DVME-611B/DVME-612B	8 μS at a gain of 1 102 μS at a gain of 128
DVME-611C/DVME-612C	35 μS at a gain of 1 110 μS at a gain of 128
DVME-611D/DVME-612D	400 mS at a gain of 1 400 mS at a gain of 128

Actual Conversion Time

DVME-611A/DVME-612A	20 μS, typical 25 μS, maximum
DVME-611B/DVME-612B	4 μS, typical 5 μS, maximum
DVME-611C/DVME-612C	35 μS typical 45 μS, maximum
DVME-611D/DVME-612D	200 mS, typical 400 mS, maximum

*Single channel, gain = 1, convert-on-read

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Optional Multiplexer Expansion Boards

Model	Number of expansion channels		Input type
	Single-ended	Differential	
DVME-641	32	16	High-level, non-isolated
DVME-643T	-	8	Thermocouple Isolated
DVME-643H	-	8	High-level Isolated
DVME-643R	-	8	RTD
DVME-643S	-	8	Strain Gage
DVME-645	16	8	Simultaneous Sample/Hold high-level non-isolated

ANALOG OUTPUT (For DVME-612 models only)

Number of Channels	2
Output Range	±10V, ±5, 0 to 5, or 0 to 10V
Digital Input Coding	Bipolar 2's complement, bipolar offset binary or unipolar straight binary
Resolution	12 Bits, bits D0 through D3 not used
Reset	Minus full-scale, −10V for 2's complement and offset binary 0V for Unipolar
Full-Scale Range Accuracy	.05%, minimum
Differential Non-linearity	.5 LSB, minimum
Zero Temperature Drift	5 ppm/°C, maximum
Offset Temperature Drift	20 ppm/°C, maximum
Gain Temperature Drift	20 ppm/°C, maximum
Settling time	10 μS, maximum
Output Current	5 milliamps, typical
Output Impedance	50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±5% at 2.5 Amperes
On-board dc-to-dc converter generates ±15V dc for the DVME-611/612 logic circuits

PHYSICAL—ENVIRONMENTAL

Outline Dimensions	9.19″W x 6.3″D x 0.6″H (233.5 x 160 x 15.24 mm)
Weight	1 lb 0.5 oz (467.8 Grams)
Operating Temperature Range	0 to 60°C
Storage Temperature Range	-20 to 80°C
Relative Humidity	0 to 90%, non-condensing

DVME-611/612 PROGRAMMING INFORMATION

The DVME-611/612 A/D boards use ten registers for data acquisition and control purposes. Table 1 lists the DVME-611/612 registers and their base address offsets. These registers are addressable locations in the host system's address space.

Table 1: DVME-611/612 Hardware Register Functions

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 128	Write	Command register
Base + 128	Read	Status register
Base + 130	Write	Interrupt ID register
Base + 132	Write	EOC/EOS F/F Reset
Base + 134	Write	Gain register
Base + 136	Write	Start channel register
Base + 136	Read	Current channel register
Base + 138	Write	Final channel register
Base + 140	Write	Start conversion register
Base + 140	Read	A/D data register
Base + 142	Read	Status register
Base + 160	Write	D/A channel 0
Base + 162	Write	D/A channel 1

Command Register

The 16-bit command register controls how the DVME-611/612 boards scan their selected channels. Programming the command register selects the modes for starting conversion, calibration, and fast throughput. This register also enables the interrupt, channel address auto-increment, and channel rescan capabilities. Figure 2 shows the command register format.

Status Register

The DVME-611/612 status register indicates conditions relating to conversion status, channel scanning information, and modes selected. Figure 3 shows the status register format.

Total System Throughput

Total sample-to-sample throughput rate depends on the A/D-S/H settling and conversion period and the user's software period. During this software interval, data is transferred to the host and the next A/D conversion is started. By combining fast throughput mode (DTACK* EOC holdoff) with convert-on-read-data, throughput over 160 kHz may be achieved for gain = 1 in single channel mode. Data transfer and host memory pointer management may partially overlap A/D conversion by using the convert-on-read mode.

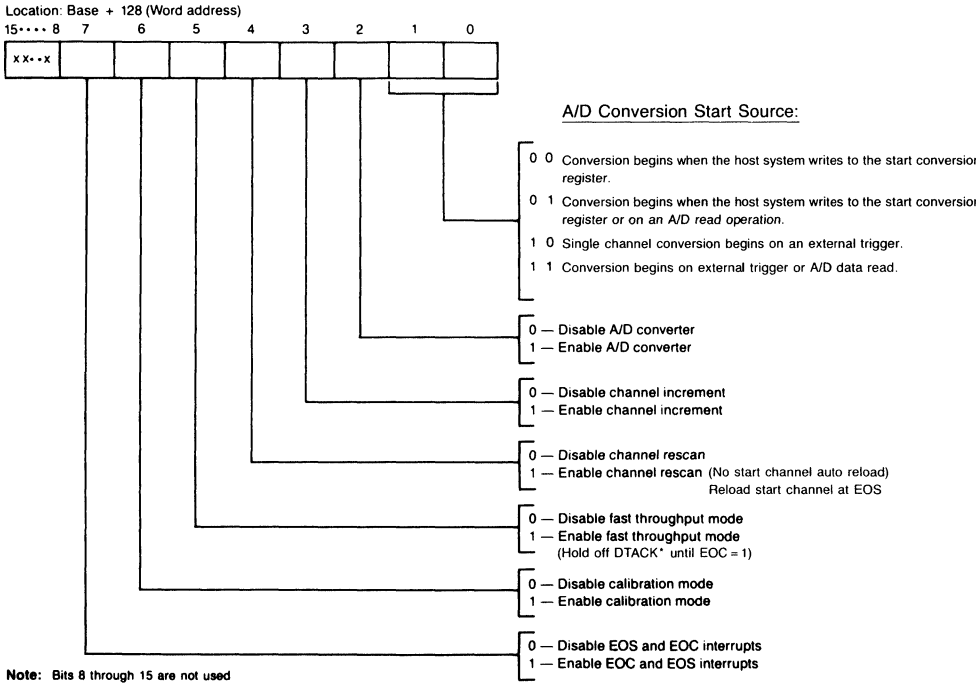

Figure 2: DVME-611/612 Command Register Format (WRITE)

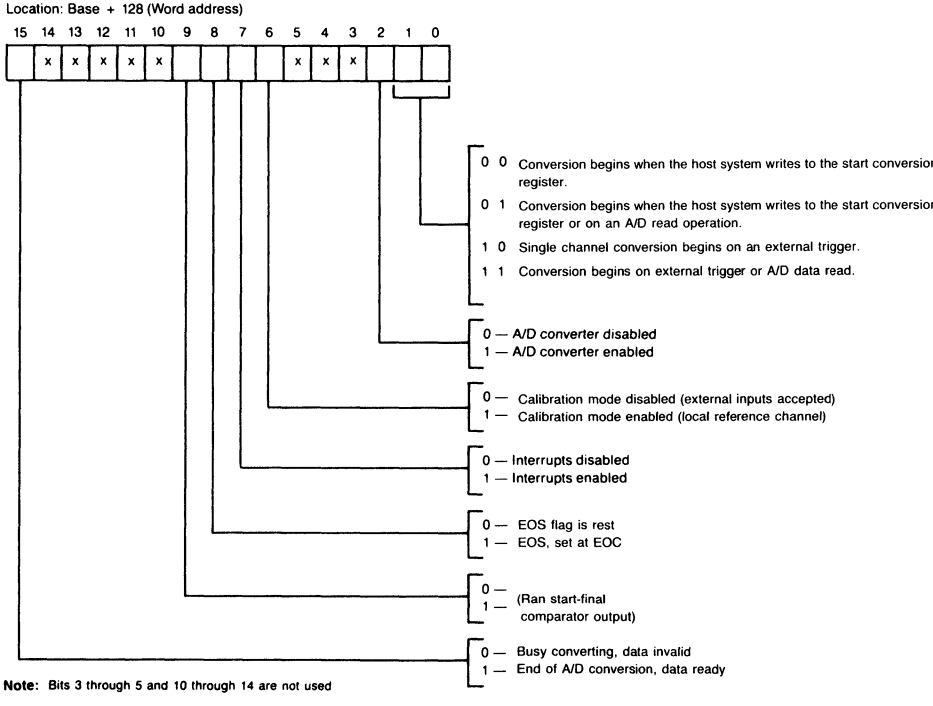

Figure 3: DVME-611/612 Status Register Format (READ)

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-611/612 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number on to the VMEbus (low byte). If the EOC/EOS interrupts and the multiple channel scan option are enabled, the board loads the ID number plus one on to the VMEbus data lines. The host system may use these ID's to differentiate the EOC and EOS interrupts. Figure 4 shows the register format of the interrupt ID register.

Word address: Base + 130 (Write) X = Don't Care

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	ID7	ID6	ID5	ID4	ID3	ID2	ID1	0

Figure 4: Interrupt ID Register Format

Gain Register and Digital Outputs

The least three significant bits of this register, when programmed, assign the gain to the differential amplifier in the PGA section. This register is programmable for gains from 1 to 128 in binary increments. Bits 6 and 7 of this register provide a general purpose digital output. The output signal lines from these two bits are available on pins 18 and 6 of the J4 connector. Figure 5 shows the gain register format.

Word address: Base + 134 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	GP1	GP0	x	x	x	G2	G1	G0

Figure 5: Gain Register Format

Start Channel/Current Channel Register

User must load this register with the starting channel address when scanning a group of channels. This register contains the address of the channel being scanned. Figure 6 shows the format of this register.

Word address: Base + 136 (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 6: Start Channel/Current Channel Register

Final Channel Register

User must load this register with the final channel address when scanning a group of channels. The on-board comparator compares this register contents with the current channel register and generates the end of scan (EOS) signal. Figure 7 shows the format of this register.

Word address: Base + 138 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 7: Final Channel Register Format

Start Conversion Register

Writing any value to this register starts an A/D conversions on the channel indicated by the current channel register. Figure 8 shows the format of this register.

Word address: Base + 140 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 8: Start Conversion Register Format

A/D Data Register

The 16 bits of the A/D data register are connected to 16 VMEbus data lines. The host system may read this register to obtain the binary data of the analog input from the channel selected. Models DVME-611/612 A and B do not use the four least significant data bits. The value of these bits defaults to zero for these models. Figure 9 shows the format of this register.

Word address: Base + 140 (Read)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16

MSB LSB

Figure 9: A/D Register Format

D/A Channel Registers

The DVME-612 boards have two D/A channel registers. These registers form the input to the 12-bit hybrid D/A converters. These registers are programmable by the most significant 12 bits from the VMEbus data lines. Figure 10 shows the format of these registers.

Word address: Base + 160 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10a: D/A Channel 0 Register Format

Word address: Base + 162 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10b: D/A Channel 1 Register Format

EOC/EOS F/F Register

Writing any value to this register resets the EOC/EOS flip-flops. Figure 11 shows the format of this register.

Word address: Base + 132 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 11: EOC/EOS F/F Register Format

(These F/F's are also reset by the next start of conversion.)

I/O Connections

The DVME-611/612 A/D boards use the J1 and J2 connectors for analog input connections and the J4 connector for channel expansion. The DVME-612 uses the J3 connector for analog output connections. Tables 2, 3, 4, and 5 list the I/O signals of the J1, J2, J3, and J4 connector respectively.

Table 2: DVME-611/612 Analog Input Connector-J1

	CONFIGURATION	
PIN #	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 0 IN	CHANNEL 0 HIGH
12	CHANNEL 16 IN	CHANNEL 0 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 1 IN	CHANNEL 1 HIGH
23	CHANNEL 17 IN	CHANNEL 1 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 2 IN	CHANNEL 2 HIGH
9	CHANNEL 18 IN	CHANNEL 2 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 3 IN	CHANNEL 3 HIGH
20	CHANNEL 19 IN	CHANNEL 3 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 4 IN	CHANNEL 4 HIGH
6	CHANNEL 20 IN	CHANNEL 4 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 5 IN	CHANNEL 5 HIGH
17	CHANNEL 21 IN	CHANNEL 5 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 6 IN	CHANNEL 6 HIGH
3	CHANNEL 22 IN	CHANNEL 6 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 7 IN	CHANNEL 7 HIGH
14	CHANNEL 23 IN	CHANNEL 7 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 4: DVME-612 Analog Output Connector-J3

PIN #	SIGNAL LINE
1	CHANNEL 0 VOUT
6	ANALOG RETURN
4	CHANNEL 1 VOUT
9	ANALOG RETURN

Table 3: DVME-611/612 Analog Input Connector-J2

	CONFIGURATION	
PIN #	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 8	CHANNEL 8 HIGH
12	CHANNEL 24	CHANNEL 8 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 9	CHANNEL 9 HIGH
23	CHANNEL 25	CHANNEL 9 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 10	CHANNEL 10 HIGH
9	CHANNEL 26	CHANNEL 10 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 11	CHANNEL 11 HIGH
20	CHANNEL 27	CHANNEL 11 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 12	CHANNEL 12 HIGH
6	CHANNEL 28	CHANNEL 12 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 13	CHANNEL 13 HIGH
17	CHANNEL 29	CHANNEL 13 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 14	CHANNEL 14 HIGH
3	CHANNEL 30	CHANNEL 14 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 15	CHANNEL 15 HIGH
14	CHANNEL 31	CHANNEL 15 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 5: DVME-611/612 Expansion Connector-J4

PIN #	SIGNAL LINE
13	EXTERNAL CHANNEL ADDRESS 0 OUT
25	EXTERNAL CHANNEL ADDRESS 1 OUT
12	EXTERNAL CHANNEL ADDRESS 2 OUT
24	EXTERNAL CHANNEL ADDRESS 3 OUT
11	EXTERNAL CHANNEL ADDRESS 4 OUT
23	EXTERNAL CHANNEL ADDRESS 5 OUT
10	EXTERNAL CHANNEL ADDRESS 6 OUT
22	EXTERNAL CHANNEL ADDRESS 7 OUT
16	DIGITAL GROUND
9	EXTERNAL CHANNEL ADDRESS VALID OUT
8	START CONVERSION STROBE OUT
20	SETTLING DELAY* IN
7	END OF CONVERSION OUT
19	END OF SCAN OUT
17	EXTERNAL TRIGGER IN*
18	GENERAL PURPOSE OUTPUT 0
6	GENERAL PURPOSE OUTPUT 1
4	DIGITAL GROUND
21	RESERVED
5	RESERVED
1	EXTERNAL ANALOG LOW IN
14	EXTERNAL ANALOG HIGH IN
2, 15	ANALOG COMMON
3	+5V dc REFERENCE OUT

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DVME-611/612 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	1	
+ 1F	1 or 2	

Fast Throughput Mode

This mode holds off response of the DTACK* VMEbus signal with the simultaneous ANDing of three conditions: command register bit 5 = 1, EOC = 0 and a host read of the A/D data register. While DTACK* is held off, the host CPU executes wait states. When A/D conversion finishes, EOC = 1 and DTACK* is released. Normally the attempted A/D data read now completes, and data is transferred without any EOC polling. Fast throughput should be used with caution since the host must be completely dedicated to A/D data acquisition.

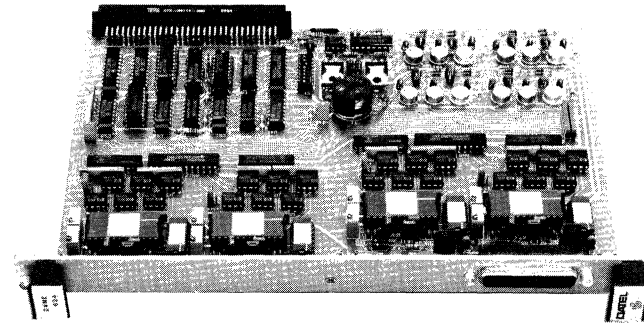
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gages, high-level, low-level, and 4-to-20mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-624
ISOLATED 4-CHANNEL, 12-BIT, VMEbus D/A BOARD

FEATURES

- 4-Channel memory mapped D/A board
- 300 VRMS channel-to-channel and channel-to-bus isolation
- Hardware compatible with VMEbus specifications
- On-board isolated dc-to-dc power converter
- Optional 6 μS or 30 μS settling time models
- 12-Bit resolution
- Choice of output voltages:
  a. 0 to 5V dc
  b. 0 to 10V dc
  c. ±2.5V dc
  d. ±5V dc
  e. ±10V dc
- Optional 4-to-20mA current loop capability conforming to ISA standards
- ±1/2 LSB differential non-linearity
- ±0.05% Full-scale range accuracy



GENERAL DESCRIPTION

The DVME-624 is DATEL's 12-bit, 4-channel D/A board, totally compatible with VMEbus specifications. In a typical application the board provides analog outputs in real-time to the host system at a high speed. The different full-scale output voltage ranges the board offers conform to process control and test and measurement industrial requirements.

Each channel is configurable to different output voltage ranges. The salient feature of the DVME-624 board is the 300 VRMS channel-to-channel and channel-to-bus isolation. The board uses high performance optoisolators to provide the isolation. An on-board dc-to-dc power converter provides isolated power to each D/A converter section.

The isolation makes the DVME-624 an ideal choice for applications where a low-level signal superimposes a high voltage such as in testing of power supplies. The channel-to-bus isolation protects the host system against any catastrophic damages due to an external malfunction such as an actuator failure.

The DVME-624 offers ±1/2 LSB differential non-linearity and operates at ±0.05% full-scale range accuracy. The DVME-624 models are available at two different settling times. The lower cost DVME-624C1 and DVME-624V1 models offer 30 μS settling time and the DVME-624C2 and DVME-624V2 models offer 6 μS settling time. The DVME-624 may be obtained with an optional 4-to-20mA industrial current loop output in addition to the voltage outputs. Refer to the ordering information for models with current loop option.

Functionally, the digital data from the VME host system is transferred through a 12-bit data register to one-of-four D/A sections. The DVME-624 converts the 12 most significant bits from the VME data bus to an analog output. Data from the host system may be in straight binary, offset binary, or 2's complement coding. The D/A converter sections are optically isolated from the VME interface logic. The DVME-624 uses monolithic D/A converters to increase the product's reliability and endurance.

The DVME-624 D/A boards will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the DVME-624. The DVME-624 is shipped with an 68010 assembly language diagnostic program example on a 5 1/4" VERSAdos formatted diskettes. Consult factory regarding the availability of the diagnostic program's source code in other disk formats.

ORDERING INFORMATION

DVME-624

- 1 — 30 μS Settling time
- 2 — 6 μS Settling time
- V — Voltage output only
- C — Voltage and 4-to-20 mA current loop output

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VME Interface

The DVME-624 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to the address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-624 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems. Figure 1 shows the functional block diagram of the DVME-624 D/A board.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, V_{exc} = +24V dc, R_{loop} = 250 ohms, unless otherwise specified.)

INTERFACE SPECIFICATIONS

Data Bus	16 bits
Address Bus	Short I/O Space, 16 address lines
Address modifiers codes	Codes used 29H, 2DH, 39H, and 3DH
Memory Mapping	Short I/O space, user or supervisor 256 bytes allocated per board (A16:D16 slave).

INTERNAL HARDWARE REGISTER/SOFTWARE ASSIGNMENTS

Register Memory Mapping

Relative Address	Function	READ/WRITE
0 through 63	Board Identification Code	Read Only
64 through 127	See Note 1	Read Only
128 through 159	See Note 2	Write Only
160	D/A Channel 0	Write Only
162	D/A Channel 1	Write Only
164	D/A Channel 2	Write Only
166	D/A Channel 3	Write Only
168 through 255	See Note 2	Write Only

Note 1: These addresses are redundant with ID PROM addresses, base + 0 through base + 63.

Note 2: These addresses are redundant in 8-byte blocks with the DAC data registers, base + 160 through base + 166.

The VMEbus SYSCLK signal is required.

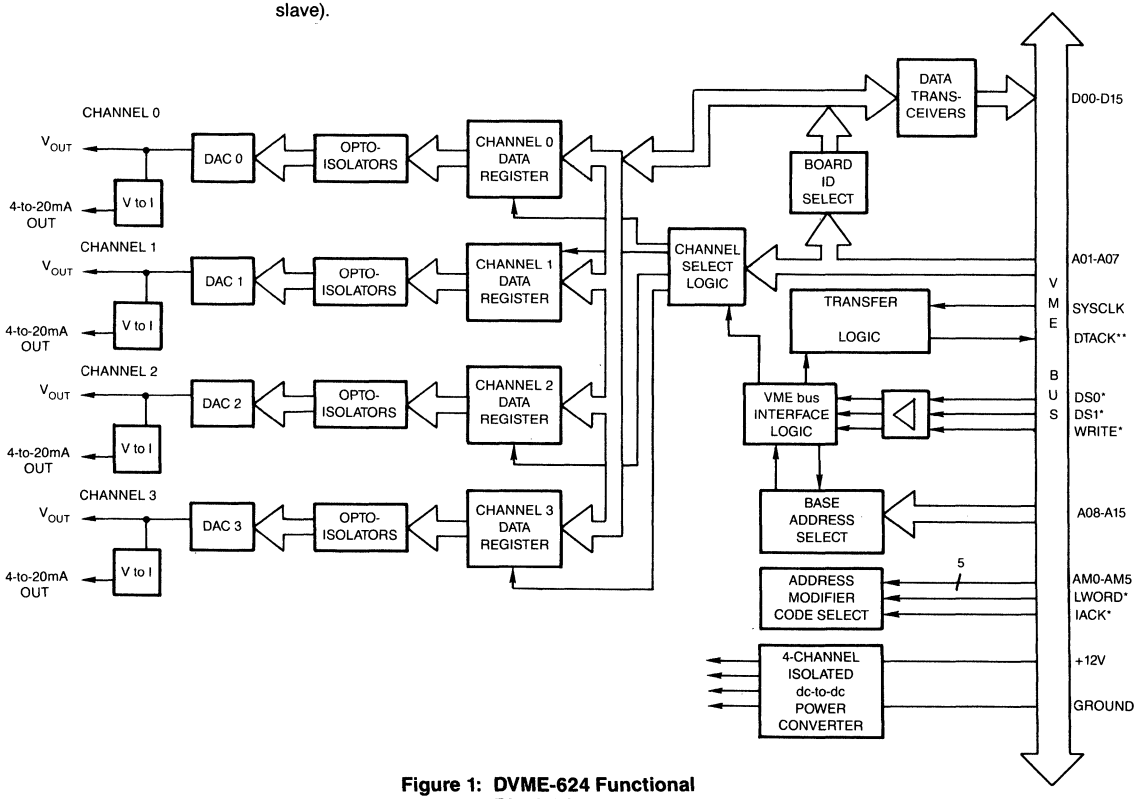


Figure 1: DVME-624 Functional Block Diagram

CONNECTOR SPECIFICATIONS

VME bus — P1 ..... 96-pin male DIN connector

Analog Output — J1 ..... 25-pin D Type female connector, Amp P/N 745783-1 or equivalent

ANALOG OUTPUT SPECIFICATONS

Number of Channels 4

Channel-to-channel Isolation ..... 300 VRMS, sustained maximum

Output full-scale voltage ranges ..... 0 to 5V dc
0 to 10V dc
±2.5V dc
±5V dc
±10V dc (standard)

Input data coding ..... Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

Resolution ..... 12 Bits. Uses 12 most significant data bits from the data bus. Ignores bits D0 through D3.

Reset ..... Minus full-scale, output resets to 0.000V dc

Current Loop ..... 4-to-20 mA. Meets ISA standard 550.1 Type 4 Class U

Excitation Voltage (User-supplied) ..... 15 to 36V dc

PERFORMANCE

Specification	Minimum	Typical	Maximum
Accuracy	0.05% of FSR	—	—
Differential non-linearity	—	—	0.5 LSB
Zero temperature drift	—	3 ppm/°C	5 ppm/°C
Offset temperature	—	5 ppm/°C	10 ppm/°C
Gain temp drift	—	15 ppm/°C	30 ppm/°C
Settling time:			
DVME-624V1 DVME-624C1	—	—	30 μseconds
DVME-624V2 DVME-624C2	—	—	6 μseconds
Output current	—	±5 mA	—
Output impedance	—	50 milliohms	—

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.0A typical, 1.2A maximum

+12V dc ±2.0% at 0.4A typical, .7A maximum

CURRENT LOOP

Specification	Minimum	Maximum
Accuracy	0.1% of FSR	—
Excitation (user-supplied)	15V dc	36V dc
Load resistance	100 Ohms	1000 Ohms
Isolation channel-to-channel	300 VRMS	—
Isolation output-to-bus	300 VRMS	—

PHYSICAL CHARACTERISTICS

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight ..... 9.6 oz (272.3 grams)

Operating temperature range ..... 0 to 60°C

Storage temperature range ..... −20 to +80°C

Relative humidity ..... 0 to 90%, non-condensing

DVME-624 ANALOG OUTPUT CONNECTOR J1

The DVME-624 provides analog outputs using the J1 connector. Depending on the model, the J1 connector contains voltage and current loop outputs. Figure 2 shows the output signals on the J1 connector.

PIN NUMBER	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	

Figure 2: Analog output pinout details

DVME-624 DATA FORMAT

The DVME-624 uses a 12-bit D/A converter for converting the digital data to analog signal. The board uses the 12 most significant bits of the VME data lines as input signals. Figure 3 shows the data format the DVME-624 is designed for.

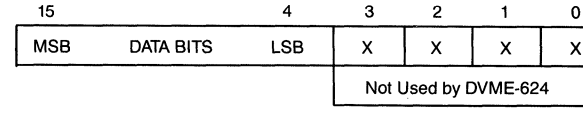


Figure 3: DVME-624 data format

DVME-624 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	4	

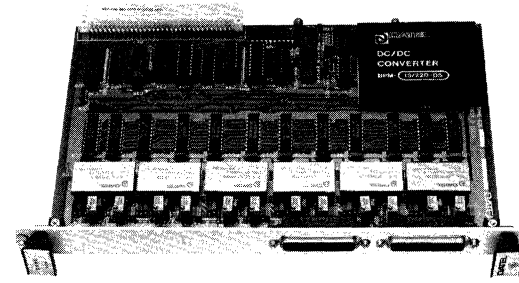
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-626
16-BIT, 6-CHANNEL
VMEbus D/A BOARD

FEATURES

- 6 D/A channels
- 16-Bit resolution
- 14-Bit monotonicity
- Designed to meet precision servo control requirements
- Complete hardware-compatible with VMEbus specifications
- 15 μSecond settling time
- Available in two models:
  DVME-626V1 for ±10V dc output
  DVME-626V2 for 0 to +10V dc and ±5V dc outputs
- Three input coding types:
  A. Bipolar 2's complement
  B. Bipolar offset binary
  C. Unipolar straight binary
- Up to 0.005% full-scale range accuracy
- ±0.005% of full-scale range differential nonlinearity
- On-board dc-to-dc power converter supplies ±15V dc for internal logic circuits



The DVME-626 is DATEL's high resolution VMEbus-based D/A board that provides analog outputs for up to 6 channels. The 16-bit D/A board is designed to deliver exceptionally high-performance in rugged industrial environments. The 14-bit monotonicity and 0.005% FSR accuracy makes the board an ideal choice for precision servo control and similiar applications. The DVME-626 is supported by VERSAdos-based and PDOS-based software for calibration and diagnostics.

GENERAL DESCRIPTION

The DVME-626 is a D/A member of DATEL's VMEbus family. The board delivers precision and performance that makes it easily acceptable for various test and control applications. On-board hardware resources provide 6 high-resolution analog outputs with an accuracy of better than 0.005% of full-scale range. The DVME-626 accepts 16-bit digital data, coded in bipolar 2's complement, bipolar offset binary, or unipolar straight binary. The board is rigorously tested under extreme environmental conditions to meet DATEL's stringent quality assurance requirements.

The DVME-626 easily fits into a VMEbus card cage and is addressable using short I/O space address lines. The on-board switches select the base address of the board. Functions relating to input data coding and output voltage range are easily selectable using jumpers.

Functionally, the DVME-626 consists of a VMEbus interface section and a digital-to-analog converter (DAC) section. The DAC data register section contains a data register and D/A converter for each section. One unique feature of the DVME-626 is that the DAC outputs will reset to 0.000V during reset, regardless of whether unipolar or bipolar outputs are selected. Figure 1 shows the functional block diagram of the board.

The DVME-626 D/A board will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the board. The user's manual also contains information on troubleshooting the board.

The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted for either VERSAdos or PDOS operating systems. Consult the factory regarding the availability of the diagnostic program's source code on other disk formats.

ORDERING INFORMATION

DVME-626V
- 1 — ± 10V dc output range
- 2 — 0 to 10V and ±5V dc output ranges

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VMEbus Interface

The DVME-626 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-626 generates the data acknowledge (DTACK *) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK * signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host CPU response times.

The interface logic decodes the VMEbus control lines WRITE *, DS0 *, DS1 *, and SYSRESET * to select and control the interface. These signals control the board select and the VMEbus transfer functions. The DVME-626 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

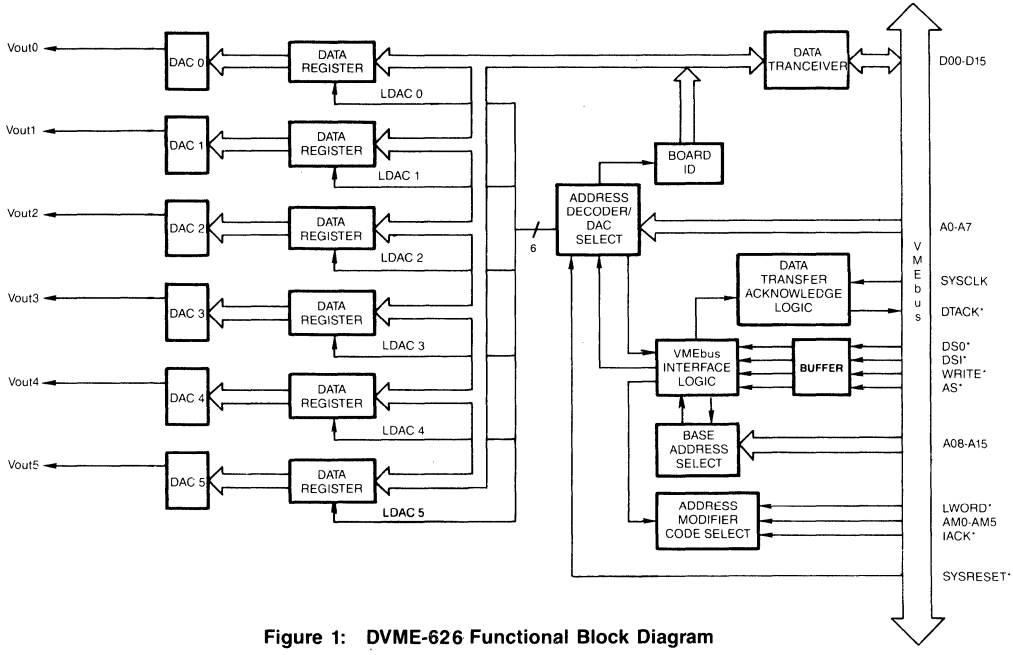


Figure 1: DVME-626 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

INTERFACE SPECIFICATIONS

Data Bus.....16 Bits (A16:D16 slave)

Address Bus.....Short I/O Space; 16 address lines

Address Modifier Codes.....Codes used 29H, 2DH, 39H, and 3DH

Memory Mapping.....Short I/O space, user or supervisor, 256 words allocated per board.

Data Transfer.....DTACK * signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector.....96-pin male DIN connector.

J1 and J2 Analog Output Connectors.....25-pin D-type female connector, DB-25S

ANALOG SPECIFICATONS

ANALOG OUTPUT

Number of Channels.....6, non-isolated

Output Range
DVME-626V1.....±10V dc
DVME-626V2.....0 to 10V and ± 5V dc

Digital Input Coding.....Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary
(jumperable)

Note: The VMEbus SYSCLK signal is required.

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

Resolution ..... 16 Bits
Monotonicity ..... 14 bits
Reset ..... Output resets to 0.000V dc at power-on
Accuracy ..... 0.005% of FSR, minimum
Differential nonlinearity ..... 0.005% of FSR, maximum
Zero temperature drift ..... 5 ppm/°C, typical
Offset temperature drift ..... 8 ppm/°C, typical
Gain temperature drift ..... 20 ppm/°C, typical
Settling time ..... 15 μseconds
Output current ..... ±5 mA, typical
Output impedance ..... 50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 3.0 Amperes, typical
Power Supply Rejection ..... ±0.002%, typical

PHYSICAL CHARACTERISTICS

Outline Dimensions ..... 9.19" W×6.3" D×0.6" H (233.35×160×15.24 mm)
Weight ..... 1 lb. (453.6 grams)
Operating Temperature Range ..... 0 to +60° C Range
Storage Temperature Range ..... −20 to +80° C Range
Humidity ..... 0 to 90%, non-condensing

DVME-626 PROGRAMMING INFORMATION

The DVME-626 contains six programmable registers that store digital data for each 16-bit D/A converter. The board responds only to word data transfers on write operations. Table 1 shows the addresses of the identification code and the registers. Figure 2 shows the format of the DAC data register.

Table 1: DVME-626 Register Locations.

ADDRESS	FUNCTION	CONTENTS
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 160	Write	D/A Channel 0
Base + 162	Write	D/A Channel 1
Base + 164	Write	D/A Channel 2
Base + 166	Write	D/A Channel 3
Base + 168	Write	D/A Channel 4
Base + 170	Write	D/A Channel 5

Word Address: Base + 160, Base+162, Base+164, Base+166, Base + 168, and Base + 170

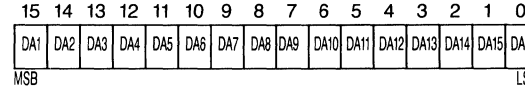


Figure 2: DVME-626 DAC Data Register Format

I/O CONNECTIONS

The DVME-626 D/A boards provide front panel J1 and J2 connectors for analog output connections. Tables 2 and 3 list the output signals of the J1 and J2 connectors respectively.

Table 2: DVME-626 ANALOG OUTPUT CONNECTOR J1

PIN #	DESCRIPTION
1	DAC 0 V OUT
2	NO CONNECTION
3	NO CONNECTION
4	DAC 1 V OUT
5	NO CONNECTION
6	NO CONNECTION
7	DAC 2 V OUT
8	NO CONNECTION
9	NO CONNECTION
10	DAC 3 V OUT
11	NO CONNECTION
12	NO CONNECTION
13	NO CONNECTION
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	NO CONNECTION
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	NO CONNECTION
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	NO CONNECTION
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	NO CONNECTION

Table 3: DVME-626 ANALOG OUTPUT CONNECTOR J2

PIN #	DESCRIPTION
1	DAC 4 V OUT
2	NO CONNECTION
3	NO CONNECTION
4	DAC 5 V OUT
5	NO CONNECTION
6	NO CONNECTION
7	NO CONNECTION
8	NO CONNECTION
9	NO CONNECTION
10	NO CONNECTION
11	NO CONNECTION
12	NO CONNECTION
13	NO CONNECTION
14	DAC 4 ANALOG RETURN
15	DAC 4 ANALOG RETURN
16	NO CONNECTION
17	DAC 5 ANALOG RETURN
18	DAC 5 ANALOG RETURN
19	NO CONNECTION
20	NO CONNECTION
21	NO CONNECTION
22	NO CONNECTION
23	NO CONNECTION
24	NO CONNECTION
25	NO CONNECTION

DVME-626 Board Identification Code

Byte Address	ASCII Code	FUNCTION
Base + 1	V	Identifier.
Base + 3	M	This ASCII code is present
Base + 5	E	for all DATEL VMEbus
Base + 7	I	boards
Base + 9	D	
Base + 0B	D	Manufacturer ID.
Base + 0D	A	DAT is the ID for DATEL
Base + 0F	T	
Base + 11	d	Board model number
Base + 13	V	
Base + 15	M	
Base + 17	E	
Base + 19	–	
Base + 1B	6	
Base + 1D	2	
Base + 1F	6	

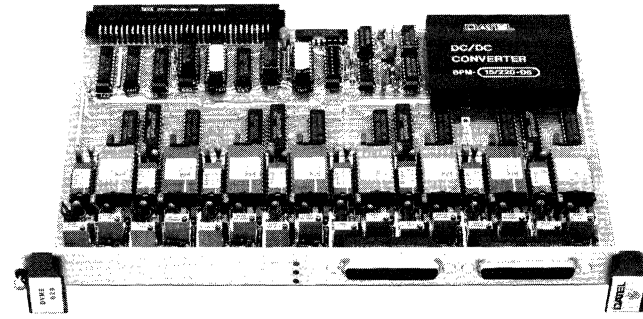
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base+0 through Base+63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base+64 through Base+77	DVME-660	48 line digital I/O board
Base+78 through Base+127		Not Used
Base+128 through Base+143	DVME-611	DVME-611: 32 single-ended/ 16 differential channel A/D board
	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base+144 through Base+151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base+152 through Base+159		Not Used
Base+160 through Base+175	DVME-612	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
	DVME-624	DVME-624: 4-channel isolated board
	DVME-626	DVME-626: 6-channel 16-bit D/A board
	DVME-628	DVME-628: 8-channel 12-bit D/A board
Base+176 through Base+191		Not Used
Base+192 through Base+255		Not Used

DVME-628
12-BIT, 8-CHANNEL
VMEbus D/A BOARD

FEATURES

- **8 D/A channels**
- **12-Bit resolution**
- **Complete hardware-compatible with VMEbus specifications.**
- **6 μSecond settling time.**
- **Three types of input coding:**
  - **A. Bipolar 2's complement**
  - **B. Bipolar offset binary**
  - **C. Unipolar straight binary**
- **Five output voltage ranges:**
  - **A. 0 to +5V dc**
  - **B. 0 to +10V dc**
  - **C. ±2.5V dc**
  - **D. ±5V dc**
  - **E. ±10V dc**
- **Up to 0.05% full-scale range accuracy.**
- **±1/2 LSB differential nonlinearity**
- **4-to-20 mA current loop output capability for DVME-628C model.**
- **On-board dc-to-dc power converter supplies ±15V dc for internal logic circuits.**



THE DVME-628 IS DATEL's HIGH-END, VMEbus-BASED D/A BOARD THAT PROVIDES ANALOG OUTPUT FOR UP TO 8 CHANNELS. THE 12-BIT D/A BOARD, WITH 6 MICROSECOND SETTLING TIME, IS DESIGNED TO DELIVER HIGH-PERFORMANCE IN PROCESS CONTROL, TEST INSTRUMENTATION AND SIMILAR APPLICATIONS. THE THREE INPUT CODING SCHEMES AND FIVE ANALOG OUTPUT VOLTAGE RANGES MAKES THE BOARD AN IDEAL CHOICE FOR MOST INDUSTRIAL APPLICATIONS.

GENERAL DESCRIPTION

DATEL's VMEbus family of boards offer a complete solution to various data acquisition applications. The DVME-628 is the D/A member of this family, providing up to 8 analog outputs for the host VMEbus system. The D/A board offers a resolution of 12 bits and operates with an accuracy of beter than 0.05% of full-scale range. The board is rigorously tested under extreme environmental conditions for DATEL's stringent quality assurance requirements.

The DVME-628 easily fits into a VMEbus card cage and is addressable using short I/O space address lines. The on-board switches select the base address of the board. Functions relating to input data coding and output voltage range are easily selectable using jumpers.

Functionally, the DVME-628 consists of a VMEbus interface section and a digital-to-analog conveter (DAC) section. The DAC data register section contains a data register and D/A converter for each section. For DVME-628C models the DAC section also contains voltage to 4-to-20 mA current loop conversion logic for each channel. One unique feature of the DVME-628 is that the DAC outputs will reset to 0.000V during reset regardless of whether unipolar or bipolar outputs are selected.

The DVME-628 D/A board will be shipped with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the board. The user's manual also contains information on troubleshooting the board.

The board is shipped with an example 68010 assembly language diagnostic program on a 5 1/4" floppy diskette, formatted using VERSAdos. The diagnostic program source code is available in hard copy from DATEL. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

ORDERING INFORMATION

DVME-628
- V - Voltage outputs only
- C - Voltage and 4-to-20mA current loop outputs

11

VMEbus Interface

The DVME-628 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes. The DVME-628 generates the data acknowledge (DTACK★) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK★ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes the VMEbus control lines WRITE ★, DS0 ★, DS1 ★, and AS ★ to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-628 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

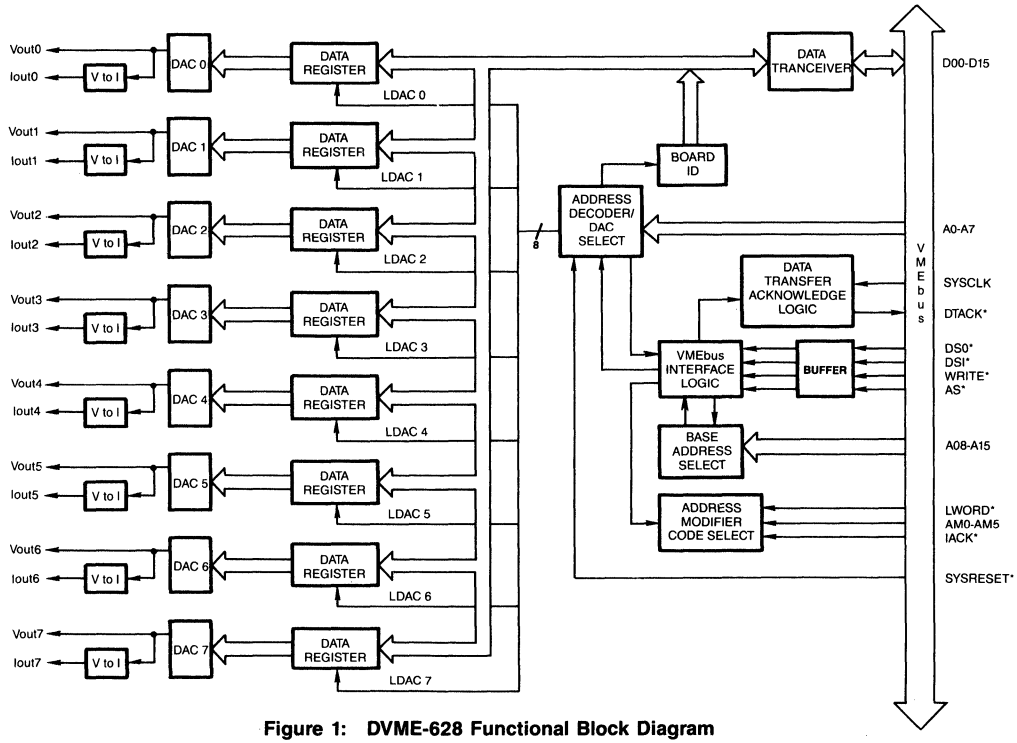


Figure 1: DVME-628 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 degrees Celcius, unless otherwise noted)

Interface specifications

Data Bus.....16 Bits (A16:D16 slave)

Address Bus.....Short I/O Space; 16 address lines

Address Modifier Codes.....Codes used 29H, 2DH, 39H, and 3DH

Memory Mapping.....Short I/O space, user or supervisor, 256 words allocated per board

Data Transfer.....DTACK ★ signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector.....96-pin male DIN connector

J1 and J2 Analog Output Connectors....25-pin D-type female connector.

ANALOG SPECIFICATONS

ANALOG OUTPUT

Number of Channels..... 8 non-isolated

Output Range.....0 to +5V dc
0 to +10V dc
± 2.5V dc
± 5V dc
± 10V dc

Digital Input Coding.....Bipolar 2's complement
Bipolar offset binary
Unipolar straight binary

NOTE: The VMEbus SYSCLK signal is required.

Resolution ..... 12 Bits

Reset ..... Output resets to 0.000V dc at power-on

Accuracy ..... 0.05% of FSR, minimum

Differential ..... 0.5 LSB, maximum non-linearity

Zero Temperature Drift ..... 3 ppm/ °C, typical
5 ppm/ °C, maximum

Offset Temperature Drift ..... 5 ppm/ °C, typical
10 ppm/ °C, maximum

Gain Temperature Drift ..... 15 ppm/ °C, typical
30 ppm/ °C, maximum

Settling Time ..... 6 μSeconds, maximum

Output Current ..... ±5 mA, typical

Output Impedance ..... 50 milliohms, typical

CURRENT LOOP

Current Loop ..... 4-to-20 mA, conforming to ISA Standard 550.1, Type 4, Class U

Accuracy ..... 0.1% of FSR, minimum

Excitation ..... +15V dc, minimum
(User-supplied) ..... +24V dc, typical
+36V dc, maximum

Load Resistance ..... 100 Ohms, minimum
1000 Ohms, maximum

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at ..... 2.0 Amperes, typical
2.3 Amperes, maximum

PHYSICAL CHARACTERISTICS

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight ..... 1 lb. (453.6 grams)

Operating Temperature Range ..... 0 to +60 °C

Storage Temperature Range ..... -20 to +80 °C

Humidity ..... 0 to 90%, non-condensing

DVME-628 PROGRAMMING INFORMATION

The DVME-628 contains eight programmable registers that store digital data for the D/A converters. The board responds only to word data transfers on write operations. Since the DVME-628 uses 12-bit D/A converters, the 12 most significant bits of the DAC data registers are used for conversion. Table 1 shows the addresses of the identification code and the registers. Figure 2 shows the format of the DAC data register.

Table 1: DVME-628 Register Locations

ADDRESS	FUNCTION	CONTENTS
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 160	Write	D/A Channel 0
Base + 162	Write	D/A Channel 1
Base + 164	Write	D/A Channel 2
Base + 166	Write	D/A Channel 3
Base + 168	Write	D/A Channel 4
Base + 170	Write	D/A Channel 5
Base + 172	Write	D/A Channel 6
Base + 174	Write	D/A Channel 7

Word Address: Base + 160, Base + 162, Base + 164, Base + 166, Base + 168, Base + 170, Base + 172, and Base + 174

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x
MSB											LSB				

Figure 2: DVME-628 DAC Data Register Format

OUTPUT CONNECTIONS

The DVME-628 D/A boards use the J1 and J2 connectors for analog output connections. Tables 2 and 3 list the output signals of the J1 and J2 connector respectively.

Table 2: DVME-628 Analog Output Pinout Details (J1)

PIN #	DESCRIPTION
1	DAC 0 V OUT
2	DAC 0 I LOOP
3	DAC 0 V LOOP
4	DAC 1 V OUT
5	DAC 1 I LOOP
6	DAC 1 V LOOP
7	DAC 2 V OUT
8	DAC 2 I LOOP
9	DAC 2 V LOOP
10	DAC 3 V OUT
11	DAC 3 I LOOP
12	DAC 3 V LOOP
13	NO CONNECTION
14	DAC 0 ANALOG RETURN
15	DAC 0 ANALOG RETURN
16	NO CONNECTION
17	DAC 1 ANALOG RETURN
18	DAC 1 ANALOG RETURN
19	NO CONNECTION
20	DAC 2 ANALOG RETURN
21	DAC 2 ANALOG RETURN
22	NO CONNECTION
23	DAC 3 ANALOG RETURN
24	DAC 3 ANALOG RETURN
25	NO CONNECTION

Table 3: DVME-628 Analog Output Pinout Details (J2)

PIN #	DESCRIPTION
1	DAC 4 V OUT
2	DAC 4 I LOOP
3	DAC 4 V LOOP
4	DAC 5 V OUT
5	DAC 5 I LOOP
6	DAC 5 V LOOP
7	DAC 6 V OUT
8	DAC 6 I LOOP
9	DAC 6 V LOOP
10	DAC 7 V OUT
11	DAC 7 I LOOP
12	DAC 7 V LOOP
13	NO CONNECTION
14	DAC 4 ANALOG RETURN
15	DAC 4 ANALOG RETURN
16	NO CONNECTION
17	DAC 5 ANALOG RETURN
18	DAC 5 ANALOG RETURN
19	NO CONNECTION
20	DAC 6 ANALOG RETURN
21	DAC 6 ANALOG RETURN
22	NO CONNECTION
23	DAC 7 ANALOG RETURN
24	DAC 7 ANALOG RETURN
25	NO CONNECTION

DVME-628 BOARD IDENTIFICATION CODE

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	2	
+ 1F	8	

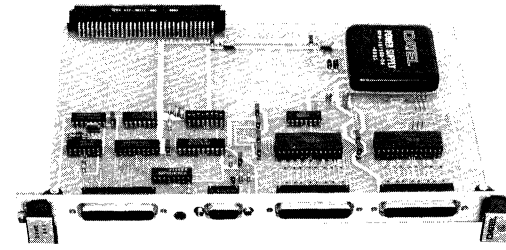
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-641
32-CHANNEL HIGH-LEVEL, VMEbus EXPANSION BOARD

FEATURES

- **Accepts 32 single-ended/16 differential expansion channels**
- **Directly accepts high-level inputs**
- **Hardware compatible with VMEbus specifications**
- **Interfaces to DATEL's DVME-601/611/612 A/D boards**
- **6 Microseconds settling time**
- **0.01% Full-scale range accuracy**
- **Low-cost**
- **Cascadable to up to 256 channels**
- **Includes a board selection LED**



THE DVME-641 OFFERS CHANNEL EXPANSION TO DATEL's DVME-601/611/612 SERIES OF A/D BOARDS. THE CHANNEL EXPANSION BOARD IS DESIGNED TO ACCEPT HIGH-LEVEL INPUTS FROM UP TO 32 SINGLE-ENDED OR 16 DIFFERENTIAL INPUT CHANNELS. THE DVME-641 DRAWS POWER FROM THE VMEbus P1 CONNECTOR AND FITS INTO VMEbus CARD CAGES.

GENERAL DESCRIPTION

The DVME-641 is a low-cost channel expansion board that interfaces directly to DATEL's DVME-601/611/612 high-performance A/D boards. The board externally multiplexes up to 32 single-ended or 16 differential high-level input channels. The channel expansion board fits into a typical VMEbus host system. The DVME-641 is specifically useful for applications involving multiple-channel data acquisition or controlling numerous discrete process control loops. The low cost per channel makes the board ideal for most applications.

Figure 1 shows a typical multi-channel application for data acquisition from different types of inputs. In this application the host system selects the expansion channel on the DVME-641, DVME-643 or DVME-645 through the DVME-601/611/612 A/D board. The DVME-601/611/612 digital data is available on the VMEbus data lines for host system access.

ORDERING INFORMATION

DVME-641	32S/16D MUX board

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

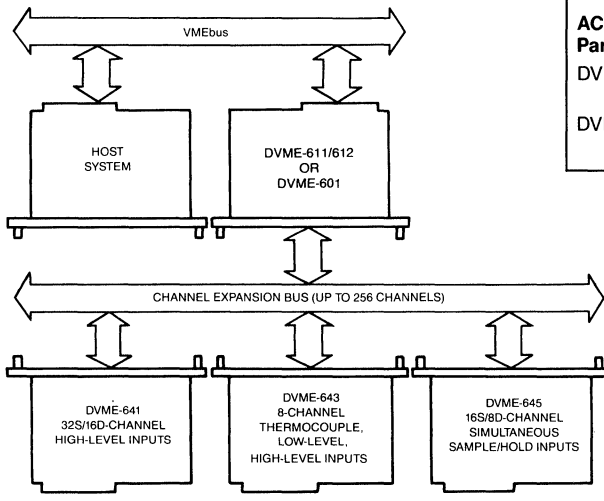


Figure 1: DVME-641 Application Configuration

11

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C unless otherwise noted)

ANALOG INPUT

Number of Channels 32S/16D

Channel Expansion 256S/256D*

Input Configuration ..... Single-ended or Differential

Input Range ..... ± 10V dc

Analog Output ..... Differential

Interface ..... Analog Expansion Bus for DVME-601/611/612 boards

Common Mode Voltage... (Specified for differential configuration only) ±10V dc, maximum non-isolated

Overvoltage Protection... ± 35V dc, maximum

Off-Channel Leakage current ..... 0.03 nanoamperes, typical 60 nanoamperes, maximum

On-Channel Leakage Current ..... 0.1 nanoamperes,typical 300 nanoamperes, maximum

Output Settling Time (0 to 10V step input, channel-to-channel settling) ..... 6 μseconds, maximum to rated accuracy

Full-scale Range Accuracy ..... 0.01%, maximum

Output Impedance ..... 2.5 Kohms, maximum

*Up to 10 slave MUX boards may be driven from one A/D master board at derated setting.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector .... 96-pin male DIN connector

Analog Input - J1,J2 Connectors ..... Two 25-pin D-type DB-25S female connectors

External Trigger - J3 Connector ..... 9-pin D-type DB-9S female connector

Analog Expansion - J4 Connector .... 25-pin D-type DB-25S female connector

POWER SUPPLY REQUIRMENTS

+5V dc ±0.5% at 0.4A typical, 0.6A maximum from P1 VMEbus connector

PHYSICAL CHARACTERISTICS

Outline Dimensions ..... 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight ..... 11 oz. (311.85 grams)

Operating Temperature Range ... 0 to +60 °C

Storage Temperature Range ..... -20 to +80 °C

Relative Humidity ..... 0 to 90% non-condensing

I/O CONNECTIONS

The DVME-641 uses J1, J2, J3, and J4 for analog input, external trigger, and channels expansion connections. Tables 1,2, 3, and 4 list these signals. VMEbus IACK and bus grant signals are daisy-chained.

Table 1: DVME-641 Analog Input Connector (J1)

PIN #	Single-ended	Differential
24	Channel 0 IN	Channel 0 High IN
12	Channel 16 IN	Channel 0 Low IN
25	Analog Return	Analog Return
10	Channel 1 IN	Channel 1 High IN
23	Channel 17 IN	Channel 1 Low IN
11	Analog Return	Analog Return
21	Channel 2 IN	Channel 2 High IN
9	Channel 18 IN	Channel 2 Low IN
22	Analog Return	Analog Return
7	Channel 3 IN	Channel 3 High IN
20	Channel 19 IN	Channel 3 Low IN
8	Analog Return	Analog Return
18	Channel 4 IN	Channel 4 High IN
6	Channel 20 IN	Channel 4 Low IN
19	Analog Return	Analog Return
4	Channel 5 IN	Channel 5 High IN
17	Channel 21 IN	Channel 5 Low IN
5	Analog Return	Analog Return
15	Channel 6 IN	Channel 6 High IN
3	Channel 22 IN	Channel 6 Low IN
16	Analog Return	Analog Return
1	Channel 7 IN	Channel 7 High IN
14	Channel 23 IN	Channel 7 Low IN
2	Analog Return	Analog Return

Table 2: DVME-641 Analog Input Connector (J2)

PIN #	Single-ended	Differential
24	Channel 8 IN	Channel 8 High IN
12	Channel 24 IN	Channel 8 Low IN
25	Analog Return	Analog Return
10	Channel 9 IN	Channel 9 High IN
23	Channel 25 IN	Channel 9 Low IN
11	Analog Return	Analog Return
21	Channel 10 IN	Channel 10 High IN
9	Channel 26 IN	Channel 10 Low IN
22	Analog Return	Analog Return
7	Channel 11 IN	Channel 11 High IN
20	Channel 27 IN	Channel 11 Low IN
8	Analog Return	Analog Return
18	Channel 12 IN	Channel 12 High IN
6	Channel 28 IN	Channel 12 Low IN
19	Analog Return	Analog Return
4	Channel 13 IN	Channel 13 High IN
17	Channel 29 IN	Channel 13 Low IN
5	Analog Return	Analog Return
15	Channel 14 IN	Channel 14 High IN
3	Channel 30 IN	Channel 14 Low IN
16	Analog Return	Analog Return
1	Channel 15 IN	Channel 15 High IN
14	Channel 31 IN	Channel 15 Low IN
2	Analog Return	Analog Return

Table 3: DVME-641 External Trigger Input Connections (J3)

PIN #	SIGNAL
1	External Trigger IN*
6	Digital Ground

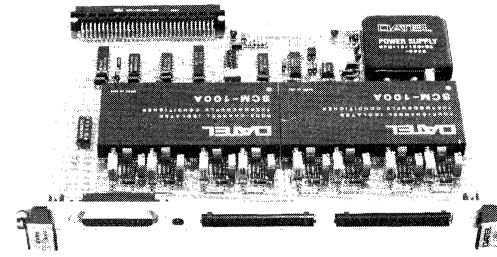
Table 4: DVME-641 Expansion Channel Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address Line 0 IN
25	Expansion Channel Address Line 1 IN
12	Expansion Channel Address Line 2 IN
24	Expansion Channel Address Line 3 IN
11	Expansion Channel Address Line 4 IN
23	Expansion Channel Address Line 5 IN
10	Expansion Channel Address Line 6 IN
22	Expansion Channel Address Line 7 IN
4,16	Digital Ground
9	Expansion Channel Address Valid IN
20	Setting Delay OUT*
17	External Trigger OUT*
21	Not Used
5	Not Used
1	Analog Low OUT
14	Analog High OUT
2,15	Analog Common

DVME-643
8-CHANNEL ISOLATED ANALOG VMEbus EXPANSION BOARD

FEATURES

- **Offers channel expansion to DATEL's DVME-601/611/612 A/D boards**
- **Two models of channel expansion boards**
  DVME-643T: Thermocouple and low-level inputs
  DVME-643H: High-level inputs
- **On-board cold junction compensation sensor**
- **Offers 1000V peak isolation**
- **On-board signal conditioning**
- **120 dB minimum CMRR**
- **55 dB minimum NMR**
- **2.5 millisecond settling time**
- **On-board dc-to-dc power converter**
- **Cascadable to up to 10 MUX boards**
- **Includes a board selection LED**



THE DVME-643 BOARDS OFFER CHANNEL EXPANSION TO DATEL's DVME-601/611/612 A/D BOARDS. THESE MULTIPLEXER BOARDS PROVIDE 1000V ISOLATION AND SIGNAL CONDITIONING FOR EIGHT THERMOCOUPLE, LOW-LEVEL, OR HIGH-LEVEL INPUTS. THE DVME-643T BOARD INCORPORATES A COLD JUNCTION COMPENSATION OUTPUT FOR THERMOCOUPLE INPUTS TO CORRECT AGAINST REFERENCE JUNCTION TEMPERATURE VARIATIONS.

GENERAL DESCRIPTION

Designed specifically for applications requiring multiple channel data acquisition, the DVME-643 boards expand the analog input capability of DATEL's DVME-601/611/612 A/D boards. The DVME-643 boards are offered in two versions. The DVME-643T provides isolation and signal conditioning for thermocouple and low-level inputs. The DVME-643H accepts for high-level voltage and 4-to-20 mA current loop inputs.

The DVME-643T allows mixing thermocouple and low-level signals on the same board. The DVME-601/611/612 boards offer channel expansion for up to 256 channels. In addition to the DVME-643 boards, DATEL's channel expansion boards for high-level and simultaneous sample and hold inputs may also be used with a DVME-601/611/612 board. Figure 1 shows typical multi-channel application configuration.

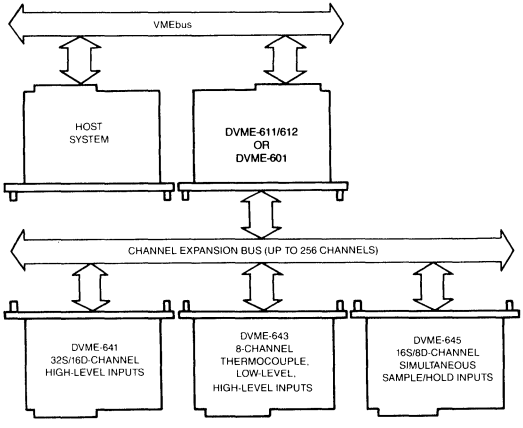


Figure 1: DVME-643 Application Configuration

ORDERING INFORMATION

DVME-643

- T — Thermocouple and low-level isolated inputs
  input ranges: ±25.6, 51.2, and 102.4mV
- H — High-level voltage and current loop isolated inputs
  High-level voltage ranges: ±5V dc
  Current loop inputs: 4-to-20 mA
- R — RTD inputs*
- S — Strain gage inputs*

*(Consult factory for availability)

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

11

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise noted)

ANALOG INPUT

Number of Channels ..... 8 Differential and CJC channels

Channel Expansion ..... Up to 256S/256D*

Isolation ..... 750V RMS
(ch-ch. & ch.-bus) 1000V Peak

Input Range DVME-643T ..... ±25.6 mV dc
±51.2 mV dc
±102.4 mV dc
DVME-643H ..... ±5V dc

Common Mode Voltage ..... 750V RMS
AC, 50 or 60Hz 1000V Peak

Input Bias Current ..... 8 nano amperes, maximum

Overvoltage Protection ..... 130V RMS, maximum

Input Impedance, ... 100 megohms
differential input to ground

Common Mode Rejection Ratio, f = .01 to 100Hz
DVME-643T ..... 120 dB, minimum
DVME-643H ..... 110 dB, minimum

Normal Mode Rejection ..... 55 dB, minimum
50 or 60 Hz

Settling Time ..... 2.5 milliseconds, maximum

dc Gain Accuracy
DVME-643T ..... 0.03% FSR, minimum
DVME-643H ..... 0.05% FSR, minimum

Gain Drift ..... 35 ppm/°C, maximum

Offset Drift
DVME-643T ..... 3 μV/°C, maximum
DVME-643H ..... 60 μV/°C, maximum

CJC Error
At Room Temperature ..... 0.5°C, maximum
At Full Temperature Range ... 1.5°C, maximum

Output Impedance ..... 0.5 K ohms, maximum

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1A typical, 1.5A maximum from P1 VMEbus connector.

I/O CONNECTIONS

The DVME-643 uses J1 and J2 for analog input connections and J4 for channel expansion connections. Tables 1 and 2 list these signals. VMEbus IACK and bus grant signals are daisy-chained.

CONNECTOR SPECIFICATIONS

VMEbus-P1 Connector ..... 96-pin male DIN connector

Analog Input J1 and J2 Connectors ..... 12-pin male connector

Analog Expansion J4 Connector ..... 25-pin D-type female connector, DB-25S

PHYSICAL—ENVIRONMENTAL

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)

Weight ..... 1 lb (453.59 grams)

Operating Temperature Range .. 0 to +60°C

Storage Temperature Range ..... -20 to +80°C

Relative Humidity ..... 0 to 90%, non-condensing

*Up to 10 slave MUX boards may be driven from one A/D master board.

Table 1: Analog Input Connections (J1 and J2)

PIN #	SIGNAL (J1)	PIN #	SIGNAL (J2)
12	Channel 0 High IN	12	Channel 4 High IN
11	Channel 0 Low IN	11	Channel 4 Low IN
10	Analog Return	10	Analog Return
9	Channel 1 High IN	9	Channel 5 High IN
8	Channel 1 Low IN	8	Channel 5 Low IN
7	Analog Return	7	Analog Return
6	Channel 2 High IN	6	Channel 6 High IN
5	Channel 2 Low IN	5	Channel 6 Low IN
4	Analog Return	4	Analog Return
3	Channel 3 High IN	3	Channel 7 High IN
2	Channel 3 Low IN	2	Channel 7 Low IN
1	Analog Return	1	Analog Return

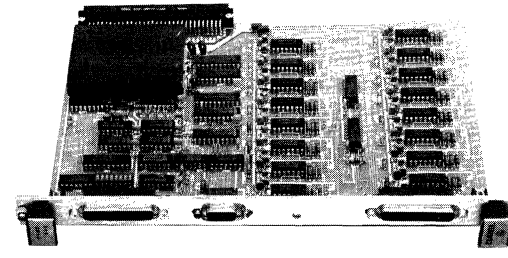
Table 2: Channel Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address 0
25	Expansion Channel Address 1
12	Expansion Channel Address 2
24	Expansion Channel Address 3
11	Expansion Channel Address 4
23	Expansion Channel Address 5
10	Expansion Channel Address 6
22	Expansion Channel Address 7
4,16	Digital Ground
20	Settling Delay OUT*
17	External Trigger OUT
9	Expansion Channel Address Valid IN
14	Analog High OUT
1	Analog Low OUT
2,15	Analog Common

DVME-645
16-CHANNEL SIMULTANEOUS SAMPLE-AND-HOLD VMEbus EXPANSION BOARD

FEATURES

- **Offers channel expansion to DVME-601/611/612 A/D boards**
- **Offers simultaneous sample-and-hold capability to up to 16S/8D channels**
- **1.2 μV/μS sample-and-hold droop rate**
- **6 Microsecond settling time**
- **Complete compatibility to VMEbus hardware specifications**
- **Cascadable to up to 256 channels**
- **0.05% Full-scale range accuracy**
- **On-board dc-to-dc converter**



THE DVME-645 IS DESIGNED TO PROVIDE CHANNEL EXPANSION TO DATEL'S DVME-601/611/612 BOARDS FOR APPLICATIONS REQUIRING SAMPLE AND HOLD CAPABILITY. THE BOARD IS EQUIPPED WITH 16 SAMPLE-AND-HOLD AMPLIFIERS, ACQUIRING DATA SIMULTANEOUSLY FROM 16 CHANNELS. THE BOARD IS IDEALLY SUITED FOR TRANSIENT ANALYSIS, SIGNAL RECONSTRUCTION AND RELATED APPLICATIONS.

GENERAL DESCRIPTION

The DVME-645 offers simultaneous sample-and-hold capability to DATEL's family of multiplexer boards. The board expands the analog input channels of the DVME-601/611/612 A/D boards. In a typical application, the DVME-645 is usable with other multiplexer boards using thermocouple, isolated and non-isolated voltage inputs. Figure 1 shows the channel expansion to the DVME-601/611/612 A/D boards.

Simultaneous Sample-and-Hold

A sample-and-hold circuit holds or freezes a changing analog input signal for up to a few milliseconds. With 16 on-board amplifiers, the DVME-645 simultaneously holds analog signals from 16 individual channels. An A/D subsystem (DVME-601/611/612 may scan and convert the samples stored. The digital data now represents the analog signal values at an instant of time from all the 16 channels.

The DVME-645 also allows measuring high-speed transients and spikes during a specified window of time. For applications requiring sampling at rates up to 8 MHz all 16 channels may be connected to a single measuring point. The sample-and-hold circuits may then sequentially acquire the analog input signal. In this application, the DVME-645 functions as a very low-cost 8 MHz storage device. Typical applications of the DVME-645 with the DVME-601/611/612 include pulse analysis and reconstruction and data skew elimination for seismic measurements.

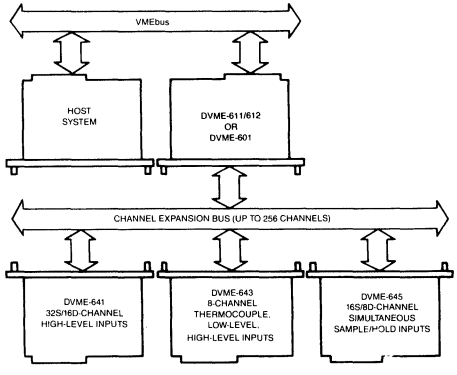


Figure 1: DVME-645 Application Configuration

ORDERING INFORMATION

DVME-645	16S/8D SSH MUX board

ACCESSORIES

Part Number	Description
DVME-C-01	Two-connector expansion cable (for use with one multiplexer board).
DVME-C-02	Three-connector expansion cable (for use with two multiplexer boards).

11

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise noted)

Number of Channels ..... 16S/8D non-isolated
Channel Expansion ..... Up to 256S/256D*
Input Range ..... ±10V dc
Analog Output ..... Differential
Interface ..... Analog expansion bus for DVME-611/612 boards

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector .... 96-pin male DIN connector
Analog Input J1 Connector 25-pin D-type female connector
External Trigger and Sample-and-hold Control J3 Connector ..... 9-pin D-type female connector
Analog Expansion J4 Connector ..... 25-pin D-type female connector

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 2.0A typical, 3.0A maximum from P1 VMEbus connector.

I/O CONNECTIONS

The DVME-645 uses J1 and J4 connectors for analog input and channel expansion connections respectively. Tables 1 and 2 list the signals for the connections. Table 3 lists signals for trigger and sample-and-hold control. VMEbus IACK and bus grant signals are daisy-chained.

ANALOG SPECIFICATIONS

Common Mode Voltage .... ±10V dc, maximum
Over Voltage Protection ... ±35V dc, maximum
Input Bias Current ..... 300 nanoamperes, maximum
Input Impedance ..... 1 Megohm, minimum
Output Settling Time (For 0 to -10V step input, channel-to-channel settling) ..... 6 μseconds, maximum to rated accuracy
dc Gain Accuracy ..... 0.05%, minimum
Output Impedance ..... 0.5 Kohms, maximum
Input Offset Voltage ..... 1.0 mV, maximum
Input Offset Voltage Drift ..... 20 μV/°C, maximum
Aperture Delay ..... 50 nS
Aperture Time ..... 100 nS
Sample-and-Hold Droop Rate ... 1.2 μV/μS, typical
2.0 μV/μS, maximum
Sample-and-Hold Pedestal . 1.0 mV, typical
2.5 mV, maximum

PHYSICAL—ENVIRONMENTAL

Outline Dimensions ..... 9.19"W x 6.3"D x 0.6"H (233.35 x 160 x 15.24 mm)
Weight ..... 12.5 Oz. (354.75 grams)
Operating Temperature Range .... 0 to +60°C
Storage Temperature Range ..... 20 to +80°C
Relative Humidity ..... 0 to 90% non-condensing

Table 1: DVME-645 Analog Input Connector (J1)

PIN #	Single-ended	Differential
24	Channel 0 IN	Channel 0 High IN
12	Channel 8 IN	Channel 0 Low IN
25	Analog Return	Analog Return
10	Channel 1 IN	Channel 1 High IN
23	Channel 9 IN	Channel 1 Low IN
11	Analog Return	Analog Return
21	Channel 2 IN	Channel 2 High IN
9	Channel 10 IN	Channel 2 Low IN
22	Analog Return	Analog Return
7	Channel 3 IN	Channel 3 High IN
20	Channel 11 IN	Channel 3 Low IN
8	Analog Return	Analog Return
18	Channel 4 IN	Channel 4 High IN
6	Channel 12 IN	Channel 4 Low IN
19	Analog Return	Analog Return
4	Channel 5 IN	Channel 5 High IN
17	Channel 13 IN	Channel 5 Low IN
5	Analog Return	Analog Return
15	Channel 6 IN	Channel 6 High IN
3	Channel 14 IN	Channel 6 Low IN
16	Analog Return	Analog Return
1	Channel 7 IN	Channel 7 High IN
14	Channel 15 IN	Channel 7 Low IN
2	Analog Return	Analog Return

Table 2: DVME-645 Expansion Connections (J4)

PIN #	SIGNAL
13	Expansion Channel Address Line 0 IN
25	Expansion Channel Address Line 1 IN
12	Expansion Channel Address Line 2 IN
24	Expansion Channel Address Line 3 IN
11	Expansion Channel Address Line 4 IN
23	Expansion Channel Address Line 5 IN
10	Expansion Channel Address Line 6 IN
22	Expansion Channel Address Line 7 IN
4,16	Digital Ground
9	Channel Address Valid IN
8	Start Conversion Strobe IN
20	Strobe Delay OUT*
7	End of Conversion IN
19	End of Scan IN
17	External Trigger OUT*
6	General Purpose Input (XMODSEL)
5,21	Not Used
1	Analog Low OUT
14	Analog High OUT
2,15	Analog Common

Table 3: DVME-645 Digital Control Connections (J3)

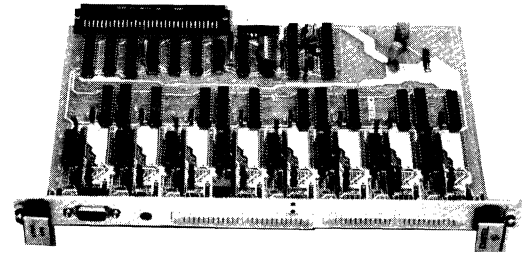
PIN #	SIGNAL
1	External Trigger IN*
6	Digital Ground
9	Sample/Hold Skew IN
5	Sample/Hold Skew OUT
3	Sample and Hold Skew Clock IN/OUT
4	Sample and Hold Control IN/OUT

*Up to 10 slave MUX boards may be driven from one A/D master board at derated settling.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

DVME-660
48-LINE DIGITAL I/O
VMEbus BOARD

FEATURES



- **Complete compatibility with VMEbus specifications**
- **48 Digital I/O lines**
- **Software programmable input and outputs**
- **Interrupt levels, IRQ1 through IRQ7**
- **On-board timer**
- **24- and 16-stage timer operation**
- **Interrupts on 1. Timer**
  2. Compare register
  3. External trigger
- **Compatible with GORDOS I/O module systems**
- **Compatible with OPTO-22 I/O module systems**

DATEL EXPANDS ITS VMEbus PRODUCT LINE WITH THE DVME-660. THE DVME-660 HAS 48 INDIVIDUALLY PROGRAMMABLE TTL INPUT OR OUTPUT LINES. THE ON-BOARD HARDWARE INCLUDES AN INTERRUPT CONTROLLER THAT ALLOWS UP TO EIGHT USER-PROGRAMMABLE INTERRUPT LINES AND A TIMER THAT ALLOWS DELAYS UP TO A FEW MINUTES.

GENERAL DESCRIPTION

The DVME-660 is a high-performance digital I/O board that allows programming 48 lines individually. The board is electrically and mechanically compatible with GORDOS and OPTO-22 I/O module systems. The board is ideally suitable for industrial and process control applications.

Functionally the board consists of six bi-directional ports of eight lines each, a programmable timer and a VMEbus interrupter. The data direction of the eight lines in each port is programmable by the host system. The timer may receive the input frequency from the VMEbus SYSCLK signal or an on-board RC network. 16 of 24 timer stages are programmable by the VMEbus data lines. The timer is also programmable to bypass the first eight stages. Figure 1 shows the DVME-660 functional block diagram.

ORDERING INFORMATION

DVME-660

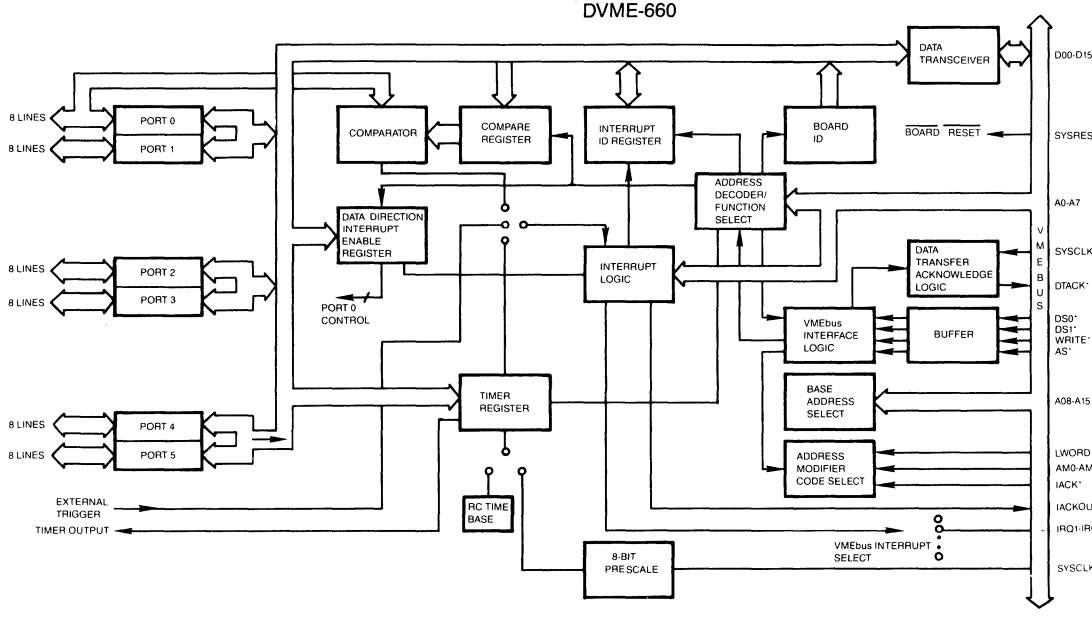


Figure 1: DVME-660 Functional Block Diagram

11

If enabled, the DVME-660 interrupt logic section generates an interrupt request on one of the VMEbus interrupt lines (IRQ1* through IRQ7*). The interrupt line is jumper-selectable. The interrupt logic accepts a 3-bit interrupt acknowledge level, IACK*, and IACKIN* signals from the host system as interrupt acknowledge and daisy chain input signals. If this interrupt level matches the DVME-660 interrupt request level, the on-board logic loads the interrupt ID number on to the VMEbus. If the level does not match, the board generates the daisy chain IACKOUT* signal. The DVME-660 may generate interrupt request from one of three sources: timer section, port 0 comparator section, or an external trigger. The timer output is jumper-selectable to cause periodic VMEbus interrupts. The board also generates an interrupt if port 0 inputs match data in compare register. The VMEbus data lines (D00 through D07) may load the compare register.

FUNCTIONAL SPECIFICATIONS

(Typical at 25 °C, unless otherwise noted)

INTERFACE SPECIFICATIONS

Data Bus ..... 16 bits (A16:D16 slave)

Address Bus ..... Short I/O space, 16 address lines, 6 address modifier lines. Uses address modifier codes 29H, 2DH, 39H and 3DH

Interrupts ..... IRQ1* through IRQ7*

Memory Mapping ..... Short I/O space, user or supervisor, 256 words allocated per board

Data Transfer ..... DTACK* signal line. Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines. This signal is derived from 16MHz VMEbus clock

I/O SPECIFICATIONS

Number of Port Lines .... 48, programmable as inputs or outputs non-isolated

DIGITAL OUTPUTS

Output Port Current ..... I_{OL} = 24 mA maximum at V_{OL} = 0.5V maximum
I_{OH} = -15 mA maximum at V_{OH} = 2.0V minimum

DIGITAL INPUTS

Input Port Voltage ..... V_{IL} = 0.8V maximum
V_{IH} = 2.0V minimum

Input Port Current ..... I_{IL} = -1.26 mA maximum at V_i = 0.4V
I_{IH} = 20 μA maximum at V_i = 2.7V

POWER SUPPLY REQUIREMENTS

+5V dc ±0.5% at 1.3 Amperes, typical

VMEbus Interface

The DVME-660 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data input and output purposes. The DVME-660 generates the data acknowledge (DTACK*) signal to notify acceptance of data from the VMEbus data lines, D00 through D15. The DTACK* signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE*, DS0*, DS1*, and SYSRESET*) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-660 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

CONNECTOR SPECIFICATIONS

VMEbus P1 Connector ... 96-pin male connector

Port Connectors J1 and J2 ..... 50-pin header male connectors

Trigger Control Connector J3 ..... 9-pin D-type female connector, DB-95

PHYSICAL CHARACTERISTICS

Outline Dimensions ..... 9.19″W x 6.3″D x 0.6″H (233.35 x 160 x 15.24 mm)

Weight ..... 1 lb (453.6 grams)

Operating Temperature Range ... 0 to +60 °C

Storage Temperature Range .... -20 to +80 °C

Relative Humidity ..... 0 to 90%, non-condensing

DVME-660 PROGRAMMING

The DVME-660 maps onto 256 consecutive bytes in the host system's address space. The contents of this address space are the board ID number, data registers, port compare register, data direction/interrupt enable register, interrupt ID register and the programmable timer register. Table 1 lists the contents of the DVME-660 address space.

Table 1: DVME-660 Address Register

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification code
Base + 64	Read/Write	Data direction/Interrupt enable register
Base + 66	Read/Write	Interrupt ID register
Base + 68	Write	Timer register
Base + 70	Write	Compare register
Base + 72	Read/Write	Port 0 and 1 I/O register
Base + 74	Read/Write	Port 2 and 3 I/O register
Base + 76	Read/Write	Port 4 and 5 I/O register

Data Direction/Interrupt Enable Register

The host system may program bits 0 through 5 of this register to assign direction of the six I/O ports. When programmed, all eight lines in a port will function as either inputs or outputs. Programming the bit 6 of this register enables the on-board interrupt logic. If this bit is set, the DVME-660 interrupts the host system. The interrupt may be from the timer section, the port 0 comparator section, or an external trigger. Figure 2 shows the format of this register.

Word address: Base + 64

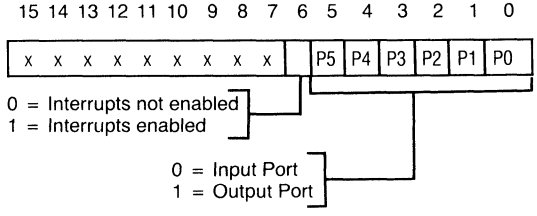


Figure 2: DVME-660 Data Direction/Interrupt Enable Register

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-660 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number onto the VMEbus (low byte). Figure 3 shows the format of the interrupt ID register.

Word address: Base + 66

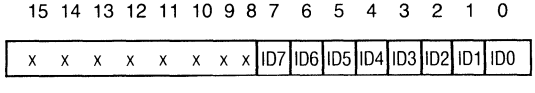


Figure 3: DVME-660 Interrupt ID Register Format

Port Compare Register

The DVME-660 has a port comparator section that compares inputs from port 0 to the contents of the port compare register. The host system may load the port compare register using VMEbus data lines D00 through D07. The port comparator section generates a single VMEbus interrupt if the port 0 inputs match the port compare register contents. Figure 4 shows the format of the port compare register.

Word address: Base + 70

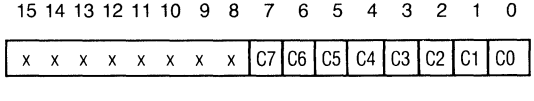


Figure 4: DVME-660 Port Compare Register

Programmable Timer Register

Eight LSB's of this register allows programming the on-board programmable timer section. Bits 0 through 3 assign a timer divide ratio that selects one of sixteen timer stages. The maximum timer input frequency is approximately 1MHz. Bit 4 sets the time for 24 or 16-stage operation by bypassing the first eight stages. Programming bit 6 enables the port 0 comparator. Bit 7 is usable to turn ON an on-board LED lamp. Figure 5 shows the format of this register.

Word address: Base + 68

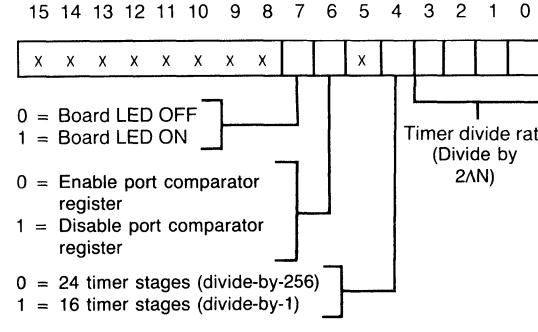


Figure 5: DVME-660 Programmable Timer Register

Port I/O Registers

The DVME-660 uses three 16-bit registers as six 8-line ports. The lower 8 bits of these registers correspond to ports 0, 2, and 4 respectively and the higher 8 bits correspond to ports 1, 3, and 5 respectively. Figure 6 shows the format of these registers.

Word address: Base + 72, 74 and 76

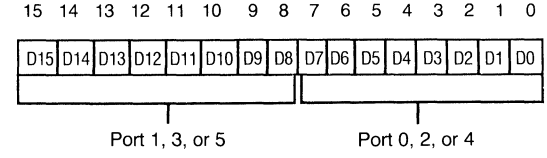


Figure 6: DVME-660 Port I/O Registers

I/O CONNECTIONS

The DVME-660 digital I/O board uses J3 connection for trigger control, and J1 and J2 connectors for digital I/O connections. Tables 2 and 3 lists signals for these connectors.

Table 2: Trigger Control Connections (J3)

Pin #	Signal
1	External Interrupt Request In
2	Trigger Output
3	External Timer Clock In
4	No Connection
5,6	+5V dc
7,8,9	Digital Ground

Table 3: DVME-660 I/O Connections (J1 and J2)

J1 Connector		J2 Connector	
Pin #	**Signal**	**Pin #**	**Signal**
47	Channel 0	47	Channel 24
45	Channel 1	45	Channel 25
43	Channel 2	43	Channel 26
41	Channel 3	41	Channel 27
39	Channel 4	39	Channel 28
37	Channel 5	37	Channel 29
35	Channel 6	35	Channel 30
33	Channel 7	33	Channel 31
31	Channel 8	31	Channel 32
29	Channel 9	29	Channel 33
27	Channel 10	27	Channel 34
25	Channel 11	25	Channel 35
23	Channel 12	23	Channel 36
21	Channel 13	21	Channel 37
19	Channel 14	19	Channel 38
17	Channel 15	19	Channel 39
15	Channel 16	15	Channel 40
13	Channel 17	13	Channel 41
11	Channel 18	11	Channel 42
9	Channel 19	9	Channel 43
7	Channel 20	7	Channel 44
5	Channel 21	5	Channel 45
3	Channel 22	3	Channel 46
1	Channel 23	1	Channel 47
49	+5V dc OUT	49	+5V dc OUT
2 through 50	Digital Ground	2 through 50	Digital Ground

DVME-660 Board Identification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+ 3	M	This ASCII code is present
+ 5	E	for all DATEL VMEbus boards
+ 7	I	
+ 9	D	
+ 0B	D	Manufacturer ID
+ 0D	A	DAT is the ID for DATEL
+ 0F	T	
+ 11	d	Board model number
+ 13	V	
+ 15	M	
+ 17	E	
+ 19	—	
+ 1B	6	
+ 1D	6	
+ 1F	0	

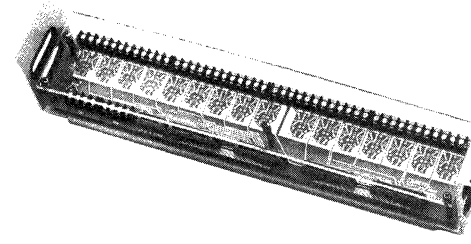
DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base + 64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	----------	Not Used ----------
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples RTD's, strain gage, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	----------	Not Used ----------
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board DVME-628: 8-channel D/A board
Base + 176 through Base + 191	----------	Not Used ----------
Base + 192 through Base + 255	----------	Not Used ----------

DVME-691A and -691D
Rack-mounted, Signal-Conditioning Screw Terminator Panel

FEATURES

- **Rack-mounted screw-terminations for factory wiring**
- **Two models available:**
  DVME-691A for analog inputs
  DVME-691D for analog outputs
- **Both versions have component etch wiring ready to accept discrete components for signal conditioning**
- **DVME-691A Version includes component pads for shunts, attenuators, filters, and spike clamps**
- **DVME-691D Version includes component pads for current loop excitation**
- **DVME-691A handles up to 32 single-ended inputs**
- **DVME-691D provides up to eight analog output channels**
- **Designed for 19 inch RETMA racks**
- **Complete with mounting hardware and cables**
- **Plexiglas safety shield for connector labeling**



THE DVME-691A AND DVME-691D TERMINATION PANELS OFFER A CONVENIENT WAY OF INTERFACING FIELD WIRING TO DATEL'S LINE OF VMEbus BOARDS. IN ADDITION, THE PANELS ARE DESIGNED TO INCORPORATE DISCRETE SIGNAL CONDITIONING COMPONENTS FOR EITHER ANALOG INPUTS OR OUTPUTS.

GENERAL DESCRIPTION

Offering a convenient method of connecting A/D or D/A channel wiring through screw terminators, the DVME-691 rack-mount interface panel is ideal for industrial and process control analog I/O connections. Field cabling need no longer be brought directly to the I/O connectors of the VMEbus boards. Instead, the user terminates all field wiring at the panel then uses DATEL's ribbon cabling system to bring signals to the specific boards.

The 3.5-inch high panel mounts into a standard RETMA 19" rack, letting the unit mount directly in the same rack as the user's VMEbus cardcage. All interwiring consists of flat ribbon cables, affording a quick disconnect capability.

Both versions interface I/O channels of DATEL's VMEbus boards to the user's field wiring using dedicated connectors, signal paths, and additional etch for user-installed discrete components. The DVME-691A can accommodate up to 32 single-ended or 16 differential analog input channels, plus two analog output channels. The DVME-691D accommodates up to eight analog output channels.

As supplied by the factory, signals pass from the screw terminals to specific flat ribbon connectors via etched circuitry. The user's sensor, transducer, and actuator cabling connects to screw terminals on the top portion of the DVME-691's. Prior to passing the signals on to the VMEbus cards, the user may introduce signal conditioning circuitry using the provided etch layout. The user solders in discrete components per the application requirements, cutting the etch (where necessary) which normally connects the input to the output connectors.

The DVME-691A and DVME-691D include five-foot-long flat cables used to pass the signals directly to DATEL's DVME-600 Series of high-performance VME A/D and D/A boards.

The mounting bracket, included in both versions, also has a Plexiglas safety shield which accommodates labeling requirements.

Two Versions for A/D or D/A

The DVME-691A and DVME-691D differ only in the placement and pinout of mating flat cable connectors. For analog inputs, Model DVME-691A accepts up to 32 single-ended or 16 differential inputs, as supplied by DATEL's 32S/16D-channel DVME-611 A/D board. The DVME-691A has two additional channels designated as analog output channels when using DATEL's DVME-612 combination A/D-D/A board.

For analog input channel expansion (up to 256 channels), the DVME-691A also works with DATEL's DVME-641 and DVME-645 slave analog input multiplexer channel expander boards. These expanders share the same A/D converter on the A/D master board, offering low channel costs and a simple means of adding more channels.

For analog outputs, Model DVME-691D distributes up to 8 D/A channels. The DVME-691D is directly compatible with DATEL's DVME-624, -626, -628 and -620 Series D/A boards.

FUNCTIONAL SPECIFICATIONS

(Apply to the DVME-691A and DVME-691D unless otherwise noted.)

DVME-691A

Number of Analog Input Channels . . . . 32 single-ended or 16 differential plus 2 DVME-612 D/A channels.

Connections per Channel . . . . . Hi, Lo, Ground (Differential) and G,H,H,G,H,H, ... (Single-ended). Single-ended inputs share one ground for every two channels. There are 48 A/D terminals, total.

There are 4 screw terminals for the DVME-612 D/A outputs.

DVME-691D

Number of Analog Output Channels . . . 8 voltage outputs or current loops.

Connections per Channel . . . . . Voltage output, voltage return, current loop voltage, current loop output, current loop return. There are 5 terminals per D/A channel.

DVME-691A and DVME-691D

Screw Terminal Type . . . . . Barrier terminals using 6-32 screws on 0.325" centers, suitable for lugs or bare wire, 16 gauge or smaller.

Mating Cables . . . . . Two 25-conductor flat cables are included to mate with DATEL's DVME-600 Series boards. The board end includes a DB-25P connector. The DVME-691 end includes a 26-pin self-keying flat cable header connector. Cable length is five feet.

The 691A also includes a five foot, 10-pin flat cable and DB-9P connector for the 2 DVME-612 D/A channels.

Front Safety Shield . . . . . 0.125" thick Plexiglas shield accepts user terminal labelling. Remove shield for signal conditioning component installation.

Signal Conditioning . . . . . Component Pads accept user-supplied passive components for voltage attenuation, current shunt, RC filters, protective clamps, loop excitation, etc.

DC Power Rails . . . . . Bipolar DC power from a user-supplied power supply is distributed to all channels for loop excitation, clamps, etc. The rails are brought out to screw terminals for power supply connection.

Outline Dimensions . . . . . 19" W x 3.5" H x 4.62" D with mounting slots on 3" vertical centers and 18.5" horizontal centers. (Suitable for 19" RETMA rack mounting).

Operating Temperature . . . . . 0 to +70 degrees Celsius

COMPATIBILITY TABLE

TERMINATOR	USED WITH	TOTAL NUMBER OF CHANNELS
	Analog Inputs	
DVME-691A	DVME-611/612	32S or 16D A/D plus 2 D/A
DVME-691A	DVME-641	32S or 16D Slave multiplexing A/D *
DVME-691A	(2)DVME-645	16S or 8D Simultaneous sample/hold *
	Analog Outputs	
DVME-691D	(2)DVME-624	8 Isolated D/A or 4-20 mA loop outputs
DVME-691D	DVME-626	6 High-resolution D/A
DVME-691D	DVME-628	8 D/A or 4-20 mA loop outputs

* (The slave MUX boards require a host DVME-611 or 612 A/D board).

DATEL's DVME-602 and DVME-643 boards include their own screw terminal interfaces and do not connect to the DVME-691.

Signal Conditioning Component Pads

DATEL ships the DVME-691 with straight-through connections between external devices and analog channels. However, the DVME-691 easily adapts to an extensive variety of signal conditioning circuits. Circuits consisting of passive components (resistors, capacitors, diodes, etc.) install directly on the 691's printed circuit board using etch provided.

The plated-through PC board pads are pre-drilled and clearly identified by screening labels. As configured, the pads support circuits for input attenuation, current shunt input (including 4-to-20 mA applications), noise filtering, and overvoltage protection clamps.

OUTLINE DIMENSIONS (TOP VIEW) IN (mm)

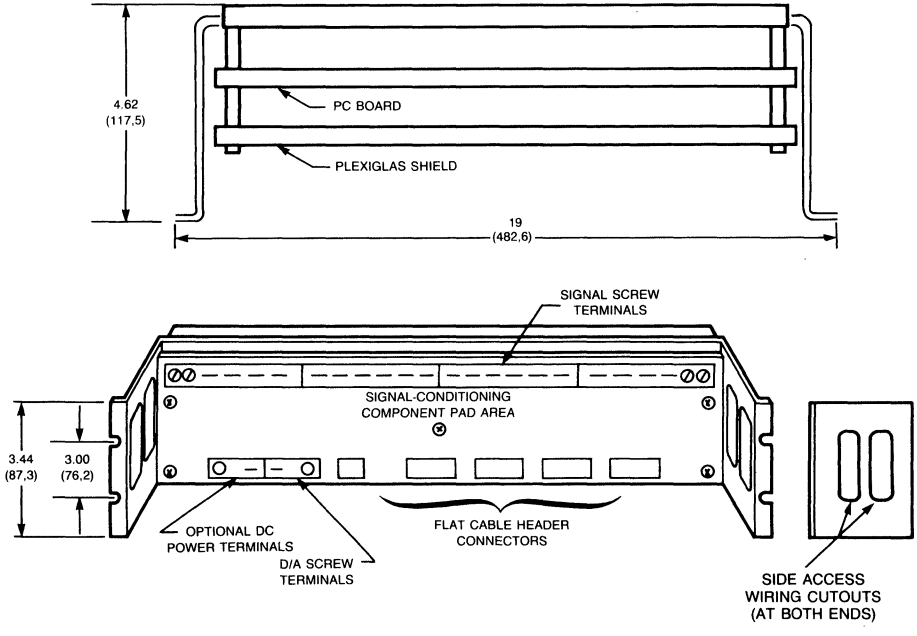


Figure 1. Connector Locations/Dimensions

DC Power Rails

Adjacent to each channel are bipolar dc power supply rails. These may be used for clamp circuits, for sensor excitation, or open-circuit detection. The dc rails are brought out to screw terminals suitable for connection to an adjacent dc power supply. There is ample room to mount a supply on standoffs on the rear of the DVME-691. Voltages up to ±15V dc may be distributed to each channel.

For D/A outputs, the signal conditioning pads could be used for excitation of 4-to-20 mA current loops. Such excitation circuits would use the dc power supply, the distributed dc rails, and current-excitation resistors on a per-channel basis.

Signal Conditioning Circuitry

Signal-conditioning circuitry can be of the user's design or DATEL can provide the design, testing, and installation of such circuitry under special quantity order.

Sensor Families

As configured, the DVME-691A is ideal for voltage and millivolt-input sources. These include bridges, strain gages, load cells, and RTD's. The DVME-691 adapts to 4-to-20 mA loop inputs by adding current loop shunts. The DVME-691A accepts thermocouple inputs if the user supplies external cold junction compensation (CJC).

Alternatively, electronic CJC may be provided on the A/D board by using DATEL's Model DVME-602T or DVME-643T slave thermocouple channel expander boards. These two products include their own front panel screw terminals. For a stand-alone 4-channel RTD A/D board with screw terminals, refer to DATEL's DVME-602R.

OTHER FEATURES

The DVME-691 is intended for factory-floor, industrial, and laboratory applications. As shown in Figure 1, the screw terminals accept field signal wiring either as bare wire or terminated with strain-relieved lugs. Access holes in the sides of the DVME-196 permit routing the wiring through the rear of the DVME-691. Because of this access, several DVME-691's can mount above each other in the same rack or directly adjacent to the host A/D-D/A computer.

The DVME-691 also includes a transparent safety shield which prevents accidental contacts while providing a means of labelling each connection. The DVME-691 does not protrude from the rack.

TYPICAL RACK-MOUNT APPLICATION

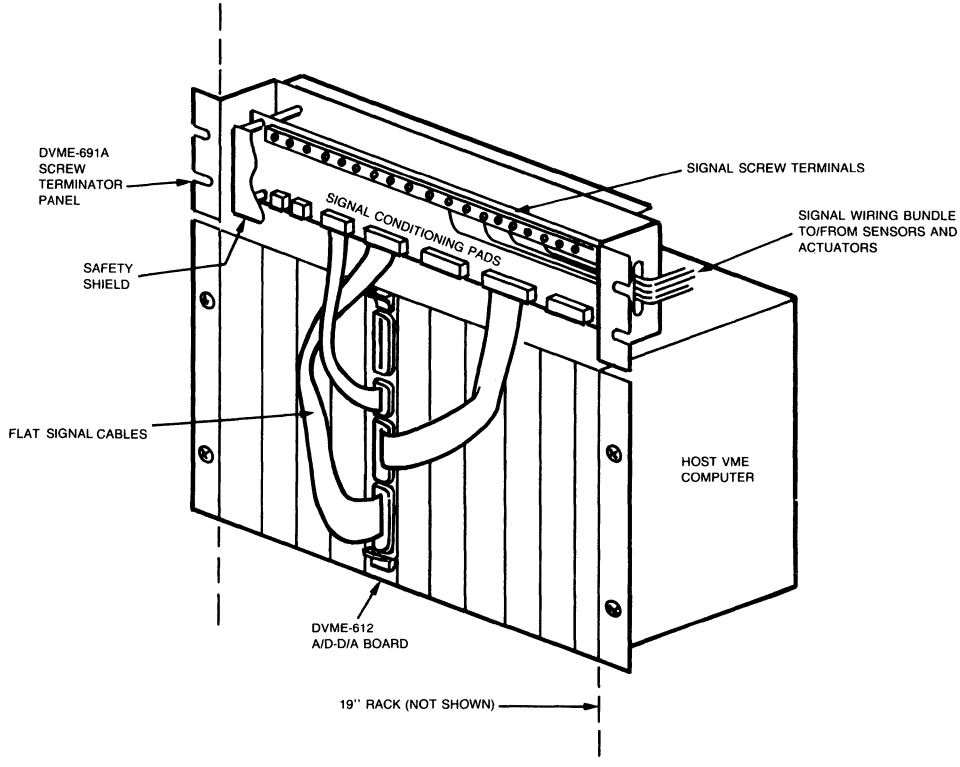


Figure 2. Typical Rack-Mount Configuration

Typical Rack Mount Application
(Figure 2)

This diagram shows the DVME-691 mounted in a 19″ rack adjacent to its host computer. Three supplied flat cables connect the DVME-691 to a Model DVME-612 combination A/D-D/A board. The DVME-691 may be positioned either above or below the computer. The cables are each one meter long so that, if required, the 691 may be located in an adjacent rack.

Before connecting the field wiring, the 691's PC board is removed for optional signal conditioning component installation by the user. Signal wiring for input sensors and transducers or output devices connects to the screw terminals along the top of the DVME-691. This wiring may be collected in bundles and routed either through the slots at the ends of the DVME-691 or over the top edge. Wire bundle routing through the slots allows adjacent equipment to be rack-mounted immediately above the DVME-691.

This application uses three flat cables — two for A/D signals and the third for the two DVME-612 D/A channels. User-supplied dc power, if required for sensor excitation or protective clamps, would connect to the screw terminals at the lower left corner of the DVME-691. Ample room is available on the rear mounting bracket to attach a small dc power supply.

Signal Conditioning Pads per Channel
(Figure 3)

This drawing shows the arrangement of PC board circuit pads for each analog channel. The user selects and installs suggested components shown in the illustration. (DATEL will review custom applications under special order). The pad area is intended for a wide range of applications and the user does not have to use the components indicated. As supplied, connections are made straight-through from the screw terminals.

DC power rails are bussed to each channel and are brought out to screw terminals.

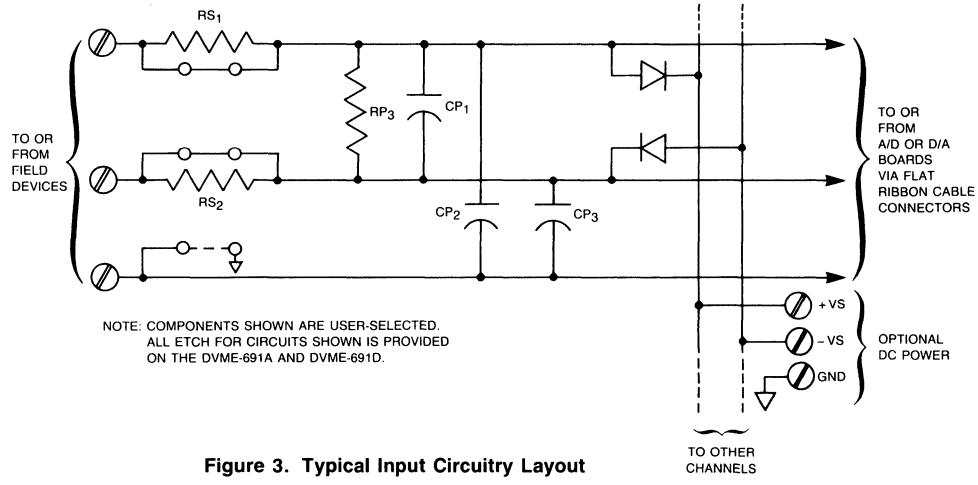


Figure 3. Typical Input Circuitry Layout

Filters and Attenuators

When measuring some signals, it may become necessary to filter out unwanted noise or to attenuate the signals prior to passing them to the analog-to-digital converter board. The DVME-691A provides the user with a convenient area for user-configured passive signal conditioning.

Figures 4, 5, and 6 show typical configurations of simple high-pass, low-pass, and attenuator circuits.

Typical values for a high-pass filter

If the desired cutoff frequency (Fc) is 60 Hz and if Rp is chosen as 10K ohms for differential inputs into the DVME-691,

$$\text{then, } Cs = \frac{1}{2\pi\,(Rp)\,(Fc)} = \frac{1}{2\pi\,(10K)\,(60)} = 0.265\ \mu F$$

Refer to Figure 4, installing a 0.265 μF capacitor in the place of RS1 and a 10K ohm resistor in place of RP3.

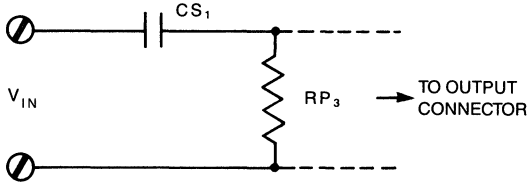


Figure 4. Typical High-Pass Filter

Typical Values For a Low-pass Filter

If the desired cutoff frequency (fc) is 40 Hz, and if Rs is chosen as 20K ohms for single-ended inputs into the DVME-691,

$$\text{then, } Cp = \frac{1}{2\pi\,(Rs)\,(fc)} = \frac{1}{2\pi\,(20K)\,(40)} = 0.2\mu F$$

Refer to Figure 5, installing a 0.2μF capacitor in the place of CP2 and a 20K ohm resistor in place of RS1.

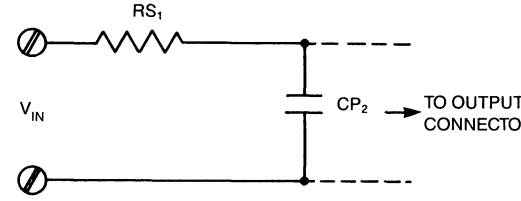


Figure 5. Typical Low-Pass Filter

Typical Attenuator Circuit

If the input signal is 50V dc and the input circuit device can only handle +10V dc maximum, an attenuation circuit can be made up as follows:

If choosing a 100K ohm resistor for Rs,

$$Rp = \frac{Vp\ Rs}{Vin - Vp} = \frac{10(100K)}{50 - 10} = \frac{1\ \text{megohm}}{40} = 25K\ \text{ohms}$$

Refer to Figure 6, installing a 25K ohm resistor in the place of RS3 and a 100K ohm resistor in place of RS1.

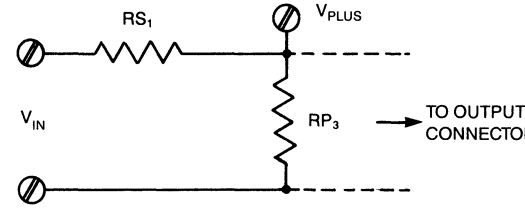


Figure 6. Typical Attenuation Circuitry

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ORDERING GUIDE

Model Number	Description
DVME-691A (for VME)	Screw terminator panel for 32 single-ended or 16 differential analog input and 2 analog output channels (includes 3 cables for DVME-611/612 boards).
DVME-691D (for VME)	Screw terminator panel for 8 analog output channels (includes 2 cables for DVME-62X series boards).

Contact DATEL for custom component configurations.

DVME-UTIL
VMEbus SOFTWARE UTILITIES for VERSAdos or PDOS

DATA ACQUISITION SOFTWARE UTILITIES SUPPORTING ALL DATEL VMEbus BOARDS

(Except DVME-601. Contact DATEL for DVME-601 software.)

FEATURES

- **Three main program modules**
  1. **UTIL module data acquisition functions**
     a) **Physical-to-logical channel mapping**
     b) **Typical data acquisition routines**
  2. **IOSUBR module I/O console tasks**
     a) **Input/output console routines**
     b) **ASCII conversion routines**
  3. **MATCH high-level language module and interface for passing paramaters.**
- **Easy integration to user application software**
- **Includes a demonstration program written in "C" to exercise all utilities**
- **All modules written in linkable 68000 assembly language code**
- **All routines callable using assembly language and "C" language main programs**
- **Includes fully commented source code and user's manual**
- **VERSAdos-compatible and PDOS-compatible versions currently available**

The DVME-UTIL software package offers complete data acquisition software support for all DATEL VMEBUS I/O boards. Source code for all of the routines is provided for easy integration into users' application programs. The software modules offer physical-to-logical channel mapping, analog and digital I/O functions, console I/O utilities, high-level language compatibility, and even an example demonstration program written in "C."

GENERAL DESCRIPTION

The DVME-UTIL integrates DATEL's DVME family of VMEbus analog I/O boards to the user's application program. DVME-UTIL relieves the system programmer's burden of writing application software to drive and manage multiple analog and digital I/O boards. The full set of data acquisition utilities are callable from either 68000 assembly language or "C" language main programs. Other high-level languages can be easily supported by modifying the parameter passing module.

The main feature of the DVME-UTIL is that all of DATEL's VMEbus boards are directly usable without the user's concern for the physical location of the on-board registers. At initialization time a physical-to-logical channel map is generated. Once initialized, all data acquisition functions are accomplished through logical symbol specifiers.

The DVME-UTIL software comes complete with a detailed software manual and two 5¼"diskettes formatted for either the VERSAdos or PDOS operating systems. The diskettes contain 68000 assembly source codes and object codes for all the routines. The diskettes also contain an example demonstration program, SHOUTIL written in "C." The list file, link list, and executable code of the SHOUTIL is also included. A chain, or procedure, file is also included to serve as an example of how the DVME-UTIL modules can be assembled and linked to a main program. The manual describes each subroutine in explicit detail and provides syntax for using with assembly and "C" language programs. The user's manual also provides examples for each routine.

FUNCTIONAL DESCRIPTION

The DVME-UTIL essentially consists of three functional modules. The modules are UTIL, IOSUBR, and a high-level language MATCH module.

The UTIL module contains routines categorized into six classes. The six classes of the routines perform functions relating to initialization, analog input, analog output, thermocouple/RTD input, expansion connector, and digital I/O. Refer to Table 1 for a description of the routines in this module. The UTIL module implements a logical channel concept which maps physical board addresses and channel numbers to logical channel references. When running the VERSAdos version, and depending on the total number of channels being mapped, one or more pages of system RAM are attached to the running task. When running the PDOS version, the user must allocate sufficient free RAM space. This RAM area is used to hold the channel control tables which provide the physical-to-logical channel mapping. Simple subroutine calls to the UTIL module replace many lines of code that would be required by the user's main program software. In addition to inter-board physical-to-logical channel mapping, there are subroutines which perform many of the typical data acquisition functions. Any required operating system interaction is taken care of by the UTIL module.

The IOSUBR module contains 15 console input/output and ASCII conversion routines. Although the UTIL module only calls a few of these routines, the entire IOSUBR module is available for the user's application program. Refer to Table 2 for a description of the routines in this module.

The MATCH module allows calling the routines in UTIL and IOSUBR modules using "C" language programs compatible with Whitesmith's parameter passing convention. The MATCH module copies the arguments of "C" language programs into the appropriate registers in the UTIL and IOSUBR routines. Data passed back to the calling program is also taken care of by the MATCH module. Matching modules for other compiler types can easily be written to meet different parameter passing requirements.

There are two possible ways to interface to UTIL and IOSUBR module subroutines. Most high-speed and memory critical applications will require that the main applications program be written entirely in assembly language. In order to meet the high-speed requirements, DVME-UTIL subroutines use 68000 internal registers where ever possible. Other less time critical applications could have their main program written in a high level language such as "C." In these applications use the MATCH module. Figures 1 and 2 show the data flow to the DVME-UTIL from main programs written in assembly language and Whitesmith's "C" respectively.

ORDERING INFORMATION	
DVME-UTIL/V	VERSAdos version
DVME-UTIL/P	PDOS version

IBM-PC/XT/AT 5¼" disk format is also available.

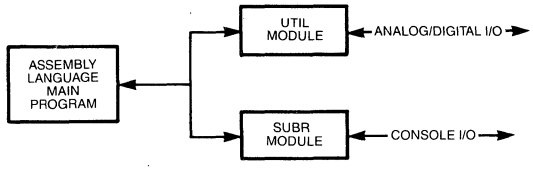


Figure 1. Data Flow for Using DVME-UTIL With Assembly Language

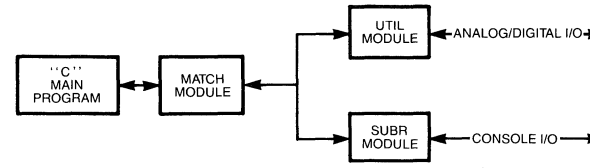


Figure 2. Data Flow for Using DVME-UTIL With "C" Language

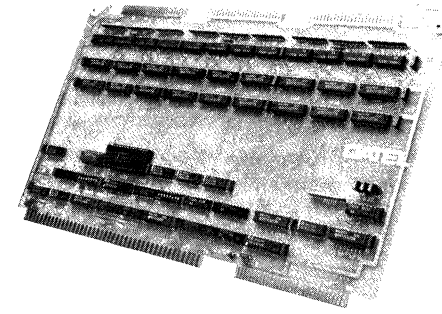
Table 1. List of Routines in the UTIL Module

SUBROUTINE CLASS	SUBROUTINE	DESCRIPTION
Initialization	INICCT	Initializes channel control tables.
	MAPAD	Maps all A/D channels to logical reference.
	MAPDA	Maps all D/A channels to logical reference.
	MAPTH	Maps all thermocouple/RTD input channels to logical reference.
	MAPDI	Maps all digital I/O channels to logical reference.
	SHOMAP	Displays physical-to-logical map.
Analog Input	ALADIN	Controls interrupt allocation for interrupt driven A/D conversion.
	ENADIN	Enables/disables A/D input in the interrupt mode.
	ADTRC	Enables/disables A/D conversion on an external trigger.
	ADGAI	Loads gain value.
	ADSNG	Performs a single channel scan on a logical channel.
	NADSNG	Perfoms "N" scans on a single logical channel.
	ADSCN	Performs a single sequential chanel scan on logical channels specified.
	NADSCN	Performs "N" scans on logical channels specified.
	ADRDM	Performs single scan on channels from a table of random logical channels.
	NADROM	Performs "N" scans on channels from a table of random logical channels.
	INFSNG	Initializes A/D registers for fast A/D operations on a single logical channel.
	FSTSNG	Performs a fast scan on a channel.
	FSNSNG	Performs "N" fast scans on a channel.
	INFSCN	Initializes A/D registers for fast A/D operations on a sequential channel scan.
	FSTSCN	Performs a fast scan on sequential channels.
	FSNSCN	Performs "N" fast scans on sequential channels.
Analog Output	DASNG	Provides a single output to a logical channel.
	DASCN	Provides buffered output data to sequential logical channels.
	DARDM	Provides buffered output data to random logical channels.
Thermocouple/ RTD Input	ALTHIN	Controls allocation of interrupts for interrupt driven thermocouple/RTD inputs.
	ENTHIN	Enables/disables thermocouple/RTD inputs in interrupt mode.
	THSNG	Performs a single scan on a thermocouple/ RTD input logical channel.
	NTHSNG	Performs "N" scans on a thermocouple/ RTD logical channel.
	THSCN	Performs a sequential scan on logical channels.
	NTHSCN	Performs "N" sequential scans on thermocouple/RTD logical channels
	THRDM	Performs a scan on thermocouple/RTD channels from a random channel table.
	NTHRDM	Performs "N" scans on thermocouple/RTD channels from a random channel table.
Expansion Connector Digital Output	ADGP0 } ADGP1 }	Provide a single bit digital output on two pins on a DVME-611/612 board.
	THGP0 } THGP1 }	Provide a single bit digital output on two pins on a DVME-602 board.
Digital I/O	ALTRIN	Controls allocation of external trigger generated interrupts from a DVME-660 board.
	ALCMIN	Controls allocation of port 0 comparator register generated interrupts from a DVME-660 board.
	ALTMIN	Controls allocation of timer generated interrupts from a DVME-660 board.
	ENDGIN	Enables/disables interrupts on a DVME-660 board.
	LODDIR	Loads port direction bits in a DVME-660 register.
	LODCMP	Loads port 0/compare register on a DVME-660.
	LED660	Turns on or off an LED on a selected DVME-660 board.
	PRGTIM	Loads the timer control register in a DVME-660 board.
	INPBIT	Accepts a data bit from a logically mapped DVME-660 input port.
	INPBYT	Accepts a data byte from a logically mapped DVME-660 input port.
	INPWRD	Accepts a word from adjacent logically mapped DVME-660 input ports.
	OUTBYT	Provides a byte output to a logically mapped DVME-660 output port.
	OUTWRD	Provides a word output to logically mapped DVME-660 output ports.

Table 2. List of Routines in the IOSUBR Module

SUBROUTINE	DESCRIPTION
ASCHEX	Converts "N" number hex ASCII characters to binary format.
HEXDEC	Converts a 16-bit hex number to a decimal ASCII string.
GETID	Builds a VMEbus ID output buffer from the ID PROM on a DVME board.
HEXASC	Converts a 16-bit hex number to a hex ASCII string.
PRCR	Outputs an ASCII message to the console followed by a carriage return and line feed.
PRNCR	Outputs an ASCII message to the console without a carriage return or line feed.
OHXCR } OHXNCR }	Convert a 16-bit number to hex ASCII and displays it on the console with or without a carriage return.
PROMPT	Provides an ASCII message to the console and waits for the console input.
CRLF	Provides carriage return and line feed output.
MAKECAP	Converts a string of ASCII characters into all capitals.
PMTCHR	Provides an ASCII message output to the console and waits for a single character input.
SHOCHR	Provides a single character output to the console.
INPCHR	Accepts a single character input from the console.
SMPCON	Samples the console for any possible input. On receiving any input halts I/O operation and sets "Z" condition flag.

ST-519 MULTIBUS
72-Line Digital I/O Board With Interrupt



FEATURES

- **72 Individually-programmable input/output lines**
- **IEEE 796 MULTIBUS Compatible**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Memory mapped, optional I/O map**
- **20- or 16-bit user-selectable base address (24-bit base address optional)**
- **Eight maskable interrupt lines**
- **Interfaces to pluggable modules for 2.5KV isolation**

DATEL expands its line of MULTIBUS compatible system boards with the ST-519. The ST-519 provides 72 individually-programmable lines for input or output (I/O). Also, an interrupt controller is provided to allow up to eight user-programmable interrupt lines. Like other DATEL MULTIBUS products, the ST-519 is fully hardware- and software-compatible with all MULTIBUS microcomputers. All necessary address decoders, logic controls, and data transceivers are incorporated on board.

DESCRIPTION

The DATEL ST-519 is a MULTIBUS-compatible system board providing 72 software programmable input/output (I/O) lines. These I/O lines are fully TTL compatible and each line can be individually programmed as either an input or an output.

The ST-519 may be used with both 8- and 16-bit microprocessors. The BHEN/line on the MULTIBUS sets the ST-519's address decoders and data latches for compatibility with 8- or 16-bit computers. The ST-519 also supports 24-bit MULTIBUS addressing capability, and is downward compatible with 16- or 20-bit address systems.

The ST-519 has an 8259A Programmable Interrupt Controller which provides vectoring information for eight user-definable interrupt levels. In normal slave operation, the Interrupt Request (IR) lines of the 8259A are hard-wired to an I/O line. When the I/O event occurs the 8259A generates an Interrupt (INT) which would go to one of the MULTIBUS vector interrupt lines INTØ thru INT7.

The 72 I/O lines are brought out on three 50-pin edge-card connectors: J1, J2, and J3. These edge-card connectors are fully compatible to the Gordos and OPTO 22 type pluggable modules systems that offer an input to output isolation of 2.5K VAC. A flat ribbon cable interconnects the DATEL ST-519 to other electronic module systems.

The ST-519 is a memory-mapped peripheral occupying 16 consecutive locations in the computer's address space. The board's base address is preset at ØØFFAØ hex. However, a user may relocate the board address anywhere up to FFFFFØ on 16-byte boundaries using DIP switches on the board.

In order to make the ST-519 compatible with different speed CPU and memory systems, a transfer acknowledge delay (XACK/DELAY) is provided. This permits 8 selectable delays from 100 to 800 nanoseconds.

The ST-519 is fully bus- and card-cage compatible with the MULTIBUS and IEEE 796. The board is 12.0"W x 6.75"D x 0.47"H (305 x 172 x 12 mm). When used with the standard MULTIBUS card cage, the ST-519 board may be installed adjacent to other boards.

The ST-519 draws all power from the MULTIBUS +5V dc power line. The ST-519 weighs approximately 12 ounces (0,341 kg). It can operate over a temperature range of 0 to +55 degrees Celcius with relative humidity from 10 to 90% (noncondensing), and from 0 to 15,000 feet (0 to 4,600 m) in altitude.

ORDERING GUIDE

MODEL	DESCRIPTION
ST-519	72 line digital I/O board with interrupt

FUNCTIONAL SPECIFICATIONS

CHANNELS

I/O number of channels..... 72 I/O Channels
Channel expansion.... Indefinite channel expansion using separate ST-519 boards at different base addresses; limited by available card slots and supply current

OUTPUT DRIVER

Output current sink (Vout = 0.6V)..... 24 mA (max.)
Output current source (Open collector 4.7KΩ from +5V)..... 1 mA (max.)

INPUT RECEIVER

High level input current (Vin = 2.7V).....100 µA (max.)
Low level input current (Vin = 0.4V).....-1.2 mA (max.)

ADDRESSING

Occupies a block of 16 consecutive memory (I/O) locations. Base address may be located on any 16 byte boundary in the 20-bit (24-bit optional) address space by two DIP switches.

PHYSICAL

Outline Dimensions... 12.00"W x 6.75"D x 0.50"H (max.)
304,8W x 171,5D x 12,7H mm
Weight..... 12 ounces (0.34 kg)
Operating Temperature Range..... 0 to +55°C
Storage Temperature Range..... -25 to +85°C
Relative Humidity..... 10% to 90% non-condensing
Altitude..... 0 to 15,000 feet (4,600 m)

POWER CONSUMPTION +5V dc ±5%

ST-519 (stand alone)..... 1.7 A typical
ST-519 + 72 I/O modules.....3.3 A typical

GENERAL

Bus Compatibility..... Pin-for-pin, card guide, and program compatible with MULTIBUS (IEEE 796) and SBC series microcomputers
CPU Compatibility.....8 or 16 bit compatible

DATA FORMAT

The ST-519 is a memory-mapped peripheral that appears to the system CPU as 16 bytes of consecutive memory. These registers can be accessed as 16 single bytes (8-bit CPU) or as 8 double bytes (16-bit CPU).

The ST-519 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS pin 27 of connector P1 goes to zero volts. A high input on BHEN/, consequently, sets the board for an 8-bit format.

INTERRUPT

An 8259A Programmable Interrupt Controller provides onboard interrupt generation to the host's interrupt controller. This device generates interrupts on low-to-high transitions from user-selected digital inputs coming into the ST-519. Jumpers (pins 64 through 71) tie the selected digital input lines directly to the selected IR interrupt.

Jumper pins 64 through 71 have two different uses based upon the mode of operation. In one mode, the MULTIBUS interrupt priority level (INT 0-7) is jumper-selectable between pin 111 (INT) and the jumper pins for the priority levels as outlined below (pins 103, 104, 105 . . .). For this single-interrupt scheme, the user wires the interrupt source to an interrupt input pin (pins 64 through 71). Jumper pins 97 through 101, 109 and 110 are not used in this mode.

In the other mode, up to eight interrupt levels are defined using eight digital input bits to the ST-519. Each input has a jumper, pins 97 through 113 (excluding 111). Pins 64 through 71 are user-prioritized and connected (through buffers and jumpers) to the MULTIBUS INT 0-7 lines. This mode bypasses the 8259A and its interrupt vector address function. Use this mode when the host provides the necessary vectoring information for servicing the interrupt caused by the digital input.

8259A		MULTIBUS	
Line Name	ST-519 Jumper Pin#	Line Name	ST-519 Jumper Pin#
INT	111	INT0	112
IR0	67	INT1	113
IR1	68	INT2	107
IR2	66	INT3	108
IR3	71	INT4	105
IR4	65	INT5	106
IR5	70	INT6	103
IR6	64	INT7	104
IR7	69		

CONNECTORS

The ST-519 board contains five connectors: P1 and P2 are the MULTIBUS connectors, and J1, J2, and J3 are the digital I/O connectors.

The P2 MULTIBUS connector is used only when a system controller's address capability is 24 bits. The pin assignment for the four extended address lines on P2 are shown in Table 1.

The digital I/O lines use connectors J1, J2, and J3; Table 2 describes these connections.

Table 1. MULTIBUS Connector P2

PIN	SIGNAL	Functional Description
55	ADR 16	
56	ADR 17	4 address line inputs for 24
57	ADR 14	bit address controllers
58	ADR 15	

Table 2. I/O Connector

Connector Pin Number	J1 Register Addr	J1 Bit	J2 Register Addr	J2 Bit	J3 Register Addr	J3 Bit	I/O Module	Connector Pin Number	J1 Register Addr	J1 Bit	J2 Register Addr	J2 Bit	J3 Register Addr	J3 Bit	I/O Module
2	2	7	5	7	8	7	23	26	1	3	4	3	7	3	11
4	2	6	5	6	8	6	22	28	1	2	4	2	7	2	10
6	2	5	5	5	8	5	21	30	1	1	4	1	7	1	9
8	2	4	5	4	8	4	20	32	1	0	4	0	7	0	8
10	2	3	5	3	8	3	19	34	0	7	3	7	6	7	7
12	2	2	5	2	8	2	18	36	0	6	3	6	6	6	6
14	2	1	5	1	8	1	17	38	0	5	3	5	6	5	5
16	2	0	5	0	8	0	16	40	0	4	3	4	6	4	4
18	1	7	4	7	7	7	15	42	0	3	3	3	6	3	3
20	1	6	4	6	7	6	14	44	0	2	3	2	6	2	2
22	1	5	4	5	7	5	13	46	0	1	3	1	6	1	1
24	1	4	4	4	7	4	12	48	0	0	3	0	6	0	0

1–49: All odd number pins are tied to ground.

REGISTER

The following chart details the memory address assignments of the 16 memory locations the ST-519 occupies. Please note that when the ST-519 is used with 16-bit CPU's, every other (even-numbered) address location is used.

ST-519 Register Assignments

8 BIT CPU ADDRESS	FUNCTION	REGISTER	COMMENTS	ADDRESS (16 BIT CPU)
BASE + 0	WRITE	WRITE OUTPUT 0–7	REG 0 J1	
BASE + 0	READ	READ INPUT 0–7		BASE + 0
BASE + 1	WRITE	WRITE OUTPUT 8–15	REG 1 J1	
BASE + 1	READ	READ INPUT 8–15		
BASE + 2	WRITE	WRITE OUTPUT 16–23	REG 2 J1	
BASE + 2	READ	READ INPUT 16–23		BASE + 2
BASE + 3	WRITE	WRITE OUTPUT 24–31	REG 3 J2	
BASE + 3	READ	READ INPUT 24–31		
BASE + 4	WRITE	WRITE OUTPUT 32–39	REG 4 J2	
BASE + 4	READ	READ INPUT 32–39		BASE + 4
BASE + 5	WRITE	WRITE OUTPUT 40–47	REG 5 J2	
BASE + 5	READ	READ INPUT 40–47		
BASE + 6	WRITE	WRITE OUTPUT 48–55	REG 6 J3	
BASE + 6	READ	READ INPUT 48–55		BASE + 6
BASE + 7	WRITE	WRITE OUTPUT 56–63	REG 7 J3	
BASE + 7	READ	READ INPUT 56–63		
BASE + 8	WRITE	WRITE OUTPUT 64–71	REG 8 J3	
BASE + 8	READ	READ INPUT 64–71		BASE + 8
BASE + 9	—	NOT USED		
BASE + A	WRITE	CLEAR OUTPUT REG 0–7	CLR REG 0	
BASE + A	READ	READ CLEAR REG		BASE + A
BASE + B	WRITE	CLEAR OUTPUT REG 8	CLR REG 1	
BASE + B	READ	READ CLEAR REG		
BASE + C	WRITE	CONTROL REG 1, 8259A	8259A	
BASE + C	READ	STATUS REG 1, 8259A	INTERRUPT	BASE + C
BASE + D	—	—	CONTROLLER	
BASE + D	—	—	Refer to INTEL data sheet	
BASE + E	WRITE	CONTROL REG 2, 8259A		
BASE + E	READ	STATUS REG 2, 8259A		BASE + E
BASE + F	—	—		
BASE + F	—	—		

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CLEAR REGISTERS

The clear registers are used to clear (reset) the output registers to all 0's. On power-up or system reset, the clear register bits reset all output registers which disables all output lines. Only after the clear register bits have been set to 1's will the output (write) function be enabled.

The clear registers format is shown. Refer to I/O line section for programming of input/output registers.

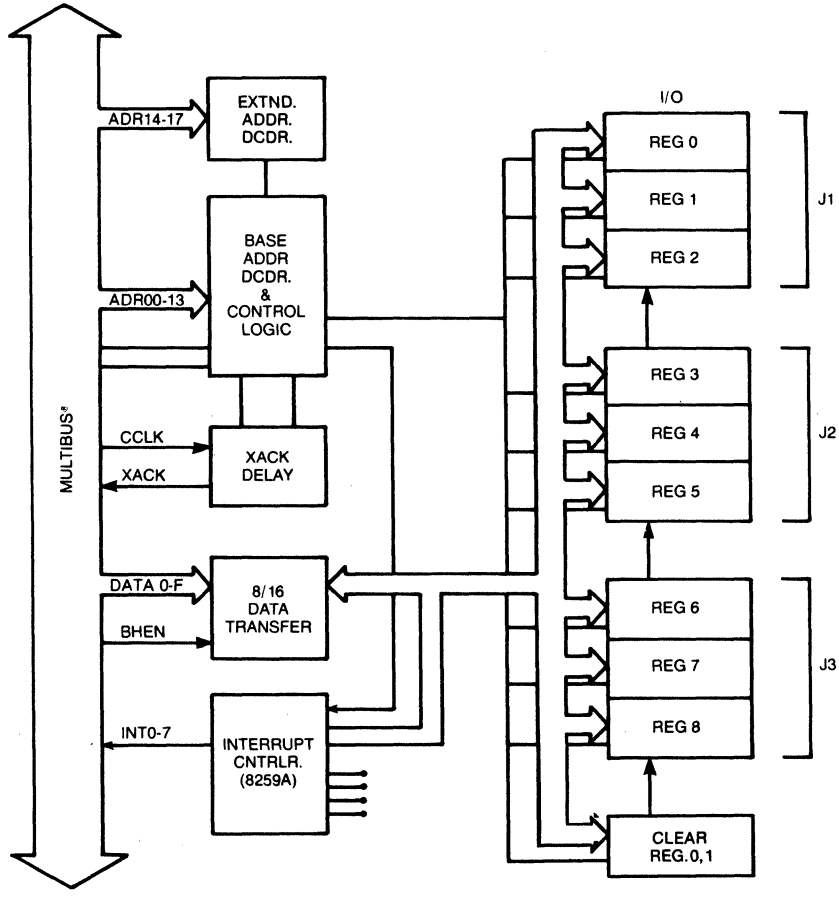
CLEAR REGISTER FORMAT

CLR REG (16 BIT CPU)															
DF							D0								
CLR REG 1 (8 BIT CPU)								CLR REG 0 (8 BIT CPU)							
D7							D0	D7							D0
X	X	X	X	X	X	X	X	8	7	6	5	4	3	2	1	0
DON'T CARE								OUTPUT REGISTER CLEARED							

When a clear register bit is 0, the corresponding output register is cleared forcing output lines to logic high (1).

When a clear register bit is 1, the corresponding output register is enabled to be programmed.

ST-519 Block Diagram



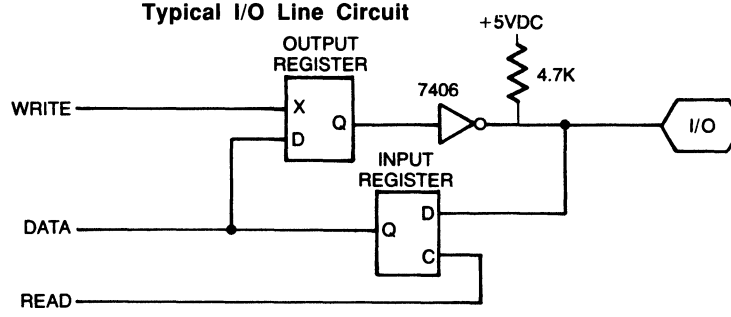
MULTIBUS® is a trademark of the Intel Corp.

I/O LINE

All output lines are comprised of an output latch driving an inverting open collector output buffer. During a write cycle to an output register, the data latched will appear inverted at the edge card connector. If the status of an output line is read back thru the ST-519, the previously written data will appear inverted.

An I/O line which is to be used as an input must have its corresponding output line set to a zero. During a read cycle, data from an input line is the true logic level from the edge card connector.

Typical I/O Line Circuit



24 BIT ADDRESS SELECT

The ST-519 is factory configured for 16- or 20-bit addressing. A 24-bit adddress capability is selected by installing programming plugs and soldering a jumper as follows:

1. Cut and remove etch between 46–47.
2. Install wire jumper between 48–47, solder the jumper.
3. Install programming plugs at 75–83, 77–85, 79–87, and 81–89.

BASE ADDRESS SELECTION

The ST-519 is a memory-mapped peripheral that occupies 16 consecutive, byte-wide, memory locations in the computer address space. The base address decoding supports both 16- and 20-bit addressig with 24-bit address capability being optional. Base address selection is accomplished by setting DIP switches on the PC board.

1. Select a base address, in hex, between 000X (00000X) and FFFX (FFFFFX). Write the base address in the Base Address, Hex boxes.
2. Convert the hex code to binary by writing 1's and 0's in the Hex Bit Weighting boxes.
3. Set the desired base address on DIP switch S1 and S2 or the jumper area for extended address. A switch position ON or a wire jumper corresponds to a "1". An OFF switch position or a removed wire jumper corresponds to a "0". If the CPU provides only 16 address lines, the address switches corresponding to ADR10/ through ADR13/ must be left OFF.

BASE ADDRESS HEX	(0 to F)				(0 to F)				(0 to F)				(0 TO F)				(0 TO F)			
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1	8	4	2	1
ADDRESS BIT #	17	16	15	14	13	12	11	10	F	E	D	C	B	A	9	8	7	6	5	4
SWITCH/ JUMPER POSITION	84-76	86-78	88-80	90-82	S1 1	S1 2	S1 3	S1 4	S1 5	S1 6	S1 7	S1 8	S2 1	S2 2	S2 3	S2 4	S2 5	S2 6	S2 7	S2 8

I/O SELECT

The ST-519 is factory configured as a memory-mapped peripheral. I/O addressing is an option that may be selected by soldering jumpers by:

1. Cutting and removing etch between 96–93 and 95–91.

2. Installing wire jumpers between 94–93 and 92–91; solder the jumpers.

INPUT PORT MODE SELECT

Each I/O line consists of an output latch driving a 7406 open collector output buffer, and an input device which can be jumper programmed as a transparent input buffer or as an input latch.

Each card edge connection (J1, J2, and J3) has a group of three ports with associated logic circuitry and jumpers to provide the end-user with the capability to latch one or more of the input ports on any given event. At each port group there is an inverter/ jumper network to select the polarity of the latching function.

The input ports are factory configured to appear as three-state transparent buffers. The latched input port option is selected by removing circuit-etch jumpers, and then soldering wire jumpers for the input port(s) to be changed. Refer to the Input Port Mode Select chart.

The level and the event that latches the ports must also be selected by the end-user. The port latch event is factory configured to be a positive level (logic level one). A negative level (logic level zero) option is selected by programming plug. The port latch event input must then be hardwired to the event (I/O line, Interrupt Required) that will control the latching of the input port(s).

Refer to the Input Port Mode select chart.

		INPUT PORT		PORT LATCH EVENT		
CONN.	REGISTER	TRANSPARENT (STANDARD)	LATCHED (OPTIONAL*)	POSITIVE (STANDARD)	NEGATIVE (OPTION)	INPUT
	REG 0	7-8	8-9			
J1	REG 1	10-11	11-12	37-43	37-38	49
	REG 2	13-14	14-15			
	REG 3	16-17	17-18			
J2	REG 4	19-20	20-21	39-44	39-40	50
	REG 5	22-23	23-24			
	REG 6	25-26	26-27			
J3	REG 7	28-29	29-30	41-45	41-42	51
	REG 8	31-32	32-33			

*To program to OPTION, first remove etch jumpers under standard and then install and solder option jumpers.

TRANSFER ACKNOWLEDGE (XACK) DELAY SELECTION

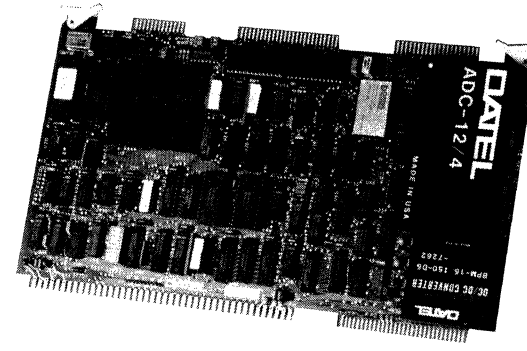
The ST-519 generates a transfer acknowledge (XACK/) signal in response to read or write commands from the MULTIBUS. It is sometimes desirable to delay this signal in order to match this signal to the CPU timing. A jumper selectable transfer acknowledge delay ranging from 100 to 800 nanoseconds is available on the ST-519. It should be noted that the XACK/ delay is generated from the MULTIBUS CCLK/ signal which is assumed to have a period of 100 nanoseconds. Also, since this signal is asynchronous, the actual delay can only be set within a tolerance of one clock period or 100 nanoseconds. The accuracy of the XACK/ delay is dependent on the period (T) of the CCLK signal generated by the host computer. The programming of XACK/ delay is in multiple increments of T, ranging from one to a maximum of eight, refer to XACK/ delay selection table below.

DELAY		JUMPERS
100 nsec.		52-53
200 nsec.	(Standard)	52-54
300 nsec.		52-55
400 nsec.		52-56
500 nsec.		52-57
600 nsec.		52-58
700 nsec.		52-59
800 nsec.		52-60

ST-701 MULTIBUS A/D MICROCOMPUTER BOARD

FEATURES

- On-board 32 single-ended or 16 differential A/D channels with addressing expansion up to 256 channels.
- Selectable 12-, 14-, or 16-bit A/D resolution.
- Maps onto 16-, 20-, or 24-bit host address systems.
- Allows 8- or 16-bit data transfers to any MULTIBUS host.
- True 12-bit A/D transfers of up to 132,000 samples per second.
- On-board 4K dual-ported RAM-to-host data/command/program transfer window controlled by selectable 2-way interrupts.
- EPROM contains Real-time Data Acquisition Executive (RDX) and monitor routines. Both use simple ASCII command structures.
- On-board programmable gain amplifier, dc-to-dc converters.
- 3 general purpose digital I/O lines user-programmable as interrupts, control lines, channel extension selection lines, etc.



- Local Z-80 microcomputer, 8 or 16K EPROM, 8K local RAM, 4K dual-port RAM, timer, interrupt controller, DMA controller and supporting firmware.
- Runs optional memory-downloaded extended-command code blocks.
- Auxiliary asynchronous RS-232/422/423 serial port for commands, user-programmed LAN connection, printer/plotter, etc.

DATEL's ST-701 is much more than the standard analog-to-digital converter board. With its on-board microcomputer and communications capabilities, the ST-701 is an extremely versatile, intelligent device. It is equally powerful at the MULTIBUS subsystem level or as a stand-alone signal processing system.

GENERAL DESCRIPTION

Designed to offload a host MULTIBUS computer, the ST-701 intelligent analog-to-digital board is the newest addition to Datel's line of MULTIBUS boards. It features high performance analog signal conversion, a fast, interrupt-driven host DMA interface, and can accept user-developed programs as well. The ST-701 manages data acquisition activities, offering a high throughput speed of digitized analog input data. This reduces the host computer's software overhead time for signal processing. Unlike conventional analog-to-digital (A/D) converter boards, the ST-701 may be programmed to perform A/D data manipulation (reformatting, data structure conversion, etc.) as well as data collection.

A feature of the ST-701 is its ease of use through the RDX, an EPROM-resident high-level command-line executive. The ST-701 is ideal for development systems. Upon powering up, it appears to the host as an area of non-conflicting Read/Write memory, unaffected by host memory testing. A new, 2-microsecond, 12-bit A/D option is also available (ST-701E).

ORDERING INFORMATION

ST-701

A/D Resolution and Speed	DC/DC Power Converter	MULTIBUS Address Width
A= 12-bit, 20 μS B= 12-bit, 4 μS C= 14-bit, 45 μS D= 16-bit, 400 mS	1= Not included (External +/–15V Required) 2= Included	No designator = 16 or 20 bits /24= 16, 20, or 24 bits

Example: ST-701A2/24 (12-bit, 20μS A/D, with DC/DC, 24-bit addressing).

All models include J1, J2 connectors.
Companion channel expansion slave multiplexer:
ST-742: 32S or 16D channels, non-isolated.
56-8071723: Interconnect flat cable between ST-701 and ST-742 slave MUX board.
EPROM source code is available. Contact DATEL.

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The ST-701 consists of five major hardware sections under local firmware and host software control. Refer to Figure 1.

These hardware sections consist of:

1. Analog input channels,
2. A/D converter module/signal conditioning,
3. Local microcomputer/DMA controller,
4. Communication interface, and
5. the dc power converter circuitry.

The on-board microcomputer consists of a Z80 CPU, dedicated 8K of random-access (RAM) and 8K of read-only (PROM) memory, a 4K dual-port RAM area, a timer, an interrupt controller, and a direct memory access (DMA) controller. The PROM contains all the firmware needed to control all other ST-701 resources via a local bus.

The CPU receives commands through two communications channels: a memory-mapped MULTIBUS interface and an auxiliary asynchronous serial port. Control and programming of the ST-701 uses both local Real-time Data acquisition Executive (RDX) firmware as well as user-written Interrupt Service Routines (ISR's) resident in the host.

On-board ST-701 PROM also contains a simplified high-level ASCII command line interpreter. The ST-701 is ideal for use with high-level application programs,providing automatic control of hardware-intensive, timing-critical A/D functions. Transfers of pre-processed A/D data blocks occur under full interrupt control from the host computer.

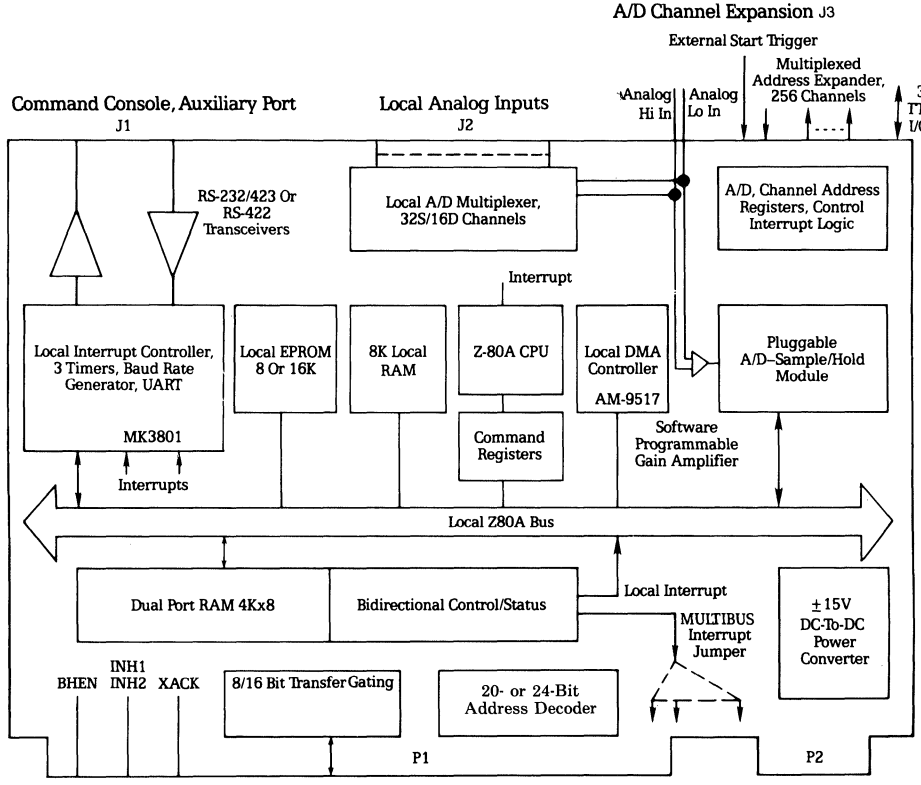

Figure 1: ST-701 Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25 degrees C, unless noted)

ANALOG INPUTS

Number of on-board channels . . . . . 32 single-ended or 16 differential

Number of off-board channels . . . . . up to 224S/240D, using external channel multiplexer (ST-742)

Total addressable channels . . up to 256S or 256D

Analog Input Range (at PGA gain = 1) . . . . . ±10 Volts (± 5V, 0 to 10V, 0 to 5 volts are jumperable)

Input Configuration for on-board multiplexed channels . . . . . High impedance, voltage input, non-isolated

A/D Output Coding . . . . . Bipolar 2's complement binary, bipolar offset binary or unipolar straight binary.

Input Bias Current . . . . . 8 nanoamps

Input Impedance . . . . . Power on: 10 megohms minimum differential or to ground.
Power off: 1.5 kilohms

Common-Mode Input Range . Both inputs must remain within ±10 Volts maximum of analog ground.

Common-Mode Rejection ±10V, 60Hz, 1 kilohm imbalance . . . . 75 dB minimum, gain = 2, 80 dB minimum, gain = 128

External A/D start trigger . . . . TTL compatible, falling edge, 500nS minimum, software gatable

Input Overvoltage for on-board channels . . . . ±35V dc, maximum sustained

Software Programmable Gain Amplifier range (DATEL AM-543). 1, 2, 4, 8, 16, 32, 64 and 128 gain steps

PGA PERFORMANCE

Maximum Settling Time (PGA plus mux) at 10V output step

Gain	Settling Time	Accuracy
1	8 microseconds	±0.02%
16	12 microseconds	±0.05%
64	40 microseconds	±0.10%
128	100 microseconds	±0.20%

SYSTEM PERFORMANCE (MUX+PGA+S/H+A/D):

Following specifications relate to the performance of the multiplexer, PGA, sample and hold, and the A/D converter.

Specification	A/D type			
	12-bit 4 µS	12-bit 20 µS	14-bit 45 µS	16-bit 400 mS
Accuracy, minimum (% of 10V full scale)				
At gain = 1	0.05%	.025%	0.01%	.0063%
At gain = 128	.20%	.20%	.20%	.20%
Linearity Error, maximum	1/2 LSB	1/2 LSB	1/2 LSB	2 LSB
Zero Tempco, maximum ppm of full scale range per degree Celsius	20	20	20	10
Full Scale Tempco, maximum ppm of full scale range per degree Celsius	20	20	20	10
Throughput Period (10V step input)				
At gain = 1	8 µS	20 µS	45 µS	400 mS
At gain = 128	102 µS	110 µS	110 µS	400 mS
A/D Conversion Period,				
Typical	4 µS	20 µS	45 µS	400 mS
Maximum	5 µS	25 µS	54 µS	400 mS

LOCAL MICROCOMPUTER

Microprocessor Z-80A, 3.6864MHz

Maskable interrupt . . . . . connected to MK3801 Serial Interrupt Timer.

Default Priority	Function
I7	End of A/D Scan (EOS)
I6	End of A/D Conversion (EOC)
I5	DMA end of process
I4	Host to 701 new command interrupt
I3	Dual Port RAM Lock
I2	Digital I/O #2
I1	Digital I/O #1
I0	Digital I/O #0

Local Random Access Memory (no MULTIBUS access) . . . . . 8K bytes, with 256 bytes reserved for RDX use

Dual-Port RAM Memory-mapped . . . . . 4K bytes, relocatable in host memory on 4K byte boundaries.

Programmable Read-Only Memory (no MULTIBUS access) . . . Up to 16,384 bytes. Accepts 27128, 2764, 2732, 2716 EPROM's. Supplied with 8K (2764) EPROM for monitor and RDX Executive.

Direct Memory Access . . . . . Allows transfers from:
1. A/D converter to Dual-Port RAM
2. A/D converter to Local RAM
3. Local RAM to Dual-Port RAM

Watchdog Timer . . . . . Approximately 152 mS timeout. Synchronizes local DPR access with Z-80 WAIT states while waiting for the host MULTIBUS LOCK signal to grant DPR access. Continuous host DPR access cannot exceed 152mS. Also recovers from out-of-range memory access and failed interrupt acknowledge.

Command Parse Time . . . . . 1 to 4mS, typical.

MULTIBUS INTERFACE

Specification Conformance . . IEEE-796 MULTIBUS

Type . . . . . Memory-mapped, 4096 bytes

Address Selection (Uses on-board DIP Switches) . . . . . 16 or 20 bits (for models without "/24" designator). 16, 20 or 24 bits (for models with "/24" designator).

Data Transfer . . . . . 8 or 16 bits, bus slave.

ST-701 Interrupt to Host . . . . . 1 line, 8 jumper-selectable sources or by software command.

Host Interrupt to ST-701 . . . . . caused by writing to the DPR Status/Interrupt Byte.

Bidirectional Interrupt Arbitration . . . . . Implemented in RDX to resolve simultaneous interrupt conflicts.

MULTIBUS CONTROL SIGNALS

Transfer Acknowledge (XACK/) . . . . . Jumper-selectable delay, 100 to 800 nanoseconds. Note: XACK/ is derived from the bus CCLK/ used to arbitrate DPR access.

Inhibit (INH1/,INH2/) . . . . . These lines are asserted when the host addresses within the DPR range.

Bus Lock (LOCK/) . . . . . The ST-701 will not access MULTIBUS when the host asserts this line. During ST-701 DPR access, LOCK will cause watch-dog timeout if held more than 152 milliseconds.

BHEN/ . . . . . Controls 8-or 16-bit data transfer.

SERIAL INTERFACE

Uses MK3801 Serial Interrupt Timer Controller

Mode . . . . . Full duplex, asynchronous

Baud rate . . . . . 300 to 9600 baud. Monitor initializes at 9600 baud. Operates above 9600 baud using external clock.

Levels . . . . . RS-232-C (standard), RS-422/423 (optional plug-gable transceivers)

Word Format . . . . . 1 start, 8 data, 1 stop, no parity

Connector . . . . . 26-pin, J1 edgeboard, 0.1" centers

Digital I/O Ports . . . . . 3 bits, TTL levels, programmable as inputs, interrupts or outputs on analog channel extension J3.

Programmable Timer . . . . . 4 internal timers included in MK3801. Each 16-bit counter is user-programmable to interrupt the Z-80A CPU. Timer D is assigned to the serial port baud clock.

PROGRAMMING LEVELS

Monitor Level . . . . . Resident in EPROM for ASCII commands from a serial port

RDX Executive . . . . . Included in EPROM. Accepts ASCII command lines loaded at either the DUAL-PORT RAM or the serial port.

Machine Code Program Load . Local RAM accepts user-programs in Z-80A, or INTEL HEX format, downloaded through the Dual Port RAM.

PHYSICAL-ENVIRONMENTAL

Operating Temperature Range . . . . . 0 to +60 degrees Celsius

Storage Temperature Range . . −25 degrees Celsius to +85 degrees Celsius

Outline Dimensions . . . . . 12.0" W x 6.75" D x 0.5" H

MULTIBUS dimensions . . . . . (305 x 172 x 13mm)

***NOTE:** Simultaneous DPR access attempts by the host and the ST-701 are arbitrated by fast address steering logic. The ST-701 CPU temporarily executes waits for delayed access. For interleaved access, use moderate duty cycle.

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ON-BOARD HARDWARE RESOURCES

1. Analog Input Channels

This section includes local, non-isolated analog channel-switching multiplexers (for 32 single-ended or 16 differential channels), channel address registers, and a software-programmable gain amplifier (PGA). The channel address registers include automatic channel sequencing and address drivers for up to 240 single-ended or 224 differential external multiplexer channels through an expansion bus connector. The differential PGA offers gains from 1 to 128 using a software-loadable gain code register.

2. A/D Converter Module/Signal Conditioning

The A/D converter is a plugable module with a compatible Sample and Hold (S/H) amplifier, settling delay and start convert logic, and buffers. Combined resolutions and speeds are offered from down to 12 binary bits and 4 microseconds (settling and conversion), 14 bits and 45 microseconds, up to 16 bits and 400 microseconds.

3. Local Microcomputer/DMA Controller

Using a 4 MHz Z-80A CPU, the ST-701's on-board microcomputer includes up to 16K of ROM and 8K of RAM. The ROM contents, as shipped, include the RDX command processor and the hex monitor. This ROM is mounted on a 24-pin socket. The user can replace this ROM with one of a higher memory density, copying the software supplied onto the new device. This allows the user to further customize the microcomputer.

The local microcomputer also consists of a 4k dual-port RAM host interface, a local DMA controller, an interrupt generator, serial port, and programmable timers.

The local DMA provides high speed, non-host memory-mapped transfers between the A/D section, local memory and the dual-port memory. The local microcomputer also has three general purpose TTL digital lines available on the expansion connector. These bits are programmable as interrupts, enables, inputs, or outputs.

4. Communications Interfaces

Communications with the ST-701 CPU is through two channels: an asynchronous serial port and a high speed, 4 kilobyte dual-port RAM MULTIBUS host interface.

Serial communications

The serial port uses a separate edgeboard connector and supports conventional EIA RS-232-C communications. A programmable timer from the CPU is assigned as a baud rate generator, offering speeds up to 9600 baud. An external clock may be used to go beyond 9600 baud. Optional circuits on the ST-701 offer differential multidropped RS-422 levels. The serial port has access to the hex monitor and the RDX executive.

After application development, the serial port may be re-assigned to any application under user program control, such as printer or magnetic tape output or a LAN interface. It is even possible to fully control the ST-701 only through the serial port, without installation into a MULTIBUS card cage.

MULTIBUS Communications

Primary control and data interface to the ST-701 is through the dual-port RAM (DPR). The DPR overlays host read/write memory and maps memory addresses in the DPR range from the host into the ST-701 using fully standard MULTIBUS arbitration. The DPR is relocatable within 24-bit memory space on 4K boundaries.

ST-701 transfer logic allows passing 8- or 16-bit data words. ASCII command strings are written by the host into the DPR, and pre-formatted A/D scans are read from the DPR from two user-definable DPR buffers. Asynchronous control and status is managed by bidirectional interrupts through a reserved area at the top of DPR.

When A/D data is ready, the host is notified by a maskable interrupt. The user's interrupt service routine then transfers A/D data blocks to mass storage or processes the information. All transfers of A/D data blocks from local RAM to shared DPR are fully arbitrated on MULTIBUS using bidirectional lock and transfer acknowledge signals. No I/O addresses are used.

For extended commands (either user-written or developed by DATEL), the DPR also accepts downloads of executable Z-80 code blocks and corresponding uploads. The RDX firmware allows for user-defined commands. Thus the ST-701 may function as a general purpose data acquisition computer which may be dynamically reprogrammed on the fly (for example, from downloaded disk code blocks for different functions).

5. On-board Power Converter

A modular dc-to-dc power converter supplies low-noise ±15 volt dc power to analog circuits. The dc-to-dc converter generates this from the host +5V dc input, also distributed to the remaining ST-701 circuits.

SOFTWARE OVERVIEW

Controlling the ST-701 requires using programs resident upon the ST-701 and within the host. Those on the ST-701 consist of PROM-resident routines, user-loaded command strings, and optional transient RAM-executable code. Programs in the host are written by the user in any language to control the ST-701 and retrieve A/D data blocks. For highest speed, host programs must be linked to the host interrupt processing scheme. This requires response to the MULTIBUS interrupt signal selected for the ST-701 using a pre-stored vector address in the host interrupt service address table.

If this is not possible, the ST-701 may be operated by polling its control byte in the top of DPR, but at lower overall host performance because of polling overhead. The ST-701 does not assert a vector address on MULTIBUS when it generates an interrupt. Therefore a host interrupt controller is required to respond to the interrupt. If a single interrupt line must be shared with other devices, some form of fast polling may be required to determine whether the ST-701 caused the interrupt.

Real-Time Data Acquisition Executive (RDX)

The ST-701 PROM operates at two levels: a low level Monitor and a command line Executive (RDX). The RDX may be accessed from either the serial port or the DPR whereas the Monitor uses only the serial port. The hexadecimal Monitor accesses local memory, the DPR, I/O channels and the local Z-80 registers. The Monitor functions as a user-accessable area of memory for debugging routines, command strings, etc. The ST-701 can be switched between the two levels by both a local ST-701 terminal and the MULTIBUS host console.

The Executive mode contains a command line interpreter to load ST-701 operation modes from an ASCII command structure. The user builds a command line (either manually or from a host program), loads this into the ST-701, then requests execution. The command line does not have to be reloaded to repeat an operation. Thus, sequential A/D blocks may be collected at high speed.

To assure compatibility with development systems, RDX powers up in the OFF state, ready for a wake-up command. This leaves the DPR unaffected by host memory testing. RDX may be commanded ON or OFF at any time.

ST-701 COMMAND FAMILIES

ST-701 Monitor Level Commands

Monitor commands let the user develop ST-701 programs or extended commands. The user may display blocks of local memory (including the DPR), examine/modify memory locations or CPU registers, and JUMP to start execution at any memory address. An optional breakpoint may be used for debugging. Commands written to the RDX and the Monitor are in ASCII and hexidecimal formats. From the serial port, the user may easily switch between the Monitor and the Executive.

Monitor Commands

Monitor commands allow the examination and modification of ST-701 registers and RAM memory. The contents of the examined registers and/or memory locations remain unchanged if no new data is entered prior to a Carriage Return. A description of the available Monitor Level commands follows.

ST-701 EXECUTIVE ON (CR) — Enters the ON mode. Processes all Executive Level commands sent through the serial port or dual-port RAM command area.

ST-701 EXECUTIVE OFF (CR) — Enters the OFF mode. Processes all Monitor Level commands sent through the serial port except the G... command.

S adrs (CR) — Examines/modifies ST-701 memory and ST-701 Memory Mapped hardware registers (CR) increments the address and "." (CR) terminates the command.

Where:

adrs - Memory address in Hex.

^ C (control C) — Returns to the MONITOR mode if operating at the Executive Level. Processes all Monitor Level commands entered through the serial port including the G... command. "G (CR)" will return the ST-701 to the prior EXECUTIVE state.

X reg (CR) — Examines/modifies the given Z-80 CPU register. The register designations are as follows:

Z-80 REGISTER	reg
Accumulator	A or a
BC pair	B or b
DE pair	D or d
HL pair	H or h
X index	X or x
Y index	Y or y
Stack pointer	S or s
PC	P or p
Flags	F or f

To access the second bank of Z-80 registers append the register mnemonic with an apostrophe. (eg., X B')

D str adrs [,end adrs] (CR) — Displays the ST-701 memory starting at the given address.

Where:

str adrs - Start memory address (HEX)
end adrs - End memory address (HEX)

G [adrs, break adrs] (CR) — Begins executing at the given address. A single breakpoint can be included if executing out of ST-701 RAM.

Where:

adrs - Optional starting address.
break adrs - Optional breakpoint address.

Note: This command is disabled while ST-701 is in the OFF mode.

ST-701 Executive Level Commands

The ASCII commands supported at the RDX level can be categorized into three types:

1. General purpose commands
2. MULTIBUS Host/ST-701 interface control commands
3. A/D control commands

The Executive Level ASCII commands are supported either through the serial port or the dual-port RAM (DPR) window. Command strings entered throught the dual-port RAM are to be loaded eight (8) bytes down from the top of DPR in descending order. Once the command has been loaded, a "01" HEX write to the top byte of DPR causes the Executive to process the command.

General Purpose Commands

The RDX Executive (accessible from either the DPR or the serial port) manages the command registers, A/D channel address registers and the PGA gain register. The user may load and read the command, channel, status, and gain registers or download ASCII hex programs via the DPR. The commands also allow jumping to an address, releasing ST-701 control to an executing program in local memory.

CE (CR) — Disables echoing to the serial port of ST-701 command received via the dual-port RAM.

CE 1 (CR) — Echos the ST-701 command received via the dual-port RAM out through the serial port.

WC xx (CR) — Loads the ST-701 COMMAND REGISTER.

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Where:

xx - byte value in HEX

RC (CR) — Reads the ST-701 COMMAND REGISTER.

RS (CR) — Reads the ST-701 STATUS REGISTER.

WR ss[,ff] (CR) — Loads the ST-701 START CHANNEL REGISTER and optionally loads the FINAL CHANNEL REGISTER.

Where:

ss - START CHANNEL byte address in HEX.
ff - FINAL CHANNEL byte address in HEX.

RR (CR) — Reads the ST-701 START and FINAL CHANNEL REGISTERS.

WG xx (CR) — Loads the ST-701 GAIN REGISTER.

Where:

xx - HEX value between 0 (GAIN = 1) and 7 (GAIN = 128).

RG (CR) — Reads the ST-701 GAIN REGISTER.

MULTIBUS Host/ST-701 Interface Control Commands

The RDX manages the DPR interface by controlling dual transfer buffers. Using these commands, the user may define the actual dual-buffer configuration, control the origin of the command acknowledge interrupt, or disable DPR data transfers.

Interface Commands

CA (CR) — Resets bit 0 of the dual-port RAM interrupt/status byte for status-driven command acknowledge.

CA 1 (CR) — Resets bit 0 of the dual-port RAM interrupt/status byte then sets it for interrupt-driven command acknowledge.

DB adr 1, len 1 [,adr2, len2] (CR) — Defines the given dual-port RAM transfer buffer(s).

Where:

adr1 - address in HEX of DPR BUF 1.
len1 - length in HEX of DPR BUF 1.
adr2 - address in HEX of DPR BUF 2.
len2 - length in HEX of DPR BUF 2.

Example: DB F000, 100, FA00, 100 (CR)

Note: adr1 and 2 are relative to the ST-701 internal memory.

DS 1 (CR) — Makes BUF 1 the current Active Buffer. (DEFAULT)

DS 2 (CR) — Makes BUF 2 the current Active Buffer.

DD (CR) — Disables dual-port RAM data transfers until a new "DB" command is received.

TR M (CR) — Starts multiple conversions on external trigger if a single channel A/D command is sent or starts multiple channel scans if a sequential or random channel scan A/D command is sent.

TR (CR) — Disables external trigger.

G adrs (CR) — Begins executing at the given address. Releases full ST-701 Control to the executing program.

Where:

adrs - Program starting address in HEX.

LD B (CR) — Loads a program into LOCAL RAM or an EXTENDED ST-701 command. The Program or EXTENDED command must be in INTEL HEX format and is loaded via the dual-port RAM.

Xnewcmd (CR) — Processes the EXTENDED ST-701 COMMAND previously loaded using the "LD B" command.

Where:

X - The required prefix for all EXTENDED COMMANDS.

newcmd - The user defined mnemonic for the given EXTENDED COMMAND.

A/D Control Commands

Using the RDX dual buffers, the A/D commands are extensively structured to allow selection of different analog input channel scan modes. Types of scan modes include single channel, sequential multi-channel and random multi-channel addressing. The start and end addresses imbedded within a scan command could come from a previously-downloaded address table.

The structured syntax of the A/D command lines allows start/final addresses and number of scan repeats to be specified in the command. The command also may specify output routing of the A/D (to either DPR, local RAM and/or serial port) as well as trigger starts from external input or A/D reads. Several automatically repeating modes are possible and groups of commands may be strung together on the same command line as long as the A/D commands come last.

The A/D converter may operate in a free-run overlay mode where the host continually reads scan blocks. This mode precludes entering further command lines. A second mode allows the A/D to interrupt the host whenever the buffer is full to smoothly synchronize DMA transfers to the host.

All data transfers are fully arbitrated with the MULTIBUS host and may occur simultaneously with host memory activity in non-DPR space. Refer to Figure 2.

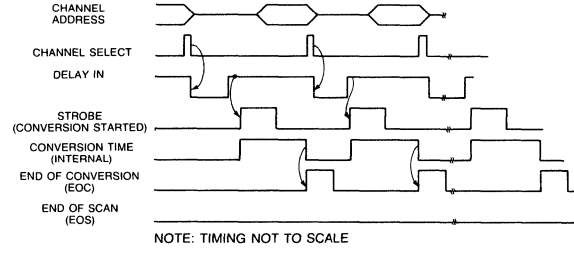


Figure 2: ST-701 and Host Processing Sequences

11

A/D Commands

AK [chan], mode (CR) — Performs single channel A/D conversions according to the data acquisition mode selected. No channel increment is performed.

Where:

chan - channel address number in HEX.
mode: S - Single conversion only.
C - Continuous conversions.
F - Continuous conversions until DPR buffer is full.
N, XXXX- "XXXX" number of conversions in HEX.

HL (CR) — Stops processing the current A/D command and returns control to ST-701 Executive level.

AS [str chan, fin chan], mode (CR) — Performs sequential channel scanning according to the data acquisition mode selected.

Where:

str chan - Start channel in HEX.
fin chan - Final channel address in HEX.
mode: S - Single sequential scan.
C - Continuous sequential scan.
F - Continuous requential scan until DPR buffer is full.
N,XXXX - "XXXX" number of channel scans in HEX.

LC x, nn, adr1, adr2, adr3. . . adrn (CR) — Loads random channel addresses into Channel Address Table.

Where:

x - "I" to initialize new table.
"A" to append to table
nn - HEX number of addresses to input
adr1. . . n - Channel Addresses (HEX) to load into Channel Address Table

AR mode (CR) — Performs random channel scanning according to the data acquisition mode selected.

mode: S - Single random channel scan.
C - Continuous random channel scans.
F - Continuous random channel scans until DPR buffer is full.
N,XXXX - "XXXX" number of random scans in HEX.

LC (CR) — Deletes the contents of the current Random Channel Address Table.

TR S (CR) — Starts single conversions on External Trigger if a single channel A/D command is sent or start single channel scan if a sequential or random channel scan A/D command is sent.

LEVELS OF USER PROGRAMMING

Users may program the ST-701's microcomputer at three possible levels: command line, code download and EPROM reprogramming. The highest level uses only the ASCII command line Executive. Most applications will use only this mode since it is simple and requires no programming (except the host interrupt routines).

The second mode requires user Z-80 programming and should be considered for special functions (unique data structures, arithmetic, etc.) Using the X command, users may define their own extended ASCII commands which call executable code developed by the user (or DATEL) and downloaded from mass storage for execution in local RAM. Such user programming would call routines documented in EPROM.

The third possible user programming level would be a reprogram of the EPROM to avoid downloads and permanently store custom data processing and/or extended commands.

DUAL-PORTED READ/WRITE MEMORY (DPR)

The ST-701's 4096-byte read/write dual-port RAM (DPR) is shared with the MULTIBUS host computer. The DPR's fixed base address is selected by ST-701 address decoder switches. The DPR is accessed through a high speed arbitration circuit which resolves simultaneous access conflicts between the ST-701 and its host.

The four major uses for the DPR are control/status, ASCII command line loading, A/D data block transfer, and optional upload/download of Z-80 code or data. The control/status functions (including interrupt flags and interrupt arbitration semaphore) occupy a few bytes at the top of DPR. Command lines (terminated by a carriage return) load downward from this top area after being granted access by the semaphore. The host system sets a control bit in the DPR status/interrupt byte location, causing a local ST-701 interrupt to parse the command line.

As each command is accepted for execution, the command line is internally stored in non-MULTIBUS RAM and the host is optionally interrupted to signal successful command start. A/D data blocks are transferred out to the host through two user-defined buffers within the DPR space. Preloaded length and offset pointers near the top of the DPR manage these two buffers using high level ST-701 data transfer commands. Large data blocks overlay previous data blocks and/or command lines. This is particularly true for some long command lines which have tables or code/data blocks.

Command Listing

ST-701 ASCII command strings sent to the DPR reflect the simplicity of the structured high-level commands. Both buffer switching and scan starts may be combined on the same line separated by an exclamation point. This is similar to combining BASIC statements on one line separated by colons. All the initialization commands (after turning on the RDX EXEC) could be combined on the same command line.

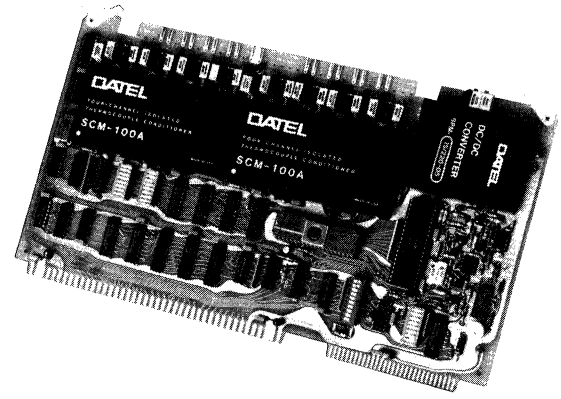
Example: CA1!CE!WR0,1F!DB0,FF,100,FF <cr>.

As a general purpose microcomputer dedicated to A/D data acquisition, many simple functions are easily programmed. Access to the local Z-80 microcomputer is fully documented in the ST-701 User Manual.

ST-702 MULTIBUS HIGH-ISOLATION THERMOCOUPLE BOARD

FEATURES:

- **8-Channel MULTIBUS board for temperature measurements**
- **Supports J, K, T, S, B, E, and R type thermocouples**
- **High-level voltage and 4-to-20 mA input capability**
- **On-board CPU for temperature calculation**
- **Up to 1,000V peak input isolation**
- **13-Bit resolution**
- **True electronic cold junction compensation**
- **Output in degrees Celsius or Fahrenheit**
- **128 dB CMRR**
- **55 dB NMR**
- **Screw terminal signal connections**



DATEL's SINETRAC ST-702 is an intelligent MULTIBUS board designed specifically for temperature measurements from J, K, T, S, B, E, and R thermocouples. The 8-channel A/D board filters, amplifies the input signal and provides linearized digital data to a MULTIBUS host system in °C or °F. The board performs as an ideal front-end to programmable controllers and similar systems.

GENERAL DESCRIPTION

The ST-702 is an intelligent MULTIBUS analog input board primarily suited for thermocouple measurements. Features include isolation, 60 Hz line rejection, and screw terminals for input signals. The physical, functional, and electrical attributes of the ST-702 meet and exceed standards demanded by the process control industry.

Low-level isolated analog signals from up to eight thermocouples are filtered, amplified, and converted to digital data using a 12-bit- and sign-integrating A/D converter. The on-board microprocessor linearizes the digital data and outputs a binary quantity directly to the MULTIBUS host computer in degrees Celsius or Farenheit. The ST-702 board also provides electronic cold junction compensation for the thermocouple inputs. The on-board resources relieve the host system of tasks relating to thermocouple linearization.

The ST-702 measures temperature from J, K, S, T, E, R, and B type thermocouples. The analog inputs are galvanically isolated from the MULTIBUS, providing a minimum of 750 Volts RMS common mode isolation. The board's 128 dB Common Mode Rejection Ratio (CMRR) allows thermocouple measurements even in the presence of high common mode voltages. The high isolation protects the host computer from high voltage damages if a thermocouple accidentally contacts a high voltage line. The on-board status register indicates error status information which includes open thermocouple inputs, and over and under range conditions for the thermocouple inputs.

ORDERING INFORMATION

ST-702 — Input Type

INPUT TYPE		INPUT RANGES
A	Thermocouple Isolated Types J, K, S, T, E, R, B	J −200 to + 760 °C
		K −200 to +1,232 °C
		T −200 to + 400 °C
		S 0 to +1,768 °C
		E −270 to +1,000 °C
		R 0 to +1,768 °C
		B +300 to +1,820 °C
		±25.6 mV
		±51.2 mV
		±102.4 mV
B	High Level Inputs Isolated	±2.500 V
		±5.000 V
	Current Loops	0-20 mA
		4-20 mA
		0-50 mA
		10-50 mA

Part No. 60-2105600 Detachable screw terminal analog input connector (formerly No. 60-12474-1).

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

The ST-702 also measures low level ±51.2 mV or ±102.4 mV full-scale range analog signals from sources other than thermocouples, and provides the raw, unlinearized A/D data to the host CPU. The ST-702 offers gain settings of 1 and 2 when used with low-level voltage inputs.

Applications with high-level signal inputs may use model ST-702B. This model provides ±5V, ±2.5V and current loop signal input capability. High voltage isolation, 1,000V peak, offered by the ST-702 makes it ideal for most industrial applications.

Functionally, temperature is determined by measuring the potential difference between the measurement (hot) junction and the reference (cold) junction of the thermocouple leads. The on-board electronic cold junction compensation logic eliminates errors caused by temperature variations of the cold junction. The CJC is effective over a range of 0 to +60 degrees Celsius.

The ST-702 hardware consists of five sections: MULTIBUS interface section, microprocessor control section, A/D converter section, input signal conditioning section, and CJC section. Figure 1 shows the functional block diagram of the board identifying these sections.

The ST-702 operates from a MULTIBUS host with up to 24-bit addressing capability. The board also supports 8- or 16-bit data transfers, allowing use with 8- or 16-bit MULTIBUS systems. The ST-702 maps onto four consecutive locations in the host system's memory space. Optionally, the board is configurable in the host system's I/O address space using jumper selections. The ST-702's MULTIBUS interface signal includes an XACK/ signal that allows delays from 100 to 800 nanoseconds.

The ST-702 is fully bus and card cage compatible with the MULTIBUS. The board is 12.0 inches wide x 6.75 inches deep x 0.5 inches high (305 x 172 x 13 mm). Multiple ST-702's fit into adjacent card slots of a standard .60 inch spacing card cage. The ST-702 uses power from the MULTIBUS +5V line. The on-board dc-to-dc converter provides ±15V to drive the board's analog circuitry. Total current drawn from the MULTIBUS +5V line is 1.6 A, typical.

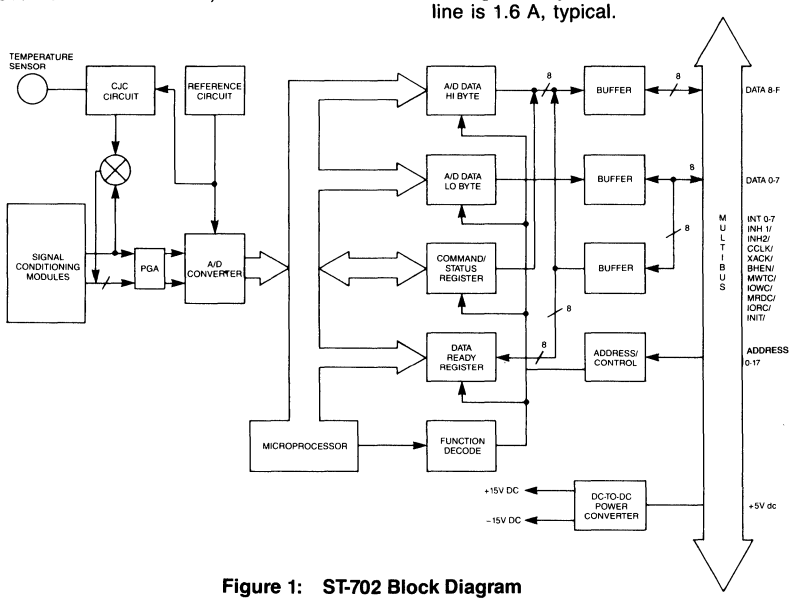


Figure 1: ST-702 Block Diagram

FUNCTIONAL SPECIFICATIONS

All specifications typical at +25 degrees Celsius unless otherwise noted.

Electrical Characteristics

Analog Inputs 8

Input Impedance ..... 100 Megohms

Input Bias Current, maximum ..... 8 nanoamps

Common Mode Voltage Range, Channel to Channel and Channel to MULTIBUS ground AC, 50 or 60 Hz ..... 750V RMS

AC or dc Isolation, peak maximum ..... ±1,000V

Common Mode Rejection Ratio, minimum, Rs = 1k f = 0.01 to 100 Hz

ST-702A ..... 128 dB

ST-702B ..... 110 dB

Maximum Safe Differential Voltage without Damage ..... 130V RMS

Normal Mode Rejection at 50 or 60 Hz minimum ... 55 dB

Input Lead Resistance Effects ..... none

Input Voltage Ranges ..... ±25.6m V
(combined range jumpers and software PGA) ±51.2m V
±102.4m V :702A
±2.5, ±5V dc :702B

Voltage Range Accuracy, maximum

ST-702A ..... 0.03% FSR

ST-702B ..... 0.1% FSR

Voltage Range Gain Drift, maximum ..... 45 ppm/°C

Voltage Range Input Offset Drift

Input Range	Offset Drift (RT I)
±25 mV	3μV/°C
±50 mV	3μV/°C
±100 mV	3.5μV/°C
±2.5 V	55μV/°C
±5 V	55μV/°C

Address bus ..... 16, 20 or 24 bits

Data transfer ..... 8 or 16 bits
using BHEN/, memory mapped (standard) or I/O mapped (jumperable)

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

Power Supply Requirements
With internal dc-to-dc Converter . . . . . +5V dc ±0.5% @1.6 A
No dc-to-dc Converter . . . . . +5V dc ±0.5% @1.0 A
+15V dc ±0.5% @.15 A
−15V dc ±0.5% @.075 A
Interrupt to MULTIBUS . . . . . 1 line
jumperable INT0/ to INT7/

THERMOCOUPLE INPUT RANGES

Thermocouple Type	Temperature Range (degrees C)	Input Voltage Range (mV)
J	−200 to 760	−7.890 to +42.922
K	−200 to 1232	−5.891 to +49.988
S	0 to 1768	0.000 to +18.698
T	−200 to 400	−5.603 to +20.869
E	−270 to 1000	−9.835 to +76.358
R	0 to 1768	0.000 to +21.108
B	300 to 1820	+0.431 to +13.814

THERMOCOUPLE TEMPERATURE ACCURACY
(Maximum) with board at +25°C

Thermocouple Type	Temperature Range (degrees C)	Input Voltage Range (mV)	Accuracy (degrees C)
J	−200 to −100	−7.890 to −4.632	±3
	−100 to +760	−4.632 to +42.922	±1
K	−200 to −100	−5.891 to −3.553	±3
	−100 to +1,232	−3.553 to +49.988	±1
S	0 to +300	0.0000 to +2.323	±6
	+300 to +1,768	+2.323 to +18.698	±3
T	−200 to 0	−5.603 to 0.000	±3
	0 to +400	0.000 to +20.869	±1
E	−270 to −200	−9.835 to −8.824	±10
	−200 to 0	−8.824 to 0.000	±3
	0 to +1,000	0.000 to +76.358	±1
R	0 to +300	0.000 to +2.400	±4
	+300 to +1,768	+2.400 to +21.108	±2
B	+300 to +500	+0.431 to +1.241	±5
	+500 to +1,000	+1.241 to +4.833	±3
	+1,000 to +1,820	+4.833 to +13.814	±2

TIME AND TEMPERATURE RELATED DRIFT

Thermocouple Type	Time related drift (degrees C/6 months)	Temperature related drift (degrees C/degree C)
J	±0.2	±0.1
K	±0.25	±0.15
S	±1.0	±0.3
T	±0.25	±0.1
E	±0.2	±0.15
R	±0.8	±0.3
B	±1.0	±0.3

PHYSICAL/ENVIRONMENTAL

Outline Dimensions . . . . . 12.0 inches wide x 6.75 inches deep x 0.5 inch high (305 x 172 x 13 mm)
Weight . . . . . 1 pound 2 ounces
Operating Temperature Range . . . . 0 to 60 degrees Celsius
Storage Temperature Range . . . . . −20 to +80 degrees Celsius
Relative Humidity noncondensing . . . . . 0 to 80%
Altitude . . . . . 0 to 15,000 feet (4,500 meters)

ST-702 PROGRAMMING INFORMATION

Programming the ST-702 essentially consists of using four registers. The registers are the Data Ready register, Command register, Status register and the A/D data register. These registers appear as four consecutive locations in the CPU's address space. Table 1 lists the functions of these registers.

Table 1: ST-702 Register Assignments

Address	Function	Register Name	Description
BASE + 0	READ	Data Ready	Read Data Ready status
BASE + 1	WRITE	Command	Write Analog Data command
BASE + 1	READ	Status	Read Analog Data status
BASE + 2	WRITE	—	—
BASE + 2	READ	A/D Data (low)	Read Analog Data, low byte
BASE + 3	WRITE	—	—
BASE + 3	READ	A/D Data (high)	Read Analog Data, high byte

Data Ready Register

The host CPU reads this register to determine if valid data and status information is available in the A/D Data and Status registers. The Data Ready register indicates to the host system if the Command register is ready to receive a new command. Bit 0 is set to 1 when a command is written to the register, then resets to a zero as soon as the command is accepted. Figure 2 shows the format of the data ready register.

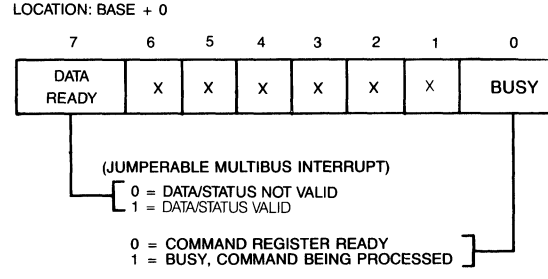


Figure 2: ST-702 Data Ready Register

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Command Register

The Command register allows the ST-702 to operate in random mode or sequential mode. Programming the Command register selects the output data coding, PGA gain code, and calibration. The Data Ready register monitors successful completion of the command. Figure 3 shows the Command register format.

LOCATION: BASE + 1

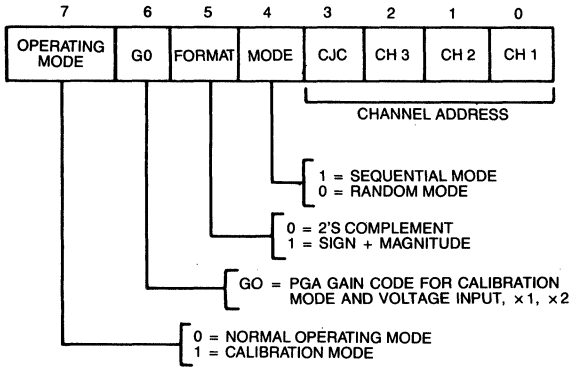


Figure 3: ST-702 Command Register Format

Status Register

The contents of the status register indicate error conditions, channel selected, and the unit for temperature measurement. Figure 4 shows the status register format. The status register determines validity of data in the A/D data register. Bits 4 through 7 of this register indicate open inputs, CJC and data out of range status, and possible ST-702 hardware failures. If the ST-702 fails the self-test at power-up, the status bits indicate RAM or ROM failure and turn the BOARD OK lamp off. If the calibration switch is turned on during normal operation, the status bits indicate this condition. Table 2 lists the error status indications.

LOCATION: BASE + 1

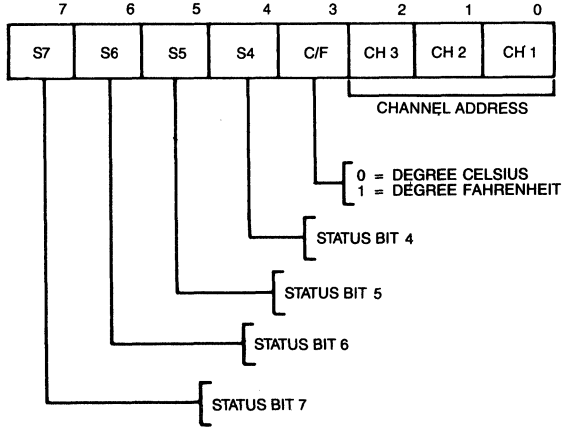


Figure 4: Status Register Format

Table 2: Error Status Conditions

Error Number S7	S6	S5	S4	Error
0	0	0	0	No error
1	0	0	0	Calibration mode
1	0	0	1	Data out of range
1	0	1	0	Open wire detection
1	0	1	1	Board not ready
1	1	0	0	CJC out of range
1	1	0	1	CJC and data out of range
1	1	1	0	CJC or open wire
1	1	1	1	Memory or board failure

A/D Data Register

The A/D data register contains either the raw reading from the A/D converter or the linearized data from a thermocouple, depending on the operating mode. Data is either a 12-bit 2's complement or a sign plus 12-bit number. MSB or sign bit appear in the four MSB positions for ease of sign detection. The data is in a binary format. Figures 5a and 5b show register formats for the A/D data registers.

LOCATION: BASE + 3

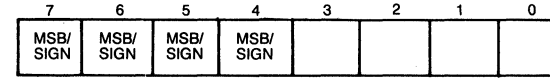


Figure 5a: A/D Data Register Format (High Byte)

LOCATION: BASE + 2

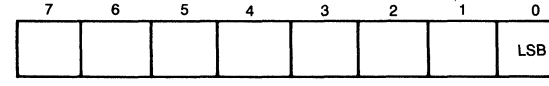
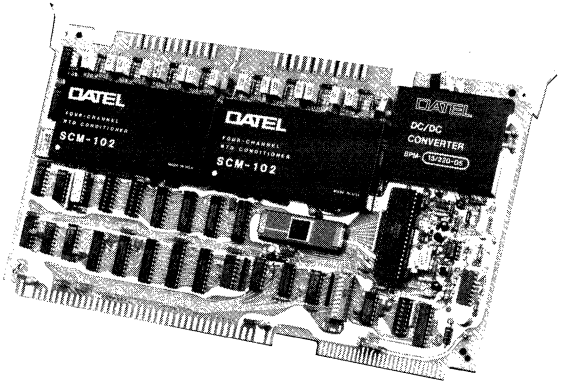


Figure 5b: A/D Data Register Format (Low Byte)

ST-702R
8-CHANNEL MULTIBUS RTD A/D BOARD



FEATURES

- **8-Channel MULTIBUS* board for RTD temperature measurements**
- **Internal 0.4 mA current excitation**
- **Supports 100 ohm RTD's**
- **Output in degrees Celcius or Fahrenheit**
- **12-bit plus sign resolution**
- **On-board CPU for temperature calculation/linearization**
- **4 switch selectable sample rates to 30s/sec**
- **Screw terminal signal connections**

DATEL'S SINETRAC ST-702R IS AN INTELLIGENT MULTIBUS BOARD DESIGNED SPECIFICALLY FOR TEMPERATURE MEASUREMENTS FROM 100 OHM RTD'S. THE 8-CHANNEL A/D BOARD FILTERS, AMPLIFIES THE INPUT SIGNAL AND PROVIDES LINEARIZED DIGITAL DATA TO A MULTIBUS HOST SYSTEM IN °C OR °F. THE BOARD PERFORMS AS AN IDEAL FRONT-END TO PROGRAMMABLE CONTROLLERS AND SIMILAR SYSTEMS.

GENERAL DESCRIPTION

The ST-702R is an intelligent analog I/O board for MULTIBUS based computers that is primarily suited for RTD measurements. Low level analog signals from an RTD are filtered, amplified and converted to digital data using a 12-bit plus sign integrating A/D converter. The on-board microprocessor linearizes this data and outputs a binary quantity to the MULTIBUS host computer directly in degrees Celsius or Fahrenheit, thus relieving the host CPU of the time-consuming task of RTD linearization.

The ST-702R is fully compatible with all MULTIBUS computers and supports systems with up to 24 bit addressing capability. The board also supports 8 or 16 bit data transfers, allowing use with 8 or 16 bit MULTIBUS CPU boards. The ST-702R is shipped as a memory mapped peripheral occupying 4 consecutive locations in the CPU address space. Alternatively, it can be configured to appear in the I/O address space of the CPU through jumper option.

In order to make the ST-702R compatible with different speed CPU and memory systems, a Transfer Acknowledge Delay circuit (XACK/DELAY) is provided. Eight delays from 100 to 800 nsec are jumper selectable by the user.

The ST-702R is fully bus and card cage compatible with the MULTIBUS. The board is 12.0″W x 6.75″D x 0.5″H (305 x 172 x 13 mm). Multiple ST-702R boards may be mounted in adjacent card slots when used with a standard .60″ spacing card cage.

The ST-702R draws all of its power from the MULTIBUS + 5V line. An on-board DC to DC Converter provides the ± 15V to drive the board's analog circuitry. Total current drawn from the MULTIBUS + 5V is 1.6A typical.

The ST-702R hardware consists of four main sections; MULTIBUS interface, microprocessor, A/D converter and signal conditioning (with excitation) sections. Refer to the block diagram in figure 1 for the general layout of the ST-702R board.

ST-702R PROGRAMMING INFORMATION

Programming the ST-702R essentially consists of using four registers. The registers are the Data Ready register, Command register, Status register and the A/D data register. These registers appear as four consecutive locations in the CPU's address space. Table 1 lists the functions of these registers.

Table 1: ST-702R REGISTER ASSIGNMENTS

ADDRESS	FUNCTION	REGISTER NAME	DESCRIPTION
BASE + 0	READ	ADRDY	Read Data Ready Status
BASE + 1	WRITE	ADCMD	Write Analog Data Command
BASE + 1	READ	ADSTAT	Read Analog Data Status
BASE + 2	WRITE	—	
BASE + 2	READ	ADLOW	Read Analog Data Low Byte
BASE + 3	WRITE	—	
BASE + 3	READ	ADHIGH	Read Analog Data High Byte

ORDERING INFORMATION

ST-702R	RTD A/D Board
60-2105600 (formerly 60-12474-1)	Detachable Screw Terminal Connector (not included with board).

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FUNCTIONAL SPECIFICATIONS

A/D Conversion Rate Selection

The ST-702R provides for a choice of four A/D Conversion rates: 15 or 30 conversions per second for 60 Hz environments, and 12.5 or 25 conversions per second for 50 Hz. Since an integrating A/D converter is used on the ST-702R, it is desirable to operate it as a multiple of the AC line frequency in order to obtain normal mode rejection of any AC signals on the analog inputs. The board is shipped standard configured for 15 conversions per second. Use of the faster (30/25) conversion rate will result in decreased normal mode rejection (NMR). A/D Conversion Rate Selection is accomplished by switches S3-2 and S3-3 on the best ST-702 board. Switch settings are described below.

CONV/SEC	S3-2	S3-3	FREQ
12.5	OFF	OFF	50HZ
15	OFF	ON	60HZ
25	ON	OFF	50HZ
30	ON	ON	60HZ

A/D Conversion Rate Selection

PERFORMANCE — ANALOG INPUT

SPECIFICATION	MINIMUM	MAXIMUM
Input Offset Volt Adj. to zero		± 150μV
Channel to channel		± 25μV
Input Bias Current		10na
Over Volt Protect		130 VRMS
Input Impedance [Differential to ground]	100 megohms	
Input Noise volt. 0.01 Hz to 100Hz		1.5μV p-p
Input Span Range	18.49 ohms	400 ohms
Normal Mode Rejection 50/60 Hz	24 DB	
Temperature Drift		± 1μV/deg.C
Gain Drift		25 ppm/deg.C
Offset Drift		0.03 deg/deg
System Accuracy		
European Alpha = .0385		
−200 to 0°C		±3 deg.C
0 to 850°C		±1 deg.C
American Alpha = .0392		
−200 to 0°C		±3 deg.C
0 to 630°C		±1 deg.C

ANALOG INPUT SPECIFICATIONS

General

Number of Channels	8	
Isolation	None	
Input Configuration	3 Wire	
Input Type	RTD	
RTD Input Type		
	Range	Equivalent Ohms
European curve Alpha = .00385	−200 to 850 deg C	[18.49 − 390.265 ohms]
American curve Alpha = .00392	−200 to 630 deg C	[17.14 − 327.02 ohms]
Input Lead Resistance Effect	None	
Internal Current Excitation	0.4mA	
Digital Output	deg C or deg F	[Selected by Switch]
Digital Output Coding	2's Complement or Sign and Magnitude	[Selected by ADCMD 2'Comp. for Voltage Range]
Resolution	12 Bit Plus Sign and Over Range	
Switch Selectable Sample Rates	12.5/Sec	(50 Hz)*
	15/Sec	(60 Hz)*
	25/Sec	(50 Hz)*
	30/Sec	(60 Hz)*

* Frequency Environments

POWER SUPPLY REQUIREMENTS

With DC/DC Converter Installed for ± 15 Volts	+5V dc ± 0.5% @ 1.6A	(2.5A max)
No DC/DC Converter	+5V dc ± 0.5% @ 1.0A	(1.5A max)
	+15V dc ± 0.5% @ .15A	(.2A max)
	−15V dc ± 0.5% @ .075A	(.1A max)

CONNECTOR SPECIFICATIONS

MULTIBUS	— P1	86 (dual 43) pin card edge connector	[.156 inch center]
	— P2	60 (dual 30) pin card edge connector	[.100 inch center]
Analog Input	— J1	36 (dual 18) pin card edge connector	[.200 inch center] Mating connector Buchanan-PCB3A36A Datel Ref. 60-12474-1

PHYSICAL — ENVIRONMENTAL

Outline Dimensions	12.0"W x 6.75"D x 0.5"H (305 x 172 x 13 mm)
Weight	1 lb. 2 oz.
Operating Temperature Range	0 to 60 Degree C
Storage Temperature Range	− 20 to + 80 Degree C
Relative Humidity noncondensing	0 to 80%
Altitude	0 to 15000 feet (4500 meters)

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Data Ready Register

The host CPU reads this register to determine if valid data and status information is available in the A/D data and status registers. Bit 0 indicates whether the on-board microprocessor has read the previous command that was written to the Command Register by the MULTIBUS. Data Ready is cleared upon power-up and is set by the Microprocessor when Data/Status is loaded. Data Ready is cleared when MULTIBUS writes a command or reads A/D data. Command Ready is cleared on power-up and is set when a command is written. Command Ready is cleared when the Microprocessor reads a command. Figure 2 shows the format of the data ready register.

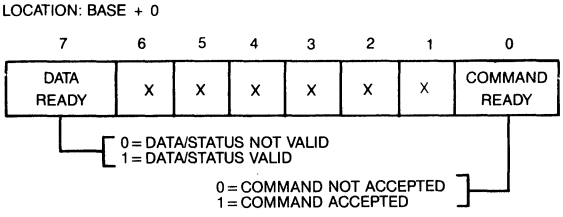

Figure 2: ST-702R Data Ready Register (BASE +0)

Command Register

The ST-702R may be easily programmed to operate in two basic modes of operation: Random Mode or Sequential. It may also be programmed to output data in several different formats to the host computer. In Random Mode, the host computer simply writes a command word to the ST-702R Command Register as depicted in Figure 3. The Data Ready Register may then be monitored to determine when data and status information is ready.

Bits 0-2 are used to map which channel the ST-702R is to convert and subsequently place the data in the A/D Data register. In Random Mode, the ST-702R will transmit the analog data for the channel number in Bits 0-2. Data from the next consecutive channel will be loaded into the A/D Data register when the previous data is read by the host CPU.

Bit 4 is used to select either random or sequential scanning operation and must be set to '0' for random mode operation. In Random Mode, the data from the analog channel in Bits 0-2 will be loaded into the A/D Data Register. When the host CPU reads this data, the ST-702R will re-execute the last command loaded into the Command Register and load the new data into the A/D Data Register. Operation in Sequential Mode is similar, except that when the host CPU reads the A/D Data Register, the data from the next sequential channel is loaded. For example, in order to continuously monitor a single channel, the host CPU must write the channel number with Bit 4 set to a "0" in the Command Register. When the Data Ready Register indicates that the data is valid, (or an interrupt occurs), the host CPU reads the data from the A/D Data Register. At this time, the ST-702R will load the last acquired sample from the selected channel into the A/D Data Register. It should be noted that the Command Register may be written with a new command to change either the channel number or the operating mode, providing that Bit 0 of the Data Ready Register is set.

Bit 5 is used to determine whether the ST-702R will output the analog data in either 2's Complement or Sign plus Magnitude format.

Calibration Mode

A mode is provided for use in calibrating the analog circuitry on the ST-702R board. Writing a 1 in bit 7 of the Command Register will place the ST-702R in the Calibration Mode. In normal operation, the on-board microprocessor is continuously performing A/D conversions sequentially on all eight A/D channels.

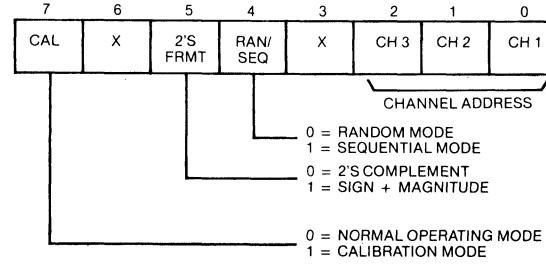

Figure 3: ST-702R Command Register Format (BASE +1)

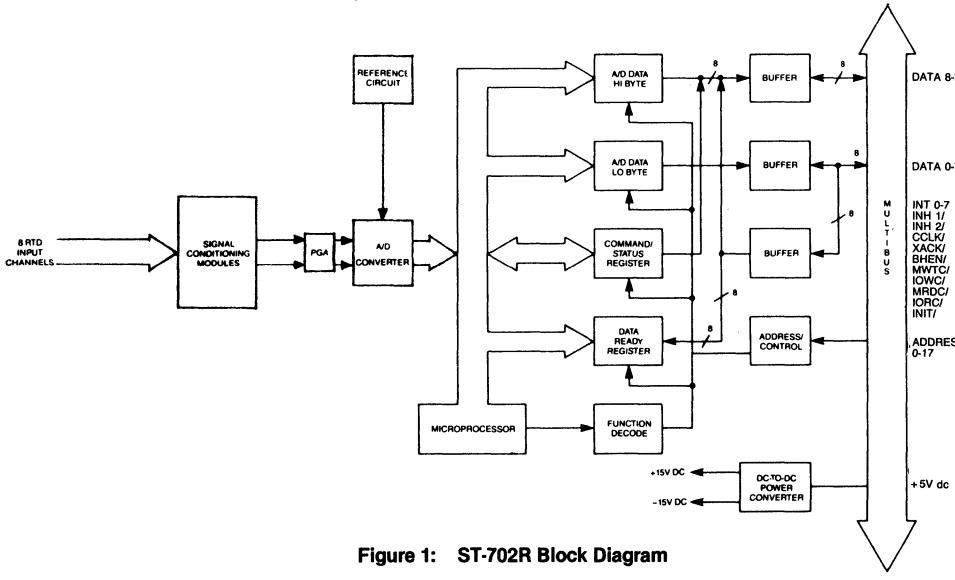

Figure 1: ST-702R Block Diagram

Status Register

The ST-702R Status Register is loaded by the on-board microprocessor along with the A/D Data register. This register should be monitored by the host CPU to determine whether the A/D Data Register contains valid A/D Data or if some error has been detected. It also contains status information in Bits 4-7 indicating DATA out of range status, and indications of possible hardware malfunction in the ST-702R. Also, Bits 0-2 of the Status register contain the channel number for the data in the A/D Data Register.

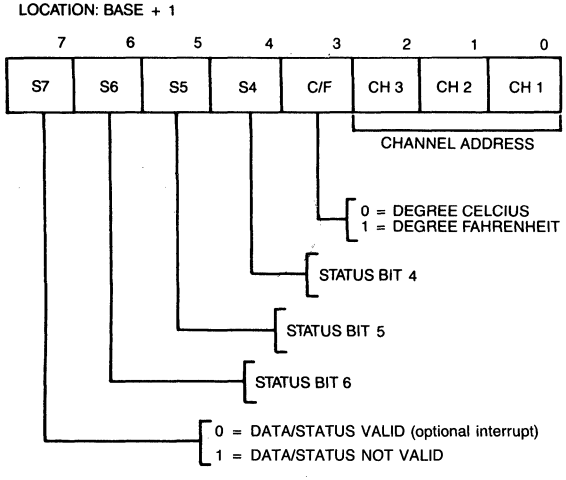

Figure 4: ST-702R Status Register Format (BASE + 1)

Error Status Indication

The ST-702R performs some self-testing at power-up time. The on-board microprocessor tests its internal ROM and RAM. While this test is being conducted, the Status Register indicates the Board Not Ready Status code. Commands should not be written to the Command Register at this time. If either test should fail, the ST-702R sets the Status bits indicating RAM or ROM failure. If this occurs, the board will endlessly loop with the BOARD OK lamp off. If the board detects that an input channel is open, or that measurements are outside of the normal operating RTD temperature range, the Status Bits will reflect this condition. Finally, if the Command Register is written while the Board Calibrate Switch is ON, the Status Register will indicate this error condition.

Error Number				
S7	S6	S5	S4	Error
0	0	0	0	No error
1	0	0	0	Calibration mode
1	0	0	1	Data out of range
1	0	1	0	Open wire detection
1	0	1	1	Board not ready
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Memory or board failure

Table 2: Error Decoding

A/D Data Register

The A/D Data Register is loaded by the ST-702R board and contains either the raw reading from the A/D Converter or the linearized data from an RTD depending on the mode of operation. Data is either a 16 bit 2's Complement or Sign plus Magnitude format.

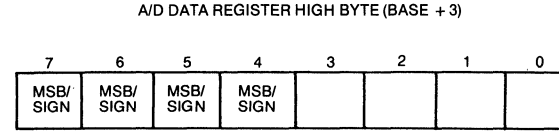

Figure 5a: A/D Data Register Format (High Byte)

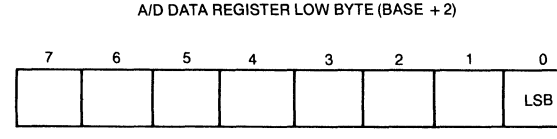

Figure 5b: A/D Data Register Format (Low Byte)

RTD Type Selection

The ST-702R provides the capability to independently select the desired type of RTD for each group of 4 input channels. For example, Channels 0-3 could be set for European operation while Channels 4-7 could be set for American. RTD type selection is selected by a combination of switches and jumpers on the PC Board. This is described in Figure 6.

CH 4-7	S3-5	S3-6	S3-7
CH 0-3	S3-8	S3-9	S3-10
European $\alpha = .00385$	ON	ON	ON
American $\alpha = .00392$	ON	ON	OFF

Figure 6: RTD Input Range Selection

Degree C/Degree F Selection

Degree C — Place S3-4 ON position
Degree F — Place S3-4 OFF position

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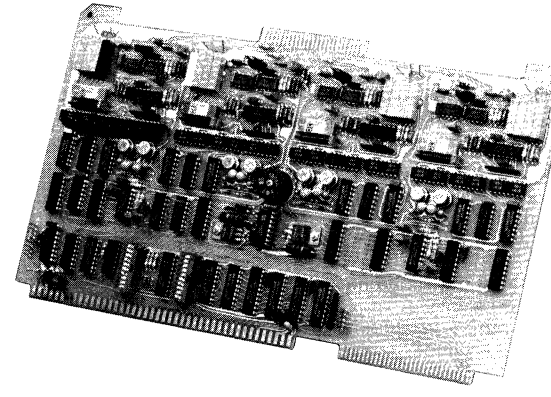
SineTrac™ ST-703
12-Bit, 4 Channel Isolated MULTIBUS D/A Board

FEATURES

- **4 D/A Channels using 12-bit monolithic converters**
- **300 VRMS Isolation, channel-to-channel and channel-to-bus**
- **Accurate to .05% of full-scale reading**
- **Uses identical programming and register assignments to SBC-711/732/724 and ST-711/732/724 boards**
- **Includes 4 externally excitation 4-20 mA current loop channels**
- **Memory mapped, with 24-, 20-, or 16-bit user selectable base address**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Complete hardware and software compatibility with MULTIBUS and SBC series microcomputers**



INTRODUCTION

DATEL expands its line of MULTIBUS and SBC compatible analog output boards with the SineTrac ST-703. The ST-703 provides 4 channels of isolated digital-to-analog (D/A) conversion with 12 bits of resolution. Overall voltage output accuracy is within ± .05% of full-scale range. To ensure the board's compatibility with popular process control and test instrumentation, four voltage ranges and a 4-20 mA current loop output are jumper selectable for each D/A channel.

Like other SineTrac products, the ST-703 is fully hardware-and-software-compatible with its host iSBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built-in. The user installs the ST-703 into an Intel-compatible card cage and wires the analog outputs. The ST-703 is then configured as a memory-mapped peripheral which is addressed by the host computer as eight consecutive memory locations with a user selectable base address. This memory-mapped format allows unlimited D/A channel expansion by using multiple ST-703's, each with a different base address.

The ST-703 is pin compatible with the ST-724, SBC-724, and ST-728 analog output boards. The ST-703 may be used with both 8- and 16-bit microprocessors. The BHEN/line on the MULTIBUS sets the ST-703's address decoders and data latches for compatibility with 8- or 16-bit computers. The ST-703 also supports 24-bit MULTIBUS addressing capability and is downward compatible with 16- or 20-bit systems.

The most unique feature of the ST-703 is its 300 V channel-to-channel and channel-to-bus isolation. Applications include situations where a low-level analog signal must be superimposed on a high voltage, such as testing of power supplies, isolation amplifiers, et cetera. The ST-703 is also useful in applications where actuator failure could cause computer errors or destruction from line voltages being applied to the MULTIBUS. Isolation is accomplished through a combination of optoisolators for digital signals, and transformer isolation for power distribution. An onboard dc-to-dc converter provides four individually isolated supplies for the D/A converters.

The systems manual shipped with each board provides installation instructions, theory of operation, and engineering drawings.

GENERAL DESCRIPTION

Data inputs to the ST-703 are from the host computer's bus. Input coding may be straight binary, offset binary, or 2's complement, and is selectable on the board.

The MULTIBUS BHEN/line is used to set the ST-703's address and data coding for compatibility with 8- or 16-bit CPU's. In the eight-bit mode, the 12 bits of data required for the D/A converters are acquired in two bytes. The lower byte contains the four lower data bits, and is loaded into a storage register for each D/A channel on the ST-703. The next data byte contains the eight higher bits. Upon conversion, the eight MSB's and the four stored LSB's are loaded simultaneously into the DAC. In the 16-bit mode, all 12 data bits are transferred in a single word to the DAC data register. The register outputs are optically isolated and transferred to the D/A converter.

Each channel uses a DATEL model DAC-7541, a 12-bit monolithic device which offers linearity of ± .02% of full-scale range. The converter output is monotonic, having a differential nonlinearity of ± .02% FSR maximum. Offset error on each channel is preadjusted to zero. Trim positions on the board permit recalibration of zero (or offset) and gain settings. Two-speed versions of the board provide settling times of 5 μSec. and 30 μSec. respectively. Zero tempco is ± 2 ppm of FSR/degree Celsius and gain tempco is within ± 10 ppm of FSR/degree Celsius.

The output of each isolated DAC is fed to its own I-to-V conversion amplifier. A total of four voltage output ranges may be jumper selected by the user: 0 to +5V, 0 to +10V, ±5V, and ± 10V. In addition, a V-to-I converter circuit is provided for each D/A output channel. A 4 to 20 mA output, usable with an output load from 0 to 500 Ohms, is also jumper selectable.

The ST-703 contains a power-on reset circuit that allows each D/A output to be set to 0.000V at power-on time regardless of the input coding and output range configuration.

The current output requires an external excitation source, a +18V to +30V dc regulated supply capable of 25 mA per D/A channel. Voltage and current ranges on the ST-703 are selected individually for each channel. This allows a mix of voltage or current outputs on a single board.

The ST-703 is a memory-mapped peripheral occupying eight consecutive locations in the computer's address space. The board's base address is factory-set at 00FF10 Hex. However, a user may relocate the board address anywhere up to FFFFF8 on 8-byte boundaries using DIP switches on the board.

To make the ST-703 compatible with different speed CPU's and memory systems, a Transfer Acknowledge Delay (XACK/ Delay) is provided, permitting eight selectable delays from 0 to 700 nSec. in 100 nSec. increments.

The ST-703 is fully bus-, card cage-, and software-compatible with the MULTIBUS and with Intel RMX software. The board is 12.0 inches wide × 6.75 inches deep × 0.54 inch high (305 × 172 × 14 mm). Multiple ST-703 boards may be mounted in adjacent card slots when used with a standard .60 inch spacing Intel card cage.

The ST-703 draws all its power from the MULTIBUS +5V and +12V lines. An on-board dc-to-dc converter provides four isolated ±15V supplies to drive the analog output circuits.

The ST-703 weighs approximately 12 ounces (0,341 kilograms). It can operate over a temperature range of 0 to +55 degrees Celsius with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4,600 m) in altitude.

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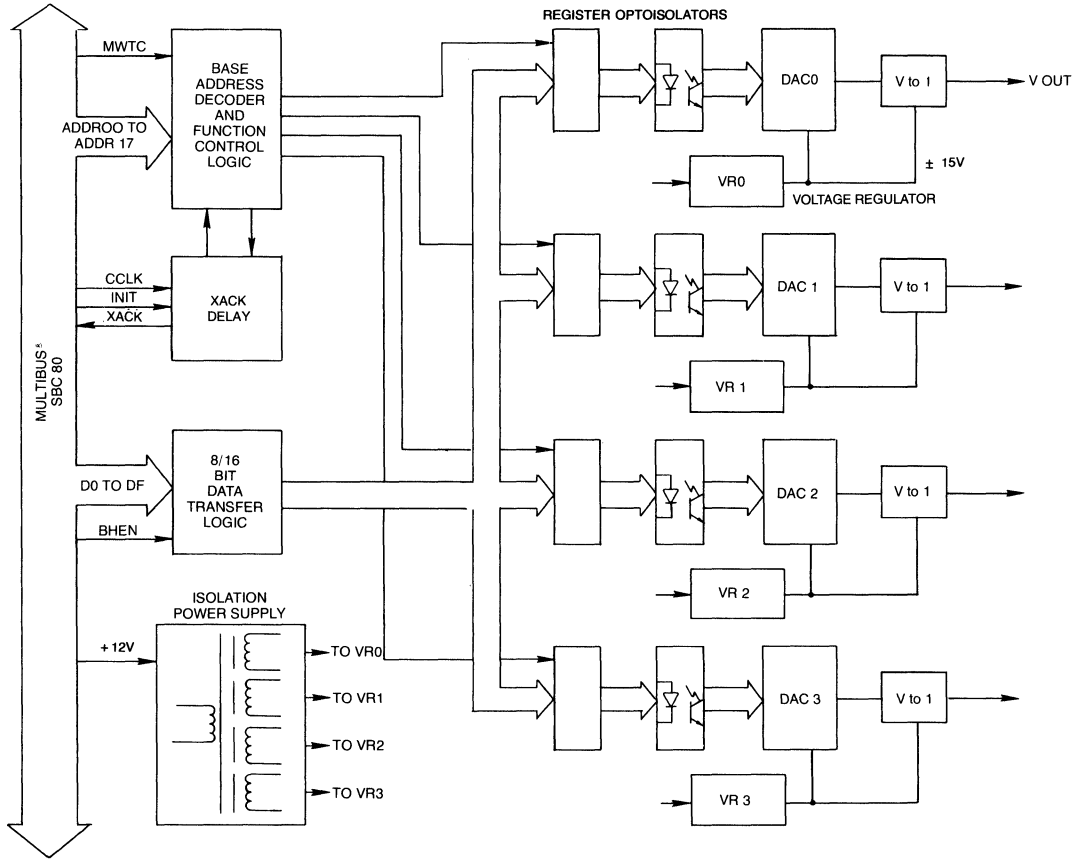
ST-703
BLOCK DIAGRAM



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FUNCTIONAL SPECIFICATIONS

(typical at 25°C unless otherwise noted) — use generic.

D/A ANALOG OUTPUT

Number of Channels . . 4 D/A channels

Channel Expansion . . . Indefinite channel expansion using separate ST-703 boards at different base addresses; limited by available card slots and supply current

Full-Scale Output Ranges *	±10V (standard) ±5V 0 to +5V 0 to +10V 4 to 20 mA	Individually selectable per channel
Digital Input Coding	Straight Binary Offset Binary (standard) 2's Complement	Selectable per channel
Output Impedance	50 Milliohms	
Output Current (Voltage Output)	Maximum ±5 mA @ ±10V short-circuit-proof to ground.	
Current Loop Excitation Voltage	Maximum +10V to +30V, regulated, user supplied, 25 mA dc maximum channel.	
Isolation Voltage (continuous)	300V RMS channel-to-channel and channel-to-bus	

*NOTE: Outputs are short circuit protected.

ADDRESSING

Reserves a block of eight consecutive memory locations. Base address may be located on an eight byte boundary in the 24-bit CPU address space, provided the least significant byte equals 0 or 8 H.

PERFORMANCE

Accuracy at +25°C	±0.05% of FSR, ±1 LSB (includes noise and nonlinearity).
Differential Nonlinearity	±0.5 LSB, 0 to +55°C
Zero Temperature Drift (Unipolar Output)	Within ±5 ppm of FSR/°C
Offset Temperature Drift (Bipolar Output)	Within ±10 ppm of FSR/°C
Gain Temperature Drift	Within ±20 ppm of FSR/°C
Settling Time	
ST-703B	6 μSec. to 0.5 LSB of final value
ST-703A	30 μSec. to 0.5 LSB of final value
Slew Rate	8 V/μSec.

PHYSICAL

Outline Dimensions	12.00 inches wide x 6.75 inches deep x 0.54 inch high
Weight	304,8 wide x 171,5 deep x 13,7 high mm
Operating Temperature Range	12 ounces (0.34 kilograms)
Storage Temperature Range	−25 to +85°C
Relative Humidity	10% to 90% non-condensing
Altitude	0 to 15,000 feet (4,600 M)

POWER CONSUMPTION

+5V @ 1 A
+12V @ 450 mA

GENERAL

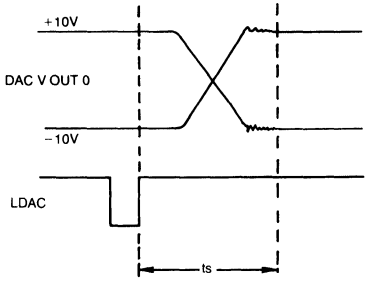
Bus Compatibility	Pin-for-pin, card guide, and program compatible with MULTIBUS (IEEE 796) and SBC series microcomputers.
CPU Compatibility	8- or 16-bit CPU compatible

ORDERING GUIDE

Model ST-703A	Isolated 4 Channel D/A board, 30 μsec. settling time
Model ST-703B*	Isolated 4 Channel board, 5 μsec. settling time

*Note: ST-703B should be selected for applications requiring low transient energy such as amplifier inputs.

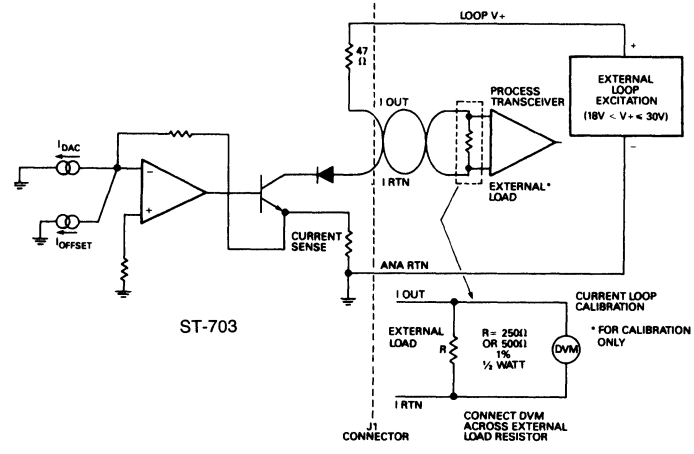
SETTLING TIME



ts: settling time = optoisolator delay + slew time + settling to ±½ LSB final voltage value

Full-scale output ranges*

TYPICAL CURRENT LOOP CIRCUIT



ST-703

11

DATA FORMAT

The ST-703 is a memory-mapped peripheral and appears to the CPU as a group of eight consecutive memory locations. Two locations are assigned to each D/A channel. The ST-703 requires 12 bits of digital data from the CPU for a single D/A conversion. The following chart shows how 8- and 16-bit CPU's format this data.

The ST-703 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS goes to zero volts (pin 27 of the connector P1). Consequently, a high input on BHEN/ sets the ST-703 for the 8-bit format.

D15								SINGLE WORD (16-BIT CPU)							D0
HIGH BYTE (8-BIT CPU)								LOW BYTE (8-BIT CPU)							
D7							D0	D7							D0
DAC BIT 1 (MSB)	DAC BIT 2	DAC BIT 3	DAC BIT 4	DAC BIT 5	DAC BIT 6	DAC BIT 7	DAC BIT 8	DAC BIT 9	DAC BIT 10	DAC BIT 11	DAC BIT 12 (LSB)	X	X	X	X

X = Don't care

REGISTERS

Note that 8-bit CPU's must transfer the 12 data bits in two bytes. The low byte contains the four least-significant data bits which are stored in a register on the ST-703. The high byte contains the eight most-significant data bits. When the high byte is transferred, all 12 data bits are loaded into the DAC holding register and the D/A output is updated. Data transfer with a 16-bit CPU is done with a single word transfer; all 12 bits are simultaneously updated. Selection of 8- or 16-bit transfers is accomplished automatically, depending on the state of the MULTIBUS BHEN/line. The following chart details the memory address assignments of the ST-703 board. Note that when the ST-703 is used with a 16-bit CPU, data transfer must be to an even-numbered memory location.

ST-703 REGISTER ASSIGNMENTS

MEMORY ADDRESS (8-BIT CPU)	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-BIT CPU)
BASE + 0	DAC 0 LSB Byte	BASE + 0
BASE + 1	DAC 0 MSB Byte	
BASE + 2	DAC 1 LSB Byte	BASE + 2
BASE + 3	DAC 1 MSB Byte	
BASE + 4	DAC 2 LSB Byte	BASE + 4
BASE + 5	DAC 2 MSB Byte	
BASE + 6	DAC 3 LSB Byte	BASE + 6
BASE + 7	DAC 3 MSB Byte	

BASE ADDRESS SELECTION

The ST-703 is a memory-mapped peripheral that occupies eight consecutive memory locations in the computer address space. The full 24-bit MULTIBUS addressing is supported, although the board may be used with CPU's that provide 16- or 20-bit addresses. The base address is selected by a combination of jumpers and DIP switches on the PC board. The board is factory-configured for 16-bit addressing and with a base address of 00FF10 hexidecimal.

24-, 20-, 16-BIT ADDRESS SELECT

Referring to the table below, remove or install the programming jumpers for the correct number of address select bits used in the system where the ST-703 is to be installed.

JUMPER	24 BIT	20 BIT	16 BIT
E103-E104	IN	OUT	OUT
E105-E106	IN	OUT	OUT
E107-E108	IN	OUT	OUT
E109-E110	IN	OUT	OUT
E111-E112	IN	IN	OUT
E 97-E 98	IN	IN	OUT
E 99-E100	IN	IN	OUT
E101-E102	IN	IN	OUT

BASE ADDRESS SELECTION

(1. Select a base address, in hexidecimal, and write it in Base Address, Hex.

(2. Convert the hexidecimal code to binary by writing 1's and 0's in the appropriate boxes (opposite Hex Bit Weighting).

(3. Set the base address desired on DIP switches S1 and S2. A closed switch (ON) corresponds to a 1 on the corresponding address line. An open (OFF) switch corresponds to a 0. Unused high order address switches must be left in the open (OFF) position. For example, if the CPU provides only 16 address lines, the address switches corresponding to ADR10 through ADR17 must be OFF.

1. To select a base address in hexidecimal use the following chart for changing configurations.

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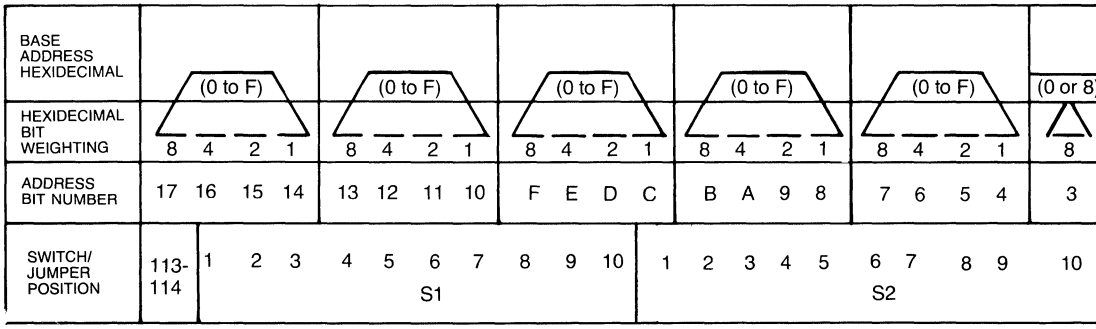
BASE ADDRESS SELECTION



TRANSFER ACKNOWLEDGE (XACK) DELAY SELECTOR

The ST-703 generates a Transfer Acknowledge (XACK) signal in response to memory/write commands from the MULTIBUS. It is sometimes desirable to delay this signal in order to match the signal to the CPU timing. A jumper selectable Transfer Acknowledge Delay, ranging from 100 to 800 nSec., is available in the ST-703. It should be noted that the XACK/delay is generated from the MULTIBUS CCLK/signal which is assumed to have a period of 100 nSec. Also, since this signal is asynchronous, the actual delay can only be set within a tolerance of one clock period, or 100 nSec. The jumper selections to configure the XACK/delay is as follows:

DELAY (nSec.) (standard)	JUMPER
100	E85 - E86
200	E87 - E88
300	E89 - E90
400	E93 - E94
500	E95 - E96
600	E91 - E92
700	E83 - E84
800	E81 - E82

Install only one jumper. The standard jumper from E85-E86 is connected in etch on the printed circuit board and must be cut if this jumper is changed.

INPUT CODING/POWER-ON RESET JUMPERS

The ST-703 may be configured to allow a choice of input coding formats. These are straight or offset binary, or 2's complement formats. In many applications it is desirable for the D/A converters to output a voltage of 0.000 Volts at power-on time. Jumpers are provided to accomplish this and depend on the range and input coding selected.

Jumpering is as follows:

INPUT CODING/POWER-ON RESET JUMPERS

INPUT CODING	DAC 0	DAC 1	DAC 2	DAC 3
Unipolar, Offset Binary	E61-E62 E58-E59	E66-E67 E63-E64	E73-E74 E70-E71	E78-E79 E75-E76
Bipolar, Offset Binary (Standard)	E61-E62 E57-E58	E66-E67 E64-E65	E73-E74 E69-E70	E78-E79 E76-E77
Unipolar, 2's Complement	E60-E61 E57-E58	E67-E68 E64-E65	E72-E73 E69-E70	E79-E80 E76-E77
Bipolar, 2's Complement	E60-E61 E58-E59	E67-E68 E63-E64	E72-E73 E70-E71	E79-E80 E75-E76

OUTPUT RANGE SELECTION

The output range of each D/A converter may be individually selected to provide a choice of four voltage output ranges or a single current loop range. The jumper-selected ranges may be set according to the following chart.

The ST-703 board is normally shipped with jumpers set for the ± 10V output, and an offset binary output coding. Whenever there is a change in output range on a given channel, that channel should be recalibrated.

OUTPUT RANGE JUMPERS

RANGE	DAC 0	DAC 1	DAC 2	DAC 3
0 to +5V	E9-E10 E1-E3	E23-E24 E15-E17	E34-E35 E29-E31	E48-E49 E43-E45
0 to +10V	E9-E10 E3-E5	E23-E24 E17-E19	E34-E35 E31-E33	E48-E49 E45-E47
+/−5V	E10-E11 E6-E7 E3-E5	E24-E25 E20-E21 E17-E19	E35-E36 E37-E38 E31-E33	E49-E50 E51-E52 E45-E47
+/−10V (Standard)	E10-E11 E7-E8 E3-E4	E24-E25 E21-E22 E17-E18	E35-E36 E38-E39 E31-E32	E49-E50 E52-E53 E45-E46
4 - 20 mA	E9-E10 E7-8 E2-E3	E23-E24 E21-E22 E16-E17	E34-E35 E38-E39 E30-E31	E48-E49 E52-E53 E44-E45

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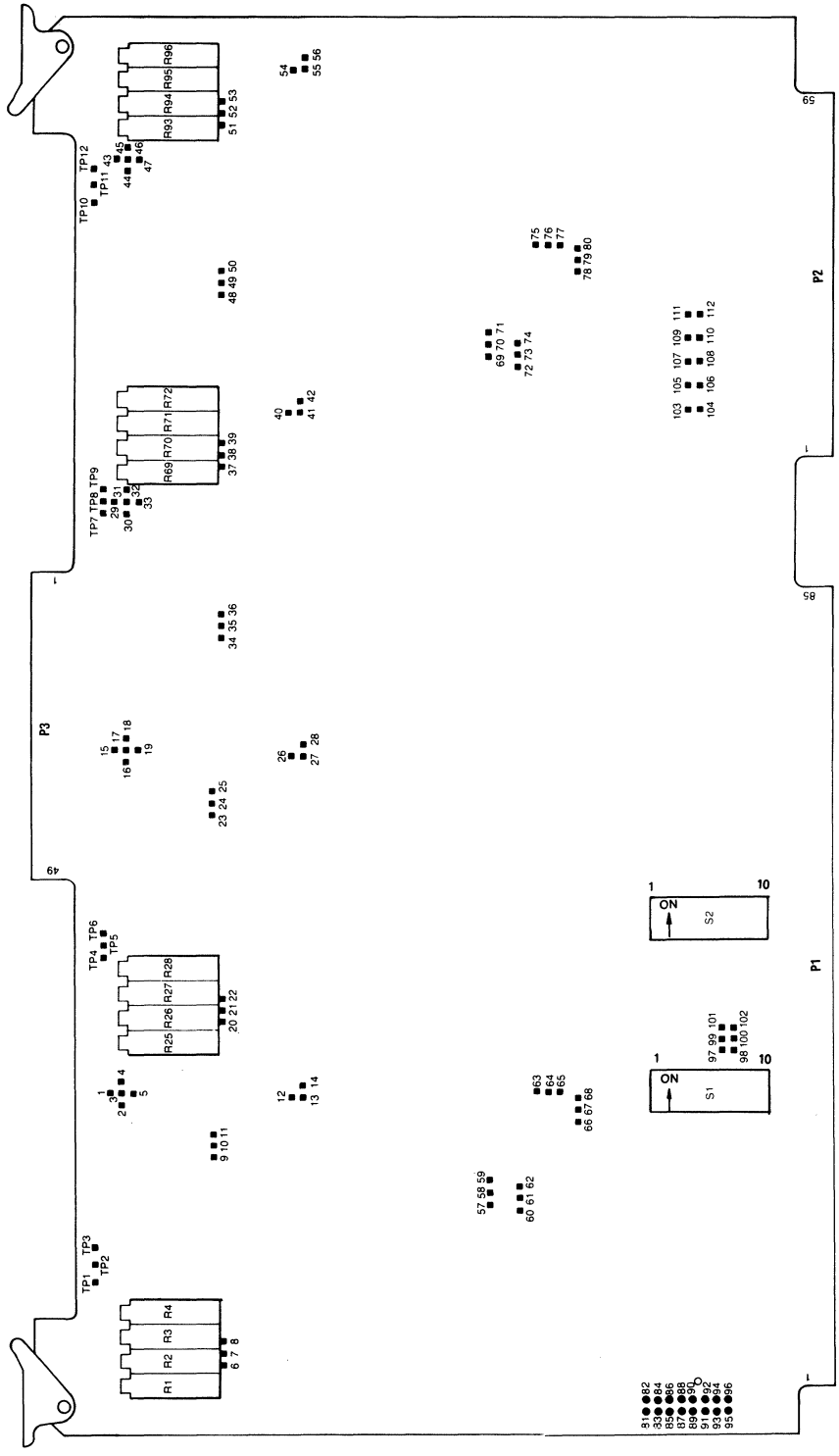
ST-703
BOARD LAYOUT



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OPTOISOLATOR SPEED CONFIGURATION

The ST-703 is available with a choice of two setting time options. Since/because the DAC data lines are optically coupled, the DAC settling time is dependent on the switching times of the optoisolators used. A jumper is provided to select the settling time and is dependent on the type of optoisolator installed on the board.

SETTLING TIME JUMPER

MODEL	DAC 0	DAC 1	DAC 2	DAC 3
ST-703A	E12-E13	E26-E27	E40-E41	E54-E55
ST-703B	E13-E14	E27-E28	E41-E42	E55-E56

NOTE: The settling time jumper is programmed per the model number. It should not be changed to avoid permanent damage to the optoisolators.

CONNECTORS

The ST-703 board contains three connectors: P1 and P2 are the MULTIBUS connectors, and P3 is the Analog Output connector.

The P2 MULTIBUS connector is used only when a system controller's address is 24 bits. The pin assignment for the four (extended) address lines on P2 are shown in Table 1.

P3 is the Analog Output connector, which is described in Table 2. For current loop connection, refer to the current loop circuit.

Table 1. Multibus Connector (P2)

PIN	SIGNAL	FUNCTIONAL DESCRIPTION
55	ADR 16	
56	ADR 17	4 address line inputs
57	ADR 14	for 24 bit address controllers.
58	ADR 15	

Table 2. Analog Output Connector (P3)

PIN	(COMPONENT SIDE) FUNCTION	PIN	FUNCTION
	Pins 1 through 22 are no connection		
23	Analog Ground D/A CH 3	24	DAC V OUT CH 3
25	LOOP I RTN D/A CH 3	26	LOOP I IOUT CH 3
27	Analog Ground D/A CH 3	28	LOOP V EXC CH 3
29	Analog Ground D/A CH 2	30	DAC V OUT CH 2
31	LOOP I RTN D/A CH 2	32	LOOP I OUT CH 2
33	Analog Ground D/A CH 2	34	LOOP V EXC CH 2
35	Analog Ground D/A CH 1	36	DAC V OUT CH 1
37	LOOP I RTN D/A CH 1	38	LOOP I OUT CH 1
39	Analog Ground D/A CH 1	40	LOOP V EXC CH 1
41	Analog Ground D/A CH 0	42	DAC V OUT CH 0
43	LOOP I RTN D/A CH 0	44	LOOP I OUT CH 0
45	Analog Ground D/A CH 0	46	LOOP V EXC CH 0
47		48	
49		50	

NOTE: The Analog Ground lines for the D/A channels are not connected to each other or to the MULTIBUS ground.

CALIBRATION

The ST-703 board is calibrated for a voltage output range of ± 10V and Offset Binary coding. Calibration is required if the output range is changed for any of the D/A converters. A 4½ digit digital voltmeter is required. To calibrate the ST-703, perform the following steps in order.

1. Use the following table (specifications) to connect the digital voltmeter (DVM) to the test point, corresponding to the DAC to be calibrated.

(FULL-SCALE) +9.9800 V REFERENCE ADJUSTMENT TEST POINTS

	DAC 0	DAC 1	DAC 2	DAC 3
DVM + INPUT	TP1	TP4	TP7	TP10
DVM – INPUT	TP3	TP6	TP9	TP12
POT	R3	R25	R69	R93

Adjust the potentiometer for a reading of +9.9800 volts.

2. Connect the digital voltmeter (DVM) to the test point in the following table, corresponding to the DAC to be calibrated.

NEGATIVE REFERENCE ADJUSTMENT TEST POINTS

	DAC 0	DAC 1	DAC 2	DAC 3
DVM + INPUT	TP2	TP5	TP8	TP11
DVM – INPUT	TP3	TP6	TP9	TP12
POT	R2	R26	R70	R94

Adjust the potentiometer for a reading of –2.500 volts if the DAC is to be configured for the ±5 Volt range. Otherwise, adjust the pot for a reading of –3.333 Volts.

3. Monitor the D/A output to be calibrated with the DVM. If calibrating for 4-20 mA output range, use a 250 Ohm .1% loop resistor to measure the voltage drop across the resistor.

Use the Diagnostic Test Program Calibration Test to enter the –full-scale hexidecimal data for the D/A channel under test. This data would be 0000 hexidecimal for binary coding, or 8,000 hexidecimal for 2's complement coding. Adjust the proper Zero (Offset) pot for the correct reading, as shown below.

ZERO OR OFFSET ADJUSTMENT POTENTIOMETERS

CHANNEL	POT
DAC 0	R3
DAC 1	R27
DAC 2	R71
DAC 3	R95

DAC – FULL-SCALE READINGS

RANGE	READING
0 to +5 V	0.0000 V
0 to +10 V	0.0000 V
±5V	– 5.0000 V
±10V	–10.0000 V
4 - 20 mA	1.0000 V

4. Monitor the D/A output to be calibrated with the DVM. Use the Diagnostic Test Program Calibration Test to enter the + full-scale hexidecimal data for the D/A channel under test. This data would be FFFF hexidecimal for binary coding, or 7FFF hexidecimal for 2's complement coding. Adjust the proper GAIN pot for the correct reading, as shown below.

GAIN ADJUSTMENT POTENTIOMETERS

CHANNEL	POT
DAC 0	R4
DAC 1	R28
DAC 2	R72
DAC 3	R96

DAC + FULL-SCALE READINGS

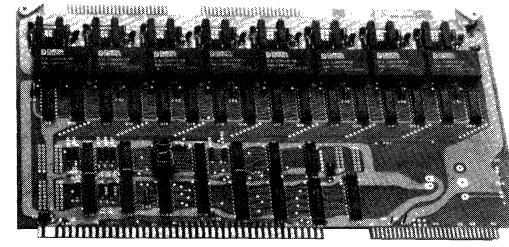
RANGE	READING
0 to +5 V	+4.9988 V
0 to +10 V	+9.9976 V
±5V	+4.9976 V
±10 V	+9.9951 V
4 - 20 mA	+4.9990 V

SineTrac™ D/A and Current Loop Boards for SBC-80 and MULTIBUS® Microcomputers

SineTrac™ ST-716

FEATURES

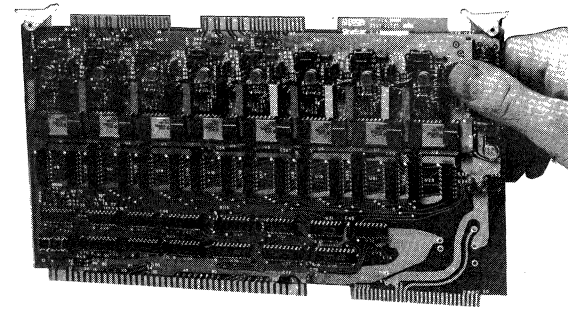
- **4 or 8 D/A Channels, 16-bit resolution**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Accurate to 0.005% of full-scale reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **20-Bit addressing**
- **Memory-mapped, with User-Selectable Base Address**
- **Three user-selectable output ranges available: ±5V dc, and 0 ⟶ +10V dc, ±10V dc**
- **Selectable Transfer Acknowledge Delay (XACK/); ensures compatibility with different memory speeds**



SineTrac™ ST-728

FEATURES

- **4 or 8 D/A channels, 12-bit resolution**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Accurate to .05% of full-scale reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **Memory-mapped, with user-selectable Base Address, 16-, 20- or 24-bit addressing**
- **Three user-selectable input data codes: Straight Binary, Offset Binary, or Two's Complement**
- **Five user-selectable output ranges available: ±5V dc, ±10V dc, 0 ⟶ +10V dc, 0 ⟶ +10V dc, and 4-20 mA current loop, individually selected for each channel**
- **Selectable Transfer Acknowledge Delay (XACK/); ensures compatibility with different memory speeds**



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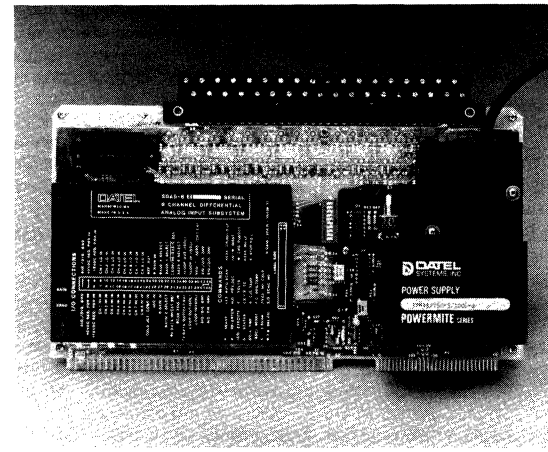
ST-705 Analog Input 8-Channel ASCII Serial Single Board Subsystem

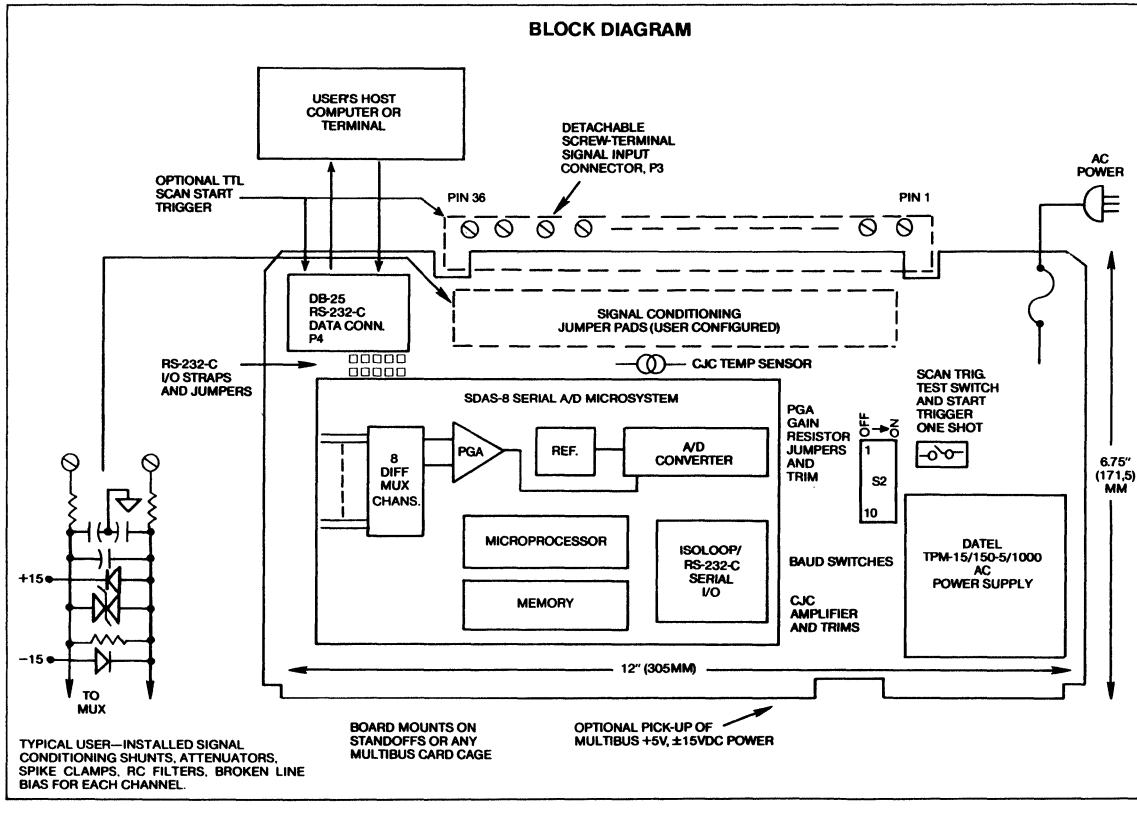


FEATURES

- **8 differential A/D channels using the SDAS-8 microsystem**
- **RS-232-C or 20mA serial isolated loop**
- **Includes input conditioning PC board pads**
- **Includes direct thermocouple measurement with cold-junction temperature sensor and compensation amplifier**
- **Local TTL one-shot scan start trigger from pushbutton or contact closure**
- **Directly connects to Datel's APP-20 and 48 miniature serial thermal panel printers**
- **Selectable gain instrumentation amplifier board pads and trim pot.**

(Refer to the SDAS-8 product literature for full functional description of the SDAS-8 microsystem).

BLOCK DIAGRAM



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DESCRIPTION

Designed as a complete, serially accessed 8 channel data acquisition subsystem, the ST-705 is configured on a 12" × 6.75" × 1.7"H MULTIBUS size board.

The ST-705 contains the SDAS-8 data acquisition microsystem, an AC power supply, screw terminal analog input connections and a standard 25-pin RS-232-C DB-25P connector for direct plug-in to the user's terminal or computer. The ST-705 also includes the local thermocouple cold-junction compensation amplifier and connector temperature sensor. For local triggered scan starts, a TTL one-shot circuit accepts an onboard or remotted pushbutton switch or contact closure. Extra PC board pads are included for user-installed input voltage dividers (higher voltage ranges), current shunts (direct 4-20mA measurement, etc.), over-voltage protection clamp diodes or RC hash filters. Barrier screw terminals are installed for an AC line cord.

A board pad matrix is included for user-installed SDAS-8 gain resistors and a gain trim pot is included. These pads would normally be used for the x80 and x160 gain resistors for direct SDAS-8 thermocouple measurement.

The ST-705 may be mounted in a MULTIBUS card cage (available from SCANBE/ZERO, MUPAC, Electronic Solutions, Intel and others) or in the user's host MULTIBUS computer. The ST-705 may also be mounted in a user-supplied separate chassis on standoffs. Although the ST-705 does not connect to MULTIBUS backplane bus signals, pads are included to use +5 Vdc and ±15Vdc power from the host computer, thereby eliminating the ST-705 AC power supply. Using a combination of the transformer-isolated AC supply and the optoisolated 20mA loop serial port, isolation of the analog inputs from the AC line or serial interface is achieved.

USER PC BOARD PADS

There are three primary areas where the user may customize the ST-705 for his application. Caution: This requires mounting and soldering components on a PC board and assumes that the user is skilled at component procurement and electronic assembly. If you need assistance, please contact Datel or a competent engineer.

The three areas are:

1. Input signal conditioning
2. SDAS-8 gain resistor selection and trim
3. Serial port baud rate and pinout strapping

For each of those option areas, refer to the revision level schematic (drawing C-12301) and assembly/layout diagrams (drawing D-12300) for the ST-705 in this brochure.

Input signal conditioning encompasses a wealth of possible options, referring to the schematic drawing. If no conditioning is desired, PC board etch is installed for straight-through unmodified inputs (standard supplied configuration).

The gain resistor pad area includes options for the two fixed thermo-couple gains (J, K require x80; S, T require x160). Also available is a user-selected gain and trim pot pad area.

Serial port board options include baud rate selection using the on-board DIP-switch and RS-232-C handshake pinout options to accept a variety of smart and dumb terminals and host computers. By judicious jumpering, the ST-705 may be made to emulate either an RS-232-C modem DCE device or a terminal DTE device. Most CRT terminals require the ST-705 to interface as a modem. Some small printers and computer serial ports require the ST-705 to interface as a terminal. Many RS-232-C devices ignore the DTR, DSR, CTS, RTS and carrier detect handshakes whereas some require that they are asserted. Refer to the EIA RS-232-C specification and the user documentation of the host device you are connecting to.

The 20mA serial isoloop is normally disconnected from the DB-25P receptacle since no standard 20mA connection exists. Jumpers may be installed as suggested on the ST-705 diagram or at the user's discretion.

The screw-terminal input connector is Datel model 60-12474-1.

MODEL NUMBER/ORDERING GUIDE

ST-705 ___ ___

AC POWER

A = 115 VAC, 60 Hz NMR
E = 230 VAC 50 Hz NMR
J = 100 VAC, 60 Hz NMR
X = AC POWER SUPPLY OMITTED (Requires regulated +5, +/−15 VDC power. May be jumpered from MULTIBUS if available)

(All models accept 47 to 440 Hz. However maximum rejection of AC noise occurs at the normal mode rejection frequencies listed above)

STATION NUMBER

1 = CHANNELS 1-8 (MASTER, ECHOS ALL COMMANDS)
2 = SLAVE, CHANNELS 9-16
3 = SLAVE, CHANNELS 17-24
4 = SLAVE, CHANNELS 25-32

(Use Stations 2, 3, 4 only in 20mA multidrop with Station 1 Master)

Example:
ST-705A1
(115VAC, 60Hz NMR, Master Station 1, Channels 1-8).
A screw-terminal analog input connector is included.

ACCESSORIES/ RELATED PRODUCTS

MODEL/ DESCRIPTION

60-12474-1
Spare screw terminal. Analog input connector (One is included with ST-705)

58-2079130
DB-25S serial data mating connector, solder tab. (Optional if you do not have an RS-232 cable).

58-2079260
DB-25P solder tab connector (if required at terminal or computer).

APP-20A21
APP-48A2
RS-232-C/20 mA miniature panel-mount thermal printers. Please request brochures.

TABLE OF CONTENTS

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SPECIFICATIONS (Typical @ +25°C)

ANALOG INPUTS

Input Configuration
Differential, high-impedance, true balanced non-isolated, voltage input.

Number of Channels
8 differential channels plus 1 single-ended CJC sensor input

Full Scale Input Range
+/− 4.095Vdc (gain=1)

Thermocouple Temperature Ranges
Type J − 165°C to + 760°C
Type K − 165°C to + 1232°C
Type S − 0°C to + 1768°C
Type T − 200°C to + 400°C

Progammable Gain Amplifier
Resistor-selected up to gain = 200 (+/−20mVdc FSR)

A/D Converter
12 binary bits and polarity
(1 part in 8192), 0.02% FSR linearity

Resolution
1 Count = 1 millivolt at GAIN = 1

Common Mode Voltage Range
+/−11Vdc max to analog ground

Common Mode Rejection
70dB min.

Isolation
20mA serial port optoisolation: +/−2500 V pk, 100 megohms. AC power supply transformer isolation: 1500 VAC, min., 100 megohms, 250 pF

Normal Mode Rejection
40dB @ 50Hz (SDAS-8E), 40dB @ 60Hz (SDAS-8A)

Input Impedance
800 kilohms

Temperature Coefficient
+/−20ppm of FSR°C (GAIN = 1)

A/D Sampling Rate
15 Samples/Sec. (SDAS-8A) to RAM buffer (12.5Hz, SDAS-8E)

COMMUNICATIONS

Data Encoding
Upper case ASCII characters per ANSI X 3.4−1977

Baud Rates
75 to 9600 (Except 110)

Mode
Full duplex, asynchronous

Character Format
1 Start, 8 Data, no parity, 1 Stop bit (all popular 10-bit formats). Output data bit 7(8th bit) = 0

Levels
1. RS-232-C subset, non-isolated
2. 20mA loop, optoisolated

Host Buffer Control
XON, XOFF, (Control Q, Control S) Character encoded

RS-232-C Signals
RxD, TxD, Logic Gnd, Prot. Gnd.

Multidrop
Up to 4 stations, 32D chans., isoloop only, 4 wire

Error Detection
4 ASCII/HEX checksum characters, per A/D scan

DATA TYPES

A/D Data
Selectable decimal/hexadecimal

Thermocouple Data
Linearized to J, K, S, T, Fahrenheit/Celsius conversion, cold-junction compensated

Time of Day Clock
23:59:59 hours, 1 second resolution, 0.05% crystal accuracy

Status Message
Hex encoded and text

A/D SCAN TRANSMISSION START

1. Polled by remote serial command
2. Auto-start from internal timer, command-selected 1 second to 17:59:59 hours
3. Local TTL event trigger input or switch closure.

LINK COMMAND TYPES

Line length (20 to 132 characters), editing, clock controls, A/D controls, resets, data select, terminal controls

PHYSICAL

Outline dimensions
6.75" X 12.00" X 1.62" (171,5 X 304,8 X 41,15mm) excluding standoffs,
MULTIBUS format

Operating Temperature
0° to +60°C

Power Required
Choice of:
115 VAC, +/−10%, 60-440Hz
230 VAC, +/−10%, 48-440Hz
100 VAC, +/−10%, 48-440Hz

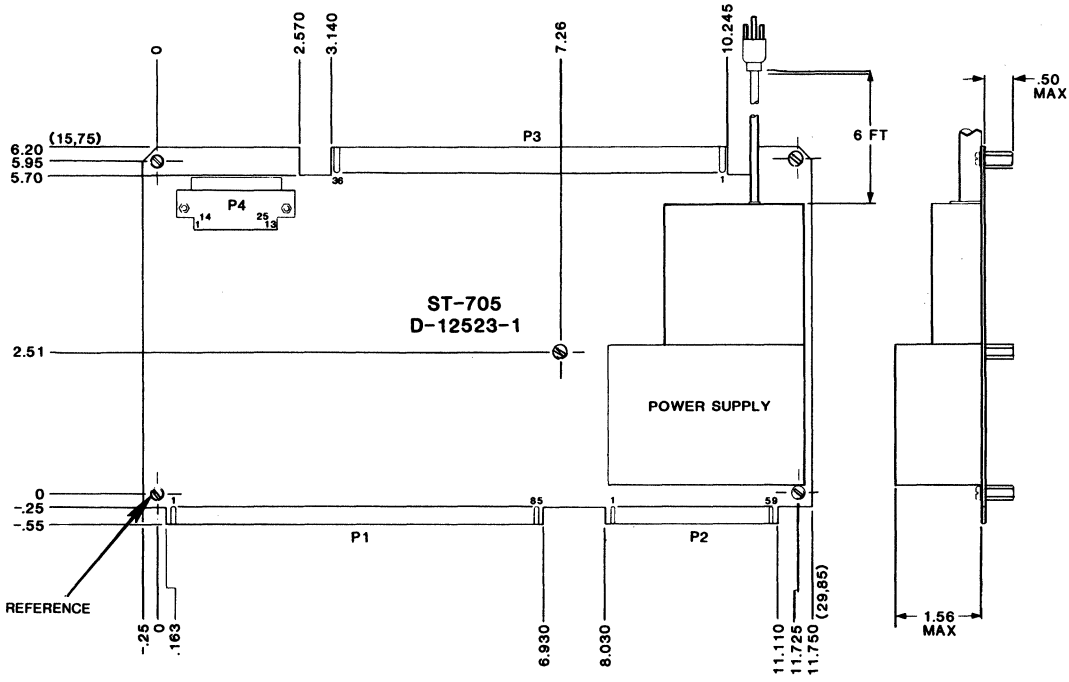
Analog Input Connector
Screw terminal detachable from PCB edge fingers, 0.200" centers, Datel #60-12474-1.

Serial Data Connector
DB-25P 25-pin suitable for most RS-232-C devices.

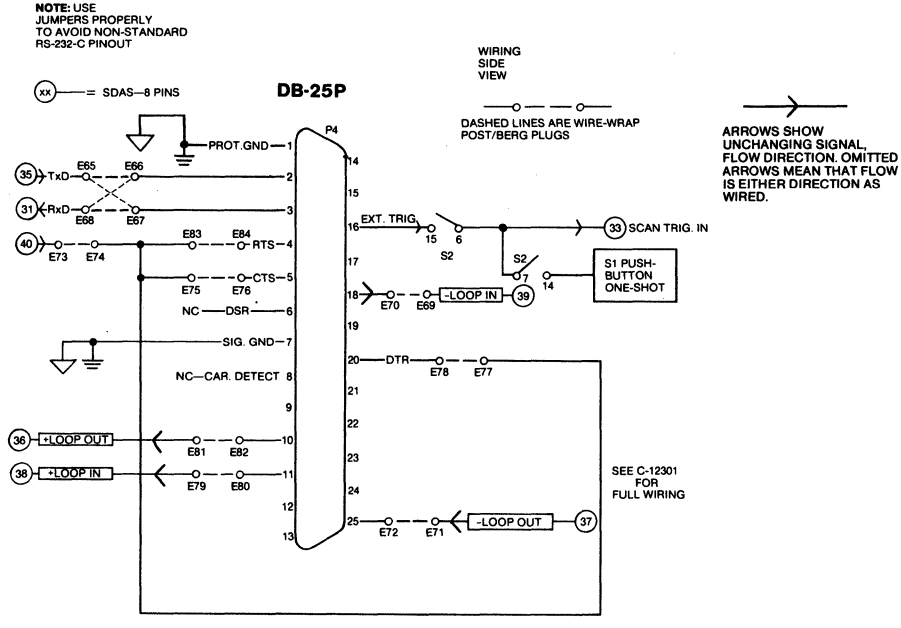
MULTIBUS is an Intel Corp. trademark.

For detailed information about the SDAS-8 Data Acquisition Microsystem mounted on ST-705, refer to the SDAS-8 User's Guide, available on request.

OUTLINE DIMENSIONS
Inches (mm)



P4 DATA CONNECTOR WIRING



RS-232-C SERIAL DATA INTERFACE

The serial data connections shown describe interface to three common RS-232-C devices: most terminals, computer serial ports and modems. There are several basic rules to properly interface to RS-232-C devices. They are:

(1) One end must be the "modem" (DCE device) and the other must be the "terminal" (DTE device). This has to do with the direction of data transmission on pins 2 and 3 of the RS-232-C interface and not the function of the actual devices.

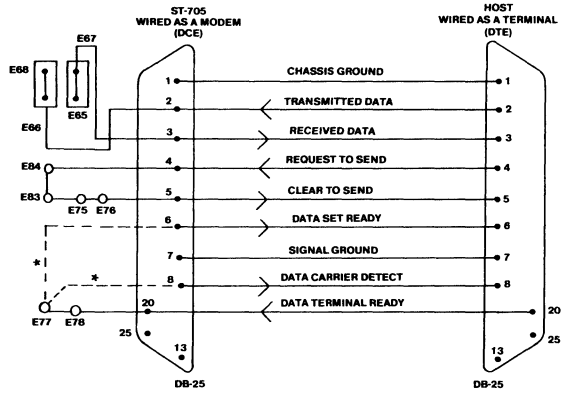
Most modems are wired as DCE devices. Most terminals are DTE devices, as you would expect. Many computer serial ports are DTE but some are DCE. The ST-705 may be jumpered either way. Do not let line names confuse you. Instead, observe the direction of signal flow shown by the arrows in the diagrams.

(2) Most RS-232-C devices require connection to the important handshake signals shown. The ST-705 does not use these handshakes but contains a mini "breakout" function to accommodate correct connection of these handshakes. Minimal RS-232-C connection to ST-705 requires only pins 2, 3 and 7 between AC-isolated devices.

(3) The character coding, length and protocol between both ends must agree. ST-705 ASCII usage is widely accepted for terminals and computers. Modems are transparent to coding conventions.

For further background, consult the EIA RS-232-C specification and other references on data communications.

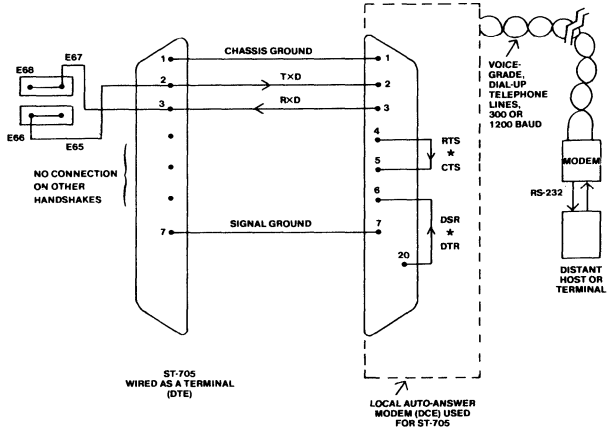
WIRING TO MOST TERMINALS AND COMPUTER SERIAL PORTS



* User-installed optional jumper connections DTR-DSR (pins 20-6) and DTR-DCD (pins 20-8) may be required for many terminals.

The connections shown above will work for most terminals and computer serial RS-232-C ports wired as a terminal. (Consult your computer technical documentation.)

WIRING TO MOST RS-232-C MODEMS



* Many modems require RTS and DTR to be asserted. This may be jumpered as shown on the modem connector or on the ST-705. The ST-705 does not require these handshake signals.

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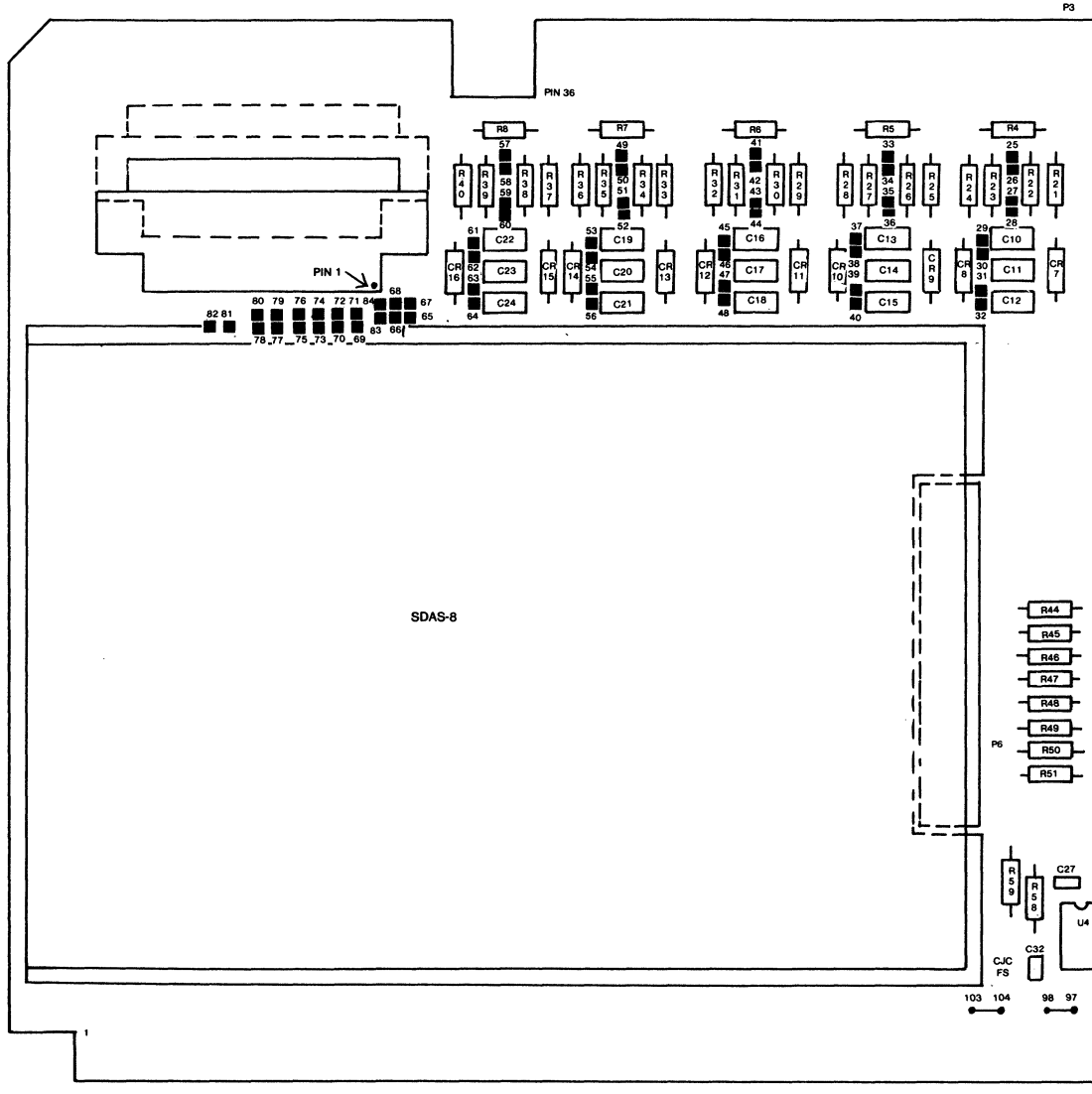
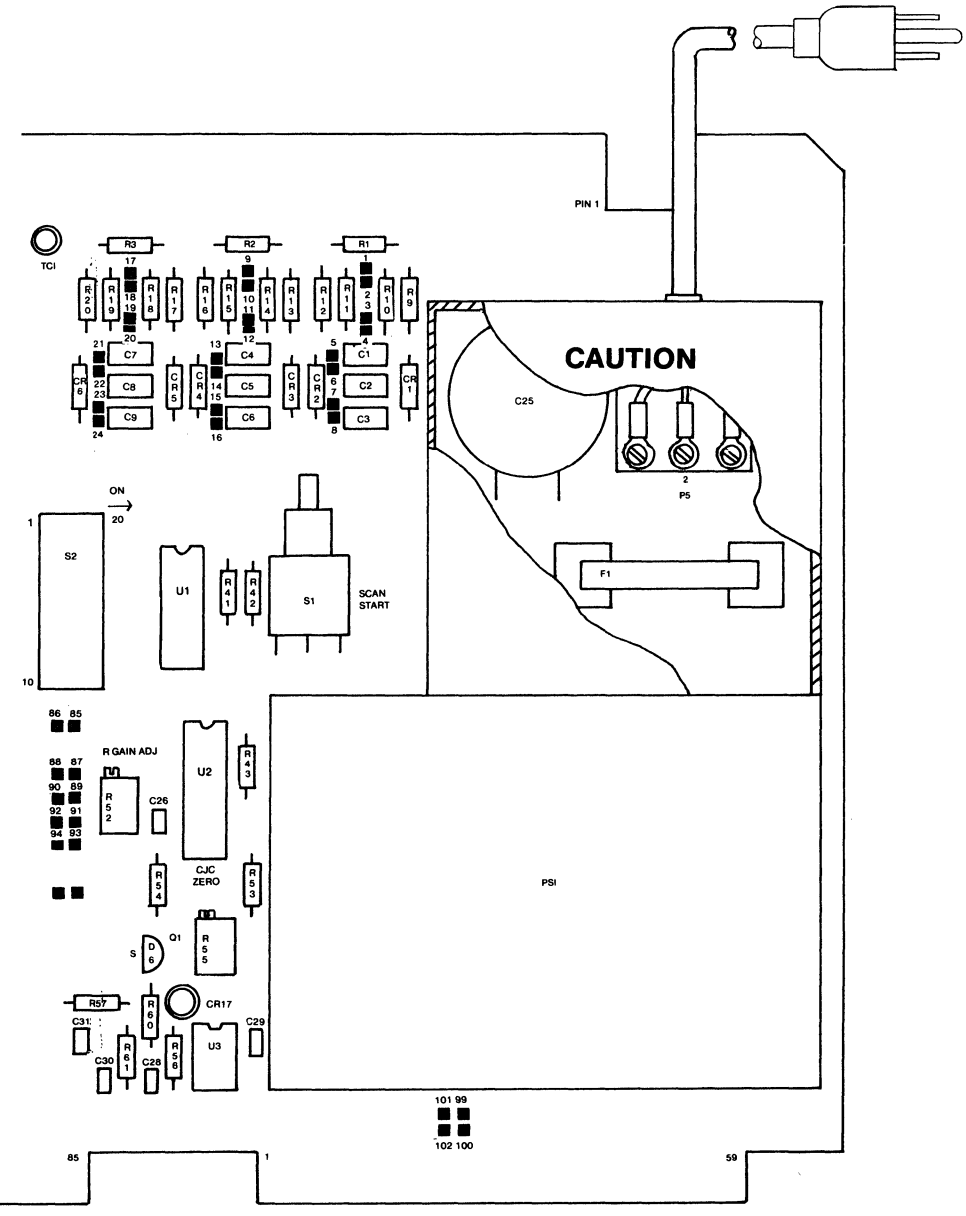
CIRCUIT BOARD COMPONENT LOCATIONS

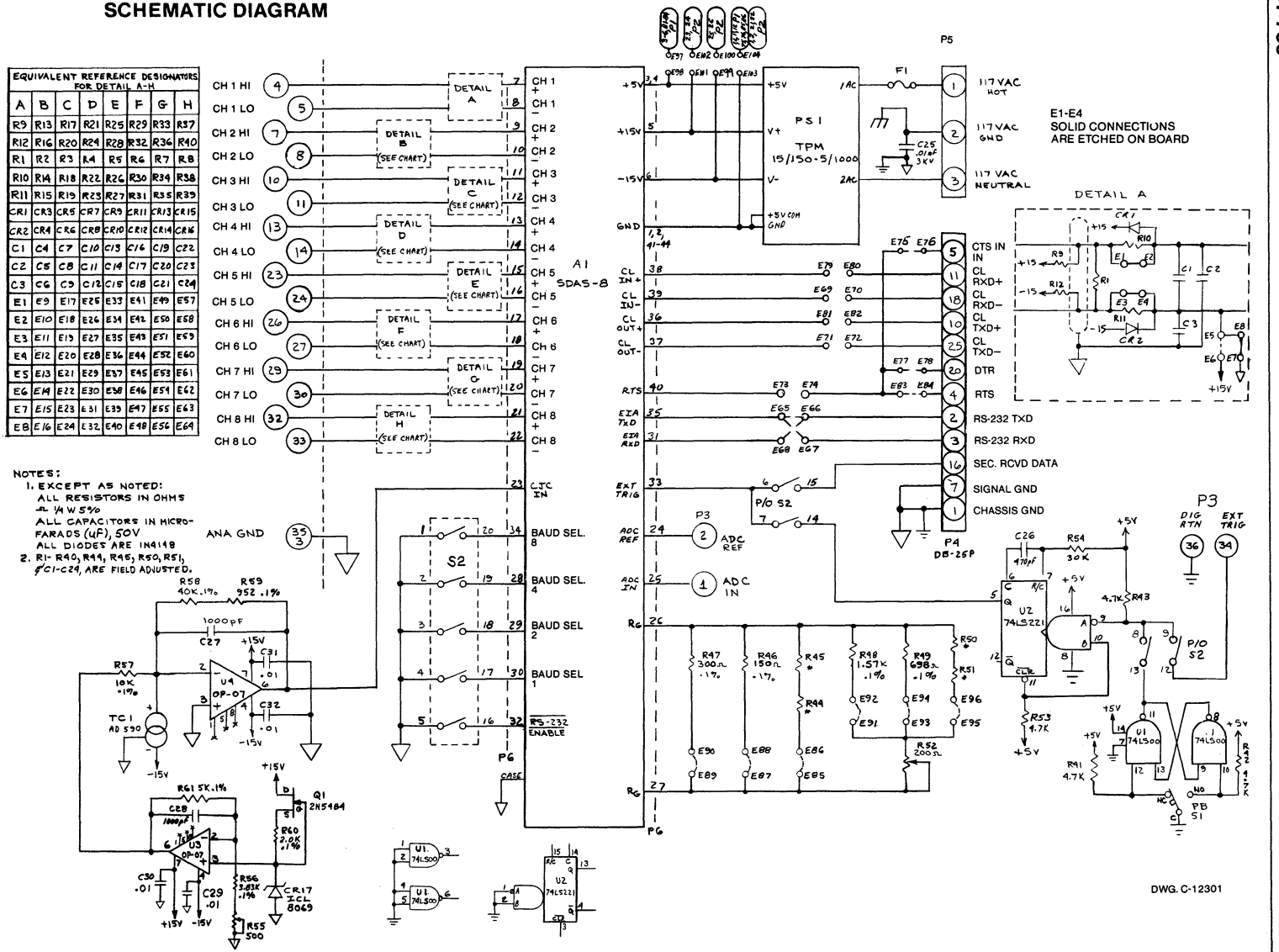



PIN 1
TCI
R3
R2
R1
CAUTION
C25
P5
ON
S2
U1
S1
SCAN
START
F1
R GAIN ADJ
U2
C26
C/C
ZERO
PSI
Q1
CR17
C29
C30
C28
U3
101 99
102 100
85
1
59

D-12300

11-97

SCHEMATIC DIAGRAM



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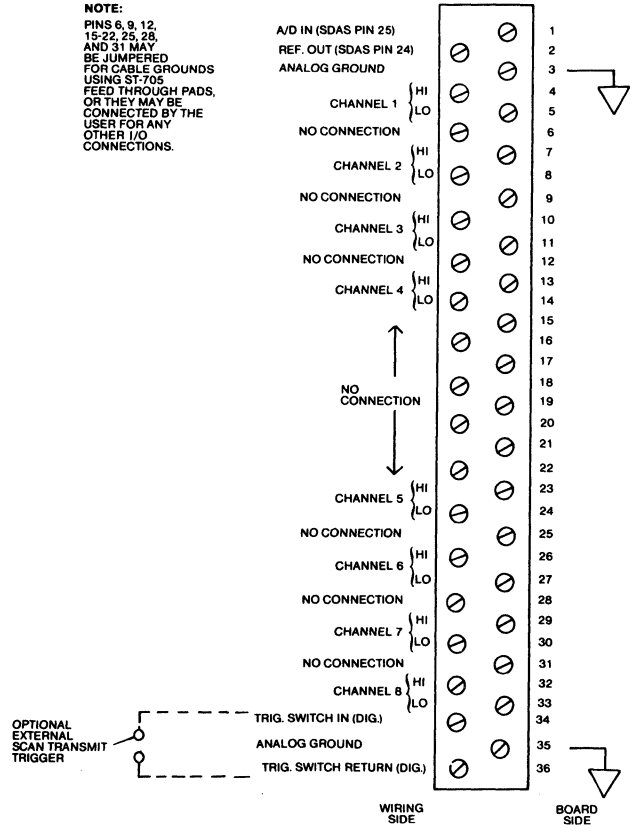
DETACHABLE ANALOG SIGNAL INPUT CONNECTOR, P3



POWERING THE ST-705X FROM MULTIBUS

As an alternate mounting method, users may install model ST-705X in a low-cost MULTIBUS card cage. Although no digital connections are made to MULTIBUS, +5V power connections are standard MULTIBUS. Some computers include +/−15Vdc power supplies at the standard P2 locations shown. If preferred, a separate isolated 5 and 15 volt DC supply may be bussed along MULTIBUS to drive one or more ST-705X's in multidrop.

(Caution: This is for the ST-705X only, which omits the AC isolated power supply. Using DC power from a MULTIBUS host may no longer be isolated, causing safety, damage and data error difficulties).

MULTIBUS regulated DC power	Close jumpers	Power supplied through
+5Vdc @ 500mA	E97-E98	P1 pins 3-6, 81-84
+15Vdc @ 50mA	E101-E102	P2 pins 23, 24
−15Vdc @ 50mA	E99-E100	P2 pins 25, 26
Power Return	E103-E104	P1 pins 1, 2, 11, 12 75, 76, 85, 86 P2 pins 1, 2, 21, 22

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BAUD RATE SELECTION

SDAS-8 PIN = (34 BAUD 8 SEL) (28 BAUD 4 SEL) (29 BAUD 2 SEL) (30 BAUD 1 SEL)

BAUD RATE	S2 DIPSWITCH =	1	2	3	4
75		1	0	0	1
150		1	0	0	0
300		0	1	1	1
600		0	1	1	0
1200		0	1	0	1
2400		0	1	0	0
4800		0	0	1	1
9600		0	0	1	0

ON = "0", OFF = "1"

S2 GROUNDS SELECTED PIN

PROGRAMMABLE GAIN AMPLIFIER

Usage	Gain	Jumper	Notes
Type J & K Thermocouples	× 80	Close E89-E90 E91-E92 Only	Trim Full Scale Gain with R52
Type S & T Thermocouples	× 160	Close E-87-E88 E93-E94 Only	Trim Full Scale Gain with R52
User-selected Gain	R Gain = 20KΩ÷ (Gain-1)	Close E85-E86 E95-E96 Only	Install Resistors at R45, R44 with Trims at R50, R51. Choose low resistor Tempco to avoid degrading accuracy.

LOCALLY-TRIGGERED SCAN TRANSMISSION

INPUT TYPE	INPUT CONNECTIONS	DIP SWITCH S2 (Close=ON, Open=OFF)
10 Microsecond positive TTL Pulse	P4: input, pin 16 ground, pin 7	Close S2 SW.6 Open S2 SW.7
Switch closure to ground. (P3, PIN 34 includes a 4.7 Kilohm pullup to +5V)	P3: switch, pin 34 return, pin 36	Open S2 SW.6 Close S2 SW.7 Open S2 SW.8 Close S2 SW.9
ST-705 on-board pushbutton S1	None	Open S2 SW.6 Close S2 SW.7 Close S2 SW.8 Open S2 SW.9

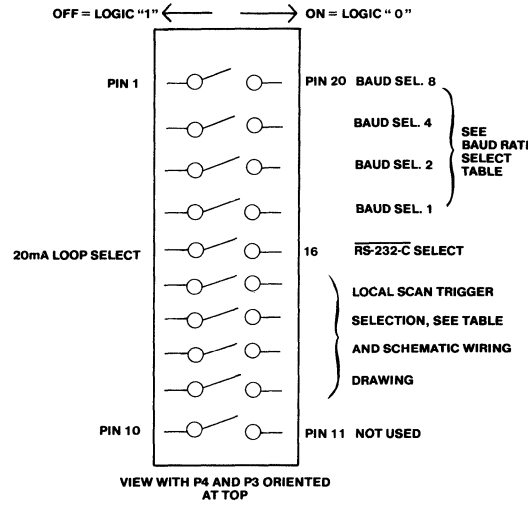
SERIAL CHARACTER FORMATS RECEIVED

START BIT	DATA BITS (LSB first)	PARITY BIT	STOP Bit(s)
1	7	None	2
1	7	Odd, Even, ϕ* or 1	1
1	8	None	1

*Upper case ASCII characters transmitted from ST-705 set data bit 7 equal to logic 0.

ST-705 doesn't care about received character parity.

DIPSWITCH, S2



A/D CODING TABLE

Input Volts (R GAIN = ∞ no connection)	Hexadecimal Display*	Decimal Display
+4.096V	+++++	+++++
+4.095 V	0FFFH	+4.095
+2.048V	0800H	+2.048
+1.024V	0400H	+1.024
+0.256V	0100H	+0.256
+0.002	0010H	+0.002
+0.001	0001H	+0.001
0.000	0000H	+0.000
−0.001	FFFFH	−0.001
−0.002	FFFEH	−0.002
−0.256V	FF00H	−0.256
−1.024V	FC00H	−1.024
−2.048V	F800H	−2.048
−4.095V	F001H	−4.095
−4.096V	-----	-----

*In hex, the polarity bit 12 has been extended to the top 3 MSB's (Bits 13, 14 15)

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SERIAL COMMAND SUMMARY

LEGEND:

1. XXX — X are characters entered and displayed on the terminal.
2. ( ) are blind control characters (such as carriage return or escape) which do not appear on the terminal.
3. Carriage return (CR) requests the SDAS-8 to execute the command consisting of the previous character string. Terminate all commands with "Return" or "Enter".
4. The asterisk (*) confirms that the command was executed, and is ready for the next command.
5. The pound sign (#) indicates that the returned character string is not executable. Re-enter a corrected string.

COMMAND EXAMPLES

* — Power-up prompt. Previous command executed; ready for next command
# — Echoed string not executable; try again
G(CR) — Display status message
B(CR) — Display time (HR:MIN:SEC)
B23:59:59(CR) — Set time in 24 hour format
(Escape) — Reset all controls to power-up status except clock
(DEL or backspace) — Delete previous character for editing before execution
(Control S or DC3 or XOFF) — [13HEX] Stop transmission immediate and wait
(Control Q or DC1 or XON) — [11HEX] Start transmission immediate, mid string
R — Stop output transmission from SDAS-8. Stop L mode auto-start timer. (CR) not required. Revert to trigger or polled-start mode.

A/D CONTROLS

X(CR) — Display one scan
M:2(CR) — Set up to display channel 2 only
M:1,8(CR) — Set up to display channels 1-8
L02(CR) — Start automatic scan transmissions every 2 seconds. R or (ESC) are the only way to stop L mode.
L59:59(CR) — Start automatic scan transmissions every 59 minutes: 59 seconds
L17:59:59(CR) — Start automatic scan transmissions every 17:59:59 hours:minutes/seconds (max.)
H(CR) — Format A/D data as hexadecimal ASCII
D(CR) — Format A/D data as decimal ASCII (cancel hex)
V(CR) — Format A/D data as DC volts, (cancel thermocouple)
J(CR) — Format A/D data linearized to selected thermocouple
K(CR)
S(CR)
T(CR)
A(CR) — Transmit A/D data from CJC channel, equivalent ambient temperature. Range +/−99°C.
F(CR) — Format A/D data as Fahrenheit
C(CR) — Format A/D data as Celsius

TERMINAL CONTROLS

W(CR) — Toggles between rubout echo as BS-SP-BS or /X where X is the last character
P80(CR) — Set column width to 20, 40, 48, 72, 80 or 132 (20 = power up state)
E(CR) — Echo all printables (power up state) for full duplex
Q(CR) — Don't echo printables (for half duplex)
Nnnn(CR) — Insert nnn nulls between, CR, NULL's, LF, (Range ϕ -254)
N255(CR) — Suppress line feed. End all scans with CR, (NULL's), no line feed. N255 (CR) is a toggle, which cycles on and off with each application. Confirm the line feed status bit using the G status.
I:nnn - n(CR) — Start all A/D scans with the Ident character string nnn - n (20 characters max)
Cancel with I:(CR)
All lower case printables - Echo if selected. Not acted upon.
All non-specified controls - Echo if selected. Not acted upon.
BN(CR) — Delete time and station
BY(CR) — Resume time and station

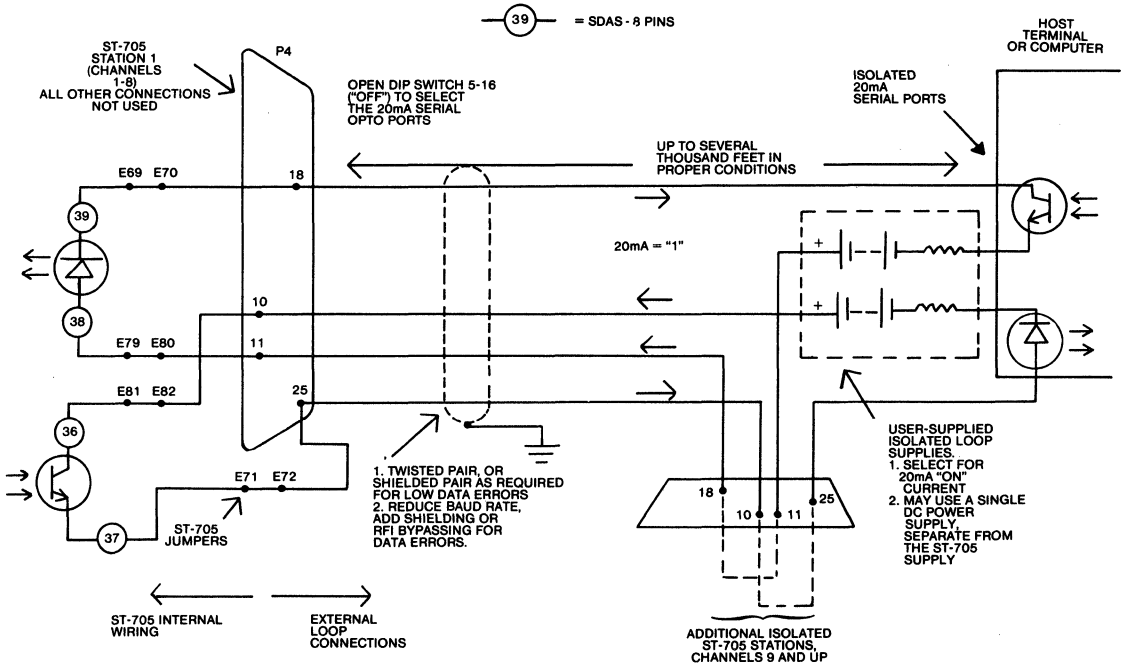
POWER UP MODE

Station 1
20 characters per line
Trigger/polled scan start
8 channels, 1-8
Echo on
Elapsed time from power-on
The line terminator sequence at power up is:
<CR, NUL, NUL, - (216 NUL's), no LF>

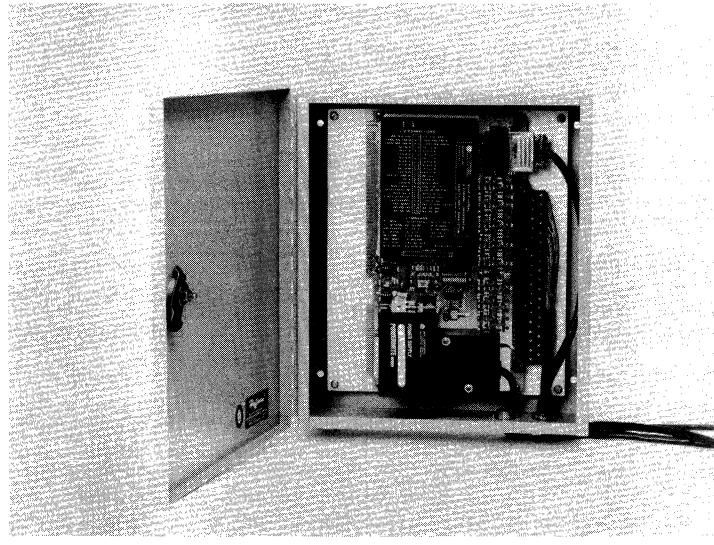
VERY IMPORTANT
For CRT's, send ESCAPE first to cancel the NUL's and restore LF.

11

TYPICAL 20mA ISOLOOP MULTIDROP WIRING



TYPICAL ST-705 MOUNTING IN A NEMA HOUSING



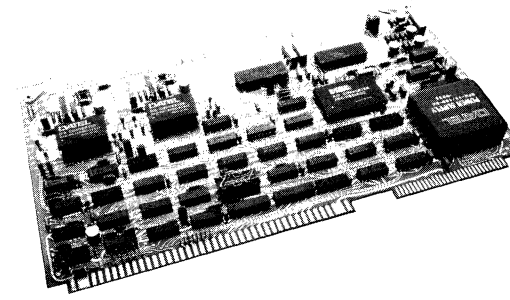
SineTrac ST-711,ST-732
32 A/D, 2 D/A Channel Analog Boards for MULTIBUS Microcomputers

FEATURES

- **Model ST-711: 32S A/D Channels, no D/A Channels**
- **Model ST-732: 32S/16D A/D Channels, Includes 2 D/A Channels plus current loop outputs**

BOTH MODELS INCLUDE:

- **Full mechanical, electrical, and pinout compatibility to Datel's iSBC711/732 Analog I/O Boards and Datel's ST-711RLY Board.**
- **Operates with all MULTIBUS and iSBC-Series compatible microcomputers using 16, 20 or 24-bit addressing, 8-bit data transfer.**
- **Works directly from Datel's RMX-80 Analog I/O Driver operating software.**
- **Includes an 10-stage jumper-selected, program-gatable pacer start clock, 1 mS to 1 sec., crystal-controlled.**
- **A/D input accept up to 16 user-installed shunts for 4-20 mA etc., current inputs.**
- **FET-Input differential amplifier accepts on-board resistor for fixed high gain up to X1000 (10 mV full scale range).**
- **Includes Programmable Gain Amplifier (X1, 2, 4, 8 gains).**



GENERAL DESCRIPTION

The Sine-Trac ST-711 and ST-732 A/D-D/A Analog Input/Output systems extend Datel's SineTrac family concept of slide-in peripheral boards for popular mini-and-micro-computers. The ST-711 and ST-732 interface to the growing Datel's Single Board Computer (SBC) Series and other Multibus-compatible micro-computers. The iSBC has multiple sources and has been proposed as an ANSI standard. The ST-711/732 also interfaces to the 16-bit iSBC-86/12 from Datel which also uses MULTIBUS, thus insuring present and future product compatibility for the user.

Models ST-711 and ST-732 are second generation combination A/D-D/A peripheral board systems for the iSBC-80 only boards and they feature functional, hardware and programming differences to the ST-800 by adding 2 D/A converters plus current loop amplifiers (ST-732 only) without sacrificing the high A/D channel density of 32 single-ended or 16 differential channels per board. Other important differences include memory-mapped interfacing (vs. conventional register transfer I/O for the ST-800), addition of a FET input programmable differential amplifier (with optional high gain operation), a jumper-programmed, 10-stage crystal Pacer clock and complete pin-for-pin form, fit, and function identity to competitive iSBC-711/732 series A/D-D/A board systems. This last feature allows Datel's ST-711/732 to operate directly from Datel's RMX-80 Analog I/O Drivers (Real-time Multitasking Executive Software.).

Hardware differences include the change from an MDAS-16 data acquisition module on the ST-800 to a hybrid ADC-HS combined A/D converter and Sample/Hold Amplifier on the ST-711/732. Substantial addressing, register and DMA logic is saved on the ST-711/732, making room for the D/A's, current amplifiers, and Pacer clock.

ORDERING GUIDE	
ST-711	32 S/16D A/D, D/A
ST-732	32 S/16D A/D, 2 D/A Loops

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INTRODUCTION

The ST-711 is a full analog input system only (use Model ST-732 for D/A outputs) including either 32 single-ended A/D input channels (standard) or 16 differential channels (jumper change). The ST-711 includes the DC/DC Power Converter to supply all on-board ±15 V dc requirements, Programmable Gain Amplifier (X1, 2, 4, 8 gains) with optional (added resistor) gain selection up to X100 (.10mV full scale range). Also included is a 10-stage jumper-selected crystal Pacer clock, selectable base memory address, jumper-selected End of Conversion (EOC), End of Scan (EOS) and Pacer Clock/External Start Interrupts (external TTL A/D conversion starts are software-gatable). Up to 16 differential channels contain pads to accept user-installed shunt resistors for 4-20 mA, 1-5 mA, 10-50 mA and other current input ranges.

For conversion control, the ST-711 includes on-board registers to store start and final A/D channel address, status bits, conversion modes and interrupt enables.

An A/D Converter auto-increment mode, which is program-selected, automatically advances the channel address after each conversion. Successive A/D samples will continue until the program-selected last channel address is reached.

The ST-732 is identical to the ST-711; both include two 12-

ST-711/732 COMPARISON TO ST-800

MODEL	NO. A/D CHANS.	A/D CHANS EXPANSION	A/D THRUPUT RATE	PROG. GAIN AMPL.	HI-GAIN DIFF. AMPL. & RANGES	CURRENT LOOP OUTPUTS	CLOCK	EXTERNAL START	INTERFACE TYPE
ST-711 (No D/A)	32S/16D	Must use additional 711 boards with different base addresses. Indefinite expansion	23,000 Samples/sec	Included X1, 2, 4, 8	User-option, up to X1000 (10mV FSR)	None, use 732 board.	Included, 10-stage bin. devider 1mS to 1 sec, Stal or jumper-select. Starts A/D	Included, gatable starts A/D Conv.	Memory-mapped 16 reserved locations, any base 16m
ST-732 (2 D/A's)	"	"	"	"	"	2 Chans. Incl. 4-20 Loops Incl.		"	"
ST-800 (No D/A)	16S, 8D, 32S or 16D	Up to 256S/12D using ST-800ADX Boards	35,000 Samples/sec. (DMA Mode)	No	No	None	None	RC adj. one-shot start clk. Set status bit or interrupt	Register Transefer Program or interrupt I/O

MODEL	DC/DC POWERA	NOTES	INTERRUPTS	COMPATIBLE COMPUTERS	OPERATING SOFTWARE	IDENTICAL PIN-OUTS REGISTER BITS TO COMPET. MODELS	DIAGNOSTIC TAPE PROGRAM	DMA
ST-711 (No D/A)	Included	Uses ADC-HS Combined A/D Converter and Sample/Hold. Stores Start & Final Chan. Addr.	End of conversion End of Scan Pacer clk. 2 of 3 may be wired to INTAA, INTB or 8 Multibus interrupts	iSBC-80/05 iSBC-80-10 iSBC-80-20 iSBC-80-30 iSBC-80-20 (-4) iSBC-86/12 & Multibus compatible omputers	RMX-80 Analog I/O Drivers (Diagnostic Supplied)	iSBC-711 iSBC-732	Includes program listing in manual	No
ST-732 (No D/A)	"	"	"	"	"	"	"	"
ST-800 (No D/A)	Included	Uses MDAS-16 Data Acquisition Module	EOC, EOS, Start Clock. May be wired to any of 8 Multibus Interrupts	iSBC-80/05 iSBC-80/10 iSBC-80/20 iSBC-80/30 iSBC-80/20 (-4) iSBC-86/12 & Multibus Compatible computers	None (Diagnostic Supplied)	None	Includes program listing in manual	Yes, requires Datel's DMA controller board

bit hybrid DAC-HK D/A converters with input registers. Also included with each D/A converter is a current loop output amplifier with unipolar range of 4 to 20 mA, which is compatible with industrial process transceivers and is especially suited to driving long cables in noisy, industrial applications.

DESCRIPTION

The A/D section of the ST-711/732 used Datel's hybrid technology ADC-H12B combined successive approximation A/D converter and Sample/Hold Amplifier. The ADC-HS features 5 µsec S/H acquisition time and 8 µsec A/D conversion time and 12 bit binary resolution. System accuracy varies from ±0.5% of FSR ±1/2 LSB (10V range) to ±.03% FSR ±1/2 LSB (10 mV range), including noise, quantization, nonlinearity and dynamic errors. The ST-711/732 employ Datel's MX-1606 series fast CMOS multiplexers which incorporate ±35V overvoltage protection. Input impedance is 100 meg-ohms minimum (power on) with 30 pA typical input bias current. Balanced inputs require 5 kilohms maximum source impedance to maintain accuracy and throughput rate.

All models include an FET input differential amplifier which is wired as single-ended for the 32-channel models. This amplifier will accept a fixed resistor to increase the gain to 100, making 10 millivolt full scale ranges practical. For differential inputs, the common mode noise rejection varies from 120 dB at dc with a gain of 8 to 60 Hz with a gain of 1000. Sample/Hold aperature delay time is 100 nanoseconds, maximum.

System temperature coefficients are ±25 ppm of FSR/°C (gain drift of gain = 1) and ±20 µV°C (RTI) zero drift. Amplifier settling time is 8 microseconds (high level) and typically 110 microseconds (low level). Overall system throughput rate for high level signals is 23,000 samples per second.

The standard A/D-D/A digital coding is offset binary (bipolar) but jumpers may easily be changed to straight binary (unipolar) or 2's complement (bipolar). Standard A/D-D/A analog signal ranges are +10V full scale but may be jumper selected to ±5V, or +5V, or 10V unipolar.

D/A outputs include operational amplifiers for voltage outputs, giving very low output impedance (2/10's of an ohm) at 5 mA short circuit proof output current. D/A settling time is 4 µS (Fs pk-pk change). Output temperature drift is ±50 ppm to FSR/°C. 4 to 20 mA current loop outputs accept a 15 to 30V dc voltage compliance with ±0.075% FSR accuracy and ±50 ppm FSR/°C drift.

SPECIFICATIONS, MODELS ST-711/732

(Typical at 25°C, dynamic conditions, unless noted)

GENERAL

Configurations Available

Model ST-711
32S/16D A/D Chans, No D/A Channels

Model ST-732
32S/16 A/D Chans, 2 D/A Channels

ANALOG INPUTS

Number of Channels
32 single-ended or 16 differential
(Jumper-selected, 32S suplied standard)

Channel Expansion
May expand indenfinitely by using additional ST-711/732 boards with different base address. Expansion limited by board slots and power.

Input Type
With impedance voltage input, non-isolated. Differential inputs are balanced.

Current Inputs
Up to 16 differential voltage inputs may be converted to differential current inputs with shunt resistors provided and installed by the user. Pads on the board will accomodate 4-20 mA, 1-5 mA, 10-50 mA and other ranges. 4-20 mA ranges require 250-ohm, 1/4W ±1% resistors, +100 ppm/°C max.

Input Overvoltage
±35V sustained (no damage)

Input Capacitance to Ground
5 pF - Off channels, 100 pF - On channels

Full Scale Input Ranges
±10V, ±5V ±2.5V, ±1.25V (supplied standard, selectable by 2-bit programmable gain code). Board pads are etched for the user to install a fixed gain resistor, providing down to ±10 mV full scale range.

Programmable Gain Amplifier
Supplied, X1, X2, X4, X8 gains (see ranges above). Fixed high gain X1000 optional (see above)

Input Impedance.
100 megohms min., differential or to ground (power on)
1.5 kilohms min. (power off)

Input Source Resistance
5K ohms max. (balanced)
1K ohms max. (unbalanced)

Input Bias Current
30 pA typ., 200 pA max.

Overall Accuracy at +25°C
(including 3-sigma noise and quantization error, dynamic response errors, referred to input, after initial calibration)

GAIN	ACCURACY
X1	±0.05% FSR ±1/2 LSB
X2	±0.07% FSR ±1/2 LSB
X4	±0.07% FSR ±1/2 LSB
X8	±0.07% FSR ±1/2 LSB
X100*	±0.1% FSR ±1/2 LSB
X1000*	±0.3% FSR ±1/2 LSB

*Requires rewiring diff. ampl. for fixed high gain

Common Mode Voltage Range
Within ±12V of analog common (signal plus common mode)
Common Mode Rejection
At Gain = 1
0 Hz 100 dB
100 Hz 80 dB
1 KHZ 60 dB

At Gain = 8
0 Hz 120 dB
100 Hz 100 dB
1 KHZ 80 dB

At Gain = 1000 (Requires rewiring diff. ampl. for fixed high gain)
60 Hz 100 dB
Nonlinearity ±1/2 LSB
Differential Nonlinearity ±1/2 LSB
Resolution 12 binary bits (1 part in 4096)
Multiplexer Crosstalk From Off Channels 0.01% max.
Sample/Hold Switch Feed Through 0.01% max.
Sample/Hold Aperture Time
100 nanoseconds, max.
System Temperature Coefficients
Gain
±25 ppm of FSR/°C (Gain X1)
±30 ppm of FSR/°C (Gain X2, 4, 8)
Zero
±20µV/°C
A/D Conversion Period 20 microseconds
Amplifier Settling Time
(Input = ±FSR pk-pk step)
8 microseconds (HL)
110 microseconds (LL)
System Throughput Rate
(High Level Inputs)
23,000 samples/seconds
A/D Digital Outputs
Offsset binary (bipolar) - Supplied standard
Two's complement (bipolar) } Rewired with jumpers by user
Straight Binary (unipolar) }
Output Data Format
12 bit binary group compatible to SBC-Series computers. The A/D Bit 1 (MSB) may be inverted by jumper to 2's complement coding.

ANALOG OUTPUTS (ST-732 only)
VOLTAGE OUTPUTS
Number of Channels
2 non-isolated
Full Scale voltage Output Ranges

0 to +5V	Jumpers may be rewired
0 to +10V	by the user or by Datel
-5 to +5V	in OEM quantities
-10 to +10V	(Supplied Standard)

Digital Input Coding

Straight binary	Jumpers may be rewired by the user or by Datel in OEM quantities
2's Complement	

Offset Binary (Supplied standard)
Output Impedance 200 milliohms
Output Current ±5 mA, short circuit proof to ground
Slew Rate 10V/µS (with no Ext. Cap. Load)
SettlingTime
4 microseconds to within ±1/2 LSB of final value
Accuracy at +25°C ±50 ppm of FSR/°C

CURRENT LOOP OUTPUTS
Full Scale Current Output Range
4 to 20 mA, unipolar. (May be rewired to other ranges by the user.)
Current Loop Load Resistance 0 to 500 ohms
Current Loop Voltage Compliance
18 to 30V dc, unipolar, provided by the user
Accuracy at +25°C ±50 ppm of FSR/°C

PHYSICAL
Outline Dimensions
12W X 6.75D X 0.5H inches*
(305 X 171 X 13 mm)
Pin-for-pin and card guide compatible to the Multibus SBC-Series computers
Weight 22 ounces (0.6 kg)
Operating Temperature Range 0 to +55°C
Storage Temperature Range -25°C to +85°C
Relative Humidity 10% to 90%, non-condensing
Altitude 0 to 15,000 feet (4600 m)

POWER CONSUMPTION
+5V dc ±5% @ 2.5 Amps. max
An on-board DC/DC Power Converter operated from +5V, is provided to supply regulated ±15V for linear circuits.
Programming and Architecture Type of Interface
Memory-mapped interface
The ST-711/732 appears to the CPU as 16 consecutive memory locations with 4 unused locations
Compatibility
Pin-for-pin and card guide compatible to the Multibus, SBC-Series computers
Compatible Software
RMX-80 Analog I/O Drivers
ASM-80 8080 Assembly Language
Compatible Computers:
iSBC-80/10
iSBC-80/05
iSBC-80/20
iSBC-80/20 (-4)
iSBC-80/30
iSBC-86/12
Data Transfer - 8 bits DØ/-D7/

*Cards may be stacked adjacent if standard 0.60" spacing cages are used.

MEMORY ADDRESS ASSIGNMENTS (All addresses in hex)

New Addr.	Datel Supplied	Command	Function
M+0	ØØF7ØØ	Write	Load Command Register
M+0	ØØF7ØØ	Read	Read Status Register
M+1	ØØF7Ø1	Write	Load RGA and Ch. Addr. Register
M+1	ØØF7Ø1	Read	Read PGA and Ch. Addr. Register
M+2	ØØF7Ø2	Write	Load Last Chan. Addr, Register
M+3	ØØF7Ø3	Write	Clear Interrupts
M+4	ØØF7Ø4	Read	Read A/D Data LO Byte
M+5	ØØF7Ø5	Read	Read A/D Data HI Byte
M+8	ØØF7Ø8	Write	DACo LO ByteÆ Hid, Reg.
M+9	ØØF7Ø9	Write	DACo HI ByteÆ DACo (HRÆDACo)
M+A	ØØF7ØA	Write	DAC1 LO ByteÆ Hid. Reg.
M+B	ØØF7ØB	Write	DAC 1 HI ByteÆ DAC 1 (HRÆDAC 1)
CÆF	ØØF7ØC/F & ØØF7Ø6/7		Don't Use

M must be on 16-byte boundaries (A2/-AØ/ = Ø)

CLEAR INTERRUPTS (WRITE ØØF7Ø3)

Bits	Function
7, 6	Not Used
5	0 = Clear EOC Interrupt
4	0 = Clear EOS Interrupt
3	0 = Clear Pacer Clk. Interrupt
2, 1, 0	Not Used

Transfer Acknowledge Delay

The ST-711/732 responds with a Transfer Acknowledge (XACK) with any Read or Write Command. The XACK may be delayed to suit different processors. 16 delay steps are jumper-selected from 50 nS to 1.5 µS. Standard units are set to 50 nS.

Pacer Clock

Adjustable time-base consisting of a 10-stage binary divider capable of starting A/D conversions in the External Trigger Mode. Time-base periods are jumper-selected and the oscillator may be either crystal or RC controlled. The standard range is 97 µS to 1 second.

Interrupts

2 of 3 possible interrupts may be jumper-selected to one or both (INTA and INTB) interrupt lines. The interrupts are EOC, EOS and Pacer Clock. They are factory-jumpered as: INT A - EOS, INT B - EOC. Additionally, any of the 8 Multibus interrupts may be wired to any combination of the EOC, EOS Pacer Interrupts.

A/D CONTROL ADDRESSES

LOAD COMMAND REGISTER (WRITE ØØF7ØØ)

Bits	Function
7	Not Used
6	Not Used
5	1 = Enable End of Convert (EOC) Interrupt
4	1 = Enable End of Scan (EOS) Interrupt
3	0 = Clear Board Busy Status
2	1 = Enable External Trigger
1	1 = Enable Automatic Ch. Addr. Increment
0	1 = Enable A/D Conversion

READ STATUS REGISTER (READ ØØF7ØØ)

Bits	Function
7	1 = A/D Conversion Done
6	1 = Scan Done
5	1 = EOC Interrupt Enabled
4	1 = EOS Interrupt Enabled
3	1 = Board is Busy
2	1 = External Trigger Enabled
1	1 = Auto-increment Enabled
0	1 = A/D Conversion Enabled

READ/LOAD PGA DNA START CHAN. ADDR. A/D (READ WRITE ØØF7Ø1)

Bits	Function	
7, 6	00 = Gain X1 01 = Gain X2 10 = Gain X4 11 = Gain X8	
5	Not Used	
4	$1 = 2^4$	Start Chan. Addr. Select (1 of 32)
3	$1 = 2^3$	
2	$1 = 2^2$	
1	$1 = 2^1$	
	$1 = 2^0$	

LOAD A/D LAST CHANNEL ADDRESS (WRITE ØØF7Ø2)

Bits	Function	
7, 6, 5	Not Used	
4	$1 = 2^4$	Last Chan. Addr. Select (1 of 32)
3	$1 = 2^3$	
2	$1 = 2^2$	
1	$1 = 2^1$	
0	$1 = 2^0$	

D/A COMMANDS

LOAD HOLD REGISTER with DAC LO Byte D/A (WriteØØF7Ø8 DAC0, Write ØØF7ØA-DAC1)

Bits	Function
7	DAC Bit 9
6	DAC Bit 10
5	DAC Bit 11
4	DAC Bit 12 (LSB)
3, 2, 1, 0	Zeros

LOAD HI BYTE TO DAC; Load Hold Reg. to DAC (Write ØØF7Ø9 DAC0, WriteØØF7ØB-DAC1) Enable DAC Input Register Strobe

Bits	Function*
7	DAC Bit 1 (MSB)
6	DAC Bit 2
5	DAC Bit 3
4	DAC Bit 4
3	DAC Bit 5
2	DAC Bit 6
1	DAC Bit 7
0	DAC Bit 8

*A/D-D/A convention is to label the converter's Most Significant Bit as Number 1 (MSB). (Note that D/A addressing is mapped continuous to A/D addressing).

A/D DATA ADDRESSES

READ A/D DATA HI BYTE (Read ØØF7Ø5)

Bits	Function
7	ADC Bit 1 (MSB)
6	ADC Bit 2
'	'
'	'
'	'
0	ADC Bit 8

READ A/D DATE LO BYTE (Read ØØF7Ø4)

Bits	Function
7	ADC Bit 9
6	ADC Bit 10
5	ADC Bit 11
4	ADC Bit 12 (LSB)
3, 2, 1, 0	Not Used

INTERFACE CONNECTORS

Programmable Gain	Unipolar		Bipolar		Low Level Unipolar	Low Level Bipolar
X1	0 +5V	0 +10V	±5V	±10V	Up to +80 mV	Up to ±1V
X2	0 +2.5V	0 +5V	±2.5V	±5V	Up to +40 mV	Up to ±500mV
X4	0 +1.25V	0 +2.5V	±1.25V	±2.5V	Up to +20 mV	Up to ±200mV
X8	0 +675 mV	0 +1.25	±675mV	±1.25V	Up to +10 mV	Up to ±100mV

(Standard, Offset Binary)

Selected by on-board jumpers

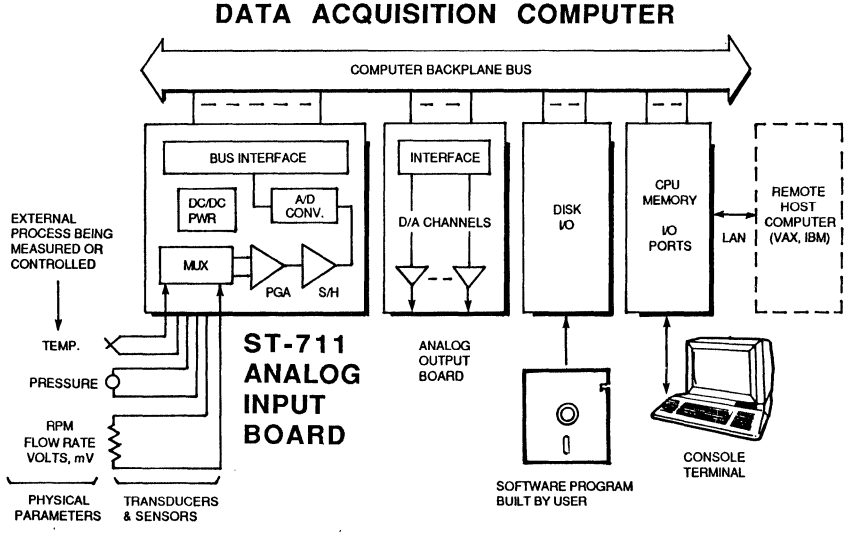
Requires substitution by user of fixed gain resistor on the on-board differential amplifier

Memory Base Address

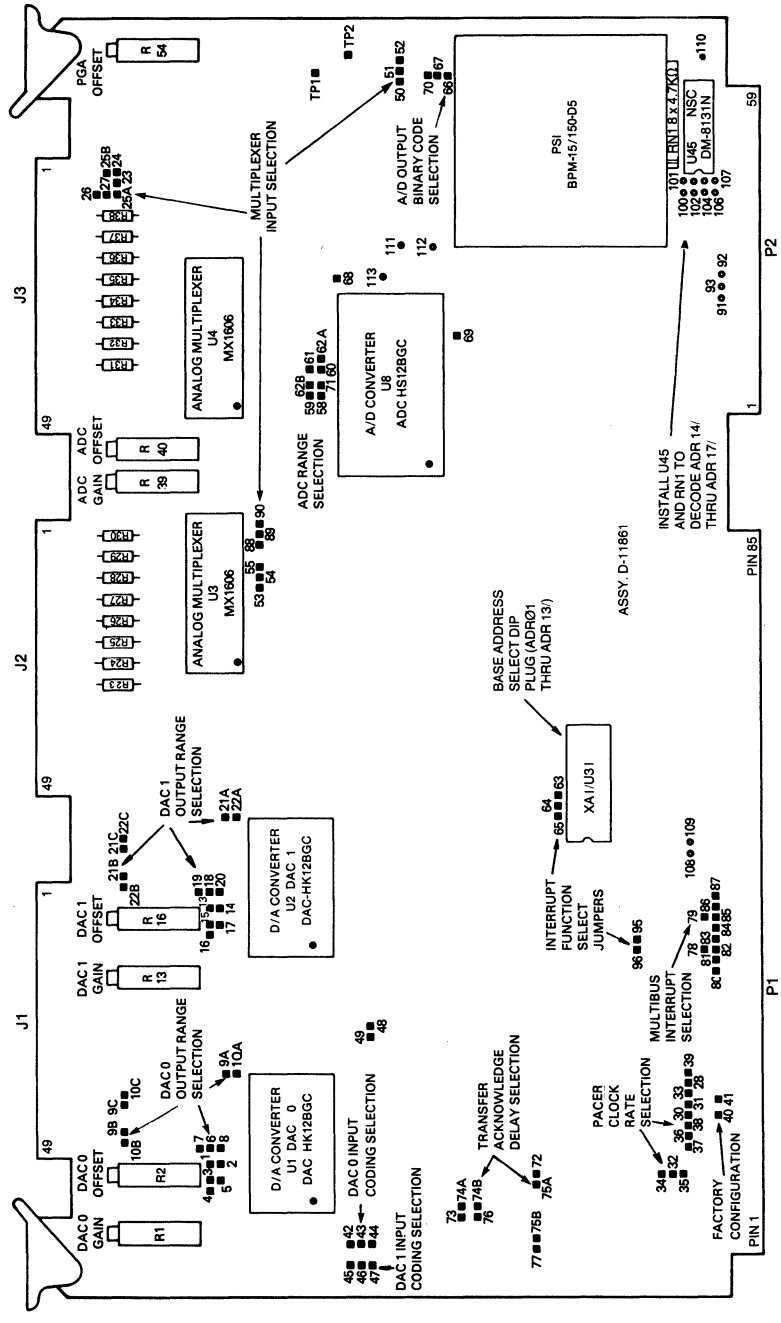
The 16-location starting base address is factory set at ØØF7ØØ (hex) but may be reassigned on 16-byte boundries (LSB = Ø) by altering a supplied DIP jumper plug. However, the supplied diagnostic program is preset to operate from base address ØØF7ØØH.

INTERFACE CONNECTORS

DESIG.	FUNCTION	NO. OF PINS	PIN SPACING CENTERS (IN)	MATING RIBBON CONNECTORS
P1	SBC Multiabus Bus Connector	86	0.156	
P2	±15V Aux. Power (Bus)	60	0.1	
J1	2 D/A Analog Outpput Channels	50	01	58-2076061
J2	1st 8D/16S A/D Input Channels	50	01	58-2076061
J3	2nd 8D/16S A/D Input Channels	50	01	58-2076061



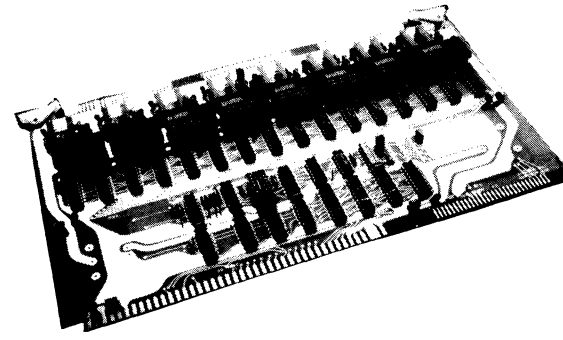
ST-711/732 BOARD LAYOUT



SineTrac ST-716
16-Bit D/A Board for MULTIBUS ISBC-80 Microcomputers

FEATURES

- **4 or 8 D/A channels, 16-bit resolution**
- **Compatible with both 8- and 16-bit CPU's (8- or 16-bit data transfer)**
- **Accurate to 0.005% of Full-Scale reading**
- **Complete hardware and software compatibility with MULTIBUS and ISBC-Series microcomputers**
- **24-bit addressing**
- **Memory-mapped, with user-selectable base address**
- **Three user-selectable output ranges available: ±5 V dc, 0 to +10 V dc, and ±10 V dc**
- **Selectable Transfer Acknowledge delay (XACK/) ensures compatibility with different memory speeds**



DATEL'S SineTrac ST-716 D/A BOARD PROVIDES END USERS AND OEM's WITH A MEANS OF PRODUCING HIGH RESOLUTION ANALOG OUTPUTS FROM THEIR MULTIBUS AND ISBC MICROCOMPUTERS, WITH 16 BITS OF RESOLUTION, THIS BOARD IS AN IDEAL CHOICE FOR PRECISION SERVO CONTROL AND SIMILAR APPLICATIONS.

GENERAL DESCRIPTION

The ST-716 provides 4 or 8 channels of digital-to-analog (D/A) conversion with 16 bits of resolution. Overall accuracy is within .005% of full scale reading. Voltage range outputs are jumper-selectable to ensure the board's compatibility with popular process control and test instrumentation.

Like other SineTrac products, the ST-716 is fully hardware and software compatible with its host ISBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built in. The user simply slides the ST-716 into an Intel-compatible card cage and wires the analog outputs. The ST-716 is then ready as a memory-mapped D/A peripheral. It is addressed by the host computer as 16 consecutive memory locations with a user-defined base address. This memory-mapped format permits virtually unlimited D/A channel expansion by using multiple ST-716's, each with a different base address.

A systems manual is shipped with each board, providing installation instructions, theory of operation, and engineering drawings.

Figure 1 is a simplified block diagram of the ST-716, with the 8 D/A channel circuitry for Model ST-716D shown within dashed lines. The ST-716 is pin-compatible with DATEL's ST-724, ST-728, ISBC-724, and ISBC-728 analog output boards. The 4-channel ST-716's are software-compatible with the ST-724's and ST-728's while the 8-channel ST-716's are software-compatible with the ST-728's.

Data inputs to the ST-716 are from the host computer's bus. Input coding is offset binary.

Each channel uses a DATEL Model DAC-HP16B (or DAC-HP16B-1), a 16-bit hybrid device which offers linearity to ±0.003% of Full-Scale reading. The output of the converter is monotonic to 14 bits between +10°C and +40°C. Offset error on each channel has been adjusted to zero prior to shipping the boards. Trim pots on the board permit recalibration of zero (or offset) and range setting. The converter settles in 15μS to within ±0.005% of FSR. Zero tempco is ±5 ppm of FSR/°C, and gain tempco is within ±20 ppm of FSR/°C.

The board's base address is factory set at 0F710. However, the user may relocate the board's address anywhere up to FFFF0 by rewiring a 20-pin DIP plug supplied with the board. The user may also extend the addressing to a full 24 bits by soldering jumpers into holes provided on the board adding four more bits. This would extend the addressing capability to FFFFF0 hex.

In order to make the ST-716 compatible with different speed CPU and memory systems, a Transfer Acknowledge delay (XACK/Delay) circuit is provided. The user enables 16 jumper-selectable delays from .05 to 1.5 microseconds.

The ST-716 is fully bus, card cage, and software compatible with the MULTIBUS. The board is 12″W x 6.75″D x 0.5″H (305 x 172 x 13 mm). Multiple ST-716 boards can mount in adjacent card slots when used with a standard, .60″ spacing Intel card cage. The ST-716C and ST-716D draw all their power from the MULTIBUS +5V line.

An on-board dc-to-dc converter provides the ±15V to drive the board analog output circuits. The St-716 weighs approximately 11.2 ounces (0,318 kg). It can operate over a temperature range of 0 to +55°C with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4600m) in altitude.

Refer to Figure 2 for information regarding the location of all user-selectable jumpers for addressing, XACK/Delay, and output range selection.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

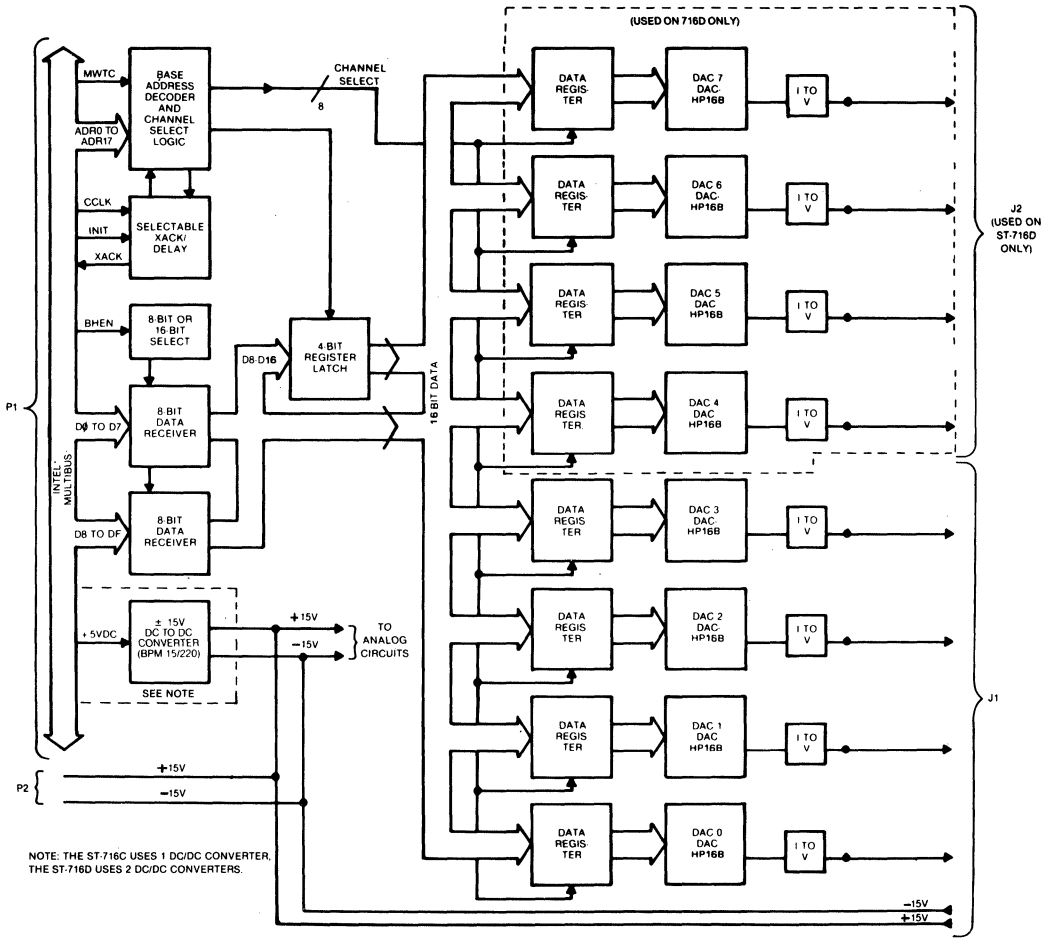


Figure 1. ST-716 Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25°C, unless otherwise specified)

D/A ANALOG OUTPUT

Number of Channels
ST-716C . . . . . 4 D/A Channels with on-board dc-to-dc converter.
ST716D . . . . . 8 D/A channels with 2 on-board dc-to-dc converters.

Full Scale Output Ranges . . . . . ±5V, 0 to +10, ±10V dc
Digital Input Coding . . . . Offset Binary
Output Impedance . . . . . 50 Milliohms
Maximum Current Available on Voltage Outputs . . ±5 mA

Data Register Memory Mapping . . . . . Reserves a block of 16 consecutive memory locations

PERFORMANCE

Accuracy at +25°C . . . . . ±0.005% of FSR (includes noise and nonlinearity)
Setting Time . . . . . 10V change, 26 µSec. (to 0.005% FSR)
Power Supply Rejection . . ±0.002% FSR/%
Monotonicity . . . . . To 14 bits over +10°C to +40°C temp Range
Zero Temperature Drift (Unipolar Output Only) . . . Within ±5 ppm of FSR/°C
Offset Temperature Drift (Bipolar Output Only) . . ±8 ppm of FSR/°C
Gain Temperature Drift . . . Within ±20 ppm of FSR/°C

POWER CONSUMPTION

(From MULTIBUS +5 V dc, no load)

ST-716C . . . . . 2.0 Amps, typical
ST-716D . . . . . 4.2 Amps, typical

FUNCTIONAL SPECIFICATIONS (cont.)

PHYSICAL

Outline Dimensions . . . . . 12.00"W x 6.75"D x 0.50"H (304,8 x 171,5 x 12,7 mm) ST-716 boards may be installed adjacent to each other in SBC card cages with 0.60" spacing
Weight . . . . . 11.2 ounces (0,318 kg)
Operating Temperature Range . . . . . 0 to +55°C
Relative Humidity . . . . . 10% to 95%, non-condensing
Altitude . . . . . 0 to 15,000 ft.

SELECTION OF 8-BIT OR 16-BIT CPU's

The ST-716 board automatically changes to a 16-bit format when the BHEN/line on the MULTIBUS goes to zero volts (pin 27 of connector P1). A high input on BHEN/, consequently, sets the ST-716 for the 8-bit format.

DATA FORMAT

The ST-716 requires 16 bits of digital data, input from the host computer, for a single digital-to-analog (D/A) conversion. Table 1 indicates how 8-bit and 16-bit CPU's format this data.

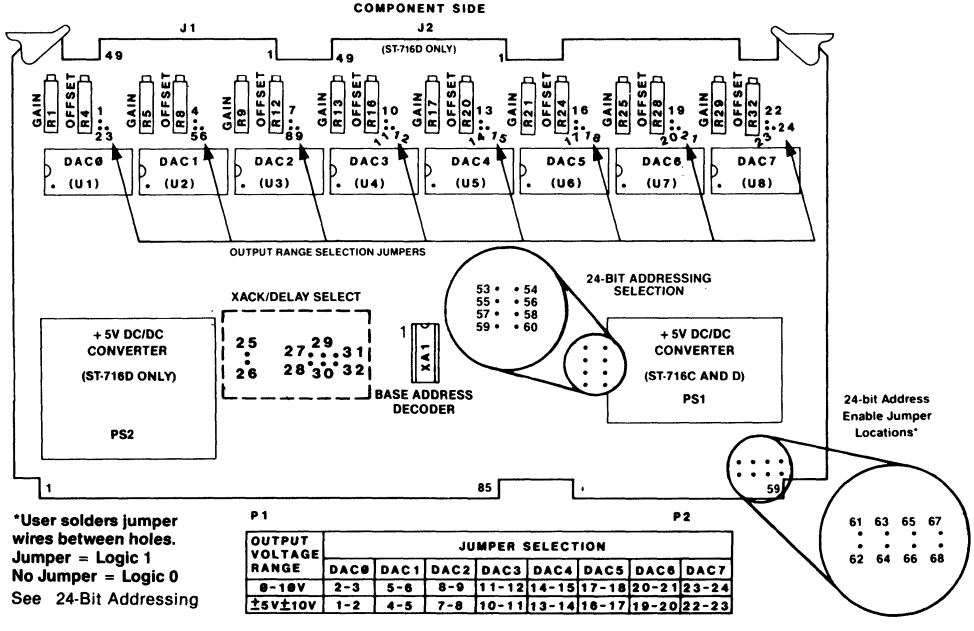
Note that 8-bit CPU's must transmit the 16 data bits in two bytes. The low byte contains the 8 least significant data bits; these are stored in a data register on the ST-716. The high byte contains the remaining 8 data bits. When the host transmits the high byte containing the 8 MSB's, the data register places the 8 LSB's also onto the selected DAC's input. Digital to-analog conversion then begins. Data transfer with a 16-bit CPU is somewhat simpler. All 16 data bits are transmitted as a single word. Data is loaded directly into the selected DAC, and a D/A conversion takes place.

Table 1. Data Formats for 8- or 16-Bit CPU's

SINGLE WORD, 16-BIT CPU	
HIGH BYTE (8-BIT CPU) BASE + 1,3,5,7,9,B,D, or F	LOW BYTE (8-BIT CPU) BASE + 0, 2,4,6,8,A,C, or E
D15 D14 D13 D12 D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0
↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑	↑ ↑ ↑ ↑ ↑ ↑ ↑ ↑
DAC DATA 1 (MSB) DAC DATA 2 DAC DATA 3 DAC DATA 4 DAC DATA 5 DAC DATA 6 DAC DATA 7 DAC DATA 8	DAC DATA 9 DAC DATA 10 DAC DATA 11 DAC DATA 12 DAC DATA 13 DAC DATA 14 DAC DATA 15 DAC DATA 16 (LSB)

ST-716 REGISTER ASSIGNMENTS

Table 2 details the memory address assignments of the 16 memory locations the ST-716 occupies. Please note that when the ST-716 is used with 16-bit CPU's, every other (even-numbered) address location is used.



*User solders jumper wires between holes.
Jumper = Logic 1
No Jumper = Logic 0
See 24-Bit Addressing

OUTPUT VOLTAGE RANGE	JUMPER SELECTION							
	DAC0	DAC1	DAC2	DAC3	DAC4	DAC5	DAC6	DAC7
0-10V	2-3	5-6	8-9	11-12	14-15	17-18	20-21	23-24
±5V±10V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23

Figure 2. ST-716 Board Layout Drawing

BASE ADDRESS SELECTION

NOTE: The ST-716 may be used with both 8- and 16-bit microprocessors. Bits 10, 11, 12 and 13 are used or 20-bit addressing. Full 24-bit addressing would use these bits and address bits 14, 15, 16 and 17.

Use Table 3 as a worksheet to assign the base address.

Table 2. ST-716 Register Assignments

MEMORY ADDRESS (8-BIT CPU'S)	FUNC-TION	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-BIT) CPU'S
BASE + 0	WRITE	Output LSB Byte for DAC 0 (Channel 0)	
BASE + 1	WRITE	Output MSB Byte for DAC 0 (Channel 0)	BASE + 0)
BASE + 2	WRITE	Output LSB Byte for DAC 1 (Channel 1)	
BASE + 3	WRITE	Output MSB Byte for DAC 1 (Channel 1)	BASE + 2
BASE + 4	WRITE	Output LSB Byte for DAC 2 (Channel 2)	
BASE + 5	WRITE	Output MSB Byte for DAC 2 (Channel 2)	BASE + 4
BASE + 6	WRITE	Output LSB Byte for DAC 3 (Channel 3)	
BASE + 7	WRITE	Output MSB Byte for DAC 3 (Channel 3)	BASE + 6
BASE + 8	WRITE	Output LSB Byte for DAC 4 (Channel 4)	
BASE + 9	WRITE	Output MSB Byte for DAC 4 (Channel 4)	BASE + 8
BASE + A	WRITE	Output LSB Byte for DAC 5 (Channel 5)	
BASE + B	WRITE	Output MSB Byte for DAC 5 (Channel 5)	BASE + A
BASE + C	WRITE	Output LSB Byte for DAC 6 (Channel 6)	
BASE + D	WRITE	Output MSB Byte for DAC 6 (Channel 6)	BASE + C
BASE + E	WRITE	Output LSB Byte for DAC 7 (Channel 7)	BASE + E
BASE + F	WRITE	Output MSB Byte for DAC 7 (Channel 7)	

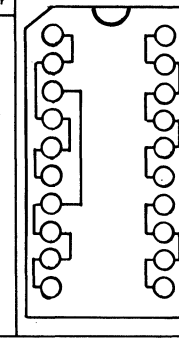
Procedure

1. Select a base address, in hex, between 00000X and FFFFFX. Write all but the last digit in the boxes. (The last hex digit selects the 8 D/A channels, and cannot be preset).
2. Convert the hex code to binary by writing 1's and 0's in the boxes opposite "Hex Bit Weighting".
3. To set the ST-716 for a particular base address:

   Address bits 4 through 13: Connect the "1" pins together to pin 10 or 11 and the "0" pins together to pin 1 or 16, on DIP plug XA-1.
4. Address bits 0 through 3 select the 8 D/A channels and are not shown.
5. For 16-bit processors, bits 10, 11, 12 and 13 must be tied to pin 1.
6. XA-1 is a 20-pin DIP plug. (See Table 4)
7. Full 24-Bit addressing requires soldering jumper wires between etched holes provided on the ST-716 boards. See the ST-716 board component layout diagram for the location of these holes.

Table 4. Dip Plug XA-1 Pin Assignments

Set For Base Address of 0F700H

SIGNAL	PIN #		PIN #	SIGNAL
+5V	1		20	+5V
ADR 10	2		19	ADR 4
ADR C	3		18	ADR 5
ADR 11	4		17	ADR 6
ADR 12	5		16	ADR B
ADR 13	6		15	ADR 7
ADR F	7		14	ADR 8
ADR E	8		13	ADR 9
ADR D	9		12	ADR A
GND	10		11	GND

TOP VIEW

NOTES:

1. Address inputs to the ST-716 are low true. Tie pins to ground (Pin 10 or 11) for logic 1; tie them to +5V. (Pin 1 or 20) for a logic 0.
2. Etch holes exist on the board to assign logic levels to the additional four bits. Refer to the component layout diagram for the location of these holes.

Table 3. Base Address Selection

24-bit Addressing

20-bit Addressing

16-bit Addressing

BASE ADDRESS (HEX)	0 to F	0 to F	0 to F	0 to F	0 to F	x
HEX BIT WEIGHTING	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	•
ADDRESS BIT # HEX	17 16 15 14	13 12 11 10	F E D C	B A 9 8	7 6 5 4	
XA-1-PIN #'s/JUMPERS	NOT APPLICABLE SEE NOTE 1	Pin 6 Pin 5 Pin 4 Pin 2	Pin 7 Pin 8 Pin 9 Pin 3	Pin 16 Pin 12 Pin 13 Pin 14	Pin 15 Pin 17 Pin 18 Pin 19	

NOTES

1. Address bits 14, 15, 16 and 17 are enabled by placing jumpers across etched holes provided on the printed wiring board. See '24-Bit Addressing'
2. Boards are factory set for a base address of 00F10 hex.

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-716 board generates a Transfer Acknowledge (XACK/) signal in response to write commands from the host computer. It is sometimes desirable to delay this signal, in order to match the XACK/ signal to the host computer timing. The ST-716 has a jumper-selectable Transfer Acknowledge Delay (XACK/delay) ranging from 50 nanoseconds to 1.5 microseconds.

The accuracy of the XACK/delay is dependent in part on the duty cycle of the CCLK/signal generated by the computer, shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

Please refer to Table 5 for jumper configurations yielding different delay times.

OUTPUT RANGE CODING SELECTION

Datel ships the ST-716 boards with the full-scale output ranges configured as follows:

ST-716C1	± 5V dc
ST-716D1	0 to +10V dc
ST-716C2, D2	±10V dc

The particular jumper connections for individual DAC's appear in Table 6.

Tables 7 and 8 show the signals present on the output connectors of the ST-716.

Table 5. XACK/Delay Selection

DELAY µsec	JUMPERS		
*0.05	—	—	—
0.1	31-32	—	—
0.2	—	25-26	—
0.3	31-32	25-26	—
0.4	—	—	27-28
0.5	31-32	—	27-38
0.6	—	25-26	27-28
0.7	31-32	25-26	27-28
0.8	—	—	—
0.9	31-32	—	—
1.0	—	25-26	—
1.1	31-32	25-26	—
1.2	—	—	27-28
1.3	31-32	—	27-28
1.4	—	25-26	27-28
1.5	31-32	25-26	27-28

*Factory supplied configurations

Table 6. ST-716 Output Range Selection Jumpers

MODEL	RANGE	DAC 0	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6	DAC 7
ST-716C2 ST-716D2	± 10V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23
ST-716C1	± 5V	1-2	4-5	7-8	10-11	13-14	16-17	19-20	22-23
ST-716D1	0 to + 10V	2-3	5-6	8-9	11-12	14-15	17-18	20-21	22-24

Table 7. J1 Analog Output Connections

WIRING SIDE	PIN #'S		COMPONENT SIDE
N/C	2	1	N/C
N/C	4	3	N/C
N/C	6	5	N/C
N/C	8	7	N/C
N/C	10	9	N/C
N/C	12	11	N/C
N/C	14	13	N/C
N/C	16	15	N/C
N/C	18	17	N/C
N/C	20	19	N/C
N/C	22	21	N/C
DAC 3, V OUT	24	23	DAC 3, ANA RTN
N/C	26	25	N/C
N/C	28	27	GND
DAC 2, V OUT	30	29	DAC 2, ANA RTN
N/C	32	31	N/C
N/C	34	33	GND
DAC 1, V OUT	36	35	DAC 1, ANA RTN
N/C	38	37	N/C
N/C	40	39	GND
DAC 0, V OUT	42	41	DAC 0, ANA RTN
N/C	44	43	N/C
N/C	46	45	GND
POWER COMMON	48	47	POWER COMMON
– 15V POWER[1]	50	49	+ 15V POWER[1]

NOTE: Pins 49 and 50 are outputs; 1 mA maximum (for reference only)

Table 8. J2 Analog Output Connections

WIRING SIDE	PIN #'S		COMPONENT SIDE
N/C	2	1	N/C
N/C	4	3	N/C
N/C	6	5	N/C
N/C	8	7	N/C
N/C	10	9	N/C
N/C	12	11	N/C
N/C	14	13	N/C
N/C	16	15	N/C
N/C	18	17	N/C
N/C	20	19	N/C
N/C	22	21	N/C
DAC 7, V OUT	24	23	DAC 7, ANA RTN
N/C	26	25	N/C
N/C	28	27	GND
DAC 6, V OUT	30	29	DAC 6, ANA RTN
N/C	32	31	N/C
N/C	34	33	GND
DAC 5, V OUT	36	35	DAC 5, ANA RTN
N/C	38	37	N/C
N/C	40	39	GND
DAC 4, V OUT	42	41	DAC 4, ANA RTN
N/C	44	43	N/C
N/C	46	45	GND
POWER COMMON	48	47	POWER COMMON
– 15V POWER[2]	50	49	+ 15V POWER[2]

NOTES:

1. J2 not used on 4 channel versions of ST-716.
2. Pins 49 and 50 are outputs; 1 mA maximum (for reference only)

24-BIT-ADDRESSING

For 16 or 20-bit addressing, Remove jumpers 53 through 68. For 24-bit addressing, install jumpers 61 to 62, 63 to 64, 65 to 66 and 67 to 68. Also install the following according to the desired address:

Address bit:	A17/	A16/	A15/	A14/
Jumper:	59-60	57-58	55-56	53-54

OPEN = "O", CLOSED = "1"

ORDERING INFORMATION

MODEL

ST-716 ___ ___

- 1- ±5V dc, or 0 to +10V dc Output
- 2- ±10V dc Output

___

- C-4 D/A Channels
- D-8 D/A Channels

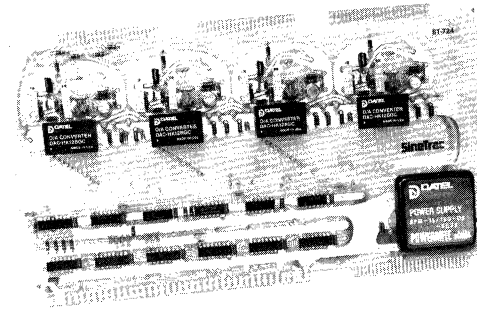
ACCESSORIES

Part Number	Description
31-20760040	Edge Connector for J1, J2, (Two supplied)

SineTrac™ ST-724
4-Channel D/A and Current Loop Board for MULTIBUS Microcomputers

FEATURES

- **4 D/A channels using 12-bit Hybrid Converters with Input Registers**
- **Accurate to .05% of Full Scale Reading**
- **Memory-mapped, with user-selectable Base Address**
- **Complete hardware and software compatibility with Multibus and SBC-series Microcomputers**
- **Pin-for-pin replacement for iSBC-724. Uses identical programming and register assignments to iSBC-711/732 and ST-711/732 A/D-D/A boards**
- **Works directly from Intel RMX Software**
- **Includes 4 externally excited 4 to 20 mA industrial current loop amplifiers.**
- **Pin-selectable Transfer Acknowledge (Xack/) Delay—ensures compatibility with different memory speeds**
- **On-board DC/DC power converter generates ±15 Vdc from +5 Vdc computer bus**



COMPATIBLE TO: **iSBC-80 SERIES**
iSBC-86 SERIES

INTRODUCTION

The ST-724 Analog Output board extends DATEL's SineTrac family of slide-in computer peripherals to a variety of industrial and instrumentation applications. It provides 4 channels of D/A conversion, each with 12 binary bits of resolution for an overall accuracy to within .05% FSR. The ST-724 is fully hardware and software compatible with the popular MULTIBUS series of microcomputers—it is a pin-for-pin replacement for the iSBC-724. And, the ST-724 is significantly less expensive than other boards with comparable features.

The ST-724 is memory mapped—it appears to the host computer as eight consecutive locations in memory. The board base address is factory set to F7Ø8 but may be reassigned by the user anywhere in memory. The ST-724 also features an adjustable Transfer Acknowledge Delay (XACK/Delay). The ST-724 generates a Transfer Acknowledge signal in response to memory write commands from the system computer. The XACK/Delay circuitry permits a delay of this signal, to ensure compatibility with the host computer.

Digital inputs to the ST-724 may be set for offset binary or 2's complement (bipolar) coding or for straight binary (unipolar). Outputs from ±5V, ±10V, 0→+5V and 0→+10V DC permit the ST-724 to interface with a variety of process receivers, proportional controllers, or recorders. A 4 to 20 mA current loop is also provided which permits the board to be used in electrically noisy industrial environments. All outputs may be shorted to ground without damage.

Power to the ST-724 comes from the host computer's +5V power bus. An on-board DC-to-DC converter generates ±15V for the analog output circuitry.

DESCRIPTION

Input to the ST-724 is from the host computer data bus. Since the Intel Multibus provides only 8 binary bits of data per memory word, and the D/A converters on the ST-724 require 12 binary bits, two memory bytes are required for each conversion. The 4 least significant bits are transmitted first, (for DAC Φ, at the base memory address) and are latched into a 4-bit register. The next data byte (base address +1) contains the 8 MSB bits, and initiates a conversion.

D/A conversion is accomplished by DATEL's DAC-HK12BGC, a 12-bit hybrid unit with an input storage register and linearity to within ±½ LSB. The output of the converter is monotonic, having a differential nonlinearity of ±½ LSB maximum. Offset zero error on each channel has been adjusted to zero prior to shipping the board; pots on the board permit recalibration of zero or offset settings.

Zero temperature coefficient (unipolar outputs only) for the converter is less than ±5 ppm/°C of Full Scale Reading. Offset temperature coefficient (bipolar outputs only) is within ±10 ppm/°C of FSR. Maximum gain tempco measures ±20 ppm/°C of FSR. DAC settling time is 4 μsec maximum (to within ½ LSB of value), and slew rate is 20V/μsec.

The voltage output ranges from the ST-724 board are jumper selectable and have an output impedance of 50 milliohms. Maximum available current on the voltage outputs is ±5mA. The ST-724 also provides voltage to current converters for each of its four D/A channels.

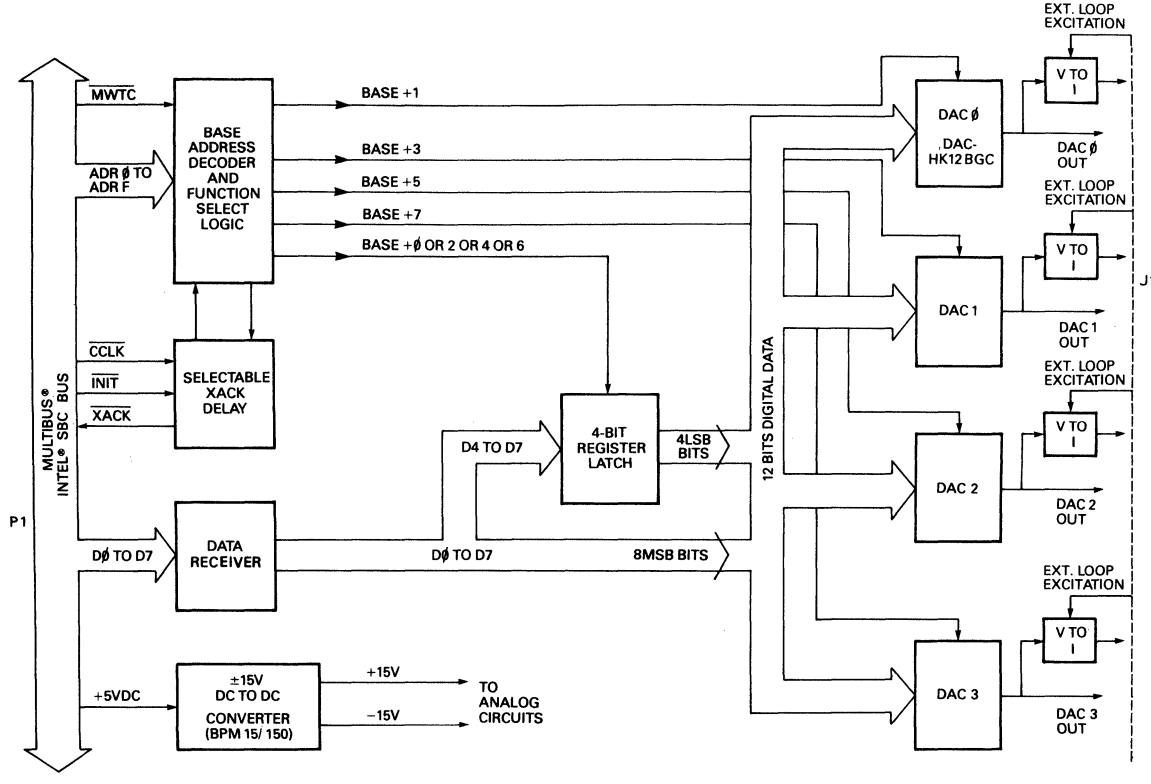
The current output option is jumper-selected by the user, and requires a user-supplied external excitation source (+18 to +30 Vdc).

The ST-724 is a memory-mapped device which occupies 8 consecutive memory locations. The starting (base) address is set at the factory to F7Ø8. However, the user may reposition this base address anywhere up to FFF8 in the host computer's memory by reconfiguring jumpers on the ST-724 board.

The selectable Transfer Acknowledge Delay Circuit (XACK/ Delay) provides 16 delays from .05 to 1.5 μsec which may be jumper-programmed by the user.

The overall size of the ST-724 is 12.0"W × 6.75"D × 0.5"H (305 × 172 × 13 mm). Multiple ST-724 boards may be installed in adjacent card slots if used in a standard (.60" spacing) Intel card cage. The ST-724 weighs 18 ounces (.51 kg). It should be operated in an ambient temperature from 0 to +55°C, with relative humidity from 10% to 95% (non-condensing), and from 0 to 15,000 ft (0 to 4600m) in altitude. The board may be stored at temperatures from −25°C to +85°C. The ST-724 is powered from the host computer bus's +5 Vdc supply, and draws 1.5A.

ST-724
BLOCK DIAGRAM
4-Channel D/A



 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SPECIFICATIONS

Typical at +25°C, dynamic conditions, unless otherwise specified

D/A ANALOG OUTPUT

Number of Channels. . 4 D/A channels

Channel Expansion. . . Indefinite channel expansion by separate, stand-alone ST-724 boards, each with a different base address; limited by available card slots, and power supply current.

Full Scale

Output Ranges. . . . . ±10V (standard) ±5V 0→+10V 0→+5V 4-20 mA (Current Loop) — Jumper Selectable by User

(The user must reassign jumpers to achieve ranges other than ±10V, offset binary)

Digital Input Coding. . . Straight Binary Offset Binary (standard) 2's Complement — Jumper Selectable by User

Output Impedance. . . . 50 Milliohms

Maximum Current Available on Voltage Outputs. . . . ±5 mA @ ±10V short-circuit-proof to ground

ADDRESSING

Reserves a block of 8 memory locations, all successive to a jumper-selectable memory base address

CURRENT LOOP EXTERNAL EXCITATION VOLTAGE

+18V to +30VDC, regulated, user-supplied. (25 mA maximum/DAC)

PERFORMANCE

Non-linearity. . . . . ±½ LSB maximum

Differential Non-linearity. . . . . ±½ LSB maximum

Offset or Zero Error. . . Adjustable to zero using pot. Each channel individually adjustable.

Zero Temperature Drift. . . . . (Unipolar Output only) Within ±5 ppm of FSR/°C

Offset Temperature Drift. . . . . (Bipolar Output only) Within ±10 ppm of FSR/°C

Gain Temperature Drift. . . . . Within ±20 ppm of FSR/°C

Settling Time. . . . . Maximum, 4 μsec to within ½ LSB of final value

Slew Rate. 20V/μsec

Power Supply Rejection. . . . . 54 dB to DC supply bus

PHYSICAL

Outline Dimensions. . . 12.00"W × 6.75"D × 0.50"H (304, 8 x 171, 5 x 12, 7 mm) ST-724 boards may be installed adjacent to each other in SBC card cages.

Weight. . . . . 18 ounces (.510 kg)

Operating Temperature Range. . . . . 0 to +55°C

Storage Temperature Range. . . . . −25°C to +85°C

Relative Humidity. . . . 10% to 95%, non-condensing

Altitude. . . . . 0 to 15,000 ft (4600m)

POWER CONSUMPTION

+5Vdc ±5/% @ 1.5A from computer bus (±15Vdc supplied from on-board DC/DC power converter.)

GENERAL

Compatibility. . . . . Pin-for-pin, cardguide, and program compatible with Multibus and SBC-series microcomputers. A pin-for-pin replacement for the SBC-724.

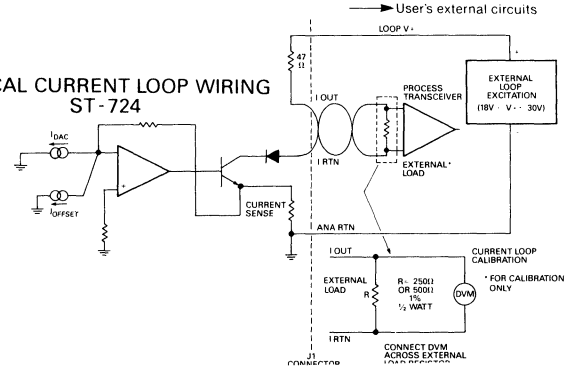
Connector . . . . . Dual 25-pin PCB, 0.1" centers

ORDERING GUIDE

MODEL	DESCRIPTION
ST-724	4 Channel, Multibus-Compatible D/A Board
31-2076040	Edge Connector, J1, Spare (One Included with Board) (PCB to solder tab)
UM-ST-724	ST-724 Manual (One Included with Board)

For 8 D/A channels, use Model ST-728.

TYPICAL CURRENT LOOP WIRING ST-724



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INPUT DATA FORMAT

Since 12-bit D/A converters are used on the ST-724, and since the Intel Multibus provides for only 8-bits of data per memory word, two 8-bit bytes in two sequential memory words are necessary for each D/A conversion.

The LS Byte is loaded onto the board first and is stored in a 4-bit register until the MS Byte is loaded. Thus, the memory location of the LS Byte is always the lower of the two locations used for a given channel. Conversion begins as soon as the MS Byte is loaded; within 4 microseconds an analog signal appears at the board's output.

LEAST SIGNIFICANT BYTE

D7	D6	D5	D4	D3	D2	D1	D0
DAC BIT 9	DAC BIT 10	DAC BIT 11	DAC BIT 12 (LSB)	X	X	X	X

MOST SIGNIFICANT BYTE

DAC BIT 1 (MSB)	DAC BIT 2	DAC BIT 3	DAC BIT 4	DAC BIT 5	DAC BIT 6	DAC BIT 7	DAC BIT 8

X = Don't care

REGISTERS

The memory address bit function assignments are as follows. For an explanation of LSB and MSB Bytes, please see "Input Data Format".

ST-724 REGISTER ASSIGNMENTS

MEMORY ADDR.	FACTORY ASSIGNED MEM. ADDR.	FUNCTION
M+Ø	F7Ø8	Output LSB Byte for DAC Ø (Channel Ø)
M+1	F7Ø9	Output MSB Byte for DAC Ø (Channel Ø)
M+2	F7ØA	Output LSB Byte for DAC 1 (Channel 1)
M+3	F7ØB	Output MSB Byte for DAC 1 (Channel 1)
M+4	F7ØC	Output LSB Byte for DAC 2 (Channel 2)
M+5	F7ØD	Output MSB Byte for DAC 2 (Channel 2)
M+6	F7ØE	Output LSB Byte for DAC 3 (Channel 3)
M+7	F7ØF	Output MSB Byte for DAC 3 (Channel 3)

D/A CALIBRATION PROCEDURE

Calibration of the ST-724 should be performed every 90 days or whenever the Analog Output Range jumpers are reconfigured. More frequent calibration may be indicated in adverse operating conditions. The Diagnostic program supplied with the ST-724 was written as part of the calibration procedure.

1. Set the board jumpers for the desired output range: 0→+5V, 0→+10V, 4→20 mA, ±5V, or ±10V. See "Output Range Selection" for details.
2. Connect a digital voltmeter (Fluke 8800A or equivalent) to the outputs of Channel Ø (DAC Ø). For voltage ranges, measure between "V OUT" and "ANA RTN". For current ranges the user must supply a precision 250Ω or 500Ω resistor; voltage measurements are then made across this resistor (see Note 1, bottom of Calibration Table).
3. Using the Diagnostic program, select the "Calibration Test", Call Key "C".
4. The teletypewriter will respond by printing out:
   CALIBRATION TEST
   CHANNEL-
5. Enter character "Ø" to select Channel Ø (DAC Ø)
   CHANNEL- Ø
   HEX DATA
6. Making reference to the Calibration Table, enter the hex code for the −Full Scale output voltage (or current), then enter a Carriage Return. Adjust the OFFSET potentiometer, until the reading on the DVM corresponds to the −Full Scale reading from the table.
7. Refer again to the Calibration Table, and enter the hex code for + Full Scale voltage or current. Adjust the GAIN potentiometer until the reading on the DVM is the + Full Scale voltage as indicated in the table.
8. Repeat steps 6 and 7.
9. Calibration for Channels 1, 2, and 3 (DAC's 1, 2 & 3) is the same as for Channel Ø.
10. The complete calibration may now be checked using the Calibration Table. Any hex value on the table may be entered followed by a carriage return. The corresponding analog output should appear on the DVM.

CALIBRATION TABLE

ANALOG OUTPUT						4-DIGIT HEX INPUT	
UNIPOLAR (STRAIGHT BINARY)				BIPOLAR (OFFSET BINARY OR 2'S COMPLEMENT		STRAIGHT OR OFFSET BINARY - NO SIGN EXTENSION	2'S COMPLEMENT WITH SIGN EXTENSION
VOLTAGE		4→20 mA CURRENT[1]					
0→+5V	0→+10V	500Ω LOAD LOOP V+>18V	250Ω LOAD LOOP V+>15V	±5V	±10V		
4.9988V	9.9976V	9.9980V	4.9990V	4.9976V	9.9951V	FFFØ	7FFØ
4.9976V	9.9951V	9.9961V	4.9980V	4.9951V	9.9902V	FFEØ	7FEØ
4.9951V	9.9902V	9.9922V	4.9961V	4.9902V	9.9805V	FFCØ	7FCØ
4.9902V	9.9805V	9.9844V	4.9922V	4.9805V	9.9609V	FF8Ø	7F8Ø
4.9805V	9.9609V	9.9687V	4.9844V	4.9609V	9.9219V	FFØØ	7FØØ
4.9609V	9.9219V	9.9375V	4.9687V	4.9219V	9.8437V	FEØØ	7EØØ
4.9219V	9.8437V	9.8750V	4.9375V	4.8437V	9.6875V	FCØØ	7CØØ
4.8437V	9.6875V	9.7500V	4.8750V	4.6875V	9.3750V	F8ØØ	78ØØ
4.6875V	9.3750V	9.5000V	4.7500V	4.3750V	8.7500V	FØØØ	7ØØØ
4.3750V	8.7500V	9.0000V	4.5000V	3.7500V	7.5000V	EØØØ	6ØØØ
3.7500V	7.5000V	8.0000V	4.0000V	2.5000V	5.0000V	CØØØ	4ØØØ
2.5000V	5.0000V	6.0000V	3.0000V	0.0000V	0.0000V	8ØØØ	ØØØØ
1.2500V	2.5000V	4.0000V	2.0000V	−2.5000V	−5.0000V	4ØØØ	CØØØ
0.6250V	1.2500V	3.0000V	1.5000V	−3.7500V	−7.5000V	2ØØØ	AØØØ
0.3125V	0.6250V	2.5000V	1.2500V	−4.3750V	−8.7500V	1ØØØ	9ØØØ
0.1563V	0.3125V	2.2500V	1.1250V	−4.6875V	−9.3750V	Ø8ØØ	88ØØ
0.0781V	0.1563V	2.1250V	1.0625V	−4.8437V	−9.6875V	Ø4ØØ	84ØØ
0.0391V	0.0781V	2.0625V	1.0312V	−4.9219V	−9.8437V	Ø2ØØ	82ØØ
0.0196V	0.0391V	2.0312V	1.0156V	−4.9609V	−9.9219V	Ø1ØØ	81ØØ
0.0098V	0.0196V	2.0156V	1.0078V	−4.9805V	−9.9609V	ØØ8Ø	8Ø8Ø
0.0049V	0.0098V	2.0078V	1.0039V	−4.9902V	−9.9805V	ØØ4Ø	8Ø4Ø
0.0024V	0.0049V	2.0039V	1.0020V	−4.9951V	−9.9902V	ØØ2Ø	8Ø2Ø
0.0012V	0.0024V	2.0020V	1.0010V	−4.9976V	−9.9951V	ØØ1Ø	8Ø1Ø
0.0000V	0.0000V	2.0000V	1.0000V	−5.0000V	−10.0000V	ØØØØ	8ØØØ

Note 1: Both the 250Ω and the 500Ω resistors (.1% precision) provide 4 to 20 mA output. The current output circuit is calibrated in terms of voltage since most digital multimeters provide greater resolution and accuracy on voltage measurements than on current.

The voltages listed are those measured across a 250Ω or a 500Ω precision resistor, connected between "I RTN" and "I OUT" on any DAC output. A user-supplied DC regulated voltage, V+ (+15V ≤ V + ≤ + 30V for 250Ω resistor, +18V ≤ V + ≤ + 30V for 500Ω resistor; 25 mA max) is required for current output and calibration, and should be connected to "V + LOOP". The supply providing V+ should be grounded at "ANA RTN".

BASE ADDRESS SELECTION

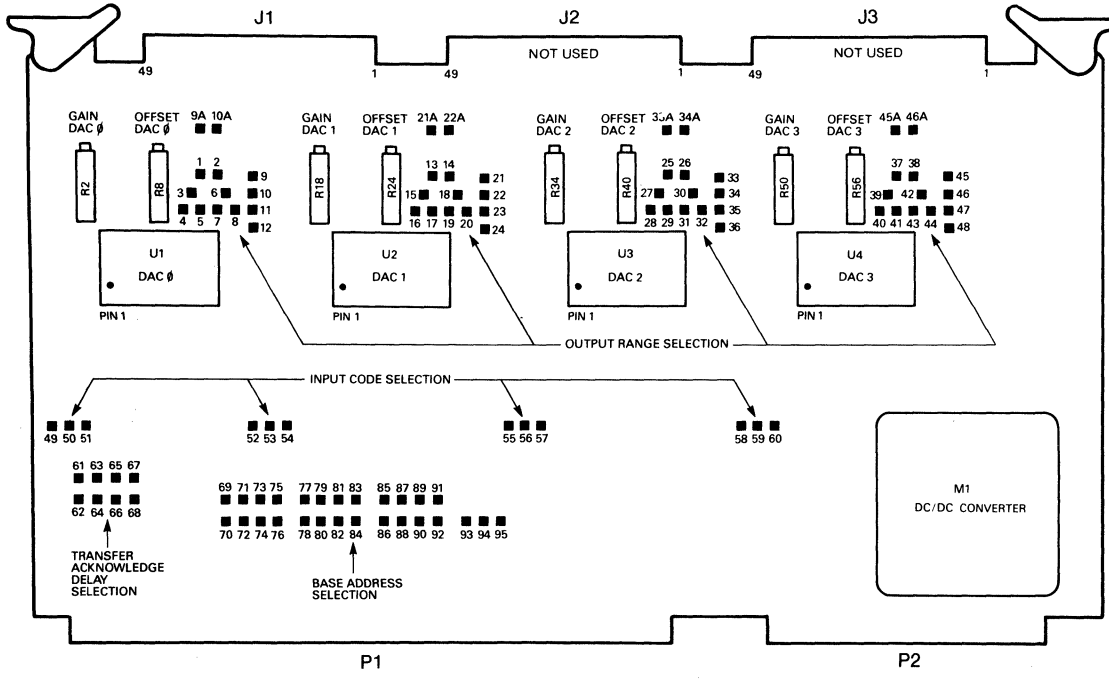
1. Select a base address, in hex, between ØØØØ and FFF8.
2. Write it in squares below opposite "Base Address, Hex".
3. Convert the hex code to binary by writing 1's and 0's in the appropriate boxes below (opposite "Hex Bit Weighting").
4. To set the base address, insert a jumper at each location opposite a "1". Please note that to obtain a "low" ("0") on bit 3, the jumper between 93 and 94 must be removed, and a jumper between 94 and 95 must be added.

BASE ADDRESS HEX	(Ø to F)				(Ø to F)				(Ø to F)				(Ø or 8)
HEX BIT WEIGHTING	8	4	2	1	8	4	2	1	8	4	2	1	8
ADDRESS BIT #	F	E	D	C	B	A	9	8	7	6	5	4	3
JUMPERS IN FOR "1", OUT FOR BIT "0"	69 to 70	71 to 72	73 to 74	75 to 76	77 to 78	79 to 80	81 to 82	83 to 84	85 to 86	87 to 88	89 to 90	91 to 92	93 to 94*

*For low on bit 3, remove 93 to 93 and add 94 to 95

BOARD LAYOUT

COMPONENT SIDE



OUTPUT RANGE AND INPUT CODING SELECTION

The ST-724's 4 D/A output channels may be set independently for any of four voltage ranges or a single current output range. Full scale ranges of ±10V, ±5V, 0→+ 10V, 0→+5V, or 4→20 mA may be jumper-selected according to the chart below. Input digital coding may be offset binary, 2's complement, or straight binary on any channel. Again, refer to the chart below for details.

The ST-724 board is normally shipped with jumpers set for the ±10V output, and an offset binary input coding. Please note that whenever there is a change in output range on a given channel, that channel should be recalibrated.

INPUT CODE SELECTION JUMPERS				
CODE	DAC Ø	DAC 1	DAC 2	DAC 3
UNIPOLAR OR OFFSET BINARY (STANDARD)	49-50	52-53	55-56	58-59
2'S COMPLEMENT	50-51	53-54	56-57	59-60

OUTPUT RANGE SELECTION JUMPERS				
RANGE	DAC Ø	DAC 1	DAC 2	DAC 3
± 10V (STANDARD)	3-5 6-7	15-17 18-19	27-29 30-31	39-41 42-43
±5 V	3-5 6-8	15-17 18-20	27-29 30-32	39-41 42-44
0 to +10V	3-4 6-8	15-16 18-20	27-28 30-32	39-40 42-44
0 to +5V	1-2 3-4 6-8	13-14 15-16 18-20	25-26 27-28 30-32	37-38 39-40 42-44
4 to 20 mA CURRENT LOOP	9-10 11-12 9A-10A	21-22 23-24 21A-22A	33-34 35-36 33A-34A	45-46 47-48 45A-46A

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-724 board generates a Transfer Acknowledge (XACK/) signal in response to Write commands from the host computer. It is sometimes desirable to delay this signal, in order to match the XACK/ signal to the host computer timing. A jumper selectable Transfer Acknowledge Delay (XACK/ delay) ranging from 50 nanoseconds to 1.5 microseconds is available in the ST-724.

The accuracy of the XACK/ delay is dependent in part on the duty cycle of the CCLK/ signal generated by the computer—shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

Please refer to the table below for jumper configurations yielding different delay times.

XACK/ DELAY SELECTION

DELAY µsec.	JUMPERS			
*0.05	—	—	—	—
0.1	61-62	—	—	—
0.2	—	63-64	—	—
0.3	61-62	63-64	—	—
0.4	—	—	65-66	—
0.5	61-62	—	65-66	—
0.6	—	63-64	65-66	—
0.7	61-62	63-64	65-66	—
0.8	—	—	—	67-68
0.9	61-62	—	—	67-68
1.0	—	63-64	—	67-68
1.1	61-62	63-64	—	67-68
1.2	—	—	65-66	67-68
1.3	61-62	—	65-66	67-68
1.4	—	63-64	65-66	67-68
1.5	61-62	63-64	65-66	67-68

*Factory supplied configuration.

ANALOG OUTPUT CONNECTIONS

J 1

ETCH SIDE	PIN #'S		COMPONENT SIDE
NC	2	1	NC
NC	4	3	NC
NC	6	5	NC
NC	8	7	NC
NC	10	9	NC
NC	12	11	NC
NC	14	13	NC
NC	16	15	NC
NC	18	17	NC
NC	20	19	NC
NC	22	21	NC
DAC 3, V OUT	24	23	NC
DAC 3, I OUT	26	25	DAC 3, I RTN
DAC 3, LOOP V + IN	28	27	DAC 3, ANA RTN
DAC 2, V OUT	30	29	NC
DAC 2, I OUT	32	31	DAC 2, I RTN
DAC 2, LOOP V + IN	34	33	DAC 2, ANA RTN
DAC 1, V OUT	36	35	NC
DAC 1, I OUT	38	37	DAC 1, I RTN
DAC 1, LOOP V + IN	40	39	DAC 1, ANA RTN
DAC Ø, V OUT	42	41	NC
DAC Ø, I OUT	44	43	DAC Ø, I RTN
DAC Ø, LOOP V + IN	46	45	DAC Ø, ANA RTN
POWER COMMON	48	47	POWER COMMON
−15 REF. VOLT. OUT*	50	49	+15 REF. VOLT. OUT*

*Not intended to power external circuitry; 1 mA max.

SineTrac ST-728
D/A Board for MULTIBUS Microcomputers

DATEL

FEATURES

- **4 or 8 D/A channels, 12 bit resolution**
- **Compatible with both 8 and 16 bit CPU's (8 or 16 bit data transfer)**
- **16, 20-, or 24-Bit addressing**
- **Accurate to 0.05% of Full Scale Reading**
- **Complete hardware and software compatibility with MULTIBUS and iSBC-Series microcomputers**
- **Memory-mapped, with user selectable Base Address**
- **Three user-selectable input data codes: Straight Binary, Offset Binary, or Two's Complement**
- **Five user-selectable output ranges: ±5V dc, ±10V dc, 0 to +5V dc, 0 to +10V dc, and 4-20 mA current loop, individually selected for each channel**
- **Selectable Transfer Acknowledge Delay (XACK/) – ensures compatibility with different memory speeds**
- **ST-728A (4 D/A channels)**
  ST-728B (8 D/A channels)
  ST-728C (4 D/A channels, DC-to-DC **converter)**
  ST-728D (8 D/A channels, DC-to-DC **converter)**

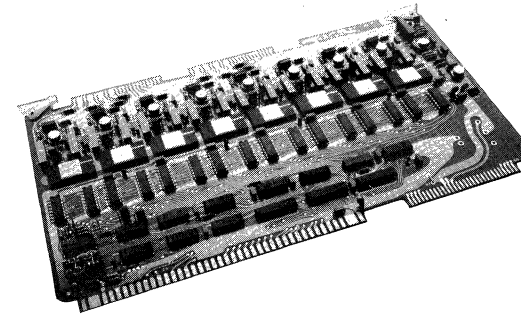
APPLICATIONS

- **Computer control of analog input chart recorders, process receivers, proportional controllers, actuators and displays**
- **Custom automatic test equipment, computer simulators, modelling systems, pattern generators, multi-channel Waveform generators**

INTRODUCTION

DATEL expands its range of MULTIBUS and SBC compatible analog output boards with the SineTrac ST-728. The ST-728 provides 4 or 8 channels of digital to analog (D/A) conversion with 12 bits of resolution. Overall accuracy is within ±.05% of full scale reading. To ensure the board's compatibility with popular process receiver, control, and test instrumentation, four voltages ranges, and a 4-20 mA current loop output are jumper selectable for each D/A channel.

Like other SineTrac products, the ST-728 is fully hardware and software compatible with its host SBC or MULTIBUS computer. All necessary address decoders, logic controls, and data receivers are built in. The user simply slides the ST-728 into an Intel compatible card cage and wires the analog outputs. The ST-728 is then ready as a memory-mapped D/A peripheral. It is addressed by the host computer as 16 consecutive memory locations with a user-locatable base address. This memory-mapped format permits unlimited D/A channel expansion by using multiple ST-728's, each with a different base address.



Compatible with: iSBC-80 Series
iSBC-86 Series

The ST-728 is pin compatible with the ST-724 and SBC-724 analog output boards (4 channel ST-728's are software compatible with ST-724's; 8-channel ST-728's look like two ST-724's). Unlike the ST-724, however, the ST-728 may be used with both 8-and 16-bit microprocessors. The BHEN/ line on the MULTIBUS sets the ST-728's address decoders and data latches for compatibility with 8- or 16-bit computers.

A systems manual is shipped with each board, which provides a source listing of the Diagnostic as well as installation instructions, theory of operation, and engineering drawings.

GENERAL DESCRIPTION

Data inputs to the ST-728 are from the host computer's bus. Input coding may be straight binary, offset binary, or two's complement, and is selected by jumper plugs on the board.

The MULTIBUS BHEN/ line is used to set the ST-728's address and data decoding for compatibility with 8 to 16 bit CPU's. In the 8 bit mode, the twelve bits of data required for D/A conversion are acquired in two bytes. The lower byte contains the four lower data bits, and is loaded into a storage register for each D/A channel on the ST-728. The next data byte contains the 8 higher bits. Upon converion, the 8 MSB's and the 4 stored bits are loaded simultaneously into the DAC. In the 16-bit mode, all twelve data bits are transferred in a single byte.

Prior to being converted, the digital data is held in a storage register. Enabling the register loads the data into the digital to analog converter (DAC), and a conversion proceeds.

Each channel uses a 12-bit monolithic D/A device which of-

 DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

fers linearity to ±1/2 LSB of full scale reading. The output of the converter is monotonic, having a differential nonlinearity of ±1/2 LSB maximum. Offset error on each channel has been adjusted to zero prior to shipping the boards. Trim pots on the board permit recalibration of zero (or offset) and range settings using the supplied Diagnostic program. The converter settles in 400 nS to within 1/2 LSB of it final value. Zero tempco is ±2 ppm of FSR/°C, and gain tempco is within ±10 ppm of FSR/°C.

The output of each DAC is fed to its own I-to-V conversion amplifier. A total of 4 voltage output ranges may be jumper-selected by the user: ±5V and ±10V bipolar; and 0 to +5V or 0 to +10V single-ended. In addition, a V to I converter circuit is included for each D/A output channel. 4-20 mA output, usable with an output load from 0 to 500 Ω, is also jumper-selectable.

The current output requires an external excitation source – a +18V to + 30V dc regulated supply, capable of 25 mA per D/A channel, must be provided. Voltage and current output ranges on the ST-728 are selected independently for each channel, permitting a mix of different voltage or current outputs on a single board.

The ST-728 is a memory-mapped peripheral occupying 16 consecutive locations in the host computer's memory. The board's base address is factory set at 0F700[1]. However, the user may relocate his address anywhere up to FFFFFØH.

In order to make the ST-728 compatible with different speed CPU and memory systems, a Transfer Acknowledge Delay (XACK/Delay) circuit is provided. 16 delays from 0.05 to 1.5 µS are jumper-selectable by the user.

The ST-728 is fully bus, card cage, and software compatible with the MULTIBUS and with Intel RMX software. The board is 12.0"W x 6.75"D x 0.5"H (305 x 172 x 13 mm). Multiple ST-728 boards may be mounted in adjacent card slots when used with a standard, 0.60" spacing Intel card cage.

The ST-728C draws all its power from the MULTIBUS +5V line. An on-board DC-to-DC converter provides the ±15 to drive the board's analog output circuits. The ST-728A and ST-728B do not have a DC-to-DC converter. They are powered from the +5V MULTIBUS line, and an external ±15V supply.

The ST-728 weighs approximately 11.2 ounces (0,318 kg). It can operate over a temperature range of 0 to +55°C with relative humidity from 10 to 90% (non-condensing), and from 0 to 15,000 feet (0 to 4600 m) in altitude.

INPUT DATA FORMAT AND REGISTER ASSIGNMENTS

DATA FORMAT

The ST-728 requires 12 bits of digital data, input from the host computer for single digital to analog (D/A) conversion. The chart below indicates how 8-bit and 16-bit CPU's format this data.

SINGLE BYTE, 16-BIT CPU	
HIGH BYTE (8-bit CPU) BASE +1, 3, 5, 7, 9, B, D, or F	LOW BYTE (8-bit CPU) BASE +2, 4, 6, 8, A, C, or E
D15 D14 D13 D12 D11 D10 D9 D8	D7 D6 D5 D4 D3 D2 D1 D0

Note that 8-bit CPU's must transit the 12 data bits in two bytes. The low byte contains the four least significant data bits: these are stored in a data register on the ST-728. The high byte contains the remaining 8 data bits. When the high byte is transmitted, all twelve bits of data - the 4 LSB's stored in a register and the 8 MSB's coming from the host computer - are loaded into the input of the selected DAC on the ST-728, and D/A conversion proceeds. Data transfer with a 16-bit CPU is somewhat simpler. All twelve data bits are transmitted in a single word. Data is loaded directly into the selected DAC, and a D/A conversion takes place.

SELECTION OF 8-BIT OR 16-BIT CPU'S

The ST-728 board automatically changes to a 16-bit format when the BHEN/ line on the MULTIBUS goes to zero volts (pin 27 of the connector P1). A high input on BHEN/, consequently, sets the ST-728 for the 8-bit format.

ST-728 REGISTER ASSIGNMENTS

The following chart details the memory address assignments of the 16 memory locations the ST-728 occupies. Please note that when the ST-728 is used with 16-bit CPU's, every other (even-numbered) address location is used.

ST-728 REGISTER ASSIGNMENTS

MEMORY ADDRESS (8-bit CPU's)	FUNCTION	REGISTER ASSIGNMENT	MEMORY ADDRESS (16-bit CPU's)
BASE +0	WRITE	Output LSB Byte for DAC 0 (Channel 0)	BASE +0
BASE +1	WRITE	Output MSB Byte for DAC 0 (Channel 0)	
BASE +2	WRITE	Output LSB Byte for DAC 1 (Channel 1)	BASE +2
BASE +3	WRITE	Output MSB Byte for DAC 1 (Channel 1)	
BASE +4	WRITE	Output LSB Byte for DAC 2 (Channel 2)	BASE +4
BASE +5	WRITE	Output MSB Byte for DAC 2 (Channel 2)	
BASE +6	WRITE	Output LSB Byte for DAC 3 (Channel 3)	BASE +6
BASE +7	WRITE	Output MSB Byte for DAC 3 (Channel 3)	
BASE +8	WRITE	Output LSB Byte for DAC 4 (Channel 4)	BASE +8
BASE +9	WRITE	Output MSB Byte for DAC 4 (Channel 4)	
BASE +A	WRITE	Output LSB Byte for DAC 5 (Channel 5)	BASE +A
BASE +B	WRITE	Output MSB Byte for DAC 5 (Channel 5)	

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FUNCTIONAL SPECIFICATIONS
(Typical at +25°C, dynamic conditions, unless otherwise specified)

D/A ANALOG OUTPUT
Number of Channels
ST-728A, C - 4 D/A Channels
ST-728B, D - 8 D/A Channels
Indefinite channel expansion by separate, stand-alone ST-728 boards, each with a different base address; limited by available card slots, and power supply current.

Full Scale Output Ranges

±10V (standard)	Jumper Selectable by User for each channel
±5V	
0 to +10V	
0 to +5V	
4-20 mA	

Digital Input Coding

Straight Binary	Jumper Selectable by User in 4-channel groups
Offset Binary (Standard)	
2's Complement	

Output Impedance
50 Milliohms
Maximum Current Available on Voltage Outputs
±5 mA @ ±10V short-circuit-proof to ground
Current Loop Load Resistance
0 to 500Ω
Current Loop External Excitation Voltage
+18V to +30V dc, regulated, user-supplied (25 mA/DAC, max.)

ADDRESSING
Reserves a block of 16 consecutive memory locations. Base address may be located by jumper selection anywhere in the host computer's memory on 16-byte boundaries.

PERFORMANCE
Accuracy at +25°C
±0.05% of FSR (includes noise and nonlinearity)
Linearity Error, max. ±1/2 LSB
Linearity Error, 0°C to +70°C ±1 LSB
Differential Linearity Error ±1/2 LSB
Monotonicity
Monotonic over 0°C to +70°C temp. range
Zero Temperature Drift
(Unipolar Output only) Within ±2 ppm of FSR/°C
Offset Temperature Drift
(Bipolar Output only) Within ±5 ppm of FSR/°C

Gain Temperature Drift
Within ±10 ppm of FSR/°C
Settling Time (Board)
5 µS to within 1/2 LSB of final value

PHYSICAL
Outline Dimensions
12.00"W x 6.75"D x 0.50"H (304,8 x 171,5 x 12,7 mm)
ST-728 boards may be installed adjacent to each other in SBC card cages with 0.60" spacing
Weight (ST-728B) 11.2 ounces (0,318 kg)
Operating Temperature Range 0 to + 55°C
Relative Humidity 10% to 95%, non-condensing
Altitude 0 to 15,000 ft

POWER CONSUMPTION
All ST-728 models use some +5V power from the MULTIBUS. The ST-728C (4 channels) has an on-board DC-DC converter, so that *all* board power comes from the +5V line on the MULTIBUS. The ST-728A (4 channels no DC-to-DC) and ST-728B (8 channels, no DC-to-DC) require external ±15V supplies, input to the board via connector P2. The chart below summarizes the ST-728 board power requirements.

Except as noted, current readings are:
typical, (with output load)
typical, without output load

	from +5V MULTIBUS	(P2)	(P2)
ST-728A	750 mA	140 mA (150 mA)	70mA (90 mA)
ST-728B	1000 mA	110 mA (130 mA)	275 mA (300 mA)
ST-728C	1500 mA max.	N/A	N/A
ST-728D	2500 mA max.	N/A	N/A

GENERAL
Bus Compatibility
Pin-for-pin, card guide, and program compatible with MULTIBUS and SBC-series microcomputers.

CPU Compatibility
May be used with either 8-bit or 16-bit microprocessors.

ANALOG OUTPUT CONNECTIONS

J1 (DAC'S 0, 1, 2, 3)

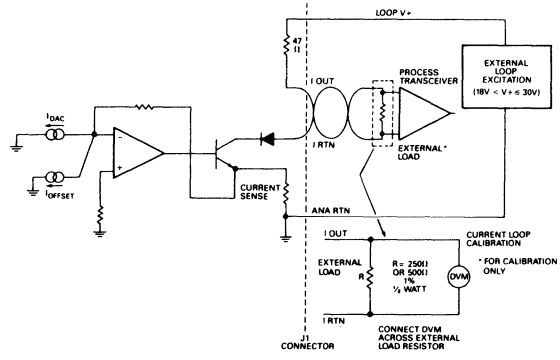
WIRING SIDE	PIN #'S		COMPONENT SIDE
NO CONNECTION	2	1	NO CONNECTION
NO CONNECTION	4	3	NO CONNECTION
NO CONNECTION	6	5	NO CONNECTION
NO CONNECTION	8	7	DAC 3, REF RTN
NO CONNECTION	10	9	DAC 3, EXT REF
NO CONNECTION	12	11	DAC 2, REF RTN
NO CONNECTION	14	13	DAC 2, EXT REF
NO CONNECTION	16	15	DAC 1, REF RTN
NO CONNECTION	18	17	DAC 1, EXT REF
NO CONNECTION	20	19	DAC 0, REF RTN
NO CONNECTION	22	21	DAC 0, EXT REF
DAC 3, V OUT	24	23	DAC 3, ANA RTN
DAC 3, I RTN	26	25	DAC 3, I RTN
DAC 3, LOOP V+	28	27	GND
DAC 2, V OUT	30	29	DAC 2, ANA RTN
DAC 2, I OUT	32	31	DAC 2, I RTN
DAC 2, LOOP V+	34	33	GND
DAC 1, V OUT	36	35	DAC 1, ANA RTN
DAC 1, I OUT	38	37	DAC 1, I RTN
DAC 1, LOOP V+	40	39	GND
DAC 0, V OUT	42	41	DAC 0, ANA RTN
DAC 0, I OUT	44	43	DAC 0, I RTN
DAC 0, LOOP V+	46	45	GND
POWER COMMON	48	47	POWER COMMON
-15V POWER[1]	50	49	+15V POWER[1]

NOTE: 1. 49 & 50 are outputs; 1 mA max (for ref. only).

J2 (DAC'S 4, 5, 6, 7)[1]

WIRING SIDE	PIN #'S		COMPONENT SIDE
NO CONNECTION	2	1	NO CONNECTION
NO CONNECTION	4	3	NO CONNECTION
NO CONNECTION	6	5	NO CONNECTION
NO CONNECTION	8	7	DAC 7, REF RTN
NO CONNECTION	10	9	DAC 7, EXT REF
NO CONNECTION	12	11	DAC 6, REF RTN
NO CONNECTION	14	13	DAC 6, EXT REF
NO CONNECTION	16	15	DAC 5, REF RTN
NO CONNECTION	18	17	DAC 5, EXT REF
NO CONNECTION	20	19	DAC 4, REF RTN
NO CONNECTION	22	21	DAC 4, EXT REF
DAC 7, V OUT	24	23	DAC 7, ANA RTN
DAC 7, I OUT	26	25	DAC 7, I RTN
DAC 7, LOOP V+	28	27	GND
DAC 6, V OUT	30	29	DAC 6, ANA RTN
DAC 6, I OUT	32	31	DAC 6, I RTN
DAC 6, LOOP V+	34	33	GND
DAC 5, V OUT	36	35	DAC 5, ANA RTN
DAC 5, I OUT	38	37	DAC 5, I RTN
DAC 5, LOOP V+	40	39	GND
DAC 4, V OUT	42	41	DAC 4, ANA RTN
DAC 4, I OUT	44	43	DAC 4, I RTN
DAC 4, LOOP V+	46	45	GND
POWER COMMON	48	47	POWER COMMON
-15V POWER [2]	50	49	+15V POWER [2]

NOTES: 1. J2 not used on 4 channel versions of ST-728
2. 49 & 50 are outputs; 1 mA max (for ref. only).



Typical ST-728 Current Loop Wiring

D/A CALIBRATION PROCEDURE (Performed with optional Diagnostic Program)

Calibration of the ST-728 should be performed every 90 days or whenever the Analog Output Range jumpers are reconfigured. More frequent calibration may be indicated in adverse operating conditions. The Diagnostic program listed in the ST-728 user manual was written as part of the calibration procedure. Please see the section entitled "Diagnostic Program".

1. Set the board jumpers for the desired output range: 0 to +5V, 0 to +10V, 4-20 mA, ±5V, or ±10V. See "Output Range Selection" for details.
2. Connect a digital voltmeter (Fluke 8800A or equivalent) to the outputs of Channel 0 (DAC 0). For voltage ranges, measure between "V OUT" and "ANA RTN". For current ranges the user must supply a precision 25Ω or 500Ω resistor; voltage measurements are then made across this resistor (see Note 1, bottom of Calibration Table.)
3. Using the Diagnostic program, select the "Calibration Test", Call Key "C".
4. The teletypewriter will respond by printing out:
   CALIBRATION TEST
   CHANNEL-
5. Enter character "0" to select Channel 0 (DAC 0)
   CHANNEL-0
   HEX DATA
6. Making reference to the Calibration Table, enter the hex code for the –Full Scale output voltage(or current), then enter a Carriage Return. Adjust the OFFSET potentiometer, until the reading on the DVM corresponds to the –Full Scale reading from the table.
7. Refer again to the Calibration Table, and enter the hex code for +Full Scale voltage or current. Adjust the GAIN potentiometer until the reading on the DVM is the +Full Scale voltage as indicated in the table.
8. Repeat steps 6 and 7.
9. Calibration for Channels 1 through 7 (DACs 1 through 7) is the same as for Channel 0.
10. The complete calibration may now be checked using the Calibration Table. Any hex value on the table may be entered followed by a carriage return. The corresponding analog output should appear on the DVM.

CALIBRATION TABLE

ANALOG OUTPUT						4-DIGIT HEX INPUT	
UNIPOLAR (STRAIGHT BINARY)				BIPOLAR (OFFSET OR 2'S COMPLEMENT)		STRAIGHT OR OFFSET BINARY-NO SIGN EXTENSION	2'S COMPLEMENT WITH SIGN EXTENSION
VOLTAGE		4-20mA CURRENT[1]					
0 TO +5V	0 TO +10V	500Ω LOAD LOOP V+>18V	200Ω LOAD LOOP V+>15V	±5V	±10V		
4.9988V	9.9976V	9.9980V	4.9990V	4.9976V	9.9951V	FFF0	7FF0
4.9976V	9.9951V	9.9961V	4.9980V	4.9951V	9.9902V	FFE0	7FE0
4.9951V	9.9902V	9.9922V	4.9961V	4.9902V	9.9805V	FFC0	7FC0
4.9902V	9.9805V	9.9844V	4.9922V	4.9805V	9.9609V	FF80	7F80
4.9805V	9.9609V	9.9687V	4.9844V	4.9609V	9.9219V	FF00	7F00
4.9609V	9.9219V	9,9375V	4.9687V	4.9219V	9.8437V	FE00	7E00
4.9219V	9.8437V	9.8750V	4.9375V	4.8437V	9.6875V	FC00	7C00
4.8437V	9.6875V	9.7500V	4.8750V	4.6875V	9.3750V	F800	7800
4.6875V	9.3750V	9.5000V	4.7500V	4.3750V	8.7500V	F000	7000
4.3750V	8.7500V	9.0000V	4.5000V	3.7500V	7.5000V	E000	6000
3.7500V	7.5000V	8.0000V	4.0000V	2.5000V	5.0000V	C000	4000
2.5000V	5.0000V	6.0000V	3.0000V	0.0000V	0.0000V	8000	0000
1.2500V	2.5000V	4.0000V	2.0000V	-2.5000V	-5.0000V	4000	C000
0.6250V	1.2500V	3.0000V	1.5000V	-3.7500V	-7.5000V	2000	A000
0.3125V	0.6250V	2.5000V	1.2500V	-4.3750V	-8.7500V	1000	9000
0.1563V	0.3125V	2.2500V	1.1250V	-4.6875V	-9.3750V	0800	8800
0.0781V	0.1563V	2.1250V	1.0625V	-4.8437V	-9.6875V	0400	8400
0.0391V	0.0781V	2.0625V	1.0312V	-4.9219V	-9.8437V	0200	8200
0.0196V	0.0391V	2.0312V	1.0156V	-4.9609V	-9.9219V	0100	8100
0.0098V	0.0196V	2.0156V	1.0078V	-4.9805V	-9.9609V	0080	8080
0.0049V	0.0098V	2.0078V	1.0039V	-4.9902V	-9.9805V	0040	8040
0.0024V	0.0049V	2.0039V	1.0020V	-4.9951V	-9.9902V	0020	8020
0.0012V	0.0024V	2.0020V	1.0010V	-4.9976V	-9.9951V	0010	8010
0.0000V	0.0000V	2.0000V	1.0000V	-5.0000V	-10.0000V	0000	8000

Note 1: Both the 250Ω and the 500Ω resistors (0.1% precision) provide 4 to 20 mA output. The current output circuit is calibrated in terms of voltage since most digital multimeters provide greater resolution and accuracy on voltage measurements than on current.

The voltages listed are those measured across a 250Ω or a 500Ω precision resistor, connected between "I RTN" and "I OUT" on any DAC output. A user-supplied DC regulated voltage, V+ (+15V < V+ ≤ +30V for 250Ω resistor, +18V < V+ ≤ +30V for 500Ω resistor; 25 mA max) is required for current output and calibration, and should be connected to "V+ LOOP". The supply providing V+ should be grounded at "ANA RTN".

TRANSFER ACKNOWLEDGE (XACK/) DELAY SELECTION

The ST-728 board generates a Transfer Acknowledge (XACK) signal in response to Write commands from the host computer. It is sometimes desirable to delay this signal in order to match the XACK/ signal to the host computer timing. A jumper selectable Transfer Acknowledge Delay (XACK/delay) ranging from 50 nanoseconds to 1.5 microseconds is available in the ST-728.

The accuracy of the XACK/delay is dependent in part on the duty cycle of the CCLK/ signal generated by the computer- shorter duty cycles result in greater accuracy. The delay time is advanced on the leading edge of CCLK/; XACK/ is generated on the trailing edge of CCLK/.

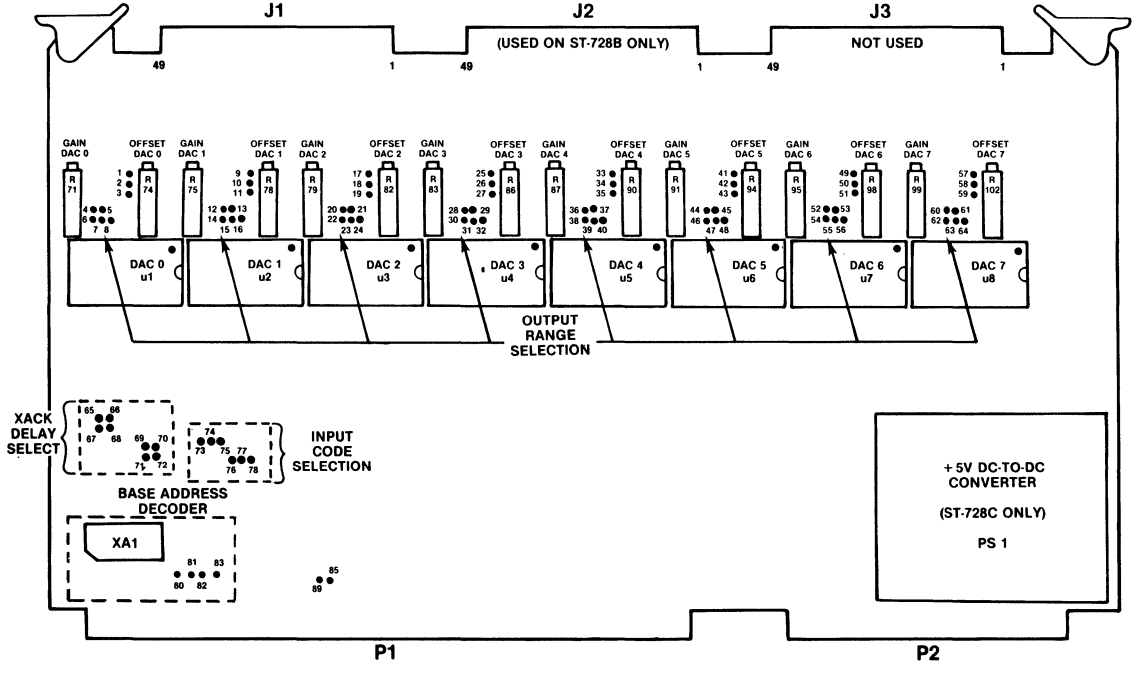
Please refer to the table for jumper configurations yielding different delay times.

XACK/ DELAY SELECTION

DELAY µsec.	JUMPERS			
0.05*	–	–	–	–
0.1	67-68	–	–	–
0.2	–	65-66	–	–
0.3	67-68	65-66	–	–
0.4	–	–	69-70	–
0.5	67-68	–	69-70	–
0.6	–	65-66	69-70	–
0.7	67-68	65-66	69-70	–
0.8	–	–	–	71-72
0.9	67-68	–	–	71-72
1.0	–	65-66	–	71-72
1.1	67-68	65-66	–	71-72
1.2	–	–	69-70	71-72
1.3	67-68	–	69-70	71-72
1.4	–	65-66	69-70	71-72
1.5	67-68	65-66	69-70	71-72

*Factory supplied configuration

COMPONENT SIDE



ST-728 Board Layout

BASE ADDRESS SELECTION

(For Assembly D–11625, Revision F or later)

Base Address (Hexadecimal)	[see note 2] (Ø to F)	(Ø to F)	(Ø to F)	(Ø to F)	(Ø to F)	* (Ø)
Hex bit weighing	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	8 4 2 1	
Address Bit (Hex)	17 16 15 14	13 12 11 10	F E D C	B A 9 8	7 6 5 4	3-0
Jumper (see note 1)	A A A A 17 16 15 14	A A A A 13 12 11 10	AF AE AD AC	AB AA A9 A8	A7 A6 A5 A4	

Note 1: Jumper Out =" Ø", Jumper In = "1".
* Address bits 3 - Ø are decoded by D/A channel addressing.
Note 2: For 24-bit addressing, install jumper 80-81. For 16- or 20-bit addressing, remove jumper 80-81.
Note 3: To control 8- or 16-bit transfers by detecting BHEN/, remove jumper 84-85. Install jumper 84-85 to ground BHEN/ (always low).

OUTPUT RANGE INPUT CODING SELECTION

The ST-728's D/A output channels may be set independently for any of four voltage ranges or a single current output range. Full scale ranges of ±10V, ±5V, 0 to +10V, 0 to +5V, or 4–20 mA may be jumper-selected according to the chart below. Input digital coding may be offset binary, 2's complement, or straight binary. Again, refer to the chart below for details.

The ST-728 board is normally shipped with jumpers set for the ±10V output, and an offset binary input coding. Please note that whenever there is a change in output range on a given channel, that channel should be recalibrated.

INPUT CODE SELECTION JUMPERS

CODE	DAC 0 TO DAC 3	DAC 4 TO DAC 7
Unipolar or Offset Bin. (Standard)	74-75	77-78
2's Complement	73-74	76-77

OUTPUT RANGE SELECTION JUMPER

RANGE	DAC 0	DAC 1	DAC 2	DAC 3	DAC 4	DAC 5	DAC 6	DAC 7
±10V	2-3	10-11	18-19	26-27	34-35	42-43	50-51	58-59
(Standard)	4-5	12-13	20-21	28-29	36-37	44-45	52-53	60-61
±5V	2-3	10-11	18-19	26-27	34-35	42-43	50-51	58-59
	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
0 to +10V	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
0 to +5V	4-6	12-14	20-22	28-30	36-38	44-46	52-54	60-62
	5-7	13-15	21-23	29-31	37-39	45-47	53-55	61-63
4 to 20 mA	1-2	9-10	17-18	25-26	33-34	41-42	49-50	57-58
Current Loop	7-8	15-16	23-24	31-32	39-40	47-48	55-56	63-64

ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
ST-728A/2/24	4 D/A Channels, no DC-DC Converter (±15V dc, +5V dc power required)
ST-728B/2/24	8 D/A Channels, no DC-DC Converter (±15V dc, +5V dc power required)
ST-728C2/24	4 D/A Channels, with DC-DC Converter (+5V dc power required)
ST-728D2/24	8 D/A Channels, with DC-DC Converter (+5V dc power required)
31-2076040	Edge Connector, J1 and J2, Spare
UM-ST-728	ST-728 Manual (Spare; one supplied with board)

Standard (2/24) versions includes the current loop option. Versions without current loops(1/24) are available at lower cost for scheduled, quantity orders.

SUBSTITUTION GUIDE FOR DISCONTINUED PRODUCTS

The following products are no longer available from DATEL. Where applicable, the nearest equivalent DATEL replacement is listed. Some of these replacement products are functionally similar only and may not be pin-for-pin compatible with the discontinued product.

DISCONTINUED MODEL	NEAREST EQUIVALENTS
9639 Series	NONE
ADC-833R	ADC-207
ADC-84,85,87	ADC-HX, -HZ
ADC-89 Series	ADC-856
ADC-E Series	ADC-7109, ADC-ET Series
ADC-G10B	ADC-816, ADC-510/515
ADC-G8B	ADC-815
ADC-HU	ADC-207
ADC-L Series	ADC-HX12B
ADC-M Series	ADC-HZ12B
ADC-MA Series	ADC-HX12B
ADC-SH4B	ADC-HS12B
ADC-TV8B	ADC-208, ADC-304
ADC-UH Series	ADC-208, ADC-304
All -E version Power Supplies	NONE
All -J version Power Supplies	NONE
AM-100 Series	AM-551
AM-200 Series	AM-542
AM-300 Series	NONE
AM-410,-411	NONE
AM-470	NONE
AM-490	AM-7650
APP-20V Series	NONE
APP-20-2 Series	APP-2-21 Series
APP-48 MIL Series	APP-M48 Series
BPM-12/210-D48	NONE
BPM-12/420-D48	NONE
BPM-15/330-D48	NONE
BPM-18/100-D12	NONE
BPM-18/100-D28	NONE
BPM-18/100-D5	NONE
BPM-18/140-D12	NONE
BPM-18/140-D24	NONE
BPM-18/140-D48	NONE
BPM-18/140-D5	NONE
BPM-18/25-D12	NONE
BPM-18/25-D28	NONE
BPM-18/25-D5	NONE
BPM-18/280-D12	NONE
BPM-18/280-D24	NONE
BPM-18/280-D28	NONE
BPM-18/280-D48	NONE
BPM-18/280-D5	NONE
CAPP-20	NONE
CDPP-Q7	NONE
DAC-19B Series	DAC-HZ12
DAC-29B Series	DAC-HZ12
DAC-49B Series	DAC-HZ12
DAC-69B Series	DAC-HZ12
DAC-71, -72	DAC-HP16
DAC-85,-87	DAC-HZ12
DAC-9B Series	DAC-IC8B
DAC-HA Series	DAC-7533,-7541, -7134
DAC-HI Series	DAC-HF Series
DAC-HR	DAC-HP16
DAC-I Series	DAC-HF Series
DAC-V Series	DAC-HZ12
DAC-VR Series	DAC-HK12

DISCONTINUED MODEL	NEAREST EQUIVALENTS
DAS-250	NONE
DAS-256 Series	DVME Series
DDS-32 Series	DVME Series
DM-2000AR	DM-3102A, B
DM-2115	NONE
DM-350	DM-3100L/DM-3100B
DM-4100L	DM-4101L
DM-4100N	DM-4101N
DPP-7	DPP-Q7
DVC-350	DVC-350A
ICT Series	NONE
LPS-16 Series	NONE
MDXP-32/32-1	NONE
SCS-16	DVME-643
SHM-1	SHM-IC1, SHM-20
SHM-2, -2E	SHM-7, SHM-40
SHM-UH	SHM-7, SHM-40
ST-LSI-RLY	NONE
ST-6800 Series	DVME Series
ST-6832 Series	DVME Series
ST-711 RLY	ST-702
ST-800 Series	ST-711/732 and ST-728
ST-MNOVA	NONE
ST-NOVA Series	NONE
ST-PDP Series	NONE
UPA-9/100	NONE
UPM-12/100A	NONE
UPM-12/420-D28	NONE
UPM-12/420-D48	NONE
UPM-12/840-D24	NONE
UPM-12/840-D28	NONE
UPM-12/840-D48	NONE
UPM-12/840-D5	NONE
UPM-15/100A	NONE
UPM-15/330-D12	NONE
UPM-15/330-D24	NONE
UPM-15/330-D28	NONE
UPM-15/330-D48	NONE
UPM-15/330-D5	NONE
UPM-15/660-D12	NONE
UPM-15/660-D24	NONE
UPM-15/660-D28	NONE
UPM-15/660-D48	NONE
UPM-15/660-D5	NONE
UPM-24/125-D5	NONE
UPM-24/420-D12	NONE
UPM-24/420-D5	NONE
UPM-28/180-D12	NONE
UPM-28/180-D5	NONE
UPM-28/360-D12	NONE
UPM-28/360-D5	NONE
UPM-5/1000-D48	NONE
UPM-5/1000-D5	NONE
UPM-5/200-D5	NONE
UPM-5/2000-D12	NONE
UPM-5/2000-D5	NONE
UPM-6/150A	NONE
UPM-9/100A	NONE
VFV Series	VFQ-1,-2,-3

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

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DATEL

CUSTOMER PRICE LIST
EFFECTIVE NOVEMBER 1, 1988

LOOK FOR SUBSTANTIAL PRICE REDUCTIONS ON SELECTED PRODUCTS.

Prices In U.S. Dollars

ORDERING GUIDE

This ordering guide is presented as a procedural guide. For a formal statement of policies, refer to the TERMS AND CONDITIONS OF SALE found on the Quotation form or on the Customer Acknowledgement copy of the Sales Order.

PLACING AN ORDER
When ordering a DATEL product, give the complete model number, product description, and option description. Place orders with a DATEL field sales representative or with the factory by letter, telephone, FAX, or TELEX. *Minimum order and minimum per shipment is $100.*

OUTSIDE THE U.S.A. AND CANADA Place overseas orders with a DATEL Sales Subsidiary (in West Germany, France, the United Kingdom, and Japan) or with a DATEL overseas sales representative. Orders received directly will be treated the same as if placed through our overseas sales representative. In countries without a DATEL representative, orders should be placed by TELEX and confirmed by air mail.

FIELD SALES REPRESENTATIVE
DATEL employs field sales representatives throughout the United States, Canada, Europe, and the Far East. In addition, it has direct Sales Offices in Santa Ana and San Jose, California. DATEL also has Sales Subsidiaries in Munich, West Germany; Paris, France; London, England; and Tokyo and Osaka, Japan. Only these sales representatives are authorized by DATEL to solicit sales, and any information or data received by sources other than these authorized representatives or the DATEL factory are not considered binding.

PRICES
All prices are F.O.B. , Mansfield, Massachusetts, U.S.A. in U.S. dollars. Applicable federal, state, and local taxes are extra and paid by buyer. Prices are subject to change without notice.

TERMS Net 30 days

DISCOUNTS
Quantity discounts are available when placed in a single order. OEM discounts are available on an order or contract basis; consult the factory for details

QUOTATIONS
Price and delivery quotations made by DATEL or its authorized field sales representatives are valid for 60 days unless otherwise stated.

DELIVERY
DATEL uses an IBM System 4381, for efficient processing of orders. All orders placed with DATEL are acknowledged within a few days by an acknowledgement copy of our sales order form. This copy indicates pertinent information including a formal statement of terms and conditions of sale and estimated delivery date. This date has preference over all other agreed upon dates unless otherwise specified.

DATEL ships all products in rugged commercial containers suitable for insuring safe delivery under normal shipping conditions. Unless shipping method is specified, the best available method will be used. Shipping charges are normally prepaid and billed to the customer except for Air Freight charges which are sent collect. The appropriate data sheet and/or instruction is packed with each product shipped.

ORDER CANCELLATION
All orders entered with DATEL are binding and are subject to a cancellation charge if cancelled before or after the scheduled shipping date appearing on the acknowledgement copy of the sales order form. Refer to DATEL's Standard Terms and Conditions for specific charges.

WARRANTY
DATEL warrants that all of its products are free from defects in material and workmanship under normal use and service for a period of one year from date of shipment. DATEL's obligations under this warranty are limited to replacing or repairing, at its option, at its factory or facility, any of the products which shall within the applicable period after shipment be returned to DATEL's facility, transportation charges prepaid, and which are after examination disclosed to the satisfaction of DATEL to be thus defective. This warranty shall not apply to any such equipment which shall have been repaired or altered except by DATEL or which shall have been subjected to misuse, negligence, or accident. In no case shall DATEL's liablity exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by DATEL.

RETURNS
You will need a **return authorization number** and shipping instructions from the factory when returning products for any reason. Items should not be returned air freight collect as they connot be accepted. It is absolutely necessary to return products in the manner stated here, otherwise considerable delay will result in processing the return.

RETURNS OUTSIDE THE U.S.A. AND CANADA Contact the local sales representative or factory for authorization and shipping instructions first.

CERTIFICATE OF COMPLIANCE
When requested by the customer DATEL will provide a standard Certificate of Compliance with all shipments. This request must be specified on the purchase order.

DATEL, INC. 11 CABOT BOULEVARD, MANSFIELD, MASS. 02048 U.S.A.

TEL. (508) 339-3000 FAX: (508) 339-6356 TELEX: 174388

CUSTOMER PRICE LIST

MODEL	PRICE
ADC-B207/208	450.00
ADC-B301E	959.00
ADC-B302E	1436.00
ADC-B303E	2426.00
ADC-B304E	509.00
ADC-B310E	2536.00
ADC-B500	726.00
ADC-B500-1	173.00
ADC-B505	702.00
ADC-EH10B1	199.00
ADC-EH10B2	242.00
ADC-EH12B2	257.00
ADC-EH12B3	263.00
ADC-EH8B1	120.00
ADC-EH8B2	170.00
ADC-EK10B	29.25
ADC-EK12B	38.25
ADC-EK12DC	12.55
ADC-EK12DM	35.10
ADC-EK12DR	26.85
ADC-EK8B	11.05
ADC-ET10BC	16.50
ADC-ET10BM	46.15
ADC-ET12BC	18.40
ADC-ET12BM	62.50
ADC-ET12BR	43.50
ADC-ET8BC	13.15
ADC-ET8BM	36.40
ADC-HC12BMC	246.00
ADC-HC12BMM	336.00
ADC-HC12BMM-QL	373.00
ADC-HS12BMC	167.00
ADC-HS12BMM	227.00
ADC-HS12BMM-QL	313.00
ADC-HX/883B	293.00
ADC-HX12BGC	106.00
ADC-HX12BMC	135.00
ADC-HX12BMM	189.00
ADC-HZ/883B	307.00
ADC-HZ12BGC	137.00
ADC-HZ12BMC	155.00
ADC-HZ12BMM	220.00
ADC-MC8BC	7.45
ADC-MC8BM	13.00
ADC-207/883B	179.00
ADC-207MC	40.00
ADC-207MM	78.00
ADC-208/883B	211.00
ADC-208MC	66.00
ADC-208MM	115.00
ADC-300	40.00
ADC-301	105.00
ADC-302	215.00
ADC-303	550.00
ADC-304	43.00
ADC-310	590.00
☆ ADC-500BMC	249.00
☆ ADC-500BMM	274.00
☆ ADC-505BMC	240.00
☆ ADC-505BMM	264.00
☆ ADC-505BMM-QL	288.00
☆ ADC-508MC	230.00
☆ ADC-508MM	253.00
☆ ADC-508MM-QL	276.00
☆ ADC-510BMC	230.00
☆ ADC-510BMM	253.00
☆ ADC-510BMM-QL	276.00
ADC-5101	224.00
ADC-5101H	300.00
ADC-5101H-QL	360.00
ADC-511MC	199.00
ADC-511MM	219.00
☆ ADC-515BMC	220.00
☆ ADC-515BMM	242.00
☆ ADC-515BMM-QL	264.00
☆ ADC-520MC	220.00
☆ ADC-520MM	242.00
☆ ADC-520MM-QL	264.00
☆ ADC-521MC	220.00
☆ ADC-521MM	242.00
☆ ADC-521MM-QL	264.00
ADC-5211	155.00
ADC-5211H	201.00
ADC-5211H-QL	330.00
ADC-5212	155.00
ADC-5212H	201.00
ADC-5212H-QL	330.00
ADC-5214	155.00
ADC-5214H	201.00
ADC-5214H-QL	330.00
ADC-5215	155.00
ADC-5215H	201.00
ADC-5215H-QL	330.00
ADC-5216	155.00
ADC-5216H	201.00
ADC-5216H-QL	330.00
ADC-574ZA	83.55
ADC-574ZB	47.45
ADC-574ZC	36.20
ADC-674ZA	93.85
ADC-674ZB	60.95
ADC-674ZC	46.45
ADC-7109	13.45
ADC-800	24.75
ADC-810MC	258.00
ADC-810MM	398.00
ADC-810MM-QL	502.00
ADC-811MC	235.00
ADC-811MM	363.00
ADC-811MM-QL	458.00
ADC-815MC	201.00
ADC-815MM	258.00
ADC-815MM-QL	284.00
ADC-816/883B	370.00
ADC-816MC	218.00
ADC-816MM	299.00
ADC-817AMC	263.00
ADC-817AMM	336.00
ADC-817AMM-QL	447.00
ADC-817MC	338.00
ADC-817MM	411.00
ADC-817MM-QL	522.00
ADC-825MC	177.00
ADC-825MM	240.00
ADC-825MM-QL	265.00
ADC-826/883B	345.00
ADC-826MC	197.00
ADC-826MM	279.00
ADC-827AMC	245.00
ADC-827AMM	313.00
ADC-827AMM-QL	416.00
ADC-827MC	320.00
ADC-827MM	388.00
ADC-827MM-QL	491.00
ADC-830C	7.00
ADC-847A	6.70
ADC-847B	18.30
ADC-847M	30.50
ADC-856C	47.00
ADC-856M	61.95
ADC-868	731.00
ADC-881	451.00
ADC-974	999.00
☆ ADS-105MC	279.00
☆ ADS-105MM	307.00
☆ ADS-105MM-QL	335.00
☆ ADS-106MC	279.00
☆ ADS-106MM	307.00
ADS-106MM-QL	335.00
ADS-111MC	229.00
ADS-111MM	252.00
☆ ADS-115MC	249.00
☆ ADS-115MM	274.00
☆ ADS-115MM-QL	324.00
☆ ADS-116MC	249.00
☆ ADS-116MM	274.00
☆ ADS-116MM-QL	324.00
ADS-125MC	250.00
ADS-125MM	274.00
ADS-126MC	250.00
ADS-126MM	274.00
☆ ADS-21AC	475.00
☆ ADS-22AC	425.00
AM-1435MC	99.00
AM-1435MM	138.00
AM-1435MM-QL	154.00
AM-227	117.00
AM-427-1A	5.00
AM-427-1B	9.40
AM-427-2A	6.50
AM-427-2B	9.00
AM-430A	6.65
AM-430B	16.50
AM-450-2	4.35
AM-450-2M	21.35
AM-452-2	6.70
AM-452-2M	20.45
AM-453-2C	5.50
AM-453-2M	6.25
AM-460-2	6.65
AM-462-2	6.65
AM-464-2	6.15
AM-500GC	113.00
AM-500MC	124.00
AM-500MM	167.00
AM-500MM-QL	185.00
AM-543MC	203.00
AM-551MC	71.00
AM-551MM	85.00
AM-551MM-QL	101.00
AM-7650-1	4.05
AM-7650-2	4.95
APP-M20A1	709.00
APP-M20A21	820.00
APP-M20D1	709.00
APP-M20D21	820.00
APP-M20D3	865.00
APP-M20E1	709.00
APP-M20E21	820.00
APP-M48D1	1165.00
APP-M48D2	1165.00
APP-M48D3	1165.00
APP-M48D4	1370.00
APP-20A1	615.00
APP-20A21	720.00
APP-20A3	775.00
APP-20D1	615.00
APP-20D21	720.00
APP-20D3	775.00
APP-20E1	615.00
APP-20E21	720.00
APP-20E3	775.00
APP-20J1	615.00
APP-20J2	820.00
APP-20J3	775.00
APP-48A1	1060.00
APP-48A2	1060.00
APP-48A3	1060.00
APP-48A4	1295.00
APP-48D1	1060.00
APP-48D2	1060.00
APP-48D3	1060.00
APP-48D4	1295.00
APP-48E1	1060.00
APP-48E2	1060.00
APP-48E3	1060.00
APP-48E4	1295.00
APP-48J2	1060.00
APP-48J3	1060.00
APP-48J4	1295.00
BCM-15/100	63.00
BCM-15/200	79.00
BCM-15/300	95.00
BCM-15/60	57.00
BPM-12/100	61.00
BPM-12/200	79.00
BPM-12/25-D12	49.00
BPM-12/25-D28	49.00
BPM-12/25-D5	49.00
BPM-12/300	101.00
BPM-12/420-D12	128.00
BPM-12/420-D24	128.00
BPM-12/420-D28	128.00
BPM-12/420-D5	128.00
BPM-12/60	57.00
BPM-120/25	105.00
BPM-15/100	63.00
BPM-15/150-D24	81.00
BPM-15/150-D28	81.00
BPM-15/150-D5	81.00
BPM-15/200	79.00
BPM-15/25-D12	49.00
BPM-15/25-D28	49.00
BPM-15/25-D5	49.00
BPM-15/300	95.00
BPM-15/60	57.00
BPM-150/20	105.00
BPM-180/16	105.00
BPM-5/250	77.00
BPM-5/500	79.00
BPS-12/125-D12	86.00
BPS-12/125-D28	86.00
BPS-12/125-D5	86.00
BPS-12/1250-D12	169.00
BPS-12/1250-D24	169.00
BPS-12/230-D12	112.00
BPS-12/230-D24	112.00
BPS-12/230-D28	112.00
BPS-12/230-D5	112.00
BPS-12/40-D5	43.00
BPS-12/625-D12	125.00
BPS-12/625-D24	125.00
BPS-15/100-D12	86.00
BPS-15/100-D28	86.00
BPS-15/100-D5	86.00
BPS-15/1000-D12	169.00
BPS-15/1000-D24	169.00
BPS-15/190-D12	112.00
BPS-15/190-D24	112.00
BPS-15/190-D28	112.00
BPS-15/190-D48	112.00
BPS-15/190-D5	112.00
BPS-15/33-D5	43.00
BPS-15/412-D12	135.00
BPS-15/412-D24	135.00
BPS-15/412-D28	135.00
BPS-15/412-D5	135.00
BPS-15/500-D12	125.00
BPS-15/500-D24	125.00
DAC-DG12B1	415.00
DAC-DG12B2	415.00
DAC-HF10BMC	171.00
DAC-HF10BMM	210.00
DAC-HF10BMM-QL	296.00
DAC-HF12BMC	201.00
DAC-HF12BMM	239.00
DAC-HF12BMM-QL	324.00
DAC-HF8BMC	158.00
DAC-HF8BMM	192.00
DAC-HF8BMM-QL	275.00
DAC-HKB-2/883B	217.00
DAC-HKB/883B	217.00
DAC-HK12BGC	67.00
DAC-HK12BGC-2	67.00
DAC-HK12BMC	82.00
DAC-HK12BMC-2	82.00
DAC-HK12BMM	139.00
DAC-HK12BMM-2	139.00
DAC-HPB-1/883B	241.00
DAC-HPB/883B	241.00
DAC-HP16BGC	78.00
DAC-HP16BGC-1	78.00
DAC-HP16BMC	93.00
DAC-HP16BMC-1	93.00
DAC-HP16BMM	163.00
DAC-HP16BMM-1	163.00
DAC-HZB/883B	185.00
DAC-HZ12BGC	48.00
DAC-HZ12BMC	58.00
DAC-HZ12BMM	108.00
DAC-HZ12DGC	87.00

MODEL	PRICE
DAC-HZ12DMC	106.00
DAC-HZ12DMM	139.00
DAC-HZ12DMM-QL	189.00
DAC-IC10B	14.95
DAC-IC10BC	9.95
DAC-IC10BM	23.15
DAC-IC8BC	2.65
DAC-IC8BM	11.45
DAC-UP10BC	12.00
DAC-UP8BC	6.50
DAC-UP8BM	16.00
DAC-08BC	2.25
DAC-08BM	4.50
DAC-0805MR	105.00
DAC-0805MR-QL	124.00
DAC-330	112.00
DAC-562C	18.35
DAC-608C	3.75
DAC-610C	10.45
DAC-612C	17.15
DAC-7134BJ	21.40
DAC-7134BK	32.95
DAC-7134BL	49.45
DAC-7134UJ	21.40
DAC-7134UK	32.95
DAC-7134UL	49.45
DAC-7523	3.75
DAC-7533	6.00
DAC-7541	13.90
DAC-8308	162.00
DAS-952R	14.90
DBM-20	59.00
DILS-1	3.80
DILS-2	3.80
DILS-3	3.30
DM-LX3-1	65.00
DM-31-1	49.00
DM-3100B-1	99.00
DM-3100L-1	65.00
DM-3100MIL-1	195.00
DM-3100N-1	59.00
DM-3100U1-1	75.00
DM-3100U2-1	85.00
DM-3100U3-1	89.00
DM-3100X-1	79.00
DM-3101-1	99.00
DM-3102A	170.00
DM-3102B	145.00
DM-3103-1	99.00
DM-3104-1	99.00
DM-4100D-1	155.00
DM-4101D-1	145.00
DM-4101L-1	89.00
DM-4101N-1	95.00
DM-4102	65.00
DM-4103	65.00
DM-4104	75.00
DM-4105-1	105.00
DM-4106	69.00
DM-4200-1	85.00
DM-500-1	29.00
DM-9100-1	89.00
DM-9115-1	99.00
DM-9150-1	99.00
DM-9165-1	99.00
DM-9200-1	95.00
DM-9215-1	109.00
DM-9250-1	115.00
DM-9265-1	109.00
DPP-Q7A1	635.00
DPP-Q7A1H	650.00
DPP-Q7A2	635.00
DPP-Q7A2H	650.00
DPP-Q7A3	635.00
DPP-Q7A3H	650.00
DPP-Q7A4	635.00
DPP-Q7A4H	650.00
DPP-Q7A5	720.00
DPP-Q7A5H	720.00
DPP-Q7A6	720.00
DPP-Q7A6H	720.00
DPP-Q7B1	635.00
DPP-Q7B1H	650.00
DPP-Q7B2	635.00
DPP-Q7B2H	650.00
DPP-Q7B3	635.00
DPP-Q7B3H	650.00
DPP-Q7B4	635.00
DPP-Q7B4H	650.00
DPP-Q7B5	720.00
DPP-Q7B5H	720.00
DPP-Q7B6	720.00
DPP-Q7E1	635.00
DPP-Q7E1H	650.00
DPP-Q7E2	635.00
DPP-Q7E2H	650.00
DPP-Q7E3	635.00
DPP-Q7E3H	650.00
DPP-Q7E4	635.00
DPP-Q7E5	720.00
DPP-Q7E6	720.00
DPP-Q7J1	635.00
DPP-Q7J2	635.00
DPP-Q7J2H	650.00
DPP-Q7J3	635.00
DPP-Q7J4	635.00
DVC-350A	387.00
DVC-8500A	959.00
DVC-8500E	959.00
DVC-8500J	959.00
DVME-C-01	40.00
DVME-C-02	50.00
DVME-IOTEST/P	50.00
DVME-IOTEST/V	50.00
DVME-UTIL/P	385.00
DVME-UTIL/V	385.00
DVME-601A	1995.00
DVME-601B	2095.00
DVME-601B-U	2095.00
DVME-601C	2695.00
DVME-601C-U	2695.00
DVME-601D	2195.00
DVME-601E	2195.00
DVME-602H	1419.00
DVME-602R	1419.00
DVME-602T	1375.00
DVME-611A	1495.00
DVME-611B	1617.00
DVME-611B-U	1617.00
DVME-611C	1638.00
DVME-611C-U	1638.00
DVME-611D	1648.00
DVME-611E	1717.00
DVME-612A	1595.00
DVME-612B	1712.00
DVME-612B-U	1712.00
DVME-612C	1732.00
DVME-612C-U	1732.00
DVME-612D	1742.00
DVME-612E	1812.00
DVME-624C1	1363.00
DVME-624C2	1577.00
DVME-624V1	1146.00
DVME-624V2	1360.00
DVME-626V1	1768.00
DVME-626V2	1768.00
DVME-628C	1708.00
DVME-628V	1345.00
DVME-641	695.00
DVME-643H	1523.00
DVME-643T	1435.00
DVME-645	1385.00
DVME-660	795.00
DVME-691A	295.00
DVME-691D	295.00
FLJ-ACR1	80.00
FLJ-ACR2	80.00
FLJ-AC01	40.00
FLJ-DC	190.00
FLJ-D1	225.00
FLJ-D2	225.00
FLJ-D5LA1	220.00
FLJ-D5LA2	220.00
FLJ-D6LA1	222.00
FLJ-D6LA2	222.00
FLJ-R3BA1	126.00
FLJ-R3BA2	126.00
FLJ-R8LA1	168.00
FLJ-R8LA2	168.00
FLJ-R8LB1	168.00
FLJ-R8LB2	168.00
FLJ-UR1BA1	40.00
FLJ-UR1BA2	40.00
FLJ-UR2BA1	61.00
FLJ-UR2BA2	61.00
FLJ-UR2EA1	59.00
FLJ-UR2EA2	59.00
FLJ-UR2LH1	40.00
FLJ-UR2LH2	40.00
FLJ-UR4HA1	47.00
FLJ-UR4HA2	47.00
FLJ-UR4HB1	47.00
FLJ-UR4HB2	47.00
FLJ-UR4LA1	47.00
FLJ-UR4LA2	47.00
FLJ-UR4LB1	47.00
FLJ-UR4LB2	47.00
FLJ-VB	176.00
FLJ-VH	176.00
FLJ-VL	176.00
FLT-C1	35.75
FLT-U2	26.50
FLT-U2-M	42.75
HDAS-16/883B	675.00
HDAS-16MC	350.00
HDAS-16MM	418.00
HDAS-8/883B	675.00
HDAS-8MC	350.00
HDAS-8MM	418.00
MDAS-16	339.00
MDAS-8D	339.00
MDAS-940D	386.00
MDAS-940S	386.00
MPP-20A	440.00
MPP-20D	440.00
MPP-20E	440.00
MPP-20J	440.00
MS-1	33.25
MS-11	5.40
MS-13	5.40
MS-2	33.25
MS-3	33.25
MS-4	33.25
MS-5	33.25
MS-6	5.40
MS-7	5.40
MS-9	5.40
MV-1606	11.80
MV-1606M	25.70
MV-808	12.65
MVD-409	12.65
MVD-807	11.80
MX-1606	20.95
MX-1616C	27.90
MX-808	11.75
MX-818C	14.50
MXD-409	11.70
MXD-807	20.95
PC-6	169.00
PM-5050-1000A	395.00
PM-5050-1000D	430.00
PM-5050-1000E	395.00
PM-5050-1000J	395.00
PM-5050-1010A	460.00
PM-5050-1010D	495.00
PM-5050-1010E	460.00
PM-5050-1010J	460.00
PM-5060-1000A	395.00
PM-5060-1000E	395.00
PM-5060-1000J	395.00
PM-5060-1010A	460.00
PM-5060-1010E	460.00
PM-5060-1010J	460.00
PM-5070-1000A	425.00
PM-5070-1000E	425.00
PM-5070-1000J	425.00
PM-5070-1010A	490.00
PM-5070-1010E	490.00
PM-5070-1010J	490.00
PM-5080-1000A	395.00
PM-5080-1000E	395.00
PM-5080-1000J	395.00
PM-5080-1010A	460.00
PM-5080-1010E	460.00
PM-5080-1010J	460.00
ROJ-1K	97.00
ROJ-20	97.00
SCM-100A	253.00
SCM-100B	300.00
SCM-101	244.00
SCM-103	165.00
SDAS-8A1	479.00
SDAS-8A2	479.00
SDAS-8A3	479.00
SDAS-8A4	479.00
SDAS-8E1	479.00
SDAS-8E2	479.00
SDAS-8E3	479.00
SDAS-8E4	479.00
SHM-HUMC	150.00
SHM-HUMM	178.00
SHM-HUMM-QL	197.00
SHM-IC-1	10.05
SHM-IC-1M	45.85
SHM-LM-2	4.05
SHM-UH3	268.00
SHM-2	136.00
SHM-2E	150.00
SHM-20C	13.40
SHM-30C	29.45
SHM-360	18.00
SHM-361	27.00
☆ SHM-40MC	143.00
☆ SHM-40MM	157.00
☆ SHM-45MC	154.00
☆ SHM-45MM	169.00
☆ SHM-45MM-QL	185.00
☆ SHM-4860MC	149.00
☆ SHM-4860MM	164.00
☆ SHM-4860MM-QL	179.00
SHM-5	204.00
SHM-6MC	153.00
SHM-6MM	219.00
SHM-6MM-QL	243.00
SHM-7MC	136.00
SHM-9MC	65.00
SHM-9MM	117.00
SHM-9MM-QL	129.00
SHM-91MC	144.00
SHM-91MM	214.00
SHM-91MM-QL	250.00
ST-519	465.00
ST-701A2	1748.00
ST-701A2/24	1748.00
ST-701B2	1823.00
ST-701B2-U	1823.00
ST-701B2/24	1823.00
ST-701C2	2140.00
ST-701C2/24	2140.00
ST-701D2	1674.00
ST-701D2/24	1674.00
ST-701E2/24	1923.00
ST-702A	1478.00
ST-702B	1478.00
ST-702R	1478.00
ST-703A	1033.00
ST-703B	1208.00
ST-705A1	785.00
ST-705A2	785.00
ST-705A3	785.00

CUSTOMER PRICE LIST

MODEL	PRICE
ST-705A4	785.00
ST-705E1	785.00
ST-705E2	785.00
ST-705E3	785.00
ST-705E4	785.00
ST-705J1	785.00
ST-705J2	785.00
ST-705J3	785.00
ST-705J4	785.00
ST-711	884.00
ST-716B1	1405.00
ST-716B2	1405.00
ST-716C1	1006.00
ST-716C2	1006.00
ST-716D1	1613.00
ST-716D2	1613.00
ST-724	849.00
ST-728A2/24	773.00
ST-728B2/24	1085.00
ST-728C2/24	915.00
ST-728D2/24	1219.00
ST-732	1117.00
ST-742	595.00
TP-1K	4.00
TP-1M	4.00
TP-10	4.00
TP-10K	4.00
TP-100	4.00
TP-100K	4.00
TP-2K	4.00
TP-20	4.00
TP-20K	4.00
TP-200	4.00
TP-200K	4.00
TP-25K	4.00
TP-250	4.00
TP-5K	4.00
TP-50	4.00
TP-50K	4.00
TP-500	4.00
TPM-12/100-5/500	90.00
TPM-12/150-5/1000	108.00
TPM-12/200-5/500	108.00
TPM-15/100-5/500	90.00
TPM-15/150-5/1000	108.00
TPM-15/200-5/500	108.00
TPS-12/310-5/1500-D12	107.00
TPS-12/310-5/1500-D24	107.00
TPS-5/1500-12/310-D12	107.00
TPS-5/1500-12/310-D24	107.00
TPS-5/1500-15/250-D12	107.00
TPS-5/1500-15/250-D24	107.00
UCM-5/1000	83.00
UCM-5/1000-B	71.00
UCM-5/2000	93.00
UCM-5/250	64.00
UCM-5/500	56.00
UM-APP-20AEJ1/AEJ2	30.00
UM-APP-20AEJ3	30.00
UM-APP-48AEJ2	30.00
UM-APP-48AEJ3	30.00
UM-DPP-Q7	30.00
UM-DVC-350A	30.00
UM-DVME-601	30.00
UM-DVME-602	30.00
UM-DVME-611/612	30.00
UM-DVME-624	30.00
UM-DVME-626	30.00
UM-DVME-628	30.00
UM-DVME-641	30.00
UM-DVME-643	30.00
UM-DVME-645	30.00
UM-DVME-660	30.00
UM-DVME-691	10.00
UM-PM-5050	30.00
UM-PM-5060	30.00
UM-PM-5080	30.00
UM-ST-519	10.00
UM-ST-701	30.00
UM-ST-702	30.00
UM-ST-703	30.00
UM-ST-705	10.00
UM-ST-711/732	30.00
UM-ST-716	30.00
UM-ST-724	30.00
UM-ST-728	30.00
UPA-12/200	18.00
UPA-5/500	16.50
UPM-12/80-D5	44.00
UPM-24/125-D12	79.00
UPM-24/210-D12	84.00
UPM-24/210-D5	84.00
UPM-24/40-D12	43.00
UPM-24/40-D5	43.00
UPM-28/100-D12	73.00
UPM-28/100-D5	73.00
UPM-28/25-D12	43.00
UPM-28/25-D5	43.00
UPM-5/1000	79.00
UPM-5/1000B	67.00
UPM-5/200-D12	44.00
UPM-5/200-D28	44.00
UPM-5/2000	89.00
UPM-5/250	60.00
UPM-5/500	64.00
UPS-12/1250-D12	119.00
UPS-12/1250-D24	119.00
UPS-12/250-D28	81.00
UPS-12/250-D5	81.00
UPS-12/2500-D12	159.00
UPS-12/2500-D24	159.00
UPS-12/470-D24	107.00
UPS-12/470-D5	107.00
UPS-12/80-D5	42.00
UPS-15/1000-D12	119.00
UPS-15/1000-D24	119.00
UPS-15/2000-D12	159.00
UPS-15/2000-D24	159.00
UPS-15/65-D5	42.00
UPS-5/1000-D12	107.00
UPS-5/1000-D24	107.00
UPS-5/1000-D28	107.00
UPS-5/2000-D24	134.00
UPS-5/2000-D28	134.00
UPS-5/2000-D48	134.00
UPS-5/3000-D12	119.00
UPS-5/3000-D24	119.00
UPS-5/5000-D12	159.00
UPS-5/5000-D24	159.00
UPS-5/600-D12	81.00
UPS-5/600-D28	81.00
UPS-5/600-D5	81.00
USC-5/3	135.00
USC-5/5	144.00
USM-5/3	135.00
USM-5/5	144.00
VFQ-1C	4.50
VFQ-1R	12.00
VFQ-2C	11.65
VFQ-3C	2.65
VI-7660-1	2.10
VI-7660-2	3.00
VR-182A	1.10
VR-182B	1.35
VR-182C	1.55

ACCESSORIES

ADC-12/2 VME	550.00
ADC-12/20 VME	295.00
ADC-12/4 VME	450.00
ADC-12/4-U VME	450.00
ADC-16/35 VME	695.00
ADC-16/35-U VME	695.00
ADC-16/400K VME	395.00
APP-TR1A	130.00
APP-TR1D	130.00
APP-TR1E	130.00
APP-TR2A	130.00
APP-TR2D	130.00
APP-TR2E	130.00
APP-TR5A	130.00
APP-TR5D	130.00
APP-TR5E	130.00
BPM-15/220-D5	115.00
32-2242568	55.00
32-2242570	35.00
32-2242572	35.00
33-8193200	10.00
33-8193205	10.00
38-8193022	36.00
38-8193900	54.00
38-8193901	59.00
38-8193902	17.00
39-2106705	5.00
39-7267690	27.00
39-7341560	20.00
39-8194910	11.00
58-12140-50	6.95
58-2073078	6.00
58-2073082	4.00
58-2073083	5.00
58-2075010	5.00
60-2105600	62.00

DESCRIPTION OF ACCESSORIES

32-2242568	48 Column Printer Paper; 10 Rolls
32-2242570	DPP-Q7 Printer Paper; 10 Rolls
32-2242572	20 Column Printer Paper; 10 Rolls
33-8193200	DPP-Q7/APP-20 Stand Kit
33-8193205	APP-48 Stand Kit
38-8193022	DVC-8500 Panel Mount Kit
38-8193900	DVC-8500 10:1 Attenuator
38-8193901	DVC-8500 100:1 Attenuator
38-8193902	DVC-8500 Test Lead Set
39-2106705	DM-LX3/DM-31 14 Pin DIP Connector
39-7267690	DVC-350A Accessory Kit (AC Recharger and NiCad Battery)
39-7341560	DM-9000 Screw Terminal Connector
39-8194910	DM-31 Accessory Kit (Bezel, Connector, and Mounting Hardware)
58-1214050	Data Acquisition Handbook
58-2073078	DM-9000 Solder Tab Connector
58-2073082	DPM Connector; 10 Pin
58-2073083	DPM Connector; 15 Pin
58-2075010	DPM Connector; 18 Pin
60-2105600	ST-702 and ST-705 Detachable Screw Terminal Connector (Formerly 6012474-1)

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