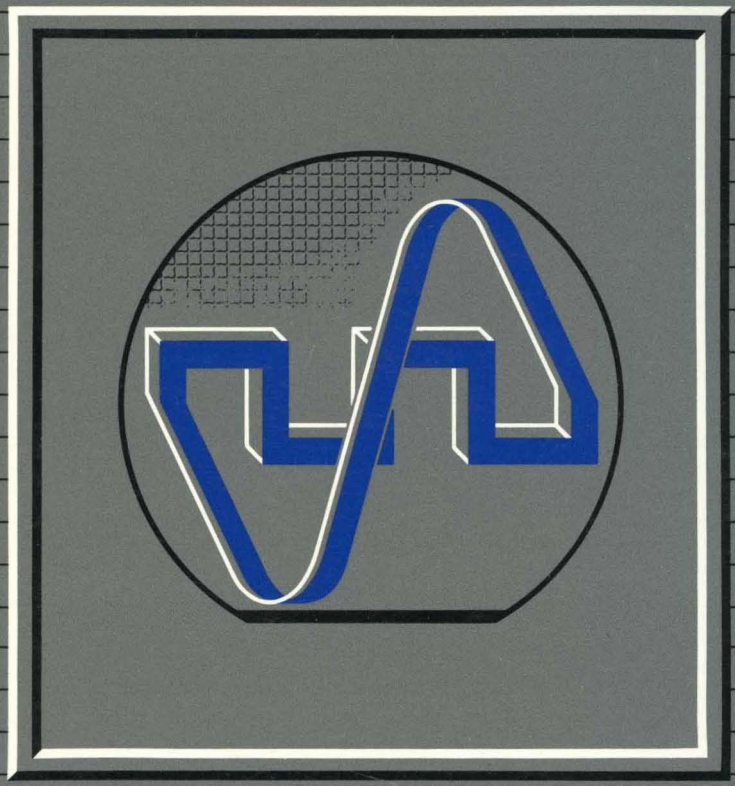
SPT

Honeywell

ANALOG PRODUCT CATALOG

January 1988

SIGNAL PROCESSING TECHNOLOGIES



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JANUARY 1988

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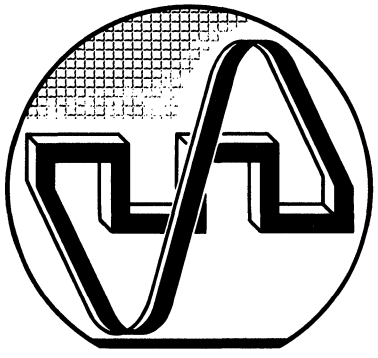

Honeywell

SIGNAL PROCESSING TECHNOLOGIES

JANUARY 1988 ANALOG PRODUCT CATALOG

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GENERAL DISCLAIMER

This data book presents technical data for a wide variety of integrated circuits and has been organized into sections by product type. Additional sections include product selection guides, ordering information, package specifications, quality flows and application notes.

There are three types of data sheets in this book:

ADVANCE INFORMATION — These data sheets contain the description of products that are in development. The specifications are based on engineering calculations, computer simulations and/or initial prototype evaluation.

PRELIMINARY — These data sheets contain minimum and maximum specifications that are based upon initial device characterization. These limits are subject to change upon the completion of full characterization over the specified temperature and supply voltage ranges.

FINAL — These data sheets contain specifications based on a complete characterization of the device over the specified temperature and supply voltage ranges.

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TABLE OF CONTENTS

PRODUCT SELECTION GUIDE

A/D CONVERTERS

PART NO.	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CONVERSION TIME (μs)	LOGIC FAMILY	LINEARITY INT	LINEARITY DIF	FEATURES
HADC 77300A	8	250		ECL	½	½	PIN COMPATABLE WITH HADC77200 IMPROVED ANALOG PERFORMANCE
HADC 77300B	8	250		ECL	¾	¾	
HADC 77200A	8	150		ECL	½	½	DATA READY AND OVERRANGE OUTPUTS, QUARTER POINT LADDER TAPS, IMPROVED ANALOG PERFORMANCE
HADC 77200B	8	150		ECL	¾	¾	
HADC 77100A	8	150		ECL	½	½	PRE AMPLIFIER DESIGN
HADC 77100B	8	150		ECL	¾	¾	
HADC 77600	10	50		ECL	1	½	ON BOARD BUFFER, METASTABLE STATE ERROR REDUCTION
HADC 674A	12		15	TTL	½	½	S/H FUNCTION, LOW POWER, NO NEGATIVE SUPPLY REQUIRED, NO TRANSIENTS AT INPUT, FULL BIPOLAR INPUT, ALTERNATES FOR HI574, HI 674 AND AD574
HADC 674B	12		15	TTL	½	½	
HADC 674C	12		15	TTL	1	1	
HADC 574A	12		25	TTL	½	½	
HADC 574B	12		25	TTL	½	½	
HADC 574C	12		25	TTL	1	1	

D/A CONVERTERS

PART NO.	RESOLUTION (BITS)	UPDATE RATE (MSPS)	SETTLING TIME (ns)	LOGIC FAMILY	LINEARITY INT	LINEARITY DIF	FEATURES
HDAC 34020	4	100	4	TTL	½	½	TRIPLE 4-BIT, REF, VIDEO CONTROL
HDAC 34010	4	200	4	ECL	½	½	TRIPLE 4-BIT, REF, VIDEO CONTROL
HDAM 51100	8	125	3	ECL	½	½	512 X 8 PALETTE, REF, VIDEO CONTROL
HDAC 51600	8	165 (250 TYP)	3	TTL	½	½	5:1, 4:1, MUX, REF, VIDEO CONTROL
HDAC 10180B	8	180	3	ECL	½	½	VIDEO CONTROL, ALTERNATE FOR TDC 1018
HDAC 10181B	8	180	3	ECL	½	½	REF, VIDEO CONTROL
HDAM 51200	8	200	3	ECL	½	½	512 X 8 PALETTE, REF, VIDEO CONTROL
HDAC 97000	8	200	10	ECL	½	½	REF, ALTERNATE FOR AD9700
HDAC 10180A	8	275	3	ECL	½	½	VIDEO CONTROL, ALTERNATE FOR TDC 1018
HDAC 10181A	8	275	3	ECL	½	½	REF, VIDEO CONTROL
HDAC 51400	8	385	3	ECL	½	½	REF, VIDEO CONTROL
HDAC 7541Z	12		500	TTL	½	½	ALTERNATE FOR AD7541A
HDAC 7542A	12		500	TTL	½	½	ALTERNATE FOR AD7542
HDAC 7543A	12		500	TTL	½	½	ALTERNATE FOR AD7543
HDAC 7545A	12		500	TTL	½	½	ALTERNATE FOR AD7545
HDAC 50500	12		500	TTL	½	½	MICROPROCESSOR INTERFACE
HDAC 50600	14		500	TTL	½	½	PARALLEL INPUT
HDAC 50800	14		500	TTL	½	½	2 BYTE INPUT
HDAC 52160	16		100	TTL	½	½	PARALLEL INPUT

COMPARATORS

PART NO.	t_r/t_f (ns)	PROP DELAY (ns)	V_{CM} (V)	V_{OS} (mV)	R_{IN} (kΩ)	AV (V/V)	FEATURES
HCMP 96850	1.76/1.72	3.0	±2.5V	±3.0	60	4k	SYMETRICAL t_r/t_f, ALTERNATE FOR SP9685, AM6685
HCMP 96870A	1.2/1.2	2.3	±2.5	±3.0	60	4k	HIGH PERFORMANCE, ALTERNATE FOR SP9687, AM6687
HCMP 96900	1.6/1.6	4.2	+10 −3	±0.5	10,000	1k	HIGH Vcm RANGE, SYMETRICAL t_r/t_f AND PROP DELAY INDEPENDENT OF OVERDRIVE AND Vcm

INSTRUMENTATION AMPLIFIERS

PART NO.	NON-LINEARITY	V_{OS} (μV)	GAIN BANDWIDTH (MHz)	SUPPLY VOLTAGE (V)	FEATURES
HINA 522	.001% MAX AV = 1	25		±15	ALTERNATE SOURCES FOR ANALOG DEVICES MONOLITHIC CONSTRUCTION
HINA 524	.003% MAX AV = 1	25	25 AV = 1000	±15	
HINA 624	.001% MAX AV = 1	25	25 AV = 1000	±15	

FILTER

PART NO.	DYNAMIC RANGE (dB)	MAX BANDEDGE (kHz)	BANDEDGE TOLERANCE (%)	SUPPLY VOLTAGE (V)	FEATURES
HSCF 24040	85	20	±0.5	±5	7TH ORDER LOW PASS, >76dB STOPBAND ATTENUATION, ON CHIP ANTIALIAS FILTER, DIGITALLY PROGRAMMABLE BANDEDGE AND DC GAIN

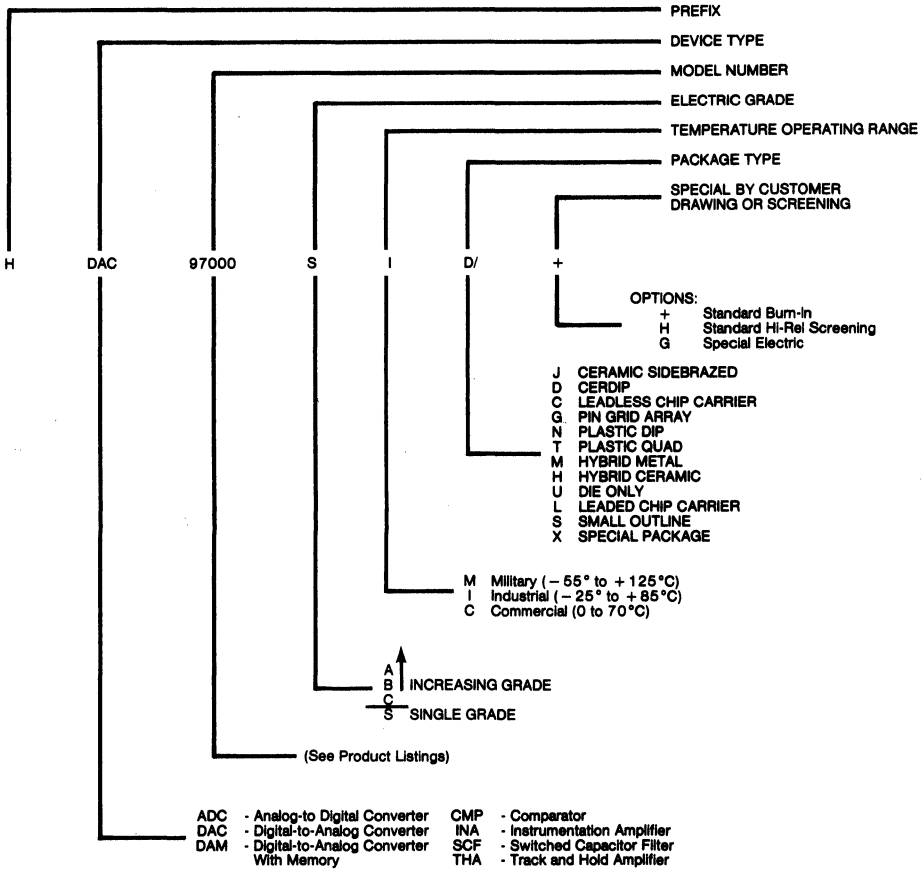
EVALUATION BOARDS	FEATURED PRODUCT	FEATURES
EB 100	HADC77100	150MSPS A/D, D/A
EB 101	HADC77200	150MSPS A/D, D/A
EB 102	N/A	100MHz BUFFER AMP, 8-BITS
EB 103	HADC77200/77300	300MSPS A/D, D/A PING-PONG
EB 104	HADC574/674	A/D, D/A, OPTIONAL S/H
EB 105	HSCF24040	ON-BOARD OR EXTERNAL PROGRAMMING

PRODUCT CROSS REFERENCE GUIDE

INDUSTRY PART NO.	SPT EQUIVALENT
AD522AD	HINA522BIJ
AD522BD	HINA522AIJ
AD522SD	HINA522BMJ
AD524AD	HINA524CIJ
AD524BD	HINA524BIJ
AD524CD	HINA524AIJ
AD524SD	HINA524CMJ
AD574AJD	HADC574ZCCJ
AD574AJN	HADC574ZCCN
AD574AKD	HADC574ZBCJ
AD574AKN	HADC574ZBCN
AD574ALD	HADC574ZACJ
AD574ALN	HADC574ZACN
AD624AD	HINA624CIJ
AD624BD	HINA624BIJ
AD624CD	HINA624AIJ
AD624SD	HINA624CMJ
AD7541AAQ	HDAC7541ZBID
AD7541ABQ	HDAC7541ZAID
AD7541ACHIPS	HDAC7541ZBCU
AD7541AJN	HDAC7541ZBCN
AD7541AKN	HDAC7541ZACN
AD7541ASD	HDAC7541ZBMD
AD7541ATD	HDAC7541ZAMD
AD7542AD	HDAC7542ABID
AD7542BD	HDAC7542AAID
AD7542CHIPS	HDAC7542ABCU
AD7542GBD	HDAC7542AAID/G
AD7542GKN	HDAC7542AACN/G
AD7542GTD	HDAC7542AAMD/G
AD7542JN	HDAC7542ABCN
AD7542KN	HDAC7542AACN
AD7542SD	HDAC7542ABMD
AD7542TD	HDAC7542AAMD
AD7543AD	HDAC7543ABID
AD7543BD	HDAC7543AAID
AD7543CHIPS	HDAC7543ABCU
AD7543GBD	HDAC7543AAID/G
AD7543GKN	HDAC7543AACN/G
AD7543GTD	HDAC7543AAMD/G
AD7543JN	HDAC7543ABCN
AD7543KN	HDAC7543AACN
AD7543SD	HDAC7543ABMD
AD7543TD	HDAC7543AAMD

INDUSTRY PART NO.	SPT EQUIVALENT
AD7545AQ	HDAC7545ABID
AD7545BQ	HDAC7545ABID
AD7545CHIPS	HDAC7545ABCU
AD7545CQ	HDAC7545AAID
AD7545GCQ	HDAC7545AAID/G
AD7545GLN	HDAC7545AACN/G
AD7545GUD	HDAC7545AAMD/G
AD7545JN	HDAC7545ABCN
AD7545KN	HDAC7545ABCN
AD7545LN	HDAC7545AACN
AD7545SD	HDAC7545ABMD
AD7545TD	HDAC7545ABMD
AD7545UD	HDAC7545AAMD
AD9700D22A	HDAC97000SJM
AM6685DL	HCMP96850SID
AM6687DL	HCMP96870SID
AM6687LL	HCMP96870SIC
CXO2116	HADC77100AIJ
HI1-574AJD-5	HADC574ZCCJ
HI1-574AKD-5	HADC574ZBCJ
HI1-574ALD-5	HADC574ZACJ
HI1-674AJD-5	HADC674ZCCJ
HI1-674AKD-5	HADC674ZBCJ
HI1-674ALD-5	HADC674ZACJ
MP7542	HDAC7542ABCU
MP7542AD	HDAC7542ABID
MP7542BD	HDAC7542AAID
MP7542JN	HDAC7542ABCN
MP7542KN	HDAC7542AACN
MP7542SD	HDAC7542ABMD
MP7542TD	HDAC7542AAMD
MP7543	HDAC7543ABCU
MP7543AD	HDAC7543ABID
MP7543BD	HDAC7543AAID
MP7543JN	HDAC7543ABCN
MP7543KN	HDAC7543AACN
MP7543SD	HDAC7543ABMD
MP7543TD	HDAC7543AAMD
MP7545	HDAC7545ABCU
MP7545AD	HDAC7545ABID
MP7545BD	HDAC7545ABID
MP7545CD	HDAC7545AAID
MP7545JN	HDAC7545ABCN
MP7545KN	HDAC7545ABCN

INDUSTRY PART NO.	SPT EQUIVALENT
MP7545LN	HDAC7545AACN
MP7545SD	HDAC7545ABMD
MP7545TD	HDAC7545ABMD
MP7545UD	HDAC7545AAMD
MP7623	HDAC7541ZCCU
MP7623AD	HDAC7541ZBID
MP7623BD	HDAC7541ZAID
MP7623JN	HDAC7541ZBCN
MP7623KN	HDAC7541ZACN
MP7623SD	HDAC7541ZBMD
MP7623TD	HDAC7541ZAMD
PM7542AQ	HDAC7542AAMD/G
PM7542BQ	HDAC7542AAMD
PM7542BQ	HDAC7542ABMD
PM7542EQ	HDAC7542AAID/G
PM7542FQ	HDAC7542AAID
PM7542FQ	HDAC7542ABID
PM7542G	HDAC7542ABCU
PM7542GP	HDAC7542AACN/G
PM7542HP	HDAC7542AACN
PM7542HP	HDAC7542ABCN
PM7543AQ	HDAC7543AAMD/G
PM7543BQ	HDAC7543AAMD
PM7543BQ	HDAC7543ABMD
PM7543EQ	HDAC7543AAID/G
PM7543FQ	HDAC7543AAID
PM7543FQ	HDAC7543ABID
PM7543G	HDAC7543ABCU
PM7543GP	HDAC7543AACN/G
PM7543HP	HDAC7543AACN
PM7543HP	HDAC7543ABCN
PM7545AR	HDAC7545AAMD/G
PM7545BR	HDAC7545AAMD
PM7545BR	HDAC7545ABMD
PM7545ER	HDAC7545AAID/G
PM7545FR	HDAC7545AAID
PM7545FR	HDAC7545ABID
PM7545G	HDAC7545ABCU
PM7545GP	HDAC7545AACN/G
PM7545HP	HDAC7545AACN
PM7545HP	HDAC7545ABCN
SP9685DG16	HCMP96850SID
SP9687DG16	HCMP96870AID
TDC1018J7C	HDAC10180AMJ


PREFIX
DEVICE TYPE
MODEL NUMBER
ELECTRIC GRADE
TEMPERATURE OPERATING RANGE
PACKAGE TYPE
SPECIAL BY CUSTOMER DRAWING OR SCREENING
H
DAC
97000
S
I
D/
+
OPTIONS:
+ Standard Burn-In
H Standard Hi-Rel Screening
G Special Electric
J CERAMIC SIDEBRAZED
D CERDIP
C LEADLESS CHIP CARRIER
G PIN GRID ARRAY
N PLASTIC DIP
T PLASTIC QUAD
M HYBRID METAL
H HYBRID CERAMIC
U DIE ONLY
L LEADED CHIP CARRIER
S SMALL OUTLINE
X SPECIAL PACKAGE
M Military (– 55° to + 125°C)
I Industrial (– 25° to + 85°C)
C Commercial (0 to 70°C)
A
B
C
S
INCREASING GRADE
SINGLE GRADE
(See Product Listings)
ADC - Analog-to Digital Converter
DAC - Digital-to-Analog Converter
DAM - Digital-to-Analog Converter With Memory
CMP - Comparator
INA - Instrumentation Amplifier
SCF - Switched Capacitor Filter
THA - Track and Hold Amplifier

ORDERING INFORMATION

ANALOG TO DIGITAL CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE
HADC574ZACN	12-BIT RES ADC; 12-BIT LIN	PLASTIC*	28	COMMERCIAL
HADC574ZBCN	12-BIT RES ADC; 12-BIT LIN	PLASTIC*	28	COMMERCIAL
HADC574ZCCN	12-BIT RES ADC; 11-BIT LIN	PLASTIC*	28	COMMERCIAL
HADC574ZACJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC574ZBCJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC574ZCCJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC574ZAMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC574ZBMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC574ZCMJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	MILITARY
HADC574ZCCU	12-BIT RES ADC; 11-BIT LIN	DIE		+25°C
HADC674ZACN	12-BIT RES ADC; 12-BIT LIN	PLASTIC*	28	COMMERCIAL
HADC674ZBCN	12-BIT RES ADC; 12-BIT LIN	PLASTIC*	28	COMMERCIAL
HADC674ZCCN	12-BIT RES ADC; 11-BIT LIN	PLASTIC*	28	COMMERCIAL
HADC674ZACJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC674ZBCJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC674ZCCJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC674ZAMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC674ZBMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC674ZCMJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	MILITARY
HADC674ZCCU	12-BIT RES ADC; 11-BIT LIN	DIE		+25°C
HADC77100AIJ	8-BIT, 150 MSPS ADC ± ½ LSB	SIDEBRAZED	42	INDUSTRIAL
HADC77100AMJ	8-BIT, 150 MSPS ADC ± ½ LSB	SIDEBRAZED	42	MILITARY
HADC77100AMJ/MIL	8-BIT, 150 MSPS ADC ± ½ LSB	SIDEBRAZED	42	MILITARY
HADC77100BIJ	8-BIT, 150 MSPS ADC ± ¾ LSB	SIDEBRAZED	42	INDUSTRIAL
HADC77100BMJ	8-BIT, 150 MSPS ADC ± ¾ LSB	SIDEBRAZED	42	MILITARY
HADC77100AIG	8-BIT, 150 MSPS ADC ± ½ LSB	PGA	46	INDUSTRIAL
HADC77100AMG	8-BIT, 150 MSPS ADC ± ½ LSB	PGA	46	MILITARY
HADC77100AMJ/MIL	8-BIT, 150 MSPS ADC ± ½ LSB	PGA	46	MILITARY
HADC77100BIG	8-BIT, 150 MSPS ADC ± ¾ LSB	PGA	46	INDUSTRIAL
HADC77100BMG	8-BIT, 150 MSPS ADC ± ¾ LSB	PGA	46	MILITARY
HADC77200AIJ	8-BIT, 150 MSPS ADC ± ½ LSB	SIDEBRAZED	48	INDUSTRIAL
HADC77200AMJ	8-BIT, 150 MSPS ADC ± ½ LSB	SIDEBRAZED	48	MILITARY
HADC77200AMG/MIL	8-BIT, 150 MSPS ADC ± ½ LSB	SIDEBRAZED	48	MILITARY
HADC77200BIJ	8-BIT, 150 MSPS ADC ± ¾ LSB	SIDEBRAZED	48	INDUSTRIAL
HADC77200BMJ	8-BIT, 150 MSPS ADC ± ¾ LSB	SIDEBRAZED	48	MILITARY
HADC77200AIG	8-BIT, 150 MSPS ADC ± ½ LSB	PGA	46	INDUSTRIAL
HADC77200AMG	8-BIT, 150 MSPS ADC ± ½ LSB	PGA	46	MILITARY
HADC77200AMJ/MIL	8-BIT, 150 MSPS ADC ± ½ LSB	PGA	46	MILITARY
HADC77200BIG	8-BIT, 150 MSPS ADC ± ¾ LSB	PGA	46	INDUSTRIAL
HADC77200BMG	8-BIT, 150 MSPS ADC ± ¾ LSB	PGA	46	MILITARY
HADC77300ACG	8-BIT, 250 MSPS ADC ± ½ LSB	PGA	46	COMMERCIAL
HADC77300BCG	8-BIT, 250 MSPS ADC ± ¾ LSB	PGA	46	COMMERCIAL
HADC77600SCG	10-BIT, 50 MSPS ADC ± ½ LSB	PGA	72	COMMERCIAL
HADC77600SIG	10-BIT, 50 MSPS ADC ± ½ LSB	PGA	72	INDUSTRIAL
HADC77600SMG	10-BIT, 50 MSPS ADC ± ½ LSB	PGA	72	MILITARY
HADC78160	CONTACT FACTORY FOR ORDERING INFORMATION			

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DIGITAL TO ANALOG CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE
HDAC10180AID	8-BIT, 275 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180AMJ	8-BIT, 275 MWPS DAC	SIDEBRAZED	24	MILITARY
HDAC10180BID	8-BIT, 165 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180BMJ	8-BIT, 165 MWPS DAC	SIDEBRAZED	24	MILITARY
HDAC10181AID	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181AMJ	8-BIT, 275 MWPS DAC W/REF	SIDEBRAZED	24	MILITARY
HDAC10181BID	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181BMJ	8-BIT, 165 MWPS DAC W/REF	SIDEBRAZED	24	MILITARY
HDAC34010SCJ	3 X 4-BIT DAC, 200 MWPS	SIDEBRAZED	28	COMMERCIAL
HDAC34020SCJ	3 X 4-BIT DAC, 100 MWPS	SIDEBRAZED	28	COMMERCIAL
HDAC50500ACN/G	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	20	COMMERCIAL
HDAC50500ACN	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	20	COMMERCIAL
HDAC50500BCN	12-BIT RES DAC; 11-BIT LIN	PLASTIC*	20	COMMERCIAL
HDAC50500AID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC50500AID	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC50500BID	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC50500AMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	MILITARY
HDAC50500AMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	MILITARY
HDAC50500BMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	MILITARY
HDAC50500BCU	12-BIT RES DAC; 11-BIT LIN	DIE		+25°C
HDAC50600AID	14-BIT RES DAC; 14-BIT LIN	CERDIP	28	INDUSTRIAL
HDAC50600BID	14-BIT RES DAC; 13-BIT LIN	CERDIP	28	INDUSTRIAL
HDAC50600AMD	14-BIT RES DAC; 14-BIT LIN	CERDIP	28	MILITARY
HDAC50600BMD	14-BIT RES DAC; 13-BIT LIN	CERDIP	28	MILITARY
HDAC50600BCU	14-BIT RES DAC; 13-BIT LIN	DIE		+25°C
HDAC50800AID	14-BIT RES DAC; 14-BIT LIN	CERDIP	24	INDUSTRIAL
HDAC50800BID	14-BIT RES DAC; 13-BIT LIN	CERDIP	24	INDUSTRIAL
HDAC50800AMD	14-BIT RES DAC; 14-BIT LIN	CERDIP	24	MILITARY
HDAC50800BMD	14-BIT RES DAC; 13-BIT LIN	CERDIP	24	MILITARY
HDAC50800BCU	14-BIT RES DAC; 13-BIT LIN	DIE		+25°C
HDAC51400SIJ	8-BIT, 385 MWPS DAC W/REF	SIDEBRAZED	24	INDUSTRIAL
HDAC51400SMJ	8-BIT, 385 MWPS DAC W/REF	SIDEBRAZED	24	MILITARY
HDAC51600SCG	8-BIT, 165 MWPS DAC	PGA	72	COMMERCIAL
HDAC52160SCG	CONTACT FACTORY FOR ORDERING INFORMATION			
HDAC7541ZACN	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	18	COMMERCIAL
HDAC7541ZBCN	12-BIT RES DAC; 11-BIT LIN	PLASTIC*	18	COMMERCIAL
HDAC7541ZAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7541ZBID	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7541ZAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	MILITARY
HDAC7541ZBMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	MILITARY
HDAC7541ZBCU	12-BIT RES DAC; 11-BIT LIN	DIE		+25°C

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DIGITAL TO ANALOG CONVERTERS CONTINUED

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE
HDAC7542AACN/G	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	16	COMMERCIAL
HDAC7542AACN	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	16	COMMERCIAL
HDAC7542ABCN	12-BIT RES DAC; 11-BIT LIN	PLASTIC*	16	COMMERCIAL
HDAC7542AAID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	INDUSTRIAL
HDAC7542AAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	INDUSTRIAL
HDAC7542ABID	12-BIT RES DAC; 11-BIT LIN	CERDIP	16	INDUSTRIAL
HDAC7542AAMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	MILITARY
HDAC7542AAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	MILITARY
HDDC7542ABMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	16	MILITARY
HDAC7542ABCU	12-BIT RES DAC; 11-BIT LIN	DIE		+25°C
HDAC7543AACN/G	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	16	COMMERCIAL
HDAC7543AACN	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	16	COMMERCIAL
HDAC7543ABCN	12-BIT RES DAC; 11-BIT LIN	PLASTIC*	16	COMMERCIAL
HDAC7543AAID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	INDUSTRIAL
HDAC7543AAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	INDUSTRIAL
HDAC7543ABID	12-BIT RES DAC; 11-BIT LIN	CERDIP	16	INDUSTRIAL
HDAC7543AAMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	MILITARY
HDAC7543AAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	16	MILITARY
HDAC7543ABMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	16	MILITARY
HDAC7543ABCU	12-BIT RES DAC; 11-BIT LIN	DIE		+25°C
HDAC7545AACN/G	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	20	COMMERCIAL
HDAC7545AACN	12-BIT RES DAC; 12-BIT LIN	PLASTIC*	20	COMMERCIAL
HDAC7545ABCN	12-BIT RES DAC; 11-BIT LIN	PLASTIC*	20	COMMERCIAL
HDAC7545AAID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC7545AAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC7545ABID	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC7545AAMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	MILITARY
HDAC7545AAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	MILITARY
HDAC7545ABMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	MILITARY
HDAC7545ABCU	12-BIT RES DAC; 11-BIT LIN	DIE		+25°C
HDAC97000SIJ	8-BIT, 200 MWPS DAC W/REF	SIDEBRAZED	22	INDUSTRIAL
HDAC97000SID	8-BIT, 200 MWPS DAC W/REF	CERDIP	22	INDUSTRIAL
HDAC97000SMJ	8-BIT, 200 MWPS DAC W/REF	SIDEBRAZED	22	MILITARY
HDAM51100SCG	125MHz W/512 X 8 MEMORY	PGA	46	COMMERCIAL

*HONEYWELL RESERVES THE RIGHT TO SHIP CERDIP IN LIEU OF PLASTIC PACKAGES.

COMPARATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE
HCMP96850SID	HIGH SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96850SCU	HIGH SPEED COMPARATOR	DIE		+25°C
HCMP96870AID	DUAL HIGH SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96870AIC	DUAL HIGH SPEED COMPARATOR	LCC	20	INDUSTRIAL
HCMP96870AIJ	DUAL HIGH SPEED COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
HCMP96870ACU	DUAL HIGH SPEED COMPARATOR	DIE		+25°C
HCMP96900	CONTACT FACTORY FOR ORDERING INFORMATION			

INSTRUMENTATION AMPLIFIER

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE
HINA522AIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	14	INDUSTRIAL
HINA522BIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	14	INDUSTRIAL
HINA522BMJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	14	MILITARY
HINA522BCU	INSTRUMENTATION AMPLIFIER	DIE		+25°C
HINA524AIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	INDUSTRIAL
HINA524BIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	INDUSTRIAL
HINA524CIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	INDUSTRIAL
HINA524CMJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	MILITARY
HINA524CCU	INSTRUMENTATION AMPLIFIER	DIE		+25°C
HINA624AIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	INDUSTRIAL
HINA624BIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	INDUSTRIAL
HINA624CIJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	INDUSTRIAL
HINA624CMJ	INSTRUMENTATION AMPLIFIER	SIDEBRAZED	16	MILITARY
HINA624CCU	12-BIT INSTRUMENTATION AMPLIFIER	DIE		+25°C

SPECIAL FUNCTIONS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE
HTHA27140	CONTACT FACTORY FOR ORDERING INFORMATION			
HSCF24040ACN	7 POLE LOW PASS SC FILTER	PLASTIC*	32	COMMERCIAL
HSCF24040ACJ	7 POLE LOW PASS SC FILTER	SIDEBRAZED	32	COMMERCIAL
HSCF24040AMJ	7 POLE LOW PASS SC FILTER	SIDEBRAZED	32	MILITARY
HSCF24040CCU	7 POLE LOW PASS SC FILTER	DIE		+25°C

EVALUATION BOARDS

PART NUMBER	DESCRIPTION
EB100A	HADC77100AIJ DEMO BOARD
EB100B	HADC77100BIJ DEMO BOARD
EB101A	HADC77200AIJ DEMO BOARD
EB101B	HADC77200BIJ DEMO BOARD
EB102A	CLC221 BUFFER BOARD
EB102B	CLC231 BUFFER BOARD
EB103	HADC77200/77300 PING-PONG BOARD
EB104	HADC574 DEMO BOARD
EB105	HSCF24040 DEMO BOARD

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HADC574Z

FAST, COMPLETE 12-BIT μP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

PRELIMINARY INFORMATION

FEATURES:

- **IMPROVED PIN-TO-PIN COMPATIBLE MONOLITHIC VERSION OF THE HI574A AND AD574A**
- **Complete 12-bit A/D Converter with Sample-Hold, Reference and Clock**
- **Low Power Dissipation (150mW Max)**
- 12-bit Linearity (over temp)
- 25μs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS:

- **MILITARY/INDUSTRIAL DATA ACQUISITION SYSTEMS**
- 8 OR 12-bit μP Input Functions
- Process Control Systems
- Test And Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC574Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI574A and AD574A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC574Z features 25μs (Max) conversion time of 10 or 20 Volt input signals. Also, a 3-state output buffer is added for direct interface to an 8-, 12-, or 16-bit μP bus.

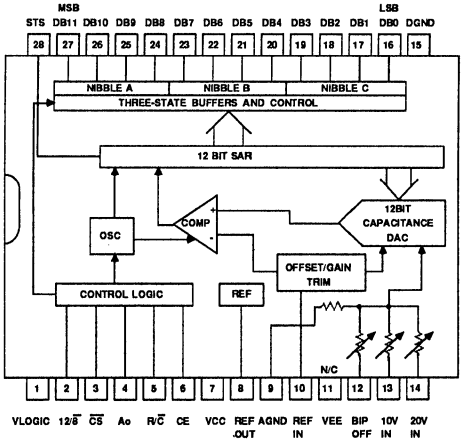
The HADC574Z is manufactured on Honeywell SPT's Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC574Z has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (V_{CC} to DGND)...0 to +16.5V
Logic Supply Voltage (V_{LOGIC} to DGND).....0 to +7V
Analog to Digital Ground (AGND to DGND)...-0.5 to +1V

Input Voltages
Control Input Voltages (to DGND).
(CE, $\overline{CS}$, Ao, 12/8, R/$\overline{C}$).....-0.5 to V_{LOGIC} +0.5V
Analog Input Voltage (to AGND).....±16.5V
(REF IN, BIP OFF, 10Vin)
20V Vin Input Voltage (to AGND).....±24V

Output
Reference Output Voltage.....Indefinite short to GND
Momentary short to V_{CC}

Temperature
Operating Temperature, ambient.-55 to +125(case) °C
junction.....+175 °C
Lead Temperature, (soldering 10 seconds).....+300 °C
Storage Temperature.....-65 to +150 °C
Power Dissipation.....1000mW
Thermal Resistance (θ_{jA}).....48°C/W

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE 0 TO +70°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCC MIN	HADC574ZCC TYP	HADC574ZCC MAX	HADC574ZBC MIN	HADC574ZBC TYP	HADC574ZBC MAX	HADC574ZAC MIN	HADC574ZAC TYP	HADC574ZAC MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution				12			12			12		BITS
Linearity Error	Tmin to Tmax	I			±1			±1/2			±1/2	LSB
Differential Linearity Error	Tmin to Tmax	I			±1			±1/2			±1/2	LSB
Unipolar Offset	Adjustable to zero	I		±.1	±2		±.1	±2		±.1	±2	LSB
Bipolar Offset[1]	Adjustable to zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[1]		I			0.3			0.3			0.3	% of FS
	No adjustment at +25°C Tmin to Tmax	II		0.5			0.4			0.35		% of FS
	With adjustment at +25°C Tmin to Tmax	II		0.22			0.12			0.05		% of FS
Temperature Coefficients	Using internal reference											
Unipolar Offset		I		±.2	±2 (10)		±.1	±1 (5)		±.1	±1 (5)	LSB (ppm/°C)
Bipolar Offset		I		±.2	±2 (10)		±.1	±1 (5)		±.1	±1 (5)	LSB (ppm/°C)
Full Scale Calibration		I			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

COMMERCIAL TEMPERATURE RANGE 0 TO +70°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCC MIN	HADC574ZCC TYP	HADC574ZCC MAX	HADC574ZBC MIN	HADC574ZBC TYP	HADC574ZBC MAX	HADC574ZAC MIN	HADC574ZAC TYP	HADC574ZAC MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I			±2			±1			±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I			±1/2			±1/2			±1/2	LSB
Analog Inputs Ranges		I	-5		+5	-5		+5	-5		+5	VOLTS
Bipolar			-10		+10	-10		+10	-10		+10	VOLTS
Unipolar		I	0		+10	0		+10	0		+10	VOLTS
			0		+20	0		+20	0		+20	VOLTS
Input Impedance 10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											VOLTS
Operating Current I_{LOGIC}		I		1	3		1	3		1	3	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}		II		0			0			0		mA
Power Dissipation +15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[2]		I			2			2			2	mA

Note 2: Available for external loads, external load should not change during conversion.
When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.

COMMERCIAL TEMPERATURE RANGE 0 TO +70°C

V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCC MIN	HADC574ZCC TYP	HADC574ZCC MAX	HADC574ZBC MIN	HADC574ZBC TYP	HADC574ZBC MAX	HADC574ZAC MIN	HADC574ZAC TYP	HADC574ZAC MAX	UNITS
DIGITAL CHARACTERISTICS The following specifications are guaranteed over the full temperature range.												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "1"[3]		I	2.4		5.5	2.4		5.5	2.4		5.5	VOLTS
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	VOLTS
Current	0 to 5.5V Input	I		± .01	+5		± .01	+5		± .01	+5	µA
Capacitance		II		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6mA)	I			+0.4			+0.4			+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500µA)	I	+2.4			+2.4			+2.4			VOLTS
Leakage	(High Z State, DB11-DB0 Only)	I	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		II		5			5			5		pF

Note 3: Although the guaranteed threshold is higher than the standard TTL threshold (+2 Volts), loading is much less than standard TTL due to the CMOS nature of the inputs.

MILITARY TEMPERATURE RANGE -55 TO +125°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCM MIN	HADC574ZCM TYP	HADC574ZCM MAX	HADC574ZBM MIN	HADC574ZBM TYP	HADC574ZBM MAX	HADC574ZAM MIN	HADC574ZAM TYP	HADC574ZAM MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution					12			12			12	BITS
Linearity Error		I			±1/2			±1/2			±1/2	LSB
Linearity Error	Tmin to Tmax	I			±1/2			±1/2			±1/2	LSB
Differential Linearity Error	Tmin to Tmax	I			±1/2			±1/2			±1/2	LSB
Unipolar Offset	Adjustable to zero	I			±2			±2			±2	LSB
Bipolar Offset[1]	Adjustable to zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[1]		I			0.3			0.3			0.3	% of FS
	No adjustment at +25°C Tmin to Tmax	II		0.8			0.6			0.4		% of FS
	With adjustment at +25°C Tmin to Tmax	II		0.5			0.25			0.12		% of FS
Temperature Coefficients	Using internal reference Tmin to Tmax											
Unipolar Offset		I			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset		I			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration		I			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I			±2			±1			±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I			±1/2			±1/2			±1/2	LSB
Analog Inputs Input Ranges		I	-5		+5	-5		+5	-5		+5	VOLTS
Bipolar		I	-10		+10	-10		+10	-10		+10	VOLTS
Unipolar		I	0		+10	0		+10	0		+10	VOLTS
Unipolar		I	0		+20	0		+20	0		+20	VOLTS
Input Impedance 10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span		I	15	20	25	15	20	25	15	20	25	kΩ

MILITARY TEMPERATURE RANGE -55 TO +125°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCM MIN	HADC574ZCM TYP	HADC574ZCM MAX	HADC574ZBM MIN	HADC574ZBM TYP	HADC574ZBM MAX	HADC574ZAM MIN	HADC574ZAM TYP	HADC574ZAM MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											VOLTS
Operating Current I_{LOGIC}		I		1	3		1	3		1	3	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}		II		0			0			0		mA
Power Dissipation ±15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[4]		I			2			2			2	mA
DIGITAL CHARACTERISTICS	The following specifications are guaranteed over the full temperature range.											
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao,12/$\overline{8}$)												
Logic "1"		I	2.4		5.5	2.4		5.5	2.4		5.5	VOLTS
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	VOLTS
Current	0 to +5.5V Input	I		± .01	+5		± .01	+5		± .01	+5	µA
Capacitance		II		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6mA)	I			+0.4			+0.4			+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500µA)	I	+2.4			+2.4			+2.4			VOLTS
Leakage	(High Z State, DB11- DB0 Only)		-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		II		5			5			5		pF

Note 4: Available for external loads, external load should not change during conversion.
When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

CONVERT MODE TIMING CHARACTERISTICS

Typical @ 25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time 12-Bit Cycle	Tmin to Tmax	I	13	18	25	15	18	25	15	18	25	µs
8-Bit Cycle	Tmin to Tmax	I	10	13	19	10	13	17	10	13	17	µs

Note 5: Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3KΩ load for drive to high impedance.

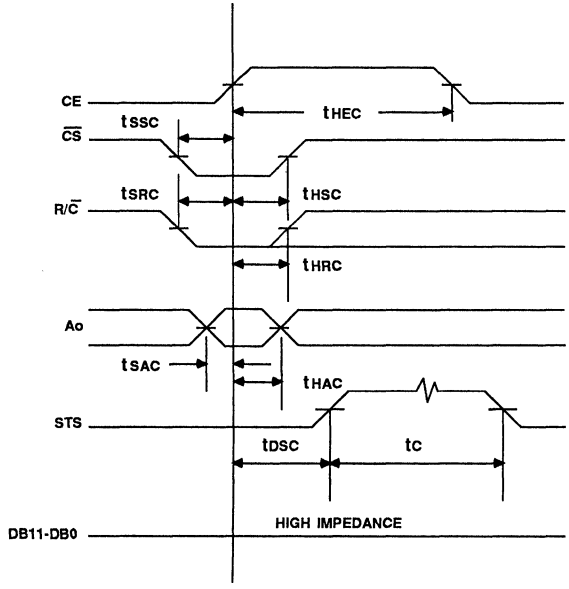


Figure 1 - Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	0	0		0	0		0	0		ns
t_{HAR} Ao Valid After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns

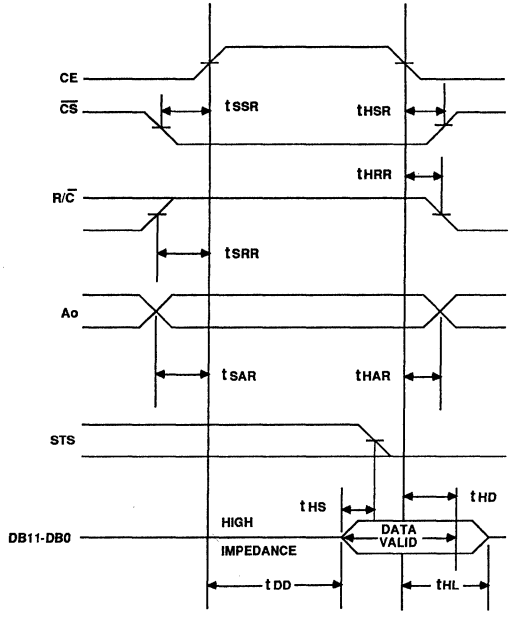


Figure 2 - Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		II	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	µs
Aperture Uncertainty Time		II		20			20			20		ns

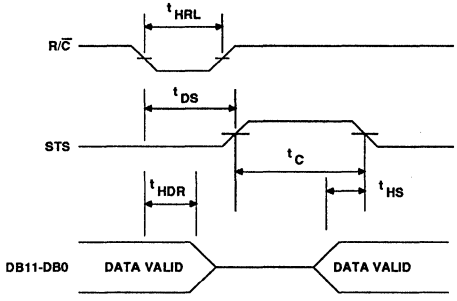


Figure 3 - Low Pulse For R/C - Outputs Enabled After Conversion

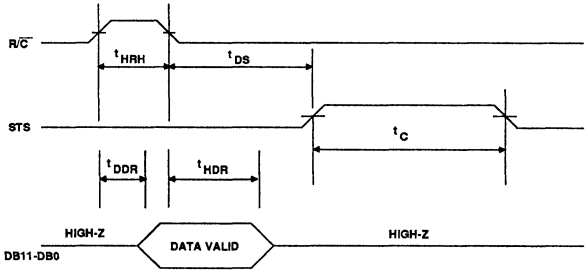


Figure 4 - High Pulse For R/C - Outputs Enabled While R/C is High, Otherwise High Impedance

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_{junc} = T_{case} = T_{ambient}$.

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.
II	Parameter is guaranteed by design and sampled characterization data.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 7). The point used as "zero" occurs 1/2LSB (1.22mV for a 10 Volt span) before the first code transistion (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC574Z A and B grades are guaranteed for maximum nonlinearity of ±1/2LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC574ZCC and CM grades are guaranteed to ±1LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC574Z type BC, AC, BM, and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC574Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 7 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC574Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential non-linearity of -1 LSB. Figure 7 points out two missed codes in the transfer function.

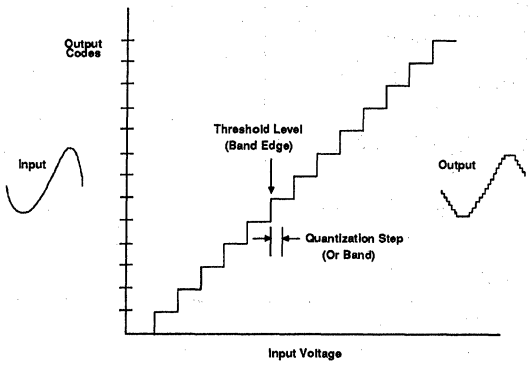


Figure 5 - Static Input Conditions

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can re-present an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = 12. Non- ideal quantization bands represent differential nonlinearity errors (See Figures 5, 6 and 7).

RESOLUTION - ACTUAL VS. AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically posssible to generate 2^N unique output codes.

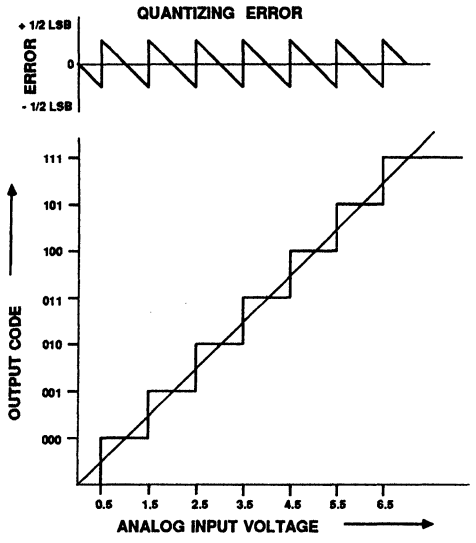


Figure 6 - Quantizing error

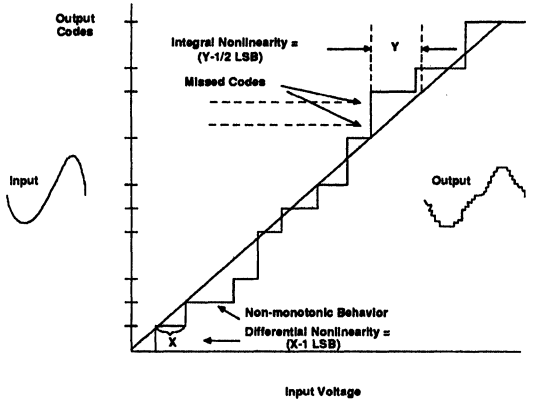


Figure 7 - Dynamic Conditions

THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC574Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC574Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at Tmin or Tmax .

POWER SUPPLY REJECTION

The standard specifications for the HADC574Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC574Z is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC574Z is a complete 12-bit Analog-To-Digital converter which consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample & hold, clock, output buffers and control circuitry to make it possible to use the HADC574Z with few external components.

When the control section of the HADC574Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC574Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the HADC574Z is used with ±12V supplies, or if external current must be supplied over the full temperature range, an

external buffer amplifier is recommended. Any external load on the HADC574Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC574Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC574Z is disconnected from the user's sample and hold. This prevents transients occuring during conversion from being inflicted upon the attached sample and hold buffer. All other 574 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HADC574Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC574Z acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HADC574Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC574Z and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8.) When the R/$\overline{C}$ line makes a negative transition, the HADC574Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

During T_{acq}, the equivalent circuit of the HADC574Z in-put is as shown in Figure 9 (the time constant of the input is independant of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs., there is more than enough time for settling the input to 12 bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the R/$\overline{C}$ transition, T_{acq} is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} = 2.4 µsecs ± 0.6 µsecs. between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC574Z.

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken - i.e. the "aperture jitter" or T_{AJ}. The HADC574Z has a nominal aperture jitter of 20 nsecs. between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 10). The magnitude of this change for a sine-wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, $Sr = 2\pi f Vp$ (Vp = peak voltage, f = frequency of sine wave)
For an N-bit converter to maintain +/- 1/2 LSB accuracy :

$Verr \leq Vfs/2^{N+1}$ (where Verr is the allowable error voltage and Vfs is the full scale voltage)

From Figure 10:

$Sr = \Delta V/\Delta T = 2\pi f Vp$

Let $\Delta V = Verr = V_{fs}2^{-(N+1)}$, Vp = Vin/2 and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

$Vfs/2^{N+1} \geq \pi f Vin\, t_{AJ}$ or $f_{max} \leq Vfs/(\pi Vin\, t_{AJ})2^{N+1}$

For the HADC574Z, $T_{AJ} = 20$ nsec, therefore $f_{max} \leq 2$KHz.

For higher frequency signal inputs, an external sample and hold is recommended.

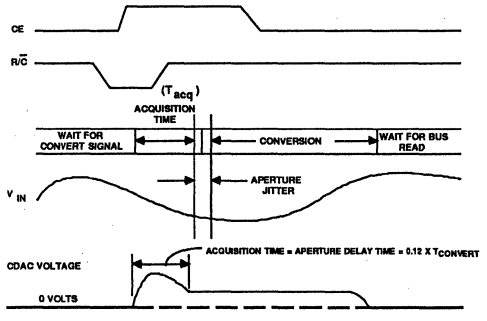


Figure 8 - Sample and Hold Function

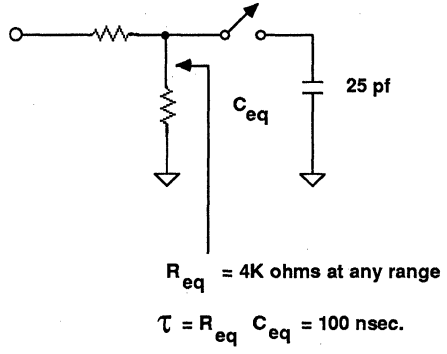


Figure 9 - Equivalent HADC574Z Input Circuit

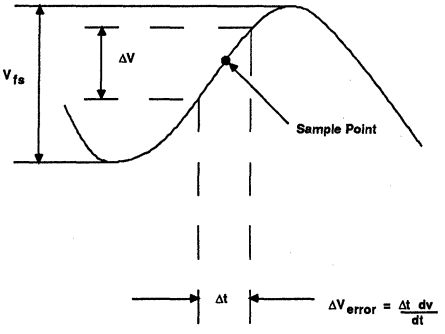


Figure 10 - Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HADC574Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 11 and 12. The two typical interface circuits are for operating the HADC574Z in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the P.C. board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC574Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10μF tantalum and a 0.1μF ceramic type in parallel between V_{LOGIC} (pin1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC574Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accomodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependant currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC574Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the HADC574Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R1 with a 50Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage 1/2LSB above negative full scale which is -4.9988V for the ±5V range or -9.9976V for the ±10V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2LSB below positive full scale which is +4.9963V for the ±5V range or +9.9927V for the ±10V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for an LSB of 2.5mV) or 20.48V (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HADC574Z

The HADC574Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE). The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 13.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table 1. The latched state determines if the conversion stops with 8-bits (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

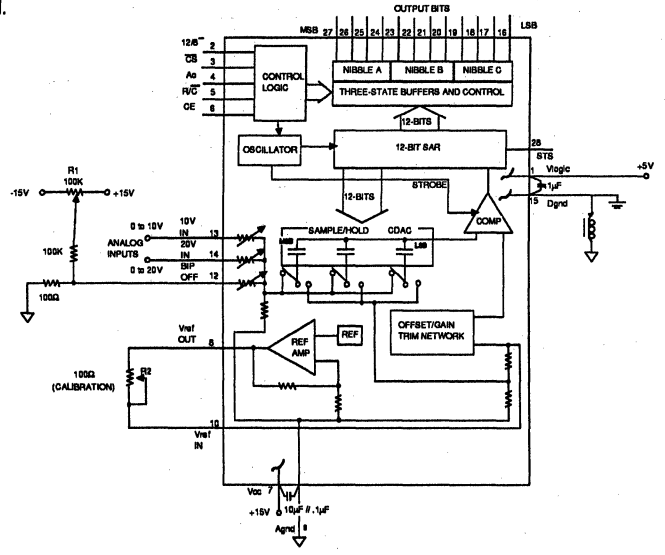


Figure 11 - Unipolar Input Connections

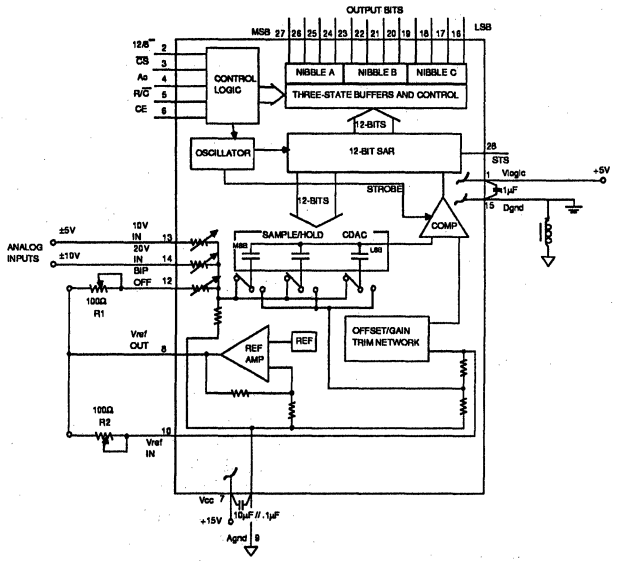


Figure 12 - Bipolar Input Connections

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new state of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

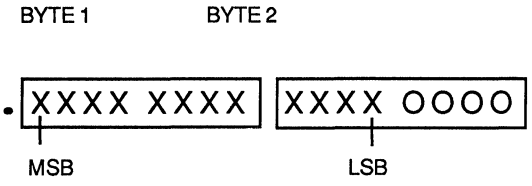
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible.

Table 1 - Truth Table for the HADC574Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

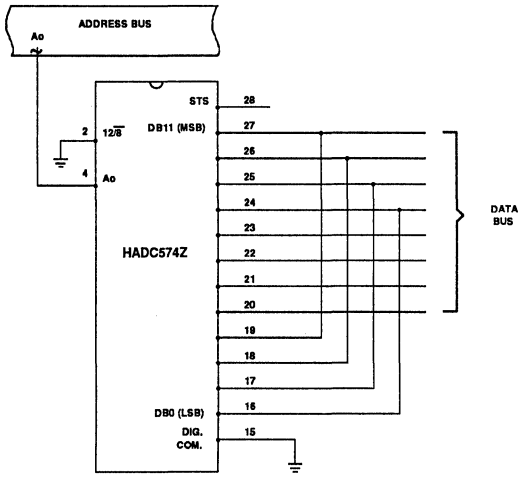


Figure 13 - Interfacing the HADC574Z to an 8-bit Data Bus

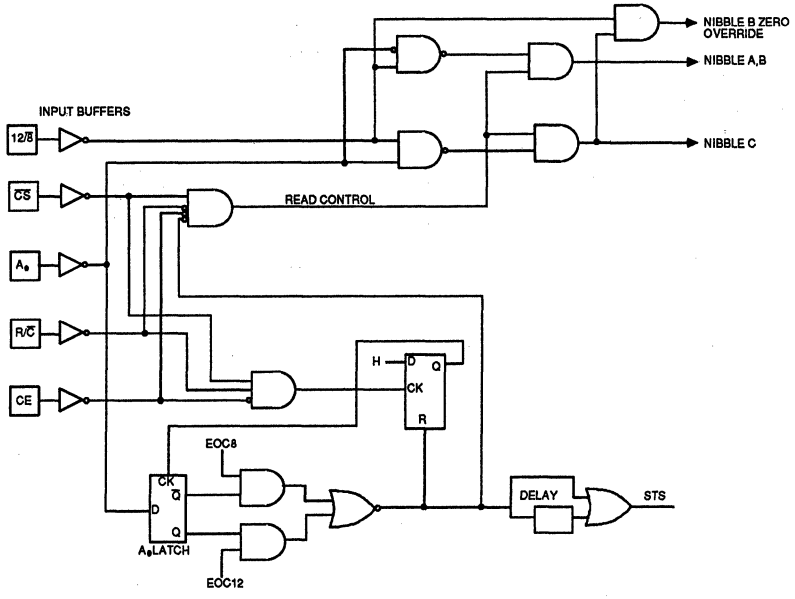


Figure 14 - HADC574Z Control Logic

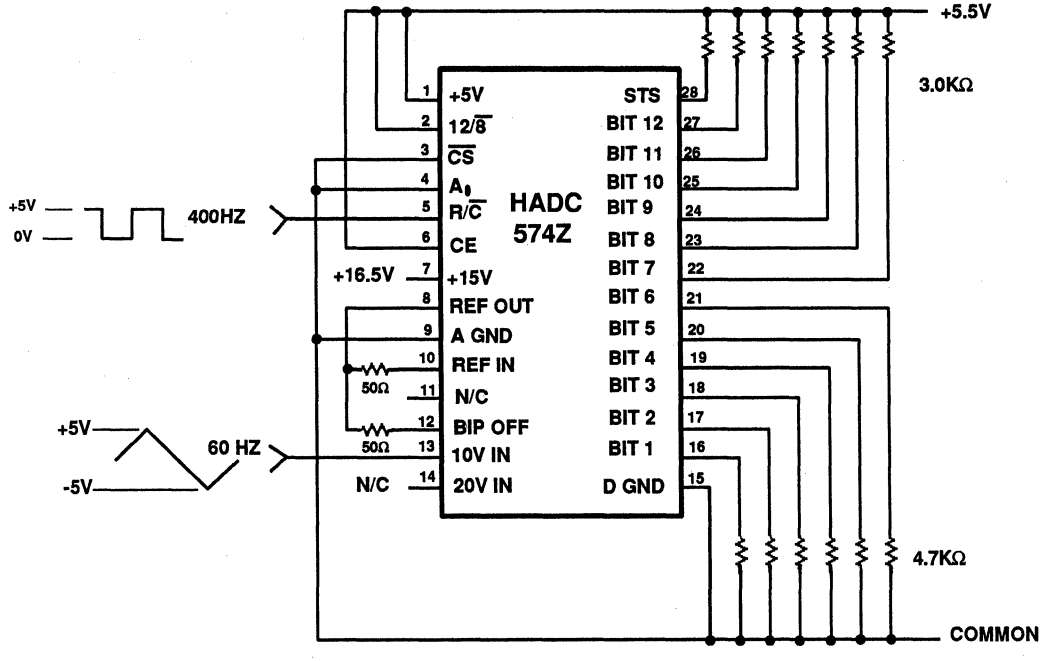
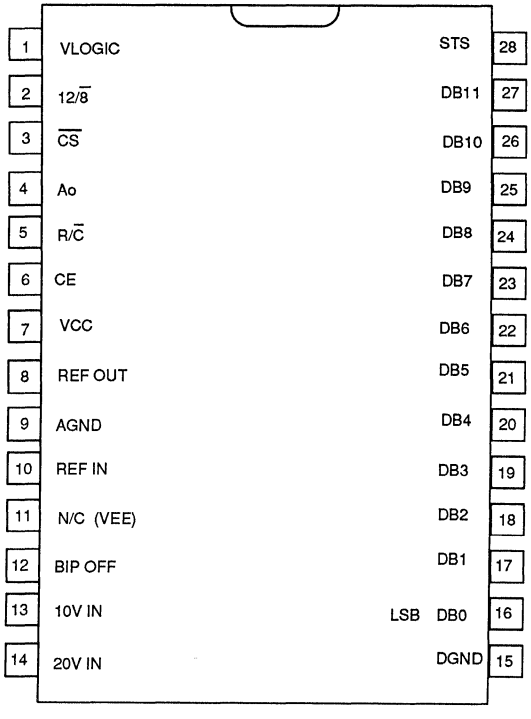


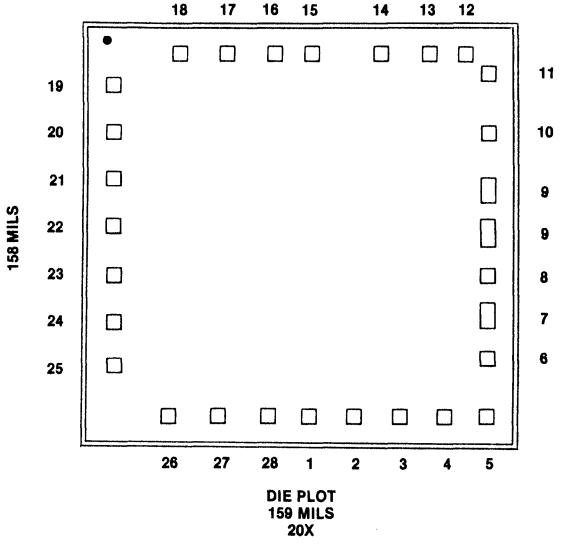
Figure 15 - Burn-in Schematic

PIN ASSIGNMENT HADC574Z

TOP VIEW



28 LEAD DIP



DIE PLOT
159 MILS
20X

PIN FUNCTIONS HADC574Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5V
12/$\overline{8}$	Data Mode Select
$\overline{CS}$	Chip Select
Ao	Byte Address/ Short cycle
R/$\overline{C}$	Read/ Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage Nominally +15V
REF OUT	Reference Output Nominally +10V
AGND	Analog Ground
REF IN	Reference Input
N/C (VEE)	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10V IN	10 Volt Analog Input
20V IN	20V Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

***For Ordering Information See Section 1.*

NOTES:

HADC674Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

PRELIMINARY INFORMATION

FEATURES:

- **IMPROVED PIN-TO-PIN COMPATIBLE MONOLITHIC VERSION OF THE HI674A**
- **Complete 12-bit A/D Converter with Sample-Hold, Reference and Clock**
- **Low Power Dissipation (150mW Max)**
- Faster Conversion and Pin Compatible with HADC574Z
- 12-bit Linearity (over temp)
- 15µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS:

- **MILITARY/INDUSTRIAL DATA ACQUISITION SYSTEMS**
- 8 OR 12-bit µP Input Functions
- Process Control Systems
- Test And Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15µs (Max) conversion time of 10 or 20 Volt input signals. Also, a 3-state output buffer is added for direct interface to an 8-, 12-, or 16-bit µP bus.

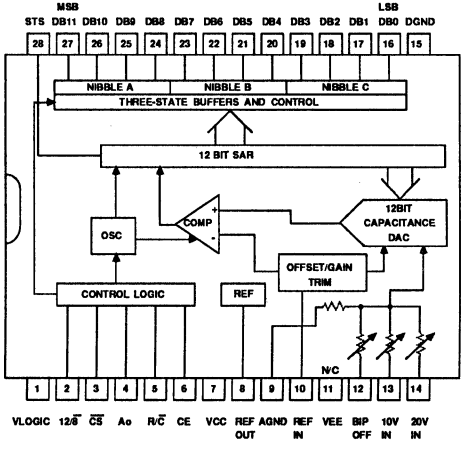
The HADC674Z is manufactured on Honeywell SPT's Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (V_{CC} to DGND)...0 to +16.5V
Logic Supply Voltage (V_{LOGIC} to DGND).....0 to +7V
Analog to Digital Ground (AGND to DGND)...-0.5 to +1V

Input Voltages
Control Input Voltages (to DGND).
(CE, CS, Ao, 12/8, R/C).....-0.5 to V_{LOGIC} +0.5V
Analog Input Voltage (to AGND).....±16.5V
(REF IN, BIP OFF, 10Vin)
20V Vin Input Voltage (to AGND).....±24V

Output
Reference Output Voltage.....Indefinite short to GND
Momentary short to V_{CC}

Temperature
Operating Temperature, ambient.-55 to +125(case) °C
junction.....+175 °C
Lead Temperature, (soldering 10 seconds).....+300 °C
Storage Temperature.....-65 to +150 °C
Power Dissipation.....1000mW
Thermal Resistance (θ_{jA}).....48°C/W

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE 0 TO +70°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC MIN	HADC674ZCC TYP	HADC674ZCC MAX	HADC674ZBC MIN	HADC674ZBC TYP	HADC674ZBC MAX	HADC674ZAC MIN	HADC674ZAC TYP	HADC674ZAC MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution					12			12			12	BITS
Linearity Error	Tmin to Tmax	I			±1			±½			±½	LSB
Differential Linearity Error	Tmin to Tmax	I			±1			±½			±½	LSB
Unipolar Offset	Adjustable to zero	I		±.1	±2		±.1	±2		±.1	±2	LSB
Bipolar Offset[1]	Adjustable to zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[1]		I			0.3			0.3			0.3	% of FS
	No adjustment at +25°C Tmin to Tmax	II		0.5			0.4			0.35		% of FS
	With adjustment at +25°C Tmin to Tmax	II		0.22			0.12			0.05		% of FS
Temperature Coefficients	Using internal reference											
Unipolar Offset		I		±.2	±2 (10)		±.1	±1 (5)		±.1	±1 (5)	LSB (ppm/°C)
Bipolar Offset		I		±.2	±2 (10)		±.1	±1 (5)		±.1	±1 (5)	LSB (ppm/°C)
Full Scale Calibration		I			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

COMMERCIAL TEMPERATURE RANGE 0 TO +70°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC MIN	HADC674ZCC TYP	HADC674ZCC MAX	HADC674ZBC MIN	HADC674ZBC TYP	HADC674ZBC MAX	HADC674ZAC MIN	HADC674ZAC TYP	HADC674ZAC MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I			±2			±1			±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I			±1/2			±1/2			±1/2	LSB
Analog Inputs Ranges		I	-5		+5	-5		+5	-5		+5	VOLTS
Bipolar			-10		+10	-10		+10	-10		+10	VOLTS
Unipolar		I	0		+10	0		+10	0		+10	VOLTS
			0		+20	0		+20	0		+20	VOLTS
Input Impedance 10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											VOLTS
Operating Current I_{LOGIC}		I		1	3		1	3		1	3	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}		II		0			0			0		mA
Power Dissipation +15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[2]		I			2			2			2	mA

Note 2: Available for external loads, external load should not change during conversion.
When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.

COMMERCIAL TEMPERATURE RANGE 0 TO +70°C

V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC MIN	HADC674ZCC TYP	HADC674ZCC MAX	HADC674ZBC MIN	HADC674ZBC TYP	HADC674ZBC MAX	HADC674ZAC MIN	HADC674ZAC TYP	HADC674ZAC MAX	UNITS
DIGITAL CHARACTERISTICS	The following specifications are guaranteed over the full temperature range.											
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "1"[3]		I	2.4		5.5	2.4		5.5	2.4		5.5	VOLTS
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	VOLTS
Current	0 to 5.5V Input	I		±.01	+5		±.01	+5		±.01	+5	µA
Capacitance		II		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6mA)	I			+0.4			+0.4			+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500µA)	I	+2.4			+2.4			+2.4			VOLTS
Leakage	(High Z State, DB11- DB0 Only)	I	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		II		5			5			5		pF

Note 3: Although the guaranteed threshold is higher than the standard TTL threshold (+2 Volts), loading is much less than standard TTL due to the CMOS nature of the inputs.

MILITARY TEMPERATURE RANGE -55 TO +125°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCM MIN	HADC674ZCM TYP	HADC674ZCM MAX	HADC674ZBM MIN	HADC674ZBM TYP	HADC674ZBM MAX	HADC674ZAM MIN	HADC674ZAM TYP	HADC674ZAM MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution					12			12			12	BITS
Linearity Error		I			±1			±1/2			±1/2	LSB
Linearity Error	Tmin to Tmax	I			±1			±1/2			±1/2	LSB
Differential Linearity Error	Tmin to Tmax	I			±1			±1/2			±1/2	LSB
Unipolar Offset	Adjustable to zero	I			±2			±2			±2	LSB
Bipolar Offset[1]	Adjustable to zero	I			±10			±4			±4	LSB
Full Scale Calibration Error[1]		I			0.3			0.3			0.3	% of FS
	No adjustment at +25°C Tmin to Tmax	II		0.8			0.6			0.4		% of FS
	With adjustment at +25°C Tmin to Tmax	II		0.5			0.25			0.12		% of FS
Temperature Coefficients	Using internal reference Tmin to Tmax											
Unipolar Offset		I			±2 (5)			±1 (2.5)			±1 (2.5)	LSB (ppm/°C)
Bipolar Offset		I			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration		I			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V<Vcc<+16.5V or +11.4V<Vcc<+12.6V		I			±2			±1			±1	LSB
+4.5V<V_{LOGIC}<+5.5V		I			±1/2			±1/2			±1/2	LSB
Analog Inputs Input Ranges												
Bipolar		I	-5		+5	-5		+5	-5		+5	VOLTS
			-10		+10	-10		+10	-10		+10	VOLTS
Unipolar		I	0		+10	0		+10	0		+10	VOLTS
			0		+20	0		+20	0		+20	VOLTS
Input Impedance												
10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ

MILITARY TEMPERATURE RANGE -55 TO +125°C

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCM			HADC674ZBM			HADC674ZAM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC ELECTRICAL CHARACTERISTICS												
Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	VOLTS
V_{CC}		I	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	VOLTS
V_{EE}	Not required for circuit operation.											VOLTS
Operating Current I_{LOGIC}		I		1	3		1	3		1	3	mA
I_{CC}		I		7	9		7	9		7	9	mA
I_{EE}		II		0			0			0		mA
Power Dissipation ±15V, +5V		I		110	150		110	150		110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current[4]		I			2			2			2	mA
DIGITAL CHARACTERISTICS	The following specifications are guaranteed over the full temperature range.											
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "1"		I	2.4		5.5	2.4		5.5	2.4		5.5	VOLTS
Logic "0"		I	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	VOLTS
Current	0 to +5.5V Input	I		±.01	+5		±.01	+5		±.01	+5	µA
Capacitance		II		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6mA)	I			+0.4			+0.4			+0.4	VOLTS
Logic "1"	(I_{SOURCE} = 500µA)	I	+2.4			+2.4			+2.4			VOLTS
Leakage	(High Z State, DB11-DB0 Only)		-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		II		5			5			5		pF

Note 4: Available for external loads, external load should not change during conversion. When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

CONVERT MODE TIMING CHARACTERISTICS

Typical @ 25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time 12-Bit Cycle	Tmin to Tmax	I	9		15	9		15	9		15	µs
8-Bit Cycle	Tmin to Tmax	I	6		10	6		10	6		10	µs

Note 5: Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3KΩ load for drive to high impedance.

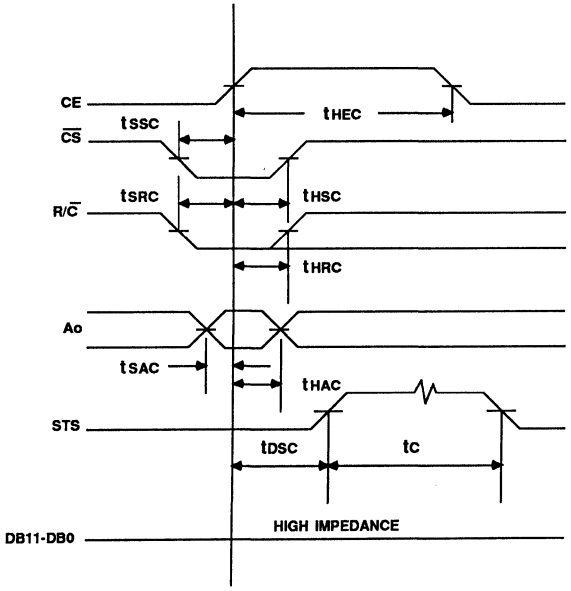


Figure 1 - Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	0	0		0	0		0	0		ns
t_{HAR} Ao Valid After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns

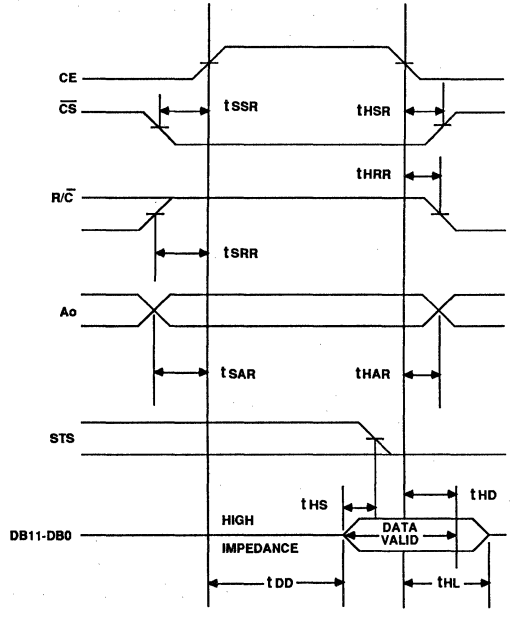


Figure 2 - Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		II	1.0	1.4	1.8	1.0	1.4	1.8	1.0	1.4	1.8	µs
Aperture Uncertainty Time		II		20			20			20		ns

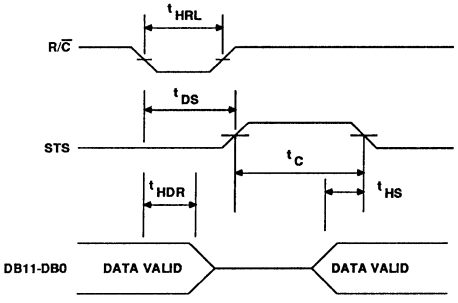


Figure 3 - Low Pulse For R/C - Outputs Enabled After Conversion

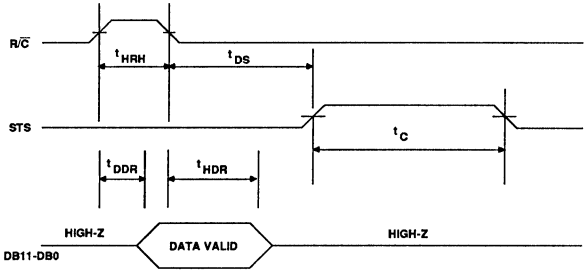


Figure 4 - High Pulse For R/C - Outputs Enabled While R/C is High, Otherwise High Impedance

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_{junc} = T_{case} = T_{ambient}$.

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.
II	Parameter is guaranteed by design and sampled characterization data.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 7). The point used as "zero" occurs 1/2LSB (1.22mV for a 10 Volt span) before the first code transistion (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674Z A and B grades are guaranteed for maximum nonlinearity of ±1/2LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674ZCC and CM grades are guaranteed to ±1LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type BC, AC, BM, and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 7 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential non-linearity of -1 LSB. Figure 7 points out two missed codes in the transfer function.

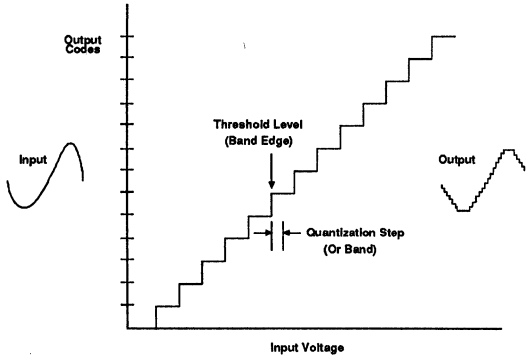


Figure 5 - Static Input Conditions

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = FSR/2^N$ where FSR = full scale range and N = 12. Non- ideal quantization bands represent differential nonlinearity errors (See Figures 5, 6 and 7).

RESOLUTION - ACTUAL VS. AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically posssible to generate 2^N unique output codes.

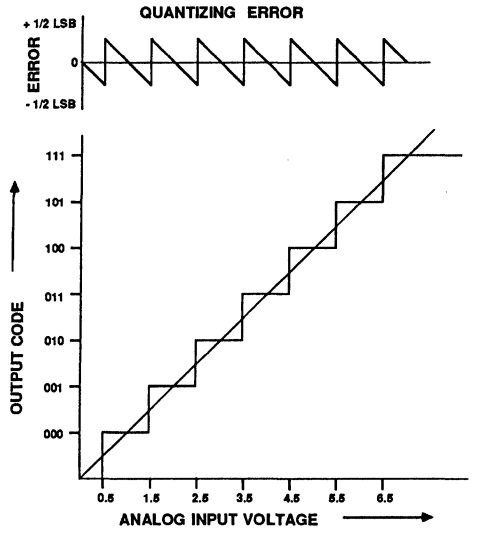


Figure 6 - Quantizing error

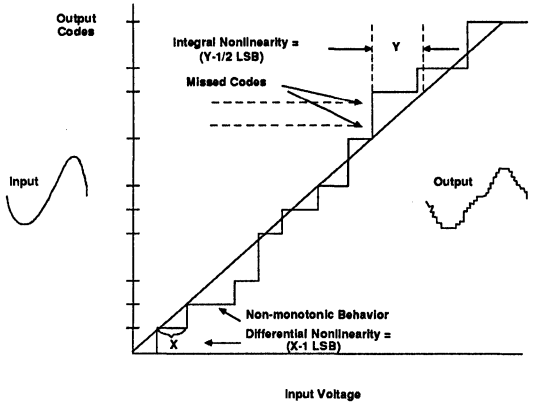


Figure 7 - Dynamic Conditions

THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the $R/\overline{C}$ falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit Analog-To-Digital converter which consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample & hold, clock, output buffers and control circuitry to make it possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the HADC674Z is used with ±12V supplies, or if external current must be supplied over the full temperature range, an

external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample and hold. This prevents transients occuring during conversion from being inflicted upon the attached sample and hold buffer. All other 674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC674Z and is controlled through the normal R/$\overline{C}$ control line (refer to Figure 8.) When the R/$\overline{C}$ line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

During T_{acq}, the equivalent circuit of the HADC674Z in-put is as shown in Figure 9 (the time constant of the input is independant of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs., there is more than enough time for settling the input to 12 bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the R/$\overline{C}$ transition, T_{acq} is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} = 1.4 µsecs ± 0.4 µsecs. between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC674Z.

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken - i.e. the "aperture jitter" or T_{AJ}. The HADC674Z has a nominal aperture jitter of 20 nsecs. between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 10). The magnitude of this change for a sine-wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, Sr = $2\pi fVp$ (Vp = peak voltage, f = frequency of sine wave)
For an N-bit converter to maintain +/- 1/2 LSB accuracy :

$Verr \leq Vfs/2^{N+1}$ (where Verr is the allowable error voltage and Vfs is the full scale voltage)

From Figure 10:

$Sr = \Delta V/\Delta T = 2\pi fVp$

Let $\Delta V = Verr = V_{fs}2^{-(N+1)}$, Vp = Vin/2 and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

$Vfs/2^{N+1} \geq \pi f Vin\, t_{AJ}$ or $f_{max} \leq Vfs/(\pi Vin\, t_{AJ})2^{N+1}$

For the HADC674Z, $T_{AJ} = 20$ nsec, therefore $f_{max} \leq 2KHz$.

For higher frequency signal inputs, an external sample and hold is recommended.

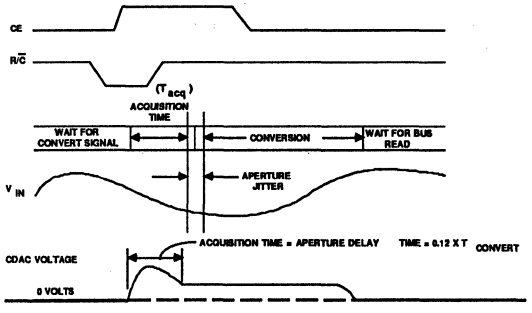


Figure 8 - Sample and Hold Function

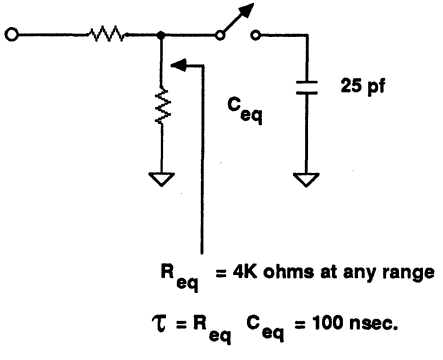


Figure 9 - Equivalent HADC674Z Input Circuit

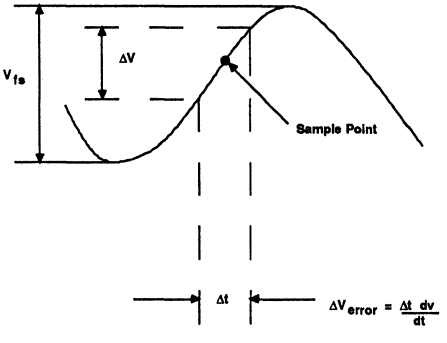


Figure 10 - Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 11 and 12. The two typical interface circuits are for operating the HADC674Z in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the P.C. board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to it's respective ground to filter noise and counter the problems caused by the variations in supply current. A 10μF tantalum and a 0.1μF ceramic type in parallel between V_{LOGIC} (pin1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accomodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependant currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R1 with a 50Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1 and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage 1/2LSB above negative full scale which is -4.9988V for the ±5V range or -9.9976V for the ±10V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2LSB below positive full scale which is +4.9963V for the ±5V range or +9.9927V for the ±10V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for an LSB of 2.5mV) or 20.48V (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HADC674Z

The HADC674Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/C input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/8, CS, Ao, R/C and CE). The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 13.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and 12/8 are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table 1. The latched state determines if the conversion stops with 8-bits (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

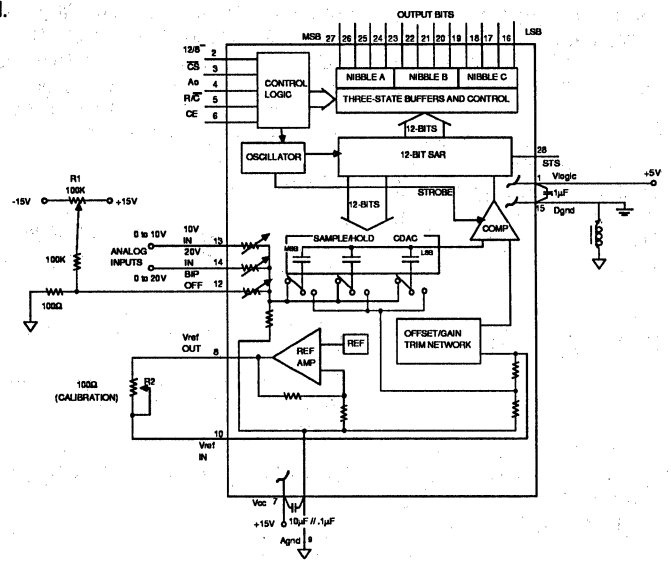


Figure 11 - Unipolar Input Connections

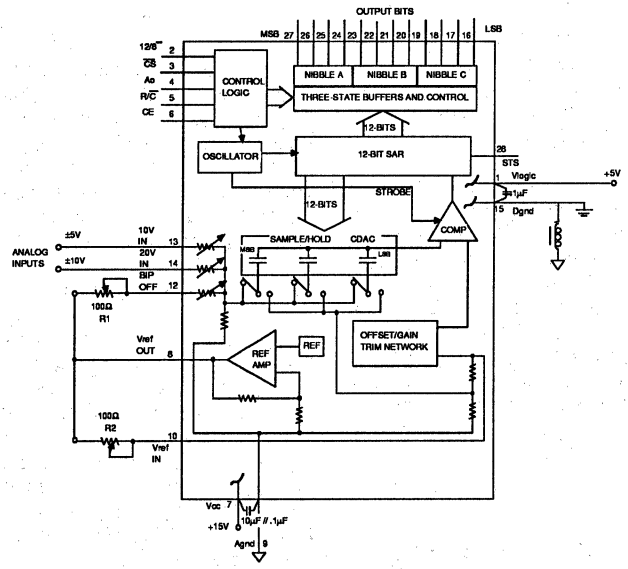


Figure 12 - Bipolar Input Connections

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new state of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

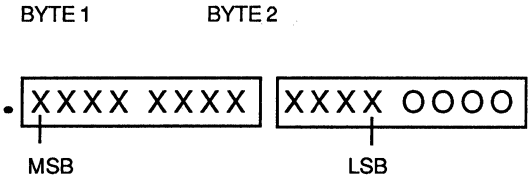
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible.

Table 1 - Truth Table for the HADC674Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

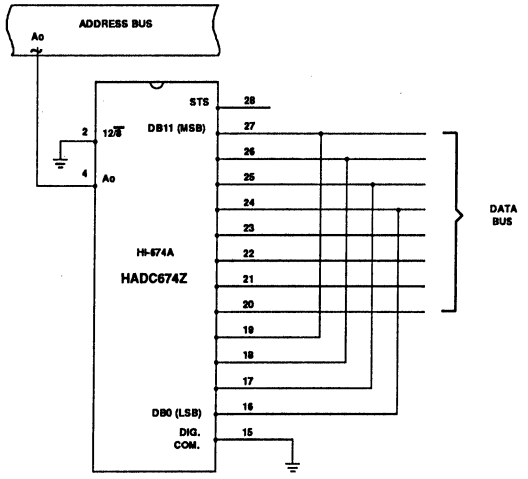


Figure 13 - Interfacing the HADC674Z to an 8-bit Data Bus

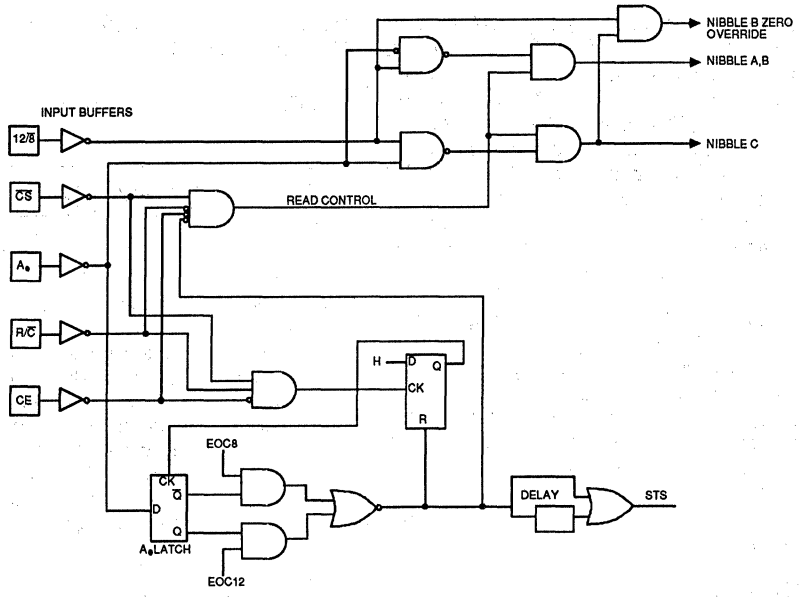


Figure 14 - HADC674Z Control Logic

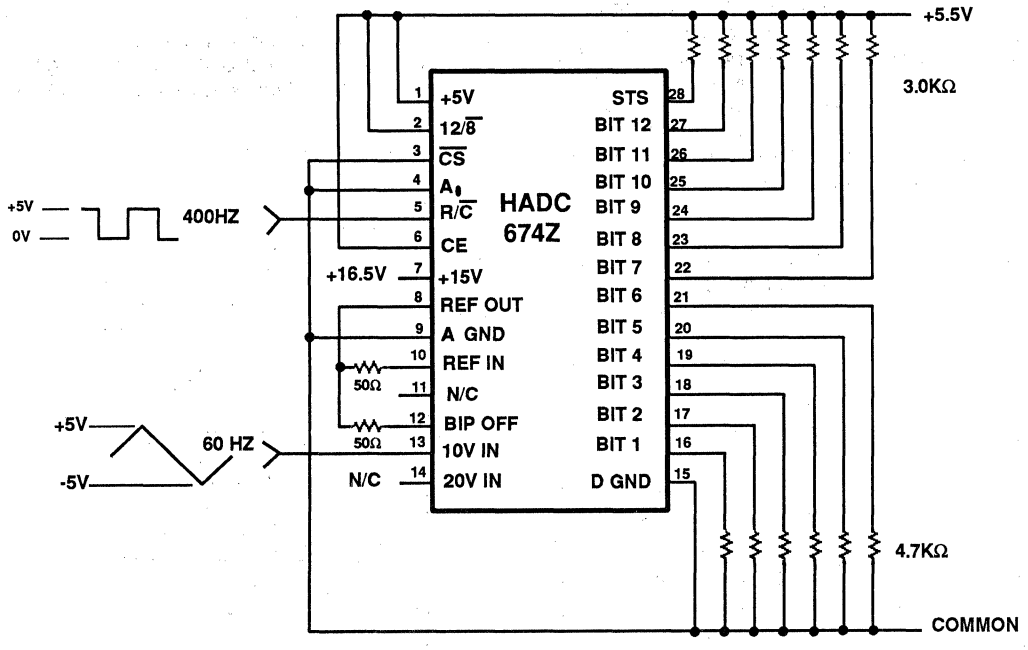
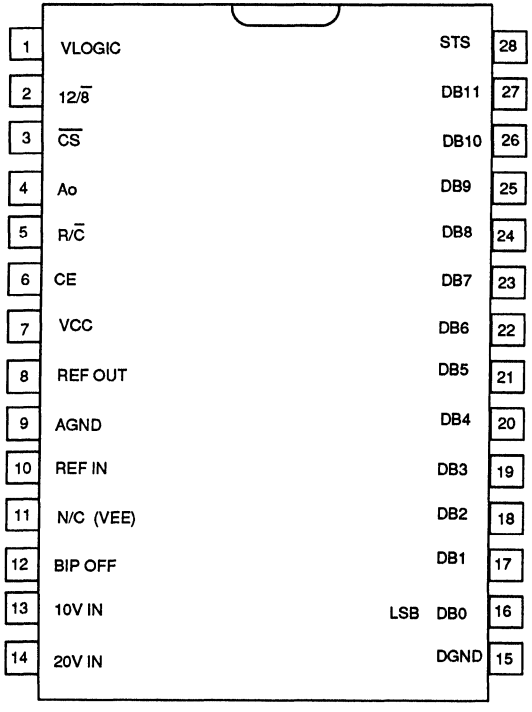


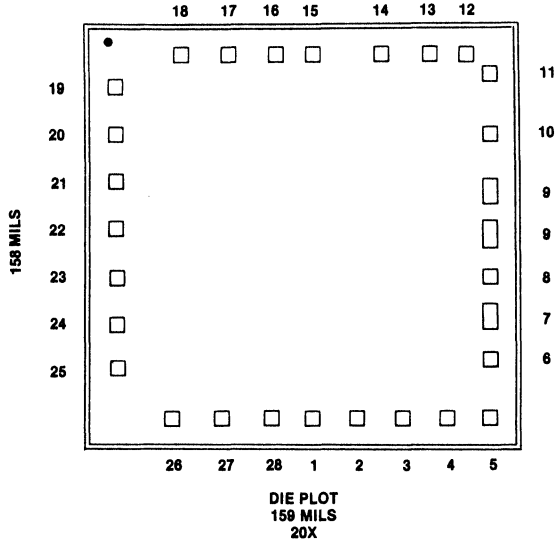
Figure 15 - Burn-in Schematic

PIN ASSIGNMENT HADC674

TOP VIEW



28 LEAD DIP



DIE PLOT
159 MILS
20X

PIN FUNCTIONS HADC674Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5V
12/$\overline{8}$	Data Mode Select
$\overline{CS}$	Chip Select
Ao	Byte Address/ Short cycle
R/$\overline{C}$	Read/ Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage Nominally +15V
REF OUT	Reference Output Nominally +10V
AGND	Analog Ground
REF IN	Reference Input
N/C (VEE)	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10V IN	10 Volt Analog Input
20V IN	20V Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

***For Ordering Information See Section 1.*

NOTES:

HADC77100

8-BIT, 150 MSPS FLASH A/D CONVERTER

PRELIMINARY INFORMATION

FEATURES

- **150 MSPS NOMINAL CONVERSION RATE**
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Maximum Power Dissipation < 2.0 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

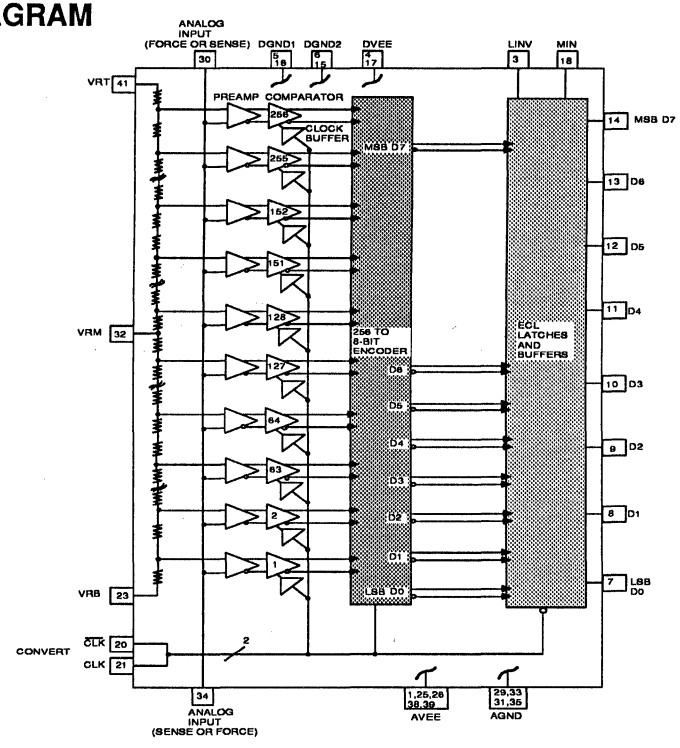
GENERAL DESCRIPTION

The HADC77100 is a monolithic flash A/D converter capable of digitizing a 2 volt analog input signal with full scale frequency components to 50 MHz into 8-bit digital words at a 150 MSPS update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time. A single standard -5.2 Volt power supply is required for operation of the HADC77100, with nominal power dissipation of less than 1.75 Watts.

The part is packaged in a 42 Lead Ceramic DIP that is pin compatible with the CX20116. Careful attention to design and layout has provided a device with better linearity, lower noise floor, stable input capacitance, and lower data error rates. The HADC77100 is available in Industrial and Military Temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages Output
Negative Supply Voltage (V_{EE} TO GND) ..-7.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5V
A_{VEE} to D_{VEE} Differential.....50mV

Input Voltage
Analog Input Voltage.....+0.5 to V_{EE} V
Reference Input Voltage.....+0.5 to V_{EE} V
Digital Input Voltage.....+0.5 to V_{EE} V
Reference Current VRT to VRB.....25 mA
Midtap Reference Current.....-6 to +6 mA

Output
Digital Output Current.....0 to -25 mA

Temperature
Operating Temperature, ambient.....-65 to +150°C
junction.....+150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity, 77100A		II			±1/2		±1/2		±1/2	LSB
Differential Linearity, 77100A		II			±1/2		±1/2		±1/2	LSB
Integral Linearity, 77100B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77100B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT		I		18	-30		-30		-30	mV
Offset Error VRB		I		18	+30		+30		+30	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range		I	-2.0		0.0					VOLTS
Input Capacitance	Over full input range	V		56						pF
Input Resistance		V		4						kΩ
Input Current		II		175	275		225		350	µA
Clock Synchronous Input Currents		V		40						µA

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
POWER SUPPLIES										
Supply Current (analog)		II		280	300		300		300	mA
Supply Current (digital)		II		50	70		70		70	mA
REFERENCE										
Positive Reference Voltage	Operating Condition	I	>VRT		0.0					VOLTS
Negative Reference Voltage	Operating Condition	I	-2.5		<VRB					VOLTS
Reference Tap Current	V_{RM} = -1.00V	IV			4					mA
Ladder Resistance		II	100		160	100	180	80	120	Ω
Reference Bandwidth		V		50						MHz
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	VOLTS
Output Low Voltage	50Ω to -2V	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	VOLTS
Input High Voltage (MINV, LINV)		II	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS
Output Rise Time 10% to 90%	50Ω to -2V	IV			2					ns
Output Fall Time 10% to 90%	50Ω to -2V	IV			2					ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
CONVERSION TIMING, See Figure 1A										
Maximum Sample Rate		II	125	150		125		125		MSPS
Clock Low Width, TPW0		II	4	3		4		4		ns
Clock High Width, TPW1		II	4	3		4		4		ns
Output Latency		IV			1		1		1	CYCLE
Output Delay, TD	Differential Clock	V		4.2						ns
Output Delay Tempco	Differential Clock	V		15						ps/°C

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	II		60						MHz
Small Signal Bandwidth	Vin = 500mV PP	II	100	120						MHz
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	V		1.8						ns
Aperture Delay Tempco	Differential Clock	V		7						ps/°C
Aperture Time		V		<100						ps
Settle-to-Hold Time		V		3						ns
Input Slew Rate		V		300						V/µs

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 125MHz										
RMS Sinewave Curve Fit	Vin = FS @ 1MHz	II		8						LSB
RMS Sinewave Curve Fit	Vin = FS @ 25MHz	II		7						LSB
RMS Sinewave Curve Fit	Vin = FS @ 50MHz	II		5.3						LSB
Signal to noise ratio	Vin = FS @ 1MHz	II		48						dB
Signal to noise ratio	Vin = FS @ 25MHz	II		43						dB
Signal to noise ratio	Vin = FS @ 50MHz	II		36						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	V		44						dBc
Total Harmonic Distortion	Vin = FS @ 25MHz	V		35						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	V		24						dBc
Mean Differential Non-Linearity		V		.001						LSB
RMS Differential Non-Linearity		V		.2						LSB
Differential Gain	NTSC 40IRE mod. ramp,Fc = 125MSPS	V		1.0						%
Differential Phase		V		.5						DEG

TEST LEVEL CODE: See page 7.

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity, 77100A		I			±1/4 ±1/2		±1/2		±1/2	LSB
Differential Linearity, 77100A		I			±1/4 ±1/2		±1/2		±1/2	LSB
Offset Error VRT		I		18	-30		-30		-30	mV
Offset Error VRB		I		18	30				30	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range		I	-2.5		+0.5	-2.5	+0.5	-2.5	+0.5	VOLTS
Input Capacitance	Over full input range	V		56						pF
Input Resistance		V		4						kΩ
Input Current		I		175	275		200		400	µA
Clock Synchronous Input Currents		V		40						µA
POWER SUPPLIES										
Supply Current (analog)		I	210	250	300		330		330	mA
Supply Current (digital)		I		50	70		70		70	mA
REFERENCE										
Positive Reference Voltage	Operating Condition	I	>VRT		0.0					VOLTS
Negative Reference Voltage	Operating Condition	I	-2.5		<VRB					VOLTS
Reference Tap Current	V_{RM} = -1.00V	V			4					mA
Ladder Resistance		II	100		160	130	210	80	120	Ω
Reference Bandwidth		V		50						MHz

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	VOLTS
Output Low Voltage	50Ω to -2V	I	-1.95	1.80	-1.65	-1.95	-1.65	-1.95	-1.70	VOLTS
Input High Voltage (MINV, LINV)		I	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS
Output Rise Time (10% to 90%)	50Ω to -2V				2					ns
Output Fall Time (10% to 90%)	50Ω to -2V				2					ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
CONVERSION TIMING (See Figure1A)										
Maximum Sample Rate		II	125	150						MSPS
Clock Low Width, TPW0		II	4	3						ns
Clock High Width, TPW1		II	4	3						ns
Output Latency		IV			1		1		1	CYCLE
Data Ready Delay, TD		II		4.2						ns
Output Delay, TD	Differential Clock	II	3.2	4.2	4.8	6.1	7.3	1.7		ns
Output Delay Tempco		V		15						ps/°C
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	II		60						MHz
Small Signal Bandwidth	Vin = 500mVPP	II	100	120						MHz
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	II	1.2	1.8	2.4	2.4	3.6	.5		ns
Aperture Time		V		<100						ps
Settle-to-Hold Time		V		3						ns
Aperture Delay Tempco	Differential Clock	V		7						ps/°C

TEST LEVEL CODE: See page 7.

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL CHARACTERISTICS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 125MHz										
RMS Sinewave Curve Fit	Vin = FS @ 1MHz	II								LSB
RMS Sinewave Curve Fit	Vin = FS @ 25MHz	II								LSB
RMS Sinewave Curve Fit	Vin = FS @ 50MHz	II								LSB
Signal to noise ratio	Vin = FS @ 1MHz	II		48						dB
Signal to noise ratio	Vin = FS @ 25MHz	II		43						dB
Signal to noise ratio	Vin = FS @ 50MHz	II		36						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	V		44						dBc
Total Harmonic Distortion	Vin = FS @ 25MHz	V		35						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	V		24						dBc
Mean Differential Non-Linearity		V		.001						LSB
RMS Differential Non-Linearity		V		.2						LSB

TEST LEVEL CODE: See page 7.

TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperatures.
II	100% production tested at Ta = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

GENERAL DESCRIPTION

The HADC77100 is the fastest monolithic 8-bit parallel flash A/D converter available today. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 50 MHZ. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low ac beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash A/Ds. The preamplfiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The HADC77100 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77100 has an on-board power supply bypass of 1500pF to reduce external component needs, and the output drive capability of the device can provide full ECL swings into 50Ω loads.

TYPICAL INTERFACE CIRCUIT

The HADC77100 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

AVEE, DVEE, AGND, DGND

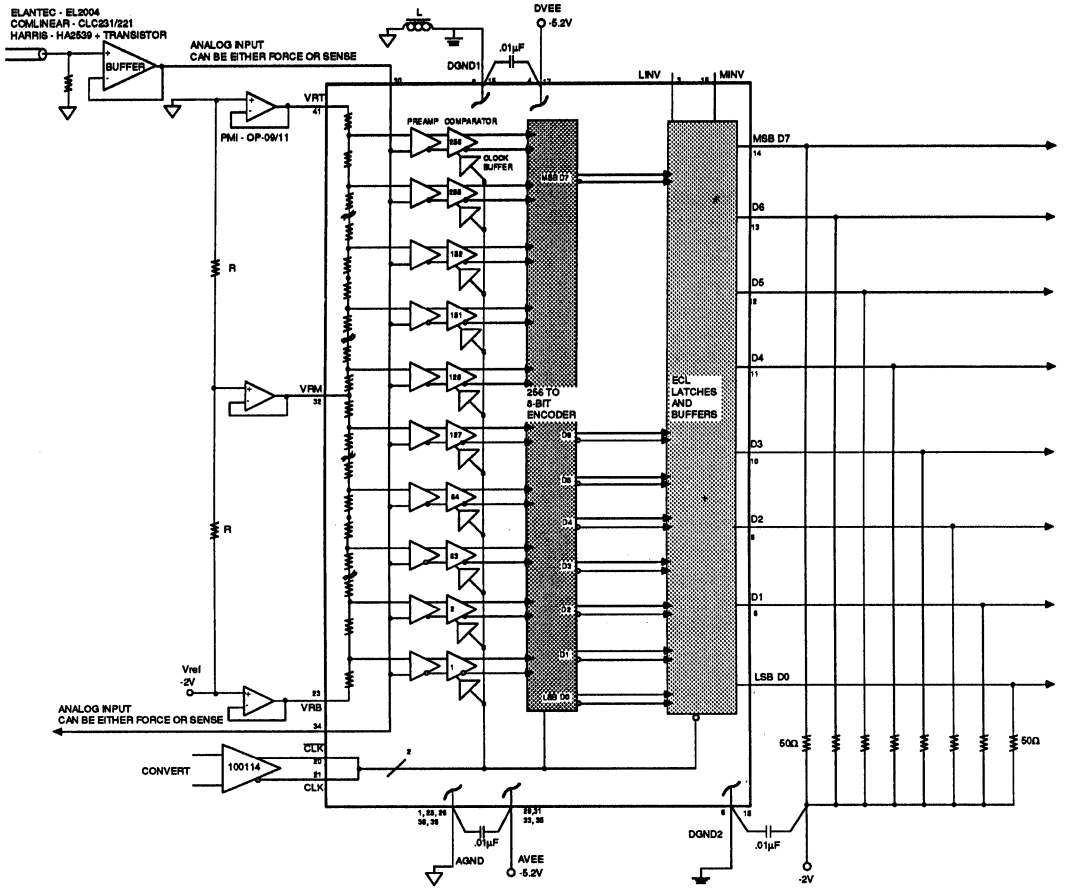
The analog and digital supply and ground pins are physically separated on the device. It is recommended to take advantage of the noise suppression benefits by utilizing separate ground and supply planes when operating the part above 50 MSPS clock rates.

If separate AVEE and DVEE are used, be sure to power both up simultaneously to avoid damaging the device. The digital and analog power supply terminals should be bypassed as close to the device as possible to their respective grounds with at least a .01μF ceramic capacitor. A 1μF tantalum can also be used for low frequency suppression. The digital ground is further divided into internal circuit ground (DGND1) and output ground (DGND2). The digital output ground should be referenced to the pulldown voltage and bypassed to it as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77100 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836/7 transistor. Very high performance can be achieved by using a comlinear CLC100.

FIGURE 1 HADC77100 TYPICAL INTERFACE CIRCUIT



CLK, $\overline{\text{CLK}}$ (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{\text{CLK}}$ is internally biased to -1.3V (see clock input circuit on page 12). It may be left open but a .01µF bypass capacitor from $\overline{\text{CLK}}$ to DGND1 is recommended. The duty cycle of the clock should be kept at 50% to avoid causing larger 2nd harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

MINV, LINV (Output Logic Control)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table 1. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to DGND1 through a diode or 3.9kΩ resistor.

D0 to D7 (Digital Outputs)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V the outputs can drive 130Ω to 1KΩ loads.

VRB, VRM, VRT (Reference Input)

There are two reference inputs and one external reference voltage tap. These are -2V(VRB), mid-tap (VRM), and AGND (VRT). The reference pins and tap can be driven by op amps as shown in Figure 1 or VRM may be bypassed for limited temperature operation. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired.

N/C

All "Not Connected" pins should be tied to DGND1 on the left side of the package and to AGND on the right side.

TABLE 1 - OUTPUT CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

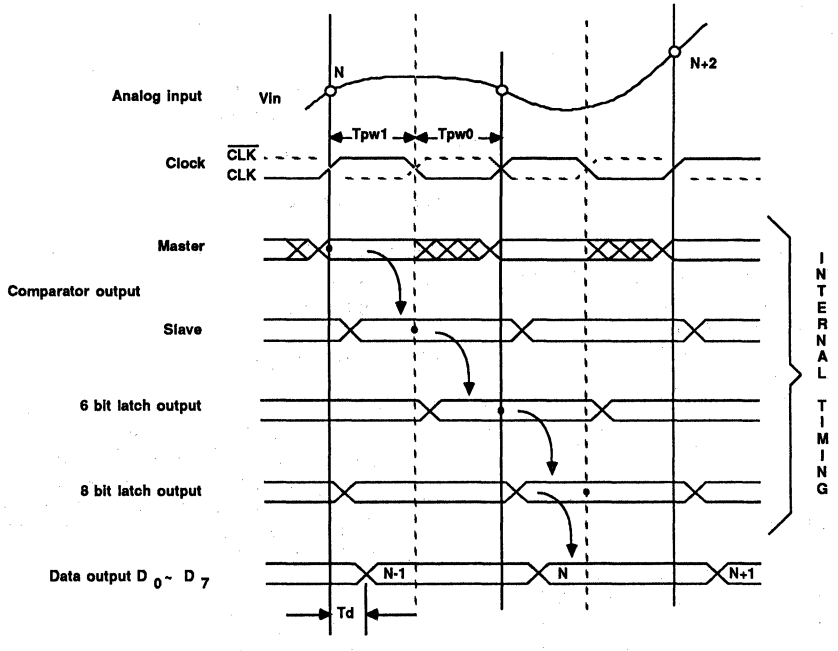
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

OPERATION

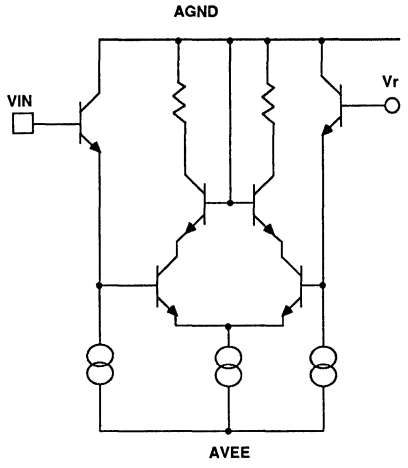
The HADC77100 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram on page 1. This voltage is applied to the positive input of each preamplifier and comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT(0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from four columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions and they consist of a set of eight XOR gates. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

FIGURE 1A - TIMING DIAGRAM

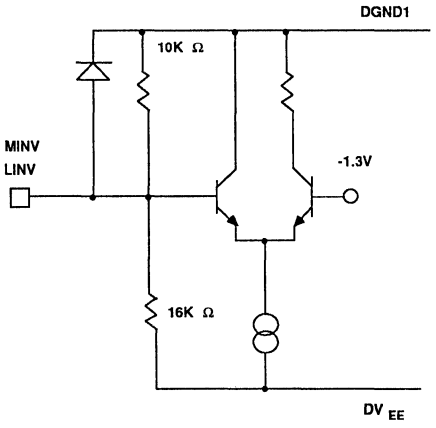


Dots (•) in the chart denote respective latch timings.

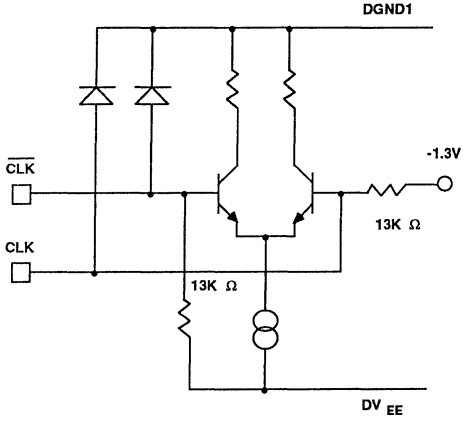
INPUT CIRCUIT



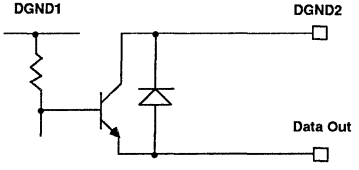
MINV, LINV INPUT CIRCUIT



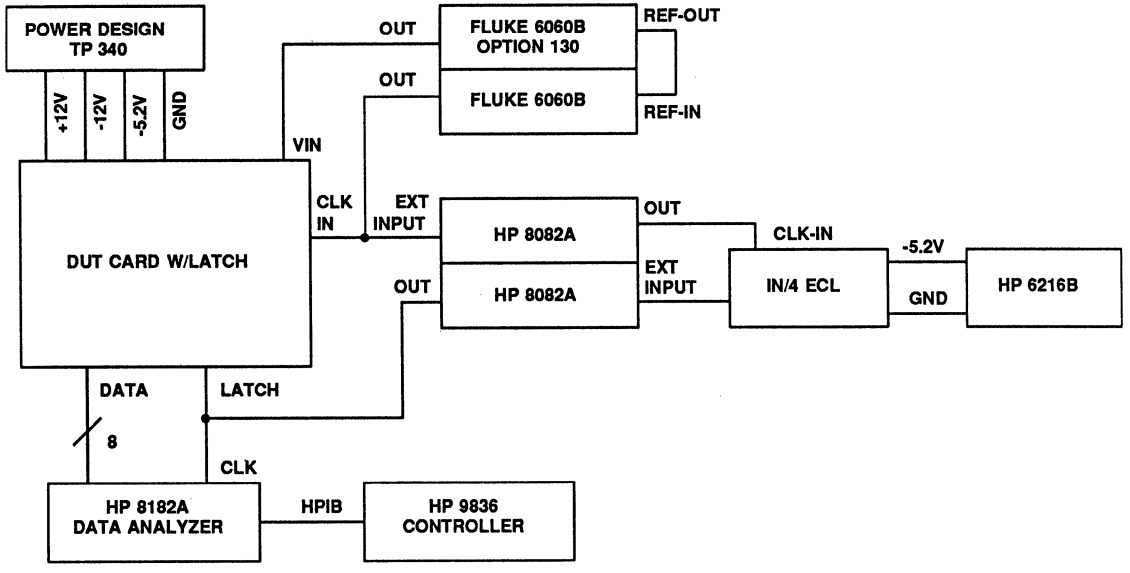
CLOCK INPUT



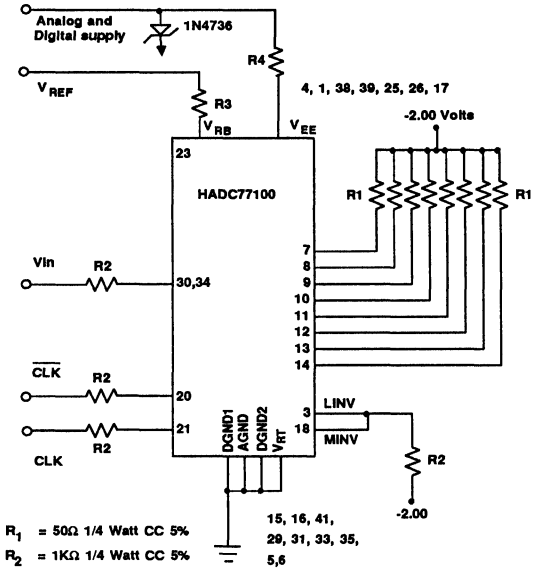
OUTPUT CIRCUIT



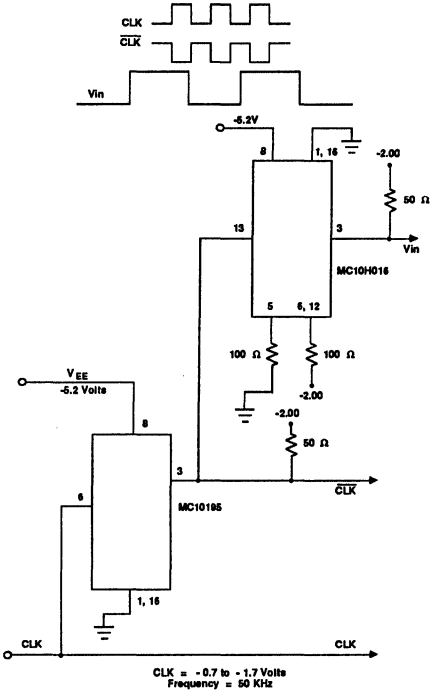
DYNAMIC EVALUATION



BURN-IN CIRCUIT $T_{BURN-IN}$ = 125°C



BURN-IN CIRCUIT



CIRCUIT TO GENERATE CLOCK AND INPUT FOR BURN-IN CIRCUIT

DEFINITION OF TERMS

SPECIFICATIONS

A/D CONVERTER ERROR SUMMARY

Honeywell SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 2B) while a static dc input level may appear close to the ideal (Figure 2A). That is why we are including many dynamic tests as well as the the industry standard dc specifications.

EFFECTIVE BITS (SNR)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from measured rms error for the ideal sinewave and the measured actual rms error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual rms error}}{\text{ideal rms error}}$$

Furthermore, signal-to-noise ratio (SNR) can be related to effective bits by the following formula:

$$\text{SNR(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D tranfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q = FSR/2^N where FSR = full scale range and N = 8. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 2A and 2B).

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 2B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77100's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 2B points out two missed codes in the transfer function.

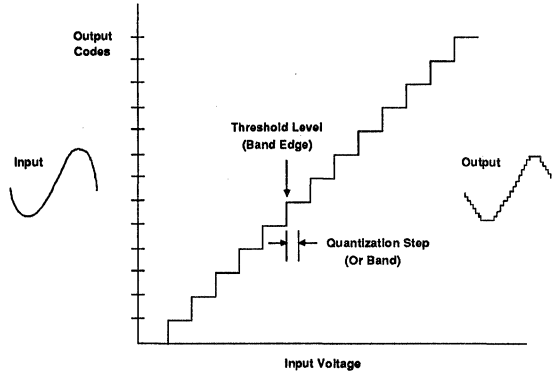


Figure 2A Static Input Conditions

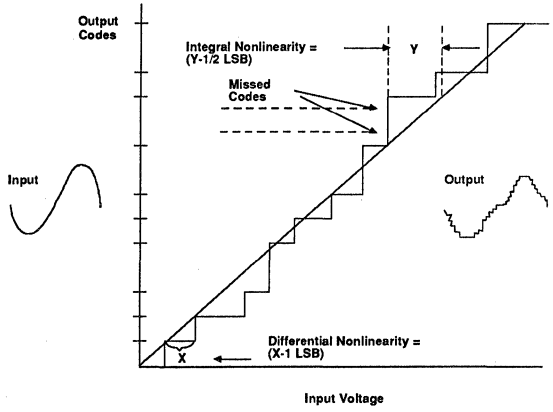


Figure 2B Dynamic Conditions

SPECIFICATIONS CONTINUED

INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 3A). Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 2B shows an integral nonlinearity error of 2 LSB. The HADC77100's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 1. The resulting effect on the linearity is shown in Figure 3B.

APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 3C .

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 4 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from Figure 4 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70ps.

Aperture time and delay are very difficult to measure, however these values are needed to make intelligent design decisions. Honeywell SPT supplies these values for the HADC77100 based on both computer design simulations and verified by characterization of samples.

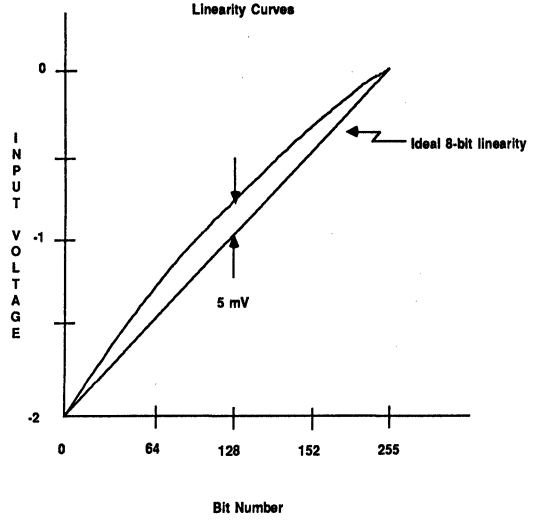


FIGURE 3A Linearity Curve with no TAP adjustment

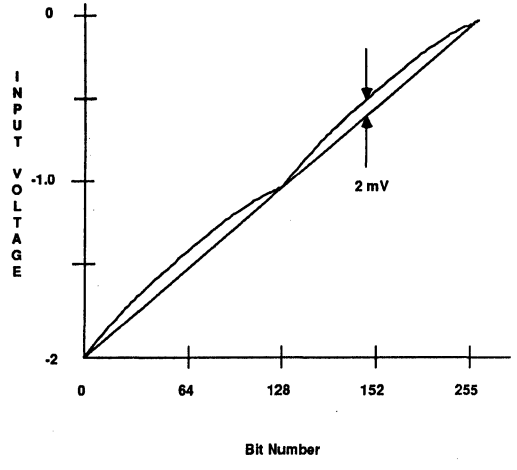


FIGURE 3B Linearity Curve with TAPS Forced to Within .5mV of Ideal

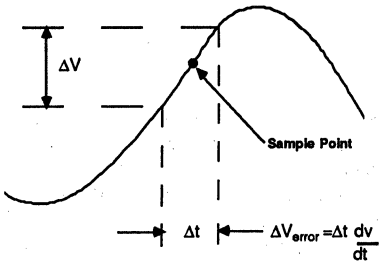


FIGURE 3C Aperture Uncertainty

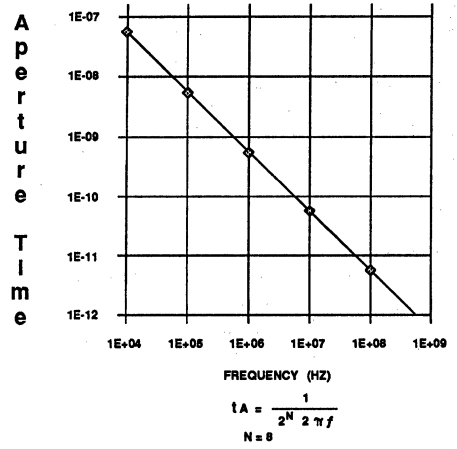
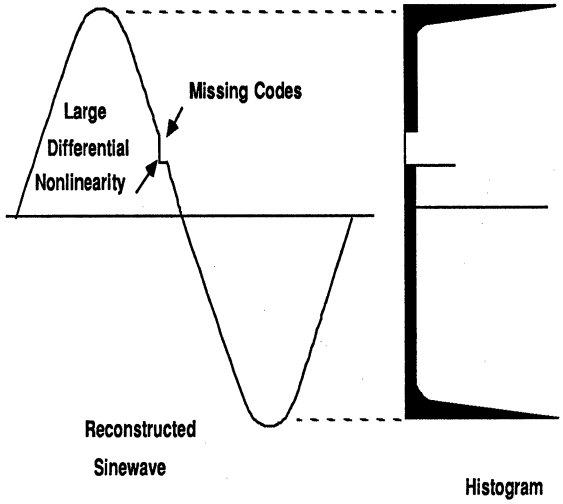


FIGURE 4 Aperture Time - Sinewaves



In the histogram test, A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FIGURE 5 Histogram Testing

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 2.

HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77100. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurance along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurance at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 5).

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased

SPECIFICATION TESTING CONTINUED:

into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table 2.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77100. Using least squared error minimization techniques, an idealized sinewave fit to the data is calulated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A,f,θ,DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave, $A_0\sin(2\pi f_0 t+\theta_0)+DC_0$ is then subtracted from the digitized time record.

The rms errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77100. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

TABLE 2
TESTS

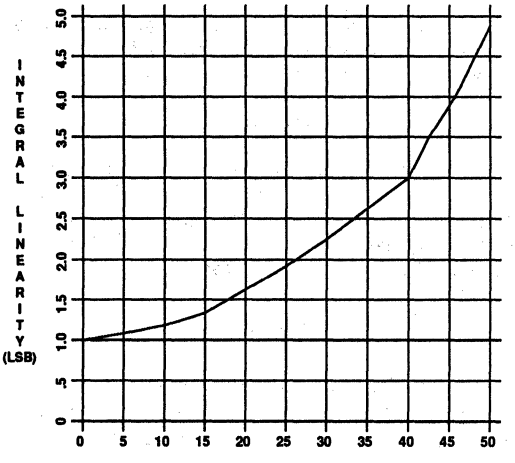
The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

(Table from H. P. Product Note 5180A-2)

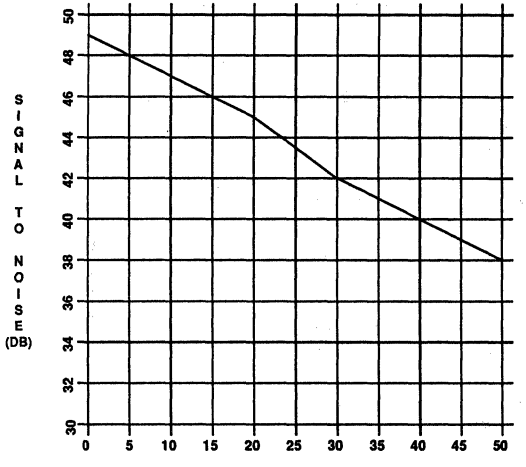
ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperature Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Noise	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth.
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

CHARACTERIZATION GRAPHS

DFT DERIVED THD VERSUS
INPUT FREQUENCY FOR 125 MSPS

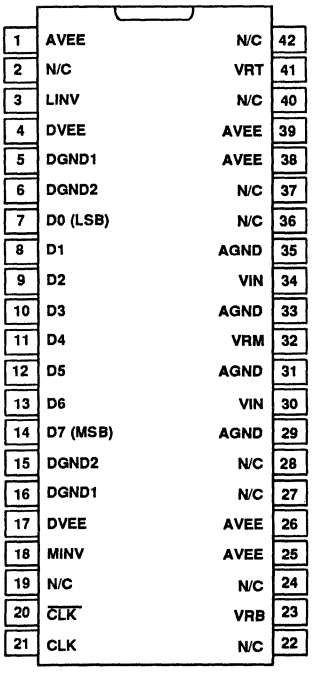


DYNAMIC LINEARITY VERSUS
INPUT FREQUENCY FOR 125 MSPS



DFT DERIVED SNR VERSUS
INPUT FREQUENCY FOR 125 MSPS

PIN ASSIGNMENT HADC77100



42 LEAD CERAMIC SIDEBRAZED DIP

PIN FUNCTIONS HADC77100

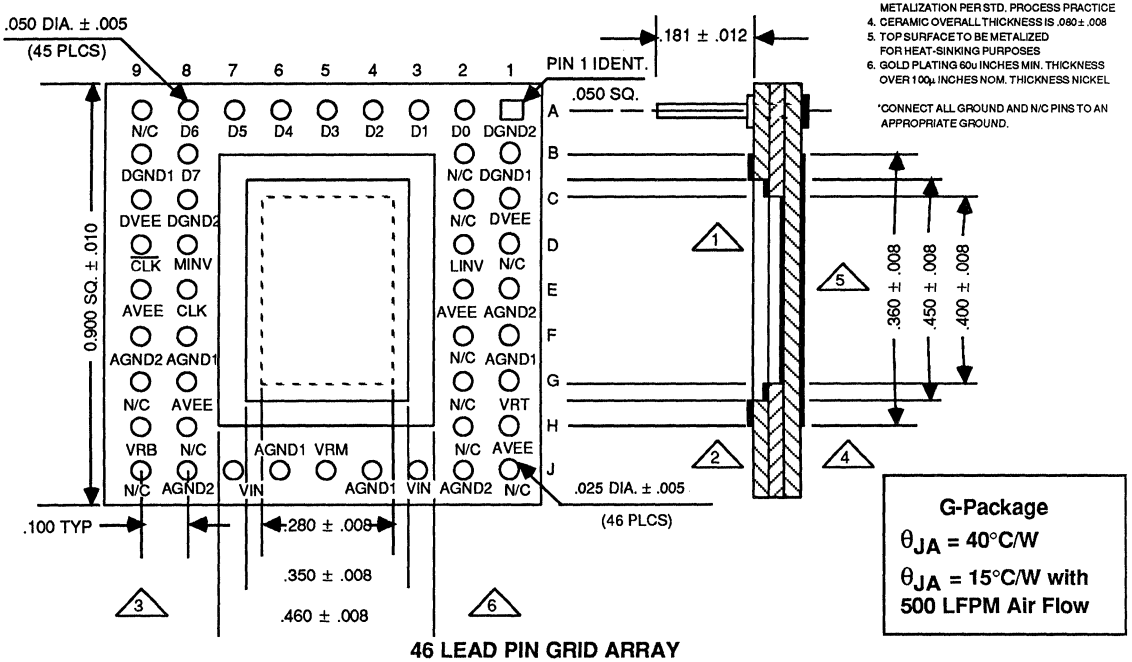
NAME	FUNCTION
AVEE	Negative Analog Supply Nominally -5.2V
LINV	D0 through D6 Output Inversion Control Pin
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
D0	Digital Data Output (LSB)
D1- D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin

NAME	FUNCTION
$\overline{CLK}$	ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRB	Reference Voltage Bottom Nominally -2.0V
AGND	Analog Ground
VIN	Analog Input Can be connected to the input signal or used as Sense
VRM	Reference Voltage Tap Middle
VIN	Analog Input Can be connected to the input signal or used as Sense
VRT	Reference Voltage, Top Nominally 0.0V

NOTES:

1. CAVITY DOWN
2. RING METALIZATION IS .055"
3. DIMENSIONING ON BONDING - PADS & DISTANCE TO THE RING - METALIZATION PER STD. PROCESS PRACTICE
4. CERAMIC OVERALL THICKNESS IS .080 ± .008
5. TOP SURFACE TO BE METALIZED FOR HEAT-SINKING PURPOSES
6. GOLD PLATING 60u INCHES MIN. THICKNESS OVER 100µ INCHES NOM. THICKNESS NICKEL

*CONNECT ALL GROUND AND N/C PINS TO AN APPROPRIATE GROUND.



46 LEAD PIN GRID ARRAY

G-Package
θ_{JA} = 40°C/W
θ_{JA} = 15°C/W with 500 LFPM Air Flow

**For Ordering Information See Section 1.*

NOTES:

HADC77200

8-BIT, 150 MSPS FLASH A/D CONVERTER

PRELIMINARY INFORMATION

FEATURES

- **150 MSPS CONVERSION RATE**
- 100 MHz Full Scale Bandwidth
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Maximum Power Dissipation < 2.7 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Medical Electronics: Ultrasound, CAT Instrumentation

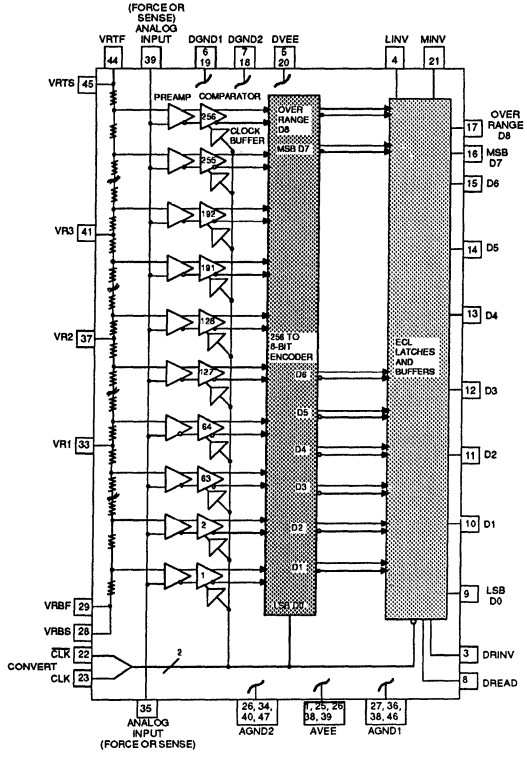
GENERAL DESCRIPTION

The HADC77200 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 100 MHz into 8-bit digital words at a 150 MSPS update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth. A single standard -5.2 Volt power supply is required for operation of the HADC77200, with nominal power dissipation of 2.2 Watts.

The part is packaged in a 48 Lead Ceramic Sidebrazed DIP and a 46 Lead PGA. The HADC77200 includes five external reference ladder TAPS to gain better control over linearity; an overrange bit for use in higher resolution systems; and a data ready output pin for ease in interfacing to high-speed memory. Careful attention to design and layout has provided a device with low noise floor, stable input characteristics, and low data error rate. The HADC77200 is available in Industrial and Military Temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages Output
Negative Supply Voltage (V_{EE} TO GND) ..-7.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5V
A_{VEE} to D_{VEE} Differential.....50mV

Input Voltage
Analog Input Voltage.....+0.5 to V_{EE} V
Reference Input Voltage.....+0.5 to V_{EE} V
Digital Input Voltage.....+0.5 to V_{EE} V
Reference Current VRT to VRB.....25 mA
Midtap Reference Current.....-6 to +6 mA

Output
Digital Output Current.....0 to -25 mA

Temperature
Operating Temperature, ambient.....-65 to +150°C
junction.....+150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity, 77200A		II			±1/2		±1/2		±1/2	LSB
Differential Linearity, 77200A		II			±1/2		±1/2		±1/2	LSB
Integral Linearity, 77200B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77200B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT		I		-8	-15		-15		-15	mV
Offset Error VRB		I		+8	+15		+15		+15	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range		I		-2.0	0.0					VOLTS
Input Capacitance	Over full input range	V		56						pF
Input Resistance		V		4						kΩ
Input Current		II		300	500		450		650	µA
Clock Synchronous Input Currents		V		40						µA

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
POWER SUPPLIES										
Supply Current (analog)		II		360	425		440		425	mA
Supply Current (digital)		II		60	80		85		80	mA
REFERENCE										
Positive Reference Voltage	Operating Condition	I	>VRB		0.0					VOLTS
Negative Reference Voltage	Operating Condition	I	-2.5		<VRT					VOLTS
Reference Tap Current	V_{RM} = -1.00V	IV			4					mA
Ladder Resistance		II	100		160	100	180	80	120	Ω
Reference Bandwidth		V		50						MHz
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	VOLTS
Output Low Voltage	50Ω to -2V	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	VOLTS
Input High Voltage (MINV, LINV)		II	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS
Output Rise Time 10% to 90%	50Ω to -2V	IV			2					ns
Output Fall Time 10% to 90%	50Ω to -2V	IV			2					ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
CONVERSION TIMING, See Figure 1A										
Maximum Sample Rate		II	125	150		125		125		MSPS
Clock Low Width, TPW0		II	4	3		4		4		ns
Clock High Width, TPW1		II	4	3		4		4		ns
Output Latency		IV	1		1	1	1	1	1	CYCLE
Output Delay, TD	Differential Clock	V		4.2						ns
Output Delay Tempco	Differential Clock	V		15						ps/°C

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	II		100						MHz
Small Signal Bandwidth	Vin = 500mV PP	II	100	175						MHz
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	V		1.8						ns
Aperture Delay Tempco	Differential Clock	V		7						ps/°C
Aperture Time		V		<100						ps
Acquisition Time	F.S. to ±1/2 LSB	V		5						ns
Input Slew Rate		V		800						V/µs

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 125MHz										
RMS Sinewave Curve Fit	Vin = FS @ 1MHz	II		8						Bits
RMS Sinewave Curve Fit	Vin = FS @ 25MHz	II		7						Bits
RMS Sinewave Curve Fit	Vin = FS @ 50MHz	II		5.3						Bits
Signal to noise ratio	Vin = FS @ 1MHz	II		48						dB
Signal to noise ratio	Vin = FS @ 25MHz	II		46						dB
Signal to noise ratio	Vin = FS @ 50MHz	II		42						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	V		46						dBc
Total Harmonic Distortion	Vin = FS @ 25MHz	V		38						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	V		34						dBc
Mean Differential Non-Linearity		V		.001						LSB
RMS Differential Non-Linearity		V		.2						LSB
Differential Gain	NTSC 40IRE mod. ramp, Fc = 125MSPS	V		1.0						%
Differential Phase		V		.5						DEG

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity, 77200A		I			±1/4 ±1/2		±1/2		±1/2	LSB
Differential Linearity, 77200A		I			±1/4 ±1/2		±1/2		±1/2	LSB
Offset Error VRT		I		18	-30		-30		-30	mV
Offset Error VRB		I		18	30				30	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range		I	-2.5		+0.5	-2.5	+0.5	-2.5	+0.5	VOLTS
Input Capacitance	Over full input range	V		56						pF
Input Resistance		V		4						kΩ
Input Current		I		300	500		400		750	µA
Clock Synchronous Input Currents		V		40						µA
POWER SUPPLIES										
Supply Current (analog)		I		360	425		450		425	mA
Supply Current (digital)		I		60	80		80		80	mA
REFERENCE										
Positive Reference Voltage	Operating Condition	I	>VRB		0.0					VOLTS
Negative Reference Voltage	Operating Condition	I	-2.5		<VRT					VOLTS
Reference Tap Current	V_{RM} = -1.00V	V			4					mA
Ladder Resistance		II	100		160	130	210	80	120	Ω
Reference Bandwidth		V		50						MHz

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	VOLTS
Output Low Voltage	50Ω to -2V	I	-1.95	1.80	-1.65	-1.95	-1.65	-1.95	-1.70	VOLTS
Input High Voltage (MINV, LINV)		I	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS
Output Rise Time (10% to 90%)	50Ω to -2V				2					ns
Output Fall Time (10% to 90%)	50Ω to -2V				2					ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
CONVERSION TIMING (See Figure1A)										
Maximum Sample Rate		II	125	150						MSPS
Clock Low Width, TPW0		II	4	3						ns
Clock High Width, TPW1		II	4	3						ns
Output Latency		IV	1	1	1	1	1	1	1	CYCLE
Data Ready Delay, TD		II		4.2						ns
Output Delay, TD	Differential Clock	II	3.2	4.2	4.8	6.1	7.3	1.7		ns
Output Delay Tempco		V		15						ps/°C
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	II		100						MHz
Small Signal Bandwidth	Vin = 500mVPP	II	100	175						MHz
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	II	1.2	1.8	2.4	2.4	3.6	.5		ns
Aperture Time		V		<100						ps
Settle-to-Hold Time		V		3						ns
Aperture Delay Tempco	Differential Clock	V		7						ps/°C

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 125MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 125MHz										
RMS Sinewave Curve Fit	Vin = FS @ 1MHz	II		8						Bits
RMS Sinewave Curve Fit	Vin = FS @ 25MHz	I		7						Bits
RMS Sinewave Curve Fit	Vin = FS @ 50MHz	II		5.3						Bits
Signal to noise ratio	Vin = FS @ 1MHz	II		48						dB
Signal to noise ratio	Vin = FS @ 25MHz	I		46						dB
Signal to noise ratio	Vin = FS @ 50MHz	II		42						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	V		46						dBc
Total Harmonic Distortion	Vin = FS @ 25MHz	V		38						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	V		34						dBc
Mean Differential Non-Linearity		V		.001						LSB
RMS Differential Non-Linearity		V		.2						LSB

TEST LEVEL CODE: See page 7.

TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests performed after a 3 min. power soak.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperatures.
II	100% production tested at Ta = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

GENERAL DESCRIPTION

The HADC77200 is the fastest monolithic 8-bit parallel flash A/D converter available today. The conversion rate is 150 MSPS and the analog bandwidth is in excess of 100 MHZ. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This reduces clock transient kickback to the input and reference ladder. The preamplfiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces meta-stable states that can cause errors at the output.

An additional advantage of the HADC77200 over similar devices is a better integral linearity specification over the part's entire usable range.

The center reference ladder taps are optional as needed to futher decrease this specification.

The HADC77200 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77200 has an on-board power supply bypass of 1500pF to reduce external component needs, and the output drive capability of the device can provide full ECL swings into 50Ω loads.

TYPICAL INTERFACE CIRCUIT

The HADC77200 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows.

AVEE, DVEE, AGND, DGND

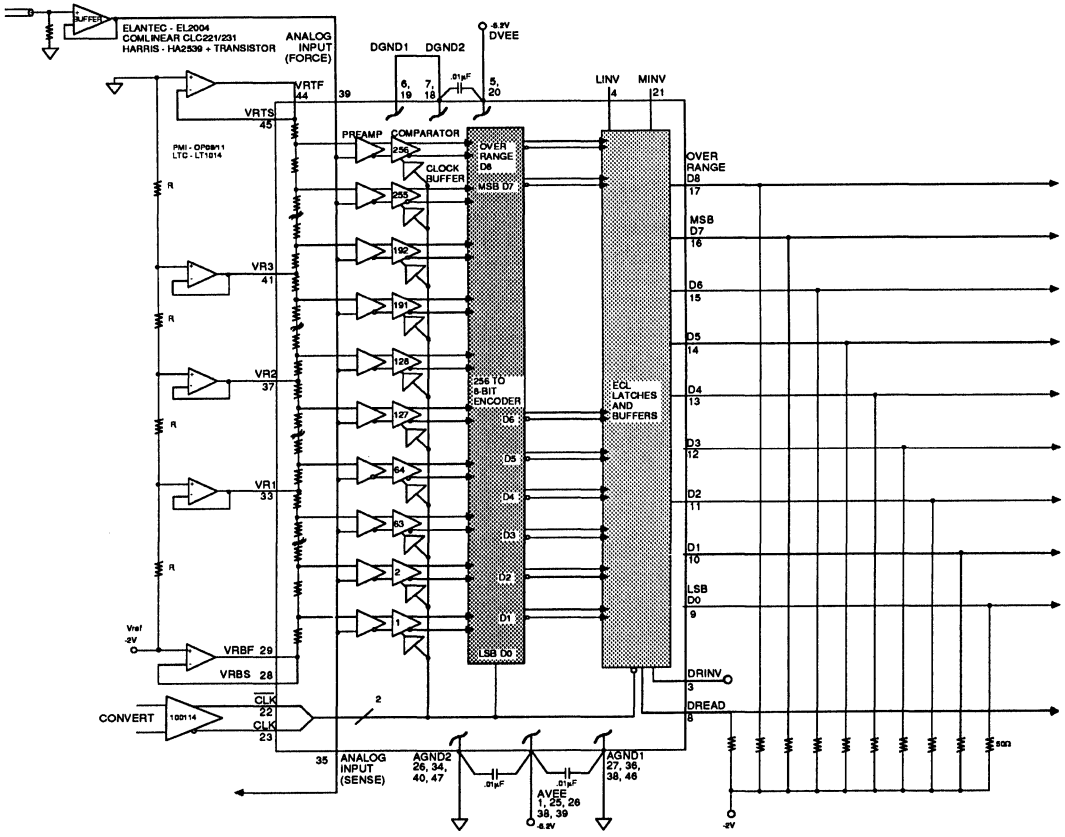
The analog and digital supply and ground pins are physically connected on the device. It is recommended to take advantage of the noise suppression benefits by utilizing separate ground and supply planes when operating the part above 50 MSPS clock rates.

If separate AVEE and DVEE are used, be sure to power both up simultaneously to avoid damaging the device. The digital and analog power supply terminals should be bypassed as close to the device as possible to their respective grounds with at least a .01μF ceramic capacitor. A 1μF tantalum can also be used for low frequency suppression. The digital ground is further divided into internal circuit ground (DGND1) and output ground (DGND2). The digital output ground should be referenced to the pulldown voltage and bypassed to it as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77200 is superior to similar devices due to a preamplifier stage before the comparators. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

FIGURE 1 HADC77200 TYPICAL INTERFACE CIRCUIT



CLK, $\overline{CLK}$ (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3V (see clock input circuit on page 12). It may be left open but a .01µF bypass capacitor from $\overline{CLK}$ to DGND1 is recommended. The duty cycle of the clock is not important as long as minimum pulse width is maintained.

MINV, LINV (Output Logic Control)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table 1. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to DGND1 through a diode or 3.9kΩ resistor.

D0 to D7 (Digital Outputs)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V the outputs can drive 130Ω to 1KΩ loads.

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (Reference Inputs)

These are five external reference voltage taps from -2V (VRB) to AGND (VRT) which can be used to control integral linearity over temperature. The TAPS can be can be driven by Op amps as shown in Figure 1. These voltage level inputs can be bypassed to AGND for futher noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD (Data Ready), DRINV (Data Ready Inverse)

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the HADC77200's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin. Timing is shown in Figure 1A.

D8 (Overrange)

This is an overrange function. When the HADC77200 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the HADC77200 into higher resolution systems.

N/C

All "Not Connected" pins should be tied to DGND1 on the left side of the package and to AGND on the right side.

TABLE 1 - OUTPUT CODING

	MINV LINV	0 0	0 1	1 0	1 1
	0V	111...11	100...00	011...11	000...00
	.	111...10	100...01	011...10	000...01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
V_{IN}	.	100...00	111...11	000...00	011...11
	.	011...11	000...00	111...11	100...00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000...01	011...10	100...01	111...10
	-2V	000...00	011...11	100...00	111...11

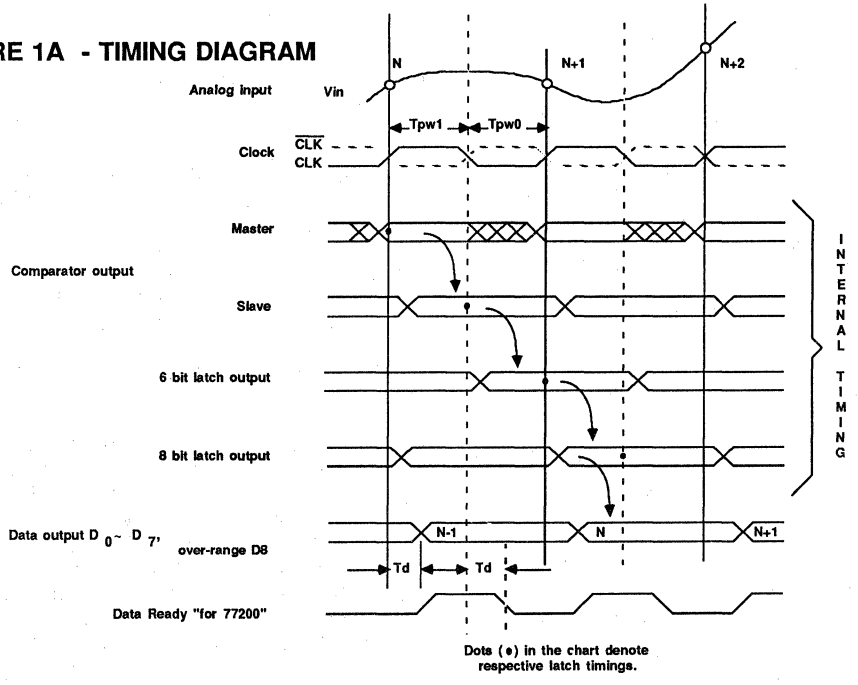
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

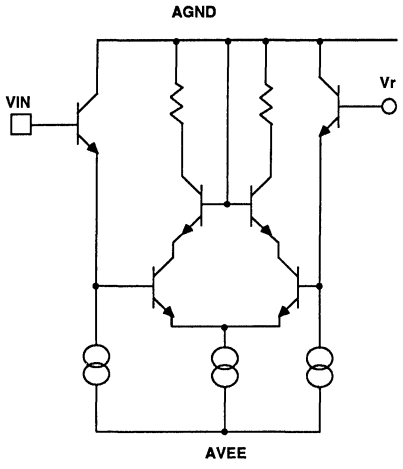
OPERATION

The HADC77200 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram on page 1. This voltage is applied to the positive input of each preamplifier and comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT(0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from four columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions and they consist of a set of eight XOR gates. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

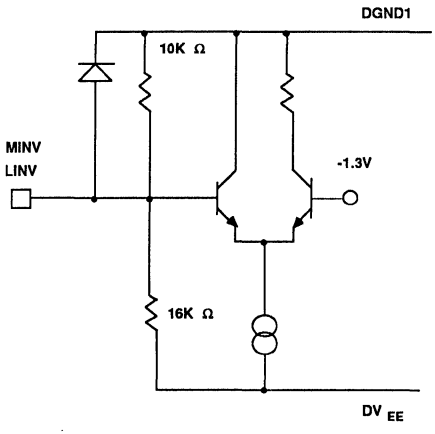
FIGURE 1A - TIMING DIAGRAM



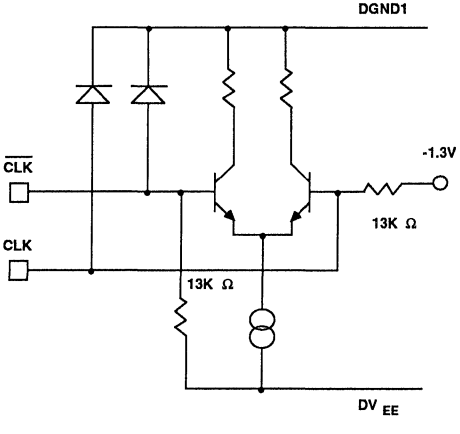
INPUT CIRCUIT



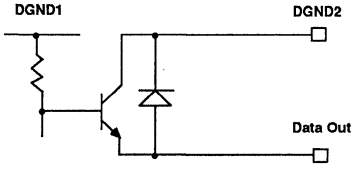
DRINV, MINV, LINV INPUT CIRCUIT



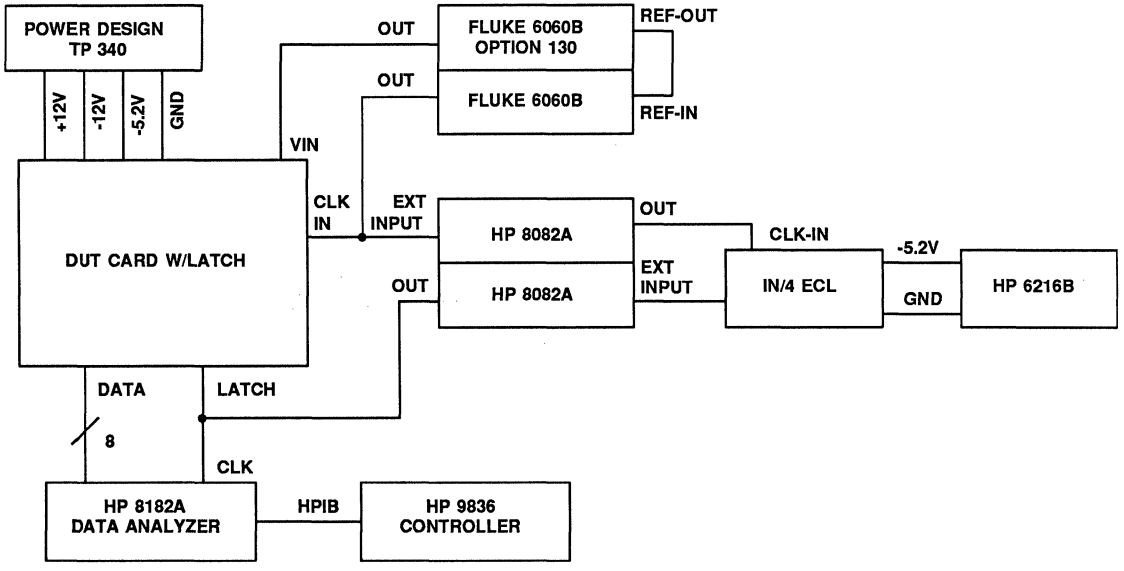
CLOCK INPUT



OUTPUT CIRCUIT D0 THROUGH D8, DREAD

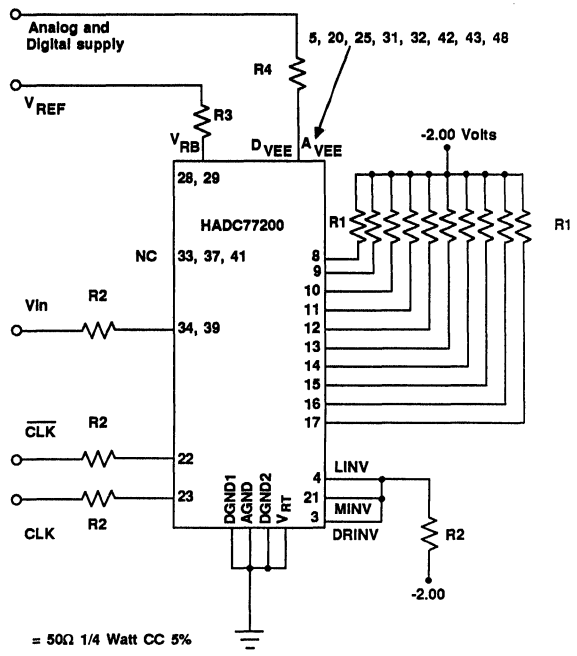


DYNAMIC EVALUATION



BURN-IN CIRCUIT

$T_{BURN-IN}$ = 125°C



R1 = 50Ω 1/4 Watt CC 5%

R2 = 1KΩ 1/4 Watt CC 5%

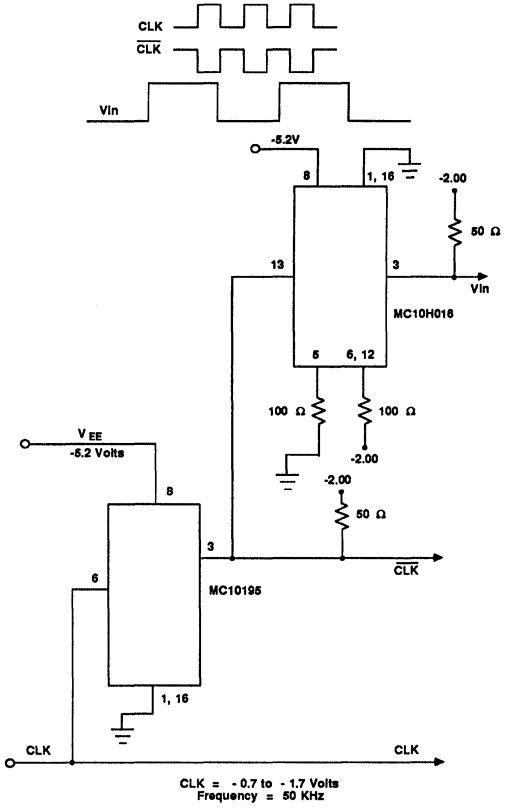
R3 = 6.5Ω 1/4 Watt CC 5%

R4 = 3.25Ω 1/2 Watt CC 5%

V_{REF} = -2.00 Volts

V_{EE} = -6.6 Volts

Pin numbers refer to dip packages only.



CIRCUIT TO GENERATE CLOCK AND INPUT FOR BURN-IN CIRCUIT

DEFINITION OF TERMS

SPECIFICATIONS

A/D CONVERTER ERROR SUMMARY

Honeywell SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 2B) while a static dc input level may appear close to the ideal (Figure 2A). That is why we are including many dynamic tests as well as the the industry standard dc specifications.

EFFECTIVE BITS (SNR)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from measured rms error for the ideal sinewave and the measured actual rms error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual rms error}}{\text{ideal rms error}}$$

Furthermore, signal-to-noise ratio (SNR) can be related to effective bits by the following formula:

$$\text{SNR(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D tranfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q = FSR/2^N where FSR = full scale range and N = 8. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 2A and 2B).

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 2B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77200's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 2B points out two missed codes in the transfer function.

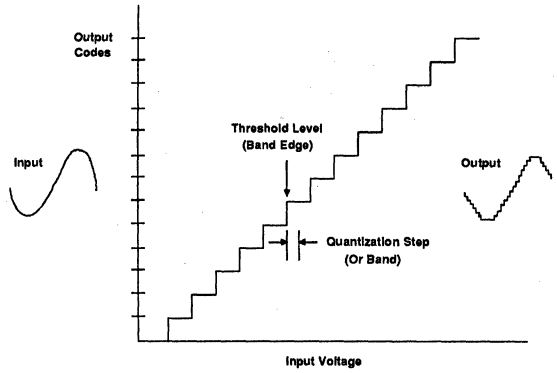


Figure 2A Static Input Conditions

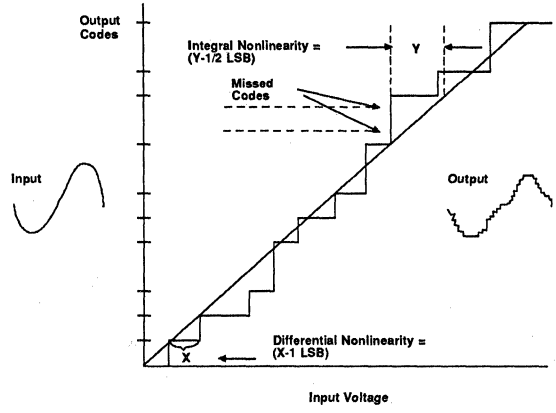


Figure 2B Dynamic Conditions

SPECIFICATIONS CONTINUED

INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 3A). Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 2B shows an integral nonlinearity error of 2 LSB. The HADC77200's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 1. The resulting effect on the linearity is shown in Figure 3B.

APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 3C .

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 4 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from Figure 4 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70ps.

Aperture time and delay are very difficult to measure, however these values are needed to make intelligent design decisions. Honeywell SPT supplies these values for the HADC77200 based on both computer design simulations and verified by characterization of samples.

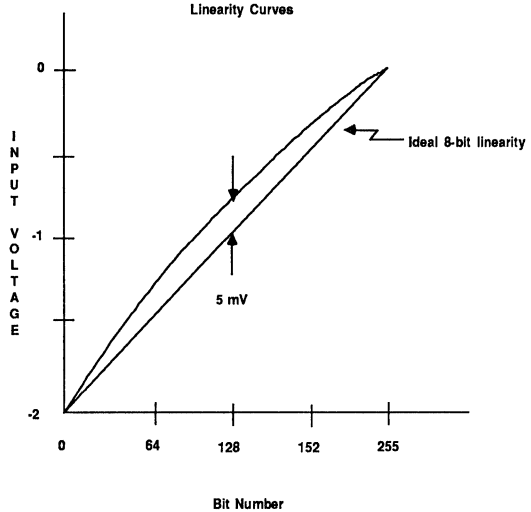


FIGURE 3A Linearity Curve with no TAP adjustment

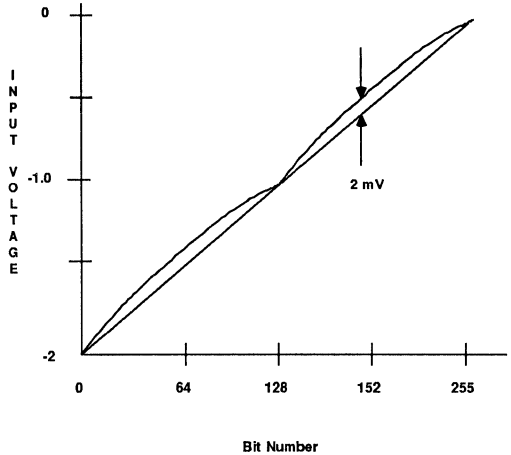


FIGURE 3B Linearity Curve with TAPS Forced to Within .5mV of Ideal

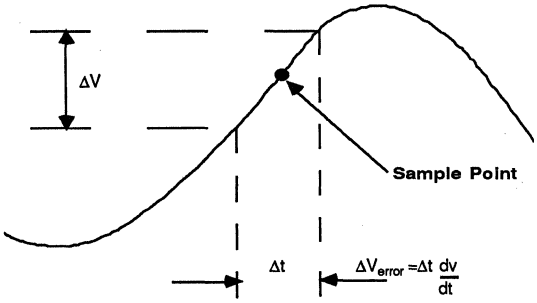


FIGURE 3C Aperture Uncertainty

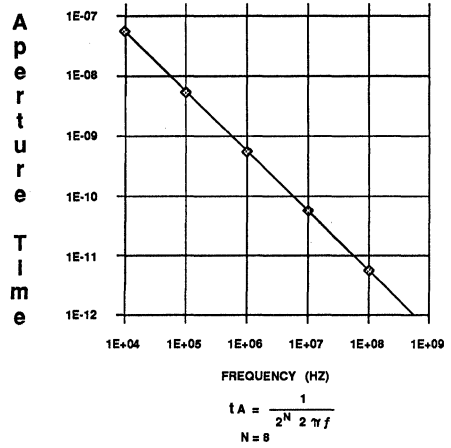
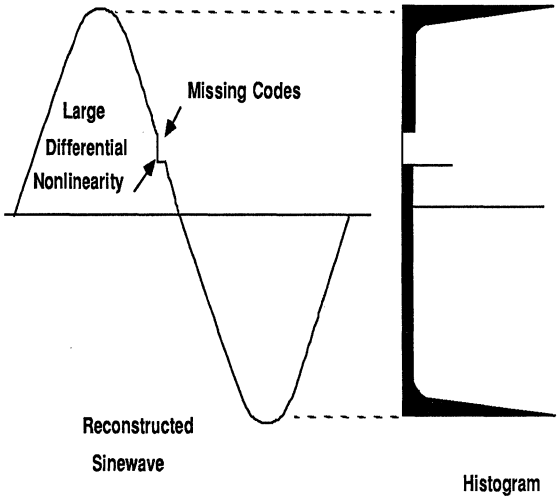


FIGURE 4 Aperture Time - Sinewaves



In the histogram test, A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FIGURE 5 Histogram Testing

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 2.

HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77200. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurance along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurance at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 5).

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased

SPECIFICATION TESTING CONTINUED:

into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table 2.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77200. Using least squared error minimization techniques, an idealized sinewave fit to the data is calulated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A,f,θ,DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave, $A_0\sin(2\pi f_0 t+\theta_0)+DC_0$ is then subtracted from the digitized time record.

The rms errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77200. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

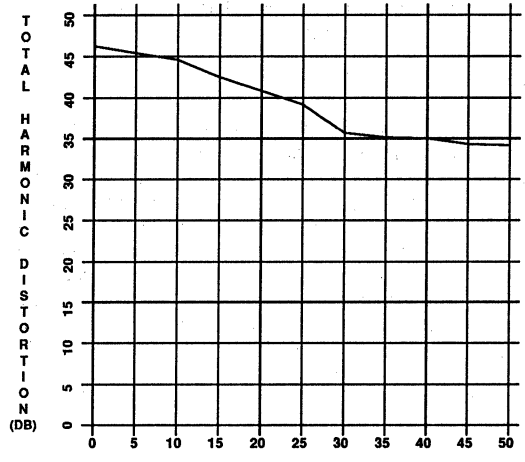
TABLE 2
TESTS

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

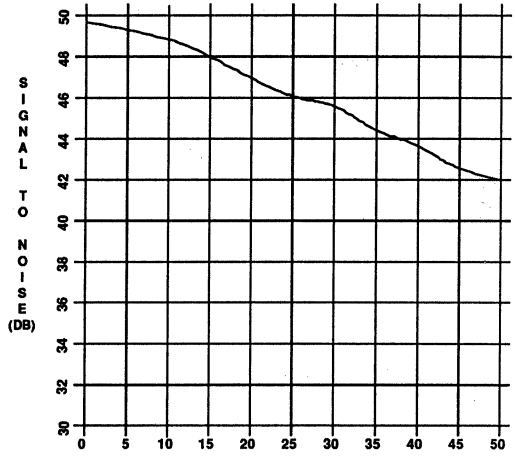
(Table from H. P. Product Note 5180A-2)

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperature Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Noise	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth.
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

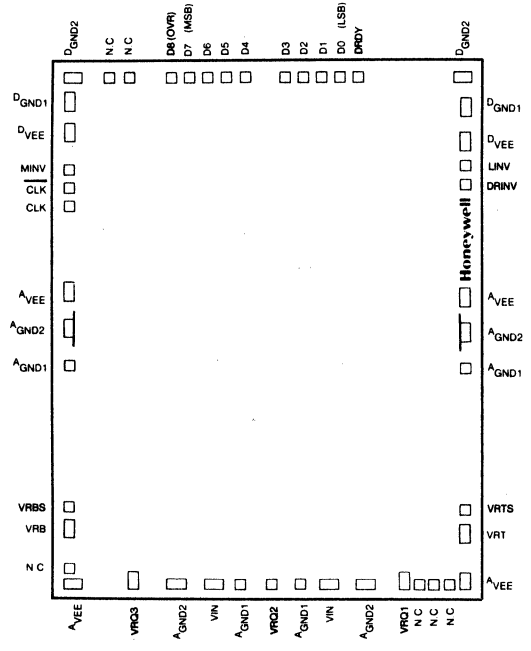
CHARACTERIZATION GRAPHS



DFT DERIVED THD VERSUS
INPUT FREQUENCY FOR 125 MSPS



DFT DERIVED SNR VERSUS
INPUT FREQUENCY FOR 125MSPS



DIE LAYOUT

PIN ASSIGNMENT HADC77200

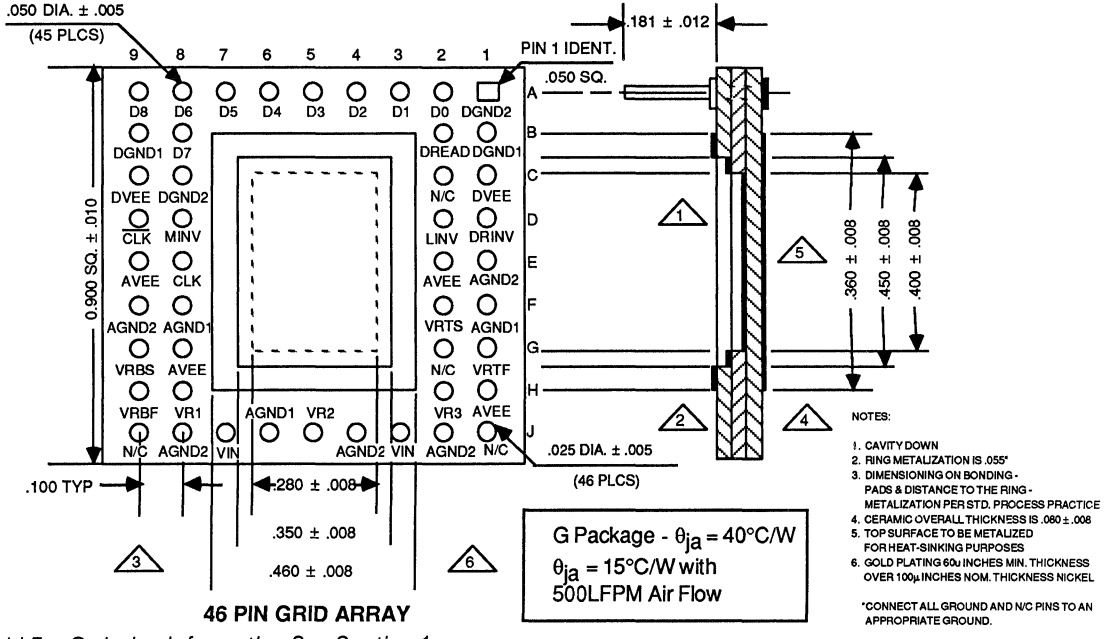
TOP VIEW

1	N/C	AVEE	48
2	N/C	AGND2	47
3	DRINV	AGND1	46
4	LINV	VRTS	45
5	DVEE	VRTF	44
6	DGND1	AVEE	43
7	DGND2	AVEE	42
8	DREAD	VR3	41
9	D0 (LSB)	AGND2	40
10	D1	VIN	39
11	D2	AGND1	38
12	D3	VR2	37
13	D4	AGND1	36
14	D5	VIN	35
15	D6	AGND2	34
16	D7 (MSB)	VR1	33
17	D8 (OVERRANGE)	AVEE	32
18	DGND2	AVEE	31
19	DGND1	N/C	30
20	DVEE	VRBF	29
21	MINV	VRBS	28
22	$\overline{CLK}$	AGND1	27
23	CLK	AGND2	26
24	N/C	AVEE	25

48 LEAD CERAMIC SIDEBRAZED DIP

NAME	FUNCTION
DRINV	Data Ready Inverse
LINV	D0 through D6 Output Inversion Control Pin
AVEE	Negative Analog Supply Nominally -5.2V
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
DREAD	Data Ready Output
DO	Digital Data Output Pin 1 (LSB)
D1~D6	Digital Data Output Pin 2 Through 6
D7	Digital Data Output Pin 7 (MSB)
D8	Overrange Output
MINV	D7 Output Inversion Control Pin

NAME	FUNCTION
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRBS	Reference Voltage Bottom, Sense Nominally -2.0V
VRBF	Reference Voltage Bottom, Force Nominally -2.0V
VR1	Reference Voltage Tap 1
AGND1	Analog Ground 1
VIN	Analog Input , can be connected to the input signal or used as a Sense
AGND2	Analog Ground 2
VR2	Reference Voltage Tap 2
VIN	Analog Input , can be connected to the input signal or used as a Sense.
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense Nominally 0V
VRTF	Reference Voltage Top, Force Nominally 0V



46 PIN GRID ARRAY

***For Ordering Information See Section 1.*

NOTES:

HADC77300

8-BIT, 250 MSPS FLASH A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- **250 MSPS CONVERSION RATE**
- 150 MHz Full Scale Bandwidth
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Maximum Power Dissipation < 4.3 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Medical Electronics: Ultrasound, CAT Instrumentation

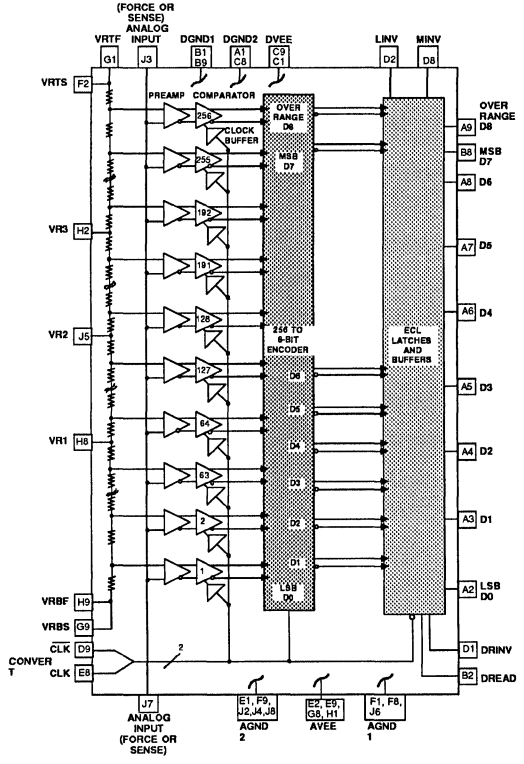
GENERAL DESCRIPTION

The HADC77300 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 150 MHz into 8-bit digital words at a 250 MSPS update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth. A single standard -5.2 Volt power supply is required for operation of the HADC77300, with nominal power dissipation of 4 Watts.

The part is packaged in a 46 Lead PGA. The HADC77300 includes five external reference ladder TAPS to gain better control over linearity; an overrange bit for use in higher resolution systems; and a data ready output pin for ease in interfacing to high-speed memory. Careful attention to design and layout has provided a device with low noise floor, stable input characteristics, and low data error rate. The HADC77300 is available in Industrial and Military Temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages Output
Negative Supply Voltage (V_{EE} TO GND) ..-7.0 to +0.5 V
Ground Voltage Differential.....-0.5 to +0.5V
A_{VEE} to D_{VEE} Differential.....50mV

Input Voltage
Analog Input Voltage.....+0.5 to V_{EE} V
Reference Input Voltage.....+0.5 to V_{EE} V
Digital Input Voltage.....+0.5 to V_{EE} V
Reference Current VRT to VRB.....25 mA
Midtap Reference Current.....-6 to +6 mA

Output
Digital Output Current.....0 to -25 mA

Temperature
Operating Temperature, ambient.....-65 to +150°C
junction.....+175°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE
V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity , 77300A		II			±1/2		±1/2		±1/2	LSB
Differential Linearity , 77300A		II			±1/2		±1/2		±1/2	LSB
Integral Linearity, 77300B		II			±3/4		±3/4		±3/4	LSB
Differential Linearity, 77300B (No missing codes)		II			±3/4		±3/4		±3/4	LSB
Offset Error VRT		I	-8	-15		-15		-15		mV
Offset Error VRB		I	+8	+15		+15		+15		mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range		I	-2.0		0.0					Volts
Input Capacitance	Over Full Input Range	V		30						pF
Input Resistance		V		4						kΩ
Input Current		II			1.5					mA
Clock Synchronous Input Currents		V		40						µA

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
POWER SUPPLIES										
Supply Current (Analog)		II			750		775		750	mA
Supply Current (Digital)		II		60	80		85		80	mA
REFERENCE										
Positive Reference Voltage	Operating Condition	I	>VRB		0.0					Volts
Negative Reference Voltage	Operating Condition	I	-2.5		<VRT					Volts
Reference Tap Current	V_{RM} = -1.00V	IV			8					mA
Ladder Resistance		II	100		160	100	180	80	120	Ω
Reference Bandwidth		V		50						MHz
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	Volts
Output Low Voltage	50Ω to -2V	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	Volts
Input High Voltage (MINV, LINV)		II	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	Volts
Input Low Voltage (MINV, LINV)		II	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	Volts
Output Rise Time 20% to 80%	50Ω to -2V	IV			1					ns
Output Fall Time 20% to 80%	50Ω to -2V	IV			1					ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
CONVERSION TIMING, See Figure 1A										
Maximum Sample Rate		II	250			250		250		MSPS
Clock Low Width, TPW0		II	2			2		2		ns
Clock High Width, TPW1		II	2			2		2		ns
Output Delay, TD	Differential Clock	V		2.1						ns
Output Delay Tempco	Differential Clock	V		15						ps/°C

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	II		150						MHz
Small Signal Bandwidth	Vin = 500mV PP	II		200						MHz
Aperture Jitter		V		8						ps RMS
Aperture Delay	Differential Clock	V		1.0						ns
Aperture Delay Tempco	Differential Clock	V		7						ps/°C
Aperture Time		V		<70						ps
Acquisition Time	F.S. to ±1/2 LSB	V		2						ns
Input Slew Rate		V		2						V/ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +85°C MIN	HOT +85°C MAX	COLD -25°C MIN	COLD -25°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 250MHz										
RMS Sinewave Curve Fit	Vin = FS @ 1MHz	II		8						Bits
RMS Sinewave Curve Fit	Vin = FS @ 50MHz	II		7						Bits
RMS Sinewave Curve Fit	Vin = FS @ 100MHz	II		5.3						Bits
Signal to Noise Ratio	Vin = FS @ 1MHz	II		48						dB
Signal to Noise Ratio	Vin = FS @ 50MHz	II		46						dB
Signal to Noise Ratio	Vin = FS @ 100MHz	II		42						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	V		46						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	V		38						dBc
Total Harmonic Distortion	Vin = FS @ 100MHz	V		34						dBc

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
TRANSFER CHARACTERISTICS										
Integral Linearity, 77300A		I			±1/4		±1/2		±1/2	LSB
Differential Linearity, 77300A		I			±1/4		±1/2		±1/2	LSB
Offset Error VRT		I			-15		-15		-15	mV
Offset Error VRB		I			+15				+15	mV
ANALOG INPUT CHARACTERISTICS										
Input Voltage Range	Over Full Input Range	I	-2.5		+0.5	-2.5	+0.5	-2.5	+0.5	Volts
Input Capacitance		V		30						pF
Input Resistance		V		4						kΩ
Input Current		I			1.5					mA
Clock Synchronous Input Currents		V		40						µA
POWER SUPPLIES										
Supply Current (Analog)		I			750		775		750	mA
Supply Current (Digital)		I		60	80		80		80	mA
REFERENCE										
Positive Reference Voltage	Operating Condition	I	>VRB		0.0					Volts
Negative Reference Voltage	Operating Condition	I	-2.5		<VRT					Volts
Reference Tap Current	V_{RM} = -1.00V	V			8					mA
Ladder Resistance		II	100		160	130	210	80	120	Ω
Reference Bandwidth		V		50						MHz

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
DIGITAL LOGIC										
Output High Voltage	50Ω to -2V	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	Volts
Output Low Voltage	50Ω to -2V	I	-1.95	1.80	-1.65	-1.95	-1.65	-1.95	-1.70	Volts
Input Low Voltage (MINV, LINV)		I	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	Volts
Input High Voltage (MINV, LINV)		I	-1.95		-1.48			-1.95	-1.50	Volts
Output Rise Time (20% to 80%)	50Ω to -2V				1					ns
Output Fall Time (20% to 80%)	50Ω to -2V				1					ns

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
CONVERSION TIMING (See Figure1A)										
Maximum Sample Rate		II	250							MSPS
Clock Low Width, TPW0		II	2							ns
Clock High Width, TPW1		II	2							ns
Data Ready Delay, TD		II		2.1						ns
Output Delay, TD	Differential Clock	II		2.1						ns
Output Delay Tempco		V		15						ps/°C
ANALOG INPUTS										
Large Signal Bandwidth	Vin = F.S.	II		150						MHz
Small Signal Bandwidth	Vin = 500mVPP	II	200							MHz
Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	II		1.0						ns
Aperture Time		V		<70						ps
Acquisition Time				2						ns
Aperture Delay Tempco	Differential Clock	V		7						ps/°C

TEST LEVEL CODE: See page 7.

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 250MHz, Duty Cycle = 50%, VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
SIGNAL QUALITY f_{clock} = 250MHz										
RMS Sinewave Curve Fit	Vin = FS @ 1MHz	II		8						Bits
RMS Sinewave Curve Fit	Vin = FS @ 50MHz	I		7						Bits
RMS Sinewave Curve Fit	Vin = FS @ 100MHz	II		5.3						Bits
Signal to noise ratio	Vin = FS @ 1MHz	II		48						dB
Signal to noise ratio	Vin = FS @ 50MHz	I		46						dB
Signal to noise ratio	Vin = FS @ 100MHz	II		42						dB
Total Harmonic Distortion	Vin = FS @ 1MHz	V		46						dBc
Total Harmonic Distortion	Vin = FS @ 50MHz	V		38						dBc
Total Harmonic Distortion	Vin = FS @ 100MHz	V		34						dBc

TEST LEVEL CODE: See following chart.

TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests performed after a 3 min. power soak.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperatures.
II	100% production tested at Ta = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

GENERAL DESCRIPTION

The HADC77300 is ta very wide bandwidth monolithic 8-bit parallel flash A/D converter available today. The minimum conversion rate is 250 MSPS and the analog bandwidth is in excess of 200MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This reduces clock transient kickback to the input and reference ladder. The preamplfiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces meta- stable states that can cause errors at the output.

An additional advantage of the HADC77300 over similar devices is a better integral linearity specification over the part's entire usable range.

The specification is improved from 1/2 LSB to 1/4 LSB. The center reference ladder tap is optional as needed to futher decrease this specification.

The HADC77300 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77300 has an on-board power supply bypass of 1500pF to reduce external component needs, and the output drive capability of the device can provide full ECL swings into 50Ω loads.

TYPICAL INTERFACE CIRCUIT

The HADC77300 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

AVEE, DVEE, AGND, DGND

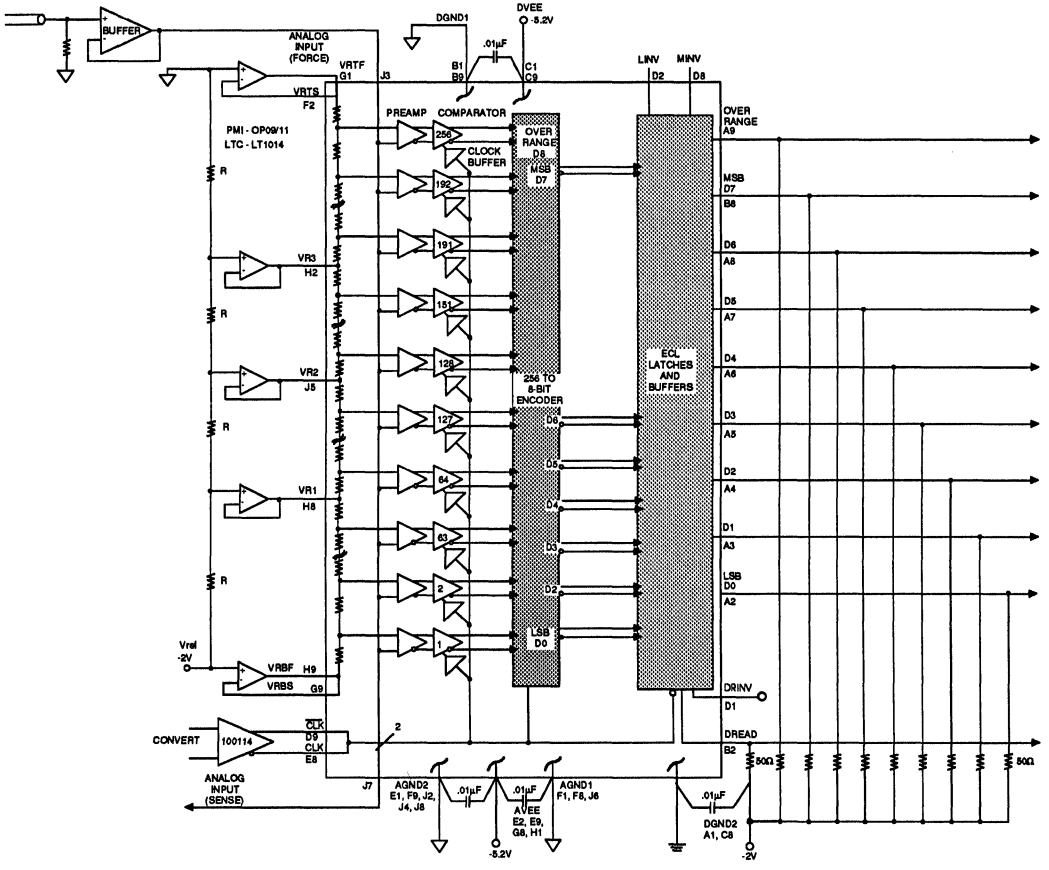
The analog and digital supply and ground pins are physically separated on the device. It is recommended to take advantage of the noise suppression benefits by utilizing separate ground planes when operating the part above 50 MSPS clock rates. Separate supply planes are not necessary for the HADC77300.

If separate AVEE and DVEE planes are used on a board, the AVEE plane can be tied together at the device pins to DVEE because the digital and analog supply pins are connected internally through a 50Ω resistor. There is no need for supply sequencing on the HADC77300 if separate supplies are used. The digital and analog power supply terminals should be bypassed as close to the device as possible to their respective grounds with at least a .01μF ceramic capacitor. A 1μF tantalum can also be used for low frequency suppression. The digital ground is further divided into internal circuit ground (DGND1) and output ground (DGND2). The digital output ground should be referenced to the pulldown voltage and bypassed to it as shown in Figure 1. DGND1 should be connected to AGND if DVEE is connected to AVEE.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77300 is superior to similar devices due to a preamplifier stage before the comparators.

FIGURE 1 HADC77300 TYPICAL INTERFACE CIRCUIT



CLK, $\overline{CLK}$ (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3V (see clock input circuit on page 12). It may be left open but a .01µF bypass capacitor from $\overline{CLK}$ to DGND1 is recommended. The duty cycle of the clock is not important as long as minimum pulse width is maintained.

MINV, LINV (Output Logic Control)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table 1. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to DGND1 through a diode or 3.9kΩ resistor.

D0 to D7 (Digital Outputs)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V the outputs can drive 130Ω to 1KΩ loads.

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (Reference Inputs)

These are five external reference voltage taps from -2V (VRB) to AGND (VRT) which can be used to control integral linearity over temperature. The TAPS can be can be driven by Op amps as shown in Figure 1. These voltage level inputs can be bypassed to AGND for futher noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD (Data Ready), DRINV (Data Ready Inverse)

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the HADC77300's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin. Timing is shown in Figure 1A.

D8 (Overrange)

This is an overrange function. When the HADC77300 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the HADC77300 into higher resolution systems.

N/C

All "Not Connected" pins should be tied to DGND1 or AGND.

TABLE 1 - OUTPUT CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

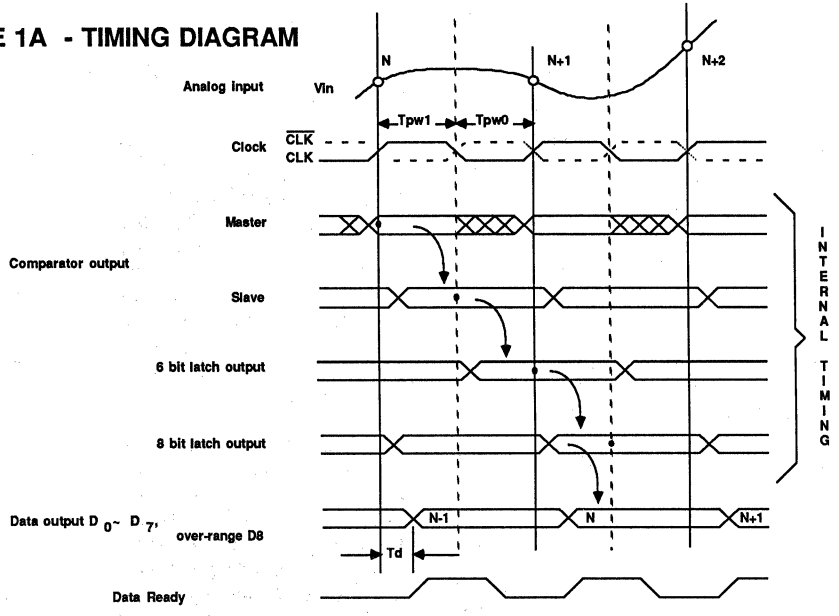
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

OPERATION

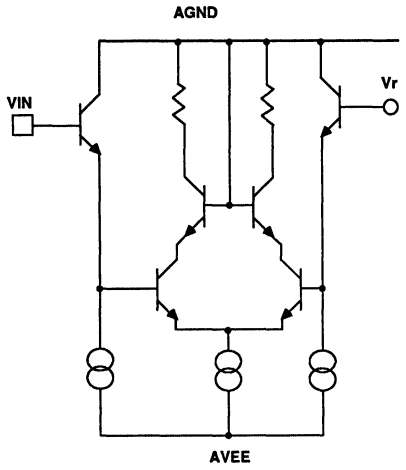
The HADC77300 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram on page 1. This voltage is applied to the positive input of each preamplifier and comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT(0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from four columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions and they consist of a set of eight XOR gates. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

FIGURE 1A - TIMING DIAGRAM

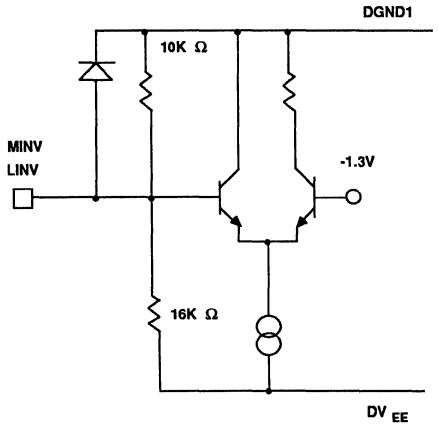


Dots (•) in the chart denote respective latch timings.

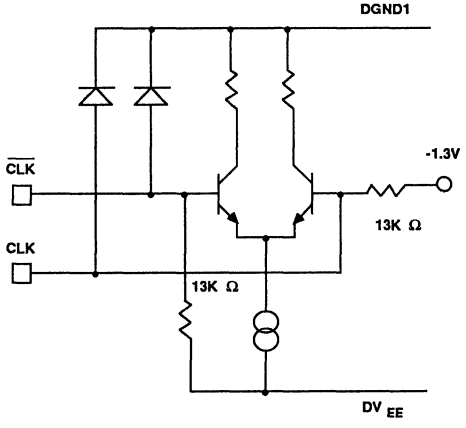
INPUT CIRCUIT



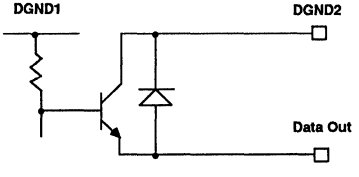
DRINV, MINV, LINV INPUT CIRCUIT



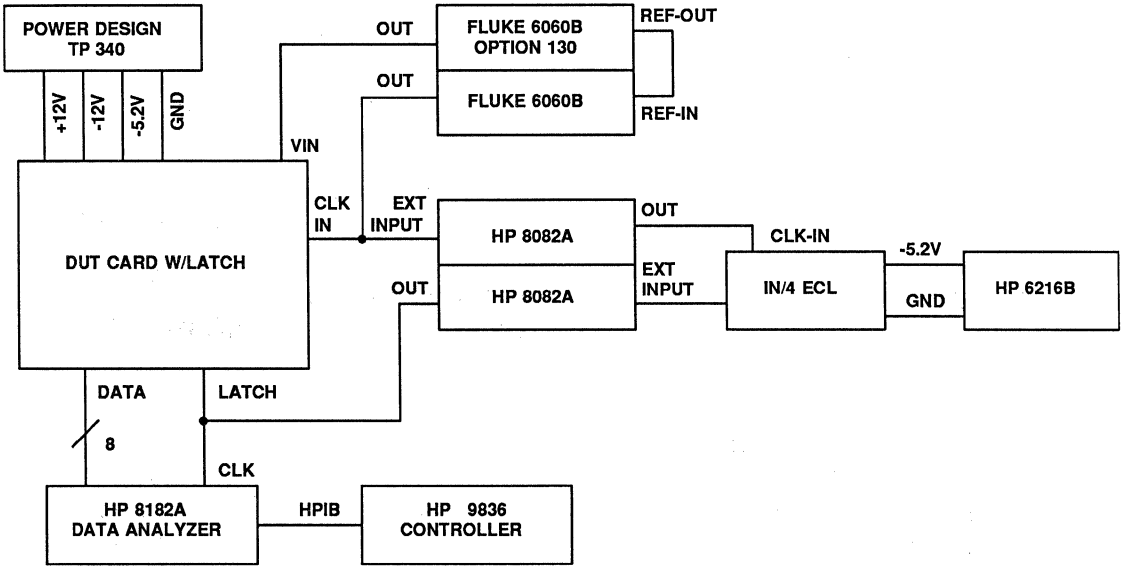
CLOCK INPUT



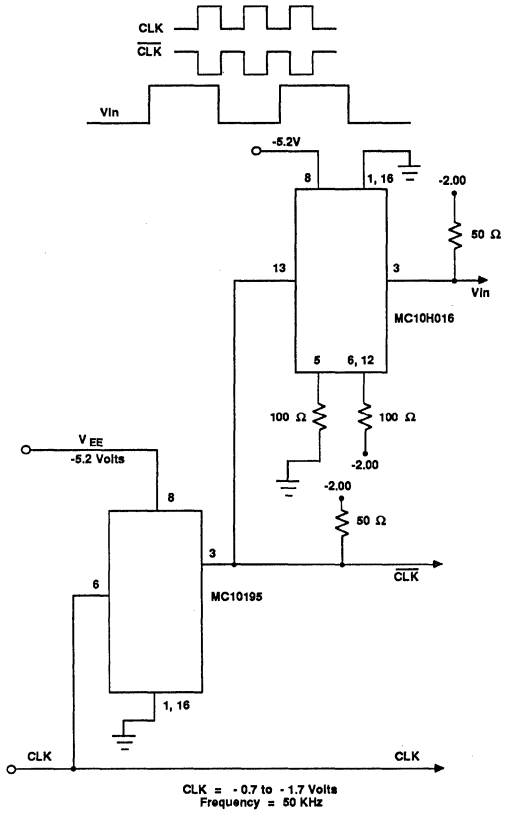
OUTPUT CIRCUIT D0 THROUGH D8, DREAD



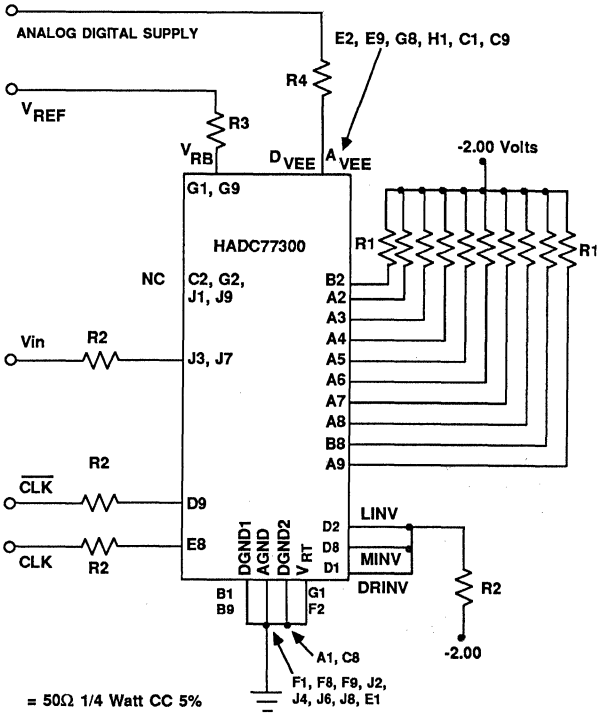
DYNAMIC EVALUATION



CIRCUIT TO GENERATE CLOCK AND INPUT FOR BURN-IN CIRCUIT



BURN-IN CIRCUIT



R1 = 50Ω 1/4 Watt CC 5%

R2 = 1KΩ 1/4 Watt CC 5%

R3 = 6.5Ω 1/4 Watt CC 5%

R4 = 3.25Ω 1/2 Watt CC 5%

V_{REF} = -2.00 Volts

V_{EE} = -6.6 Volts

DEFINITION OF TERMS

SPECIFICATIONS

A/D CONVERTER ERROR SUMMARY

Honeywell SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 2B) while a static dc input level may appear close to the ideal (Figure 2A). That is why we are including many dynamic tests as well as the the industry standard dc specifications.

EFFECTIVE BITS (SNR)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from measured rms error for the ideal sinewave and the measured actual rms error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual rms error}}{\text{ideal rms error}}$$

Furthermore, signal-to-noise ratio (SNR) can be related to effective bits by the following formula:

$$\text{SNR(dB)} = 1.8 + 6.02 \times \text{N(eff bits)}$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D tranfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is Q = FSR/2^N where FSR = full scale range and N = 8. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 2A and 2B).

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 2B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77300's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 2B points out two missed codes in the transfer function.

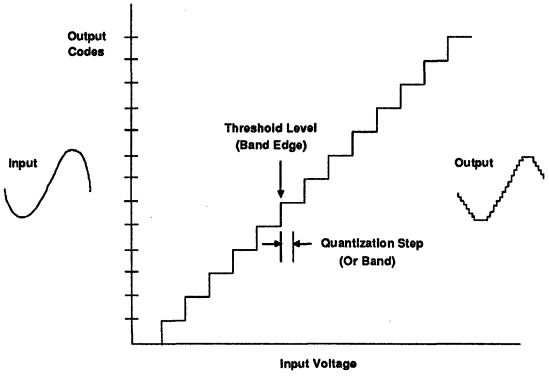


Figure 2A Static Input Conditions

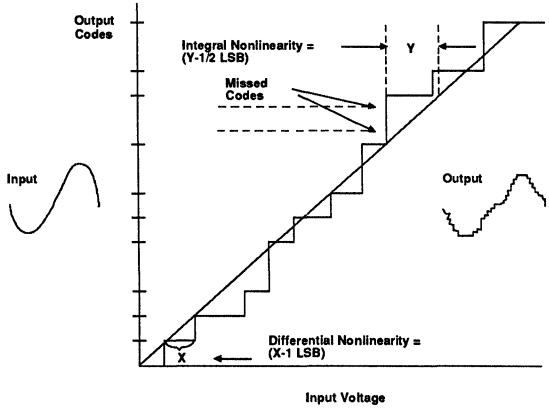


Figure 2B Dynamic Conditions

SPECIFICATIONS CONTINUED

INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 3A). Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 2B shows an integral nonlinearity error of 2 LSB. The HADC77300's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 1. The resulting effect on the linearity is shown in Figure 3B.

APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 3C .

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sinewave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 4 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from Figure 4 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70ps.

Aperture time and delay are very difficult to measure, however these values are needed to make intelligent design decisions. Honeywell SPT supplies these values for the HADC77300 based on both computer design simulations and verified by characterization of samples.

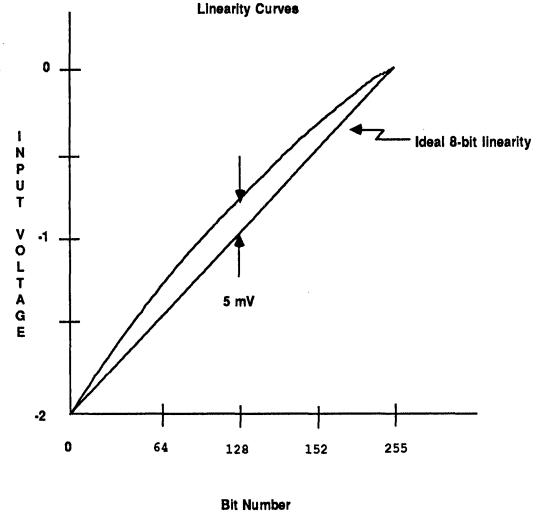


FIGURE 3A Linearity Curve with no TAP adjustment

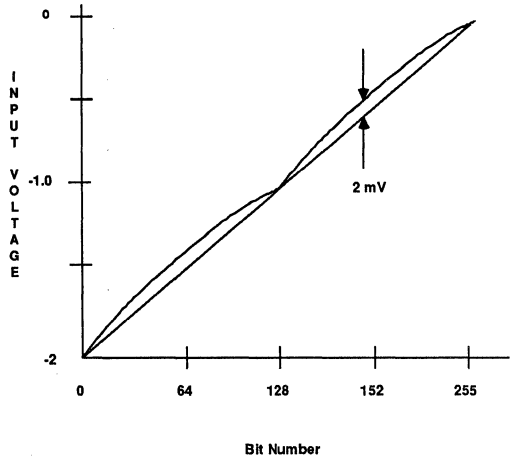


FIGURE 3B Linearity Curve with TAPS Forced to Within .5mV of Ideal

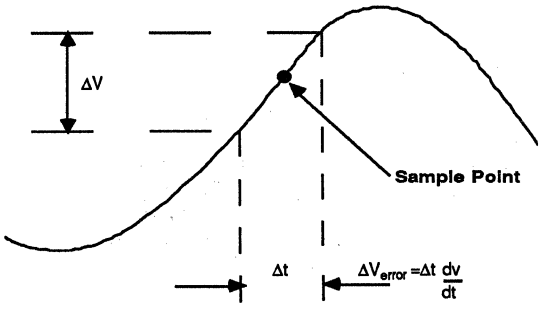


FIGURE 3C Aperture Uncertainty

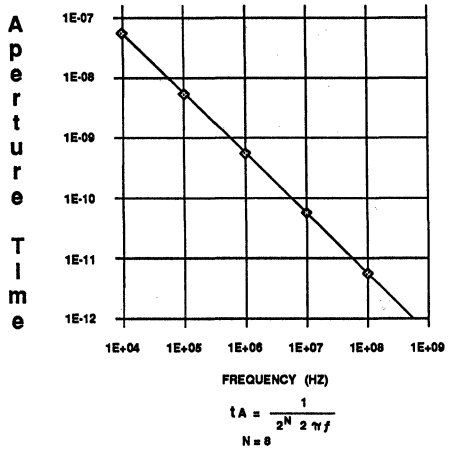
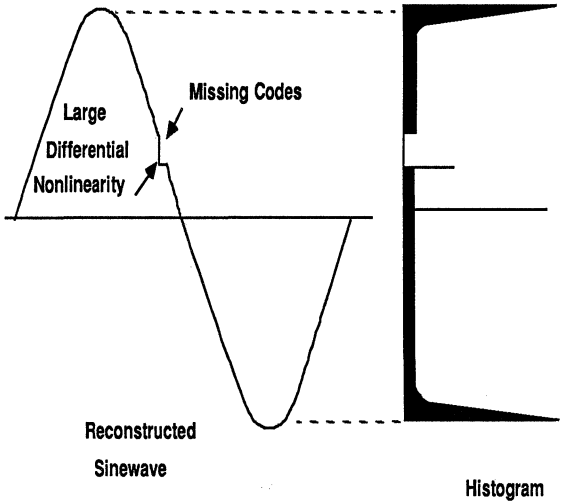


FIGURE 4 Aperture Time - Sinewaves



In the histogram test, A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FIGURE 5 Histogram Testing

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 2.

HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77300. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurance along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurance at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 5).

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sinewave, caused by the integral nonlinearity, are aliased

SPECIFICATION TESTING CONTINUED:

into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table 2.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77300. Using least squared error minimization techniques, an idealized sinewave fit to the data is calulated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A,f,θ,DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave, $A_0\sin(2\pi f_0 t+\theta_0)+DC_0$ is then subtracted from the digitized time record.

The RMS errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77300. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δ f, is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

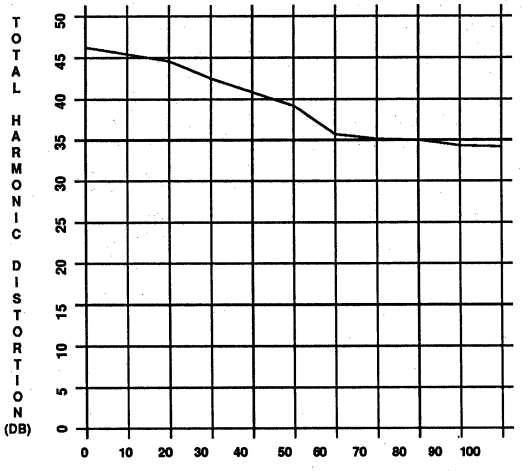
TABLE 2
TESTS

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

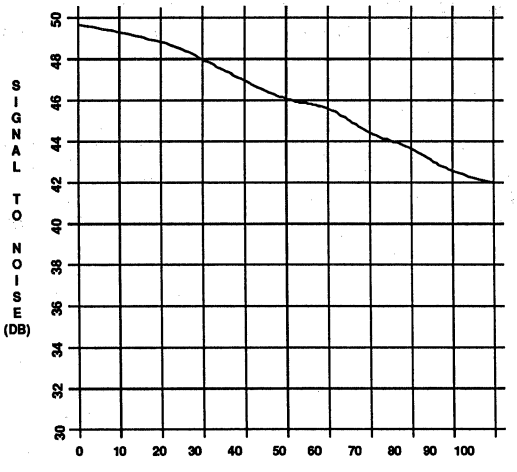
(Table from H. P. Product Note 5180A-2)

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperature Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Noise	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth.
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

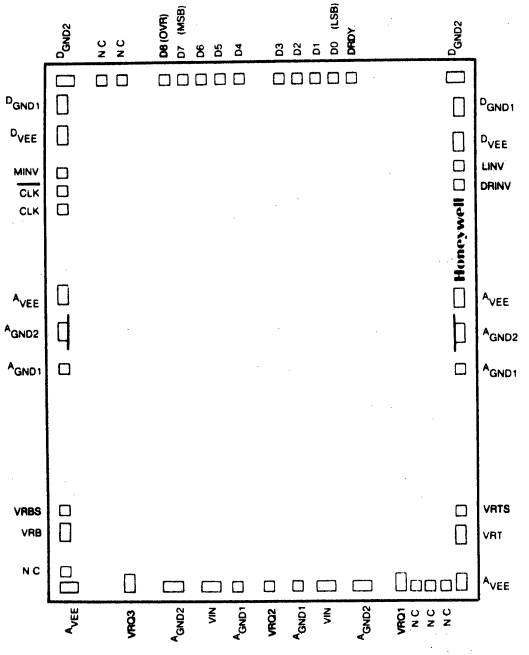
CHARACTERIZATION GRAPHS



DFT DERIVED THD VERSUS INPUT FREQUENCY FOR 250 MSPS



DFT DERIVED SNR VERSUS INPUT FREQUENCY FOR 250 MSPS



DIE LAYOUT

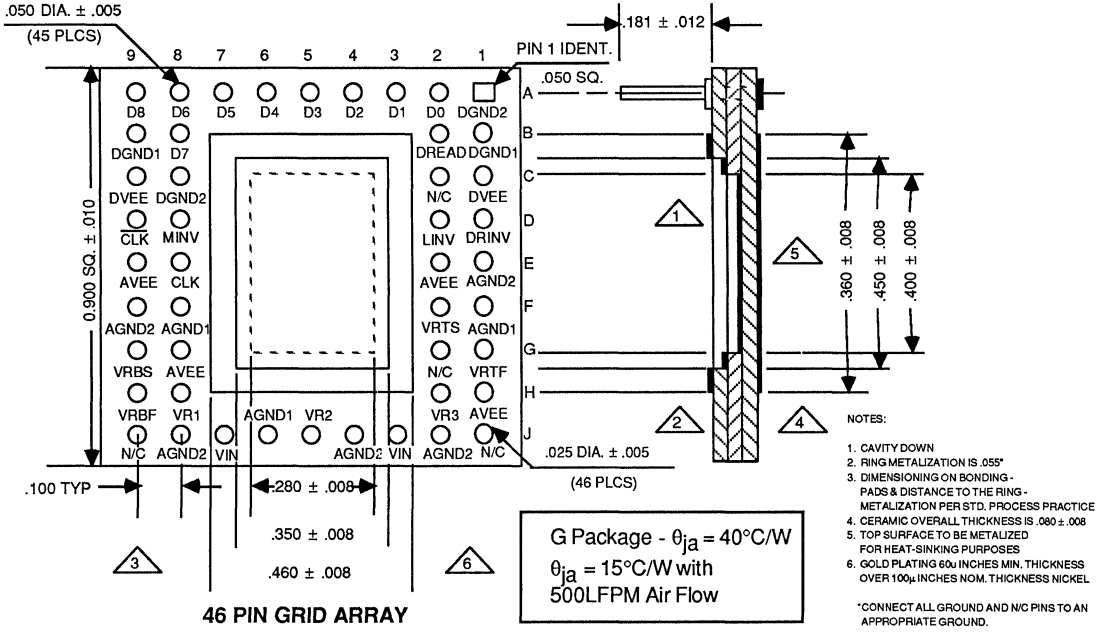
DIE SIZE 225 x 280

HADC77300 PIN ASSIGNMENT

NAME	FUNCTION
DRINV	Data Ready Inverse
LINV	D0 through D6 Output Inversion Control Pin
AVEE	Negative Analog Supply Nominally -5.2V
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
DREAD	Data Ready Output
DO	Digital Data Output Pin 1 (LSB)
D1~D6	Digital Data Output Pin 2 Through 6
D7	Digital Data Output Pin 7 (MSB)
D8	Overrange Output
MINV	D7 Output Inversion Control Pin

NAME	FUNCTION
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRBS	Reference Voltage Bottom, Sense Nominally -2.0V
VRBF	Reference Voltage Bottom, Force Nominally -2.0V
VR1	Reference Voltage Tap 1
AGND1	Analog Ground 1
VIN	Analog Input , can be connected to the input signal or used as a Sense
AGND2	Analog Ground 2
VR2	Reference Voltage Tap 2
VIN	Analog Input , can be connected to the input signal or used as a Sense.
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense Nominally 0V
VRTF	Reference Voltage Top, Force Nominally 0V

HADC77300 PACKAGING INFORMATION



46 PIN GRID ARRAY

***For Ordering Information See Section 1.*

NOTES:

HADC77600

10-BIT, 50 MSPS FLASH ANALOG TO DIGITAL CONVERTER

ADVANCE INFORMATION

FEATURES:

- Output Glitches Eliminated
- Trimmed to ±3/4 LSB
- On-Chip Input Buffer Amplifier
- Gray Coded Logic for Low Noise
- Preamplifier/Comparator Inputs

APPLICATIONS:

- Radar
- Digital Oscilloscopes
- Video Equipment
- Spectrum Analyzers
- Medical Imaging

GENERAL DESCRIPTION

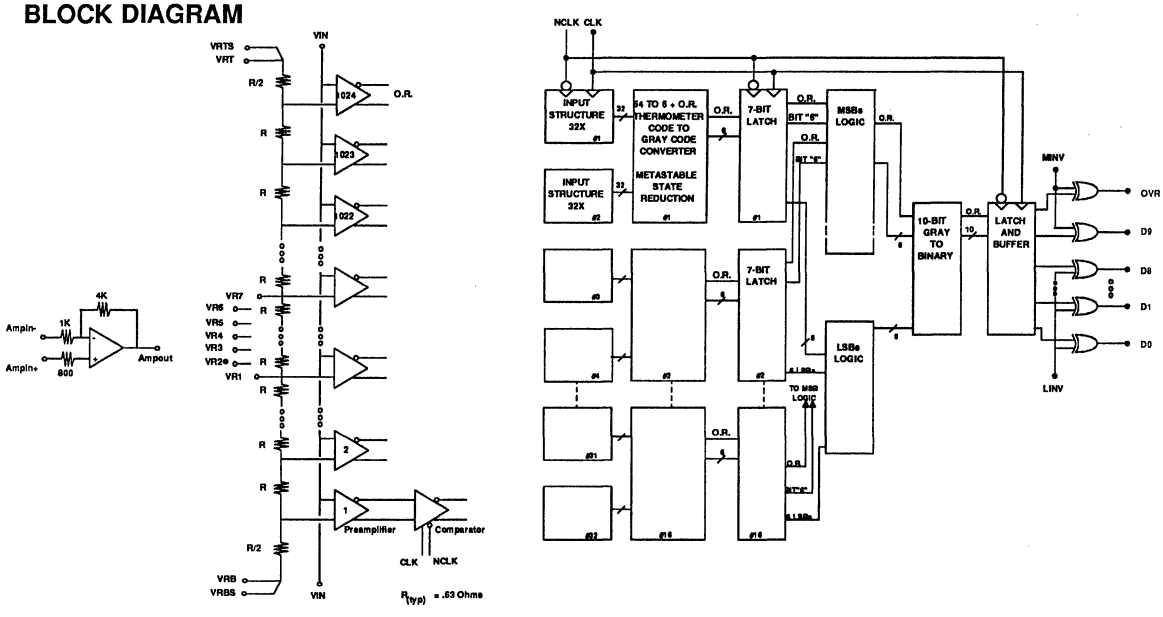
The HADC77600 is a monolithic l0-bit parallel converter with an on-chip buffer amplifier for ease in driving the input. The sample rate can be set up to 50MSPS (75MSPS TYPICAL) for digitizing signals up to 25MHz. Without the input buffer, the full scale input range is -2.0 to +2.0 Volts. With the input amplifier connected, the input range is ± 400mV into a 1KΩ in parallel with 5pF input impedance.

The HADC77600 has a wide bandwidth to allow it to be used in many applications without a track and hold. If a track and hold is required for the application, the converter has excellent step response.

New design techniques have been used to eliminate random errors commonly found in flash converters. Glitches and metastable states have been reduced to the 1 LSB level. This provides a great advantage to designers of single event detection systems for better performance than previously possible.

The device is packaged in a 72-lead Pin Grid Array (PGA), and power dissipation is only 4.7 Watts. Operation is guaranteed over both the commercial and military temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS 25°C (1)

Supply Votages
Positive Supply Votage (VCC to AGND).....+6.0 to -0.5V
Negative Supply Voltage (VEE to AGND)....-6.0 to+0.5V
GND Voltage Differential (AGND to DGND).. +0.5 to -0.5V

Input Voltages
Data, Controls (ECL, measured to AGND).....+0.5 to VEE
Analog (VIN).....+/-2.5V for +/-2.0V Ref

Output
Applied Voltage..... -.8V to + .4V

Temperature
Temperature, ambient.....-60 to +140°C
, junction..... +150°C
Lead Temperature (soldering 10 seconds)....+300°C
Storage Temperature.....-65 to +150°C

Note: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

VCC = +5.0V, VEE = -5.2V, VBIAS = +2.0V, fCLOCK = 50MHz, VRT= 2.0V, VRB= -2.0V, Duty Cycle = 50%, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C Min	Room +25°C Typ	Room +25°C Max	Hot +70°C Min	Hot +70°C Typ	Hot +70°C Max	Cold -25°C Min	Cold -25°C Typ	Cold -25°C Max	Units
TRANSFER CHARACTERISTICS												
Integral Linearity					±1							LSB
Differential Linearity					±3/4							LSB
Offset Error VRT				-15								mV
Offset Error VRB				15								mV
ANALOG INPUT CHARACTERISTICS (ADC)												
Input Voltage Range			-2		+2	-2		+2	-2		+2	Volts
Input Capacitance	Without Amplifier			300								pF
Input Current				1.0								mA
Input Resistance				20								K Ohms
Clock Synchronous Input Currents				50								µA
ANALOG INPUT CHARACTERISTICS (Amplifier)												
Input Voltage Range	Inverting Input		-500		+500	-500		+500	-500		+500	mV
Input Voltage Range	Non-Inverting Input		-400		+400	-400		+400	-400		+400	mV
Input Capacitance				5								pF
Input Resistance	Inverting Non-Inverting			1 500								K Ohms
Input Current				3								µA

(1) See page 4.

ELECTRICAL SPECIFICATIONS

VCC = +5.0V, VEE = -5.2V, VBIAS = +2.0V, fCLOCK = 50MHz, VRT= 2.0V, VRB= -2.0V, Duty Cycle = 50%, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C Min	Room +25°C Typ	Room +25°C Max	Hot +70°C Min	Hot +70°C Typ	Hot +70°C Max	Cold -25°C Min	Cold -25°C Typ	Cold -25°C Max	Units
POWER SUPPLY CHARACTERISTICS												
Positive Supply Current				440								mA
Negative Supply Current				380								mA
Bias Supply Current				130								mA
Power Dissipation				4.7								Watts
REFERENCE CHARACTERISTICS												
Positive Reference Voltage					+2.5							Volts
Negative Reference Voltage				-2.5								Volts
Reference Current				6								mA
Reference Tap Currents				0.4	15							mA
Ladder Resistance				650								Ohms
Reference Bandwidth				10								MHz
DIGITAL LOGIC CHARACTERISTICS												
Output High Voltage	100 Ohms to -2V		-0.98		-0.91	-0.89		-0.70	-1.10		-0.87	Volts
Output Low Voltage	100 Ohms to -2V		-1.95		-1.65	-1.95		-1.57	-1.95		-1.65	Volts
Input High Voltage			-1.13		-0.81	-1.07		-0.67	-1.27		-0.87	Volts
Input Low Voltage			-1.95		-1.48	-1.95		-1.42	-1.95		-1.50	Volts

AC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C Min	Room +25°C Typ	Room +25°C Max	Hot +70°C Min	Hot +70°C Typ	Hot +70°C Max	Cold -25°C Min	Cold -25°C Typ	Cold -25°C Max	Units
CONVERSION TIMING CHARACTERISTICS												
Minimum Sample Rate				50	75							MSPS
Clock Width (tPW)	Figure 1			10								ns
Output Latency					1							Cycle
Output Delay (tD)				5	TBD		8		2			ns
Acquisition Time	Figure 2; Full Scale to .1%			20								ns
Aperture Jitter				12								psRMS
Aperture Delay (tAP)				5								ns
ANALOG INPUT CHARACTERISTICS (Amplifier)												
Slew Rate				300								V/µS
Bandwidth	-3dB			45								MHz
Bandwidth	45° Phase Shift			25								MHz
Settling Time	Full Scale to .1%			30								ns

(1) See page 4.

ELECTRICAL SPECIFICATIONS

VCC = +5.0V, VEE = -5.2V, VBIAS = +2.0V, fCLOCK = 50MHz, VRT= 2.0V, VRB= -2.0V, Duty Cycle = 50%, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C Min Typ Max	Hot +70°C Min Typ Max	Cold -25°C Min Typ Max	Units
SIGNAL QUALITY CHARACTERISTICS (f_{clock} = 50MHz)						
Total Harmonic Distortion	VIN = FS @ 1 MHz		55			dB
Total Harmonic Distortion	VIN = FS @ 5 MHz		50			dB
Total Harmonic Distortion	VIN = FS @ 10 MHz		44			dB
Signal to Noise Ratio	VIN = FS @ 1 MHz		58			dB
Signal to Noise Ratio	VIN = FS @ 5 MHz		55			dB
Signal to Noise Ratio	VIN = FS @ 10 MHz		48			dB
Differential Gain	NTSC 140 IRE Mod. Ramp		TBD			%
Differential Phase			TBD			Degrees

(1) All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level Column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests performed after a three minute power soak.

Test Level I - 100% production tested at the specified temperatures.
Test Level II - 100% production tested at Ta=25°C and sample tested at the specified temperatures.
Test Level III - QA sample tested only at the specified temperatures.
Test Level IV - Parameter is guaranteed (but not tested) by design and characterization data.
Test Level V - Parameter is a typical value for information purposes only.

FIGURE 1. CONVERSION TIME CHARACTERISTICS

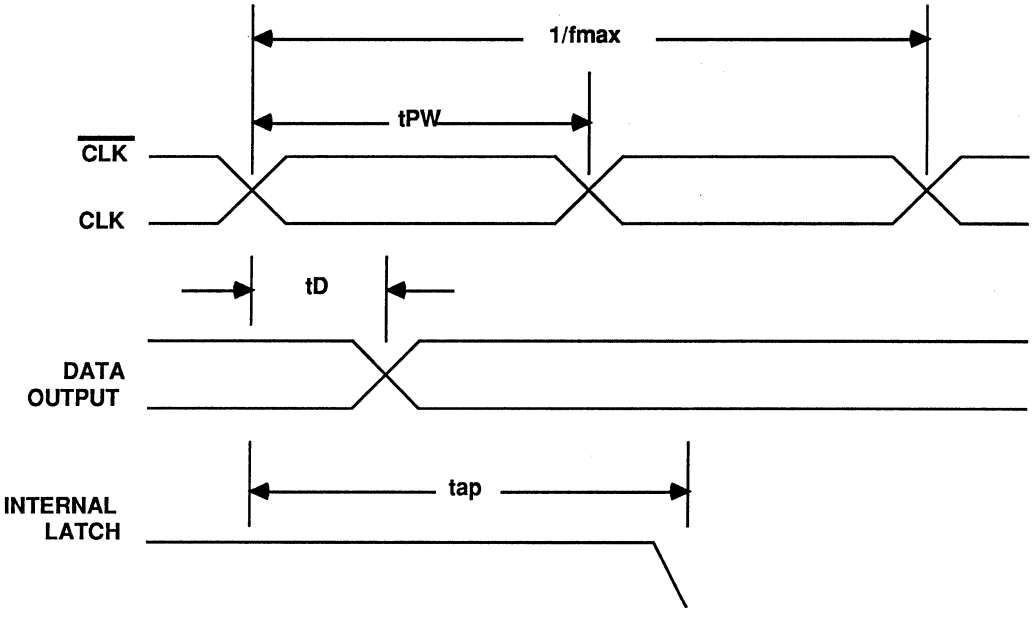
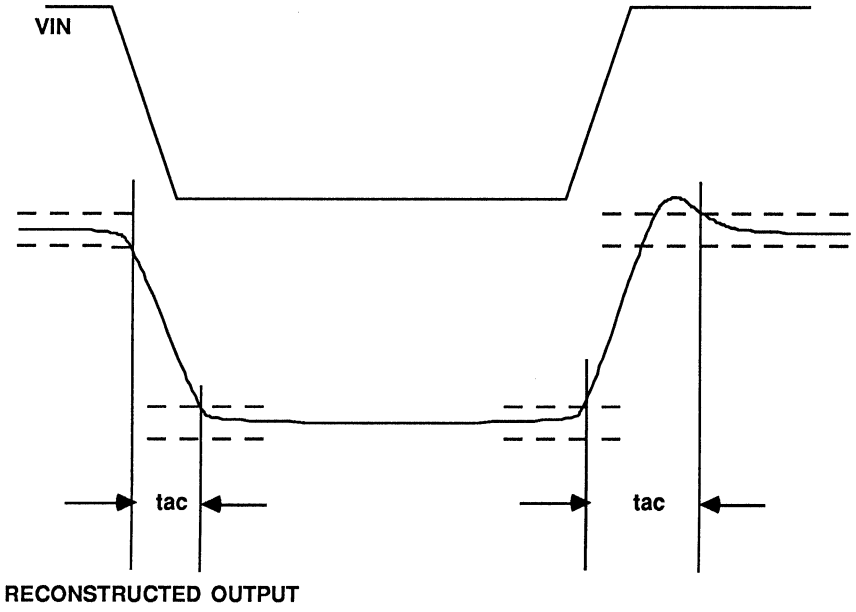


FIGURE 2. ACQUISITION TIME IS WORST CASE VALUE



DESCRIPTION

The HADC77600 is a full parallel 10-bit, 50MSPS (75MSPS Typical) flash converter with linearity trimmed to ± 3/4 LSB and random error reduction to the LSB level. It is designed with preamplifier inputs to each comparator and has an on-chip input amplifier. Linearity is trimmed to better than ± 3/4 LSB without affecting temperature performance or reliability. Data sheet specifications include both time and frequency domain data to assist the designer in making accurate predictions of system performance.

TRIMMING

The linearity of the HADC77600 is capable of being trimmed to at least ±3/4 LSB. The trimming is accomplished by adjusting each of the comparator offsets that is off by greater than 3/4 LSB. The trim sites are set for bipolar adjustments so that either direction of offset is capable of being trimmed. Adjustments are done in discrete steps on metal link sites. This method of trimming completely removes resistors from the circuit. This results in a trim that does not affect either reliability of long-term stability. Stability and reliability are not effected because current carrying structures are not altered, they are either left in the circuit or they are completely removed. The resistor ladder is not altered in any manner.

ERROR REDUCTION

All flash converters prior to the HADC77600 exhibit random errors that are called metastable states or sparkle codes. These errors have the possibility of occurring at any speed or at any code. A similar error is signature error, commonly referred to as glitches. They are most likely to appear at mid, quarter or eighth scale points and the possibility of these errors increases as the input frequency increases. The latter is especially true at the very highest input frequencies that the part is capable of accepting, while random errors increase with clock frequency at a rate that appears to be exponential.

The HADC77600 addresses this problem in a new manner. First a Gray code is used to decrease the internal data synchronous noise. The Gray code also allows the addition of circuitry after the comparators to eliminate errors. The error detection is accomplished by looking for the thermometer code output from the comparators and making an error detection decision based on the comparator outputs.

This thermometer code should have the specific form of all comparators being in either a "0" or a "1" state, and all codes above a certain point should be zeroes and all below should be ones. If this does not occur then an error will be detected. Once an error is detected, the logic looks at a number of codes near the error code or codes, and makes a logical decision of what the correct code should have been. This logical decision can either choose the correct code or it can be off by one LSB. For this reason errors will not be any greater than 1 LSB.

TABLE 1. LOGIC TABLE

Data Format: OVR, D9, D8, D7 through D0

MINV LINV	0 0		0 1		1 0		1 1	
>+1.998V	1	1111111111	1	1000000000	0	0111111111	0	0000000000
+1.996V	0	1111111111	0	1000000000	1	0111111111	1	0000000000
+1.992V	0	1111111110	0	1000000001	1	0111111110	1	0000000001
0.0V	0	1000000000	0	1111111111	1	0000000000	1	0111111111
-0.004V	0	0111111111	0	0000000000	1	1111111111	1	1000000000
-1.996V	0	0000000001	0	0111111110	1	1000000001	1	1111111110
<-1.998V	0	0000000000	0	0111111111	1	1000000000	1	1111111111

Note: Voltages given are the mid-point for the codes.
1 = VOH, 0 = VOL.

REFERENCE LADDER

The ladder of the HADC77600 is composed of 1023 metal resistors of approximately .63 Ohms each and a resistor of half that value at each end of the ladder. Each resistor is actually a different value, with each value calculated to offset the typical 25°C bias current value of the preamplifiers. This results in a typical integral linearity curve that has very little, if any bow due to the effects of the summation of bias currents. The reference top and bottom are both connected to sense pins to reduce the offset of the ladder. In addition to the top and bottom reference points to the ladder there are also external taps to the ladder at 1/8 scale increments. These taps can be used to maintain the ladder's linearity if operation over a wide temperature range in required.

A better use for the ladder taps is in applications, where the linearity of the ladder is to be changed to piece-wise approximate a non-linear transfer function. This is often done to increase the dynamic range of the converter. Each ladder tap has been designed to handle the full reference current so that a wide variety of curves can be accommodated.

The top reference to the ladder is typically driven to +2.0 Volts, and the bottom of the ladder to -2.00 Volts. These points can be driven by any op amp that can supply 6mA. Care must be taken to assure that the amplifier offsets and drifts are commensurate with the system design. Ladder taps can be driven in a similar manner if desired. If they are not used they can be left open or by-passed to VRT or VRB.

INPUT PREAMPLIFIERS

The input to each comparator is buffered by a preamplifier to prevent currents caused by the dynamic switching of the comparator latches from feeding back to the input. These preamplifiers also isolate the ladder from these same currents.

INPUT AMPLIFIER

A wide bandwidth input amplifier has been provided for driving the input to the flash converter. This amplifier has an inverting gain of 4 to reduce the input swing from the ±2Volt full-scale input swings to ±500mV. If the amplifier is not used, then the inputs should be tied to ground and the output should be left floating.

CLK AND $\overline{\text{CLK}}$ INPUTS

The clock inputs are designed to be driven with differential ECL levels. Single-ended operation can be accomplished by bypassing the $\overline{\text{CLK}}$ input, which is internally biased to -1.3V, and driving CLK input.

OVER-RANGE

The over-range output can be used to either alarm the system when an over-range occurs or it can be used in applications where the dynamic range of the system is to be increased by stacking two converters. Over-range is true when the top reference (VRT) is exceeded by l/2 and LSB. The 1/2 rather than 1 LSB limit is the result of the top ladder resistor being 1/2 the value of the other ladder resistors.

OPERATING TEMPERATURE RANGE

The HADC77600 is designed to operate over the full military temperature range. A custom package with the cavity down has been designed for the HADC77600. There is an internal heat sink built into the package. This package has a θ_{JA} of approximately 30°C/W. This can be reduced to 15°C/W by airflow at a rate of 500 LFPM across the package. Further reduction can be obtained by adding a heat sink.

FIGURE 3. BURN-IN SCHEMATIC

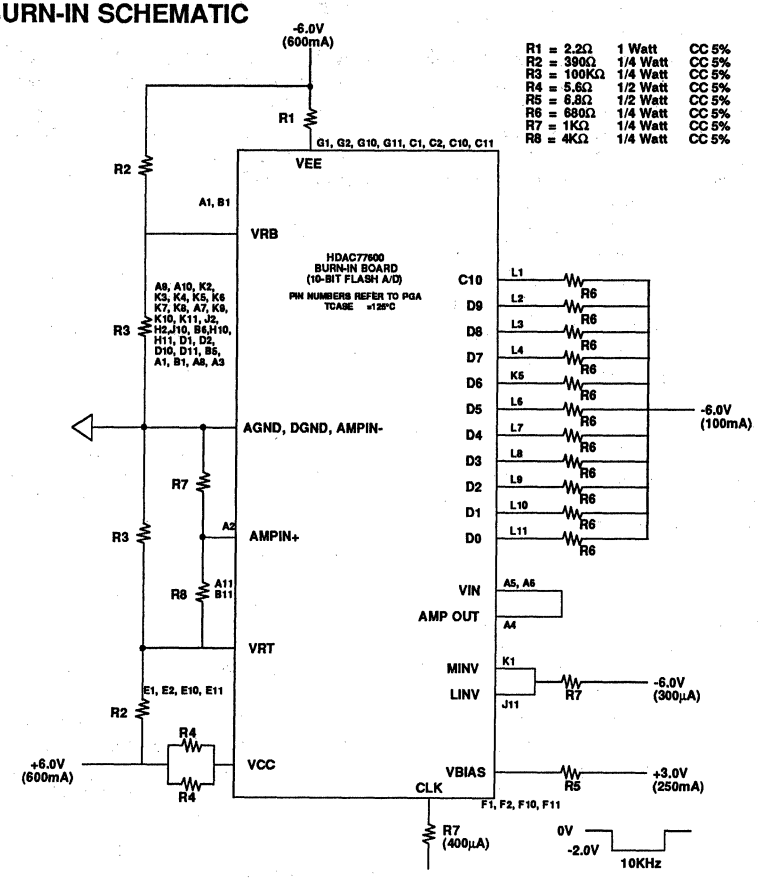
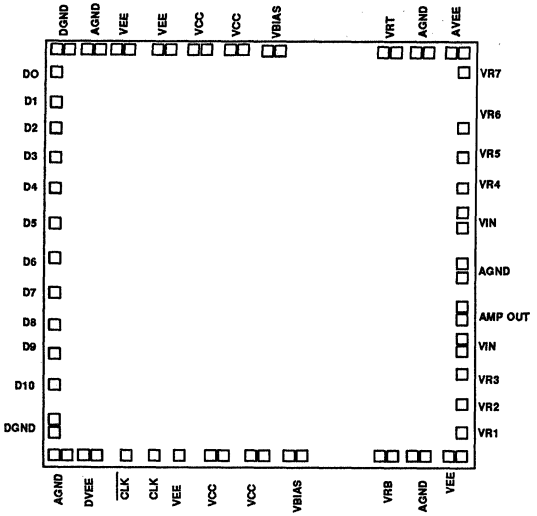


FIGURE 4. 77600 DIE PLOT

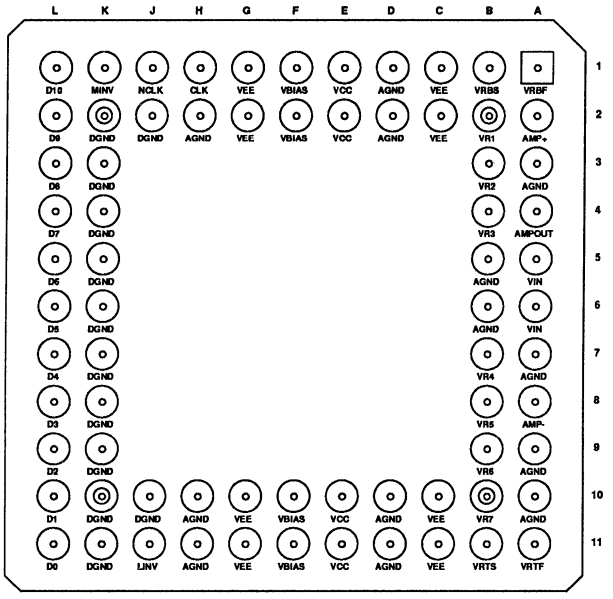


HADC77600 PIN DESCRIPTION

Pins	Description
VEE	Analog and digital negative supply. Typically -5.2 Volts.
VBIAS	Supply voltage. Typically +2.0 Volts.
VCC	Positive digital supply. Typically +5.0 Volts.
AGND	Analog ground.
DGND	Digital ground. Return for ECL outputs. Return to termination ground.
VRT	Most positive reference. Typically +2.00 Volts.
VRTS	Sense pin for the positive reference.
VRB	Most negative reference. Typically -2.00 Volts.
VRBS	Sense pin for the negative reference.
VR1 thru VR7	Reference ladder taps in 1/8 scale increments for ladder adjustments.
LINV	Data complement control for bits 0 through 8.
MINV	Data complement control for bits 9 and 10 (OVR).
AMPIN-	Inverting amplifier input.
AMPIN+	Non-inverting amplifier input.
AMPOUT	Amplifier output.
VIN	Flash converter input.
D0 thru D9	Digital ECL outputs. Capable of driving 100 Ohm loads to 10KH specifications.
D10 or OVR	Over-range bit. True when the input exceeds the voltage at VRT.

HADC77600 PIN OUT

TOP VIEW



**For Ordering Information See Section 1.*

NOTES:

HADC78160

16-BIT, µP COMPATIBLE HIGH PERFORMANCE A/D CONVERTER

ADVANCE INFORMATION

FEATURES

- **3µS CONVERSION RATE**
- Low Power - .9W
- Parallel, serial or 2-byte output configuration
- 16 or 8-bit µP Compatible
- ±2.5V or ±5V pin programmable input
- External or Internal clock

APPLICATIONS

- Sonar
- Digital Scales
- Instrumentation
- Communications
- DSP Interface
- Acoustic Analysis

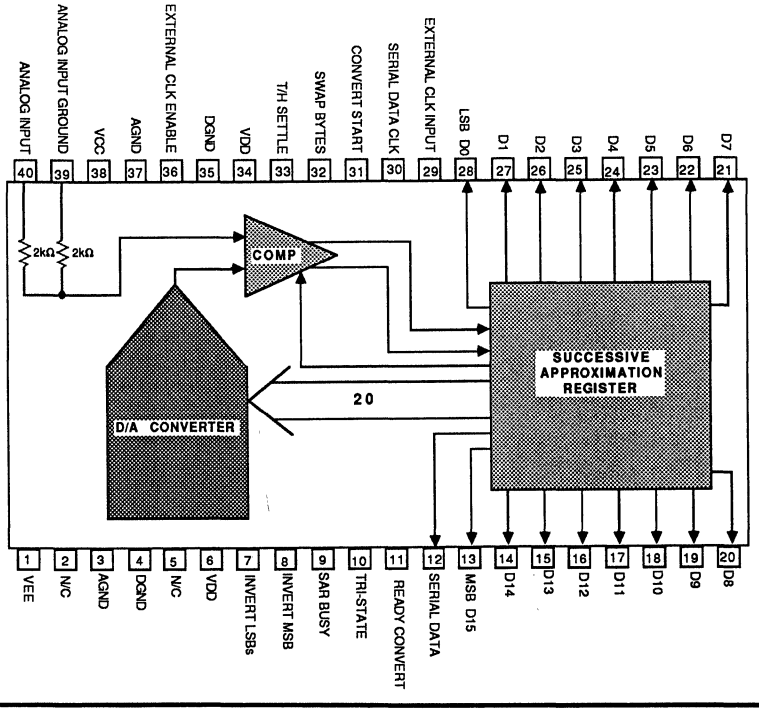
GENERAL DESCRIPTION

The HADC78160 is a 16-bit, hybrid successive approximation A/D converter containing µP compatible control pins. It is capable of digitizing up to a ±5Volt analog signal at an 3µS conversion rate.

The device contains a 16-bit DAC, comparator, and a successive approximation register that can output 16-bit parallel, serial or 2-byte configuration. The part has an internal clock but can be externally clocked if necessary. The input voltage is pin programmable at either ±2.5V or ±5V full scale input ranges. The HADC78160 is fully µP compatible with all the necessary control pins for various applications. These include a ready to convert control, SAR busy flag, external clock enable, convert start, serial data clock, tri-state control for a high impedance output state, NRZ serial output data option, LSBs and MSB invert, and swap bytes output format. The outputs are TTL compatible. On-board power supply bypass capacitors add additional noise immunity and a smaller overall decrete parts count.

The part is packaged in a 40 Lead ,600 MIL Ceramic DIP and operates on ±15V and +5V power supplies.

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

@ 25°C case temperature and nominal supplies.

ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
ANALOG-TO-DIGITAL CONVERTER										
Conversion Time				3						µS
Linearity				±1/2						LSB
Differential Linearity				±1						LSB
Gain Error				±.1						%
Gain Temperature Coefficient				±20						PPM/°C
Offset				±3						mV
Offset Temperature Coefficient				±10						µV/°C
Analog Input				±2.5/±5						V
Input Impedance				2						KΩ
POWER REQUIREMENTS										
Supply Current (Analog)	V_{CC} = +15V			5						mA
	V_{EE} = -15V			40						
Supply Current (Digital)	V_{DD} = +5V			45						mA

TEST LEVELS: I- Production tested at the specified conditions; II Sample tested to ensure compliance.

**For Ordering Information See Section 1.

HDAC10180A/B

8-BIT, HIGH SPEED D/A CONVERTERS

FEATURES

- **275 MWPS Conversion Rate - A Version**
- **165 MWPS Conversion Rate - B Version**
- **Compatible with TDC1018 with Improved Performance**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Registered Data And Video Controls
- Differential Current Outputs

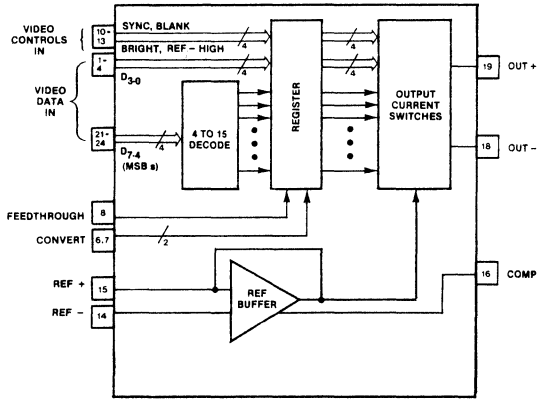
APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC10180 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10180 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE, and O IRE set-up is available as a mask programmed option. The HDAC10180 is pin-compatible with the TDC1018, with improved performance, and two can be used with the HDAC10181. The HDAC10180 contains data and control input registers, video control logic, reference buffer, and current switches in 24 Lead CERDIP, or ceramic sidebrazed DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) . . . . . −7.0 to 0.5V
V_{EEA} (measured to V_{CCA}) . . . . . −7.0 to 0.5V
V_{CCA} (measured to V_{CCD}) . . . . . −0.5 to 0.5V

Input Voltages

CONV, Data, and Controls V_{EED} to 0.5V . . . . . (measured to V_{CCD})

REF + (measured to V_{CCA}) . . . . . V_{EEA} to 0.5V
REF − (measured to V_{CCA}) . . . . . V_{EEA} to 0.5V

Temperature

Operating, Ambient . . . . . −60 to +140°C
Junction . . . . . +175°C
Lead, Soldering (10 seconds) . . . . . +300°C
Storage . . . . . −60 to +150°C

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF., I_{SET} = 1.105 mA							
E_{LI}	Integral Linearity Error	1.0mA < I_{SET} < 1.3mA	I	−0.2 −½		+0.2 +½	% Full Scale LSB
E_{LD}	Differential Linearity Error	1.0mA < I_{SET} < 1.3mA	I	−0.2 −½		+0.2 +½	% Full Scale LSB
E_G	Gain Error		III	−5		+5	% Full Scale
TC_G	Gain Error Tempco		V		250		PPM/°C
V_{BG}	Bandgap Voltage	(measured to V_{CCA})	V		−1.2		V
I_{REF}	Reference Output Current		I	−50			μA
C_{REF}	Input Capacitance, REF+, REF−		V		5		pF
V_{OCP}	Compliance Voltage, + Output		I	−1.5		+3	V
V_{OCN}	Compliance Voltage, − Output		I	−1.5		+3	V
R_{OUT}	Equivalent Output Resistance		I	20			K Ohm
C_{OUT}	Output Capacitance		V		12		pF
I_{OP}	Maximum Current, + Output		V			45	mA
I_{ON}	Maximum Current, − Output		V			45	mA
I_{OS}	Output Offset Current		I			½	LSB
V_{IH}	Input Voltage, Logic HIGH		I			−1.4	V
V_{IL}	Input Voltage, Logic LOW		I	−1.0			V
V_{ICM}	Convert Voltage, Common Mode Range		I	−0.5		−2.5	V
V_{IDF}	Convert Voltage, Differential		IV	0.4		1.2	V

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF., I_{SET} = 1.105 mA							
I_{IL}	Input Current, Logic LOW, Data and Controls					120	µA
I_{IH}	Input Current, Logic HIGH, Data and Controls				10	120	µA
I_{IC}	Input Current, Convert				2	60	µA
C_I	Input Capacitance, Data and Controls		V		3		pF
PSR	Power Supply Sensitivity (HDAC10180)		I	−120		+120	µA/V
PSR	Power Supply Sensitivity (HDAC10181)			−120		+120	µA/V
I_{EE}	Supply Current		I		175	200	mA
DYNAMIC CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF, TA = 25°C, I_{SET} = 1.105 mA							
F_S	Maximum Conversion Rate	B Grade A Grade	I I	165 275			MWPS
t_{RI}	Rise Time	10% to 90% G.S.	I			1.6	ns
t_{RI}	Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV			1.0	ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2%	IV			7	ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.8%	IV			5.5	ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% R_L = 25Ω	IV			4.5	ns
t_{DSC}	Clock to Ouptut Delay, Clocked Mode		I			4	ns
t_{DST}	Data to Output Delay, Transparent Mode		I			6	ns
t_{PWL}	Convert Pulse Width, LOW	B Grade A Grade	I I	3.0 1.8			ns
	Glitch Energy	Area = ½ VT	V		10		pV-s
t_{PWH}	Convert Pulse Width, HIGH	B Grade A Grade	I I	3.0 1.8			ns
BW_{REF}	Reference Bandwidth, −3dB		V		1		MHz

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF, TA = 25°C, I_{SET} = 1.105 mA							
t_S	Set-up Time, Data and Controls		I	1.3	1.8	2	ns
t_H	Hold Time, Data and Controls		I	0.5	0		ns
SR	Slew Rate	20% to 80% G.S.	I	400			V/μS
FT_C	Clock Feedthrough		I			−48	dB

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at $T_a = 25°C$, and sample tested at specified temperature.
III	QA sample tested per QA test plan TA100.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

APPLICATION INFORMATION

The HDAC10180 is a high speed video Digital-to-Analog converters capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The HDAC10180 is separated into different conversion rate categories as shown in Table 2.

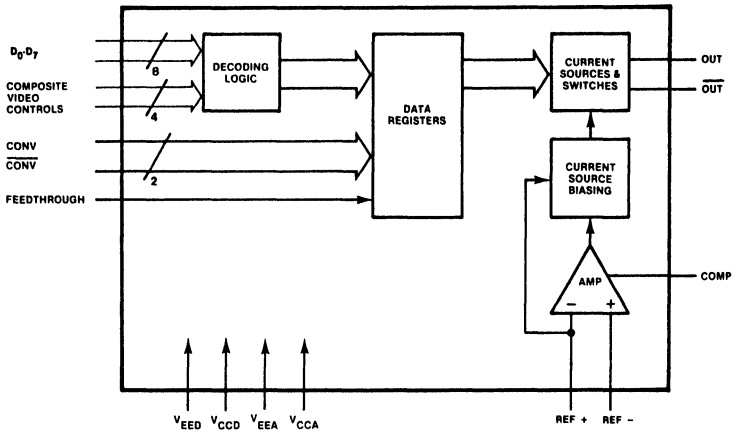
The HDAC10180 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10180 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10180 in a color raster application is shown in Figure 2. The HDAC10180 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10180 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10180. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10180 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10180 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

FIGURE 1 TIMING DIAGRAM

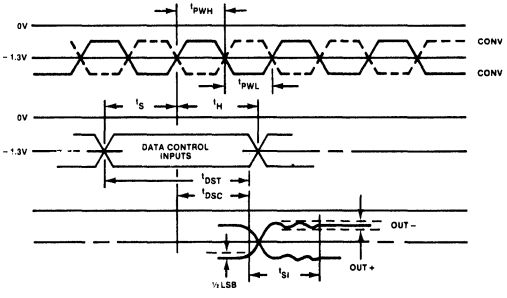
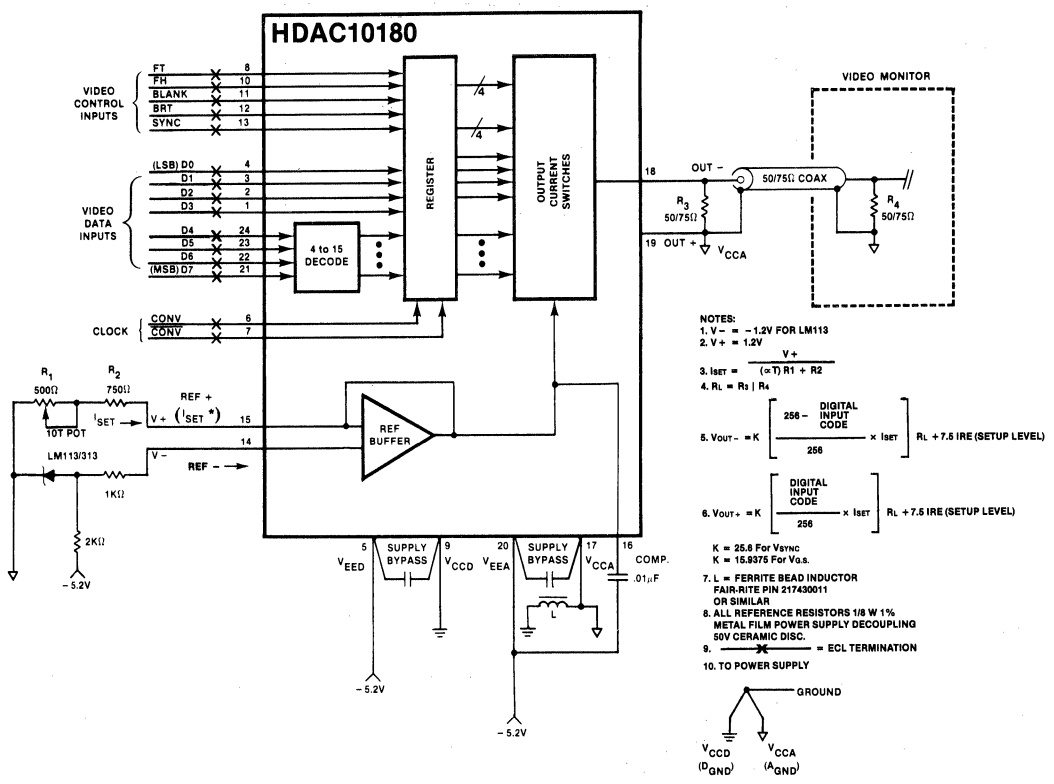


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC10180 operates from a single standard −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10180 inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10180 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10180 has two reference inputs: REF− and REF+. Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the REF+ input on the HDAC10180. A method and equations to set I_{SET} is shown in Figure 2. The HDAC10180 uses an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF− pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10180 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (Cc) should be connected between COMP and V_{EEA} as shown in Figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the Cc should be large (.01μF). The value of Cc determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of Cc can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10180 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10180 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10180. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10180 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and -1.07V. The OUT$-$ output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the -1.07V level. The OUT+ is inverted with SYNC up.

Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out – (mA)	Out – (V)	Out – (IRE)	Description
1	X	X	X	X	28.57	– 1.071	– 40	Sync Level
0	1	X	X	X	20.83	– 0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	– 0.073	100	Normal High Level
0	0	0	0	000...	19.40	– 0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	– 0.073	100	Normal High Level
0	0	0	1	000...	17.44	– 0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

Table 2 The HDAC10180 family and speed designations.

Part Number	Update	Comments
HDAC10180A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10180B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

Figure 3: CONVert, $\overline{\text{CONV}}$ert SWITCHING LEVELS

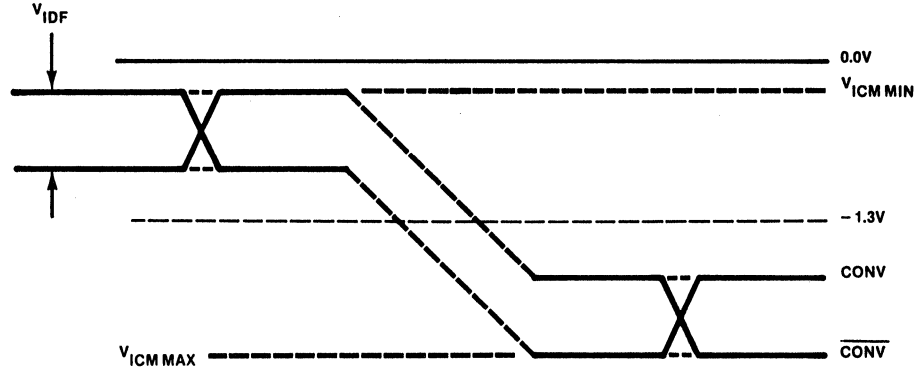


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

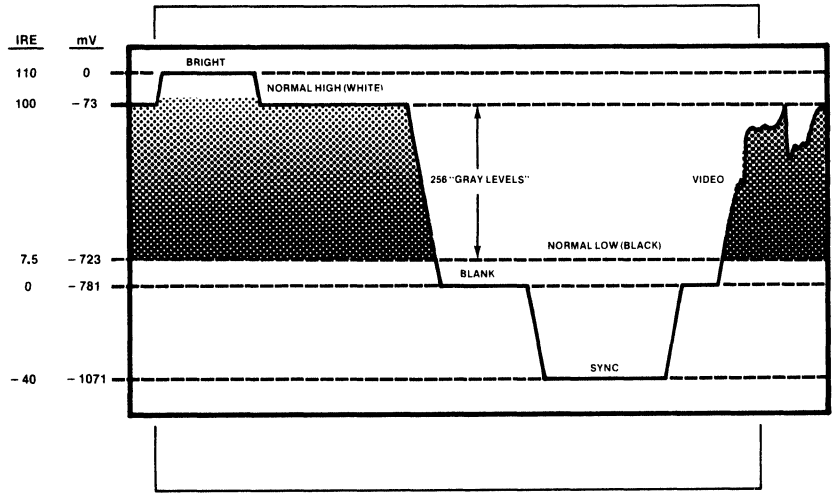


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

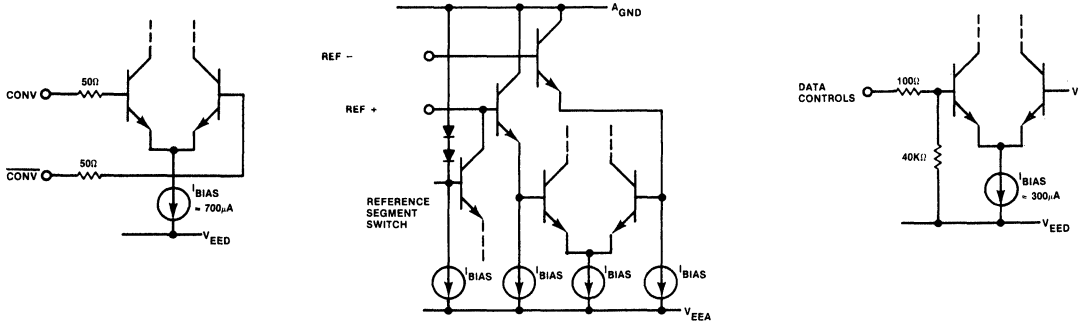


FIGURE6 DAC OUTPUT CIRCUIT

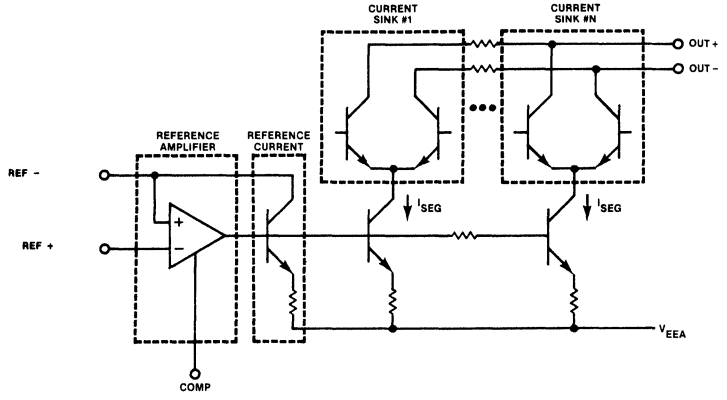


FIGURE 7A STANDARD LOAD

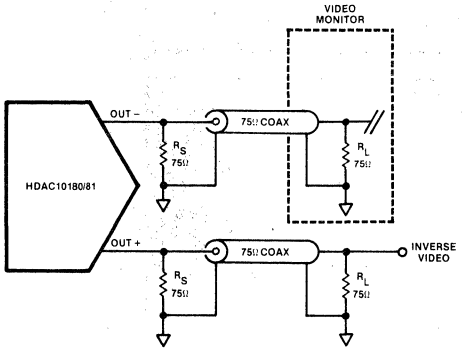
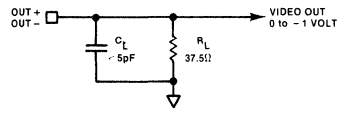


FIGURE 7B TEST LOAD



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50μA to an external load, such as another DAC reference input. (See HDAC10181 Data Sheet)

The circuits shown in Figure 8 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which like the 10180, does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 is the best choice for new designs.

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

FIGURE 8
TYPICAL RBG GRAPHICS SYSTEM

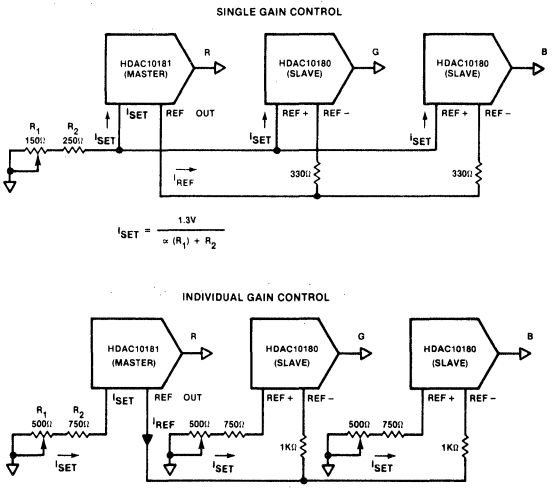
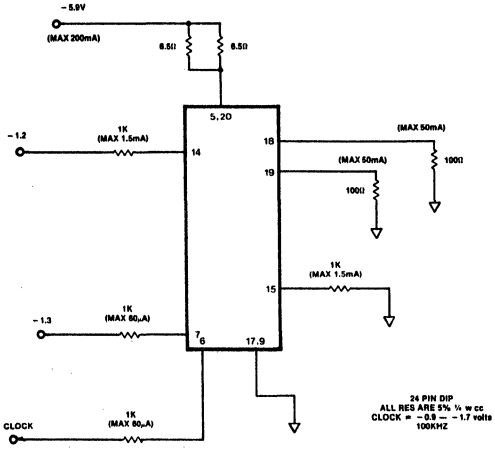
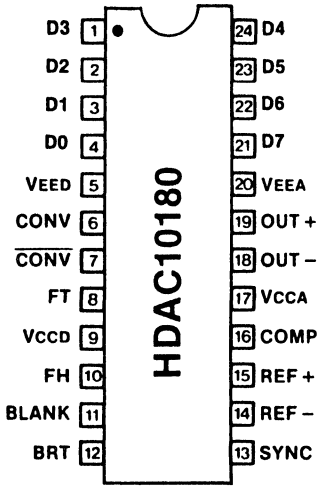


FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF –	Reference Current – Input
REF +	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT –	Output Current Negative
OUT +	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

***For Ordering Information See Section 1.*

NOTES:

HDAC10181A/B

8-BIT, HIGH SPEED D/A CONVERTERS

FEATURES

- **275 MWPS Conversion Rate - A Version**
- **165 MWPS Conversion Rate - B Version**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Stable On-chip Bandgap Reference
- Registered Data And Video Controls
- Differential Current Outputs

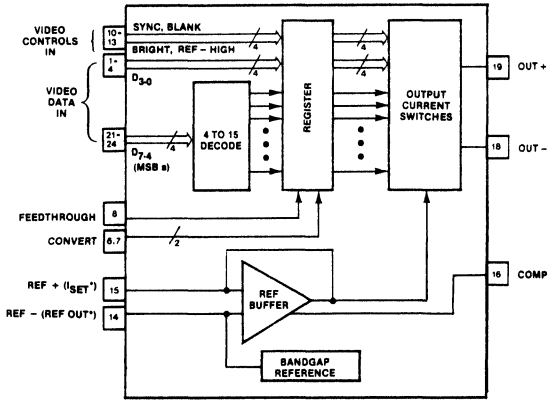
APPLICATIONS

- High Resolution Color or Monochrome Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC10181 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10181 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE, and O IRE set-up is available as a mask programmed option. The HDAC10181 includes an internal precision bandgap reference which can drive two HDAC10180s in an RGB graphics system. The HDAC10181 contains data and control input registers, video control logic, reference, and current switches in 24 Lead CERDIP, or ceramic sidebrazed DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) . . . . . −7.0 to 0.5V
V_{EEA} (measured to V_{CCA}) . . . . . −7.0 to 0.5V
V_{CCA} (measured to V_{CCD}) . . . . . −0.5 to 0.5V

Input Voltages

CONV, Data, and Controls V_{EED} to 0.5V . . . . . (measured to V_{CCD})

REF + (measured to V_{CCA}) . . . . . V_{EEA} to 0.5V
REF − (measured to V_{CCA}) . . . . . V_{EEA} to 0.5V

Temperature

Operating, Ambient . . . . . −60 to +140°C
Junction . . . . . +175°C
Lead, Soldering (10 seconds) . . . . . +300°C
Storage . . . . . −60 to +150°C

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF., I_{SET} = 1.105 mA							
E_{LI}	Integral Linearity Error	1.0mA < I_{SET} < 1.3mA	I	−0.2 −½		+0.2 +½	% Full Scale LSB
E_{LD}	Differential Linearity Error	1.0mA < I_{SET} < 1.3mA	I	−0.2 −½		+0.2 +½	% Full Scale LSB
E_G	Gain Error	T_A = 25°C OVER TEMP RANGE	III	−15 −19		+15 +19	% Full Scale
TC_G	Gain Error Tempco		V		250		PPM/°C
C_{REF}	Input Capacitance, REF +, REF −		V		5		pF
V_{OCP}	Compliance Voltage, + Output		I	−1.5		+3	V
V_{OCN}	Compliance Voltage, − Output		I	−1.5		+3	V
R_{OUT}	Equivalent Output Resistance		I	20			K Ohm
C_{OUT}	Output Capacitance		V		12		pF
I_{OP}	Maximum Current, + Output		V			45	mA
I_{ON}	Maximum Current, − Output		V			45	mA
I_{OS}	Output Offset Current		I			½	LSB
V_{IH}	Input Voltage, Logic HIGH		I			−1.4	V
V_{IL}	Input Voltage, Logic LOW		I	−1.0			V
V_{ICM}	Convert Voltage, Common Mode Range		I	−0.5		−2.5	V
V_{IDF}	Convert Voltage, Differential		IV	0.4		1.2	V
I_{IL}	Input Current, Logic LOW, Data and Controls					120	µA
I_{IH}	Input Current, Logic HIGH, Data and Controls				10	120	µA
I_{IC}	Input Current, Convert				2	60	µA

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = 25°C, C_C = 0pF., I_{SET} = 1.105 mA							
C_I	Input Capacitance, Data and Controls		V		3		pF
PSR	Power Supply Sensitivity		I	−120		+120	μA/V
I_{EE}	Supply Current		I		175	200	mA
DYNAMIC CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF, TA = 25°C, I_{SET} = 1.105 mA							
F_S	Maximum Conversion Rate	B Grade A Grade	I I	165 275			MWPS
t_{RI}	Rise Time	10% to 90% G.S.	I			1.6	ns
t_{RI}	Rise Time	10% to 90% G.S. R_L = 25 Ohms	IV			1.0	ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2%	IV			7	ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.8%	IV			5.5	ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% R_L = 25Ω	IV			4.5	ns
t_{DSC}	Clock to Ouptut Delay, Clocked Mode		I			4	ns
t_{DST}	Data to Output Delay, Transparent Mode		I			6	ns
t_{PWL}	Convert Pulse Width, LOW	B Grade A Grade	I I	3.0 1.8			ns
	Glitch Energy	Area = ½ VT	V		10		pV-s
t_{PWH}	Convert Pulse Width, HIGH	B Grade A Grade	I I	3.0 1.8			ns
BW_{REF}	Reference Bandwidth, −3dB		V		1		MHz
t_S	Set-up Time, Data and Controls		I	1.3	1.8	2	ns
t_H	Hold Time, Data and Controls		I	0.5	0		ns
SR	Slew Rate	20% to 80% G.S.	I	400			V/μS
FT_C	Clock Feedthrough		I			−48	dB

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at $T_a = 25°C$, and sample tested at specified temperature.
III	QA sample tested only at specified temperatures
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

APPLICATION INFORMATION

The HDAC10181 is a high speed video Digital-to-Analog converters capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates. In addition, the HDAC10181 includes an internal bandgap reference which may be used to drive other HDAC10180s if desired. (See HDAC10180 Data Sheet)

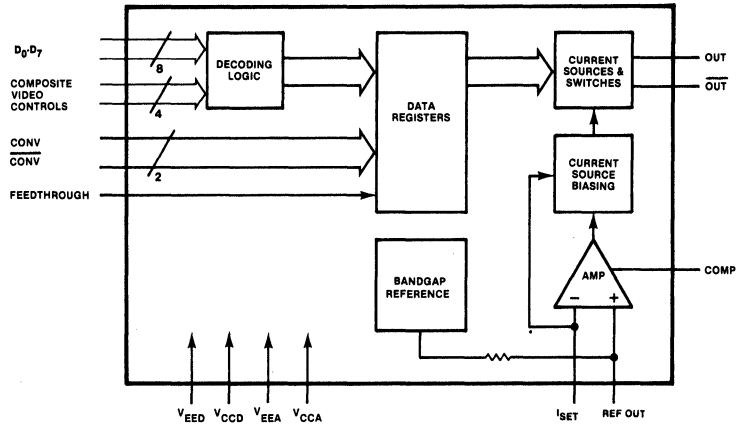
The HDAC10181 is separated into different conversion rate categories as shown in Table 2.

The HDAC10181 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10181 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10181 in a color raster application is shown in Figure 2. The HDAC10181 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10181 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10181. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10181 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10181 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

FIGURE 1 TIMING DIAGRAM

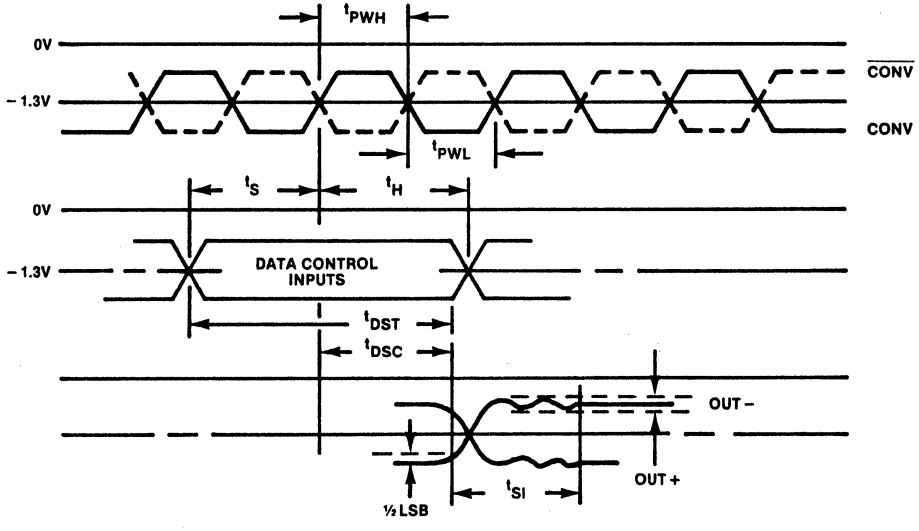
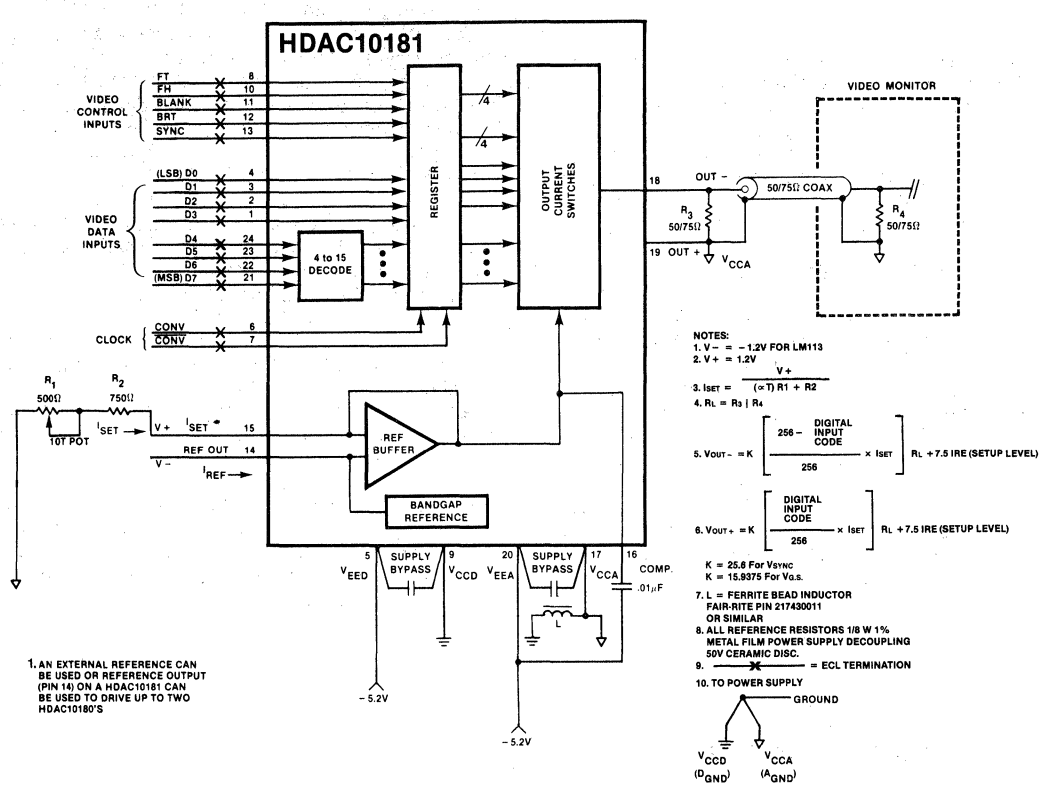


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC10181 operates from a single standard −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10181's inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10181 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10181 has one input (I_{SET}) and one reference output (REF OUT). Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The HDAC10181 has a bandgap reference connected internally to the inverting input of the buffer amplifier and the REF OUT.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{SET} input on the HDAC10181. A method and equations to set I_{SET} is shown in Figure 2. The HDAC10181 uses its own reference voltage for setting up I_{SET} as shown in Figure 2. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10181 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (Cc) should be connected between COMP and V_{EEA} as shown in Figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the Cc should be large (.01μF). The value of Cc determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of Cc can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10181 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10181 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10181. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10181 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and – 1.07V. The OUT – output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the – 1.07V level. The OUT + is inverted with SYNC up.

Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out – (mA)	Out – (V)	Out – (IRE)	Description
1	X	X	X	X	28.57	– 1.071	– 40	Sync Level
0	1	X	X	X	20.83	– 0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	– 0.073	100	Normal High Level
0	0	0	0	000...	19.40	– 0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	– 0.073	100	Normal High Level
0	0	0	1	000...	17.44	– 0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

Table 2 The HDAC10181 family and speed designations.

Part Number	Update	Comments
HDAC10181A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10181B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

FIGURE 3 CONVert, $\overline{\text{CONV}}$ert SWITCHING LEVELS

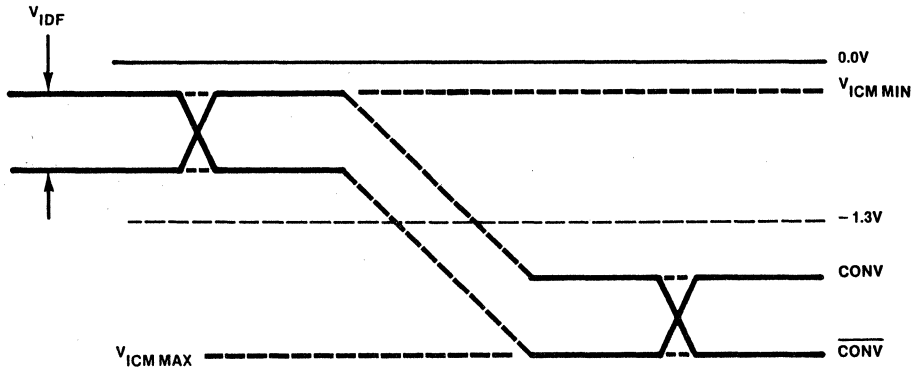


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

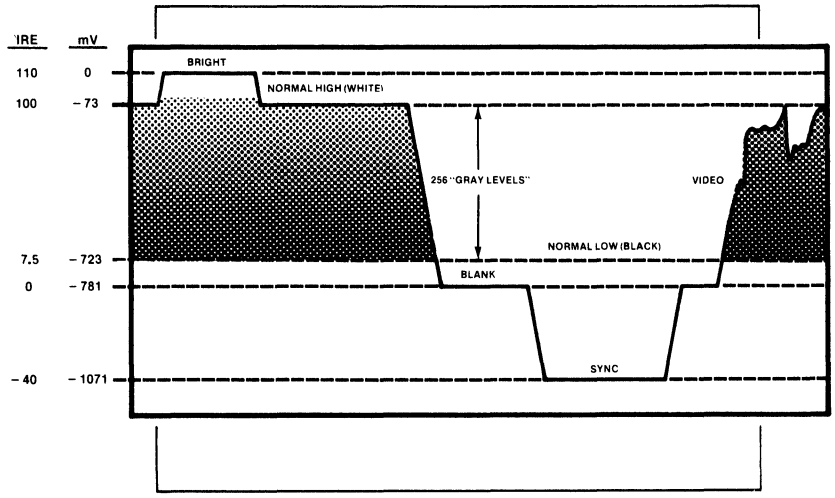


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

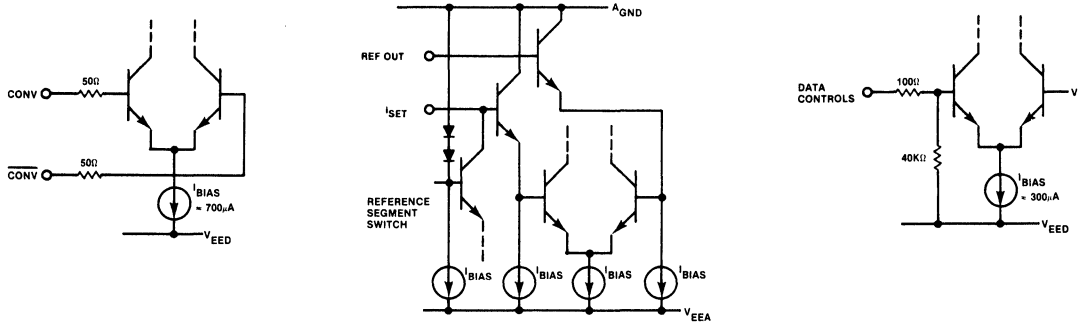


FIGURE6 DAC OUTPUT CIRCUIT

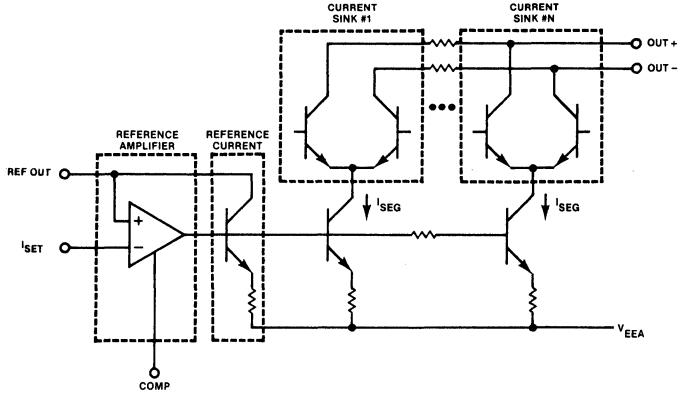


FIGURE 7A STANDARD LOAD

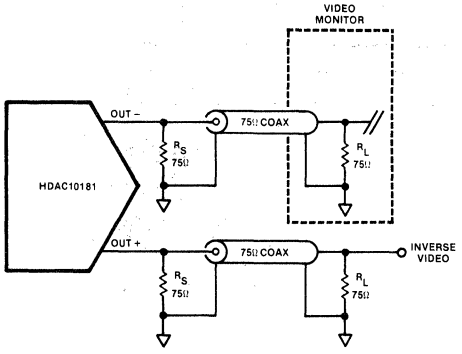
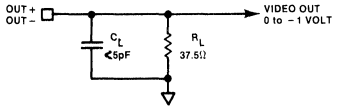


FIGURE 7B TEST LOAD



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50μA to an external load, such as another DAC reference input.

The circuits shown in Figure 8 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which like the 10180, does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 is the best choice for new designs. (See HDAC10180 Data Sheet)

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

FIGURE 8
TYPICAL RBG GRAPHICS SYSTEM

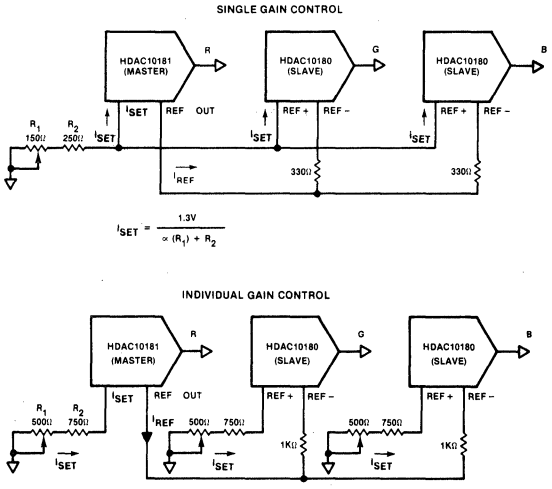
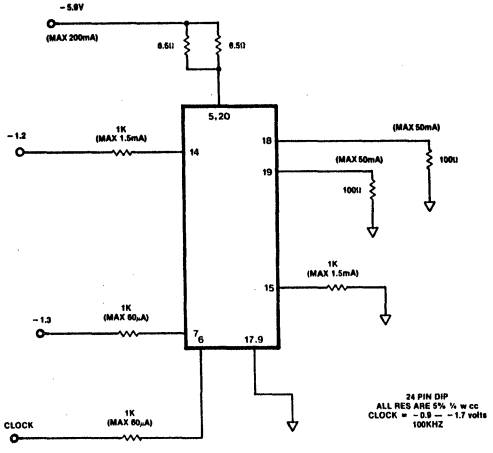
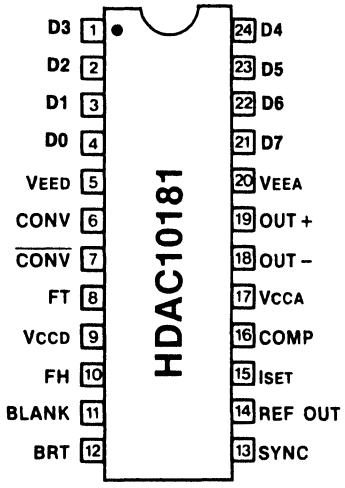


FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	0Analog Positive Supply
OUT –	Output Current Negative
OUT +	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

***For Ordering Information See Section 1.*

NOTES:

HDAC34010

TRIPLE 4-BIT, HIGH SPEED RASTER D/A CONVERTER

PRELIMINARY INFORMATION

FEATURES

- **200 MWPS Conversion Rate**
- **Complete RGB D/A Solution**
- RS-343-A Compatible
- Video Controls: Sync, Blank, Bright and Reference White
- Registered for Low Glitch
- Single Power Supply
- On-chip Bandgap Reference

APPLICATIONS

- RGB Color Graphics
- CAD/CAE
- Instrumentation Displays
- Medical Electronics: CAT, PET, NMR Displays
- Business Computer Graphics
- CRT Terminals

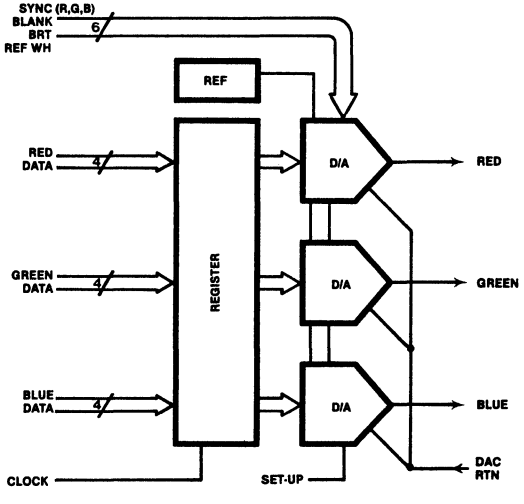
The HDAC34010 is a monolithic, triple 4-bit raster digital-to-analog (D/A) converter, complete with special video controls, on-chip reference, registers, and precision output termination. Only one device is required for a complete RGB D/A system.

Four special video controls (Sync, Blank, +10% Bright and Reference White) allow full reconstruction of RS-343-A compatible video signals from composite inputs. All data and control inputs are ECL compatible.

The HDAC34010 will directly drive a 75 Ohm coaxial cable and monitor termination to standard video levels.

The gain and output termination of each D/A is precisely adjusted using a proprietary trimming procedure. The HDAC34010 is fabricated using an advanced VLSI bipolar process for excellent performance, low power consumption, and high reliability in a choice of convenient packages.

BLOCK DIAGRAM



Absolute Maximum Ratings (Beyond which the useful life will be impaired)[1]

Supply Voltages
V_{EE} (measured to D_{GND}) . . . . . −7.0 to 0.5V
A_{GND} (measured to D_{GND}) . . . . . −0.5 to 0.5V

Input Voltages
Clock, Data and Controls (measured to D_{GND}) . . . . . V_{EE} to 0.5V

Outputs
Analog Output (R, G and B), applied voltage (measured to A_{GND}) . . . . . −3.0 to 3.0V
Analog Output (R, G and B), applied current[2] . . . . . 60 mA
Output Short Circuit Duration . . . . . Unlimited

Temperature
Operating, ambient . . . . . −60 to +140°C
junction . . . . . +175°C
Lead, soldering (10 seconds) . . . . . +300°C
Storage . . . . . −60 to +150°C

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE

D/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
STATIC CHARACTISTICS V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
V_{EE}	Supply Voltage (Measured to D_{GND})			−4.75	−5.2	−5.5	V
I_{EE}	Supply Current				−345	−385	mA
D_{GND}- A_{GND}	Ground Voltage Differential			−0.1	0.0	+0.1	V
C_I	Input Capacitance, Clock Data and Controls				3	5	pF
V_{OC}	Compliance Voltage	Note 2		−2		0.5	V
R_O	Output Resistance	Note 2		71	75	79	Ohms
C_O	Output Capacitance	Note 2			15	20	pF
I_O	Maximum Output Current	Note 2			28	30	mA
I_{IL}	Input Current, Logic LOW, Data and Controls				70	120	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls				90	150	μA

Notes:

1. Standard test load given in Figure 6.
2. Specification applies to each R, G and B DAC.

A/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTISTICS V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
F_S	Maximum Conversion Rate	Note 2		200	225		MWPS
t_D	Clock to Output Delay				4	5	ns
t_{ST}	Settling Time, ± ½ LSB	± ½ LSB[3]				4	ns
t_R	Rise Time	10% to 90% of Gray Scale[4]				2.5	ns
SR	Slew Rate			200			V/µs
t_{PWL}	Clock Pulse Width, LOW[1]			2.0			ns
t_{PWH}	Clock Pulse Width, HIGH[1]			2.0			ns
t_S	Setup Time, Data and Controls			2.0	1.5		ns
t_{HL}	Hold Time, Data and Controls			1.0	0.5		ns

Notes:

1. Standard test load given in Figure 6. Specification applies to each R, G and B DAC.
2. MWPS = MegaWords Per Second. Setting time from 50% point to ± ½LSB is 3.5ns Maximum.
3. ± ½ LSB = ± 3.2% of Gray Scale.
4. Gray Scale = |video white level - video black level | = 600mv (nominal).
5. The minimum specified conversion rate is given in the Dynamic Characteristics section. The sum of t_{PWL} and t_{PWH} must always equal or exceed the minimum conversion cycle time.

D/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
E_{LI}	Linearity Error Integral, Terminal Based	Note 2, 3			± 1.6	± 3.2	%G.S.
E_{LD}	Linearity Error, Differential	Note 2, 4			± 0.4	± 0.8	%G.S.
I_{OF}	Output Offset Current	DATA = SYNC = BLANK = 1 BRIGHT = 0				± 10	µA
E_G	Absolute Gain Error					± 1	G.S.
TC_G	Gain Error Tempco				± 0.01	± 0.02	%G.S./°C
PSRR	Power Supply Rejection Ratio	Supply to Output[5]		22	28		db
PSS	Power Supply Sensitivity	Supply to Output			5	10	mV/V

D/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
G_V	Peak Glitch Voltage	Note 6			2	5	mV
G_E	Peak Glitch Area ("Energy")	Note 7			4	10	pico-Volt-seconds
FT_C	Feedthrough, Clock	Data = Constant[8]			−50	−45	dB
FT_D	Feedthrough, Data	Clock = Constant[8]			−70	−65	dB
V_{IL}	Input Voltage, Logic LOW			−1.65			V
V_{IH}	Input Voltage, Logic HIGH					−0.95	V
T_A	Ambient Temperature[2]			0		70	°C
T_C	Case Temperature[2]			0		125	°C

Notes:

1. Standard test load given in Figure 6. Specification applies to each R, G, and B DAC.
2. %G.S. = Percent Gray Scale, where G.S. = |video white level -video black level| = 600mv (nominal).
3. ±3.2% G.S. = ± 1/2 LSB (Least Significant Bit).
4. ±0.8% G.S. = ± 1/8 LSB (Least Significant Bit).
5. 20kHz, 600mV p-p ripple superimposed on V_{EE} or Vcc; dB relative to full G.S. = 0dB.
6. Peak Glitch Voltage is the maximum voltage deviation from ideal voltage during the glitch period.
7. Glitch Area (voltage x time) is sometimes referred to as an "energy", although this is not dimensionally correct. The Peak Glitch Area is the maximum area deviation from the ideal output. Since glitches are typically "doublets" of symmetric positive and negative excursions, the average glitch area approaches zero.
8. dB relative to full G.S. = 0dB, 300MHz bandwidth limit.
9. 500 LFPM moving air required above T_A = 50°C; θ_{CA} = 30° C/W Typical at 500 LFPM.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at T_a = 25°C, and sample tested at specified temperature.
III	QA sample tested per QA test plan TA100.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

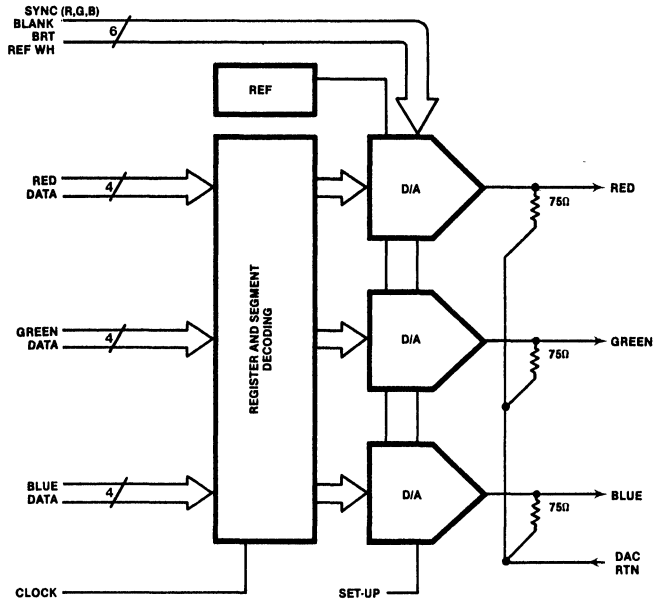
GENERAL INFORMATION

The HDAC34010 is especially suited for Red-Green-Blue (RGB) color raster applications. The HDAC34010 comprises three complete 4-bit digital-to-analog converters (DACs), precision bandgap reference, input data registers, decoding logic, video controls, and 75 Ohm source output termination as shown in the Functional Diagram. Each DAC has independent data and control inputs, with the exception of video Blank, Bright, and Reference White, which are common to all three converters. Parallel data input registers are provided for each DAC. A single Clock input synchronizes the video data entry and conversion cycle for all three converters. All data, clock, and control inputs of the HDAC34010 are compatible with standard Emitter-Coupled Logic (ECL).

The video control inputs (Sync, Blank, Bright and Reference White) are used for reconstruction of RS-343-A compatible signals from video control inputs. Video setup level (the difference between video black and video blank) may be programmed for 0, 10, or 20 IRE units, depending on the condition of the Setup Select control.

The HDAC34010 utilizes a partially segmented approach whereby the upper 2 MSBs (Most Significant Bits) are decoded into a parallel code which drive individual and identical current switches. The advantage of this approach is that currents are added sequentially as codes increase, thereby eliminating the switching in and out of currents (as with straight binary-weighted DACs). This technique reduces glitching and improves linearity and other performance character-

FUNCTIONAL DIAGRAM



APPLICATIONS CIRCUIT DISCRIPTION

A typical interface circuit using the HDAC34010 in an RGB color raster application is shown in Figure 1 A/B. Although the HDAC34010 requires few external components and is extremely easy to use, there are several considerations that should be noted to achieve best performance. The very high operating speeds of the HDAC34010 require good circuit layout, decoupling of supplies, and proper design of transmission lines.

Video input data and controls may be directly connected to the HDAC34010. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

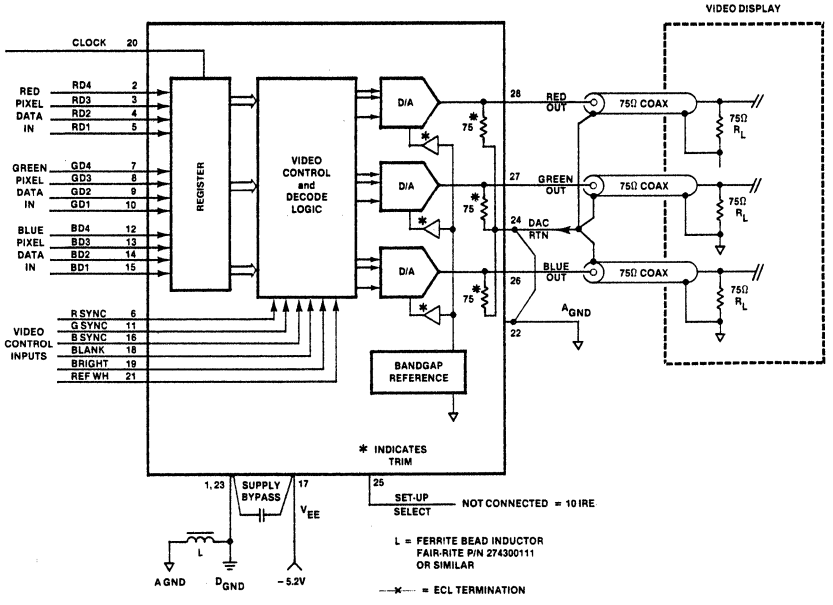
It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC34010 provides separate digital and analog ground connections to simplify grounding layout.

The R, G, and B analog outputs are designed to directly drive a 75 Ohm transmission system as shown. The source impedances of the HDAC34010's RGB outputs are factory-trimmed to 75 Ohms +/− 5%, thus eliminating the need for an external source-termination resistor. The RGB load impedance (R_L) must be 75 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse travelling waves in the analog transmission system. The return path for analog output current is DAC RTN, which is connected internally to the source-termination resistors, R_S.

No external reference is required for operation of the HDAC34010, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges.

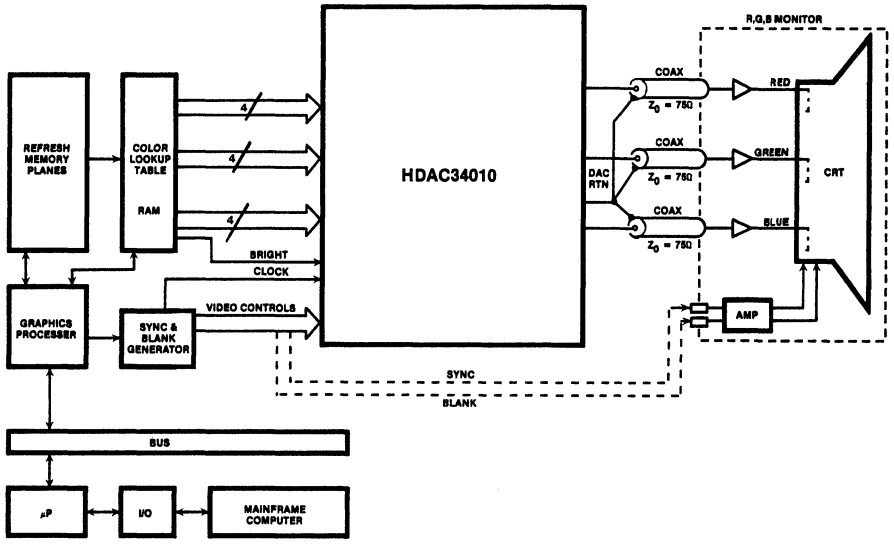
The HDAC34010 operates from a single standard −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC34010's inherent supply noise rejection characteristics. As shown, a large value Tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

FIGURE 1A HDAC34010 TYPICAL INTERFACE CIRCUIT



Honeywell

FIGURE 1B TYPICAL RGB GRAPHICS SYSTEM



The timing diagram for the HDAC34010 is shown in Figure 2. Data to all three DACs (Red, Green, and Blue) is simultaneously entered on the rising edge of the clock. Data must be valid for a setup time of t_S before, and for a hold time of t_H after the rising edge of the clock, in order to be correctly entered. The DAC outputs will change in accordance to the clocked input data after a delay time of t_D. The settling time is specified as the time from when the DAC output is no longer within ½ LSB of the previous value until it is within ½ LSB of the new value.

The video control inputs cause the DAC outputs to change directly, without regard to the clock input. All video controls (Sync, Blank, Bright and Reference White) are active-Low (negative true) logic. Figure 3 illustrates the operation of Sync and Blank inputs and the resulting video output signal. As shown, both Sync and Blank must be Low to achieve the proper video Sync level. The video control input hierarchy is given in Table 1, with typical output levels for a setup level of 10 IRE.

Setup level is the difference between video Blank and Black levels. The HDAC34010 supports setups of 0, 10, and 20 IRE, which are programmed by connecting the Setup select input to ground (0V), not connected, or to V_{EE} (−5.2V), respectively. For most applications the 10 IRE option is suitable.

The Reference White input forces the DAC outputs to an all "1"s level, which is video "white" in most systems. This is especially useful for clearing the display screen to white during system reset or power-up. The Bright input adds 10% of full-scale video to the present video level. The Bright feature is commonly used for highlighting cursors or creating overlays of video information. Sync, Blank and Reference White override the RGB data inputs, while Bright may be applied to any video level.

FIGURE 2 TIMING DIAGRAM

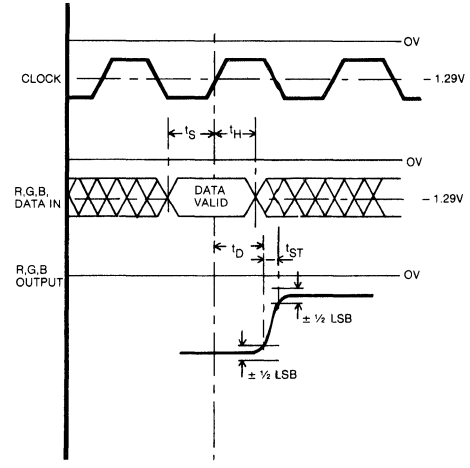


Table 1 Video Control Operation (Output values for Setup = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out (V)	Out (IRE)	Description
0	0	1	1	XXXX	−1.028	−40	Sync Level
1	0	1	1	XXXX	−0.742	0	Blank Level
1	1	0	1	XXXX	−0.071	84	Normal White Level
1	1	0	0	XXXX	0.0	94	Enhanced White Level
1	1	1	1	1111	−0.071	84	Normal White Level
1	1	1	0	1111	0.0	94	Enhanced White Level
1	1	1	1	0000	−0.671	10	Normal Black Level
1	1	1	0	0000	−0.600	20	Enhanced Black Level

Notes:

1. All Video Controls are active-Low (negative true) logic.
2. Sync and Blank output levels are dependent on setup level selected. Values indicated are for setup = 10 IRE (setup select left unconnected).
3. Sync level requires that both Sync and Blank = 0.
4. 140 IRE = 1.00 Volts.
5. All control values are subject to tolerance of ± 2% Gray Scale.

Setup Select

Setup Control Input	Setup Level
0 Volts (GND)	0 IRE
Not Connected	10 IRE
−5.2 Volts (V_{EE})	20 IRE

FIGURE 3 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD & 10 IRE SETUP

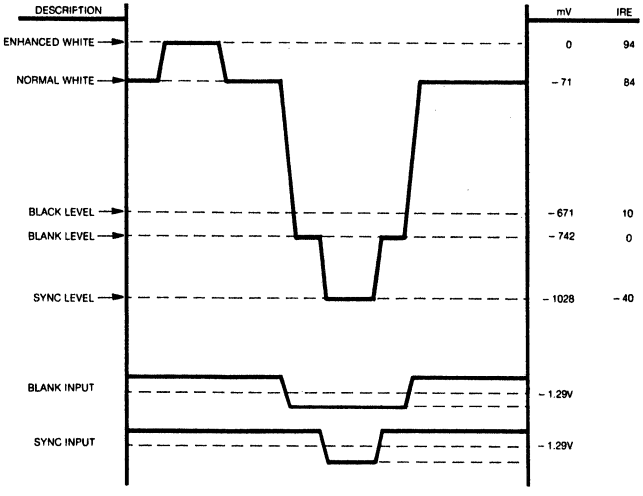


FIGURE 4 EQUIVALENT INPUT CIRCUIT, DATA, CLOCK & CONTROL

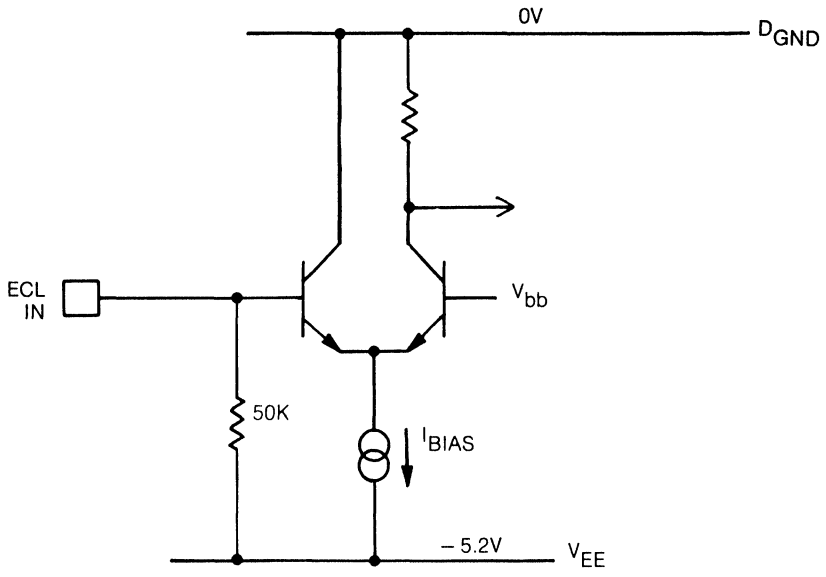


FIGURE 5 DAC OUTPUT CIRCUIT

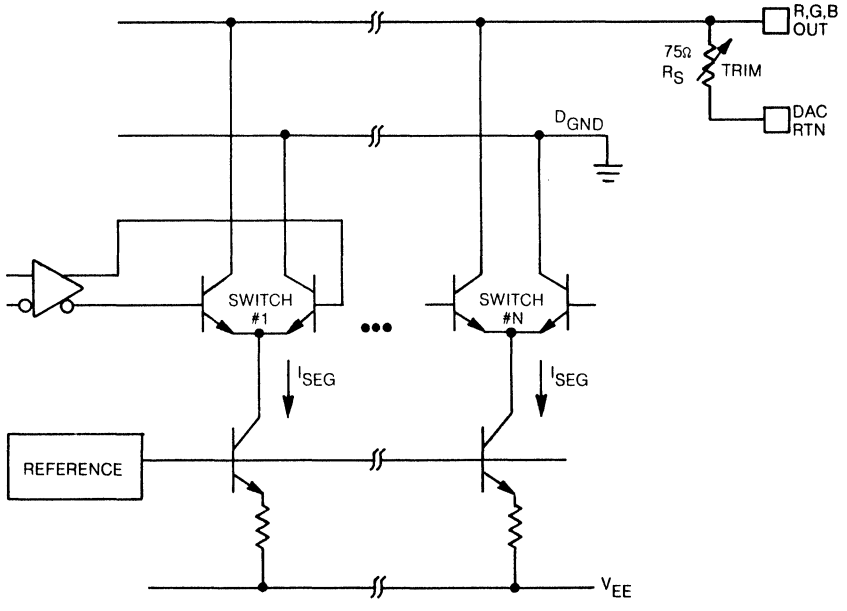


FIGURE 6A STANDARD LOAD

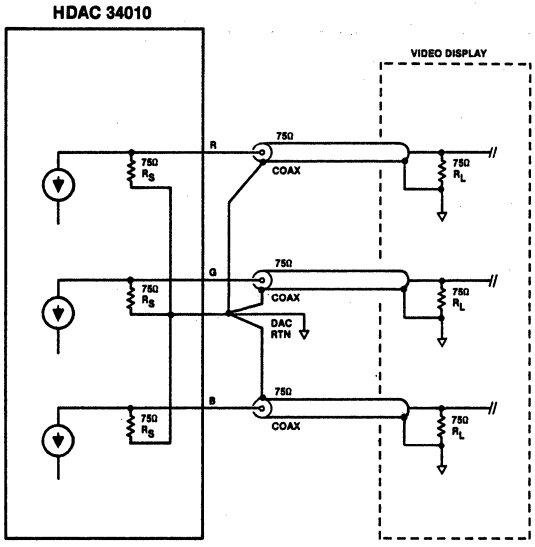
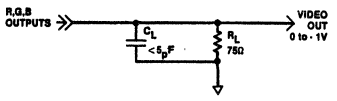
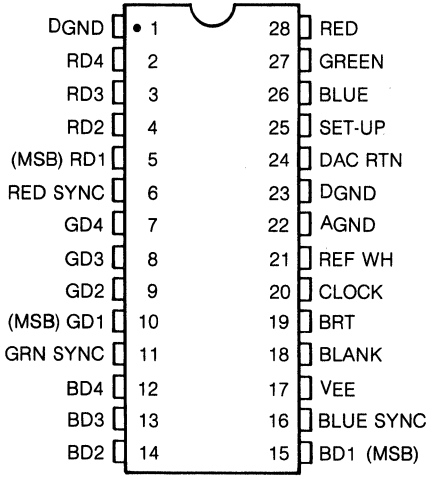


FIGURE 6B TEST LOAD



PIN ASSIGNMENTS



28 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
RD4	R Data Bit 4 (LSB)
RD3	R Data Bit 3
RD2	R Data Bit 2
RD1	R Data Bit 1 (MSB)
RED SYNC	Red Composite Sync Input
GD4	G Data Bit 4 (LSB)
GD3	G Data Bit 3
GD2	G Data Bit 2
GD1	G Data Bit 1 (MSB)
GRN SYNC	Green Composite Sync Input
BD4	B Data Bit 4 (LSB)
BD3	B Data Bit 3
BD2	B Data Bit 2
BD1	B Data Bit 1 (MSB)
BLUE SYNC	Blue Composite Sync Input
VEE	Negative Supply Voltage Input (−5.2V)
BLANK	Video Blank Input
BRT	+10% Bright Input
CLOCK	Conversion Clock Input
REF WH	Reference White Input
AGND	Analog Ground
DGND	Digital Ground
DAC RTN	DAC Return
SET-UP	Video Set-up Select
BLUE	Blue DAC Video Output
GREEN	Green DAC Video Output
RED	Red DAC Video Output

***For Ordering Information See Section 1.*

HDAC34020

TRIPLE 4-BIT, HIGH SPEED RASTER D/A CONVERTER

PRELIMINARY INFORMATION

FEATURES

- **100 MWPS Conversion Rate**
- **Complete RGB D/A Solution**
- RS-343-A Compatible
- Video Controls: Sync, Blank, Bright and Reference White
- Registered for Low Glitch
- Standard +5, −5.2V Supplies
- On-chip Bandgap Reference
- TTL Compatible
- Immune to Power-On Latchup

APPLICATIONS

- RGB Color Graphics
- CAD/CAE Workstations
- Instrumentation Displays
- Medical Electronics: CAT, PET, NMR Displays
- Business Computer Graphics
- CRT Terminals

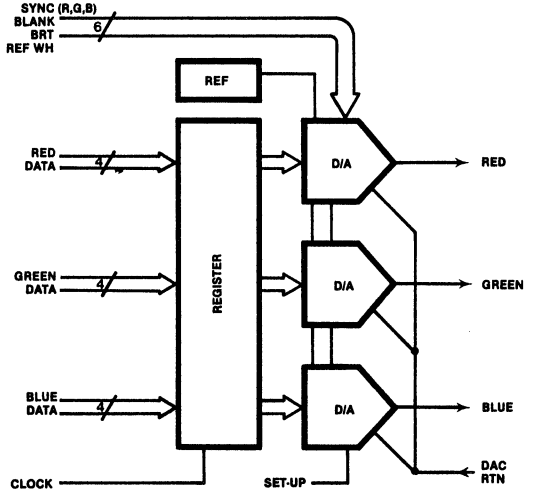
The HDAC34020 is a monolithic, triple 4-bit raster digital-to-analog (D/A) converter, complete with special video controls, on-chip reference, registers, and precision output termination. Only one device is required for a complete RGB D/A system.

Four special video controls (Sync, Blank, +10% Bright and Reference White) allow full reconstruction of RS-343-A compatible video signals from composite inputs. All data and control inputs are TTL compatible.

The HDAC34020 will directly drive a 75 Ohm coaxial cable and monitor termination to standard video levels.

The gain and output termination of each D/A is precisely adjusted using a proprietary trimming procedure. The HDAC34020 is fabricated using an advanced VLSI bipolar process for excellent performance, low power consumption, and high reliability in a choice of convenient packages.

BLOCK DIAGRAM



Absolute Maximum Ratings (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EE} (measured to D_{GND}) . . . . . −7.0 to 0.5V
V_{CC} (measured to D_{GND}) . . . . . +7.0 to −0.5V
A_{GND} (measured to D_{GND}) . . . . . −0.5 to 0.5V

Input Voltages

Clock, Data and Controls (measured to D_{GND}) . . . . . V_{CC} to −0.5V

Outputs

Analog Output (R, G and B), applied voltage (measured to A_{GND}) . . . . . −3.0 to 3.0V
Analog Output (R, G and B), applied current[2] . . . . . 60 mA
Output Short Circuit Duration . . . . . Unlimited

Temperature

Operating, ambient . . . . . −60 to +140°C
junction . . . . . +175°C
Lead, soldering (10 seconds) . . . . . +300°C
Storage . . . . . −60 to +150°C

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE

D/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
STATIC CHARACTISTICS V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
V_{EE}	Negative Supply Voltage (Measured to D_{GND})			−4.75	−5.2	−5.5	V
V_{CC}	Positive Supply Voltage (Measured to D_{GND})			4.75	5.0	5.25	V
I_{EE}	Negative Supply Current				−345	−385	mA
I_{CC}	Positive Supply Current				26	40	mA
D_{GND}- A_{GND}	Ground Voltage Differential			−0.1	0.0	+0.1	V
C_I	Input Capacitance, Clock Data and Controls				3	5	pF
V_{OC}	Compliance Voltage	Note 2		−2		0.5	V
R_O	Output Resistance	Note 2		71	75	79	Ohms
C_O	Output Capacitance	Note 2			15	20	pF
I_O	Maximum Output Current	Note 2		28	30		mA
I_{IL}	Input Current, Logic LOW, Data and Controls			−1.30	−0.5		mA
I_{IH}	Input Current, Logic HIGH, Data and Controls				0	100	μA

Notes:

1. Test load given in Figure 6B
2. Specification applies to each R, G and B DAC.

A/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTISTICS V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
F_S	Maximum Conversion Rate	Note 2		100	125		MWPS
t_D	Clock to Output Delay				4	5	ns
t_{ST}	Settling Time	± ½ LSB to ± ½ LSB[3]			3	4	ns
t_R	Rise Time	10% to 90% of Gray Scale[4]				2.5	ns
SR	Slew Rate			200			V/µs
t_{PWL}	Clock Pulse Width, LOW[1]			4			ns
t_{PWH}	Clock Pulse Width, HIGH[1]			4			ns
t_S	Setup Time, Data and Controls			3	2		ns
t_{HL}	Hold Time, Data and Controls			2	1		ns

Notes:

1. Test load given in Figure 6B. Specification applies to each R, G and B DAC.
2. MWPS = MegaWords Per Second. Setting time from 50% point to ± ½LSB is 3.5ns Maximum.
3. ± ½ LSB = ±3.2% of Gray Scale.
4. Gray Scale = |video white level - video black level | = 600mv (nominal).
5. The minimum specified conversion rate is given in the Dynamic Characteristics section. The sum of t_{PWL} and t_{PWH} must always equal or exceed the minimum conversion cycle time.

D/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
E_{LI}	Linearity Error Integral, Terminal Based	Note 2, 3			±1.6	±3.2	%G.S.
E_{LD}	Linearity Error, Differential	Note 2, 4			±0.4	±0.8	%G.S.
I_{OF}	Output Offset Current	DATA = SYNC = BLANK = 1 REF WH = BRT = 0				±10	µA
E_G	Absolute Gain Error					±1	G.S.
TC_G	Gain Error Tempco				±0.01	±0.02	%G.S./°C
PSRR	Power Supply Rejection Ratio	Supply to Output[5]		22	28		db
PSS	Power Supply Sensitivity	Supply to Output			5	10	mV/V

COMMERCIAL TEMPERATURE RANGE

D/C PARAMETER		TEST CONDITIONS[1]	TEST LEVEL	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE V_{EE} = 5.2V, f_{CLOCK} = 200 MHz, Test Load Figure 6 unless otherwise specified							
G_V	Peak Glitch Voltage	Note 6			2	5	mV
G_E	Peak Glitch Area ("Energy")	Note 7			4	10	pico-Volt-seconds
FT_C	Feedthrough, Clock	Data = Constant[8]			−50	−45	dB
FT_D	Feedthrough, Data	Clock = Constant[8]			−70	−65	dB
V_{IL}	Input Voltage, Logic LOW			0.8			V
V_{IH}	Input Voltage, Logic HIGH					2.4	V
T_A	Ambient Temperature[2]			0		70	°C
T_C	Case Temperature[2]			0		125	°C

Notes:

1. Standard test load given in Figure 6. Specification applies to each R, G, and B DAC.
2. %G.S. = Percent Gray Scale, where G.S. = |video white level -video black level| = 600mv (nominal).
3. ±3.2% G.S. = ± 1/2 LSB (Least Significant Bit).
4. ±0.8% G.S. = ± 1/8 LSB (Least Significant Bit).
5. 20kHz, 600mV p-p ripple superimposed on V_{EE} or V_{CC}; dB relative to full G.S. = 0dB.
6. Peak Glitch Voltage is the maximum voltage deviation from ideal voltage during the glitch period.
7. Glitch Area (voltage x time) is sometimes referred to as an "energy", although this is not dimensionally correct. The Peak Glitch Area is the maximum area deviation from the ideal output. Since glitches are typically "doublets" of symmetric positive and negative excursions, the average glitch area approaches zero.
8. dB relative to full G.S. = 0dB, 300MHz bandwidth limit.
9. 500 LFPM moving air required above T_A = 50°C; θ_{CA} = 30° C/W Typical at 500 LFPM.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at T_a = 25°C, and sample tested at specified temperature.
III	QA sample tested only at specified temperatures
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

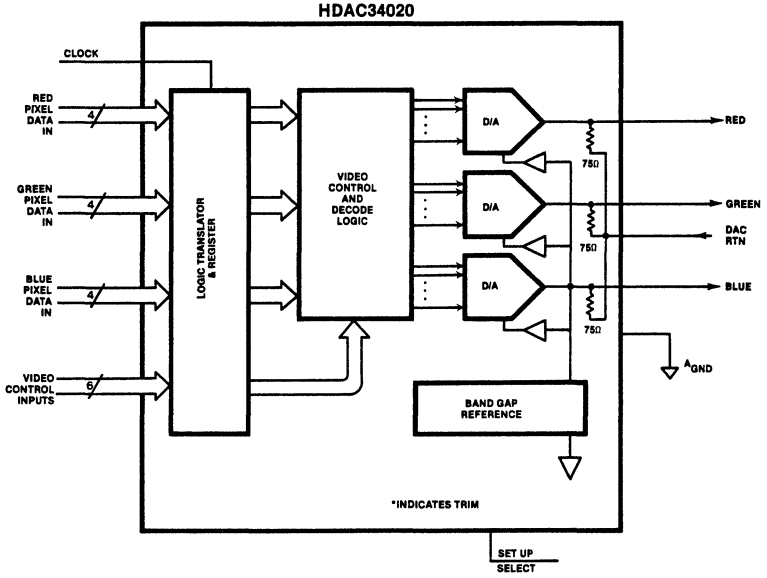
GENERAL INFORMATION

The HDAC34020 is especially suited for Red-Green-Blue (RGB) color raster applications. The HDAC34020 comprises three complete 4-bit digital-to-analog converters (DACs), precision bandgap reference, input data registers, decoding logic, video controls, and 75 Ohm source output termination as shown in the Functional Diagram. Each DAC has independent data and control inputs, with the exception of video Blank, Bright, and Reference White, which are common to all three converters. Parallel data input registers are provided for each DAC. A single Clock input synchronizes the video data entry and conversion cycle for all three converters. All data, clock, and control inputs of the HDAC34020 are compatible with standard Transistor -Transistor Logic (TTL).

The video control inputs (Sync, Blank, Bright and Reference White) are used for reconstruction of RS-343-A compatible signals from video control inputs. Video setup level (the difference between video black and video blank) may be programmed for 0, 10, or 20 IRE units, depending on the condition of the Setup Select control.

The HDAC34020 utilizes a partially segmented approach whereby the upper 2 MSBs (Most Significant Bits) are decoded into a parallel code which drive individual and identical current switches. The advantage of this approach is that currents are added sequentially as codes increase, thereby eliminating the switching in and out of currents (as with straight binary-weighted DACs). This technique reduces glitching and improves linearity and other performance characteristics.

FUNCTIONAL DIAGRAM



APPLICATIONS CIRCUIT DISCRIPTION

A typical interface circuit using the HDAC34020 in an RGB color raster application is shown in Figure 1 A/B. Although the HDAC34020 requires few external components and is extremely easy to use, there are several considerations that should be noted to achieve best performance. The very high operating speeds of the HDAC34020 require good circuit layout, decoupling of supplies, and proper design of transmission lines.

TTL video input data and controls may be directly connected to the HDAC34020. It is recommended that stripline or microstrip techniques be used for all TTL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC34020 provides separate digital and analog ground connections to simplify grounding layout.

The R, G, and B analog outputs are designed to directly drive a 75 Ohm transmission system as shown. The source impedances of the HDAC34020's RGB outputs are factory-trimmed to 75 Ohms ± 5%, thus eliminating the need for an external source-termination resistor. The RGB load impedance (R_L) must be 75 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse travelling waves in the analog transmission system. The return path for analog output current is DAC RTN, which is connected internally to the source-termination resistors, R_S.

No external reference is required for operation of the HDAC34020, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges.

The HDAC34020 operates from standard +5 and −5.2 Volt supplies. Proper bypassing of the supplies will augment the HDAC34020's inherent supply noise rejection characteristics. As shown, a large value Tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the Tantalum capacitor may be placed up to a few inches away.

FIGURE 1A HDAC34020 TYPICAL INTERFACE CIRCUIT

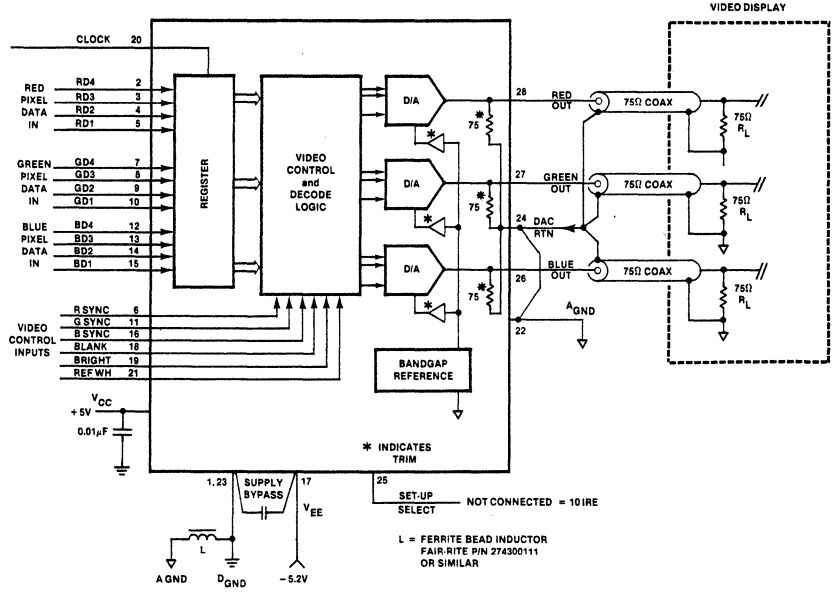
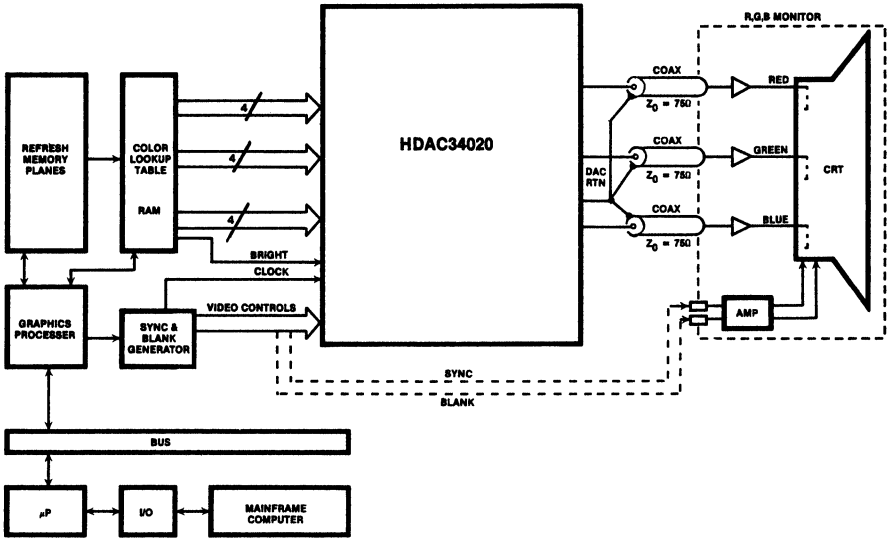


FIGURE 1B TYPICAL RGB GRAPHICS SYSTEM



The timing diagram for the HDAC34020 is shown in Figure 2. Data to all three DACs (Red, Green, and Blue) is simultaneously entered on the rising edge of the clock. Data must be valid for a setup time of t_S before, and for a hold time of t_H after the rising edge of the clock, in order to be correctly entered. The DAC outputs will change in accordance to the clocked input data after a delay time of t_D. The settling time is specified as the time from when the DAC output is no longer within ½ LSB of the previous value until it is within ½ LSB of the new value.

The video control inputs cause the DAC outputs to change directly, without regard to the clock input. All video controls (Sync, Blank, Bright and Reference White) are active-Low (negative true) logic. Figure 3 illustrates the operation of Sync and Blank inputs and the resulting video output signal. As shown, both Sync and Blank must be Low to achieve the proper video Sync level. The video control input hierarchy is given in Table 1, with typical output levels for a setup level of 10 IRE.

Setup level is the difference between video Blank and Black levels. The HDAC34020 supports setups of 0, 10, and 20 IRE, which are programmed by connecting the Setup select input to ground (0V), not connected, or to V_{EE} (– 5.2V), respectively. For most applications the 10 IRE option is suitable.

The Reference White input forces the DAC outputs to an all "1"s level, which is video "white" in most systems. This is especially useful for clearing the display screen to white during system reset or power-up. The Bright input adds 10% of full-scale video to the present video level. The Bright feature is commonly used for highlighting cursors or creating overlays of video information. Sync, Blank and Reference White override the RGB data inputs, while Bright may be applied to any video level.

FIGURE 2 TIMING DIAGRAM

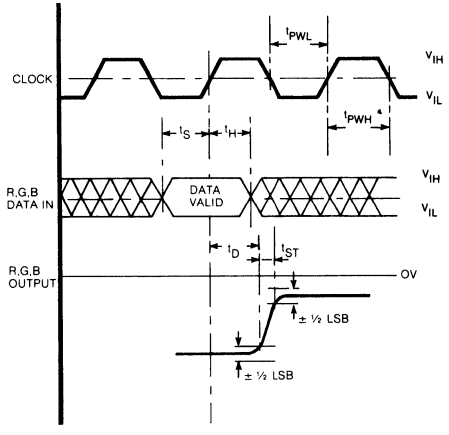


Table 1 Video Control Operation (Output values for Setup = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out (V)	Out (IRE)	Description
0	0	1	1	XXXX	−1.028	−40	Sync Level
1	0	1	1	XXXX	−0.742	0	Blank Level
1	1	0	1	XXXX	−0.071	84	Normal White Level
1	1	0	0	XXXX	0.0	94	Enhanced White Level
1	1	1	1	1111	−0.071	84	Normal White Level
1	1	1	0	1111	0.0	94	Enhanced White Level
1	1	1	1	0000	−0.671	10	Normal Black Level
1	1	1	0	0000	−0.600	20	Enhanced Black Level

Notes:

1. All Video Controls are active-Low (negative true) logic.
2. Sync and Blank output levels are dependent on setup level selected. Values indicated are for setup = 10 IRE (setup select left unconnected).
3. Sync level requires that both Sync and Blank = 0.
4. 140 IRE = 1.00 Volts.
5. All control values are subject to tolerance of ± 2% Gray Scale.

Setup Select

Setup Control Input	Setup Level
0 Volts (GND)	0 IRE
Not Connected	10 IRE
−5.2 Volts (V_{EE})	20 IRE

FIGURE 3 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD & 10 IRE SETUP

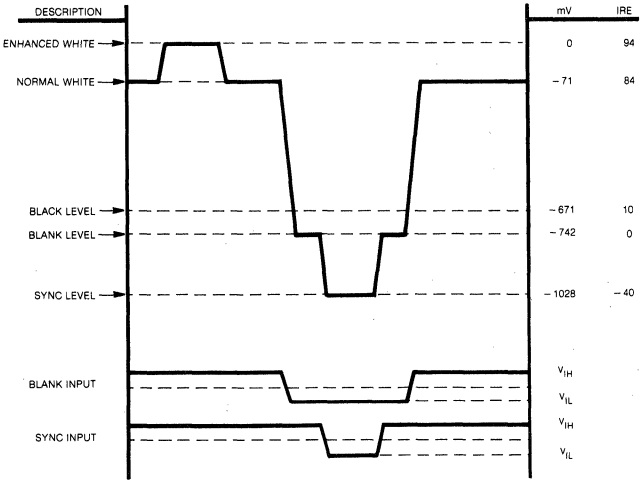


FIGURE 4 EQUIVALENT INPUT CIRCUIT, DATA, CLOCK & CONTROL

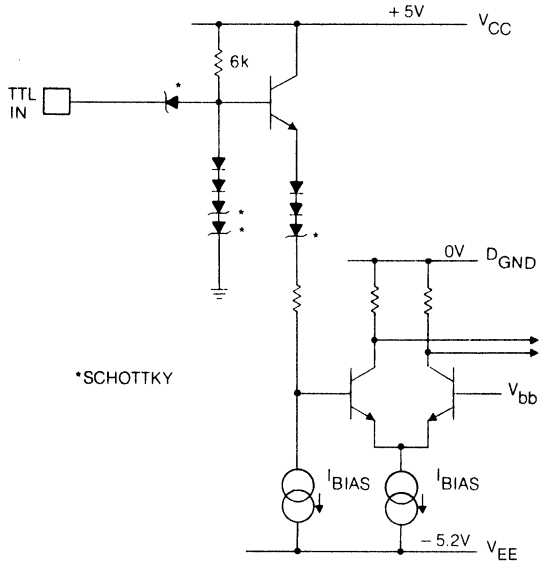


FIGURE 5 DAC OUTPUT CIRCUIT

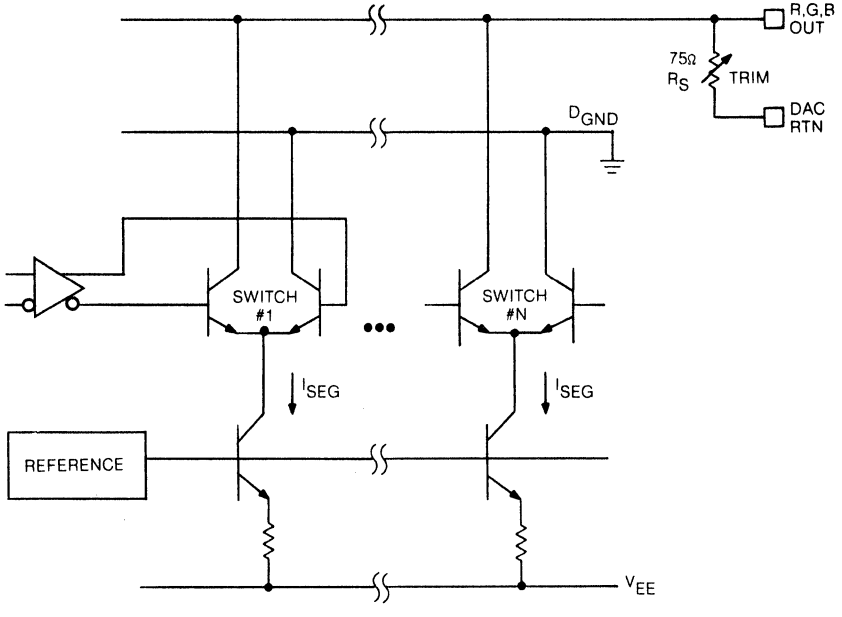


FIGURE 6A STANDARD LOAD

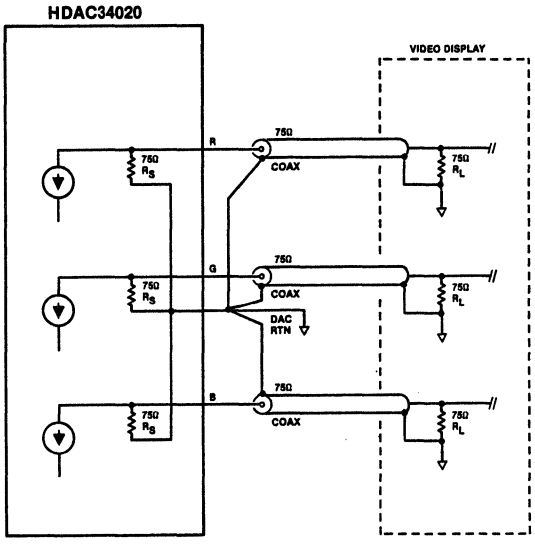
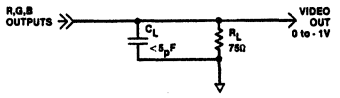
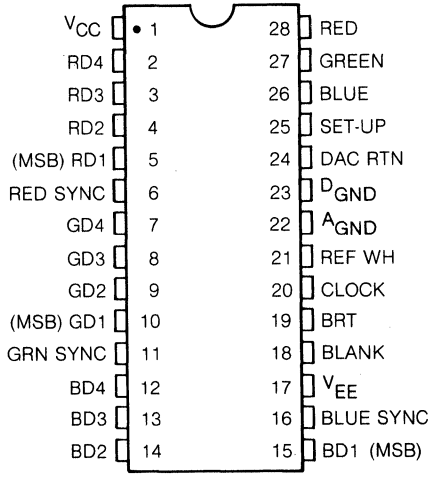


FIGURE 6B TEST LOAD



PIN ASSIGNMENTS



28 LEAD DIP

***For Ordering Information See Section 1.*

PIN FUNCTIONS

NAME	FUNCTION
VCC	Positive Supply Voltage Input (+5V)
RD4	R Data Bit 4 (LSB)
RD3	R Data Bit 3
RD2	R Data Bit 2
RD1	R Data Bit 1 (MSB)
RED SYNC	Red Composite Sync Input
GD4	G Data Bit 4 (LSB)
GD3	G Data Bit 3
GD2	G Data Bit 2
GD1	G Data Bit 1 (MSB)
GRN SYNC	Green Composite Sync Input
BD4	B Data Bit 4 (LSB)
BD3	B Data Bit 3
BD2	B Data Bit 2
BD1	B Data Bit 1 (MSB)
BLUE SYNC	Blue Composite Sync Input
VEE	Negative Supply Voltage Input (−5.2V)
BLANK	Video Blank Input
BRT	+10% Bright Input
CLOCK	Conversion Clock Input
REF WH	Reference White Input
AGND	Analog Ground
DGND	Digital Ground
DAC RTN	DAC Return
SET-UP	Video Set-up Select
BLUE	Blue DAC Video Output
GREEN	Green DAC Video Output
RED	Red DAC Video Output

HDAC50500

12-BIT MONOLITHIC MDAC WITH FULL μP INTERFACE

ADVANCE INFORMATION

FEATURES:

- Directly Interfaces to Intel and Motorola 8-Bit Microprocessors Without Additional Glue Logic
- Input Data Latches
- 12-Bit Linearity ± 1/2 LSB (End Point Over Temperature Range)
- 500ns Output Settling Time
- 4 Quadrant Multiplication
- Single Supply Operation

APPLICATIONS:

- Industrial Automation
- Process Control
- Bus Structured Instrumentation
- Microprocessor Controlled Gain/Function Circuits

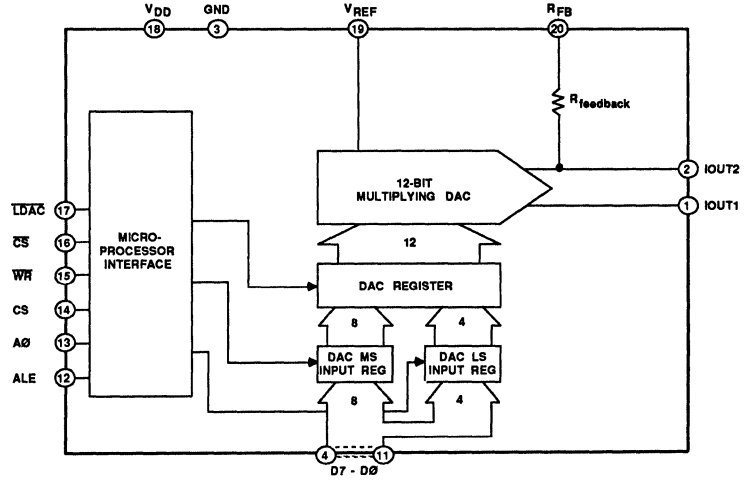
GENERAL DESCRIPTION

The HDAC50500 is a 12-bit multiplying digital-to-analog converter that will interface directly to most 8-bit microprocessors with no additional glue logic required. Both Motorola's MPX'ed and non-MPX'ed bus formats as well as Intel's MPX'ed bus format are supported.

Performance specifications of ±1/2 LSB maximum nonlinearity, ±1/2 LSB maximum gain error and 500ns typical output settling time (A/G grade) are the best in the industry! Additionally, timing specifications are the fastest currently available thus allowing more efficient usage of today's faster microprocessors.

This part is manufactured using Honeywell's Bipolar Enhanced CMOS (BEMOS) process. This process allows the combination of dense high speed digital logic with precision analog circuitry, all on a single monolithic chip.

BLOCK DIAGRAM



SPECIFICATIONS (V_{DD} = 5V, V_{REF} = 10V)

Over Temperature Range Specified Below, Unless Otherwise Indicated

Parameter	Test Conditions	Test Level (1)	HDAC50500A/G Min	Nom	Max	HDAC50500A Min	Nom	Max	HDAC50500B Min	Nom	Max	Units
Relative Accuracy		I	-1/2		+1/2	-1/2		+1/2	-1		+1	LSB
Differential Nonlinearity		I	-1/2		+1/2	-1/2		+1/2	-1		+1	LSB
Gain Error:	25°C	I	-1/2		+1/2	-2		+2	-3		+3	LSB
	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Output Settling Time	OUT1 Load = 100Ω + 13pF	II		0.5			0.5			0.5		µs
Output Capacitance on OUT1	Inputs Low	II			30			30			30	pF
	Inputs High	II			75			75			75	pF
t_{DS}: Data Set-up Time		I	60			60			60			ns
t_{DH}: Data Hold Time		I	10			10			10			ns
Address Hold Time		I	10			10			10			ns
Address Set-Up Time		I	20			20			20			ns

(1) Test Procedure: I - Production tested at the specified conditions; II - Sample tested to ensure compliance.

**For Ordering Information See Section 1.*

HDAC50600

14-BIT VOLTAGE-OUTPUT DIGITAL TO ANALOG CONVERTER

PRELIMINARY INFORMATION

FEATURES:

- Fast Voltage Settling Time of 750 nS (Typical) to 0.5 LSB
- On-Chip Reference Buffer
- Single Supply Operation
- On-Chip Application Resistors to Support Output Gain Selection
- Low Power Dissipation of 15 mW (Typical)
- 1/2 LSB Maximum Differential Nonlinearity Over Temperature
- High-Speed Microprocessor Compatible Interfacing

APPLICATIONS:

- µP Controlled Instruments
- Automatic Test Equipment
- Data Acquisition and Control Systems
- Frequency Synthesizers
- Battery Powered Systems
- High Speed A/D Converters

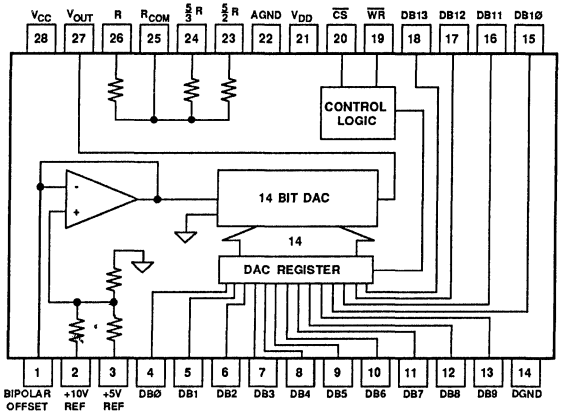
GENERAL DESCRIPTION

The HDAC50600 is a 14-bit voltage-output digital to analog converter. This high-performance monolithic device provides fast output voltage settling, single supply operation, and low power dissipation. Unique on-chip functions include an input reference buffer and precision application resistors used to support output voltage scaling. Unlike current-output devices, this voltage-output DAC simplifies the task of output buffering.

The device input accepts full 14-bit wide parallel data which makes the HDAC50600 ideal for 16-bit bus architectures. Data loading is controlled by standard $\overline{CS}$ and $\overline{WR}$ signals which simplify microprocessor interfacing. High-speed microprocessors, such as Intel's 80386 or Motorola's 68020, are supported by the 100 nS (minimum) write pulse width timing. All logic input levels are TTL and 5 volt CMOS compatible.

The HDAC50600 is manufactured on Honeywell's Bipolar Enhanced CMOS (BEMOS) process. This process is optimized to allow the combination of dense, high-speed digital logic with precision analog circuitry on a single chip.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond Which Damage May Occur) 25°C (1)

Supply Votages
Positive Supply Votage (VCC to AGND) +7
Positive Supply Voltage (VDD to DGND) +7
Ground Voltage Differential (AGND to DGND) -0.3 to 1V
VCC to VDD Differential -0.5 to +0.5V

Input Voltages
Digital Inputs to DGND -0.3 to VDD+0.3V
Pins 23-26 to DGND ± 25V
Pins 2,3 to AGND -0.3 to +25V

Output
VOUT to DGND -0.3 to VCC

Temperature
Temperature, ambient -60 to +140°C
junction +150°C
Lead Temperature (soldering 10 seconds) +300°C
Storage Temperature -65 to +150°C

(1) Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

All specifications Tmin to Tmax unless otherwise noted.
VDD = VCC = 5V; VREF = 10V; AGND = DGND = 0V unless otherwise noted.

DC Parameters	Test Conditions	Test Level (1)	HDAC50600A Min	HDAC50600A Typ	HDAC50600A Max	HDAC50600B Min	HDAC50600B Typ	HDAC50600B Max	Units
ACCURACY									
Resolution		I			14			14	Bits
Relative Accuracy		I			±1/2			±1	LSB
Differential Linearity Error		I			±1/2			±1	LSB
Offset Error		I			+3			+4	LSB
Gain Error		I			±4			±8	LSB
Offset Error Tempco		II			±2			±2	ppm/°C
Gain Error Tempco		II			±2.5			±5	ppm/°C
Power Supply Rejection (Δ Gain/Δ VCC)	VCC= 5V±5%	I			±1/2			±1/2	LSB
Application Resistor Value (R)		II	10	13	16	10	13	16	kΩ
Application Resistor Matching Error (5/3R, 5/2R to R)		I			±.05			±.05	%
REFERENCE INPUTS									
IIN (Input Current)	+10V REF or +5V REF Input	I			1			1	mA
CIN (Input Capacitance)	+10V REF or +5V REF Input	II			10			10	pF

(1) Test Procedure: I - Production tested at the specified conditions
II - Guaranteed by design and sampled characterization data.

ELECTRICAL SPECIFICATIONS

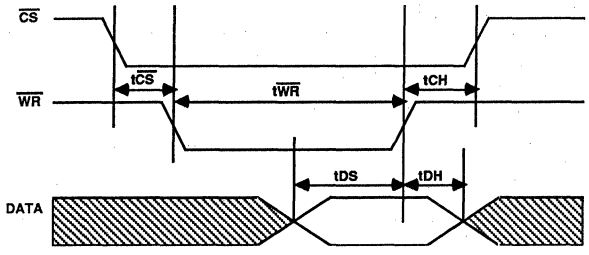
All specifications Tmin to Tmax unless otherwise noted.
VDD = VCC = 5V; VREF = 10V; AGND = DGND = 0V unless otherwise noted.

DC Parameters	Test Conditions	Test Level (1)	HDAC50600A Min	HDAC50600A Typ	HDAC50600A Max	HDAC50600B Min	HDAC50600B Typ	HDAC50600B Max	Units
LOGIC INPUTS (Pins DBO - DB13, $\overline{WR}$, $\overline{CS}$)									
VIH (High Input Voltage)		I	2.4			2.4			Volts
VIL (Low Input Voltage)		I			0.8			0.8	Volts
IIN Input Current)	VIN=0 or 5V	I			1			1	µA
CIN (Input Capacitance)	VIN=0 or 5V	II			10			10	pF
ANALOG OUTPUTS (Pins VOUT)									
ROUT (Output Resistance)	DBO-DB13 Are Zero	I	4.5	6.5	8.5	4.5	6.5	8.5	KΩ
Output Resistance Tempco		II		-300			-300		ppm/°C
COUT (Output Capacitance)		II		10	15		10	15	pF
Output Voltage Swings	$R_L \geq 1M\Omega$	I		3			3		Volts
POWER SUPPLY									
VDD, VCC Range		I	4.75		5.25	4.75		5.25	Volts
IDD	All Digital inputs VIL or VIH	I			2			2	mA
IDD	All Digital inputs 0 or 5V	I			100			100	µA
ICC		I		3	6		3	6	mA

AC Parameters	Test Conditions	Test Level (1)	HDAC50600A Min	HDAC50600A Typ	HDAC50600A Max	HDAC50600B Min	HDAC50600B Typ	HDAC50600B Max	Units
DYNAMIC PERFORMANCE									
Output Voltage Settling Time	Input Logic Levels 0 to 5V	II		0.75			0.75		µS
Digital to Analog Glitch Impulse		II		20			20		nV-Sec
Output Voltage Noise Density		II		20			20		nV/$\sqrt{Hz}$
TIMING CHARACTERISTICS									
t$\overline{CS}$ (Chip Select to Write Setup Time)		II	0			0			ns
tCH (Chip Select to Write Hold Time)		II	0			0			ns
t$\overline{WR}$ ($\overline{WR}$ Pulse Width)		II	100			100			ns
tDS (Data Setup Time)		II	80			80			ns
tDH (Data Hold Time)		II	10			10			ns

(1) Test Procedure: I - Production tested at the specified conditions
II - Guaranteed by design and sampled characterization data.

TIMING DIAGRAM



MODE SELECTION

Write Mode:

$\overline{CS}$ and $\overline{WR}$ low: DAC responds to data inputs DB0-DB13.

HOLD MODE:

Either $\overline{CS}$ or $\overline{WR}$ high: data inputs DB0-DB13 are locked out, DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumes high state.

TERMINOLOGY

Relative Accuracy

Relative accuracy, also known as endpoint nonlinearity, is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is expressed in % of full scale range or (sub)multiples of 1 LSB.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

Gain Error

Gain error, also known as full-scale error, is a measure of the deviation of the actual DAC full-scale output from the ideal full-scale output. For the HDAC50600, ideal full-scale output is (16383/16384)•3V + (Offset Error). Gain error and offset error are adjustable to zero using external trims as shown in Figure 5.

Output Voltage Settling Time

Time required for Vout to settle to within 1/2 LSB for a given digital stimulus, ie., zero to full-scale.

Digital to Analog Glitch Impulse

This is a measure of the amount of charge injected from the digital inputs to Vout when the input changes state. It is specified as the area of the glitch in nV-secs. The digital input is toggled between 01 1111 1111 1111 and 10 0000 0000 0000 with Vref at 3 Volts.

GENERAL CIRCUIT DESCRIPTION

Conversion Section

The HDAC50600 uses a modified R-2R resistor ladder network for digital-to-analog conversion. A functional diagram of this internal network is shown in Figure 2. To ensure a low Differential Linearity Error, the three most significant bits of the DAC use a segmented architecture, while the remaining eleven bits use the classical R-2R structure. Laser trimmed thin-film resistors assure high accuracy and stability over time and temperature.

Position of internal switches S0-S17 determine the DAC output voltage and are controlled by the DAC input code DB0-DB13. The internal Vref node is maintained at 3 Volts by the reference buffer which provides a DAC output range of 0 to 3 Volts.

Reference Buffer

The internal Vref node is driven by the on-chip Reference Buffer as illustrated in the block diagram. By using internal buffering, the DAC's settling time is minimized and less constraint is placed on the external reference. The on-chip reference buffer also simplifies the bipolar output option covered later in this section.

Reference Input Voltage Divider

The HDAC50600 can use either a 5 or 10 Volt reference using input pins +5V REF or +10V REF, respectively. The unused reference pin must be tied to AGND. The input reference voltage is divided down internally to provide an internal reference voltage of 3 Volts. Gain matching between the two references is ensured by thin film laser trimming.

Internal Application Resistors

The Vout pin provides an output signal ranging from 0 to 3 Volts with an output impedance of 6.5 kΩ typical. In many applications, output buffering and gain are desirable to increase the output voltage range. The HDAC50600 contains trimmed thin-film application resistors for use with an external op amp. These can be configured to provide output ranges of 0 to 10 Volts or -5 to +5 Volts.

Figure 3 shows how to connect the external op amp. As shown in the table of Figure 3, pin R is connected to analog ground to provide a 0 to 10 Volt unipolar output. In this configuration, the op amp is connected as a non-inverting amplifier with a gain of 10/3.

Pin R is connected to pin BIP OFF (bipolar offset) to provide a -5 to +5 Volt bipolar output range. BIP OFF is internally connected to the Reference Buffer output. The op amp in the bipolar output mode is configured so that:

$V_{BUFF-OUT} = (10/3)(Vout) - (5/3)(Vref)$

No attempt should be made to use the BIP OFF output as a reference source for other external devices. Additional loading of this pin may degrade device performance.

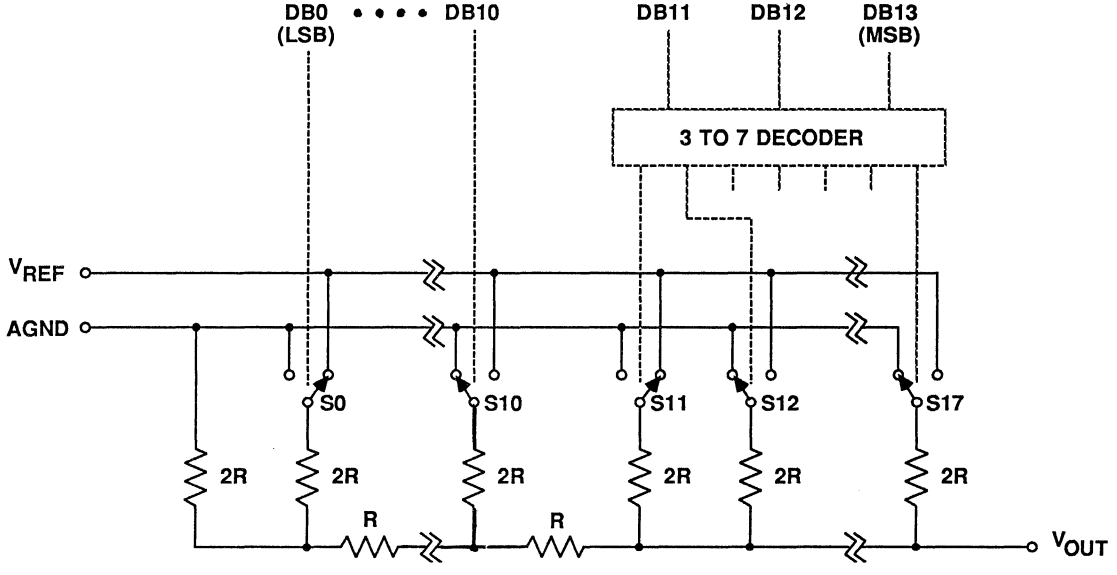
Unlike a current-output type DAC, the input offset voltage of the external op amp will not cause a non-linearity over the output range. Because of the constant output impedance of the HDAC50600, output offset will remain constant over the output range. Output offset adjustment therefore is only required in those applications requiring absolute accuracy.

Input Logic and Interfacing

Data is loaded into the HDAC50600 with a single 14-bit wide data word on pins DB0-DB13, where DB0 is the least significant bit (LSB). Pins $\overline{CS}$ and $\overline{WR}$ control the loading of the DAC input register. When both $\overline{CS}$ and $\overline{WR}$ are logic low, the input latches are transparent. If either $\overline{CS}$ or $\overline{WR}$ (or both) goes to logic high, the DAC data register is latched and Vout retains its present value. The timing relationship of $\overline{WR}$, $\overline{CS}$ and input data is shown in the the Write Timing Diagram of Figure 1. Pins $\overline{WR}$ and $\overline{CS}$ may be used interchangeably.

The input logic scheme of the HDAC50600 is designed for direct interface and control by a 16-bit microprocessor. Since the device is designed for write pulse widths as short as 100 ns, it is compatible with the latest high-speed general purpose microprocessors such as Motorola's 68000 or 68020 or Intel's 80286 or 80386. Typical microprocessor interfacing is shown in Figure 4.

Figure 2. Equivalent Resistor Network for the HDAC50600 DAC Circuitry



APPLICATION HINTS

External Operational Amplifier Selection

When application of the HDAC50600 requires an external op amp for output signal gain or buffering, selection of the op amp type can involve trade-offs between cost, accuracy, and speed. As an example, consider the circuit of Figure 3. In this application, the amplifier is configured for a non-inverting gain of 10/3 to provide a 10 Volt output swing. To contribute less than 1/4 LSB linearity error at Vbuff-out, the op amp's large-signal open loop voltage gain (Avol) must be 250 V/mV (108 dB) minimum. Input offset drift over temperature, which is also multiplied by 10/3, will also effect Vbuff-out accuracy. For the circuit of Figure 3, an error of less than 1/4 LSB over a 50°C temperature change will be maintained with an op amp having a ΔVos/°C of 3 μV/°C maximum; for a 100°C change, 1.5 μV/°C maximum is required.

The slew rate and bandwidth requirement will vary depending on application. Fast op amps, such as the OP17 at 60 V/μs slew rate and 30 MHz bandwidth, will provide a very fast settling time so that the output Vbuff-out in Figure 3 can approach the 750ns settling time of the HDAC50600. Input noise, like input offset, is multiplied by the non-inverting gain of the circuit (noise gain). Most modern high-accuracy op amps which provide suitable gain also have sufficiently low input noise. Proper op amp decoupling and good layout techniques are also essential to maintain low input noise.

Good op amp choices for high gain accuracy include the OP-43, OP-77, and the LT1001-LT1008. For high accuracy and high speed the OP-27 or the still faster OP-37 are good choices.

Offset and Full Scale Trim Adjustments

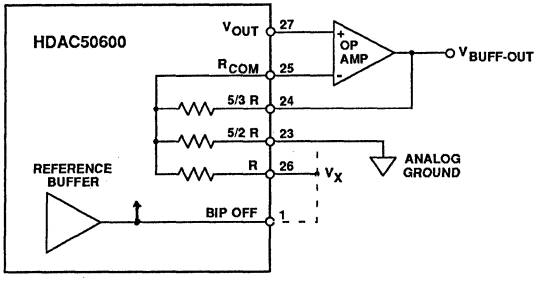
Although the application resistor ratios are matched to better than ±0.05%, this error combined with the DAC's offset and gain errors are important to consider when utilizing the circuit of Figure 3. With the addition of external trim resistors as shown in Figure 5, offset and gain errors can be eliminated. The values of Ra, Rb and Rc as shown will work for both the HDAC50600A and HDAC50600B grades.

Calibration for 0-10 Volt Unipolar Output Operation

When using the 0 - 10 Volt unipolar output circuit option of Figure 5, the Zero setting (offset) is accomplished by adjustment of potentiometer Ros. Ros performs internal nulling of the op amp. The value and connection of Ros should be as specified in the op amp manufacturer's data sheet to minimize temperature drift. Range of offset adjustment using this procedure will typically be ±5 mV. A thermally stable multi-turn potentiometer should be used for Ros.

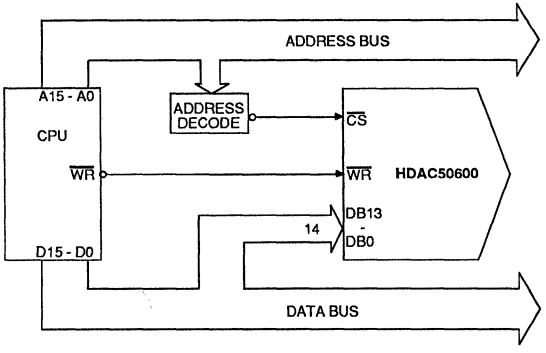
Full-scale adjustment is provided by external resistor Ra and potentiometer Rc. Ra and Rc add to the the total input and feedback resistance provided by the internal application resistors and allow a ±10 LSB adjustment range. Like Ros, Ra and Rc should have low temperature coefficients with the latter being a multi-turn potentiometer. Rb is not used and can be omitted for unipolar operation.

Figure 3. Connection Diagram of External Operational Amplifier Utilizing Internal Application Resistors



V_X CONNECTION	$V_{BUFF-OUT}$ RANGE
ANALOG GROUND PIN BIP OFF	0→+10V (UNIPOLAR) -5→+5V (BIPOLAR)

Figure 4. Typical Microprocessor Interface (Simplified)



The procedure for trim adjustment using the 0-10 Volt unipolar circuit option of Figure 5 is as follows:

1) Set zero value: With [00 0000 0000 0000] in the input register, adjust potentiometer Ros to obtain 0.0000 Volts at Vbuff-out.
(0.00061 V equals 1 LSB)

2) Set full scale value: With [11 1111 1111 1111] in the input register, adjust potentiometer Rc to obtain the correct Full-scale output minus 1 LSB which is 9.99939 Volts.
([Full-scale output] = [(16383/16384)•10V] + [Zero output])

Calibration for ±5 Volt Bipolar Output Operation

For the ±5 Volt bipolar output circuit option of Figure 5, Zero output occurs at - 5 Volts. By use of the application resistors connected as shown, the Zero output is derived by multiplying the 3 Volt reference at pin BIP OFF by -5/3. Zero output at Vbuff-out is adjusted by potentiometer Rb which changes the -5/3 gain. Potentiometer Ros is optional and should only be used with op amps that are not internally trimmed. When Ros is used, the op amp offset is adjusted first. As in the bipolar circuit option, potentiometer Rc is used to adjust full-scale value.

The procedure for trim adjustment using the ±5 Volt bipolar circuit option of Figure 5 is as follows:

1) Zero the input offset voltage to the op amp. Do this by writing [00 0000 0000 0000] into the input register and shorting the inverting and non-inverting op amp inputs to ground. Adjust Ros until Vbuff-out is as near to 0 Volts as possible. Delete this step if resistor Ros is not used.

(1) Set Zero value: With [00 0000 0000 0000] in the input register, adjust potentiometer Rb to obtain a -5.0000 Volt output at Vbuff-out. (0.00061 V equals 1 LSB)

2) Set full scale value: With [11 1111 1111 1111] in the input register, adjust potentiometer Rc to obtain the correct Full-scale output minus 1 LSB which is 4.99939 Volts. [Full-scale output] = [(16383/16384)•10V] + [Zero output])

Die Plot

136 X 172 mils

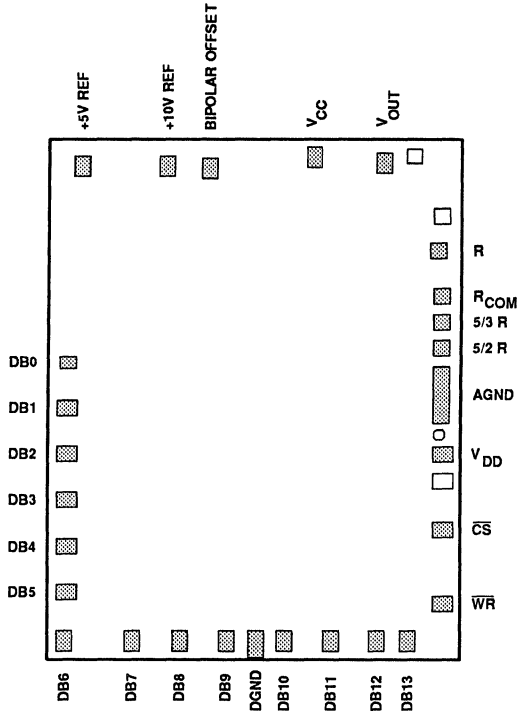
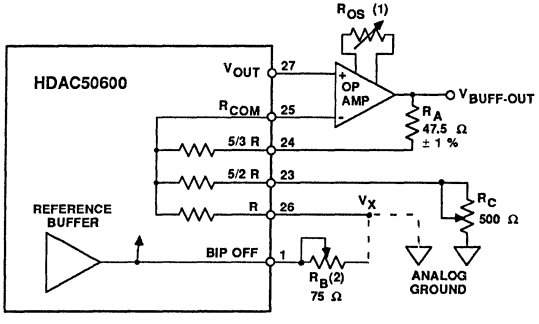


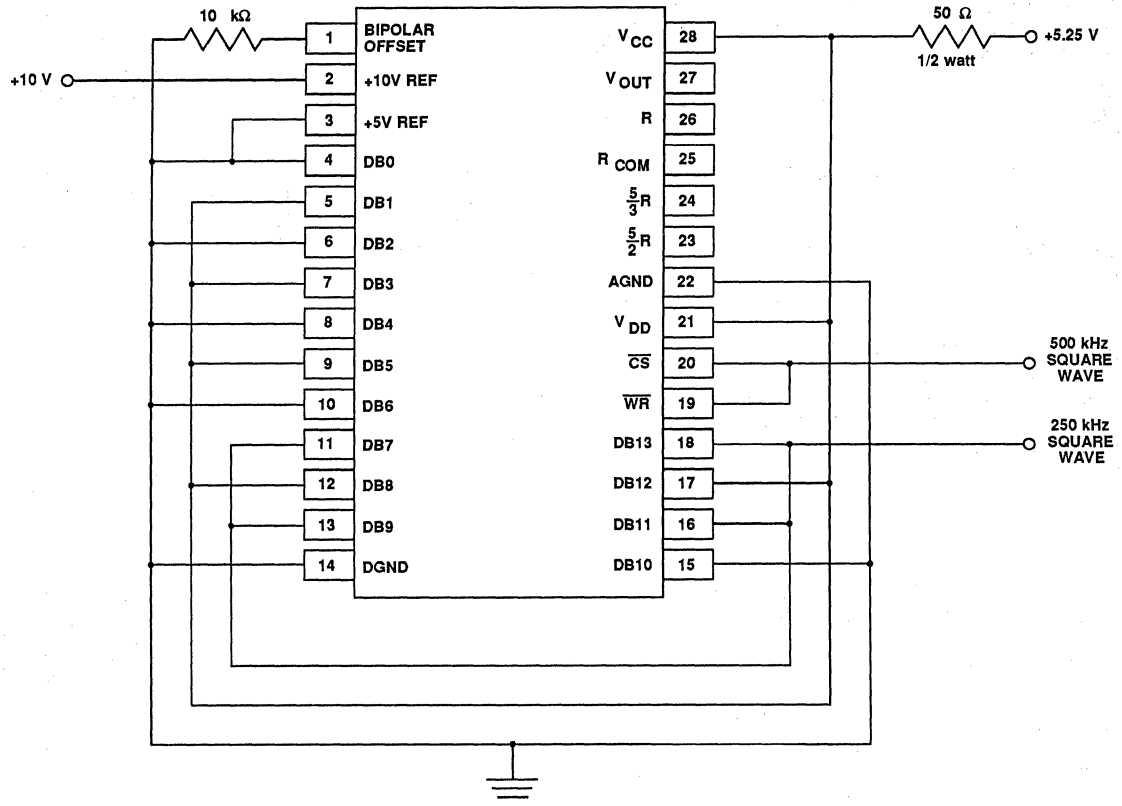
Figure 5. Modification of Figure 3 Showing Use of External Trim Resistors

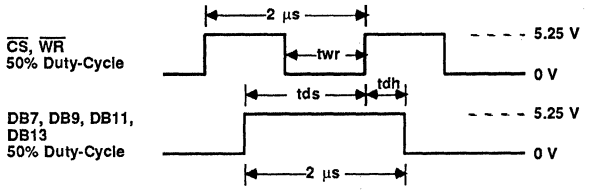


V_X CONNECTION	$V_{BUFF-OUT}$ RANGE
ANALOG GROUND R_B	0→+10V (UNIPOLAR) -5→+5V (BIPOLAR)

NOTES: (1) R_{OS} IS OPTIONAL IN BIPOLAR OPERATION.
(2) R_B IS NOT USED AND THEREFORE CAN BE ELLIMINATED IN UNIPOLAR O PERATION.

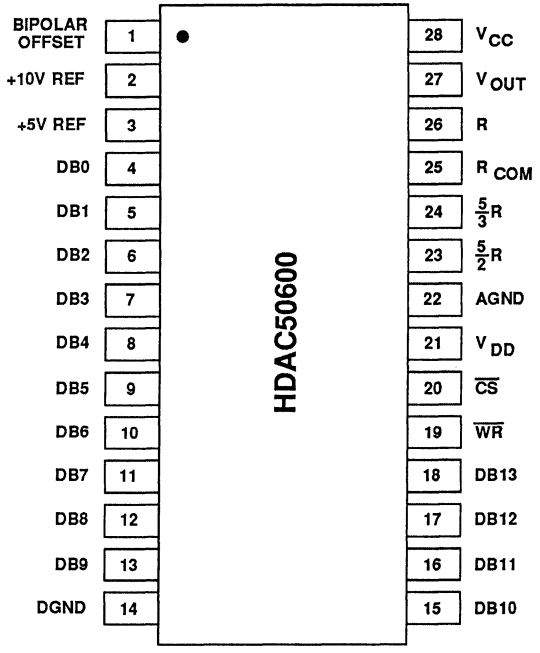
Burn-In Configuration





tds = 1.5 µs ± 200 ns
tdh = 0.5 µs ± 200 ns
twr = 1.0 us ± 200 ns

Pin Assignment



Pin Functions

PIN	PIN NAME	FUNCTION
1	BIPOLAR OFFSET	VREF OUTPUT FOR BIPOLAR OPERATIOI
2	+10V REF	INPUT FOR 10V REFERENCE VOLTAGE
3	+5V REF	INPUT FOR 5V REFERENCE VOLTAGE
4	DB0	INPUT DATA BIT 0 (LSB)
5	DB1	INPUT DATA BIT 1
6	DB2	INPUT DATA BIT 2
7	DB3	INPUT DATA BIT 3
8	DB4	INPUT DATA BIT 4
9	DB5	INPUT DATA BIT 5
10	DB6	INPUT DATA BIT 6
11	DB7	INPUT DATA BIT 7
12	DB8	INPUT DATA BIT 8
13	DB9	INPUT DATA BIT 9
14	DGND	DIGITAL GROUND
15	DB10	INPUT DATA BIT 10
16	DB11	INPUT DATA BIT 11
17	DB12	INPUT DATA BIT 12
18	DB13	INPUT DATA BIT 13 (MSB)
19	$\overline{WR}$	DATA WRITE
20	$\overline{CS}$	CHIP SELECT
21	V_{DD}	DIGITAL POSITIVE POWER SUPPLY
22	AGND	ANALOG GROUND
23	5/2 R	APPLICATION RESISTOR NETWORK
24	5/3 R	APPLICATION RESISTOR NETWORK
25	R_{COM}	APPLICATION RESISTOR NETWORK
26	R	APPLICATION RESISTOR NETWORK
27	V_{OUT}	ANALOG VOLTAGE OUTPUT
28	V_{CC}	ANALOG POSITIVE POWER SUPPLY

**For Ordering Information See Section 1.*

NOTES:

HDAC50800

14-BIT VOLTAGE-OUTPUT DIGITAL TO ANALOG CONVERTER

PRELIMINARY INFORMATION

FEATURES:

- Small 24 Pin, 0.3" Wide DIP Package
- Fast Voltage Settling Time of 750 nS (Typical) to 0.5 LSB
- On-Chip Reference Buffer
- Single Supply Operation
- On-Chip Application Resistors to Support Output Gain Selection
- Low Power Dissipation of 15 mW (Typical)
- 1/2 LSB Maximum Differential Nonlinearity Over Temperature
- Double Buffered Microprocessor Compatible Interfacing

APPLICATIONS:

- µP Controlled Instruments
- Automatic Test Equipment
- Data Acquisition and Control Systems
- Frequency Synthesizers
- Battery Powered Systems
- High Speed A/D Converters

3

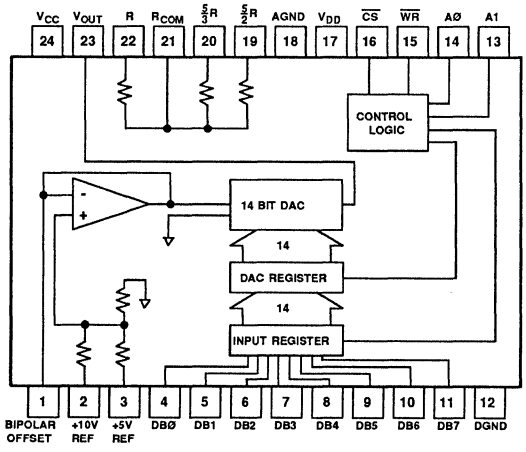
GENERAL DESCRIPTION

The HDAC50800 is a 14-bit voltage-output digital to analog converter. This high-performance monolithic device provides fast output voltage settling, single supply operation, and low power dissipation. Unique on-chip functions include an input reference buffer and precision application resistors used to support output voltage scaling. Unlike current-output devices, this voltage-output DAC simplifies the task of output buffering.

The device input accepts right-justified data in two bytes from an 8-bit data bus. DAC data loading is controlled by standard $\overline{CS}$ and $\overline{WR}$ signals. Address lines A0 and A1 control internal register loading and data transfer. The 100 nS (minimum) write pulse width ensures operation with a wide range of high-speed microprocessors. All logic input levels are TTL and 5 volt CMOS compatible.

The HDAC50800 is manufactured on Honeywell's Bipolar Enhanced CMOS (BEMOS) process. This process is optimized to allow the combination of dense, high-speed digital logic with precision analog circuitry on a single chip.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond Which Damage May Occur) 25°C (1)

Supply Votages
Positive Supply Votage (VCC to AGND) +7V
Positive Supply Voltage (VDD to DGND) +7V
Ground Voltage Differential (AGND to DGND) -0.3 to 1V
VCC to VDD Differential -0.5 to +0.5V

Input Voltages
Digital Inputs to DGND -0.3 to VDD+0.3V
Pins 19-22 to DGND ± 25V
Pins 2,3 to AGND -0.3 to +25V

Output
VOUT to DGND -0.3 to VCC

Temperature
Temperature, ambient -60 to +140°C
junction +150°C
Lead Temperature (soldering 10 seconds) +300°C
Storage Temperature -65 to +150°C

(1) Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

All specifications Tmin to Tmax unless otherwise noted.
VDD = VCC = 5V; VREF = 10V; AGND = DGND = 0V unless otherwise noted.

DC Parameters	Test Conditions	Test Level (1)	HDAC50800A Min	HDAC50800A Typ	HDAC50800A Max	HDAC50800B Min	HDAC50800B Typ	HDAC50800B Max	Units
ACCURACY									
Resolution		I			14			14	Bits
Relative Accuracy		I			±1/2			±1	LSB
Differential Linearity Error		I			±1/2			±1	LSB
Offset Error		I			+3			+4	LSB
Gain Error		I			±4			±8	LSB
Offset Error Tempco		II			±2			±2	ppm/°C
Gain Error Tempco		II			±2.5			±5	ppm/°C
Power Supply Rejection (Δ Gain/Δ VCC)	VCC= 5V±5%	I			±1/2			±1/2	LSB
Application Resistor Value (R)		II	10	13	16	10	13	16	kΩ
Application Resistor Matching Error (5/3R, 5/2R to R)		I			±.05			±.05	%
REFERENCE INPUTS									
IIN (Input Current)	+10V REF or +5V REF Input	I			1			1	mA
CIN (Input Capacitance)	+10V REF or +5V REF Input	II			10			10	pF

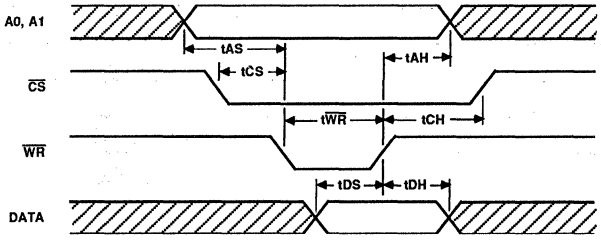
(1) Test Procedure: I - Production tested at the specified conditions
II - Guaranteed by design and sampled characterization data.

DC Parameters	Test Conditions	Test Level (1)	HDAC50800A Min	HDAC50800A Typ	HDAC50800A Max	HDAC50800B Min	HDAC50800B Typ	HDAC50800B Max	Units
LOGIC INPUTS (Pins DBO - DB7, $\overline{WR}$, $\overline{CS}$, A0, A1)									
VIH (High Input Voltage)		I	2.4			2.4			Volts
VIL (Low Input Voltage)		I			0.8			0.8	Volts
IIN Input Current)	VIN=0 or 5V	I			1			1	µA
CIN (Input Capacitance)	VIN=0 or 5V	II			10			10	pF
ANALOG OUTPUTS (Pin VOUT)									
ROUT (Output Resistance)	DAC is loaded with all zeros	I	4.5	6.5	8.5	4.5	6.5	8.5	KΩ
Output Resistance Tempco		II		-300			-300		ppm/°C
COUT (Output Capacitance)		II		10	15		10	15	pF
Output Voltage Swings	$R_L \geq 1M\Omega$	I		3			3		Volts
POWER SUPPLY									
VDD, VCC Range		I	4.75		5.25	4.75		5.25	Volts
IDD	All Digital inputs VIL or VIH	I			2			2	mA
IDD	All Digital inputs 0 or 5V	I			100			100	µA
ICC		I		3	6		3	6	mA

AC Parameters	Test Conditions	Test Level (1)	HDAC50800A Min	HDAC50800A Typ	HDAC50800A Max	HDAC50800B Min	HDAC50800B Typ	HDAC50800B Max	Units
DYNAMIC PERFOMANCE									
Output Voltage Settling Time	DAC is toggled between zero and full-scale	II		0.75			0.75		µS
Digital to Analog Glitch Impulse		II		20			20		nV-Sec
Output Voltage Noise Density		II		20			20		nV/ $\sqrt{Hz}$
TIMING CHARACTERISTICS									
tAS (Address Valid to Write Setup Time)		II	30			30			ns
tAH (Address Valid to Write Hold Time)		II	0			0			ns
tCS (Chip Select to Write Setup Time)		II	0			0			ns
tCH (Chip Select to Write Hold Time)		II	0			0			ns
$t\overline{WR}$ ($\overline{WR}$ Pulse Width)		II	100			100			ns
tDS (Data Setup Time)		II	80			80			ns
tDH (Data Hold Time)		II	10			10			ns

(1) Test Procedure: I - Production tested at the specified conditions. II - Guaranteed by design and sampled characterization data.

FIGURE 1 TIMING DIAGRAM



MODE SELECTION

WR	CS	A1	A0	FUNCTION
X	1	X	X	DEVICE NOT SELECTED
1	X	X	X	DEVICE NOT SELECTED
0	0	0	0	DIRECT DAC LOADING (2)
0	0	0	1	M.S. INPUT REGISTER LOADED FROM DATA BUS (BIT 8-13)
0	0	1	0	L.S. INPUT REGISTER LOADED FROM DATA BUS (BIT 0-7)
0	0	1	1	DAC REGISTER LOADED FROM INPUT REGISTERS

NOTES:
1. X = DON'T CARE CONDITION
2. WHEN A1=A2=0, INPUT REGISTERS ARE TRANSPARENT. BY PLACING ALL 0'S OR 1'S ON THE DATA INPUTS, THE DAC IS SET TO ZERO OR FULL SCALE CONDITION. THIS IS A USEFUL CALIBRATION TOOL.

TERMINOLOGY

Relative Accuracy

Relative accuracy, also known as endpoint nonlinearity, is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is expressed in % of full scale range or (sub)multiples of 1 LSB.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

Gain Error

Gain error, also known as full-scale error, is a measure of the deviation of the actual DAC full-scale output from the ideal full-scale output. For the HDAC50800, ideal full-scale output is (16383/16384)•3V + (Offset Error). Gain error and offset error are adjustable to zero using external trims as shown in Figure 5.

Output Voltage Settling Time

Time required for Vout to settle to within 1/2 LSB for a given digital stimulus, ie., zero to full-scale.

Digital to Analog Glitch Impulse

This is a measure of the amount of charge injected from the digital inputs to Vout when the input changes state. It is specified as the area of the glitch in nV-secs. The digital input is toggled between 01 1111 1111 1111 and 10 0000 0000 0000 with Vref at 3 Volts.

GENERAL CIRCUIT DESCRIPTION

Conversion Section

The HDAC50800 uses a modified R-2R resistor ladder network for digital-to-analog conversion. A functional diagram of this internal network is shown in Figure 2. To ensure a low Differential Linearity Error, the three most significant bits of the DAC use a segmented architecture, while the remaining eleven bits use the classical R-2R structure. Laser trimmed thin-film resistors assure high accuracy and stability over time and temperature.

Position of internal switches S0-S17 determine the DAC output voltage and are controlled by the the DAC input code DB0-DB13. The internal Vref node is maintained at 3 Volts by the reference buffer which provides a DAC output range of 0 to 3 Volts.

Reference Buffer

The internal Vref node is driven by the on-chip Reference Buffer as illustrated in the block diagram. By using internal buffering, the DAC's settling time is minimized and less constraint is placed on the external reference. The on-chip reference buffer also simplifies the bipolar output option covered later in this section.

Reference Input Voltage Divider

The HDAC50800 can use either a 5 or 10 Volt reference using input pins +5V REF or +10V REF, respectively. The unused reference pin must be tied to AGND. The input reference voltage is divided down internally to provide an internal reference voltage of 3 Volts. Gain matching between the two references is ensured by thin film laser trimming.

Internal Application Resistors

The Vout pin provides an output signal ranging from 0 to 3 Volts with an output impedance of 6.5 kΩ typical. In many applications, output buffering and gain are desirable to increase the output voltage range. The HDAC50800 contains trimmed thin-film application resistors for use with an external op amp. These can be configured to provide output ranges of 0 to 10 Volts or -5 to +5 Volts.

Figure 3 shows how to connect the external op amp. As shown in the table of Figure 3, pin R is connected to analog ground to provide a 0 to 10 Volt unipolar output. In this configuration, the op amp is connected as a non-inverting amplifier with a gain of 10/3.

Pin R is connected to pin BIPOLAR OFFSET (bipolar offset) to provide a -5 to +5 Volt bipolar output range. BIPOLAR OFFSET is internally connected to the Reference Buffer output. The op amp in the bipolar output mode is configured so that:

$V_{BUFF-OUT} = (10/3)(Vout) - (5/3)(Vref)$

No attempt should be made to use the BIPOLAR OFFSET output as a reference source for other external devices. Additional loading of this pin may degrade device performance.

Unlike a current-output type DAC, the input offset voltage of the external op amp will not cause a non-linearity over the output range. Because of the constant output impedance of the HDAC50800, output offset will remain constant over the output range. Output offset adjustment therefore is only required in those applications requiring absolute accuracy.

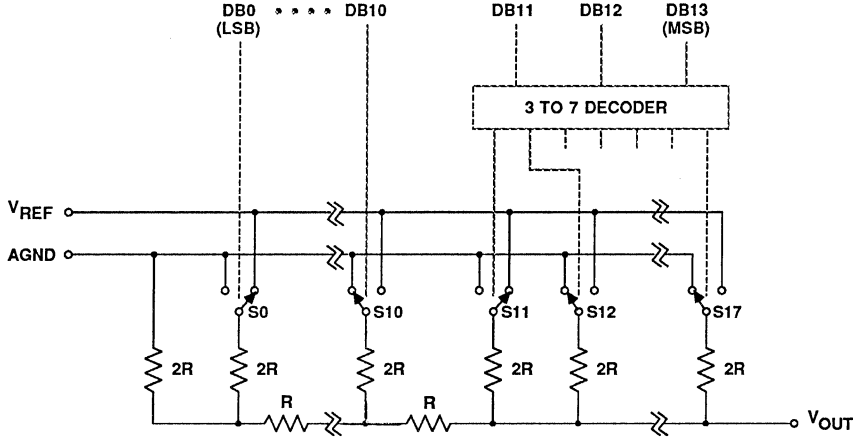
Input Logic and Interfacing

Data is loaded into the HDAC50800 with two 8-bit bytes of right-justified data, where DB0 is the least significant bit (LSB). Pins $\overline{CS}$ and $\overline{WR}$ control the loading of the DAC input registers and pins A0 and A1 determine the register address. With the proper register address selected, data is loaded when either $\overline{WR}$ or $\overline{CS}$ returns to logic high. For complete information on input register loading, please refer to the Timing Diagram of Figure 1 and to the Timing Characteristics. Pins $\overline{WR}$ and $\overline{CS}$ may be used interchangeably.

Table 1 summarizes the control logic functions. Pins A0 and A1 define a total of four memory locations, two of which are the input registers. Addressing A0=A1=1 loads the DAC register from the input register with the occurrence of $\overline{WR}$=$\overline{CS}$=0. This immediately effects the value of Vout. Addressing A0=A1=0 causes the input registers to be transparent. In this case, input logic codes of all 0's or all 1's create a DAC zero output or a full-scale output, respectively. No other input codes are valid in this mode.

The input logic scheme of the HDAC50800 is designed for direct interface and control by an 8-bit microprocessor. Since the device is designed for write pulse widths as short as 100 ns, it ensures operation with a wide range of high-speed microprocessors. Figure 4 illustrates simplified microprocessor interfacing.

Figure 2. Equivalent Resistor Network for the HDAC50800 DAC Circuitry



APPLICATION HINTS

External Operational Amplifier Selection

When application of the HDAC50800 requires an external op amp for output signal gain or buffering, selection of the op amp type can involve trade-offs between cost, accuracy, and speed. As an example, consider the circuit of Figure 3. In this application, if R is tied to AGND, the amplifier is configured for a non-inverting gain of 10/3 to provide a 10 Volt output swing. To contribute less than 1/4 LSB linearity error at Vbuff-out, the op amp's large-signal open loop voltage gain (Avol) must be 250 V/mV (108 dB) minimum. Input offset drift over temperature, which is also multiplied by 10/3, will also effect Vbuff-out accuracy. For the circuit of Figure 3, an error of less than 1/4 LSB over a 50°C temperature change will be maintained with an op amp having a ΔVos/°C of 3 μV/°C maximum; for a 100°C change, 1.5 μV/°C maximum is required.

The slew rate and bandwidth requirement will vary depending on application. Fast op amps, such as the OP17 at 60 V/μs slew rate and 30 MHz bandwidth, will provide a very fast settling time so that the output Vbuff-out in Figure 3 can approach the 750ns settling time of the HDAC50800. Input noise, like input offset, is multiplied by the non-inverting gain of the circuit (noise gain). Most modern high-accuracy op amps which provide suitable gain also have sufficiently low input noise. Proper op amp decoupling and good layout techniques are also essential to maintain low input noise.

Good op amp choices for high gain accuracy include the OP-43, OP-77, and the LT1001-LT1008. For high accuracy and high speed the OP-27 or the still faster OP-37 are good choices.

Offset and Full Scale Trim Adjustments

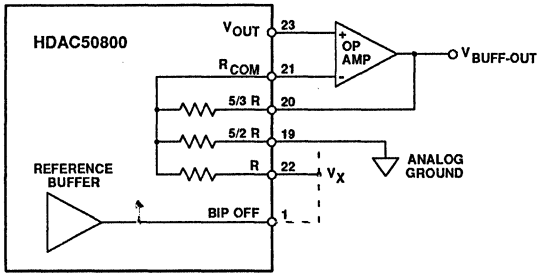
Although the application resistor ratios are matched to better than ±0.05%, this error combined with the DAC's offset and gain errors are important to consider when utilizing the circuit of Figure 3. With the addition of external trim resistors as shown in Figure 5, offset and gain errors can be eliminated. The values of Ra, Rb and Rc as shown will work for both the HDAC50800A and HDAC50800B grades.

Calibration for 0-10 Volt Unipolar Output Operation

When using the 0 - 10 Volt unipolar output circuit option of Figure 5, the Zero setting (offset) is accomplished by adjustment of potentiometer Ros. Ros performs internal nulling of the op amp. The value and connection of Ros should be as specified in the op amp manufacturer's data sheet to minimize temperature drift. Range of offset adjustment using this procedure will typically be ±5 mV. A thermally stable multi-turn potentiometer should be used for Ros.

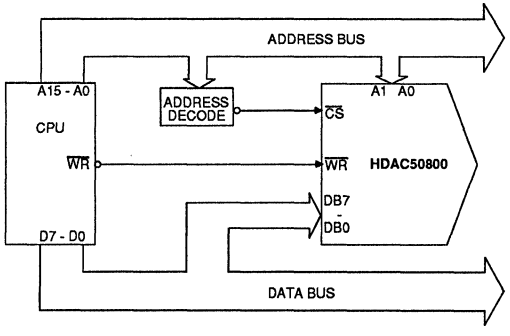
Full-scale adjustment is provided by external resistor Ra and potentiometer Rc. Ra and Rc add to the the total input and feedback resistance provided by the internal application resistors and allow a ±10 LSB adjustment range. Like Ros, Ra and Rc should have low temperature coefficients with the latter being a multi-turn potentiometer. Rb is not used and can be omitted for unipolar operation.

Figure 3. Connection Diagram of External Operational Amplifier Utilizing Internal Application Resistors



V_X CONNECTION	$V_{BUFF-OUT}$ RANGE
ANALOG GROUND	0- ↘+10V (UNIPOLAR)
PIN BIP OFF	-5 → +5V (BIPOLAR)

Figure 4. Typical Microprocessor Interface (Simplified)



The procedure for trim adjustment using the 0-10 Volt unipolar circuit option of Figure 5 is as follows:

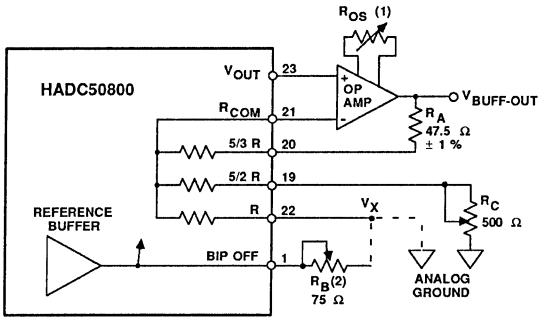
1) Set zero value: With [00 0000 0000 0000] in the input register, adjust potentiometer Ros to obtain 0.0000 Volts at Vbuff-out.
(0.00061 V equals 1 LSB)

2) Set full scale value: With [11 1111 1111 1111] in the input register, adjust potentiometer Rc to obtain the correct Full-scale output minus 1 LSB which is 9.99939 Volts.
([Full-scale output] = [(16383/16384)•10V] + [Zero output])

Calibration for ±5 Volt Bipolar Output Operation

For the ±5 Volt bipolar output circuit option of Figure 5, Zero output occurs at - 5 Volts. By use of the application resistors connected as shown, the Zero output is derived by multiplying the 3 Volt reference at pin BIPOLAR OFFSET by -5/3. Zero output at Vbuff-out is adjusted by potentiometer Rb which changes the -5/3 gain. Potentiometer Ros is optional and should only be used with op amps that are not internally trimmed. When Ros is used, the op amp offset is adjusted first. As in the bipolar circuit option, potentiometer Rc is used to adjust full-scale value.

Figure 5. Modification of Figure 3 Showing Use of External Trim Resistors



V_X CONNECTION	$V_{BUFF-OUT}$ RANGE
ANALOG GROUND R_B	0→+10V (UNIPOLAR) -5→+5V (BIPOLAR)

NOTES: (1) R_{OS} IS OPTIONAL IN BIPOLAR OPERATION.
(2) R_B IS NOT USED AND THEREFORE CAN BE ELLIMINATED IN UNIPOLAR O PERATION.

The procedure for trim adjustment using the ±5 Volt bipolar circuit option of Figure 5 is as follows:

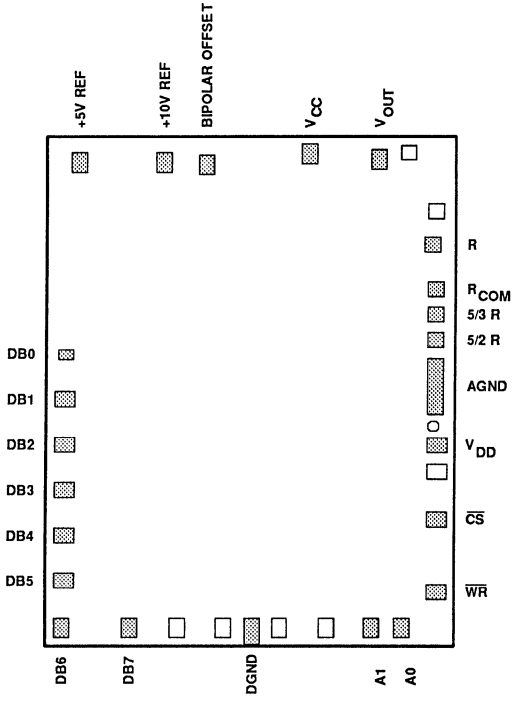
1) Zero the input offset voltage to the op amp. Do this by writing [00 0000 0000 0000] into the input register and shorting the inverting and non-inverting op amp inputs to ground. Adjust Ros until Vbuff-out is as near to 0 Volts as possible. Delete this step if resistor Ros is not used.

1) Set Zero value: With [00 0000 0000 0000] in the input register, adjust potentiometer Rb to obtain a -5.0000 Volt output at Vbuff-out.
(0.00061 V equals 1 LSB)

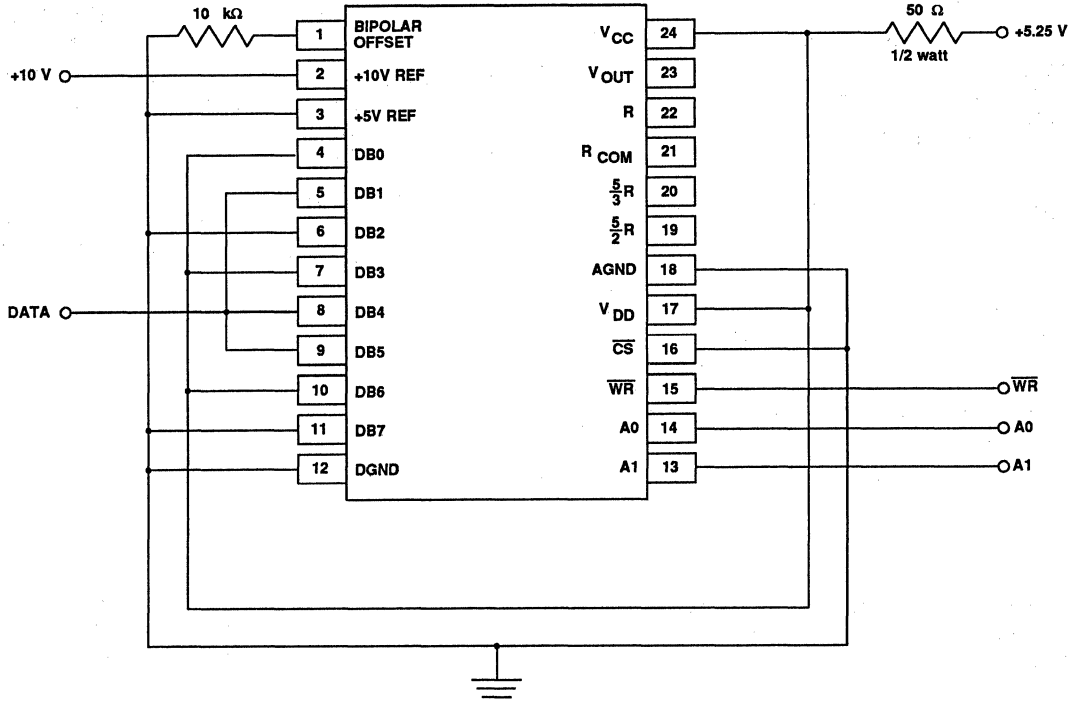
2) Set full scale value: With [11 1111 1111 1111] in the input register, adjust potentiometer Rc to obtain the correct Full-scale output minus 1 LSB which is 4.99939 Volts.
[Full-scale output] = [(16383/16384)•10V] + [Zero output])

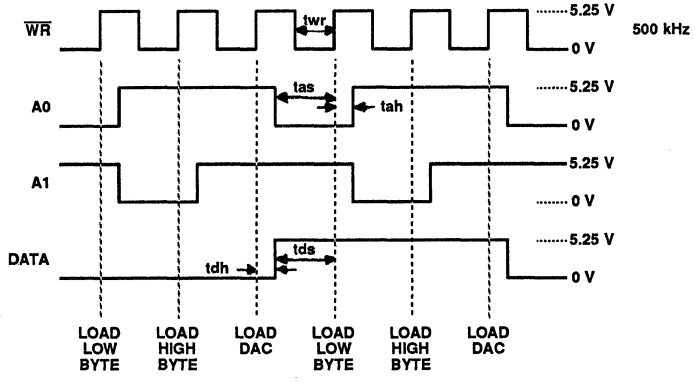
Die Plot

136 X 172 mils



Burn-In Configuration



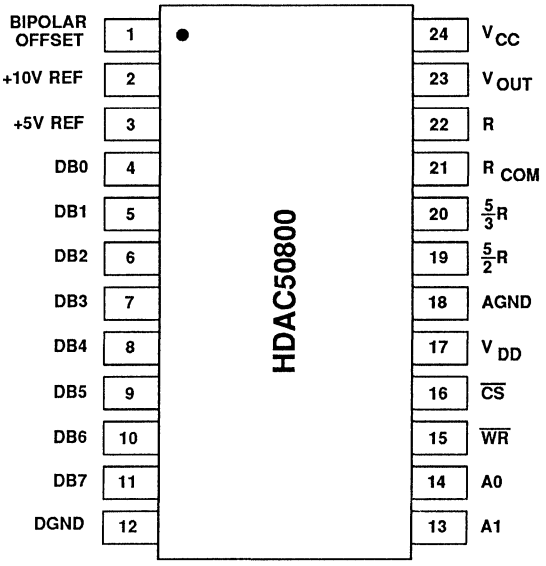


twr = 1.0 µs ± 200 ns

tas = tds = 1.5 µs ± 200 ns

tah = tdh = 0.5 µs ± 200 ns

Pin Assignment



Pin Functions

PIN	PIN NAME	FUNCTION
1	BIPOLAR OFFSET	VREF OUTPUT FOR BIPOLAR OPERATION
2	+10V REF	INPUT FOR 10V REFERENCE VOLTAGE
3	+5V REF	INPUT FOR 5V REFERENCE VOLTAGE
4	DB0	INPUT DATA BIT 0 (LSB) OR 8
5	DB1	INPUT DATA BIT 1 OR 9
6	DB2	INPUT DATA BIT 2 OR 10
7	DB3	INPUT DATA BIT 3 OR 11
8	DB4	INPUT DATA BIT 4 OR 12
9	DB5	INPUT DATA BIT 5 OR 13 (MSB)
10	DB6	INPUT DATA BIT 6
11	DB7	INPUT DATA BIT 7
12	DGND	DIGITAL GROUND
13	A1	INPUT ADDRESS LINE A1
14	$\overline{A0}$	INPUT ADDRESS LINE A0
15	$\overline{WR}$	DATA WRITE
16	$\overline{CS}$	CHIP SELECT
17	V_{DD}	DIGITAL POSITIVE POWER SUPPLY
18	AGND	ANALOG GROUND
19	5/2 R	APPLICATION RESISTOR NETWORK
20	5/3 R	APPLICATION RESISTOR NETWORK
21	R_{COM}	APPLICATION RESISTOR NETWORK
22	R	APPLICATION RESISTOR NETWORK
23	V_{OUT}	ANALOG VOLTAGE OUTPUT
24	V_{CC}	ANALOG POSITIVE POWER SUPPLY

***For Ordering Information See Section 1.*

NOTES:

HDAC51400

8-BIT, ULTRA HIGH SPEED D/A CONVERTER

FEATURES

- **400 MWPS Nominal Conversion Rate**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Stable On-chip Bandgap Reference
- Registered Data And Video Controls
- Differential Current Outputs
- 50 and 75 Ohm Output Drive

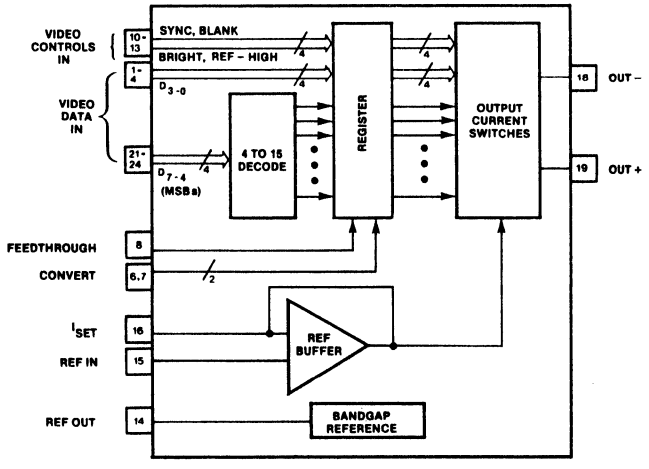
APPLICATIONS

- **Raster Graphics**
- High Resolution Color or Monochrome Displays to 2K x 2K Pixels
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

GENERAL DESCRIPTION

The HDAC51400 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at 400 MWPS. Complete with video controls (Sync, Blank, Reference White [Force High], Bright) the HDAC51400 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC51400 includes an internal precision bandgap reference which can drive two other 51400s in an RGB graphics system. The HDAC51400 contains data and control input registers, video control logic, reference, and current switches in 24 Lead CERDIP, or ceramic sidebrazed DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 20°C

Supply Voltages

V_{EED} (measured to V_{CCD}) . . . . . −7.0 to 0.5V
V_{EEA} (measured to V_{CCA}) . . . . . −7.0 to 0.5V
V_{CCA} (measured to V_{CCD}) . . . . . −0.5 to 0.5V

Input Voltages

CONV, Data, and Controls . . . . . V_{EED} to 0.5V
(measured to V_{CCD})

REF + (measured to V_{CCA}) . . . . . V_{EEA} to 0.5V
REF − (measured to V_{CCA}) . . . . . V_{EEA} to 0.5V

Temperature

Operating, Ambient . . . . . −60 to +140°C
Junction . . . . . +175°C
Lead, Soldering (10 seconds) . . . . . +300°C
Storage . . . . . −60 to +150°C

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS		$V_{CCA} = V_{CCD} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25°C, I_{SET} = 1.105$ mA					
E_{LI}	Integral Linearity Error	$1.0mA < I_{SET} < 1.8mA$	I	−0.2 −½		+0.2 +½	% Full Scale LSB
E_{LD}	Differential Linearity Error	$1.0mA < I_{SET} < 1.8mA$	I	−0.2 −½		+0.2 +½	% Full Scale LSB
E_G	Gain Error		III	−5		+5	% Full Scale
TC_G	Gain Error Tempco				150		PPM/°C
TC_B	Bandgap Tempco				100		PPM/°C
$V_{REF-OUT}$	Reference Voltage	(measured to V_{CCA})			−1.2		V
$I_{REF-OUT}$	Reference Output Current					−50	μA
C_{REF}	Input Capacitance, I_{SET}, REF IN		V		5		pF
V_{OCP}	Compliance Voltage, + Output		I	−1.5		+3	V
V_{OCN}	Compliance Voltage, − Output		I	−1.5		+3	V
R_{OUT}	Equivalent Output Resistance		I	20			K Ohm
C_{OUT}	Output Capacitance		V		9		pF
I_{OP}	Maximum Current, + Output	$R_L = 0\Omega$	V			45	mA
I_{ON}	Maximum Current, − Output	$R_L = 0\Omega$	V			45	mA
I_{OS}	Output Offset Current		I			½	LSB
V_{IH}	Input Voltage, Logic HIGH		I			−1.4	V
V_{IL}	Input Voltage, Logic LOW		I	−1.0			V
V_{ICM}	Convert Voltage, Common Mode Range		I	−0.5		−2.5	V

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS	$V_{CCA} = V_{CCD} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25°C, I_{SET} = 1.105mA$						
V_{IDF}	Convert Voltage, Differential		IV	0.4		1.2	V
I_{IL}	Input Current, Logic LOW, Data and Controls					120	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls				10	120	μA
I_{IC}	Input Current, Convert				2	60	μA
C_I	Input Capacitance, Data and Controls		V		3		pF
PSR	Power Supply Sensitivity		I	−120		+120	μA/V
I_{EE}	Supply Current		I		175	200	mA
I_{SET}	Reference Input Current	$R_L = 37.5\Omega$ $R_L = 25\Omega$			1.105 1.658		mA mA

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS	$R_L = 37.5$ Ohms, $C_L = 5pF$ (unless otherwise specified), $T_A = 25°C$, $I_{SET} = 1.105$ mA						
F_S	Maximum Conversion Rate		I	385	400		MWPS
t_{RI}	Rise Time	10% to 90% G.S.	I			900	ps
t_{RI}	Rise Time	10% to 90% G.S. $R_L = 25$ Ohms Total	I			600	ps
t_{SI}	Current Settling Time, Clocked Mode	To 0.2%	IV		4		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% $R_L = 25$ Ohms Total	IV		3		ns
t_{DSC}	Clock to Ouptut Delay, Clocked Mode		I			4	ns
t_{DST}	Data to Output Delay, Transparent Mode		I			6	ns
t_{PWL}	Convert Pulse Width, LOW		I		1.25		ns
t_{PWH}	Convert Pulse Width, HIGH		I		1.25		ns
BW_{REF}	Reference Bandwidth, −3dB		V	0.7	1.25		MHz

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF (unless otherwise specified), T_A = 25°C, I_{SET} = 1.105 mA							
	Glitch Energy	Area = ½ VT	V		10		pV-s
t_S	Set-up Time, Data and Controls		I		1		ns
t_H	Hold Time, Data and Controls		I	0	−200		ps
SR	Slew Rate	20% to 80% G.S.	I	700			V/μS
FT_C	Clock Feedthrough		I			−48	dB

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at T_a = 25°C, and sample tested at specified temperature.
III	QA sample tested only at specified temperatures
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

APPLICATION INFORMATION

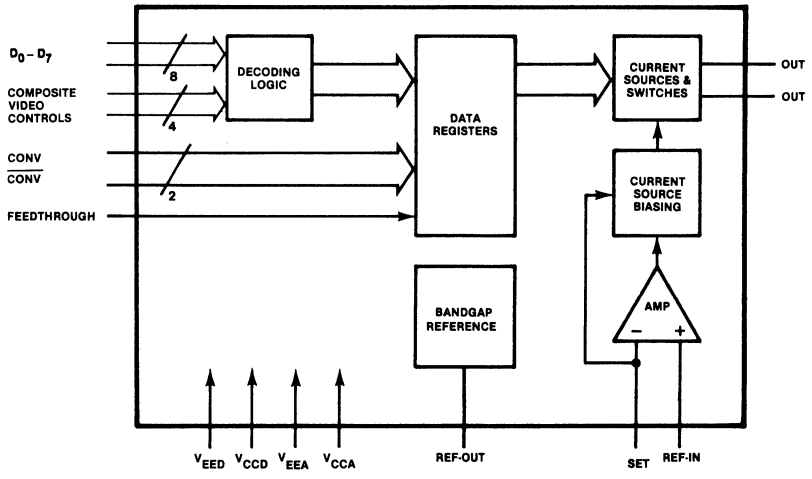
The HDAC51400 is a high speed video Digital-to-Analog converter capable of up to a 400 MWPS conversion rate. This makes the device suitable for driving 2048 X 2048 pixel displays at 60 to 90 Hz update rates. In addition, the HDAC51400 includes an internal bandgap reference which may be used to drive two other HDAC51400s if desired.

The HDAC51400 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC51400 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC51400 in a color raster application is shown in Figure 2. The HDAC51400 requires few external components and is extremely easy to use. The very high operating speed of the HDAC51400 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC51400. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a −2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC51400 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 Ohm transmission system as shown. The source impedances of the HDAC51400 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

FIGURE 1 TIMING DIAGRAM

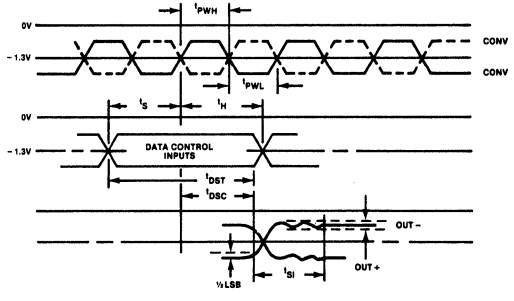
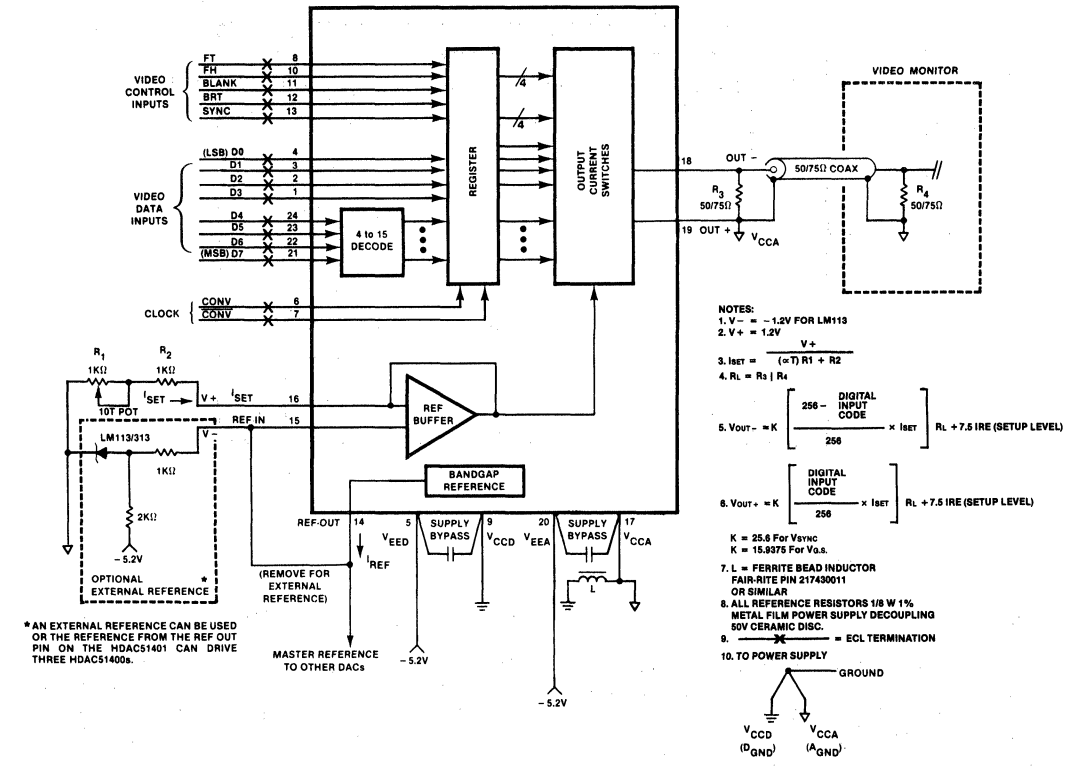


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC51400 operates from a single standard −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC51400's inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC51400 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog supply return is V_{CCA}. All power and ground pins must be connected in any application. If a +5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC51400 has two reference inputs: REF IN and I_{SET} and one reference output REF OUT. The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the (I_{SET}) input on the HDAC51400. A method and equations to set I_{SET} is shown in Figure 2. The HDAC51400 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF − IN pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 to 1K Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased by 50% above for doubly terminated 75 Ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The HDAC51400 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) minimizing glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC51400 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_S before, and a hold time of t_H after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC51400. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC51400 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{SET} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and − 1.07V. The OUT − output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the − 1.07V level. The OUT + is inverted with SYNC up.

Table 1 Video Control Operation

Sync	Blank	Ref White	Bright	Data Input	Out − (mA)	Out − (V)	Out − (IRE)	Description
1	X	X	X	X	28.57	− 1.071	− 40	Sync Level
0	1	X	X	X	20.83	− 0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	− 0.073	100	Normal High Level
0	0	0	0	000...	19.40	− 0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	− 0.073	100	Normal High Level
0	0	0	1	000...	17.44	− 0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

FIGURE 3 CONVert, $\overline{\text{CONV}}$ SWITCHING LEVELS

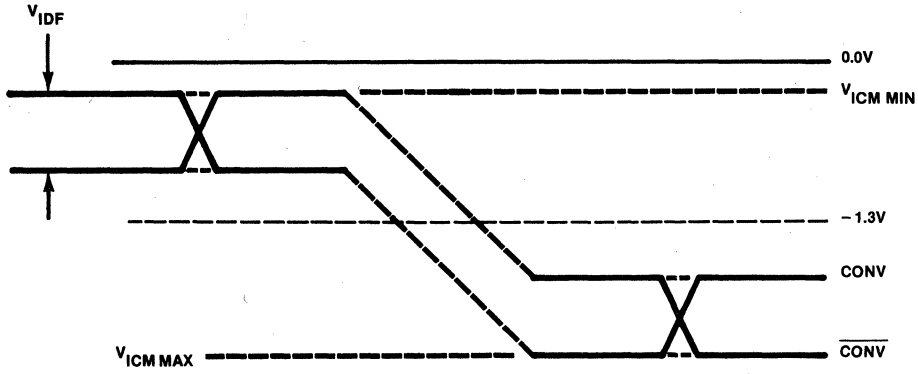


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

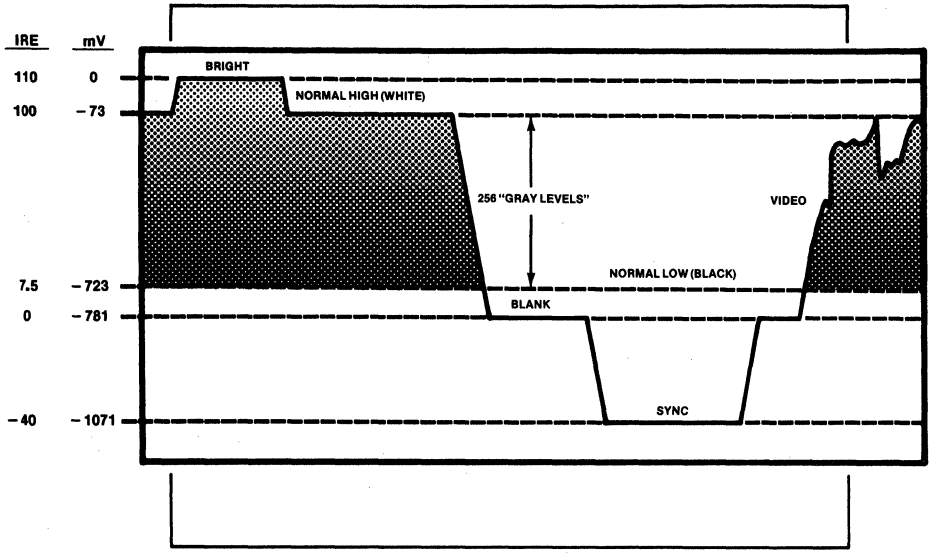


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

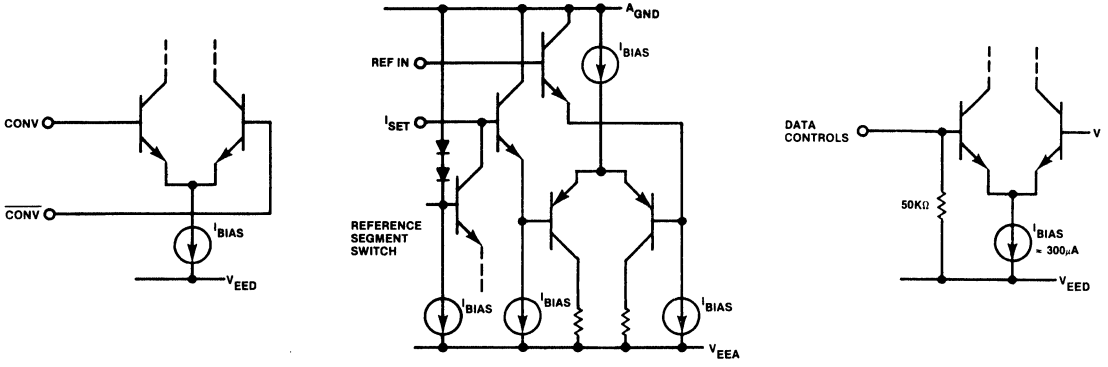


FIGURE6 DAC OUTPUT CIRCUIT

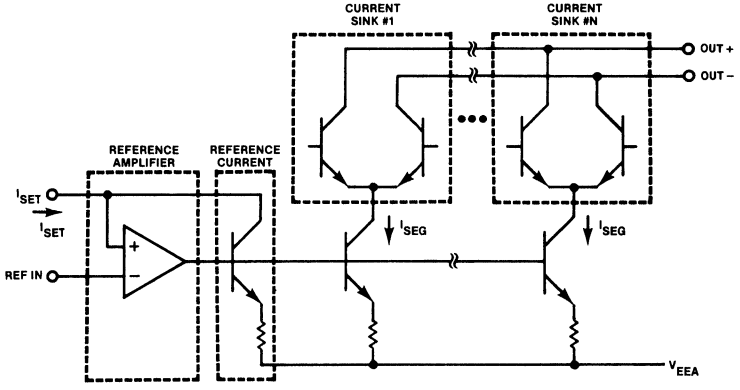


FIGURE 7A STANDARD LOAD

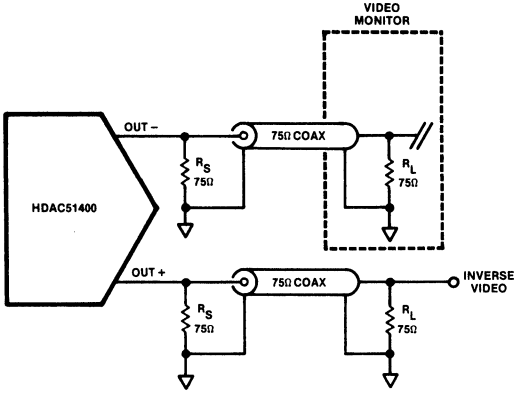


FIGURE 7B TEST LOAD

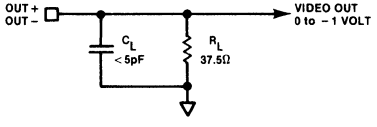
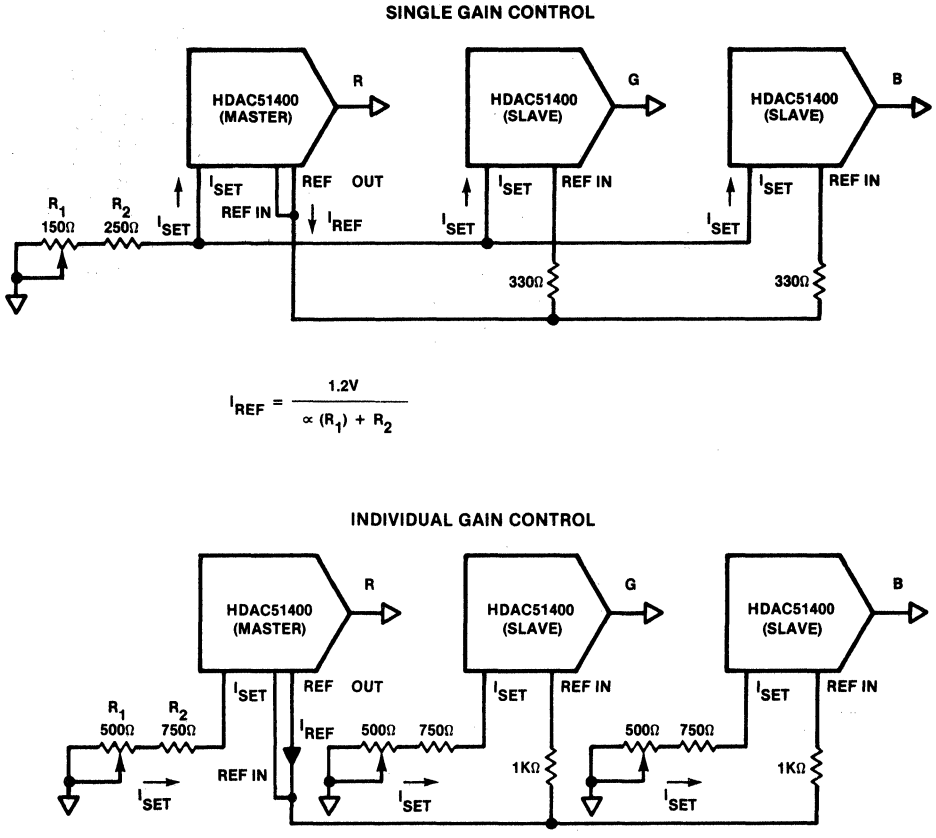


FIGURE 8 TYPICAL RBG GRAPHICS SYSTEM



TYPICAL RGB GRAPHICS SYSTEM

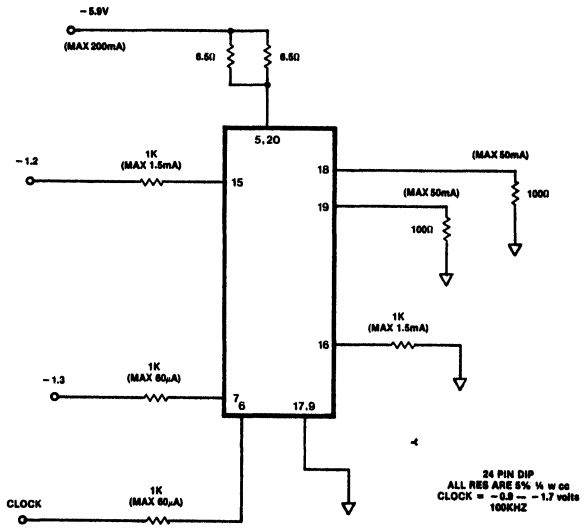
In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

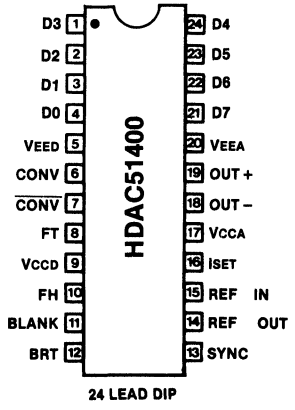
The HDAC51400 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50μA to an external load. This can accommodate three DAC reference inputs.

The circuits shown in Figure 8 illustrate how a single HDAC51400 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC51400's reference output.

FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS



24 LEAD DIP

PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
REF IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

**For Ordering Information See Section 1.*

NOTES:

HDAC51600

8-BIT, 250 MWPS MULTIPLEXED VIDEO DAC

PRELIMINARY INFORMATION

FEATURES:

- 5:1 OR 4:1 Data Multiplexer
- 250 MWPS Conversion Rate
- TTL Compatible Data I/O
- On-Chip Bandgap Reference
- RS-343-A Compatible Video Levels

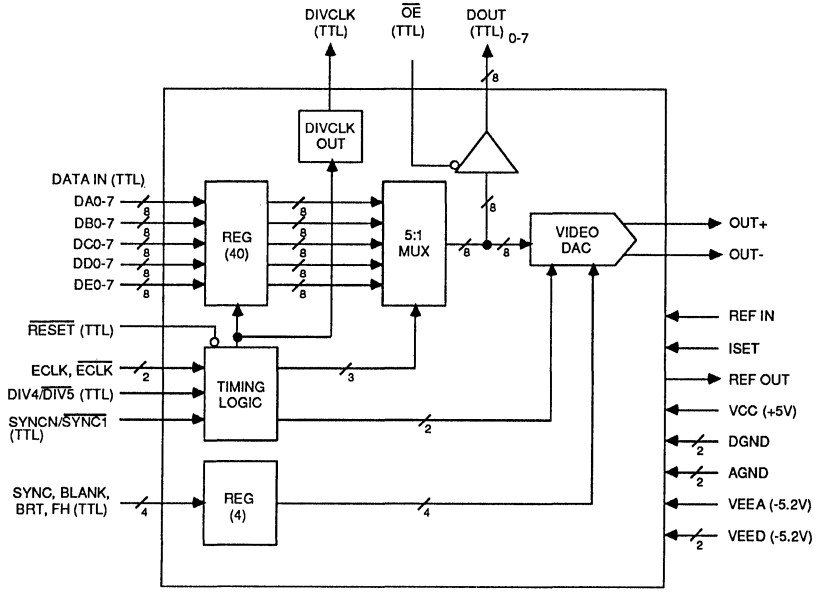
APPLICATIONS:

- Digital Video Signal Processing
- High Resolution Color or Monochrome Displays
- Medical Elecronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Waveform Generation

GENERAL DESCRIPTION

The HDAC51600 is a monolithic high-speed video DAC with a multiplexed data interface, and an internal voltage reference. All digital inputs and outputs are TTL compatible except the input clock, which is ECL compatible for high speed. The multiplexer is selectable as a divide by 4 or 5, and the multiplexed data is available through an output port. A divided clock output is provided for synchronization with external circuitry. The video control inputs (SYNC, BLANK, BRighT, and Force High) are fully synchronous with the pixel data at either the input clock or divided clock rate. The DAC has a differential output that can directly drive doubly terminated 50 or 75 Ohm loads to standard RS-343-A levels. The standard set-up level is 7.5 IRE.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS 25°C (1)

Supply Voltages

Positive Supply Voltage (VCC to GND).....+6.0 to - 0.5V
Negative Supply Voltage (VEE to GND)..... - 6.0 to +5.0V
Voltage Differential (DGND to AGND, VEED to VEEA) ..... - 0.5 to +0.5V

Input Voltages

Data, Controls (TTL, measured to DGND) ..... - 0.5 to VCC
ECLK, $\overline{\text{ECLK}}$ (ECL, measured to DGND) ..... - 0.5 to VEE

Output

Applied Voltage..... VEE - 0.5 to VCC +0.5

Temperature

Operating Temperature, junction ..... +175°C
Lead Temperature (soldering 10 seconds) ..... +300°C
Storage Temperature ..... - 65 to +150°C

(1) Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS (1)

Figure 3. VCC= 5V, VEEA= VEED= -5.2V, AGND= DGND= 0.0V, TA= 25°C, ISET= 1.105mA, unless otherwise specified.

DC Electrical Parameters	Test Conditions	Test Level (1)	Room +25°C MIN	Room +25°C TYP	Room +25°C MAX	Hot +70°C MIN	Hot +70°C MAX	Cold 0°C MIN	Cold 0°C MAX	Units
DAC CHARACTERISTICS										
Resolution		I		8						Bits
Integral Linearity, Gray Scale	1.2mA≤ISET ≤1.8mA	I	-0.2	±0.1	+0.2					%G.S.
			-1/2	±1/4	±1/2					LSB
Integral Linearity Tempco		V		TBD						ppm/°C
Differential Linearity, Gray Scale	1.2mA≤ISET ≤1.8mA	I	-0.2	±0.1	+0.2					%G.S.
			-1/2	±1/4	±1/2					LSB
Differential Linearity Tempco		V		TBD						ppm/°C
Gain Error, Gray Scale	(Excluding Reference)	I	-5		+5					%G.S.
Gain Error Tempco		V		±150						ppm/°C
Offset Current, Outputs, IOS		I		5	15					µA
Gray Scale Current, Outputs, IGS		V	16.7	17.6	18.5					mA
Gray Scale Voltage, Outputs, VGS		V	629	661	694					mV
SYNC Voltage, Outputs		I	260	286	314					mV
Blank Voltage, Outputs		I	48	54	59					mV
BRighT Voltage, Outputs		I	64	71	79					mV

ELECTRICAL SPECIFICATIONS (Cont'd)

DC Electrical Parameters	Test Conditions	Test Level (1)	Room +25°C MIN	Room +25°C TYP	Room +25°C MAX	Hot +70°C MIN	Hot +70°C MAX	Cold 0°C MIN	Cold 0°C MAX	Units
DAC CHARACTERISTICS (Cont'd)										
Maximum Allowable Current, Outputs	ISET is User Defined	IV			45		45		45	mA
Compliance Voltage, Outputs		V	-1.5		+1.5					V
Output Resistance	RL = ∞	I	20							KΩ
Output Capacitance	CL = 0	IV		10	13					pF
Power Supply Sensitivity	$\frac{\Delta IGS}{\Delta VEEA}$	I			±120					µA/V
REFERENCE CHARACTERISTICS										
Bandgap Voltage	IREF = -50µA	I	1.17		1.29					V
Bandgap Output Current, IREF		I			-50					µA
Bandgap Tempco	IREF = -10µA	V		±100						ppm/°C
Common Mode Range REF IN, ISET Pins		IV	-2.45		-0.275					V
Bandgap Power Supply Sensitivity	ΔVREF / ΔVEEA	V		TBD						dB
Input Capacitance REF IN, ISET Pins		V		5						pF
Input Current, REF IN		IV		3	15					µA
Input Current, ISET		IV			1.80		1.80			mA
DIGITAL LOGIC CHARACTERISTICS										
Input Voltage, Logic Low, TTL		I			0.8					V
Input Voltage, Logic High, TTL		I	2.0							V
Input Current, Logic Low, TTL		I			- 500					µA

ELECTRICAL SPECIFICATIONS (Cont'd)

DC Electrical Parameters	Test Conditions	Test Level (1)	Room +25°C MIN	Room +25°C TYP	Room +25°C MAX	Hot +70°C MIN	Hot +70°C MAX	Cold 0°C MIN	Cold 0°C MAX	Units
DIGITAL LOGIC CHARACTERISTICS										
Input Current, Logic High, TTL		I			-500					µA
Differential Range, ECLK, $\overline{ECLK}$, VIDF	See Fig. 5	IV	0.35		1.65					V
Common Mode Range, ECLK, $\overline{ECLK}$, VICM	See Fig. 5	IV	- 0.5		- 2.5					V
Input Current, ECLK, $\overline{ECLK}$		I		5	60					µA
Input Capacitance, ECLK, $\overline{ECLK}$		V		5	10					pF
Output Voltage, Logic Low, DOUT, DIVCLK		I			0.4					V
Output Voltage, Logic High, DOUT, DIVCLK		I	2.4							V
Output Current, DIVCLK		I			16					mA
Output Current, DOUT		I			TBD					mA
POWER SUPPLY CHARACTERISTICS										
Supply Voltage, VCC		IV	4.5		5.5					V
Supply Voltage, VEEA, VEED		IV	- 5.5		- 4.5					V
Supply Current, ICC		I		95	115					mA
Supply Current, IEEA		I		- 50	- 60					mA
Supply Current, IEED		I		- 395	- 475					mA
Differential Voltage, AGND to DGND, VEEA to VEED		IV	- 0.1		+0.1					V

AC Electrical Parameters	Test Conditions	Test Level (1)	Room +25°C MIN	Room +25°C TYP	Room +25°C MAX	Hot +70°C MIN	Hot +70°C MAX	Cold 0°C MIN	Cold 0°C MAX	Units
Maximum Conversion Rate		I	165	250						MWPS

ELECTRICAL SPECIFICATIONS (Cont'd)

AC Electrical Parameters	Test Conditions	Test Level (1)	Room +25°C MIN	Room +25°C TYP	Room +25°C MAX	Hot +70°C MIN	Hot +70°C MAX	Cold 0°C MIN	Cold 0°C MAX	Units
DAC CHARACTERISTICS (See Timing Diagrams)										
Rise/Fall Times, Outputs	10-90% G.S. ISET=1.65mA RL=25Ω	I			1					ns
Rise/Fall Times, Outputs	10-90% G.S.	IV			1.5					ns
Slew Rate, Outputs		I	525							V/µS
Settling Time, Outputs	Full Scale Transition to 0.2%	V		4						ns
Settling Time, Outputs	Full Scale Transition to 0.8%	V		3						ns
ECLK to Output Delay		I	TBD		5					ns
Clock to Output Latency, Data, Video Controls		I	2		2					Cycles
Feedthrough, Clock, Data, Controls		I			TBD					dB
Peak Glitch, VGL	1 LSB Transition at midscale	V		2.8						mV
Glitch (1/2 VGL X Time)	1 LSB Transition at midscale	V		3						pV-s
REFERENCE CHARACTERISTICS										
Amplifier Bandwidth, - 3dB		V		1						MHz
DIGITAL LOGIC CHARACTERISTICS (See Timing Diagrams)										
Maximum Clock Period		I	6	4						ns
Pulse Width, High ECLK, $\overline{\text{ECLK}}$, TPWH		I	2.5	2						ns
Pulse Width, Low ECLK, $\overline{\text{ECLK}}$, TPWH		I	2.5	2						ns
Set-Up Time, Data to DIVCLK, TSD		I	10	6.5						ns

ELECTRICAL SPECIFICATIONS (Cont'd)

AC Electrical Parameters	Test Conditions	Test Level (1)	Room +25°C MIN	Room +25°C TYP	Room +25°C MAX	Hot +70°C MIN	Hot +70°C MAX	Cold 0°C MIN	Cold 0°C MAX	Units
Hold Time, Controls to DIVCLK, THV		I	0	- 3.5						ns
Set-Up Time, Controls to ECLK, TSV	$\overline{SYNCN}$ / $\overline{SYNC1}$ = 0	I	10	6.5						ns
Hold Time, Controls to DIVCLK, THV	$\overline{SYNCN}$ / $\overline{SYNC1}$ = 0	I	0	- 3.5						ns
Set-Up Time, Controls to ECLK, TSV	$\overline{SYNCN}$ / $\overline{SYNC1}$ = 0	I	4	1.75						ns
Hold Time, Controls to ECLK, THV	$\overline{SYNCN}$ / $\overline{SYNC1}$ = 0	I	3	0.75						ns
Output Data Rate		IV			60					MWPS
Output Delay, ECLK to DIVCLK, Rise/Fall, TDDC		I		6.0 / 12.0						ns
Output Delay, ECLK to Data Out, Rise/Fall, TDDM		I		6.0 / 12.0						ns
Set-Up Time, $\overline{RESET}$ to ECLK, TSR		I	4	1						ns

(1) All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level Column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests performed after a three minute power soak.

Test Level I - 100% production tested at the specified temperatures.
Test Level II - 100% production tested at Ta=25°C and sample tested at the specified temperatures.
Test Level III - QA sample tested only at the specified temperatures.
Test Level IV - Parameter is guaranteed (but not tested) by design and characterization data.
Test Level V - Parameter is a typical value for information purposes only.

FUNCTIONAL DESCRIPTION

The HDAC51600 is a 250 MWPS raster graphics subsystem that includes an 8-bit DAC with precision bandgap reference, 5:1 or 4:1 selectable multiplexer, MUX output port, and MUX timing logic. The DAC will directly drive doubly-terminated 50 or 75 Ohm loads to standard RS-343-A levels.

All digital inputs and outputs are TTL compatible, except ECLK, which is ECL compatible. This allows the pixel data to be run at 50 MWPS data rates requiring only one high speed differential ECL clock. A reset input ($\overline{\text{RESET}}$) and divided clock output (DIVCLK) are provided for synchronizing external circuitry. Video control inputs are fully synchronous with the pixel inputs. A MUX data output provides the multiplexed pixel data for reading at the DOUT port.

DIV4/$\overline{\text{DIV5}}$ AND SYNCN/$\overline{\text{SYNC1}}$ CONTROLS

Two control lines (DIV4/$\overline{\text{DIV5}}$ and SYNCN/$\overline{\text{SYNC1}}$) determine which of four operating modes is to be selected: 5:1 or 4:1 MUX with either ECLK or DIVCLK timing for the video controls. These control lines should not be dynamically switched, as this will upset the internal state machine.

5:1 MUX

With DIV4/$\overline{\text{DIV5}}$=0 and SYNCN/$\overline{\text{SYNC1}}$=1 (Mode A; see Timing Diagram A), the IC operates in a 5:1 MUX mode. The five data words and video controls (SYNC, BLANK, BRighT, and Force High) are latched on the rising edge of DIVCLK. If any video controls are asserted they remain active for a full DIVCLK period (five ECLK cycles).

In Mode B, with SYNCN/$\overline{\text{SYNC1}}$=0 (see Timing Diagram B), the five data words are latched as in Mode A, but the video controls are latched on the rising edge of ECLK. If any video controls are asserted they will remain active for one full ECLK cycle.

4:1 MUX

With DIV4/$\overline{\text{DIV5}}$=1 and SYNCN/$\overline{\text{SYNC1}}$=1 (Mode C; see Timing Diagram C), the IC operates in a 4:1 MUX mode. The four data words A-D and all video controls are latched on the rising edge of DIVCLK. If any video controls are asserted, they remain active for a full DIVCLK cycle (four ECLK cycles).

In Mode D, with SYNCN/$\overline{\text{SYNC1}}$=0 (see Timing Diagram D), the four data words A-D are latched as in Mode C, but the video controls are latched on the rising edge of ECLK. If any video controls are asserted, they remain valid for one full ECLK cycle.

DATA MUX OUTPUT

The data words are sequenced through the MUX in order A-E (A-D for DIV4/$\overline{\text{DIV5}}$=1) and appear at the DOUT port with one clock cycle latency. The DOUT port is limited to data rates of ≤60 MWPS.

RESET CONTROL

For synchronizing multiple DACs in a system, a reset function is provided. Timing Diagrams E and F illustrate the operation of this function. When $\overline{\text{RESET}}$ is asserted low, the MUX will continue to run until the internal state machine reaches State B. Once it reaches State B, Word B will appear at the DAC outputs two clock cycles later and remain for subsequent clock cycles. If $\overline{\text{RESET}}$ is applied to multiple DACs in a system, all DACs will be stopped in State B, thus synchronizing them. When $\overline{\text{RESET}}$ goes high, all DACs will cycle through the remaining latched words (C, D, E; DIV4/$\overline{\text{DIV5}}$=0 and C, D; DIV4/$\overline{\text{DIV5}}$=1) and a new set of data words will be latched on the next rising edge of DIVCLK.

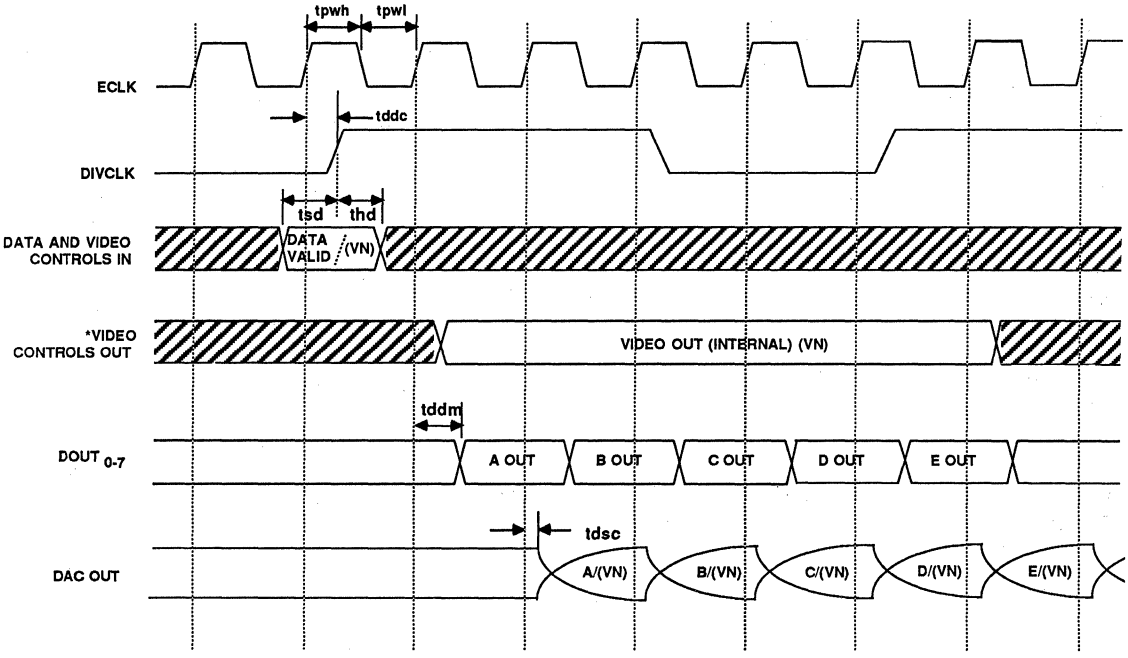
VIDEO CONTROLS

Modes B and D (Timing Diagrams B and D) allow for video controls to be asserted on any pixel boundary while Modes A and C (Timing Diagrams A and C) only allow for the video controls to be asserted at Pixel A for a full DIVCLK cycle.

DAC

The DAC provides 256 shades of gray for displaying video information. SYNC, BLANK, BRighT and Force High are proportional to the DAC gray scale voltage and provide RS-343-A compatible levels when adjusted as shown in Table 1 and Figure 1. Out- is standard video (SYNC down) with negative true logic; all zeroes equal full scale (BLACK). Out+ is inverse video (SYNC up) with positive true logic; all ones equal full scale. Bit 0 of each word is the LSB. The DAC can drive doubly terminated 50 or 75 Ohm loads to RS-343-A levels.

TIMING DIAGRAM A. 5:1 MUX, 5 PIXEL VIDEO CONTROLS (1)

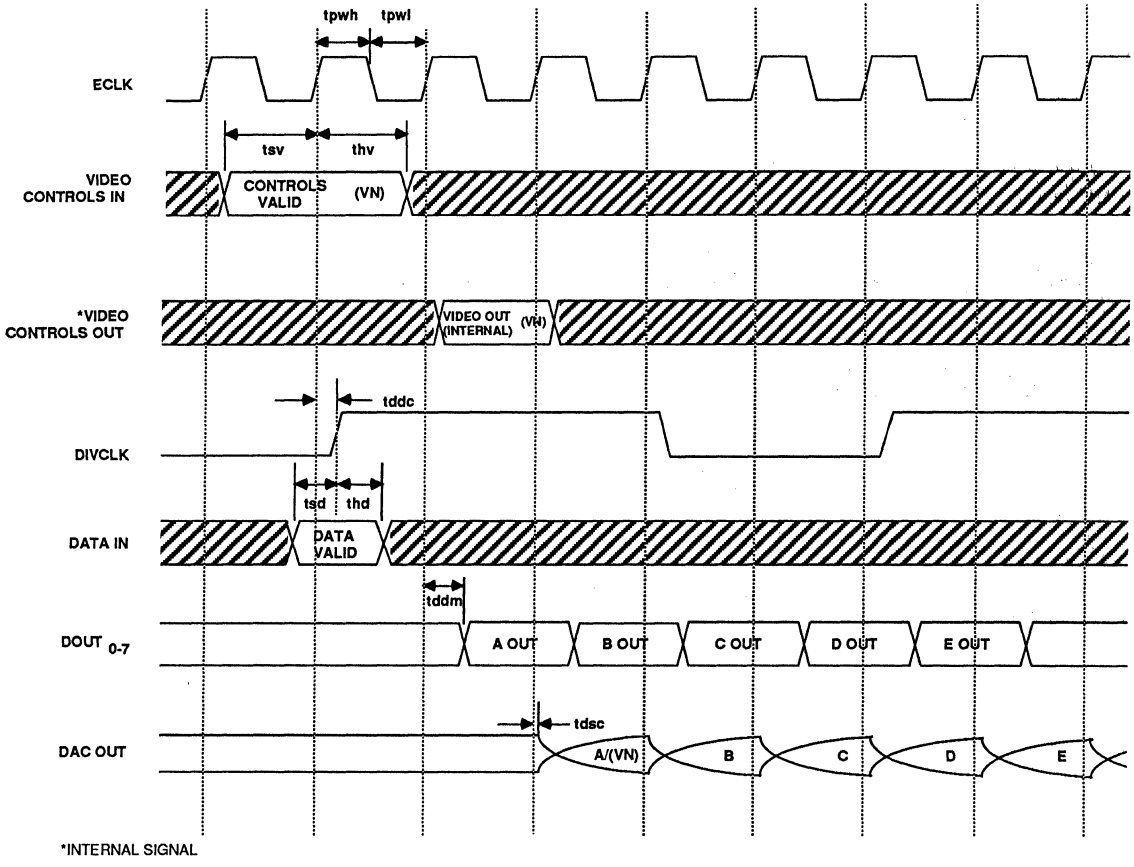


*INTERNAL SIGNAL

(1) DIV4/$\overline{\text{DIV5}}$ = 0; SYNCN/$\overline{\text{SYNC1}}$ = 1

All logic levels measured with respect to +1.4 TTL threshold with the exception of ECLK, which is measured at 0.0V differential.

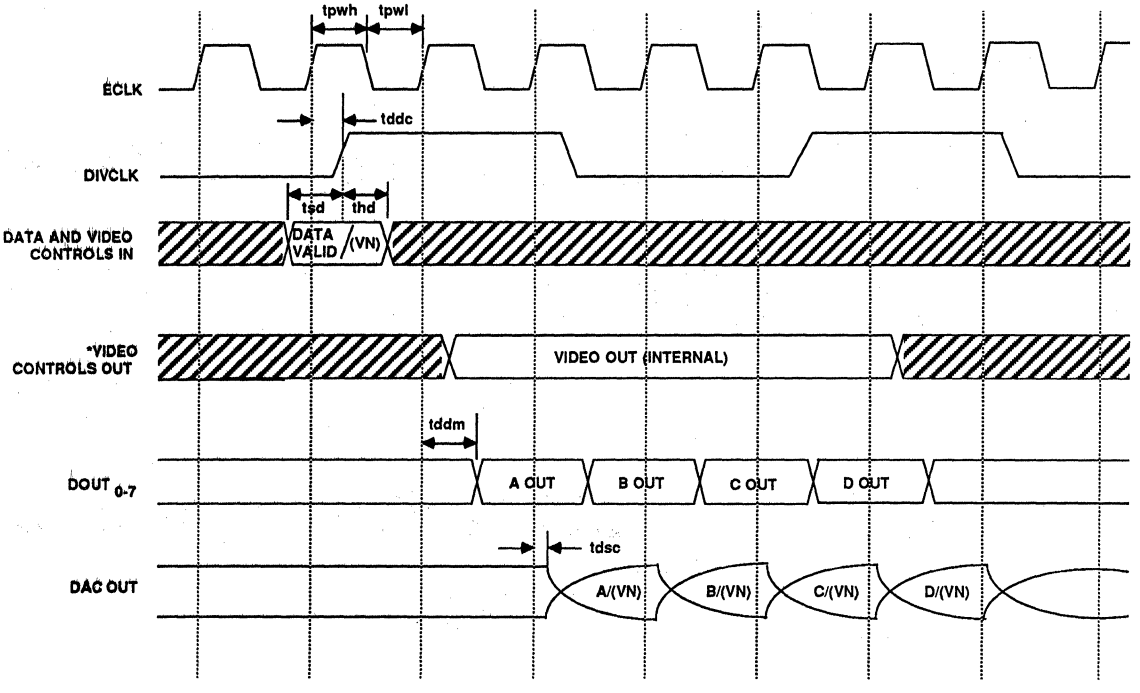
TIMING DIAGRAM B. 5:1 MUX, 1 PIXEL VIDEO CONTROLS (1)



(1) DIV4/$\overline{\text{DIV5}}$ = 0; SYNCN/$\overline{\text{SYNC1}}$ = 0

All logic levels measured with respect to +1.4TTL threshold with the exception of ECLK, which is measured at 0.0V differential.

TIMING DIAGRAM C. 4:1 MUX, 4 PIXEL VIDEO CONTROLS (1)

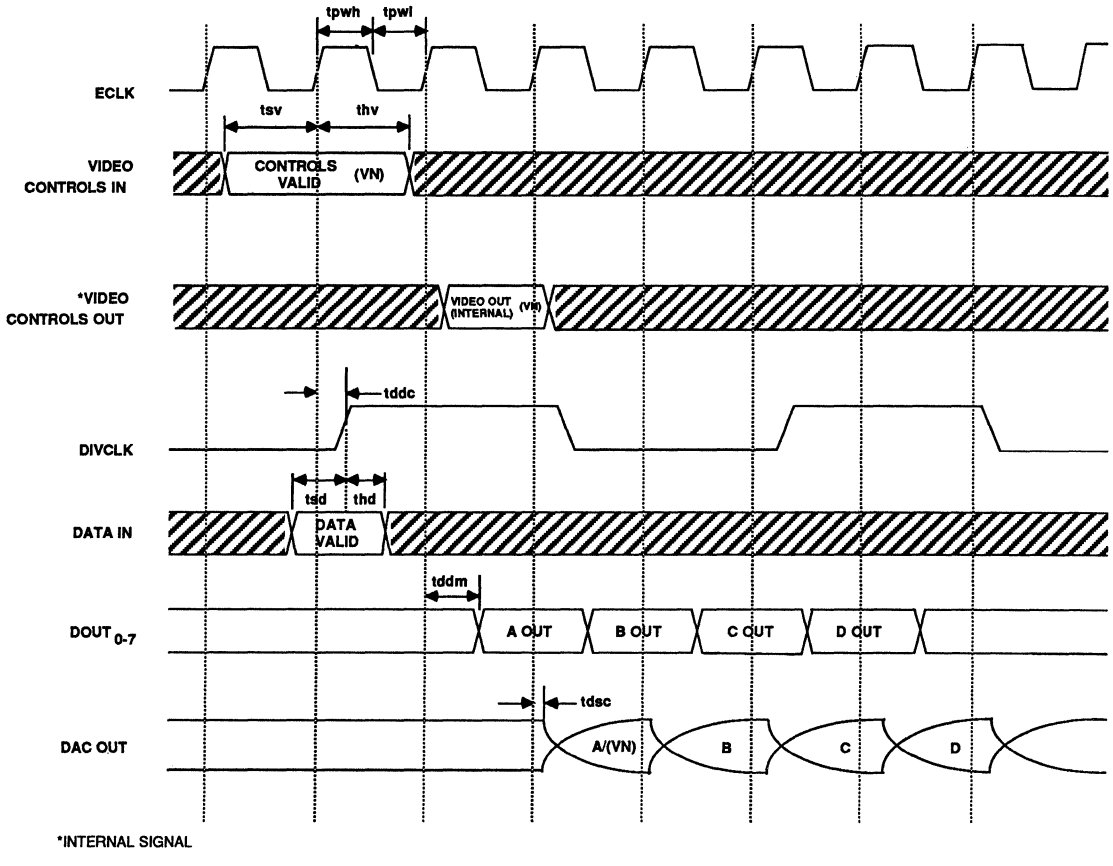


*INTERNAL SIGNAL

(1) DIV4/$\overline{\text{DIV5}}$ = 1; SYNCN/$\overline{\text{SYNC1}}$ = 1

All logic levels measured with respect to +1.4TTL threshold with the exception of ECLK, which is measured at 0.0V differential.

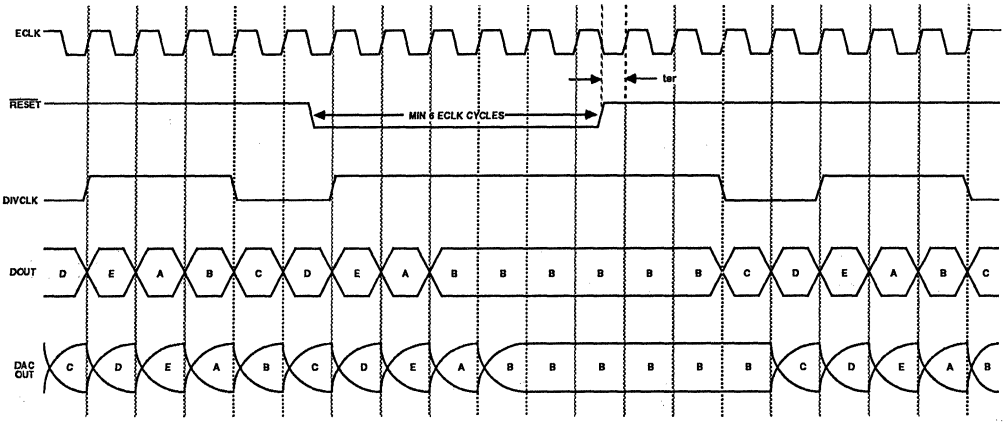
TIMING DIAGRAM D. 4:1 MUX, 1 PIXEL VIDEO CONTROLS (1)



(1) DIV4/$\overline{\text{DIV5}}$ = 1; SYNCN/$\overline{\text{SYNC1}}$ = 0

All logic levels measured with respect to +1.4TTL threshold with the exception of ECLK, which is measured at 0.0V differential.

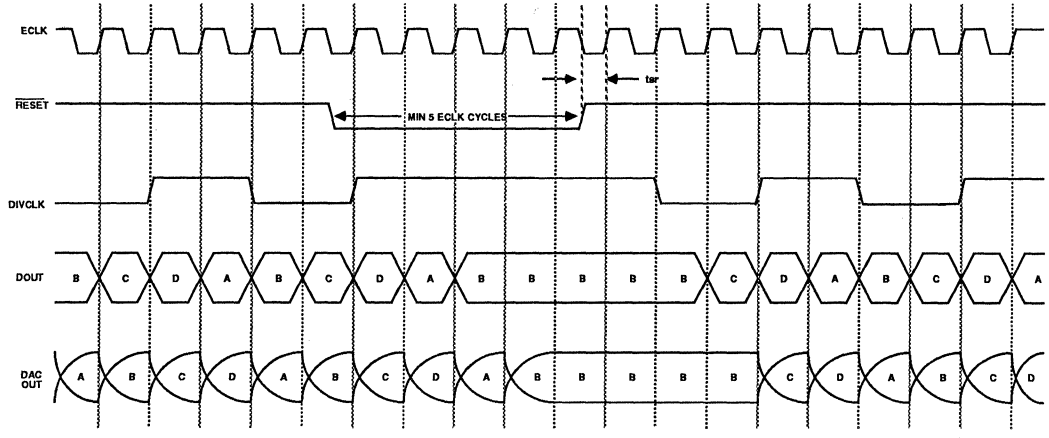
TIMING DIAGRAM E. 5:1 MUX (1)



(1) DIV4/$\overline{\text{DIV5}}$ = 0

All logic levels measured with respect to +1.4TTL threshold with the exception of ECLK, which is measured at 0.0V differential.

TIMING DIAGRAM F. 4:1 MUX (2)



(2) DIV4/$\overline{\text{DIV5}}$ = 1

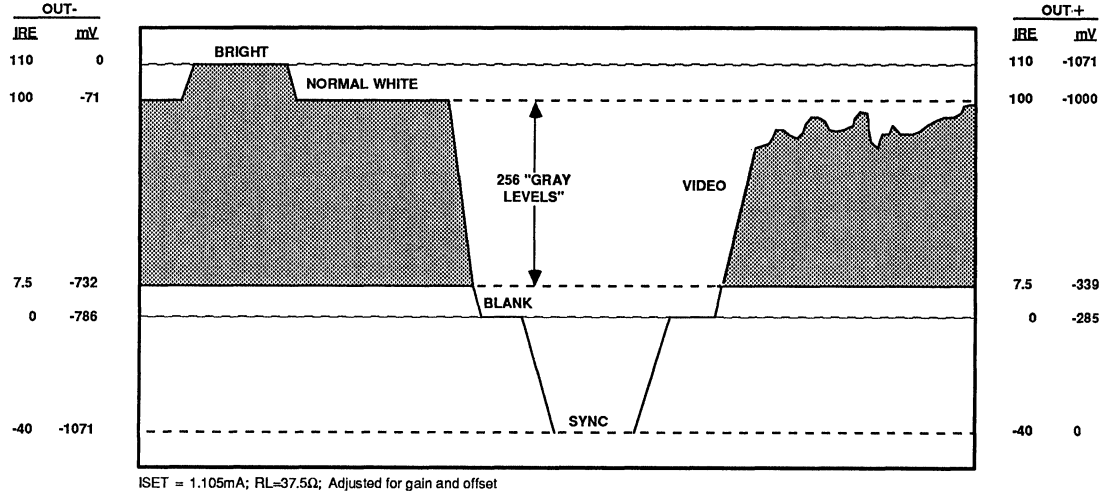
All logic levels measured with respect to +1.4TTL threshold with the exception of ECLK, which is measured at 0.0V differential.

TABLE 1. VIDEO CONTROL OPERATION

SYNC	BLANK	FORCE HIGH	BRIGHT	DATA INPUT	OUT- (mA)	OUT+ (mA)	OUT+,- (IRE)	DESCRIPTION
1	X	X	X	X	28.56	0	-40	SYNC LEVEL
0	1	X	X	X	20.96	7.60	0	BLANK LEVEL
0	0	1	1	X	0.00	28.56	110	BRIGHT
0	0	1	0	X	1.89	26.67	100	NORMAL WHITE LEVEL
0	0	0	0	000...	19.52	9.03	7.5	NORMAL BLACK LEVEL
0	0	0	0	111...	1.89	26.67	100	NORMAL WHITE LEVEL
0	0	0	1	000...	17.63	10.93	17.5	ENHANCED BLACK LEVEL
0	0	0	1	111...	0.00	28.56	110	BRIGHT

ISET = 1.105mA; RL=37.5Ω; Adjusted for gain and offset.

FIGURE 1. VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD



ISET = 1.105mA; RL=37.5Ω; Adjusted for gain and offset

TYPICAL APPLICATIONS

Figure 2 illustrates a typical application circuit for a single HDAC51600. It shows how to terminate the DAC for either 50 or 75 Ohm loads. The DAC outputs are proportional to the reference voltage (internal or external) divided by the sum of R1 and R2. The equation for the DAC gray scale output voltage is:

$$VOUT\ (G.S.) = \frac{VREF}{\propto TR1 + R2}\ (15.9375)\ RL,$$

where
VREF is the reference voltage,
$\propto$ TR1 is the active portion of resistor R1,
RL is the load resistance (R3||R4).

RGB GRAPHICS APPLICATION

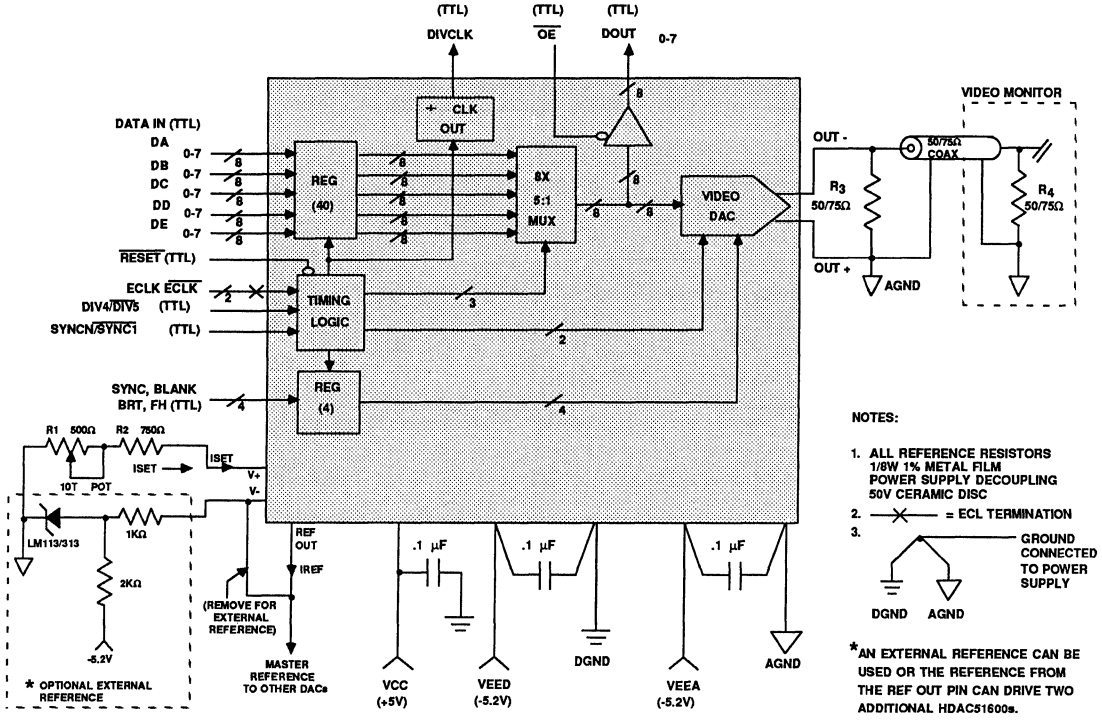
The circuits shown in Figure 4 illustrate how a single HDAC51600 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the reference output.

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference can be used to drive all three D/As in an RGB system to minimize RBG DAC to DAC mismatch.

This may also eliminate the need for individual calibration of each DAC during production assembly. The HDAC51600 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply enough current to drive two other HDAC51600s.

FIGURE 2. TYPICAL APPLICATION CIRCUIT



NOTES:

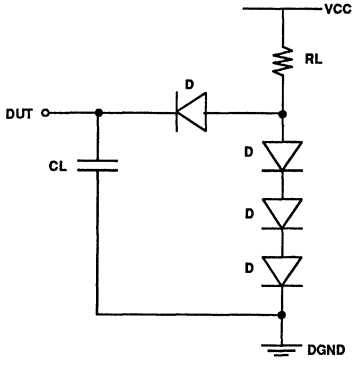
1. ALL REFERENCE RESISTORS 1/8W 1% METAL FILM POWER SUPPLY DECOUPLING 50V CERAMIC DISC
2. = ECL TERMINATION
3. GROUND CONNECTED TO POWER SUPPLY

DGND AGND

*AN EXTERNAL REFERENCE CAN BE USED OR THE REFERENCE FROM THE REF OUT PIN CAN DRIVE TWO ADDITIONAL HDAC51600s.

FIGURE 3. TEST LOADS

DIVCLK/DOUT LOAD



	DIVCLK	DOUT
CL =	15pF	TBD
RL =	260Ω	TBD

D = IN916 OR EQUIVALENT

DAC LOAD

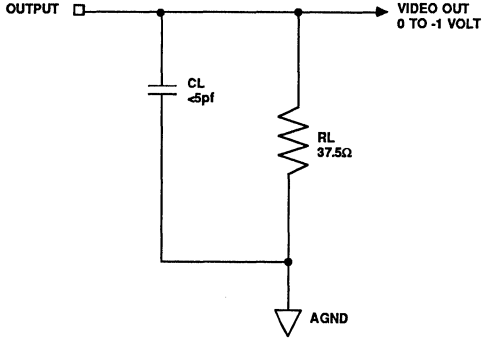
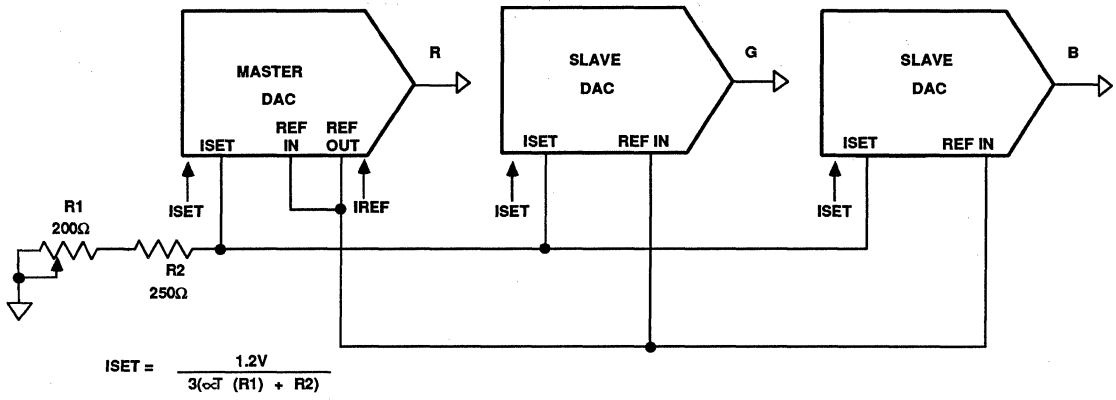


FIGURE 4. TYPICAL RGB GRAPHICS SYSTEM

SINGLE GAIN CONTROL



INDIVIDUAL GAIN CONTROL

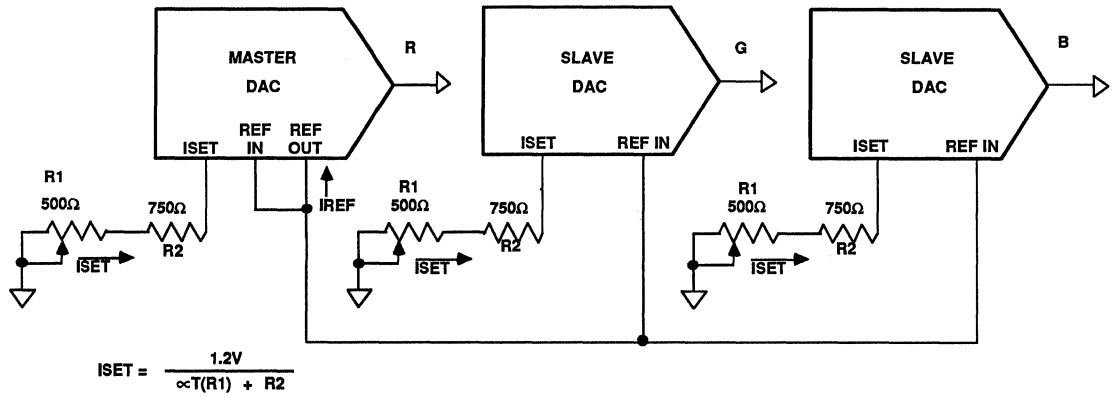


FIGURE 5. ECLK, $\overline{\text{ECLK}}$ SWITCHING LEVELS

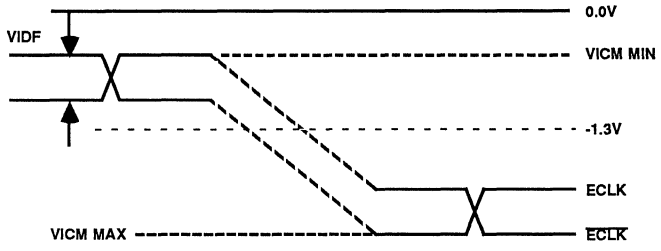


FIGURE 6. EQUIVALENT INPUT CIRCUITS—CLOCK, REFERENCE, DATA AND CONTROLS

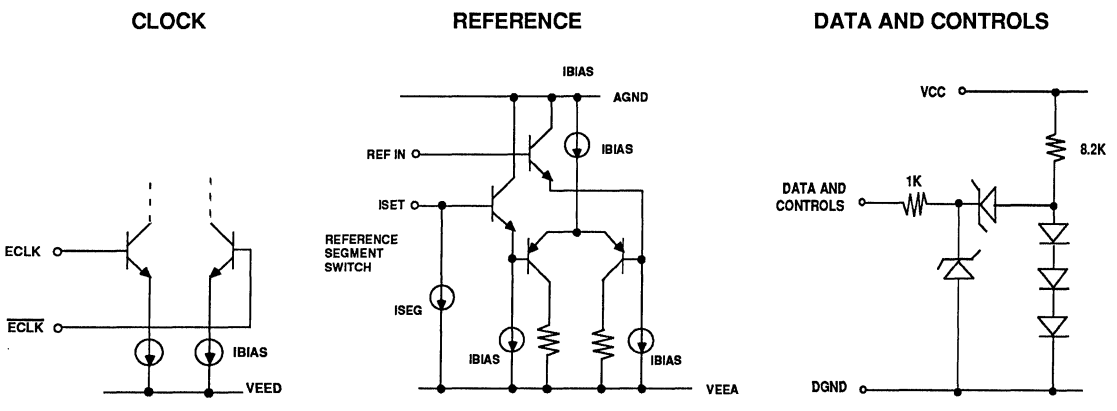
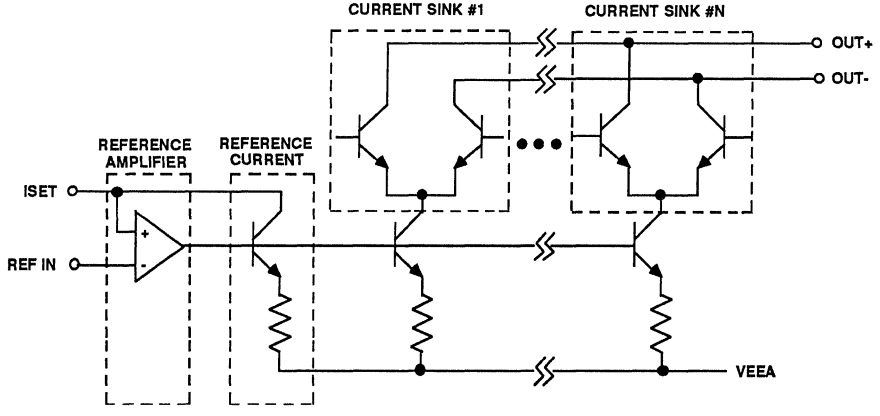
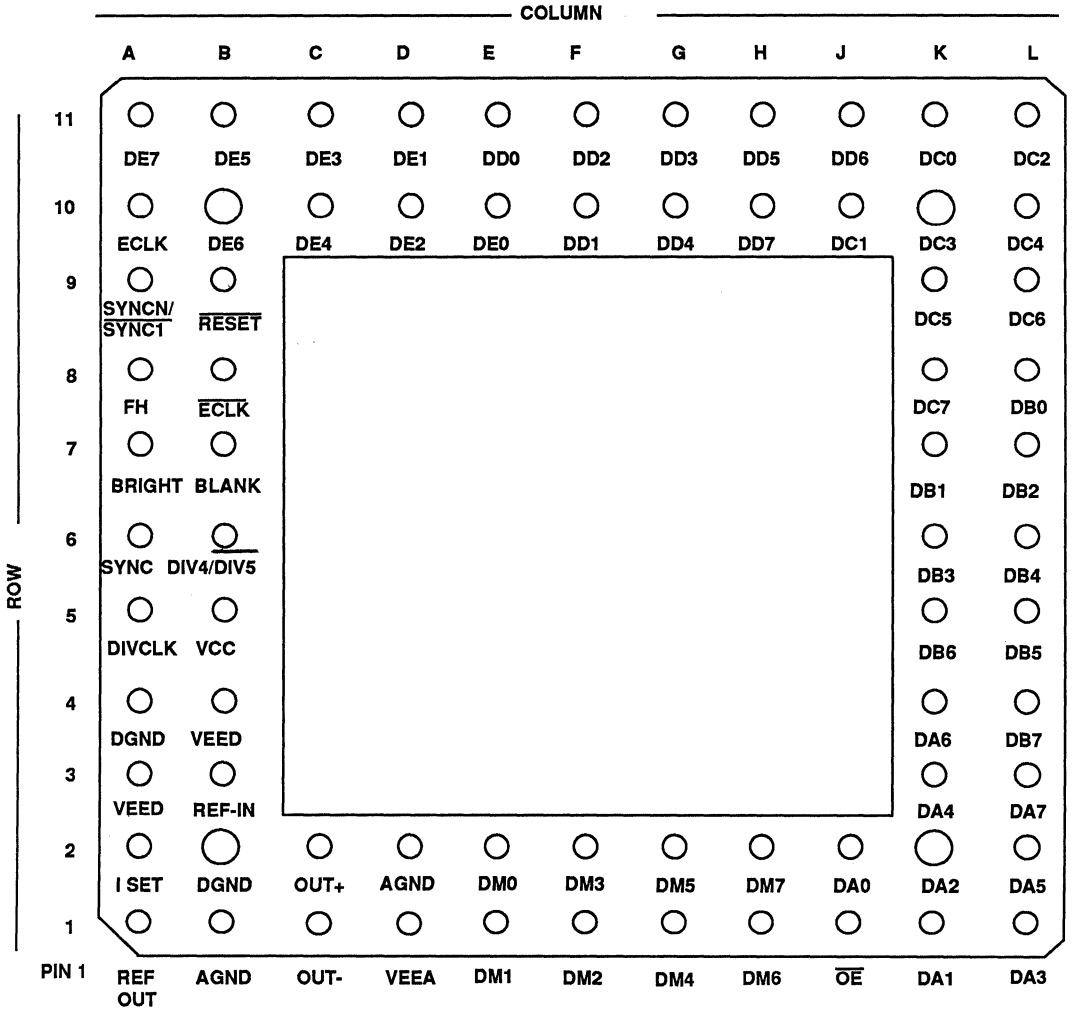


FIGURE 7. EQUIVALENT DAC OUTPUT CIRCUIT



TOP VIEW


COLUMN
A B C D E F G H J K L
ROW
11 DE7 DE5 DE3 DE1 DD0 DD2 DD3 DD5 DD6 DC0 DC2
10 ECLK DE6 DE4 DE2 DE0 DD1 DD4 DD7 DC1 DC3 DC4
9 SYNCN/SYNC1 RESET DC5 DC6
8 FH ECLK DC7 DB0
7 BRIGHT BLANK DB1 DB2
6 SYNC DIV4/DIV5 DB3 DB4
5 DIVCLK VCC DB6 DB5
4 DGND VEED DA6 DB7
3 VEED REF-IN DA4 DA7
2 I SET DGND OUT+ AGND DM0 DM3 DM5 DM7 DA0 DA2 DA5
1 PIN 1 REF OUT AGND OUT- VEEA DM1 DM2 DM4 DM6 OE DA1 DA3

Column	Row	Pin Name	Function
A	1	REF OUT	REFERENCE OUTPUT
A	2	ISET	ISET REFERENCE CURRENT SET
A	3	VEED	NEGATIVE DIGITAL SUPPLY (-5.2V)
A	4	DGND	DIGITAL GROUND (0V)
A	5	DIVCLK	DIVIDED CLOCK OUTPUT
A	6	SYNC	VIDEO SYNC INPUT
A	7	BRIGHT	VIDEO BRIGHT INPUT
A	8	FH	FORCE D/A DATA HIGH INPUT
A	9	SYNCN/$\overline{\text{SYNC1}}$	VIDEO CONTROLS SYNC MODE
A	10	ECLK	ECL CLOCK INPUT
A	11	DE7	INPUT DATA WORD E, BIT 7 (MSB)
B	1	AGND	ANALOG GROUND (0V)
B	2	DGND	DIGITAL GROUND (0V)
B	3	REF IN	REFERENCE INPUT
B	4	VEED	NEGATIVE DIGITAL SUPPLY (-5.2V)
B	5	VCC	POSITIVE DIGITAL SUPPLY (+5.0V)
B	6	DIV4/$\overline{\text{DIV5}}$	DIVIDE SELECT 4 OR 5 (5 ACTIVE LOW)
B	7	BLANK	VIDEO BLANK INPUT
B	8	$\overline{\text{ECLK}}$	ECL CLOCK INPUT, COMPLEMENT
B	9	$\overline{\text{RESET}}$	RESET CONTROL, ACTIVE LOW
B	10	DE6	INPUT DATA WORD E, BIT 6
B	11	DE5	INPUT DATA WORD E, BIT 5
C	1	OUT-	DAC OUTPUT, SYNC DOWN
C	2	OUT+	DAC OUTPUT COMPLEMENT, SYNC UP
C	10	DE4	INPUT DATA WORD E, BIT 4
C	11	DE3	INPUT DATA WORD E, BIT 3
D	1	VEEA	NEGATIVE ANALOG SUPPLY (-5.2V)
D	2	AGND	ANALOG GROUND (0V)
D	10	DE2	INPUT DATA WORD E, BIT 2
D	11	DE1	INPUT DATA WORD E, BIT 1
E	1	DOUT 1	MUX DATA OUT, BIT 1
E	2	DOUT 0	MUX DATA OUT, BIT 0 (LSB)
E	10	DE0	INPUT DATA WORD E, BIT 0 (LSB)
E	11	DD0	INPUT DATA WORD D, BIT 0 (LSB)
F	1	DOUT 2	MUX DATA OUT, BIT 2
F	2	DOUT 3	MUX DATA OUT, BIT 3

Column	Row	Pin Name	Function
F	10	DD1	INPUT DATA WORD D, BIT 1
F	11	DD2	INPUT DATA WORD D, BIT 2
G	1	DOUT 4	MUX DATA OUT, BIT 4
G	2	DOUT 5	MUX DATA DOUT, BIT 5
G	10	DD4	INPUT DATA WORD D, BIT 4
G	11	DD3	INPUT DATA WORD D, BIT 3
H	1	DOUT 6	MUX DATA OUT, BIT 6
H	2	DOUT 7	MUX DATA OUT, BIT 7 (MSB)
H	10	DD7	INPUT DATA WORD D, BIT 7 (MSB)
H	11	DD5	INPUT DATA WORD D, BIT 5
J	1	$\overline{\text{OE}}$	MUX OUT ENABLE, ACTIVE LOW
J	2	DA0	INPUT DATA WORD A, BIT 0 (LSB)
J	10	DC1	INPUT DATA WORD C, BIT 1
J	11	DD6	INPUT DATA WORD D, BIT 6
K	1	DA1	INPUT DATA WORD A, BIT 1
K	2	DA2	INPUT DATA WORD A, BIT 2
K	3	DA4	INPUT DATA WORD A, BIT 4
K	4	DA6	INPUT DATA WORD A, BIT 6
K	5	DB6	INPUT DATA WORD B, BIT 6
K	6	DB3	INPUT DATA WORD B, BIT 3
K	7	DB1	INPUT DATA WORD B, BIT 1
K	8	DC7	INPUT DATA WORD C, BIT 7 (MSB)
K	9	DC5	INPUT DATA WORD C, BIT 5
K	10	DC3	INPUT DATA WORD C, BIT 3
K	11	DC0	INPUT DATA WORD C, BIT 0 (LSB)
L	1	DA3	INPUT DATA WORD A, BIT 3
L	2	DA5	INPUT DATA WORD A, BIT 5
L	3	DA7	INPUT DATA WORD A, BIT 7 (MSB)
L	4	DB7	INPUT DATA WORD B, BIT 7 (MSB)
L	5	DB5	INPUT DATA WORD B, BIT 5
L	6	DB4	INPUT DATA WORD B, BIT 4
L	7	DB2	INPUT DATA WORD B, BIT 2
L	8	DB0	INPUT DATA WORD B, BIT 0 (LSB)
L	9	DC6	INPUT DATA WORD C, BIT 6
L	10	DC4	INPUT DATA WORD C, BIT 4
L	11	DC2	INPUT DATA WORD C, BIT 2

**For Ordering Information See Section 1.*

NOTES:

HDAC52160

16-BIT VOLTAGE-OUTPUT DIGITAL TO ANALOG CONVERTER

ADVANCE INFORMATION

FEATURES:

- 16-Bit Accuracy
- On-Chip Band-Gap Voltage Reference
- On-Chip Application Resistors for Gain Selection
- Settling Time of 100 nS Typical to 16-Bit Accuracy
- -55 to +125°C Operating Temperature
- TTL Input Compatible

APPLICATIONS:

- Automatic Test Equipment
- Digital Attenuators
- Digital Communication Equipment
- Vector Stroke Video Imaging

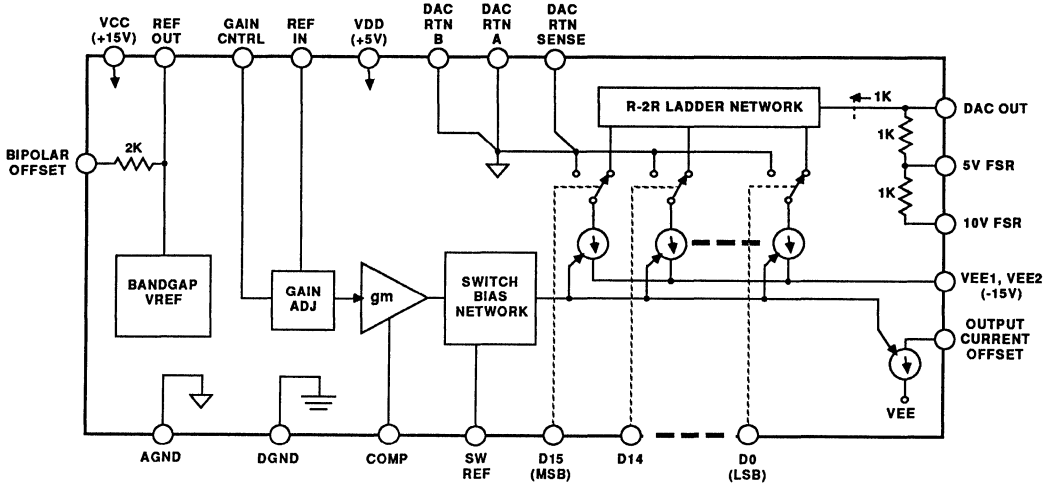
GENERAL DESCRIPTION

The HDAC52160 is a 16-bit voltage-output digital to analog converter. This high-performance monolithic device offers the highest speed/power ratio in the industry. Unique on-chip functions include a band-gap voltage reference and precision application resistors used to support output voltage scaling. Unlike current-output devices, this voltage-output DAC simplifies the task of output buffering.

Several output voltage ranges are available depending on external interconnection of pins IOS, BPO, 5V FSR, and 10V FSR. With respect to an all 0's or all 1's input, these ranges are +10 to 0V, +5 to 0V, +5 to -5V, +2.5 to -2.5V, +15 to +5V or +7.5 to +2.5V.

The HDAC52160 operates with separate ±15V analog supplies and a +5V digital supply to provide maximum noise immunity. All logic input levels are TTL and 5 volt CMOS compatible. The device is manufactured on Honeywell's Advanced Bipolar Linear process. This process process allow the combination of dense, high-speed digital logic with precision analog circuitry on a single chip.

BLOCK DIAGRAM



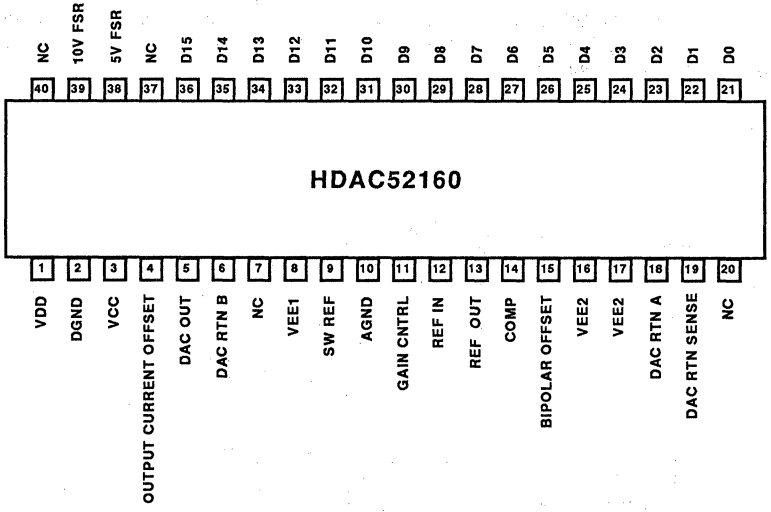
SPECIFICATIONS

Typical at +25°C, VDD = +5V, VEE1 = VEE2 = -15V, VCC = +15V, Unless otherwise specified.

Parameter	Test Conditions	Test Level (1)	HDAC52160 Min	Typ	Max		Units
Resolution		I		16			Bits
Integral Linearity		I		± 1/2			LSB
Differential Linearity Error		I		± 1			LSB
Gain Error		I		± 0.01			% of Full Scale
Gain Error Tempco		I		± 15			ppm/°C
Offset Error		I		± 1			mV
Reference Input Current		I		1			mA
VIH (Logic High Input Voltage)		I	2.4				V
VIL (Logic Low Input Voltage)		I			0.8		V
Output Voltage Settling Time		II		100			nsec
Total Power Dissipation		II		750			mW

(1) Test Procedure: I - Production tested at the specified conditions; II - Sample tested to ensure compliance.

PINOUT



**For Ordering Information See Section 1.*

HDAC7541Z

CMOS, 12 BIT MONOLITHIC MULTIPLYING DAC

PRELIMINARY INFORMATION

FEATURES

- Improved Version of the AD7541A
- Low Output Capacitance (< 75 pf.)
- Maximum Gain Error < 2 LSB (all grades)
- 12 Bit Linearity Over Temperature
- Settling Time = 500 nsecs.
- +5V to +15V operation

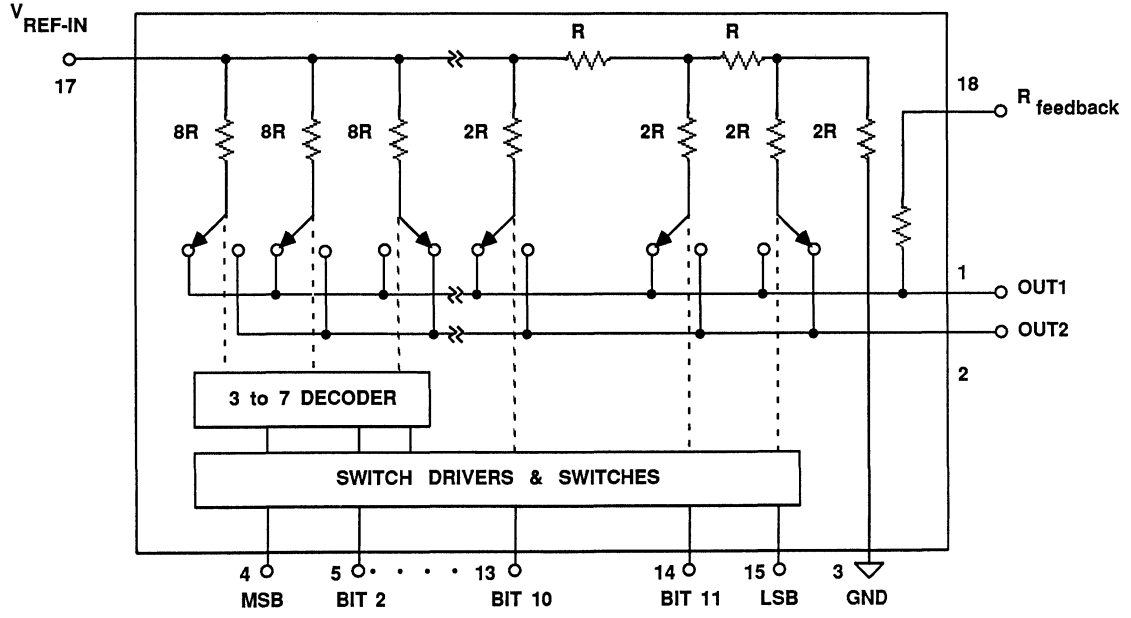
APPLICATIONS

- Gain Control Circuits
- Programmable Gain Amplifiers
- Programmble Filters
- Function Generators
- Digital/Synchro Converters
- Digitally Controlled Attenuation

GENERAL DESCRIPTION

The HDAC7541Z is a monolithic, low cost 12 bit digital to analog converter (DAC). It is compatible with the industry standard 7541A but with significant performance improvements in speed and gain accuracy. The HDAC7541Z is fabricated in a 3 micron, polysilicon gate CMOS process. The excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages

V_{DD} (pin 16) to GND.....+17V
V_{REF} (pin 17) to GND.....±25V

Input Voltages

$V_{feedback}$ (pin 18) to GND.....±25V
Digital Input Voltage to GND (pins 4-15).....-0.3V, V_{DD}

Outputs

V_{pin1}, V_{pin2} to GND.....-0.3V, V_{DD}

Temperature

Operating Temperature, ambient.....-55 to +125°C
junction.....+150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C
Power Dissipation (Any Package) to +75°C.....450mW
Derates above +75°C.....6mW/°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Excessive exposure to absolute maximum ratings may effect device reliability.

   CAUTION - ESD SENSITIVE DEVICE: The logic and analog ports of this device have special circuits to protect it against ESD damage. Although this protection should prevent permanent damage to the inputs, care should be taken in handling.

V_{DD} = 15 volts; V_{REF} = +10volts; V_{PIN1} = V_{PIN2} = 0 volts; T= 25°C unless otherwise noted

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA MIN	HDAC7541ZA NOM	HDAC7541ZA MAX	HDAC7541ZB MIN	HDAC7541ZB NOM	HDAC7541ZB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS									
Accuracy									
Resolution		I	-	12	-	-	12	-	bits
Relative Accuracy	Tmin - Tmax	I	-1/2	±1/4	+1/2	-1		+1	LSB
Differential Nonlinearity	Tmin - Tmax	I	-1/2	±1/4	+1/2	-1		+1	LSB
Gain Error	Using Internal $R_{feedback}$								
	25°C	I	-	-	.75	-	-	1.75	LSB
	Tmin - Tmax	I	-	-	2.0	-	-	3	LSB
Gain Temperature Coefficient	Tmin - Tmax	II	-	0.3	3	-	0.3	3	ppm/°C
Output Leakage									
Pin 1	25°C 0-70°C/-25 to +85°C -55 to + 125°C All digital inputs at 0V	I I I	-5 -10 -200		+5 +10 +200	-5 -10 -200		+5 +10 +200	nA

V_{DD} = 15 volts; V_{REF} = +10volts; V_{PIN1} = V_{PIN2} = 0 volts; T= 25°C unless otherwise noted

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA MIN	HDAC7541ZA NOM	HDAC7541ZA MAX	HDAC7541ZB MIN	HDAC7541ZB NOM	HDAC7541ZB MAX	UNITS
DC ELECTRICAL CHARACTERISTICS									
Output Leakage									
Pin 2	25°C 0-70°C/-25 to +85°C -55 to + 125°C All digital inputs at V_{DD}	I I I	-5 -10 -200		+5 +10 +200	-5 -10 -200		+5 +10 +200	nA
Reference Input Resistence	Pin 17 to GND +25°C Temp. Coefficient	I II	7	12.5 -180	18	7	12.5 -180	18	KΩ ppm/°C
Digital Inputs	Tmin - Tmax								
V_{IH} (High Input Voltage)		I	2.4			2.4			Volts
V_{IL} (Low Input Voltage)		I			0.8			0.8	Volts
I_{IN} (Input Current)		I			1			1	µA
C_{IN} (Input Capacitance)	V_{IN} = 0 Volts	II			8			8	pF
Power Supply									
V_{DD} Range		I	+5	+15	+16	+5	+15	+16	Volts
I_{DD}	25°C Tmin-Tmax / Digital Inputs at V_{IL} or GND	I I			1 1			1 1	mA mA
	25°C Tmin-Tmax / Digital Inputs at V_{DD} or V_{IH}	I I			3 4			3 4	mA mA
PSRR	ΔV_{DD} = ±5%	I	-	±.001	±.005	-	±.001	±.005	(Δgain%)/(ΔV_{DD}%)
AC ELECTRICAL CHARACTERISTICS									
Propagation Delay	From Digital Input to 90% of Output Final Value; Note 3	II	-	50	100	-	50	100	nsecs
Digital to Analog Glitch Impulse	V_{REF} = 0V; Note 2	II	-	200	400	-	200	400	nV-sec

V_{DD} = 15 volts; V_{REF} = +10volts; V_{PIN1} = V_{PIN2} = 0 volts; T= 25°C unless otherwise noted

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA MIN	HDAC7541ZA NOM	HDAC7541ZA MAX	HDAC7541ZB MIN	HDAC7541ZB NOM	HDAC7541ZB MAX	UNITS
AC ELECTRICAL CHARACTERISTICS									
Multiplying Feedthrough Error	V_{REF} to V_{OUT} V_{REF} = ±10 Volts 10KHz Sinewave	II	-	0.3	0.5	-	0.3	0.5	mV(p-p)
Output Current Settling Time	To 0.01% of full scale; Notes 2 & 3	II	-	0.5	1.0	-	0.5	1.0	µsec
Output Capacitance	Tmin-Tmax								
C_{OUT1}	Pin1; Digital Inputs = V_{IH}	II		48	75		48	75	pF
C_{OUT2}	Pin2; Digital Inputs = V_{IH}	II		15	25		15	25	pF
C_{OUT1}	Pin1; Digital Inputs = V_{IL}	II		19	30		19	30	pF
C_{OUT2}	Pin2; Digital Inputs = V_{IL}	II		38	65		38	65	pF

Note 2: Digital inputs change from 0V to V_{DD} or V_{DD} to 0V.
Note 3: OUT1 load: 100Ω + 13pf.
Voltage outputs derived using HOS-50 amplifier.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics that follow are subject to the following conditions:

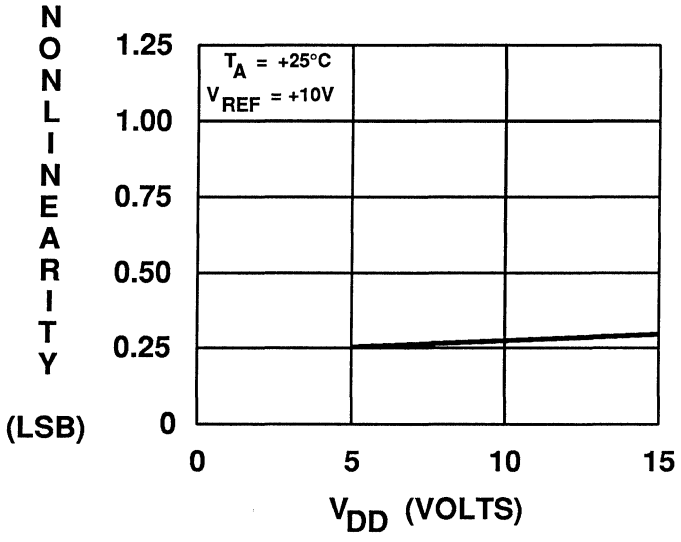
All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

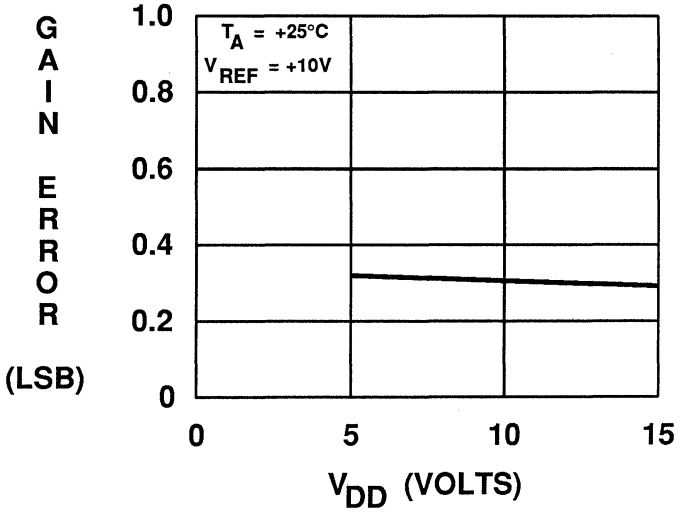
TEST LEVEL	TEST PROCEDURE
I	Production tested.
II	Parameter is guaranteed by sample testing.

TYPICAL PERFORMANCE OVER V_{DD}

NONLINEARITY vs. SUPPLY VOLTAGE



GAIN ERROR vs. SUPPLY VOLTAGE



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential non-linearity of 1LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7541Z ideal full-scale output is -(4095)/(4096)•(V_{REF}). Gain error is adjustable to zero using external trims as shown in Figures 4 and 5.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's or at OUT2 with the DAC loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-secs and is measured with V_{REF}= GND.

CIRCUIT DESCRIPTION

The HADC7541Z operation is best understood from the simplified circuit description in Figure 1. The input V_{REF} is applied to an R-2R ladder network. The R-2R network divides the V_{REF} input by 2 at each stage to produce currents in the 2R legs which decrease by a factor of 2 moving toward the LSB end of the ladder.

The switches on each 2R leg allow this current to be routed to analog ground or through the feedback resistor of the external op-amp on OUT1. This op-amp resistor converts the current to a voltage again. The sum of the selected leg currents forced through $R_{feedback}$ determines the output voltage by the equation in Figure 1.

The op-amp on OUT1 creates a virtual ground point on OUT1 such that the voltage on the 2R legs is ground no matter which positions the current steering switches are in. This makes the input resistance seen by V_{REF} a constant R Ohms.

The HDAC7541Z uses a modification of this R-2R ladder which has the largest 3 bits' current provided by equally weighted resistors rather than binary scaled resistors. This "segmentation" technique improves the linearity and gain accuracy of the HDAC7541Z and lowers the glitch energy during code transitions. This internal structure, however, does not change the way the output code is selected by the user. Therefore, the simplified schematic in Figure 1 is suitable for understanding the operation of the HDAC7541Z.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7541Z is the key to understanding offset, linearity and settling time. Figures 2 and 3 illustrate these effects.

In Figure 2, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin 17 plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 3 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 2.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 2 and 3.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 2 and 3, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

Offset gain = $1 + R_{feedback}/RDAC$

With all code bits LOW:
$RDAC >> R_{feedback}$; offset gain = 1

With all code bits HIGH:
RDAC = 10K Ohms; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, this non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 2 and 3). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 4 and 5). Although all R-2R DAC's have the need for this type of compensation, the HDAC7541Z maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7541Z.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$.

For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 would be:

$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1} = 4$ MHz or C1 = 4 pf.

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7541Z 's low output capacitance comes much closer to fulfilling this goal than most other 7541 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7541Z.

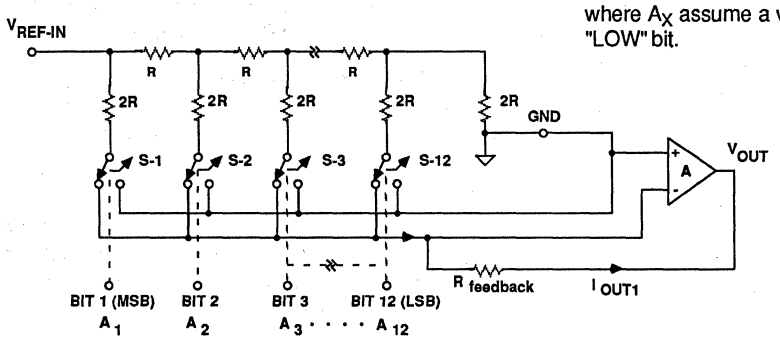
ANALOG/DIGITAL DIVISION

The transfer function for the HDAC7541Z connected in the multplying mode as shown in Figure 1 is:

$$V_O = -V_{IN} \cdot \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots\cdots\cdots \frac{A_{12}}{2^{12}} \right)$$

where A_X assume a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 1
SIMPLIFIED, TYPICAL INTERFACE CIRCUIT



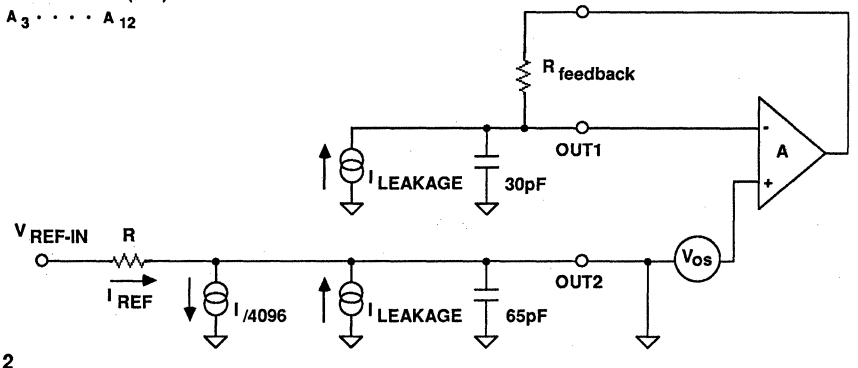


FIGURE 2
HDAC7541Z DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS LOW

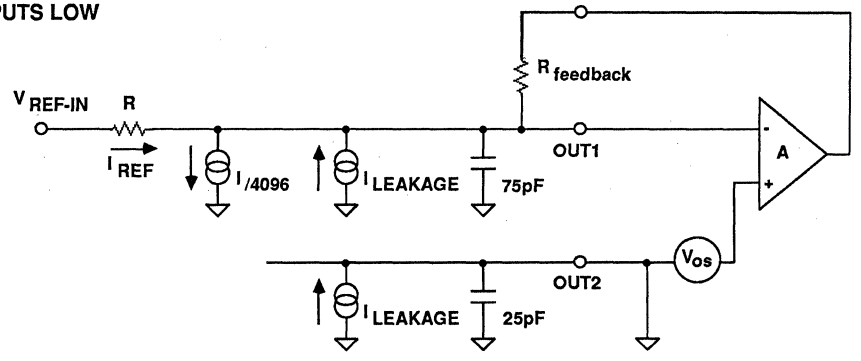


FIGURE 3
HDAC7541Z DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS HIGH

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 4 illustrates the use of the HDAC7541Z in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration.

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC7541Z should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7541Z in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 5. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table 3 for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

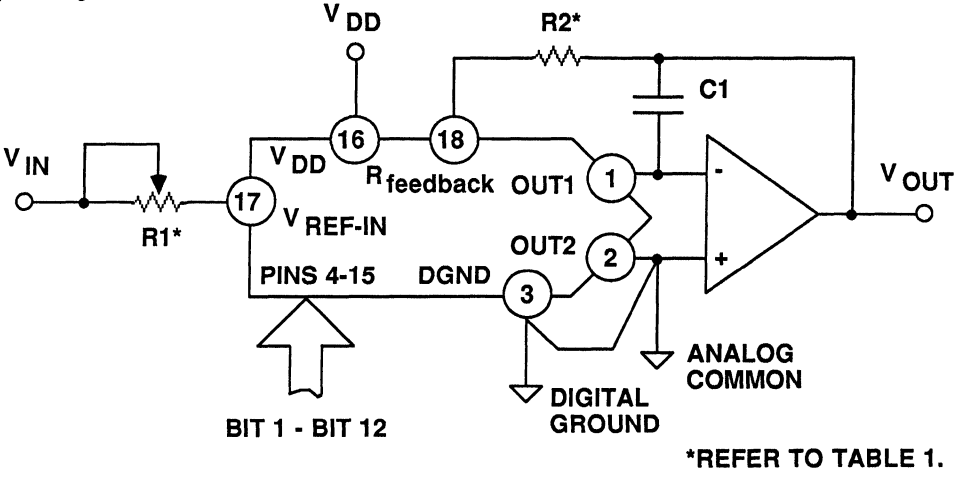


FIGURE 4 UNIPOLAR BINARY OPERATION

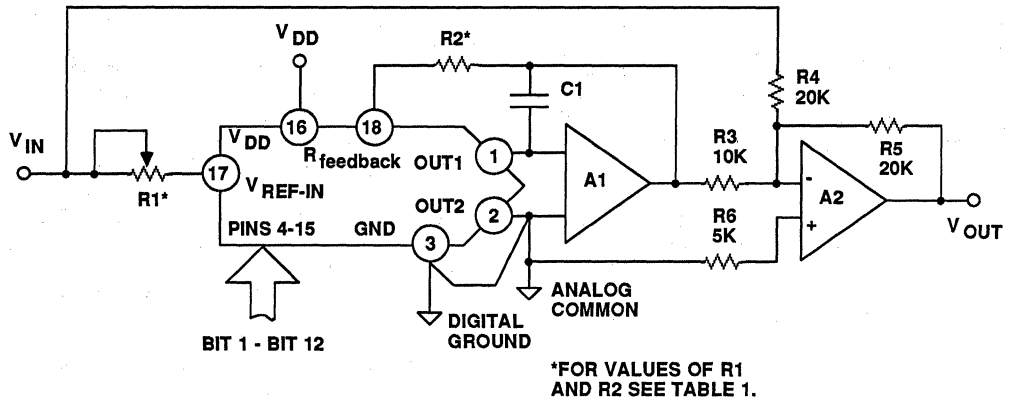


FIGURE 5: BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

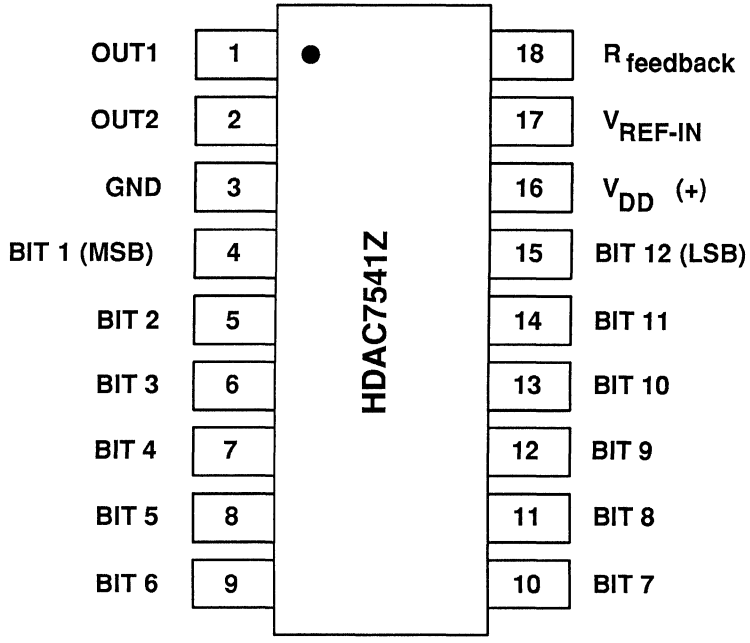
TABLE I: RECOMMENDED TRIM RESISTOR VALUES VS. GRADES

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

TABLE II: UNIPOLAR BINARY CODE TABLE FOR CIRCUIT OF FIGURE 4

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

TABLE III: BIPOLAR CODE TABLE FOR CIRCUIT OF FIGURE 5



PIN ASSIGNMENT HDAC7541Z

PIN	NAME	FUNCTION
1	OUT1	CURRENT OUTPUT 1
2	OUT2	CURRENT OUTPUT 2
3	GND	GROUND
4	BIT 1	DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5	BIT 2	DIGITAL INPUT (BIT 2)
6	BIT 3	DIGITAL INPUT (BIT 3)
7	BIT 4	DIGITAL INPUT (BIT 4)
8	BIT 5	DIGITAL INPUT (BIT 5)
9	BIT 6	DIGITAL INPUT (BIT 6)
10	BIT 7	DIGITAL INPUT (BIT 7)
11	BIT 8	DIGITAL INPUT (BIT 8)
12	BIT 9	DIGITAL INPUT (BIT 9)
13	BIT 10	DIGITAL INPUT (BIT 10)
14	BIT 11	DIGITAL INPUT (BIT 11)
15	BIT 12	DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16	V_{DD}	POSITIVE POWER SUPPLY
17	V_{REF-IN}	REFERENCE INPUT VOLTAGE
18	$R_{feedback}$	INTERNAL FEEDBACK RESISTOR

PIN FUNCTIONS HDAC7541Z

***For Ordering Information See Section 1.*

NOTES:

HDAC7542A

CMOS, 12-BIT, μP BUFFERED DAC

ADVANCE INFORMATION

FEATURES:

- **Improved Version of the AD7542**
- **Maximum Gain Error < 1/2 LSB**
- **12-Bit Linearity Over Temperature**
- **0.5 μsecs. Settling Time**
- Microprocessor Compatible I/O
- 4 Quadrant Multiplication
- Low Gain Drift (<3ppm/°C)

APPLICATIONS:

- μP Gain Control Circuits
- μP Attenuator Control
- μP Controlled Function Generators
- Bus Structured Instrumentation
- Process Controllers
- Industrial Controllers

GENERAL DESCRIPTION

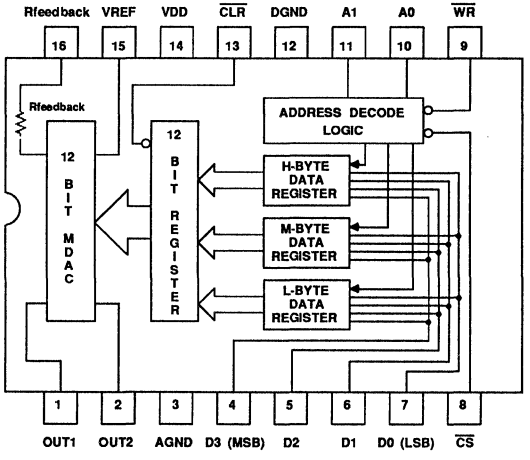
The HDAC7542A is a monolithic, low cost, multiplying 12-bit digital to analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7542 but with significant performance improvements in speed and gain accuracy.

The HDAC7542A is fabricated in a 3 micron, polysilicon gate CMOS process. The excellent linearity and gain accuracy over temperature are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes to prevent latch-up.

The data bits for selecting the DAC output are written into the HDAC7542A via a direct connection to the parallel bus of a microprocessor. Data bytes are written as 3, 4 bit groups or "nibbles" into the data registers on the chip. The input bits are double buffered on-chip. Updating the analog output is controlled via the parallel bus by writing to the chip. A clear pin ($\overline{CLR}$) allows for resetting the output to all zeros under power up or system reset conditions. All address decoding for writing to the chip registers is handled on the chip.

The HDAC7542A's direct parallel bus interconnect makes it an excellent choice for microprocessor-based instruments and industrial or process controllers utilizing microprocessors.

BLOCK DIAGRAM



VDD = +5V; VREF = +10V; VOUT1 = VOUT2 = 0V

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G MIN	HDAC7542AA/G NOM	HDAC7542AA/G MAX	HDAC7542AA MIN	HDAC7542AA NOM	HDAC7542AA MAX	HDAC7542AB MIN	HDAC7542AB NOM	HDAC7542AB MAX	UNITS
CHARACTERISTICS: The following specifications are guaranteed over the full temperature range, unless otherwise specified.												
Relative Accuracy		I	-1/2		+1/2	-1/2		+1/2	-1		+1	LSB
Differential Nonlinearity		I	-1/2		+1/2	-1/2		+1/2	-1		+1	LSB
Gain Error	25°C	I	-1/2		+1/2	-2		+2	-3		+3	LSB
	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Output Settling Time	OUT1 Load = 100Ω + 13pF	II		0.5			0.5			0.5		µsec
Output Capacitance on OUT1	All Register Bits Low	II			30			30			30	pF
	All Register Bits High	II			75			75			75	pF
t_{DS}: Data Set-up Time		I	20			20			20			nsec
t_{DH}: Data Hold Time		I	20			20			20			nsec
t_{WR}: WR Pulse Width		I	40			40			40			nsec

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.
II	Parameter is guaranteed by sample characterization data.

**For Ordering Information See Section 1.*

HDAC7543A

CMOS, 12 BIT, SERIAL INPUT, BUFFERED MULTIPLYING DAC

ADVANCE INFORMATION

FEATURES:

- **Improved Version of the AD7543**
- **Maximum Gain Error < 1/2 LSB**
- **Low Output Capacitance (< 75 pf.)**
- **0.5 μsecs. Settling Time**
- 12-Bit Linearity Over Temperature
- Serial Data load With Flexible Strobe Conditions

APPLICATIONS:

- Industrial and Process Controllers
- Proportional Controllers Requiring Serial Isolation or Remote Location

GENERAL DESCRIPTION

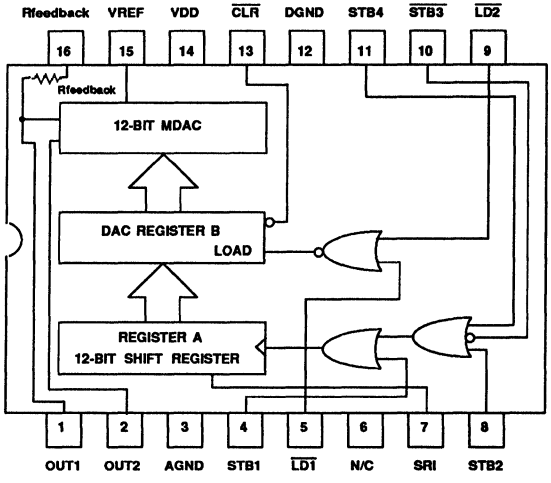
The HDAC7543A is a monolithic, low cost, multiplying12-bit digital to analog converter (DAC) designed for serial digital input. It is compatible with the industry standard 7543 but with significant performance improvements in speed and gain accuracy.

The HDAC7543A is fabricated in a 3 micron, polysilicon gate CMOS process. The excellent linearity and gain accuracy over temperature are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes to prevent latch-up.

The data bits for selecting the DAC output are written into the HDAC7543A via a serial data port prior to latching them into the output register. The input bits are double buffered on-chip. The serial bus control pins provide a great deal of flexibility in providing the serial input strobe conditions for the data transfer. A clear pin ($\overline{CLR}$) allows for resetting the output to all zero's under power up or system reset conditions.

The HDAC7543A's direct serial data interconnect makes it an excellent choice for industrial or process controllers which require electrical isolation or remote location. The serial bus minimizes the number of control lines which would require isolation devices or line drivers in these types of applications.

BLOCK DIAGRAM



VDD = +5V; VREF = +10V; VOUT1 = VOUT2 = 0V

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN	HDAC7543AA/G NOM	HDAC7543AA/G MAX	HDAC7543AA MIN	HDAC7543AA NOM	HDAC7543AA MAX	HDAC7543AB MIN	HDAC7543AB NOM	HDAC7543AB MAX	UNITS
CHARACTERISTICS: The following specifications are guaranteed over the full temperature range, unless otherwise specified.												
Relative Accuracy		I	-1/2		+1/2	-1/2		+1/2	-1		+1	LSB
Differential Nonlinearity		I	-1/2		+1/2	-1/2		+1/2	-1		+1	LSB
Gain Error	25°C	I	-1/2		+1/2	-2		+2	-3		+3	LSB
	Tmin - Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Output Settling Time	OUT1 Load = 100Ω +13pF	II		0.5			0.5			0.5		µsec
Output Capacitance on OUT1	Reg B = all LOW	II			30			30			30	pF
	Reg B = all HIGH	II			75			75			75	pF
t_{SR1}: Data Strobe Pulse Width		I	80			80			80			nsec
$t_{DS3, 4}$: Data Set-up Time on STB 3, 4		I	0			0			0			nsec
$t_{DH3, 4}$: Data Hold Time on STB 3, 4		I	80			80			80			nsec

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.
II	Parameter is guaranteed by sample characterization data.

**For Ordering Information See Section 1.*

HDAC7545A

CMOS 12-BIT BUFFERED MULTIPLYING DAC

PRELIMINARY INFORMATION

FEATURES:

- Improved Version of the AD7545
- **Maximum Gain Error < 2 LSB**
- **Low Output Capacitance (< 75 pf.)**
- **500 ns Settling Time**
- 12-Bit Linearity Over Temperature
- 8 or 16-Bit Bus Compatible

APPLICATIONS:

- µP Controlled Gain Circuits
- µP Controlled Function Generation
- Bus Structured Instruments
- µP Based Control Systems

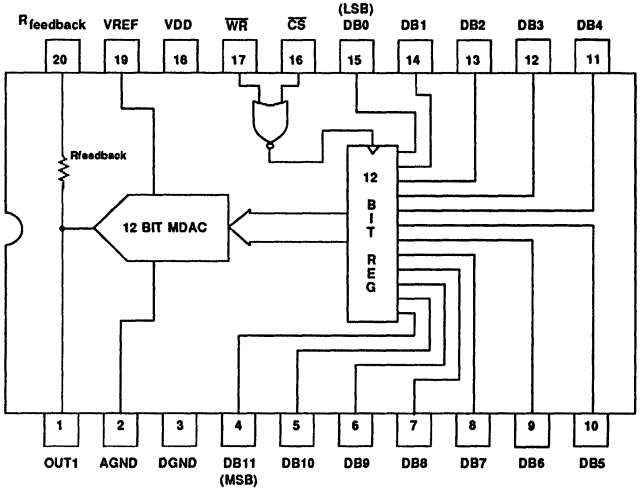
GENERAL DESCRIPTION

The HDAC7545A is a monolithic, low cost, multiplying 12-bit digital to analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7545 but has significant performance improvements in speed and gain accuracy. The HDAC7545A is fabricated in a 3 micron, polysilicon gate BEMOS process and operates from a single +5 volt (maximum) supply. Excellent linearity and gain accuracy are acheived through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base; this eliminates the need for external Schottky clamping diodes for latch-up protection.

The HDAC7545A incorporates a parallel loading architecture for the DAC conversion bits. When pins $\overline{CS}$ and $\overline{WR}$ are low, the twelve input data registers read the bus data. This single load and convert operation allows one-cycle updating by 16-bit microprocessors.

With direct parallel bus data loading, the HDAC7545A is ideally suited for microprocessor-based instruments and industrial or process controllers.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
V_{DD} to DGND..... +7V
AGND to DGND.....-0.3 to VDD

Input Voltages
Digital Inputs to DGND.....-0.3 to VDD
VRfeedback or VREF to DGND..... ±25V

Outputs
V_{OUT1} to GND.....-0.3V to VDD

Temperature
Operating Temperature, ambient.....-55 to +125°C
junction..... +150°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to+150°C
Power Dissipation (Any Package) to +75°C.....450mW
(derates above 75°C by 6 mW/°C)

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

2. CAUTION - ESD SENSITIVE DEVICE: The logic and analog ports of this device have special circuits to protect it against ESD damage. Although this protection should prevent permanent damage to the inputs, care should be taken in handling.

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G			HDAC7545AA			HDAC7545AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY												
Resolution		I	-	12	-	-	12	-	-	12	-	bits
Relative Accuracy		I	-1/2	±1/4	+1/2	-1/2		+1/2	-1		+1	LSB
Differential Nonlinearity		I	-1/2	±1/4	+1/2	-1/2		+1/2	-1		+1	LSB
Gain Error, Using $R_{feedback}$	25°C	I	-1/2		+1/2	-2		+2	-3		+3	LSB
Gain Error, Using $R_{feedback}$	Tmin – Tmax	I	-1.5		+1.5	-3		+3	-4		+4	LSB
Gain Temperature Coefficient		II		0.3	3		0.3	3		0.3	3	ppm/°C

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G MIN	HDAC7545AA/G TYP	HDAC7545AA/G MAX	HDAC7545AA MIN	HDAC7545AA TYP	HDAC7545AA MAX	HDAC7545AB MIN	HDAC7545AB TYP	HDAC7545AB MAX	UNITS
OUTPUT LEAKAGE (3)												
Pin OUT1	25°C	I	-5		+5	-5		+5	-5		+5	nA
Pin OUT1 Military Grades		I	-100		+100	-100		+100	-100		+100	nA
Pin OUT1 Other Grades		I	-10		+10	-10		+10	-10		+10	nA
INPUT RESISTANCE												
Input VREF	Pin 19 to GND 25°C	I	7	12.5	18	7	12.5	18	7	12.5	18	KΩ
Input VREF Temp. Coefficient		II		-180			-180			-180		ppm/°C
LOGIC INPUTS												
V_{IH} (High input voltage)		I	2.4			2.4			2.4			Volts
V_{IL} (Low input voltage)		I			0.8			0.8			0.8	Volts
I_{IN} (Input current)		I			1			1			1	µA
C_{IN} (Input capacitance) of Pins DB0 - DB11, $\overline{WR}$, $\overline{CS}$	V_{IN} = 0V	II			5			5			5	pF
POWER SUPPLY												
I_{DD}	All Logic Inputs at VIL or VIH	I			4			4			4	mA
I_{DD}	Logic Inputs at 0V or VDD,25°C	I		10	100		10	100		10	100	µA
I_{DD}	Logic Inputs at 0V or VDD	I			500			500			500	µA

NOTE 3. Digital inputs $\overline{WR}$ and $\overline{CS}$ at 0 volts.

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = 0V, AGND = DGND,
T_A = 0 to 70°C for Commercial Grade Units,
T_A = -25 to 85°C for Industrial Grade Units,
T_A = -55 to125°C for Military Grade Units
(Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G			HDAC7545AA			HDAC7545AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Digital to Analog Glitch Impulse	VREF = AGND Note 4	II		200	400		200	400		200	400	nV-sec
Multiplying Feedthrough Error	Note 5	II		.3	.5		.3	.5		.3	.5	mVPP
C_{OUT} (Output Capacitance)	DB0-11=0V $\overline{WR}$=$\overline{CS}$=0V	II			30			30			30	pF
C_{OUT} (Output Capacitance)	DB0-11=VDD $\overline{WR}$=$\overline{CS}$=0V	II			75			75			75	pF
Output Current Settling Time	Note 4, 6	II		0.5	1		0.5	1		0.5	1	µsec.
Propagation Delay	Note 7	II		50	100		50	100		50	100	nsec.
t_{CS} (Chip select set-up time)		I	60			60			60			nsec.
t_{CH} (Chip select hold time)		I	0			0			0			nsec.
t_{WR} ($\overline{WR}$ pulse width)	$t_{CS} \geq t_{WR}$	I	100			100			100			nsec.
t_{DS} (Data set-up time)		I	50			50			50			nsec.
t_{DH} (Data hold time)		I	9			9			9			nsec.

NOTES: 4. Load on Pin OUT1 = 100 Ω + 13 pF.
5. VREF = ±10 V @ 10 KHz Sinewave.
6. Measured from falling edge of $\overline{WR}$.
7. Measured from falling edge of $\overline{WR}$ to 90% of final output value.

ELECTRICAL CHARACTERISTICS TESTING

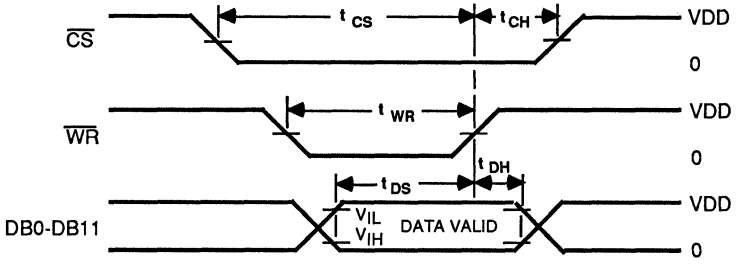
All electrical characteristics are subject to the following conditions:

Parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	Production tested.
II	Parameter is guaranteed by sample testing.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:

$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data inputs DB0-DB11.

HOLD MODE:

Either $\overline{CS}$ or $\overline{WR}$ high, data inputs DB0-DB11 are locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumes high state.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7545A ideal full-scale output is -(4095)/(4096)•(VREF). Gain error is adjustable to zero using external trims as shown in Figures 6 and 7 and Table I.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the VREF terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-secs and is measured with VREF= GND.

GENERAL CIRCUIT DESCRIPTION

As shown in the Block Diagram of the cover sheet, the HDAC7545A consists of a 12-bit multiplyng DAC and a 12-bit data latch. Data at pins DB0 - DB11 is latched when both pins $\overline{CS}$ and $\overline{WR}$ are low. Current latched data establishes the digital-to-analog conversion code, therefore, conversion is actually controlled by pins $\overline{CS}$ and $\overline{WR}$. This is further described in the Interface Logic section.

Figure 1 shows a simplified version of the 12-bit multiplyng DAC circuitry. Note that the HDAC7545A

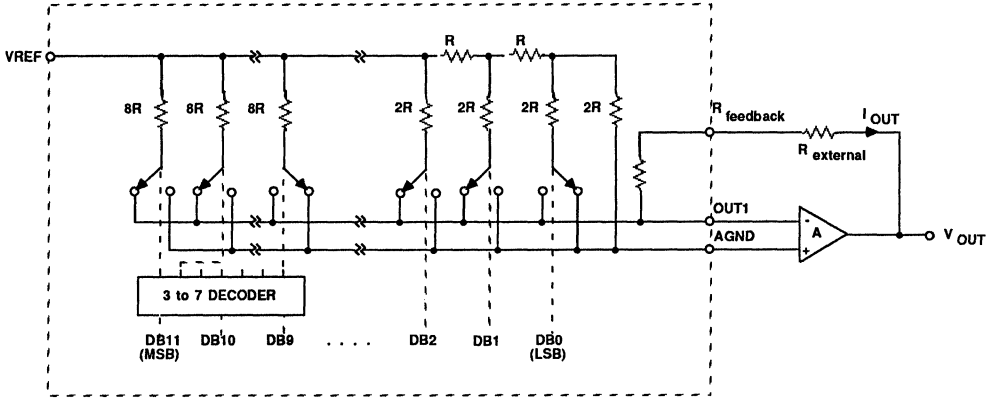


FIGURE 1 SIMPLIFIED HDAC7545A DAC CIRCUITRY
(WITH EXTERNAL OP AMP)

uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7545A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the (remaining) VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switch routes the bit-weighted current of the leg to either analog ground or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the 3 most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7545A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor of Figure 1 in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance, maintains OUT1 at virtual ground. The transfer function of Figure 2 shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed understanding of the circuit operation and performance aspects are found in the following Equivalent Circuit Analysis section.

EQUIVALENT CIRCUIT ANALYSIS

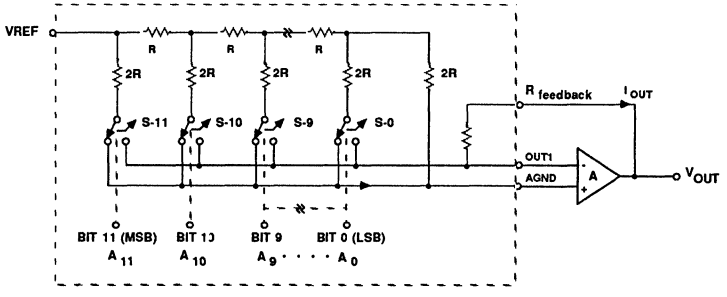
The equivalent output circuit of the HDAC7545A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to pin OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7545A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin VREF plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 3 and 4.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 3 and 4, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below: (next page)



The transfer function for the equivalent network shown is:

$$V_{OUT} = -VREF \cdot \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \cdots \frac{A_0}{2^{12}} \right)$$

where A_X assumes a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 2 EQUIVALENT R-2R RESISTOR NETWORK FOR THE HDAC7545A DAC CIRCUITRY
(WITH EXTERNAL OP AMP)

FIGURE 3
HDAC7545A DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS LOW
(WITH EXTERNAL OP AMP)

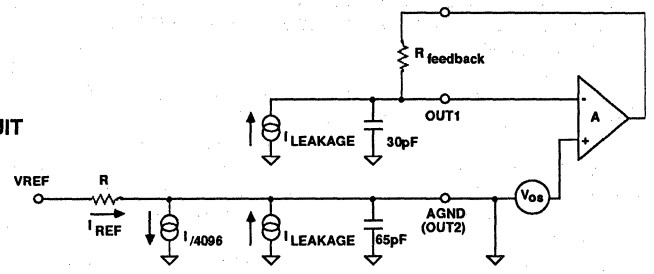
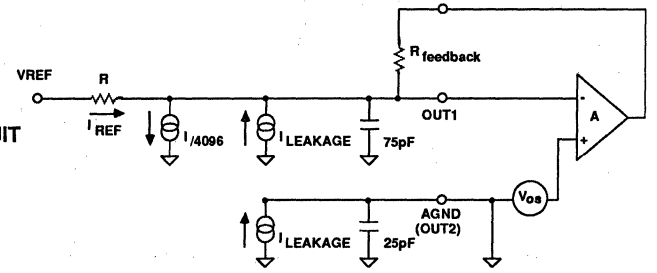


FIGURE 4
HDAC7545A DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS HIGH
(WITH EXTERNAL OP AMP)



Offset gain = 1 + $R_{feedback}$/RDAC

With all code bits LOW:
RDAC >> $R_{feedback}$; offset gain = 1

With all code bits HIGH:
RDAC = $R_{feedback}$; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code inputs. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, the non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation, the HDAC7545A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7545A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.

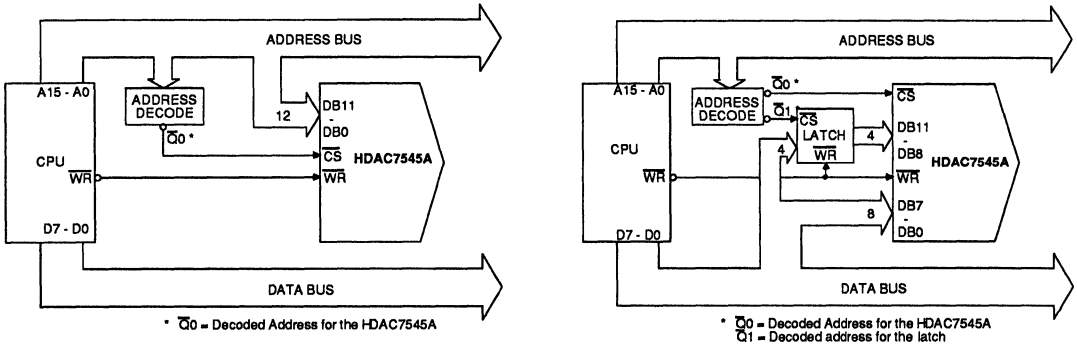
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.

- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$.

For an OP-27 used as an output op-amp with an 8 MHz gain-bandwidth, the choice of C1 would be:

$$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1} = 4\,MHz,$$
$$\text{or } C1 \approx 4\,pf \qquad (R_{feedback} \approx 12.5\,K\Omega)$$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7545A 's low output capacitance comes much closer to fulfilling this goal than most other 7545 compatible DAC's. Thus, faster, more well controlled settling is obtained with the HDAC7545A.



MULTIPLEXED BUS ARCHITECTURE

SEPARATE ADDRESS/DATA BUS ARCHITECTURE

FIGURE 5 TYPICAL MICROPROCESSOR BUS INTERFACES FOR HDAC7545A

3

INTERFACE LOGIC

The HDAC7545A is designed to allow control of the output via a parallel microprocessor bus I/O. This section describes operation of the interface controls to accomplish this.

A typical parallel bus I/O configuration is shown in figure 5 . The microprocessor provides the DAC code as well as all control signals to load the code and update the analog output. During loading the HDAC7545A accepts the DAC input code in a 12 bit word.

When the $\overline{CS}$ pin is at logic "0", the input register of the HDAC7545A is enabled. The $\overline{WR}$ input actually stobes the input data from the parallel bus into the HDAC7545A data register. This occurs on the falling edge of this $\overline{WR}$ pulse. The Write Timing Diagram of page 4 defines the minimum set-up and hold times required by the control lines to successfully transfer data in this fashion.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 6 illustrates the use of the HDAC7545A in a unipolar (or 2 quadrant multiplication) mode. The VREF is applied from pin 19 to ground voltage or an input current can be applied to pin 19. Positive or negative voltages/currents can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the VREF voltage out. If the source of VREF is adjustable, VREF could be directly adjusted for full scale calibration (refer to table II).

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

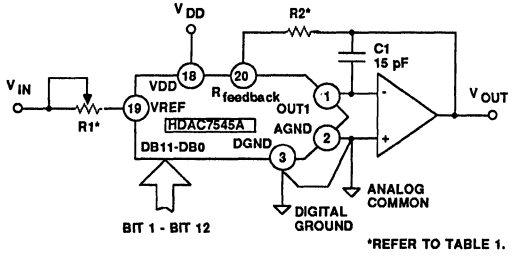


FIGURE 6 UNIPOLAR BINARY OPERATION

The op-amp used with the HDAC7545A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7545A in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 7. The VREF is applied from pin 19 to ground voltage or an input current can be applied to pin 19. Positive or negative voltages/currents can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of VREF to produce a maximum output which is half of VREF in either polarity (see Table 3 for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the VREF source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate for OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

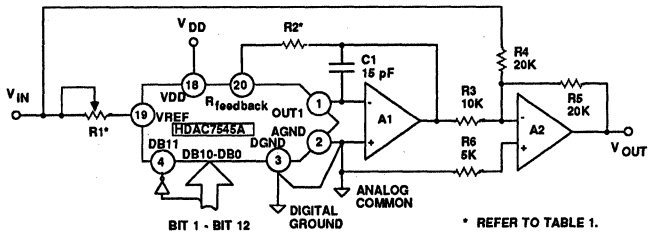


FIGURE 7 BIPOLAR OPERATION

TRIM RESISTOR	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

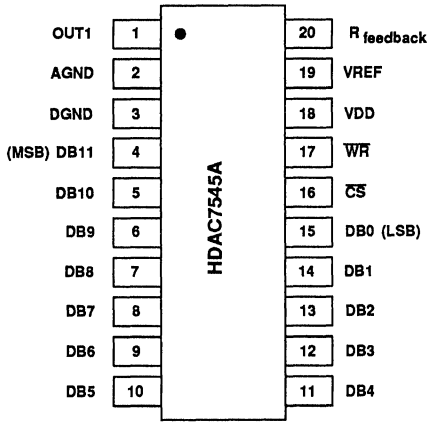
TABLE I
RECOMMENDED TRIM RESISTANCE

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

TABLE II
UNIPOLAR BINARY CODE
FOR CIRCUIT OF FIGURE 6

BINARY NUMBER IN DAC MSB		LSB	ANALOG OUTPUT, V_{OUT}
1111	1111	1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

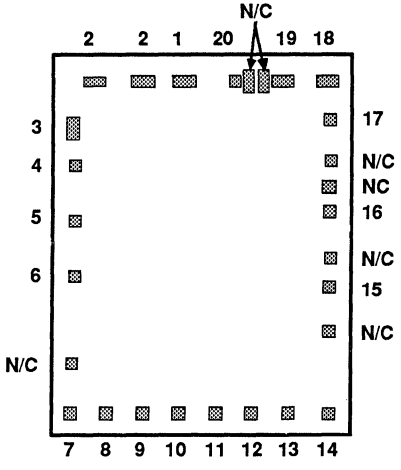
TABLE III
BIPOLAR CODE
FOR CIRCUIT OF FIGURE 7



HDAC7545A PIN ASSIGNMENT
(TOP VIEW)

PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT
2	AGND	ANALOG GROUND
3	DGND	DIGITAL LOGIC GROUND
4	DB11	INPUT DATA BIT 11 (MSB)
5	DB10	INPUT DATA BIT 10
6	DB9	INPUT DATA BIT 9
7	DB8	INPUT DATA BIT 8
8	DB7	INPUT DATA BIT 7
9	DB6	INPUT DATA BIT 6
10	DB5	INPUT DATA BIT 5
11	DB4	INPUT DATA BIT 4
12	DB3	INPUT DATA BIT 3
13	DB2	INPUT DATA BIT 2
14	DB1	INPUT DATA BIT 1
15	DB0	INPUT DATA BIT 0 (LSB)
16	$\overline{CS}$	CHIP SELECT
17	$\overline{WR}$	DATA WRITE
18	VDD	POSITIVE POWER SUPPLY
19	VREF	REFERENCE INPUT VOLTAGE
20	$R_{feedback}$	INTERNAL FEEDBACK RESISTOR

HDAC7545A PIN FUNCTIONS



N/C = No Connection.

HDAC7545A DIE PLOT
BONDING PAD LOCATION

Die Size 130 x 106 mils

***For Ordering Information See Section 1.*

NOTES:

HDAC97000

8-BIT, HIGH SPEED RASTER D/A CONVERTER

FEATURES:

- **200 MWPS Conversion Rate**
- **Pin-Compatible with AD9700 with Improved Performance**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White
- ECL Compatible
- Single Power Supply
- Stable On-Chip Bandgap Reference

APPLICATIONS:

- Color or Monochrome Displays
- High Resolution Raster Graphics
- Medical Electronics: CAT, PET, MR Imaging Displays
- CRT Terminals
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion

GENERAL DESCRIPTION

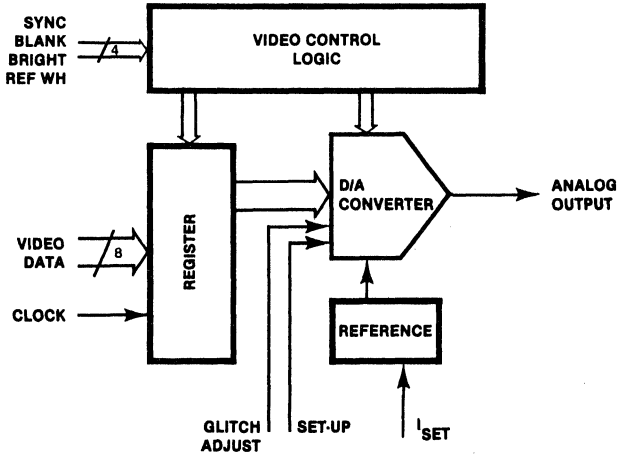
The HDAC97000 is a fully monolithic 8-bit video digital-to-analog converter specifically designed for raster graphic display applications. The HDAC97000 is complete with an 8-bit D/A converter, special video controls, on-chip bandgap reference and data registers.

Four unregistered video controls (Sync, Blank, +10% Bright and Reference White) allow full reconstruction of RS-343-A compatible video signals from composite inputs. All data and control inputs are compatible with standard ECL.

The HDAC97000 will directly drive a doubly-terminated 75 Ohm transmission line to standard video levels.

The precision internal reference is a bandgap type, suitable for stable operation over wide temperature ranges. The HDAC97000 is fabricated using an advanced VLSI Bipolar process for excellent performance, low power consumption, and high reliability in a choice of convenient packages.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltages

V_{EE} ..... −7.0 to 0.5V

Input Voltages

Clock, Data and Controls (measured to GND) ..... V_{EE} to 0.5V

Output

Analog Output applied voltage (measured to GND) ..... −3.0 to 3.0V
Analog Output applied current[2] 60mA
Output Short Circuit Duration ..... Unlimited

Temperature

Operating, ambient ..... −60 to +140°C
junction ..... +175°C
Lead, soldering (10 seconds) ..... +300°C
Storage ..... −60 to +150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. Current is specified as positive conventional current flowing into the device.

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = −25 to +85°C*, C_C = 0pF.							
I_{EE}	Supply Current		I		−155	−170	mA
C_{in}	Input Capacitance Clock, Data & Controls		V		3		pF
V_{OC}	Output Compliance Voltage		V	−2		+0.5	V
R_{OUT}	Equivalent Output Resistance			560	800	1040	Ohms
C_{OUT}	Output Capacitance		V		15		pF
I_{OUT}	Maximum Output Current	I_{REF} = MAX	IV			−30	mA
I_{IL}	Input Current, Logic LOW, Data & Controls		I		70	120	µA
I_{IH}	Input Current, Logic HIGH, Data & Controls		I		90	150	µA
IL	Linearity Error, Integral, Terminal Based	Notes 2, 3	I			±0.19	% Gray Scale
DNL	Linearity Error Differential	Notes 2, 4	I			±0.19	% Gray Scale
I_{OS}	Output Offset Current	Data = Sync = Blank = 1, Bright = 0	I		−1	−8	µA

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = −25 to +85°C*, C_C = 0pF.						
V_{OS} Output Offset Voltage		I		−37	−300	μV
E_G Absolute Gain Error		I			±5	% Gray Scale
TC_G Gain Error Tempco				50		ppm/°C
PSS Power Supply Sensitivity	Supply to Output	I			.005	%/V
V_{EE} Supply Voltage			−4.75	−5.2	−5.5	V
V_{IL} Input Voltage, Logic LOW		I			−1.70	V
V_{IH} Input Voltage, Logic HIGH		I	−0.90			V
RESOLUTION (full scale)				8		Bits
LSB WEIGHT (voltage)[5]				2.5		mV
LSB WEIGHT (current)[5]				66.67		μA
GRAY SCALE OUTPUT						
Current				0 to 17		mA
Voltage				637.5		mV
Linearity, Differential				±0.19		% Gray Scale
Linearity, Integral				±0.19		% Gray Scale
Monotonicity				Guaranteed		
Zero Offset (Initial)				0.4		mV
TEMPERATURE COEFFICIENTS						
Linearity				30		ppm/°C
Zero Offset				12		ppm/°C
Gain Error				50		ppm/°C
DATA INPUTS [Complementary Binary (CBN)]						
Logic Compatibility				ECL		
Logic Voltage Levels "1"			−0.9			V
(Positive Logic) "O"					−1.7	V
Input Capacitance	to VEE			5		pF
Input Resistance	to VEE			50		KΩ
REFERENCE WHITE, COMPOSITE SYNC, BLANKING AND 10% BRIGHT INPUTS						
Logic Compatibility				ECL		
Logic Voltage Levels "1"			−0.9			V
(Positive Logic) "O"					−1.7	V
Input Capacitance	to VEE			5		pF
Input Resistance	to VEE			50		KΩ

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS V_{CCA} = 0.0V, V_{EEA} = V_{EED} = −5.2V ±0.3V, T_A = −25 to +85°C*, C_C = 0pF.						
SET-UP CONTROL [5,6]						
Ground				0		mV (0 IRE Units)
Open				−53.6		mV (7.5 IRE Units)
1K Ohm to −5.2 Supply				−71.4		mV (10 IRE Units)
−5.2V				−142.9		mV (20 IRE Units
OUTPUT-COMPOSITE SYNC [5,6]						
Current				0 or −7.6		mA (±5%)
Voltage				0 or −286		mV ±5%)
OUTPUT-10% BRIGHT [5,7]						
Current				0 or −1.9		mA (±5%)
Voltage				0 or −71		mV (±5%)
OUTPUT-COMPOSITE BLANKING [5,6]						
Current				0 and −1.43 −1.90 or −3.81		mA (±5%)
Voltage				0 and −53.6 −71 or −142.9		mV (±5%)
POWER REQUIREMENTS						
Current Consuption (−5.2V)				140		mA
Power Dissipation				728		mW
Power Supply Rejection				.025/.25		% Gray Scale/V
TEMPERATURE RANGE						
Operating (Ambient)			−25		+85	°C
Storage			−55		+150	°C

DC ELECTRICAL CHARACTERISTICS NOTES

*θ_{CA} = 30°C/W typical at 500 LFPM.

1. The sum of t_{PWL} and t_{PWH} must always equal or exceed the minimum conversion cycle time.
2. Gray Scale = Video White Level - Video Black Level = 643mV (nominal)
3. ± % Gray Scale = LSB (Least Significant Bit).
4. ± % Gray Scale = LSB (Least Significant Bit).
5. 90 IRE Full Gray Scale.
6. Relative to Black.
7. Reference White, Composite Sync, and Composite Blanking are enabled with logic "0"; 10% Bright is enabled with logic "1". Composite Sync or Composite Blanking control signals reset input registers.

ELECTRICAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF T_A = 25 to +85°C*							
F	Maximum Conversion Rate	Note 2		200			MWPS
T_d	Clock to Output Delay				4.0		ns
t_{st}	Settling Time	± ½ LSB ± 0.2% Gray Scale[3]				10	ns
t_r, t_f	Rise/Fall Time	10% to 90% of Gray Scale[3]				1.75	ns
SR	Slew Rate			300	450		V/μs
t_{PWL}	Clock Pulse Width, LOW[1]			2.0			ns
t_{PWH}	Clock Pulse Width, HIGH			2.0			ns
t_S	Hold Time, Data and Controls			2.5	1.5		ns
t_H	Hold Time, Data and Controls			0	−0.5		ns
PSRR	Power Supply Rejection Ratio	Supply to Output[5]		−22			dB
G_E	Peak Glitch Area ("Energy")	Notes 5, 6	V		35		pico-Volt-Seconds
FT_C	Feedthrough, Clock	Data = Constant[7]		−22			dB
FT_D	Feedthrough, Data	Clock = Constant[7]					dB
SPEED PERFORMANCE-GRAY SCALE OUTPUT							
	Settling Time (Voltage Max.)				10		ns (to 0.4% of Gray Scale)
	Slew Rate				400		V/μs
	Update Rate				200		MWPS
	Rise Time				1.5		ns
	Glitch Energy				50		pV-s
STOBE INPUT							
	Logic Compatibility	Logic Loading			ECL		
	Logic Voltage Levels "1"	5pF and 50kΩ			−0.9		V
	(Positive Logic) "0"	To −5.2V			−1.7		V
	Set-up Time (Data)				1.5		ns
	Hold Time (Data)				0		ns
	Propagation Delay				4		ns

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS R_L = 37.5 Ohms, C_L = 5pF T_A = 25 to +85°C*						
SPEED PERFORMANCE-	Settling Time					
CONTROL INPUTS	To 10% of					
Composite Sync	Final Value			10		ns
Composite Blank				10		ns
Reference White				10		ns
Reference Black				10		ns
10% Bright				10		ns

AC ELECTRICAL CHARACTERISTICS NOTES

*θ_{CA} = 30°C/W typical at 500 LFPM.

1. The sum of t_{PWL} and t_{PWH} must always equal or exceed the minimum conversion cycle time.
2. MWPS-MegaWords Per Second ≈ MHz.
3. Gray Scale = Video White Level - Video Black Level = 643 mV (nominal).
4. 20 KHz, 600mV p-p ripple superimposed on V_{EE}; dB relative to full Gray Scale = 0dB.
5. Glitch can be further reduced by trimming Glitch Adjust.
6. Glitch Area (voltage time) is sometimes referred to as an "energy", although this is not dimensionally correct. The Peak Glitch Area is the maximum area deviation from the ideal output. Since glitches are typically "doublets" of symmetric positive and negative excursions, the average glitch area approches zero.
7. dB relative to full Gray Scale = 0dB, 300 MHz bandwidth limit.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at T_a = 25°C, and sample tested at specified temperature.
III	QA sample tested only at specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Paramater is a typical value for information purposes only.

HDAC97000 VIDEO DAC CHARACTERISTICS

COMPOSITE VIDEO SIGNAL
256 gray levels plus Sync, Blank, Bright and Reference White

STEP SIZE
2.5mV

GRAY SCALE RANGE
0.6375 V Peak to Peak

HDAC97000 VIDEO DAC CHARACTERISTICS

REFERENCE WHITE LEVEL
+ 100 IRE Units (+ 0.714V) relative to Blanking Level with standard set-up,
(+ 0.6375V relative to Reference Black)

DIGITAL INPUT FOR REFERENCE WHITE
All ones (11111111)

REFERENCE WHITE CONTROLS - PIN 16
Logic "0" overrides Video Input Word and drives to Reference White Level

---

REFERENCE BLACK LEVEL
– 0.7085 Absolute
+ 10 IRE Units (+ 71mV) relative to Blanking Level with standard set-up

---

DITIGAL INPUT FOR REFERENCE BLACK
All zeros (00000000)

SET-UP CONTROL
User Programmable in four levels to set Blanking Level (relative to Reference Black)

	mV	IRE Units
1. Input Grounded	0	0
2. Input Open	– 53.6	7.5
3. Input 1K Ohm to – 5.2V	– 71.4	10 (Standard Set-up)
4. Input to – 5.2V	– 142.9	20

COMPOSITE BLANKING LEVEL (with standard set-up)
– 0.785V Absolute
– 10 IRE Units (– 71mV) relative to Reference Black

COMPOSITE BLANKING CONTROL - PIN 18
Logic "0" overrides Video Input Word and drives output negative by the amount of set-up voltage relative to the Reference Black Level

---

COMPOSITE SYNC LEVEL
– 1.071V absolute with standard set-up
– 40 IRE Units (– 0.286V) relative to Blanking Level

COMPOSITE SYNC CONTROL - PIN 17
Logic "0" overrides Video Input Word and drives output 0.286V negative relative to the Reference Black Level (relative values of Blank and Sync Levels sum together with both active)

10% BRIGHT LEVEL
0V Absolute
All levels are shifted down by 71mV when the 10% Bright Control is used

---

10% BRIGHT LEVEL - PIN 19
Logic "0" causes output to go positive by 71mV relative to Reference White Level

---

STROBE INPUT - PIN 11
Logic "0" to "1" transition clocks input register - input data held by latch, slave latch tracks master latch data
Logic "1" to "0" transition - slave latch holds previous data, master latch tracks input

---

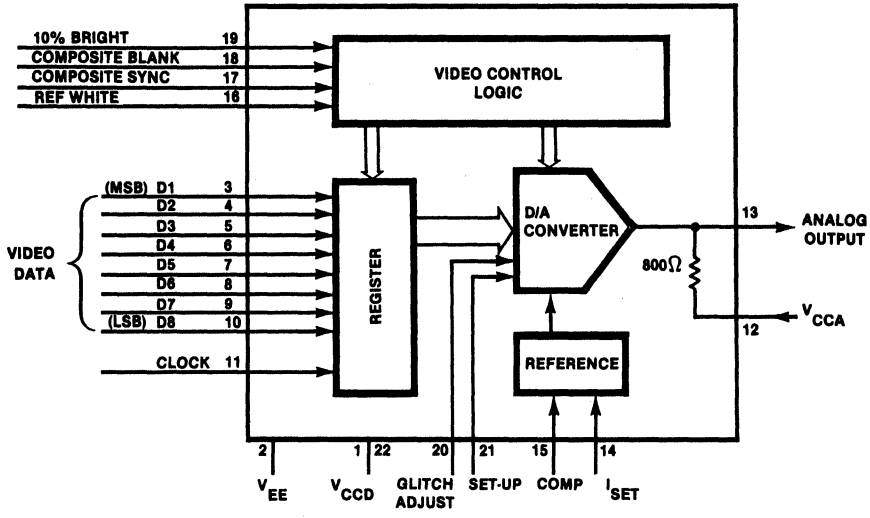
APPLICATION INFORMATION

The HDAC97000 is a fully monolithic 8-bit video D/A Converter for graphic display applications. It has complete composite controls including Sync, Blank, Reference White, Set-up and 10% Bright, and will directly drive a 75 Ohm load to RS-343-A video levels. All data and control inputs are compatible with standard ECL. The HDAC97000 is packaged in a 22 lead dual-in-line package and is pin-compatible with the Analog Devices AD9700.

The video control inputs (Sync, Blank, Bright and Reference White) are used for reconstruction of RS-343-A compatible signals from video control inputs. Video set-up level (the difference between video black and video blank) may be programmed for 0, 7.5, 10, or 20 IRE units, depending on the condition of the Set-up Select control.

The HDAC97000 uses a fully binary weighted approach utilizing current switches to implement the DAC. The upper 3 bits are segmented with interdigitated current sources for good matching and better linearity. Each data pin has latches for deskewing input data if the data arrives at different times. This prevents glitches from occurring at the output.

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the HDAC97000 in a color raster application is shown in Figure 2. Although the HDAC97000 requires few external components and is extremely easy to use, there are several considerations that should be noted to achieve best performance. The very high operating speeds of the HDAC97000 require good circuit layout, decoupling of supplies, and proper design of transmission lines.

Video input data and controls may be directly connected to the HDAC97000. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to −2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC97000 provides separate digital and analog V_{CC} connections to simplify grounding layout.

The analog output and I_{SET} pin are configured so the device can directly drive a 37.5 Ohm impedance system as shown. The source impedance of the HDAC97000 output is 800 Ohms ± 30%, thus needing an external source-termination resistor to drive a 75 Ohm transmission line. The load resistor (R_L) must be 82.8 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission line has a matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of source termination resistor R_S, load resistor R_L and load terminator R_T minimizes reflections of both forward and reverse travelling waves in the analog transmission system. The return path for analog output current is V_{CCA}, which is connected internally to the source-termination resistor, R_S.

No external reference is required for operation of the HDAC97000, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges.

The HDAC97000 operates from a single standard +5 Volt or −5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC97000's inherent supply noise rejection characteristics. As shown, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away. Additional decoupling can be accomplished by placing a .01μF between the compensation pin (15) and V_{CCA}. This pin connects internally to the DAC reference, which provides the DAC DC bias.

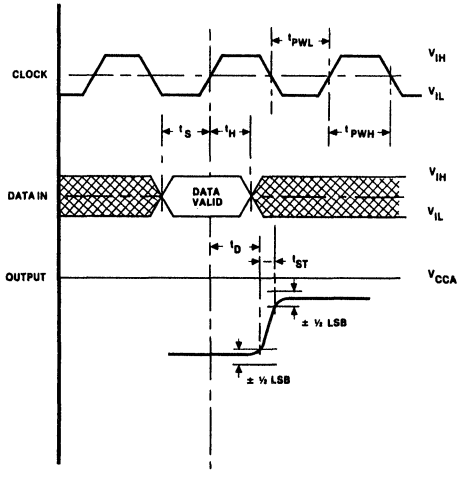
The timing diagram for the HDAC97000 is shown in Figure 1. Data to the DAC is simultaneously entered on the rising edge of the clock. Data must be valid for a set-up time of t_S before, and for a hold time of t_H after the rising edge of the clock, in order to be correctly entered. The DAC outputs will change in accordance to the clocked input data after a delay time of t_D. The settling time is specified as the time from when the DAC output is no longer within ½ LSB of the previous value until it is within ½ LSB of the new value.

The video control inputs cause the DAC output to change directly, without regard to the clock input. All video controls (Sync, Blank, Bright and Reference White) are active-Low (negative true) logic. Figure 3 illustrates the operation of Sync and Blank inputs and the resulting video output signal. As shown, both Sync and Blank must be Low to achieve the proper video Sync level. The video control input hierarchy is given in Table 1, with typical output levels for a set-up level of 10 IRE.

Set-up level is the difference between video Blank and Black levels. The HDAC97000 supports set-ups of 0, 7.5, 10, and 20 IRE, which are programmed by connecting the Set-up select input to ground (0V), not connected, to V_{EE} through a 1K Ohm resistor, or to V_{EE} (−5.2V), respectively. For most applications the 7.5 IRE option is suitable.

The Reference White input forces the DAC outputs to an all "1"s level, which is video "white" in most systems. This is especially useful for clearing the display screen to white during system reset or power-up. The Bright input adds 10% of full-scale video to the present video level. The Bright feature is commonly used for highlighting cursors or creating overlays of video information. Sync, Blank and Reference White override the data inputs, while Bright may be applied to any video level.

FIGURE 1 TIMING DIAGRAM



SETTING OUTPUT DRIVE CAPABILITY

The current set pin (pin 14) adjusts the full-scale output current of the HDAC97000. The resistor designated R_{SET}, which governs the current into pin 14, can be calculated in relation to DAC output current as follows:

$$\text{Equation 1: } R_{SET} = \frac{90}{22.59}\left[\frac{1.23V}{V_{OUT\,G.S.}/R_{LOAD}}\right]$$

Here, 1.23V is the internal reference voltage, $V_{OUT\,G.S.}$ is the DAC gray scale output voltage and R_{LOAD} is the total load resistance on the analog output. In raster scan video applications, R_{LOAD} could be equivalent to the load in Figure 2. This would be the internal DAC output resistance in parallel with the output load and cable terminating resistor. If the device is being used in raster scan applications, the total output voltage is the gray scale current plus the video function currents. The value of R_{SET} using the total current (or voltage) can be calculated with equation 2:

$$\text{Equation 2: } R_{SET} = \frac{140 + B}{22.59}\left[\frac{1.23V}{V_{OUT}/R_{LOAD}}\right]$$

where B is equal to the value of the setup (BLANK) level (0, 7.5, 10 or 20). The total output voltage capability is 1.13V, which is more than adequate for composite video waveforms.

In other applications where lighter loads are used, R_{SET} can be increased, thus decreasing power dissipation since the output current is decreased. Figure 7 shows an example where this applies if a large output voltage or current swing is not needed.

GLITCH ADJUST AND COMPENSATION

Glitch adjust and compensation are optional functions that can be used to improve dynamic performance. Glitch adjust is an external adjustment of the logic threshhold in the DAC switches to skew the speed in order to get an output glitch energy below the data sheet specification. This can be done with a resistive pot in conjunction with pin 20 and V_{EE} as shown in Figure 2. Adjust the pot for minimum output glitch when the input code is toggling between 01111111 and 10000000; the code transition which normally causes the largest glitch.

Compensation is accomplished by connecting a .01μF capacitor to pin 15. Actually this is a decoupling capacitor connected internally to the DAC biasing network. It adds more decoupling as needed if operating with a noisy supply or environment as well as decoupling internal switching noise. This is different than the AD9700, which uses the capacitor to externally compensate the voltage reference buffer amplifier. The amplifier in the HDAC97000 is internally compensated and therefore the compensation pin is used for the optional decoupling function.

FIGURE 2 HDAC97000 TYPICAL INTERFACE CIRCUIT

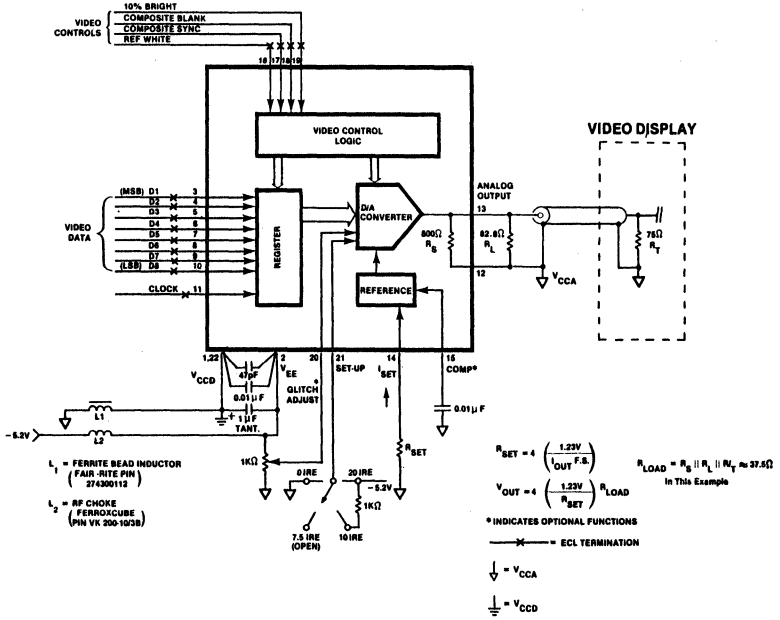


Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)[1]

Sync[2,3]	Blank[2]	Ref White	Bright	Data Input	Out (V)[5,6]	Out (IRE)[4]	Description
0	0	1	1	XXXXXXXX	−1.071	−40	Sync Level
1	0	1	1	XXXXXXXX	−0.785	0	Blank Level
1	1	0	1	XXXXXXXX	−0.071	100	Normal White Level
1	1	0	0	XXXXXXXX	0.0	110	Enhanced White Level
1	1	1	1	11111111	−0.071	100	Normal White Level
1	1	1	0	11111111	0.0	110	Enhanced White Level
1	1	1	1	00000000	−0.7085	10	Normal Black Level
1	1	1	0	00000000	−0.6375	20	Enhanced Black Level

Notes:

1. All Video Controls are active-Low (negative true) logic.
2. Sync and Blank output levels are dependent on set-up level selected. Values indicated are set-up = 10 IRE set-up select connected through a 1K Ohm resistor to V_{EE}.
3. Sync level requires that both Sync and Blank = 0.
4. 140 IRE = 1.00 Volt.
5. All control values are subject to tolerance of ±5% Gray Scale.
6. Analog output values shown are based on a step size of 2.5mV per LSB (used for ease of calibration). This causes the Gray Scale output to be 637.5mV rather than 643mV in the idealized video output waveform. Both values are within the tolerances of RS-343-A.

Table 2 Set-up Select

Set-up Control Input	Set-up Level
0 Volts (GND)	0 IRE
Not Connected	7.5 IRE
1K Ohm to −5.2V (V_{EE})	10 IRE
−5.2 Volts (V_{EE})	20 IRE

FIGURE 3 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD & 10 IRE SET-UP

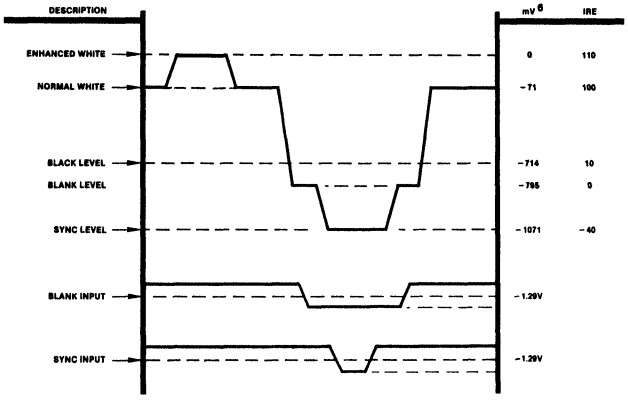


FIGURE 4 EQUIVALENT INPUT CIRCUIT, DATA, CLOCK, & CONTROL

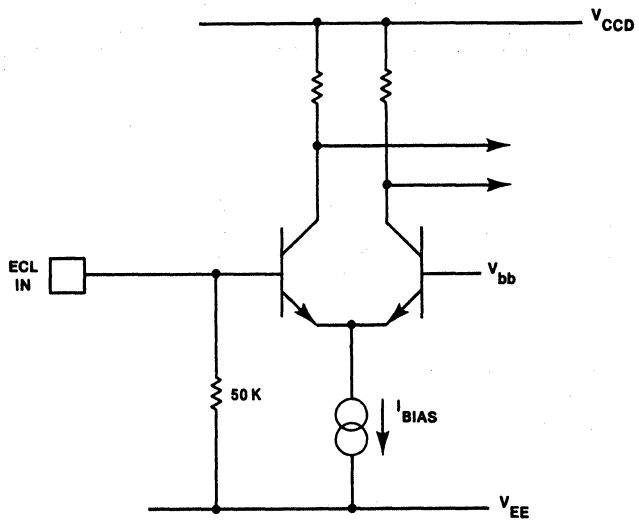


FIGURE 5 DAC OUTPUT CIRCUIT

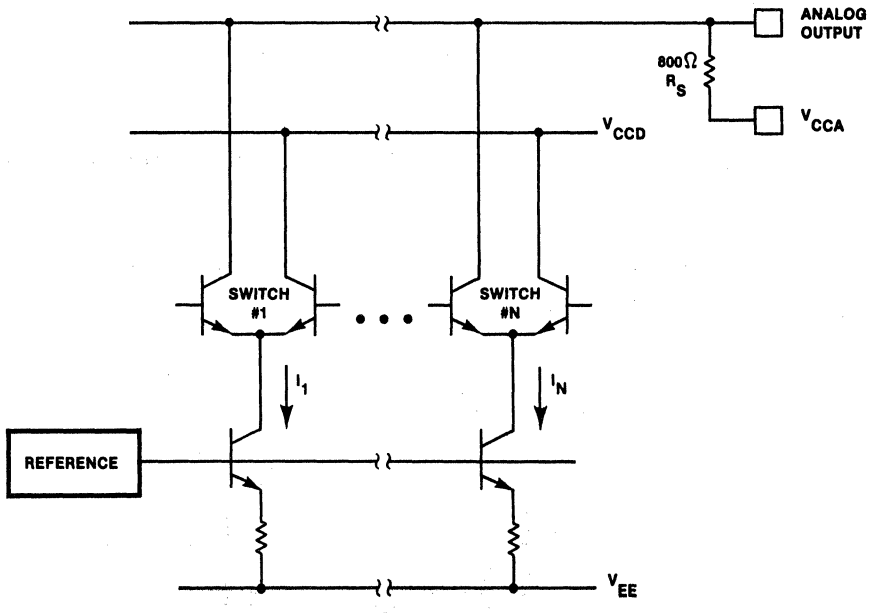
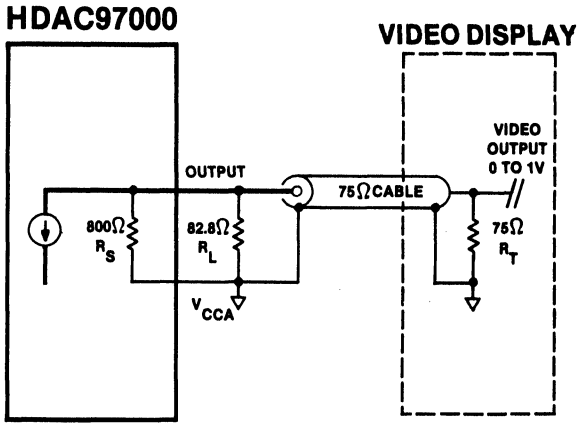


FIGURE 6 STANDARD LOAD



HDAC97000 AS A STANDARD D/A CONVERTER

The HDAC97000 is primarily designed to be used in composite video applications, but with its inherent speed, it can also be utilized in other applications requiring up to 200 MegaWords Per Second update rate.

When implemented as a standard DAC, some of the video control inputs should be connected to ground through a diode as indicated in Figure 7 (opposite page). Composite Sync and Blank as well as Reference White are connected in this manner (pin 16, 17 and 18). The set-up pin (21) is tied directly to ground and the 10% Bright pin (19) is left open. If 8-bits of resolution are not necessary, the unused inputs should be tied to ground through a diode to prevent an output offset voltage.

HDAC97000 IN A SINGLE +5V TTL LOGIC SYSTEM

The HDAC97000 is primarily designed for ECL logic systems which perform better in high-speed applications, but the DAC can be configured for TTL levels as shown in Figure 8 (opposite page). It can be used in systems that only have a +5V power supply available for the DAC. If any of the data inputs, Composite Blank and Sync or Reference White are not used, they should still be tied up to +5V as shown. If the 10% Bright is not used, it should be grounded or left open. Also, note the different set-up conditions as well as the pull-ups on the output.

FIGURE 7 STANDARD D/A CONVERTER

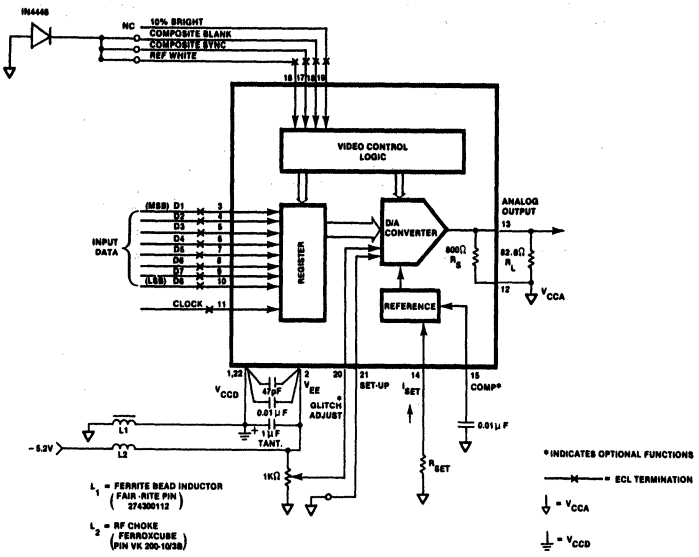
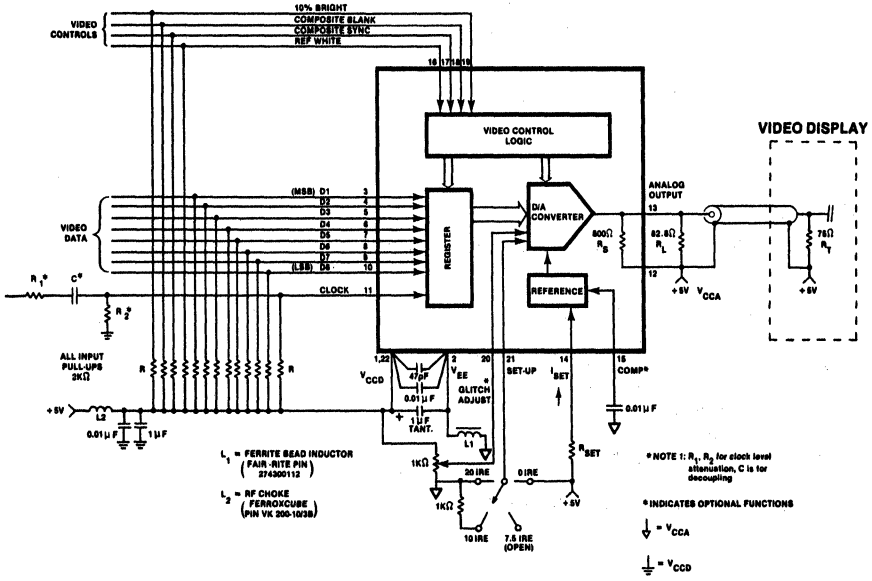
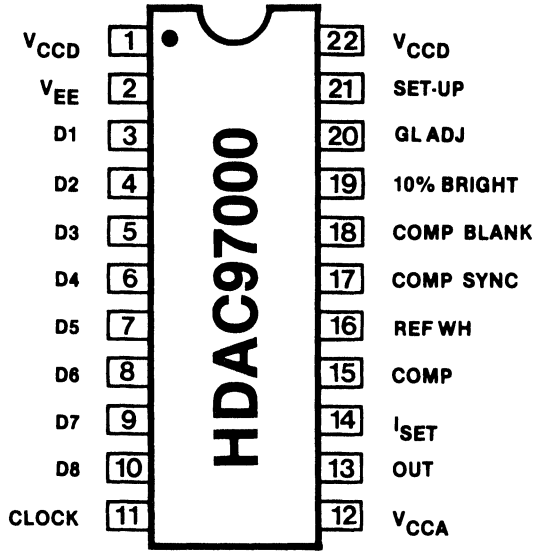


FIGURE 8 TTL-COMPATIBLE HDAC97000



Honeywell

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
V_{CCD}	Positive Digital Supply
V_{EE}	Negative Supply Voltage
D1	Data Input Bit 1 (MSB)
D2	Data Input Bit 2
D3	Data Input Bit 3
D4	Data Input Bit 4
D5	Data Input Bit 5
D6	Data Input Bit 6
D7	Data Input Bit 7
D8	Data Input Bit 8 (LSB)
CLOCK	Conversion Clock Input
OUT	Analog Video Output
I_{SET}	Reference Current Set
COMP	Decoupling Capacitor Connection
REF WH	Reference White Input
COMP SYNC	Composite Video Sync Input
COMP BLANK	Composite Video Blank Input
10% BRIGHT	+10% Bright Input
GL ADJ	Glitch Adjust Connection
SET-UP	Video Set-Up Select
V_{CCA}	Positive Analog Supply

**For Ordering Information See Section 1.*

NOTES:

HDAM51100

HIGH SPEED 8-BIT VIDEO DAC WITH 512 X 8 MEMORY

PRELIMINARY INFORMATION

FEATURES

- **Large 512 X 8 Lookup Table**
- **125 MWPS Conversion Rate**
- Fully Parallel Bidirectional Data I/O
- DAC Output Rise/Fall Time <1 ns
- Single Power Supply
- RS-343-A Compatible Video Levels

APPLICATIONS

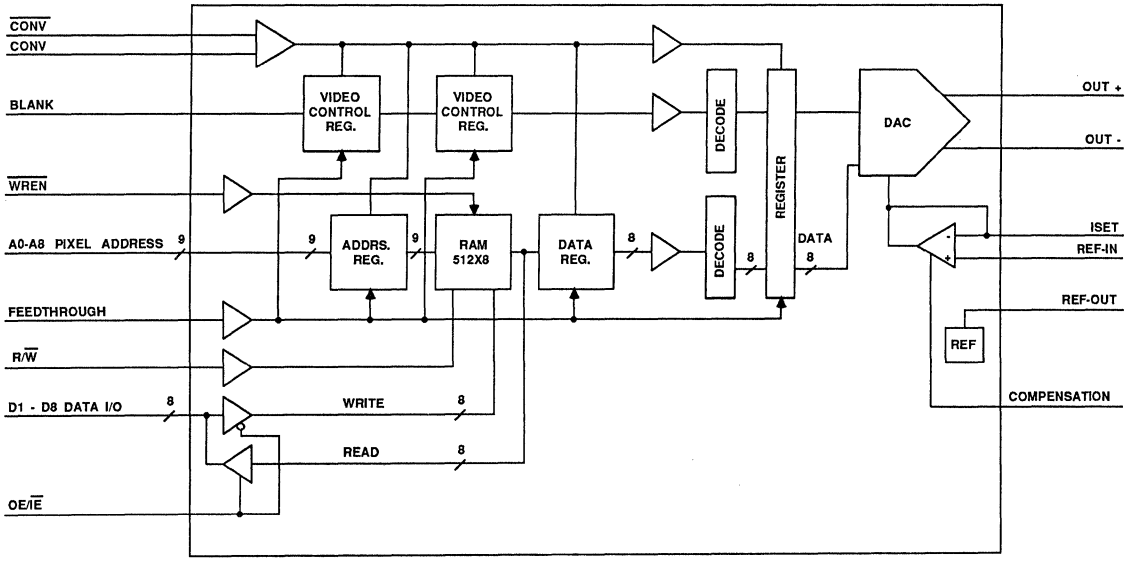
- High Resolution Color or Monochrome Displays
- CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- High-Speed D/A Conversion
- Waveform Generators
- Automated Test Equipment
- ECM

3

GENERAL DESCRIPTION

The HDAM51100 is a monolithic high performance 8-bit digital to analog converter that includes a 512 X 8 RAM (color lookup palette), a precision bandgap reference, registers, bus interface logic, parallel bidirectional data I/O, and is capable of directly driving doubly-terminated 50 or 75 Ohm loads to RS-343-A video levels. The on-chip memory allows 512 of the 16.7 million possible colors to be simultaneously displayed in an RGB format. The complete palette can be updated with a new set of 512 colors during the vertical retrace interval, even at 70-90Hz refresh rates. The memory data is available on the bidirectional data I/O port. Video controls are fully synchronous with the pixel data. SYNC and BRIGHT controls are available as an option. The standard set-up level is 0IRE with 7.5 IRE available as an option.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (VCC to VEE).....+6.0 to -0.5V
Negative Supply Voltage (VEE to VCC).....-6.0 to +0.5V
Ground Voltage Differential (VCCA to VCCD).+0.5 to -0.5V
VEEA to VEED Differential.....+0.5 to -0.5V

Input Voltages
Data, Controls (ECL, measured to VCCD).....+0.5 to VEED

Output
Applied Voltage.....VEE-0.5V to VCC + 3.5V

Temperature
Temperature, ambient.....-60 to +140°C
junction.....+150°C
Lead Temperature (soldering 10 seconds)..+300°C
Storage Temperature.....-65 to +150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL CHARACTERISTICS

COMMERCIAL TEMPERATURE RANGE

Fig. 1, VCCA = VCCD = 0.0V, VEEA = VEED = -5.2± 0.3V, TA = 25°C, CC = 0pF. ISET = 1.792mA, unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +70°C MIN	HOT +70°C MAX	COLD 0°C MIN	COLD 0°C MAX	UNITS
DAC CHARACTERISTICS										
Resolution		I	8		8					Bits
Integral Linearity	1.2mA≤ISET ≤1.8mA	I	-0.2 -1/2	±0.1 ±1/4	+0.2 +1/2					% Grey Scale LSB
Integral Linearity Tempco		V								ppm/°C
Differential Linearity	1.2mA≤ISET ≤1.8mA	I	-0.2 -1/2	±0.1 ±1/4	+0.2 +1/2					% Grey Scale LSB
Differential Linearity Tempco		V								ppm/°C
Gain Error	(Excluding Reference)	I	-5		+5					% Grey Scale
Gain Error Tempco		V		±150						ppm/°C
Offset Current, Outputs, IOS		I		5	15					µA
Full Scale Current, Outputs, IFS	Adjusted for Gain and Offset	I		28.56						mA
Blank Current, Out +	Adjusted for Gain and Offset	I		0						mA

ELECTRICAL CHARACTERISTICS

COMMERCIAL TEMPERATURE RANGE

Fig. 1, VCCA = VCCD = 0.0V, VEEA = VEED = -5.2± 0.3V, TA = 25°C, CC = 0pF. ISET = 1.792mA, unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +70°C MIN	HOT +70°C MAX	COLD 0°C MIN	COLD 0°C MAX	UNITS
DAC CHARACTERISTICS (Cont.)										
Blank Current, Out -	Adjusted for Gain and Offset	I		28.56						mA
Maximum Allowable Current, Outputs	ISET is User Defined	IV			30		30			mA
Compliance Voltage, Outputs		IV	-1.5		+1.5					V
Output Resistance	RL = ∞	I	20							KΩ
Output Capacitance	CL = 0	V		10						pF
Power Supply Sensitivity	$\frac{\Delta IFS}{\Delta VEE}$	I			±120					µA/V
REFERENCE CHARACTERISTICS										
Bandgap Voltage	IREF = – 50µA	I	1.17		1.29					V
Bandgap Output Current, IREF		I			50					µA
Bandgap Tempco	IREF = – 10µA	V		±100						ppm/°C
Common Mode Range REF IN, ISET Pins	VCCA = 0 VEEA = -5.2	IV	-2.45		-0.275					V
Input Capacitance REF IN, ISET Pins		V		5						pF
Input Current, REF IN		V		3						µA
Input Current, ISET		IV			1.80		1.80			mA
DIGITAL CONTROL CHARACTERISTICS										
Input Voltage, Logic Low Address, Controls, Data	MECL 10K/10KH Compatible	II	-1.95		-1.63	-1.95	-1.60	-1.95	-1.63	V
Input Voltage, Logic High Address, Controls, Data	MECL 10K/10KH Compatible	II	-0.98		-0.81	-0.92	-0.74	-1.02	-0.84	V

ELECTRICAL CHARACTERISTICS

COMMERCIAL TEMPERATURE RANGE

Fig. 1, VCCA = VCCD = 0.0V, VEEA = VEED = -5.2± 0.3V, TA = 25°C, CC = 0pF. ISET = 1.792mA, unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +70°C MIN	HOT +70°C MAX	COLD 0°C MIN	COLD 0°C MAX	UNITS
DIGITAL CONTROL CHARACTERISTICS (Contd.)										
Input Current, Logic Low Address, Controls, Data		I			60					µA
Input Current, Logic High Address, Controls, Data		I			120					µA
Input Resistance, Address, Controls, Data	to VEED	V		50						KΩ
Input Capacitance, Address, Controls		V		3						pF
Input Capacitance, Data		V		5						pF
Differential Range, CONVert, $\overline{\text{CONVert}}$	MECL 10K/10KH Compatible	I	0.4		1.2					V
Common Mode Range, VCCM CONVert, $\overline{\text{CONVert}}$	VCCD = 0 VEED = -5.2	I	-2.45		-0.5					V
Input Current, CONVert, $\overline{\text{CONVert}}$	V = VCCM	I			60					µA
Input Capacitance, CONVert, $\overline{\text{CONVert}}$		V		3						pF
Output Voltage, Logic Low Data			-1.95		-1.63	-1.95	-1.60	-1.95	-1.63	V
Output Voltage, Logic High Data			-0.98		-0.81	-0.92	-0.74	-1.02	-0.84	V
Output Current Data		IV			11		11		11	mA
POWER SUPPLY CHARACTERISTICS										
Supply Current, IEEA		I		56	60					mA
Supply Current, IEED		I		660	790					mA
Differential Voltage VCCA to VCCD, VEEA to VEED		IV	-0.1		+0.1					V

ELECTRICAL CHARACTERISTICS

COMMERCIAL TEMPERATURE RANGE

Fig. 1, VCCA = VCCD = 0.0V, VEEA = VEED = -5.2± 0.3V, TA = 25°C, CC = 0pF. ISET = 1.792mA, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +70°C MIN	HOT +70°C MAX	COLD 0°C MIN	COLD 0°C MAX	UNITS
DAC CHARACTERISTICS (SEE TIMING DIAGRAMS A, D)										
Maximum Update Rate, FS		I		125						MHz
Rise/Fall Times, Outputs	10% to 90% G.S.	I			1					ns
Rise/Fall Times, Outputs	10% to 90% G.S. RL = 37.5Ω	IV			1.5					ns
Slew Rate, Outputs		I	525							V/µS
Settling Time, Clocked Mode, Outputs, TSI	Full Scale Transition to 0.2%				3.0					ns
Settling Time, Clocked Mode, Outputs	Full Scale Transition to 0.8%	IV			2.2					ns
Settling Time, Clocked Mode, Outputs	Full Scale Transition to 3.2%	IV			1.6					ns
Clock to Output Delay, TDOC		I		3.25	4.25					ns
Clock to Output Latency Clocked Mode		I	2		2					cycles
Blank to Output Latency Clocked Mode		I	2		2					cycles
Address Output Delay, Transparent Mode, TDOT		V		18.5						ns
Feed Through, Clock, Controls, Data		I			-42					dB
Peak Glitch, VGL	1 LSB Transition at midscale	V		2.8						mV
Glitch Energy (½ VGL & Time)	1 LSB Transition at midscale	V		3						pV-s
REFERENCE CHARACTERISTICS										
Amplifier Bandwidth, -3dB		V		1						MHz

ELECTRICAL CHARACTERISTICS

COMMERCIAL TEMPERATURE RANGE

Fig. 1, VCCA = VCCD = 0.0V, VEEA = VEED = -5.2± 0.3V, TA = 25°C, CC = 0pF. ISET = 1.792mA, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +70°C MIN	HOT +70°C MAX	COLD 0°C MIN	COLD 0°C MAX	UNITS
DIGITAL CONTROL CHARACTERISTICS (See Timing Diagrams A, B, C)										
Maximum Clock Cycle CONVert, $\overline{\text{CONVert}}$, 1/FS		I			8					ns
Pulse Width, High CONVert, $\overline{\text{CONVert}}$, TPWH					2.5					ns
Pulse Width, Low CONVert, $\overline{\text{CONVert}}$, TPWL					2.5					ns
Set-up Time, Address, Controls, TSAC		I			2.5					ns
Hold Time, Address, Controls, THAC		I			1					ns
Set-up Time, Write, Address Latched to R/$\overline{\text{W}}$, TSCW		I			8					ns
Hold Time, Write, Address Latched to R/$\overline{\text{W}}$, THCW					1					ns
Pulse Width, Write, R/$\overline{\text{W}}$, TPWW					5.5					ns
Set-up Time, Write, $\overline{\text{WREN}}$ to R/$\overline{\text{W}}$, TSEW		IV			0					ns
Hold Time, Write, $\overline{\text{WREN}}$ to R/$\overline{\text{W}}$, THEW		IV			0					ns
Set-up Time, Write, Data to R/$\overline{\text{W}}$ Low, TSDW					2.5					ns
Hold Time, Write, Data to R/$\overline{\text{W}}$ High, THDW					1					ns
Set-up Time, Write, OE/$\overline{\text{IE}}$ Low to Data, TSID		IV			2.5					ns
Set-up Time, Read, R/$\overline{\text{W}}$, $\overline{\text{WREN}}$ High to Clock, TSR		IV			2.5					ns
Set-up Time, Read, OE/$\overline{\text{IE}}$ High to Clock, TSO		IV			2.5					ns
Data Delay, Read, Clock to Data, TDD		IV			12					ns

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests performed after a 3 minute power soak.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperatures.
II	100% production tested at Ta = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

FUNCTIONAL DESCRIPTION

The HDAM51100 is a 125 MWPS raster graphics subsystem that includes a 512 X 8 color lookup palette, 8-bit DAC, a precision bandgap reference, registers, bus interface logic and a parallel bidirectional data I/O port. Refer to Timing Diagrams for system timing.

COLOR LOOKUP TABLE

Pixel color data is applied to the RAM address register through the address lines A0-A8. This address is used to "lookup" one of the possible 512 intensities stored in the RAM through the bidirectional data port, lines D1-D8. The address register is latched on the rising edge of CONVert (the falling edge of $\overline{\text{CONVert}}$). The addressed intensity data from the RAM is latched into the data register on the next rising edge and latched into the DAC register on the next rising clock edge, which applies it to the DAC output. This results in the RAM data appearing at the DAC output two clock cycles after it is latched into the address register. If the Feedthrough (FT) control is asserted, the address is applied to the RAM and the intensity is applied to the DAC asynchronously with respect to CONVert. In either case, reading data out of the RAM requires that the Read/Write (R/$\overline{\text{W}}$) or Write Enable ($\overline{\text{WREN}}$) pin be asserted high.

DATA I/O

When the Output Enable/Input Enable (OE/$\overline{\text{IE}}$) pin, the R/$\overline{\text{W}}$ pin and the $\overline{\text{WREN}}$ pin are asserted low, the 8-bit intensity word applied to the 8-bit data I/O bus (D1 is the MSB) is written into the RAM at the address latched into address register from the address bus, pins A0-A8.

When the OE/$\overline{\text{IE}}$ pin and the R/$\overline{\text{W}}$ or $\overline{\text{WREN}}$ pin are asserted high, the 8-bit intensity word from the RAM at the address latched into the address register appears on the 8-bit data I/O bus and is available to be read by circuitry external to the chip. The data I/O bus can drive ECL loads of 120Ω to -2V.

VIDEO CONTROL

The BLANK control, when asserted high, forces the DAC output to the blank (OIRE, black) level irrespective of the digital word applied to the DAC (Refer to Figure 2). It has the same latency as the lookup table data.

VOLTAGE REFERENCE

A precision bandgap voltage reference capable of driving two additional HDAM51100's is included on chip to improve performance and reduce the number of necessary external components.

DAC

The DAC differential outputs provide R3-343-A compatible video levels for 1.1mA≤ISET≤1.8mA and a load of 25 to 37.5 Ohms. OUT- provides standard video levels (blank down) and OUT+ provides inverse video (blank up) with respect to VCCA.

OUT- is negative true logic; full scale output for all zeros from the RAM. OUT+ is positive true logic; full scale for all ones from the RAM. Refer to Figure 2 for a description of data and video controls.

Glitches are a major problem in high speed raster graphics applications. The DAC in the HDAM51100 is designed to minimize any differences in switching times of the different bits. Registering the data prior to applying it to the DAC insures that all of the data bits arrive at the same time further reducing the possibility of glitches.

LOGIC LEVELS

The HDAM51100 is compatable with ECL logic when powered by a -5.2V supply.

TYPICAL APPLICATION CIRCUIT

Figure 1 illustrates a typical application circuit for a single HDAM51100. This circuit shows how to terminate the video DAC's output using either a 50 or a 75 Ohm load and how to set the voltage reference. The internal bandgap reference or an external reference voltage can be used.

The output of the DAC is proportional to the reference voltage divided by the sum of resistors R1 and R2. The equation for the DAC full scale voltage is:

$$\text{VOUT (F.S.)} = \frac{\text{VREF}}{\alpha\,\text{TR1} + \text{R2}} \quad (15.9375)\,\text{RL where:}$$

VREF is the reference voltage

α TR1 is the useable portion of R1

RL is the total load on the output

OUT- is negative true logic; full scale output for all zeros input. OUT+ is the opposite; full scale output for all ones input.

In a multiple DAC application such as an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) DAC outputs. A change in gain or an offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen. For this reason, it is important for the outputs of all three DAC's to track each other over the entire range of operating conditions. Since the DAC output is portional to the reference current (ISET) and the digital input code, using a single reference to drive all three DACs will minimize any mismatch between them even if the reference drifts.

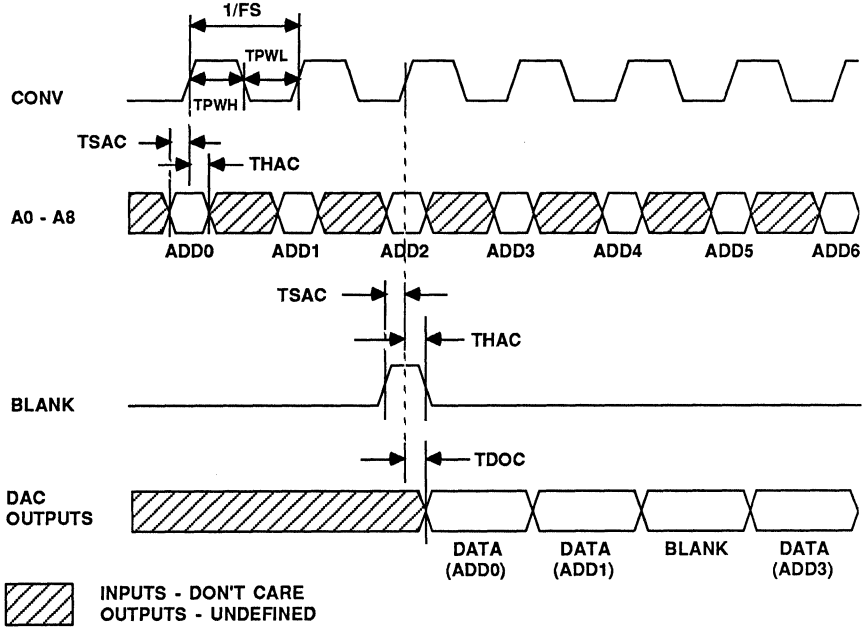
Figure 3 illustrates a circuit that slaves all three DACs from the reference of the "master" DAC. All of the DAC's have a common reference adjustment. This is the simplest reference arrangement and eliminates the need for individual calibration of each DAC during production assembly. The HDAM51100 contains an internal precision bandgap reference which completely eliminates the need for an external reference in most applications. The reference output on a HDAM51100 can supply enough current to drive itself and two additional HDAM51100's.

Figure 4 is a variation on Figure 3 in which one common reference is used but each DAC has it's own individual adjustment.

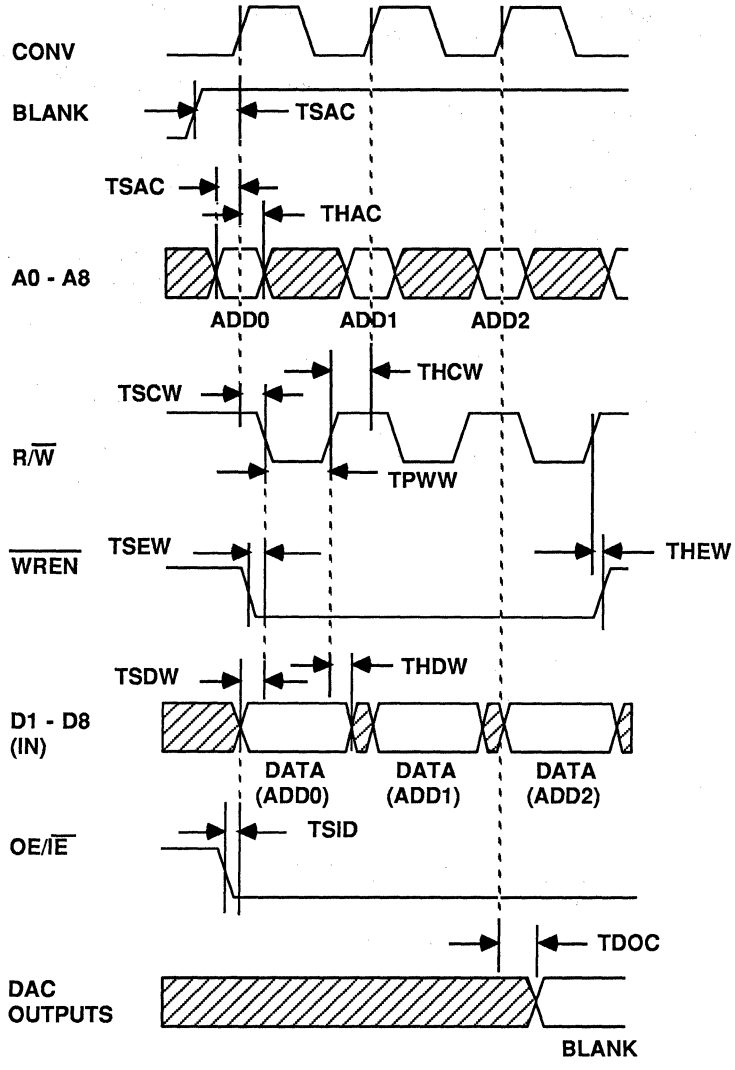
If it is desireable to use an external reference, the HDAM51100 can easily accomodate this as shown in Figure 5.

As with any high performance, high frequency device, care must be taken when laying out the connecting circuitry. All leads must be kept as short as possible. Power supply decoupling must occur at the IC pins using low inductance ceramic capacitors. Care must be taken to isolate the analog and digital grounds. If the DAC output or data and control lines are routed any appreciable distance on the PC board, transmission line techniques such as stripline or microstrip should be used. Place the three parts near each other, as well as the reference adjustment circuitry, on the board to minimize mismatch due to thermal gradients.

TIMING DIAGRAMS



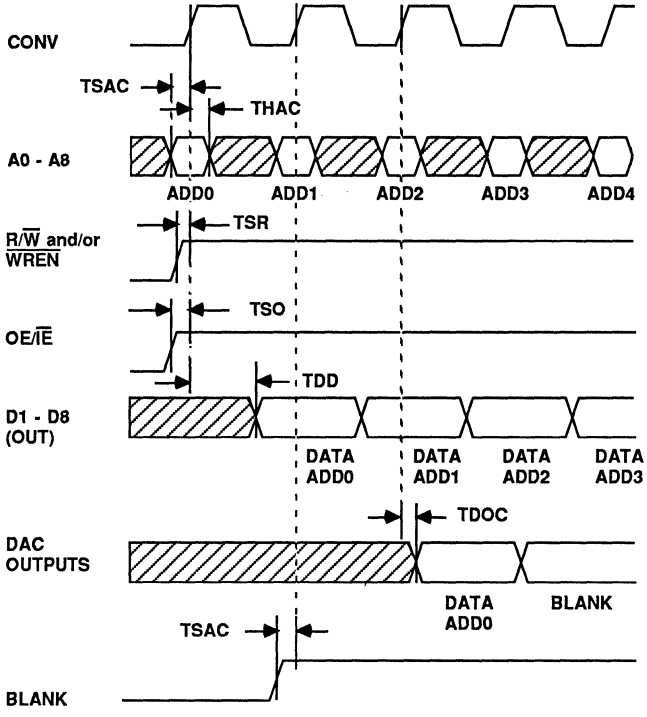
TIMING DIAGRAM A - DAC READ



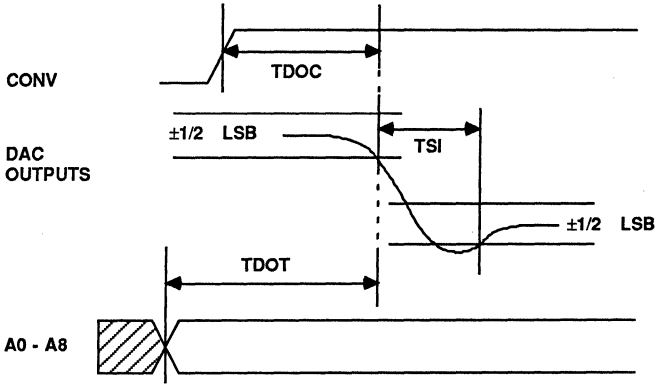
NOTE: MULTIPLE CONVERT PULSES ARE ALLOWABLE DURING WRITE CYCLES IF ADDRESS AND DATA ARE UNCHANGED.

INPUTS - DON'T CARE
OUTPUTS - UNDEFINED

TIMING DIAGRAM B - RAM WRITE



TIMING DIAGRAM C - RAM READ



TIMING DIAGRAM D - DAC

INPUTS - DON'T CARE
OUTPUTS - UNDEFINED

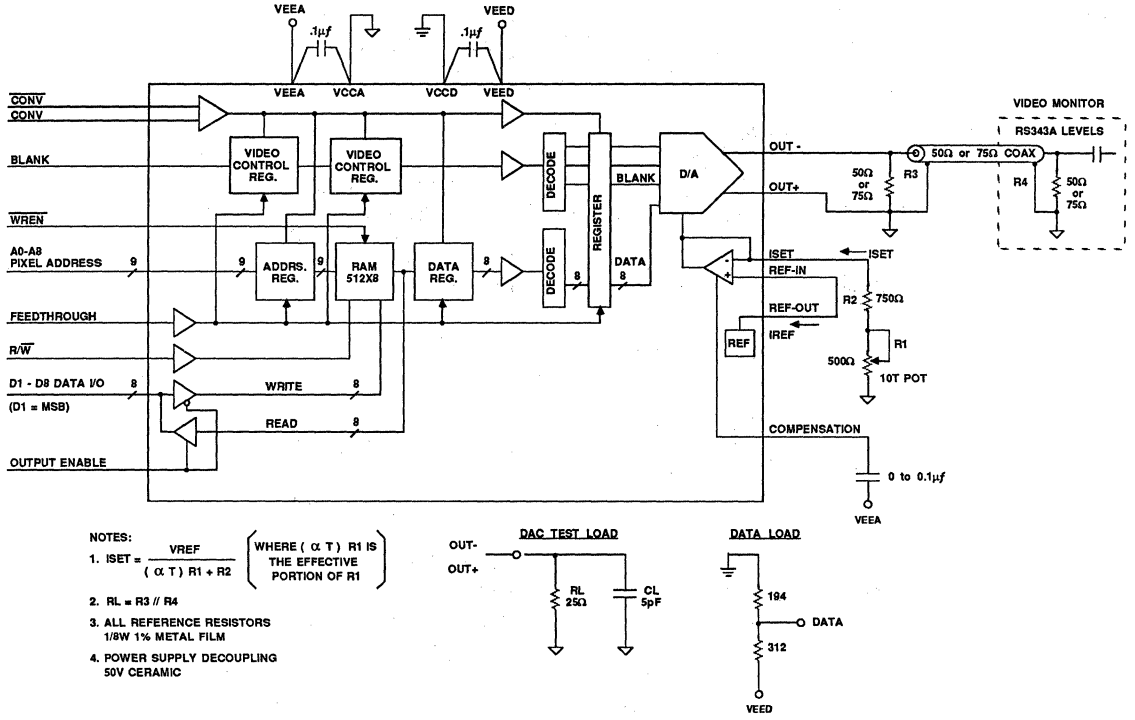
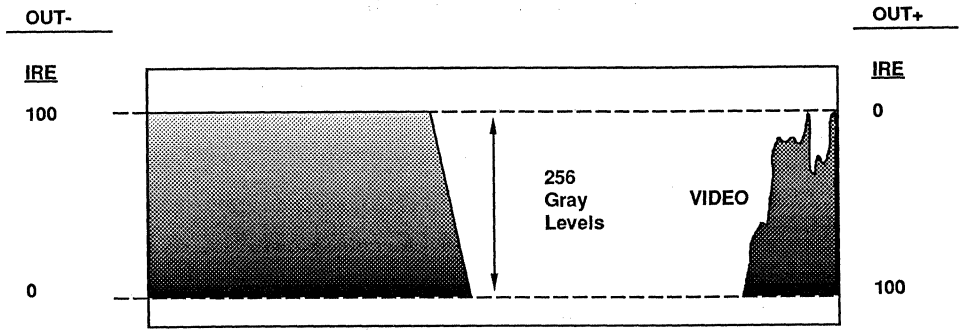


FIGURE 1: TYPICAL APPLICATIONS CIRCUIT



			OUT-			OUT+		
BLANK	RAM DATA	DESCRIPTION	(mA)	(V)	(IRE)	(mA)	(V)	(IRE)
1	X	BLANK	19.04	-0.714	0	0	0	0
0	000...	BLACK	19.04	-0.714	0	0	0	0
0	111...	WHITE	0	0	100	19.04	-0.714	100

Note: ISET = 1.792 mA, RL= 25Ω, Adjusted For Gain and Offset

FIGURE 2: VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

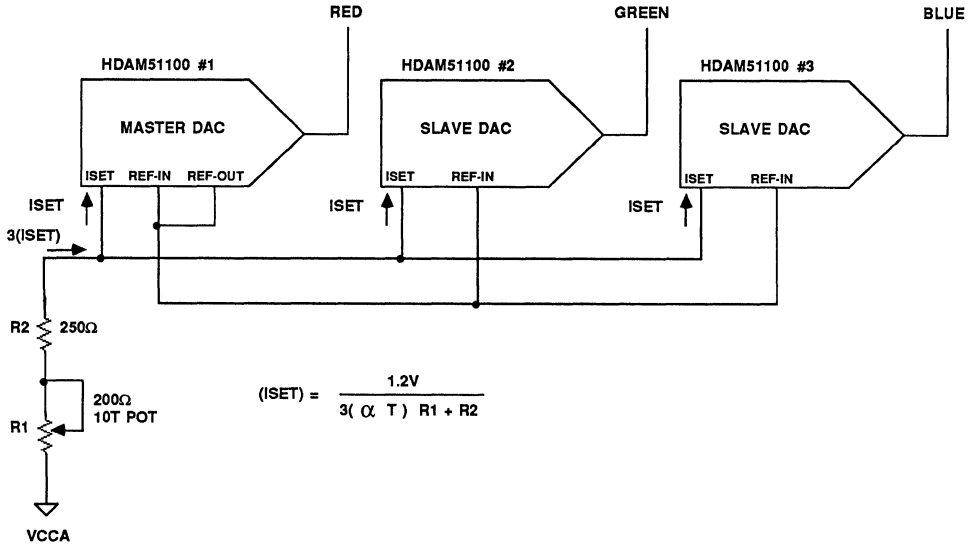


FIGURE 3: RGB SYSTEM USING A COMMON DAC REFERENCE AND COMMON REFERENCE ADJUSTMENT

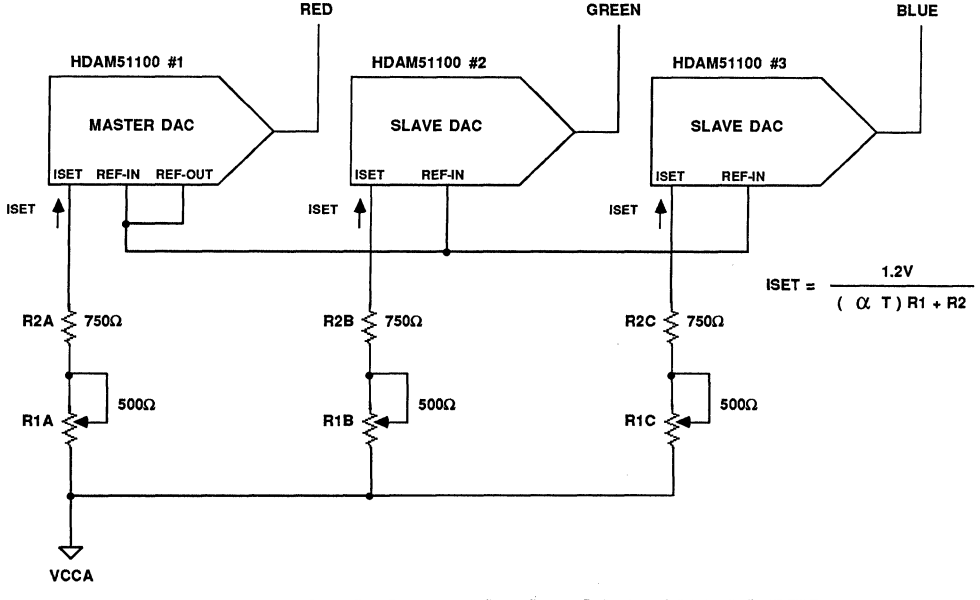


FIGURE 4: RGB SYSTEM USING A COMMON DAC REFERENCE AND INDIVIDUAL REFERENCE ADJUSTMENT

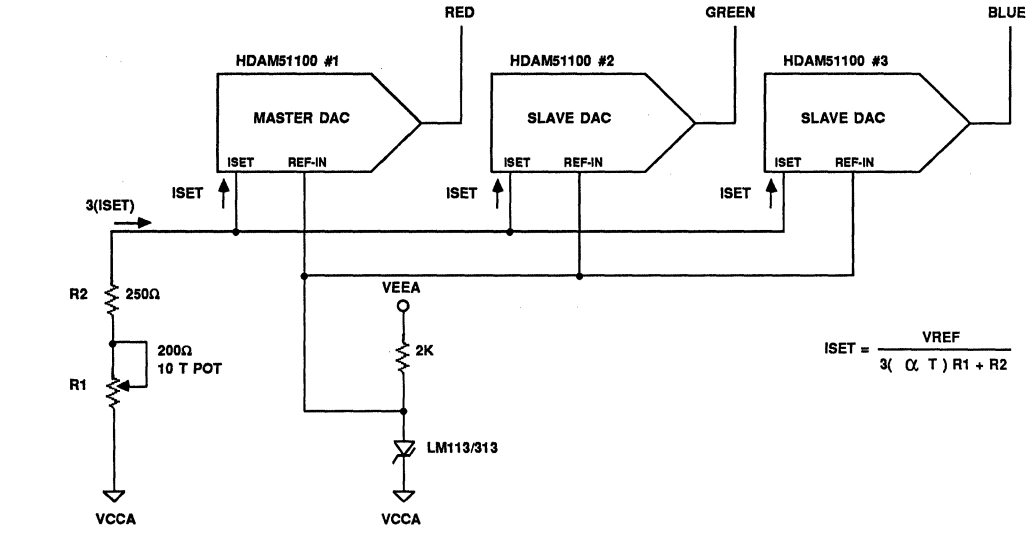


FIGURE 5: RGB SYSTEM USING AN EXTERNAL REFERENCE AND COMMON REFERENCE ADJUSTMENT

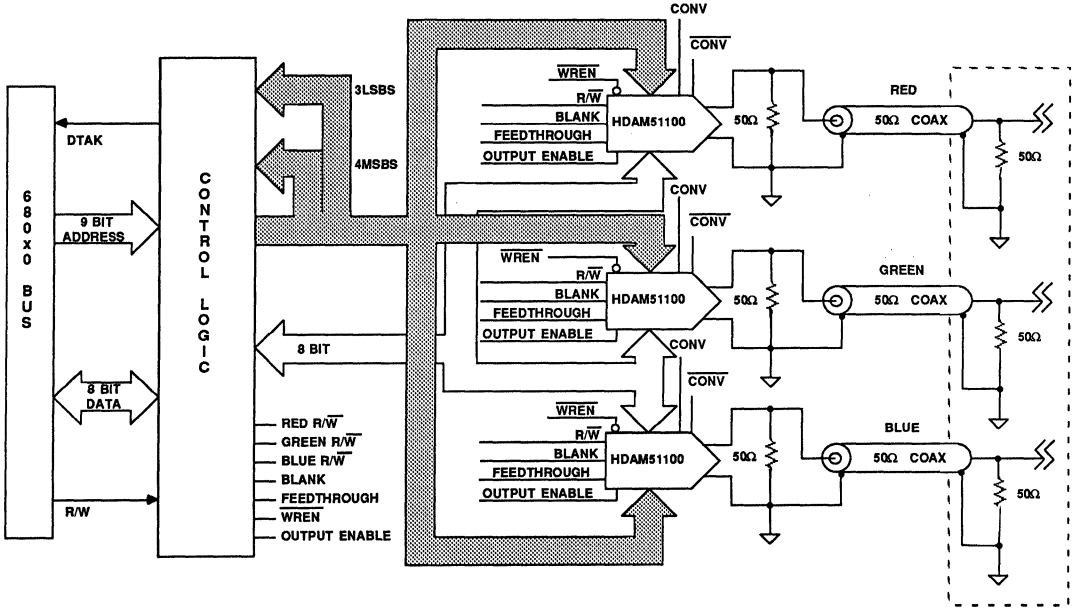


FIGURE 6: 680X0 RGB SYSTEM BLOCK DIAGRAM

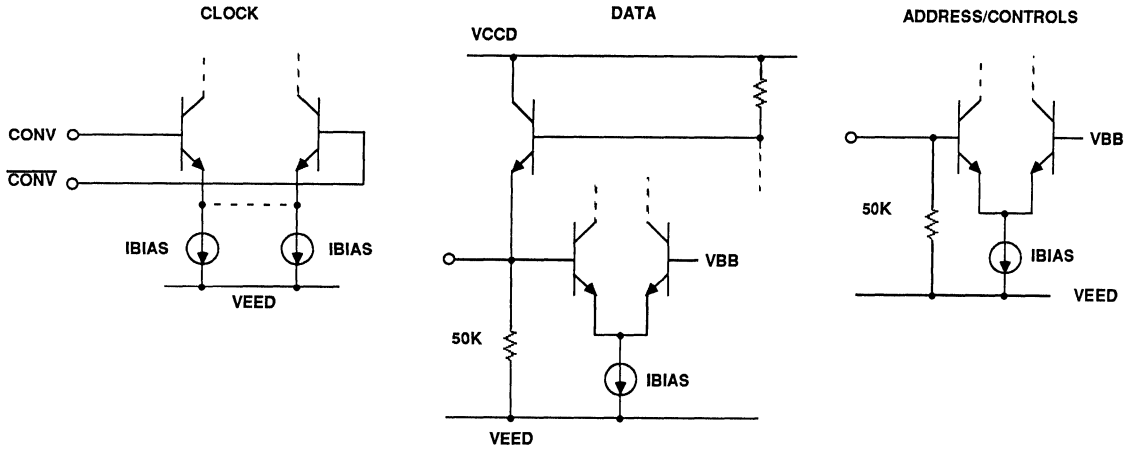


FIGURE 7: EQUIVALENT INPUT CIRCUITS - CLOCK, DATA AND ADDRESS/CONTROLS

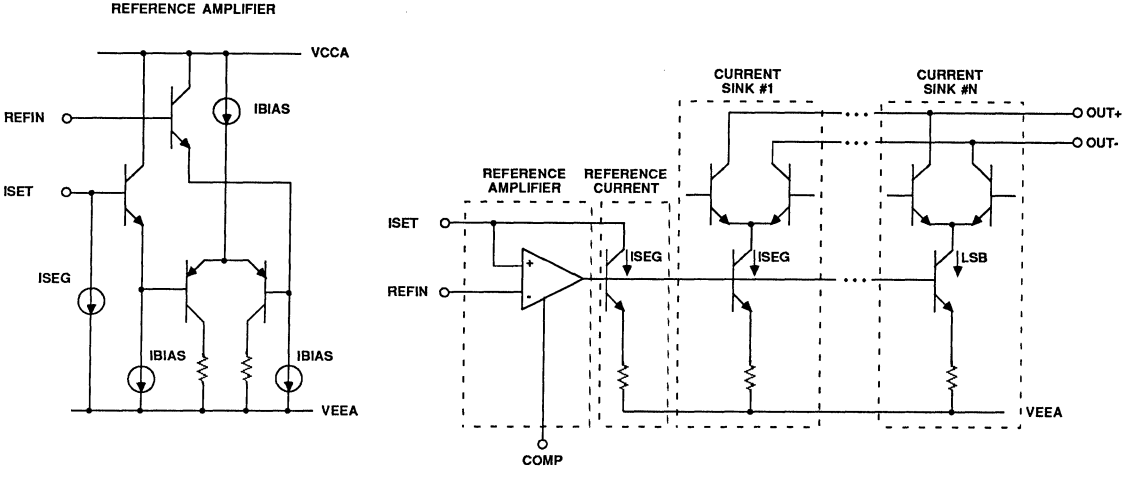
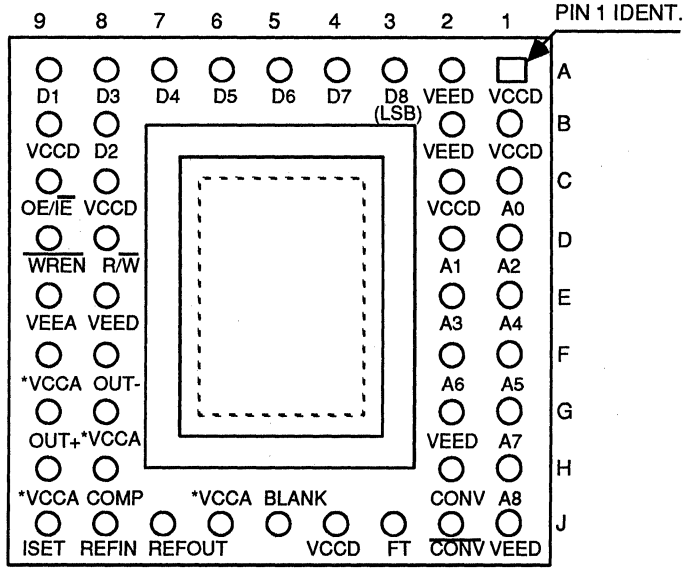


FIGURE 8: EQUIVALENT CIRCUITS - DAC AND REFERENCE AMPLIFIER

COLUMN	ROW	PIN NAME	COLUMN	ROW	PIN NAME
A	1	VCCD	E	2	A3
A	2	VEED	E	8	VEED
A	3	D8 (LSB)	E	9	VEEA
A	4	D7			
A	5	D6	F	1	A5
A	6	D5	F	2	A6
A	7	D4	F	8	OUT-
A	8	D3	F	9	*VCCA
A	9	D1 (MSB)			
			G	1	A7
B	1	VCCD	G	2	VEED
B	2	VEED	G	8	VCCA
B	8	D2	G	9	OUT+
B	9	VCCD			
C	1	A0	H	1	A8
C	2	VCCD	H	2	CONV
C	8	VCCD	H	8	COMP
C	9	OE/$\overline{IE}$ - DATA INPUT/ OUTPUT SELECT	H	9	*VCCA
			J	1	VEED
D	1	A2	J	2	$\overline{CONV}$
D	2	A1	J	3	FT
D	8	$\overline{R/W}$ - DATA READ/ WRITE SELECT	J	4	VCCD
			J	5	BLANK
D	9	$\overline{WREN}$ - DATA WRITE ENABLE	J	6	*VCCA
			J	7	REFOUT
			J	8	REFIN
E	1	A4	J	9	ISET

HDAM51100 PACKAGING INFORMATION
46 PIN GRID ARRAY



Bottom View

NOTES:

*NO INTERNAL CONNECTION - CONNECT TO VCCA FOR INTERELECTRODE SHIELDING

**For Ordering Information See Section 1.*

HCMP96850

SINGLE ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay < 2.5ns
- Propagation Delay Skew < 300ps
- 100MHz Minimum Tracking Bandwidth
- Low Offset ± 1mV
- Low Feedthrough
- Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

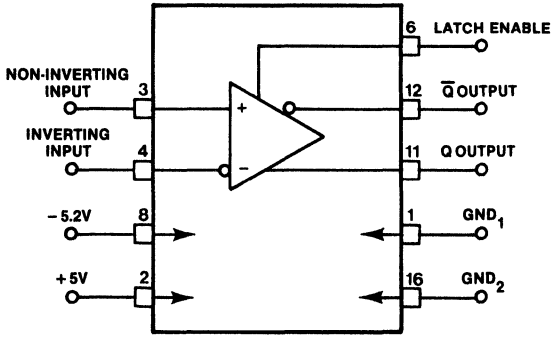
The HCMP96850 is a single, very high speed, monolithic comparator. It is pin-compatible with, and has improved performance over Plessey's SP9685 and AMD's AM6685. The HCMP96850 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96850 is available in 16 Lead DIP, or in die form.

BLOCK DIAGRAM

HCMP96850 HIGH SPEED COMPARATOR



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (V_{CC} measured to GND) . . . . . − 0.5 to + 6.0V
Negative Supply Voltage (V_{EE} to GND) . . . − 6.0 to + 0.5V
Ground Voltage Differential . . . . . − 0.5 to + 0.5V

Input Voltages
Input Voltage . . . . . − 4.0 to + 4.0V
Differential Input Voltage . . . . . − 5.0 to + 5.0V
Input Voltage, Latch Controls . . . . . V_{EE} to 0.5V

Output
Output Current 30mA

Temperature
Operating Temperature, ambient . . . . . − 55 to + 125°C
junction . . . . . + 150°C
Lead Temperature, (soldering 60 seconds) . . . . + 300°C
Storage Temperature . . . . . − 65 to + 150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

INDUSTRIAL TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS							
T_A = 25°C, V_{CC} = + 5.0V ± .25V, V_{EE} = − 5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
V_{OS}	Input Offset Voltage	R_S = 0 Ohms	I	− 3		+ 3	mV
V_{OS}	Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$[2]	IV	− 3.5		+ 3.5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco		V		4		µV/°C
I_{BIAS}	Input Bias Current		I		4	± 20	µA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}$[2]	IV		7		µA
I_{OS}	Input Offset Current		I	− 1.0		+ 1.0	µA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}$[2]	IV	− 1.3		+ 1.3	µA
I_{CC}	Positive Supply Current		I		3.3	5	mA
I_{EE}	Negative Supply Current		I		13.5	18	mA
V_{CM}	Common Mode Range		I	− 2.5		+ 2.5	V
A_{VOL}	Open Loop Gain		V		4000		V/V
R_{IN}	Input Resistance		V		60		KOhms
C_{IN}	Input Capacitance		V		3		pF
C_{IN}	Input Capacitance	(LCC Package)	V		1		pF
PSS	Power Supply Sensitivity		I	70			dB
CMRR	Common Mode Rejection Ratio		I	80			dB
P_D	Power Dissipation Single		I			125	mW
OUTPUT LOGIC LEVELS (ECL 10KH Compatible)							
V_{OH}	Output High	50 Ohms to − 2V	I	− .98		− .81	V
V_{OL}	Output Low	50 Ohms to − 2V	I	− 1.95		− 1.63	V

INDUSTRIAL TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS							
T_A 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
t_P	Propagation Delay	10mV O.D.	I		2.4	3	ns
t_S	Latch Set-up Time				0.6		ns
$t_P(E)$	Latch to Output Delay	50mV O.D.			3		ns
$t_{PW}(E)$	Latch Pulse Width				2		ns
$t_H(E)$	Latch Hold Time				0.5		ns
t_r	Rise Time	20% to 80%			1.76		ns
t_f	Fall Time	20% to 80%			1.76		ns
f_c	Min Clock Rate				300		MHz

Notes:
1. 100mV input step.
2. Temperature Range −25 to +85°C

MILITARY TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS							
T_A = 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
V_{OS}	Input Offset Voltage	R_S = 0 Ohms	I	−3		+3	mV
V_{OS}	Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$[2]	I	−4		+4	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco		V		4		µV/°C
I_{BIAS}	Input Bias Current		I		4	±20	µA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}$[2]	I	−50	7	50	µA
I_{OS}	Input Offset Current		I	−1.0		+1.0	µA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}$[2]	I	−7		+7	µA
I_{CC}	Positive Supply Current		I		7	10	mA
I_{EE}	Negative Supply Current		I		27	36	mA
V_{CM}	Common Mode Range		I	−2.5		+2.5	V
A_{VOL}	Open Loop Gain		V		4000		V/V
R_{IN}	Input Resistance		V		60		KOhms
C_{IN}	Input Capacitance		V		3		pF
C_{IN}	Input Capacitance	(LCC Package)	V		1		pF

MILITARY TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS							
T_A = 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
PSS	Power Supply Sensitivity	Over Temp		70 58			dB
CMRR	Common Mode Rejection Ratio	Over Temp		−80 −68			dB
P_D	Power Dissipation Single		I			125	mW
OUTPUT LOGIC LEVELS (ECL 10KH Compatible)							
V_{OH}	Output High	50 Ohms to −2V	I	−.98		−.81	V
V_{OL}	Output Low	50 Ohms to −2V	I	−1.95		−1.63	V
AC ELECTRICAL CHARACTERISTICS							
T_A25°C, V_{CC} = +5.0V ± .25V, V_{EE} = 5.2V ±.3V, R_L = 50 Ohms (Unless otherwise specified)							
t_P	Propagation Delay	10mV O.D.	I		2.4	3	ns
t_S	Latch Set-up Time				0.6		ns
$t_P(E)$	Latch to Output Delay	50mV O.D.			3		ns
$t_{PW}(E)$	Latch Pulse Width				2		ns
$t_H(E)$	Latch Hold Time				0.5		ns
t_r	Rise Time	20% to 80%			1.76		ns
t_f	Fall Time	20% to 80%			1.76		ns
f_c	Min Clock Rate				300		MHz

Notes:

1. 100mV input step.
2. Temperature Range −55 to +125°C

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperatures.
II	100% production tested at Ta = 25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

GENERAL INFORMATION

The HCMP96850 is an ultra high speed single voltage comparator. It offers tight absolute characteristics which guarantee matching from package-to-package. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

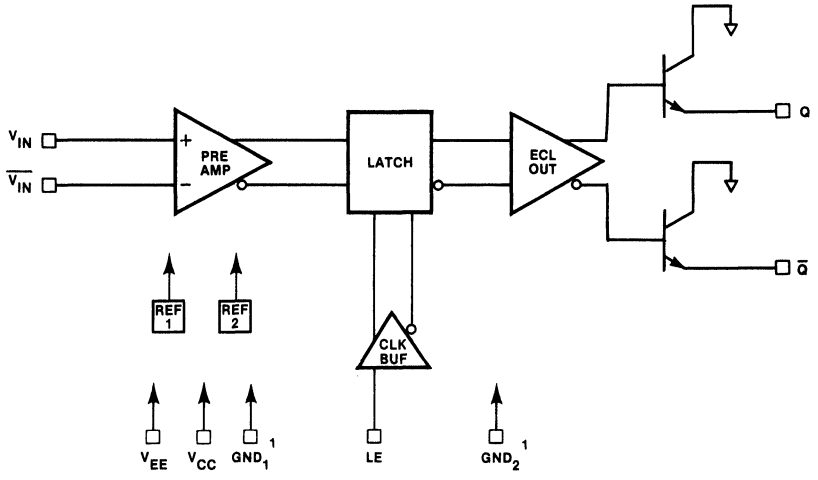
The HCMP96850 has one latch enable control and can be driven by standard ECL logic. It also has two separate ground pins, one for the output to accommodate large ground currents without affecting the rest of the circuit, while the other is for the small signal intermediate stages. The input stage is referenced to V_{CC} and V_{EE}.

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

INTERNAL FUNCTIONAL DIAGRAM



NOTES: 1. HCMP96850 HAS SEPARATE OUTPUT AND INTERMEDIATE STAGE GROUND PINS

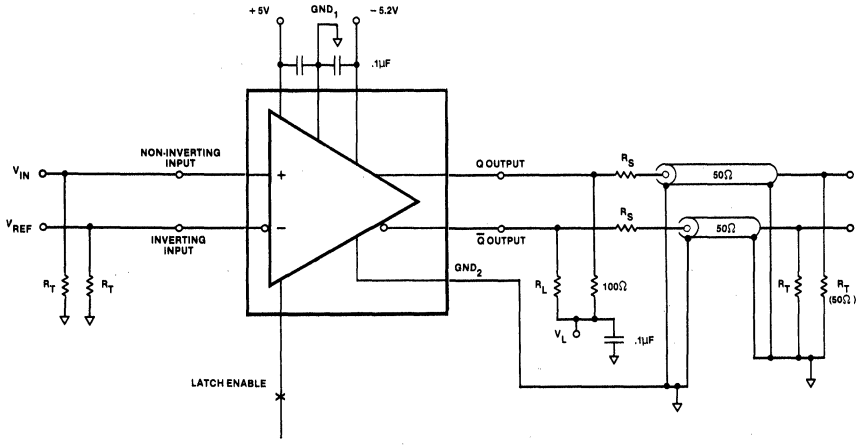
TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96850 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96850 is capable of driving 50 Ohm terminated lines. The termination can be directly tied to $-2.0V$, or a Thevenin equivalent terminated to the negative supply if a $-2.0V$ supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

FIGURE 1 HCMP96850 TYPICAL INTERFACE CIRCUIT



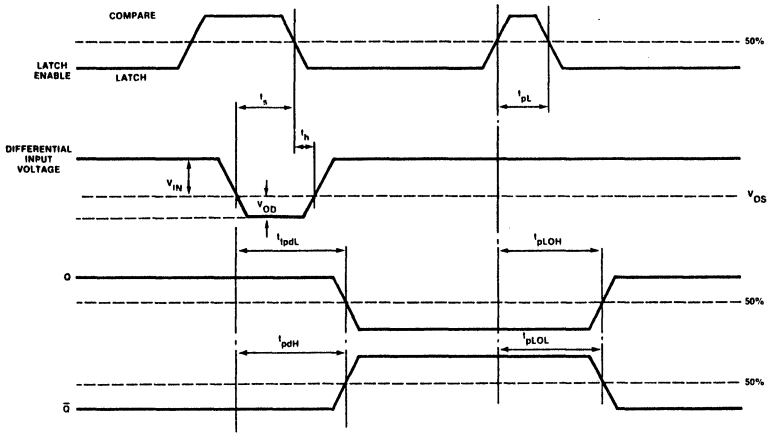
——×—— = ECL TERMINATION.

The timing diagram for the comparator is shown in Figure 2. The latch enable (LE) pulse is shown at the top. If LE is high in the HCMP96850, the comparator tracks the input difference voltage. When LE is driven low the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the latch enable falling edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

FIGURE 2 TIMING DIAGRAM



V_{IN} = 100mV, V_{OD} = 10mV

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

SWITCHING TERMS (refer to Figure 2)

t_{pdH} — INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} — INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} — LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

t_{pLOL} — LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_S — MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h — MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} — MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

t_{pdL}-t_{pdH} — DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.

t_{pLOL}-t_{pLOH} — DIFFERENTIAL PROPAGATION DELAY (SKEW) LATCH TO OUTPUT - The skew from one comparator to another.

V_{OD} — VOLTAGE OVERDRIVE.

FIGURE 3 EQUIVALENT INPUT CIRCUIT

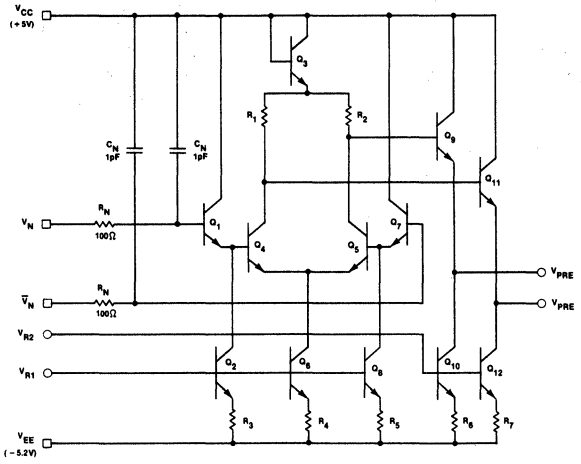


FIGURE 4 OUTPUT CIRCUIT

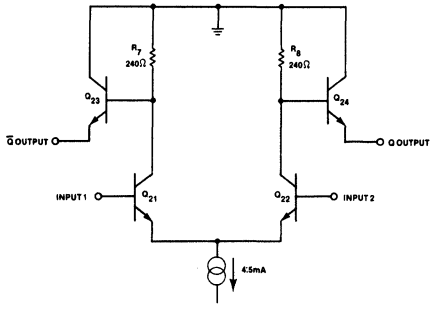


FIGURE 5A TEST LOAD

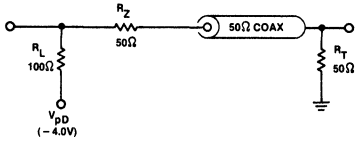
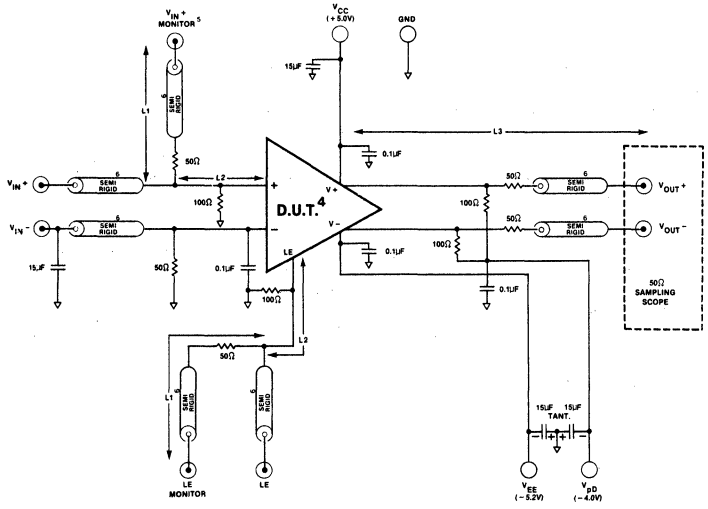
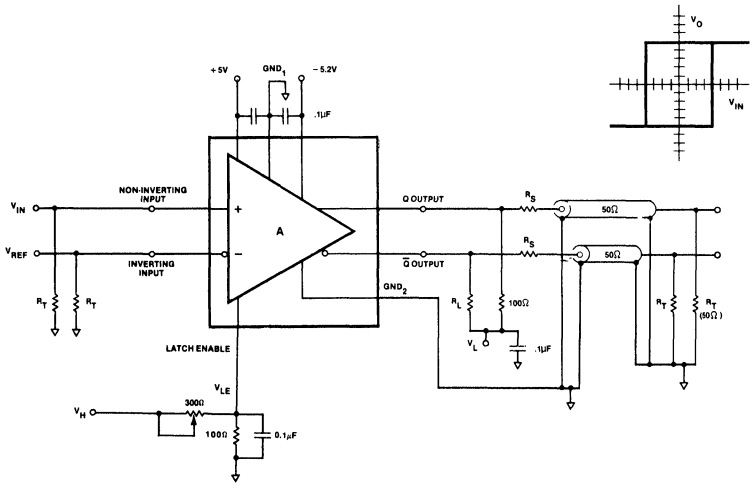


FIGURE 5B AC TEST FIXTURE



NOTES:
1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (50Ω = 49.9Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50Ω TO GND.
6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

FIGURE 6 HCMP96850 WITH HYSTERESIS

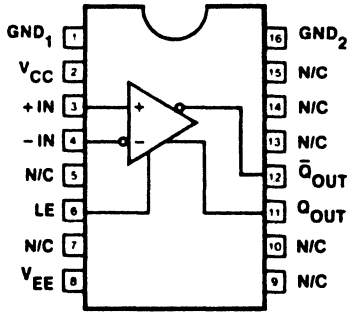


HYSTERESIS IS OBTAINED BY APPLYING A DC BIAS TO THE LE PIN
$V_H = -5.2V$
$V_{LE} = -1.3V \pm 100mV$

4

PIN ASSIGNMENTS

TOP VIEW



16 LEAD CERDIP

PIN FUNCTIONS

NAME	FUNCTION
GND1	Circuit Ground
VCC	Positive Supply Voltage
+ IN	Non-Inverting Input
− IN	Inverting Input
N/C	No Connection
LE	Latch Enable
VEE	Negative Supply Voltage
QOUT	Output
$\overline{Q}$OUT	Inverted Output
GND2	Output Ground

**For Ordering Information See Section 1.*

NOTES:

HCMP96870A

DUAL ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay < 2.3ns
- Propagation Delay Skew < 300ps
- 300MHz Minimum Tracking Bandwidth
- Low Offset ± 1mV
- Low Feedthrough and Crosstalk
- Differential Latch Control – Dual Version

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

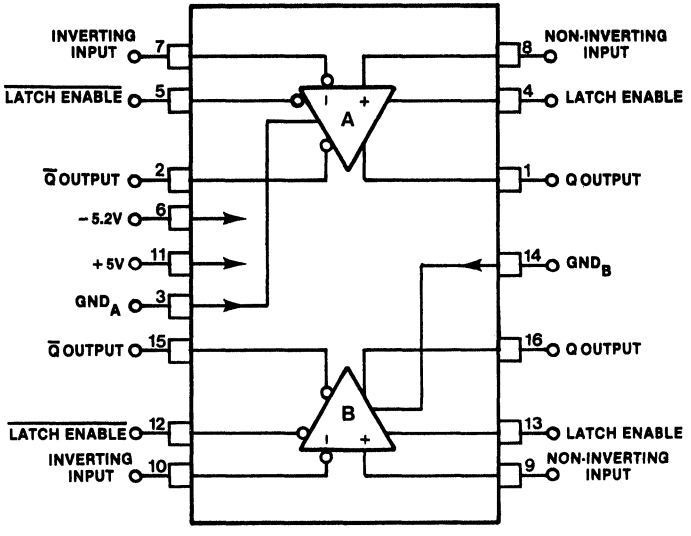
The HCMP96870A is a dual, very high speed monolithic comparators. It is pin-compatible with, and has improved performance over Plessey's SP9687 and AMD's AM6687. The HCMP96870 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96870A is available in 16 Lead CERDIP, 20 Contact Leadless Chip Carriers (LCC), or in die form.

BLOCK DIAGRAM

HCMP96870 DUAL HIGH SPEED COMPARATOR



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (V_{CC} measured to GND) . . . . . −0.5 to +6.0V
Negative Supply Voltage (V_{EE} to GND) . . . −6.0 to +0.5V
Ground Voltage Differential . . . . . −0.5 to +0.5V

Input Voltages
Input Voltage . . . . . −4.0 to +4.0V
Differential Input Voltage . . . . . −5.0 to +5.0V
Input Voltage, Latch Controls . . . . . V_{EE} to 0.5V

Output
Output Current 30mA

Temperature
Operating Temperature, ambient . . . . . −55 to +125°C
junction . . . . . +150°C
Lead Temperature, (soldering 60 seconds) . . . . +300°C
Storage Temperature . . . . . −65 to +150°C

Notes:
1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

INDUSTRIAL TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS							
T_A = 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
V_{OS}	Input Offset Voltage	R_S = 0 Ohms	I	−3		+3	mV
V_{OS}	Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$[2]	IV	−3.5		+3.5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco		V		4		µV/°C
I_{BIAS}	Input Bias Current		I		4	±20	µA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}$[2]	IV		7		µA
I_{OS}	Input Offset Current		I	−1.0		+1.0	µA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}$[2]	IV	−1.3		+1.3	µA
I_{CC}	Positive Supply Current		I		3.3	5	mA
I_{EE}	Negative Supply Current		I		13.5	18	mA
V_{CM}	Common Mode Range		I	−2.5		+2.5	V
A_{VOL}	Open Loop Gain		V		4000		V/V
R_{IN}	Input Resistance		V		60		KOhms
C_{IN}	Input Capacitance		V		3		pF
C_{IN}	Input Capacitance	(LCC Package)	V		1		pF
PSS	Power Supply Sensitivity		I	70			dB
CMRR	Common Mode Rejection Ratio		I	80			dB
P_D	Power Dissipation Dual		I			250	mW
OUTPUT LOGIC LEVELS (ECL 10KH Compatible)							
V_{OH}	Output High	50 Ohms to −2V	I	−.98		−.81	V
V_{OL}	Output Low	50 Ohms to −2V	I	−1.95		−1.63	V

INDUSTRIAL TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS T_A 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
t_P	Propagation Delay	10mV O.D.	I		2.0	2.3	ns
t_S	Latch Set-up Time				0.6		ns
$t_{P(E)}$	Latch to Output Delay	50mV O.D.			3		ns
$t_{PW(E)}$	Latch Pulse Width				2		ns
$t_{H(E)}$	Latch Hold Time				0.5		ns
t_r	Rise Time	20% to 80%			1.2		ns
t_f	Fall Time	20% to 80%			1.2		ns
f_c	Min Clock Rate				300		MHz

Notes:
1. 100mV input step.
2. Temperature Range −25 to +85°C

MILITARY TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
V_{OS}	Input Offset Voltage	R_S = 0 Ohms	I	−3		+3	mV
V_{OS}	Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$[2]	I	−4		+4	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco		V		4		µV/°C
I_{BIAS}	Input Bias Current		I		4	±20	µA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}$[2]	I	−50	7	50	µA
I_{OS}	Input Offset Current		I	−1.0		+1.0	µA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}$[2]	I	−7		+7	µA
I_{CC}	Positive Supply Current		I		7	10	mA
I_{EE}	Negative Supply Current		I		27	36	mA
V_{CM}	Common Mode Range		I	−2.5		+2.5	V
A_{VOL}	Open Loop Gain		V		4000		V/V
R_{IN}	Input Resistance		V		60		KOhms
C_{IN}	Input Capacitance		V		3		pF
C_{IN}	Input Capacitance	(LCC Package)	V		1		pF

MILITARY TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS							
T_A = 25°C, V_{CC} = +5.0V ± .25V, V_{EE} = −5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
PSS	Power Supply Sensitivity	Over Temp		70 58			dB
CMRR	Common Mode Rejection Ratio	Over Temp		−80 −68			dB
P_D	Power Dissipation Dual		I			250	mW
OUTPUT LOGIC LEVELS (ECL 10KH Compatible)							
V_{OH}	Output High	50 Ohms to −2V	I	−.98		−.81	V
V_{OL}	Output Low	50 Ohms to −2V	I	−1.95		−1.63	V
AC ELECTRICAL CHARACTERISTICS							
T_A25°C, V_{CC} = +5.0V ± .25V, V_{EE} = 5.2V ± .3V, R_L = 50 Ohms (Unless otherwise specified)							
t_P	Propagation Delay	10mV O.D.	I		2.0	2.3	ns
t_S	Latch Set-up Time				0.6		ns
$t_P(E)$	Latch to Output Delay	50mV O.D.			3		ns
$t_{PW}(E)$	Latch Pulse Width				2		ns
$t_H(E)$	Latch Hold Time				0.5		ns
t_r	Rise Time	20% to 80%			1.2		ns
t_f	Fall Time	20% to 80%			1.2		ns
f_c	Min Clock Rate				300		MHz

Notes:

1. 100mV input step.
2. Temperature Range −55 to +125°C

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics that follow are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL	TEST PROCEDURE
I	Production tested.
II	Parameter is guaranteed by sample testing.

GENERAL INFORMATION

The HCMP96870A is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

The HCMP96870A has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

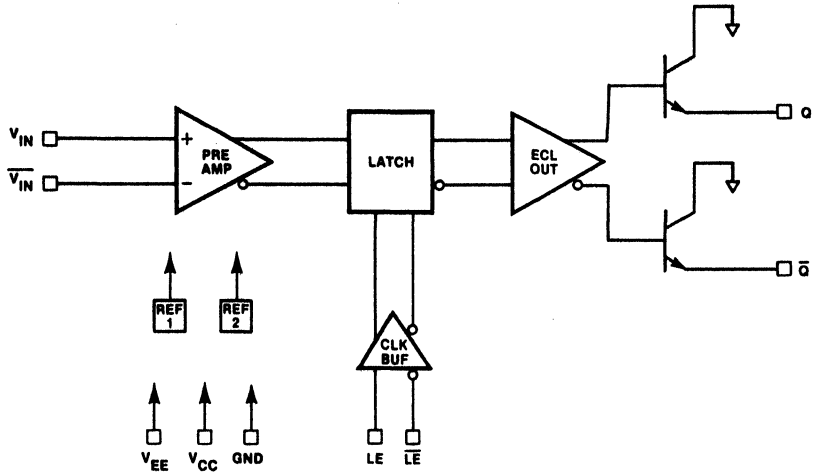
The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection. The output stage ground and intermediate ground are separated on the die, but are not bonded to the same pin.

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power for SMD packaging and low system power
- Good rejection between comparator channels
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

INTERNAL FUNCTIONAL DIAGRAM



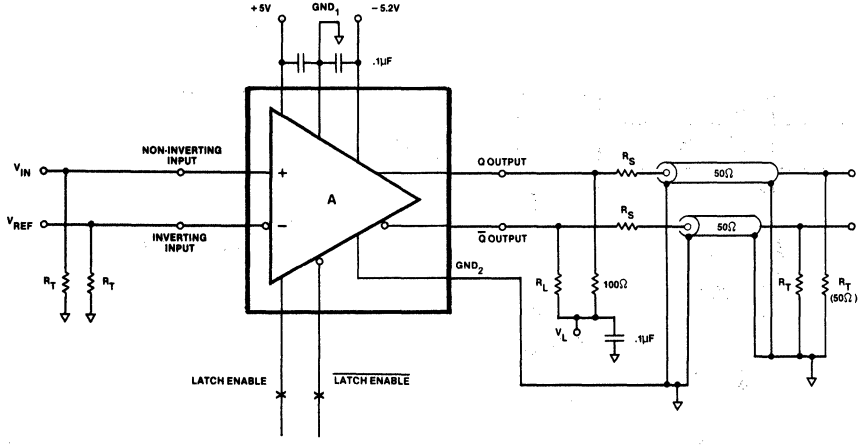
TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96870A comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96870A is capable of driving 50 Ohm terminated lines. The termination can be directly tied to −2.0V, or a Thevenin equivalent terminated to the negative supply if a −2.0V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

FIGURE 1 HCMP96870A TYPICAL INTERFACE CIRCUIT



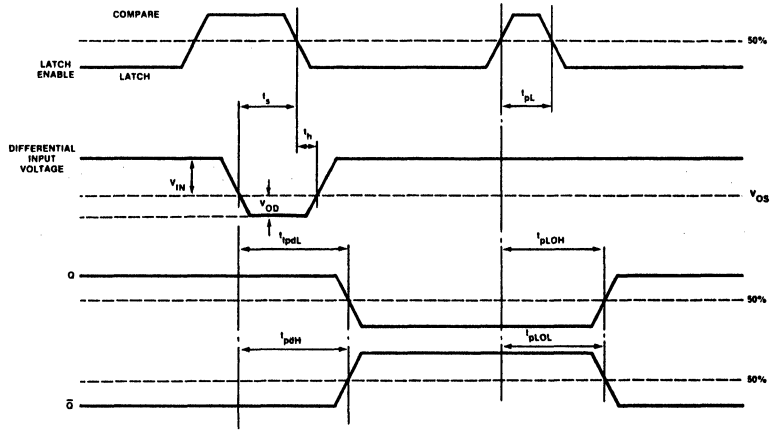
——×—— = ECL TERMINATION.

The timing diagram for the comparator is shown in Figure 2. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the HCMP96870A, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the latch enable falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

FIGURE 2 TIMING DIAGRAM



V_{IN} = 100mV, V_{OD} = 10mV

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected. (LE is the inverse of $\overline{LE}$.)

SWITCHING TERMS (refer to Figure 2)

t_{pdH} — INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} — INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} — LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

t_{pLOL} — LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_S — MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h — MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} — MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

t_{pdL}-t_{pdH} — DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.

t_{pLOL}-t_{pLOH} — DIFFERENTIAL PROPAGATION DELAY (SKEW) LATCH TO OUTPUT - The skew from one comparator to another.

V_{OD} — VOLTAGE OVERDRIVE.

FIGURE 3 EQUIVALENT INPUT CIRCUIT

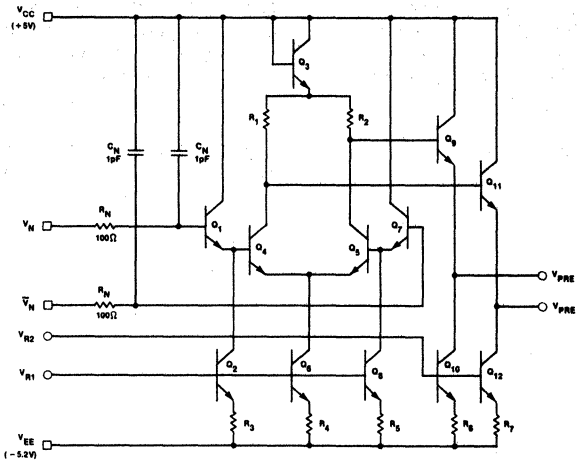


FIGURE 4 OUTPUT CIRCUIT

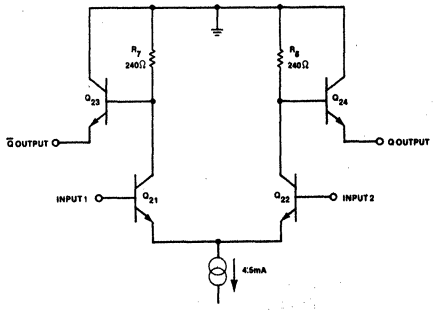


FIGURE 5A TEST LOAD

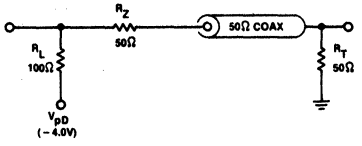
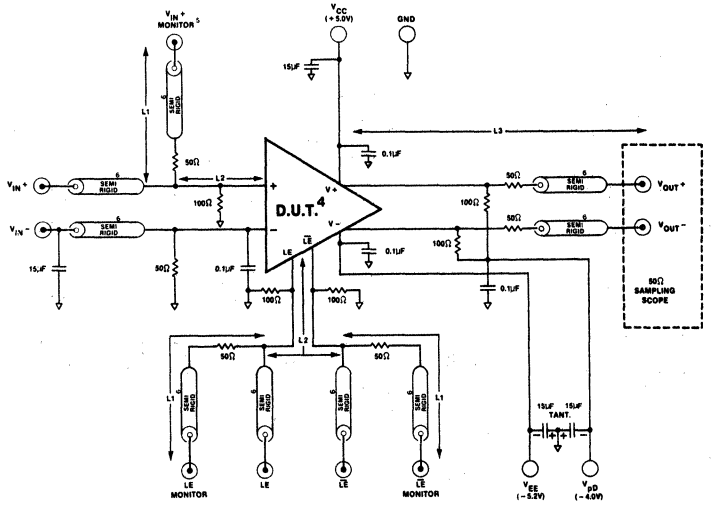
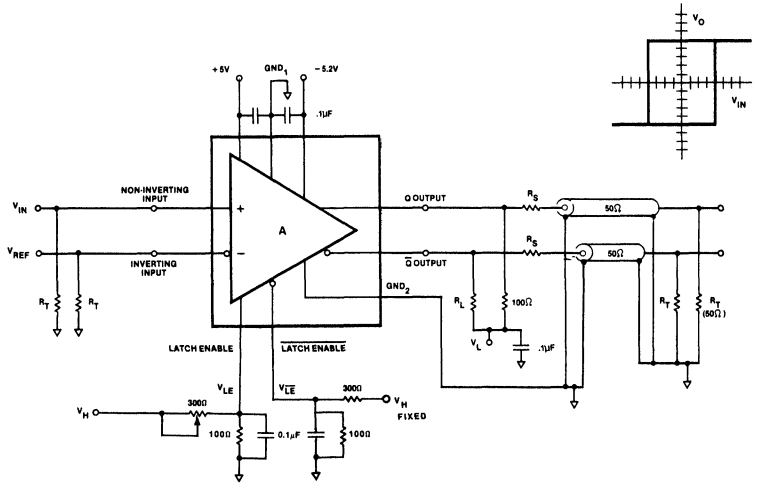


FIGURE 5B AC TEST FIXTURE



NOTES:
1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (50Ω = 49.9Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50Ω TO GND.
6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

FIGURE 6 HCMP96870A WITH HYSTERESIS



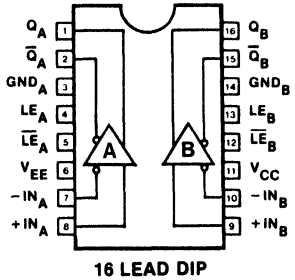
HYSTERESIS IS OBTAINED BY APPLYING A DC BIAS TO THE LE PIN

$V_H = -5.2V$

$V_{LE} = -1.3V \pm 100mV$, $V_{\overline{LE}} = -1.3V$

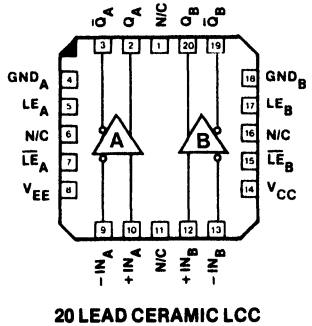
PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

TOP VIEW



20 LEAD CERAMIC LCC

PIN FUNCTIONS

NAME	FUNCTION
$\overline{Q}_A$	Output A
Q_A	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
$\overline{LE}_B$	Inverted Latch Enable B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

**For Ordering Information See Section 1.*

NOTES:

HCMP96900

DUAL HIGH SPEED, WIDE VOLTAGE RANGE COMPARATOR

PRELIMINARY INFORMATION

FEATURES:

- Wide Input Range -8 To +13V
- Input Protected to 1V Above Supplies
- Constant Propagation Delays
- High Speed - 4.2ns Propagation Delay
- Constant Input Current

APPLICATIONS:

- ATE Pin Receivers
- Timing Ramp Generators
- Line Receivers
- High Speed Window Detectors

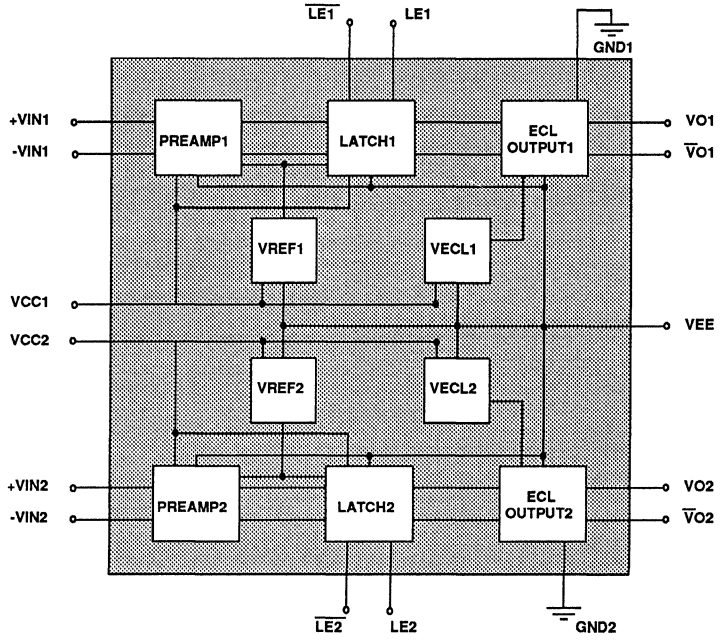
GENERAL DESCRIPTION

The HCMP96900 is a dual, high speed, wide common mode voltage comparator. It is designed for applications measuring critical timing parameters where wide common mode input voltages are required. Propagation delays are constant for varying input slew rates, common mode voltage, overdrive or polarity. Input protection is provided to one volt in excess of the power supplies to ease design of input protection circuitry.

For many applications, the comparator allows the designer to input signals directly into the comparator without the need for either very high speed voltage dividers or buffers. Therefore, designs are easy to protect, high in reliability, and lower in power and space than previous high speed comparators. The device is available in an 18-pin ceramic sidebrazed dip, 20 lead LCC or in die form.

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS 25°C (1)

Operating Temperature Range.....-25 to +85°C
Positive Supply Voltage .....+18.0V
Negative Supply Voltage.....- 13.0V

Differential Supply Voltage.....24V
Input Voltage Range.....VEE -1.0V to VCC +1.0V
Power Dissipation.....800mW
Differential Input Voltage.....±24.0V
Output Current.....40mA

(1) Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

Industrial Temperature Range

Vcc =+12.0V, Vee = -7.0V, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C Min	Room +25°C Typ	Room +25°C Max	Hot +85°C Min	Hot +85°C Typ	Hot +85°C Max	Cold -25°C Min	Cold -25°C Typ	Cold -25°C Max	Units
Input Offset Voltage			-3.0	±0.5	+3.0							mV
ΔVOS/ΔT				20								µV/°C
Input Offset Current	VIN = 0.0V				1.0							µA
Input Bias Current	VIN = 0.0V			8	20							µA
ΔIBIAS/ΔVIN	-2V <VIN <5V			0.1	0.3							µA/V
Input Capacitance	LCC			2								pF
Power Supply Rejection Ratio			80									dB
Common Mode Rejection Ratio			80									dB
Input Common Mode Range			-3.0		10.0							V
Differential Input Voltage Range			13.0									V
Gain				60								dB
Common Mode Input Resistance	-2V <VIN <5V			10								MOhm
Differential Mode Input Resistance				2.5								MOhm
Input Hysteresis				2								mV
Crosstalk												dB
Positive Supply Current				25								mA
Negative Supply Current				60								mA
Power Dissipation												Watts
Output High Voltage	50 Ohms to -2.0V		-.98		-.81							V
Output Low Voltage	50 Ohms to -2.0V		-1.95		-1.63							V
Input High Voltage			-1.13		-.81							V
Input Low Voltage			-1.95		-1.48							V

(1) See page 3.

ELECTRICAL SPECIFICATIONS

Industrial Temperature Range

Vcc =+12.0V, Vee = -7.0V, unless otherwise specified.

AC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C Min Typ Max	Hot +85°C Min Typ Max	Cold -25°C Min Typ Max	Units
Propagation Delay	50mV Overdrive		4.2			ns
Propagation Delay	10mV Overdrive					ns
Output Rise/Fall Time	10% to 90%		1.6			ns
Input Slew Rate			1.5			V/ns
Latch Set-Up Time						ns
Latch Hold Time						ns
Minimum Latch Pulse Width						ns
tp with 100mVOD minus tp with 500mVOD (2)	VIN = +1.0V		100			ps
tp with 100m VOD minus tp with 500mVOD (2)	VIN = -1.0V		100			ps
tp with 100mVOD minus tp with 500mVOD (2)	VIN = +10.0V		100			ps
tp with 100mVOD minus tp with 500mVOD (2)	VIN = -10.0V		100			ps
10ns Pulse Reproduction			60			ps

(1) All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level Column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests performed after a three minute power soak.

Test Level I - 100% production tested at the specified temperatures.
Test Level II - 100% production tested at Ta=25°C and sample tested at the specified temperatures.
Test Level III - QA sample tested only at the specified temperatures.
Test Level IV - Parameter is guaranteed (but not tested) by design and characterization data.
Test Level V - Parameter is a typical value for information purposes only.

(2) Propagation delay with 100mV overdrive minus propagation delay with 500mV overdrive.

INPUT

The input of the HCMP96900 is designed to accept wide common mode and differential voltages. With the standard supplies of +12.0V and -7.0V the input voltage range (both common mode and differential) is +10.0V to -3.0V. If a wider or different range is desired, either supply can be changed within the following limits: The positive supply should not exceed +15.0V nor be less than +10.0V. The negative supply should not be greater than -3.3V nor be less than -12.0V. Total differential supply voltage should not exceed 22V. Input voltage range is always VCC -2.0V to VEE +4.0V, and differential input range is equal to the common mode range. (See Figure 2)

PROPAGATION DELAY

Propagation delay has been designed to be as constant as possible with a wide variety of input conditions. For all conditions given below the 25°C deltas in delays are typically 100ps, increasing to a typical 250ps at 85°C ambient. For this reason keeping the devices as cool as possible is desirable. Propagation delay has been designed to be constant, independent of edge direction, common mode voltage, input slew rate (up to 1.5V/ns) or over-drive. Over-drive deltas are specified between l00mV and 500mV because these are the types of values seen in test systems. As the over-drive becomes greater than 500mV, very little change in the delay occurs.

Controlled delays result in very accurate pulse reproduction. For characterization a 10ns pulse is input into the comparator and the time between its 50% points are measured. The output pulse from the comparators is then measured. The difference in time is typically 60ps at 25°C and decreases to half this value at 85°C.

PULSE DETECTION

Digital ATE testing often requires the detection of pulses that are much shorter than the signals that are being measured. This is required to detect glitches in outputs from tested digital products. The HCMP96900 can detect pulses as narrow as 1.5ns in the unlatched mode and still output full ECL swings.

INPUT BIAS CURRENT

High speed comparators are often used as integrators with a current source charging a capacitor on the input. this circuit is used to generate very fast, accurate timing pulses. The input bias currents of the HCMP96900 have a linear response over the full input voltage range. While this isn't ideal as no change, it is much better than the nonlinear variations of previous high speed comparators. The change from -3.0V to +10.0V is typically less then 3μA.

LATCH ENABLE INPUTS

The timing diagram for the comparators is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low, the comparators track the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

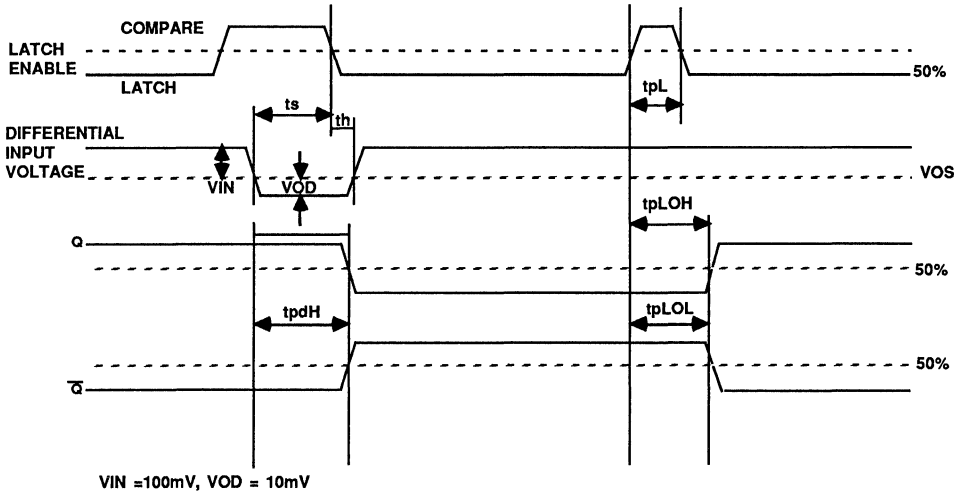
The leading edge of the input signal (which consists of 100mV overdrive) changes the comparator output after a time of tpdL or tpdh (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the latch enable falling edge or $\overline{LE}$ rising edge and held for a time th after the falling edge for the comparator to accept data. After t_h, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of tpL is needed for strobe operation, and the output transitions occur after a time of tpLOH or tpLOL.

Unused outputs must be terminated with 50Ω to ground while unused latch enable pins should be connected directly to ground.

OUTPUTS

The outputs are very high speed differential ECL that are 10KH compatible and capable of driving 50 Ohm loads. The difference between these outputs and the 10KH specifications is that they have much faster rise and fall times. Both rise and fall times are 1.2ns.

FIGURE 1. TIMING DIAGRAM



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry, input signals occuring before t_s will be detected and held; those occuring after t_h will not be detected. Changes between t_s and t_h may not be detected ($\overline{LE}$ is the inverse of LE).

SWITCHING TERMS

tpdH - INPUT TO OUTPUT HIGH DELAY
The propagation delay measured from the time the imput signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transistion.

tpdL - INPUT TO OUTPUT LOW DELAY
The propagation delay measured from the time the imput signal crosses the tmput offset voltage to the 50% point of an output HIGH to LOW transistion.

tpLOH - LATCH ENABLE TO OUTPUT HIGH DELAY
The propagation delay measured from the 59% point of the Latch Enable signal Low to HIGH transition to 50% point of an output LOW to HIGH transistion.

tpLOL - LATCH ENABLE TO OUTPUT LOW DELAY
The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

ts - MIMINUN SET-UP TIME
The minimum time before the negative transistion of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

th -MINIMUM HOLD TIME
The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

tpL - MINIMUM LATCH ENABLE PULSE WIDTH
The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an imput signal change.

tpdL - tpdH - DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT
The delay or skew between comparators.

tpLOL - tpLOH - DIFFERENTIAL PROPAGATION DELAY (SKEW) LATCH TO OUTPUT The skew from one comparator to another

VOD - VOLTAGE OVERDRIVE

FIGURE 2. HCMP96900 SUPPLY VOLTAGES INPUT VOLTAGE RANGE

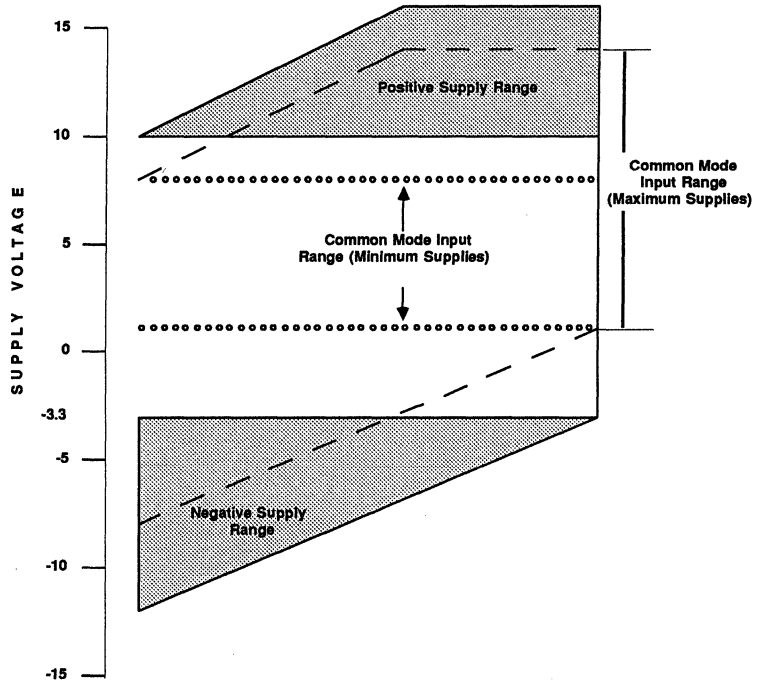
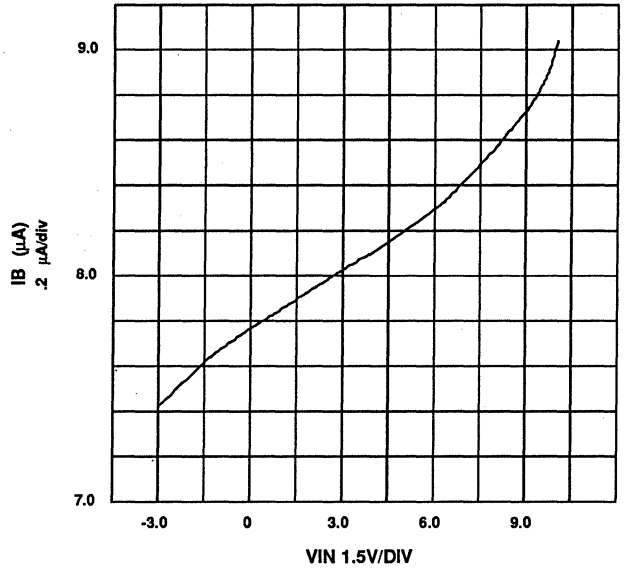
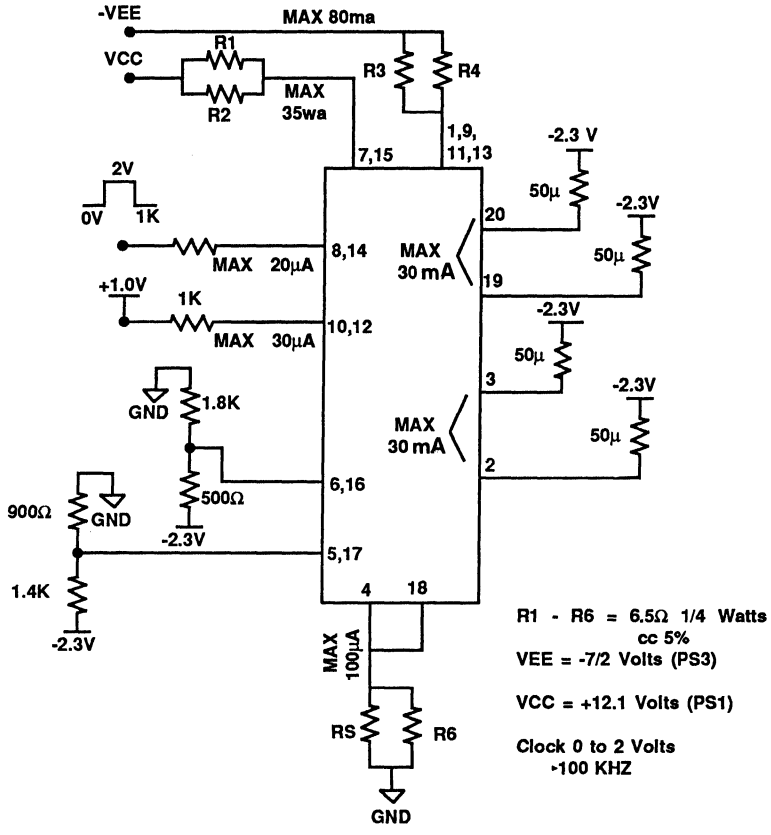


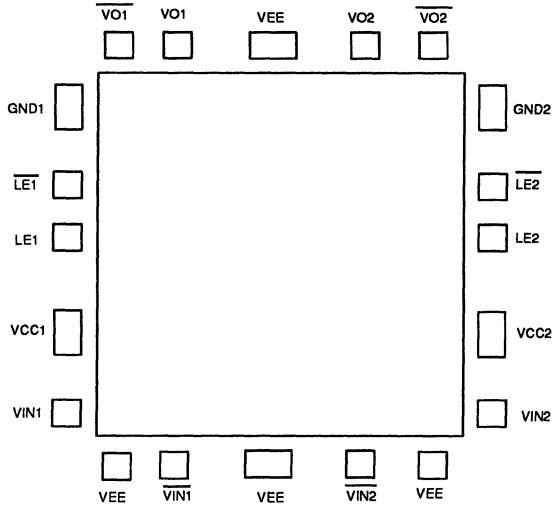
FIGURE 3. HCMP96900 VIN VERSUS IB (Common Mode)



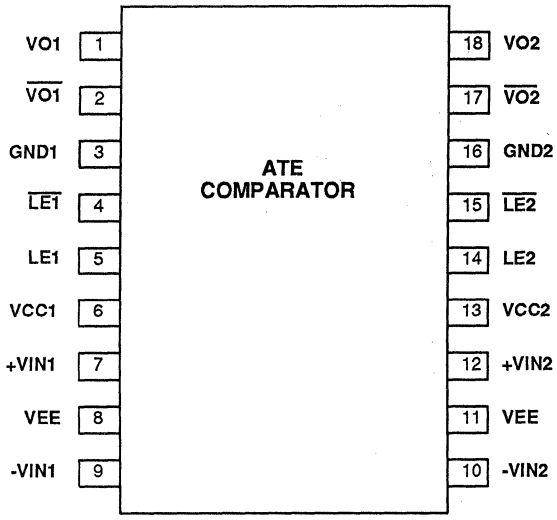
HCMP96900 BURN-IN DIAGRAM (LCC Package)



HCMP96900 DIE PLOT

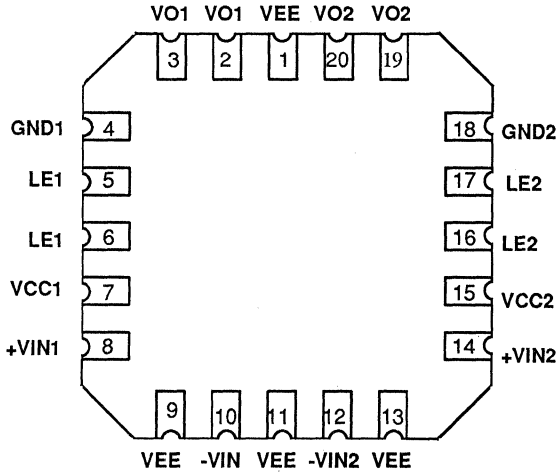


HCMP96900 18-PIN DIP PACKAGE



Pins	Description
VO1	Output 1
$\overline{VO1}$	Inverted Output 1
GND1	Ground
LE1	Latch Enable 1
$\overline{LE1}$	Inverted Latch Enable
VEE	Negative Supply Voltage
-VIN1	Inverting Input 1
+VIN1	Non-inverting Input 1
+VIN2	Non-inverting Input 2
-VIN2	Inverting Input 2
VCC1	Positive Supply Voltage 1
VCC2	Positive Supply Voltage 2
LE2	Latch Enable 2
$\overline{LE2}$	Inverted Latch Enable 2
VO2	Output 2
$\overline{VO2}$	Inverted Output 2
GND2	Ground 2

HCMP96900 20-PIN LCC PACKAGE



**For Ordering Information See Section 1.*

HINA522

HIGH ACCURACY DATA ACQUISITION INSTRUMENTATION AMPLIFIER

ADVANCE INFORMATION

FEATURES:

- Direct **MONOLITHIC** Replacement for AD522
- Low Nonlinearity: 0.001% (G=1)
- High CMRR: >100 dB (G=1000)
- Low Input Voltage Drift: 2.0 µV/°C
- Low Noise: 9 nV/√Hz (@1 kHz, G=1000)
- Single Resistor Gain Programmable 1<G<1000

APPLICATIONS:

- Industrial and Process Control
- Bridge Amplifiers
- Signal Conditioning
- Test and Medical Instrumentation

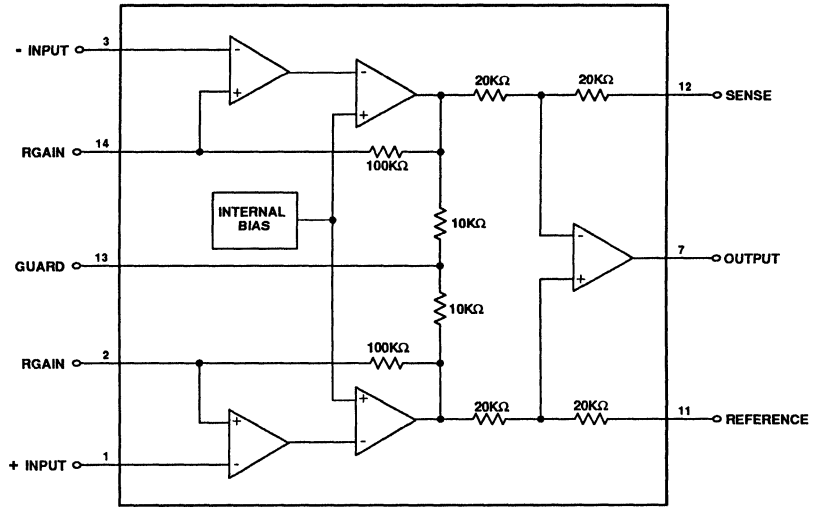
GENERAL DESCRIPTION

The HINA522 is a precision instrumentation amplifier designed for high accuracy data acquisition applications of up to 12 bits. It represents an excellent combination of high common mode rejection, low noise and low nonlinearity. A passive data guard is provided to improve AC common mode rejection and prevent degradation of system bandwidth.

The HINA522 is implemented in Honeywell's Advanced Linear Bipolar process (ALB1A) which combines state-of-the-art, laser trimmed thin film technology with high density junction isolated bipolar technology. The HINA522 is the only fully monolithic direct replacement for the AD522 and thus provides superior stability and reliability for extremely cost-effective low-level amplification.

5

BLOCK DIAGRAM



SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	HINA522A MIN TYP MAX	HINA522B MIN TYP MAX		UNITS
ELECTRICAL CHARACTERISTICS	$V_S = \pm 15$ V, $R_L = 2$ KΩ, Over Temperature Range Specified Below, Unless Otherwise Indicated					
Gain Error	G = 1 $T_A = 25$ °C	I	±.05	±.20		%
Gain Temperature Coefficient	G = 1	I	±2	±2		ppm/°C
Nonlinearity	G = 1	I	±.001	±.005		%
Input Offset Voltage	$T_A = 25$ °C	I	±25	±75		µV
Input Offset Voltage Temp. Co.		I	±.50	±2.0		µV/°C
Input Bias Current	$T_A = 25$ °C	I	±15	±25		nA
Common Mode Rejection	G = 1000	I	110	100		dB
Linear Differential Input Voltage Range	G = 1	I	±10	±10		Volts
Linear Common Mode Input Voltage Range	G = 1000	I	±12	±12		Volts
Output Voltage		I	±10	±10		Volts

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.

**For Ordering Information See Section 1.*

HINA524

PRECISION INSTRUMENTATION AMPLIFIER

ADVANCE INFORMATION

FEATURES:

- **Improved Direct Replacement for AD524**
- Low Nonlinearity: 0.003% (G=1)
- Low Input Offset Voltage: 25 µV Max
- Low RTI Noise: 4 nV/√Hz (@1 kHz, G=1000)
- Gain Bandwidth: 25 MHz (G = 1)
- High CMRR: 120 dB (G = 1000)

APPLICATIONS:

- Data Acquisition System Amplifiers
- Signal Conditioning
- Medical Instrumentation

GENERAL DESCRIPTION

The HINA524 from Honeywell is a highly accurate, precision instrumentation amplifier designed for data acquisition applications where low noise and very high DC performance is required. Features such as maximum Nonlinearity of .003% (G = 1), Common Mode Rejection of 120 dB (G = 1000) and Input Offset Voltage Drift of 0.5µV/°C make the HINA524 the ideal choice for use in many high resolution data acquisition systems.

Along with outstanding DC specifications, the AC performance of a 25 MHz Gain Bandwidth Product, 5 V/µs Slew Rate and 15 µs Settling Time make the HINA524 suitable for may high speed data acquisition applications. Gain selections of 1, 10, 100 and 1000 require no additional components. With the use of a single external resistor, any gain setting can be achieved in the range of 1<G<1000.

The HINA524 is implemented in Honeywell's Advanced Linear Bipolar process (ALB1A) which combines state-of-the-art, laser trimmed thin film techniques with high density junction isolated bipolar technology. Honeywell's improved design approach provides a high precision, highly reliable device as a cost effective instrumentation solution. The HINA524 is a direct pin-for-pin replacement for the AD524.

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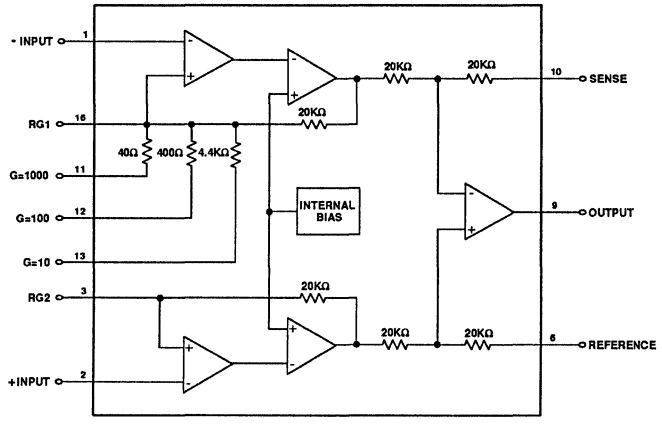

SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	HINA524A MIN TYP MAX	HINA524B MIN TYP MAX	HINA524C MIN TYP MAX	UNITS
ELECTRICAL CHARACTERISTICS	$V_S = \pm 15$ V, $R_L = 2$ KΩ, Over Temperature Range Specified Below, Unless Otherwise Indicated					
Gain Error	G = 1 $T_A = 25$ °C	I	±.02	±.03	±.05	%
Gain Temperature Coefficient	G = 1	I	±5	±5	±5	ppm/°C
Nonlinearity	G = 1	I	±.003	±.003	±.005	%
Input Offset Voltage	$T_A = 25$ °C	I	±25	±75	±200	µV
Input Offset Voltage Temp. Co.		I	±.50	±.75	±2	µV/°C
Input Bias Current	$T_A = 25$ °C	I	±15	±25	±50	nA
Common Mode Rejection	G = 1000	I	120	120	110	dB
Linear Differential Input Voltage Range	G = 1	I	±10	±10	±10	Volts
Linear Common Mode Input Voltage Range	G = 1000	I	±12	±12	±12	Volts
Output Voltage		I	±10	±10	±10	Volts

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.

**For Ordering Information See Section 1.*

HINA624

PRECISION INSTRUMENTATION AMPLIFIER

ADVANCE INFORMATION

FEATURES:

- **Direct Replacement for AD624**
- Low Nonlinearity: 0.001% (G=1)
- High CMRR: >130 dB (G>500)
- Low Input Offset Voltage: 25 μV
- Low RTI Noise: 4 nV/√Hz (@1 kHz, G=1000)
- Gain Bandwidth: 25 MHz (G = 1000)

APPLICATIONS:

- Data Acquisition System Amplifiers
- Signal Conditioning
- Medical Instrumentation

GENERAL DESCRIPTION

The HINA624 from Honeywell is a highly accurate, precision instrumentation amplifier designed for data acquisition applications where low noise and very high DC performance is required. Features such as maximum Nonlinearity of .001 % (G = 1), Gain Temperature Coefficient of 5 ppm/°C, and Input Offset Voltage Drift of .25 μV/°C make the HINA624 the ideal choice for use in high resolution data acquisition systems.

Both simplicity in gain programming and extreme flexibility are offered by the HINA624. No external components are required for selection of the pre-trimmed gains of 1, 100, 200, and 1000. Nine additional gain values can also be be achieved by pin strapping. Any arbitrary gain value of 1<G<10,000 may be programmed with the use of a single external resistor.

The HINA624 is implemented in Honeywell's Advanced Linear Bipolar process (ALB1A) which combines state-of-the-art, laser trimmed thin film technology with high density junction isolated bipolar technology. Honeywell's improved design approach provides a high precision, highly reliable device as a cost effective instrumentation solution. The HINA624 is a direct pin-for-pin replacement for the AD624.

5

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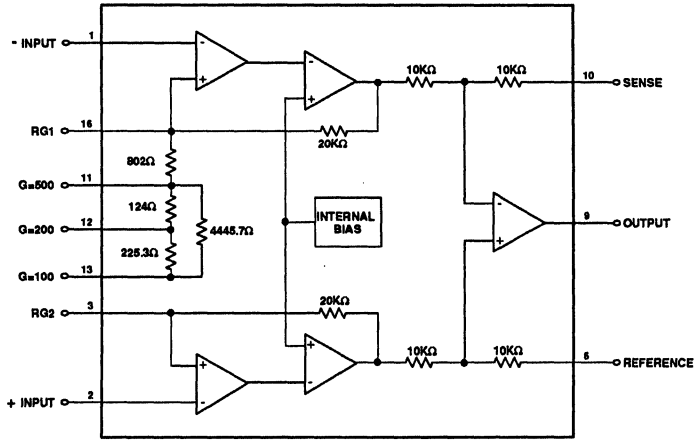


SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	HINA624A MIN TYP MAX	HINA624B MIN TYP MAX	HINA624C MIN TYP MAX	UNITS
ELECTRICAL CHARACTERISTICS	$V_S = \pm 15$ V, $R_L = 2$ KΩ, Over Temperature Range Specified Below, Unless Otherwise Indicated					
Gain Error	G = 1 $T_A = 25$ °C	I	±.02	±.03	±.05	%
Gain Temperature Coefficient	G = 1	I	±5	±5	±5	ppm/°C
Nonlinearity	G = 1	I	±.001	±.003	±.005	%
Input Offset Voltage	$T_A = 25$ °C	I	±25	±75	±200	µV
Input Offset Voltage Temp. Co.		I	±.25	±.5	±2	µV/°C
Input Bias Current	$T_A = 25$ °C	I	±15	±25	±50	nA
Common Mode Rejection	G = 1000	I	130	120	110	dB
Linear Differential Input Voltage Range	G = 1	I	±10	±10	±10	Volts
Linear Common Mode Input Voltage Range	G = 1000	I	±12	±12	±12	Volts
Output Voltage		I	±10	±10	±10	Volts

TEST LEVEL	TEST PROCEDURE
I	Production tested at the specified conditions.

***For Ordering Information See Section 1.*

HTHA27140

16-BIT ACCURATE, MONOLITHIC TRACK AND HOLD AMPLIFIER

ADVANCE INFORMATION

FEATURES

- **5μS ACQUISITION TIME**
- Low Power - 300mW
- Internal Hold Capacitor
- 16-bit Accuracy
- ±5V analog input
- Linearity - 0.0008%

APPLICATIONS

- Sonar
- Digital Scales
- Instrumentation
- Communications
- DSP Interface
- Acoustic Analysis
- Use With HADC78160 16-bit A/D Converter

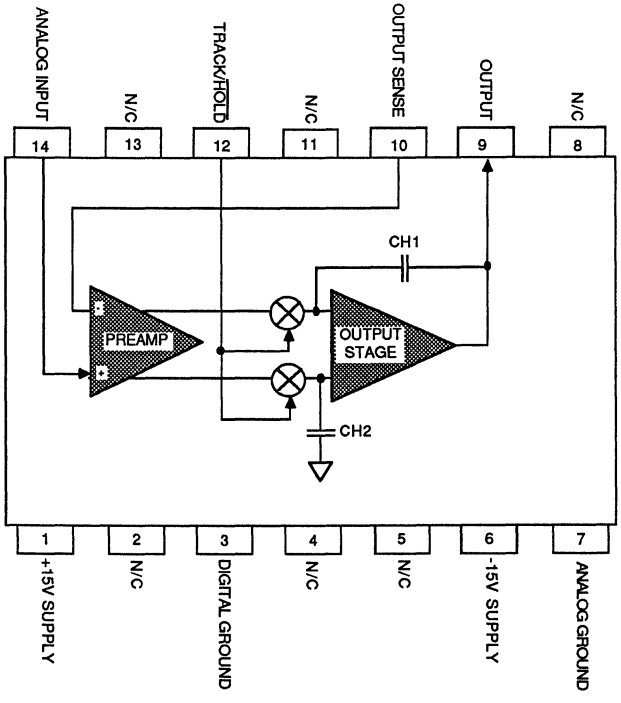
GENERAL DESCRIPTION

The HTHA27140 is a 16-bit accurate, monolithic track-and-hold amplifier capable of acquiring ±5V analog signals within 5uS yet only consuming 300mW of power. Included on-chip are two internal hold capacitors that keep the track-to-hold settling time down to 300nS. The part has the highest speed and accuracy for the power in the industry.

There is a track-and-hold control pin and an output sense pin connected to the inverting input of the preamp stage. Separate analog and digital ground pins are provided to achieve 16-bit accuracy in board layout, and to be compatible with other components that require separate ground planes. The HTHA27140 is optimized to be used with the HADC78160 16-bit A/D converter to increase the A/D analog input frequency range. The device is manufactured on Honeywell SPTs small geometry bipolar process, and military and industrial temperature grades are available.

The part is packaged in a 14 Lead Ceramic DIP and operates on ±15V power supplies.

BLOCK DIAGRAM



6

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

@ 25°C case temperature and nominal supplies.

ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C MIN	ROOM +25°C TYP	ROOM +25°C MAX	HOT +125°C MIN	HOT +125°C MAX	COLD -55°C MIN	COLD -55°C MAX	UNITS
STATIC PARAMETERS										
Power Dissipation				300						mW
Gain				1±0.01%						V/V
Gain Temperature Coefficient				0.1						PPM/°C
Offset				1.0						mV
Offset Temperature Coefficient	Full Scale Range			0.5						PPM/°C
Pedestal				1.0						mV
Pedestal Temp. Coefficient	Full Scale Range			0.1						PPM/°C
Linearity	Full Scale Range			10						PPM
Input Impedance				5						KΩ
Logic Loading				1						LS TTL
Voltage Range				±5						V
DYNAMIC PARAMETERS										
Acquisition Time	10V step to 0.0008%			5.0						µS
Settling Time	Track to Hold			300						nS
Bandwidth				4.0						MHz
Slew Rate				3.0						V/µS
Noise				15.0						nV/√Hz

TEST LEVELS: I - Production tested at the specified conditions; II - Sample tested to ensure compliance.

**For Ordering Information See Section 1.*

SIGNAL PROCESSING TECHNOLOGIES

HSCF24040

PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

PRELIMINARY INFORMATION

FEATURES

- 85 dB Dynamic Range
- Cut Off Frequency (fc) up to 20KHz
- **On-Chip** Anti-Aliasing Protection
- Programmable Bandedge Frequency for both RC and Switched Capacitor Filter
- S/H Output
- Microprocessor Compatible
- 7th Order Ladder Filter with Cosine Prefiltering Stage
- Stopband Attenuation > 76 dB at 3 fc
- Programmable DC Gains of 1, 2, 4, 8
- On-Chip Oscillator (External Crystal)

APPLICATIONS

- Anti-Alias Filtering
- Test Equipment/Instrumentation
- Spectrum Analyzers
- Medical Telemetry/Filtering
- Speech Analysis and Synthesis
- Data Acquisition Systems
- Computer Controlled Test Systems

GENERAL DESCRIPTION

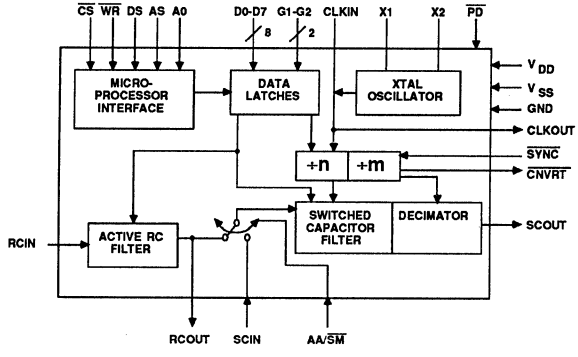
The HSCF24040 is a monolithic 7th order active filter system. It is manufactured using Honeywell's state-of-the-art BEMOS process which allows the fabrication of low power CMOS logic, linear CMOS circuits, bipolar linear circuitry and thin film resistors on a single chip. The HSCF24040 is designed using switched-capacitor techniques which allows easy programming of the filter cut-off frequency.

The HSCF24040 contains a fully differential, 7-pole, lowpass switched-capacitor filter (SCF) which is designed to provide an accurate, programmable passband for fixed or dynamic applications. The switched-capacitor filter section is preceeded by a 3-pole active RC filter (RCF) with a programmable bandedge. Together, the RCF and SCF provide greater than 76 dB of anti-aliasing protection. The last stage of the SC filter contains a programmable decimator that reduces the sample rate at SCOUT. This insures that the hold period of the sampled and held output is long enough to perform an A/D conversion or be re-sampled by an external S/H.

The topology and layout of the HSCF24040 is sufficiently flexible to allow customization of the filter function and/or logic. The HSCF24040 is packaged in a 32 pin DIP, operates on a +/- 5V supply voltage and is offered in commercial and military temperature ranges.

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages
Positive Supply Voltage (VDD to GND).....0 to +7V
Negative Supply Voltage (VSS to GND).....0 to -7V

Input Voltages
Digital Input Voltages
All Except CLKIN, $\overline{CS}$.....-0.3 to VDD+0.3V
CLKIN, $\overline{CS}$.....VSS-0.3 to VDD+0.3V

Temperature
Operating Temperature, ambient.....-55 to +125°C
junction.....+175°C
Lead Temperature, (soldering 10 seconds).....+300°C
Storage Temperature.....-65 to +150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Excessive exposure to absolute maximum ratings may effect device reliability.

2. The XTAL oscillator must not be enabled unless the external crystal is connected between pins X1 and X2.

VDD = +5.0V, VSS = -5.0V, +25°C (Unless Otherwise Specified)

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
VDD		I	4.75	5.0	5.25	Volts
VSS		I	-5.25	-5.0	-4.75	Volts
IDD	VDD = 5V, VSS = -5V	I		15		mA
ISS	VDD = 5V, VSS = -5V	I		-15		mA
Power Dissipation	VDD = 5V, VSS = -5V	I		150		mW
Gain Tolerance	Gain = 1 V/V	I		±0.1		%
Gain		I		Programmable 1, 2, 4, 8		Volts/Volts
Offset Voltage	Gain = 1 V/V	I		5		mV
Power Down/Power Dissipation		I		15		mW
AC ELECTRICAL CHARACTERISTICS						
RC FILTER & SC FILTER						
Input CLK Frequency		I	1	4		MHz
Cut-off Frequency Range	*fc*		78		20,000	Hz
Input Signal Level		I			±3	Volts

VDD = +5.0V, VSS = -5.0V, +25°C (Unless Otherwise Specified)

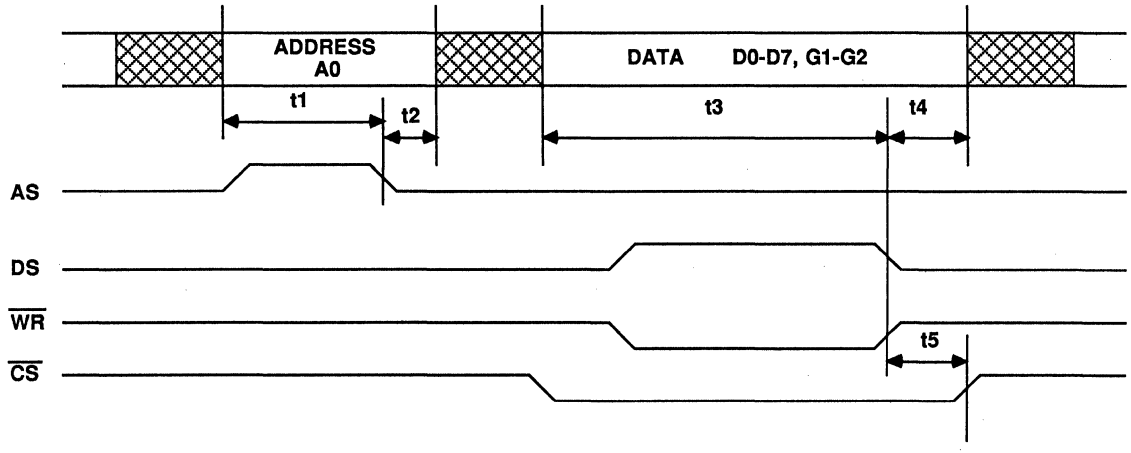
PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS						
Output Voltage Swing	ZL = 5KΩ//50pF	I			±3	Volts
Output Current Drive	RCOUT & SCOUT	I		0.6		mA
Pass Band Ripple		I	-0.1		+0.1	dB
Bandedge Tolerance	*fc*=(-0.1) dB freq	II		*fc*± 0.5		%
Filter Response	0 to 1.0 *fc*	I	-0.1		+0.1	dB
(Relative to DC Gain)	1.5 *fc*	I			-30	dB
	2.0 *fc*	I			-52	dB
	≥3.0 *fc*	I			-76	dB
Dynamic Range		I	85			dB
Wideband Noise	SCF BW = 20 kHz RCF BW = 80 kHz	II			100	µVrms
Harmonic Distortion	Magnitude of Harmonic	I		-72		dB
	THD	I		0.05		%
PSRR: In-Band		II		50		dB
High Frequency Aliasing		II		35		dB
RC FILTER						
DC Gain		I	-0.1		+0.1	%
Bandedge Tolerance		I		*fc* (RCF) $^{+5}_{-0}$		%
Cut-off Frequency Range	*fc* (RCF)	I	7		80	KHz
Filter Response	*fc* (RCF)/4	I		-0.05		dB
	fc (RCF)	I		-3.45		dB
	17 *fc* (RCF)	I		-76		dB
CLOCK						
Internal Oscillator Frequency	See Note 2	I	1		4	MHz

VDD = +5.0V, VSS = -5.0V, +25°C (Unless Otherwise Specified)

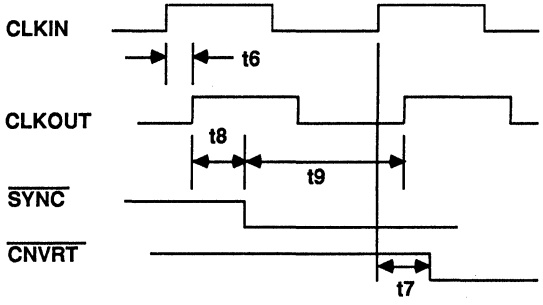
PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS						
DIGITAL ELECTRICAL PARAMETERS						
Input High Voltage		I	2.0		VDD	Volts
Input Low Voltage		I	0.0		0.8	Volts
Input Leakage Current		I			1	µA
Input Capacitance		II			10	pF
TIMING CHARACTERISTICS (See Timing Diagrams)						
µP INTERFACE TIMING						
$\overline{CS}$ Hold Time	t5	I	10			nsec
Data Hold Time	t4	I	10			nsec
Data Set-up Time	t3	I	100			nsec
Address Hold Time	t2	I	10			nsec
Address Set-up Time	t1	I	20			nsec
SCOUT SYNCHRONIZATION TIMING						
SyncB Delay Time	t8	I	25			nsec
SyncB Set-up Time	t9	I	25			nsec
CLKIN to CLKOUT Delay	t6	I		10		nsec
CLKIN to $\overline{CNVRT}$ Delay	t7	I		20		nsec

TIMING DIAGRAMS

MICROPROCESSOR INTERFACE TIMING



SCOUT SYNCHRONIZATION TIMING



TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING	TEST LEVEL	TEST PROCEDURE
All electrical characteristics that follow are subject to the following conditions:	I	Production tested at the specified temperatures.
All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.	II	Parameter is guaranteed by design and sampled characterization data.
Unless otherwise noted, all tests are pulsed tests, therefore Tj = Tc = Ta.		

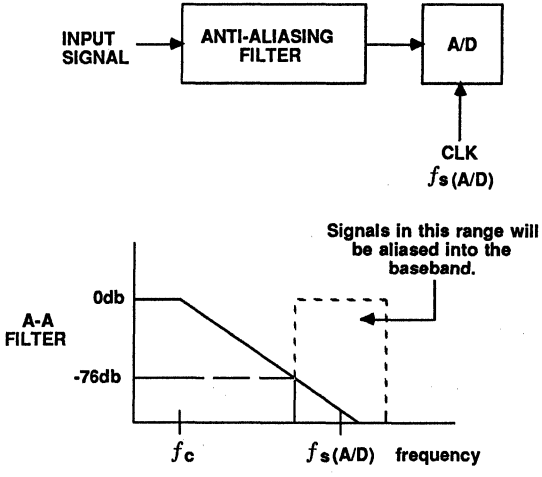
GENERAL DESCRIPTION

SC FILTER

SC filters are sampled data filters that provide extremely accurate and stable responses. This is because their internal "time constants" depend only upon the switching frequency and the ratios of monolithic capacitors. The switching frequency is normally derived from a crystal controlled oscillator and is thus, extremely precise. On-chip capacitor ratios are accurate to within approximately 0.1%. Therefore, high order sharp rolloff filters can be manufactured that require no post production trimming. Since the filter bandedge can be programmed by varying the frequency of the clock that controls the filter's switches, the filter bandedge can be made to track the sample rate of an external A/D converter. The filter in the HSCF24040 has 7 poles (Chebyshev approximation) to insure a minimum loss of 76dB at 3 times the bandedge so that the system A/D can sample as low as 4 times the bandedge (see Figure 1). The SC filter has a differential signal path to improve its PSRR, distortion, and dynamic range. Through digital programming, bandedges of up to 20KHz and DC gains of 1, 2, 4 or 8 can be achieved.

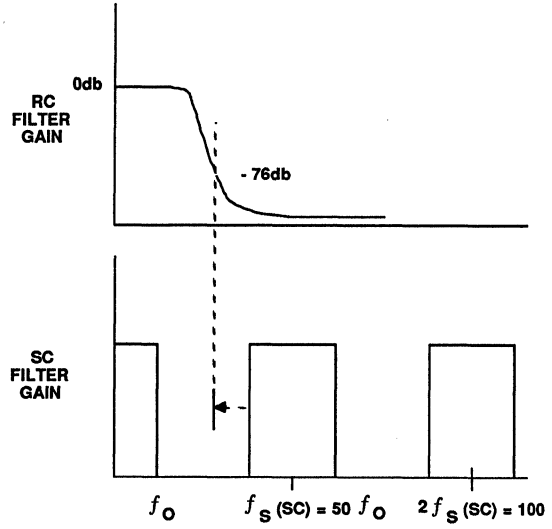
ACTIVE RC FILTER

Although the SC filter is programmable and offers excellent performance, it does have one major drawback. Because it is a sampled data filter, it can fold or alias out-of-band energy into the desired passband in much the same way as the external A/D. Therefore, a continuous-time filter is required in front of the SC filter to provide aliasing protection. We are, however, aided by the fact that the filter sampling rate is many times greater than the bandedge frequency (50 times in this case). Thus, a low order, active RC filter with a bandedge accuracy of only 5% will suffice. This concept is illustrated in Figure 2. The bandedge for this RC filter must be programmable to insure sufficient rejection of the SC filter images located at multiples of the SC filter rate. Eight different RC filter bandedges spanning a 12-to-1 range are available on the HSCF24040. The programmability is achieved by switching different resistor and capacitor values into the filter. A single RC filter bandwith setting (3dB) of f_C(RCF) will provide 76dB of anti-aliasing protection for SC filter bandwidths ranging from f_C(RCF)/5.71 to f_C(RCF)/4.



Since the filter loss is greater than 76 dB, any aliased signals will be below the 12 bit level.

FIGURE 1 - REQUIREMENTS FOR AN ANTI-ALIASING FILTER PRIOR TO A/D CONVERSION



Note: The RC filter should provide > 76 dB of loss for several different SC filter sample rates f_S (SC).

FIGURE 2 - RC FILTER PROVIDES ANTI-ALIASING FOR SC FILTER

The topology of the RC filter has been chosen so that the DC gain and the pole Q's rely on ratio matching of the on-chip resistors and capacitors. The RC filter bandedge is laser trimmed for high accuracy during the manufacturing process.

DECIMATOR

The decimator block samples the differential output of the SC filter and converts it to a single ended signal. The decimator also provides a sample-and-hold output (SCOUT) at a programmable sample rate of $25fc$, $12.5fc$, $6.25fc$, or $4.167fc$, where fc is the SC filter bandwidth. By choosing the proper decimation rate, the hold time at SCOUT will be sufficiently long to allow an A/D conversion to take place. (An external sample and hold may be required for hold times longer than 100μsec to prevent more than 1/2 LSB of droop for a 12-bit A/D converter).

The $\overline{\text{CNVRT}}$ output is an active low digital output that indicates when the SCOUT output is valid. Applying a falling edge to the $\overline{\text{SYNC}}$ input initiates the $\overline{\text{CNVRT}}$ pulse on the next rising edge of CLKOUT. The use of the decimator block with $\overline{\text{SYNC}}$ and $\overline{\text{CNVRT}}$ insures a proper timing interface between SCOUT and an external A/D converter or sample and hold and eliminates the need for a smoothing filter at the SCOUT output.

PROGRAMMABILITY

The chip contains an 8-bit and a 2-bit data register. Data in the 8-bit register controls the SC filter bandedge, RC filter bandedge, and the decimation rate. (A programmable divide down chain generates the SC filter clocks from the master clock. A similar divide down chain determines the decimation rate from the SC filter clocks). Data in the 2-bit register controls the programmable D.C. gain of the SC filter. The truth tables for both registers are shown in Table 1.

The SC filter's bandedge is programmed by selecting one of the divide down ratios shown in Table 1. This ratio is divided into the master clock frequency to arrive at the filter cutoff frequency. As an example, assuming a typical master clock frequency of 4 MHz and a divide down ratio of 400 (D0, D1, D2=001), the filter's bandedge would be 10kHz. Alternately, selecting a divide down ratio of 3200 (D0, D1, D2 = 100) would provide a filter bandedge of 1250Hz. With a constant master clock frequency, up to seven (7) different discrete SC filter bandedges can be obtained. An infinite number of different bandedges can be derived by varying both the divide down ratios and the master clock frequency. This provides the ultimate level in programming flexibility.

The five control signals A0, AS, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and DS allow the user to directly interface to 8-bit microprocessors without additional glue logic. Both Motorola's MPX'ed and non-MPX'ed bus formats as well as Intel's MPX'ed bus format is supported. Interface connections for both the Intel and Motorola 8-bit microprocessors are shown in Table 2. In addition to the data-latch format, the D0-D7 and G1-G2 inputs can be hardwired for direct programming without the need for a latch signal by tying the $\overline{\text{CS}}$ input to VSS.

TABLE 1 - PROGRAMMABLE FEATURES

RCF BANDEDGE

RCF 3dB BW	D7	D6	D5
80KHz	0	0	0
56KHz	0	0	1
40KHz	0	1	0
28KHz	0	1	1
20KHz	1	0	0
14KHz	1	0	1
10KHz	1	1	0
7KHz	1	1	1

DC GAIN

DC GAIN	G1	G2
1	1	1
2	1	0
4	0	1
8	0	0

CLOCK TO SCF BANDEDGE DIVIDE DOWN RATIO

fCLK / fC	D0	D1	D2
200	0	0	0
400	0	0	1
800	0	1	0
1,600	0	1	1
3,200	1	0	0
6,400	1	0	1
12,800	1	1	X

DECIMATOR SAMPLE RATE

fS/H / fC	D3	D4
25.000	0	0
12.500	0	1
6.250	1	0
4.167	1	1

fC = 0.1db Bandwidth of the SC filter.
fCLK = Master clock frequency at CLKOUT.
fS/H = Sample rate at SCOUT output.

TABLE 2 - MICROPROCESSOR INTERFACE CONNECTIONS

HSCF24040	INTEL (MPX'ED) 8088, 8085, 8051	MOTOROLA (MPX'ED) 6801, 6803	MOTOROLA (NON-MPX'ED) 680D, 6801, 6802, 6809
$\overline{CS}$	Generated from A8-A15	Generated from A8-A15	Generated from A0-A15
DS	VDD Supply	E	E
$\overline{WR}$	$\overline{WR}$	R/$\overline{WR}$	R/$\overline{WR}$
A0	ADi	ADi	Ai
AS	ALE	AS	VDD Supply
D0-D7	AD0-AD7	AD0-AD7	D0-D7
G1-G2	ADi	ADi	Di

Note: Tying $\overline{CS}$ to the VSS supply disables the microprocessor interface and allows D0-D7, G1-G2 to be programmed directly without the need for a latch signal.

OSCILLATOR

The HSCF24040 provides an on-chip oscillator (external crystal) for applications where a system clock is not available. The user has a choice of either the clock driven or the oscillator mode. The oscillator mode is enabled by tying the CLKIN input to VSS.

TYPICAL APPLICATION CIRCUIT

Figure 3 illustrates how the HSCF24040 might be used for smoothing the output from a D/A converter. In this case, the D/A output is fed into the SCIN input of the device. The SCIN input is enabled by tying AA/$\overline{SM}$ to ground. The SCOUT output is fed externally into the RCIN input. The smoothed output is finally brought off-chip via the RCOUT pin. (Note that the smoothed output will not correct for the inherent sin (X)/(X) droop of the original D/A converter output).

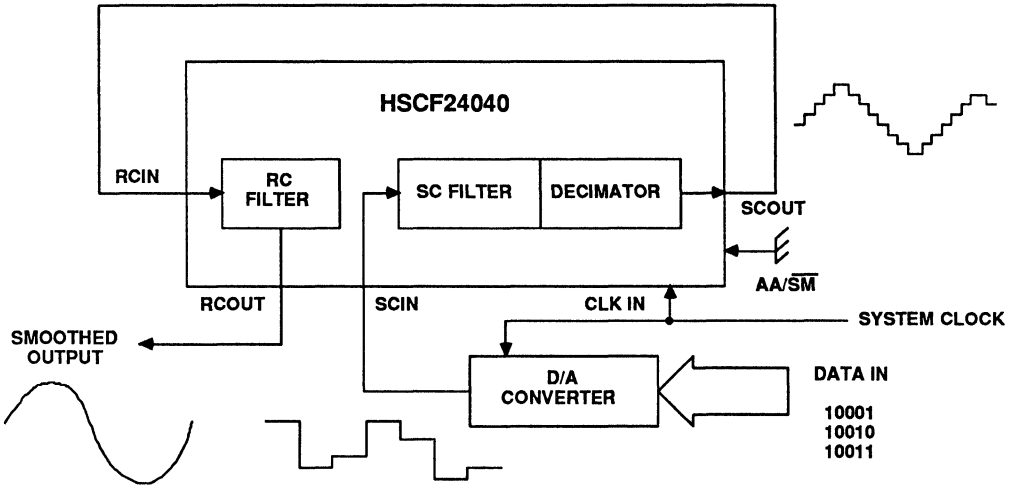


FIGURE 3 - THE HSCF24040 AS A SMOOTHING FILTER FOR A D/A CONVERTER

TYPICAL APPLICATION CIRCUIT

The HSCF24040 can be used as the band limiting filter for a 12-bit data acquisition system as shown in Figure 4. The basic function of the device is to bandlimit the input signal so that unwanted out-of-band signals are not aliased (folded) into the desired passband. The input signal enters the HSCF24040 through RCIN and is processed by the RC filter. The signal is then processed by the switched-capacitor filter and finally the decimator to facilitate its interface with the A/D converter. Figure 1 shows that for a 12-bit system the filter must provide at least 76dB of loss at the frequency fs-fc (where fs is the sampling rate of the A/D converter and fc is the desired channel bandwidth).

In many applications the user may want a programmable channel bandwidth. An instrument that records signals that range from 100Hz to 20kHz would require that the A/D sample rate be variable. Figure 1 shows that the required filter bandwidth is directly proportional to the sample rate of the A/D converter. The filtering necessary for multiple sampling rates can be accomplished by using the programmable bandwidth capability of the HSCF24040 to adjust the desired filter response to the sample rate. This eliminates the need for a parallel bank of fixed bandwidth anti-aliasing filters, one for each sample rate.

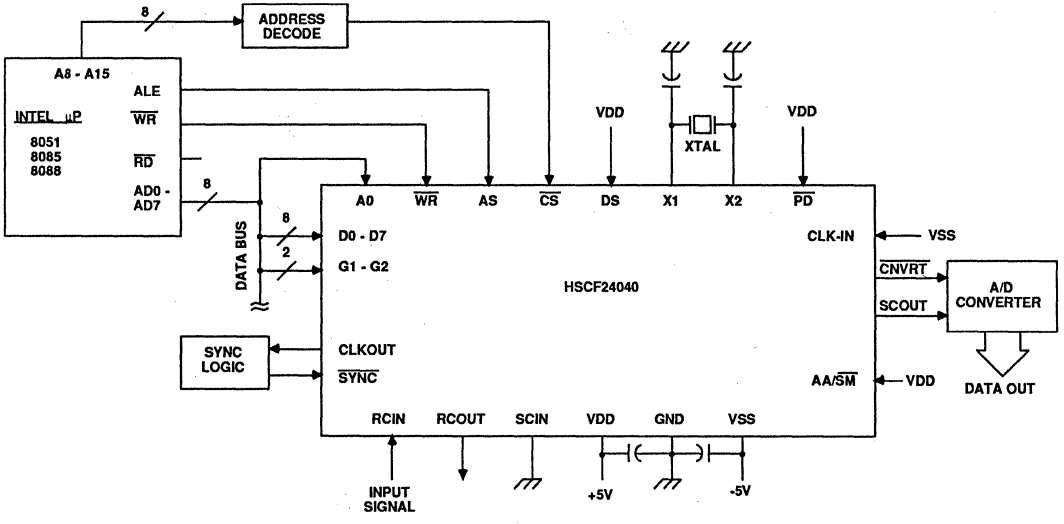
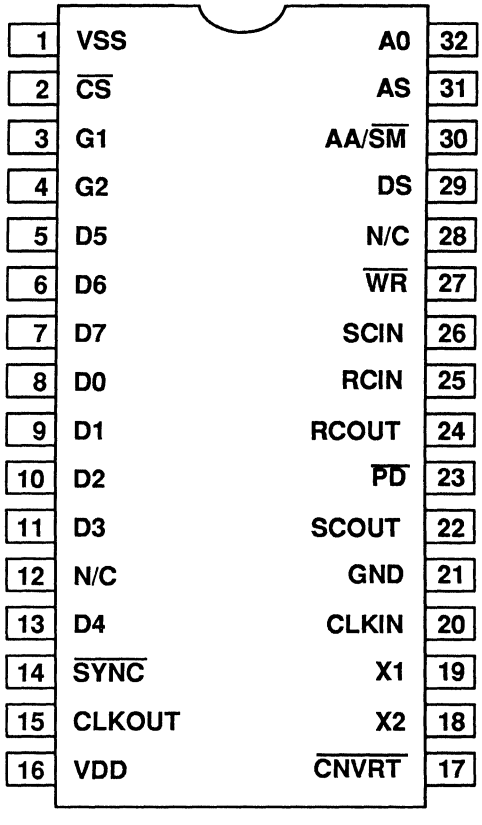


FIGURE 4 - THE HSCF24040 AS AN ANTI-ALIASING FILTER IN A 12-BIT DATA ACQUISITION SYSTEM

PIN ASSIGNMENT HSCF24040

TOP VIEW



PIN FUNCTIONS HSCF24040

NAME	FUNCTION
VSS	Negative supply voltage
$\overline{CS}$	Chip select; active low
G1 - G2	The digital inputs that control the DC gain of the SC filter
D0 - D7	The digital inputs that control the RC filter bandedge, SC filter bandedge, and SC filter decimation rate
$\overline{SYNC}$	This digital input controls the sampling instant for the SC filter decimated output; active low
CLKOUT	Master clock output capable of driving 1 standard TTL load. It is a buffered version of either CLKIN or the internally generated crystal oscillator output.
VDD	Positive supply voltage
$\overline{CNVRT}$	This digital output indicates that the SCOUT output has settled and can now be converted or sampled (drive capability is 1 standard TTL load); active low
X1-X2	An external crystal is connected between these pins to generate an accurate clock for chip operation
CLKIN	The master clock input. Forcing CLKIN to VSS enables the on-chip oscillator (external crystal).
GND	Ground
SCOUT	SC filter output
$\overline{PD}$	This digital input is used to power down the analog circuitry; active low
RCOUT	RC filter output
RCIN	RC filter input
SCIN	SC filter input (only valid when AA/$\overline{SM}$ is forced low)
$\overline{WR}$	Write strobe; active low
DS	Data strobe
AA/$\overline{SM}$	This digital input controls whether the input to the SC filter comes from RCOUT or SCIN
AS	Address strobe
A0	Register address select

***For Ordering Information See Section 1.*

NOTES:

EB100 EVALUATION BOARD

FEATURES

- **150 MSPS MINIMUM CONVERSION RATE**
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- Clock produced from any signal generator
- Improved Output Drive (Doubly-Terminated 50Ω)
- Optional clock divider board provided

APPLICATIONS

- Evaluation of HADC77100 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB100 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77100A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

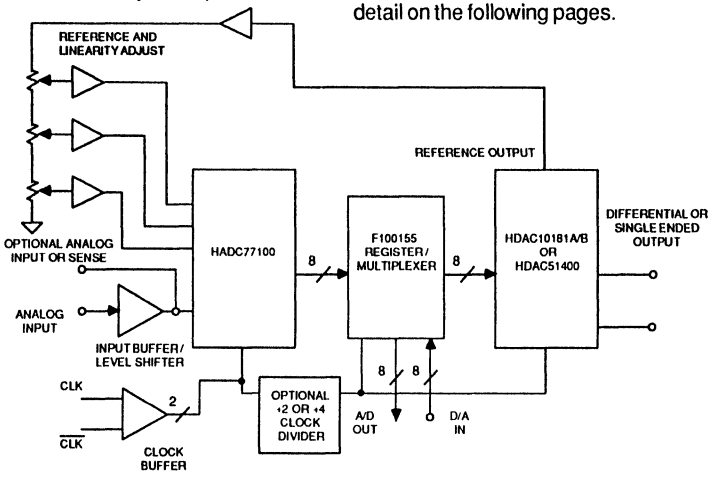
The HADC77100A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77100 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB100, with nominal power dissipation of less than 10 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

BLOCK DIAGRAM



**For Ordering Information See Section 1.*

EB101 EVALUATION BOARD

FEATURES

- **150 MSPS MINIMUM CONVERSION RATE**
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- ECL clock produced from any signal generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB101 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77200A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

The HADC77200A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

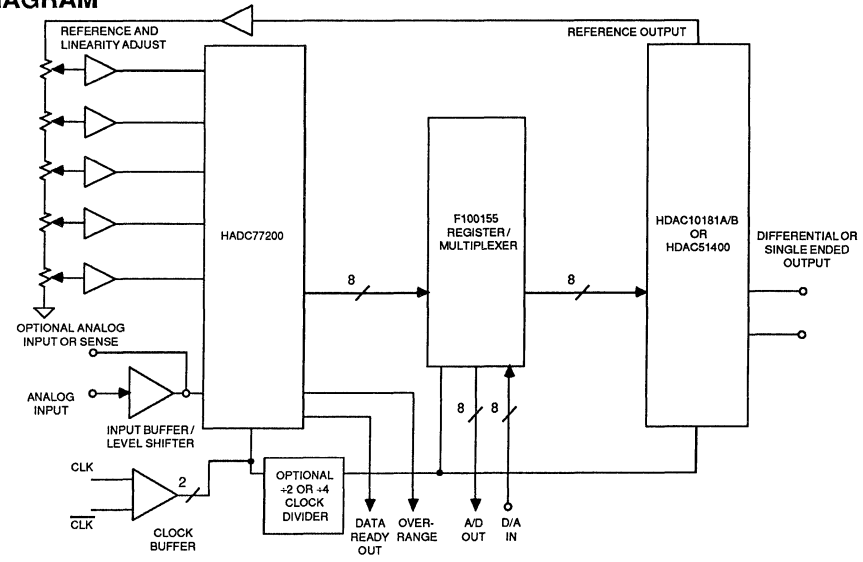
The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77200 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed dual differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB101, with nominal power dissipation of less than 11 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

7

BLOCK DIAGRAM



***For Ordering Information See Section 1.*

EB102 EVALUATION BOARD

FEATURES

- **USE WITH EB100/101 EVALUATION BOARDS**
- 70 MHz Full Scale input Bandwidth driving the converters
- Up to ±100mA Drive current
- Low Distortion
- 15nS Settling Time

APPLICATIONS

- Evaluation of HADC77100/200 A/D Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

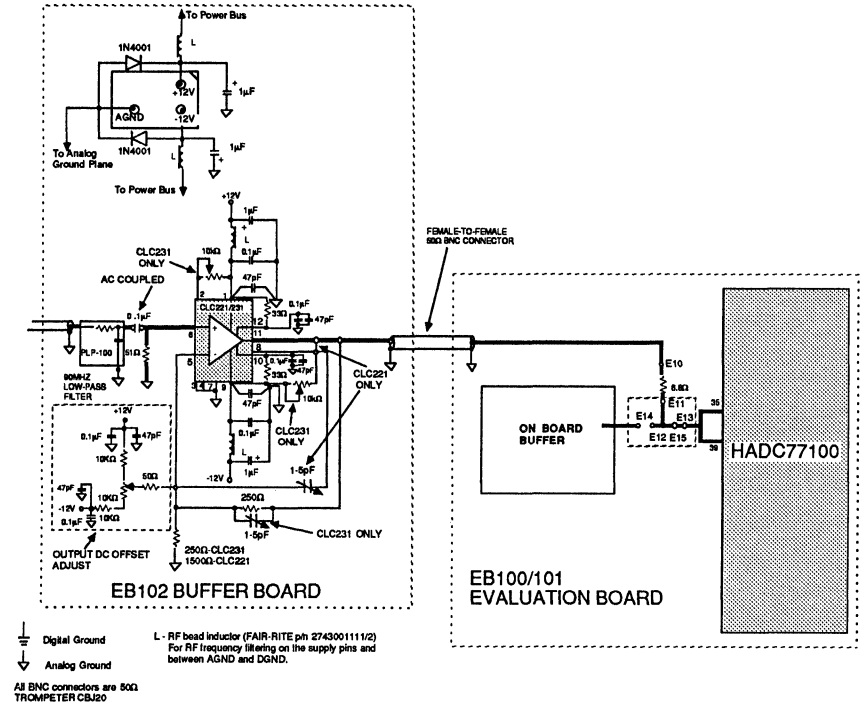
The EB102 is intended to demonstrate the high performance achievable with the HADC77100/200 flash A/D converters. The EB102 is a very low distortion, 70MHz buffer amplifier board. It provides for higher frequency operation than the buffer on the EB100 or EB101 evaluation boards. Included on the unit is either the Comlinear CLC221 Operational Amplifier or CLC231 Buffer-Amplifier as shown in the circuit diagram below.

The two versions are identical but are jumpered to provide for the different amplifier pinouts. The CLC221 version has the advantage of being configured up to a gain of 50 as required, and has slightly better harmonic distortion specifications. The CLC231 version has a much higher output drive capability and faster settling time.

The EB102 analog input and output are standard 50Ω BNC connectors. Standard ±12 to ±15 Volt power supplies are required for operation. The board comes fully assembled, calibrated and tested.

The HADC77100/200 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components from 50 up to 70 MHz into 8-bit digital words at a 150 MSPS update rate.

BLOCK DIAGRAM



**For Ordering Information See Section 1.*

EB103 EVALUATION BOARD

FEATURES

- **400 MSPS NOMINAL CONVERSION RATE**
- 100 to 150 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamp Comparator Design/Optional Input Buffer
- ECL Timing skew clock generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200/300 A/D Converters
- Evaluation of HDAC51400 D/A Converter
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB103 evaluation board is intended to show the performance of the HADC77200 or HADC77300 flash A/D converters in a ping-ponged mode, and the HDAC54100 Ultra High Speed D/A converter for reconstruction. Included on the unit are two 100K ECL multiplexers for combining the ping-ponged A/D converters' 16 bits of output data into 8 bits at twice the speed. The high speed data is routed between the A/D and D/A, and also off the board as full speed or as divided down data (external clock) for slower speed FFT measurements. This is shown in the block diagram below.

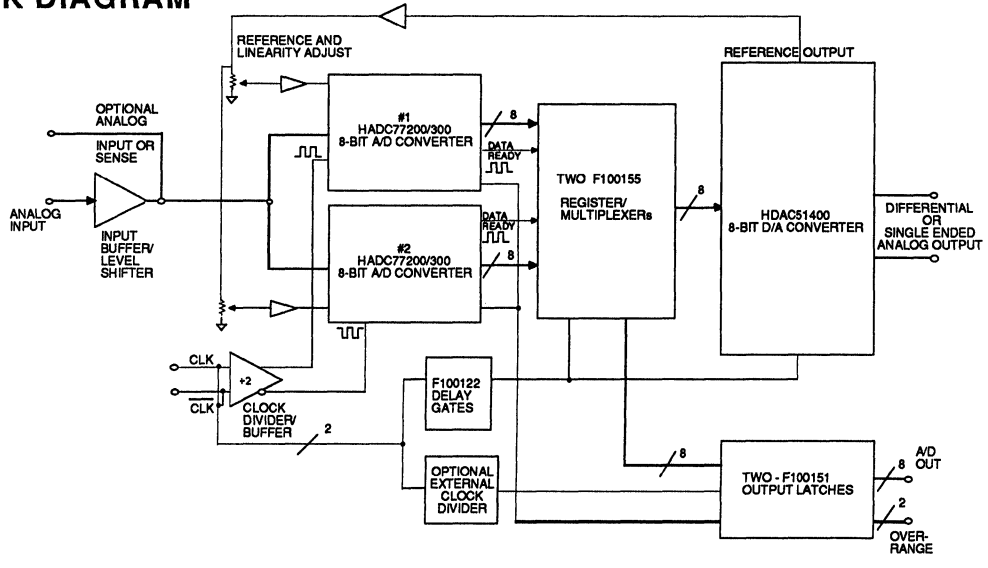
The HADC77200 is a monolithic, 8-bit flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 100 MHz at a 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HADC77300 is identical to the HADC77200 except that the analog input is 150MHz with a 250 MSPS clock rate and a corresponding increase in power dissipation.

The HDAC51400 is a monolithic 8-bit D/A converter capable of converting data at rates of 400 MWPS. The part has optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DAC has an internal reference to supply itself and the two HADC77200/300 with a stable voltage reference. It also has gain control to provide different output voltage swings so it can be used as a standard voltage output DAC.

The HCMP96870A is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the two A/D converters and D/A converter.

BLOCK DIAGRAM



**For Ordering Information See Section 1.*

EB104 EVALUATION BOARD

FEATURES:

- Provides operating environment for HADC574Z or HADC674Z and HDAC7545A Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold Amp and Output Op Amp IC's
- Unipolar or Bipolar Operation

APPLICATIONS:

- Evaluation/Comparison of HADC574/674Z Converters
- Evaluation/Comparison of HDAC7545A Converters
- System Development
- Data Acquision Systems
- Bus Structured Instrumentation
- Process Control Systems

GENERAL DESCRIPTION

The EB104 Evaluation Board fully demonstrates the capabilities of Honeywell's HADC574/674Z and HDAC7545A 12-bit data conversion products. All of the basic power supply connections, controls lines and external components are included. The board can operate in an analog input/output fashion utilizing both A/D and D/A devices, or the devices can be operated separately. Unlike most laboratory breadboarding, the ground-planed PC board provides the necessary low-noise evironment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins. When considering the HADC574/674Z or HDAC7545A for system design, the EB104 Evaluation Board provides a flexible, high performance evaluation vehicle.

The EB104 is supplied with an HADC574ZBCJ and an HDAC7545AACD. It will support all 574/674 and 7545 type devices.

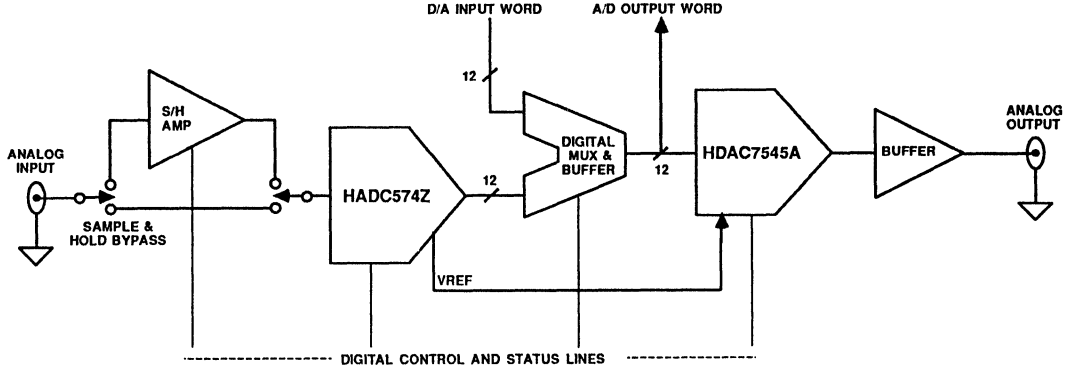


FIGURE 1 EB104 BLOCK DIAGRAM

***For Ordering Information See Section 1.*

EB105 EVALUATION BOARD

FEATURES

- Complete With Socketed HSCF24040ACD Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches for On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

APPLICATIONS

- HSCF24040 Evaluation
- Prototype System Development
- Programmable General-Purpose Subassembly

GENERAL DESCRIPTION

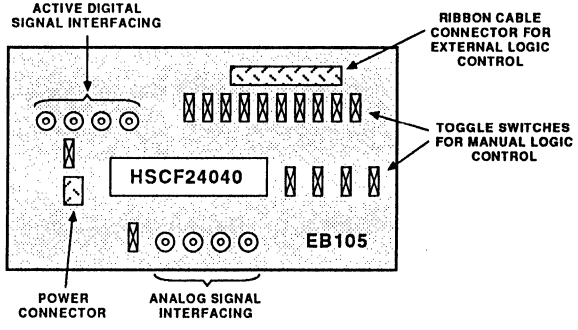
The EB105 Evaluation Board allows full exercise of the Honeywell HSCF24040 Programmable 7th Order Low Pass Active Filter. Unlike a handwired breadboard, this ground-planed, printed circuit board provides a high performance, noise-free environment. It provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is conveniently enabled by on-board toggle switches. Alternately, programming and control can be accomplished though the on-board ribbon cable connector. This option allows software control which can aid in system development.

By making full use of the HSCF24040, the EB105 provides an analog input and output for both the RC and switched-capacitor filters. Both of these low-pass filters are fully programmable. Analog interfacing is accomplished with on-board BNC connectors to minimize noise and digital signal coupling. The EB105 also makes use of separate analog and digital supply grounds to further minimize digital coupling.

A clock crystal is supplied on the board which utilizes the HSCF24040 crystal oscillator feature. An external time base can be used optionally. BNC connectors are provided for external clock input and clock output, for the $\overline{\text{CONVERT}}$ output and the $\overline{\text{SYNC}}$ control line. Use of BNC connectors on these active digital lines assure a minimum of digital to analog coupling.

7

FIGURE 1 EB105 BOARD FEATURES



**For Ordering Information See Section 1.*

EB100 EVALUATION BOARD 8-BIT, 150 MSPS FLASH A/D CONVERTER AND 8-BIT, 165 TO 400 MWPS RASTER D/A CONVERTER WITH REFERENCE

by Tom DeLurio Senior Applications Engineer

FEATURES

- **150 MSPS MINIMUM CONVERSION RATE**
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- Clock produced from any signal generator
- Improved Output Drive (Doubly-Terminated 50Ω)
- Optional clock divider board provided

APPLICATIONS

- Evaluation of HADC77100 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB100 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77100A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

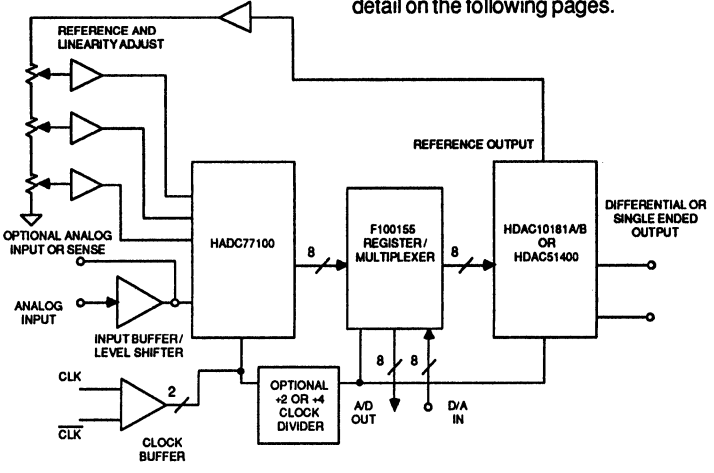
The HADC77100A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77100 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB100, with nominal power dissipation of less than 10 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

BLOCK DIAGRAM



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GENERAL INFORMATION

The EB100 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of Honeywell's HADC77100 8-bit A/D converter, HDAC-10181/54100 8-bit D/A converters and HCMP96870 dual comparator. The board contains circuitry for buffering the input signals, generating reference voltages, dividing the DAC and multiplexer clocks, routing input / output data, and generating ECL level differential clock signals from any signal generator. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments. The board requires -5.2, +5 and ±12 to ±15 Volt supplies.

The EB100 evaluation board consists of seven functional sections that include an analog input buffer, A/D converter, input/output multiplexer and data latches, D/A converter, reference voltage generator, ECL clock generator, and ECL clock divider. The analog and digital grounds are separated on the board for better system grounding characteristics.

There are numerous jumper options available to switch sections in or out of the system to suit individual needs. The clock divider circuitry is on a separate board that plugs into the main board to provide divide by 2 or 4 for the multiplexer and DAC. The jumper options will be discussed in more detail in the following sections. In addition, 90MHz low pass input and output filters are on board.

ON BOARD ANALOG INPUT BUFFER

This section consists of a 90MHz low pass filter, HA2539 high frequency op-amp, and a 2N5836 rf transistor. The input impedance is 50Ω and the gain is set at 2X so that a 1 Volt input can be applied. Compensation components are provided and can be adjusted for the desired frequency range needed. The compensation is factory adjusted for 50MHz bandwidth operation. The bandwidth of the buffer amplifier can be increased by decreasing the gain to 1X. The BNC connector shown in the schematics and layout near the output of the buffer can be used for monitoring the buffer output and input to the HADC77100. The BNC should be connected to a 50Ω terminated oscilliscope and will provide a 10X attenuated signal.

The positive input to the HA2539 is tied to an offset adjust to center the input signal to the HADC77100 around -1V , which is needed if a $2V_{p-p}$ input signal is applied. The input buffer can be bypassed by removing the 6.8Ω resistor at the emitter of the 2N5836 and the 450Ω resistor between the BNC connector and the HADC77100. Bypass the 450Ω resistor with a jumper wire and the HADC77100 can now be driven directly. The input impedance is 4KΩ in parallel with a 56pF distributed capacitance.

OPTIONAL ANALOG INPUT BUFFER BOARD - EB102

An alternate and higher performance input buffer is available as an option and sold separately. The EB102 is intended for users operating at the top end of the input bandwidth range of the HADC77100. The reason for a separate board is that the amplifiers utilized are quite a bit more expensive then the "on-board" buffer. But, with the added expense, increased input bandwidth with less harmonic distortion is realized.

There are two versions of the EB102 buffer board, one with a wideband op-amp (CLC221) and one with a wideband buffer amplifier (CLC231). Both versions are identical but are jumpered to provide for the different amplifier pinouts (See Figure 1A). The CLC221 version has the advantage of being configured up to a gain of 50 as required, and has slightly better harmonic distortion specifications. The CLC231 version has the advantage of a much higher output drive current and better settling time.

The Following table shows a breakdown of some of the more important specifications:

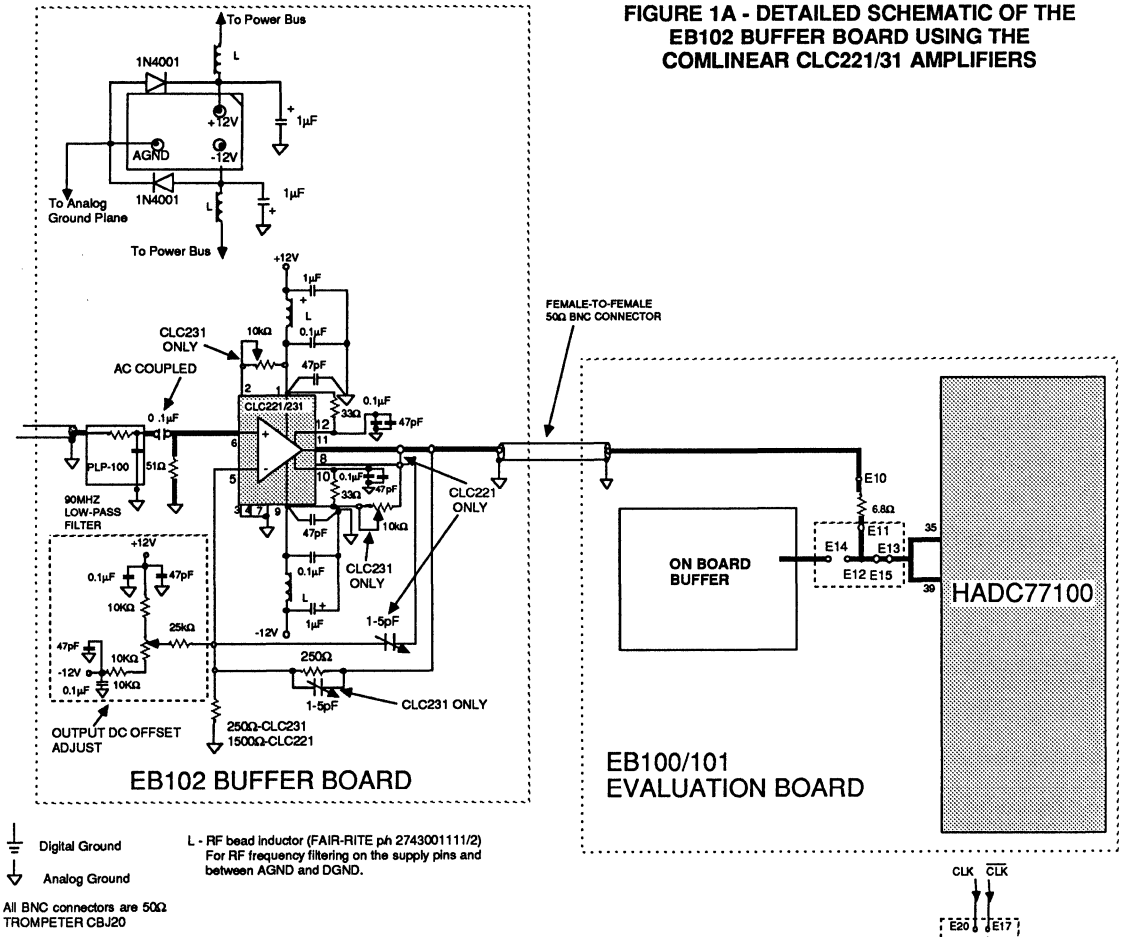
TABLE 1 - COMPARISON OF COMLINEAR CLC221/31 AMPLIFIERS

SPECIFICATION	CLC221	CLC231
Gain Range	±1 to 50	±1 to 5
Output (V, mA)	±12,500	±11,100
Slew Rate (V/µsec)	6500	3000
-3dB Bandwidth (Av=2)	275MHz	165MHz
Settling Time (nsec, %)	15, 0.1 18, 0.02	12, 0.1 15, 0.05
Harmonic(dBc) Second Distortion Third	-58 -62	-55 -59

100K ECL CLOCK GENERATOR

The ECL clock section consists of an HCMP96870 dual comparator, duty cycle and hysteresis adjust, F100131 triple D flip-flop and several jumper options. Any type high frequency signal generator can be connected to the BNC input to the comparators. Both inputs to the dual comparators are connected to the BNC. There are four outputs which generate differential 100K ECL clock signals. One set goes directly to the HADC77100 while the other two can go to the F100155 multiplexers and HDAC10181/51400 or to the clock divider circuitry.

FIGURE 1A - DETAILED SCHEMATIC OF THE EB102 BUFFER BOARD USING THE COMLINEAR CLC221/31 AMPLIFIERS



The threshold input to the HCMP96870 comparators are connected together to a pot to adjust the duty cycle of the clock. The latch enable pins are also connected together to a pot to adjust hysteresis.

100K ECL CLOCK DIVIDER

The clock divider section is shown below in Figure 1B and consists of a triple D type flip-flop, which if jumpered as shown, will provide divided down clock outputs. The clock divider can be bypassed to provide a full frequency clock. The divider is provided to make it easier to monitor the HADC77100 output with a low frequency logic analyzer and to provide the DAC with a reduced sampling rate. When switching between divide by 2 or 4, the unused outputs "Q" and "$\overline{Q}$" must be terminated. The board is initially set in the divide by 4 mode. Furthermore, the jumpers on the clock lines to the multiplexer and DAC must be removed.

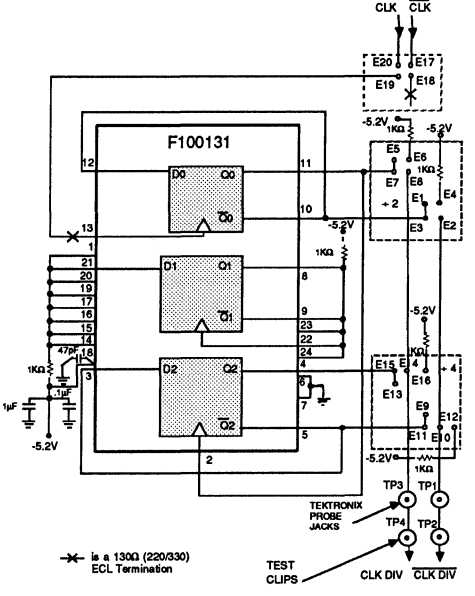


FIGURE 1B - 100K ECL CLOCK DIVIDER

REFERENCE VOLTAGE GENERATOR

The reference voltage for the HADC77100 and HDAC-10181/51400 is internally generated by the D/A converter voltage reference of approximately 1.2Volts. The A/D converters 2Volt reference, 1Volt midtap and ground are controlled by the PMI quad op-amp OP-11. The magnitude of each setting is further adjusted with potentiometer R26, R25, and R32 as shown in the detailed schematic and board layout.

INPUT/OUTPUT REGISTER AND MULTIPLEXER

The multiplexer section consists of two F100155 which select between external 8-bit digital data from the 64-pin DIN connector or data from the output of the HADC-77100. The choice is controlled by tying the SELECT pins to either an ECL high for external data or an ECL low for HADC77100 data. This data is then fed to the HDAC10181/51400 on the "Q" outputs of the F100155 and the "Q" outputs are tied to the external connector.

A/D CONVERTER SECTION

Both input pins to the HADC77100 are tied together to be either fed by the input buffer or by an external source. The MINV and LINV inputs are left open and tied internally to an ECL low. Diodes are provided to tie them high and change the output logic. The connection choices for determining the output logic are in Table 2.

D/A CONVERTER SECTION

The D/A converter section contains jumpers to use either the HDAC10181 or HDAC51400. The primary difference in the two parts is the reference voltage connections. These differences are shown in the detailed schematic in Figure 2. All EB100 boards and jumpers will be connected for the HDAC10181A part. If an HDAC51400 is indicated when the board is ordered (See last page), the board jumpers must be configured as shown in Figure 4A and 4B by the user.

The output current magnitude for the HDAC10181/51400 is controlled by a potentiometer (R36) through the DAC's Iset control pin. In addition, two 90 MHz low pass filters are provided at both out- and out+ output pins as well as 50Ω terminating resistors. The terminating resistors can be changed to 75Ω if desired. Keep in mind that the transmission line must be terminated at the receiving end with the same value resistor. The video and feedthrough controls are routed to the 64-pin DIN connector and are normally disabled.

TABLE 2 - OUTPUT LOGIC CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: VIH, VOH
0: VIL, VOL

TABLE 2A - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO.	FUNCTION
R26	Pot for adjusting gain to produce a 2V reference voltage for the VRB pin on the HADC77100 from the1.2V reference voltage supplied by the HDAC10181/51400.
R25	Pot for setting the linearity adjustment or midtap pin (VRM ≈ 1V) on the HADC77100.
R32	Pot for setting the top point (VRT) on the reference voltage ladder. Nominally set at 50mV below AGND.
R36	Pot for adjusting output current drive from the HDAC10181/51400 (See data sheets). Vout+=25.6(digital code X Iset)/RL
R5	Pot for setting the HCMP96870 comparator threshold voltage to adjust the ECL clock duty cycle.
R4	Pot for adjusting comparator hysteresis.
R23	Pot for adjusting up to a 2V offset voltage at the buffer output for driving the HADC77100.
R22	Pot for adjusting compensation for the buffer. This has been set for a flat response. The frequency range can be increased at the expense of gain peaking and phase margin reduction by decreasing the potentiometer resistor value.
C25	"Lead" Capacitor for controlling gain peaking in the input buffer. Used in conjunction with Pot R22 and Cap C44 for the HA2539.
C44	"Lag-lead" compenstion capacitor used with R22.

POWER SUPPLY CONNECTIONS

Power to the EB100 is supplied through a six pin Molex type connector. The supply lines are color coded as shown in Figure1C. Connect the wire end of the power supply harness to power supplies as shown by Figure 1C and the silk screen near the mating connector on the PC board itself. The power harness is attached to the board with the bevelled edges and hollow connector alligned to the mating connector.

The power requirements for the EB100 at different supplies and with or without the clock divider board is shown in Table 3. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

TABLE 3 - POWER DISSIPATION

EB100 WITH CLOCK DIVIDER, ±15V			
Voltage	Current	Power	
+15V	.145A	2.175W	
-15V	.148A	2.220W	
+5V	.006A	0.030W	
-5.2V	1.39A	7.228W	
		11.653W	
EB100 W/O CLOCK DIVIDER, ±12V			
Voltage	Current	Power	
+12V	.119A	1.428W	
-12V	.123A	1.476W	
+5V	.006A	0.030W	
-5.2V	1.27A	6.604W	
		9.538W	

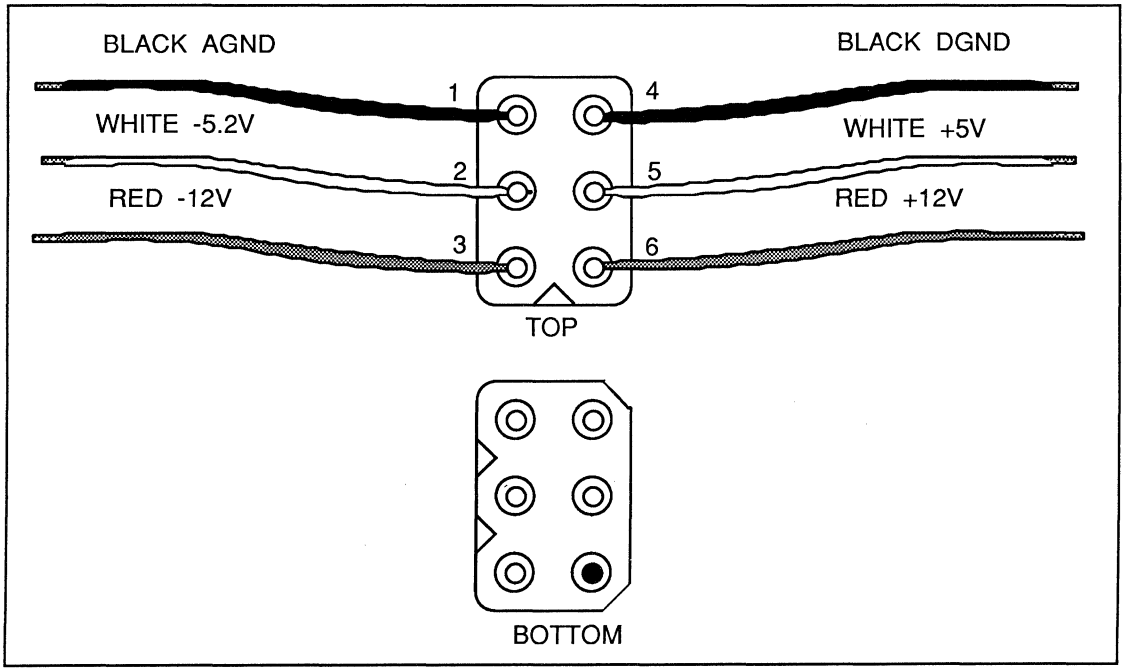


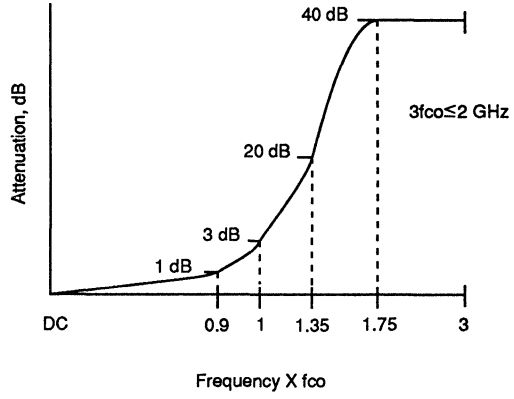
FIGURE 1C - POWER SUPPLY HARNESS CONFIGURATION

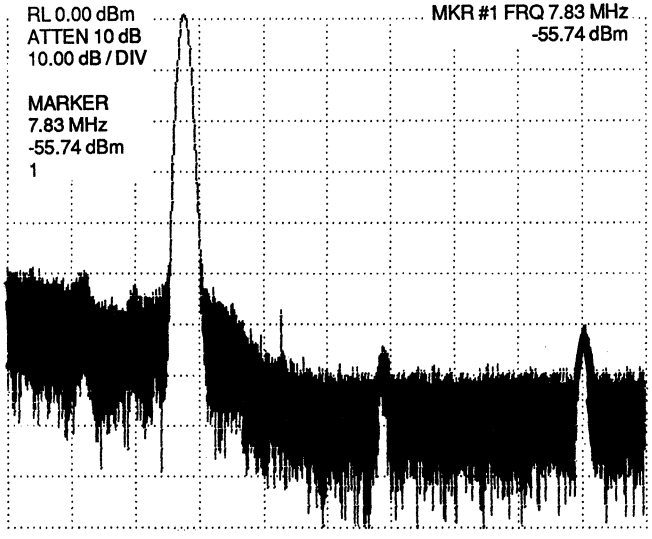
ANTI-ALIASING AND CLOCK NOISE FILTERS

The input to the EB100 buffer circuitry and the differential outputs from the D/A converter are provided with high frequency noise filters. The three filters are 90MHz low pass and are intended to be used with the full analog input frequency and full clock sampling rate of the HADC77100 A/D converter. If lower frequencies are used, the filters should be changed to filter clock noise and harmonics for a particular application. Mini-Circuits Inc. (see below) supplies a range of low pass filters that fit into the same position as the 90MHz filters on the EB100 Evaluation board.

Also, adjustment of the clock duty cycle with potentiometer R5 will lower the overall noise floor by controlling the setup and hold time of the digital data for the multiplexers (F100155) and DAC (HDAC10181).

Low Pass
Typical Frequency Response



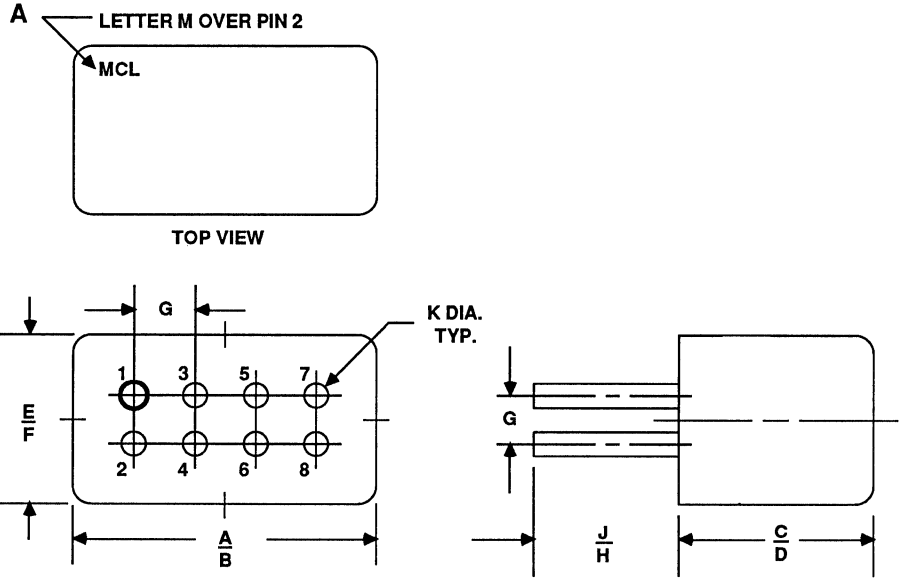


DAC OUTPUT SPECTRUM ANALYSIS OF A 10MHz INPUT FUNDAMENTAL WITH 10.7MHz (PLP-10.7) INPUT/OUTPUT LOW PASS FILTERS AND 100MHz CLOCK RATE

PLP
case A01

MODEL NO.	PASSBAND, MHz (loss < 1dB) Min.	fco, MHz (loss 3dB) Nom.	STOP BAND, MHz (loss > 20dB) Max.	STOP BAND, MHz (loss > 40dB) Max.	STOP BAND, MHz (loss > 40dB) Min.	VSWR, Passband Typ.	VSWR, Stopband Typ.
PLP-10.7	DC-11	14	19	24	200	1.7	1.7
PLP-50	DC-48	55	70	90	200	1.7	17
PLP-70	DC-60	67	90	117	300	1.7	17
PLP-100	DC-98	108	146	189	400	1.7	17

Case no.	A	B	C	D	E	F	G	H	J	K
A01	.770	.800	.385	.400	.370	.400	.200	.20	.14	.031
	19.56	20.32	9.78	10.16	9.40	10.16	5.08	5.08	3.56	.79



NOTE: BLACK BEAD INDICATES PIN 1. PIN NUMBERS DO NOT APPEAR ON UNIT. FOR REFERENCE ONLY.

PIN CONNECTIONS

SEE CASE STYLE OUTLINE DRAWING

SERIES	IN	OUT	GROUND
PLP	1	8	2, 3, 4, 5, 6, 7

FIGURE 2 - DETAILED SCHEMATIC OF EB100, REVISION C

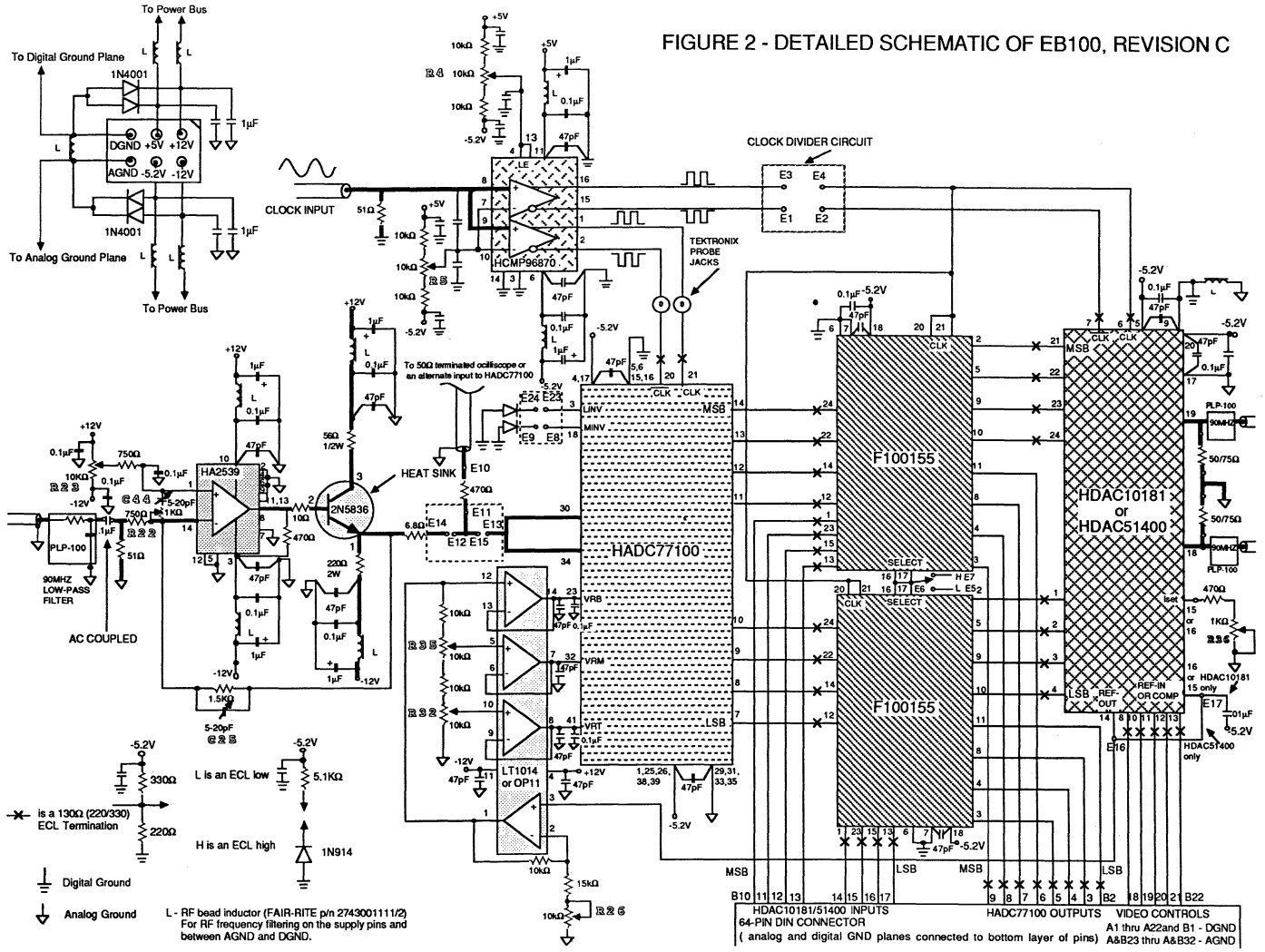


FIGURE 3 - TIMING DIAGRAM

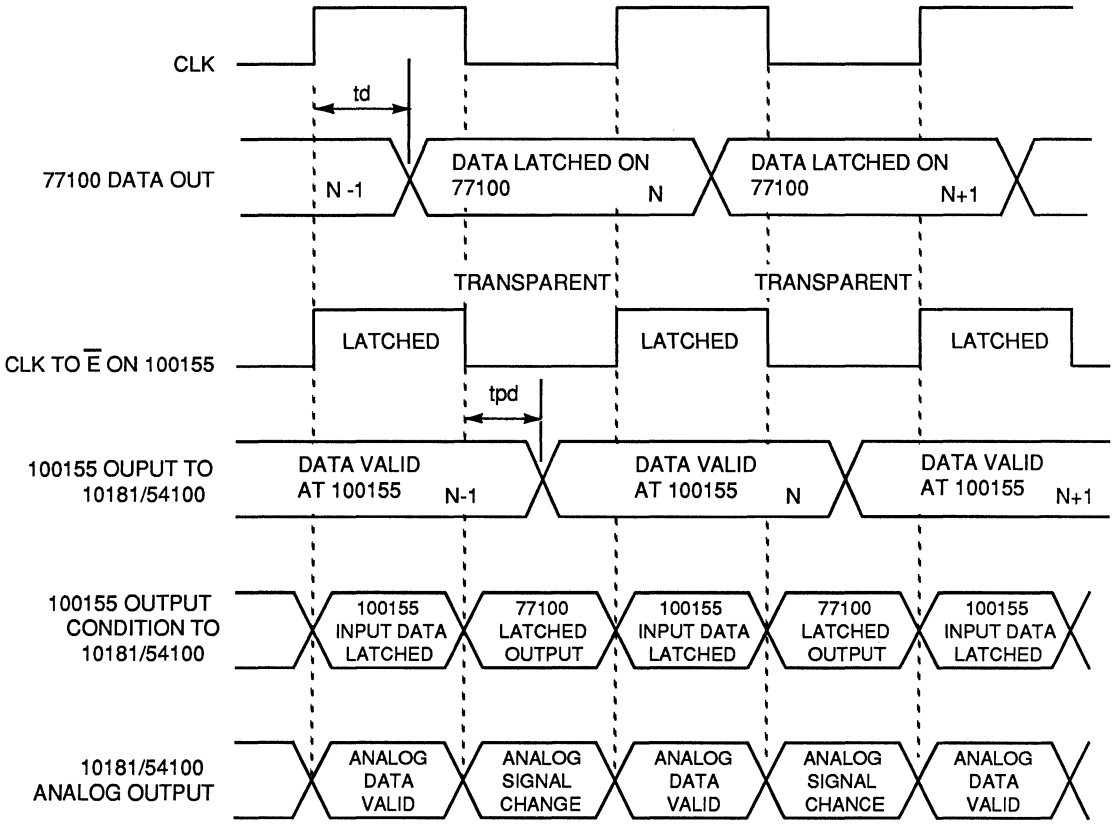


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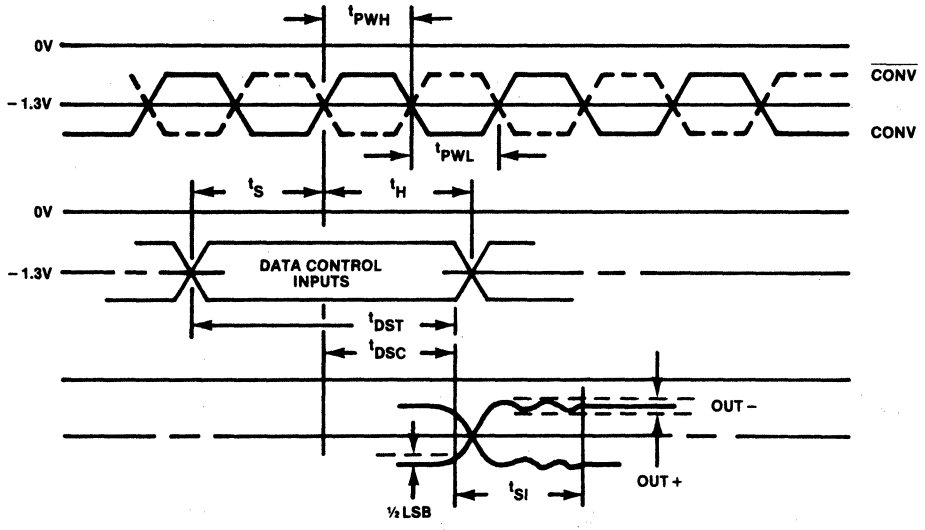
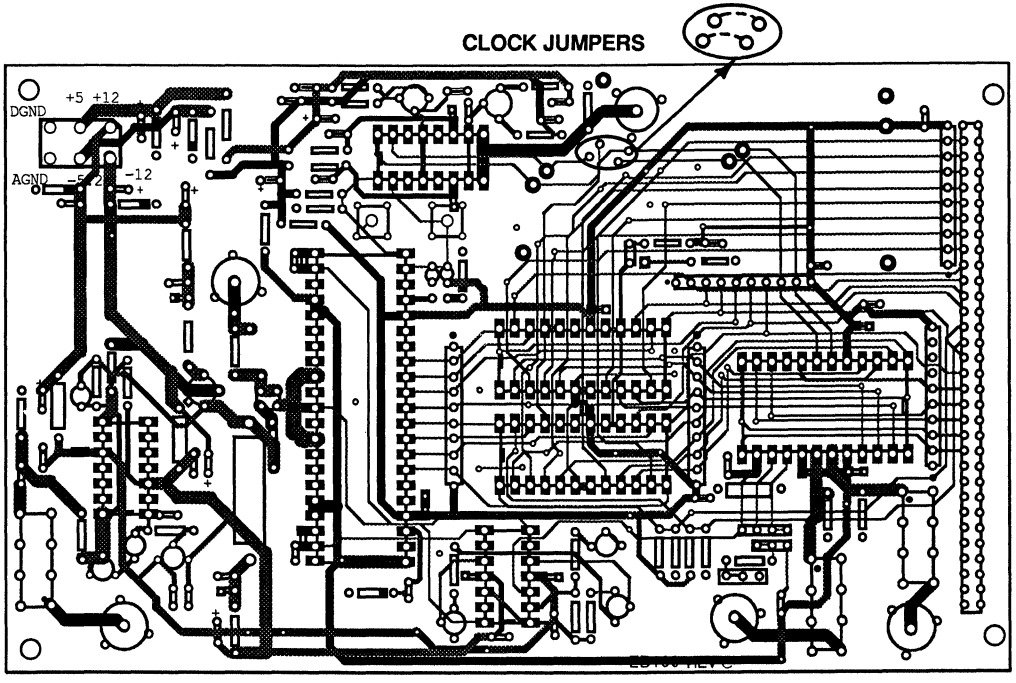
Figure 3 Continued 10181/51400 Timing Diagram





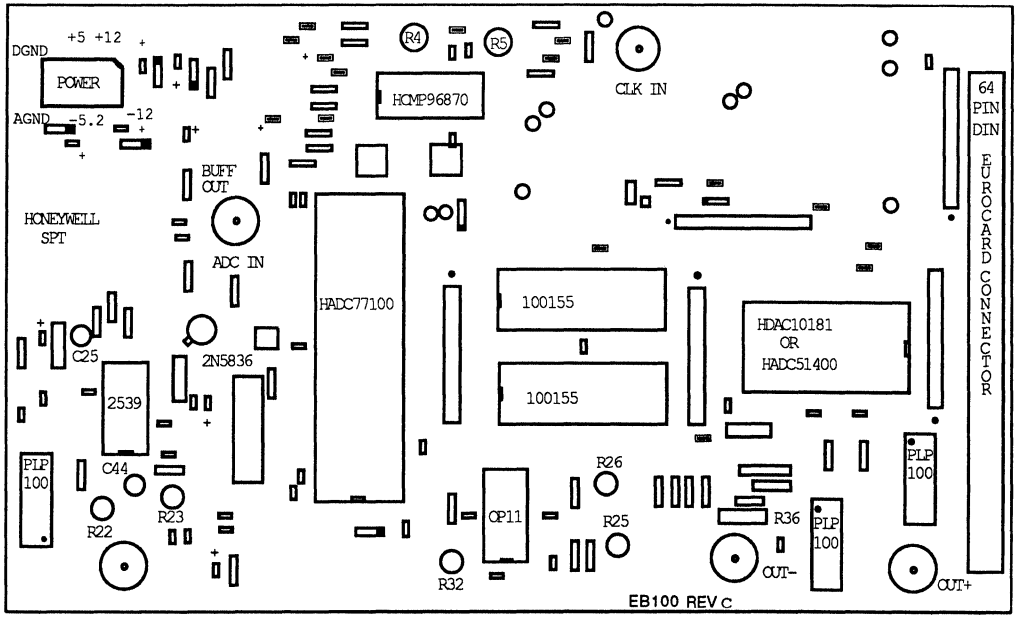


FIGURE 4A - MAIN BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

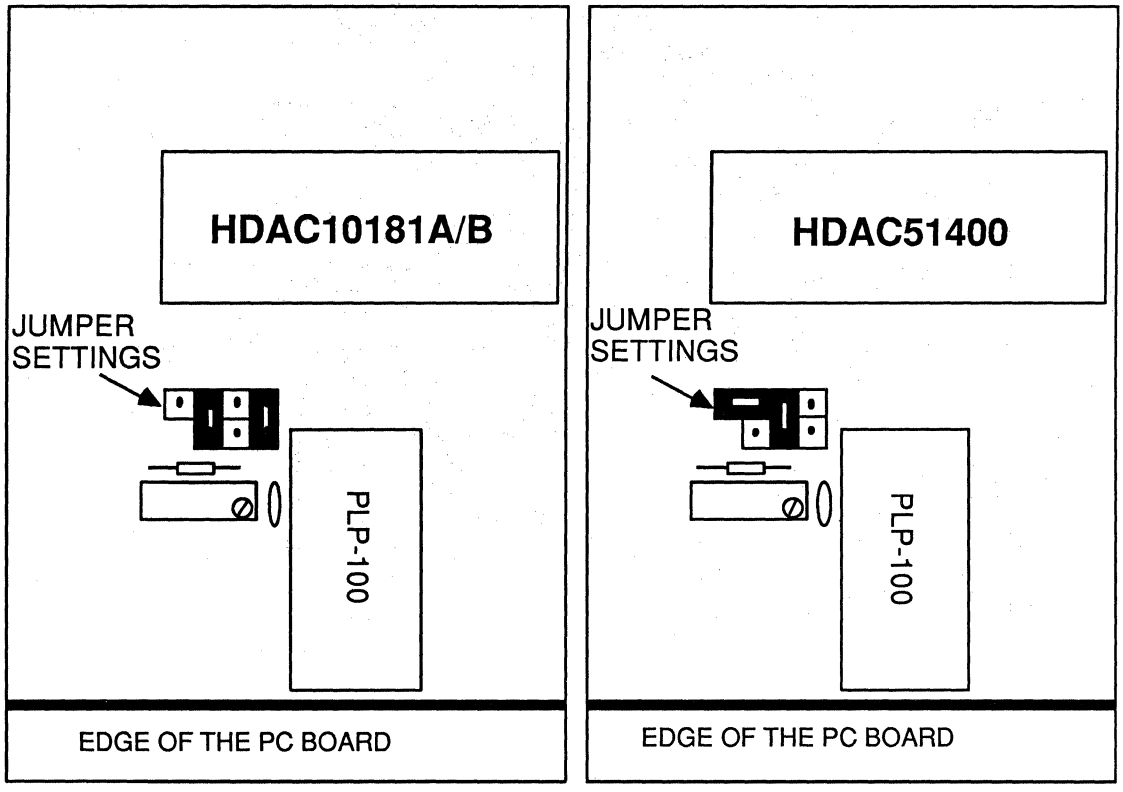
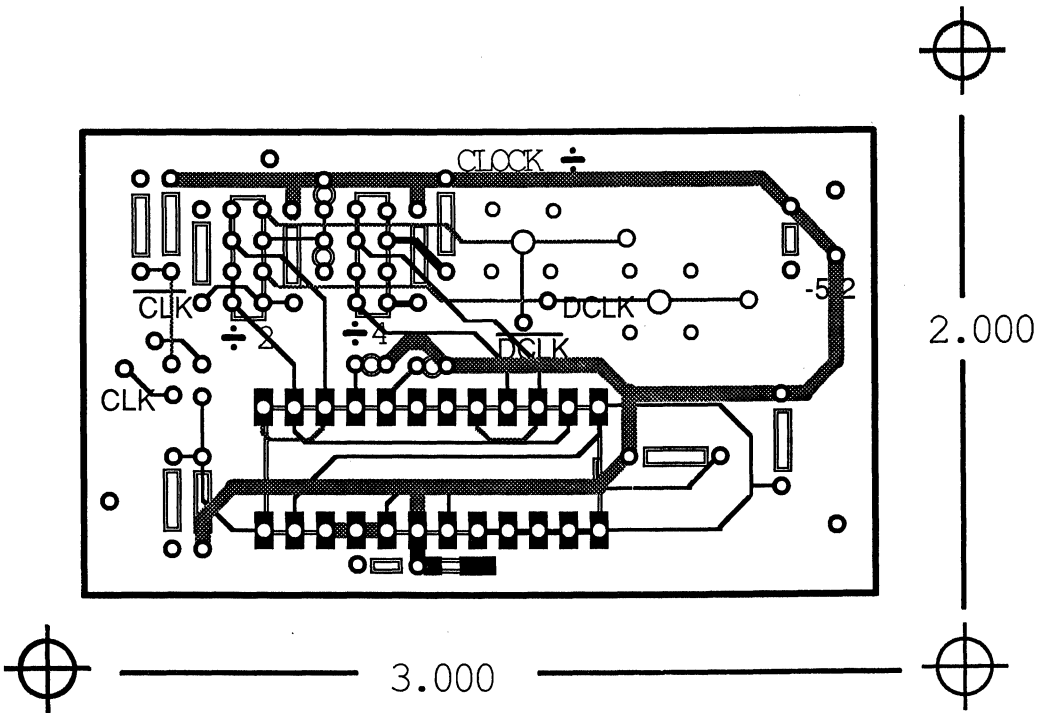


FIGURE 4B - JUMPER POSITION AND CONNECTIONS FOR EITHER THE HDAC10181A/B OR HDAC51400
(Not To Scale)



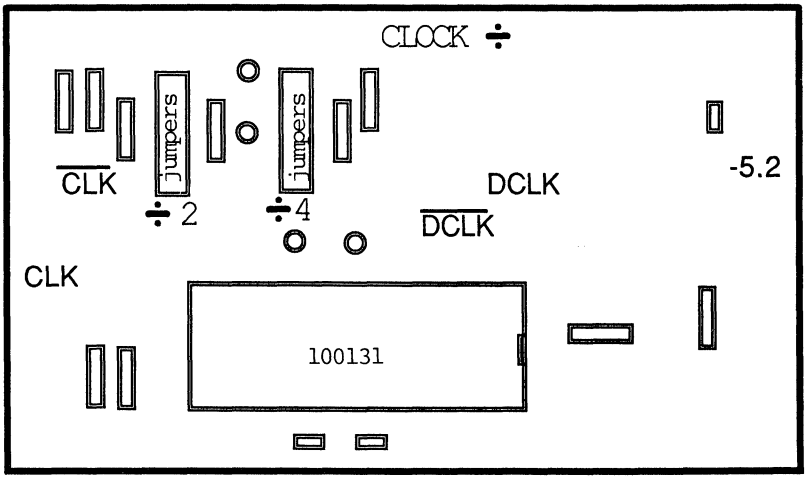


FIGURE 5 - CLOCK DIVIDER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

EB100 REVISION C PARTS LIST

PARTS LIST			
NO.	**DESCRIPTION**	**QTY.**	**MANUFACTURER / PART NO.**
1	FERRITE BEAD	11	FAIR-RITE CORP.-2743001111
2	DIODE	4	1N4001
3	TRANSISTOR	1	MOTOROLA-2N5836
4	I.C.	1	HONEYWELL-HDAC10181A/B OR HDAC51400
5	I.C.	1	HONEYWELL-HCMP96870
6	I.C.	2	FAIRCHILD-F100155
7	I.C.	1	PMI-OP-11
8	I.C.	1	HONEYWELL-HADC77100B
9	I.C.	1	HARRIS-HA2539
10	FILTER	3	MINI-CIRCUITS-PLP-100
11	RESISTOR	1	240Ω, 2w
12	RESISTOR	1	56Ω, 1/2w
13	RESISTOR	1	6.8Ω, 1/8w
14	RESISTOR	7	10KΩ, 1/8w
15	SIP RESISTOR PACK	5	220/330Ω
16	RESISTOR	4	220Ω, 1/8w
17	RESISTOR	4	330Ω, 1/8w
18	RESISTOR	2	750Ω, 1/8w
19	RESISTOR	3	50Ω, 1/8w
20	RESISTOR	3	470Ω, 1/8w
21	RESISTOR	1	10Ω, 1/8w
22	RESISTOR	1	15.1Ω, 1/8w
23	RESISTOR	1	5kΩ, 1/8w
24	RESISTOR	1	1.5kΩ, 1/8w
25	POTENTIOMETER	2	BOURNS-1KΩ, 3329-H-102 & MOUSER-ME323-4290W-1kΩ
26	POTENTIOMETER	6	BOURNS-10KΩ, 3329-H-103
27	CONNECTOR, DIN	1	BELL IND.-905-72184C
28	CONNECTOR	1	MOLEX-09-18-5069
29	CAPACITOR, CHIP	16	JOHANSON-47pf 500R15N470JP4
30	CAPACITOR	10	SPRAGUE-1uf TANT, 35V
31	CAPACITOR	29	SPC TECHNOLOGY-0.1μf
32	CAPACITOR, ADJ	2	JOHANSON-47pF-9629
33	CONNECTOR, BNC	5	TRUMPETER-CBJ20, 50Ω
34	TEST POINTS	2	TEKTRONIX 131-2766-01,136-0352-02
35	PIN RECEPTACLE	42	MILL MAX-0552-1-15-15-11-27-10-0
36	PIN SOCKET	9	SAMTEC-SL-132-G-12
37	SOCKET, 24PIN	1	SAMTEC-ICO-624-NGT
38	PRINTED CIRCUIT BOARD	1	HONEYWELL-EB100

EB100 CLOCK DIVIDER BOARD

NO.	DESCRIPTION	QTY.	MANUFACTURER / PART NO.
39	F100131	1	FAIRCHILD TRIPLE D-TYPE FLIP-FLOP
40	CAPACITOR	2	.1μF
41	TEST POINTS	2	TEKTRONIX 131-2766-01, 136-0352-02
42	RESISTOR	6	1KΩ, 1/8w 5%
43	RESISTOR	4	220Ω,1/8w 5%
44	RESISTOR	4	330Ω, 1/8w 5%
45	CAPACITOR	1	JOHANSON-47pF CHIP
46	TEST POINTS	2	COMPONENTS CORP.-TP-102

PARTS LIST				
NO.	REF. DESIG.	QTY.	DESCRIPTION	MANUFACTURER / PART NO.
1	C1, 3, 5, 8, 12, 13, 15	7	CAPACITOR, .1µf - 50V	AVX / SR205E104MAA
2	C2, 4, 7, 14	4	CAPACITOR, 47pf - CHIP	JOHANSON / 500R15N470JP4
3	C10, 11, (NOTE 3)	2	CAPACITOR, SEALTRIM 5-20pf	JOHANSON / 9629
4	CR1, 2	2	DIODE, 1N4001	
5	E1, 2	2	JUMPER PINS (HEADER STRIP)	CYPRESS / TSW-1-36-07-T-S
6	FL1	1	FILTER, 90MHz LOWPASS	MINICIRCUITS / PLP-100
7	J1, 2 (NOTE4)	2	RECEPTACLE, BNC	TRUMPETER / CBJ20
8	L1, 2	2	RF BEAD	FAIR-RITE / 2743001111/2
9	P1	1	PLUG	MOLEX / 09-18-5031
10	R1, 2	2	RESISTOR, 10K OHM	HAMILTON / AVNET / CF1/8-10K-5%-T/R
11	R4, 12	2	RESISTOR, 33 OHM	HAMILTON / AVNET / CF1/8-33-5%-T/R
12	R5	1	RESISTOR, 25K OHM	HAMILTON / AVNET / CF1/8-25K-5%-T/R
13	R7 (NOTE 1)	1	RESISTOR, 1.5K OHM	HAMILTON / AVNET / CF1/8-1.5K-5%-T/R
14	R7, 8 (NOTE 2)	2	RESISTOR, 250 OHM	HAMILTON / AVNET / CF1/8-250-5%-T/R
15	R9	1	RESISTOR, 150 OHM	HAMILTON / AVNET / CF1/8-150-5%-T/R
16	R10	1	RESISTOR, 51 OHM	HAMILTON / AVNET / CF1/8-51-5%-T/R
17	R3	1	POTENTIOMETER, 10K OHM	BOURNS / 3339-1-103
18	R6, 11	2	POTENTIOMETER, 1M OHM	BOURNS / 3339-1-106
19	C6, 9	2	CAPACITOR, 1µf TANT, 35V	SPRAGUE / 196 DIO5X9035HAI
20	U1 (NOTE 1)	1	I.C., OP-AMP	COMLINEAR / CLC221A1
21	U1 (NOTE 2)	1	I.C., BUFF-AMP	COMLINEAR / CLC231A1
22	PCB1	1	PRINTED CIRCUIT BOARD	HONEYWELL / EB102 REV. B

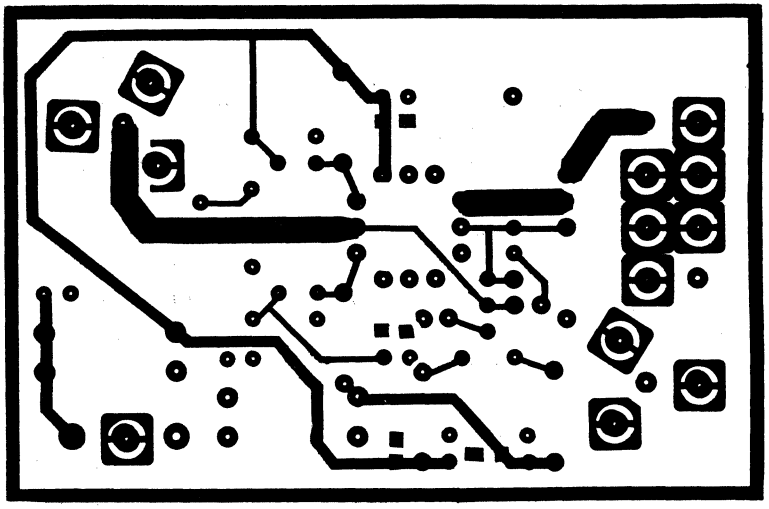
NOTES:

1) USE ITEM NO. 13 WITH ITEM NO. 20 AND JUMPER E1, 2.

2) USE ITEM NO. 14 WITH ITEM NO. 21.

3) USE C10 WITH ITEM NO. 21 ONLY.

4) J2 IS MOUNTED ON THE BACKSIDE OF PCB1.



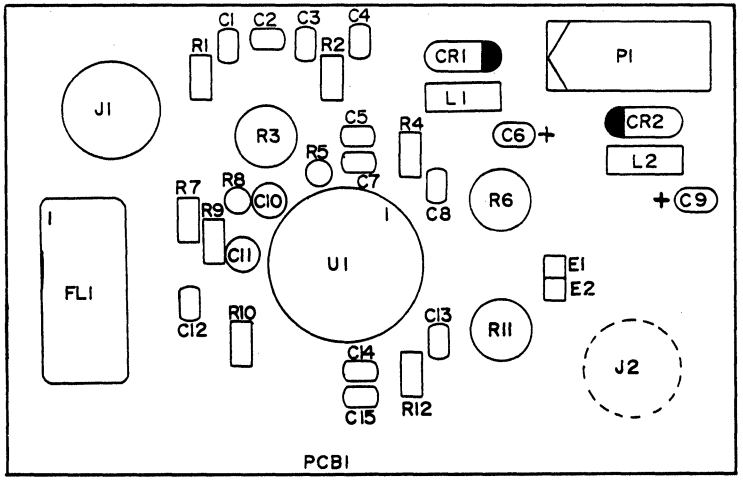


FIGURE 6 - EB102 BUFFER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

SET-UP PROCEDURE FOR THE EB100 DEMONSTRATION BOARD

The following setup procedure is completed at Honeywell before the EB100 board is shipped to the customer. It is not necessary for the user to perform this exercise, but it is included for informational purposes.

The EB100 demonstration board is accompanied with a literature package containing the "AN100 APPLICATION NOTE" , the "HADC77100", "HDAC51400", "HDAC-10181", and "HCMP96870" data sheets, and an applications department business card. Also, a power harness, and a capacitor alignment tool are included. If there are any questions, please call the applications engineer on the card.

STEP 1

Connect the wire end of the power supply harness to power supplies as shown in Figure 1C. The power harness should be connected to the board with the bevelled edges and hollow connector alligned for correct operation.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

Table 3 (page 6) shows the power requirements for the EB100. Use the current gauges on the power supply or a DMM in line with the power lines and set on current (I). these current values will vary somewhat until all the potentiometers are adjusted. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

STEP 2

Refer to Figure 2 and 4 on the previous pages. Place a DMM probe (set to voltage selection) on the black jumpers at the input to the HADC77100 (E14). This should read -1V and is adjusted by turning potentiometer R23 (See Table 2A).

STEP 3

Again, refer to Figures 2 and 4 on the previous pages and Table 5 on this page. Place a DMM probe (set to voltage selection) on pin 3 of the OP11 and read approximately -1.2V. If it does not then check to see if the black jumpers for the HDAC10181/51400 are set up

TABLE 5 - EQUIPMENT LIST

2 - SIGNAL GENERATORS CAPABLE OF PRODUCING 1MHZ AND 20MHZ SINEWAVES AT UP TO 1Vp-p OUTPUT LEVELS INTO 50Ω. H.P. 8656A OR EQUIVALENT.

1 - OSCILLISCOPE, EITHER H.P. DIGITIZING OSCILLISCOPE MODEL 54100D OR EQUIVALENT OR TEKTRONIX MODEL 2465.

1 - DIGITAL MULTIMETER(DMM), KEITHLEY 197 OR EQUIVALENT.

4 - POWER SUPPLIES CAPABLE OF PRODUCING THE POWER LISTED IN TABLE 1. 2 LAMBDA LPT-7202-FM OR EQUIVALENT.

5 - 50Ω COAX CABLES (RG58) WITH BNC TYPE CONNECTORS.

1 - HIGH IMPEDANCE PROBE (1MΩ) - TEKTRONIX OR H.P.

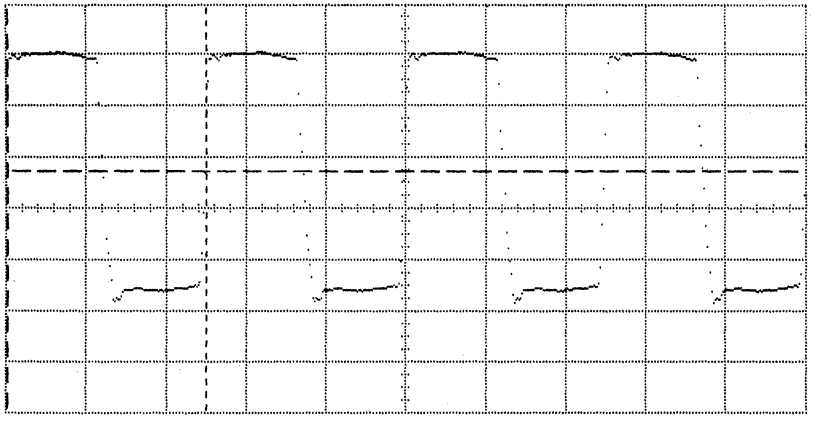
for the right part (see Figure 4B). Next set the probe on pin 1 of the OP11. This should read -2V and is adjusted by turning potentiometer R26. Now set the probe on pin 7 of the OP11. This should read approximately -1V and is adjusted by potentiometer R35. Pin 8 of the OP11 should read approximately -50mV and is adjusted by potentiometer R32.

STEP 4

Refer to Figures 2 and 4. Attach a 50Ω BNC cable to the "CLK IN" BNC connector. Attach the other end to a sinewave or signal generator set at 20MHz frequency and 1Vp-p amplitude (if 1Vp-p is not available, amplitudes down to 100mVp-p are acceptable). Put a Tektronix or H.P. high impedance probe in one or both of the probe jacks immediately below the HCMP96870 comparator. Adjust potentiometer R5 to achieve a 50% duty cycle square wave (both "high" and "low" states are the same length). Adjust potentiometer R4 if no waveform is present and/or to get rid of any jitter in the square wave (this is a hysteresis adjustment). The square wave amplitude should be approximately 900mVp-p and look like Figure 7 below.

STEP 5

Refer to Figure 2 and 4. Attach a 50Ω coax cable to the BNC connector marked "BUFFER IN". Use a second sinewave or signal generator set at 1 MHz frequency and 1Vp-p amplitude (See Figure 8). Attach another cable to the BNC connector "A/D IN / BUFFER OUT" and to an oscilliscope set at 50Ω input impedance. A 200mVp-p amplitude signal swinging around -100mVdc should apear at a 1MHz frequency (See Figure 9). If oscillation is evident (erratic signal amplitude or wrong frequency), potentiometer and capacitor C44 must be adjusted as well as capacitor C25. Adjust capacitor C25 first to minimize the oscillation. If this does not work, set it at the lowest amplitude oscillation and adjust potentiometer R22. Adjust potentiometer R22 to midturn and then adjust capacitor C44 until the oscillation stops. See Figures 10, 11, and 12.



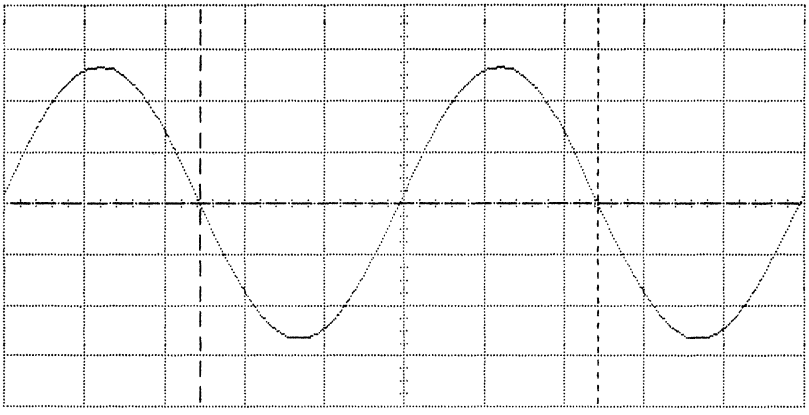
-100.000 nsec 0.00000 sec 100.000 nsec

Ch. 2	=	200.0 mvolts / div	Offset	=	-1.330 volts
Timebase	=	20.0 nsec / div	Delay	=	0.00000 sec
Ch. 2 Parameters			P-P Volts	=	968.7 mvolts
Rise Time	=	1.670 nsec	Fall Time	=	2.910 nsec
Freq.	=	20.1532 MHz	Period	=	49.620 nsec
+ Width	=	24.940 nsec	- Width	=	24.680 nsec
Overshoot	=	6.249 mvolts	Preshoot	=	43.75 mvolts

Trigger mode: Edge
On Pos. Edge on Chan2
Trigger Levels
Chan2 = -1.180 volts
Holdoff = 70.000 nsecs

FIGURE 7 - CLOCK OUTPUT AT THE TEKTRONIX PROBE JACKS

FIGURE 8 - INPUT SIGNAL TO THE BOARD (50Ω INPUT IMPEDANCE)



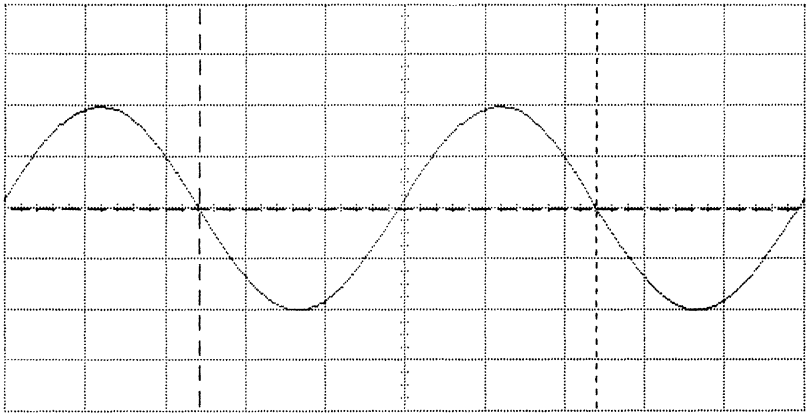
-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	1.062 volts
Rise Time	=	289.640 nsec	Fall Time	=	289.320 nsec
Freq.	=	1.00014 MHz	Period	=	999.860 nsec
+ Width	=	497.520 nsec	- Width	=	502.340 nsec
Overshoot	=	6.249 mvolts	Preshoot	=	6.249 mvolts

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels

Chan1	=	0.000 volts
Holdoff	=	70.000 nsecs

FIGURE 9 - OUTPUT SIGNAL FROM THE "BUFFER OUT" BNC CONNECTOR (50Ω IMPEDANCE)



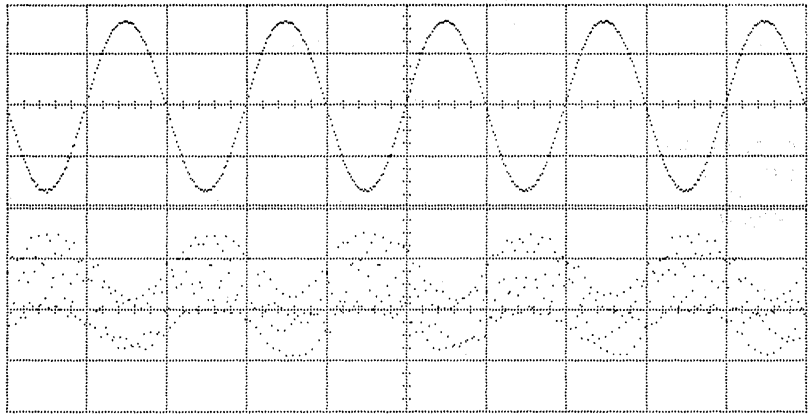
-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	50.00 mvolts / div	Offset	=	-100.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	200.0 mvolts
Rise Time	=	294.080 nsec	Fall Time	=	289.910 nsec
Freq.	=	997.904 KHz	Period	=	1.00210 usec
+ Width	=	499.810 nsec	- Width	=	502.290 nsec
Overshoot	=	1.562 mvolts	Preshoot	=	1.562 mvolts

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels

Chan1	=	-100.0 mvolts
Holdoff	=	70.000 nsecs

FIGURE 10 - OSCILLATIONS ARE APPARENT AND ADJUSTMENT IS NECESSARY

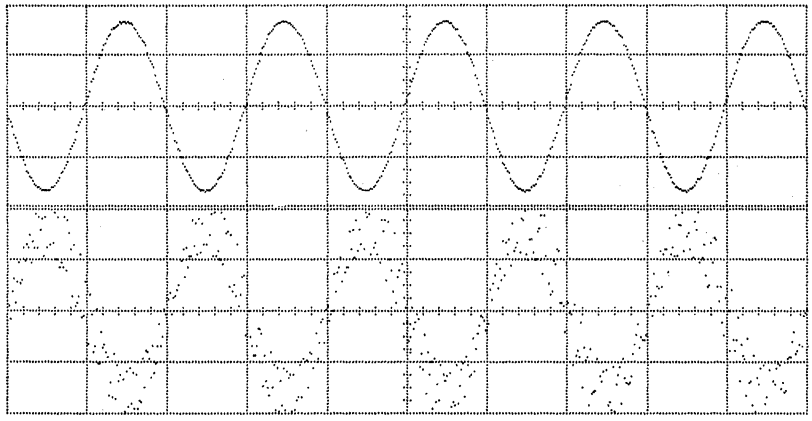


-2.50000 usec 0.00000 sec 2.50000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Ch. 2	=	40.00 mvolts / div	Offset	=	-102.0 mvolts
Timebase	=	500 nsec / div	Delay	=	0.00000 sec

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 0.000 volts
Holdoff = 70.000 nsecs

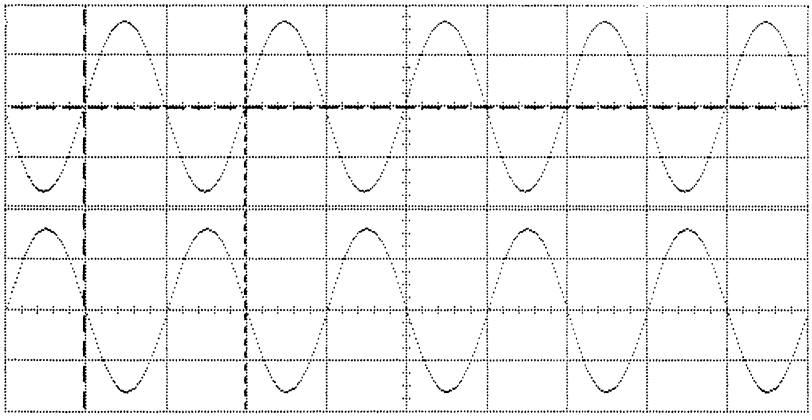
FIGURE 11 - THE OSCILLATIONS ARE DECREASING AND THE BOTTOM WAVEFORM IS STARTING TO APPROACH THE SAME SHAPE AS THE TOP WAVEFORM



-2.50000 usec 0.00000 sec 2.50000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Ch. 2	=	40.00 mvolts / div	Offset	=	-102.0 mvolts
Timebase	=	500 nsec / div	Delay	=	0.00000 sec

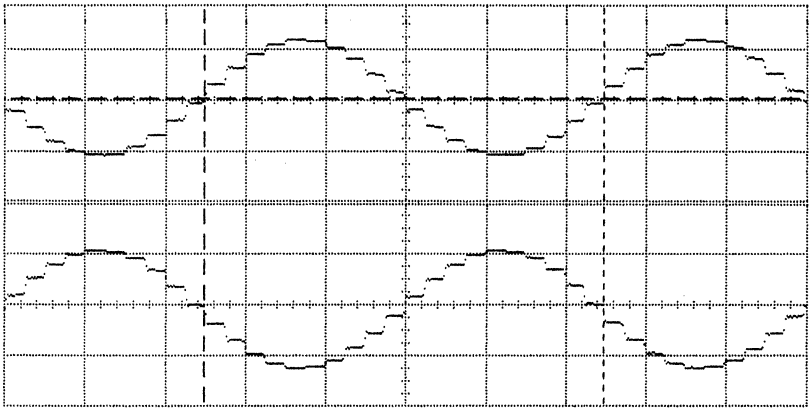
Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels
Chan1 = 0.000 volts
Holdoff = 70.000 nsecs



-2.50000 usec 0.00000 sec 2.50000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Ch. 2	=	40.00 mvolts / div	Offset	=	-102.0 mvolts
Timebase	=	500 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	665.6 mvolts
Rise Time	=	290.790 nsec	Fall Time	=	291.830 nsec
Freq.	=	999.990 KHz	Period	=	1.00001 usec
+ Width	=	500.180 nsec	- Width	=	499.830 nsec
Overshoot	=	0.000 volts	Preshoot	=	0.000 volts

FIGURE12 - OSCILLATION HAS STOPPED AND THE BOTTOM WAVE-FORM IS THE SAME SHAPE AS THE TOP WAVEFORM BUT IS INVERTED



-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	400.0 mvolts / div	Offset	=	-964.0 mvolts
Ch. 2	=	400.0 mvolts / div	Offset	=	-544.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	912.5 mvolts
Rise Time	=	290.470 nsec	Fall Time	=	297.770 nsec
Freq.	=	1.00264 MHz	Period	=	997.370 nsec
+ Width	=	499.250 nsec	- Width	=	498.120 nsec
Overshoot	=	6.249 mvolts	Preshoot	=	6.249 mvolts

Trigger mode: Edge
On Neg. Edge on Chan1
Trigger Levels

Chan1	=	-964.0 mvolts
Holdoff	=	70.000 nsecs

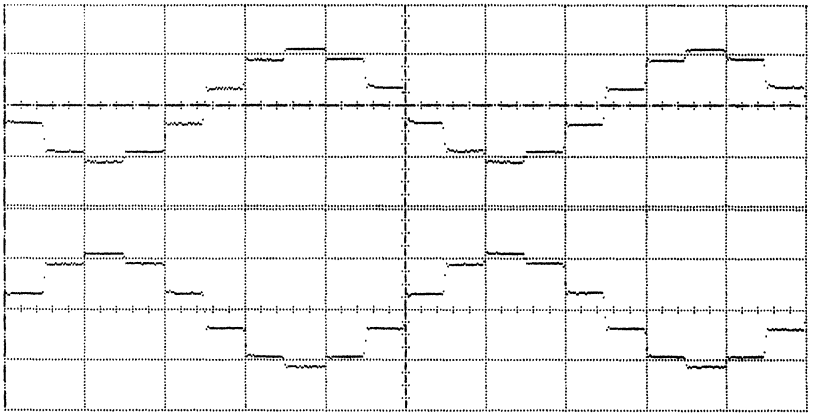
FIGURE 13 - OUTPUT WAVEFORMS FROM "OUT-" AND "OUT+" WITHOUT THE CLOCK DIVIDER BOARD INSERTED AND THE CLOCK JUMPERS CONNECTED AS SHOWN IN THE TOP OF FIGURE 4

STEP 6

This measurement is done without the clock divider board connected and clock jumpers inserted as shown in the top of Figure 4. Again referring to Figures 2 an 4, attach a 50Ω coax cable to the BNC connector marked "OUT-" and another cable to "OUT+". Attach the other end to an oscilliscope set to 50Ω input impedance. The outputs should be the opposite of each other and at approximately a 900mV amplitude. Adjust potentiometer R36 to achieve this level. Do not adjust too far or the signal will start deteriorating. See Figure 13. After completing step 6, remove one end of each "clock jumper" wire and leave the other end soldered to the board.

STEP 7

Insert the clock divider board and connect the shorting jumpers to the posts in the +2 configuration and compare to the waveform in Figure 14.



-1.00000 usec 0.00000 sec 1.00000 usec

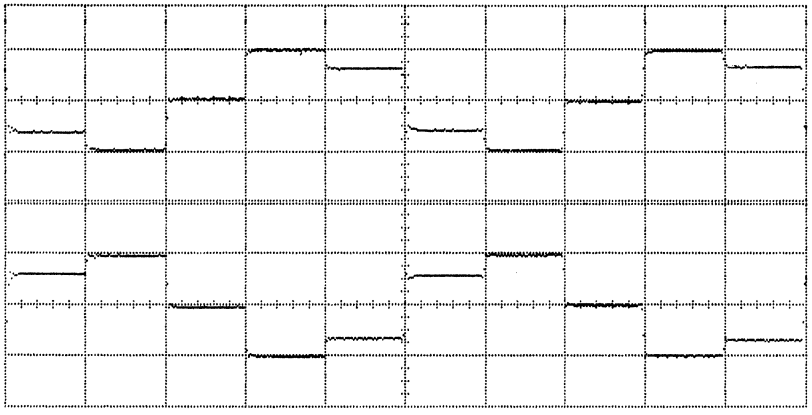
Ch. 1	=	400.0 mvolts / div	Offset	=	-936.0 mvolts
Ch. 2	=	400.0 mvolts / div	Offset	=	-576.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	912.5 mvolts
Rise Time	=	201.240 nsec	Fall Time	=	201.350 nsec
Freq.	=	1.00255 MHz	Period	=	997.460 nsec
+ Width	=	499.050 nsec	- Width	=	498.410 nsec
Overshoot	=	100.0 mvolts	Preshoot	=	100.0 mvolts

Trigger mode: Edge
On Neg. Edge on Chan1
Trigger Levels
Chan1 = -936.0 mvolts
Holdoff = 70.000 nsecs

FIGURE 14 - "OUT-" AND "OUT+" WITH THE CLOCK DIVIDER BOARD INSERTED AND SET AT +2 MODE

STEP 8

Insert the clock divider board and connect the shorting jumpers to the posts in the ÷4 configuration and compare to the waveform in Figure 15.



-1.00000 usec 0.00000 sec 1.00000 usec

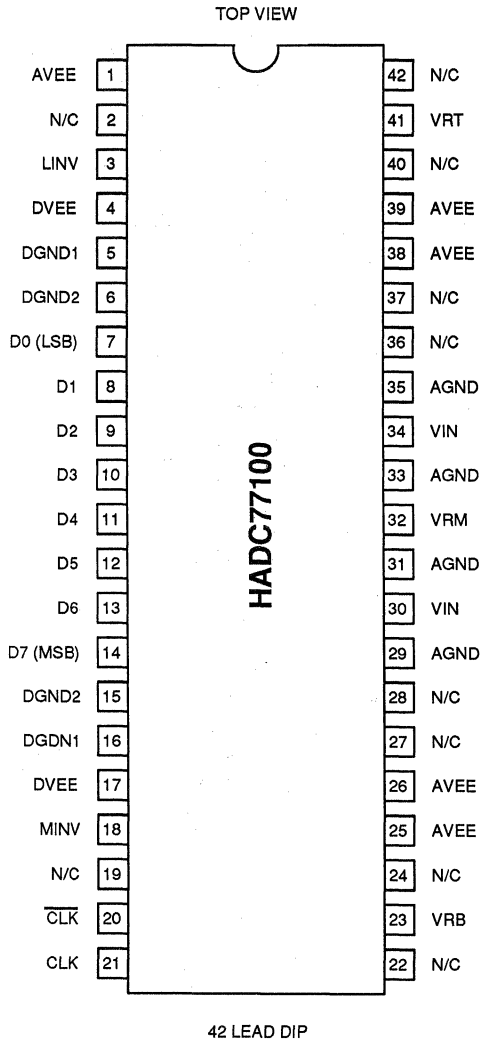
Ch. 1	=	400.0 mvolts / div	Offset	=	-944.0 mvolts
Ch. 2	=	400.0 mvolts / div	Offset	=	-568.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec

Trigger mode: Edge
On Neg. Edge on Chan1
Trigger Levels

Chan1	=	-944.0 mvolts
Holdoff	=	70.000 nsecs

FIGURE 15 - "OUT-" AND "OUT+" WITH ÷4 CLOCK DIVIDER MODE

PIN ASSIGNMENTS HADC77100

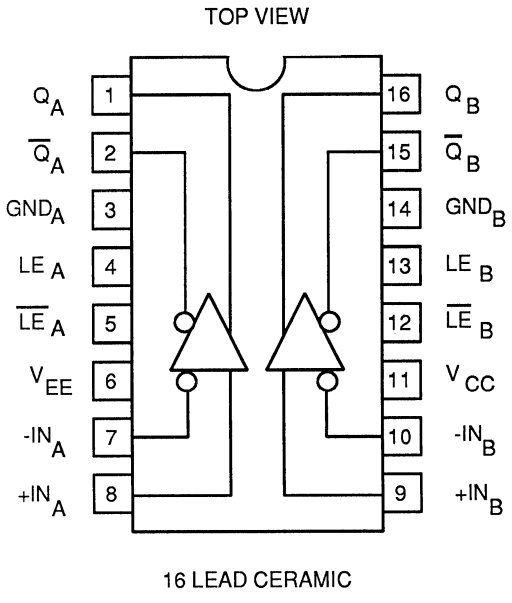


42 LEAD DIP

PIN FUNCTIONS HADC77100

NAME	FUNCTION
AVEE	Negative Analog Supply Nominally -5.2V
LINV	D0 through D6 Output Inversion Control Pin
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
DO	Digital Data Output (LSB)
D1 - D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{\text{CLK}}$	ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRB	Reference Voltage Bottom Nominally -2.0V
AGND	Analog Ground
VIN	Analog Input (can be connected to the input signal or used as Sense)
VRM	Reference Voltage Tap Middle
VIN	Analog Input (can be connected to the input signal or used as Sense)
VRT	Reference Voltage, Top Nominally 0.0V

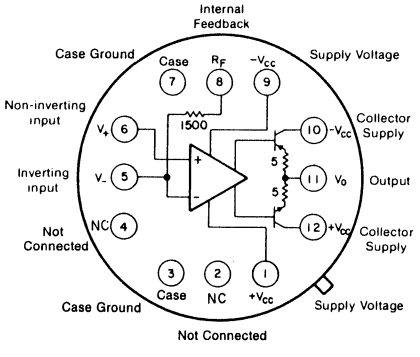
FIGURE 8B
PIN ASSIGNMENTS HCMP96870



PIN FUNCTIONS HCMP96870

NAME	FUNCTION
$\overline{Q}_A$	Output A
Q_A	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Inverted Latch Enable B
$\overline{LE}_B$	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

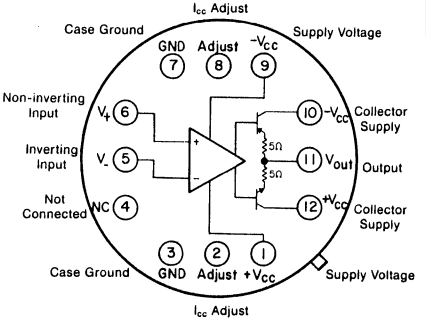
BOTTOM VIEW



Pin 8 provides access to a 1500 ohm (0.1% thin film) feedback resistor. Though not electrically connected to the circuit, the case provides EMI shielding and should be connected to a low impedance signal return.

PIN ASSIGNMENTS
COMLINEAR CLC221

BOTTOM VIEW

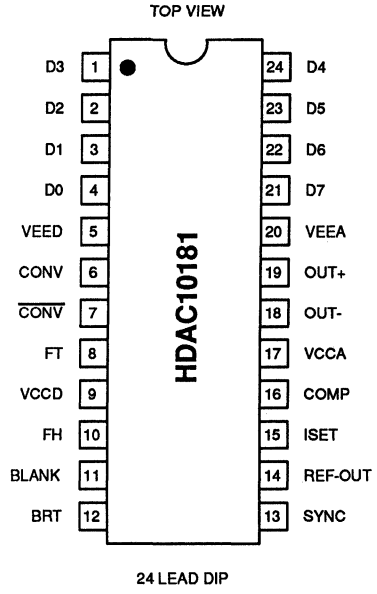


Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

PIN ASSIGNMENTS
COMLINEAR CLC231

8

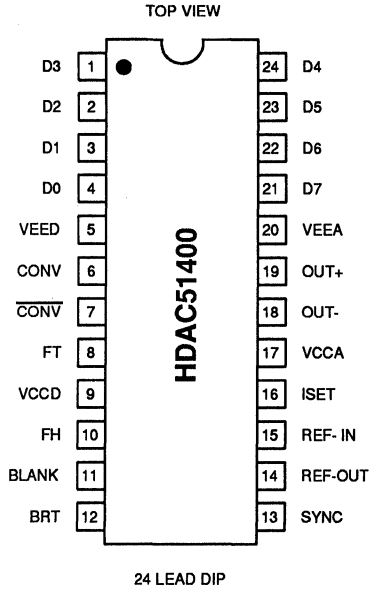
PIN ASSIGNMENTS HDAC10181



PIN FUNCTIONS HDAC10181

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

PIN ASSIGNMENTS HDAC51400



PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
REF-IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

SIGNAL PROCESSING TECHNOLOGY'S PARALLEL ANALOG TO DIGITAL CONVERTERS

by STEVE SOCKOLOV MARKETING MANAGER

GENERAL

The fastest type of analog to digital converter known at this time is the parallel or flash converter. This type of converter (see Figure 1) has one comparator for each possible output code. This results in the fact that there are 2^N or 2^N-1 comparators for an "N"-bit flash converter. The difference between the two numbers of comparators depends on whether or not an overrange bit is included. This can be a very large number of comparators, to fit on a single die, for values of N greater than eight.

Flash converters are now available with up to 10 bits of resolution. There are also products available that are called flash converters, but are actually a variation known as "two-step" flash converters. Almost all data sheets that now claim to have 10- or 11- bit flash converters, and even some lower resolution converters, are not true parallel converters with 2^N-1 comparators. These converters (see Figure 2) go by a variety of names including two-step, sub-ranging, half flash, feed forward and series/parallel converters. "Two-step" or sub-ranging converters require a different system design approach than parallel flash converters and require extra support circuits in many applications. A major advantage of these sub-ranging architectures is that they should cost less than a comparable full parallel type. Disadvantages include the need for a sample and hold (unless it is included on the device) and their problems with dynamic performance over processing and temperature have not yet been solved.

Flash converters are currently available with 4 to 10 bits of resolution with 8 bits being by far the most common configuration. There are several trade-offs that are made as resolution is increased. These are,

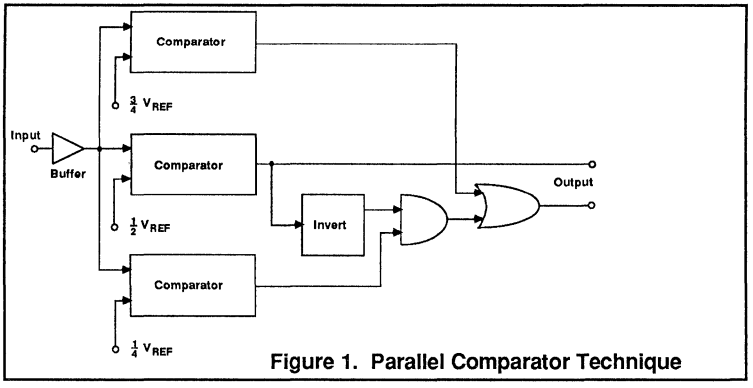


Figure 1. Parallel Comparator Technique

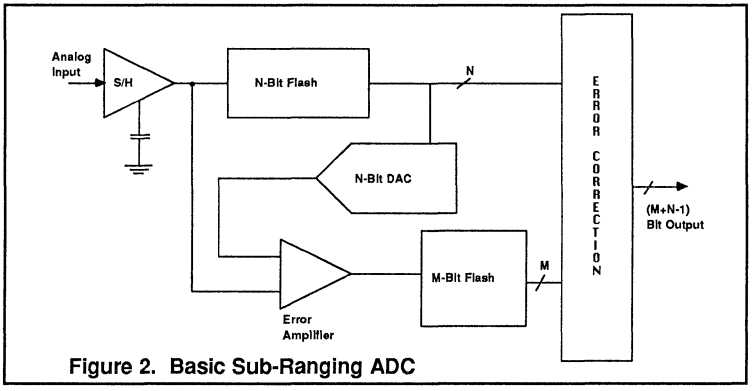


Figure 2. Basic Sub-Ranging ADC

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for a given process, as the resolution is increased and if the basic design is unchanged the speed may decrease slightly, input capacitance will almost double for each bit added, power will go up and cost will increase due to die size and the associated effect on yields. It is for all of these reasons that there are no flashes with greater than 10 bits of resolution available today.

DESCRIPTIONS

Honeywell's 8-bit flash converters, the HADC77100, 77200 and 77300 (see Figures 3A and 3B) have an input structure that improves their performance over previous flash converter designs. This structure is the inclusion of a preamplifier with inputs connected to the resistor ladder and the analog inputs of each of the 256 comparators.

After the comparator outputs (see Figure 4) the structure of the HADC77100 family of converters is similar to many other 8-bit flash converters. They are configured in four columns, each of which functions as a 6-bit converter. The outputs of each column are then logically combined to generate the 8-bit output. Output coding can be controlled by the Most Significant Bit Invert (MINV for bit D7) line and the Least Significant Bits Invert (LINV for bits D0 through D6) line.

Figure 5 shows a macro block diagram of Honeywell's 10-bit high speed flash converter. The analog signal enters the preamplifier/comparator front end and is digitized by the comparators into a "thermometer" code. After the comparators there are 16 blocks of 64 "thermometer" code to Gray code converters. This block also contains new patented circuitry to eliminate metastable states. Gray coding was chosen because it reduces glitches and digital noise caused by switching transients and glitches caused by "OR'ing" more than 1 code. The results are reduced signature effects and improved dynamic performance. Following this first decode are the column latches. After the latches the MSBs and the overrange bits of each of the16 banks are decoded to form the 4 MSBs. In parallel with this, the 6 LSBs from each of the 16 banks are OR'ed to form the 6 LSBs.

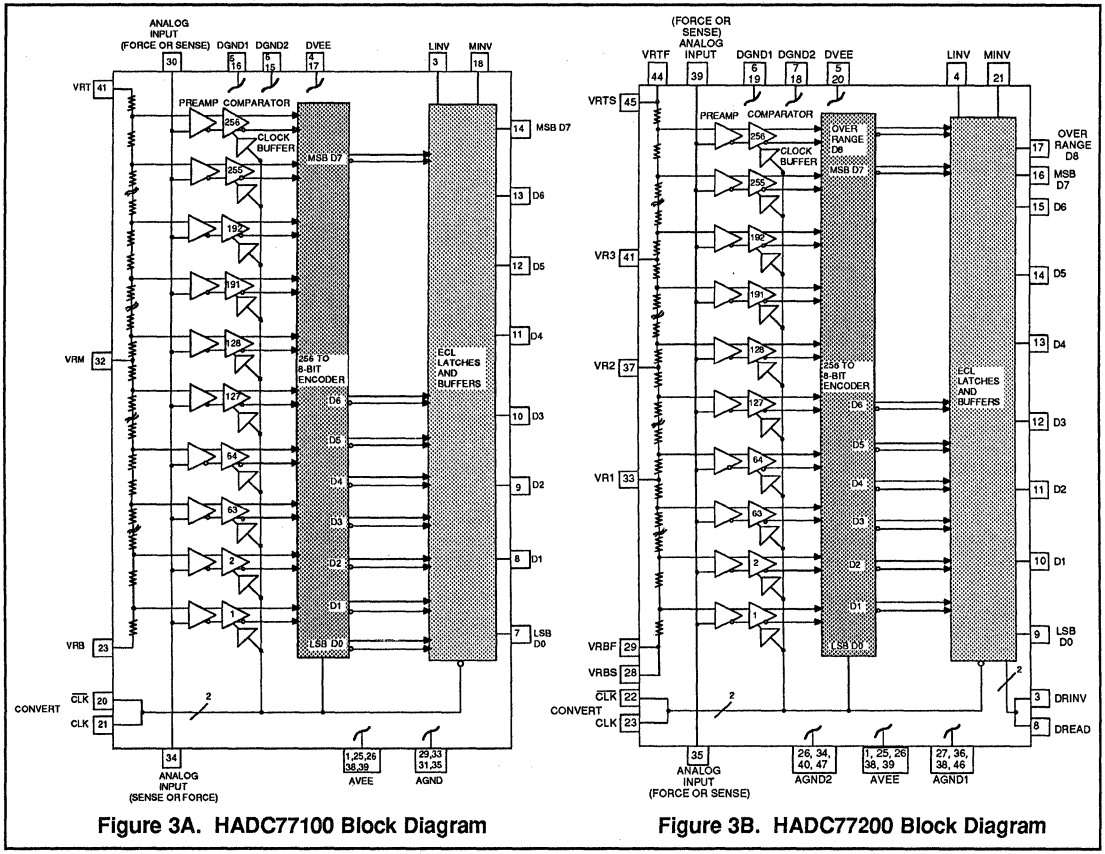


Figure 3A. HADC77100 Block Diagram

Figure 3B. HADC77200 Block Diagram

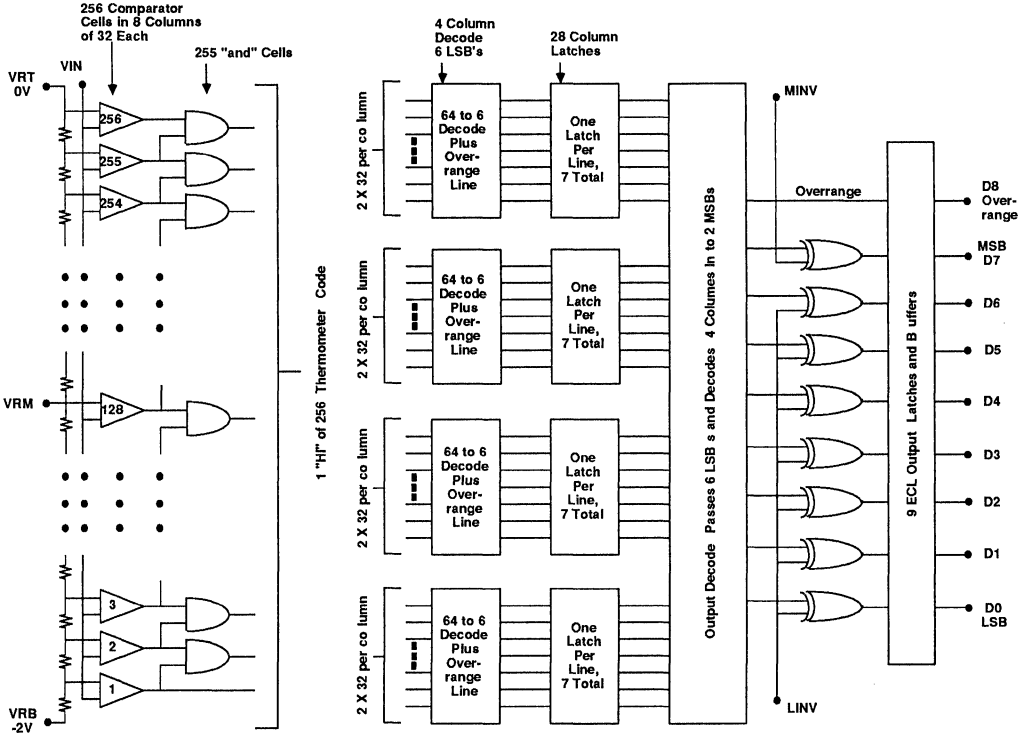


Figure 4. HADC77100 Family Block Diagram

Following this first decode are the column latches. After the latches the MSBs and the overrange bits of each of the 16 banks are decoded to form the 4 MSBs. In parallel with this, the 6 LSBs from each of the 16 banks are ORed to form the 6 LSBs. All coding has been Gray code to this point and in the next block it is decoded to binary. Control bits are available to invert either the MSB and/or the LSBs to generate other common codes such as two's complement or offset binary. The final block contains the output latches and buffers.

INPUT STRUCTURE

There are two inputs to all of Honeywell's flash converters. These inputs are connected to a single point internally so they may be either tied together externally, or used as force and sense lines. Using the force and sense approach will take the effect of the lead inductance out of the input. This would not be much of an advantage at bandwidths below 50 MHz. But it will be useful at higher frequencies. Connected directly to the inputs are the preamplifiers. The purpose of these preamplifiers is to reduce both kickback currents and the possibility of metastable states. These input amplifiers have a very high gain bandwidth product which results in greatly improved dynamic performance (over previous flash converters). Part of this improvement comes by providing gain prior to the comparator increasing its overdrive, thus reducing the chances for metastable states. Following the input to the preamplifiers the entire circuit to the output latches is differential to reduce clock synchronous noise.

Input capacitance is a very critical parameter to the users of high speed ADCs. In the best of cases this capacitance would be both low and constant. The greater the capacitance, the greater the drive requirements of the signal source and if it varies over input voltage, as it does in most semiconductor devices, then the compensation of the driving amplifier must be designed to account for the worst case. When reading input capacitance on data sheets pay

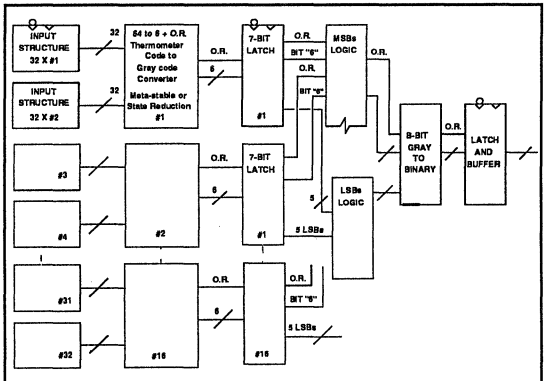


Figure 5. Digital Logic Configuration, 10-Bit Flash ADC

TABLE 1

3-BIT FLASH CONVERTER

LOGIC EQUATION		BINARY	GRAY
$\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+\overline{G}$	=	000	000
$\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+\overline{F}+G$	=	001	001
$\overline{A}+\overline{B}+\overline{C}+\overline{D}+\overline{E}+F+G$	=	010	011
$\overline{A}+\overline{B}+\overline{C}+\overline{D}+E+F+G$	=	011	010
$\overline{A}+B+\overline{C}+D+E+F+G$	=	100	110
$\overline{A}+\overline{B}+C+D+E+F+G$	=	101	100
$\overline{A}+B+C+D+E+F+G$	=	110	101
$A+B+C+D+E+F+G$	=	111	111

attention to the test conditions. Semiconductors have the highest capacitance with the lowest voltage across them. For worst case designs with ECL compatible converters V_{IN} is at 0.0 Volts.

In some cases, especially in testing, the converter is driven from 50 Ohm sources and this can cause a pole to appear at the input caused by the 50 Ohms in series with the input capacitance. Another characteristic of input capacitance is that it can vary with input frequency and/or input voltage. Signal Processing Technology's converter input capacitance varies only a few pico Farads with either frequency or voltage within its specified operating range.

RANDOM ERRORS -- SPARKLE CODES, GLITCHES AND METASTABLE STATES

In an ideal flash converter every comparator will be in a defined logic state (either a "0" or a "1") at the time that the latches are strobed. At the strobe all of the comparators below the input voltage would be "off" and all of the comparators above the input voltage would be "on." This is the "thermometer" code that was previously referred to.

It is possible to strobe the comparators while one of them is in its linear region. This would cause the decode logic to possibly enter either an undefined state or not have time to change states. This could result in the decode logic equation (see Figure 6) such as A+B+C+?+E+F+G for the 3-bit converter shown in this example. Since the logic has been minimized to only implement the set of equations shown in Table 1, the output would be erroneous. This erroneous data is the result of a metastable state.

Another possible decode error that could result is due to differences in propagation delays and offsets of the individual comparators. These differences could result in a comparator output such as A+B+C+D+E+F+G. Again, the decode logic has not been designed to solve this equation and could produce erroneous data. These types of errors are often referred to as sparkle code or glitches.

Both of these error sources may appear to be random and appear as incorrect output data when compared to the analog input. Possibilities of the errors caused by metastable states increase exponentially with increased clock speeds. Sparkle codes, caused by differences in propagation delays and offsets, may appear to be random but are repeatable for given clock frequencies and input conditions. This type of error often appears as a signature error. Signature errors are caused by the way the internal structure is partitioned or layed out. An example would be if the internal structure were partitioned into blocks of eight banks of comparators, then at eighth scale intervals there may be either wider or narrower codes than those that exist at other codes. These signature errors can appear with DC inputs, but are more commonly seen at higher frequencies.

Honeywell has added proprietary logic (patent applied for) after the comparators in the 10-bit flash converter to reduce metastable states, for a given frequency, to the LSB level. The preamplifiers in the HADC77100 family flash converter reduce the metastable error rate by a theoretical factor of six. Signature effects in all Honeywell flash converter designs have also been reduced to a minimum.

DIGITAL I/O AND INTERNAL LOGIC

All digital inputs, outputs, and clock signals are ECL compatible. ECL was chosen for its low switching noise and its fast clock edges. The fast differential clocks reduce aperture width and jitter. The room temperature specifications for all ECL logic levels are the same as Motorola's 10KH, but they have been designed to operate over the full military temperature range of the converter.

Internal logic is fully differential Current Mode Logic. This is a very high speed, low power logic that has proven performance in high speed converters.

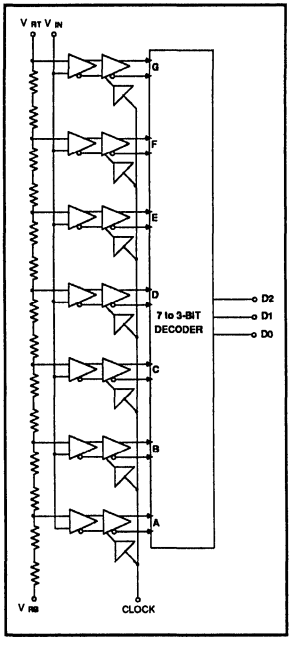
Outputs of the 10-bit flash are specified terminated to 100 Ohms. This will be to save power, since the speed of 50 Ohm termination is not required at its rated speed. Outputs of the 8-bit, 125MHz and above converters are specified with 50 Ohm termination.

CLOCKING

At this time all of Honeywell's flash converters are driven by differential ECL clocks. We realize that slower converters may be in systems that are totally TTL compatible. But in order to assure optimum performance, ECL clocks have been chosen. The relatively slow edges of TTL signals could cause hundreds of picoseconds of aperture jitter, unacceptable performance for high speed systems. Differential clocks also provide better system noise performance.

For Honeywell's flash converters clock duty cycles are designed to be 50% for the highest operating speeds. Duty cycles of 50% were chosen because they are easy to generate and are useful in applications such as ping-ponging. At sample rates below maximum, clock duty cycle is not important to the device operation. What is important at any sample rate is to assure that at least the minimum pulse width is maintained.

Clock inputs were designed to accept differential ECL levels but they may be driven in a variety of different ways. Care must be taken to assure that the method of clock driving is commensurate with the application and temperature range required. For applications where aperture delay is not a critical concern, the clock may be driven single-ended. An ECL signal, or a sine wave with ECL levels may be fed to one of the clock inputs and the other input would be tied to the ECL threshold of approximately -1.3V. The disadvantage of this method is that due to V_{BB} shifts with temperature, the aperture delay will shift 15ps/^{0}C (for the HADC77100) from a typical value of 1.8ns at 25^{0}C. This temperature dependent shift is designed to track MECL 10KH logic and can be driven single-ended without problems when driven from 10KH logic. For aperture delay critical requirements such as when the converter is used in conjunction with a track and hold or when phase information must be maintained, then differential clocking should be used. This will have much better stability (7ps/°C) over temperature.



Tracking of different devices over temperature appears to be very good with almost no difference from device to device in the few HADC77100s that have been measured.

Because the inputs to the internal clock drivers have a gain stage in front of them, signals less than full ECL levels may also be used. Differential signals of greater than ±100mV are adequate.

Figure 6. 3-Bit Parallel Converter Example

SPECIFICATIONS AND TESTING

All data sheet specifications with minimums or maximums will be tested at the temperatures specified unless otherwise noted. Those that have only typical numbers Honeywell intends to characterize, but not test. Honeywell's data sheets also include a Test Level to specify how the devices are tested.

Testing of flash converters at full operating speeds is extremely complicated. Honeywell uses an automated test system to perform all of the production tests on these devices. Characterization is performed using the test equipment shown in Figure 7. Since testing is so complex and costly, the user may wish to consider using Honeywell's evaluation board with bench top test equipment for incoming sample tests.

There are several tests listed in the specifications that may need explanations. It is important to understand that these devices attain new levels of performance,

and Honeywell believes that traditional analog to digital converter specifications such as gain and linearity are not the only specifications needed for high speed system design. These specifications are static and therefore are applicable to input signals that are at or near DC. Perhaps one could test a parameter such as linearity at a given frequency. This can be done using histogram testing. Another test that can be performed is a RMS sine wave curve fit. This is often referred to as "effective bits." This is a dynamic test that measures the sum of several errors and relates them to the fidelity of a sine wave.

OFFSET TESTING

Because these converters have two references, one at the top and the other at the bottom of the ladder, the traditional gain and offset specifications do not apply. Honeywell's specifications contain two offset specifications, one for each end of the ladder. The following is an example of testing for these offsets using an 8-bit converter. Any other flash converter with two reference inputs could be tested similarly using different values. Offsets will be tested by applying V_{REF+} (0.000V for the 8-bit converters) to the input and increasing the positive reference from an arbitrary voltage, say -0.100V, and finding the code transition to full scale. The difference between the voltage at which the transition occurs, plus 1/2 LSB (3.91mV), and 0.000V is the V_{RT} offset. The V_{RB} offset will be determined in a similar manner with an input voltage of -2.000V.

DYNAMIC TESTING

The following are brief explanations of some of the dynamic tests that Honeywell performs when evaluating flash converters. For more complete explanations consult Hewlett Packard's product note 5180A-2 "Dynamic Testing of A to D Converters."

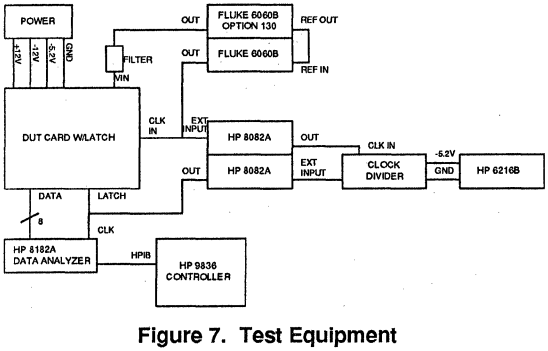


Figure 7. Test Equipment

HISTOGRAM TESTING:
In this test a full scale sine wave is input to the ADC and many samples (perhaps 100,000) are taken. Then the number of times each code appears is plotted. Since a sine wave is slowest at its extremes the number of codes for zero scale and full scale are the greatest. This should make a graph with a flattened "U" shape. Honeywell's data does not exhibit this shape because the data has been normalized. This test can be conducted at different input frequencies to show response over the full dynamic range of the converter. This test can give data on differential linearity, integral linearity, mean differential linearity, RMS differential, and on the number of missing codes. The mean differential linearity is the sum of all of the differential errors. Ideally, it should be zero. Most flash converters come very close to this value at DC because this parameter measures the magnitude of the sum of superposition errors. As the analog input slew rate increases this error also increases. This is probably due to dynamic currents in the ladder.

Histogram testing does have one weakness. It measures only the number of occurances of each code and not the order of them. For this reason, it is possible to have random errors or missing codes and because the test averages many data points a code may appear wider or narrower than it actually is.

An alternative to sine wave testing is triangle wave testing. This signal would give a very good indication of the performance of the ADC because every comparator would be tested at maximum slew rate. The difficulty with this type of test is generating a triangle wave with a very high frequency.

Square wave testing can also be used to evaluate flash converters. This test measures step response. Evaluation with square waves should be performed on flash converters whenever their input is being driven from either a multiplexer, sample and hold or will, by the nature of the input signal, be required to have good step response.

RMS DIFFERENTIAL LINEARITY ERROR:
The square root of the sum of the squares of the differential non-linearities. This error term can be an indication of the signal-to-noise ratio of the converter. The device numbered 153 shows a part that has .2 LSB of RMS DL at 10MHz and 47.5dB of SNR at the same frequency. Another device measured .28 LSB and 45.68dB at the same frequency. However, this relationship only holds true for devices that have randomly distributed DNL errors. Those with large spikes may have SNRs that are so poor they are unmeasurable.

SINE WAVE CURVE FIT (Effective Bits):
Testing flash ADCs for sine wave curve fit provides a quantitative value that represents the RMS sum of four error sources. These error sources are DNL, IL, aperture uncertainty and noise. This value could be useful in predicting over-all system performance. To adequately test performance, the converter should be tested with sample and input frequencies selected to change the output at least 1 LSB every clock cycle. This yields much more useful data about the actual performance of the converter than testing with a much lower beat frequency.

Many articles give a formula for calculating effective bits from the Total Error. This formula is given as:

Total Error (dB) =
1.8 + 6.02N (Eff. Bits)

This formula will only be true in cases where the signal is a full scale sine wave. Other literature may use SNR in this formula.

To select the beat frequency for testing the converter at its full sampling frequency with the input at the Nyquist frequency, use the following formula:

$$\frac{f_S}{2^N} = \pi \ f_B$$

Where f_B = Beat frequency,
f_S = Sample frequency,
N = Number of bits.

Using the above sampling technique will exercise all digital outputs and assure one LSB code change for each clock cycle. If the application requires that the analog input be able to slew at maximum slew rate for any input, then testing using a triangle wave may be more appropriate.

FFT TESTING:
Discrete Fourier Transform testing can be used to evaluate the dynamic performance of an ADC for Signal-to-Noise Ratio (SNR) and Harmonic distortion. Honeywell defines Total Harmonic Distortion (THD) as the sum of the second through the ninth (though it is usually dominated by 2nd and 3rd) harmonics, and SNR is any remaining signal. The sum of these two parameters is the Total Dynamic Error and it is this value that can be used to calculate sine wave curve fit. These parameters are excellent indicators of flash converter performance. Signal-to-Noise Ratio is one test that needs to be carefully watched because if there are any glitches in the data the repeatability of the test is poor. This test can be used with confidence at lower analog input bandwidths where there is a low probability of glitches but it must be used carefully when near the limit of flash converter performance.

FILTERS

Most dynamic ADC testing requires sine waves for inputs and derive data based on that sine wave being ideal. To assure that the test signal is accurate, filters may be required to increase the purity of the input signal. Another method of testing is to eliminate the filters. This is done by measuring the harmonic contents of the input signal and digitally subtracting them from the output data.

APERTURE

As in any sampled data system the aperture jitter and width affect the accuracy of the system. If the aperture jitter time is converted to an amplitude uncertainty for any input where the voltage is changing, then the magnitude of this change for a sine wave can be calculated for time or voltage by the equation:

$$\frac{dV}{V} = 2\pi f \quad t_a$$

By calculating the aperture jitter for a given system accuracy and comparing it to the aperture time of the flash converter, the need for a track and hold may be determined. The graph in Figure 8 summarizes required aperture jitter time for different resolution high

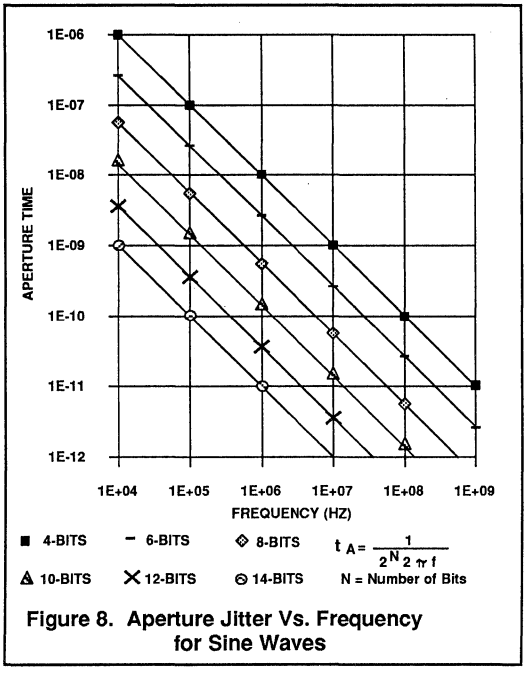


Figure 8. Aperture Jitter Vs. Frequency for Sine Waves

speed converters, for sinusoidal frequencies. The aperture width is an integration period and the signal will be integrated over its period. This would only cause a filtering effect, assuming that the aperture itself is well behaved.

An example to determine the maximum aperture jitter using an 8-bit flash converter: If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from the graph in Figure 8, it can be determined that to assure less than 8 bits of error due to aperture jitter alone, the ADC must have an aperture jitter of less than 70ps. Most data sheets do not state aperture jitter, so to be safe the designer may wish to use a sample and hold. It may be difficult to find sample and holds that sample that fast. Since aperture times for ADCs are usually not specified, though for flash converters they can be very good, it is possible to add a sample and hold to the circuit and decrease the system performance.

Aperture width and jitter are very difficult to measure because of the extremely small time periods that are in the range of picoseconds to tens of picoseconds. Another problem is that they are not absolute numbers, but are random and are usually calculated based on statistical data. However, these values are needed to make intelligent design decisions, especially in sample and hold selection. These values are on the Honeywell SPT flash converter data sheets as typical values that have been based on both computer design simulations and verified by characterization of samples. Aperture delay is the time from the clock edge to the time that the sample is taken. Aperture jitter is the time variation in the point that the sample is taken.

Aperture delay is the delay from the time the clock is strobed until the sample is taken. Figure 9 shows a circuit based on driving both the clock input and the analog input with the same sine wave. This technique can accurately and easily measure aperture delay. It can also be used in a system to align several different channels in time. When using this technique be sure to use differential signals to the clock or errors may result.

Example using the HADC77100:

$$V_{in} = V_{offset} + A_o \sin wt$$

Choose $f_{in} = 30\,MHz$

$A_o = .75$

$V_{offset} = -1.25V$

Note that these voltage values will work well for any ECL flash converter with an input that swings below ground.

At ECL logic threshold, $V_1 = -1.3V$,

Measure V_2 and calculate T_2.

Where $$T_1 = \frac{\arcsin((V_1 - V_{offset})/A_o)}{\omega}$$

For $V_{rb} = -2.00V$ and $V_{rt} = 0.0V$,

$V_2 = 2.0\,((Code\ No./256)-1)$

And $T_2 = 1/w \arcsin((V_2 - V_{offset})/A_o)$

Aperture delay = $T_2 - T_1$

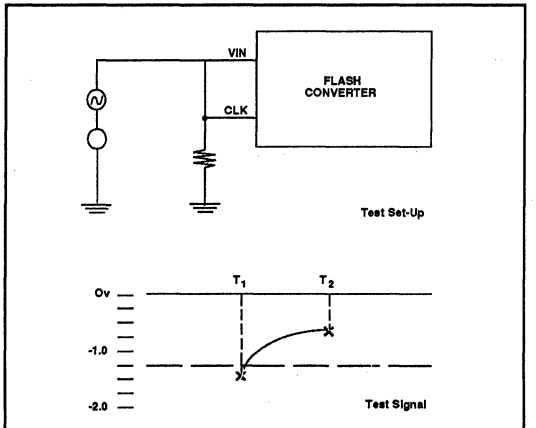


Figure 9. Aperture Delay Measurement

LINEARITY

Honeywell specifies both integral and differential linearities of the flash converters. Differential nonlinearity is specified from an ideal 1 LSB code width. Therefore, for a device that is specified ±1/2 LSB every code will have widths between 1/2 LSB and 1 l/2 LSBs wide. A device specified ±3/4 LSB could have code widths from 1/4 LSB to l 3/4 LSBs wide. To have missing codes the device would need to be specified -1 LSB or greater.

Honeywell has demonstrated the capability of producing flash converters with differential linearity in excess of 9 bits without any type of trimming. The 10-bit converter is capable of being trimmed because a 10-bit converter has four times the number of compar-ators as an 8-bit flash converter. An offset error of only 2mV in any single comparator could destroy the linearity of

the converter. Trimming is in the form of four aluminum links that can be laser cut to select different resistors that will alter the comparator offsets. This method of trimming was chosen because no active or current carrying structure is altered. It is either in the circuit or it is completely deleted. This assures that there is no affect on either long-term stability, reliability, or on temperature performance.

Absolute linearity of converters can be adjusted by the use of external taps. The 10-bit converter can be adjusted by the use of seven external taps, and for the 8-bit converters either one or three taps are available (see Figure 7). These taps can be used to cancel the effect of the bias currents of each preamplifier (see Figure 10). If each wafer had exactly the same betas and absolute bias current, the ladder could be designed to compensate for the bias currents. This would imply that bias currents on each preamplifier could be the same, not only from device to device, but also from chip to chip. Honeywell's designs correct for these first order effects. These effects would appear as bows (see Figures 11A & 11B) in the linearity curve caused by bias currents. Honeywell's correction works very well so that at the 8-bit level this typical center tap offset is less than a millivolt. So taps are not required to maintain 8-bit linearity at room temperature.

External taps, for the 8-bit converters have half or quarter scale connections and the 10-bit converter has taps placed at eighth scale intervals to allow the user to force the ladder. Externally altering the ladder's linearity, if required, is low in cost and can also be used to change the dynamic range of the converter. Honeywell recommends the use of the PMI OP9 or OP11 quad op amps to force the ladder. These op amps have the required low offset voltage and drift.

The dynamic range of the HADC77200 can be increased by using external ladder taps to bend the ladder and create a piecewise approximation of a curve (Figure 12). There are two primary considerations for this application. The first is to assure that the low end of the scale has no missing codes due to comparator offsets. The second consideration is to assure the maximum ladder current specification is not exceeded.

In normal applications the ladder is referenced to a -2.0 Volt full scale. This results in an LSB of 7.8mV. Therefore a part that is ±1/2 LSB linear will have comparator offsets of less than half this value or 4mV. The 100 Ohm ladder will have 20mA through it, which is close to its maximum rated current of 25mA.

If a device was to be screened to be ±1/4 LSB then a 2mV LSB would be possible for the linearity point of view.

So lets start with a 2mV LSB and geometrically progress, doubling the LSB weight at a quarter, half and three quarters scales, the points available on the HADC77200. This would result in --128mV, -384mV and -896mV taps respectively. Full scale would be at --1.920V. Current in the ladder can now be calculated to be (1920-896mV)/25 Ohms = 41mA. This does exceed the maximum ladder current at 25 mA. But if the device is operated at room temperature there should be little effect on the devices life. Starting with a 39% lower LSB weight will soohe power problem but initial accuracy would not be good enough to guarantee no missing codes.

The above application has the ability to resolve 2mV out of a possible 1960mV or 59.8dB of dynamic range.

If the 25mA specification for the ladder is not to be exceeded then the weight of an LSB cannot exceed 9.8mV. Because of comparator offsets in our process an LSB should not be less than 2mV. A geometric progression where each LSB value changes at the quarter scale points by a factor of 1.7 times the previous LSB value could be used. The results would be within the above constraints of an LSB being between 2mV and 9.8mV. The taps would then be at -128mV, -345.6mV, -715.5mV and full scale would be at -1.3444V. Dynamic range would be 56.6dB.

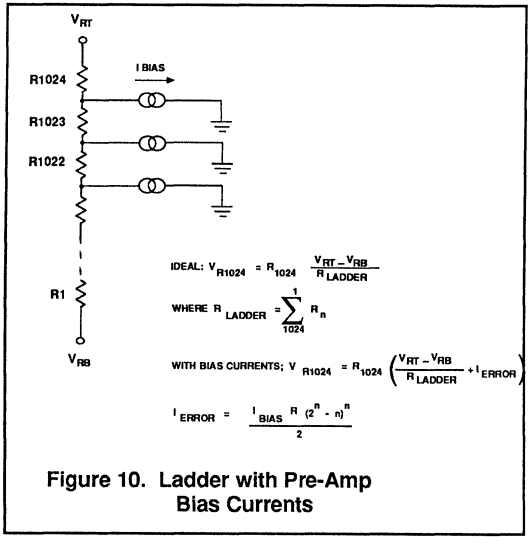


Figure 10. Ladder with Pre-Amp Bias Currents

The original assumption was that parts could be screened to ±1/4 LSB. Now that the LSB is designed to be 2mV and this is for the first 64 codes only, screening could be for the first 64 codes to ±1/4 LSB and the remaining codes to ±1/2 LSB. This may help yields and keep the cost of this screened device lower than screening all codes to a tightened specification.

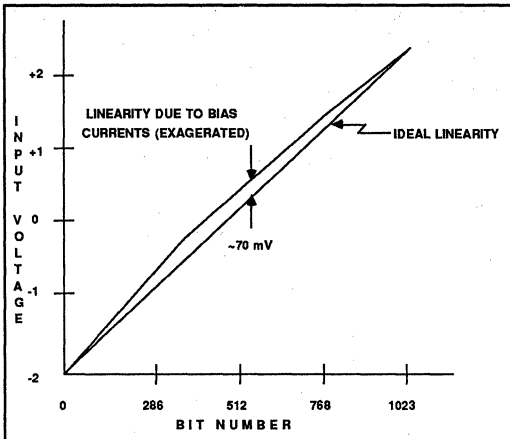
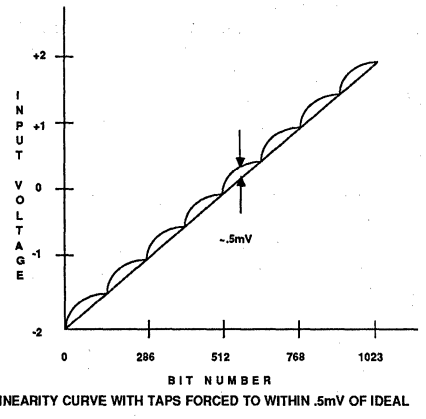


Figure 11A. Ladder Bow 10-Bit Flash ADC



LINEARITY CURVE WITH TAPS FORCED TO WITHIN .5mV OF IDEAL

Figure 11B. Corrected Ladder 10-Bit Flash ADC

The coding of the flash converter is such that Vrt is full scale. It may therefore be easier to start with the 2mV step in the portion of the ladder between Vrb and Vr1. The concept is the same only the taps would be switched.

Because of their very low impedance the reference ladders of flash converters have very high bandwidths. This can be used to dynamically scale the input at very high switching speeds. There is a penalty paid in the SNR and accuracy, but this may be less than that of using a programmable gain amplifier. It is not recommended to go below 500mV full scale range. This will give a range changing ability of 4 to 1 when a -2.0V reference is used.

SUMMARY OF RESULTS

Vrt	0.0	0.0	mV
Vr3	128	128	mV
Vr2	384	345.6	mV
Vr1	896	715.5	mV
Vrb	1920	1344.4	mV
LSB1	2.0	2.00	mV
LSB2	4.0	3.4	mV
LSB3	8.0	5.78	mV
LSB4	16.0	9.83	mV
Dyn Range	59.8	56.6	dB
Max Current	40	25	mA

INCREASING DYNAMIC RANGE

The dynamic range of a system can be increased by stacking ADCs in groups of two or four. Prior to the HADC77100, this was a very difficult task due to two sources of error. The first error source was the static errors of the ADCs with their linearity equal to their number of bits yields greater resolution, but there is still only the accuracy of the original converters plus other errors due to offsets and differences in gain. The accuracy of the ADCs should be at least 9 bits accurate to form a 9-bit accurate 9-bit system. The second error source was due to dynamic currents flowing from the input of one converter and perturbating the input of the other device(s).

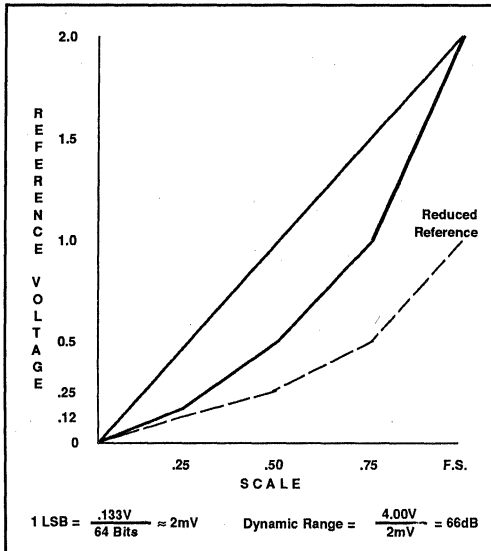


Figure 12. Using Ladder Taps to Extend Dynamic Range

Figure 13 shows an example of two 2-bit ADCs connected to form a 3-bit ADC. This example does not show the logic required to change the output code from all ones to all zeros when the overrange bit goes high. An alternative method of implementing this data conversion is to connect the overrange bit (NOTE: OVR goes True if V_{in} is greater than V_{rt} minus the offsets) to the MINV and LINV bits of each converter. The individual bits can then be wire ORed together and no additional logic is required. The delay of 6ns from INV to data out must be taken into account when setting up the timing for this method. Implementing this circuit with N-bits is identical to the 3-bit example. This stacking of ADCs has no adverse affect on the data throughput; only data output delay is affected. This method of combining ADCs does increase the input capacitance and this must be accounted for in selecting the input amplifier.

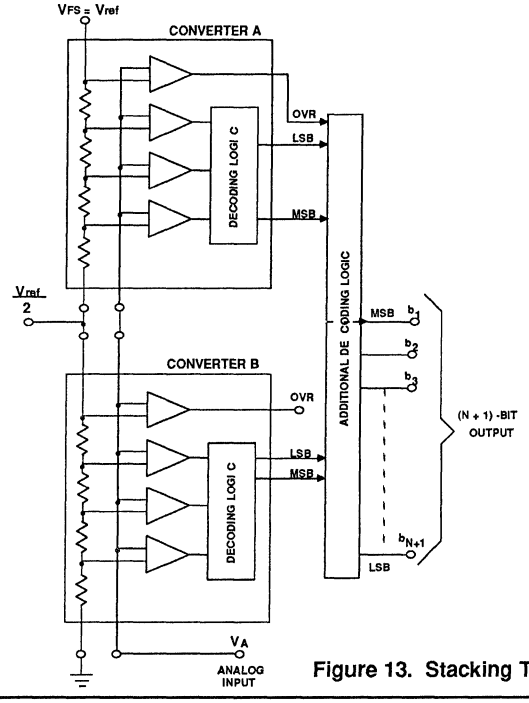
Stacking four ADCs is also possible. In this circuit, logic would have to be implemented to control the data from the overrange bits to the outputs. This circuit may have an additional clock delay to the output.

SPT can custom manufacture any of the HADC77100 family for use in stacked applications. These ADCs would then have the correct logic coding at the outputs so that additional logic and their associated delays would not be present.

INCREASING SAMPLE RATE

The sample rate of a system can often be increased by combining two flash ADCs with their clocks connected out of phase (this is known as ping-ponging) as shown in Figure 14. This technique works especially well with the HADC77100 because of several of its performance parameters. First, the greatly reduced kick-back allows both converters to be driven from the same buffer or amplifier without one converter affecting the other. This eliminates any problems that may arise from different frequency responses of separate amplifiers. Other advantages are that the excellent linearity of the HADC77100 or HADC77200 will enable the design of a true 8-bit system with sample rates of over 250MHz. The data would then be available on two separate busses, a useful feature for data rates in excess of 100MHz. By using the HADC77200 data could be easily clocked into memory or onto the data bus by using the Data Ready output.

The best advantage to using Honeywell flash converters in these applications is that they only require a single clock that has an ideal 50% duty cycle. This eases design by eliminating the need for delay lines in generating the timing signals.



OVR "A"	MSB "A"	LSB "A"	VOLTS
0	0	0	-2.00
0	0	1	-1.75
0	1	0	-1.50
0	1	1	-1.25
1	0	0	>-1.00

OVR "B"	MSB "B"	LSB "B"	VOLTS
0	0	0	-1.00
0	0	1	-.75
0	1	0	-.50
0	1	1	-.25
1	0	0	>0.0

Figure 13. Stacking Two ADC's to Double Dynamic Range

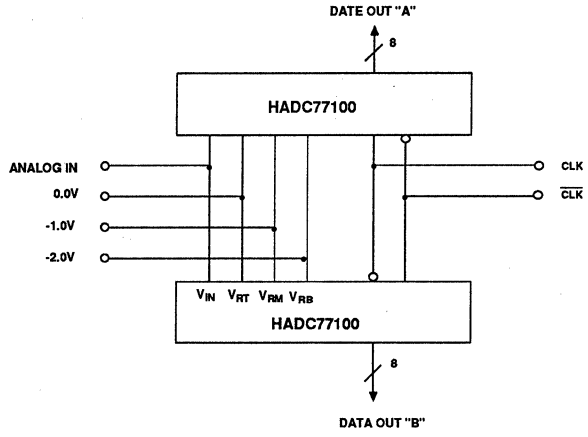


Figure 14. Ping Pong 2 ADC's for 2X Sample Rate

EB101 EVALUATION BOARD 8-BIT, 150 MSPS FLASH A/D CONVERTER AND 8-BIT, 165 TO 400 MWPS RASTER D/A CONVERTER WITH REFERENCE

by Tom DeLurio Senior Applications Engineer

FEATURES

- **150 MSPS MINIMUM CONVERSION RATE**
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- ECL clock produced from any signal generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB101 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77200A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

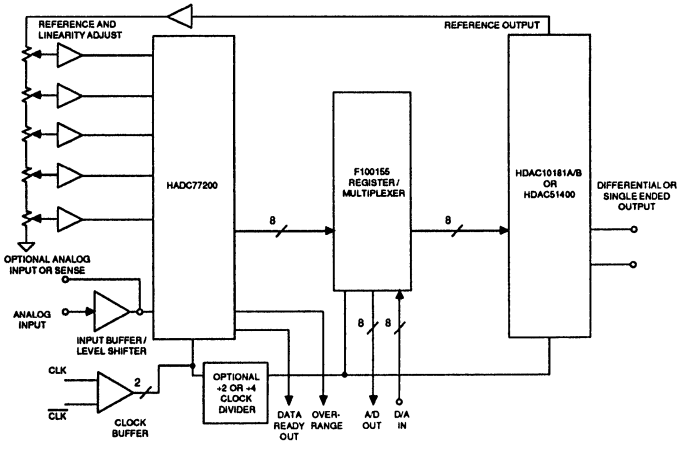
The HADC77200A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77200 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed dual differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB101, with nominal power dissipation of less than 11 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

BLOCK DIAGRAM



8

GENERAL INFORMATION

The EB101 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of Honeywell's HADC77200 8-bit A/D converter, HDAC-10181/54100 8-bit D/A converters and HCMP96870 dual comparator. The board contains circuitry for buffering the input signals, generating reference voltages, dividing the DAC and multiplexer clocks, routing input / output data, and generating ECL level differential clock signals from any signal generator. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments. The board requires -5.2, +5 and ±12 to ±15 Volt supplies.

The EB101 evaluation board consists of seven functional sections that include an analog input buffer, A/D converter, input/output multiplexer and data latches, D/A converter, reference voltage generator, ECL clock generator, and ECL clock divider. The analog and digital grounds are separated on the board for better system grounding characteristics.

There are numerous jumper options available to switch sections in or out of the system to suit individual needs. The clock divider circuitry is on a separate board that plugs into the main board to provide divide by 2 or 4 for the multiplexer and DAC. The jumper options will be discussed in more detail in the following sections. In addition, 90MHz low pass input and output filters are on board.

ON BOARD ANALOG INPUT BUFFER

This section consists of a 90MHz low pass filter, HA2539 high frequency op-amp, and a 2N5836 rf transistor. The input impedance is 50Ω and the gain is set at 2X so that a 1 Volt input can be applied. Compensation components are provided and can be adjusted for the desired frequency range needed. The compensation is factory adjusted for 50MHz bandwidth operation. The bandwidth of the buffer amplifier can be increased by decreasing the gain to 1X by changing the 1.5kΩ feedback resistor to 750Ω. The BNC connector shown in the schematics and layout near the output of the buffer can be used for monitoring the buffer output and input to the HADC77200. The BNC should be connected to a 50Ω terminated oscilliscope and will provide a 10X attenuated signal.

The positive input to the HA2539 is tied to an offset adjust to center the input signal to the HADC77200 around -1V , which is needed if a $2V_{p-p}$ input signal is applied. The input buffer can be bypassed by removing the 6.8Ω resistor at the emitter of the 2N5836 and the 450Ω resistor between the BNC connector and the HADC77200. Bypass the 450Ω resistor with a jumper wire and the HADC77200 can now be driven directly. The input impedance is 4KΩ in parallel with a 56pF distributed capacitance.

OPTIONAL ANALOG INPUT BUFFER BOARD - EB102

An alternate and higher performance input buffer is available as an option and sold separately. The EB102 is intended for users operating at the top end of the input bandwidth range of the HADC77200. The reason for a separate board is that the amplifiers utilized are quite a bit more expensive then the "on-board" buffer. But, with the added expense, increased input bandwidth with less harmonic distortion is realized.

There are two versions of the EB102 buffer board, one with a wideband op-amp (CLC221) and one with a wideband buffer amplifier (CLC231). Both versions are identical but are jumpered to provide for the different amplifier pinouts (See Figure 1A). The CLC221 version has the advantage of being configured up to a gain of 50 as required, and has slightly better harmonic distortion specifications. The CLC231 version has the advantage of a much higher output drive current and better settling time.

The Following table shows a breakdown of some of the more important specifications:

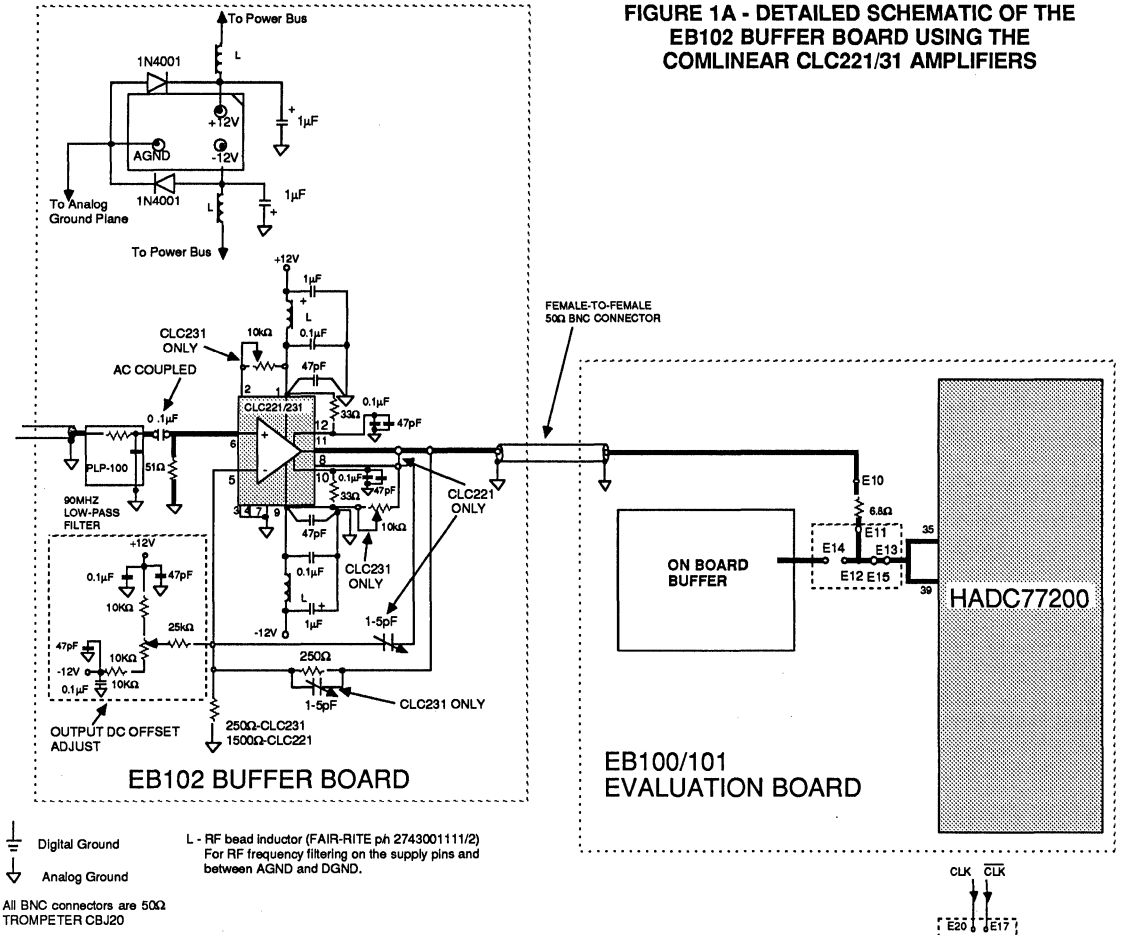
TABLE 1 - COMPARISON OF COMLINEAR CLC221/31 AMPLIFIERS

SPECIFICATION	CLC221	CLC231
Gain Range	±1 to 50	±1 to 5
Output (V, mA)	±12,500	±11,100
Slew Rate (V/µsec)	6500	3000
-3dB Bandwidth (Av=2)	275MHz	165MHz
Settling Time (nsec, %)	15, 0.1 18, 0.02	12, 0.1 15, 0.05
Harmonic(dBc) Second Distortion Third	-58 -62	-55 -59

100K ECL CLOCK GENERATOR

The ECL clock section consists of an HCMP96870 dual comparator, duty cycle and hysteresis adjust, F100131 triple D flip-flop and several jumper options. Any type high frequency signal generator can be connected to the BNC input to the comparators. Both inputs to the dual comparators are connected to the BNC. There are four outputs which generate differential 100K ECL clock signals. One set goes directly to the HADC77200 while the other two can go to the F100155 multiplexers and HDAC10181/51400 or to the clock divider circuitry.

FIGURE 1A - DETAILED SCHEMATIC OF THE EB102 BUFFER BOARD USING THE COMLINEAR CLC221/31 AMPLIFIERS



The threshold input to the HCMP96870 comparators are connected together to a pot to adjust the duty cycle of the clock. The latch enable pins are also connected together to a pot to adjust hysteresis.

100K ECL CLOCK DIVIDER

The clock divider section is shown below in Figure 1B and consists of a triple D type flip-flop, which if jumpered as shown, will provide divided down clock outputs. The clock divider can be bypassed to provide a full frequency clock. The divider is provided to make it easier to monitor the HADC77200 output with a low frequency logic analyzer and to provide the DAC with a reduced sampling rate. When switching between divide by 2 or 4, the unused outputs "Q" and "$\overline{Q}$" must be terminated. The board is initially set in the divide by 4 mode. Furthermore, the jumpers on the clock lines to the multiplexer and DAC must be removed.

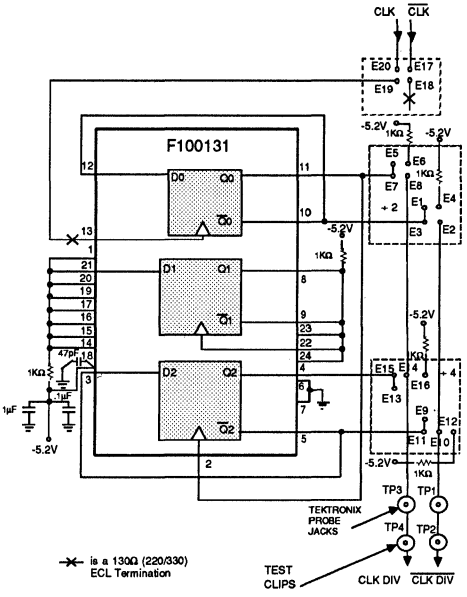


FIGURE 1B - 100K ECL CLOCK DIVIDER

REFERENCE VOLTAGE GENERATOR

The reference voltage for the HADC77200 and HDAC-10181/51400 is internally generated by the D/A converter voltage reference of approximately 1.2Volts. The A/D converter's 2Volt reference, 3 volltage midtaps and ground are controlled by two PMI quad op-amps (OP-11). The magnitude of each setting is further adjusted with potentiometer R25, R26, R32, R37, and R38 as shown in the detailed schematic and board layout.

INPUT/OUTPUT REGISTER AND MULTIPLEXER

The multiplexer section consists of two F100155 which select between external 8-bit digital data from the 64-pin DIN connector or data from the output of the HADC-77200. The choice is controlled by tying the SELECT pins to either an ECL high for external data or an ECL low for HADC77200 data. This data is then fed to the HDAC10181/51400 on the "Q" outputs of the F100155 and the "Q" outputs are tied to the external connector.

A/D CONVERTER SECTION

Both input pins to the HADC77200 are tied together to be either fed by the input buffer or by an external source. The MINV and LINV inputs are left open and tied internally to an ECL low. Diodes are provided to tie them high and change the output logic. The connection choices for determining the output logic are in Table 2.

D/A CONVERTER SECTION

The D/A converter section contains jumpers to use either the HDAC10181 or HDAC51400. The primary difference in the two parts is the reference voltage connections. These differences are shown in the detailed schematic in Figure 2. All EB100 boards and jumpers will be connected for the HDAC10181A part. If an HDAC51400 is indicated when the board is ordered (See last page), the board jumpers must be configured as shown in Figure 4A and 4B by the user.

The output current magnitude for the HDAC10181/51400 is controlled by a potentiometer (R36) through the DAC's Iset control pin. In addition, two 90 MHz low pass filters are provided at both out- and out+ output pins as well as 50Ω terminating resistors. The terminating resistors can be changed to 75Ω if desired. Keep in mind that the transmission line must be terminated at the receiving end with the same value resistor. The video and feedthrough controls are routed to the 64-pin DIN connector and are normally disabled.

TABLE 2 - OUTPUT LOGIC CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
VIN .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: VIH, VOH
0: VIL, VOL

TABLE 2A - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO.	FUNCTION
R26	Pot for adjusting gain to produce a 2V reference voltage for the VRB pin on the HADC77200 from the1.2V reference voltage supplied by the HDAC10181/51400.
R25/ 37/38	Pots for setting the linearity adjustments at the comparator reference ladder on the HADC77200.
R32	Pot for setting the top point (VRT) on the reference voltage ladder. Nominally set at 50mV below AGND.
R36	Pot for adjusting output current drive from the HDAC10181/51400 (See data sheets). Vout+=25.6(digital code X Iset)/RL
R5	Pot for setting the HCMP96870 comparator threshold voltage to adjust the ECL clock duty cycle.
R4	Pot for adjusting comparator hysteresis.
R23	Pot for adjusting up to a 2V offset voltage at the buffer output for driving the HADC77200.
R22	Pot for adjusting compensation and bandwidth for the buffer circuitry. This has been set for maximum bandwidth by turning to the full counterclockwise range. The frequency range can be decreased by adjusting the potentiometer clockwise.
C25	"Lead" Capacitor for changing the damping factor of the input buffer, used in conjunction with Pot R22. This has been set for a flat response.

POWER SUPPLY CONNECTIONS

Power to the EB101 is supplied through a six pin Molex type connector. The supply lines are color coded as shown in Figure1C. Connect the wire end of the power supply harness to power supplies as shown by Figure 1C and the silk screen near the mating connector on the PC board itself. The power harness is attached to the board with the bevelled edges and hollow connector alligned to the mating connector.

The power requirements for the EB101 at different supplies and with or without the clock divider board is shown in Table 3. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

TABLE 3 - POWER DISSIPATION

EB100 WITH CLOCK DIVIDER, ±15V			
Voltage	Current	Power	
+15V	.145A	2.175W	
-15V	.148A	2.220W	
+5V	.006A	0.030W	
-5.2V	1.65A	8.580W	
		13.005W	
EB100 W/O CLOCK DIVIDER, ±12V			
Voltage	Current	Power	
+12V	.119A	1.428W	
-12V	.123A	1.476W	
+5V	.006A	0.030W	
-5.2V	1.49A	7.748W	
		10.682W	

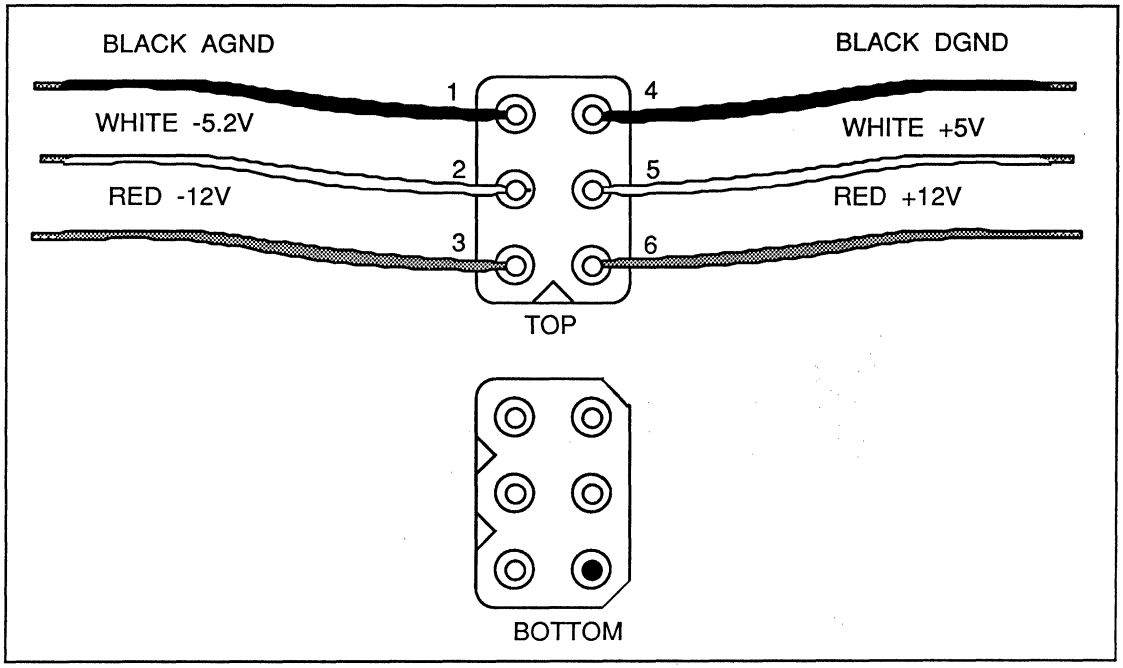


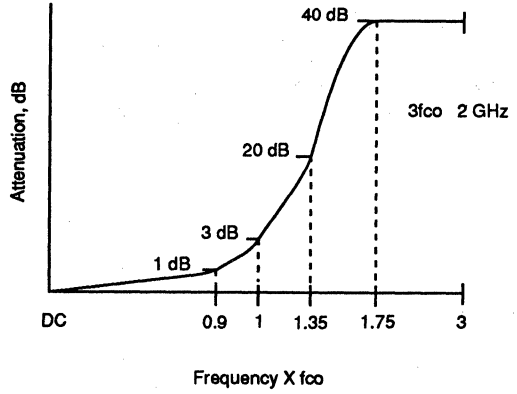
FIGURE 1C - POWER SUPPLY HARNESS CONFIGURATION

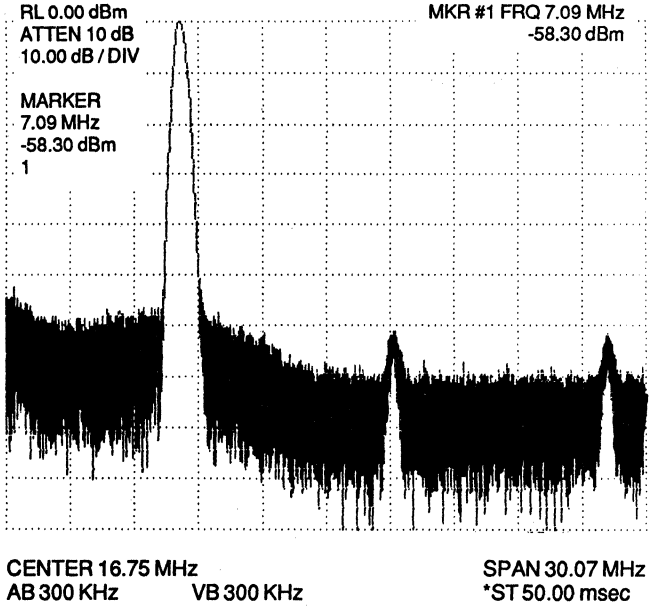
ANTI-ALIASING AND CLOCK NOISE FILTERS

The input to the EB101 buffer circuitry and the differential outputs from the D/A converter are provided with high frequency noise filters. The three filters are 90MHz low pass and are intended to be used with the full analog input frequency and full clock sampling rate of the HADC77200 A/D converter. If lower frequencies are used, the filters should be changed to filter clock noise and harmonics for a particular application. Mini-Circuits Inc. (see below) supplies a range of low pass filters that fit into the same position as the 90MHz filters on the EB101 Evaluation board.

Additional filtering can be achieved by decreasing the bandwidth of the input buffer by adjusting the 500Ω potentiometer (R22 in Figure 4) clockwise. Also, adjustment of the clock duty cycle with potentiometer R5 will lower the overall noise floor by controlling the setup and hold time of the digital data for the multiplexers (F100155) and DAC (HDAC10181).

Low Pass
Typical Frequency Response



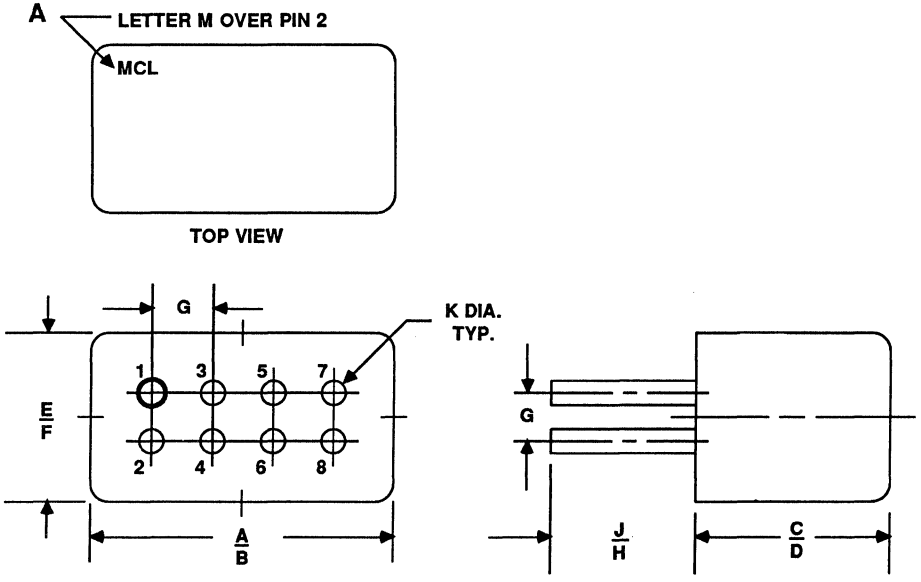


DAC OUTPUT SPECTRUM ANALYSIS OF A 10MHz INPUT FUNDAMENTAL WITH A 10.7MHz (PLP-10.7) OUTPUT LOW PASS FILTER AND 100MHz CLOCK RATE

PLP
case A01

MODEL NO.	PASSBAND, MHz (loss < 1dB) Min.	fco, MHz (loss 3dB) Nom.	STOP BAND, MHz (loss > 20dB) Max.	STOP BAND, MHz (loss > 40dB) Max.	STOP BAND, MHz (loss > 40dB) Min.	VSWR, Passband Typ.	VSWR, Stopband Typ.
PLP-10.7	DC-11	14	19	24	200	1.7	1.7
PLP-50	DC-48	55	70	90	200	1.7	17
PLP-70	DC-60	67	90	117	300	1.7	17
PLP-100	DC-98	108	146	189	400	1.7	17

Case no.	A	B	C	D	E	F	G	H	J	K
A01	.770	.800	.385	.400	.370	.400	.200	.20	.14	.031
	19.56	20.32	9.78	10.16	9.40	10.16	5.08	5.08	3.56	.79



NOTE: BLACK BEAD INDICATES PIN 1. PIN NUMBERS DO NOT APPEAR ON UNIT. FOR REFERENCE ONLY.

PIN CONNECTIONS

SEE CASE STYLE OUTLINE DRAWING

SERIES	IN	OUT	GROUND
PLP	1	8	2, 3, 4, 5, 6, 7

8

FIGURE 2 - DETAILED SCHEMATIC OF EB101, REVISION C

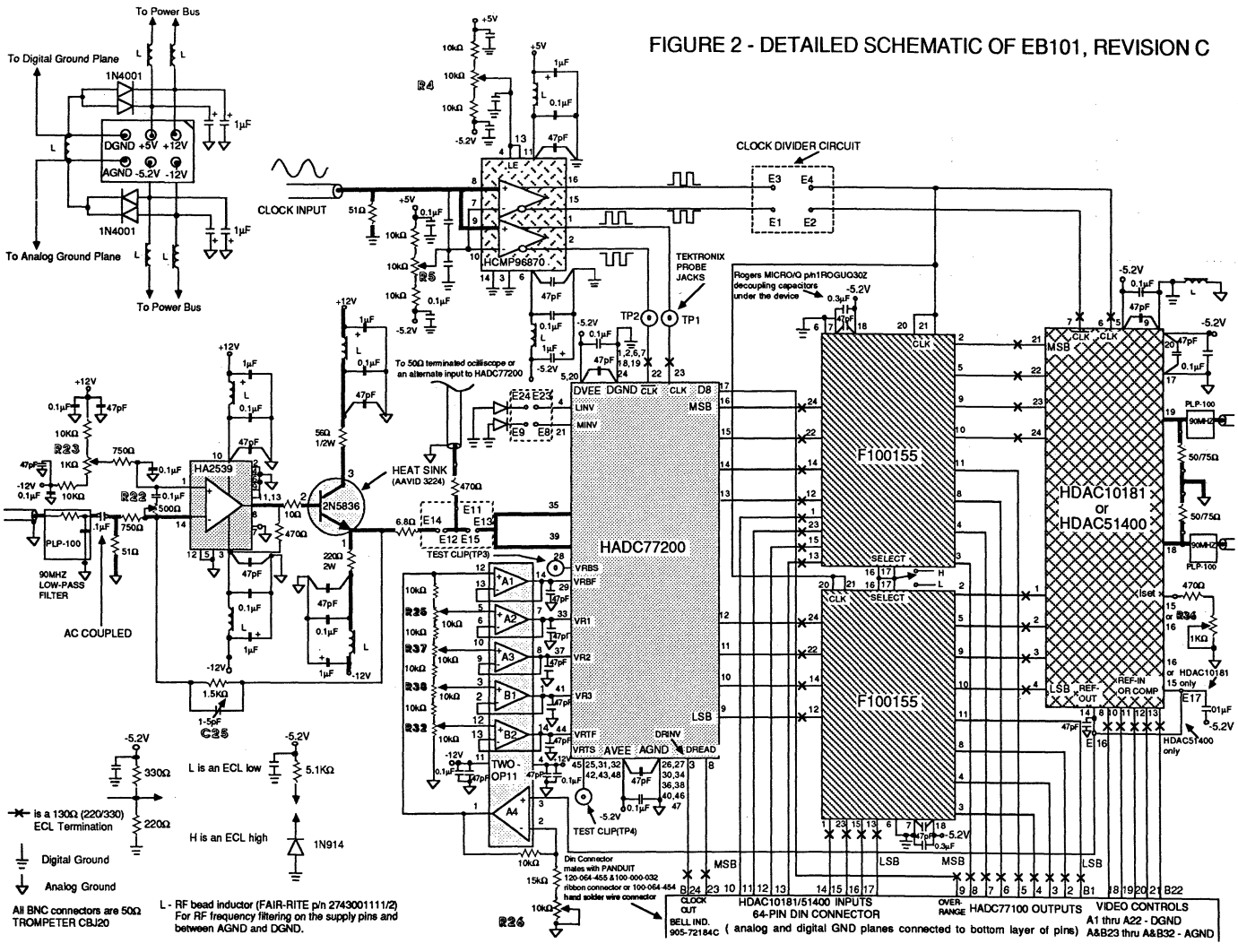
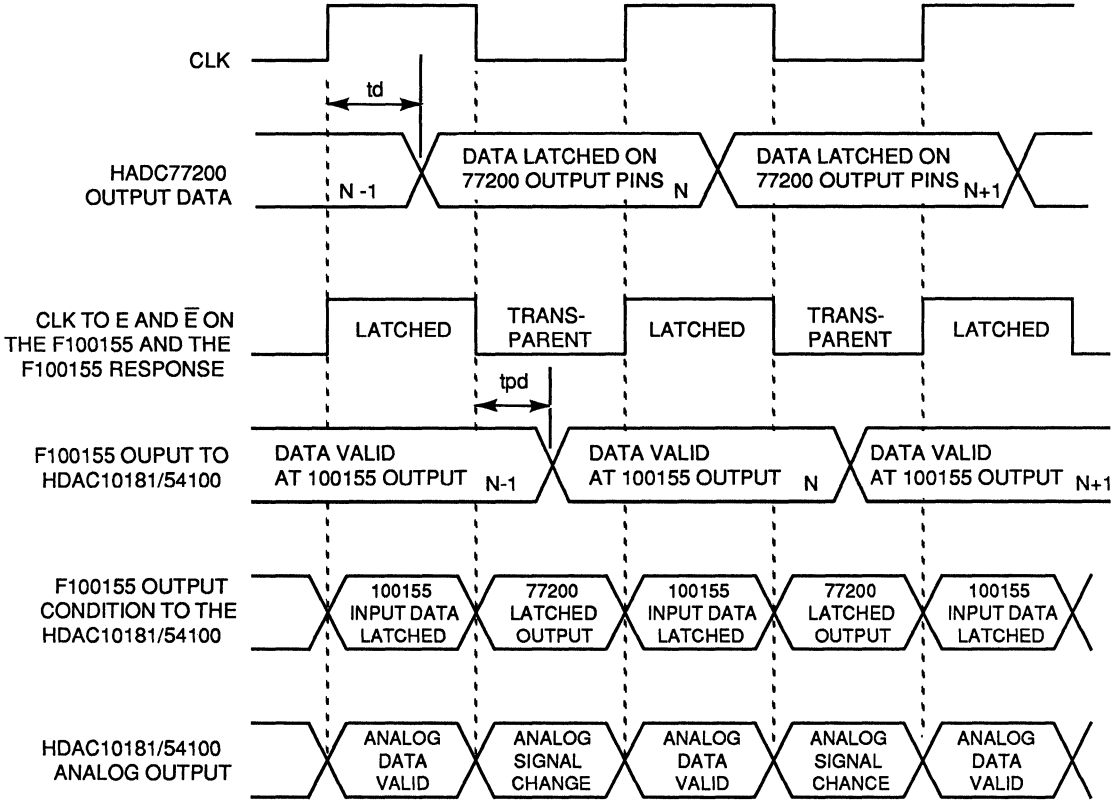
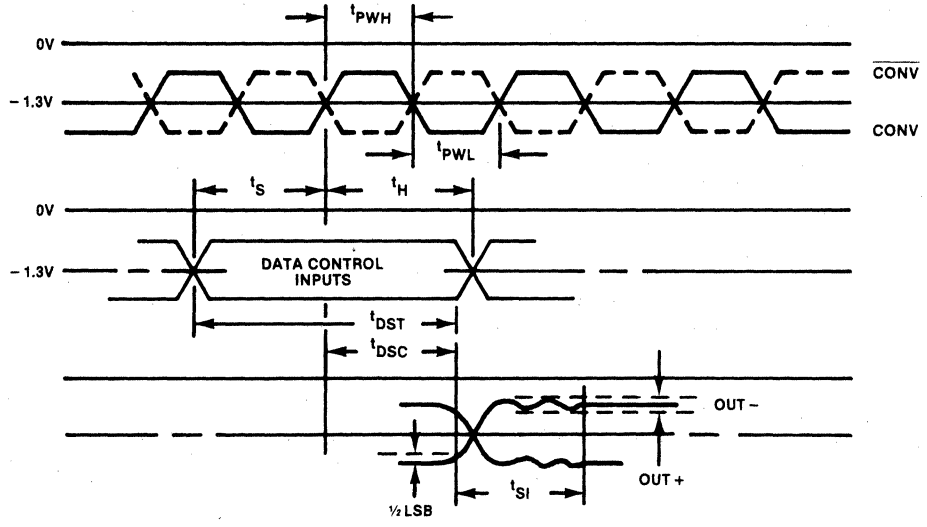


FIGURE 3 - TIMING DIAGRAM



8

FIGURE 3 CONTINUED 10181/51400 TIMING DIAGRAM



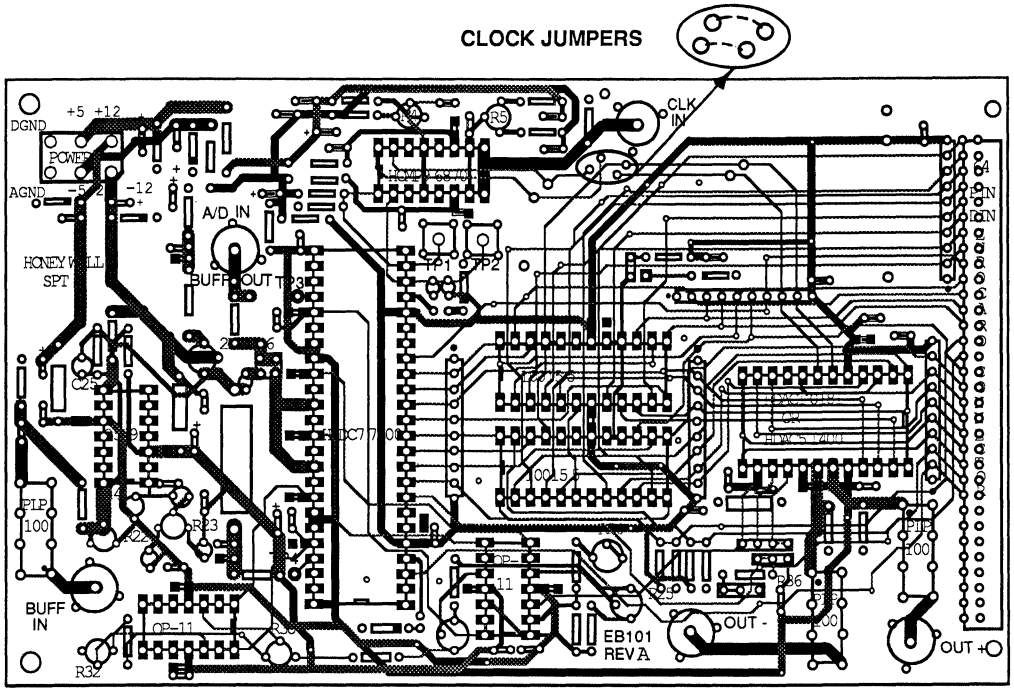


FIGURE 4A - MAIN BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

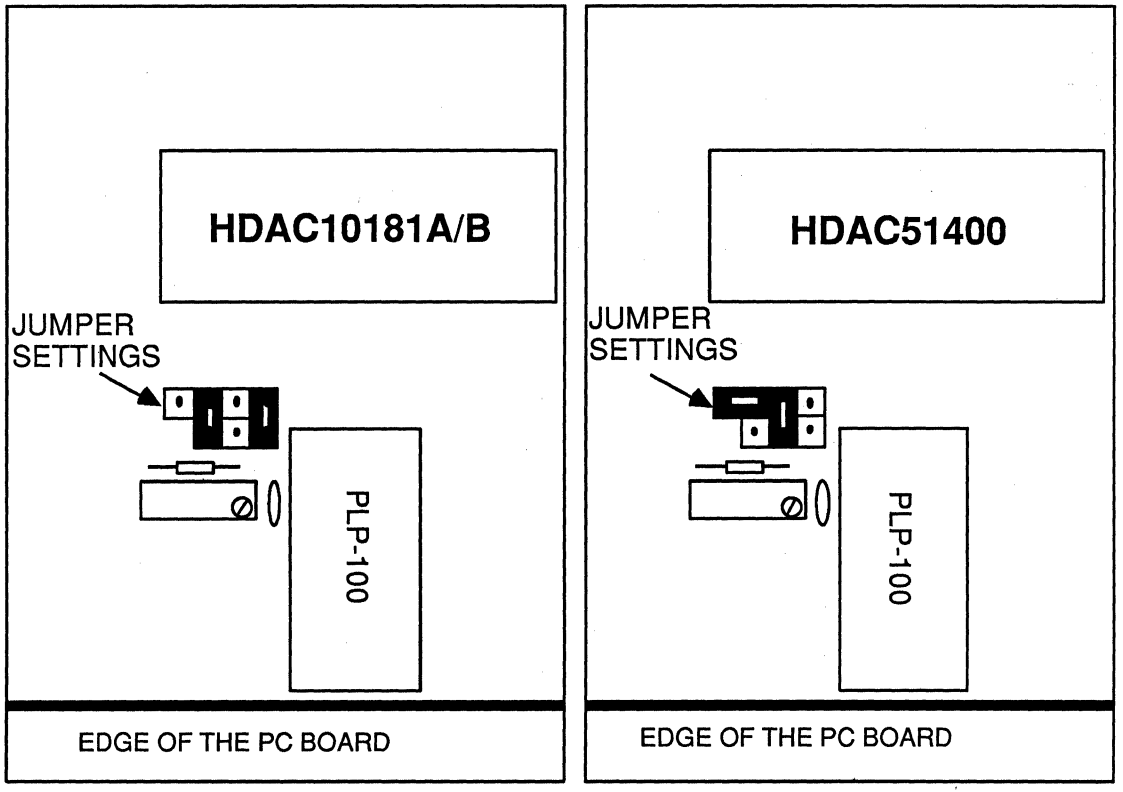
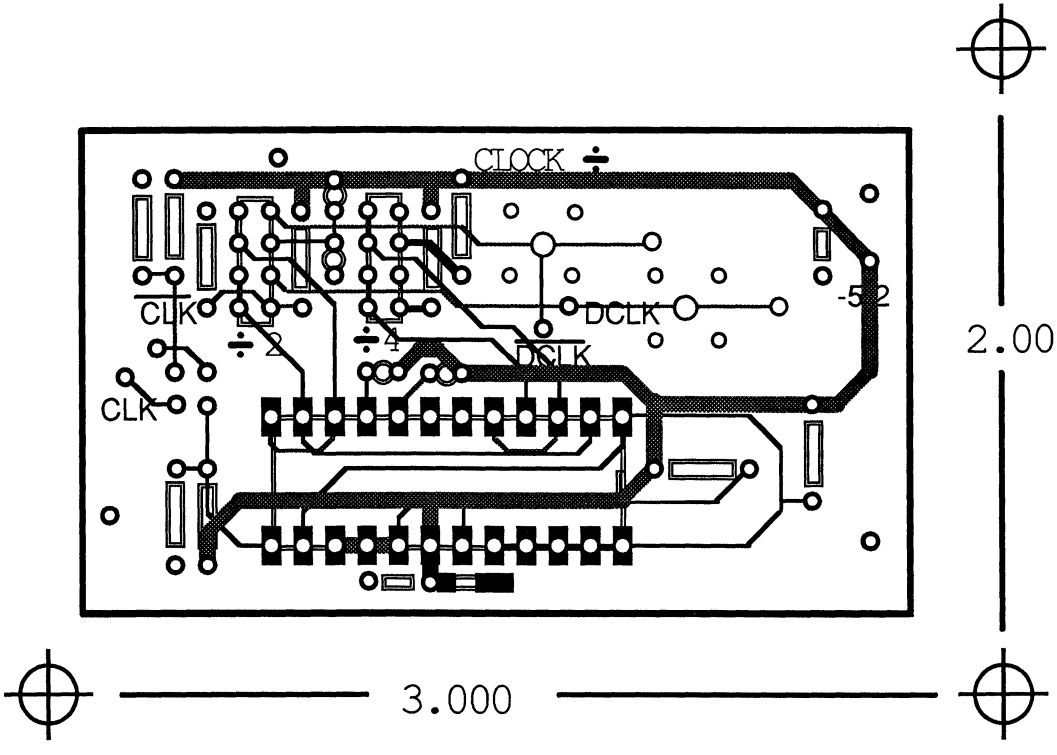


FIGURE 4B - JUMPER POSITION AND CONNECTIONS FOR EITHER THE HDAC10181A/B OR HDAC51400
(Not To Scale)



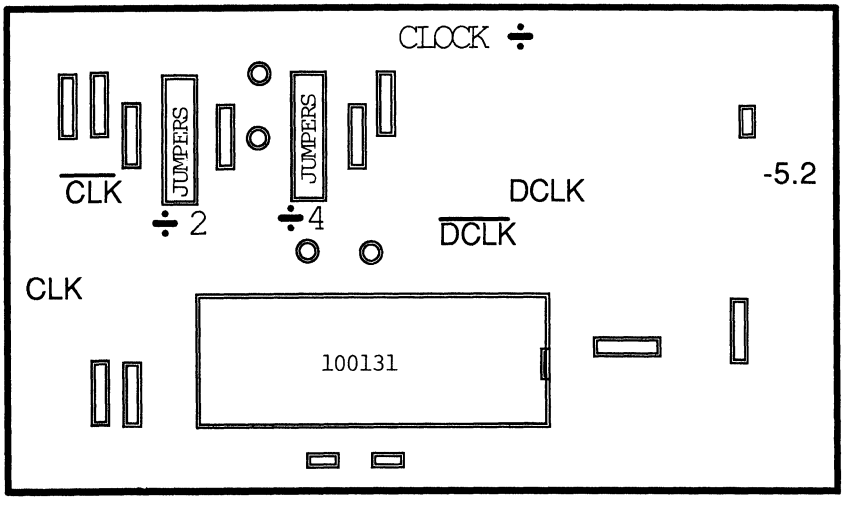


FIGURE 5 - CLOCK DIVIDER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

EB101 REVISION C PARTS LIST

PARTS LIST			
NO.	**DESCRIPTION**	**QTY.**	**MANUFACTURER / PART NO.**
1	FERRITE BEAD	11	FAIR-RITE CORP.-2743001111
2	DIODE	4	1N4001
3	DIODE	3	1N914
4	TRANSISTOR	1	MOTOROLA-2N5836
5	I.C.	1	HONEYWELL-HDAC10181A/B OR HDAC51400
6	I.C.	1	HONEYWELL-HCMP96870
7	I.C.	2	FAIRCHILD-F100155
8	I.C.	2	PMI-OP-11
9	I.C.	1	HONEYWELL—HADC77200A/B
10	I.C.	1	HARRIS-HA2539
11	FILTER	3	MINI-CIRCUITS-PLP-100
12	RESISTOR	1	240Ω, 2w
13	RESISTOR	1	56Ω, 1/2w
14	RESISTOR	1	6.8Ω, 1/8w
15	RESISTOR	11	10KΩ, 1/8w
16	SIP RESISTOR PACK	5	220/330Ω
17	RESISTOR	4	220Ω, 1/8w
18	RESISTOR	4	330Ω, 1/8w
19	RESISTOR	2	750Ω, 1/8w
20	RESISTOR	3	50Ω, 1/8w
21	RESISTOR	3	470Ω, 1/8w
22	RESISTOR	1	10Ω, 1/8w
23	RESISTOR	1	15.1Ω, 1/8w
24	RESISTOR	1	5kΩ, 1/8w
25	RESISTOR	1	1.5kΩ, 1/8w
26	POTENTIOMETER	2	BOURNS-1KΩ, 3329-H-102 & MOUSER-ME323-4290W-1kΩ
27	POTENTIOMETER	8	BOURNS-10KΩ, 3329-H-103
28	CONNECTOR, DIN	1	BELL IND.-905-72184C
29	CONNECTOR	1	MOLEX-09-18-5069
30	CAPACITOR, CHIP	16	JOHANSON-47pf 500R15N470JP4
31	CAPACITOR	10	SPRAGUE-1uf TANT, 35V
32	CAPACITOR	29	SPC TECHNOLOGY-0.1µf
33	CAPACITOR, ADJ	1	JOHANSON-47pF-9621
34	CONNECTOR, BNC	5	TRUMPETER-CBJ20, 50Ω
35	TEST POINTS	2	TEKTRONIX 131-2766-01,136-0352-02
36	PIN RECEPTACLE	42	MILL MAX-0552-1-15-15-11-27-10-0
37	PIN SOCKET	9	SAMTEC-SL-132-G-12
38	SOCKET, 24PIN	1	SAMTEC-ICO-624-NGT
39	PRINTED CIRCUIT BOARD	1	HONEYWELL-EB101
40	TEST POINTS	2	COMPONENTS CORP. TP-102
41	CAPACITOR	2	Q-PAK Q302
42	JUMPER PINS	18	SAMTEC

EB101 CLOCK DIVIDER BOARD

NO.	DESCRIPTION	QTY.	MANUFACTURER / PART NO.
43	F100131	1	FAIRCHILD TRIPLE D-TYPE FLIP-FLOP
44	CAPACITOR	2	.1µF
45	TEST POINTS	2	TEKTRONIX 131-2766-01, 136-0352-02
46	RESISTOR	6	1KΩ, 1/8w 5%
47	RESISTOR	4	220Ω,1/8w 5%
48	RESISTOR	4	330Ω, 1/8w 5%
49	CAPACITOR	1	JOHANSON-47pF CHIP
50	TEST POINTS	2	COMPONENTS CORP.-TP-102

PARTS LIST				
NO.	REF. DESIG.	QTY.	DESCRIPTION	MANUFACTURER / PART NO.
1	C1, 3, 5, 8, 12, 13, 15	7	CAPACITOR, .1µf - 50V	AVX / SR205E104MAA
2	C2, 4, 7, 14	4	CAPACITOR, 47pf - CHIP	JOHANSON / 500R15N470JP4
3	C10, 11, (NOTE 3)	2	CAPACITOR, SEALTRIM 5-20pf	JOHANSON / 9629
4	CR1, 2	2	DIODE, 1N4001	
5	E1, 2	2	JUMPER PINS (HEADER STRIP)	CYPRESS / TSW-1-36-07-T-S
6	FL1	1	FILTER, 90MHz LOWPASS	MINICIRCUITS / PLP-100
7	J1, 2 (NOTE4)	2	RECEPTACLE, BNC	TRUMPETER / CBJ20
8	L1, 2	2	RF BEAD	FAIR-RITE / 2743001111/2
9	P1	1	PLUG	MOLEX / 09-18-5031
10	R1, 2	2	RESISTOR, 10K OHM	HAMILTON / AVNET / CF1/8-10K-5%-T/R
11	R4, 12	2	RESISTOR, 33 OHM	HAMILTON / AVNET / CF1/8-33-5%-T/R
12	R5	1	RESISTOR, 25K OHM	HAMILTON / AVNET / CF1/8-25K-5%-T/R
13	R7 (NOTE 1)	1	RESISTOR, 1.5K OHM	HAMILTON / AVNET / CF1/8-1.5K-5%-T/R
14	R7, 8 (NOTE 2)	2	RESISTOR, 250 OHM	HAMILTON / AVNET / CF1/8-250-5%-T/R
15	R9	1	RESISTOR, 150 OHM	HAMILTON / AVNET / CF1/8-150-5%-T/R
16	R10	1	RESISTOR, 51 OHM	HAMILTON / AVNET / CF1/8-51-5%-T/R
17	R3	1	POTENTIOMETER, 10K OHM	BOURNS / 3339-1-103
18	R6, 11	2	POTENTIOMETER, 1M OHM	BOURNS / 3339-1-106
19	C6, 9	2	CAPACITOR, 1µf TANT, 35V	SPRAGUE / 196 DIO5X9035HAI
20	U1 (NOTE 1)	1	I.C., OP-AMP	COMLINEAR / CLC221A1
21	U1 (NOTE 2)	1	I.C., BUFF-AMP	COMLINEAR / CLC231A1
22	PCB1	1	PRINTED CIRCUIT BOARD	HONEYWELL / EB102 REV. B

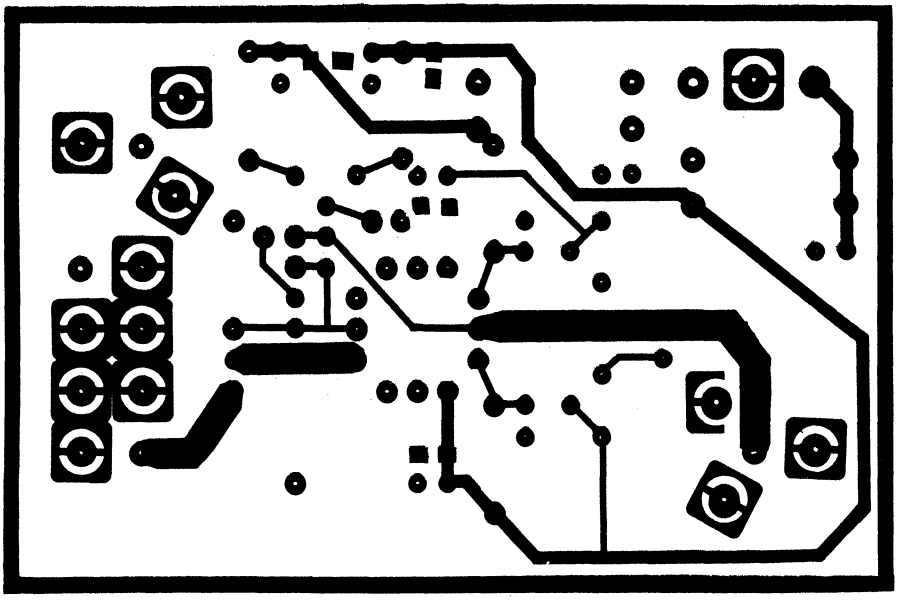
NOTES:

1) USE ITEM NO. 13 WITH ITEM NO. 20 AND JUMPER E1, 2.

2) USE ITEM NO. 14 WITH ITEM NO. 21.

3) USE C10 WITH ITEM NO. 21 ONLY.

4) J2 IS MOUNTED ON THE BACKSIDE OF PCB1.



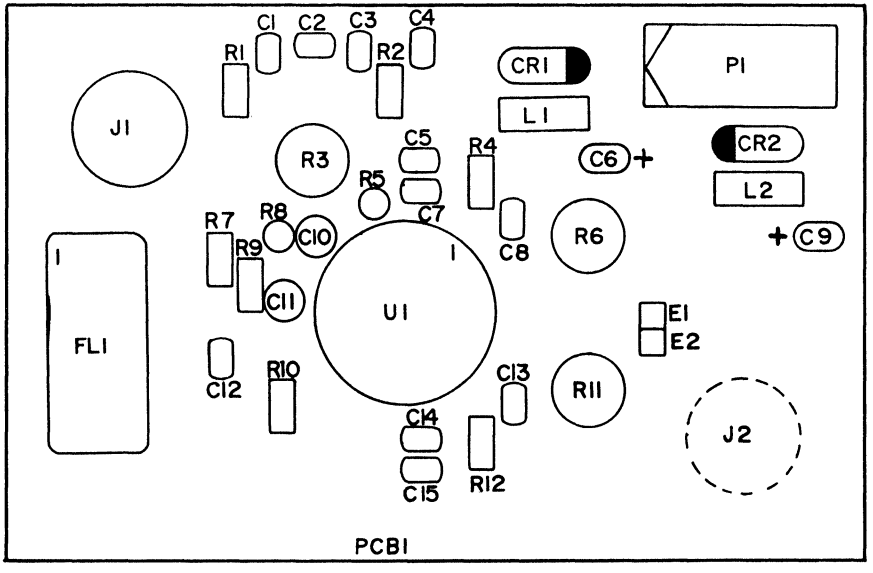


FIGURE 6 - EB102 BUFFER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

SET-UP PROCEDURE FOR THE EB101 DEMONSTRATION BOARD

The following setup procedure is completed at Honeywell before the EB101 board is shipped to the customer. It is not necessary for the user to perform this exercise, but it is included for informational purposes.

The EB101 demonstration board is accompanied with a literature package containing the "AN102 APPLICATION NOTE" , the "HADC77200", "HDAC51400", "HDAC-10181", and "HCMP96870" data sheets, and an applications department business card. Also, a power harness, and a capacitor alignment tool are included. If there are any questions, please call the applications engineer on the card.

STEP 1

Connect the wire end of the power supply harness to power supplies as shown in Figure 1C. The power harness should be connected to the board with the bevelled edges and hollow connector alligned for correct operation.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

Table 3 (page 6) shows the power requirements for the EB101. Use the current gauges on the power supply or a DMM in line with the power lines and set on current (I). these current values will vary somewhat until all the potentiometers are adjusted. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

STEP 2

Refer to Figure 2 and 4 on the previous pages. Place a DMM probe (set to voltage selection) on the black jumpers at the input to the HADC77200 (E14). This should read -1V and is adjusted by turning potentiometer R23 (See Table 2A).

STEP 3

Again, refer to Figures 2 and 4 on the previous pages and Table 5 on this page. Place a DMM probe (set to voltage selection) on pin 3 of the OP11-A and read approximately -1.2V. If it does not, then check to see if the black jumpers for the HDAC10181/51400 are set up

TABLE 5 - EQUIPMENT LIST

2 - SIGNAL GENERATORS CAPABLE OF PRODUCING 1MHZ AND 20MHZ SINEWAVES AT UP TO 1Vp-p OUTPUT LEVELS INTO 50Ω. H.P. 8656A OR EQUIVALENT.

1 - OSCILLISCOPE, EITHER H.P. DIGITIZING OSCILLISCOPE MODEL 54100D OR EQUIVALENT OR TEKTRONIX MODEL 2465.

1 - DIGITAL MULTIMETER(DMM), KEITHLEY 197 OR EQUIVALENT.

4 - POWER SUPPLIES CAPABLE OF PRODUCING THE POWER LISTED IN TABLE 1. 2 LAMBDA LPT-7202-FM OR EQUIVALENT.

5 - 50Ω COAX CABLES (RG58) WITH BNC TYPE CONNECTORS.

1 - HIGH IMPEDANCE PROBE (1MΩ) - TEKTRONIX OR H.P.

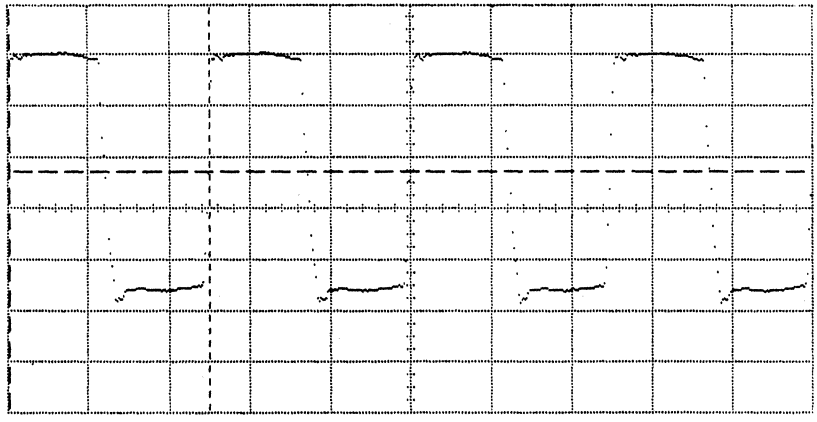
for the right part (see Figure 4B). Next set the probe on pin 1 of the OP11-A. This should read -2V and is adjusted by turning potentiometer R26. Now set the probe on pin 7 of the OP11-A. This should read -2V and is adjusted by turning potentiometer R26. Now set the prove on pin 7 of the OP11-A. This should read approximately -1.5V and is adjusted by potentiometer R25. Pin 8 of the OP11-A should read -1.0V and is adjusted by potentiometer R37. On the other amplifier, OP11-B, potentiometer R38 controls the output from pin 1 and should read -0.5V. Finally, R32 sets up the output from pin 14 on OP11-B and can be set between GROUND and -50mV.

STEP 4

Refer to Figures 2 and 4. Attach a 50Ω BNC cable to the "CLK IN" BNC connector. Attach the other end to a sinewave or signal generator set at 20MHz frequency and 1Vp-p amplitude (if 1Vp-p is not available, amplitudes down to 100mVp-p are acceptable). Put a Tektronix or H.P. high impedance probe in one or both of the probe jacks immediately below the HCMP96870 comparator. Adjust potentiometer R5 to achieve a 50% duty cycle square wave (both "high" and "low" states are the same length). Adjust potentiometer R4 if no waveform is present and/or to get rid of any jitter in the square wave (this is a hysteresis adjustment). The square wave amplitude should be approximately 900mVp-p and look like Figure 7 below.

STEP 5

Refer to Figure 2 and 4. Attach a 50Ω coax cable to the BNC connector marked "BUFFER IN". Use a second sinewave or signal generator set at 1 MHz frequency and 1Vp-p amplitude (See Figure 8). Attach another cable to the BNC connector "A/D IN / BUFFER OUT" and to an oscilliscope set at 50Ω input impedance. A 200mVp-p amplitude signal swinging around -100mVdc should apear at a 1MHz frequency (See Figure 9). If oscillation is evident (erratic signal amplitude or wrong frequency), potentiometer R22 and capacitor C25 must be adjusted. Adjust potentiometer R22 to the full counterclockwise range. Now adjust capacitor C25 to stop the oscillation. See Figures 10, 11 and 12.



-100.000 nsec 0.00000 sec 100.000 nsec

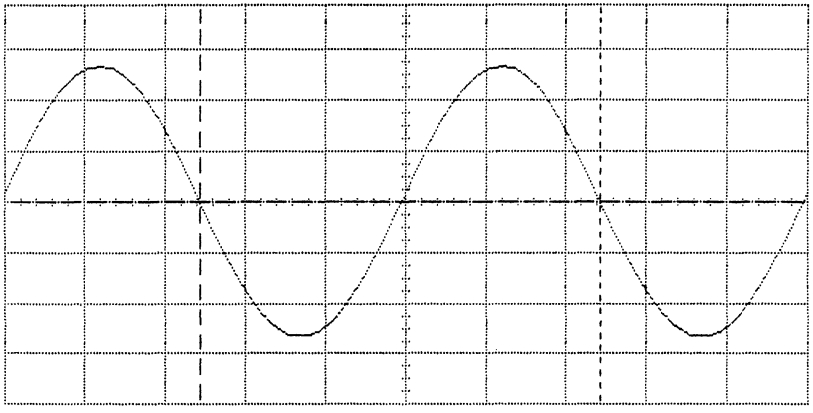
Ch. 2	=	200.0 mvolts / div	Offset	=	-1.330 volts
Timebase	=	20.0 nsec / div	Delay	=	0.00000 sec
Ch. 2 Parameters			P-P Volts	=	968.7 mvolts
Rise Time	=	1.670 nsec	Fall Time	=	2.910 nsec
Freq.	=	20.1532 MHz	Period	=	49.620 nsec
+ Width	=	24.940 nsec	- Width	=	24.680 nsec
Overshoot	=	6.249 mvolts	Preshoot	=	43.75 mvolts

Trigger mode: Edge
On Pos. Edge on Chan2
Trigger Levels

Chan2	=	-1.180 volts
Holdoff	=	70.000 nsecs

FIGURE 7 - CLOCK OUTPUT AT THE TEKTRONIX PROBE JACKS

FIGURE 8 - INPUT SIGNAL TO THE BOARD (50Ω INPUT IMPEDANCE)



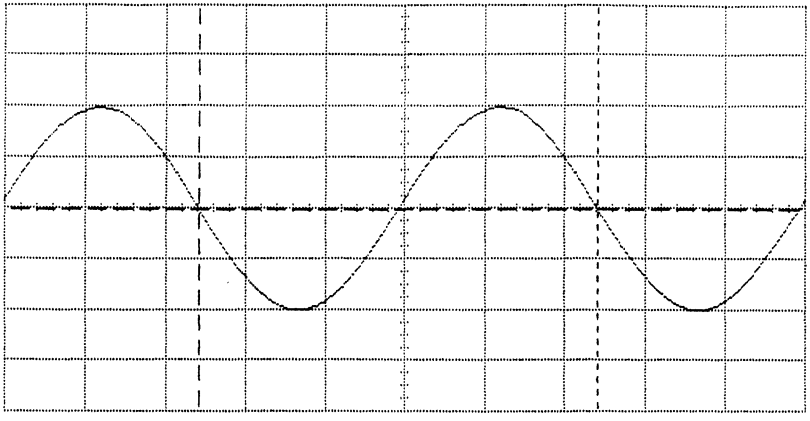
-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	1.062 volts
Rise Time	=	289.640 nsec	Fall Time	=	289.320 nsec
Freq.	=	1.00014 MHz	Period	=	999.860 nsec
+ Width	=	497.520 nsec	- Width	=	502.340 nsec
Overshoot	=	6.249 mvolts	Preshoot	=	6.249 mvolts

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels

Chan1	=	0.000 volts
Holdoff	=	70.000 nsecs

FIGURE 9 - OUTPUT SIGNAL FROM THE "BUFFER OUT" BNC CONNECTOR (50Ω IMPEDANCE)

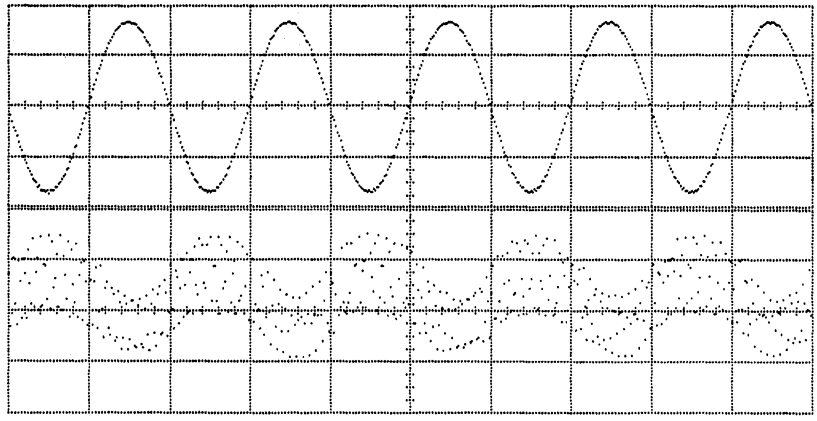


-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	50.00 mvolts / div	Offset	=	-100.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	200.0 mvolts
Rise Time	=	294.080 nsec	Fall Time	=	289.910 nsec
Freq.	=	997.904 KHz	Period	=	1.00210 usec
+ Width	=	499.810 nsec	- Width	=	502.290 nsec
Overshoot	=	1.562 mvolts	Preshoot	=	1.562 mvolts

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels

Chan1	=	-100.0 mvolts
Holdoff	=	70.000 nsecs



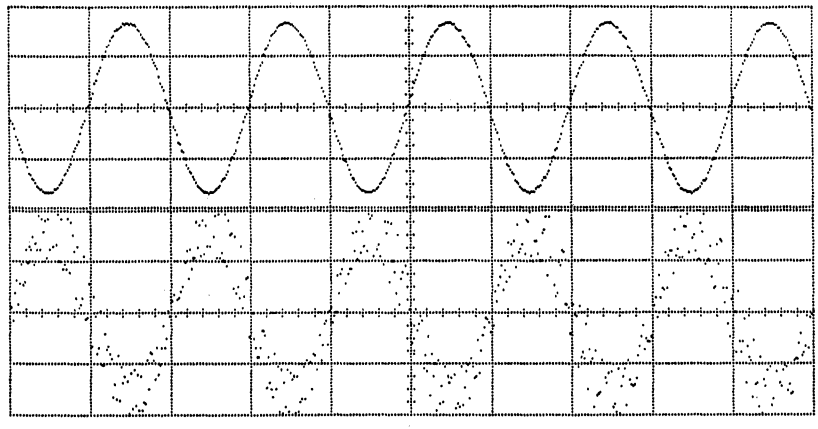
-2.50000 usec 0.00000 sec 2.50000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Ch. 2	=	40.00 mvolts / div	Offset	=	-102.0 mvolts
Timebase	=	500 nsec / div	Delay	=	0.00000 sec

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels

Chan1	=	0.000 volts
Holdoff	=	70.000 nsecs

FIGURE 10 - OSCILLATIONS ARE APPARENT AND ADJUSTMENT IS NECESSARY



-2.50000 usec 0.00000 sec 2.50000 usec

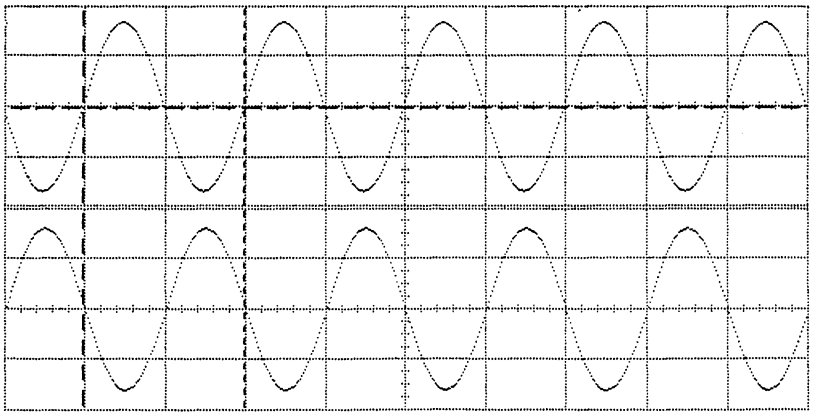
Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Ch. 2	=	40.00 mvolts / div	Offset	=	-102.0 mvolts
Timebase	=	500 nsec / div	Delay	=	0.00000 sec

Trigger mode: Edge
On Pos. Edge on Chan1
Trigger Levels

Chan1	=	0.000 volts
Holdoff	=	70.000 nsecs

FIGURE 11 - THE OSCILLATIONS ARE DECREASING AND THE BOTTOM WAVEFORM IS STARTING TO APPROACH THE SAME SHAPE AS THE TOP WAVEFORM

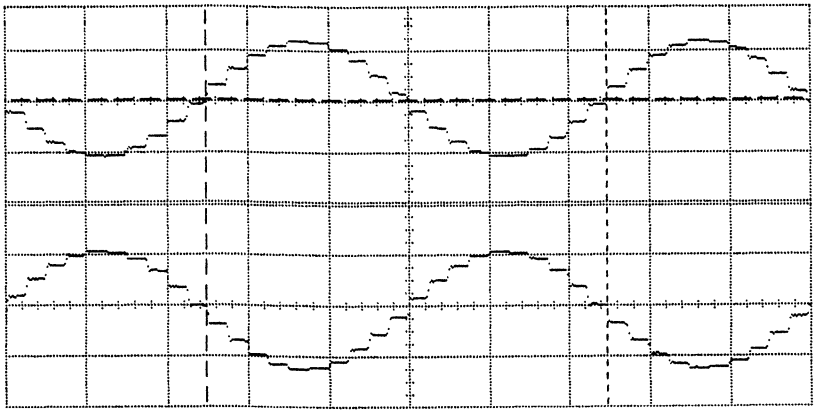
FIGURE12 - OSCILLATION HAS STOPPED AND THE BOTTOM WAVE-FORM IS THE SAME SHAPE AS THE TOP WAVEFORM BUT IS INVERTED



-2.50000 usec 0.00000 sec 2.50000 usec

Ch. 1	=	200.0 mvolts / div	Offset	=	0.000 volts
Ch. 2	=	40.00 mvolts / div	Offset	=	-102.0 mvolts
Timebase	=	500 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	665.6 mvolts
Rise Time	=	290.790 nsec	Fall Time	=	291.830 nsec
Freq.	=	999.990 KHz	Period	=	1.00001 usec
+ Width	=	500.180 nsec	- Width	=	499.830 nsec
Overshoot	=	0.000 volts	Preshoot	=	0.000 volts

FIGURE 13 - OUTPUT WAVEFORMS FROM "OUT-" AND "OUT+" WITHOUT THE CLOCK DIVIDER BOARD INSERTED AND THE CLOCK JUMPERS CONNECTED AS SHOWN IN THE TOP OF FIGURE 4



-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	400.0 mvolts / div	Offset	=	-964.0 mvolts
Ch. 2	=	400.0 mvolts / div	Offset	=	-544.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	912.5 mvolts
Rise Time	=	290.470 nsec	Fall Time	=	297.770 nsec
Freq.	=	1.00264 MHz	Period	=	997.370 nsec
+ Width	=	499.250 nsec	- Width	=	498.120 nsec
Overshoot	=	6.249 mvolts	Preshoot	=	6.249 mvolts

Trigger mode: Edge
On Neg. Edge on Chan1
Trigger Levels

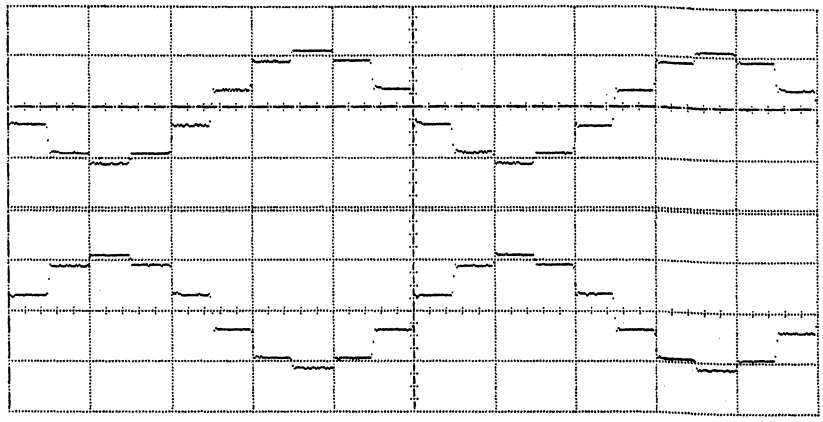
Chan1	=	-964.0 mvolts
Holdoff	=	70.000 nsecs

STEP 6

This measurement is done without the clock divider board connected and clock jumpers inserted as shown in the top of Figure 4. Again referring to Figures 2 an 4, attach a 50Ω coax cable to the BNC connector marked "OUT-" and another cable to "OUT+". Attach the other end to an oscilliscope set to 50Ω input impedance. The outputs should be the opposite of each other and at approximately a 900mV amplitude. Adjust potentiometer R36 to achieve this level. Do not adjust too far or the signal will start deteriorating. See Figure 13. After completing step 6, remove one end of each "clock jumper" wire and leave the other end soldered to the board.

STEP 7

Insert the clock divider board and connect the shorting jumpers to the posts in the +2 configuration and compare to the waveform in Figure 14.



-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	400.0 mvolts / div	Offset	=	-936.0 mvolts
Ch. 2	=	400.0 mvolts / div	Offset	=	-576.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec
Ch. 1 Parameters			P-P Volts	=	912.5 mvolts
Rise Time	=	201.240 nsec	Fall Time	=	201.350 nsec
Freq.	=	1.00255 MHz	Period	=	997.460 nsec
+ Width	=	499.050 nsec	- Width	=	498.410 nsec
Overshoot	=	100.0 mvolts	Preshoot	=	100.0 mvolts

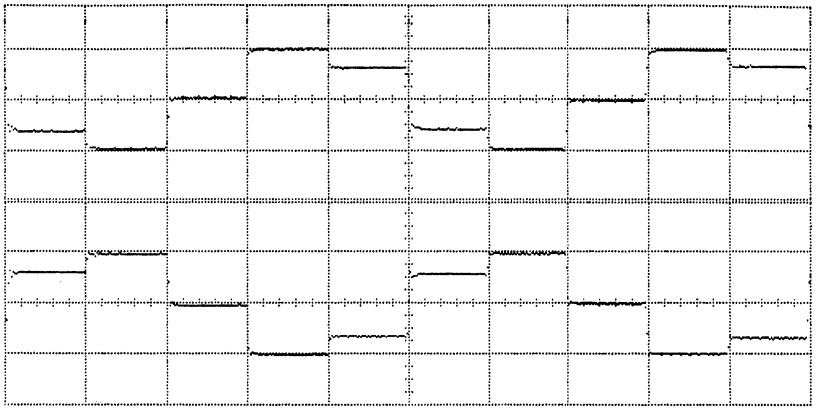
Trigger mode: Edge
On Neg. Edge on Chan1
Trigger Levels

Chan1	=	-936.0 mvolts
Holdoff	=	70.000 nsecs

FIGURE 14 - "OUT-" AND "OUT+" WITH THE CLOCK DIVIDER BOARD INSERTED AND SET AT +2 MODE

STEP 8

Insert the clock divider board and connect the shorting jumpers to the posts in the +4 configuration and compare to the waveform in Figure 15.



-1.00000 usec 0.00000 sec 1.00000 usec

Ch. 1	=	400.0 mvolts / div	Offset	=	-944.0 mvolts
Ch. 2	=	400.0 mvolts / div	Offset	=	-568.0 mvolts
Timebase	=	200 nsec / div	Delay	=	0.00000 sec

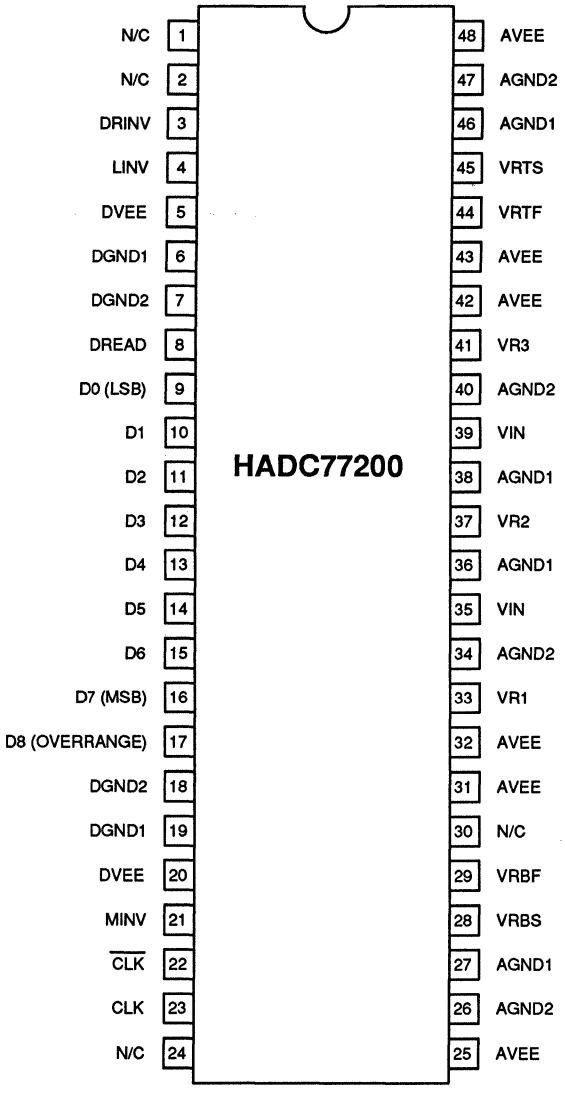
Trigger mode: Edge
On Neg. Edge on Chan1
Trigger Levels

Chan1	=	-944.0 mvolts
Holdoff	=	70.000 nsecs

FIGURE 15 - "OUT-" AND "OUT+" WITH +4 CLOCK DIVIDER MODE

PIN ASSIGNMENTS HADC77200

TOP VIEW



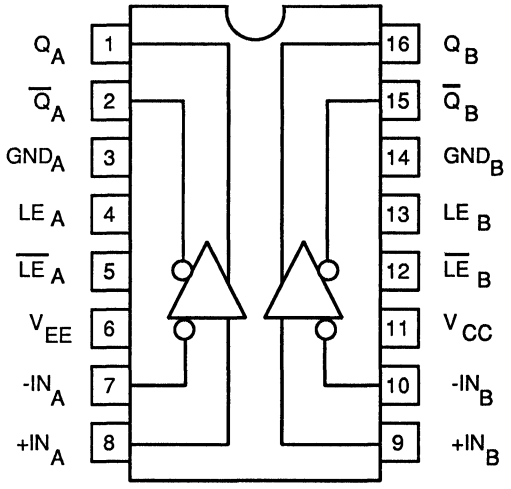
48 LEAD CERAMIC SIDEBRAZED DIP

PIN FUNCTIONS HADC77200

NAME	FUNCTION
DRINV	Data Ready Inverse
LINV	D0 through D6 Output Inversion Control Pin
AVEE	Negative Analog Supply Nominally -5.2V
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
DREAD	Data Ready Output
DO	Digital Data Output Pin 1 (LSB)
D1 - D6	Digital Data Output Pin 2 Through 6
D7	Digital Data Output Pin 7 (MSB)
D8	Overrange Output
MINV	D7 Output Inversion Control Pin
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRBS	Reference Voltage Bottom, Sense Nominally -2.0V
VRBF	Reference Voltage Bottom, Force Nominally -2.0V
VR1	Reference Voltage Tap 1
AGND1	Analog Ground 1
VIN	Analog Input, can be connected to the input signal or used as a Sense
AGND2	Analog Ground 2
VR2	Reference Voltage Tap 2
VIN	Analog Input, can be connected to the input signal or used as a Sense
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense Nominally 0V
VRTF	Reference Voltage Top, Force Nominally 0V

FIGURE 8B
PIN ASSIGNMENTS HCMP96870

TOP VIEW

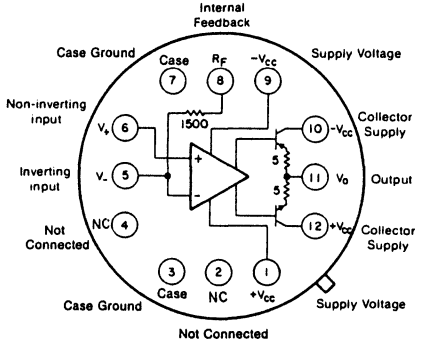


16 LEAD CERAMIC

PIN FUNCTIONS HCMP96870

NAME	FUNCTION
$\overline{Q}_A$	Output A
Q_A	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Inverted Latch Enable B
$\overline{LE}_B$	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

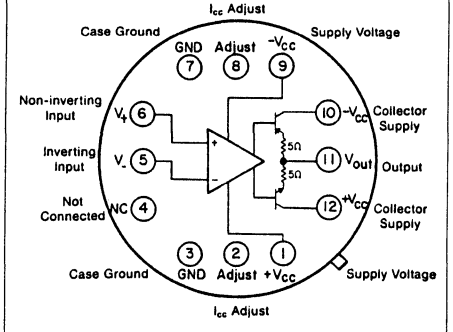
BOTTOM VIEW



Pin 8 provides access to a 1500 ohm (0.1% thin film) feedback resistor. Though not electrically connected to the circuit, the case provides EMI shielding and should be connected to a low impedance signal return.

PIN ASSIGNMENTS
COMLINEAR CLC221

BOTTOM VIEW

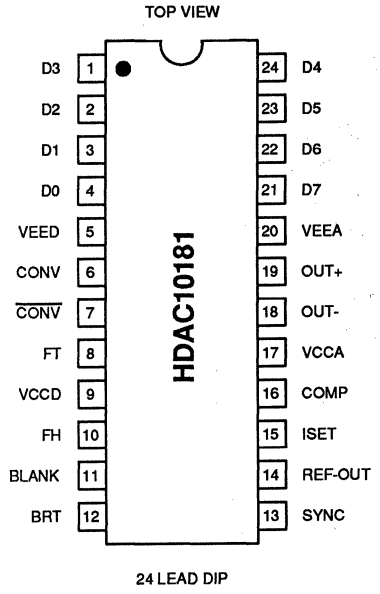


Pins 2 and 8 are used to adjust the supply current or to adjust the offset voltage (see text). These pins are normally left unconnected.

PIN ASSIGNMENTS
COMLINEAR CLC231

8

PIN ASSIGNMENTS HDAC10181

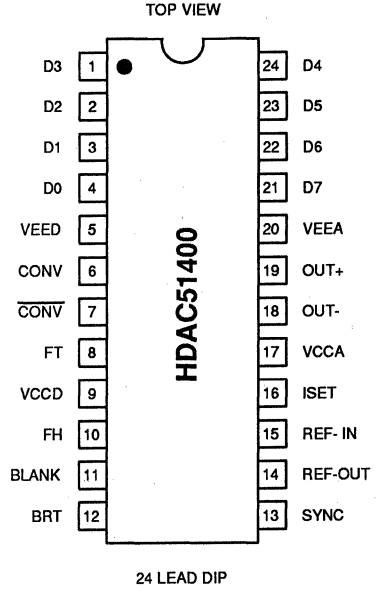


24 LEAD DIP

PIN FUNCTIONS HDAC10181

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

PIN ASSIGNMENTS HDAC51400



24 LEAD DIP

PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
REF-IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

EB103 EVALUATION BOARD APPLICATION NOTE FOR TWO PING-PONGED 8-BIT FLASH A/D CONVERTERS

Tom DeLurio, Senior Applications Engineer

FEATURES

- **400 MSPS NOMINAL CONVERSION RATE**
- 100 to 150 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamp Comparator Design/Optional Input Buffer
- ECL Timing skew clock generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200/300 A/D Converters
- Evaluation of HDAC51400 D/A Converter
- Digital Oscilliscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB103 evaluation board is intended to show the performance of the HADC77200 or HADC77300 flash A/D converters in a ping-ponged mode, and the HDAC51400 Ultra High Speed D/A converter for reconstruction. Included on the unit are two 100K ECL multiplexers for combining the ping-ponged A/D converters' 16 bits of output data into 8 bits at twice the speed. The high speed data is routed between the A/D and D/A, and also off the board as full speed or as divided down data (external clock) for slower speed FFT measurements. This is shown in the block diagram below.

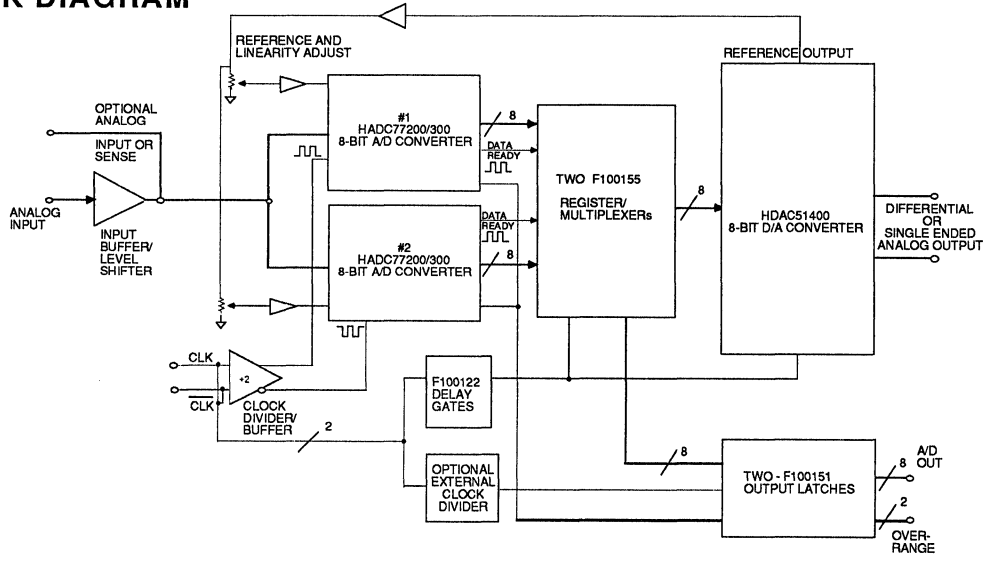
The HADC77200 is a monolithic, 8-bit flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 100 MHz at a 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HADC77300 is identical to the HADC77200 except that the analog input is 150MHz with a 250 MSPS clock rate and a corresponding increase in power dissipation.

The HDAC51400 is a monolithic 8-bit D/A converter capable of converting data at rates of 400 MWPS. The part has optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DAC has an internal reference to supply itself and the two HADC77200/300 with a stable voltage reference. It also has gain control to provide different output voltage swings so it can be used as a standard voltage output DAC.

The HCMP96870A is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the two A/D converters and D/A converter.

BLOCK DIAGRAM



8

GENERAL INFORMATION

The EB103 board is a four layer board that is manufactured for true microstrip performance. The two center copper planes are welded together to form a large ground plane. The plane is broken into digital and analog grounds to provide separate grounding for digital and analog components to achieve low noise operation. The analog inputs, outputs and clock inputs are connected with standard 50Ω BNC connectors. All interconnects achieve 50 line impedance with 50 thevenin equivalent terminations at the end of the ECL lines. Tektronix high impedance probe jacks are provided to monitor the clock lines and LSBs. Standard -5.2V, +5V, and 12 to 15 Volt power supplies are required for operation of the EB103, with nominal power dissipation of less than 30 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer and linearity TAP amplifiers are on board for high performance applications.

The EB103 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of Honeywell's HADC77200/300 8-bit Flash A/D converters, HDAC54100 8-bit Ultra High Speed D/A converter, and the HCMP96870/A dual Voltage comparator. The board contains circuitry for buffering the input signals, generating reference voltages, adjusting and dividing the A/D data and clock, and generating delays for ECL level differential clock signals. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments.

There are jumper options available to adjust clock delay between the A/D and DAC as well as Potentiometers to adjust the comparator thresholds for optimum time skew performance. The external clock option provides the ability to run the output data from the F100151 flip-flops at a slower speed for connection to a logic analyzer for digital performance tests such as FFT and Histogram, etc. (see HADC77200/300 data sheet). In addition, 100MHz or 200MHz low pass input and output filters are on board for anti-aliasing and clock noise frequency rejection.

ANALOG INPUT BUFFER

The analog input buffer is shown in Figure 1. This section consists of a low pass filter, and the CLC231 high frequency buffer-amplifier (Table 1). The input impedance is 50Ω and the gain is set at 2X so that a 1Volt$_{p-p}$ analog input can be applied for best operation. Compensation components are provided and can be adjusted for the desired gain/phase response required. The compensation is factory adjusted for 50MHz bandwidth operation. The gain of the buffer amplifier can be decreased by removing the 250Ω resistor that is connected to ground on the inverting input to achieve a voltage follower. This change will increase the available bandwidth of the amplifier. The BNC connector shown in the schematics near the output of the buffer can be used for monitoring the buffer output and input to the HADC77200/300. The BNC should be connected to a 50Ω terminated oscilliscope and will provide a 10X attenuated signal.

The input buffer can be bypassed by removing the 6.8 resistor at the output of the CLC231 and the 470 resistor between the BNC connector and the HADC77200/300. Bypass the 470 resistor with a jumper wire and the HADC77200/300 can now be driven directly. The input impedance to the two converters is 2K in parallel with a 120pF distributed capacitance.

The negative input to the CLC231 is tied to an offset adjust to center the input signal to the HADC77200 around -1V, which is needed if a 2V$_{p-p}$ input signal is applied. Futher fine adjustment is provided by the two offset adust pins on the CLC231.

TABLE 1 - COMLINEAR CLC231 BUFFER AMPLIFIER

SPECIFICATION	CLC231
Gain Range	±1 to 5
Output (V, mA)	11, 100
Slew Rate (V/ sec)	3000
-3dB Bandwidth (Av=2)	165MHz
Settling Time (nsec, %)	12, 0.1 15, 0.05
Harmonic(dBc) Second Distortion Third	-55 -59

100K ECL CLOCK GENERATOR

In order to ping-pong very fast A/D converters, timing between the two devices is critical since each part contributes data every other clock pulse. Therefore clock generation is somewhat complicated (See Figure 2). Furthermore, a timing delay section and skew is necessary between the A/D and DAC.

The ECL clock section consists of two HCMP96870/A dual comparators with duty cycle and hysteresis adjust

potentiometers. Also used are F100151 Hex D flip-flops, F100121 9-bit buffers, F100114 Quint Line Receivers, two low pass filters, and several jumper options for time delay.

Any type high frequency signal generator with differential ECL level outputs can be connected to the two clock BNC connectors at the inputs of the F100114 line receiver. For single-ended operation, there is a Vbb generator available on pin 19 which can be connected to one input of the line receiver. At least 150mV of swing must be available to achieve full output swings from the receivers in the single-ended mode.

Starting with the clock generation function for the HDAC51400 DAC and F100151 output data latches , the inverting output of one of the F100114 receivers is connected to another receiver in the same package. This is for an inversion and delay before going on to the time delay section consisting of several of the buffers in the F100121. The delay is set up to make up for time latency between the A/D converter, multiplexers and DAC. Several options are available by making a connection on the lines between the buffer outputs and PLP450 low pass filter. The filter is used to smooth out the 100K ECL output from the buffers to be used for time skew and duty cycle changes at the input to the "#1" HCMP96870A dual comparators. The time skew and duty cycle change is performed by adjusting potentiometer R2 to change the threshold of the comparator so that the devices' outputs activate at different times. The threshold inputs to the HCMP96870A comparators are connected together to a pot to also adjust the duty cycle of the clock. The latch enable pins are also connected together to a pot to adjust comparator hysteresis.

Two of the outputs of the #1 comparators are connected to the HDAC51400 clock inputs and one inverting output is connected to the F100151 output data registers that are routed to the ribbon cable connectors. The noninverting output from the comparator is fed to the F100114 receivers to obtain a differential ECL clock for the ribbon cable output. Optional external clock inputs to the HDAC51400 and F100151 are available to clock and aquire data at a slower speed. Probe test points are provided to monitor the clock lines.

The clock generation section for the two HADC77200/300s is next. The noninverting output of the first F100114 receivers is connected to the clock input of a F100151 flip-flop to divide the high speed clock in half for the A/D converters. The output is then smoothed by a 200MHz low pass filter for timing skew adjustments as before, and it is connected to the two noninverting inputs of "#2" HCMP96870A. The two comparators are configured the same way as before with hysteresis and threshold adjust. One set of differential outputs goes to the clock inputs of the "#1" A/D converter and the other set goes to the "#2" A/D converter. Probe test points are provided on each line to monitor timing skew.

VOLTAGE REFERENCE GENERATOR

There are several voltage reference options on the board to drive the two HADC77200/300 reference taps. The options are set up by soldering jumper wires across lines. The configuration shown in Figure 3 is the option that is used when the board is shipped. In this mode, the two A/D converters are driven from the same voltage reference at the top and bottom of the reference ladder. This way the A/Ds track each other. The other mode is shown in Figure 4. Here, each reference tap can be adjusted for best linearity match between the two or, if the application requires, mismatch. Each tap can be connected or just some of them according to the jumper connections made to accommodate the application. This configuration gives additional control at high speeds between the two A/D converters.

The reference voltage for the HADC77200/300 and HDAC51400 is internally generated by the D/A converter voltage reference of approximately 1.2Volts. The A/D converter's 2Volt reference, 3 voltage midtaps and ground are controlled by three PMI quad op-amps (OP-11). The magnitude of each setting is futher adjusted with potentiometer R25, R26, R32, R37, and R38 per HADC77200/300 as shown in the detailed schematic (Figure 4) and board layout (Figure 5) as well as Table 3.

ANTI-ALIASING AND CLOCK NOISE FILTERS

The input to the EB103 buffer circuitry and the differential outputs from the D/A converter are provided with high frequency noise filters. The three filters are 100MHz low pass and are intended to be used with the full analog input frequency and full clock sampling rate of the HADC77200 A/D converter. The version of the board with the HADC77300 will be provided with 200MHz filters. If lower frequencies are used, the filters should be changed to filter input harmonics, clock noise, and for recontruction filters for a particular application. Mini-Circuits inc. (see page 12) makes a range of low pass filters that fit into the same position as the 100MHz filters on the EB103 Evaluation board .

Adjustment of the clock time skews with potentiometer R2 and R5 will lower the overall noise floor by controlling the timing mismatch between the two A/D converters and the D/A converter setup and hold times.

INPUT/OUTPUT REGISTER AND MULTIPLEXER

The multiplexer section consists of two F100155 which select between each 8-bit digital data word from the output of either HADC77200/300. The choice is controlled by the SELECT pins which are tied to the DREAD (data ready) outputs of each HADC77200/300 . One DREAD output is inverted by the DRINV (data ready inverse) control pin so that the output clocks are in phase. This data is then fed to the HDAC10181/51400 on the "Q" outputs of the F100155 and the "Q" outputs are tied to the F100151 hex flip-flops which are connected to the external ribbon cable connector.

A/D CONVERTER SECTION

All input pins to each HADC77200 /300 are tied together to be either fed by the input buffer or by an external source.The differentiall clock inputs are driven 90 degrees out of phase so that when one A/D is acquiring the input signal the other is outputting data and vice-versa. The MINV and LINV inputs are left open and tied internally to an ECL low. The connection choices for determining the output logic are in Table 2.

D/A CONVERTER SECTION

The output current magnitude for the HDAC51400 is controlled by a potentiometer (R36) through the DAC's Iset control pin. In addition, two 100 MHz low pass filters are provided at both out- and out+ output pins as well as 50Ω terminating resistors. The terminating resistors can be changed to 75 if desired. Keep in mind that the transmission line must be terminated at the receiving end with the same value resistor. The video and feedthrough controls are routed to the 64-pin DIN connector and are normally disabled.

A/D OUTPUT DATA SECTION

The output data from the two HADC77200/300s is available at full clock speed or at a slower speed if an external clock is used. This data is taken from the "Q" outputs of the F100155 Multiplexers and clocked into two F100151 Hex D Flip-Flops. The "Q" outputs of the flip-flops are connected to ribbon connectors for easy connection to the outside world. The external clock can be connected through 50Ω SMA connectors as shown in Figure 2 at the output of the #1 - HCMP96870A pin 2. Be sure to cut the clock trace between the comparator and SMA connector.

TABLE 2 - OUTPUT LOGIC CODING

MINV / LINV	0 / 0	0 / 1	1 / 0	1 / 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IH} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

TABLE 3 - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO	FUNCTION
R26	Pot for adjusting gain to produce a 2V reference voltage for the VRB pin on the HADC77200 from the1.2V reference voltage supplied by the HDAC10181/51400.
R25/ 37/38	Pots for setting the linearity adjustments at the comparator reference ladder on the HADC77200.
R32	Pot for setting the top point (VRT)on the reference voltage ladder. Nominally set at 50mV below AGND
R36	Pot for adjusting output current drive from the HDAC10181/51400 (See data sheets). Vout+=25.6(digital code X Iset)/RL
R2/5	Pot for setting the HCMP96870 comparator threshold voltage to adjust the ECL clock duty cycle.
R1/4	Pot for adjusting comparator hysteresis.
R23	Pot for adjusting up to a 2V offset voltage at the buffer output for driving the HADC77200.
R22/ 22A	Pot for fine adjustment of offset voltage. Used with pot R23
C25	"Lead" Capacitor for changing the damping factor of the input buffer. This has been set for a flat response.

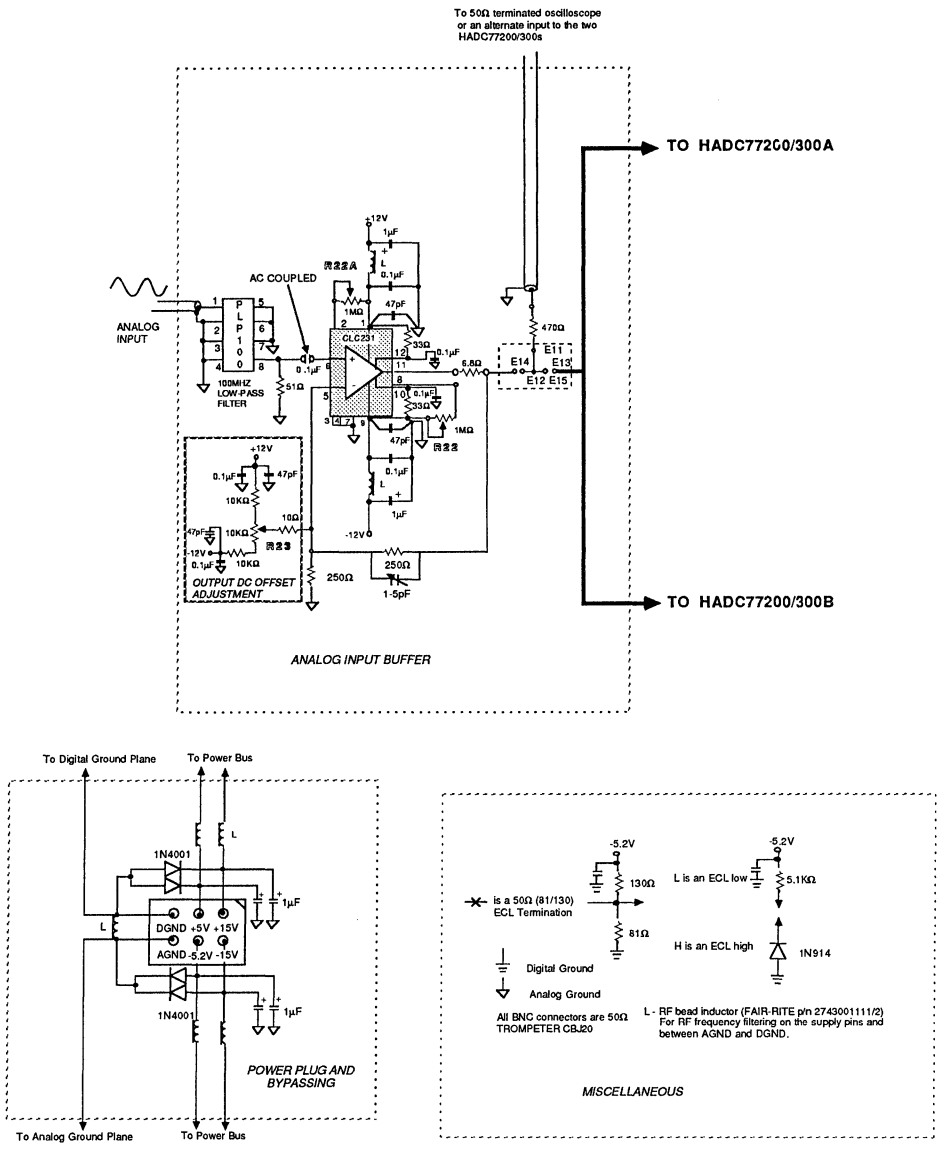


FIGURE 1 - EB103 ANALOG INPUT BUFFER, POWER SUPPLY PLUG AND TERMINATIONS.

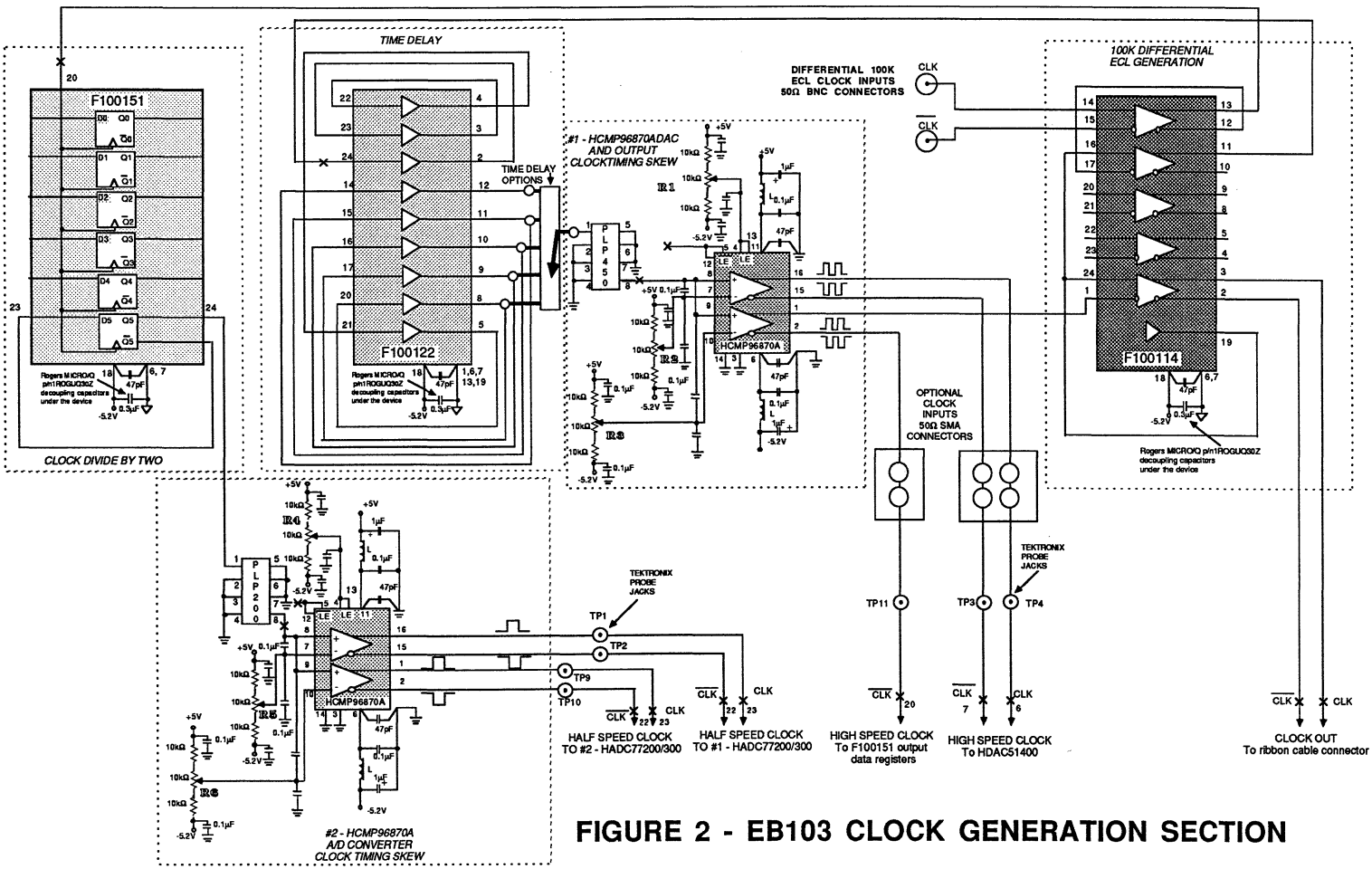


FIGURE 2 - EB103 CLOCK GENERATION SECTION

Honeywell

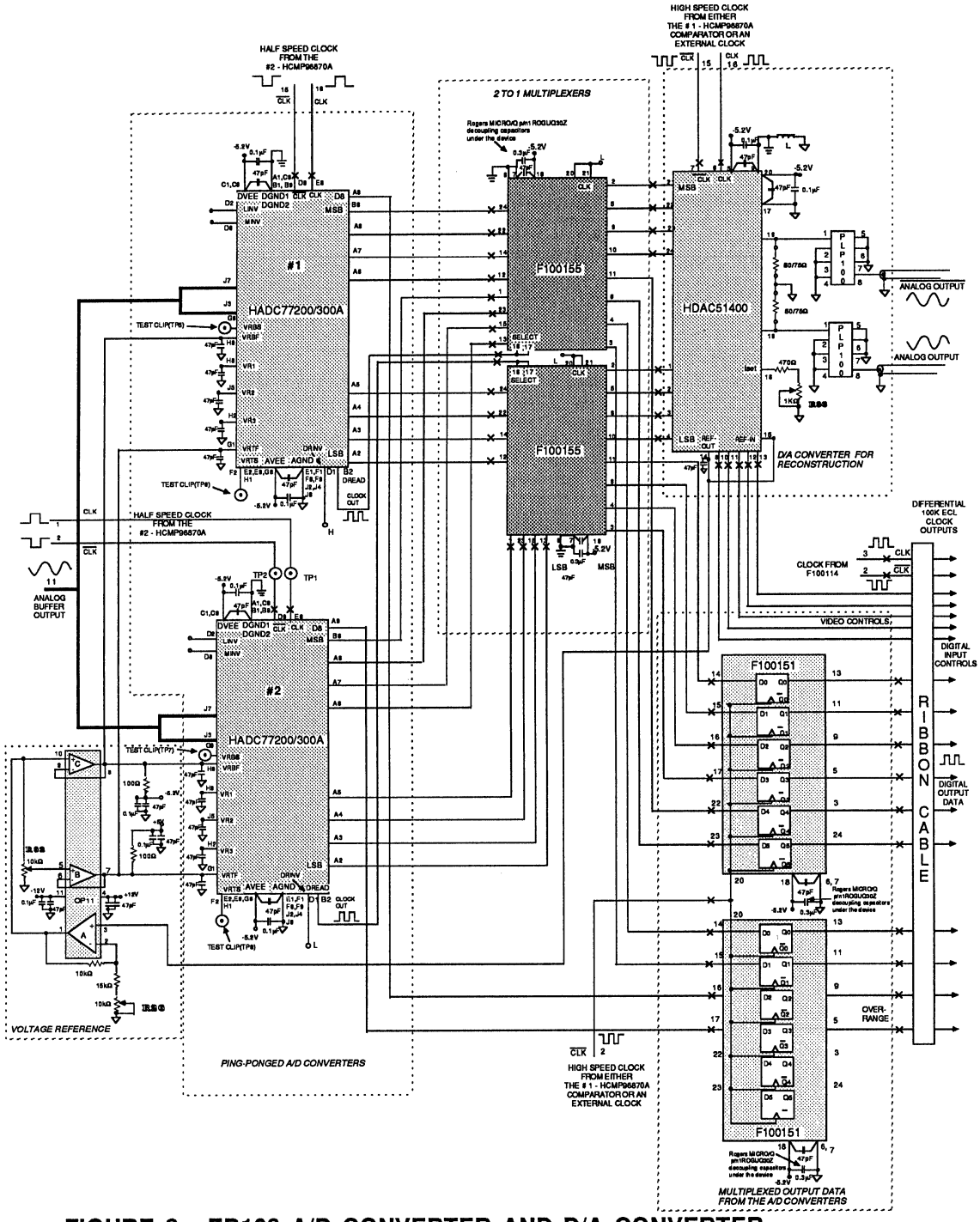


FIGURE 3 - EB103 A/D CONVERTER AND D/A CONVERTER

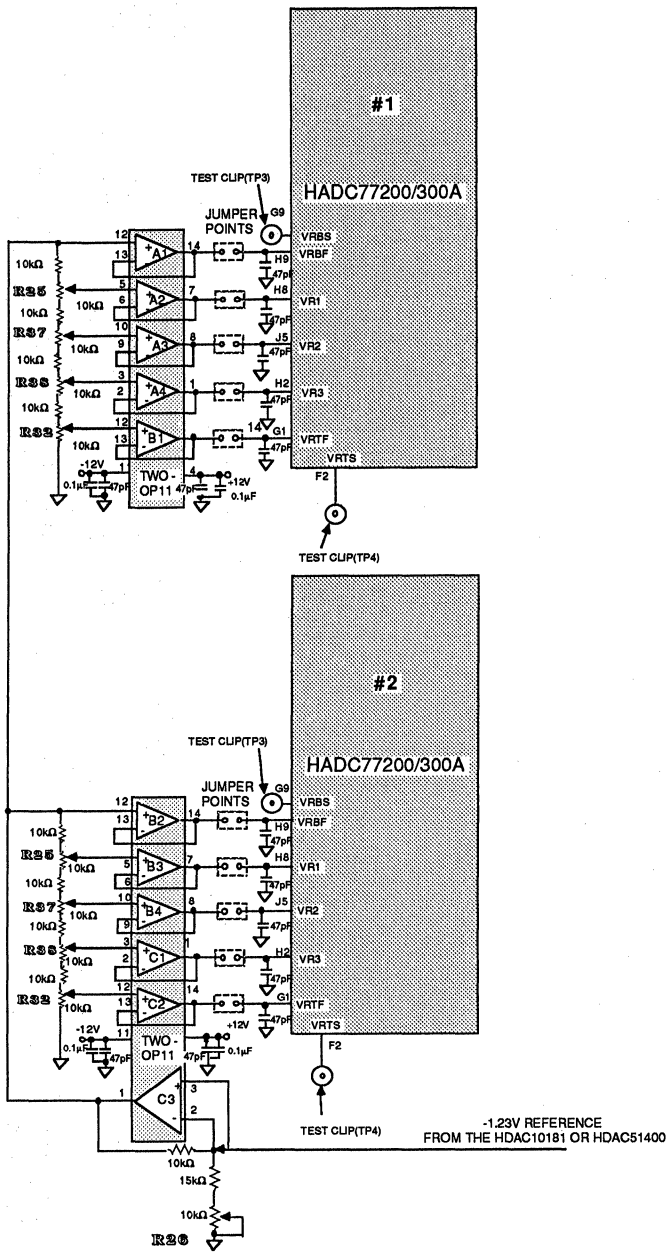


FIGURE 4 - OPTIONAL VOLTAGE REFERENCE CONTROL FOR THE TWO HADC77200/300 A/D CONVERTERS

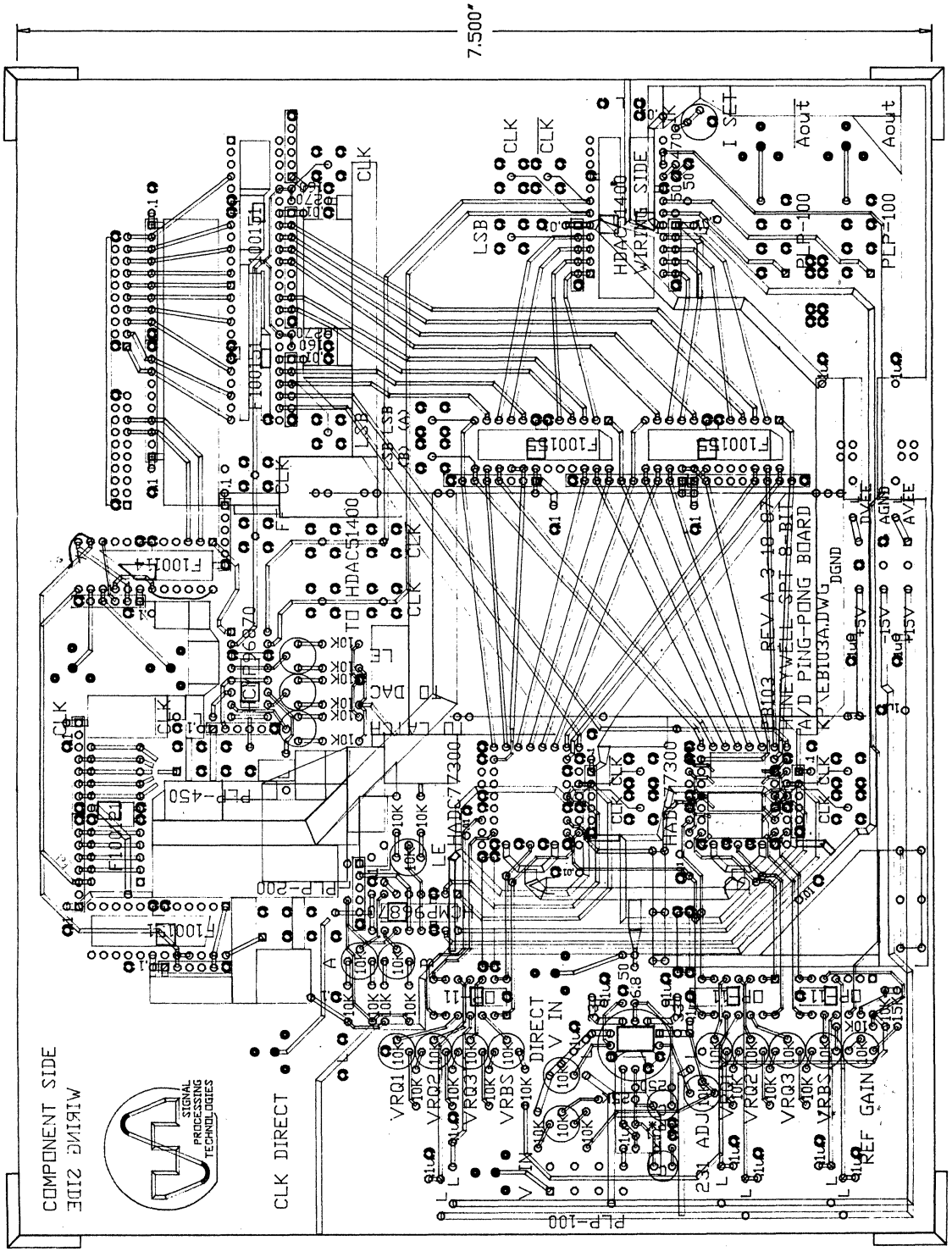


FIGURE 5 - EB103 BOARD LAYOUT

POWER SUPPLY CONNECTIONS

Power to the EB103 is supplied through a nine pin Molex type connector. The supply lines are color coded as shown in Figure5. Connect the wire end of the power supply harness to power supplies as shown by Figure 5 and the silk screen near the mating connector on the PC board itself. The power harness is attached to the board with the bevelled edges and hollow connector alligned to the mating connector.

The power requirements for the EB103 at different supplies is shown in Table 4. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

TABLE 4 - POWER DISSIPATION

EB103A		
Voltage	Current	Power
+15V	.065A	.975W
-15V	.061A	.915W
+5V	.013A	.065W
-5.2V (DVEE)	4.5A	23.4W
-5.2V (AVEE)	.878A	4.56W
		29.9W

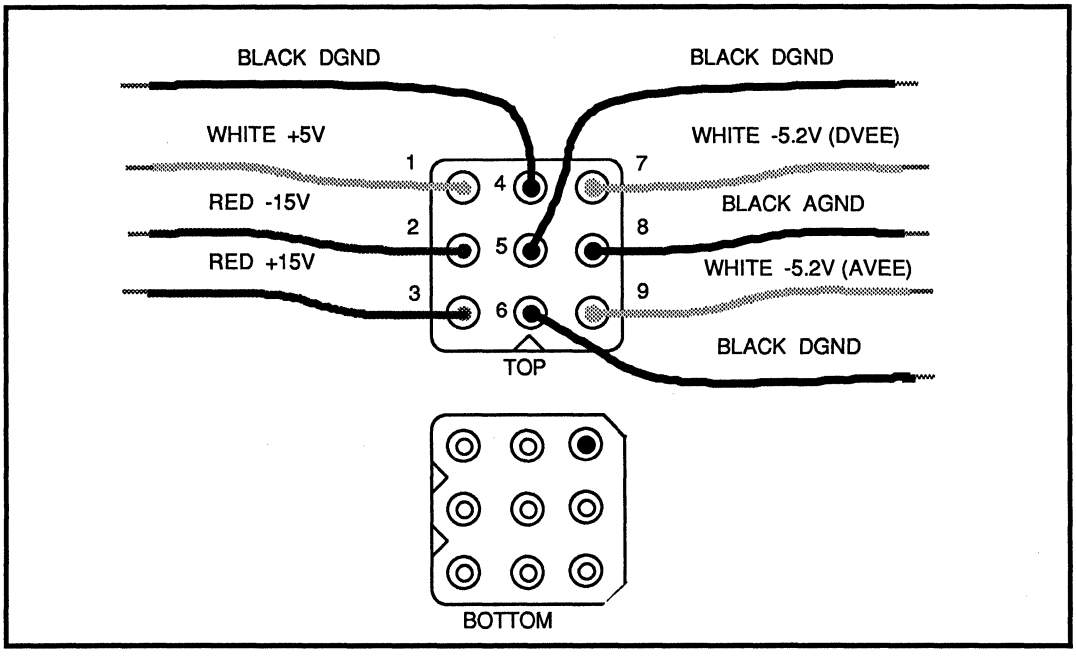
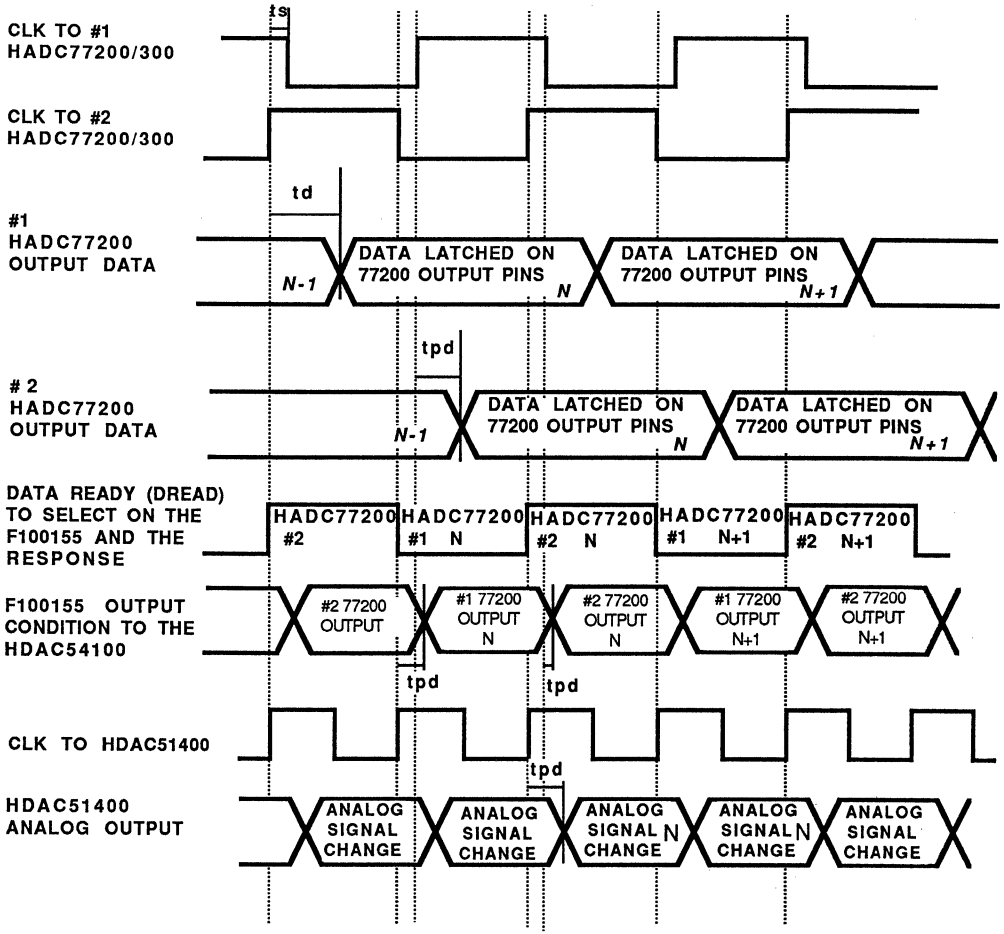


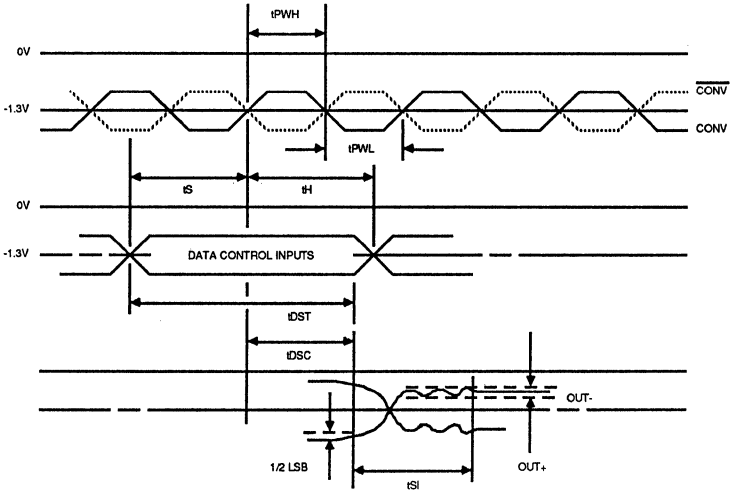
FIGURE 6 - POWER SUPPLY HARNESS CONFIGURATION

EB103 TIMING DIAGRAM

FIGURE 7 - TIMING DIAGRAMS



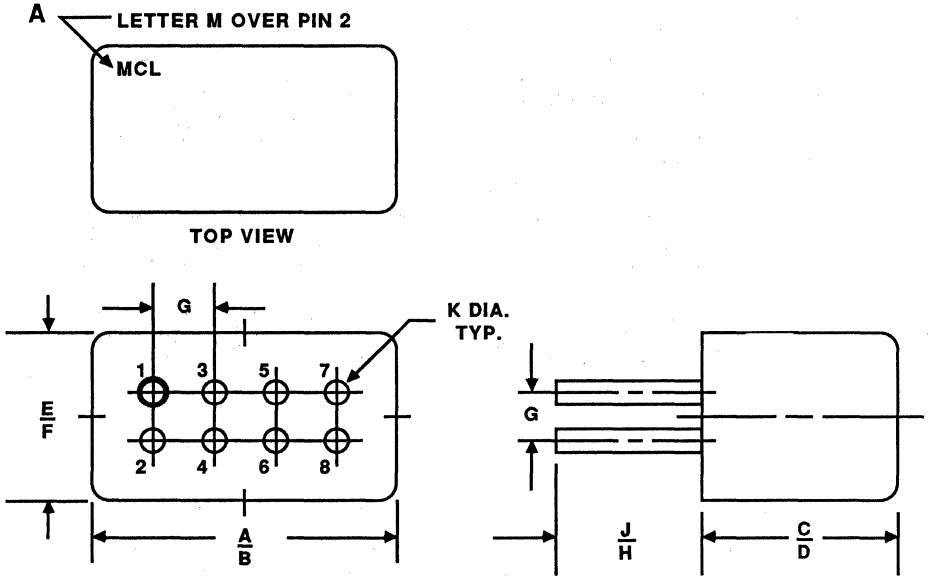
HDAC51400 TIMING DIAGRAM



8

MODEL NO.	PASSBAND, MHz (loss < 1dB) Min.	fco, MHz (loss 3dB) Nom.	STOP BAND, MHz (loss > 20dB) Max.	STOP BAND, MHz (loss > 40dB) Max.	STOP BAND, MHz (loss > 40dB) Min.	VSWR, Passband Typ.	VSWR, Stopband Typ.
PLP-10.7	DC-11	14	19	24	200	1.7	1.7
PLP-50	DC-48	55	70	90	200	1.7	17
PLP-70	DC-60	67	90	117	300	1.7	17
PLP-100	DC-98	108	146	189	400	1.7	17
PLP-150	DC-140	155	210	300	600	1.7	17
PLP-200	DC-190	210	290	390	800	1.7	17

Case no.	A	B	C	D	E	F	G	H	J	K
A01	.770	.800	.385	.400	.370	.400	.200	.20	.14	.031
	19.56	20.32	9.78	10.16	9.40	10.16	5.08	5.08	3.56	.79



NOTE: BLACK BEAD INDICATES PIN 1. PIN NUMBERS DO NOT APPEAR ON UNIT. FOR REFERENCE ONLY.

PIN CONNECTIONS

SEE CASE STYLE OUTLINE DRAWING

SERIES	IN	OUT	GROUND
PLP	1	8	2, 3, 4, 5, 6, 7

FIGURE 8 - LOW PASS FILTERS

PIN FUNCTIONS HADC77200/300

NAME	FUNCTION
DRINV	Data Ready Inverse
LINV	D0 through D7 Output Inversion Control Pin
AVEE	Negative Analog Supply Nominally -5.2V
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
DREAD	Data Ready Output
DO	Digital Data Output Pin 1 (LSB)
D1-D6	Digital Data Output Pin 2 Through 6
D7	Digital Data Output Pin 7 (MSB)
D8	Overrange Output
MINV	D7 Output Inversion Control Pin

NAME	FUNCTION
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRBS	Reference Voltage Bottom, Sense Nominally -2.0V
VRBF	Reference Voltage Bottom, Force Nominally -2.0V
VR1	Reference Voltage Tap 1
AGND1	Analog Ground 1
VIN	Analog Input , can be connected to the input signal or used as a Sense.
AGND2	Analog Ground 2
VR2	Reference Voltage Tap 2
VIN	Analog Input , can be connected to the input signal or used as a Sense.
VRTS	Reference Voltage Top, Sense Nominally 0V
VRTF	Reference Voltage Top, Force Nominally 0V

FIGURE 9 - PIN ASSIGNMENT HADC77200/300

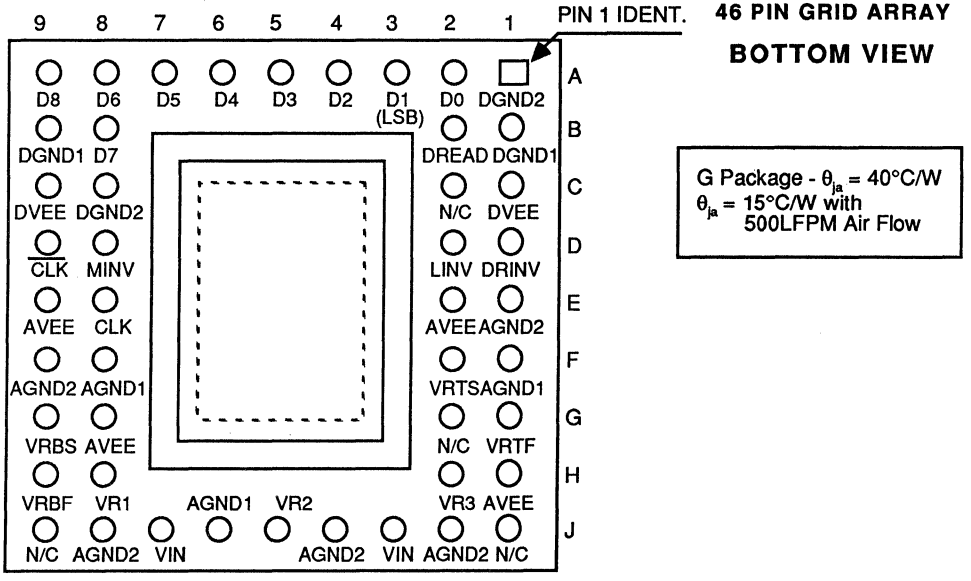
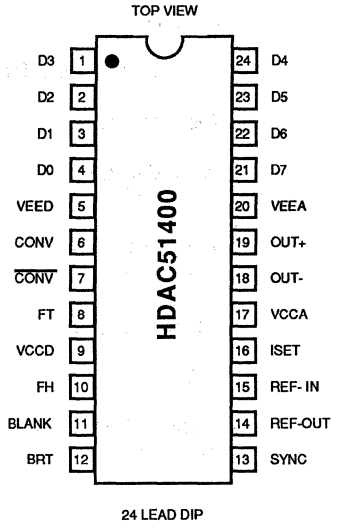


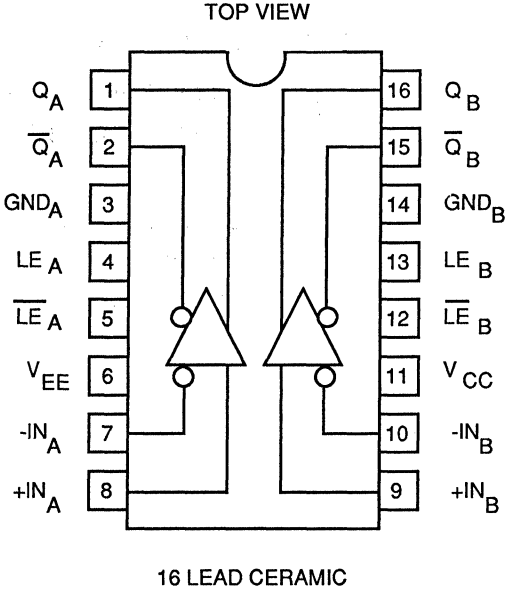
FIGURE 10 - PIN ASSIGNMENTS HDAC51400



PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
REF-IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5

FIGURE 11
PIN ASSIGNMENTS HCMP96870



PIN FUNCTIONS HCMP96870

NAME	FUNCTION
$\overline{Q}_A$	Output A
Q_A	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
$\overline{LE}_B$	Inverted Latch Enable B
LE_B	Latch Enable B
$\overline{GND}_B$	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

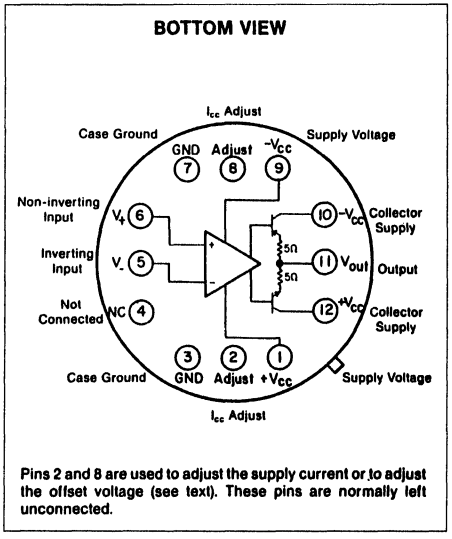


FIGURE 12 - PIN ASSIGNMENT COMLINEAR CLC231

NOTES:

VIDEO DACS AND RASTER GRAPHICS

PAUL M. BROWN

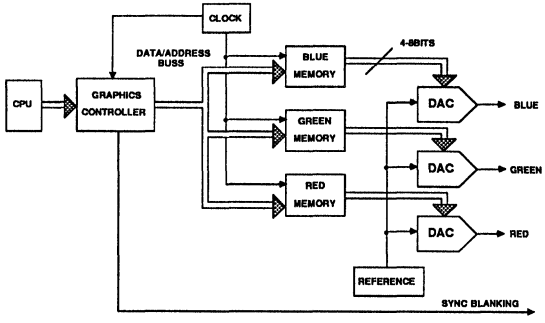
High speed DACs (digital to analog converters) and advances in CRT (cathode ray tube) technology have increased the quality and cost-effectiveness of high resolution displays. The graphics presentations available on todays personal computers and workstations range from good to nearly breathtaking. The 320X200 pixel resolution available on the IBM PC standard color display provides adequate resolution for text and simple graphics. The PC's 640X200 pixel monochrome display provides a much sharper view of text and graphics but without the dramatics of color. The IBM EGA (Enhanced Graphics Adapter) display offers color resolution to 640X350 pixels. State-of-the-art workstations, on the other hand, can achieve resolutions of over 2048X2048 pixels and palettes of nearly 17 million colors resulting in clarity rivaling 35mm film. The increasingly wide spread usage of computer terminals, personal computers and workstations for such diverse applications as word processing, desk top publishing, computer aided engineering, mechanical drafting, solids modeling and the design of integrated circuits has heightened the demand for high quality, reasonably priced graphics displays. The availability of high speed monolithic video DACs is helping to pave the way toward lowering the cost and increasing the performance of high resolution displays.

HOW VIDEO DACS ENTER THE PICTURE

The basic block diagram of a raster scan graphics system (Figure 1) has not changed dramatically in recent years. Previously, expensive laser trimmed hybrid DACs, large amounts of discrete logic and single port RAM were necessary to implement the various functions. This made high resolution graphics systems bulky, power hungry, expensive and unreliable. Now, high speed integrated circuits containing both analog and digital functions make small, efficient, reliable, reasonably priced high resolution graphics systems possible. A graphics system designed today would contain, in addition to the main processor, a graphics controller, high speed RAM, a logic array for glue logic and one or three video DACs (depending on whether the application is monochrome or color).

Graphics controllers range in function from relatively simple screen-refresh controllers, such as the Motorola 6845, to dedicated custom graphics processors. Screen-refresh controllers supply the SYNC and BLANK signals and control the flow of data between the CPU, screen buffer RAM and the video DAC. The speed and resolution of this type of controller is limited by the amount of overhead that the CPU must bear. This configuration is most frequently used in low end workstations and PCs with screen resolutions ranging from 320X200 to 1024X512. Dedicated graphics processors contain specialized instruction sets for graphics and require little CPU support. This type of architecture is found in the highest performance graphics systems.

Figure 1.Typical Raster Scan Graphics System



Reprinted from EDN, September 3, 1987

The image is made of pixels or dots on the screen (Figure 2). The graphics controller supplies the DAC with a digital word for each pixel in the display. Typically, the electron beam in the CRT scans across the screen in non-interlaced lines from left to right and top to bottom under the control of the horizontal and vertical SYNC and BLANK signals. The CRT is scanned one line for each pixel row in the vertical direction. As the beam scans from left to right across the face of the CRT, the video DAC receives one digital word for each pixel in the line. The refresh rate is the number of times in one second that all of the pixels in the display are redisplayed. It is easy to see that the rate at which the DAC must convert digital words to analog intensities depends upon the number of pixels per line (horizontal resolution), the number of lines (vertical resolution), the horizontal and vertical retrace (flyback) time and the refresh rate.

Figure 3 plots the DAC bandwidth (also called update rate) required for various common display resolutions. These bandwidths are calculated assuming a 60Hz refresh rate and that 30% of each frame time (the time it takes to scan one screen i.e. 1/60 of a second) is used for horizontal and vertical retrace. Another way to measure the required DAC performance is by available pixel time. The pixel time is the period during which the DAC is presented with a digital word and it's output must change to the analog value of that word and illuminate the pixel. Figure 4 illustrates the approximate pixel times for various resolutions. It is important to understand that a video DAC will not settle to its rated accuracy during a pixel time but will ring above and below this level at a very high frequency. The phosphor and the human eye will serve as a low pass filter and average out these variations. The most critical concern is, therefore, the rise time of the DAC output not the settling time. A fast rise time maximizes the illumination of each pixel during the pixel time.

Figure 2. Raster Display

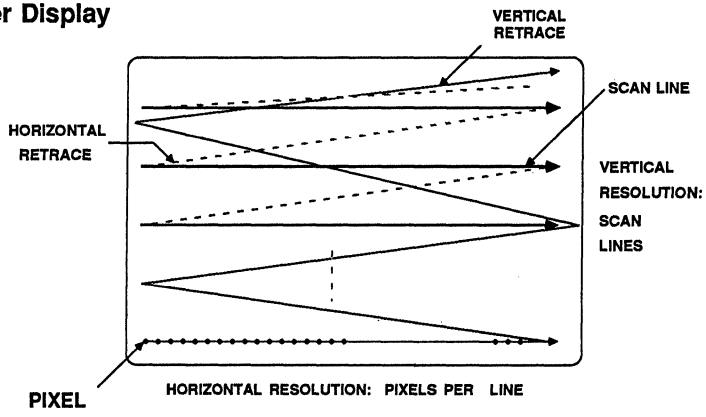
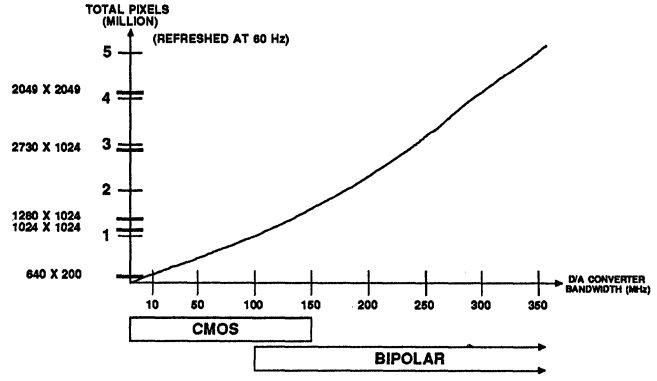


Figure 3. DAC Bandwidth vs. Resolution vs. Technology



Not only must the DAC be very fast, it must also drive a one volt signal into a doubly terminated 50 or 75 ohm load (actual impedance 25 or 37.5 ohms). Figure 5 illustrates a composite video waveform as described in the EIA RS-343 specification. The SYNC and BLANK levels are not processed through the DAC in all applications. The standard waveform (not including the 10% over bright level) is 1Vp-p which is commonly expressed as 140 IREs. An IRE,then, has a value of 7.14 mV.

The notable levels of the composite video waveform are SYNC, BLANK (the level applied during retrace and is also called "blacker than black"), REFERENCE BLACK (the darkest color), REFERENCE WHITE (the lightest color and is also called "force high") and 10% OVER-BRIGHT (sometimes called "whiter than white"). The 10% OVER-BRIGHT level is used for cursors, etc. where a large contrast is necessary with any color, even white. The portion of the waveform between reference black and reference white represents the gray scale for monochrome or potential hues for a color system. The number of discrete levels in this region depends upon the resolution of the DAC. Low end systems will use as few as 4-bits (16 levels) while high end systems intended for solids modeling applications may require 10-bits (1024 levels). Although tremendous performance is required from the DAC, it is not the only limitation on achievable resolution.

Figure 4. Pixel Time vs. Screen Rsolution

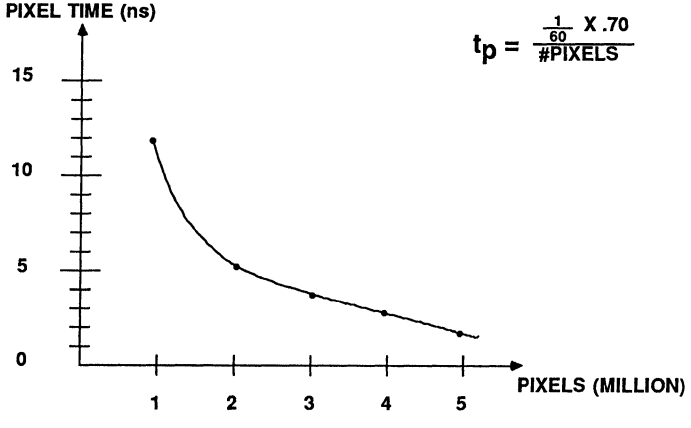
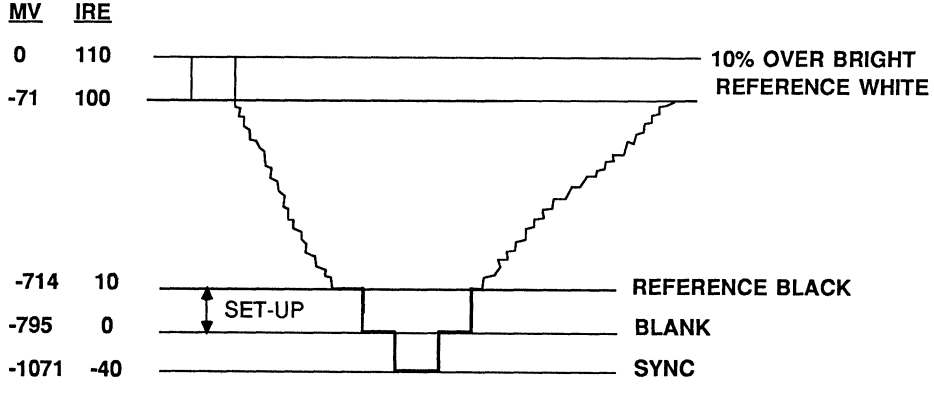


Figure 5. RS-343-A with 10 IRE Set-up



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THE CRT

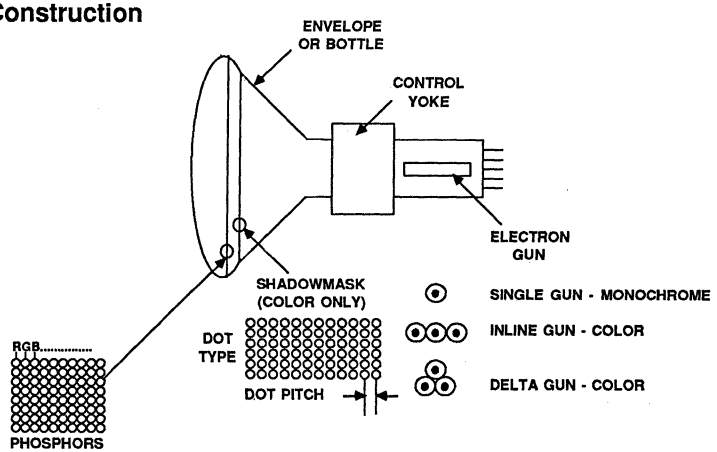
No matter how many bits of resolution or what the data rate, the graphical representation of the data depends upon the display device. The cathode ray tube or CRT is the most prevalent display technology available today. This is especially true for high resolution or color displays. The CRT (see Figure 6) consists of an evacuated glass envelope or bottle that contains an electron gun, a shadow mask (for color) and a glass surface coated with phosphors. A coil, the control yoke, is usually supplied as an integral part of the CRT. The yoke controls the deflection of the electron beam as it travels from the electron gun(s) to the phosphor coated screen. The delta gun configuration, popular in the past, requires deflection control elements that need periodic alignment. The in-line-gun, which does not require adjustment, has become the electron gun of choice in almost all applications today.

The yoke becomes a critical element for refresh rates above 40Hz due to the heat generated by the increased power necessary to drive the yoke and the back-emf that can cause arcing. A typical yoke has an inductance of 300µH and requires about 6A of drive current. The back-emf is on the order of 1200 volts. State-of-the-art yokes designed for higher resolution applications feature inductance of less than 100µH but require between 10 and 20A of drive current. The skin effect, however, increases the effective series resistance (and therefore the power dissipation) of the coil at high scan rates. Heating of the coil at higher drive currents can be minimized with the use of Litz wire. The multiple strands of Litz wire maximize the skin thickness thus reducing the effective series resistance of the coil. The lower inductance minimizes the back-emf and thus reduces the problem of arcing.

The flyback or retrace time becomes increasingly critical with higher resolution displays. The more lines of vertical resolution, the more retrace periods there are. The total time taken for horizontal and vertical retrace directly reduces the time available for writing data. This reduces each pixel time and increases the data rate required for the analog to digital converter. Typical horizontal retrace times range from 2 to 7µs per line while vertical retrace takes between 500 to 1000µs depending on display resolution and CRT design.

The most critical elements in determining CRT resolution are the beam spot size and the shadow mask. For very high resolution displays, a shadow mask dot pitch of less than .20mm is required. The phosphors on the face of the CRT are arranged in groups of red, green and blue (RGB). The electron beams from the guns are focused by the shadow mask to strike the appropriately colored phosphor. The shadow mask also insures that as the beam traces across the screen, the beam from each gun strikes only the correct color phosphor. As resolution increases, the spot size gets smaller. The smaller spot size requires more power to focus the beam and a more powerful beam to maintain the same intensity. This generates more power dissipation and more heat. The spacing between the openings on the shadow mask must also be reduced which makes the shadow mask more fragile. Only 10-20% of the beam energy strikes the phosphor. The balance of the beam heats the shadow mask causing it to bow out or dome. This mechanical deformation of the shadow mask will change the focus and blur the image. This is most apparent for the larger screen sizes. Keeping the gossamer- like shadow mask stable with localized heating from the electron beams, changes in ambient temperature and mechanical shock and vibration becomes extremely difficult. The only practical solution can be to reduce the size of the display in order to increase the mechanical strength of the shadow mask.

Figure 6. CRT Construction



VIDEO DACs

The current line-up of monolithic video DACs meets the challenge of today's high resolution graphics displays with a combination of ultra high speed process technologies and advanced architectures. The process of choice for very high speed video DACs is oxide isolated bipolar ECL. Small on-chip components reduce parasitic elements such as stray capacitance allowing high speed performance at reduced current levels. This in turn permits more circuitry to be integrated on a chip from both a die size and a power dissipation perspective.

Many of the new video DACs, such as the HDAM51100, have on chip color palettes including both address and data registers. Other possible architectures, such as found on the HDAC51600, include on-chip data multiplexers that can interleave several banks of relatively slow TTL memory into a very fast DAC to achieve the desired throughput. Having the faster circuitry such as the color palette or the multiplexer on chip with the DAC eliminates the stray capacitances due to interchip connections. Also, the additional circuitry is fabricated on the same fast process as the DAC. All logic swings and timing will be matched and tuned for the highest performance. The cost of this higher level of integration is the loss of architectural freedom for the designer and the possible difficulty of upgrading the system later without a major revision.

Raster graphics applications can be roughly broken down into low, medium and high pixel resolution which translates directly into DAC bandwidth (update rate). Within these categories, the DACs can be sorted according to their bit accuracy. Recall that a 4-bit and an 8-bit DAC operating at a given MWPS (million words per second update rate) in a particular application will produce the same display (pixel) resolution. The 8-bit converter will, however, offer more shades of gray or more possible colors. The chart, Figure 7, lists the available monolithic video DACs, their speed, accuracy, process and special features.

Figure 7.Current Video DAC Products

Resolution	Speed MWPS	Process	Part Number	Comments
4-BITS	100	Bipolar	HDAC34020	Registered Triple DAC
	200	Bipolar	HDAC34010	Registered Triple DAC
8-BITS	100	Bipolar	HDAM51100	Registered DAC, 512 x 8 Color Look-Up with Iata I/O
	200	Bipolar	HDAC97000	
	250	Bipolar	HDAC51600	Registered Data and Controls, Ref, 5:1 or 4:1 Data MUX
	275	Bipolar	HDAC10180A	Registered Data and Controls
	275	Bipolar	HDAC10181A	Registered Data and Controls, Reference
	400	Bipolar	HDAC51400	Registered Data and Controls, Reference

VIDEO DAC - CRITICAL PERFORMANCE PARAMETERS

SPEED - The DAC that is selected must be able to comfortably handle the required data rate with variations in power supply voltage and logic swing over the ambient temperature in which it must operate.

RISE TIME - The output of the DAC must be able to reach the intended analog value in a fraction of a pixel time. It is not important that the output settles to the final value due to the filtering effect of the phosphor and the human eye. The pixel should be illuminated at full intensity for the largest fraction of a pixel time possible.

GLITCH ENERGY - Output spikes (glitches) are a highly undesirable manifestation in any DAC and especially so in high resolution video applications. Glitches generally occur at major carries (1/4, 1/2, 3/4 and full scale) and appear as intensity variations on the screen. The magnitude of glitches is usually specified in terms of "glitch energy". This is a measure of both the amplitude and duration of the spike. A great deal of effort has gone into designing "glitch free" DACs. Some DAC architectures use special circuitry or adjustments to reduce or eliminate glitches while others are inherently "glitch free". The Honeywell line of video DACs has the lowest glitch energy in the industry.

POWER DISSIPATION - Power dissipation is important for several reasons. High power dissipation means the DAC will have a higher die temperature. This can lead to performance degradation at higher ambient temperatures and increase the load on the system power supply. Cooling will have to be provided and may require PC board layout considerations, heat sinks or forced air. (See AN108 for more information on thermal design). Many times, however, the only way to achieve the desired performance is to bite the power dissipation bullet.

RESOLUTION - The resolution of the DAC will determine the possible levels of intensity (monochrome) or the number of colors for the display. In the past, 4-bits was considered adequate. Now, most new designs are being done with eight or more bits. Solids modeling applications generally require eight to ten bits. More bits of resolution will require a correspondingly larger amount of high speed memory for support.

LOGIC COMPATIBILITY - The fastest DACs will require ECL logic to drive them at their rated speed and will therefore have ECL compatible logic inputs and require ECL power supplies. In these very high speed applications, all logic interconnections must be made using controlled impedance techniques such as microstrips or striplines to avoid undesirable reflections (ringing). Ringing caused by impedance mismatches can easily cause erroneous logic states to be sensed and will reek havoc with a high resolution display. Multiplexed DACs like the HDAC51600 allow up to five banks of relatively slow and inexpensive TTL memory to be multiplexed into a high speed DAC.

ANALOG OUTPUT DRIVE - Most monolithic video DACs will directly drive doubly terminated 50 or 75 ohm loads (25 or 37.5 ohms actual load). As speed increases, the improved bandwidth of the 50 ohm system becomes more attractive. This means that the DAC must be capable of driving a 25 ohm load.

EB104 EVALUATION BOARD INCLUDES HADC574Z 12-BIT A/D CONVERTER AND HDAC7545A 12-BIT D/A CONVERTER

Craig Wiley, Senior Applications Engineer

FEATURES:

- Provides operating environment for HADC574Z or HADC674Z and HDAC7545A Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold Amp and Output Op Amp IC's
- Unipolar or Bipolar Operation

APPLICATIONS:

- Evaluation/Comparison of HADC574/674Z Converters
- Evaluation/Comparison of HDAC7545A Converters
- System Development
- Data Acquision Systems
- Bus Structured Instrumentation
- Process Control Systems

GENERAL DESCRIPTION

The EB104 Evaluation Board fully demonstrates the capabilities of Honeywell's HADC574/674Z and HDAC7545A 12-bit data conversion products. All of the basic power supply connections, controls lines and external components are included. The board can operate in an analog input/output fashion utilizing both A/D and D/A devices, or the devices can be operated separately. Unlike most laboratory breadboarding, the ground-planed PC board provides the necessary low-noise evironment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins. When considering the HADC574/674Z or HDAC7545A for system design, the EB104 Evaluation Board provides a flexible, high performance evaluation vehicle.

The EB104 is supplied with an HADC574ZBCJ and an HDAC7545AACD. It will support all 574/674 and 7545 type devices.

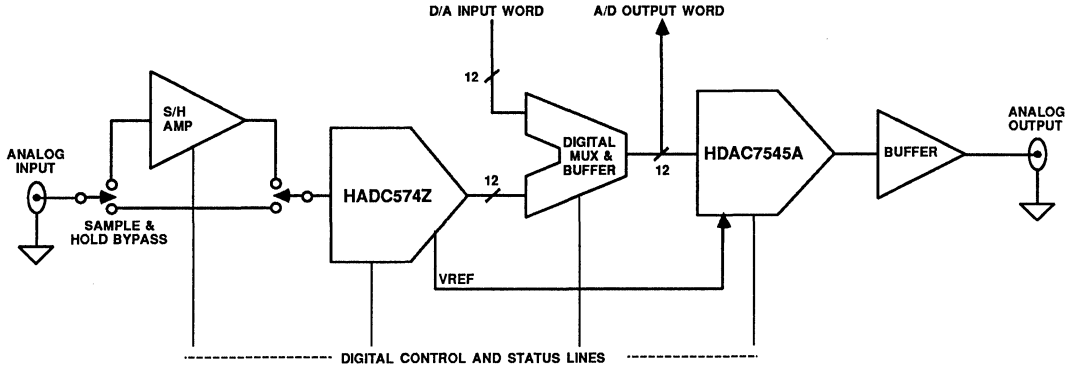


FIGURE 1 EB104 BLOCK DIAGRAM

EB104 GENERAL INFORMATION

The EB104 Evaluation Board is a fully assembled and tested circuit board developed to aide in the evaluation of Honeywell's HADC574Z or HADC674Z and HDAC7545A. A Power supply cable is supplied with the board and requires connection to +5V, +15V, and -15V. Standard BNC connectors facilitate analog input and output and 26 pin ribbon connectors provide digital interfacing. This document, along with the HADC574/674Z and HDAC7545A data sheets, is designed to serve as an operating guide.

The EB104 circuitry consists of three main sections: the Analog/Digital Conversion Section, the Multiplexer/Buffer Section, and the Digital/Analog Conversion Section.

THE A/D CONVERSION SECTION

The heart of this section is the on board HADC574Z or optional HADC674Z 12-bit A/D converter. The HA2425 sample and hold amplifier can support the A/D and can be replaced by several other types of S/H amps. Jumper pins allow the the S/H amp to be connected or bypassed. When connected, the S/H amp samples the analog input signal and outputs the it to the HADC574/674Z. When bypassed, the analog input is applied directly to the HDAC574/674Z. In either case, the 10V or 20V analog input of the HADC574/674Z can be selected with jumper pins. Another set of jumper pins allow the HADC574/674Z to be configured for either unipolar or bipolar input conditions. Trim potentiometers are used to zero the S/H amp offset voltage and trim the HADC574/674Z offset and gain values.

Control and status of the HADC574/674Z and S/H amp is facilitated by the digital control I/O ribbon connector. For convience, jumpers can be used at the ribbon connector to tie particular inputs high or low. Additionally, a jumper can be connected between the HADC574/674Z's STATUS output and the S/H amp's S/H input; this automaticly provides the appropriate "Hold" command upon a user-initiated Convert command.

With the proper input control logic conditions, the HADC574/674Z can ouput data in one 12-bit word or two 8-bit words. When using the 8-bit mode, the EB104 has jumper pins that allow the appropriate connections between HADC574/674Z data output pins.

The 12 output data bits of the HADC574/674Z are fed to the Multiplexer/Buffer Section.

THE MULTIPLEXER/BUFFER SECTION

The main purpose of this section is to select input data for the D/A converter. It allows selection of either the A/D converter's output or user-supplied data from the data input ribbon connector. Secondly, it provides buffering between the input and output ribbon connectors and the data conversion IC's.

The multiplexer/buffer section consists solely of three 74LS157 logic IC's which are quad 2-to-1 data selectors/multiplexers. Control inputs (SELECT and STROBE) are available at the control I/O ribbon connector.

THE D/A CONVERSION SECTION

This section consists of an HDAC7545A and two OP17 op amps used for output buffering. Other types of op amps can be used as well. Again, jumper pins allow selection of output configuration: in unipolar output mode, one op amp is used, and in bipolar output mode two op amps are used. Each op amp has a trim potentiometer to null input offset voltage. The HDAC7545A has trim potentiometers to adjust the zero and full scale output.

EB104 PHYSICAL DESCRIPTION

The EB104 PC board is a 5 by 7 inch, Epoxy double-sided, copper-clad printed circuit board. All components and sockets are mounted on the top side, with the exception of the analog input/output BNC connectors which are mounted on the bottom side. Digital and analog ground and all three power supplies are connected through a single 6-pin keyed Molex power connector, for which a mating power supply cable is included with the board. For digital input and output, three 26-pin ribbon connectors are mounted. One is used for data word input, another for data word output, and the last for digital control and status. All IC's are socketed to facilitate re-selection of components, if so desired. Jumper posts on the top side, jumpered by Berg type jumpers, allow the selection of circuit options.

EB104 OPERATION

CAUTIONS

1) When handling the PC board or any of the devices use procedures necessary for protection against electrostatic discharge or device damage may result.

2) No voltages or forced currents should be applied to the EB104 prior to application of power supplies or devices may be damaged. Analog and logic signals should be applied after (or during) power up and removed before (or during) power down.

USING PRE-CONFIGURED SETUP

The EB104 is pre-configured and ready to operate as delivered with no adjustments or modifications needed. Requirements for operation are limited to power supplies, an analog signal source and an oscilloscope. The jumper-programmed function options are pre-set to provide the following conditions:

a) S/H Amp bypassed
b) A/D converter in -10 to +10 V bipolar input operation mode.
c) A/D converter in free-run operation, self-generating convert command
d) A/D converter in 12-bit conversion, 12-bit output mode.
e D/A converter input from A/D converter output.
f) D/A converter in -10 to +10V bipolar output operation mode

To operate the board using this pre-established configuration, perform the following:

1) Connect the power supplies as outlined in the following section. Apply power.

3) Apply an analog signal into BNC connector jack J5, ranging between -10 and +10 volts.

4) Connect oscilloscope to BNC connector jack J6 to observe the reconstructed analog signal. Signal amplitude will range between -10 to +10 volts.

POWER SUPPLY CONNECTION

Power is supplied through the leaded Molex connector as detailed in Figure 2. Ensure that the beveled edges of the male and female connectors are aligned prior to coupling. Digital and Analog Ground should be connected together at the power supplies to provide maximum noise isolation. The connectors should be coupled and supplies connected prior to turning on the power supplies. With the provided components, the approximate power supply current consumption is:

+5 Volt supply: 16 mA
+15 Volt supply: 16 mA
- 15 Volt supply: 15 mA

Total power dissipation is therefore about 550 mW. When evaluating 574/674 type devices from manufactures other than Honeywell, the +5V supply current will increase to approximately 28 mA, the +15V supply to 22 mA, and the -15 V supply to 45 mA. In this case the total power dissipation will be about 1.15 Watts.

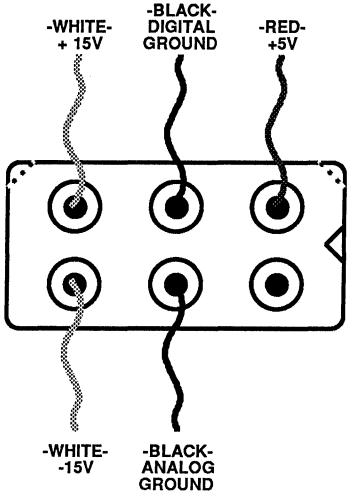


FIGURE 2
POWER SUPPLY CONNECTION

Leaded Power Connector, Top View

8

ANALOG/DIGITAL CONVERSION SECTION

OPTIONAL SAMPLE/HOLD AMPLIFIER USE

Because of it's capacitive DAC architecture, the HADC574/674Z has an inherent sample/hold function. The EB104 is supplied with an on-board sample/hold amplifier which is bypassed in order to demonstrate this fuction (the Analog Input Jack J5 is tied directly to the HADC574/674Z). The HADC574/674Z's sample/hold function works well with input signal frequencies up to about 5 KHz when using a full scale input. Above this frequency, input slew-rate limiting and aperture uncertainty time may degrade performance.

The discrete sample/hold (S/H) amplifier should be used with the HADC574/674Z when either the input signal frequency is above 5 KHz or when no aperture delay can be tolerated, such as when using the unit for transient sampling. When evaluating 574/674 devices from other manufacturers, the external sample/hold amp will be needed except for very low frequencies. During the conversion cycle, these other 574/674 units perform the successive-approximation directly on the input signal; therefore, the last bit is calculated just before the end of the 25 µS (574) or 15 µS (674) conversion cycle.

Figure 3 shows a simplified wiring diagram of the A/D conversion section. Note that the S/H amp can be inserted in the analog input path or bypassed. Table 1 below describes the jumper post connections for these two conditions.

JUMPER POSTS	S/H AMPLIFIER	
	IN ANALOG PATH	* BYPASSED
E11-E13	OPEN	CLOSED
E12-E14	CLOSED	OPEN
E15-E16	CLOSED	OPEN
E17-E18	OPEN	CLOSED

* EB104 AS DELIVERED

TABLE 1
JUMPER CONFIGURATION
FOR SAMPLE/HOLD UTILIZATION

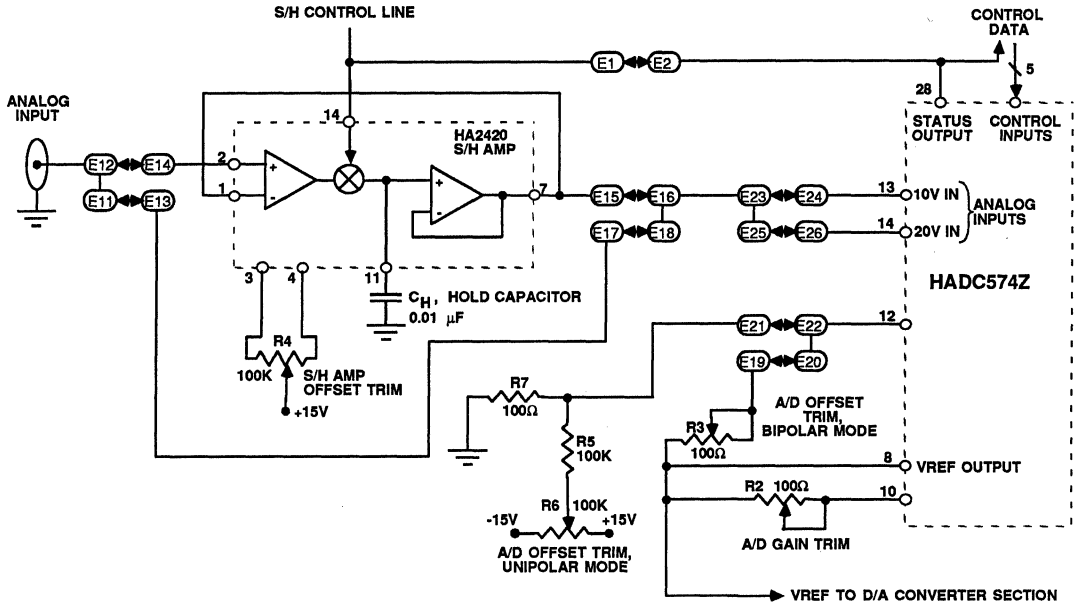


FIGURE 3
SIMPLIFIED WIRING DIAGRAM
OF ANALOG/DIGITAL CONVERTION SECTION
INPUT STRUCTURE

If operation of the EB104 will be with the sample/hold amplifier bypassed, the following section "External Sample/Hold Amplifier Operation" may be skipped.

EXTERNAL SAMPLE/HOLD AMPLIFIER OPERATION

Sample/Hold Amplifier Control

Control of the sample/hold amplifier can be performed by the HADC574/674Z's STATUS output or externally to the EB104. Table 2 describes the jumper configuration for these options. When using the STATUS output, a hold command is generated automaticaly when a convert command is issued to the HADC574/674Z. At the end of the conversion, STATUS returns to zero and commands the S/H amp to again track the analog input. This timing relationship can be seen in figure 4. As discussed in the next section, it is important that the STATUS output stays low long enough for the sample capacitor to charge when using this configuration.

JUMPER POSTS	S/H AMP CONTROL	
	EXTERNAL CONTROL	HADC574Z STATUS OUTPUT
E1-E2	OPEN	CLOSED

TABLE 2
JUMPER CONFIGURATION
FOR SAMPLE/HOLD CONTROL

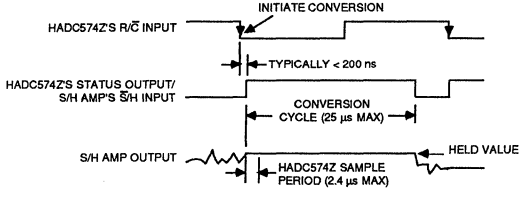


FIGURE 4
TIMING RELATIONSHIP FOR HADC574Z
R/C̄ INPUT, STATUS OUTPUT, AND
SAMPLE/HOLD FUNCTION.

External S/H amp control allows conversion initiation and sample/hold control to be asynchronous. Seperate controls are provided at the R/C̄ and S̄/H pins of Jack J2. Ensure that the Convert command is issued at or after the Hold command.

Hold Capacitor Value Selection

Selection of the hold capacitor value involves trade-offs between hold droop rate and the charge time upon sampling. Larger capacitance values will discharge slower during the hold mode which is useful for long hold times prior to conversion. Smaller capacitance values, however, will better track higher frequency signals during sample mode due to the increased slew rate. Table 3 shows several capacitor values and the approximate associated system performance. The hold capacitor should be of a polystyrene or teflon type to avoid sample hysteresis.

The Manufacture's Typical Values of Table 3 are taken from the HA2425 data sheet. The Calculated Values assume the following:

Maximum Hold Time:
Maximum allowable error = 1/4 LSB
= 1.2 mV (worst case)
t(max) = [Verr(max)]/[droop rate]

Maximum Signal Frequency:
Analog signal is sine wave
Worse-case condition of 20 V_{P-P} input
Maximum frequency limited by slew rate
$f(max) = (\text{slew rate})/2\pi V_P$

Another determining factor in sample capacitor size is aquisition time. Aquisition time is the amount of time needed for the S/H amp to again track the signal following a hold mode. Aquisition time becomes a dominent limitation when working with high sample rates. The minimum capacitor value required for the worse-case conditions using the HADC574Z can be calculated as follows:

The maximum guarranteed conversion period of the HADC574Z is 25 µs (40 KHz) and the maximum HADC574Z aperture time is 2.4 µS; therefore, the maximum S/H window = t(sample period) - t(aperture time) = 22.6 µs. It is assumed that the worst-case input conditions is a 20 KHz square wave at 20 Vpp, which would offer the highest input voltage differencial between samples. Therefore, the minimum slew rate requirement would be 20V/22.6 µs or 0.885 V/µS. Reference to the HA2425 data sheet

HA2425 HOLD CAPACITOR VALUE	MANUFACTURE'S TYPICAL VALUES		CALCULATED VALUES	
	DROOP RATE	SLEW RATE (V/μs)	(1) MAXIMUM HOLD TIME	(2) MAXIMUM SIGNAL FREQUENCY
10 pF	600 mV/s	15	2 ms	120 KHz
100 pF	50 mV/s	15	24 ms	120 KHz
1000 pF	5 mV/s	10	250 ms	80KHz
(3) 0.01 μF	500 μV/s	8	2.5 s	64 KHz
0.1 μF	60 μV/s	0.6	20.2 s	4.8 KHz
1 μF	20 μV/s	0.05	60 s	400 Hz

NOTES: (1) FOR < 1/4 LSB DROOP, Vpp = 20 V
(2) WITH ABILITY TO TRACK SIGNAL, Vpp = 20 V
(3) VALUE SUPPLIED ON EB104

TABLE 3
SAMPLE CAPACITOR SIZE VS. SYSTEM PERFORMANCE

would reveal that the largest hold capacitor value usable for these worst-case conditions is 0.05 μf.

The EB104 comes supplied with a 0.01 μf capacitor, which will track suitably for the highest sample rate as illustrated above for both the HADC574 and HADC674. At 8 V/μs slew rate, a minimum of about 3 μs sample time is required for full scale aquisition in the 0-20 or ±10 V range or about 1.5 μs in the 0-10 or ±5 V range. As seen in Table 3, droop rate is about 0.5 mV/s; maximum hold time prior to conversion is therefore 2.5 seconds if 1/4 LSB accuracy is desired.

Calibration of the Sample/Hold Amplifier

Trim potentiometer R4 is used to zero the offset of the sample/hold amplifier. Although the HADC574/674Z also has a zero adjustment (discussed later), it's range is typically not sufficient to compensate for the external sample/hold amplifier's offset. Gain error in the sample/hold amplifier can be compensated by HADC574/674's gain adjustment. Sample/hold offset trim is performed as follows:

1) Configure EB104 for S/H amp in analog signal path (Table 1).

2) Ground Analog Input (Jack J5) by short circuiting.

3) Connect power supplies.

4) Connect a $\overline{S}$/H clock; a TTL compatible, 50% duty-cycle 10 KHz square wave applied to the $\overline{S}$/H input of Jack J2 is suitable; make sure that jumper connection E1-E2 is open.

5) Using an oscilloscope, measure the voltage between jumper post E15 and analog ground (J5 shield).

6) Adjust trim potentiometer R4 for 0 volts during Hold cycle, which occurs while the $\overline{S}$/H input is logic high.

Repeat of the above calibation procedure is needed only if the S/H amp chip or the hold capacitor is replaced; otherwise, all future "zero" calibration can be performed using the HADC547/674Z calibration procedure discussed below.

HADC574/674Z OPERATION

Input Range Selection

Jumper posts on the EB104 allow configuring the HADC574/674Z for input ranges of 0-10, 0-20, ±5, or ±10 volts. The 0-10 and 0-20 volt ranges use what is called unipolar input operation and the ±5 and ±10 volt range use bipolar input operation. Feedback path of the VREF varies between unipolar and bipolar connections, while one of two input pins, 10V IN or 20V IN, are chosen for ranging. Jumper post programming for the various range options is summarized in Table 4.

JUMPER POSTS	HADC574/674Z INPUT RANGE			
	UNIPOLAR		BIPOLAR	
	0-10 V	0-20 V	±5 V	* ±10 V
E19-E20	OPEN	OPEN	CLOSED	CLOSED
E21-E22	CLOSED	CLOSED	OPEN	OPEN
E23-E24	CLOSED	OPEN	CLOSED	OPEN
E25-E26	OPEN	CLOSED	OPEN	CLOSED

* EB104 RANGE AS DELIVERED

TABLE 4
EB104 ANALOG INPUT RANGE OPTIONS AND JUMPER POST PROGRAMMING

Control Logic Inputs

The EB104 jumper posts are pre-configured to provide 12-bit operation with what is probably the simplest control scheme. Pin R/$\overline{C}$ of Jack J2, which is connected to the R/$\overline{C}$ input of the HADC574/674Z, is used to both initiate the 12-bit conversion cycle and enable the 12 bit output. For the free-running

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 5
TRUTH TABLE FOR THE HADC574/674Z
CONTROL LOGIC INPUTS

operation, as configured, the STATUS output pin of Jack J2 triggers the R/$\overline{C}$ pin. This is discussed further in the next section.

The remaining control pins are tied as follows:

CE = 12/$\overline{8}$ = +5V (Logic High)
$\overline{CS}$ = Ao = Ground (Logic Low)

These above connections result in the chip always being enabled in 12-bit conversion mode with all 12 output bits enabled. The truth logic of Table 5 summarizes the control logic functions. Refer to the HADC574Z data sheet for further information regarding these functions.

Free-Running Operation

By connecting the STATUS output of Jack J2 to the R/C input of Jack J2, the HADC574/674Z self triggers. That is, at the end of a conversion , when STATUS goes to logic low, this automaticly triggers the device for another conversion. Figure 5 shows the resultant wave form of the STATUS line when using the HADC574Z. The HADC674Z gives similar results except that conversion time is 15 µS maximum. Note that the <200 nS STATUS logic low time is not sufficiently long enough for an external sample/hold amp control. The EB104 is pre-configured for free-running operation.

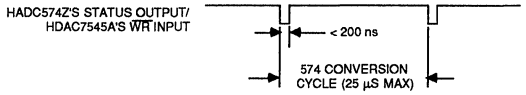


FIGURE 5
STATUS OUTPUT TIMING OF HADC574Z IN FREE-RUNNING MODE

Data Output Options

The HADC574/674Z is capable of outputing a 12-bit conversion result in two 8-bit words (with 4 trailing zeros). To accomplish this, the four MSB output lines are tied to the four LSB output lines as shown in Figure 6. The EB104 has jumper posts to facilitate these connections easily. These connections are summarized in Table 6. Following a conversion, the MSB and LSB words are selected by input pin Ao as indicated in Table 5. For full information on this mode of operation, please refer to the HADC574/674Z data sheet.

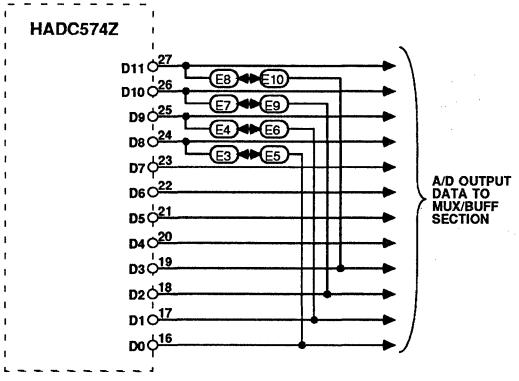


FIGURE 6
WIRING DIAGRAM OF D/A SECTION OUTPUT

JUMPER POSTS	OUTPUT FORMAT	
	* 12 BITS	8-BITS
E19-E20	OPEN	CLOSED
E21-E22	OPEN	CLOSED
E23-E24	OPEN	CLOSED
E25-E26	OPEN	CLOSED

* EB104 AS DELIVERED

TABLE 6
JUMPER POSTS SELECTION
FOR OUTPUT MODE PROGRAMMING

Calibration

The HADC574/674Z is manufactured to have only a few LSB's of zero offset and a fraction of a percentage of full scale error, depending on grade. In addition, inaccuracies in the S/H amp, if used, will contribute to the inaccuracy of the A/D Conversion Section. The EB104 includes trim potentiometers for zero and full scale adjustment to compensate for these errors which are pre-adjusted for the pre-configured operation. Shipping may effect the adjustments and alter the calibration. Re-calibration will be needed when the input range is changed , when the S/H amp utilization is changed, or when any components are replaced in this section.

Calibration involves the adjustment of the devices offset and gain. Adjustment is made so that the output of "zero" (0000 0000 0000) and "full scale" (1111 1111 1111) code values are received when the analog input's negative-most and positive-most values are input. In practice, accurate calibration is acheived by calibrating the "zero" point with an analog input voltage the equivalent of 1/2 LSB above the desired zero setting; the zero trimming is then set between the 0000 0000 0000 and 0000 0000 0001 output transition. Full scale calibration is then acheived similarly with an analog input 1/2 LSB below the maximum range; the gain trimming is then set between the 1111 1111 1111 and 1111 1111 1110 output transitions.

To calibrate the A/D section of the EB104 using the approach described above, use the following procedure:

1) Select S/H amp utilization and input range mode.

2) Apply power supplies.

3) If using S/H amp, adjust zero offset trim of S/H amp if not already done.

4) Apply an accurate programmable voltage source to EB104 Analog Input (Jack J5).

(A suitable method to accomplish this is with a variable power supply in parallel with a digital voltmeter. Voltage setting should be accurate to within 0.5 mV, which is about 1/4 LSB in the 0-10 or ±5 volt range. A potentiometer may be required to divide and trim the input reference voltage. Noise should also be kept low, less than 1 mV if possible. Accuracy of voltage source and level of noise will affect acheivable calibration.)

INPUT RANGE SELECTED	"ZERO" CALIBRATION VOLTAGE	"ZERO" TRIM POTENTIOMETER	"FULL SCALE" CALIBRATION VOLTAGE
* 0-10 V	1.22 mV	R6	9.9963 V
0-20 V	2.44 mV	R6	19.9927 V
±5V	-4.9988 V	R3	4.9963 V
±10V	-9.9976 V	R3	9.9927 V

* EB104 RANGE AS DELIVERED

TABLE 7
HADC574Z CALIBRATION VOLTAGES

5) Connect logic monitor to A/D data output jack J3. (This can be accomplished with a logic analyzer connected to Jack J3 or by determining the logic value of each pin with a voltmeter or oscilloscope.)

6) Set voltage source to zero calibration value indicated by Table 7.

7) Adjust zero trim potentiometer indicated by Table 7. Set to point where flickering occures between 0000 0000 0000 and 0000 0000 0001; both codes should occure equally. (If using a scope or volt meter, monitor pin B0 of Jack J3, the LSB; ensure pin B2-B11 are still zero and not flickering.)

8) Set voltage source to full scale calibration value indicated by Table 7.

9) Adjust gain trim potentiometer R2. Set to point where flickering occures between 1111 1111 1111 and 1111 1111 1110; again equal occurences of code should exist.

The A/D section is now calibrated and ready for use.

Component Selection

The EB104 can be used for the evaluation and comparison of similar component types. In addition to the hold capacitor discussed earlier, both the external S/H amp and HADC574/674Z can be replaced with other devices. The HA2425 supplied on the board can be replaced with an HA2420, AD583, SMP-81, or SHM-IC-1. The HADC574/674Z can also be replaced with alternate pin compatible devices for evaluation and comparison purposes. Athough pin 11 of the HADC574/674Z is not internally connected, -15 volts is supplied to the socket pad for the VEE requirement of alternate, pin compatible devices from other manufacturers.

MULTIPLIER/BUFFER SECTION

This section drives both the Digital/Analog Conversion Section and Data Output Jack J4. Input into this section is selectable from either the Analog/Digital Converstion Section or Data Input Jack J3. This allows the Analog/Digital and Digital/Analog Conversion Sections to be linked and operated together or operated separately. Digital code can be output from the HADC574/674Z through Jack J4, or data can be input directly to the HDAC7545A. All data input or output from this section is buffered. A block diagram of the Multiplier/Buffer Section is shown in Figure 7.

OPERATION

With a logic low into the SELECT input of Control Line Jack J2, the HADC574/674Z output data is selected; a logic high selects the data input into Jack J3. The STROBE input allows input data to be transferred with a logic low condition, and blocks data transfer with a logic high condition. This is shown in Table 8, Multiplexer/Buffer Section Logic Control. A Berg jumper can be used at Jack J2 to tie either the SELECT or STROBE input low (ground).

The Multiplexer/Buffer Section consists of three 74LS157 devices each of which is a quadruple 2-line-to-1-line data selector/multiplexer. The Strobe inputs and Select inputs of the three devices are tied together and controlled by the STROBE and SELECT input pins of Jack J2. Device compensation is achieved with a Q-Pak™ chip capacitor under each device. Pinout of the 74LS157 and it's logic truth table is shown in the appendix.

INPUTS		OUTPUT (12 BITS)
SELECT	STROBE	
H	X	ALL OUTPUTS LOGIC LOW
L	H	DATA INPUT JACK J2 SELECTED
L	L	*A/D CONVERTER OUTPUT SELECTED

*JUMPERED CONDITION AS DELIVERED

TABLE 8
MULTIPLEXER/BUFFER SECTION LOGIC CONTROL

Device Selection

The CMOS equivalent of the 74LS157 can be used in place of the bipolar devices. This will provide the advantage of reduced power supply current, but output drive will be reduced.

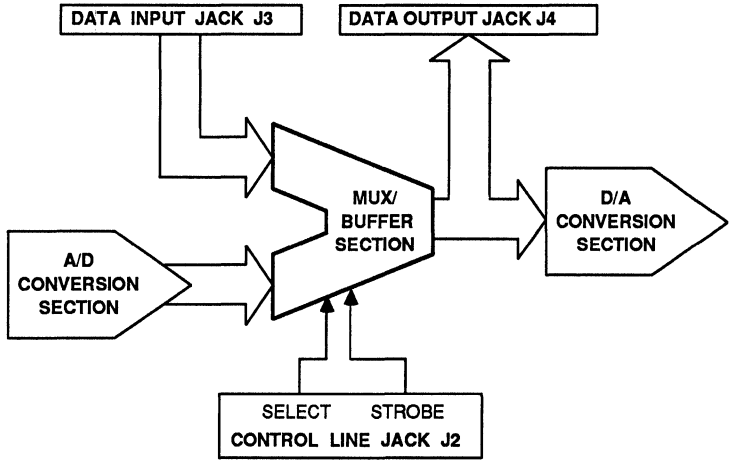


FIGURE 7
MULTIPLEXER/BUFFER SECTION BLOCK DIAGRAM

DIGITAL/ANALOG CONVERSION SECTION

The heart of this section is the HDAC7545A current output digital-to-analog converter. Parallel code received from the Buffer-Multiplexer section is input into it's internal input register and can be latched. The HDA7545A outputs a signal current corresponding to the 12-bit code residing in the input register. The analog current output of the DAC is converted to a voltage by the external op amp(s) in combination with internal resistor Rfeedback.

DATA INPUT AND LOGIC CONTROL

Input logic pins $\overline{CS}$ and $\overline{WR}$ control HDAC7545A operation and are available on the EB104 at the Control Line Jack J4. Pins $\overline{CS}$ and $\overline{WR}$ control the loading of the input register; when both pins are low, data at the input logic pins DB0-DB11 is transferred into the input register. When $\overline{CS}$ and/or $\overline{WR}$ goes high, the input register is locked and retains the last code condition. $\overline{CS}$ and $\overline{WR}$ can be tied low (grounded with Berg jumpers at J4) so that all input codes are immediately converted; this is not a good approach if a smooth continuous output is desired. Commonly, and by pin definition, pin $\overline{CS}$ is used for chip selection and $\overline{WR}$ for writing data into the input register.

The simplest method for loading the HDAC7545A on the EB104 is to ground $\overline{CS}$ with a Berg jumper. Loading the input register is accomplished with a negative pulse on $\overline{WR}$ (100 nS minimum).

In the pre-configured hook up of the EB104, pin $\overline{CS}$ is jumpered to ground and pin $\overline{WR}$ is connected to the STATUS output of the HADC574Z which is in free-run operation. As shown in Figure 9, the typical timing of the HADC574Z and HDAC7545A allows this configuration to function. Output data from the HADC574Z is transferred to the HDAC7545A via the Multiplexer/Buffer section.

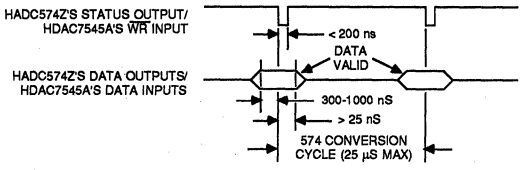


FIGURE 9
TIMING RELATIONSHIP BETWEEN HADC574Z AND HDAC7545A IN PRE-CONFIGURED OPERATION

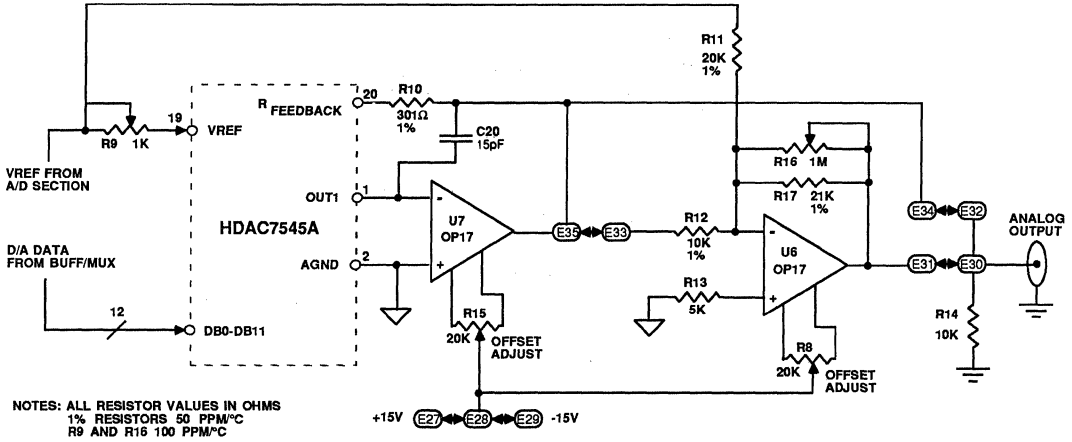


FIGURE 8
SIMPLIFIED WIRING DIAGRAM OF DIGITAL/ANALOG CONVERSION SECTON

OUTPUT MODE SELECTION

Berg jumpers allow the selection of either a unipolar or bipolar voltage output from the Digital/Analog Conversion Section. In unipolar operation, a single op amp (U7) is used in an inverted unity gain configuration to provide an inverted 0 to -10 volt output, corresponding to full scale input codes 0000 0000 0000 to 1111 1111 1111, respectively. In bipolar operation, both op amps (U6 and U7) are used to provide a non-inverted -10 to 10 volt output, corresponding to codes 0000 0000 0000 to 1111 1111 1111; 0 volts results from code 1000 0000 0000. The jumper configuration for output mode selection is summarized in Table 9.

JUMPER POSTS	D/A SECTION OUTPUT RANGE	
	-10 TO 0 V (UNIPOLAR)	-10 TO +10 V *(BIPOLAR)
E30-E31	OPEN	CLOSED
E32-E34	CLOSED	OPEN
E33-E35	OPEN	CLOSED

* EB104 RANGE AS DELIVERED

TABLE 9
EB104 ANALOG OUTPUT RANGE OPTIONS AND JUMPER POST PROGRAMMING

CALIBRATION

The EB104 is delivered pre-calibrated and ready to operate. However, due to vibration during shipment, recalibration may be necessary in order to obtain the 1/2 LSB accuracy achievable with the HDAC7545A. Calibration will again be necessary following any component replacement in the Digital/Analog Conversion Section with few exceptions, and also when changing between unipolar and bipolar modes.

As discussed later in the Trim and Gain Component section, the gain determining resistors used for bipolar operation are of a readily-available 1% accuracy variety. This can represent a 2% gain inaccuracy or an 80 LSB error (out of 4096 LSB's total). Therefore, when adjusting the trimming for a fraction of an LSB, the adjustment is "touchy" and can drift an entire LSB over an ambient temperature change of several degrees Celsius. Refer to the Component Selection section if additional temperature stability is desired.

Calibration Procedure

During calibration, all voltage measurements are taken from the Analog Output Jack J6. For a more accurate calibration, output noise is reduced by disabling the HAD574/674Z and forcing the input conditions through Data Input Jack J3; On Jack J2, jumper pins CE and SELECT to ground which will disable the HADC574/674Z and select input data from Jack J3. Also jumper pins $\overline{WR}$ and $\overline{CS}$ on Jack J2 to ground which will result in continuous conversion.

Unipolar Output Mode Calibration

1) Ensure EB104 is configured for Unipolar Output Mode.
2) Input 0000 0000 0000 into Jack J3.
3) Adjust offset trim potentiometer R15 until 0 Volts is obtained. (2.44 mV represents 1 LSB error)
4) Input 1111 1111 1111 into Jack J3.
5) Adjust Vref gain adjustment R9 until -10 Volts is obtained.

This completes the calibration for unipolar output operation.

Bipolar Output Mode Calibration

1) Perform steps 1 through 3 of Unipolar Output Mode Calibration
2) Disconnect Jumpers E33-E35 and E34-E35; Connect E30-E31.
3) Short pins 2 and 3 of U6 to ground.
4) Adjust offset trim potentiometer R8 until 0 volts is obtained; due to the high gain of the amplifier, it will be nearly impossible to actually obtain 0 volts; adjusting R8 so that the output polarity just changes is sufficient.
5) Connect Jumper E33-E35.
6) Input 0000 0000 0000 into Jack J3.
7) Adjust gain trim potentiometer R16 until -10 Volts is obtained. (4.88 mV represents 1 LSB error)
8) Input 1111 1111 1111 into Jack J3.
9) Adjust Vref trim potentiometer R9 until +10 Volts is obtained.
10) Repeat steps 6 though 9 and readjust if necessary.

This completes the calibration for bipolar output operation.

D/A SECTION COMPONENT SELECTION

Output and Trim Resistors

In conjunction with external op amp U7, the resistance of Rfeedback in series with R10 is used to convert the DAC output current to a voltage. Additionally, in bipolar output mode a summation circuit composed of op amp U6 and external resistors is used to combine Vref with the generated output voltage. Trim resistors are included to adjust for offset and full scale errors in the HDAC7545A, the Vref error, and in bipolar output mode, the resistor ratio error of the gain stage incorporating op amp U6. The component selection for unipolar output mode will be discussed first.

The worst-case gain error tolerance of the lowest-grade HDAC7545A is ±4 LSB or approximately ±0.1%. The maximum error of the Vref, derived from the HADC574, is approximately ±0.1%. Therefore, when using unipolar output mode, the gain adjustment will need to be ±0.2% to cover worst case error. In the HDAC7545A, the resistance of Rfeedback and the resistance into VREF is typically 12.5 KΩ but can be as high as 18 KΩ. For trim purposes, R10 adds to Rfeedback and R9 (potentiometer) adds to the input resistance of Vref. Working out the gain equation using 18 KΩ as internal resistance (worse case) it is found that R10 needs to be 36 Ω minimum and R9 twice the R10 value (minimum) to provide the needed ±0.2% adjustment.

The best control of adjustment and stability for unipolar output operation is achieved by using the resistance values derived above. Even lower values can be used if a better grade HDAC7545A is used and/or VREF voltage is better controlled. Actual values used on the EB104 are larger: R10 is 301 Ω and R9 is 0 to 1000 Ω. These increased values are necessary to allow calibration in bipolar mode as discussed below.

In bipolar mode, the gain stage consisting of op amp U6 is configured to gain and sum Vref and the unipolar output of the DAC; (-1)•(Vref)+(-2)•(Unipolar Out). (Recall that the unipolar output is inverted.) When 0000 0000 0000 is input, the unipolar output is zero and contributes nothing; the output is therefore (-10V)+(-2)•(0)=-10 Volts When 1111 1111 1111 is input, the output is (-10V)+(-2)•(-10V)=+10 Volts. The accuracy of the (-1) and (-2) gains directly affect final accuracy. In addition to the errors discussed in unipolar output operation, bipolar output operation gain error also needs to be considered.

Because of relative ease of availability and to therefore demonstrate a practical circuit, the EB104 is supplied with fixed gain resistors of 1 % accuracy. Therefore, ±2% worst case gain inaccuracies can be expected. The gain adjustment of the (-2)•(Vref) product is first considered. To allow calibration over the maximum ±2% error range, R16 (feedback resistance) consists of a 21 KΩ (1%) resistor in parallel with a 1 MΩ potentiometer; R11 (input resistance) consists of a 20 KΩ (1%) resistor. Working out the gain equations with nominal resistance values, this allows a gain adjustment from -∞ to +2.8% over unity. Considering worst-case resistor values, this leaves 0.8% for compensation of Vref error.

The gain of the (-1)•(Unipolar Out) product is next considered. This product, again due to the summing amp resistor tolerances, can also vary ±2%; this is due to the the 1% tolerance of R12 combined with the trimmed R16. The Error is compensated by the same adjustment made in unipolar operation; by adjustment of R9 to change the HDAC7545A output gain. However, the 0.2% adjustment allowed earlier needs to be increased to ±2% to compensate for summing amp gain error. By working out the gain equations, it is found that increasing R9 to 360 ohms and R9 to about 720 provides the desired range. Practically, however, due to typical values of HDAC7545A Vref and Rfeedback resistance and available resistance values, component values of 301 Ω and 1 KΩ were chosen for R10 and R9, respectively.

Temperature coefficient of the chosen gain determining resistors is 50 ppm and 100 ppm for the fixed resistors and potentiometers, respectively. These, again are readily available values. If the components did drift in opposite directions, calculation shows that 1 LSB error would be imposed with less that 3°C change; practically, however, similar components typically track each other and insignificant change will be noted in the laboratory environment.

Further stability of the Digital/Analog section can be attained by using fixed resistors with lower accuracy tolerance and lower temperature coefficient. The better accuracy will reduce the adjustability needed for the HADC7545A adjustment; this will then reduce the inaccuracies contributed by the external resistance due to internal/external resistor temperature differences and temperature coefficient differences.

Other 7545-Type Devices

Any competing 7545A device may be inserted in place of the HDAC7545A for evaluation. Note, however, that output compensation capacitor C20 will need be increased to the value specified by the manufacturer. Having a very uniquely low output capacitance, the HDAC7545A requires only 15 pF compensation and has a very fast settling time.

Op Amps

The high slew rate OP-17 was chosen for the EB104 to demonstrate the fast settling time of the HDAC7545A. Many other popular op amp types, having the same pin out, can be used instead. Some of these op amps require the opposite voltage polarity on the offset trim potentiometer wiper. The EB104 has Berg jumper posts that allow this polarity change. Please refer to Table 10 for the jumper position for several popular op amps.

JUMPER POSTS	OFFSET TRIM POT VOLTAGE	USED FOR OP AMPS:
E28-E29	-15 V	AD544
E27-E28	+15 V	LF155/6/7 OP07 *OP17

*SUPPLIED ON EB104

TABLE 10
JUMPER POST CONFIGURATION FOR POPULAR OP AMPS

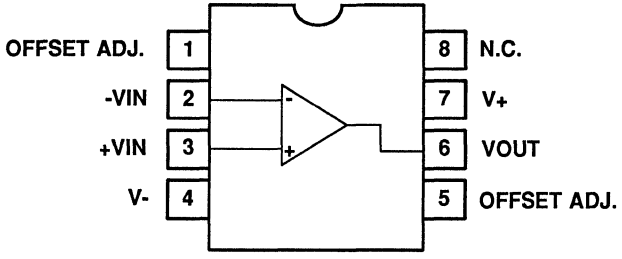


FIGURE 10
OP AMP PIN OUT
TOP VIEW

8

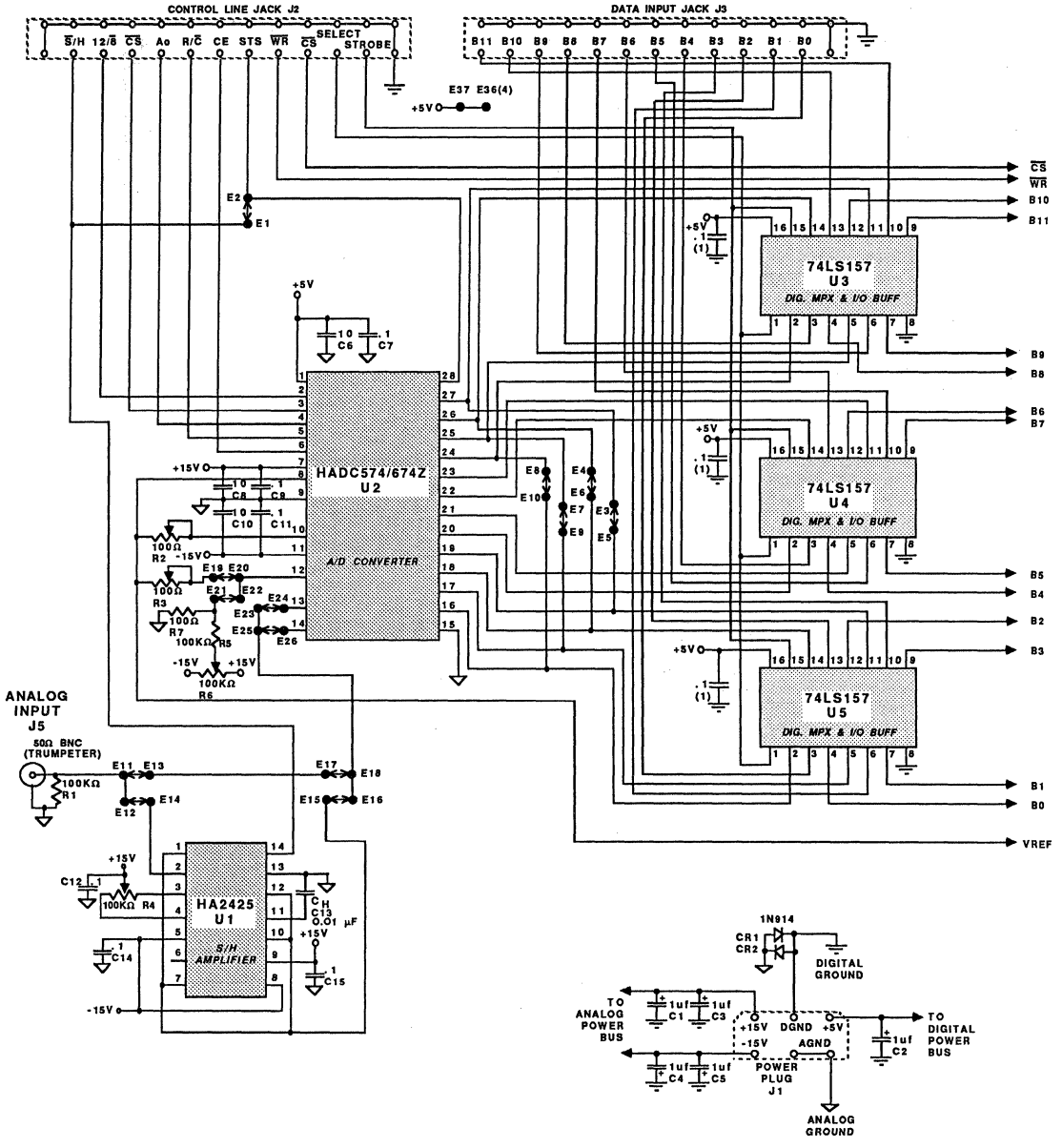
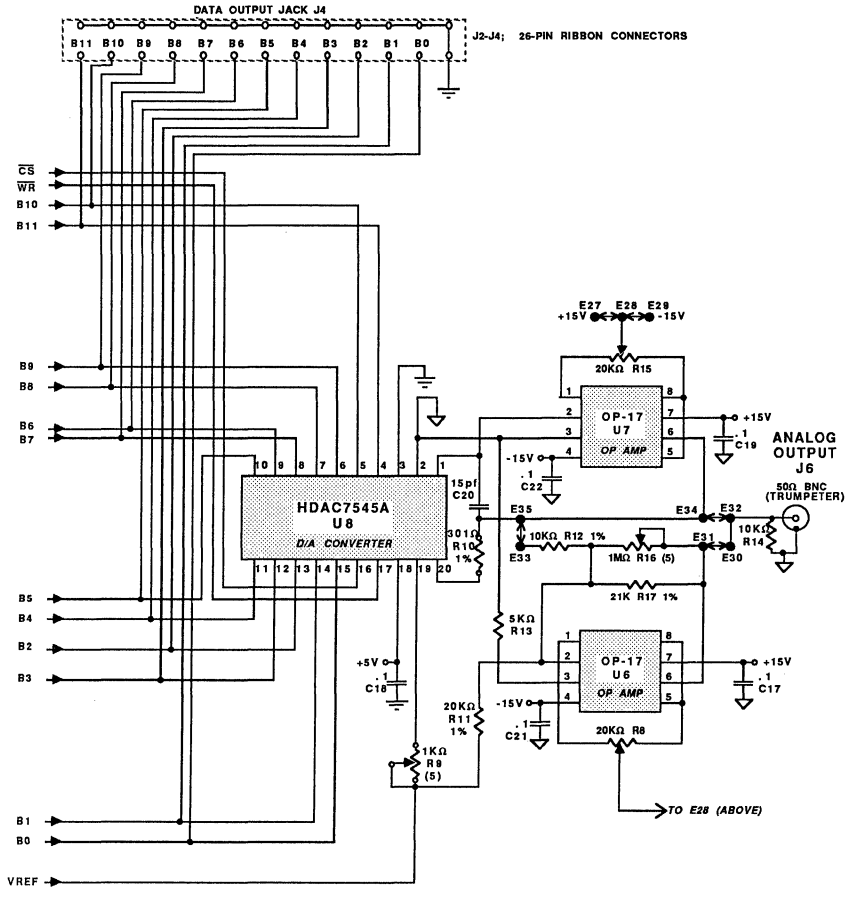


FIGURE 11 EB104 WIRING



NOTES:

(1) U3-U5 DECOUPLING CAPACITORS MOUNTED BENEATH IC (Q-PAK ™).
(2) PINOUTS OF JACKS AND IC'S (J1-J6, U1-U8) SHOWN FROM TOP VIEW.
(3) ALL CAPACITANCES IN uF UNLESS OTHERWISE INDICATED.
(4) E36 AND E37 USED AS LOGIC HIGH JUMPER POSTS FOR JACK J2.
(5) R9 AND R16 TEMP CO 100 PPM; R10, R11, R12 AND R17 TEMP CO 50 PPM.

DIAGRAM

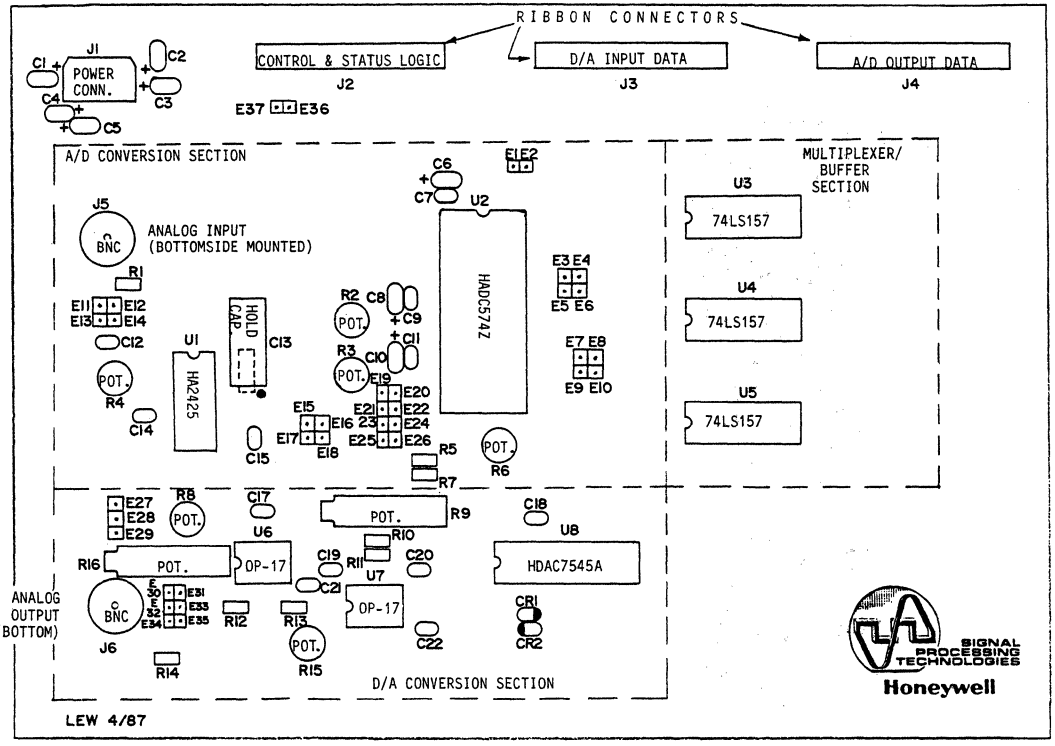
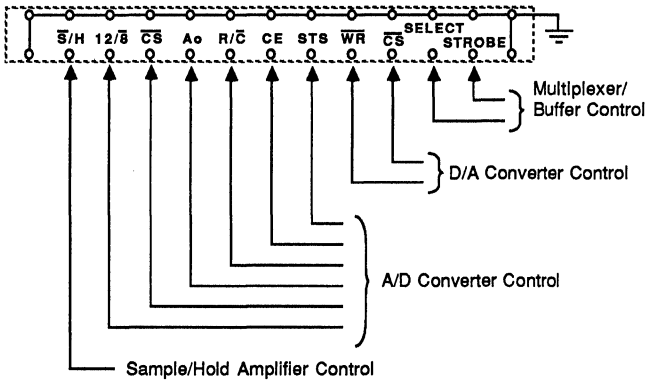


FIGURE 12
EB104 BOARD LAYOUT

Top View, Actual Size

CONTROL LINE JACK J2



S/H Input: "0" Allows S/H amp to track analog input; "1" holds value

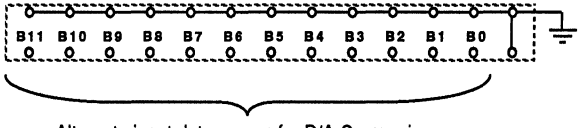
12/8 Input: "0" for 8-bit output format; "1" for 12-bit output format
CS (Chip Select Bar) Input: "0" enables chip operation; "1" prevents operation
Ao Input: "0" selects 12-bit data conversion; "1" selects 8-bit data conversion
R/C (Read/Convert Bar) Input: "0" initiates conversion cycle;
"1" Enables data output
CE (Chip Enable) Input: "0" prevents A/D operation; "1" enables operation
STS (Status) Output: A/D status output; outputs "1" while converting

WR (Write Bar) Input: "0" loads DAC input register; "1" locks register data
CS (Chip Select Bar) Input: "0" enables input register; "1" disables

STROBE Input: "0" enables data transfer; "1" results in all J4 outputs as "0"
SELECT Input: "0" selects A/D output data; "1" selects J3 input data

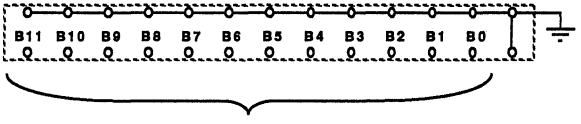
(Note "0" indicates a logic low condition, "1" indicates a logic high condition)

DATA INPUT JACK J3



Alternate input data source for D/A Conversion.
B0 is LSB, B11 is MSB

DATA OUTPUT JACK J4



Buffered output data from A/D Converter.
B0 is LSB, B11 is MSB

FIGURE 13
RIBBON CABLE CONNECTORS
PIN FUNCTION SUMMARY

Sample/Hold Utilization Options

S/H Amp in Analog Path: E12-E14, E15-E16
S/H Amp Bypassed: E11-E13, E17-E18

Sample/Hold Control Options

S/H Amp Controlled by J2 Pin: (E36, E37 Open)

S/H Amp Controlled by HADC574Z Status Output: E1-E2

HADC574Z Input Range Options

10 Volt Input Range: E23-E24
20 Volt Input Range: E25-E26

HADC574Z Unipolar/Bipolar Input Options

Unipolar Input Conditions: E21-E22
Bipolar Input Conditions: E19-E20

HADC574Z Output Format Options

12-Bit Output: (E3 Through E10 Left Open)
8-Bit Output: E3-E5, E4-E6, E7-E9, E8-E10

HDAC7545A Output Format Options

Unipolar Output: E32-E34
Bipolar Output: E30-E31, E33-E35

TABLE 11
JUMPER CONFIGURATION SUMMARY

Operation of the EB104 is taylored by positioning the Berg-type connectors between the appropriate pin pairs. This table shows a summary of the possible options and the corresponding jumper connections. In each case, it is imperative that one option is selected, but one only. For the jumper post locations refer to Figure 12 or the PC board.

A/D Conversion Section

R4: S/H Amp Offset Adjustment

R2: Gain Adjustment Of A/D Conversion, Unipolar and Bipolar Modes (Same as R2 in HADC574Z data sheet, figures 11 and 12)

R3: Offset (Zero) Adjustment of A/D Conversion, Unipolar Mode Only (Same as R1 in HADC574Z data sheet, figure 11)

R6: Offset (Zero) Adjustment of A/D Conversion, Bipolar Mode Only (Same as R1 in HADC574Z data sheet, figure 12)

D/A Conversion Section

R8: Offset (Zero) Adjustment of Op Amp U6

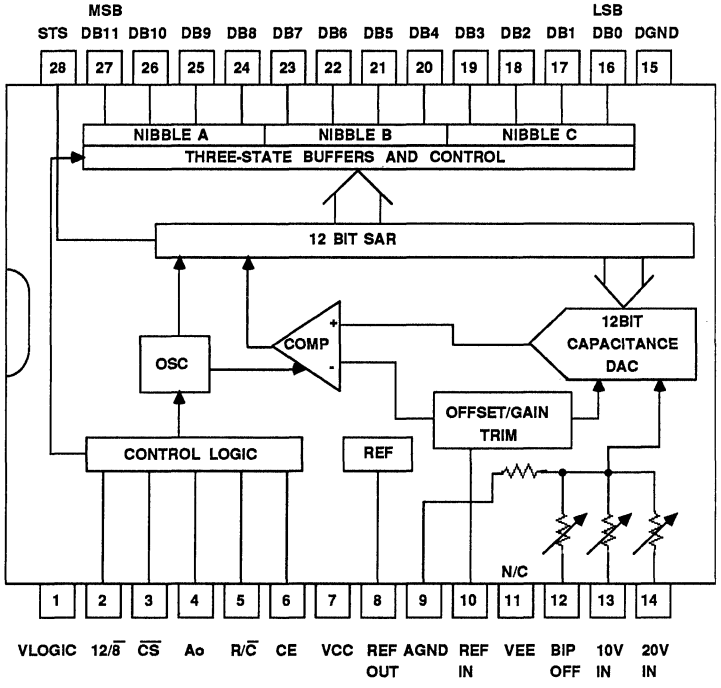
R15: Offset (Zero) Adjustment of Op Amp U7

R16: Full Scale Output Trim for use in Bipolar Mode

R9: (Optional Resistor, Board Delivered With Pins Jumpered) VREF Trim for D/A Conversion Adjustment; Used to Trim Full Scale Output in Unipolar Mode, or Zero Output in Bipolar Mode.

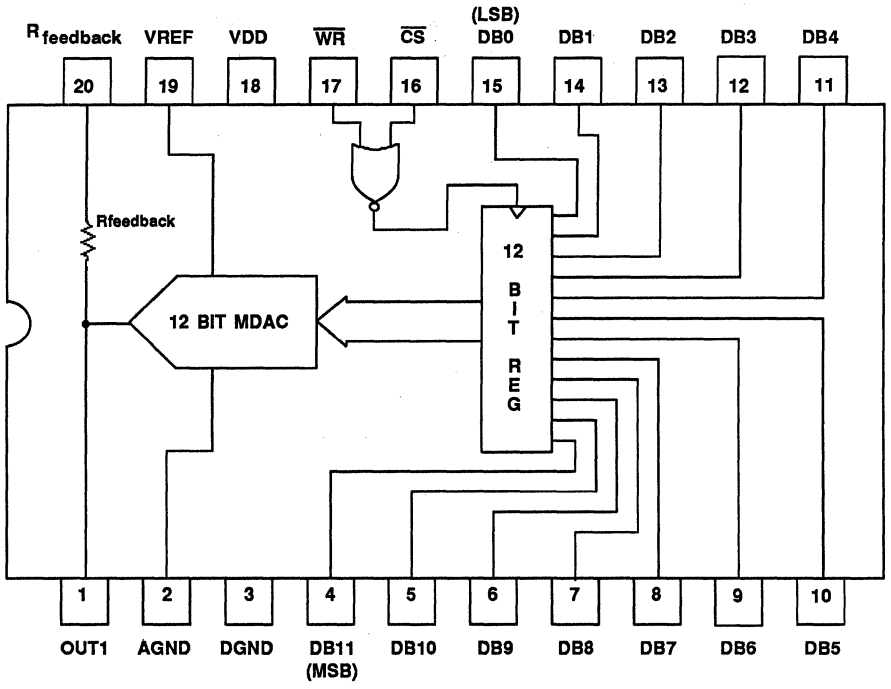
TABLE 12
TRIM POTENTIOMETER SUMMARY

Multi-turn potentiometers are supplied on the EB104 to allow fine adjustment of various analog conditions. Although the EB104 Is calibrated during manufacture to allow functionality, some adjustment may be necessary to obtain desired results.



PIN	PIN NAME	FUNCTION
1	V_{LOGIC}	LOGIC SUPPLY VOLTAGE, +5V
2	12/$\overline{8}$	DATA MODE SELECT INPUT
3	$\overline{CS}$	CHIP SELECT INPUT
4	Ao	BYTE ADDRESS/SHORT CYCLE INPUT
5	R/$\overline{C}$	READ/CONVERT INPUT
6	CE	CHIP ENABLE INPUT
7	VCC	ANALOG POSITIVE SUPPLY, +15
8	REF OUT	REFERENCE OUTPUT, +10V
9	AGND	ANALOG GROUND
10	REF IN	REFERENCE INPUT
11	N.C.	NO CONNECTION
12	BIP OFF	BIPOLAR OFFSET
13	10V IN	10 VOLT ANALOG INPUT
14	20V IN	20V ANALOG INPUT
15	DGND	DIGITAL GROUND
16-27	DB0-DB11	DIGIAL DATA OUTPUT
28	STS	STATUS OUTPUT

FIGURE 14
HADC574Z PIN ASSIGNMENT



PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT
2	AGND	ANALOG GROUND
3	DGND	DIGITAL LOGIC GROUND
4-15	DB0-DB11	OUTPUT DATA BITS
16	$\overline{CS}$	CHIP SELECT
17	$\overline{WR}$	DATA WRITE
18	VDD	POSITIVE POWER SUPPLY
19	VREF	REFERENCE INPUT VOLTAGE
20	$R_{feedback}$	INTERNAL FEEDBACK RESISTOR

FIGURE 15
HDAC7545A PIN ASSIGNMENT

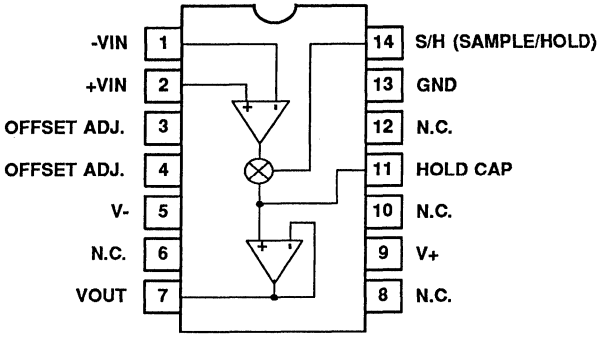
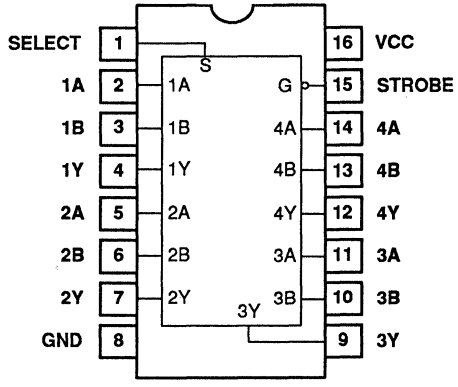


FIGURE 16
HA2425 SAMPLE/HOLD AMP PIN OUT
TOP VIEW



INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

FIGURE 17
74LS157 2-TO-1 MULTIPLEXER/SELECTOR PIN OUT AND LOGIC TRUTH TABLE
PIN OUT FROM TOP VIEW

NO.	REF. DESIG.	QTY	DESCRIPTION	MANUFACTURER / PART NO.
1	C1-C5	5	Capacitor, 1 µF Tantalum	
2	C6, C8, C10	3	Capacitor, 10 µF Tantalum	
3	C7, C9, C11, C12, C14, C15, C17, C18, C19, C21, C22	11	Capacitor, 0.1 µF	
4	C13	1	Capacitor, 0.01 µF Polystyrene	
5	C20	1	Capacitor, 15 pF	
6	See Note (1)	3	Capacitor, 0.01 µF Q-Pak™	Rogers Corporation
7	CR1, CR2	2	Diode, 1N914	
8	E1-E37	37	Jumper Pins	
9	J1	1	Connector, Power	Molex / 09-180-5061
10	J2, J3, J4	3	Connector, 26-Pin Ribbon Cable	TRW / 3593-5002
11	J5, J6, J7	3	Connector, BNC	Trumpeter / CBJ20
12	R1, R5	2	Resistor, 100 KΩ, 1/8 Watt, 5 %	
13	R7	1	Resistor, 100 Ω, 1/8 Watt, 5 %	
14	R10	1	Resistor, 301 Ω, 1/8 Watt, 1 %	Dale / RN55C
15	R11	1	Resistor, 20 KΩ, 1/8 Watt, 1 %	Dale / RN55C
16	R12	1	Resistor, 10 KΩ, 1/8 Watt, 1 %	Dale / RN55C
17	R13	1	Resistor, 4.99 KΩ, 1/8 Watt, 1 %	
18	R14	1	Resistor, 10 KΩ, 1/8 Watt, 5 %	
19	R17	1	Resistor, 21 KΩ, 1/8 Watt, 1 %	Dale / RN55D
20	R2, R3	2	Potentiometer, 100 Ω Multiturn	Bourns / 3339P-101
21	R4, R6	2	Potentiometer, 100 KΩ Multiturn	Bourns / 3339P-104
22	R8, R15	2	Potentiometer, 20 KΩ Multiturn	Bourns / 3339P-203
23	R9	1	Potentiometer, 1 KΩ Multiturn	Bourns / 3006P-102
24	R16	1	Potentiometer, 1 MΩ Multiturn	Bourns / 3006P-105
25	U1	1	I.C., HA2425, Sample/Hold Amp	Harris
26	U2	1	I.C., HADC574BCJ, A/D Converter	Honeywell
27	U3, U4, U5	3	I.C., 74LS157, TTL Quad Multiplexer	
28	U6, U7	2	I.C., OP-17, Operational Amplifier	PMI
29	U8	1	I.C., HDAC7545AACD, D/A Converter	Honeywell

(1) Note: Q-pak™ capacitors mounted in DIP sockets of U3, U4, U5

FIGURE 18
EB104 COMPONENT LIST

THERMAL CONSIDERATIONS FOR HIGH PERFORMANCE DEVICES

PAUL M. BROWN

INTRODUCTION

The package of an integrated circuit is its interface to the outside world. The pins and bonding wires conduct power and control voltages to and from the silicon chip (die). In addition, the pins, bonding wires and body of the package transfer heat from the die to the outside environment. Just as electrical resistance is a measure of the efficiency with which current is conducted by an electrical connection, thermal resistance measures the efficiency of heat flow. There are four thermal resistances of concern to the systems designer: θJC, the thermal resistance from the die (junction) to the package (case), θCS, the thermal resistance from the package (case) to the heat sink, θSA, the thermal resistance from the heat sink to the ambient environment, and θJA, the thermal resistance from the die (junction) to the ambient environment through the package with no additional heat sink attached.

The junction temperature and the temperature of the die can be easily calculated (see the example below) given the ambient temperature, the appropriate thermal resistance, and the power dissipated on the die. It is important to keep the die temperature under the maximum specified limit, usually 150°C, under worst case conditions; i.e. maximum ambient temperature, maximum power supply voltage, and maximum load to avoid permanent damage to the device. Reliability is also acutely affected by the junction temperature since many failure mechanisms are accelerated with an increase in temperature. An IC operating at a junction temperature, (TJ), of 125°C will typically exhibit a failure rate almost 150 times that of the same device operating at a junction temperature of 70°C.

SYSTEM THERMODYNAMICS

Thermal management in a board or system level application consists of transferring heat from an undesirable location (i.e. the die) to one where it can be dissipated into the environment without adversely affecting the system. There are three ways that heat is transferred: conduction, convection, and radiation.

Thermoconduction is the process of transferring heat through a medium from a relatively high temperature to a relatively low temperature. To maximize the conductive flow of heat, it is important to choose a medium with high thermal conductivity, such as copper or aluminum. The geometry of the medium should be chosen to yield the largest practical cross-sectional area and to shorten the conduction path. The rate of heat transfer is the greatest when there is a large difference between the high and low temperatures.

Thermoconvection, in the context of this discussion, is the transfer of heat from a solid (the IC and attached heat sinks) to a fluid (air). Convection depends upon the surface area across which the transfer takes place, the temperature difference between the solid and the fluid, and the characteristics of the fluid including: thermal expansion coefficient, specific heat, viscosity, density, and thermal conductivity. Free convection occurs when heat from the solid is conducted to the fluid in contact with it causing the fluid to become less dense and rise thus being displaced by fluid at a lower temperature. Convection is most effective if the fluid flow next to the solid is turbulent. This prevents boundary layers of fluid forming next to the solid thereby insulating the solid from the fluid.

Forced convection can be an order of magnitude more efficient than free convection. However, it is often more expensive to implement. When forced convection is used, the recommended air flow is usually between 200 and 500fpm (feet per minute). Care should be taken to insure that this air flow is turbulent.

To maximize the effectiveness of convection, it is important to mount the heat dissipating surfaces in the vertical direction for free convection or along the air flow for forced convection. The enclosure must have proper ventilation so that the flow of air is not restricted. Place low power devices close to the air source in forced convection systems to keep them at the lowest possible temperature.

Heat is also transferred via infra-red radiation. To maximize thermal radiation, it is important to choose a radiating element that has the largest effective surface area (surface area where fins do not face each other) and the highest emissivity. The radiating element must have a temperature that is high relative to that of near objects. This is especially true for the object or media (i.e. enclosure or air) that is meant to receive the radiated heat. If the "radiator" is not at the highest relative temperature, it will absorb radiated heat energy.

CALCULATING THE OPERATING DIE TEMPERATURE

A thermodynamic "circuit" can be used to easily calculate heat flow and temperature rises. Figures 1 and 2 below illustrate that heat is analogous to electrical current, temperature to voltage, and thermal resistance to electrical resistance. Ohms (volts per amp) are, therefore, analogous to °C per watt. The circuit in Figure 1 is for a device with no external heat sink and Figure 2 is for a device with an external heat sink. The minimum die temperature is the ambient temperature (if no power is dissipated).

Example: Calculate the junction temperature of an IC that dissipates one watt, has no external heat sink, operates in an ambient environment of 45°C, and has a θJA of 75°C/W.
Answer: TJ =120°C (see Figure 3)

Figure 1. Basic Thermal Circuit

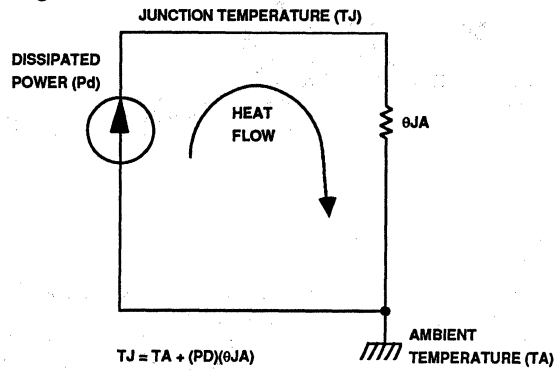


Figure 2. Thermal Circuit with External Heat Sink

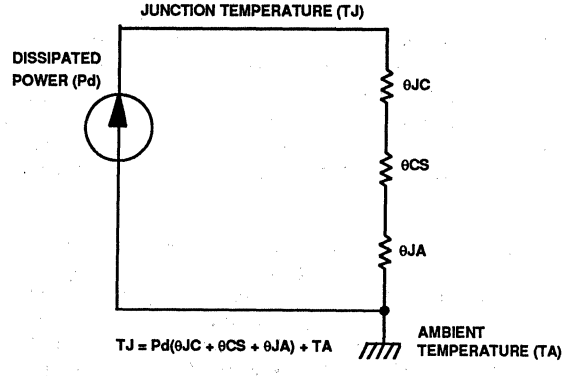
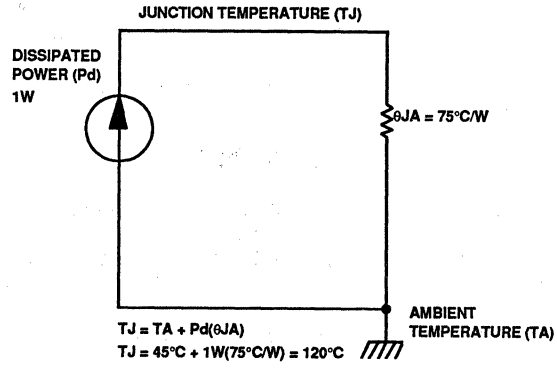


Figure 3. Junction Temperature Calculation

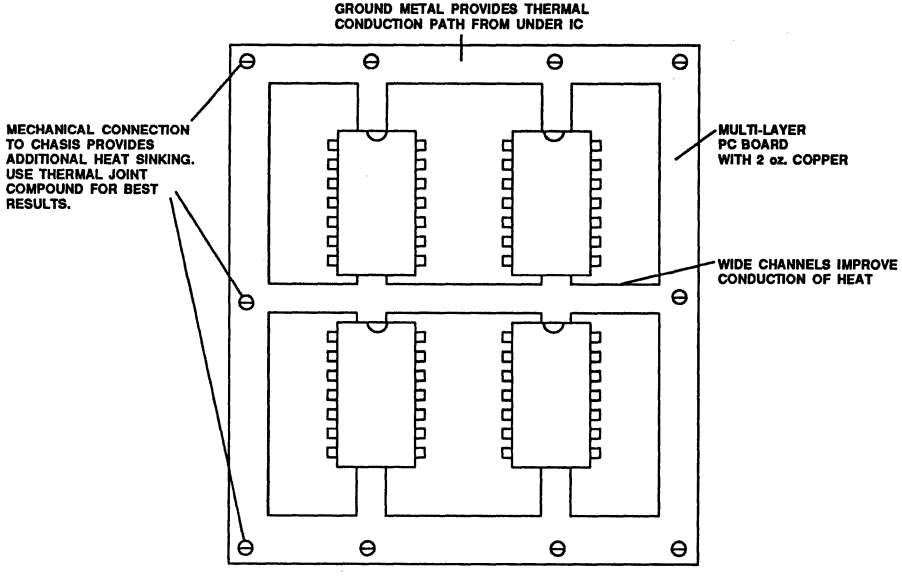


PACKAGE THERMAL RESISTANCE

The thermal resistance of an IC, both θJA and θJC, depend upon several unique product specific characteristics. Among these are: die size, the method used to attach the die to the package (glass, gold, eutectic, epoxy), bonding wire thickness, the number of bonding wires, package cavity size, package material type, package geometry and design, and package emissivity. Thermal resistance is, therefore, typically specified on the device data sheet. θJA is generally specified for a device inserted into a PC board mounted socket in still air at 25°C. This specification includes the effects of both convection and radiation. If the ambient conditions are different, i.e. moving air, θJA will be different. θJC, on the other hand, is measured with the package attached to an infinite heat sink and is a measure of thermal conduction from the die to the package.

The graphs below give a representation of the ranges of θJA and θJC that can be expected from industry standard packages. This data has been compiled from information supplied by several semiconductor and package manufacturers and is valid at sea level in still air assuming free convection. Under these conditions, approximately 70% of heat transfer occurs through convection and 30% by radiation. The thermal resistances of packages and heat sinks must be derated in other environmental conditions due to the loss in effectiveness of heat transfer. At high altitudes (770,000 ft.), only 30% of heat transfer is by convection (due to the less dense air) and 70% by radiation. In space (a very good vacuum), all heat is transferred by radiation. At ambient temperatures greater than 50°C heat transfer suffers due to decreased air density. Since there are many variables that affect thermal resistance specifications, the data supplied here is generic information and is only approximate. Consult the data sheet or the manufacturer for thermodynamic specifications of a particular device.

Figure 4. Thermal Conduction Channels



HEAT SINKING

A heat sink is a thermoconductive device that is mechanically affixed to the integrated circuit to reduce the thermal resistance from case to ambient (an infinite heat sink can only reduce θJA to θJC). Heat sinks are used with ICs that generate more heat energy than their package can effectively dissipate. Heat sinks include: devices designed to aid heat dissipation, the circuit board and its conductive traces. The ability of the circuit board to conduct heat away from the IC can be enhanced in several ways. First, whenever possible, design the P.C. board such that either a large ground or a Vcc plane is around and directly under the IC. When layout permits, wide ground traces (of 2 oz. copper) can be used to form a heat conducting channel from under the IC to the edge of the P.C. board where a good thermal connection can be made to the chassis (see Figure 4). It is important that these heat conducting channels pass under the IC since the die is usually attached to the bottom of the package (except for "cavity down pin grid arrays"). The most efficient heat conduction path is, therefore, out the bottom of the package. The package leads can also conduct a significant amount of heat away from the IC. This is especially true if 2 oz. copper traces are used. In most cases, layouts will be complicated enough that multi-layer P.C. boards will be required. This is almost unavoidable for large pin count packages or when controlled impedance techniques, such as microstrip or stripline, must be used. Multi-layer boards afford a great deal more freedom for thermal design than two layer boards. Discrete heat sink devices are available in a wide variety of forms from manufacturers, such as EG&G, Wakefield Engineering, Avid Engineering, or IERC.

Component placement is also critical. DO NOT place components that dissipate large amounts of power , such as dropping resistors, voltage regulators, etc., in close proximity to ICs that are themselves dissipating large amounts of power. Concentration of power dissipating components makes heat removal very difficult. Heat radiated by one component will be absorbed by another. Some components that appear in analog to digital and digital to analog circuitry, such as voltage references, OP amps, and buffer amplifiers, are very sensitive to temperature and should be isolated from thermal sources. Arrange components and heat sink fins to avoid blocking convection currents or forced air. Take into account the orientation that the circuit board will have when it is installed and the expected flow of convection currents and/or forced air.

It should be obvious from the above discussion that thermal design must be an integral part of the overall design of any board or system. Installing glue on or clip-on heat sinks or a fan as an afterthought is no substitute for well planned, thermal design.

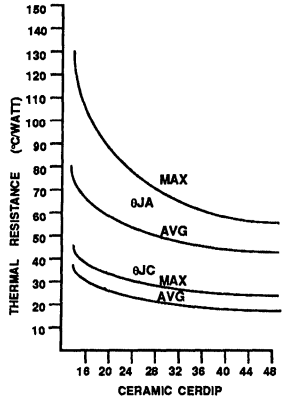
REFERENCES

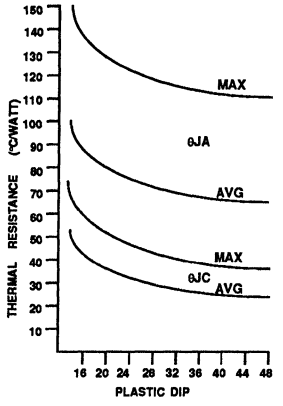
EG&G Wakefield Engineering. Active Cooling Products and Capabilities. Massachusetts: EG&G Publications and Media Center, 1985.

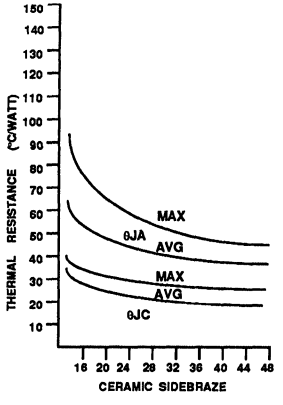
EG&G Wakefield Engineering. Standard Products Catalog. Massachusetts: EG&G Publications and Media Center, 1985.

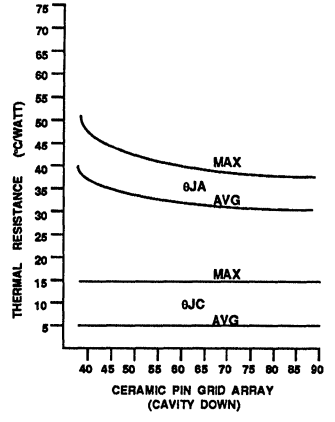
International Electronic Research Corporation. Heat Sink/Dissipator Products and Thermal Management Guide. International Electronic Research Corporation, 1985.

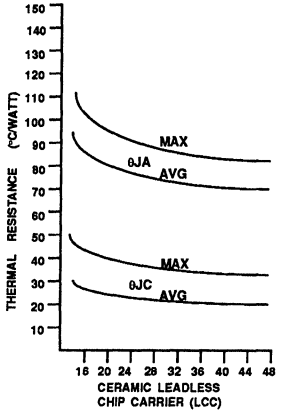
Thermal Resistance Ranges for Various Package Types in Still Air (1)











(1) This is generic data. For exact values for a given product, consult a product data sheet or the manufacturer.

NOTES:

EB105 EVALUATION BOARD

INCLUDES HSCF24040 PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

Craig Wiley

FEATURES

- Complete With Socketed HSCF24040ACD Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches for On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

APPLICATIONS

- HSCF24040 Evaluation
- Prototype System Development
- Programmable General-Purpose Subassembly

GENERAL DESCRIPTION

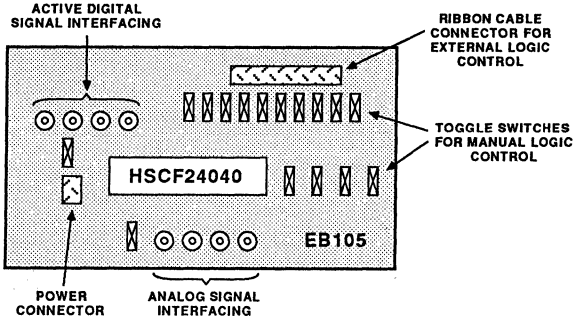
The EB105 Evaluation Board allows full exercise of the Honeywell HSCF24040 Programmable 7th Order Low Pass Active Filter. Unlike a handwired breadboard, this ground-planed, printed circuit board provides a high performance, noise-free environment. It provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is conveniently enabled by on-board toggle switches. Alternately, programming and control can be accomplished though the on-board ribbon cable connector. This option allows software control which can aid in system development.

By making full use of the HSCF24040, the EB105 provides an analog input and output for both the RC and switched-capacitor filters. Both of these low-pass filters are fully programmable. Analog interfacing is accomplished with on-board BNC connectors to minimize noise and digital signal coupling. The EB105 also makes use of separate analog and digital supply grounds to further minimize digital coupling.

A clock crystal is supplied on the board which utilizes the HSCF24040 crystal oscillator feature. An external time base can be used optionally. BNC connectors are provided for external clock input and clock output, for the $\overline{\text{CONVERT}}$ output and the $\overline{\text{SYNC}}$ control line. Use of BNC connectors on these active digital lines assure a minimum of digital to analog coupling.

8

FIGURE 1 EB105 BOARD FEATURES



EB105 LAYOUT AND GENERAL INFORMATION

The EB105 contains one socketed HSCF24040 integrated circuit, an assortment of toggle switches and connectors, and a few discrete components used for power supply decoupling and logic voltage pull-up or pull-down. Board layout is shown in Figure 3. The prime function of the EB105 is to provide a low noise operating environment for the HSCF24040 and to allow ease of interface and programming for the purpose of device evaluation.

POWER SUPPLY CONNECTION

Power is supplied though the leaded Molex connector as detailed in Figure 2. Ensure that the beveled edges of the male and female connectors are aligned prior to coupling. Digital and Analog Ground should be connected together at the power supplies to provide maximum noise isolation. The male and female connectors should be coupled and the power supplies connected prior to turning on the power supplies. The power supply current consumption will be that of the HSCF24040 which can be found in the HSCF24040 preliminary information or data sheet.

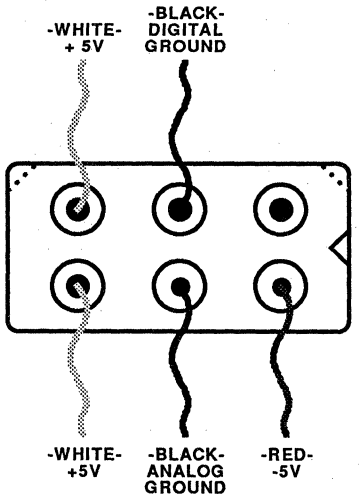


FIGURE 2
POWER SUPPLY CONNECTION
Leaded Power Connector for Jack J1
Top View

PROGRAMMING AND PARAMETER CONTROL

Operation of the EB105 must be preceded by device programming in order to establish operating characteristics. Programming involves loading the HSCF24040 data registers. This can be accomplished manually by use of the on-board toggle switches or externally by software though ribbon connector jack J1. Table 1 summarizes the EB105 toggle switches, most of which are directly related to device programming. The direct programming mode, established by switch S12, allows the HSCF24040 characterisics to be changed "on the fly" by register logic switches S1-S10.

Register programing and device control can also be accomplished externally though jack J1, the ribbon cable connector. Figure 5 shows the pinout of jack J1. Note that each pin of jack J1 is connected directly the corresponding pin of the HSCF24040. When using jack J1, ensure switches S1-S10 and S13 are in the open (center) position and S12 is in the "DP" position.

Please refer to Table 1 and the HSCF24040 preliminary information or data sheet for further information on register programming and the other input logic control.

DEVICE OPERATION

Operation of the HSCF24040 involves utilizing the device for real time filtering of an analog signal. In addition, a $\overline{\text{SYNC}}$ input and $\overline{\text{CNVRT}}$ output are available for external use which can serve as a timing interface to an A/D converter or sample/hold amplifier. Unlike the programming and parameter control inputs described above, all of the active signals used during operation utilize on-board BNC connectors to reduce coupling. This is further aided by the use of separate analog and digital ground connections. Switches S11 and S16, described in Table 1, play a part in device operation. Table 2 provides a summary of the jacks that are used during device operation. Note that each of these jacks are directly tied to the corresponding HSCF24040 pin and use similar callouts. For more information on these pin functions please refer to the the HSCF24040 preliminary information or data sheet.

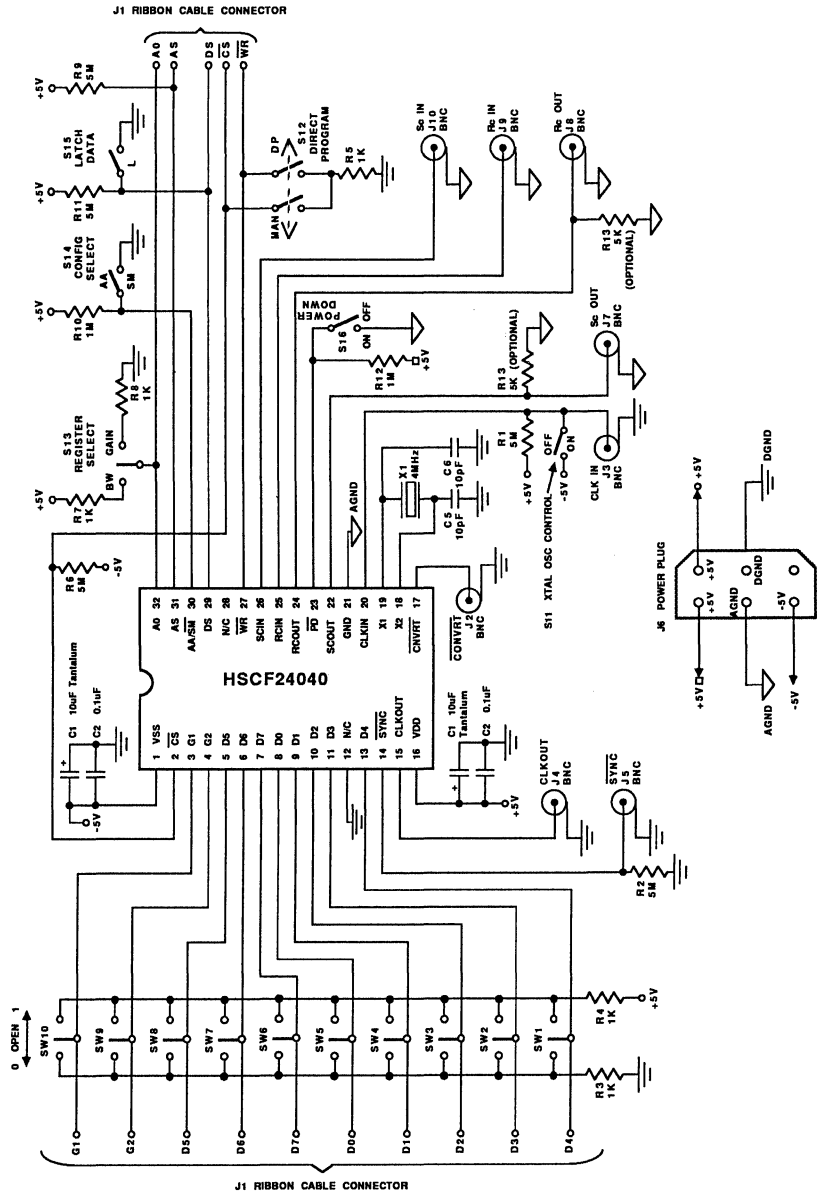


FIGURE 3
EB105 WIRING DIAGRAM

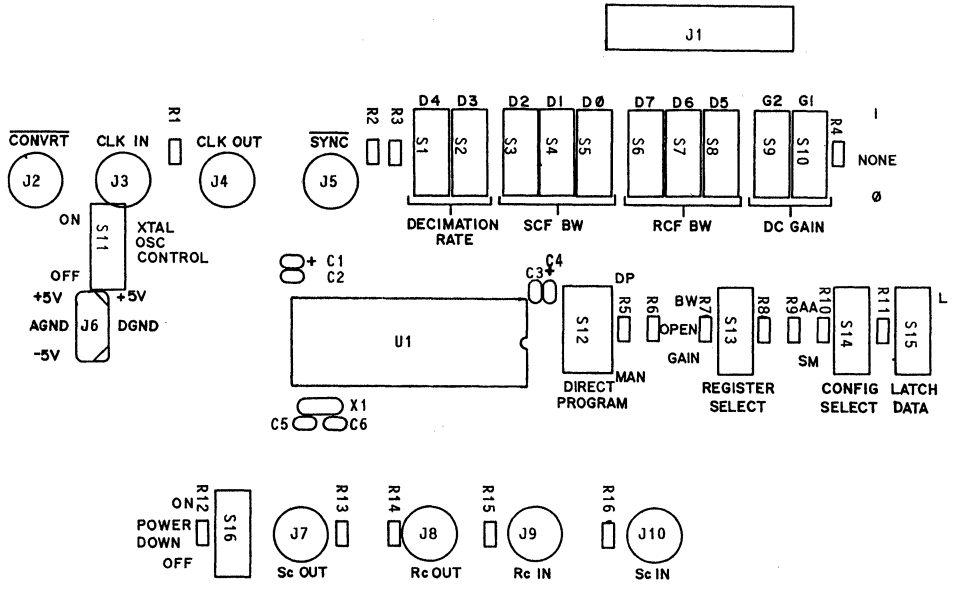


FIGURE 4
EB105 BOARD LAYOUT
Top View

TABLE 1 EB105 TOGGLE SWITCH SUMMARY (PART 1)

Switches S1 to S10: Register State Operators

Position of each switch (up or down) determines the logic state of the corresponding input register upon loading. Each switch is disconnected when in the center position which allows programming though jack J1.

Type: Double Pole, Single Throw, 3 Position
Positions;
UP: Loads Logic 1 State
CENTER: Disconnects switch, allows programming though Jack J1
DOWN: Loads Logic 0 State

S1: Decimator Sample Rate Bit D4
S2: Decimator Sample Rate Bit D3
S3: Clock to SCF Bandedge Divide Down Ratio Bit D2
S4: Clock to SCF Bandedge Divide Down Ratio Bit D1
S5: Clock to SCF Bandedge Divide Down Ratio Bit D0
S6: RC Filter Bandedge Bit D7
S7: RC Filter Bandedge Bit D6
S8: RC Filter Bandedge Bit D5
S9: DC Gain Bit G2
S10: DC Gain Bit G1

Switch S11: "XTAL OSC CONTROL", Crystal Oscillator Control Switch

This switch enables and disables the HSCF24040 crystal oscillator function. It is directly connected to pin CLKIN and jack J3. When it is down in the "OFF" position it allows a clock input into jack J3 to serve as the HSCF24040 time base. When it is in the up "ON" position pin CLKIN is tied low to -5V and the internal crystal oscillator serves as the time base.

Type: Single Pole, Single Throw
Positions;
UP: "ON" which enable the internal clock
DOWN: "OFF" which disables the internal clock and allows operation by the external clock

Switch S12: Direct Program Switch

Direct program mode causes the data registers for D0-D7, G1 and G2 to act transparent. When switch S12 is up in the "DP" or direct program position, $\overline{CS}$ is pulled to VSS (-5V) by R6. This disables the A0, AS, $\overline{WR}$, and DS inputs and places the HSCF24040 in the direct program mode. When switch S12 in down in the "MAN" or manual position, input register loading is controlled by switch S15; switch S13 must be in the "BW" or "GAIN" position. Note that data latch control inputs $\overline{CS}$, AO, AS, $\overline{WR}$, and DS can be driven from jack J1 when S12 is in the "DP" position and S13 is in the open (center) position.

Type: Single Pole, Double Throw
Positions:
UP: "DP" Direct Program mode, D0-D7, G1, G2 latches transparent (switch open)
DOWN: "MAN" Manual mode, loading controlled by S15 (switch closes)

TABLE 1 EB105 TOGGLE SWITCH SUMMARY (PART 2)

Switch S13: Register Select Switch

This switch, which is tied directly to pin AO, selects either the D0-D7 registers or G1, G2 registers during manual loading. When in the "GAIN" (down) position, it sets pin AO to logic 0 which allows access to register bits G1 and G2. When in the "BW" (up) position, it sets pin A0 to logic 1 which allows access to register D0 through D7. With switch S13 in the center position, it is disconnected and allows control of pin A0 though Jack J1. The purpose of the AO pin is to allow use of an 8-bit bus to write all ten registers. The data into pin AO can be latched by a 1 to 0 logic transition on pin AS; pin AS is pulled high by resistor R9 and can be pulled low by pin AS of jack J1.

Type: Double Pole, Single Throw, 3 Position
Positions:
- UP: "BW", Bits D0-D7 Latch Access
- CENTER: Switch Open (Control enabled by jack J1)
- DOWN: "GAIN", Bits G1, G2 Latch Access

Switch S14, "CONFIG SELECT", Filter Configuration Selection

This switch controls the logic state of HSCF24040 pin AA/$\overline{SM}$ which internally determines the analog input to the switched-capacitor filter. In the up "AA" position logic state 1 is forced which establishes the RC filter output as the SCF input. In the down "SM" position logic state 0 is forced which establishes the ScIN analog input as the input to the SCF. This switch does not have a corresponding function on Jack J1.

Type: Single Pole, Single Throw
Positions;
- UP: "AA" RC filter output is SCF input (Logic 1)
- DOWN: "SM" Analog input ScIN is SCF input (Logic 0)

Switch S15, "LATCH DATA" Data Strobe Control Switch

Pushing this momentary-contact switch up into the "L" (Latch) position loads the input registers by pulling the DS input to ground. Concurrently, switch S12 must be in the "MAN" (DOWN) position or pins $\overline{WR}$ and $\overline{CS}$ must be pulled low at jack J1.

Type: Single Pole, Single Throw, Momentary Contact
Positions;
- UP: "L" Latches register data (DS = logic 0), Momentary Contact
- DOWN: Inactive (DS = logic 1)

Switch 16: Power Down Switch

This switch is used to disable the analog circuitry of the HSCF24040 thus conserving power. Along with pullup resistor R12, it controls the logic state of pin PD.

Type: Single Pole, Single Throw
Positions;
- UP: "ON" Device Fully Functional (PD = logic 1)
- DOWN "OFF" Analog Portion Disabled (PD = logic 0)

TABLE 2 EB105 BNC CONNECTOR SUMMARY

Jack J2: "CNVRT", External A/D Converter Control Output Pin

This active low output signal is used to indicate when the Sc OUT output is valid, i.e., when the decimator output has settled. It is used to trigger an external A/D converter or sample/hold amplifier. This jack is directly connected to the CNVRT pin of the HSCF24040.

Jack J3: "CLK IN", External Clock Input

This input jack is used to drive the HSCF24040 with an external clock. Switch S11 must be in the OFF position for this input to function. This jack is connected directly to the CLKIN pin of the HSCF24040.

Jack J4: "CLK OUT", Device Clock Output

This output jack provides a buffered version of either CLKIN or the internally generated crystal oscillator output. It is connected directly to pin CLKOUT of the HSCF24040.

Jack J5: "SYNC", Decimator Sampling Sync Input

This active low input jack controls the sampling instant for the decimator output. Applying a falling edge to the SYNC input initiates the CNVRT pulse on the next rising edge of CLKOUT. This jack is connected directly to pin SYNC of the HSCF24040.

Jack J7: "Sc OUT", Switched-Capacitor Filter Output

This jack is the analog output of the switched-capacitor filter after passing through the decimator. It is directly connected to the pin SCOUT of the HSCF24040. Optional load resistor R13 can be added on the EB105 board.

Jack J8: "Rc OUT", RC Filter Output

This jack is the analog output of the RC filter and is connected directly to pin RCOUT of the HSCF24040. Optional load resistor R14 can be added on the EB105 board.

Jack J9: "Rc IN", RC Filter Input

This jack is the analog input to the RC filter and is connected directly to pin RCIN of the HSCF24040.

Jack J10: "Sc IN", Switched-Capacitor Filter Input

This jack is the analog input to the Switched-capacitor filter and is directly connected to pin SCIN of the HSCF24040. This pin is internally enabled only when switch S14 "CONFIG SELECT" is down in the "SM" position.

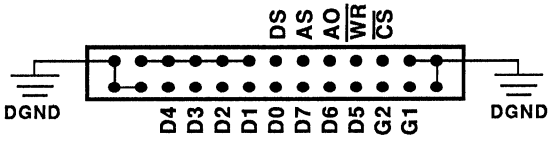


FIGURE 5
RIBBON CABLE CONNECTOR JACK J1
PIN FUNCTION SUMMARY

***For Ordering Information See Section 1.*

NOTES:

USING ECL DACs WITH TTL LOGIC

by Tom DeLurio and Russ Moen

High speed Digital-to-Analog converters are primarily designed to perform in 10K or 100K ECL systems because of the inherent speed and low noise that is characteristic of this logic group. Unfortunately, a large number of designers, are either using high speed TTL logic with the DAC or are stuck in a +5V only environment and using pseudo ECL levels. This Application Brief will address these issues and offer solutions to overcome the perceived incompatibility between -5.2V operation and +5V operation.

Although the majority of Honeywell Signal processing Technologies' High speed DACs are optimized for ECL input levels, TTL levels can be utilized by pulling up the input pins to +5V. Additionally, the Vcc or Ground pins must also be pulled up to +5V and the Vee pins are tied to ground. And, by adding optional input voltage divider resistors, decreased noise can be realized by attenuating switching levels.

In a pseudo ECL system where the preceding DAC logic or memory is ECL but is pulled up to +5V, all that needs to be done is to pull the DAC up to the same level by shifting the ground or Vcc and Vee pins. Also, in most cases, analog output level shifting is required to bring the output down to ground potential. This is not necessary if driving an AC coupled load.

Honeywell SPT makes a variety of different ECL compatible DACs which have different types of output structures, but similar inputs. Therefore, if needed, all the circuits will have the same input level shifting but different output circuits.

The first device, the HDAC97000, is an 8-bit Video DAC that operates at 200MWPS. It has an 800Ω output source resistor and standard ECL input pins. The circuit in Figure 1 shows how to attenuate and pull up the input and video control pins for TTL levels using resistors R1 and R2. R1 is for input attenuation and R2 is the pull-up resistor for each input and control pin. The associated gain setting, setup, and glitch adjust function inputs are the same as before but just shifted up to accommodate a +5V environment. The analog output is then level shifted down to ground and resistor values are determined by the following equations:

Gain Setting

$$R_{01} = \frac{(V-V_1)R_L}{V_{3\,MAX}} \qquad \text{Where } R_L = R_{L1} \parallel R_{L2}$$

Where V_{3MAX} = Maximum output voltage.

$$R_{SET} = K(3^{63}/_{64})R_{01}$$

Where $K = {}^{160}/_{90}$ for 20IRE Setup

$= {}^{150}/_{90}$ for 10IRE

$= {}^{147.5}/_{90}$ for 7.5IRE

$= {}^{140}/_{90}$ for 0IRE

$$\frac{V_1 - V_{be}(Q_1)}{1/2\ I_{DAC\ MAX}} \le R_{02} \le \frac{V_1 - V_{be}(Q_1)}{\frac{V-V_1}{10R_{01}}}$$

Example

For
V_3 = 0 to +1.071V (0 to 150IRE), 1/2 $I_{DAC\ MAX} \cong$ 18mA,
Blank = 10IRE, V1 = 3.77V ≅ V2, RL = 37.5Ω

$$R_{01} = \frac{(5V - 3.77V)}{1.071V}\,37.5 = 43\Omega,\ 1/8W$$

$$R_{SET} = {}^{150}/_{90}\,(3\,{}^{63}/_{64})\,43\Omega = 212\Omega,\ 1/8W$$

DAC Midscale ≅18mA

$$R_{02} \ge \frac{3.77V - .75V\,(Q_1\,V_{be})}{18mA} \ge 168\Omega,\ 1/8W$$

$$R_{02} \le \frac{3.77V - .75V}{\frac{5 - 3.77}{10(43)}} \le 1{,}056\Omega,\ 1/8W$$

A practical method for setting up the circuit is as follows:

1. With $I_{DAC\ out}$ = 0mA, adjust R_{01} for desired full scale voltage at V_3.
2. $I_{DAC\ out} = I_{MAX}$, adjust R_{SET} for desired minimum voltage at V_3.
3. $I_{DAC\ out}$ = 1/2 Gray Scale, adjust R_{02} for $V_1 = V_2$.
   (Readjust R_{01} and R_{SET} in steps 1 and 2)

It is important that all +5V supplies be adequately bypassed as shown in Figure 1 for input, output and power pins.

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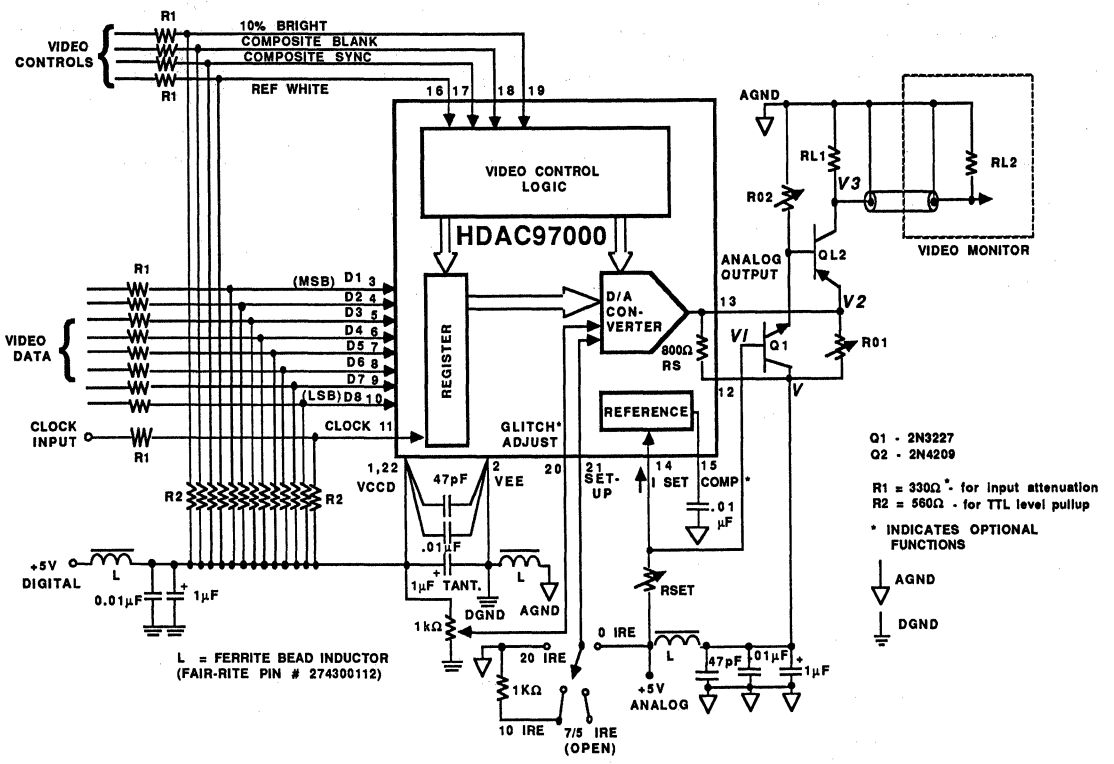
FIGURE 1 - HDAC97000 IN A TTL ENVIRONMENT.



The next devices are 8-bit High speed DACs that operate from 165, 275, and up to 400MWPS. They are respectively the HDAC10180, HDAC10181, and the HDAC51400. Each part has the same output current structures but have different voltage reference configurations. The HDAC10180 does not have an internal voltage reference and needs an external reference as shown in Figure 2. If two or more DACs are used as in an RGB monitor application, the HDAC10180s can use the reference from one HDAC10181. The HDAC51400 has a reference on board but has a separate reference out pin, whereas the HDAC10181 shares its' reference out with the reference input pin.

There are numerous ways to level shift the output from these devices to ground reference, but the circuit in Figure 2 takes advantage of the differential current output pins (OUT+ and OUT-). The equations for choosing resistor values are as follows:

For the LM113 or HDAC10181/51400 Reference Voltage

$V+ = +1.2V$

$$I_{SET} = \frac{V+}{(\propto T)\ R_1 + R_2}$$

$\propto T$ is the number of turns on potentiometer R1.

$R_L = R_3 \parallel R_4$

$$I_C = \left(\frac{1.2 + (V_{be1} - V_{be2})}{R_6} \right) - \frac{V_{OUT}}{R_L}$$

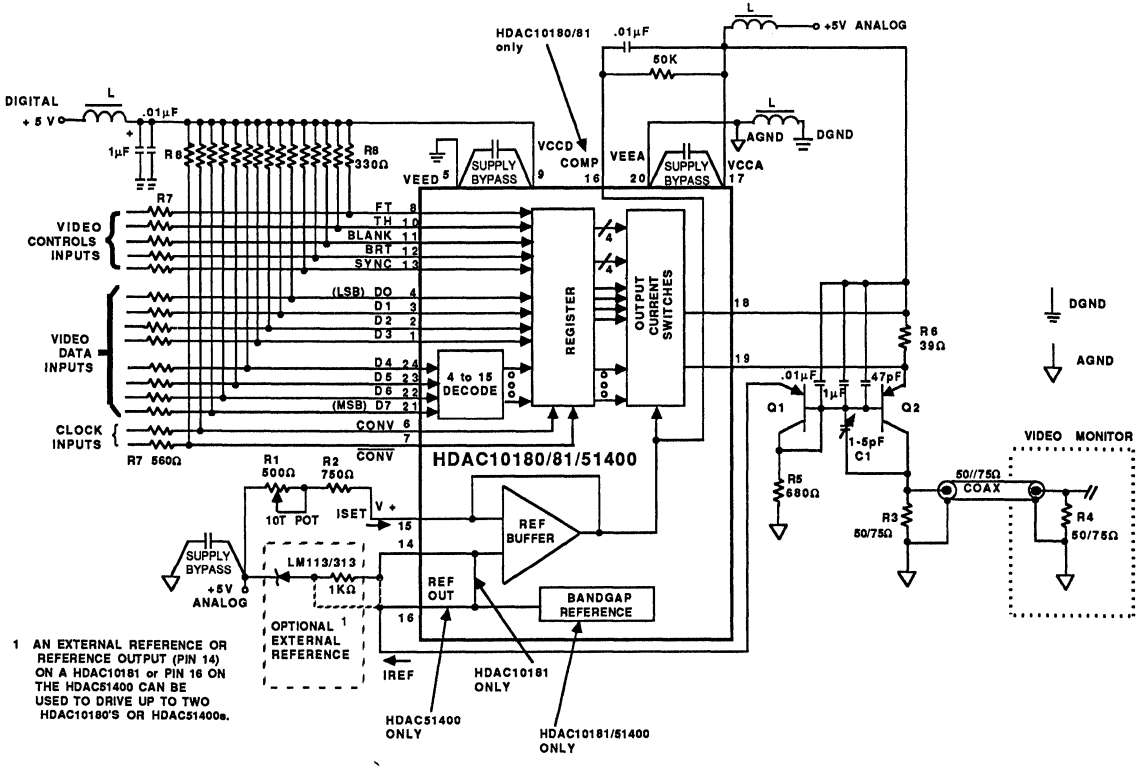
The current in Q2

V_{out} (F.S.) = 15.9375 (I_{SET}) R_L + 7.5IRE

Where Full Scale ≈ 650mV and 7.5IRE ≈ 54mV.

7.5IRE is the monitor dc setup level and is standard on the HDAC10180/81/51400 Video DAC series.

FIGURE 2 - HDAC10180/81 AND HDAC51400 IN A TTL ENVIRONMENT.



1 AN EXTERNAL REFERENCE OR REFERENCE OUTPUT (PIN 14) ON A HDAC10181 or PIN 16 ON THE HDAC51400 CAN BE USED TO DRIVE UP TO TWO HDAC10180'S OR HDAC51400s.

Q1 = Q2 = 2N4209 for HDAC10180/81B
Q1 = Q2 = 2N5583 for HDAC10180/81A
Q1 = Q2 = 2N5583 for HDAC51400

8

NOTES:

EXTERNAL SYNC CIRCUIT FOR VIDEO DACs

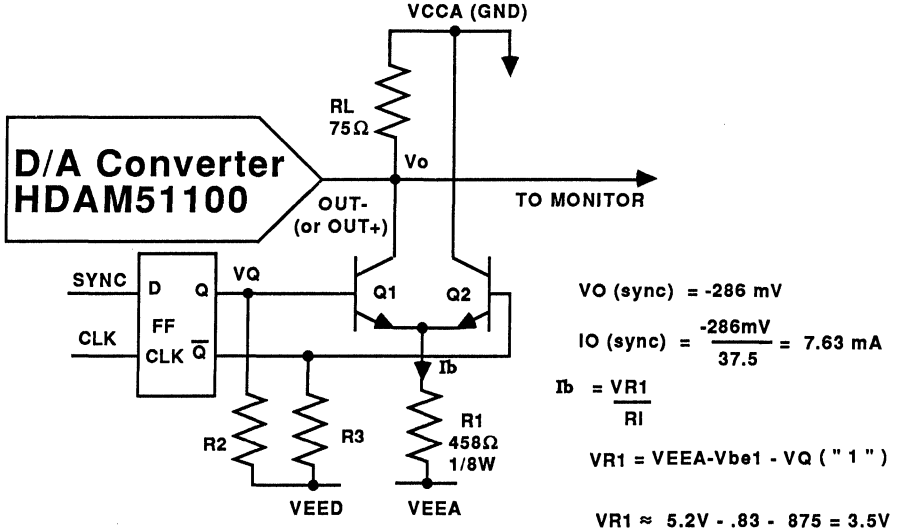
by Tom DeLurio and Russ Moen

High speed Digital-to-Analog converters and multifunction DACs with memory or multiplexers do not always have on board video SYNC pulse control inputs. This Application Brief will offer solutions to overcome the absence of video sync control pins. If needed, the circuits can equally be used for blank or 10% bright funtions as well.

Although the majority of Honeywell Signal processing Technologies' High speed DACs have video sync control inputs, some do not. Since most of SPTs DAC products are current output type devices, the sync pulse can be added directly to the output pins. One option is shown in Figure 1 using the HDAM51100 DAC with memory. This device does not have on-board sync control.

The sync pulse level is generated using an ECL type flip-flop that is clocked in phase with the DAC clock to drive a matched transistor pair. Three flip-flops can be used in series to match the clock latency of the HDAM51100 or the time can be compensated for in software.

Another option is shown in Figure 2. Here, the sync circuit takes advantage of the voltage reference available from the DACs reference output pins. This circuit is more accurate and stable then the previous one but uses more components.



Q1,Q2 = Motorola MD918

R2, R3 = ECL loads for Flip-Flop.

R1, RL same resistor type if possible

FF Requires three to match HDAM51100 part latency or compensate in software. Other DACs will vary (see data sheet).

FIGURE 1 - Video DACs with external SYNC control.

8

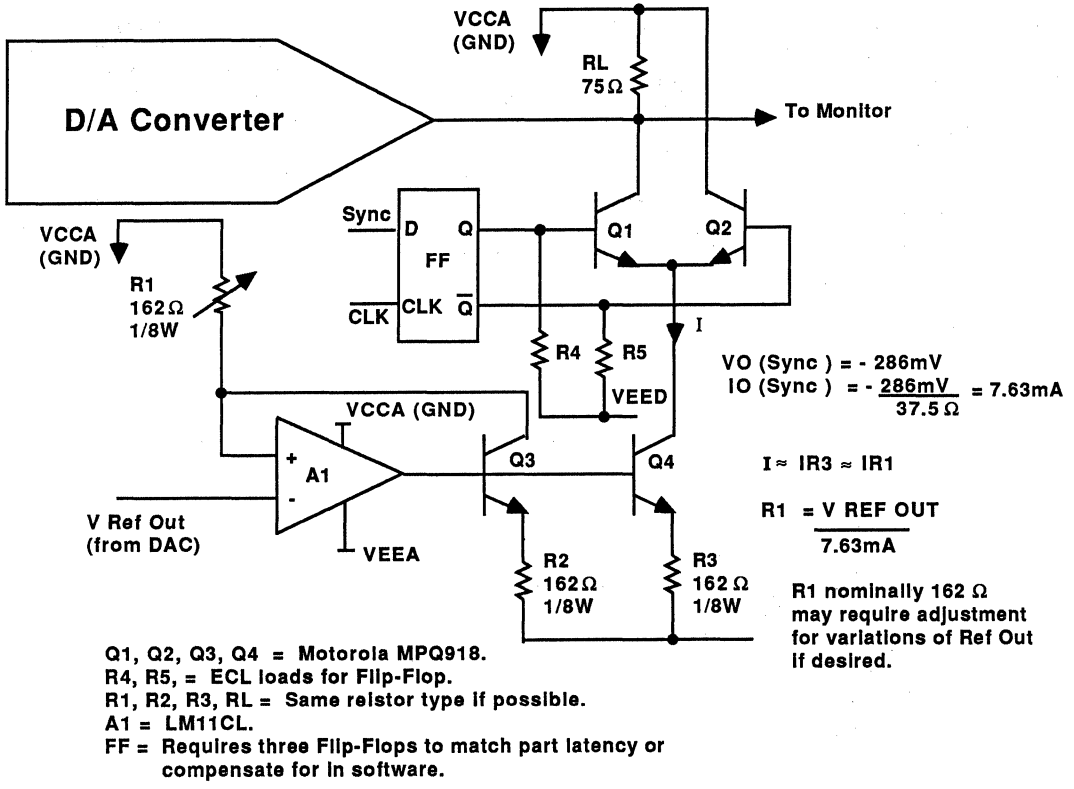


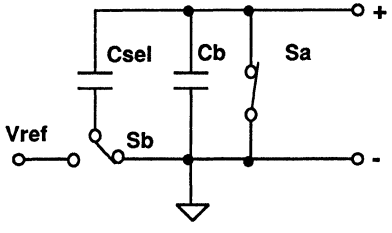
FIGURE 2 - Video DACs with external SYNC control using Internal voltage reference.

CHARGE SCALING DATA CONVERTERS

PAUL M. BROWN

High quality polysilicon MOS capacitors, inherent in Honeywell's CMOS process, have made it possible to replace the traditional data conversion technique of current scaling with charge scaling. This technique relies on carefully matched capacitors instead of matched resistors and current sources to accomplish digital to analog conversion. The advantages of this approach include ease of manufacture, low power consumption and an inherent sample-and-hold function that substantially improves analog-to-digital converter performance yet adds no extra components. This application brief will discuss the basic charge scaling DAC (digital-to-analog converter), how it functions and how it is used in The HADC574Z and the HADC674Z to achieve the "built in" sample-and-hold function.

Figure 1. Simple Capacitive Divider



$$Vout = Vref \frac{Csel}{Cb + Csel}$$

Charge scaling DAC's produce an analog output voltage by distributing charge in an array of binary weighted capacitors. The weighting of the capacitive divider is determined by the incomming digital code. Figure 1 illustrates a basic capacitive divider circuit. This circuit functions in two steps. In step 1, switch Sa is closed and switch Sb is connected to ground, discharging both Csel and Cb. In step 2, Sa is opened and Sb is connected to the reference voltage Vref. Due to the relative values of Cb and Csel and the charge distribution between them, Vref is divided between the two capacitors such that Vout = Vref X Csel/(Cb+Csel).

Figure 2 illustrates how a capacitive DAC is implemented using the above approach. Csel is the sum of all capacitors selected by the data bits to be connected to Vref and Cb is the balance of all other capacitors, including the termination capacitance, that remain connected to ground.

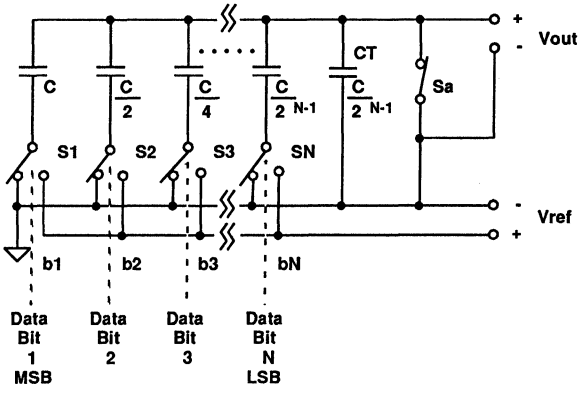
The total DAC capacitance, $Ctot = C + C/2 + C/4 + C/8 + ... + C/2^{N-1} + C/2^{N-1} = 2C$

$Ctot = Csel + Cb$

The total selected capacitance, $Csel = b_1C + b_2C/2 = b_3C/4 + ... + b_NC/2^{N-1}$ (where $b_1 ... b_N = 1$ or 0)

Vout = Vref X Csel/Ctot

Figure 2. Capacitor DAC



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The HADC574Z/674Z use the DAC in a slightly different manner (see figure 3). The DAC output is connected to one input of a comparator and a reference voltage is applied to the other comparator input. The conversion cycle begins with a "reset". The DAC is first "zeroed" to the analog input voltage with switch S1 closed. Next, S1 opens and the SAR (successive approximation register), under control of the comparator, sets the appropriate data bits to either Vref or ground to balance the comparator inputs. The significance of this is that the input voltage is sampled only during the "reset" period. Although there is no sample-and-hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z/674Z appear to have a built in sample-and-hold.

This sample-and-hold action substantially increases the signal bandwidth of the HADC574Z/674Z over that of similar competing devices.

EXAMPLE:

Assuming a sinusoidal signal, maximum slew rate, $Sr = 2\pi fVp$ (Vp = peak voltage)

For an N-bit converter to maintain +/- 1/2 LSB accuracy :

$Verr \leq Vfs/2^{N+1}$ (where Verr is the allowable error voltage and Vfs is the full scale voltage)

$Sr = \Delta V/\Delta T = 2\pi fVp$

Let ΔV = Verr, Vp = Vin/2 and ΔT = The time during which unwanted voltage changes can occur on the input signal.

This can be rewritten as:

$Vfs/2^{N+1} \geq \pi fVin\Delta T$

or

$f_{max} \leq Vfs/(\pi Vin\Delta T)2^{N+1}$

Let Vfs = Vin = 20V

AD574

ΔT = conversion time = 25µs typical

$f_{max} \leq 20V/[\pi(20V)(25\mu s)(2^{13})] = 1.55Hz$

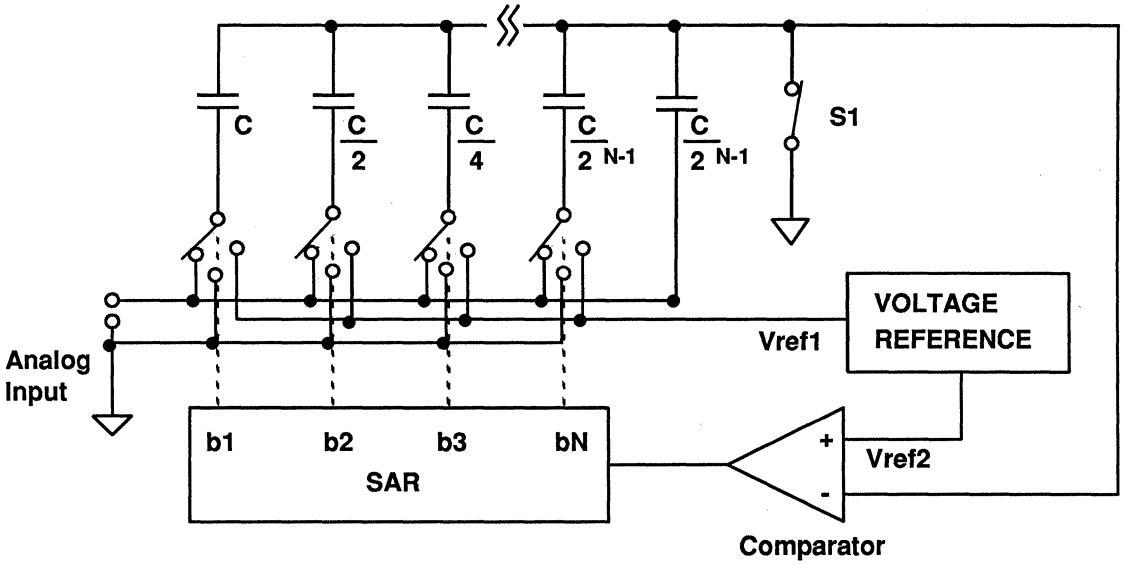
HADC574Z

ΔT = 20 ns typical (specified aperture uncertainty time)

$f_{max} \leq 20V/[\pi(20v)(20\ ns)(2^{13})] = 1.94kHz$

The HADC574Z has over a 1250:1 improvement in analog bandwidth with NO ADDITIONAL COMPONENTS!

Figure 3. HDAC574/675 DAC Configuration



HADC574Z AND HADC674Z ANALOG INPUT STRUCTURE

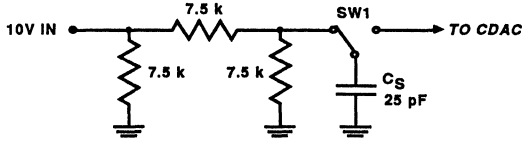
Craig Wiley

The capacitive DAC circuitry in the HADC574/674Z provides lower power dissipation, improved accuracy, and an inherent sample/hold function as compared to the traditional R-2R ladder DAC approach used in similar devices. In many applications this inherent sample/hold function can eliminate the need for an external sample/hold amplifier and provide superior performance. Additionally, it reduces the dependance on signal source characteristics during conversion eliminating the need for signal buffering. The sample/hold function of the HADC574/674Z can reduce the external circuitry requirements of data acquisition systems when used properly. This application brief will discuss the application, advantages and limitations of the HADC574/674Z analog input structure.

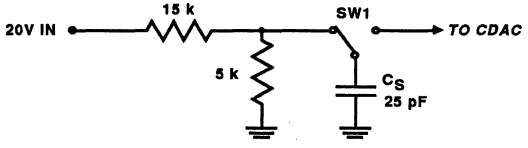
CONVERSION EVENTS

Operation of the HADC574/674Z can be broken into two basic events. The first event is referred to as the sample period and begins upon an initiation of conversion. During the sample period a capacitor array within the device is connected to the analog input and is allowed to charge to the external signal voltage. The second event, longer by comparison, is the successive-approximation operation utilizing the CDAC. During the conversion period, the internal sample capacitance is switched from the input to the internal CDAC circuitry. As shown in the simplified circuit equivalent of Figure 1, SW1 is used to transfer the capacitance Cs from the input to the CDAC circuitry. Actually, SW1 consists of several parallel MOSFET switches and Cs is a capacitor array that performs the CDAC function. Please refer to application brief AB102 for more information on charge scaling data converters.

Conversion event timing of the HADC574/674Z devices is determined by an internal clock. By virtue of the differences between internal clock frequency, the HADC674Z exhibits a shorter total conversion time compared to the HADC574Z. This also results in a different sample period between the two devices which requires application considerations. Figure 2 shows the conversion event timing (minimum-maximum values) of both devices. For additional timing information please refer to the device data sheet.



10 VOLT INPUT RANGE



20 VOLT INPUT RANGE

FIGURE 1
SIMPLIFIED INPUT CIRCUIT
OF HADC574/674Z
Typical values shown

Compared to similar devices, the HADC574/674Z places less demand on the signal source stability and output characteristics. In the similar devices, the R-2R DAC is connected to the external signal source during the successive-approximation conversion operation. During the conversion, the signal source must remain stable to within a tolerable bit accuracy. Low output impedance and close proximity of the source are normally necessary to allow quick response to the changing DAC load. These requirements are normally met with a sample/hold or buffer amp. When using the HADC574/674Z's, however, direct connection can frequently be made to the voltage source without performance degradation.

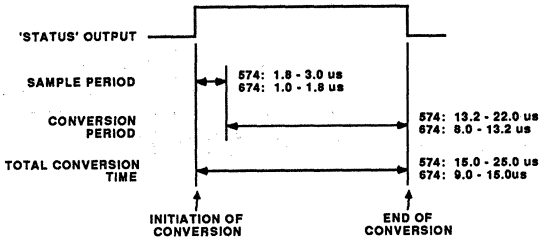


FIGURE 2
CONVERSION EVENT TIMING
OF HADC574/674Z

DC INPUT CHARACTERISTICS

The internal input scaling resistors in the HADC574/674Z have different impedance characteristics for the 10V IN and 20V IN analog input pins. The input resistance range of these pins is shown in Figure 3. When using a high signal source impedance, the attenuation caused by the internal input resistance must be considered. For example, a signal source with an output resistance of 5 kΩ driving the 10V IN pin, which has a 5 kΩ typical input resistance, would appear to have only half the signal value. Some of this error can by compensated by the external trim network (see data sheet), but drift can result due to thermal coefficient differences between the external and internal resistances. It is therefore important to keep the source impedance as low as possible.

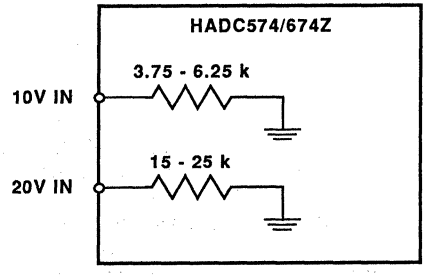


FIGURE 3
DC INPUT CHARACTERISTICS
OF HADC574/674Z

DYNAMIC INPUT CHARACTERISTICS

Input Settling

Although the sample/hold function of the HAC574/674Z provides utility, dynamically it is of modest performance when compared to dedicated sample/hold amplifiers. It can, however, provide superior noise immunity when sampling lower frequencies (below 5 kHz).

Figure 4 shows the electrical equivalent of the internal sample circuitry as it appears to Cs. The equivalent resistance using either input pin (10V IN or 20V IN) is equal, assuming zero source resistance. Figure 4 provides a usable first order approximation and ignores all other parasitic effects. The 4 kΩ resistance includes the resistance of SW1; in applications with high source resistance, source resistance effects should also be included. Charge resistance can be calculated from the circuits of Figure 1.

In Figure 4, the voltage across Cs over time is defined by:

$$\frac{e_c}{E} = 1 - e^{-t/RC} \quad \text{(equation 1)}$$

where: e_c = Voltage of Cs; E = Signal Voltage; t = time; R,C = Component Values of Figure 4.

To express Equation 1 in terms of time (t) to obtain a required charge voltage (e_c), we can rewrite equation 1 as:

$$t = -RC\ ln\ (1 - \frac{e_c}{E}) \quad \text{(equation 2)}$$

The design of a data acquisition system using the HADC574/674Z must take into account the total system settling time and the effect upon e_c, the captured signal voltage sample. The desired settling value of e_c must occur within the sample period of the device. Using equation 1, a full-scale step input will settle to within 1/2 LSB of final value in 0.9 µs. (For this calculation, (ec/E) = (4095.5/4096)). Using equation 2, the final value is within 1/5 LSB after 1 µs. Therefore, even when using the HADC674Z which has minimum sample period of 1µs, the pole introduced by the internal charge circuit is negligible.

Because this dynamically-limited sample/hold amplifier acts like a low-pass filter, it exhibits good noise immunity. An external sample/hold will usually be more susceptible to circuit noise. Even with an external sample/hold amplifier, the HADC574/674Z typically exhibits less input noise than similar 574/674 devices. Room temperature characterization shows that typical equivalent input noise of the HADC574/674Z is 1/5 LSB or 50 µV.

Dynamic Sampling Error

The bandwidth limitations of the HADC574/674Z's sample/hold feature are more apparent when performing dynamic sampling, that is, sampling of an active signal. For an AC signal voltage, the circuit of Figure 4 is low pass, phase-lag network. The transfer function of Figure 4 can be expressed as:

$$e_c = \frac{E}{1 + jwRC} \quad \text{(Equation 3)}$$

where: w = 2pf

The sample circuit equivalent, shown in Figure 4, can be viewed as a single-pole low-pass filter with a half power point at 1.6 MHz. Using equation 3, the 1/2 LSB magnitude attenuation of a full scale signal occurs at 25 kHz. At 10 kHz, the attenuation is only 0.08 LSB. As discussed in the following section, since 5 kHz is about the maximum usable range, the low-pass magnitude degradation imposes insignificant error.

Phase distortion in the input network is an important error to consider in dynamic sampling applications. As signal frequency goes up, higher reactance of the sample capacitor causes an increase in phase shift. Thus, a sampled waveform at one frequency appears to be delayed in time relative to a lower frequency. Phase shifting between frequencies is illustrated in Figure 5. Using equation 3 above, it can be determined that a full-scale sinusoidal signal is allowed a maximum frequency of 195 Hz if an amplitude error of 1/2 LSB (ΔV) maximum is allowed considering the phase shift in the time domain (Δt). Most analog data, however, is in the form of a complex waveform which consists of several fundamental frequencies. Sampling of a complex waveform with excessively high frequency components will result in a distorted digital representation.

Non-Apparent Dynamic Factors

Present architecture of the HADC574/674Z results in an inherent input slew rate limitation during the sample period described earlier. Slew rate adversely affects the switches composing SW1 in Figure 1. Problems will generally be found with slew rates above 0.25 V/µs into the 10V IN pin or 0.5 V/µs into the 20V IN pin. This corresponds to full-scale sinusoidal signal of 8 kHz into either pin. To avoid problems over all operating conditions, the maximum slew rate should be conservatively limited to 0.16 µV/s into 10V IN or 0.32 µV/s onto 20V IN. This places the conservative input frequency limit at 5 kHz for a full-scale sinusoidal signal. Exceeding the slew rate limitation during the sample period will result in an all "1" output for a positive-going input and an all "0" output for a negative-going input.

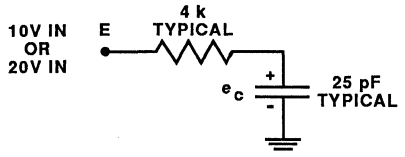


FIGURE 4
EQUIVALENT DYNAMIC CIRCUIT
OF HADC574/674Z

As described in the HADC574Z and HADC674Z data sheets, aperture jitter also places a limitation on the maximum usable input frequency. The specified 20 ns typical aperture jitter accounts for worst case changes in ambient temperature and power supply voltages. In application, however, sample-to-sample jitter typically less than 5 ns. Discrete-Fourier-transform (DFT) characterization of the HADC574Z has showed that the wide-bandwidth signal-to-noise ratio is approximately 72 dB down from the fundamental when using full-scale single-tone sinusoidal test signals up to 8 kHz. Above this frequency, the slew rate limitation described above greatly degradates the performance. Both the minimum aperture jitter and excellent linearity typically found with the HADC574/674Z provide a low dynamic distortion level which approaches ideal performance limited by 12-bit quantization error alone.

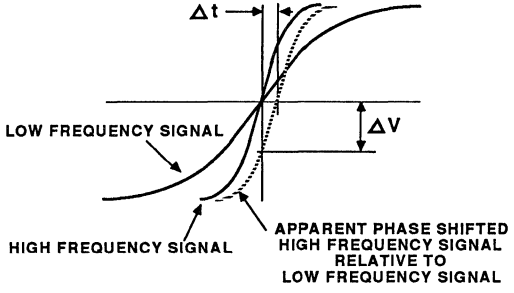


FIGURE 5
EFFECTS OF PHASE DISTORTION
THROUGH INPUT NETWORK

CONCLUSION

The analog input structure of the HADC574/674Z provides superior performance to that of similar 574/674 devices. In addition, the inherent sample/hold function can eliminate the need of an external sample/hold or buffer amplifier. Because of it's dynamic limitations, use of the internal sample/hold function is limited to lower-frequency (< 5 kHz) data-acquisition applications. Systems requiring temporal (phase) accuracy during dynamic sampling or that will sample signals over 5 kHz should use an external sample/hold amplifier.

TESTING THE HADC574Z AND HADC674Z ON THE LTS2020

Craig Wiley

Minor modifications of test hardware and software are needed in order to successfully test the Honeywell SPT HADC574Z or HADC674Z devices on the LTS2020 tester. The LTS2020 is a low-cost integrated circuit test system built by Analog Devices Incorporated and is commonly used as an Incoming Inspection test station. The HADC574/674Z devices offer enhanced performance but have slight differences in test requirements compared to 574/674 devices available from other manufacturers. Hardware modifications required for the HADC574/674Z will not effect the testing of similar pin-compatible devices.

This modification on the LTS0620 socket adapter involves changing relay K2 and making the appropriate wiring modifications. Using the LTS0620 schematic nomenclature, Figure 3 shows the board, as-is, and Figure 4 shows the modified version. For relay K2, a Coto 2211-05 is used to replace the existing Coto 2900-0017. The modification will provide a suitable range switching technique for the HADC574/674Z as well as all pin-compatible 574/674 devices. No software changes are required for this modification.

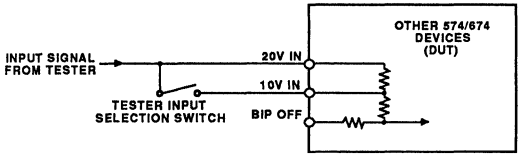


FIGURE 1
LTS2020 INPUT RANGE SWITCHING TECHNIQUE
Input structure of device shown is of 574/674 devices

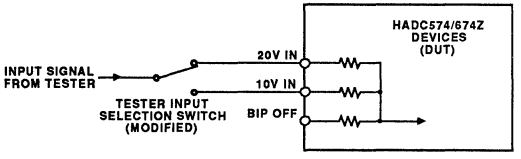


FIGURE2
MODIFIED LTS2020 INPUT RANGE SWITCHING TECHNIQUE
Input structure of device shown is of HADC574/674Z

HARDWARE MODIFICATION

The hardware modification involves a minor change to the LTS0620 socket adapter which fits into the LTS2200-ADC family board. The socket adapter, as-is, takes advantage of the input structure common to 574/674 devices by other manufacturers. A single-pole relay is used to switch between to 20V IN and 10V IN pins of the device. This relay configuration is illustrated in Figure 1. The HADC574/674Z devices, due to the more accurate input architecture, will not function properly with this simplified switching scheme and instead requires a double pole relay as shown in Figure 2.

SOFTWARE MODIFICATIONS

Testing of HADC574/674Z devices require some software changes since the LTS2020 574/674 test software is written for the similar bipolar devices. First, since HADC574/674Z devices use the BEMOS process, the limits for the power supply current tests need to be lowered. Second, since HADC574/674Z devices do not use a -15 Volt supply (VEE pin is not internally connected) the -15 Volt tests need to be bypassed. And last, because of the internal sample/hold function, the ratio between the 8-bit and 12-bit conversion times differs from similar 574/674 devices (although they still comply with the specifications).

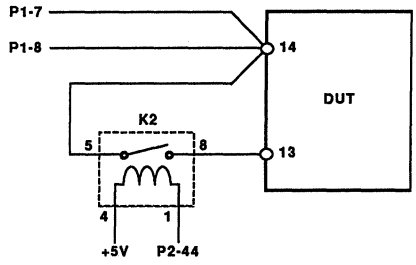


FIGURE 3
UNMODIFIED LTS0620 WIRING AS REPRESENTED BY FIGURE 1

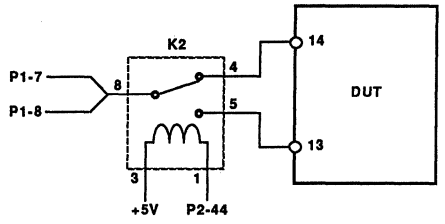


FIGURE 4
MODIFIED LTS0620 WIRING AS REPRESENTED BY FIGURE 2

The test programs available for the LTS2020 tester are the AD574_HG for testing 574 devices and the AD674_HG for testing 674 devices. The modifications of these programs for successful testing of the HADC574Z and HADC674Z devices are listed below. These modified test programs will not be suitable for testing similar 574/674 devices and should therefore be given new names avoid confusion.

AD574_HG and AD674_HG Test Program Changes:	*(Comments:)*
1) Line 310, change LL (Lower Limit) to -0.1and UL (Upper Limit) to +3 (mA)	*(New +5 Volt supply c ırrent limits)*
2) Line 340, change LL to 0 and UL to 10 (mA)	*(New +15 Volt supply current limits)*
3) Add line 355 "GOTO 380"	*(Skips -15 Volt supply test since this pin is unconnected)*
4) Line 86, change "E" conversion factor to 0.75.	*(New 8-bit conversion time limit)*
5) Add line 1005 "GOTO 1060".	*(Skips -15 Volt pin PSSR test)*

Quality Assurance

Quality and reliability of electronic components are critical issues at Honeywell Signal Processing Technologies. Customers integrate large portions of their finished products into silicon using SPT's complex high performance integrated circuits. The quality and reliability of the end products therefore, depend heavily upon the integrated circuits they contain. Realizing the intimate relationship between its customers' success and its own, SPT has put into place a continually improving quality assurance system that makes its products among the highest quality and most reliable components available.

Quality and reliability, frequently thought to be synonymous, have quite different meanings. Quality implies that a device initially conforms to a given set of performance criteria. Reliability implies that a device continuously meets a given set of performance criteria. Figure 1 illustrates the traditional "Bathtub" Failure Rate Curve. A given sample of unscreened devices that initially meet their published specifications (high quality) will tend to have a relatively high initial failure rate (infant mortality) due to parameter drift or manufacturing defects that have gone undetected during the manufacturing process (low reliability). The failure rate during the "normal life" period is affected by devices with latent failure mechanisms that normally exhibit themselves during the infant mortality period and some devices that prematurely "wear out". Failure during the "wear out" period is caused by metal migration, long term drifts, corrosion and package failure. SPT insures the high quality of its product with rigorous 100% electrical testing. Product reliability is designed in and insured through comprehensive QA (Quality Assurance) monitoring throughout the manufacturing process and screening of the final product.

Screening operations are designed to "weed out" potential infant mortality failures before they are shipped to customers. The screening procedures that SPT uses are described below with the failure mechanisms they are designed to catch.

Pre-seal Visual

Wire bonding, die bonding, package, package leads and die are visually inspected using both a high and low power microscope. Many of the defects detectable during this inspection such as defective wire bonds, contamination, scratched metalization or other defects on the die contribute to infant mortality. This inspection is performed just prior to sealing the device.

Bond Strength

This sample test verifies the mechanical strength of the wire bond. Metalization and interconnection failures (typically opens or shorts) account for nearly half of IC failures.

Stabilization

The devices are heated to 150°C in an oven for 24 hours without electrical stress. This procedure is used as a preconditioning for subsequent testing.

Temperature Cycling

The devices are cooled to − 55°C for 10 minutes then elevated to + 150°C for 10 minutes with a 5 minute transfer time in-between. This procedure is carried out 10 times. Variations in physical dimensions of defective packages can cause loss of package integrity, cracking of passivation on the die, and changes in operating characteristics due to mechanical stress. This test is performed without electrical stress.

Constant Acceleration

The monolithic devices are subjected to 30,000 gs for 1 minute in the Y1 plane. This test is performed without electrical stress and can uncover mechanical weakness that was not detected by temperature cycling. Gold wire bonds are effectively tested for integrity in cavity packages (packages in which the bond wires are not encapsulated). The test is not as conclusive for aluminum wires (due to their lighter weight). Cracked die, weak die bonds, poor lid seals and improperly dressed bonding wires can also be detected during this test.

Hermetic Seal

Fine Leak
The units are placed in a helium filled vessel under 60 psig for at least 1 hour. Helium will enter the die cavity through any cracks or pin holes. The devices are removed and placed into the test chamber of a mass spectrometer leak detector. Any helium that entered the package during the previous procedure will be drawn out by the vacuum in the test chamber. The leak rate is measured by the spectrometer. An alternative method with equal or greater sensitivity using Krypton gas may be substituted for this test.

Gross Leak
After the completion of the fine leak test (if applicable), the gross leak test is performed to test for leaks greater than 10^{-3} ATM CC/sec. The devices are placed in a vacuum/pressure chamber at 5 torr for 1 hour. Before breaking the vacuum the units are covered with liquid FC-72. The pressure is then raised to 60 psig for two hours. The devices are removed from the vacuum/pressure vessel and submerged 2 in. in FC-43, heated to 125°C, for 30 seconds and visually checked for bubbles.

These tests evaluate package integrity and detect devices that might fail when exposed to an environment containing moisture or gaseous contaminants.

Pre Burn-In Electrical Test

Devices are tested 100% at 25°C for DC parameters (AC parameters and temperature extremes as required) to detect any electrical anomalies induced by the previous mechanical and thermal stresses. Serialized devices that will be burned-in may have some parameters logged at this point to test for parameter drift after burn-in is completed.

Burn-In

Burn-in is performed for a specified number of hours at 125°C with the device electrically stressed. This procedure eliminates devices with parameters that are marginal or have latent defects. Intermittent shorts caused by pinholes in the passivation will tend to become permanently shorted. Metal that is almost discontinuous due to scratches or cracks will tend to open. Corrosion and contamination on the die will tend to impact the circuit performance and will be detectable during the post burn-in electrical testing.

Post Burn-In Electrical Test

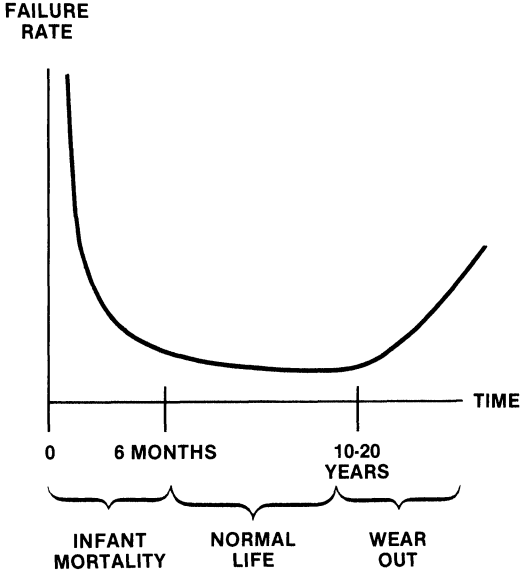
Devices are tested 100% at 25°C for DC parameters (AC parameters and temperature extremes as required) to insure that after all applicable screening the devices perform as specified.

External Visual

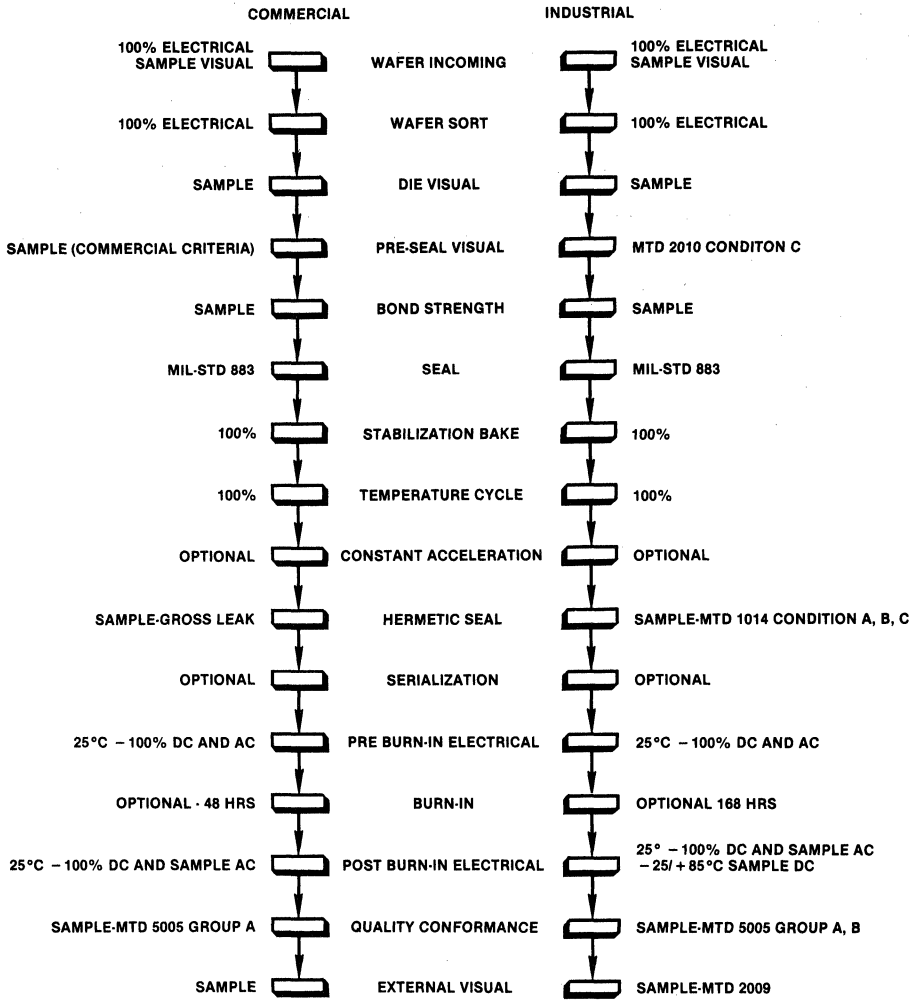
This final optical inspection insures that the packages and leads appear defect free.

Figure 2 summarizes the screening procedure and the failure mechanisms they are designed to detect. Figure 3 Quality Flow Diagrams illustrate the standard processing for SPT's various product grades. Special quality flows can be tailored to specific customer needs.

FIGURE 1: "BATHTUB" FAILURE-RATE CURVE

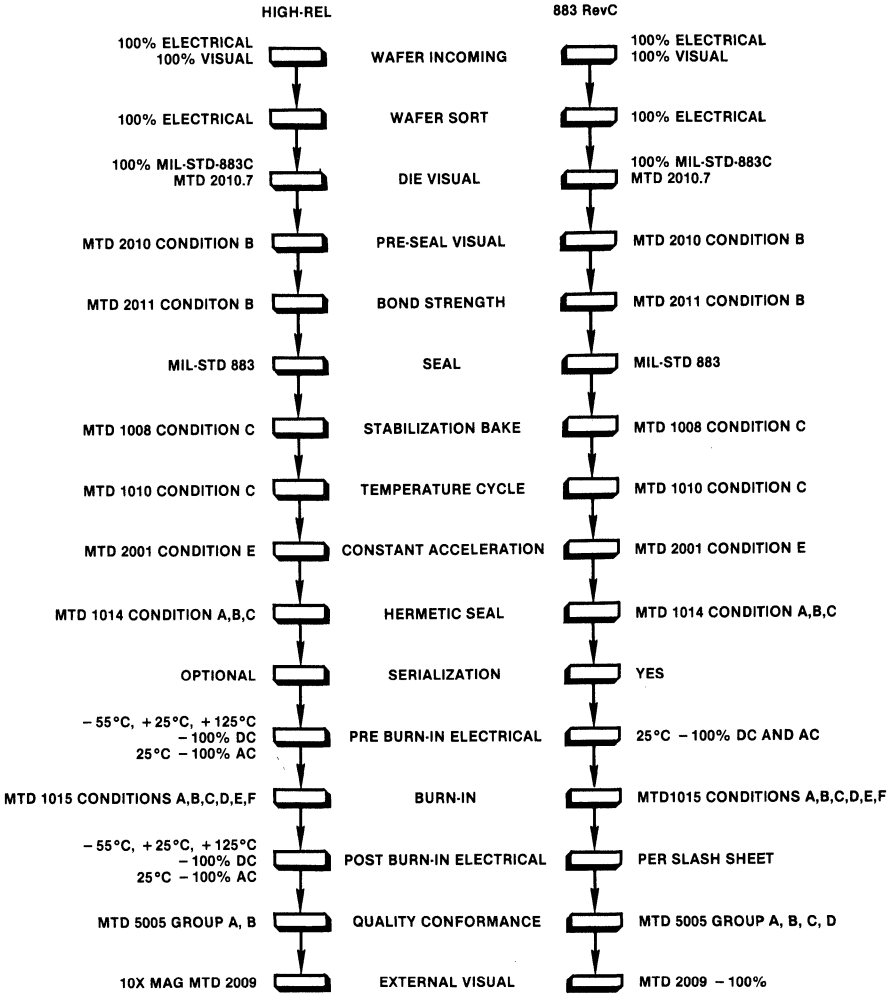


IN-LINE MANUFACTURING FLOW CHART FOR HERMETIC CAVITY TYPE PACKAGES



Honeywell

IN-LINE MANUFACTURING FLOW CHART FOR HERMETIC CAVITY TYPE PACKAGES



NOTE:
GROUP A: ELECTRICAL CHARACTERISTICS
GROUP B: PACKAGE ORIENTED TESTS
GROUP C: LIFE TESTS — PERIODIC CONFORMANCE
GROUP D: ENVIRONMENTAL TESTS — PERIODIC CONFORMANCE

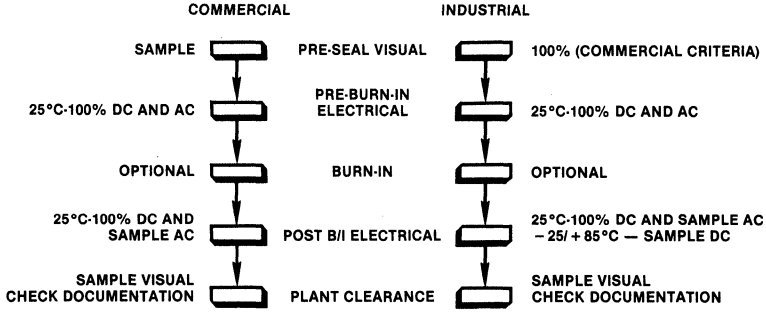
FIGURE 2: FAILURE DETECTION SUMMARY

FAILURE MECHANISM DETECTED

Procedure	wire bonds	die bonds	loose particles	process related	surface contamination	passivation failure	defective metalization	defective package	package seal	thermal stress	package leads	electrical failure
Pre-seal Visual	✓	✓	✓	✓			✓	✓				
Bond Strength	✓											
Stabilization Bake	✓	✓		✓	✓							
Temperature Cycle	✓	✓			✓			✓	✓	✓		
Constant Acceleration	✓	✓						✓				
Leak Test								✓	✓			
Pre Burn-In Electrical												✓
Burn-In					✓	✓	✓	✓				✓
Post Burn-In Electrical												✓
External Visual								✓			✓	

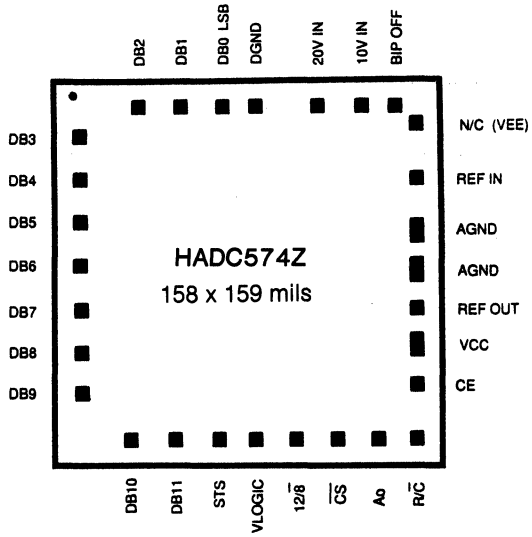
FIGURE 3: QUALITY FLOW DIAGRAMS

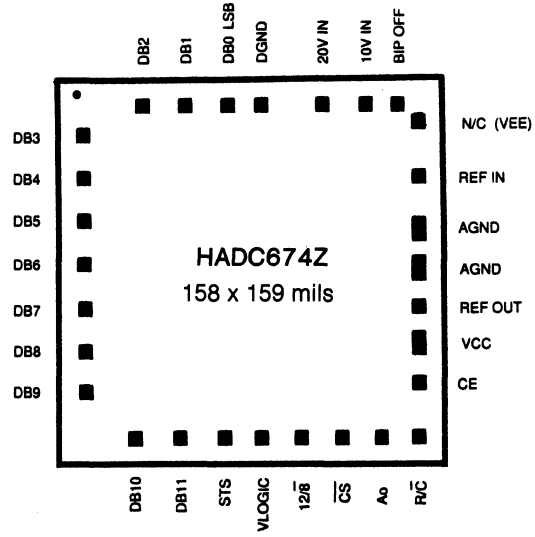
IN-LINE FLOW CHART FOR TRANSFER MOLDED (PLASTIC) AND NON-HERMETIC CAVITY TYPE PACKAGES

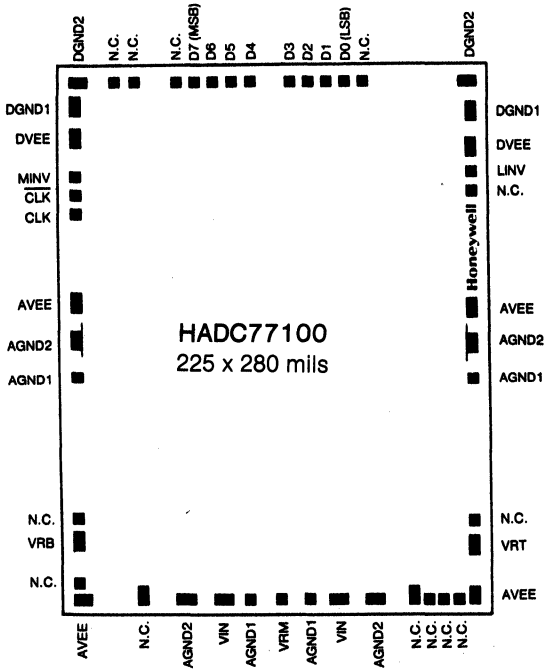


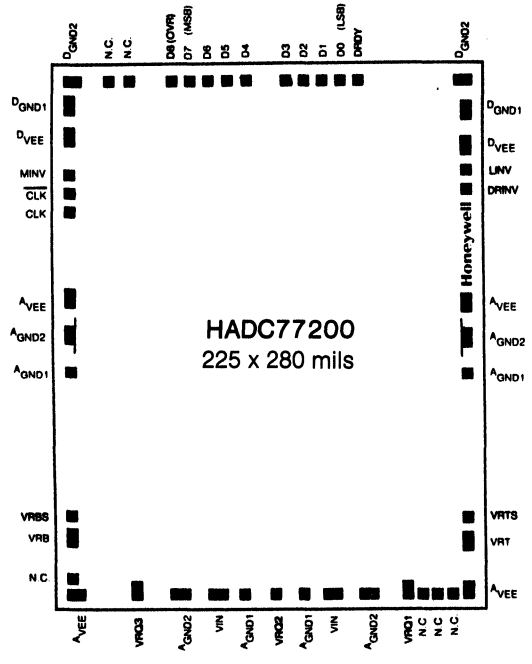
Honeywell

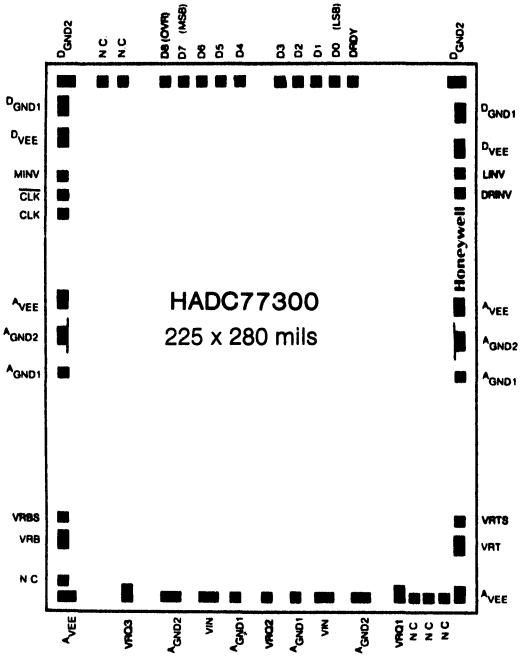
DIE PLOTS

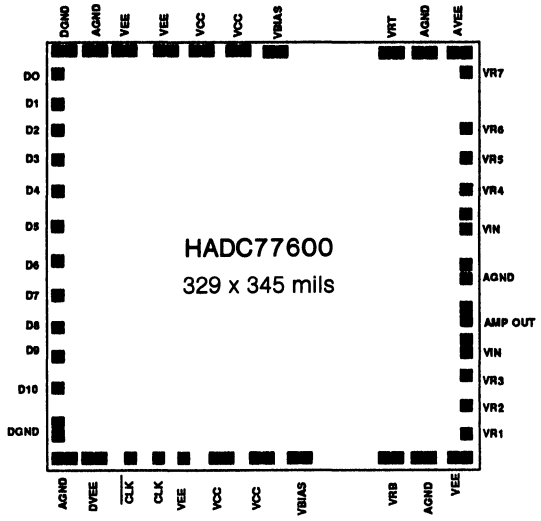

DB2
DB1
DB0 LSB
DGND
20V IN
10V IN
BIP OFF
DB3
DB4
DB5
DB6
DB7
DB8
DB9
N/C (VEE)
REF IN
AGND
AGND
REF OUT
VCC
CE
HADC574Z
158 x 159 mils
DB10
DB11
STS
VLOGIC
12/8
CS
A0
R/C

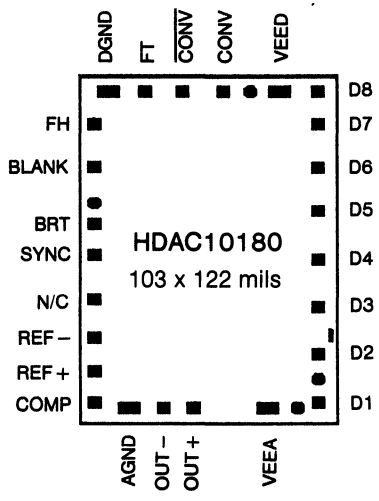

DB2
DB1
DB0 LSB
DGND
20V IN
10V IN
BIP OFF
DB3
DB4
DB5
DB6
DB7
DB8
DB9
N/C (VEE)
REF IN
AGND
AGND
REF OUT
VCC
CE
HADC674Z
158 x 159 mils
DB10
DB11
STS
VLOGIC
12/8
CS
A0
R/C

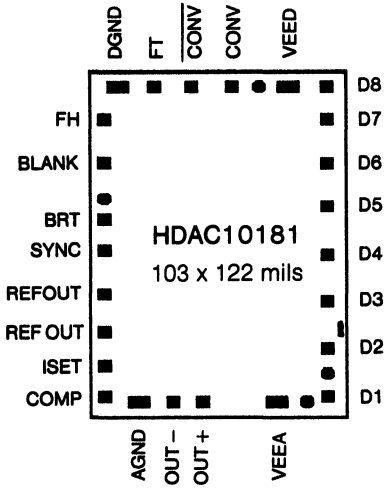

DGND2
N.C.
N.C.
N.C.
D7 (MSB)
D6
D5
D4
D3
D2
D1
D0 (LSB)
N.C.
DGND2
DGND1
DVEE
MINV
CLK
CLK
AVEE
AGND2
AGND1
N.C.
VRB
N.C.
HADC77100
225 x 280 mils
Honeywell
DGND1
DVEE
LINV
N.C.
AVEE
AGND2
AGND1
N.C.
VRT
AVEE
AVEE
N.C.
AGND2
VIN
AGND1
VRM
AGND1
VIN
AGND2
N.C.
N.C.
N.C.
N.C.


DGND2
N.C.
N.C.
D8 (OVR)
D7 (MSB)
D6
D5
D4
D3
D2
D1
D0 (LSB)
DRDY
DGND2
DGND1
DVEE
MINV
CLK
CLK
AVEE
AGND2
AGND1
VRBS
VRB
N.C
HADC77200
225 x 280 mils
Honeywell
DGND1
DVEE
LINV
DRINV
AVEE
AGND2
AGND1
VRTS
VRT
AVEE
AVEE
VRG3
AGND2
VIN
AGND1
VRG2
AGND1
VIN
AGND2
VRG1
N.C
N.C
N.C

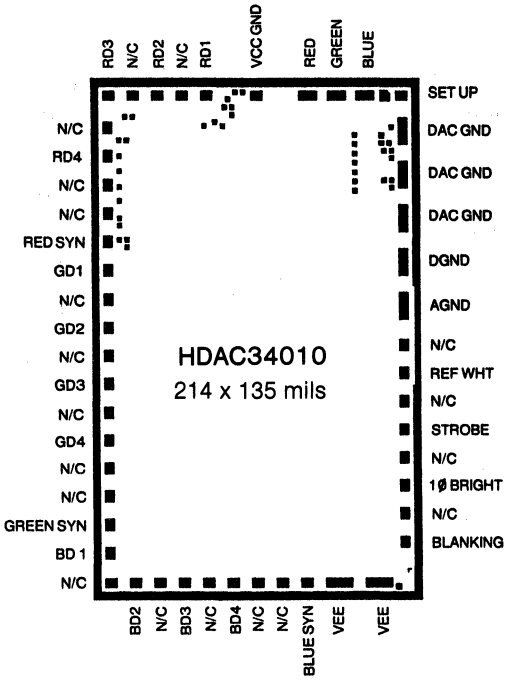

HADC77300
225 x 280 mils

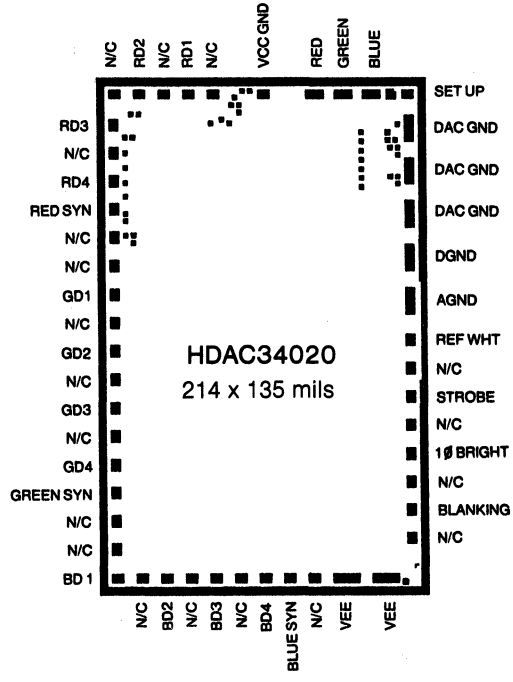

HADC77600
329 x 345 mils

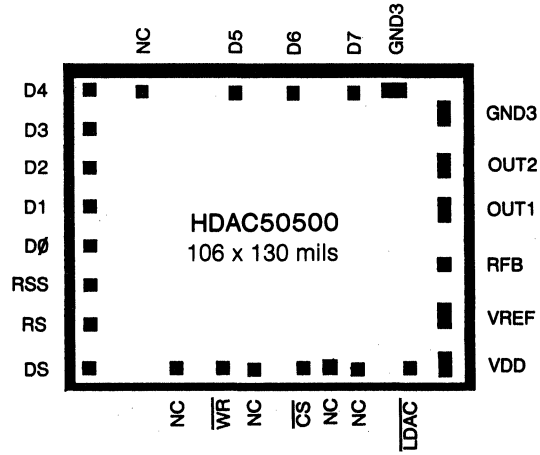

HDAC10180
103 x 122 mils

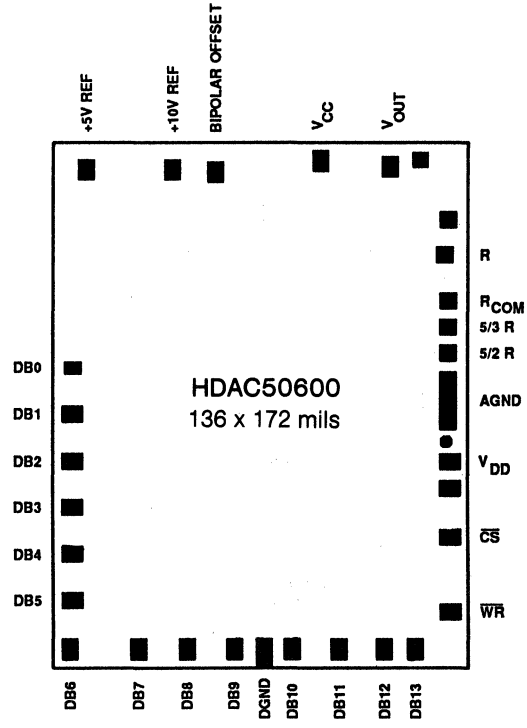

HDAC10181
103 x 122 mils

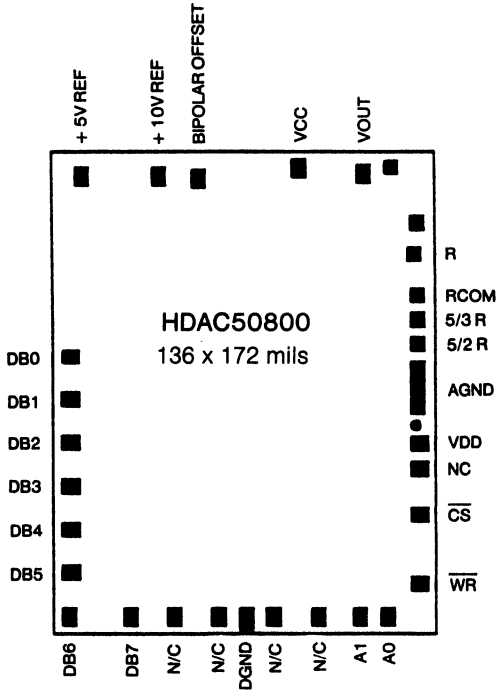
10

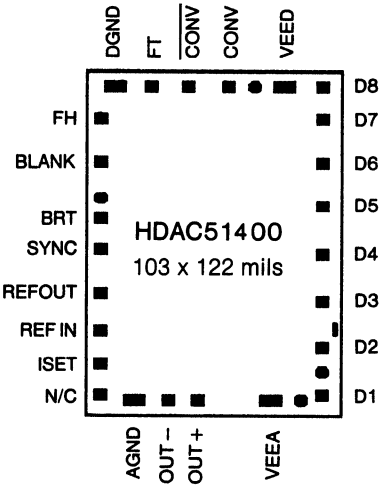

HDAC34010
214 x 135 mils
RD3
N/C
RD2
N/C
RD1
VCC GND
RED
GREEN
BLUE
SET UP
DAC GND
DAC GND
DAC GND
DGND
AGND
N/C
REF WHT
N/C
STROBE
N/C
1Ø BRIGHT
N/C
BLANKING
N/C
BD 1
N/C
GREEN SYN
N/C
N/C
BLUE SYN
N/C
BD4
N/C
BD3
N/C
BD2
VEE
VEE
N/C
RD4
N/C
N/C
RED SYN
GD1
N/C
GD2
N/C
GD3
N/C
GD4

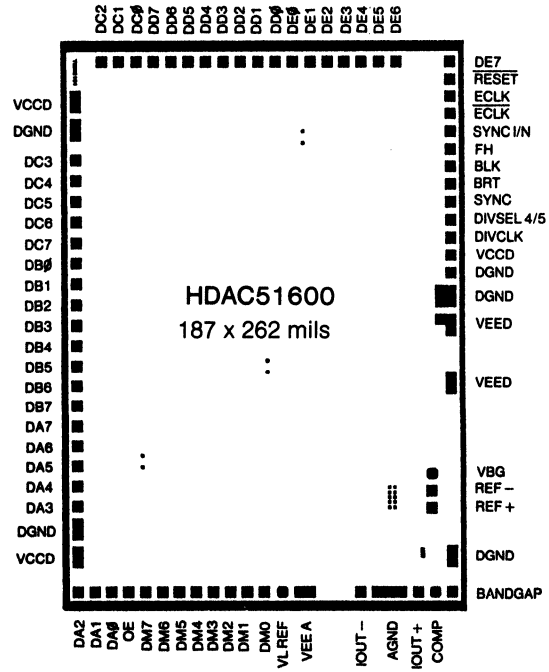

HDAC34020
214 x 135 mils
N/C
RD2
N/C
RD1
N/C
VCC GND
RED
GREEN
BLUE
SET UP
DAC GND
DAC GND
DAC GND
DGND
AGND
REF WHT
N/C
STROBE
N/C
1Ø BRIGHT
N/C
BLANKING
N/C
BD 1
N/C
GREEN SYN
N/C
N/C
BLUE SYN
N/C
BD4
N/C
BD3
N/C
BD2
VEE
VEE
RD3
N/C
RD4
RED SYN
N/C
N/C
GD1
N/C
GD2
N/C
GD3
N/C
GD4

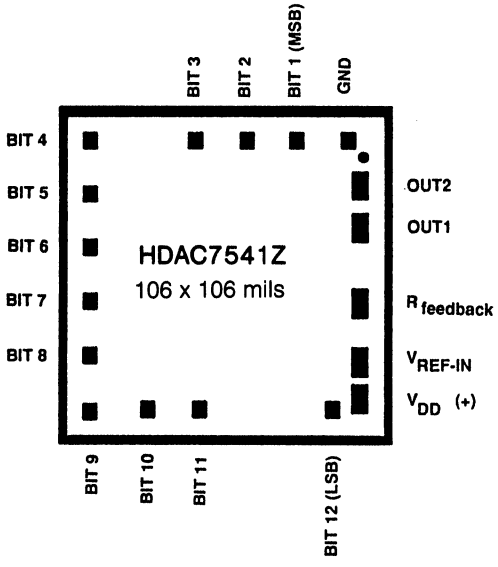

HDAC50500
106 x 130 mils
NC
D5
D6
D7
GND3
GND3
OUT2
OUT1
RFB
VREF
VDD
NC
WR
NC
CS
NC
NC
LDAC
D4
D3
D2
D1
DØ
RSS
RS
DS


HDAC50600
136 x 172 mils
+5V REF
+10V REF
BIPOLAR OFFSET
VCC
VOUT
R
RCOM
5/3 R
5/2 R
AGND
VDD
CS
WR
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DGND
DB10
DB11
DB12
DB13

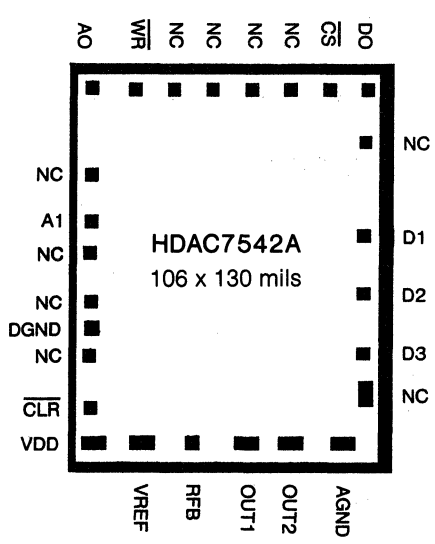

+ 5V REF
+ 10V REF
BIPOLAR OFFSET
VCC
VOUT
HDAC50800
136 x 172 mils
DB0
DB1
DB2
DB3
DB4
DB5
R
RCOM
5/3 R
5/2 R
AGND
VDD
NC
CS
WR
DB6
DB7
N/C
N/C
DGND
N/C
N/C
A1
A0

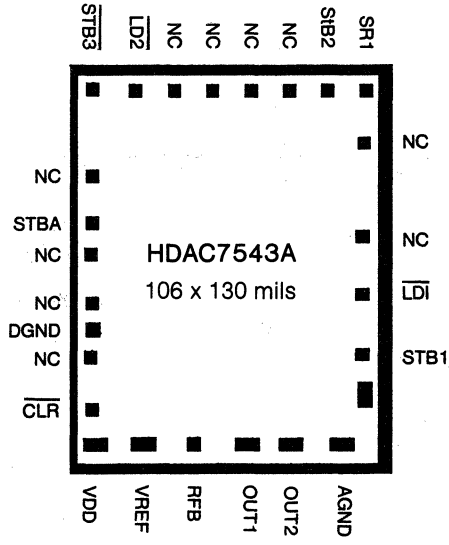

DGND
FT
CONV
CONV
VEED
HDAC51400
103 x 122 mils
FH
BLANK
BRT
SYNC
REFOUT
REF IN
ISET
N/C
D8
D7
D6
D5
D4
D3
D2
D1
AGND
OUT –
OUT +
VEEA

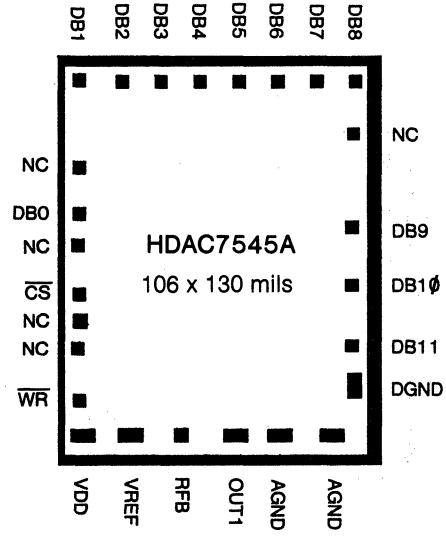

HDAC51600
187 x 262 mils
VCCD
DGND
DC3
DC4
DC5
DC6
DC7
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DA7
DA6
DA5
DA4
DA3
DGND
VCCD
DE7
RESET
ECLK
ECLK
SYNC I/N
FH
BLK
BRT
SYNC
DIVSEL 4/5
DIVCLK
VCCD
DGND
DGND
VEED
VEED
VBG
REF –
REF +
DGND
BANDGAP
DA2
DA1
DAØ
OE
DM7
DM6
DM5
DM4
DM3
DM2
DM1
DM0
VLREF
VEE A
IOUT –
AGND
IOUT +
COMP

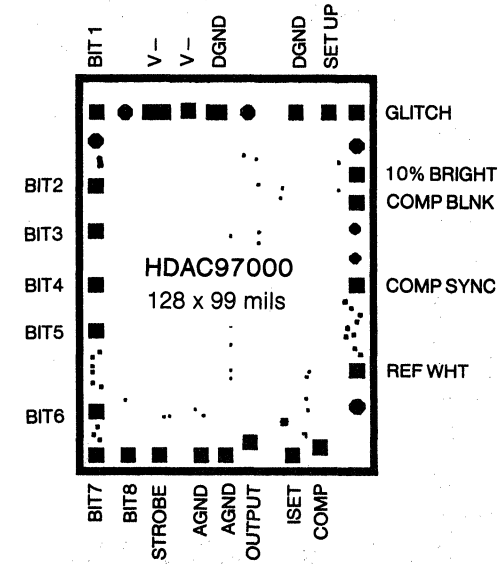

BIT 3
BIT 2
BIT 1 (MSB)
GND
HDAC7541Z
106 x 106 mils
BIT 4
BIT 5
BIT 6
BIT 7
BIT 8
OUT2
OUT1
R feedback
VREF-IN
VDD (+)
BIT 9
BIT 10
BIT 11
BIT 12 (LSB)

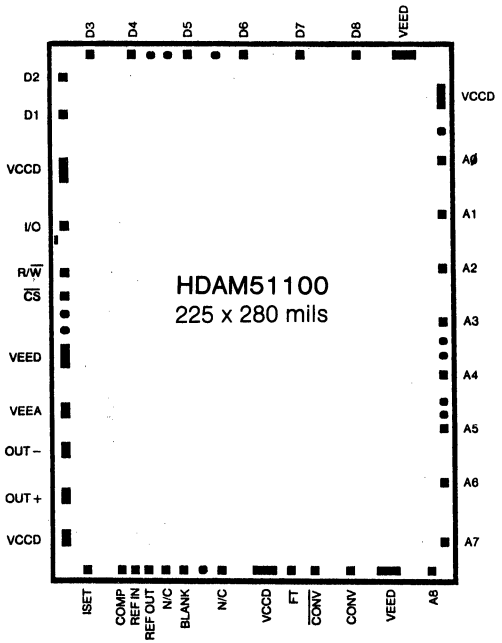
10

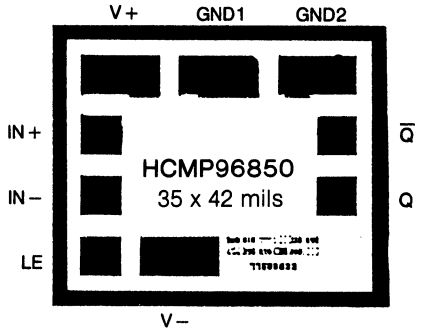

A0
WR
NC
NC
NC
NC
CS
DO
NC
NC
A1
NC
NC
DGND
NC
CLR
VDD
HDAC7542A
106 x 130 mils
NC
D1
D2
D3
NC
VREF
RFB
OUT1
OUT2
AGND

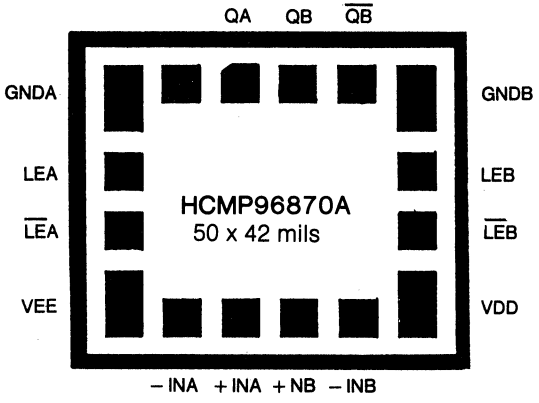

STB3
LD2
NC
NC
NC
NC
STB2
SR1
NC
NC
STBA
NC
NC
DGND
NC
CLR
HDAC7543A
106 x 130 mils
NC
NC
LDI
STB1
VDD
VREF
RFB
OUT1
OUT2
AGND

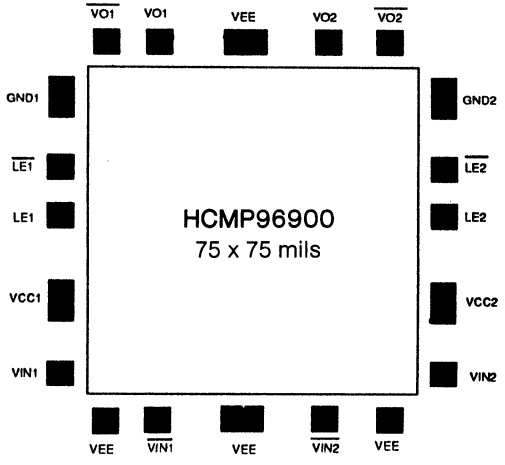

DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
NC
NC
DB0
NC
CS
NC
NC
WR
HDAC7545A
106 x 130 mils
NC
DB9
DB10
DB11
DGND
VDD
VREF
RFB
OUT1
AGND
AGND


BIT 1
V–
V–
DGND
DGND
SET UP
BIT2
BIT3
BIT4
BIT5
BIT6
HDAC97000
128 x 99 mils
GLITCH
10% BRIGHT
COMP BLNK
COMP SYNC
REF WHT
BIT7
BIT8
STROBE
AGND
AGND
OUTPUT
ISET
COMP

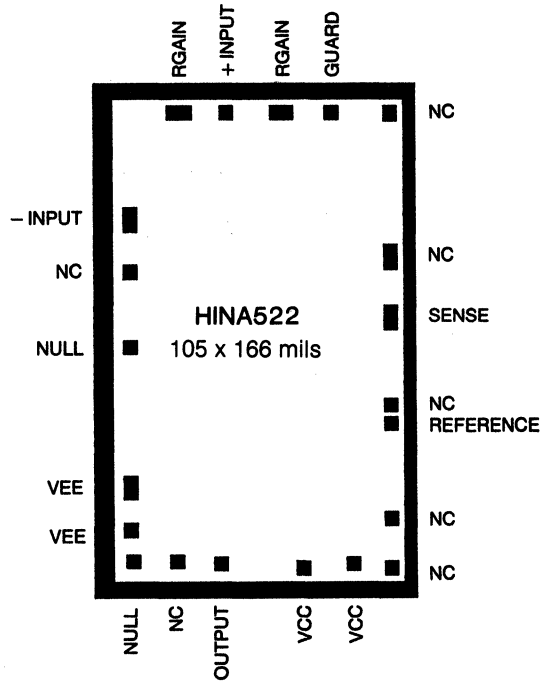

D3
D4
D5
D6
D7
D8
VEED
D2
D1
VCCD
I/O
R/W
CS
VEED
VEEA
OUT–
OUT+
VCCD
VCCD
A0
A1
A2
A3
A4
A5
A6
A7
HDAM51100
225 x 280 mils
ISET
COMP
REF IN
REF OUT
N/C
BLANK
N/C
VCCD
FT
CONV
CONV
VEED
A8

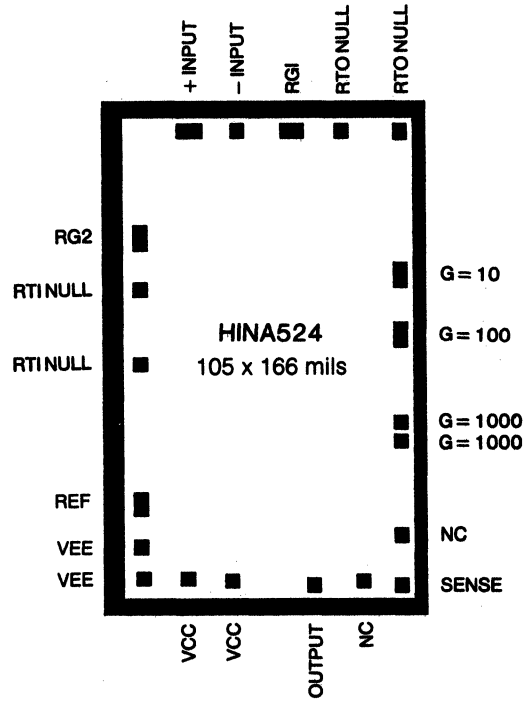

V+
GND1
GND2
IN+
IN–
LE
Q
Q
HCMP96850
35 x 42 mils
V–

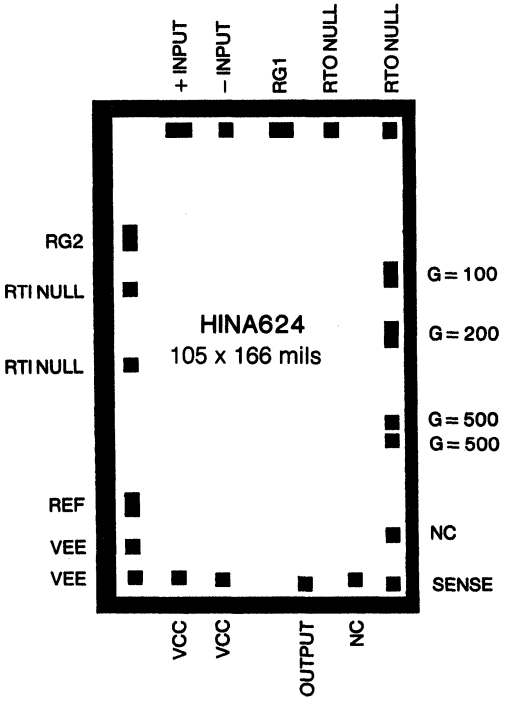

QA
QB
QB
GNDA
LEA
LEA
VEE
GNDB
LEB
LEB
VDD
HCMP96870A
50 x 42 mils
– INA
+ INA
+ NB
– INB

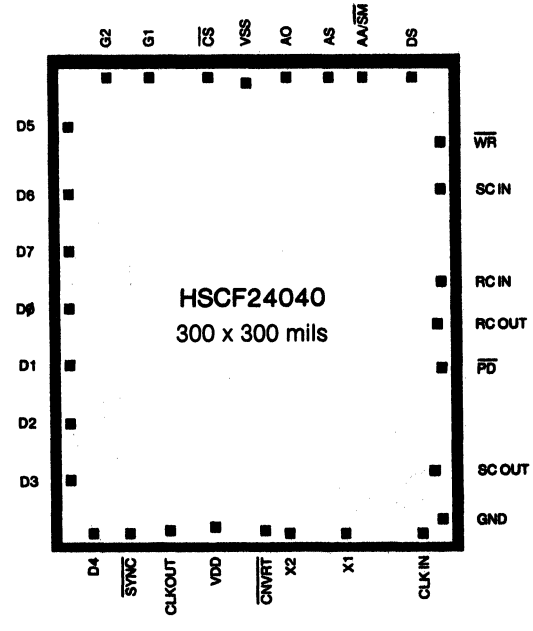

VO1
VO1
VEE
VO2
VO2
GND1
LE1
LE1
VCC1
VIN1
GND2
LE2
LE2
VCC2
VIN2
HCMP96900
75 x 75 mils
VEE
VIN1
VEE
VIN2
VEE

10


RGAIN
+ INPUT
RGAIN
GUARD
NC
– INPUT
NC
NC
SENSE
NULL
NC
REFERENCE
VEE
VEE
NC
NC
NULL
NC
OUTPUT
VCC
VCC
HINA522
105 x 166 mils

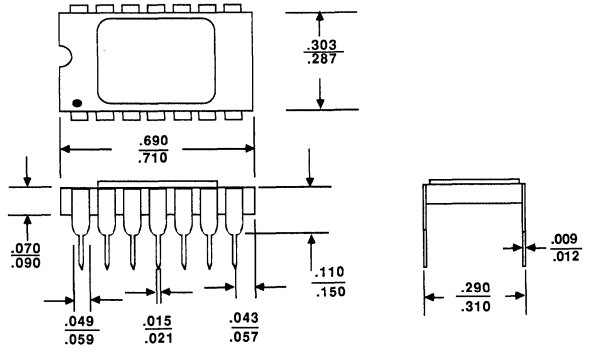

+ INPUT
– INPUT
RGI
RTO NULL
RTO NULL
RG2
G = 10
RTI NULL
G = 100
RTI NULL
G = 1000
G = 1000
REF
NC
VEE
VEE
SENSE
VCC
VCC
OUTPUT
NC
HINA524
105 x 166 mils


+ INPUT
– INPUT
RG1
RTO NULL
RTO NULL
RG2
G = 100
RTI NULL
G = 200
RTI NULL
G = 500
G = 500
REF
NC
VEE
VEE
SENSE
VCC
VCC
OUTPUT
NC
HINA624
105 x 166 mils

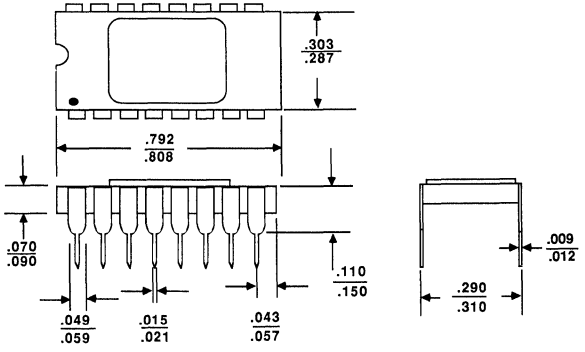

G2
G1
CS
VSS
A0
AS
AA/SM
DS
D5
WR
D6
SC IN
D7
RC IN
D8
RC OUT
D1
PD
D2
D3
SC OUT
GND
D4
SYNC
CLKOUT
VDD
CNVRT
X2
X1
CLK IN
HSCF24040
300 x 300 mils

PACKAGING INFORMATION

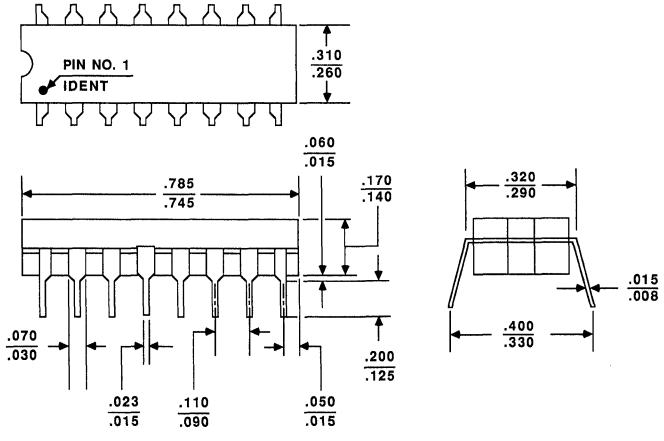
14 LEAD SIDBRAZED



16 LEAD SIDEBRAZED

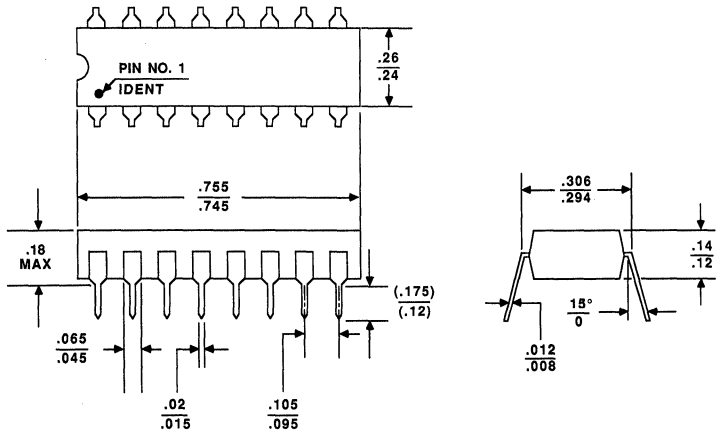


16 LEAD CERDIP

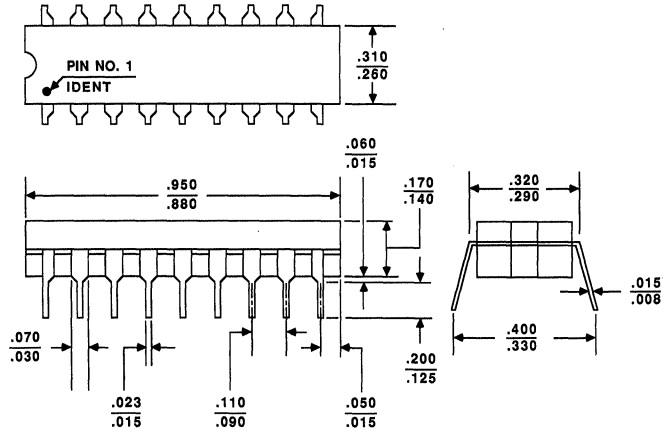


10

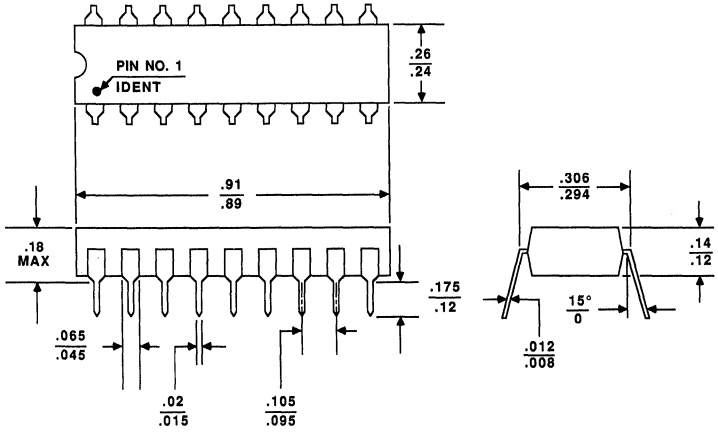
16 LEAD PLASTIC



18 LEAD CERDIP

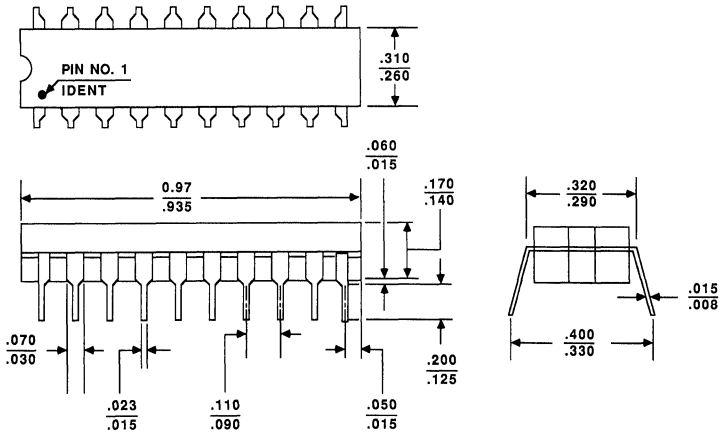


18 LEAD PLASTIC

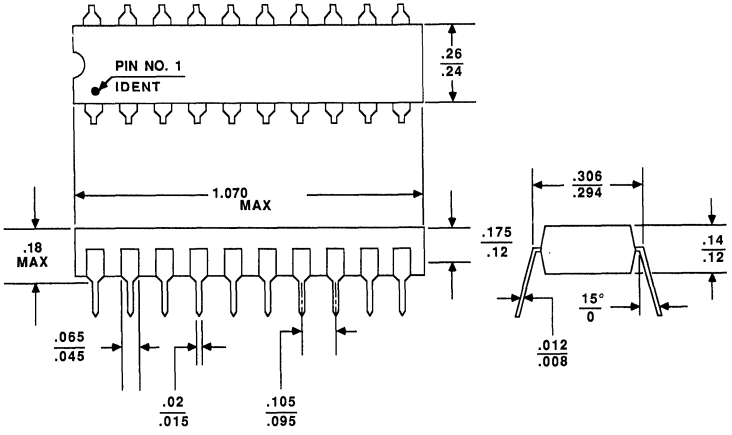


Honeywell

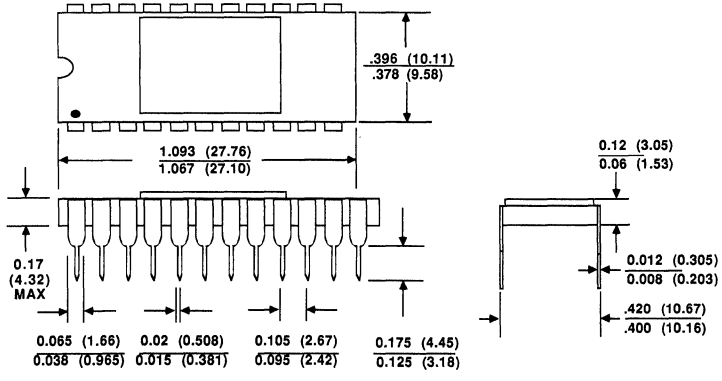
20 LEAD CERDIP



20 LEAD PLASTIC

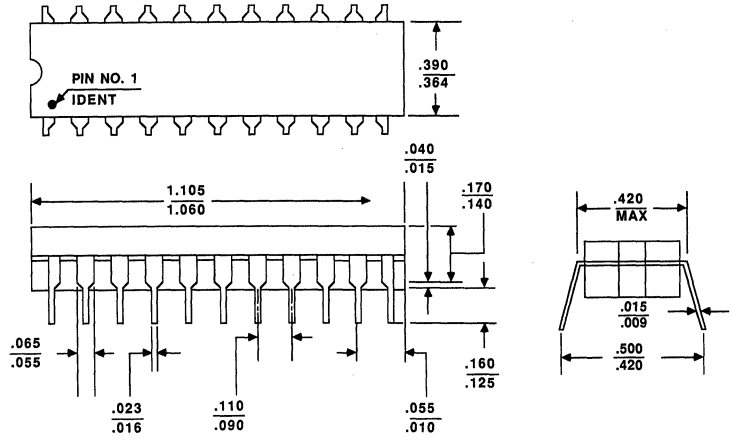


22 LEAD SIDEBRAZED

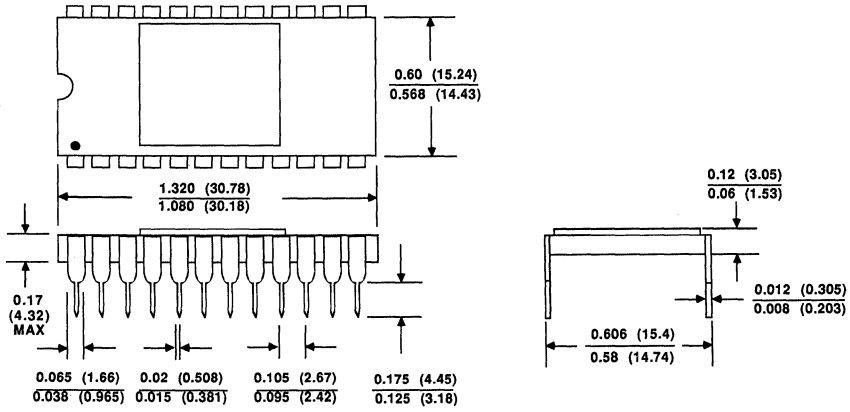


10

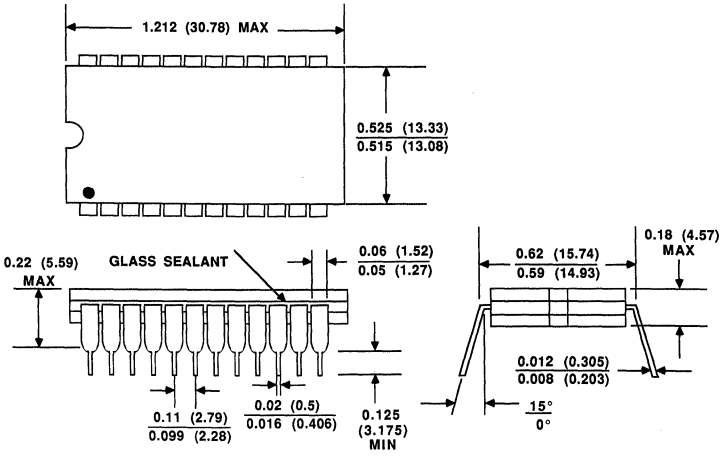
22 LEAD CERDIP



24 LEAD SIDEBRAZED



24 LEAD CERDIP



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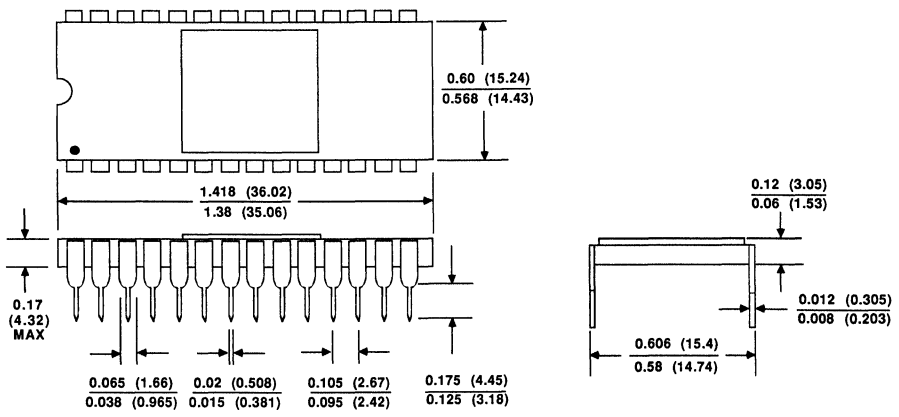
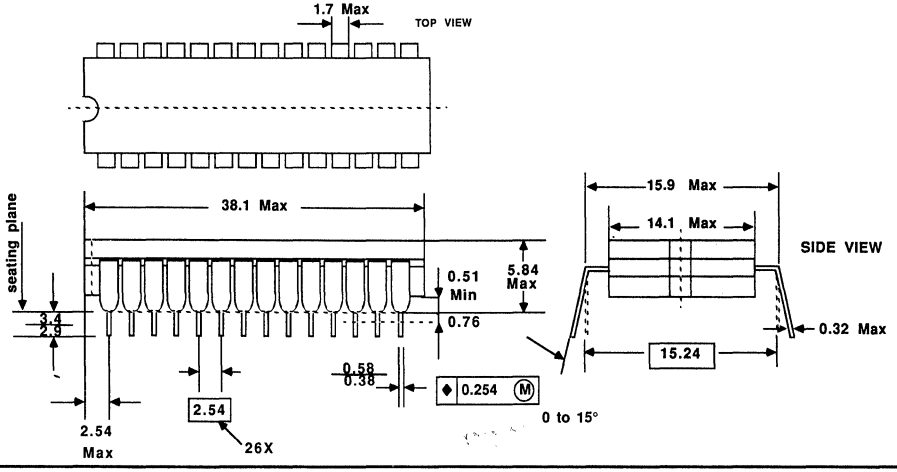
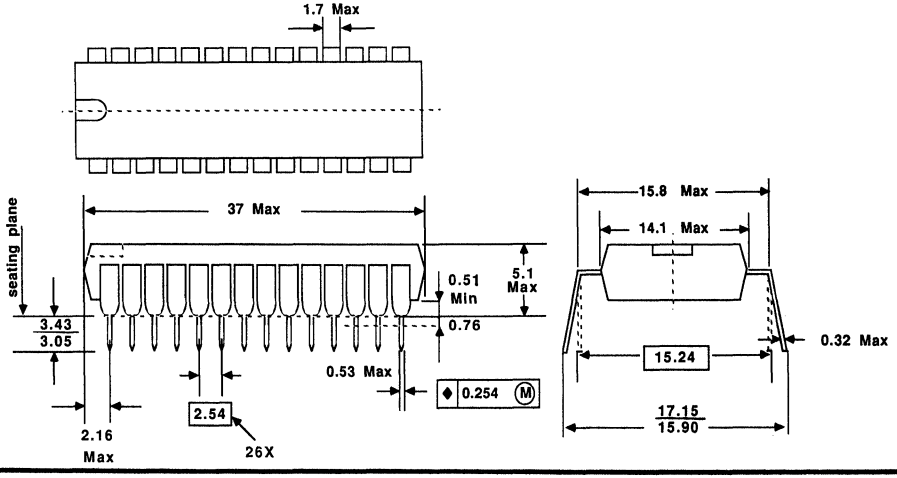
28 LEAD SIDEBRAZED



28-LEAD DUAL IN-LINE; CERDIP



28-LEAD DUAL IN-LINE; PLASTIC



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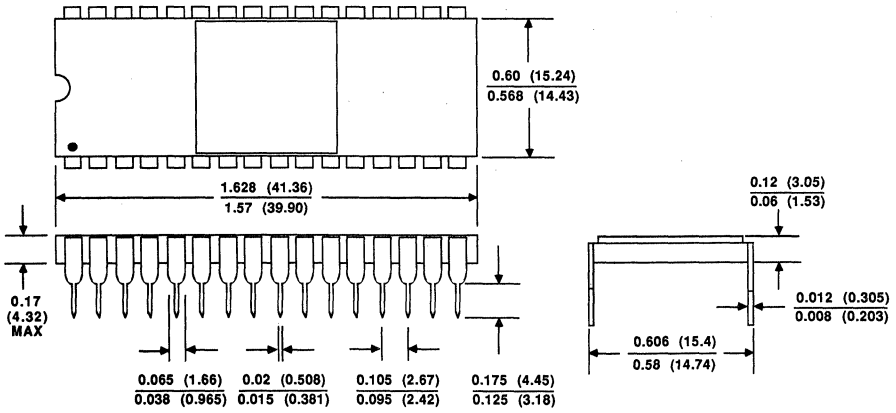
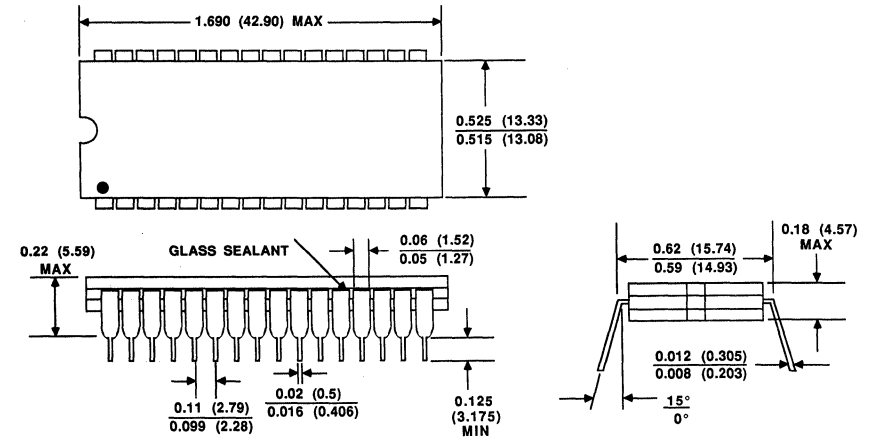
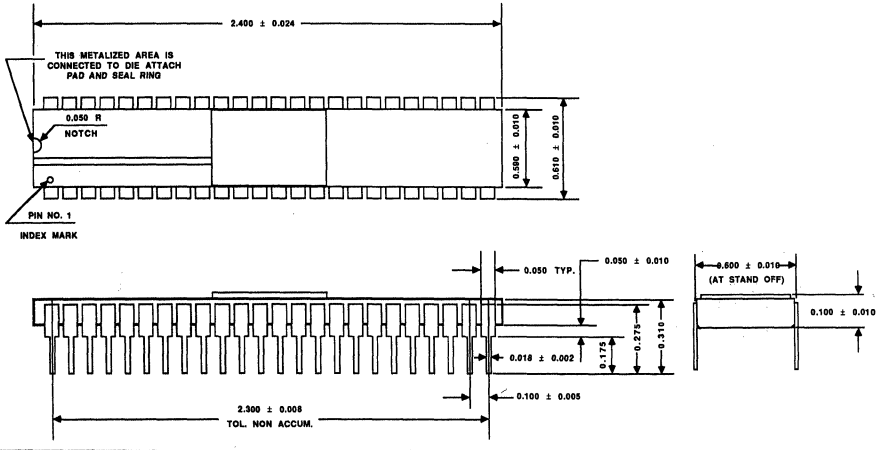
32 LEAD SIDEBRAZED



32 LEAD CERDIP



48 LEAD SIDEBRAZED



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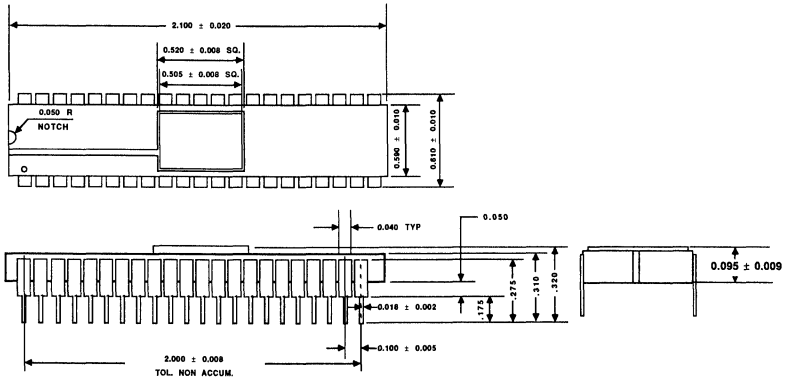
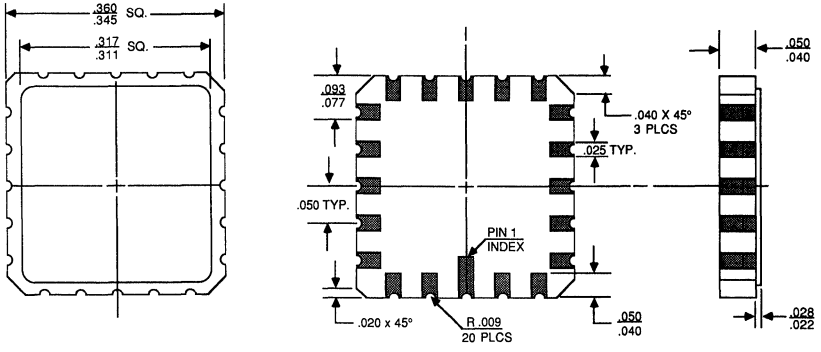
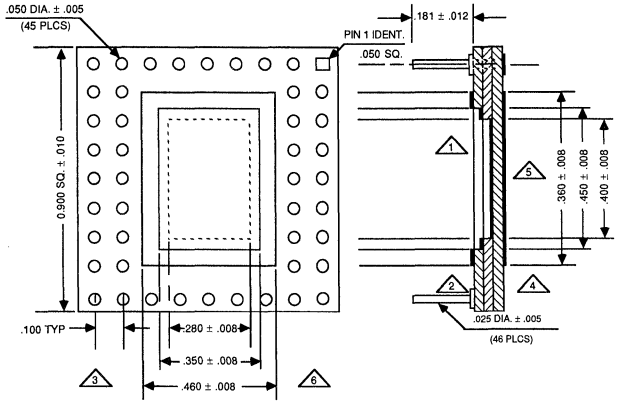
42 LEAD SIDEBRAZED



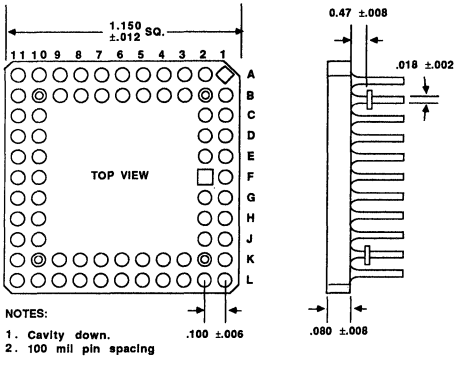
20 PIN LCC



46 PIN PGA



72 PIN PGA



10

**For Ordering Information See Section 1.*

NOTES:

AREA SALES MANAGERS

WESTERN AREA
Honeywell Inc. SPT
721 S. Parker, Bldg. C
Orange, CA 92668
(714) 953-4886
FAX: (714) 953-7204
Telex: 290651

CENTRAL AREA
Honeywell Inc. SPT
1 S. 376 Summit Avenue, Court A
Oakbrook Terrace, IL 60181
(312) 916-1826
FAX: (312) 916-1828

SOUTH CENTRAL AREA
Honeywell Inc. SPT
P.O. Box 467639
Atlanta, GA 30346
(404) 392-1399
FAX: (404) 392-9772

EASTERN AREA
Honeywell Inc. SPT
6 Misty Ridge Circle
Kinnelon, NJ 07405
(201) 492-0113
FAX: (201) 492-0210

DOMESTIC REPRESENTATIVES

ALABAMA
Rep, Inc.
11535 Gilleland Road
P.O. Box 4889 (35815)
Huntsville, AL 35803
(205) 881-9270
(800) 633-2050
TWX 810-776-2102
EasyLink 62608310
FAX 205-882-6692

ARIZONA
Electronic Development & Sales, Inc.
2105 South 48th Street,
Suite 107
Tempe, AZ 85282
(602) 438-1547
TWX 510-600-4993
FAX (602) 438-1569

ARKANSAS
(see Texas)

CALIFORNIA
Emerging Technology Sales
2030 Fortune Drive
Suite B
San Jose, CA 95131
(408) 433-9366
Telex 757199
FAX (408) 434-6730

Emerging Technology Sales
5523 Brome Court
Orangevale, CA 95662
(916) 988-4387
FAX (916) 988-3299

SC Cubed
468 Pennsfield Place
Suite 101A
Thousand Oaks, CA 91360
(805) 496-7307
FAX (805) 495-3601

SC Cubed
17862 17th Street
Suite 207
Tustin, CA 92680
(714) 731-9206
FAX (714) 731-7801

Scott Gould
753 Santa Rosita
Solana Beach, CA 92075
(619) 755-0824

COLORADO
Luscombe Engineering Company
616 Kimbark Street
Longmont, CO 80501
(303) 772-3342
FAX (303) 772-8783

CONNECTICUT
Astrorep of New England
3 Barnard Lane
P.O. Box 7220
Bloomfield, CT 06002
(203) 243-3122
FAX (203) 243-8280
Telex 882486

DELAWARE
(See Southern New Jersey)

FLORIDA (WESTERN)
Perrott Associates
473 East Shore Drive
Clearwater, FL 33515
(813) 443-5214
TWX 810-866-0328
FAX (813) 443-7629

(SOUTHERN)
Perrott Associates
9639 Oregon Road
Boca Raton, FL 33434
(305) 792-2211
TWX 510-955-9831
FAX (305) 488-9073

(CENTRAL)
Perrott Associates
7725 N, Orange Blossom Trail
Orlando, FL 32810
(305) 298-7748
TWX 810-850-0254
FAX (305) 299-1807

GEORGIA
Rep, Inc.
1944 Northlake Parkway
Suite 1
Tucker, GA 30084
(404) 938-4358
TWX 810-766-0822
EasyLink 62657560
FAX (404) 938-0914

ILLINOIS (NORTHERN)
Heartland Technical Marketing, Inc.
3315 W. Algonquin Rd.
Rolling Meadows, IL 60008
(312) 577-9222
FAX (312) 577-0325
Telex (312) 577-0329)

ILLINOIS (SOUTHERN)
(see Missouri)

INDIANA
Arete Sales Inc.
2260 Lake Ave.
Suite 250
Fort Wayne, IN 46805
Phone: (219) 423-1478

Arete Sales Inc.
918 Fry Road
Greenwood, IN 46142
Phone: (317) 882-4407

IOWA
S & O Sales Inc.
3226 Center Point Rd. N.E.
Suite 205
Cedar Rapids, IA 52402
Phone: (319) 363-7323
FAX (319) 363-7331
TWX 910-525-1317

KANSAS
Design Solutions Inc.
10000 W. 75th Street
Suite 200
Shawnee Mission, KS 66204
(913) 677-4747

DOMESTIC REPRESENTATIVES

KENTUCKY (EASTERN)
(see Ohio)

KENTUCKY (WESTERN)
(see Indiana [Southern])

LOUISIANA
(see Texas)

MAINE
(see Massachusetts)

MARYLAND
Rep-tron, Inc.6528 Waterloo Rd.
Baltimore, MD 21227
(301) 799-7490
FAX (301) 796-1948

MASSACHUSETTS
Compass Technology, Inc.
300 Wildwood Street
Woburn, MA 01801
(617) 933-3336
FAX (617) 932-3354

MICHIGAN
Greiner Associates
15324 E. Jefferson Ave.
Grosse Pointe Park, MI 48230
(313) 499-0188
FAX (313) 499-0665
Telex 62705450

MINNESOTA
Mel Foster Technical Sales, Inc.
7611 Washington Ave., South
P.O. Box 35216
Edina, MN 55635
(612) 941-9790
TWX 910-576-2746
FAX (612) 944-0634

MISSISSIPPI
(see Alabama)

MISSOURI
Design Solutions Inc.
12173 Prichard Farm Rd.
St. Louis, MO 63043
(314) 739-3630
MCI 6501813164

MONTANA
(see Colorado)

NEBRASKA
(see Kansas)

NEVADA
(call SPT direct)

NEW HAMPSHIRE
(see Massachusetts)

NEW JERSEY (NORTHERN)
Comp-Tech Sales
208 Boulevard
Suite E
Hasbrouck Heights, NJ 07604
(201) 288-7400
FAX (201) 288-7583
TWX 710-990-6118

NEW JERSEY (SOUTHERN)
Rivco January, Inc.
78 S. Trooper Rd.
Morristown, PA 19403
(215) 631-1414
FAX (215) 631-1640
TWX (510) 660-2406

NEW MEXICO (El Paso, TX)
Nelco Electronix
4801 General Bradley, N.E.
Albuquerque, NM 87111
(505) 293-1399
FAX (505) 292-3247

NEW YORK (UPSTATE)
Elcom Sales Inc.
400 Whitney Road
Rochester, NY 14625
P.O. Box 25112
(716) 385-1400
FAX (716) 248-8531
TWX (510) 254-2627

Elcom Sales Inc.
2-4 Fennell St.
P.O. Box 836
Skaneateles, NY 13152
(315) 685-8245
FAX (315) 685-6273

NEW YORK (METRO)
Comp-Tech Sales
P.O. Box 237
New Hyde Park, NY 11040
(516) 593-2628
FAX (201) 288-7583

NORTH CAROLINA
Rep, Inc.
2500 Gateway Center Blvd.
Suite 400
Morrisville, NC 27560
(919) 469-9997
EasyLink 62637570
FAX (919) 481-3879

NORTH DAKOTA
(see Minnesota)

OHIO
Meta Technical Sales Inc.
264 E. Garfield Rd.
Aurora, OH 44202
(216) 562-8772
FAX (216) 562-7129

OKLAHOMA
West Associates
9717 E. 42nd #125
Tulsa, OK 74146
(918) 665-3465
TWX 910-997-1096
FAX (918) 663-1762

OREGON
Northwest Marketing Associates
6975 S.W. Sandburg Road
Suite 330
Portland, OR 97223
(503) 620-0441
TWX 910-464-5157 NWMARKPTL
FAX (503) 684-2541

PENNSYLVANIA (WESTERN)
(see Ohio)

PENNSYLVANIA (EASTERN)
(see Southern New Jersey)

RHODE ISLAND
(see Massachusetts)

SOUTH CAROLINA
Rep, Inc.
6407 Idlewild Road
Suite 425
Charlotte, NC 28202
(704) 563-5554
Telex 821765
EasyLink 62637570
FAX (704) 535-7507

SOUTH DAKOTA
(see Minnesota)

TENNESSEE
Rep, Inc.
P.O. Box 728
113 South Branner Street
Jefferson City, TN 37760
(615) 475-9012
TWX 810-570-4203
EasyLink 62657620

TEXAS
West Associates
801 E. Campbell Rd. #350
Richardson, TX 75081
(214) 680-2800
Telex 910-997-0805
FAX (214) 699-0330

TEXAS (AUSTIN)
West Associates
8000 Centre Park Dr. #250
Austin, TX 78754
(512) 339-6886
TWX 910-997-1041
FAX (512) 339-8951

DOMESTIC REPRESENTATIVES

TEXAS (HOUSTON)
West Associates
4615 Southwest Frwy. #720
Houston, TX 77027
(713) 621-5983
TXW 910-997-1030
FAX (713) 621-5895

UTAH
Luscombe Engineering Company
47 W. 200 South
Suite 326
Salt Lake City, UT 84101
(801) 532-4118

VERMONT
(see Massachusetts)

VIRGINIA
(see Maryland)

WASHINGTON
Northwest Marketing Associates
12835 Bell-Red Road
Suite 330N
Bellevue, WA 98005
(206) 455-5846
FAX (206) 451-1130
TWX 910-443-2445, NWMARKBVUE

WASHINGTON D.C.
(see Maryland)

WEST VIRGINIA
(see Ohio)

WISCONSIN
Heartland Technical Marketing, Inc.
3846 W. Wisconsin Avenue
Milwaukee, WI 53208
Phone (414) 931-0606

WYOMING
(see Colorado)

INTERNATIONAL REPRESENTATIVES

AUSTRALIA
TO BE DETERMINED

AUSTRIA
Bacher Electronics
Gesellschaft m.b.H.
BURO
Meidlinger Hauptstrabe 78
A-1120 Wien
AUSTRIA
43-222-835646
FAX (43) 222-834276
Telex 847-131532

BELGIUM
Trade Mark Electronics (TME)
Bisschoppenhoflaan 357-359
2100 Antwerpen (Deuren)
BELGIUM
32-3-3251910
FAX (32) 3-3259542
Telex (846) 72713 TMEBEL B

DENMARK
Ditz Schweitzer
Vallensbaekvej 41
DK-2600 Glostrup
DENMARK
45-2-453044
FAX (45) 2-459206
Telex (855) -33257 SCHWEI DK

ENGLAND
Ambar Cascom Ltd.
Rabans Close
Aylesbury, Bucks. HP19 3RS
ENGLAND
0296 434141
FAX (44) 296-29670
Telex 837427

FINLAND
OY Fintronic AB
Melkonkatu 24A
SF00210 Helsinki
FINLAND
358-0-6926022
FAX (358) 0-674886
Telex 857-124224

FRANCE
Radio Equipements Antares (REA)
90, Rue de Villiers
92300 LEVALLOIS-PERRET
FRANCE
33-1-47581111
FAX (33) 1-47587913
Telex (842) 620630

MICROEL
Av. de la Baltique
ZA de Courtaboeuf - B.P.3
91941 LES ULIS CEDEX
FRANCE
331-1-69070824
FAX (33) 1-69071723
Telex 692493F

GERMANY
Kontron Halbleiter GmBH
Breslauer Strasse 16
D-8057 Eching b. Munchen
WEST GERMANY
49-89-31901381
FAX (49) 89-31901499
Telex (841) 5212467Z KHL D

HOLLAND
Techmation Electronics B.V.
Bernhardstraat 11
4175 Ed Haaften
Postbus 9, 175 ZG Haaften
HOLLAND
31-41-892222
FAX (31) 41-891872
Telex (844) -50423 TME NL

ISRAEL
Tritech Limited
5 Haarad Street
P.O. Box 53200
Tel-Aviv 61531
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FAX (972) 3-497816
Telex (922) - 379123

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Silverstar
Via del Gracchi 20
20146 Milano
ITALY
39-2-4996
FAX (39) 2-435594
Telex 843-332189

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Selco
Paseo de la Habana 190-bajo
28036 Madrid
SPAIN
34-1-4054213, 4094634
FAX (34) 1-2592284
Telex (831) 45458 (EPAP-E)

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Setron Sweden AB
Nora Torg 5
P.O. Box 2001
S-18202 Danderyd
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SWEDEN
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Telex (845) -865299 ANA CH

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Supreme Co.
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PLEASE NOTE:
After March 1, 1988 Area Code
and Prefix will change to
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