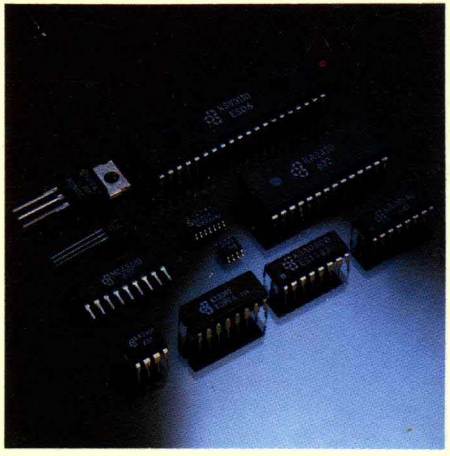
SAMSUNG

Linear IC Data Book (VOL. 2)



1988

- Telecom
- Industrial
- Data Converter

SAMSUNG SEMICONDUCTOR DATA BOOK LIST

I. Semiconductor Product Guide

II. Transistor Data Book

III. Linear IC Data Book

IV. MOS Product Data Book

V. High Performance CMOS Logic Data Book

VI. MOS Memory Data Book

VII. SFET Data Book

LINEAR IC DATA BOOK

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AUDIO ICs
VIDEO ICs

VOLUME 2.

TELECOM ICs
VOLTAGE REGURATORs
VOLTAGE REFERENCEs
OPERATIONAL AMPLIFIERs
COMPARATORs
TIMERs
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MISCELLANEOUS ICs

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KA2419	Tone Ringer with Bridge Diode	8 DIP	108
KA2425A/B	Telephone Speech Network with Dialer Interface	18 DIP	112
KS5805A/B	Telephone Pulse Dialer with Redial	18 DIP	130
KS5808	Dual Tone Multi Frequency Dialer	16 DIP	146
KS5812	Quad Universial Asychronous Receiver and Transmitter	40 DIP	152
KS5819	Tone/Pulse Dialer with Redial	22 DIP/SDIP	162
KS5820	Tone/Pulse Dialer with Redial	18 DIP	172
KS5821	Tone/Pulse Dialer with Redial	22 DIP/SDIP	162
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KT3054J	COMBO CODEC	16 CERDIP	200
KT3064J	COMBO CODEC	20 CERDIP	214
KT5116J	μ-Law Companding CODEC	16 CERDIP	226
LM567C	Tone Decoder	8 DIP/8 SOP	239
LM567L	Micropower Tone Decoder	8 DIP/8 SOP	247
MC1488	Quad Line Driver	14 DIP/14 SOP	257
MC1489/A	Quad Line Receiver	14 DIP/14 SOP	264
MC3361	Low Power Narrow Band FM IF	16 DIP/16 SOP	270
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KA2588A	8-Channel Source Drivers	20 DIP	599
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KA361	High Speed Voltage Comparator	14 DIP/14 SOP	472
KA385-1.2	Micropower Voltage Reference Diode	TO-92	397
KA431	Programmable Precision Reference	TO-92/8 DIP/8 SOP	401
KA710C	High Speed Voltage Comparator	14 DIP/14 SOP	474
KA733C	Differential Video Amplifier	14 DIP/14 SOP	412
KA3524	Regulator Pulse Width Modulator	16 DIP	285
KA9256	Dual Power Operational Amplifier	10 SIP H/S	419
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LM248	Quad Operational Amplifier	14 DIP/14 SOP	432
LM258/A	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	438
LM293/A	Dual Differential Comparator	8 DIP/8 SOP	489
LM311	Voltage Comparator	8 DIP/8 SOP	476
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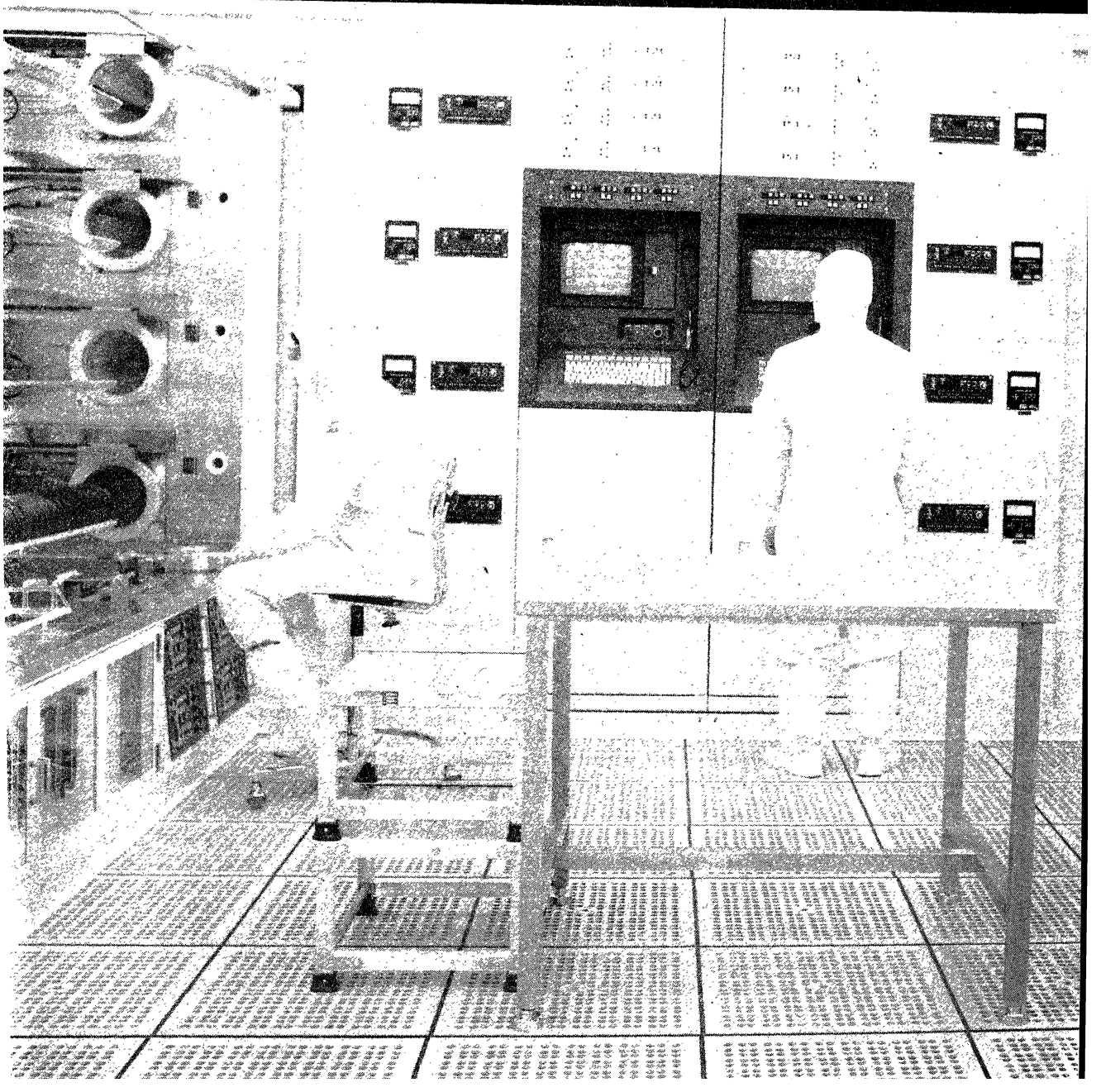
LM323	3-Terminal Positive Voltage Regulator	TO-3P	296
LM324/A	Quad Operational Amplifier	14 DIP/14 SOP	423
LM339/A	Quad Differential Comparator	14 DIP/14 SOP	481
LM348	Quad Operational Amplifier	14 DIP/14 SOP	432
LM358/A/S	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	438
LM393/A/S	Dual Differential Comparator	8 DIP/8 SOP	489
LM723	Precision Voltage Regulator	14 DIP/14 SOP	300
LM741C/E/I	Single Operational Amplifier	8 DIP/8 SOP	446
LM2901	Quad Differential Comparator	14 DIP/14 SOP	481
LM2902	Quad Operational Amplifier	14 DIP/14 SOP	423
LM2903	Dual Differential Comparator	8 DIP/8 SOP	489
LM2904	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	438
LM3302	Quad Differential Comparator	14 DIP/14 SOP	481
MC1458/C/S/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	452
MC3303	Quad Operational Amplifier	14 DIP/14 SOP	456
MC3403	Quad Operational Amplifier	14 DIP/14 SOP	456
MC4558/C/A/S/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	463
MC78XX	3-Terminal 1A Positive Voltage Regulator	TO-220	323
MC78LXX	3-Terminal Positive Voltage Regulator	TO-92	353
MC78MXX	3-Terminal 0.5A Positive Voltage Regulator	TO-220	364
MC79XX	3-Terminal Negative Voltage Regulator	TO-220	377
MC79MXX	3-Terminal 0.5A Negative Voltage Regulator	TO-220	387
KA78S40	Switching Regulator	16 DIP	306
KA78TXX	3A Positive Voltage Regulator	TO-220	312
NE555	Timer	8 DIP/8 SOP	509
NE556	Dual Timer	14 DIP/14 SOP	513
NE558	Quad Timer	16 DIP/16 SOP	516
KA2803	Low Power Consumption Earth Leakage Detector	8 DIP	607
KA2804	Zero Voltage Switch	8 DIP	610
KA33V	Silicon Monolithic Bipolar Integrated Circuit Voltage Stabilizer for Electronic Tuner	TO-92	295

5. Data Converter Application

Device	Function	Package	Page
KSV3100A	High-Speed A/D-DA Converter	40 DIP	521
KSV3110	High-Speed A/D-DA Converter	40 DIP	531
KSV3208	High-Speed A/D Converter	28 DIP	541
KAD0808	8 Bit μp-Compatible A/D Converter with 8-Channel Multiplexer	28 DIP	549
KAD0809	8 Bit μp-Compatible A/D Converter with 8-Channel Multiplexer	28 DIP	549
KAD0820A/B	8 Bit High Speed μp Compatible A/D Converter with Track/Hold Function	20 DIP	560
KDA0800	8 Bit D/A Converter	16 DIP	580
KDA0801	8 Bit D/A Converter	16 DIP	580
KDA0802	8 Bit D/A Converter	16 DIP	580
KS25C02	8 Bit CMOS Successive Approximation Register	16 DIP	586
KS25C03	8 Bit CMOS Successive Approximation Register	16 DIP	586
KS25C04	12 Bit CMOS Successive Approximation Register	24SDIP	586
KS7126	3 1/2 Digit A/D Converter	40 DIP	568

QUALITY & RELIABILITY 1



INTRODUCTION

Samsung's linear IC products are among the most reliable in the industry. Samsung has always made a commitment to achieve the highest possible quality, reliability, and customer satisfaction with its products.
Extensive qualification, monitor and outgoing programs are used to scrutinize product quality and reliability. Stringent controls are applied to every wafer fabrication and assembly lot to achieve reproducibility, and therefore maintain product reliability.
In this chapter, the quality and reliability programs established at Samsung will be discussed. In addition, a description of reliability theory, reliability tests and various support efforts provides a broad framework from which to comprehend Samsung quality and reliability.
To better understand the Quality Department's role in product develoment and manufacturing, a detailed diagram is listed below. As can be noted, Quality Engineering is involved in all phases, save that of initial product planning.

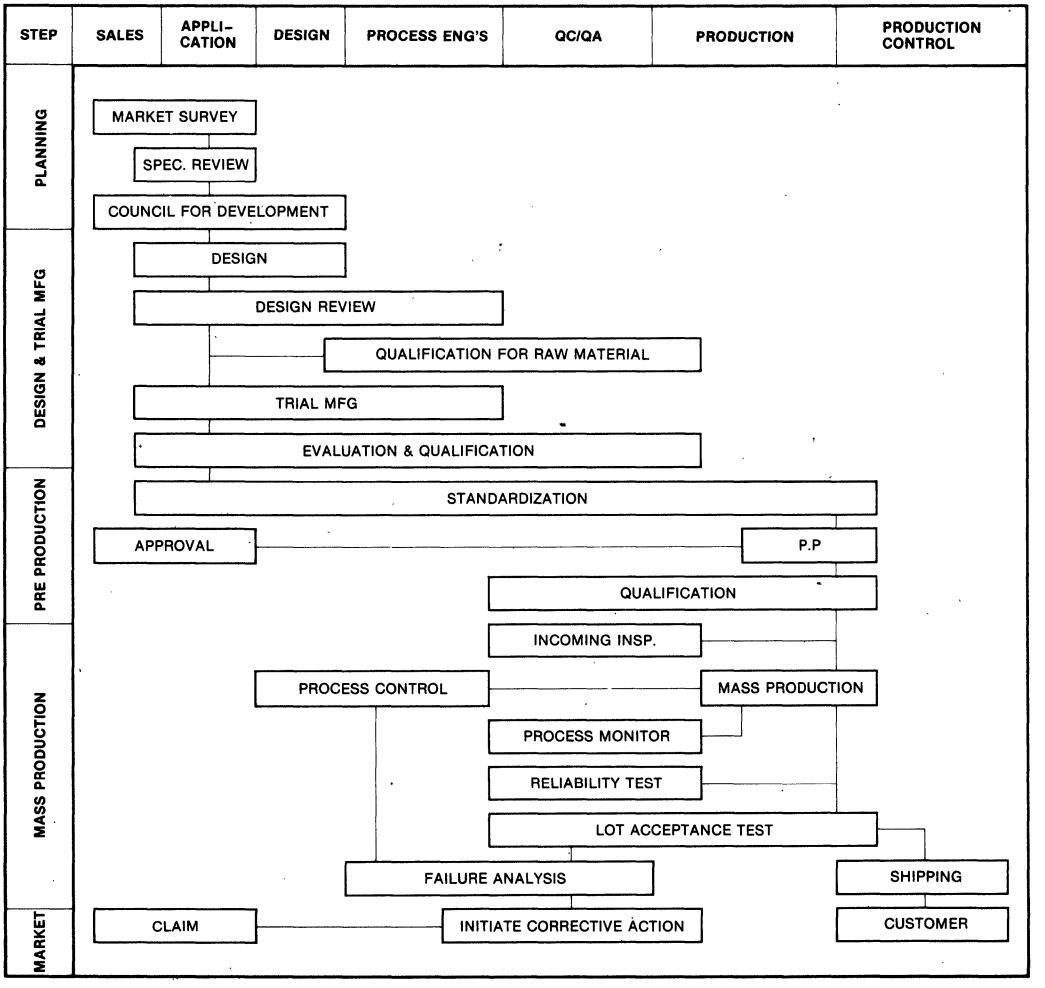


Figure 1. Quality Assurance During Development

QUALITY AND RELIABILITY PROGRAM

Since Samsung manufactures many different products using a variety of fab and assembly technologies, close attention must be paid to a variety of (potential) reliability hazards. The Samsung quality and reliability department has established a variety of procedures and programs to assess, understand, control, and eliminate reliability problems.

The major categories of reliability program management are:

a. Qualification program
b. Monitor program
c. Outgoing quality program

QUALIFICATION PROGRAM

Samsung qualification procedures are used mainly to confirm the major characteristics and reliability attributes of new technologies or products for introduction to Samsung manufacturing. The program is also utilited to evaluate changes to existing technologies or raw materials. The purpose of this program is to simulate all relevant user conditions, via accelerated and standard methods, prior to product shipment. The stresses used for qualification are detailed in following sections.

MONITOR PROGRAM

Twice per year, devices duplicate their qualification tests to obtain long-term reliability data for Linear ICs.
In this way historical data is collected and analyzed over all part types and thus assures the customer of ongoing device quality.
These results are summarized in reliability reports issued periodically by Samsung Semiconductor.

OUTGOING QUALITY PROGRAM

All wafer lots are required to pass a "QC-reliability-gate" prior to product shipment. The purpose is to track "Lot-by-lot" quality and reliability to catch any potential product anomaly at the factory site.
The customer can then expect only quality material to be delivered from Samsung. Any lot that fails the procedure listed below is scrutinized heavily, to make sure that corrective action takes place immediately.
By paying such close attention to every lot, product costs are kept at a minimum. Samsung's customer return rate is extremely low, which is where our tough outgoing policy is most powerful. Such a tight clamp to protect our customers is how we can assure that all Samsung's products are released with the highest confidence level possible.

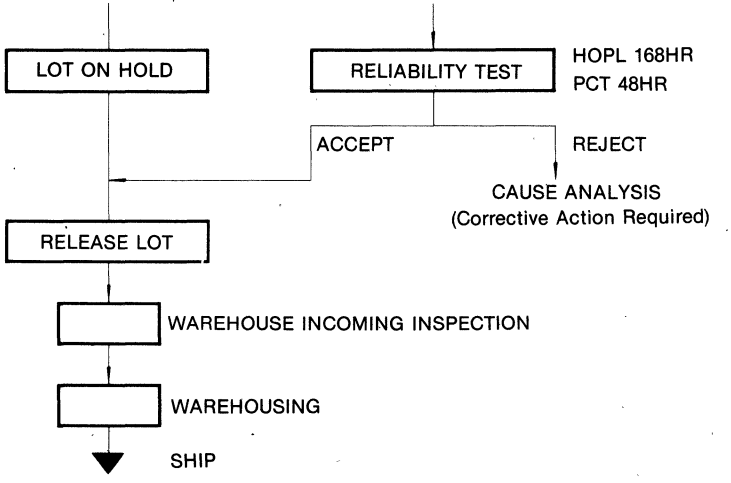


Figure 2. Linear IC Outgoing Flow

RELIABILITY TESTS

Samsung has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the linear IC family. This program involves not only reliability data collection and analysis on existing parts, but also rigorous in-line quality controls for all products.

Listed below are details of tests performed to ensure that manufactured product continues to meet Samsung's stringent quality standards. In line quality controls are reviewed extensively in later sections.

The tests run by the quality department are accelerated tests, serving to model "real world" applications through boosted temperature, voltage, and/or humidities. Accelerated conditions are used to derive device knowledge through means quicker than that of typical application situtations. These accelerated conditions are then used to assess differing failure rate mechanisms that correlate directly with ambient conditions. Following are summaries of various stresses (and their conditions) run by Samsung on linear IC products.

HIGH TEMPERATURE OPERATING LIFE TEST (HOPL)

(T_j = 125°C, V_{CC} = V_{CC} max, static)

High temperature operating life test is performed to measure actual field reliability. Life tests of 1000HR to 2000HR durations are used to accelerate failure mechanisms by operating the device at an elevated ambient temperature (125°C). Data obtained from this test are used to predict product infant mortality, early life, and random failure rates. Data are translated to standard operating temperatures via failure analysis to determine the activation energy of each of the observed failures, using the Arrhenius relationship as previously discussed.

WET HIGH TEMPERATURE OPERATING LIFE TEST (WHOPL)

(Ta = 85°C, R.H. = 81%, V_{CC} = V_{CC} opt, static)

Wet high temperature operating life test is performed to evaluate the moisture resistance characteristics of plastic encapsulated components. Long time testing is performed under static bias conditions at 85°C/81 percent relative humidity with nominal voltages. To maximize metal corrosion, the biasing configuration utilizes low power levels.

INTERMITTENT OPERATING LIFE (IOPL)

(Pmax, 25°C, 2min on/2 min off)

This test is normally applied to scrutinize die bond thermal fatigue. A stressed device undergoes an "ON" cycle, where there is thermal heating due to power dissipation, and an "OFF " cycle, where there is thermal cooling due to lack of inputted power. Die attach (between die and package) and bond attach (between wire and die) are the critical areas of concern.

HIGH TEMPERATURE STORAGE TEST (HTS)

(Ta = 125°C, UNBIASED)

High temperature storage is a test in which devices are subjected to elevated temperatures with no applied bias. The test is used to detect mechanical instabilities such as bond integrity, and process wearout mechanisms.

PRESSURE COOKER TEST (PCT)

(121°C, 15PSIG, 100% R.H., UNBIASED)

The pressure cooker test checks for resistance to moisture penetration. A highly pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

TEMPERATURE CYCLING (T/C)

(−65°C to +150°C, AIR, UNBIASED)

This stess uses a chamber with alternating temperatures of −65°C and +150°C (air ambient) to thermally cycle devices within it. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

THERMAL SHOCK (T/S)

(−65°C to +150°C, LIQUID, UNBIASED)

This stress uses a chamber with alternting temperatures of −65°C to +150°C (liquid ambient) to thermally cycle devices within it. No bias is applied. The cycling is very rapid, and primarily checks for die/package compatibility.

RELIABILITY TEST RESULTS

This section is divided into two parts-actual and predicted test results. Actual test results are those derived via accelerated stressing done by the QC department. Predicted results are calculated by taking actual test results and derating them using statistical and mathematical models to determine device performance in "real-time" user conditions.

ACTUAL TEST RESULTS

(KA2102A)

Stress	Conditions	Number of Devices	Number of Device Hours/Cycles	Number of Failures	% Failures per 1000HRS (Cycles) (60% UCL)
HOPL	Tj = 125°C $V_{CC} = V_{CC}$ max	100	100,000	0	0.91%/1K HR
WHOPL	85° C/81% R.H. $V_{CC} = V_{CC}$ opt	100	100,000	0	0.91%/1K HR
IOPL	Ta = 25°C $V_{CC} = V_{CC}$ max	100	100,000	0	0.91%/1K HR
HTS	Ta = 125°C Unbiased	100	100,000	0	0.91%/1K HR
PCT	121°C 15 PSIG	100	16,800	0	5.4 %/1K HR
T/C	−65°C to 150°C Air to Air	100	10,000	0	9.1 %/1K CL
T/S	−65°C to 150°C Liquid to Liquid	100	10,000	0	9.1 %/1K CL

PREDICTED TEST RESULTS

The Arrhenius equation, which is reviewed in another section of this chapter, can be applied to derive typical "user-condition" device failure rates.

STESS: HOPL

100,000 Device Hours at 125°C
Average Activation Energy: 1.0 eV.
De-Rating to User Conditions Yields:

70°C Operation

Equivalent Device Hours	% Failures Per 1000 Hours (60% UCL)	*FITs	**MTBF (Years)
10.7×10^6	0.0084	84	1359

55°C Operation

Equivalent Device Hours	% Failures Per 1000 Hours (600% UCL)	*FITs	**MTBF (Years)
50.4×10^6	0.0018	18	6342

* FIT : Failure in time or failure unit. Represents the number of failures expected for 10^9 (one billion) device hours.

** MTBF: Mean time between failures.

RELIABILITY AND PREDICTION THEORY

RELIABILITY

Reliability can be loosely characterized as long term product quality.

There are two types of reliability tests: those performed during design and development, and those carried out in production. The first type is usually performed on a limited sample, but for long periods or under very accelerated conditions to investigate wearout mechanisms and determine tolerances and limits in the design process. The second type of tests is performed periodically during production to check, maintain, and improve the assured quality and reliability levels. All reliability tests performed by Samsung are under conditions more severe than those encountered in the field, and although accelerated, are chosen to simulate stresses that devices will be subjected to in actual operation. Care is taken to ensure that the failure modes and mechanisms are unchanged.

FUNDAMENTALS

A semiconductor device is very dependent on its conditions of use (*e.g.,* junction temperature, ambient temperature, voltage, current, *etc.*). Therefore, to predict failure rates, accelerated reliability testing is generally used. In accelerated testing, special stress conditions are considered as parametrically related to actual failure modes. Actual operating life time is predicted using this method. Through accelerated stresses, component failure rates are ascertained in terms of how many devices (in percent) are expected to fail for every 1000 hours of operation. A typical failure rate versus time of activity graph is shown below (the so-called "bath tub curve")

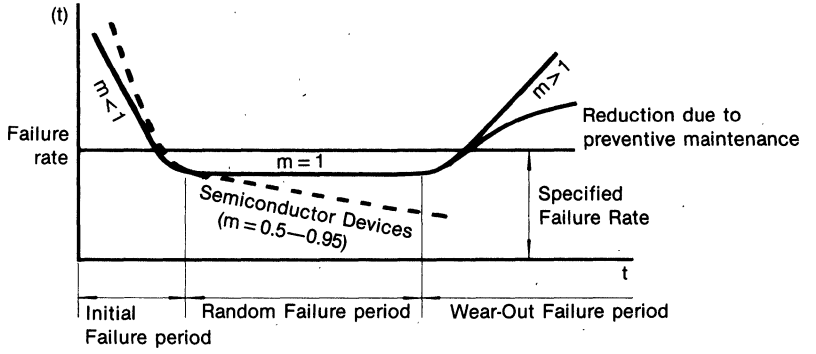


Figure 3. Failure Rate Curve ("Bath Tub Curve")

During their initial time period, products are affected by "infant mortality," intrinsic to all semiconductor technologies. End users are very sensitive to this parameter, which causes early assembly/operation failures in their own system. Periodically, Samsung reviews and publishes life time results. The goal is a steady shift of the limits as shown below.

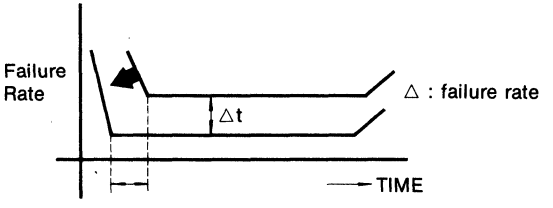


Figure 4. Failure Rate

ACCELERATED HUMIDITY TESTS

To evaluate the reliability of products assembled in plastic packages, Samsung performs accelerated humidity stressing, such as the Pressure Cooker Test (PCT) and Wet High Temperature Operating Life Test (WHOPL).

Figure 5 shows some results obtained with these tests, which illustrate the improvements in recent years. These improvements result mainly from the introduction of purer molding resins, new process methods, and improved cleanliness.

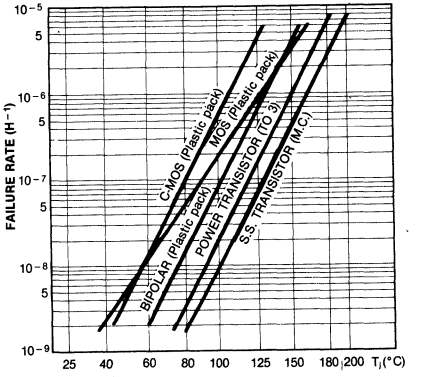


Figure 5. Improvement in Humidity Reliability

ACCELERATED TEMPERATURE TESTS

Accelerated temperature tests are carried out at temperatures ranging from 75°C to 200°C for up to 2000 hours. These tests allow Samsung to evaluate reliability rapidly and economically, as failure rates are strongly dependent on temperature.

The validity of these tests is demonstrated by the good correlation between data collected in the field and laboratory results obtained using the Arrhenius model. Figure 6 shows the relationship between failure rates and temperatures obtained with this model.

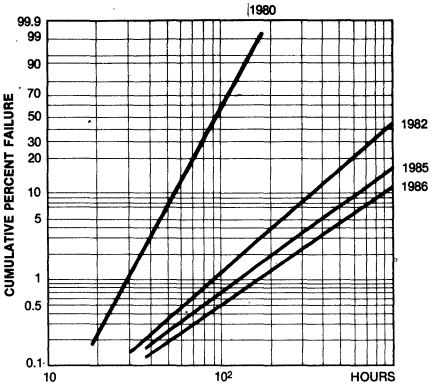


Figure 6. Failure Rate Versus Temperature

FUNDAMENTAL THEORY FOR ACCELERATED TESTING

Accelerated life testing is powerful because of its strong relation to failure physics. The Arrhenius model, which is generally used for failure modelling, is explained below.

1. Arrhenius model

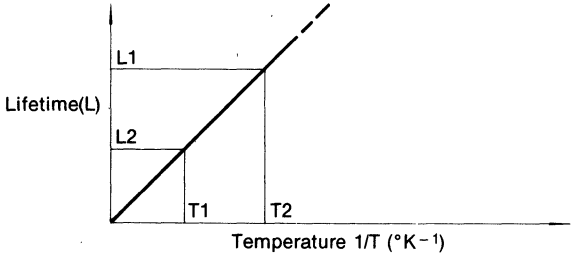
This model can be applied to accelerated Operating Life Tests and uses absolute (Kelvin) temperatures.

$L = A + Ea/K \cdot Tj$

- L : Lifetime
- A : Constant
- Ea : Activation Energy
- K : Boltzman's constant
- Tj : Absolute Junction temperature

If Lifetimes L1 and L2 correspond to Temperatures T1 and T2:

$$L1 = L2 \exp \frac{Ea}{K} \left(\frac{1}{T1} - \frac{1}{T2} \right)$$



Actual junction temperature should always be used, and can be computed using the following relationship.

$$Tj = Ta + (P \times \theta ja)$$

Where Tj = Junction temperature
Ta = Ambient temperature
P = Actual power consumption
θ ja = Junction to Ambient thermal resistance (typically 100 degrees celsius/watt for a 16-Pin PDIP).

2. Activation Energy Estimate

Clearly the choice of an appropriate activation energy, Ea, is of paramount importance. The different mechanisms which could lead to circuit failure are characterized by specific activation energies whose values are published in the literature. The Arrhenius equation describes the rate of many processes responsible for the degradation and failure of electronic components. It follows that the transition of an item from an initially stable condition to a defined degraded state occurs by a thermally activated mechanism. The time for this transition is given by an equation of the form:

MTBF = B EXP (Ea/KT)
MTBF = Mean time between failures
B = Temperature-independent constant

MTBF can be defined as the time to suffer a device degradation. The dramatic effect of the choice of the Ea value can be seen by plotting the MTBF equation. The acceleration effect for a 125°C device junction stress with respect to 70°C actual device junction operation is equal to 1000 for Ea = 1eV and 7 for Ea = 0.3eV.

Some words of caution are needed about published values of Ea:

A. They are often related to high-temp tests where a single Ea (with high value) mechanism has become dominant.
B. They are specifically related to the devices produced by that supplier (and to its technology) for a given period of time
C. They could be modified by the mutual action of other stresses (voltage, mechanical, etc.)
D. Field device-application condition(s) should be considered.

(Activation energy for each failure mode)

Failure Mechanism	Ea
Contamination	1 ~ 1.4 eV
Polarization	1 eV
Aluminum Migration	0.5 ~ 1 eV
Trapping	1 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.3 ~ 0.5 eV

THE CORRECT PROCEDURE

ACCELERATED TEST ——— CALCULATED AT TEST CONDITIONS AND WITH A CERTAIN CONFIDENCE LEVEL

FAILURE ANALYSIS

CHOICE OF Ea ——— CALCULATED AT OTHER TEMPERATURES

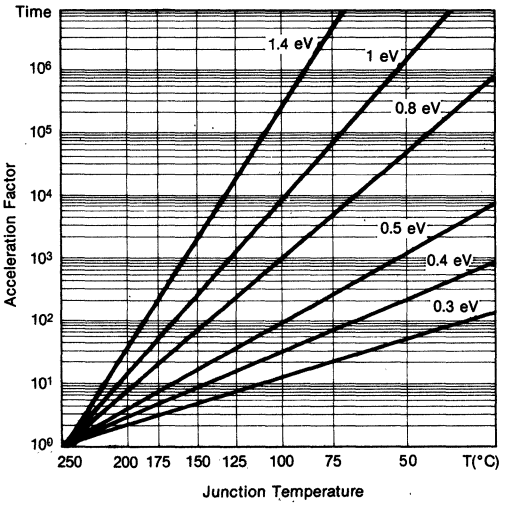


Figure 7. Life Hours

Failure Rate Prediction

Accelerated testing defines the failure rate of products. By derating the data at different conditions, the life expectancy at actual operating conditions can be predicted. In its simplest form the failure rate (at a given temperature) is:

$$FR = \frac{N}{DH}$$

Where FR = Failure Rate
N = Number of failures
D = Number of components
H = Number of testing hours

If we intend to determine the FR at different temperatures, an acceleration factor must be considered. Some failure modes are accelerated via temperature stressing based upon the accelerations of the Arrhenius Law.

For two different temperatures:

$$FR(T1) = FR(T2) \exp \frac{Ea}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)$$

FR (T1) is a point estimate, but to evaluate this data for an interval estimate, we generally use a X^2 (chi square) distribution. An example follows:

Failure Rate Elaluation

Unit: %/1000HR

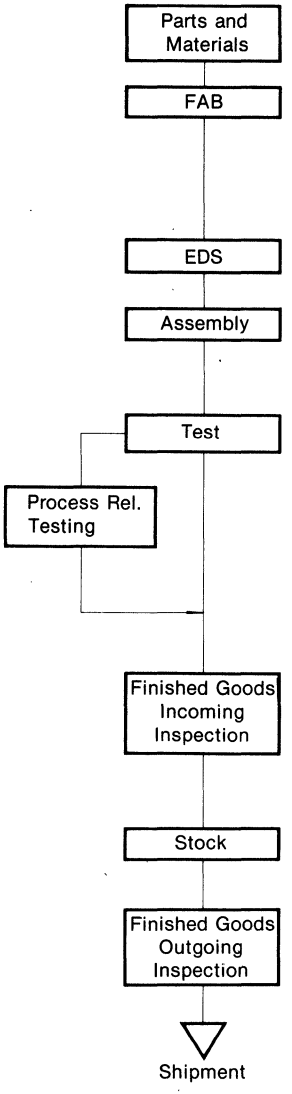
Dev. x Hours at 125°C	Fail	Failure Rate at 60% Confidence Level			
		Point Estimate	85°C	70°C	55°C
1.7×10^6	2	0.18	0.0068	0.0018	0.00036

The activation energy, from analysis, was chosen as 1.0 eV based upon test results. The failure rate at the lower operating temperature can be extrapolated by an Arrhenius plot.

PROCESS CONTROL

GENERAL PROCESS CONTROL

The general process flow in Samsung is shown in Figure 8. This illustration contains the standard process flow from incoming parts and materials to customer shipment.



Acceptance inspection (according to acceptance inspection plan)

Process quality control
- Check of each condition by process quality control procedures
- Process inspection
- Lot control
- Equipment calibration and maintenance

100% Electrical Die Sorting

Process Quality Control and screening of infant mortality defects
- Mechanical screen
- Thermal shock
- Burn-in

100% package sorting of electrical characteristics and marking

Reliability monitoring
1. PRT (Process Reliability Testing)
2. DRT (Device Reliability Testing)

- High Temperature Operating Life Test
- Environmental test
- Life Test

Sampling Inspection
- Dimensions
- Visual
- Electrical characteristics
- Periodic calibration of measuring equipment

Stock control
- Age control

Sampling Inspection (when applicable)

Figure 8. General Process Flow Chart

WAFER FABRICATION

Process Controls

The Quality Control program utilizes the following methods of control to achieve its previously stated objectives: process audits, environmental monitors, process monitors, lot acceptance inspections, and process integrity audits.

Definitions

The essential method of the Quality Control Program is defined as follows:

1. Process Audit-Performed on all operations critical to product quality and reliability.
2. Environmental Monitor-Monitors concerning the process environment, *i.e.,* water purity, temperature, humidity, particle counts.
3. Process Monitor-Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variable data.
4. Lot Acceptance-Lot-by-lot sampling. This sampling method is reserved for those operations deemed as critical, and require special attention.

Environmental Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Clean Room	• Temperature • Humidity • Particle • Air Velocity	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	24 Hrs. 24 Hrs. 24 Hrs. 24 Hrs.
D.I. Water	• Particle • Bacteria • Resistivity	• 5 ea/50ml (0.8μ) • 50 colonies/100ml (0.45μ) • Main (Line): More than 16 Mohm-cm • Using point: More than 14 Mohm-cm	24 Hrs. Weekly 24 Hrs. 24 Hrs.

* Instruments
- FMS (Facility Monitoring System) HIAC/ROYCO
- CPM (Central Particle Monitoring System-Dan Scientific)
- Liquid Dust Counter Etch Rate
- Filtration System for Bacterial check
- Air Particle counter
- Air Velocity meter

Process Monitor

Process	Control Item	Spec. Limit	Insp. Frequency
Photo	• Aligner N_2 Flow Rate • Aligner Vacuum • Aligner Air • Aligner Pressure • Aligner Intensity • Coater Soft Bake Temperature Vacuum	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift
Etch	• Etchant Temp. • Etch Rate • Spin Dryer N_2 Flow RPM • Hard Bake Temp. N_2 Flow	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift Once/Shift

Process Monitor (Continued)

Process	Control Item	Spec. Limit	Insp. Frequency
Thin Film	• Cooling Water Temp. • Thickness	• 26 ± 3°C • Individual Spec.	Once/Shift Once/Shift
CVD	• Pin Hole • Thickness	• Individual Spec. • Individual Spec.	Once/Shift Once/Shift
Diffusion	• Tube Temp. • C-V Plot Run Tube • Sheet Resistance • Thickness	• Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec. • Individual Spec.	Once/Shift Once/Shift Once/10days Once/Shift Once/Shift

Raw Material Incoming Inspection

1. Mask Inspection

Defect Detection	• Pinhole & Clear-extension • Opaque Projections & Spots • Scratch/Particle/Stain • Substrate Crack/Glass-chip • Others	All Masks	• Defect Size $\leq 1.5\mu m$ • Defect Density $\leq 0.124 EA/cm^2$
Registration	• Run-out (X-Y Coordinate) • Orthogonality • Drop-in Accuracy • Die Fit/Rotation	20% • All New Masks	$\pm 0.75\mu m$ $\pm 0.75\mu m$ $\pm 0.50\mu m$ $\pm 0.50\mu m$
Critical Dimension	• Critical Dimension	All Masks	Purchasing Spec.

* Instrument
- Auto mask inspection system for defect-detection (NJS 5MD-44)
- Comparator for registration (MVG 7X7)
- Automatic linewidth measuring system for CD (MPV-CD)

2. Wafer Inspection

Purpose	Insp. Items	Sample	Remarks
Structural	• Crystallographic Defect	All Lots	• Sirtl Etch
Electrical	• Resistivity • Conductivity	All Lots	• Monitor Water
Dimensional	• Thickness • Diameter • Orientation • Flatness	All Lots	TTV, NTV, Epi-thickness TIR (FPD) Local Slope
Visual	• Surface Quality • Cleanliness	All Lots	Purchasing Spec.

* Instrument
- 4 point probe for resistivity (Kokusai VR-40A, Tencor sonogage, ASM ÅFPP)
- Flatness measuring system (Siltec)
- Epi. layer thickness gauge (Digilab FTG-12, Qualimatic S-100)
- Automatic Surface Insp. System (Aeronca Wis-150)
- Non-contact thickness gauge (ADE6034)

In-Process Quality Inspection (FAB)

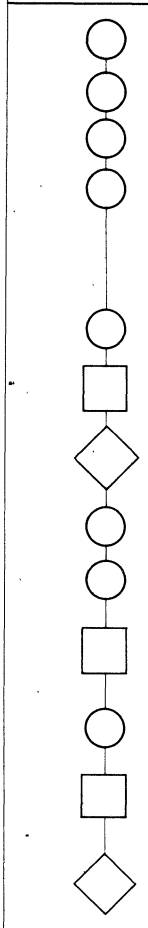
1. Manufacturing Section

Process Step	Process Control Insp.	Frequency
Oxidation	Oxide Thickness	All Lots
Diffusion	Oxide Thickness Sheet Resistance Visual	All Lots All Lots All Lots
Photo	Critical Dimension Visual Mask Clean Inspection	All Lots (MOS) All Lots All Masks with Spot Light (MOS) or Microscope (BIP)
Etch	Critical Dimension Visual	All Lots All Wafers
Thin Film	Metal Thickness Visual	All Lots All Lots
Ion Implant	Sheet Resistance	All Lots (Test Wafer)
Low Temp. Oxide	Thickness	All Lots
	Visual	All Lots
E-Test	Electrical Characteristics	All Lots
Fab. Out	Visual	All Wafers

2. FAB, QC Monitor/Gate

Process Step	FAB, QC Insp.	Frequency
Oxidation	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN Once/Shift
Diffusion	Oxide Thickness C-V Test on Tubes Visual	Once/Shift Once/10 Days and After CLN Once/Shift
Photo	Critical Dimension Visual Mask CLN Inspection	All Lots (MOS) Once/Shift All Masks After 10 Times Use
Etch	Critical Dimension Visual	All Lots (MOS) All Lots
Thin Film	C-V Test on Tubes on Lots Reflectivity	Once/10 Days and After CLN Once/Shift Once/Shift
Low Temp. Oxide	Refractive Index, Wt% of Phosphorus Visual	1 Test Wafer/Lot 1 Test Wafer/Lot 1 Test Wafer/Lot
E-Test	Measuring Data	All Lots
Calibration	Instrument for Thickness and C.D. Measuring	Once/week

3. Photo/Etch process quality control

Process Flow	Process Step	MFG. Control Item	QC Monitor/Gate
	Prebake	Oven PM, Temperature Time	Oven Particle Temp. N_2 Flow Rate
	Photo Resist (PR) —spin	Thickness Machine PM	
	Soft Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Align/Expose	Light Uniformity Alignment, Focus Test Mask Clean Inspection Mask Clean Exposure Light Intensity	Light Intensity Mask Clean Insp.
	Develop	Equipment PM Solution Control	Vacuum
	Develop Check	PR/C.D.'S Alignment Particles Mask and Resist Defects	
	QC Inspection		Critical Dimension (CD)
	Hard Bake	Oven PM, Temperature Time	Temp. N_2 Flow Rate
	Etch	Etch rate, Equipment PM & Settings, Etch Time to Clear	Etchant Temp. Etch Rate
	Inspection	Over/Under	
	PR Strip	Machine-PM	
	Final Check	C.D.'S Over and under Etch, Particles, PR Residue, Defects, Scratches	
	QC Inspection		Same as Final Check, However, More Intense on limited Sample Basis. (AQL 6.5%)

Note: PM represents Preventive Maintenance

4. Reliability-related Interlayer Dielectric, Metallization, and Passivation Process Quality Control Monitor

Item	Frequency
Wt% Phosphorus Content of the Dielectric Glass	1/Shift
Metallization Interconnect	1/Month
Al Step Coverage	1/Month
Metallization Reflectivity	1/Shift
Passivation Thickness and Composition	1/Shift
Thin Film Defect Density	1/Shift

Figure 9. General Wafer Fabrication Flow

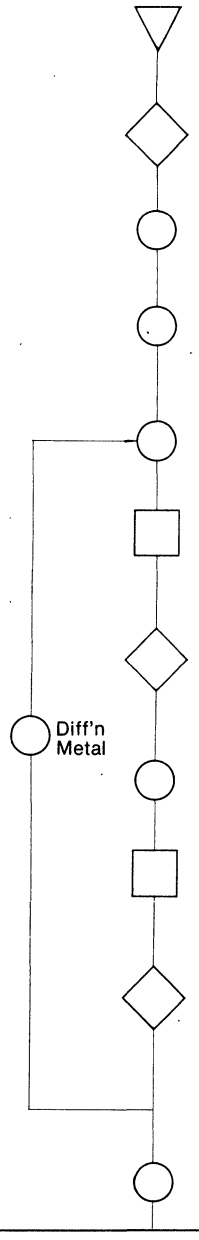
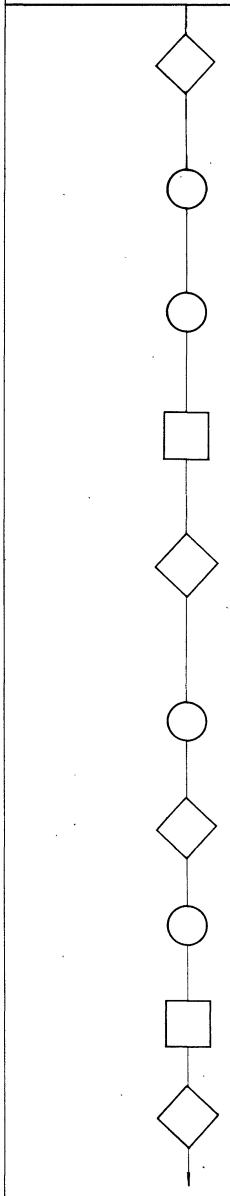
Process Flow	Process Step	Major Control Item
	Wafer and Mask Input	
	Starting Material Incoming Inspection	Mask: (See mask Inspection) Wafer: (See wafer Inspection)
	Wafer Sorting and Labelling	Resistivity
	Initial Oxidation	Oxide Thickness
	Photo	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension
	Etch	• (See manufacturing section) • (See FAB, QC Monitor/gate)
	Inspection	• Critical Dimension • Visual/Mech — Major: AQL 1.0% — Minor: AQL 6.5%
	QC Gate	• Critical Dimension • Visual/Mech
	Diffusion Metalization	• (See in-process Quality Inspection)
	E-test	• Electrical Characteristics

Figure 9. General Wafer Fabrication Flow (Continued)

Process Flow	Process Step	Major Control Item
	QC Gate	• Electrical Characteristics
	Back-Lap	• Thickness
	Back Side Evaporation	• Thickness, Time Evaporation Rate
	Final Inspection	• All Wafers Screened (Visual/Mech)
	QC Fab. Final Gate	• Visual/Mech. — Major: AQL 1.0% — Minor: AQL 6.5%
	EDS (Electrical Die Sorting)	
	QC Gate	• Function Monitor
	Sawing	
	Inspection	• Chip Screen
	QC Final Inspection	• AQL 1.0% • Fab. Defect • Test Defect • Sawing Defect
Die Attach		

ASSEMBLY

The process control and inspection points of the assembly operation are explained and listed below:

1. Die Inspection:

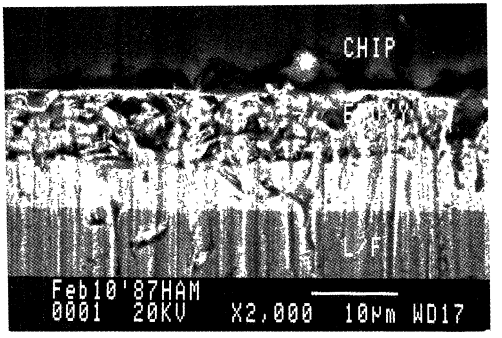
   Following 100% inspection by manufacturing, in-process Quality Control samples each lot according to internal or customer specifications and standards.

2. Die Attach Inspection:

   Visual inspection of samples is done periodically on a machine/operator basis. Die Attach techniques are monitored and temperatures are verified.

3. Die Shear Strength:

   Following Die Attach, Die Shear Strength testing is performed periodically on a machine/operator basis. Either manual or automatic die attach is used.



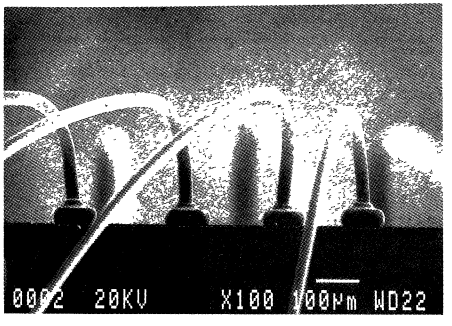
DIE ADHESIVE THICKNESS MONITOR RESULTS. (JEOL SEM, JSM IC845)

4. Wire Bond Inspection:

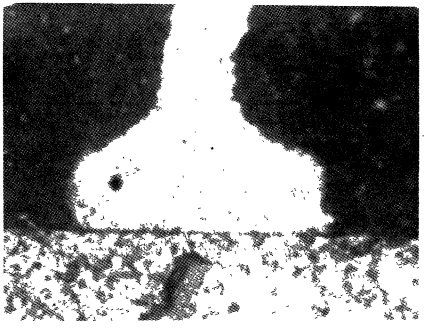
   Visual inspection of samples is complemented by a wire pull test done periodically during each shift. These checks are also done on a machine/operator basis and XR data is maintained.

5. Pre-Seal/Pre-Encapsulation Inspection:

   Following 100% inspection of each lot, samples are taken on a lot acceptance basis and are inspected according to internal or customer criteria.



WIRE LOOP MONITOR RESULTS.



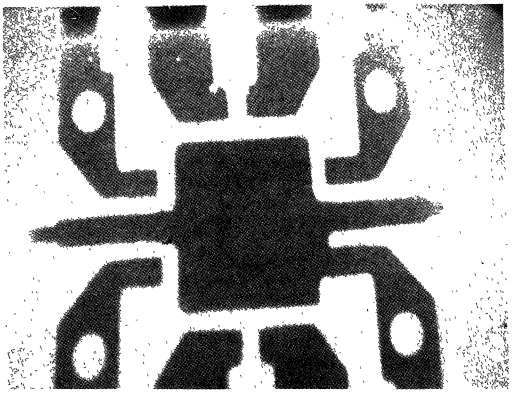
CROSS SECTION INSPECTION FOR BALL BOND.

6. Seal Inspection:

   Periodic monitoring of the sealing operation checks the critical temperature profile of the sealing oven for both glass and metal seals.

7. Post-Seal Inspection:

   Subsequent to a 100% visual inspection, In-Process Quality Control samples each for conformance to visual criteria.



X-RAY MONITOR RESULT. (PHILIPS MG161)

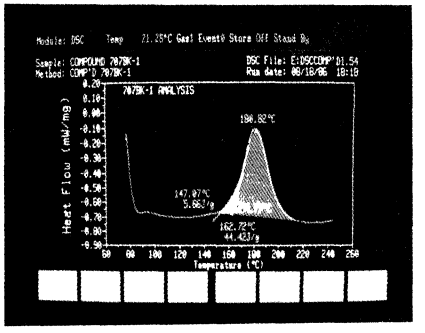
8. General Assembly Flow is shown in Figure 11.

Sampling Plans

1. Sampling plans are based on an AQL (Acceptable Quality Level) concept and are determined by internal or by customer specifications.

2. Raw Material Incoming Inspection. (confinued)

Material	Inspection Item	Acceptable Quality Level
Lead Frame	1) Visual Inspection 2) Dimension Inspection 3) Function Test 4) Work Test	LTPD 10%, C = 2 LTPD 20%, C = 0 LTPD 20%, C = 0 LTPD 20%, C = 0
Wafer	1) Visual Inspection	AQL 0.65%
Au/Al Wire	1) Visual Inspection 2) Bond Pull Strength Test 3) Bondability Test 4) Chemical Composition Analysis	n:5, C = 0 n: 13, C = 0 Critical Defect: 0.65% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C = 0
Molding Compound	1) Visual Inspection 2) Moldability Test 3) Chemical Composition Analysis	n: 5, C = 0 Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C = 0



MOLDING COMPOUND INCOMING INSPECTION
(THERMAL ANALYSER, DUPONT 9900)

(Continued)

Material	Inspection Item	Acceptable Quality Level
Packing Tube & Pin	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15%, C = 2 LTPD 15% C = 2 n: 5, C = 0 n: 5, C = 0
Solder	1) Visual Inspection 2) Weight Inspection 3) Chemical Composition Analysis	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 20% C = 0
Flux	1) Acidity Test 2) Specific Gravity Test 3) Chemical Composition Analysis	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 20% C = 0
Solder Preform	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Coating Resin	1) Visual Inspection 2) Work Test 3) Chemical Composition Analysis	AQL 1.0% AQL 1.0% AQL 1.0%
Marking Ink	1) Work Test 2) Mark Permanency Test	Critical Defect: 0.15% Major Defect: 1.0% Minor Defect: 1.5% n: 5, C = 0
Chip Carrier	1) Visual Inspection 2) Dimension Inspection 3) Electro-Static Inspection 4) Hardness Test	LTPD 15% C = 2 LTPD 15% C = 0 n: 5, C = 0 n: 5, C = 0
Vinyl Pack	1) Visual Inspection 2) Work Test 3) Electro-Static Inspection	LTPD 20% C = 0 LTPD 20% C = 0 LTPD 15% C = 0
Ag Epoxy	1) Work Test 2) Chemical Composition Analysis	n:8, C = 0 n:8, C = 0
Letter Marking	1) Visual Inspection 2) Work Test	
Spare Parts & Others	1) Dimension Inspection 2) Visual Inspection	n:5, C = 0 n:5, C = 0

3. In-Process Quality Inspection

A. Assembly Lot Acceptance Inspection

(1) Acceptance quality level for wire bond gate inspection

Defect Class	Inspection Level	Type of Defect	
Critical Defect	AQL 0.65%	— Missing Metal — Chip Crack — No Probe — Epoxy on Die — Mixed Device — Wrong Bond — Missing Bond	— Diffusion Defect — Ink Die — Exposed Contact — Bond Short — Die Lift — Broken Wire
Major Defect	AQL 1.0%	— Metal Missing — Metal Adhesion — Pad Metal Discolored — Tilted Die — Die Orientation — Partial Bond	— Oxide Defect — Probe Damage — Metal Corrosion — Incomplete Wetting — Weakened Wire
Minor Defect	AQL 1.5%	— Adjacent Die — Passivation Glass — Die Attach Defect — Wire Loop Height — Extra Wire	— Contamination — Ball Size — Wire Clearance — Bond Deformation

(2) Acceptance quality level for Mold/Trim gate inspection

Defect Class	Inspection Level	Kind of Defect	
Critical Defect	AQL 0.15%	— Incomplete Mold — Void, Broken Package — Misalignment	— Deformation — No Plating — Broken Lead
Major Defect	AQL 0.4%	— Ejector Pin Defect — Package Burr — Flash on Lead	— Crack, Lead Burr — Rough Surface — Squashed Lead
Minor Defect	AQL 0.65%	— Lead Contamination — Poor Plating — Package Contamination	— Bent Lead

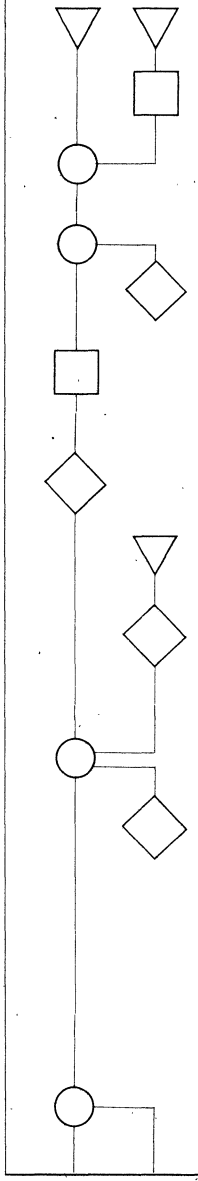
B. In-process monitor inspection

Inspection Item	Frequency	Reference
• Die Shear Test	Each Lot	MIL-STD-883C, 2019-2
• Bond Strength Test	Each Lot	MIL-STD-883C, 2011-4
• Solderability Test	Weekly	MIL-STD-883C, 2003-3
• Mark Permanency Test	Weekly	MIL-STD-883C, 2015-4
• Lead Integrity Test	Weekly	MIL-STD-883C, 2004-4
• In-Process Monitor Inspection for Product	4 Times/Shift/Each Process	Identify for Each Control Limit
• X-Ray Monitor Inspection for Molding	2 Times/Shift/Mold Press	Identify for Each Control Limit
• Monitor Inspection for Production Equipment	2 Times/Shift/Each Unit of Equipment	Identify for Each Control Limit

4. Outgoing quality inspection plan (LTPD)

Defect Class	Discrete	LSI	Kind of Defect
Critical Defect electrical visual	1%	2%	Open, short Wrong configuration, no marking
Major Defect electrical visual	1.5%	3%	Items which affect reliability most strongly
Minor Defect electrical visual	2%	5%	Items which minimally or do not affect reliability at all (cosmetic, appearance, etc.)

Figure 10. General Assembly Flow

<table>
<tr><th>Process Flow</th><th>Process Step</th><th>Major Control Item</th></tr>
<tr><td rowspan="11">  </td><td>Wafer

Wafer Incoming Inspection</td><td>Q.C. Wafer Incoming Inspection AQL 4.0%</td></tr>
<tr><td>Tape Mount</td><td></td></tr>
<tr><td>Sawing Q.C. Monitor</td><td>Q.C. Monitoring:
— Chip-out — Scratch
— Crack — Sawing Discoloration
— Sawing-speed — Cut Count
— D.I. Purity — CO_2 Bubble Purity</td></tr>
<tr><td>Visual Inspection</td><td>100% Screen:
— FAB Defect
— EDS Test Defect
— Sawing & Scratch Defect</td></tr>
<tr><td>Q.C. Gate</td><td>1st AQL 1.0%
Reinspection AQL: 0.65%</td></tr>
<tr><td>Lead Frame (L/F)</td><td></td></tr>
<tr><td>Lead Frame Incoming</td><td>*Q.C.L/F Incoming Inspection
1. Acceptance Quality Level
— Dimension LTPD 20%, C = 0
— Visual & Mechanical: LTPD 10%, C = 2
— Functional Work Test: LTPD 10%, C = 2</td></tr>
<tr><td>Die Attach (D/A)</td><td></td></tr>
<tr><td>Q.C. Monitor</td><td>*Q.C.D/A Monitor Inspection
1. Bond force
2. Frequency: 4 Times/Station/Shift
3. Sample: 24 ea Time
4. Acceptance Criteria
<table><tr><th>Defect</th><th>Acceptance</th><th>Reject</th></tr><tr><td>Critical</td><td>0</td><td>1</td></tr><tr><td>Major</td><td>1</td><td>2</td></tr></table></td></tr>
<tr><td>Cure</td><td></td></tr>
</table>

Figure 10. General Assembly Flow (Continued)

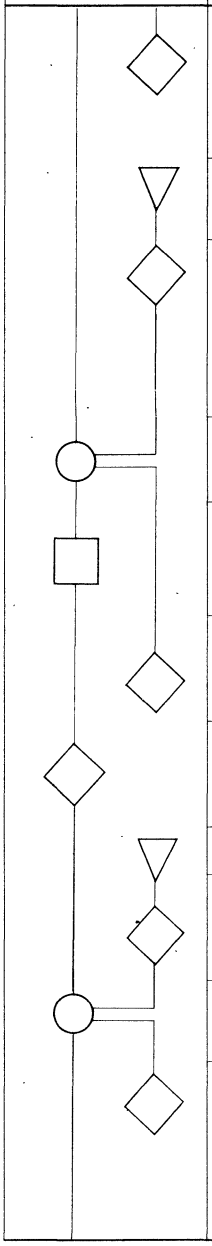
Process Flow	Process Step	Major Control Item
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/out Time 2. Frequency — 1 Time/Shift
	Au Wire	
	Bonding Wire Incoming Inspection	*Q.C Au Wire Incoming Inspection 1. Visual Inspection: N = 5, C = 0 2. Bond Pull Test Strength Test: N = 13, C = 0 3. Bondability Test — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Wire Bonding (W/B)	
	100% Visual Inspection	
	Q.C. Monitor	*Q.C. W/B Monitor Inspection 1. Frequency: 6 Times/Mach/Shift
	Q.C. Gate	1. Q.C. Acceptance Quality Level — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold Compound	
	Incoming Inspection Mold	*Moldability Test — Critical Defect: AQL 0.15% — Major Defect: AQL 1.0% — Minor Defect: AQL 1.5%
	Mold	
	Q.C. Monitor	*Q.C. Mold Monitor Inspection 1. In-Process Monitor Inspection — Frequncy: 4 Times/Station/Shift — Sample: 200 Units/Time 2. Acceptance Quality Level — Critical Defect: AQL 0.25% — Major Defect: AQL 0.4%

Figure 10. General Assembly Flow (Continued)

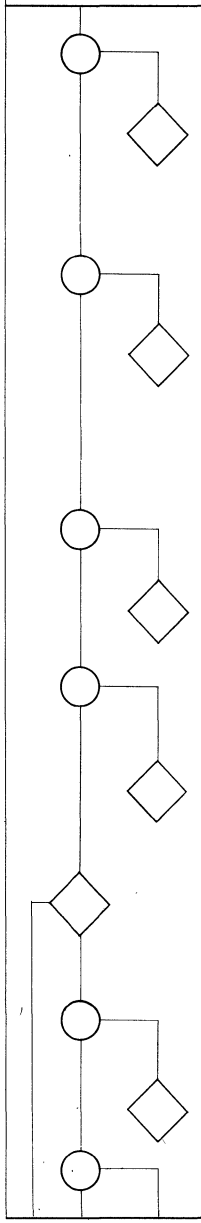
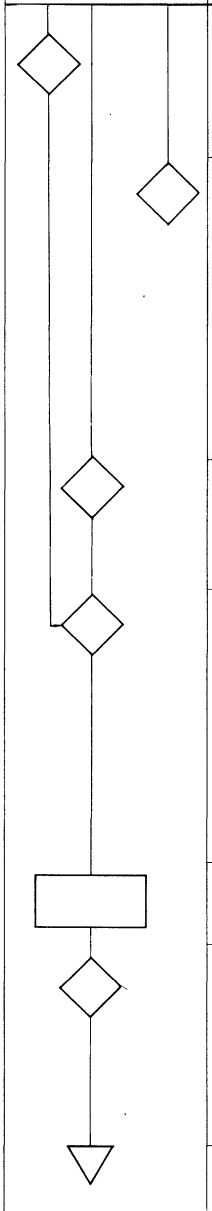
Process Flow	Process Step	Major Control Item
	Cure	
	Q.C. Monitor	*Q.C. Cure Monitor Inspection 1. Control Item — Temperature — In/out Time 2. Frequency — 1 Time/shift
	Deflash	
	Q.C. Monitor	*Q.C. Deflash Monitor Inspection 1. Control Item — Pressure — Belt Speed — Visual/Mechanical Inspection 2. Frequency: 4 Times/Mach/Shift 3. Identify each Defect Control Limit
	TRIM/BEND	
	Q.C. Monitor	*Q.C. Trim/Bend Monitor Inspection 1. Visual Inspection 2. Frequency: 4 Times/Station/Shift
	Solder	100% Visual Inspection
	Q.C. Monitor	*Q.C. Solder Monitor Inspection 1. Frequency: 4 Times/Mach/Shift 2. Criteria — Critical Defect: AQL 0.65% — Major Defect: AQL 1.0%
	Q.C. Gate	*Q.C. Mold Gate — Acceptance Criteria Critical Defect: AQL 0.15% Major Defect: AQL 0.4% Minor Defect: AQL 0.65%
	Test	100% Electrical Test
	Q.C. Monitor	Correlation Sample Reading for Initial Device Test
	Mark	100% Visual Inspection

Figure 10. General Assembly Flow (Continued)

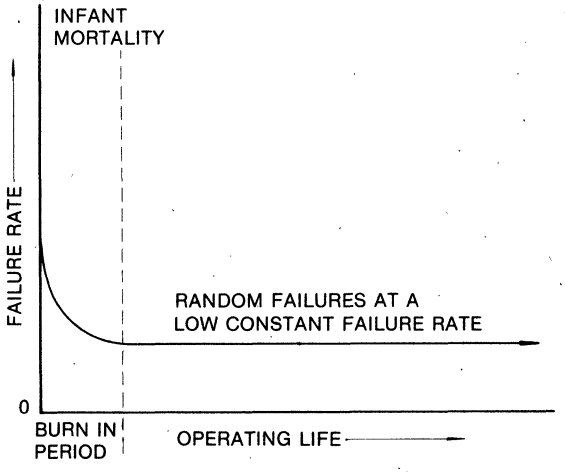
<table>
<tr><th>Process Flow</th><th>Process Step</th><th>Major Control Item</th></tr>
<tr><td rowspan="8">  </td><td>PRT Monitoring
(Process Reliability
Testing)</td><td>1. PRT
— HOPL (168 HRS), PCT (48 HRS)
— Other (when applicable)
2. Acceptance Criteria: LTPD 10%</td></tr>
<tr><td>Q.C. Monitor</td><td>*Q.C. Marking Monitor Inspection
— Frequency: 4 Times/Station/Shift
— Sample: 24 Units/Time
— Identify for Each C.L.
— Acceptance Criteria
<table><tr><th>Defect</th><th>Acceptance</th><th>Reject</th></tr><tr><td>Critical</td><td>0</td><td>1</td></tr><tr><td>Major</td><td>1</td><td>2</td></tr></table></td></tr>
<tr><td>Q.C. Gate</td><td>*Q.C. Final Acceptance Level
— Critical Defect: AQL 0.15%
— Major Defect: AQL 0.4%
— Minor Defect: AQL 0.65%</td></tr>
<tr><td>Q.A. Gate</td><td>*Q.C. Incoming Inspection
1. Critical Defect:
— Electrical Test: LTPD 2% (N = 116, C = 0)
— Visual Test: LTPD 2% (N = 116, C = 0)
2. Major Defect:
— Electrical Test: LTPD 3% (N = 116, C = 1)
— Visual Test: LTPD 3% (N = 116, C = 1)
3. Minor Defect:
— Electrical Test: LTPD 5% (N = 116, C = 2)
— Visual Test: LTPD 5% (N = 116, C = 2)</td></tr>
<tr><td>Stock</td><td>*Age Control</td></tr>
<tr><td>Q.A. Gate</td><td>*Q.A. Outgoing Inspection
1. Quantity
2. Customer
3. Packing
4. Sampling Inspection (when applicable)
— Sampling plan is same as incoming Inspection</td></tr>
<tr><td>Shipment</td><td></td></tr>
</table>

SST's BEST PROGRAM

The SST Best Program has been designed to offer the customer an alternative to standard off-the-shelf plastic encapsulated LINEAR circuits. The Best Program will significantly reduce incoming inspection requirements as well as early device failures (infant mortalify). These results are achieved by a tightened AQL inspection plan and a burn-in of each unit for 160 +8, −0 hours at 125°C or equivalent conditions established from a time/temperature regression curve.

The AQL Plan. Acceptable Quality Levels (AQL) are a measure of the quality of outgoing LINEAR circuits. These levels are established by the manufacturer to show the process percent defective being produced and to ensure that the customer is receiving material that meets his requirements. The SST Best Program has tightened these AQL levels to a point at which incoming inspection by the customer is no longer a necessity. Best product quality is monitored significantly more closely than standard product; those lots which fall the AQL level are 100% reworked before resubmission to the AQL gate.

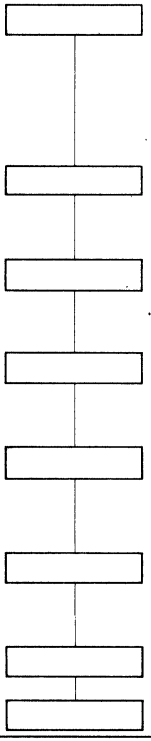
The Reliability Plan. Reliability is the statistical probability that a product will give satisfactory performance for a specified period of time when used under specified conditions. A typical rate curve is shown below:



Reliability theory assumes that devices fail according to the above curve. When a group of devices is manufactured a small portion of the units will be inherently weaker than the average. These weak units will probably fail during the first few hours of operation—hence the term "infant mortality." If the units are burned-in however, thereby allowing the weak units to fail, there is a much lower probability that those finally put into system use will fail.

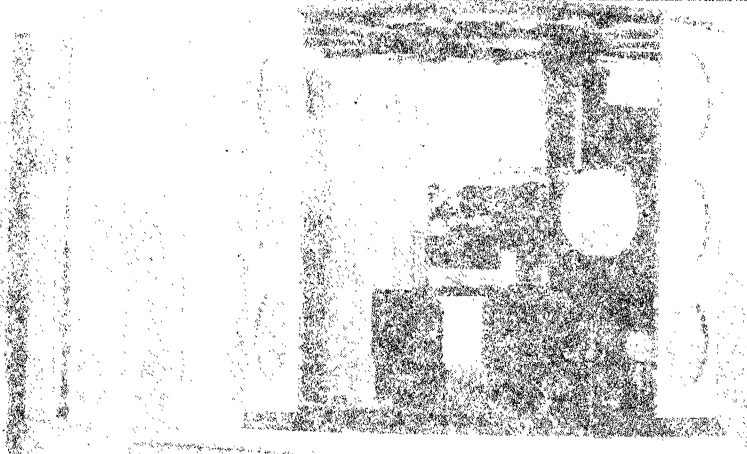
The SST Best Flow. In order to achieve an extremely high quality unit and reduce infant mortality failures the following flow has been established:

Process Flow

FLOW CHART	DESCRIPTION
	WAFER FABRICATION LINEAR PROCESS CV PLOTS OXIDE THICKNESS MEASUREMENTS OPTICAL INSPECTIONS SEM ANALYSIS
	ENCAPSULATION MOLDING COMPOUND ULTRA PURE FOR LINEAR APPLICATIONS
	POST MOLD BAKE 6 HOURS AT 175 DEG. C. CURES PLASTIC STRESSES ALL WIRE BONDS AND DIE
	O/S FUNCTIONAL ELECTRICAL 100% TESTING OPENS/SHORTS AND INTERMITTENTS REMOVE
	HIGH TEMPERATURE BURN-IN 160 HOURS AT 125 DEG. C. OR EQUIVALENT CONDITIONS ESTABLISHED FROM A TIME/ TEMPERATURE REGRESSION CURVE. 0.96 eV
	FULL FUNCTIONAL AND PARAMETRIC ELECTRICAL TESTING 100% ELECTRICAL TESTING AC, DC 88 DEG. C.
	TIGHT AQL SAMPLING PLAN ELECTRICAL – 0.05% AQL AT 88 DEG. C. MECHANICAL – 0.01% AQL CRITICAL & MAJOR
	SHIP UNITS

NOTE

PRODUCT GUIDE 2



1. Function Guide
2. Cross Reference Guide
3. Ordering Information

1. TELECOMMUNICATION APPLICATION

Application	Type	Package	Circuit Function
Tone Ringer	KA2410 KA2411	8 DIP	Adjustable warbling and 2 frequency tone External triggering or ringer disable (KA2410) Adjustable supply initiating current (KA2411) Built-in hysteresis
Tone Ringer with Bridge Rectifier	†KA2418	8 DIP	Protect against over voltage Low current consumption Allow the parallel operation of 4 devices Built-in hysteresis External components are minimized High output voltage Included bridge diode
DTMF Dialer	KS5808	16 DIP	Direct telephone line operation Standard 2 of 8 key board use Tone output: Bipolar output Mute output: N-CH open drain
	†KA2413	16 DIP	Wide operating line voltage and current range Short start up time External components are minimized Internal protection of all inputs
PULSE Dialer	KS5805A/B	18 DIP	KS5805A: Pin 2; Vref KS5805B: Pin 2; Tone output RC oscillator used as frequency reference Pulse output: "0" true Mute output: "0" true
DTMF/Pulse Switchable Dialer	†KS58A/B/C/D19	22 DIP	Tone/pulse switchable dialing, touch key or slide switch 32 digit redialing & PABX auto pause time Make/break ratio pin selectable KS5821 (Telephone lock function)
	†KS58A/B20	18 DIP	
	††KS58A/B/C/D21	22 DIP	

† New Product
†† Under Development

TELECOMMUNICATION APPLICATION (Continued)

Application	Type	Package	Circuit Function
DTMF/Pulse Switchable with 10 No. Memory	††KS5823	18 DIP	10 No. x 18 digit memory including a redial memory Including PABX auto pause time 10 pps/20 pps pin selectable Make/break ratio: 40%/60%
Speech Network	KA2412A	14 DIP	Transmit/Receiver amplifier Side tone control On chip regulator
Low Voltage Speech Network with Dialer Interface	†KA2425A/B	18 DIP	Low Voltage Operation (1.5V) Tx, Rx & side tone gain set by external resistors Loop length equalization for Tx, Rx & sidetone Provides regulated voltage for CMOS dialer DTMF level adjustable with a single resistor A: Mute active low B: Mute active high
Tone Decoder	LM567C/L	8 DIP 8 SOP	Touch tone decoding Sequential tone decoding Communication paging High stable center frequency LM567L: Micropower (4mW at 5V) dissipation
FM IF Amplifier	MC3361	16 DIP 16 SOP	Small current dissipation (Typ. 3.5mA: V_{CC} 4.0V) Excellent input sensitivity Minimum number of external parts required Used to cordless telephone parts required Work from 1.8V to 7.0V
μ-Law Codec	†KT5116J	16 DIP	μ-255 companding law ±5V operation Synchronous or Asynchronous operation On-chip sample and hold.
Codec Filter	†KT3040J	16 DIP	Exceeds all D3/D4 and CCITT spec. ±5V operation Law power consumption 20dB gain adjust range Sin X/X correction in receive filter TTL and CMOS compatible logic
μ-Law Combo Codec	††KT3054J	16 DIP	Exceeds all D3/D4 and CCITT spec. Complete CODEC and filtering system including ±5V operation Low power consumption TTL and CMOS compatible logic Receive push-pull power amp (KT3064)
	††KT3064J	20 DIP	

† New Product
†† Under Development

TELECOMMUNICATION APPLICATION (Continued)

Application	Type	Package	Circuit Function
Line Driver	MC1488	14 DIP 14 SOP	Conformance EIA standard No. RS-232C & V28 (CCITT) Quad line driver Interface between data terminal equipment (DTE) and data communication equipment (DCE) Current limited output: ±10mA typ. Power-off source impedance 300 ohms min. Compatible with DTL and TTL, HCTLS families Flexible operating supply range
Line Receiver	MC1489/A	14 DIP 14 SOP	Conformance EIA standard No. RS-232C & V28 (CCITT) Quad line receiver Interface between data terminal equipment (DTE) and data communication equipment (DCE) Input signal range ±30 volts Input threshold hysteresis built in Response control a) Logic threshold shifting b) Input noise filtering
Fluorescent Display Driver	††KA2651	18 DIP	Consisting of 8 NPN darlington output stages and associated common-emitter input stages Digit or segment drivers Low input current, internal output pull-down resistors High output breakdown voltage Single or split supply operation
8-Channel Source Driver	KA2580A	18 DIP	TTL, CMOS, PMOS, NMOS compatible High output current ratings Internal transient suppression Efficient input/output pin structure Low voltage LEDs and incandescent lamp
	KA2588A	20 DIP	KA2588A: Separated logic and driver supply line
Universial Asynchronous Receiver and Transmitter (UART)	††KS5824 †KS5812	24 DIP 40 DIP	The data formatting and control to interface serial asynchromous data communications between main system and subsystems. Low power, high speed CMOS process Serial/parallel conversion of data 8 and 9 bit transmission Programmable control register Optional ÷1, ÷16, and ÷64 clock modes Peripheral/modem control functions Double buffered Included 4 UART in one chip (KS5812)

† New Product
†† Under Development

2. VOLTAGE REGULATOR

A. 3-Terminal Fixed Positive Voltage Regulator

Function	Type	Package	Features	Application
High output Current (I_O = 1A)	MC78XX series	TO-220	Maximum output current 1A External components are minimized Internal protection circuit for output short Positive voltage regulator Variable application control	5V, 6V, 8V, 8.5V, 9V, 10V 11V, 12V, 15V, 18V and 24V fixed output voltage
Medium output current (I_S = 500mA)	MC78MXXC AC Series	TO-220	Maximum output current 500mA External components are minimized Internal protection circuit for output short Positive voltage regulator Variable application circuit	5V, 6V, 8V, 10V, 12V, 15V, 18V and 24V fixed output voltage
Low Output Current (I_O = 100mA)	MC78LXXAC series	TO-92	Output current in excess of 100mA External component minimized Internal protection circuit for output short Positive voltage regulator Variable application circuit	2.6V, 5V, 6.2V, 8V, 8.2V, 9V, 12V, 15V, 18V and 24V fixed output voltage
3A Output Current	†KA78TXX Series	TO-220	Maximum output current 3A No external components required Internal protection circuit for output short Power dissipation: 25W	5V, 6V, 8V, 12V 15V, 18V, 24V fixed output voltage
3A, 5V Positive Regulator	LM323	TO-39	Maximum output current 3A Internal current and thermal limiting. Positive voltage regulator	5V

B. 3-Terminal Fixed Negative Voltage Regulator

Function	Type	Package	Features	Application
High output Current (I_O = 1A)	MC79XXC series	TO-220	Output current in excess of 1A Internal thermal overload protection Internal short circuit current limiting	−2V, −5V, −6V, −8V, −10V, −12V, −15V, −18V, and −24V, fixed output voltage
Medium Output Current (I_O = 500mA)	MC79MXXC Series	TO-220	Output current in excess of 500mA Internal overload protection Internal short circuit current limiting	−2V, −5V, −6V, −8V, −10V, −12V, −15V, −18V and 24V fixed output voltage
Low Output Current (I_O = 100mA)	††MC79LXXAC	TO-92	Output current in excess of 100mA Internal short circuit current limiting External component minimized	−5V, −12V, −15V, −18V and −24V fixed output voltage

† New Product
†† Under Development

C. Precision Voltage Regulator

Function	Type	Package	Features	Application
Precision Regulator	LM723	14 DIP	Positive or negative supply operation Series, shunt, switching or floating operation 0.01% line and load regulation Output current to 150mA without external pass transistor	Output voltage adjustable from 2 to 37V
33V Regulator	KA33V	TO-92	Low temperature coefficient Low dymic resistance	Electronic tuning system
Adjustable Regulator	††LM317	TO-220	Output current in excess of 1.5A Output adjustable from 1.2V to 37V Internal short circuit current limiting	Floating operation for high voltage operation Eliminates stocking many fixed voltage
	††KA337	TO-220	Adjustable 3-terminal negative voltage regulator Line regulation typically 0.01%/V Load regulation typically 0.3% Internal thermal overload protection 1.5A output current	Output voltage adjustable from −1.2V to −37V
	††KA350	TO-3P	Adjustable 3-terminal positive voltage regulator 3A output current Guaranteed thermal regulation	Output voltage adjustable from 1.2V to 25V

D. Switching Voltage Regulator

Function	Type	Package	Features	Application
Adjustable 1.25V to 40V	KA78S40	16 DIP ††16 SOP	Peak output current of 1.5A without external transistor 80dB line and load regulation Operation from 2.5V to 40V	Step-down converter Step-up converter Inverter
PWM 100KHz	†KA3524	16 DIP	PWM power control circuitry Frequency adjustable to greater than 100KHz Total supply current is less than 10mA Single ended or push-pull output	Switching regulator Trans DC-DC converter Inverting voltage regulator

3. PRECISION VOLTAGE REFERENCE

Function	Type	Package	Features	Application
Adjustable Reference	KA431	TO-92 †8 DIP †8 SOP	Programmable output voltage from V_{ref} to 36V Voltage reference tolerance: ±1.0% Low output noise voltage	Switching regulator Constant current source Constant current sink
5V Reference	†KA336	TO-92	Adjustable 4V to 6V Low temperature coefficient 0.6Ω dynamic impedance Fast Turn-on	Adjustable shunt regulator Precision power regulator
1.235V Reference	KA385	TO-92	Low temperature coefficient operating current of 10μA to 20mA 1Ω dynamic impedance	Micropower reference

4. OPERATIONAL AMPLIFIER

Function	Type	Package	Features	Application
OP AMP	LM741	8 DIP 8 SOP	Internal frequency compensation Short circuit protection	Comparator, DC amp, Multivibrator, Summing amp, Integrator or differentiator Narrow band or BPF
	KA301A	8 DIP 8 SOP	Slew rate of 10V/μs as a summing amplifier External frequency compensation	Variable capacitance Multiplier Sine wave oscillator
	††KF351	8 DIP 8 SOP	JFET input Low input bias current High slew rate 13V/μs Wide gain bandwidth	High speed intergrators Fast D/A converters Sample and hold circuits
	KA733	14 DIP 14 SOP	120MHz band width Selectable gains of 10, 100, 400 No frequency compansation	Disk file memories Magnetic tape systems Wide band video amplifiers
Dual OP AMP	MC4558 MC1458	8 DIP 8 SOP	Internal frequency compensation Low noise operation	Phone pre-amplifier Tape playback amplifier Schmitt trigger.
	LM358/A LM258/A LM2904	8 DIP †8 SOP	Internal frequency compensation for unit gain Large DC voltage gain Wide power supply range	DC summing amplifier Power amplification RC active bandpass filter Compatible with all forms of logic
	†KA9256	10 SIP H/S	Internal current limiting: I_{SC} = 350mA Internal frequency compensation Minimal cross over distortion	High power amplifier CD driver
Quad OP AMP	LM324/A LM224/A LM2902	14 DIP 14 SOP	Internal frequency compensation Wide supply voltage range Single supply: DC 3V ~ 30V Dual supply: DC ± 1.5V ~ ± 15V	Audio power booster DC amp, Multivibrator Switch, Comparator Schmitt trigger
	LM348 LM248	14 DIP 14 SOP	Each amplifier is functionally equivalent to the LM741 Pin compatible with LM324 Short circuit protection	Comparator with hysteresis Voltage reference
	MC3403 †MC3303	14 DIP 14 SOP	Class AB output stage for minimal crossover distortion Single or split supply operation Internal frequency compensation	Comparator with hysteresis Bi-Quad filter

† New Product
†† Under Development

5. VOLTAGE COMPARATOR

Function	Type	Package	Features	Application
Single Comparator	LM311 †LM211	8 DIP †8 SOP	Operates from single 5V supply Maximum input current: 250nA Maximum offset current: 50nA Differential input voltage range: ±30V Power consumption: 135mW at +15V	Multivibrator output is compatible with DTL and as well as MOS circuits voltage controlled oscillator
	††KA361 ††KA261	14 DIP	Independent strobes Guaranteed high speed: 20nS max. Complementary TTL outputs	High speed analog to digital converter Zero-crossing detectors
	KA710C	14 DIP †14 SOP	Low offset and thermal drift Compatible with practically all types of integrated logic	Interface between logic types Level detector with lamp
Dual Comparator	LM393/A LM2903 LM293	8 DIP 8 SOP	High precision comparators Reduced V_{os} drift over temperature Eliminates need for dual supply Allows sensing near ground Compatible with all forms of logic Power drain suitable for battery operation Low input biasing current: 25nA Low output saturation voltage 250mV at 4mA	Output voltage compatible with TTL, DTL, ECL and CMOS logic system Basic comparator Pulse generator MOS clock driver
	KA319 KA219	14 DIP †14 SOP	Two indepentent comparators Operates from a single 5V High common mode slew rate	Relay driver Window detector
Quad Comparator	LM339/A LM2901 LM239 LM3302	14 DIP 14 SOP	Wide single supply voltage range or dual supplies Very low supply current drain (0.8mA)-independent of supply voltage (2mW/Comparator at +5V DC) Low input biasing current: 25nA Input common-mode voltage range includes GND Low output saturation voltage 250mV at 4mA	Compatible with all forms of logic Bi-stable multivibrator One-shot multivibrator Time delay generator Square wave oscillator Pulse generator Limit comparator Crystal controlled oscillatgor

† New Product
†† Under Development

6. TIMER

Function	Type	Package	Features	Application
Single Timer	NE555	8 DIP †8 SOP	Maximum operating frequency: 500KHz Adjustable duty cycle	Precision timing Pulse generator
	KS555 †KS555H	8 DIP †8 SOP	Low power consumption by using CMOS process High speed operation Wide operation supply voltage: 2 to 18 volts Pin compatible with NE555	Precision timing Pulse generator
Dual Timer	NE556	14 DIP †14 SOP	TTL Compatible Dual NE555	Time delay generation
	†KS556	14 DIP †14 SOP	Low power consumption by using C-MOS process Pin compatible with NE556	Time delay generation
Quad Timer	†NE558	16 DIP	Wide supply voltage range: 4.5 to 16V 100mA output current per section Time period equal RC	Quad monostable Sequential timing Precision timing

7. DATA CONVERTER ICs

Functions	Type	Package	Features	Applications
A/D, D/A Converter	†KSV3100A	40 DIP	High speed 8-bit A/D and 10-bit D/A converter on the single chip construction	Image processing Video/Graphics
	††KSV3110	40 DIP	Enhanced version of KSV3100A	
A/D Converter	††KSV3208	28 DIP	High speed 8-bit A/D converter	Image processing Video/Graphics
	†KAD0808/9	28 DIP	8-bit μP-compatible A/D converter with 8-channel multiplexer linearity error KAD0808: ±1/2 LSB KAD0809: ±1 LSB	General purpose and μP-interface system
	††KAD0820A/B	20 DIP	8 bit μP-compatible A/D converter with Track/Hold function linearity KAD0820A: ±1/2 LSB KAD0820B: ±1 LSB	
DMM A/D	†KS7126	40 DIP	3-1/2 digit LCD driver A/D converter	Digital multi-meter
D/A Converter	††KSV3404		High speed quad 4-bit D/A converter	Video/Graphics
	††KDA0800	16 DIP	8-bit D/A converter	General purpose and μP-interface system
	††KDA0808	16 DIP	8-bit D/A converter	
S.A.R.	††KS25C02 ††KS25C03	16 DIP	8-bit CMOS successive approximation registers	SAR of A/D converter
	††KS25C04	24 SDIP	12-bit CMOS successive approximation registers	

† New Product †† Under Development

8. MISCELLANEOUS ICs

Function	Type	Package	Features	Application
Toy Radio Control Actuator	KA2303	9 SIP	High gain amplifier, Peak detector, T flip-flop, comparator with hysteresis, regulator, motor driver	3 Function
	†KA2304	9 SIP		2 Function
	††KA2307	16 DIP	Receiver	5 Function
	††KA2308	14 DIP	Transmitter	5 Function
DC Motor Speed Controller	KA2401	8 DIP	Stable voltage reference V_{ref} = 1.27V (Typ.)	V_{CC} = 4 ~ 12V
	KA2404	TO-92L		
	KA2402	8 DIP	Stable current source	V_{CC} = 1.8 ~ 8V
	†KA2407	TO-126	Stable voltage reference V_{ref} = 1.0V (Typ.)	V_{CC} = 3.5 ~ 14.4V
Earth Leakage Detector	KA2803	8 DIP	Low power consumption High noise immunity Few external components	Earth leakage detector
Zero Voltage Switch	KA2804	8 DIP	Easy operation either through the AC line or a DC supply Supply voltage control External component are minimized Negative output current pulse up to 250mA (short circuit protection)	ON, OFF temperature control Time proportional temperature control

† New Product
†† Under Development

1. TELECOMMUNICATION ICs

A. Dialer

Application	SAMSUNG	MOSTEK	AMI	UMC	SHARP	Others
Pulse Dialer	KS5805A KS5805B	*MK50992 *MK50993	S2560A/B	*T40992 *T40993	*LR40992 *LR40993	
DTMF Dialer	KS5808 KA2413	*MK5089 *PBD3535 (RIFA)	*S25089	*UM95089 UM95087	*LR4089 LR4087	*SBA5089 SBA5091 SBA5099
Tone/Pulse Switchable with Redial Memory	†KS5819 †KS5820 ††KS5821	MK5370		*UM91230 *UM91210	LR48081 LR48082	*S7230A/B *LC7360
Tone/Pulse Switchable with 10 No. Memory	††KS5823	MK5380 MK5375/6		UM91250 UM91260	LR4803	PCD3315

B. Tone Ringer

Application	SAMSUNG	MOTOROLA	SGS	MITEL	CHERRY	Others
Tone Ringer	KA2410			*ML8204	*CS8204	*TA31001
	KA2411			*ML8205	*CS8205	*TA31002
1 Chip Tone Ringer	†KA2418	MC34012/7	*LS1240			

C. Speech Network

Application	SAMSUNG	SGS	RIFA	ITT	ERSO	Others
Subset Amplifier	KA2412A	*LS285/A	PBL3726	TEA1045	*CIC9185	
Speech Network with Dialer Interface	†KA2425A †KA2425B	LS356	PBL3781			*MC34014 (MOTOROLA)

D. Tone Decoder

Application	SAMSUNG	NATIONAL	SHARP	SIGNETICS	Others
Tone Decoder	LM567	*LM567	*IR3N05	*NE567	*XR567 (EXAR)
	LM567L				*XRL567 (EXAR)

† New Product
†† Under Development

E. FM IF Amplifier

Application	SAMSUNG	MOTOROLA	SHARP	SPRAGUE	Others
FM IF Amplifier	MC3361	*MC3361	IR3N06	ULN3859	*LM3361

F. Codec, Codec Filter, Combo Codec

Application	SAMSUNG	N/S	FAIRCHILD	SGS	Others		
μ-Law Codec	†KT5116J	*TP5116	*μA5116	*M5116	2910		*MK5116
Codec Filter	†KT3040J	*TP3040	*μA5912	*M5912	*2912		*ETC5040
μ-Law Combo Codec	††KT3064J	*TP3064			2913	MC14400-5	*ETC5064
μ-Law Combo Codec	††KT3054J	*TP3054			*2916		

G. Interfaces

Application	SAMSUNG	MOTOROLA	FAIRCHILD	TI	N/S	EXAR	SIGNETICS
Line Driver	MC1488	*MC1488	*μA1488	*SN75188	*DS1488	*XR1488	*MC1488
Line Receiver	MC1489	*MC1489	*μA1489	*SN75189	*DS1489	XR1489	*MC1489
	MC1489A	*MC1489A	*μA1489A	*SN75189A	*DS1489A	*XR1489A	*MC1489A

H. Driver

Application	SAMSUNG	SPRAGUE	Others
Fluorescent Display Driver	††KA2651	*UCN5815A	
8CH Source Driver	KA2580A	*UDN2580A	
	KA2588A	*UDN2588A	

I. UART

Application	SAMSUNG	HITACHI	MOTOROLA	Others
Single UART	††KS5824	*HD6350	*MC6850	
Quad UART	†KS5812			

† New Product
†† Under Development
* Direct Replacement

2. VOLTAGE REGULATOR

A. 3-Terminal Fixed Positive Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	NEC	MATSUSHITA	Package
MC78XXAC/C Series (I_O = 1A)	MC7805AC/C MC7806AC/C MC7808AC/C MC7885AC/C MC7809AC/C MC7810AC/C MC7811AC/C MC7812AC/C MC7815AC/C MC7818AC/C MC7824AC/C	MC7805AC/C MC7806AC/C MC7808AC/C MC7812AC/C MC7815AC/C MC7818AC/C MC7824AC/C	μA7805 μA7806 μA7808 μA7885 μA7812 μA7815 μA7818 μA7824	μPC7805 μPC7808 μPC7812 μPC7815 μPC7818 μPC7824	AN7805 AN7806 AN7808 AN7812 AN7815 AN7818 AN7824	TO-220
MC78MXXC Series (I_O = 0.5A)	MC78M05C MC78M06C MC78M08C MC78M10C MC78M12C MC78M15C MC78M18C MC78M24C	MC78M05C MC78M06C MC78M08C MC78M12C MC78M15C MC78M18C MC78M24C	μA78M05C μA78M06C μA78M08C μA78M12C μA78M15C μA78M24	μPC78M05 μPC78M08 μPC78M10 μPC78M12 μPC78M15 μPC78M18 μPC78M24	AN78M05 AN78M06 AN78M08 AN78M10 AN78M12 AN38M15 AN78M18 AN78M24	TO-220
MC78LXXAC (I_O = 0.1A)	MC78L26AC MC78L05AC MC78L62AC MC78L08AC MC78L82AC MC78L09AC MC78L12AC MC78L15AC MC78L18AC MC78L24AC	 MC78L05AC MC78L05AC MC78L12AC MC78L15AC MC78L18AC MC78L24AC	 μA78L05AC μA78L62AC μA78L82AC μA78L09AC μA78L12AC μA78L15AC			TO-92
KA78TXXAC/C Series (I_O = 3A)	KA78T05AC/C KA78T06C KA78T08C KA78T12AC/C KA78T15AC/C KA78T18C KA78T24C	MC78T05AC/C MC78T06C MC78T08C MC78T12AC/C MC78T15AC/C MC78T18C MC78T24C				TO-220
LM323 (I_O = 3A)	LM323 (TO-3P)	LM323 (TO-3/TO-220)	SH323 (TO-3)			

B. 3-Terminal Fixed Negative Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	NEC	MATSUSHITA	Package
MC79XXC Series (I_O = 1A)	MC7902C MC7905C MC7906C MC7908C MC7910C MC7912C MC7915C MC7918C MC7924C	MC7905C MC7906C MC7908C MC7912C MC7915C MC7918C MC7924C	μA7905 μA7908 μA7912 μA7915	μPC7905 μPC7908 μPC7912 μPC7915 μPC7918 μPC7924	AN7905 AN7906 AN7908 AN7912 AN7915 AN7918 AN7924	TO-220
MC79MXXC (I_O = 0.5A)	MC79M02C MC79M05C MC79M06C MC79M08C MC79M10C MC79M12C MC79M15L MC79M18C MC79M24C	MC79M05C MC79M12 MC79M15	μA79M05 μA79M08 μA79M12 μA79M15			TO-220
††MC79LXXAC (I_O = 0.1A)	MC79L05AC MC79L12AC MC79L15AC MC79L18AC MC79L24AC	MC79L05AC MC79L12AC MC79L15AC MC79L18AC MC79L24AC				TO-92

C. Precision Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	N/S	NEC	Package
Adjustable Voltage	LM723	MC1723	μA723	LM723		14 DIP
	††LM317	LM317	μA317	LM317		TO-220
Adjustable Voltage	††KA337	LM337		LM337	LM337	TO-220
	††KA350	LM350		LM350	LM350	TO-220
33V Regulator	KA33V				μPC574	TO-92

D. Switching Voltage Regulator

Description	SAMSUNG	MOTOROLA	FAIRCHILD	N/S	TI	Package
Adjustable 1.25V to 40V (fo = 100KHz)	μA78S40	μA78S40	μA78S40			16 DIP
PWM 100KHz	†KA3524			LM3524	SG3524	16 DIP

† New Product
†† Under Development

3. PRECISION VOLTAGE REFERENCE

Description	SAMSUNG	MOTOROLA	FAIRCHILD	N/S	TI	Package
Adjustable Reference (2.5V ~ 36V)	KA431	TL431	μA431		TL431	TO-92 †8 DIP †8 SOP
5V Reference	†KA336			LM336		TO-92
1.235V Reference	††KA385	LM385		LM385		TO-92

4. OPERATIONAL AMPLIFIER

Description	SAMSUNG	MOTOROLA	NATIONAL	FAIRCHILD	MATSUSHITA	Others
Single OP Amp	LM741 KA301/A KA733C ††KF351	MC1741 LM301/A MC1733C LF351	LM741 LM301/A LM733C LF351	μA741 μA301/A μA733C		μPC301C
Dual OP Amp	LM358/A LM258/A LM2904 MC1458 MC4558 †KA9256	LM358/A LM258 LM2904 MC1458 MC4558	LM358/A LM258/A LM2904 LM1458	 μA1458 μA4558	AN6562 AN4558	TA75358 NJM4558 *TA7256
Quad OP Amp	LM324/A LM224/A LM2902 LM348 LM248 MC3403 ††MC3303	LM324/A LM224 LM2902 LM348 LM248 MC3403 MC3303	LM324/A LM224/A LM2902 LM348 LM248	μA324 μA224 μA2902 μA348 μA248 μA3403 μA3303	AN6564	TA75324 NJM3403A

5. VOLTAGE COMPARATOR

Description	SAMSUNG	MOTOROLA	NATIONAL	FAIRCHILD	TI	Others
Single Comparator	LM311 LM211 †KA361 ††KA261 †KA710C	LM311 LM211	LM311 LM211 LM361 LM261 LM710	LM311 μA710C	LM311 LM211 μA710C	LM311
Dual Comparator	LM393/A LM2903 LM293 KA319 ††KA219	LM393/A LM2903 LM293	LM393/A LM2903 LM293 LM319 LM219		LM393/A LM2903 LM293 LM319 LM219	TA75393 AN6914 NJM319
Quad Comparator	LM339/A LM2901 LM239 LM3302	LM339/A LM2901 LM239	LM339/A LM2901 LM239 LM3302	μA339 μA2901 μA239 μA3302	LM339 LM2901 LM239 LM3302	TA75339 AN6912

6. TIMER

Description	SAMSUNG	MOTOROLA	NATIONAL	SIGNETICS	TI	Others
Single Timer	NE555 †KS555H KS555	MC1455	LM555	NE555	NE555 TLC555	TA75555 ICM7555
Dual Timer	NE556 †KS556		LM556	NE556	NE556 TLC556	ICM7556
Quad Timer	†NE558			NE558		

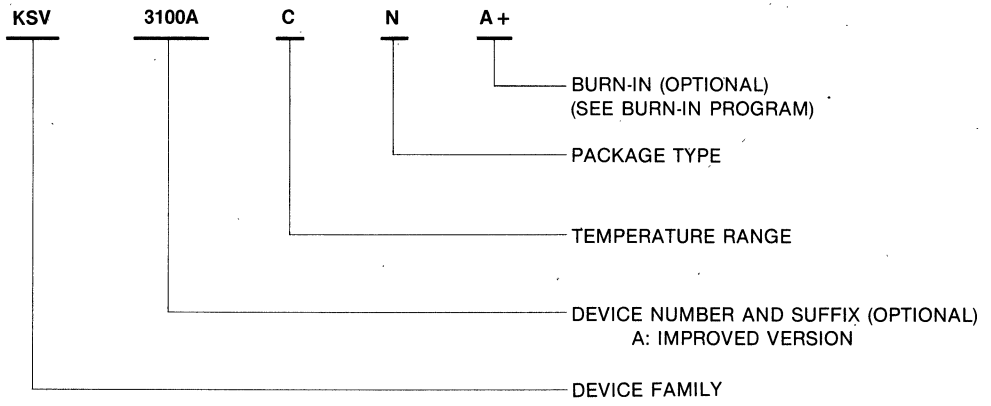
7. DATA CONVERTER ICs

Application	SAMSUNG	NATIONAL	TI	INTERSIL	ITT	Others
A/D-D/A Converter	†KSV3100A				UVC3100 UVC3100	
	††KSV3110					KSV3100A up-date version
High-Speed 8-Bit A/D	††KSV3208					
8-Bit A/D Converter	†KAD0808/9	ADC0808/9	ADC0808/9			
	††KAD0820	ADC0820				ADC82A
3-1/2 DMM A/D	KS7126					TSC7126 ICL7126
4-Bit Triple D/A Converter	††KSV3404					
8-Bit D/A Converter	††KDA0800	DAC0800				DAC82 DAC08
	††KDA0808	DAC0808		AD1408		MC1408
S.A.R.	††KS25C02	DM2502				
	††KS2503	DM2503				
	††KS2504	DM2504				

8. MISCELLANEOUS ICs

Application	SAMSUNG	SEGNETICS	NATIONAL	MITSUBISHI	NEC	Others
Toy Radio Control Actuator	KA2303					3 Function
	†KA2304					2 Function
	††KA2307					5 Function (RX)
	††KA2308					5 Function (TX)
DC Motor Speed Controller	KA2401				μPC1470H	
	†KA2402			AN6612		*LA5521D
	KA2404			AN6610		μPC1470H
	††KA2407			*AN6651		
Earth Leakage Detector	KA2803		LM1851	*M54123		A7390
Zero Voltage SW	KA2804				*μPC1701C	

† New Product †† Under Development * Direct Replacement



TEMPERATURE RANGE

BLANK	SEE INDIVIDUAL SPEC
C	COMMERCIAL 0 ~ +70°C
I	INDUSTRIAL −25 ~ +85°C −40 ~ +85°C
M	MILITARY −55 ~ +125°C

INTEGRATED CIRCUIT

KA	LINEAR IC
KS	CMOS IC
KT	TELECOM IC
LM	NATIONAL
MC	MOTOROLA
NE	SIGNETICS
KSV	A/D-D/A CONVERTER
KAD	A/D CONVERTER
KDA	D/A CONVERTER

PACKAGE TYPE

CODE	PKG. TYPE
D	SOIC
J	CERAMIC DIP
N	PLASTIC DIP (300/600 mil)
S	SIP
Q	FQP
E	SD (400 mil)
B	SSD (Skinny Shrink DIP) (400 mil. Small Pitch)
P	SHD (Shrink DIP) (300 mil. Small Pitch)
W	ZIP
U	PGA
L	LCC
PL	PLCC
M	TO-3
H	TO-3P
Z	TO-92
V	TO-92L
A	TO-126
T	TO-220
X	TO-247
G	BARE CHIP

TELECOM ICs 3

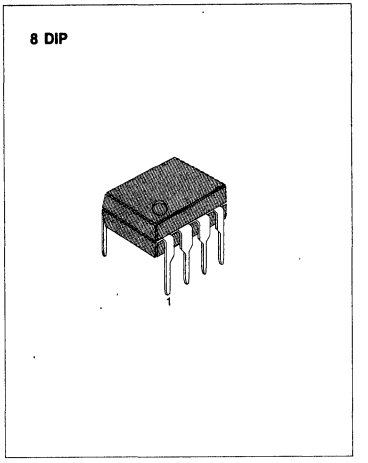
PRODUCT INDEX (Continued)

3. Telecommunication Application

Device	Function	Package	Page
KA2410	Tone Ringer	8 DIP	69
KA2411	Tone Ringer	8 DIP	69
KA2412A	Telephone Speech Circuits	14 DIP	75
KA2413	Dual Tone Multi Frequency Generator	16 DIP	83
KA2418	Tone Ringer with Bridge Diode	8 DIP	108
KA2419	Tone Ringer with Bridge Diode	8 DIP	108
KA2425A/B	Telephone Speech Network with Dialer Interface	18 DIP	112
KS5805A/B	Telephone Pulse Dialer with Redial	18 DIP	130
KS5808	Dual Tone Multi Frequency Dialer	16 DIP	146
KS5812	Quad Universial Asychronous Receiver and Transmitter	40 DIP	152
KS5819	Tone/Pulse Dialer with Redial	22 DIP/SDIP	162
KS5820	Tone/Pulse Dialer with Redial	18 DIP	172
KS5821	Tone/Pulse Dialer with Redial	22 DIP/SDIP	162
KS5824	Universial Asychronous Receiver and Transmitter	24 DIP	180
KT3040J	PCM Monolithic Filter	16 CERDIP	191
KT3054J	COMBO CODEC	16 CERDIP	200
KT3064J	COMBO CODEC	20 CERDIP	214
KT5116J	μ-Law Companding CODEC	16 CERDIP	226
LM567C	Tone Decoder	8 DIP/8 SOP	239
LM567L	Micropower Tone Decoder	8 DIP/8 SOP	247
MC1488	Quad Line Driver	14 DIP/14 SOP	257
MC1489/A	Quad Line Receiver	14 DIP/14 SOP	264
MC3361	Low Power Narrow Band FM IF	16 DIP/16 SOP	270
KA2580A	8-Channel Source Drivers	18 DIP	599
KA2588A	8-Channel Source Drivers	20 DIP	599
KA2651	Fluorescent Display Drivers	18 DIP	604

TONE RINGER

The KA2410/KA2411 is a bipolar integrated circuit designed for telephone bell replacement.



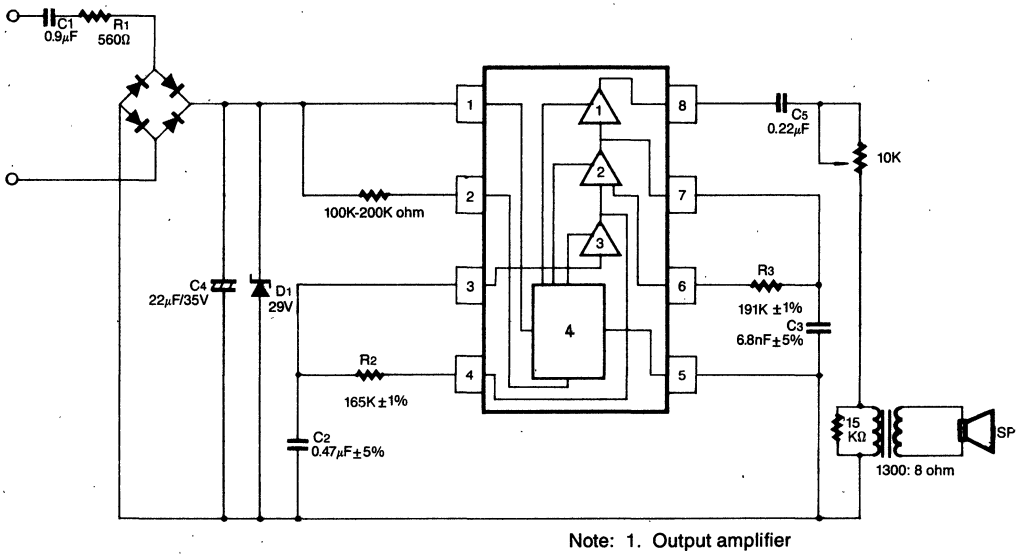
FUNCTIONS

- Two oscillators
- Output amplifier
- Power supply control circuit

FEATURES

- **Designed for telephone bell replacement**
- **Low current drain.**
- **Small size 'MINIDIP' package.**
- **Adjustable 2-frequency tone.**
- **Adjustable warbling rate.**
- **Built-in hysteresis prevents false triggering and rotary dial 'CHIRPS'**
- **Extension tone ringer modules**
- **Alarms or other alerting devices.**
- **External triggering or ringer disable (KA2410).**
- **Adjustable for reduced supply initiation current (KA2411)**

APPLICATION CIRCUIT 1 (KA2410)



Note: 1. Output amplifier
2. High frequency oscillator
3. Low frequency oscillator
4. Hysteresis regulator

Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	30	V
Power Dissipation	P_D	400	mW
Operating Temperature	T_{opr}	−45 to 65	°C
Storage Temperature	T_{stg}	−65 to 150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

(All voltage referenced to GND unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage	V_{CC}				29.0	V
Initiation Supply Voltage[1]	V_{SI}	See Fig. 2	17	19	21	V
Initiation Supply Current[1]	I_{SI}	KA2411-6.8K-Pin 2 to GND	1.4	2.5	4.2	mA
Sustaining Voltage[2]	V_{SUS}	See Fig. 2	9.7	11.0	12.0	V
Sustaining Current[2]	I_{SUS}	No Load $V_{CC}=V_{SUS}$, See Fig. 2	0.7	1.4	2.5	mA
Trigger Voltage[3]	V_{TR}	KA2410 Only V_{CC} =15V	9.0	10.5	12.0	V
Trigger Current[3]	I_{TR}	KA2410 Only		20.0	1000[5]	μA
Disable Voltage[4]	V_{DIS}	KA2410 Only			0.5	V
Disable Current[4]	I_{DIS}	KA2410 Only	−40	−50		μA
Output Voltage High	V_{OH}	V_{CC}=21V, I_8=−15mA Pin 6=6V, Pin 7=GND	17.0	19.0	21.0	V
Output Voltage Low	V_{O1}	V_{CC}=21V, I_8=15mA Pin 6=GND, Pin 7=6V			1.6	V
I_{IN} (Pin 3) I_{IN} (Pin 7)		Pin 3=6V, Pin 4=GND Pin 7=6V, Pin 6=GND	— —	— —	500 500	nA nA
High Frequency 1 High Frequency 2 Low Frequency	f_{H1} f_{H2} f_L	R_3=191K, C_3=6800pF R_3=191K, C_3=6800pF R_2=165K, C_2=0.47μF	461 576 9.0	512 640 10	563 704 11.0	Hz Hz Hz

• NOTE (see electrical characteristics sheet)

1. Initiation supply voltage (V_{SI}) is the supply voltage required to start the tone ringer oscillating.
2. Sustaining voltage (Vsus) is the supply voltage required to maintain oscillation.
3. V_{TR} and I_{TR} are the conditions applied to trigger in to start oscillation for $V_{SUS} \leqq V_{CC} \leqq V_{SI}$
4. V_{DIS} and I_{DIS} are the conditions applied to trigger in to inhibit oscillation for $V_{SI} \leqq V_{CC}$
5. Trigger current must be limited to this value externally.

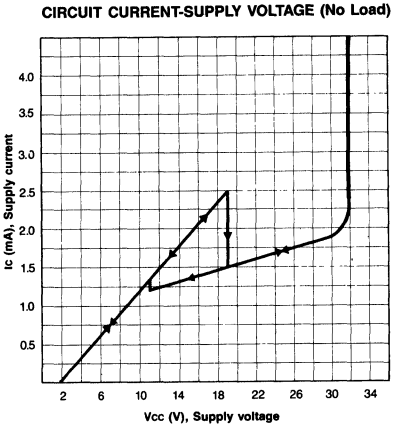


Fig. 2

APPLICATION NOTE

The application circuit illustrates the use of the KA2410/KA2411 devices in typical telephone or extension tone ringer application.

The AC ringer signal voltage appears across the TIP and RING inputs of the circuit and is attenuated by capacitor C_1 and resistor R_1.

C_1 also provides isolation from DC voltages (48V) on the exchange line.

After full wave rectification by the bridge diode, the waveform is filtered by capacitor C_4 to provide a DC supply for the tone ringer chip.

As this voltage exceeds the initiation voltage (V_{SI}),oscillation starts.

With the components shown, the output frequency chops between 512 (f_{h1}) and 640Hz (f_{h2}) at a 10Hz (f_L) rate.

The loudspeaker load is coupled through a 1300Ω to 8Ω transformer.

The output coupling capacitor C_5 is required with transformer coupled loads.

When driving a piezo-ceramic transducer type load, the coupling C_5 and transformer (1300Ω: 8Ω) are not required. However, a current limiting resistor is required.

The low frequency oscillator oscillates at a rate (f_L) controlled by an external resistor (R_2) and capacitor (C_2).

The frequency can be determined using the relation $f_L = 1/1.289\ R_2.\ C_2$. The high frequency oscillates at a f_{H1}, f_{H2} controlled by an external resistor (R_3) and capacitor (C_3). The frequency can be determined using the relation $f_{HI} = 1/1.504\ R_3.\ C_3$. $f_{H2} = 1/1.203\ R_3,\ C_3$.

Pin 2 of the KA2411 allows connection of an external resistor R_{SL}, which is used to program the slope of the supply current vs supply voltage characteristics (see Fig 4), and hence the supply current up to the initiation voltage (Vsi). This initiation voltage remains constant independent of R_{SL}.

The supply current drawn prior to triggering varies inversely with R_{SL}. decreasing for increasing value of resistance. Thus, increasing the value of R_{SL}, will decrease the amount of AC ringing current required to trigger the device. As such, longer sucribser loops are possible since less voltage is dropped per unit length of loop wire due to the lower current level. R_{SL} can also be used to compensated for smaller AC coupling capacitors (C_5 on Fig 3) (higher impedance) to the line which can be used to alter the ringer equivalence number of a tone ringer circuit.

The graph in Fig. 4 illustrates the variation of supply current with supply voltage of the KA2411. Three curves are drawn to show the variation of initiation current with R_{SL}. Curve B ($R_{SL} = 6.8K$) shows the I-V characteristic for the KA2411 tone ringer. Curve A is a plot with $R_{SL} < 6.8K\Omega$ and shows an increase in the current drawn up to the initiation voltage Vsi. The I-V characteristic after initiation remains unchanged. Curve C illurates the effect of increasing RSL above 6.8K Initiation current decreases but again current after triggering is unchanged.

APPLICATION CIRCUIT 2 (KA2411)

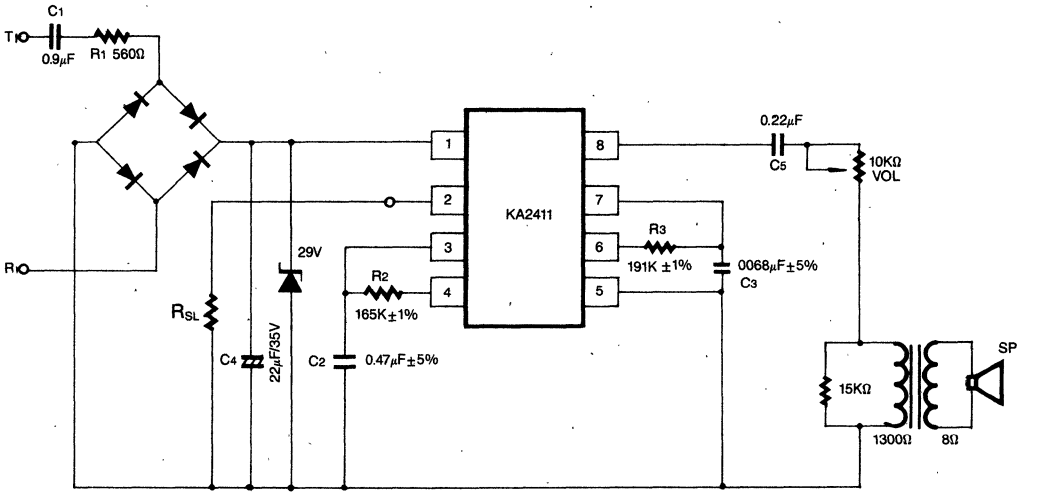


Fig. 3

LINEAR INTEGRATED CIRCUIT

KA2411 Supply Current (No Load) Vs. Supply Voltage

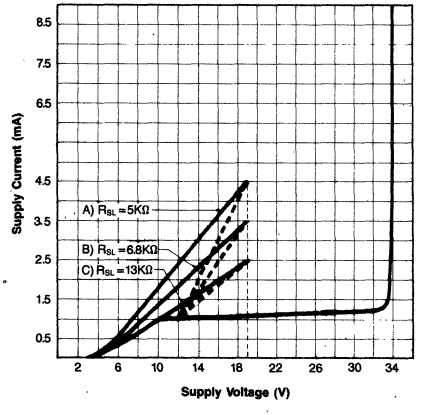


Fig. 4

EQUIVALENT CIRCUIT (Pin 2 Input)

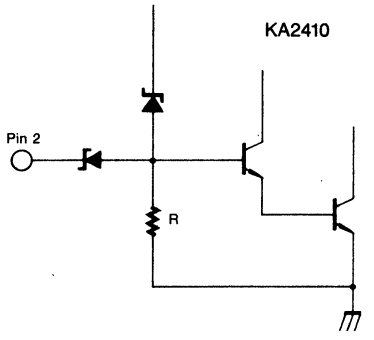


Fig. 5

INHIBITING OSCILLATION

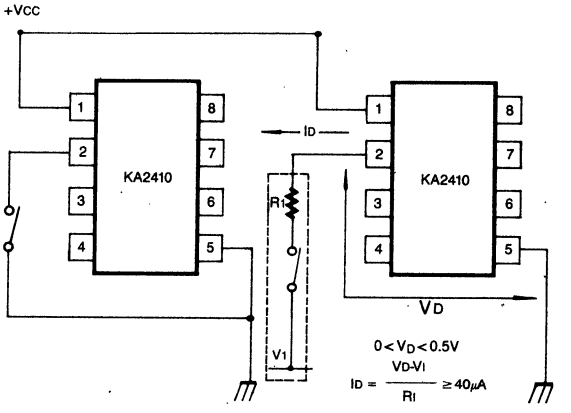


Fig. 6

PROGRAMMING THE KA2410 INITIATION SUPPLY VOLTAGE

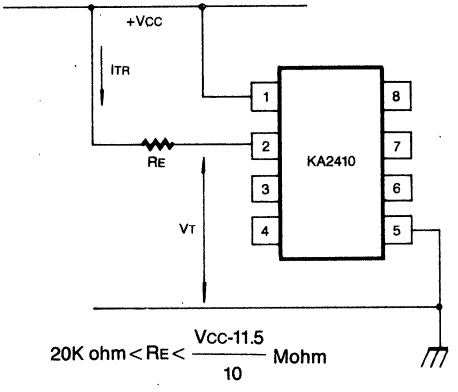


Fig. 7

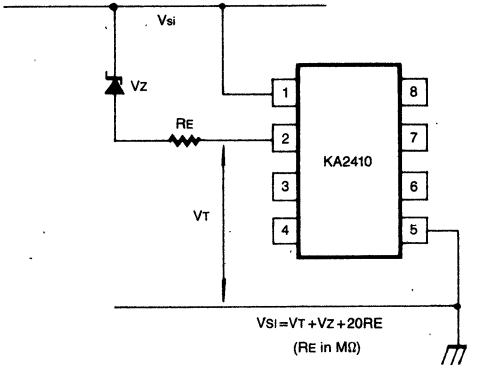


Fig. 8

TRIGGERING KA2410 FROM CMOS OR TTL LOGIC

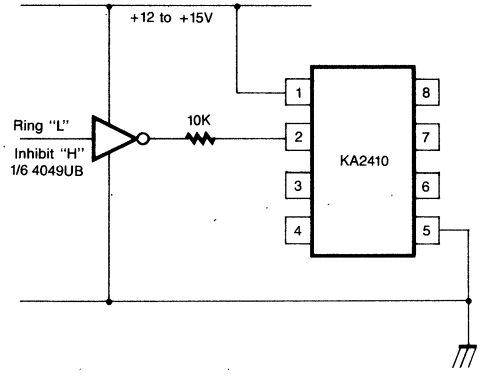


Fig. 9

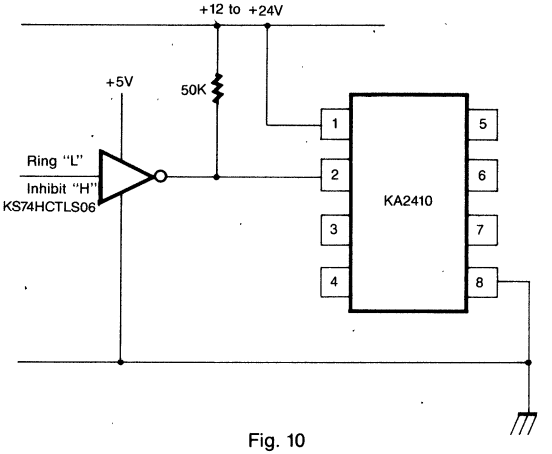
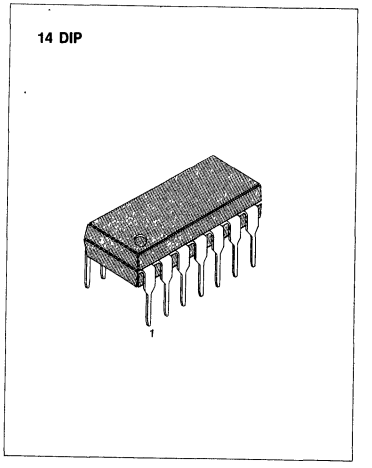


Fig. 10

TELEPHONE SPEECH CIRCUITS

The KA2412 A is designed for replacement of the hybrid circuit (2 ~ 4 wire interface) in conventional telephone.



FEATURES

- **Adjustable sending and receiving gain to compensate for line attenuation by sensing the line current.**
- **The same type of transducer can be used for both transmitter and receiver, usually a 350Ω dynamic type.**
- **Output impedance can be matched to the line, independent of transducer impedance.**
- **Minimum number of external parts required**
- **Parallel operation with pulse dialer IC (KS5805A/B, KS5806) as well as DTMF IC (KA2413, KS5808)**

3

BLOCK DIAGRAM

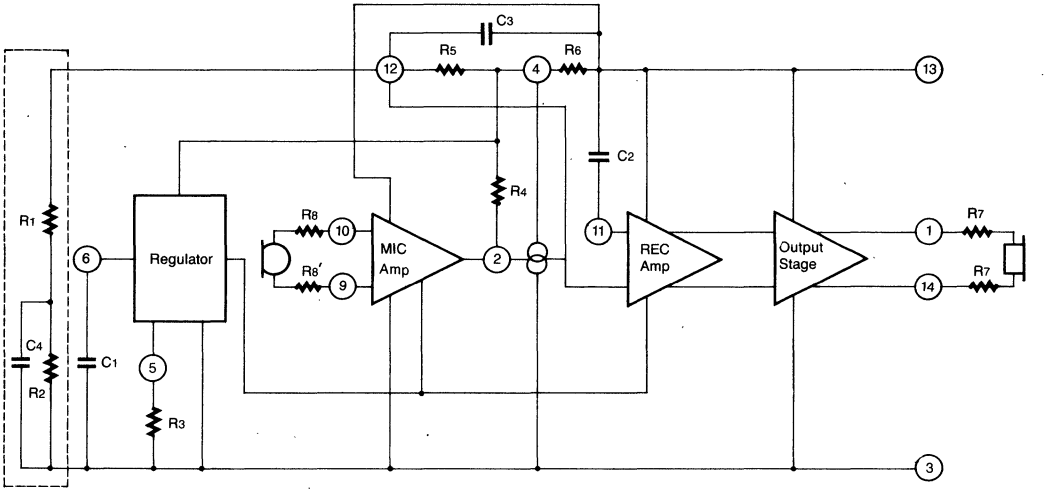


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (3 msec pulse duration)	V_L	22	V
Forword Line Current	I_{LF}	120	mA
Reverse Line Current	I_{LR}	−150	mA
Power Dissipation	P_D	1.0	W
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz unless otherwise specified. Refer to the test circuit.)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Line Voltage	V_L	Fig 2	I_L=80mA I_L=20mA I_L=10mA	10.0 5.0 3.8		11.5 5.8 4.6	V
Sending Gain	G_S	Fig 3	T_a=25°C, f=1KHz I_L=10mA I_L=20mA I_L=60mA I_L=80mA	 46.5 46.5 39.0 39.0		 50.5 50.5 43.0 43.0	dB
Sending Gain Variation vs temp	ΔG_{ST}	Fig 3	−15°C<Tamb<+45°C		±0.8		dB
Sending Gain Flatness	ΔG_{SF}	Fig 3	G_S=0dB at f=1KHz I_L=10 ~ 80mA			±0.5	dB
Sending Distortion	THD_S	Fig 3	I_L=20mA V_{SO}=1V_{P-P} I_L=80mA V_{SO}=400mVrms			2.0 2.0	% %
Sending Noise	V_{NS}		V_{MI}=0, I_L=60mA			130	μV
Maximum Sending Output	V_S (max)	Fig 3	I_L=10 V_{MI}=707mVrms			6.0	V_{P-P}
Receiving Gain	G_R	Fig 4	T_a=25°C, f=1KHz I_L=10mA I_L=20mA I_L=60mA I_L=80mA	 −12.6 −12.6 −19.9 −20.1		 −10.4 −10.6 −17.4 −17.4	dB
Receiving Gain variation vs temp	ΔG_{RT}	Fig 4	−15°C<Tamb<45°C		±0.8		dB
Receiving Gain Flatness	ΔG_{RF}	Fig 4	G_R=0dB at f=1KHz I_L=10 ~ 80mA			±0.5	dB

ELECTRICAL CHARACTERISTICS (Continued)

(T_a = −15°C ~ +45°C, f=300Hz ~ 3400Hz, unless otherwise specified refer to the test circuit)

Characteristic	Symbol	Test Circuit	Test Conditions	Min	Typ	Max	Unit
Receiving Distortion	THD_R	Fig 4	I_L =20mA ~ 80mA V_{RO} =200mVrms			2.0	%
Receiving Noise	V_{NR}	Fig 4	V_{RI} =OV, I_L =60mA Posphometric			75	μV
Max Receiving Output Current		I_{om}	I_L =10mA V_{RI} =707mVrms			2.0	mA
Side Tone	ST	Fig 5	f=1KHz, T_a =25°C I_L =20mA I_L =60mA		7.0 0.0		dB
Return Loss	R_L	Fig 6	S2 in a S2 in b		14 14		dB

PIN DESCRIPTION

1. PIN 1, PIN 14 : Recevier output
2. PIN 2 : Line impedance adjust
3. PIN 3 : Ground
4. PIN 4 : DC regulator
5. PIN 5 : Bias
6. PIN 6 : AC loop opening
7. PIN 7 : No connection
8. PIN 8 : No connection
9. PIN 9, PIN 10 : Mic input
10. PIN 11 : Input receive Amp (−)
11. PIN 12 : Input receive Amp (+)
12. PIN 13 : V_{CC}

TEST CIRCUIT

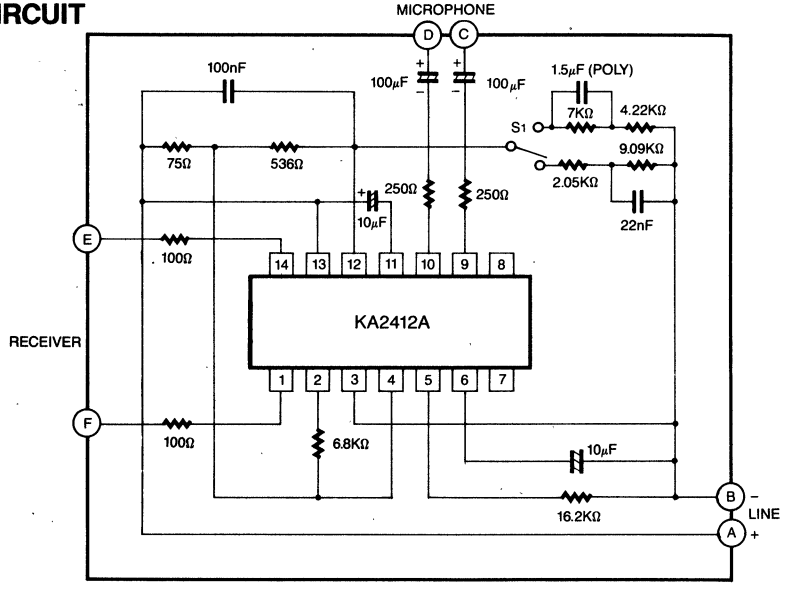


Fig. 2

Sending Gain

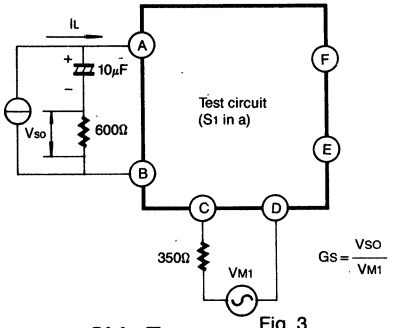


Fig. 3

Receiving Gain

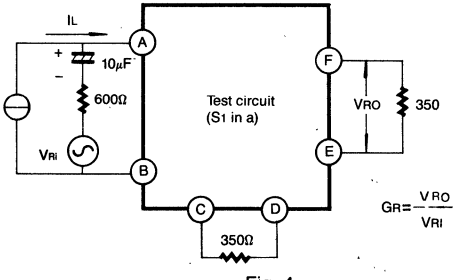


Fig. 4

Side Tone

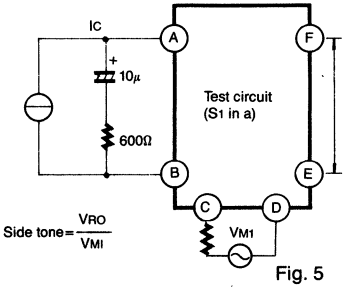


Fig. 5

Return Loss

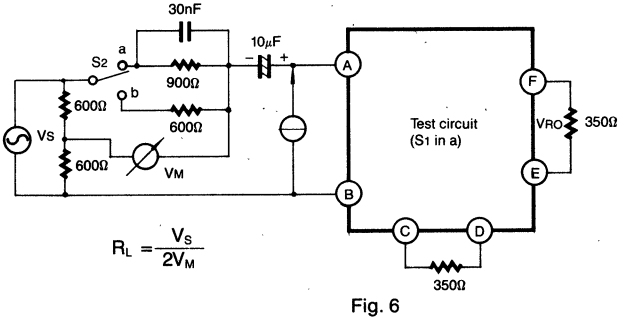


Fig. 6

APPLICATION INFOMRATION

The following table shows the recommended for the Fig 1. Different values can be used and notes are added in order to help designer.

Component	Recommended Value	Purpose	Note
R_1	2.05K	Balance network	In order to optimize the sidetone it is possible to change R_1 and R_2 values. In any case: $\frac{Z_B}{Z_L} = \frac{R_5}{R_6}$ where $Z_B = R_1 + R_2 // C_4$
R_2	9.09K		
R_3	16.2K	Bias resistor	Changing R_3 value, it is possible to shift the gain characteristics. The value can be chosen from 15K to 20K. The recommended value assures the maximum swing
R_5	536	Bridge resistors	The ratio R_5/R_6 fixes the amount of the signal delivered to the line.
R_6	75		
R_7, R_7'	100	Receiver impedance matching	R_7 and R_7' must be equal; 100Ω is a typical value for dynamic capsules
R_8, R_8'	250	Microphone impedance matching	R_8 and R_8' must be equal; 250Ω is a typical value for dynamic capsules. Furthermore, they determine a sending gain variation according to; $G_S = 20 \log \frac{R_X}{850}$ where $R_X = R_8 + R_8' + R_{MIC}$
C_1	10uF	AC loop opening	Ensures a high regulator impedance for AC signals (=20KΩ). This capacitor should not be higher than 10uF in order to have a short response time of the system.
C_2	1uF	DC decoupling for receiving input	
C_3	82nF	High frequency roll-off	C_3 determines the high frequency response of the circuit. It also acts as RF by pass.
C_4	22nF	Balance network	See note for R_1 and R_2

DESCRIPTION

1. Circuit Description:

The KA2412A is based on a bridge configuration. The KA2412A contains a regulator block, a sending amplifier and a receiving amplifier. The regulator monitors the line current and adjusts the amplifier gain to compensate for the line length.

The transmit/receiver amplifiers are connected to the line via an external bridge to provide side tone attenuation. When the subscriber is talking, A controlled amount of the sending signal is allowed to reach the receiver to give a feedback to the subscriber. The phenomenon is caused by mismatching of the wheastone bridge and is called the signal of side tone.

The line current compensation ensures that when the subscriber is talking, the signal delivered to the line is increased in according to the line length. When he is hearing, the signal level on the receiver capsule is constant.

Gain variation over the operating temperature range is less than ±1dB. The impedance to the line can be adjusted; without any change in circuit parameters; by changing an external resistor (6.8KΩ at Pin 2).

The KA2412A works with the same type of transducers for both transmitter and receiver (typically 350Ω Dynamic units).

2. Two to four wires conversion

1) In the case of the traditional telephone set:

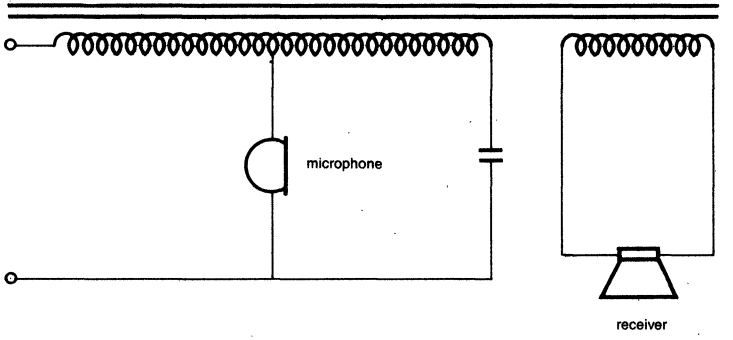


Fig. 10

A traditional speech circuit is equivalently equal to the circuit as described in Fig. 7. The microphone is composed of carbon powder. It converts the sound presure into the variation of resistance and so a AC signal is generated when the bias current flows through the microphone and a subscriber is talking. The current actuated by microphone does not affect receiver because it is compensated by the coil polarity.

But the incoming signal is transferred to receiver, so and this circuit is called 2 — 4 wires conversion, which is incoming 2 wires and Mic, Receivers 4 wires.

2) In the case of the KA2412 A

KA2412A performs the two wires (Telephone line) to four wires (Microphone, Receiver) conversion by means of a wheastone bridge configuration so obtaining the proper decoupling between sending and receiving signals (see Fig. 8)

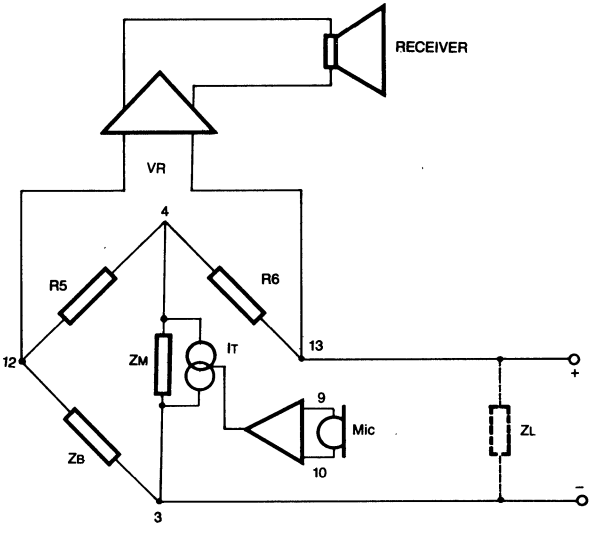


Fig. 8

For a perfect balancing of the bridge $\frac{Z_B}{Z_L} = \frac{R5}{R6}$

* In sending mode;

The AC signal from the microphone is sent to one diagonal of the bridge (pin 3 and pin 4). A small percentage of the signal power is lost on Z_B (being $Z_B >> Z_L$); the main part is sent to the line Via R6.

The impedance A_M is defined as $\frac{V_{4\text{-}3}}{I_{4\text{-}3}}$

$$V_R = \frac{(R6+Z_B)//(R5+Z_L)}{Z_M+(R6+Z_B)//(R5+Z_L)} \left(\frac{Z_L}{R6+Z_L} - \frac{Z_B}{R5+Z_B}\right) Z_M I_T$$

To reduce the receiving input signal,

$$\frac{Z_L}{R6+Z_L} = \frac{Z_B}{R5+Z_B} \rightarrow \frac{R6}{Z_L} = \frac{R5}{Z_B}$$

also, In order to reduce power loss in R5 & Z_B and to transfer the maximum power to the line via R6.

$R5+Z_B >> R6+Z_L$

$R6+Z_M = Z_L$

Then the line impedance Z_L grows from 600 ohm up to 900 ohm when the line length increases.
The voltage driven to the line is

$$V_L = \frac{Z_L}{R6+Z_M+Z_L} \times Z_{MIT}$$

In order to maximize sending Gain
$Z_L >> R6$

Therefore, in the case of the KA2412 test circuit:
R6=75, Z_M=6.8K/11, Z_L=600

$$V_L = \frac{Z_L}{Z_M+R6+Z_L} \times Z_M I_T = 286.82 I_T$$

* In receiving mode:
The AC signal coming from the line is sensed across the second diagonal of the wheastone bridge (pin 11 and pin 13). After amplification it is applied to the receiver.

$$V_R = \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} (R_6+R_5+Z_B)//Z_M \left(1-\frac{Z_B}{Z_B+R_5}\right)$$

$$= \frac{V_I}{Z_L+R_6+(R_5+Z_B)//Z_M} \left(R_6+\frac{Z_M R_5}{Z_M+R_5+R_6}\right)$$

To avoid the reflection
$Z_L = R_6+Z_M$, 10 $Z_M = R_5+Z_B$

Therefore

$$V_R = \frac{V_I}{2R_6+1.91 Z_M}\left(R_6+\frac{Z_B}{11}\right)$$

In the case of the KA2412A test circuit
Z_L=600Ω, R_6=75Ω, Z_M=6.8KΩ/11=6.8Ω
R_5=536Ω, Z_B=6.076KΩ (f_{REF}=1KHz)

$$\frac{V_R}{V_I} = 0.093$$

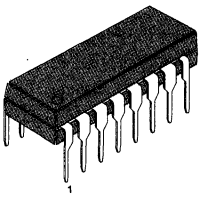
3. Automatic Gain Control.

The KA2412A automatically adjusts the gain of the sending and receiving amplifiers to compensate for line attenuation Maximum gain is reached for a line current of range 10 — 20mA and minimum gain can also be reached for a line current of range 60 — 100mA.

DUAL TONE MULTI FREQUENCY GENERATOR

The KA2413 is a monolithic integrated DTMF generator designed for use in a telephone set in parallel with an electronic speech circuit. The DC characteristic to the line is set by the speech circuit.

16 DIP



FEATURES

- **Wide operating line voltage and current range**
- **Operates with a standard crystal at 3.58MHz**
- **Operates with a single contact or matrix key-board**
- **Levels from the high and low frequency group can be adjusted separately.**
- **No individual level adjustment is necessary for every circuit**
- **The signal levels are stabilized against variations in temperature and line voltage.**
- **Short start-up time**
- **All tones can be generated separately for testing.**
- **Easy PCB layout; all keyboard connections on one side of the chip**
- **Internal protection of all inputs**
- **Minimum number of external parts required.**

BLOCK DIAGRAM

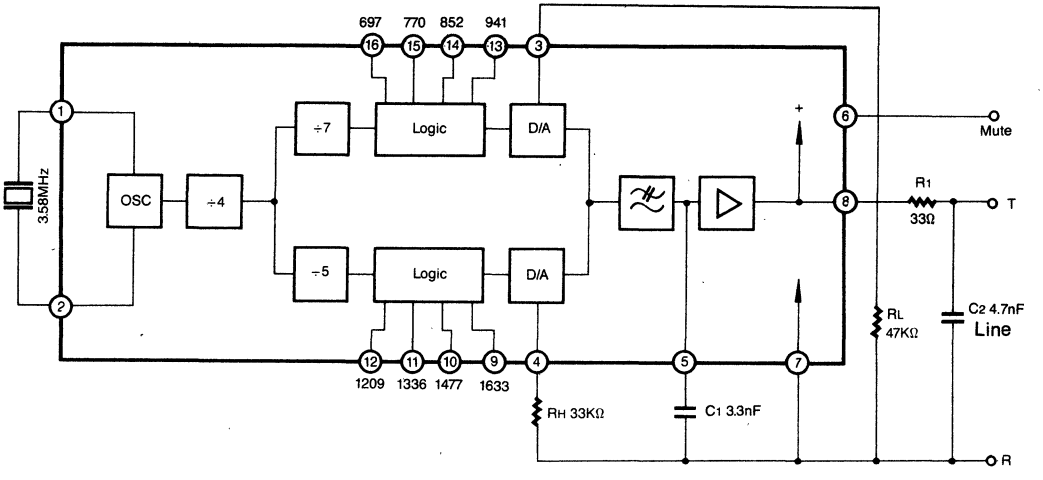


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Line Voltage (Peak) t_P =2 sec	V_L (peak)	20	V
Line Voltage (Peak) t_P =20m sec	V_L (peak)	22	V
Line Voltage (Conditions)	V_L (cont)	15	V
Power Dissipation	P_D	400	mW
Operating Temperature	Topr	−20 ~ +70	°C
Storage Temperature	Tstg	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

(V_L =4.3 ~ 9V, unless otherwise specified)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Line Voltage		V_L (opr)	Tone Generation 1.3 V_P Signal	4.3		9.0	V
Stand-By Line Voltage		V_L (std)	Stand-By 2.0 V_P Signal	4.3		9.0	V
Operating Line Current		I_L (opr)	V_L =4.3V			10.0	mA
Stand-By Line Current		I_L (std)	No Key Pressed V_L =4.3V			250	μA
Mute Current		I_M	One or More Keys Pressed	125.0			μA
Key Resistance		R_K	Key Circuit Closed			1.0	kΩ
Tone Output Frequency							
Low (Row)	f_1 = 697 Hz	Δf	f_{OSC} =3.5795 MHz	−1.0	−0.32	+1.0	%
	f_2 =770 Hz			−1.0	+0.02	+1.0	%
	f_3 =852 Hz			−1.0	+0.03	+1.0	%
	f_4 =941 Hz			−1.0	−0.11	+1.0	%
High (Column)	f_5 =1209 Hz			−1.0	−0.03	+1.0	%
	f_6 =1336 Hz			−1.0	−0.03	+1.0	%
	f_7 =1477 Hz			−1.0	−0.68	+1.0	%
	f_8 =1633 Hz			−1.0	−0.36	+1.0	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Signal level	High	V_H	R_H=46.4KΩ R_L=69.8KΩ		-9.0		dBm
	Low	V_L			-11.0		
	High	V_H	R_H=33.0KΩ R_L=47.0KΩ	-8.0	-6.0	-4.0	dBm
	Low	V_L		-10.0	-8.0	-6.0	
	High	V_H	R_H=26.1KΩ R_L=39.2KΩ		-4.0		dBm
	Low	V_L			-6.0		
Ratio Signal Level		V_H/V_L		1.0	2.0	3.0	dB
Impedance to Line		Z_L	Tone Generation Stand-By	6.0 50.0			KΩ
Total Harmonic Distortion		THD	Tone Generation			-31.0	dBm
Output Noise		V_{NO}	Stand-By			-80.0	dBm
Harmonics			300 — 3400Hz			-33.0	dBm
			3.4 — 50KHz			-33.0	dBm
			≥50KHz			-80.0	dBm
Start-up Time		t_S	Output level within 1dB from final level		3	5	mS

TEST CIRCUIT

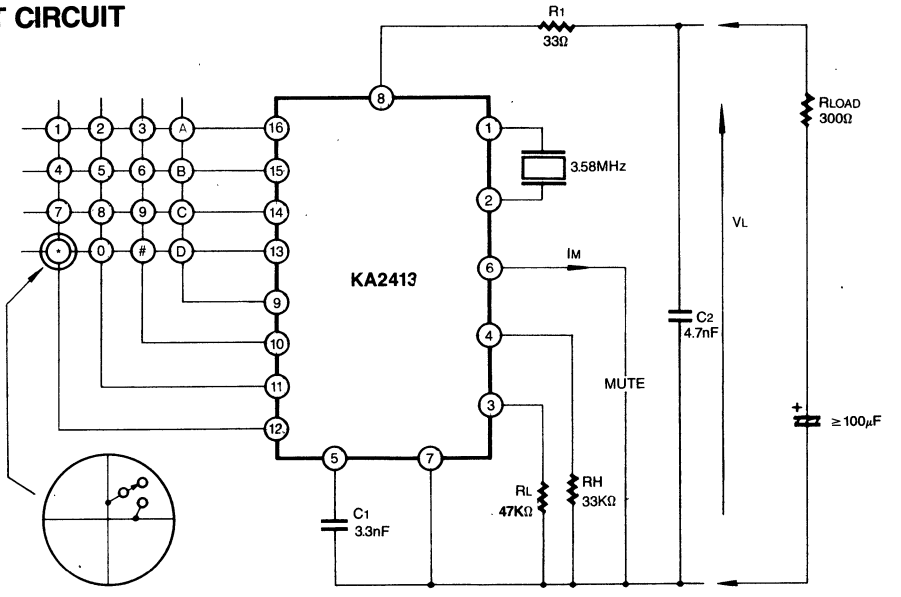


Fig. 2

- Component function:
  R1: Protecting resistor
  R_L: Signal Level (Low), R_H: Signal Level (High)
  C1: Low pass filter
  C2: Radio frequency suppression

- To find suitable resistor values for R_H and R_L to get the desired tone levels the following formula can be used for a preliminary calculation.
  Note that in R_{Load} (f=1.4KHZ) and R_{Load} (f=800HZ) both the impedance of the line and the impedance of the speech circuit are include. V_H and V_L are the desired high and low frequency levels, in dBm

$$R_H = 56.2 \times R_{LOAD}\ (f=1.4KHz) \times 10^{-\frac{V_H}{20}}$$

$$R_L = 65.2 \times R_{LOAD}\ (f=800Hz) \times 10^{-\frac{V_L}{20}}$$

- The current consumption within KA2413 can be reduced with a resistor connected in parallel with C1. (see Fig. 3)
  If the current reduction is made too large, the output signal can be distorted by clipping.

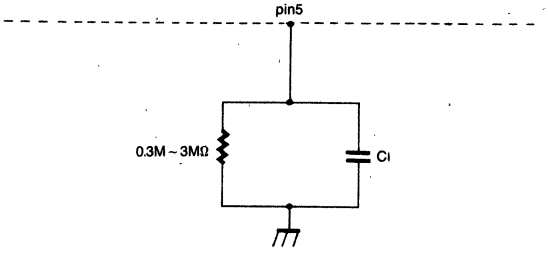


Fig. 3

- In application where a DTMF generator directly powered from the telephone line is wanted (the generator is not working in parallel with any kind of speech network), KA2413 can be used with a DC regulator as described in fig 4. This schematic gives a DC regulator for the range 16 — 100mA.

DC regulator schematic

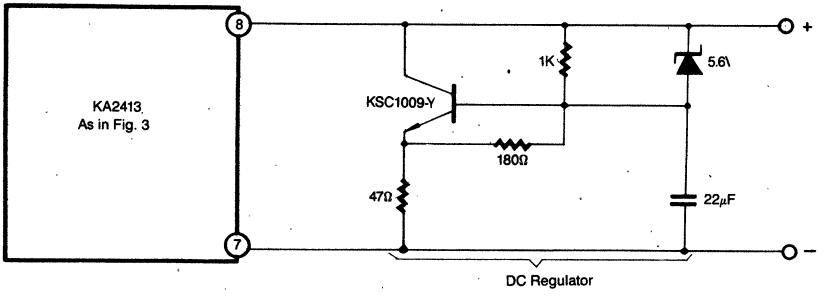


Fig. 4

- KA2413 can also be controlled by a microprocessor (see Fig 5). The negative branch of the microprocessor voltage supply is connected to pin 7 of KA2413 and the inputs (8) are connected with resistors.
  For tone-generating one input of the low group (pin 13 — 16) is connected to the positive voltage and one input of the high group (pin 9 — 12) is connected to the negative voltage, then KA2413 is activated and the mute output is put in High state.

Microcomputer interface

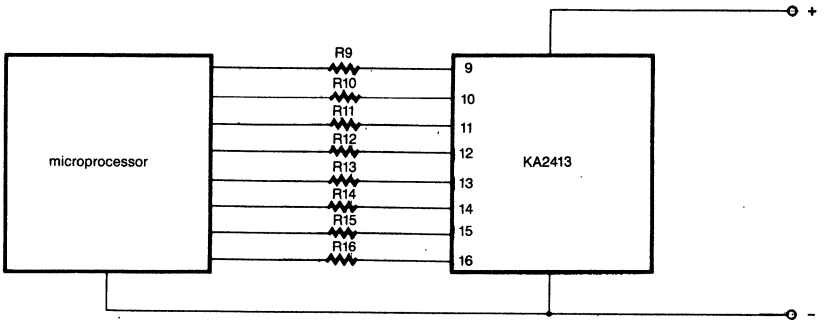


Fig. 5

1) R9, R10, R11, R12 (60K — 80K)
   The resistors have two functions are:
   — To raise the OFF/ON voltage
   — To limit the current when the input levels are high. Too high current will interfere with the functions of the other three inputs (the resistors can be exchanged with diodes directly away from KA2413)

High-frequency group resistors to microcomputer

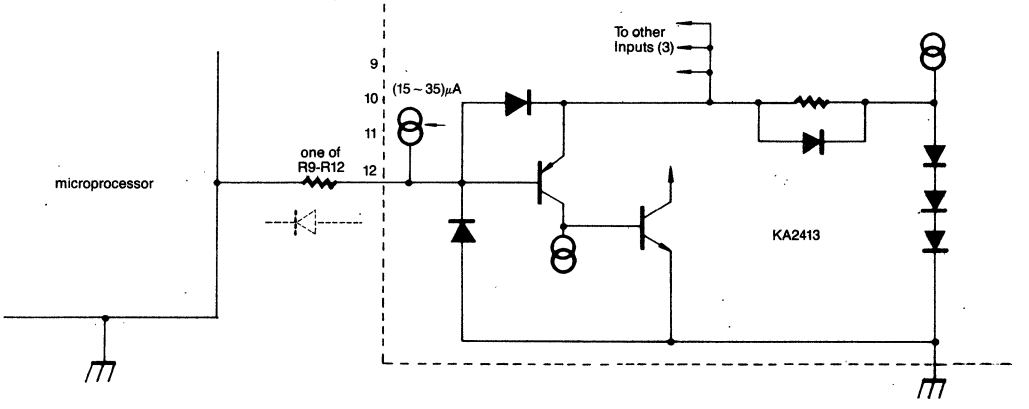


Fig. 6

2) R13, R14, R15, R16 (20K — 30K)
The two functions of the resistors are:
— To raise the OFF/ON voltage
— To limit the current when the input levels are high.

Low-frequency group resistors for microcomputer

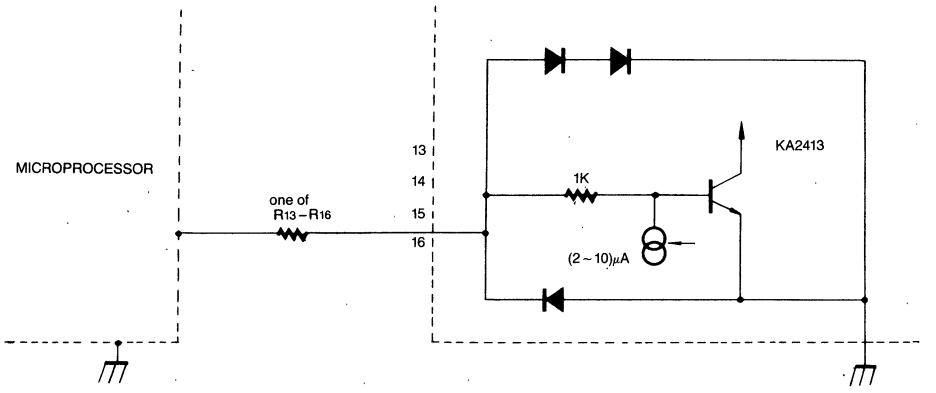
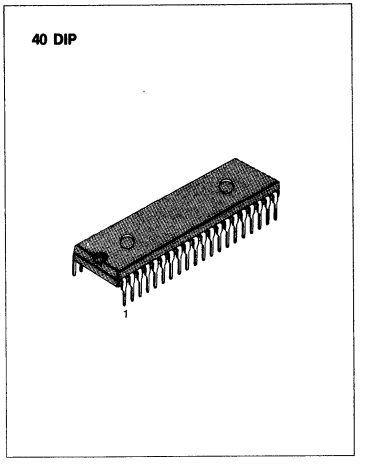


Fig. 7

ONE CHIP TELEPHONE

The KA2414/KA2417 electronic telephone circuits (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and DC line interface circuit (Fig. 1). The KA2417 also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltage below 2.5 volts. DTMF dialers operate at similary low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the KA2414/KA2417 in a bipolar/I²L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.



3

FEATURES

- **Provides all basic telephone station apparatus functions in a single IC, including DTMF dialer, tone ringer, speech network and line voltage regulator.**
- **DTMF generator uses Low-Cost ceramic resonator with accurate frequency synthesis technique.**
- **Tone ringer drives piezoelectric transducer and satisfies EIA RS-470 impedance signature requirements.**
- **Speech network provides two-four wire conversion with adjustable sidetone utilizing an electret transmitter.**
- **On-chip regulator insures stable operation over wide range of loop lengths.**
- **I²L technology provides low 1.4 volt operation and high static discharge immunity.**
- **KA2417 provides microprocessor interface port for automatic dialing features.**

BLOCK DIAGRAM

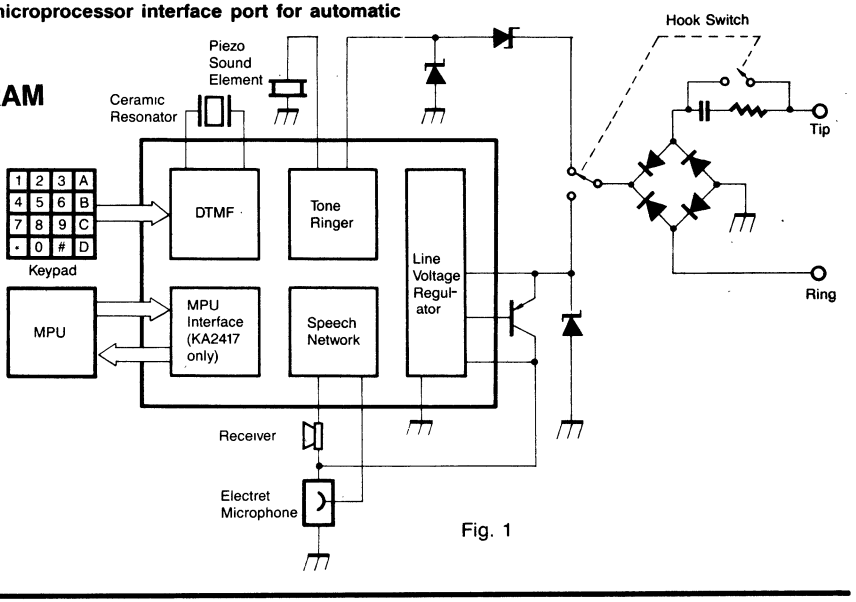


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
V^+ Terminal Voltage (Pin 34)	V_{CC}	−1.0 ~ +18	V
VR Terminal Voltage (Pin 29)	VR	−1.0 ~ +2.0	V
RXO Terminal Voltage (Pin 27)	RXO	−1.0 ~ +2.0	V
TRS Terminal Voltage (Pin 37)	TRS	−1.0 ~ +35	V
TRO (with Tone Ringer Inactive Terminal Voltage)	TRO	−1.0 ~ +2.0	V
R_1-R_4 Terminal Current (Pins 1-4)	I_R	±100	mA
C_1-C_4 Terminal Current (Pins 5-8)	I_C	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+ (KA2417 Only)		−1.0 ~ +12	V
Operating Ambient Temperature Range	T_{opr}	−20 ~ +60	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a =25°C, V_{CC} =5V Unless Otherwise Specified)

KEYPAD INTERFACE CIRCUIT

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m=1, 2, 3, 4	R_{RM}		5.0	8.0	11	KΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n=1, 2, 3, 4	R_{CN}	V_I =1.0V	5.0	8.0	11	KΩ
Ratio of Row-to-Column Input Resistance $K_{MN}=\frac{R_{RM}\ m=1,2,3,4}{R_{CN}\ n=1,2,3,4}$	$K_{M.N}$		0.88	1.0	1.12	KΩ
Row Terminal Open Circuit Voltage	V_{ROC}		950	1100	1200	mV_{DC}
Row Threshold Voltage for m^{th} Row Terminal: m=1, 2, 3, 4	V_{RM}	Decrease from V_I =1.0V to $0.7V_{ROC}$	$0.7V_{ROC}$	—	—	V
Column Threshold Voltage for n^{th} Column Terminal: n=1, 2, 3, 4	V_{CN}	Increase from V_I =0V to $0.39V_{ROC}$	—	—	$0.39V_{ROC}$	V

*V_I: Input voltage of key board pins.

ELECTRICAL CHARACTERISTICS (Continued)

MICROPROCESSOR INTERFACE (KA2417 only)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Regulator Output A+ Rgulator	V_R/A+	V_{CC}=0.6V A+=2.4V	0.95	1.1	1.3	V
A+ Input Current Off-Hook	I_A (Off)	V_{CC}=1.4V, A+=5V		50	150	μA
A+ Input Current On-Hook	I_A (On)	V_{CC}=0.6V, A+=5V	4.0	6.0	9.0	mA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	R_{IN}	A+=5V	50	100	150	KΩ
Input Current (I/O)	I_{IN}	A+=5V, $V_{I/O}$=0.8V, V_{DD}=2V		80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	V_{IH}		2.0		A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	V_{IL}				0.8	V
Output High Voltage (MS, DP, I/O)	V_{OH}	A+=5V	2.4	4.0		V
Output Low Voltage (MS, DP, I/O)	V_{OL}	A+=5V		0.1	0.4	V

LINE VOLTAGE REGULATOR

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Regulator Output	V_R	V_{CC}=1.7V	1.0	1.1	1.2	V
V+ Current in DTMF Mode	I_{DT}	V_{CC}=11.5V,R+=600Ω	8.0	12	14.5	mA
Change in I_{DT} with Change in V+ Voltage	ΔI_{DT}	V_{CC}=11.5~26V, R+=60Ω		0.8	2.0	mA
V+ Current in Speech Mode V+=1.7V V+=5.0V	I_{SP}		 3.5 8.0	 5.0 11	 7.0 15	 mA mA
Speech to DTMF Mode Current Difference	ΔI_{TR}	V+=11.5V R+=600Ω	−2.0	2.0	3.5	mA
LR Level Shift V+=5.0V, I_{LR}=10mA V+=18V, I_{LR}=110mA	ΔV_{LR}		 2.4 2.6	 2.9 3.3	 3.5 4.0	 V V
LC Terminal Resistance	R_{LC}		30	50	75	KΩ
Load Regulation	ΔV_R	V+=1.7v I_{BP}=0~150μA	−20	−6.0	20	mV_{AC}

ELECTRICAL CHARACTERISTICS (Continued)

SPEECH NETWORK

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	V_{MIC}	$I_{MIC}=500\mu A$, $V_{MM}=0.8V$	—	60	125	mV_{DC}
MIC Terminal Leakage Current	I_{MIC}	$V_{MM}=2V$, $V_{MIC}=1V$	—	0.0	5.0	μA
MM Terminal Input Resistance	R_{MM}	$V_{MM}=5V$	50	100	170	KΩ
TXO Terminal Bias	B_{TXO}	$B_{TXO}=V_{TXO}\div V_R$	0.48	0.53	0.68	—
TXI Terminal Input Bias Current	I_{TXI}	$I_{TXI}=(V_{TXO}-V_{TXI})\div 200K\Omega$	—	50	400	nA
TXO Terminal Positive Swing	$V_{TXO}(+)$	$I_{TXI}=-10\mu A$	—	25	60	mV_{DC}
TXO Terminal Negative Swing	$V_{TXO}(-)$	$I_{TXI}=10\mu A$		130	200	mV_{DC}
Transmit Amplifier Closed-Loop Gain	G_{TX}	$V_I=3.0mV_{RMS}$	16.5	19	20	V/V
Sidetone Amplifier Gain	G_{STA}	f=1.0KHz	0.40	0.45	0.54	V/V
STA Terminal Output Current	I_{STA}	$V_{STA}=0.3V$	50	100	250	μA
RXO Terminal Bias	B_{RXO}	$B_{RXO}=V_{RXO}\div V_R$	0.48	0.52	0.68	—
RXI Terminal Input Bias Current	I_{RXI}	$I_{RXI}=(V_{RXO}-V_{RXI})\div 100K\Omega$	—	100	400	nA
RXO Terminal Positive Swing	$V_{RXO}(+)$	$I_{RXI}=-10\mu A$ $V_{RXO}(+)=V_R-V_{RXO}$	—	1.0	20	mV_{DC}
RXO Terminal Negative Swing	$V_{RXO}(-)$	$I_{RXI}=+10\mu A$ $V_{RXO}(-)=V_{RXO}$	—	40	100	mV_{DC}
TXL Terminal Off Resistance	R_{TXL} (Off)	$V_{TXL}=0.4V_{DC}$	125	200	300	KΩ
TXL Terminal On Resistance	R_{TXL} (On)		—	20	100	Ω
RM Terminal Off Resistance	R_{RM} (Off)	$V_{RM}=0.4V_{DC}$	125	180	300	KΩ
RM Terminal On Resistance	R_{RM} (On)		410	570	770	Ω

DTMF GENERATOR (V+=15V, R+=600Ω)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Row Tone Frequency Row 1	f_{R1}		692.9	696.4	699.9	Hz
Row 2	f_{R2}	V+=15V	765.3	769.2	773.0	Hz
Row 3	f_{R3}	R+=600Ω	848.9	853.2	857.5	Hz
Row 4	f_{R4}		935.1	939.8	944.5	Hz
Column Tone Frequency Column 1	f_{C1}		1201.6	1207.7	1213.7	Hz
Column 2	f_{C2}	V+=15V	1330.2	1336.9	1343.6	Hz
Column 3	f_{C3}	R+=600Ω	1471.9	1479.3	1486.7	Hz
Column 4	f_{C4}		1625.2	1633.4	1641.5	Hz
Row Tone Amplitude	V_{ROW}	V+=15V, R+=600Ω	0.38	0.45	0.55	V_{RMS}
Column Tone Amplitude	V_{CO1}	V+=15V, R+=600Ω	0.48	0.55	0.67	V_{RMS}
Column Tone Pre-emphasis	dB_{CR}	V+=15V, R+=600Ω	0.5	1.8	3.0	dB
DTMF Distortion	THD		—	4.0	6.0	%
DTMF Output Resistance	R_O	$V_{FB}=1.8\sim 2.8V$	1.0	2.5	3.0	KΩ

ELECTRICAL CHARACTERISTCS (Continued)

TONE RINGER (V_{TRI}=20V)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
TRI Terminal Voltage	V_{TRI}	$I_{TRC}+I_{TRS}$=1.0mA	20	21.5	23	V_{DC}
TRS Terminal Input Current V_{TRS}=24V V_{TRS}=30V	I_{TRS}	V_{TRI}=20V	 70 0.4	 120 0.8	 170 1.5	 μA mA
TRF Threshold Voltage	V_{TRF}	V_{TRI}=20V	1.2	1.6	1.9	V_{DC}
TRF Threshold Hysteresis	ΔV_{TRF}	V_{TRI}=20V	100	200	400	mV_{DC}
TRF Filter Resistance	R_{TRF}	V_{TRF}=21V, R_{TRF}=1.0÷I_{TRA}	30	50	75	KΩ
High Tone Frequency Low Tone Frequency Warble Frequency	f_H f_L f_W		920 736 11.5	1000 800 12.5	1080 864 13.5	Hz Hz Hz
Tone Ringer Output Voltage	V_O (p-p)	V_{TRS}=22V, V_{TRI}=20V	18	20	22	V_{P-P}

TEST CIRCUIT

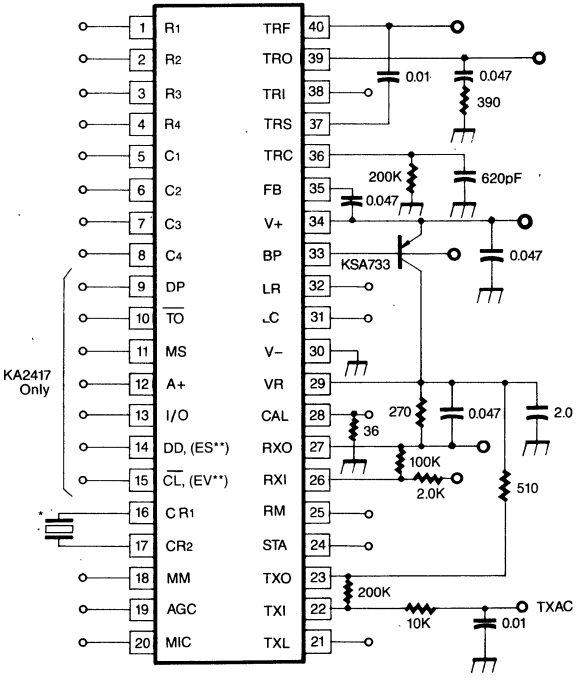


Fig. 2

Notes:
1. *Selected ceramic resonator: 500KHz±2.0KHz
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. **KA2414 only

PIN DESCRIPTION

(See Fig. 12 for external component identifications.)

Pin	Designation	Function
1-4	R1-R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0kΩ resistors pull up the row inputs to a regulated (≈1.1 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<500mV) from a microprocessor port.
5-8	C1-C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0kΩ resistors pull down the column inputs to V–. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>600mV and <3.0 volt).
9	DP*	Depressed Pushbutton (Output) — Normally low: A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
10	$\overline{TO}$*	$\overline{Tone\ Output}$ (Input) — When a Logic "1", disables the DTMF generator. Keypad is not disabled.
11	MS*	Mute/Single tone (Output) — A Logic "1" indicates a row and/or column tone is being generated. A Logic "0" indicates tone generator is disabled.
12	A+*	MPU Power Supply (input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except tone Ringer) in the absence of voltage at V–.
13	I/O*	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD=Logic "0".
14	DD*	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1", I/O is an input to the DTMF generator. As a Logic "0". I/O outputs keypad entires to the microprocessor.
	ES**	Sidetone Equalization terminal connects an external resistor between the junction of R8, R9 and V–, At loop currents greater than the equalization threshold this resistor is switched in to reduce the sidetone level.
15	$\overline{CL}$*	$\overline{Clock}$ (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20kHz.
	EV**	Voice equalization terminal connects an external resistor between V+ and V–, for loop length equalization. At loop currents greater than the equalization threshold this resistor is switched in by the equalization circuit to reduce the transmit and receive gains.
16, 17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500kHz ceramic resonator from which row and column tones are synthesized.
28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V — controls the DTMF output signal level at Tip and Ring.
35	FB	Feed Back terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transitor. At line voltages which maintain VR above. 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.

*KA2417 only **KA2414 only

PIN DESCRIPTION (Continued)

(See Fig. 12 for external component identifications.)

Pin	Designation	Function
34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
32	LR	DC Load Resistor, Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
20	MIC	Microphone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.
18	MM	Microphone Mute. The MM pin provides a means to mute the microphone and transmit amplifier in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0V) the microphone dc return path through the MIC terminal is disabled.
22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6V above V− by feedback through resistor R11 from TXO.
21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc curent flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12+R13) ratio.
19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+, RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540Ω in the mute mode and 200kΩ otherwide. Coupling capacitors C7 and C8 prevent dc current flow through RM.

* KA2417 only

(continued)

PIN DESCRIPTION (Continued)

(See Fig. 12 for external component identifications.)

Pin	Designation	Function
24	STA	Side Tone Amplifier output STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
40	TRF	Tone Ringer Input filter capacitor terminal. Capacitor C1 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C1 to 1.6 volts.
36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\mu s)^{-1}$.
39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.

GENERAL CIRCUIT DESCRIPTION

LINE VOLTAGE REGULATOR

The DC line interface circuit (Fig 3) determines the DC input characteristic of the telephone. At low input voltage (less than 3 Volts) the ETC draws only the speech and dialer bias currents through the VR regulator. As input voltage increase, Q_1 conducts the excess DC line current through resistor R_4. The 1.5 Volt level shift prevents saturation of Q_2 with telephone line signals up to 2.0 Volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the DC voltage/current characteristic of a KA2414/KA2417.

DC LINE INTERFACE BLOCK DIAGRAM

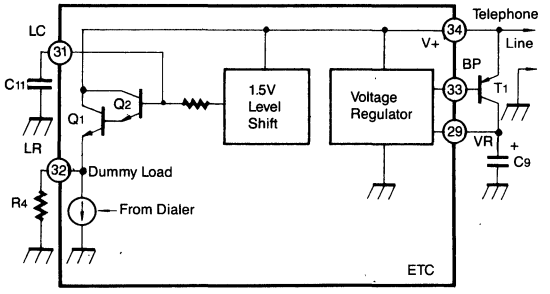


Fig. 3

DC V-I CHARACTERISTIC OF ETC

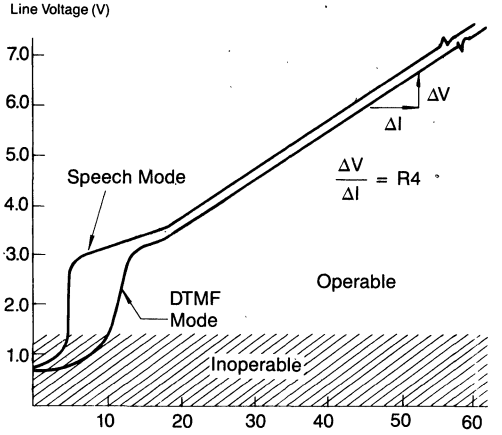


Fig. 4

SPEECH NETWORK

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched AC resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) in the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}: 2) The AC impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

SPEECH NETWORK BLOCK DIAGRAM

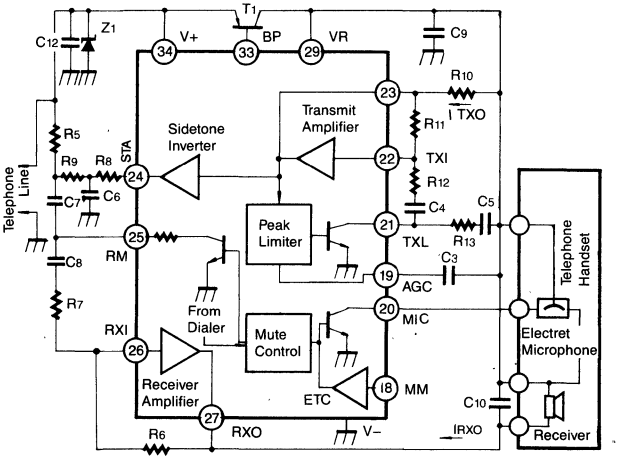


Fig. 5

EQUALIZATION CIRCUIT (KA2414 ONLY)

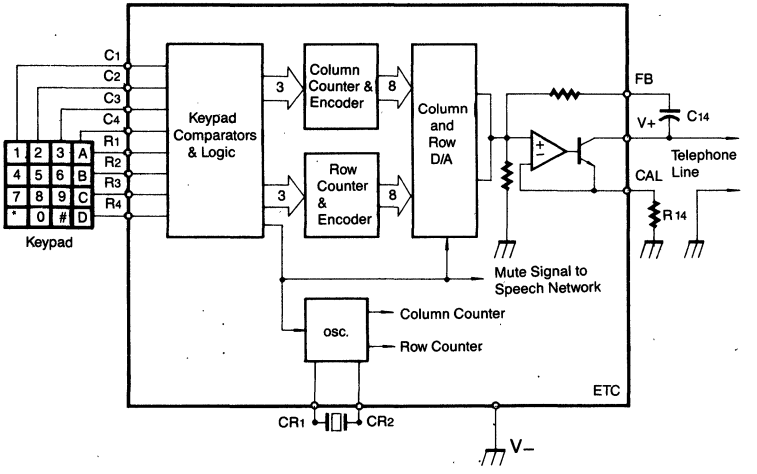
The equalization circuit varies the transmit, receive and sidetone gains with loop current to compensate for losses in long lines. The LR terminal voltage varies directly as the dc loop current. The equalization circuit senses this voltage and switches in external resistors between V+ and V− and across capacitor C6 (Figure 5) when the loop current exceeds a threshold level. The speech network operates with full transmit, receive and sidetone gains for long loops. On short loops the LR voltage exceeds the threshold and these gains are reduced. The threshold detection circuit has a dc hysteresis to prevent distortion of speech signals when the telephone is operated at the threshold current.

DTMF DIALER

Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step. approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

DTMF DIALER BLOCK DIAGRAM



TONE RINGER

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the AC line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced between the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_o/8$ and $f_o/10$ at a warble rate of $f_o/640$, where f_o is the ringer oscillator frequency.

TONE RINGER BLOCK DIAGRAM

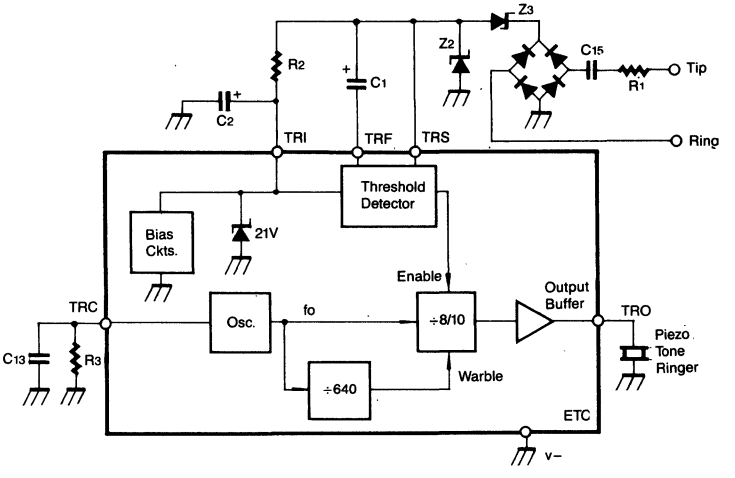


Fig. 7

MICROPROCESSOR INTERFACE (KA2417 ONLY)

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 9). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the microprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logie "0" to enable the DTMF generator. Figures 10 and 11 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to the microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

MICROPROCESSOR INTERFACE BLOCK DIAGRAM (KA2417 ONLY)

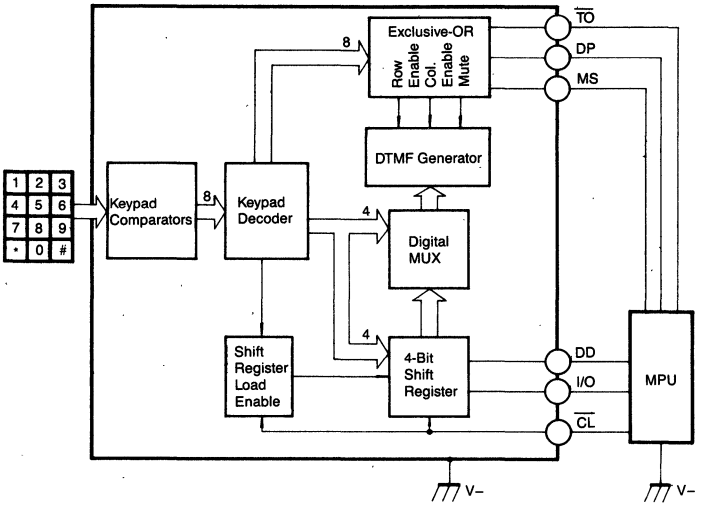
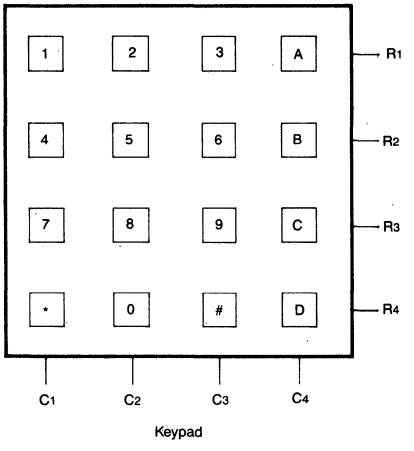


Fig. 8

MPU INTERFACE CODES



Key	Row	Column	Code (B3 ~ B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

Fig. 9

OUTPUT DATA CYCLE FROM KA2417

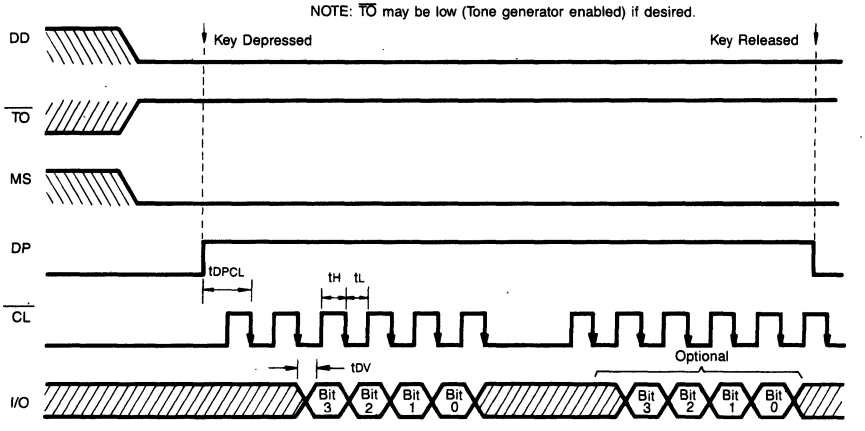


Fig. 10

INPUT DATA CYCLE TO KA2417

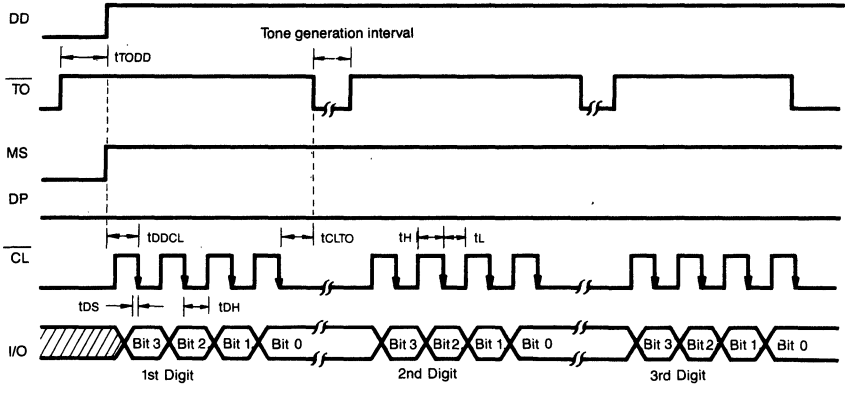


Fig. 11

TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500KHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15			μs	Figs. 10, 11
t_L	Clock Low Time	15			μs	Figs. 10, 11
t_r, t_f	Clock, Rise, Fall Time			2.0	μs	
t_{DV}	Clock Transition to Data Valid			10	μs	Fig. 10
t_{DPCL}	Time from DP High to $\overline{CL}$ Low	20			μs	Fig. 10
t_{DDCL}	Time from DD High to $\overline{CL}$ Low	20			μs	Fig. 11
t_{DS}	Data Set-up Time	10			μs	Fig. 11
t_{DH}	Data Hold Time	10			μs	Fig. 11
t_{CLTO}	Time from $\overline{CL}$ Low to $\overline{TO}$ Low	10			μs	Fig. 11
t_{TODD}	Time from $\overline{TO}$ High to DD High	20			μs	Fig. 11

APPLICATIONS INFORMATION

Fig 12 specifies a typical application circuit for the KA2414 and KA2417.

Complete listing of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration in Fig. 12 is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance.

R1, C15, and Z3 are significant components for on-hook impedance. C15 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5V and 10V impedance signature tests. C15 must generally be $\leq 1.0\mu F$ to satisfy 5.0Hz impedance specifications. (EIA RS-470)

Tone Ringer Output Frequencies

R3 and C13 control the frequency (fo) of a relaxation oscillator.

Typically $fo = (R3\ C13 + 8.0\mu S)^{-1}$. The output tone frequencies are fo/10 and fo/8. The warble rate is fo/640. The tone ringer will operate with fo from 1.0KHz to 10KHz. R3 should be limited to values between 150K and 300K.

Tone Ringer Input Threshold

After R1, C15, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold.

Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8K and 2.0KΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10mA. R4 should be selected between 30Ω and 120Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone.

Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of row and column tone amplitudes is internally fixed. R14 should be greater than 20Ωto avoid excessive current in the DTMF output Amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Microprocessor Interface (KA2417 Only)

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Figure 13. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The KA2417 clock speed requirement is slow enough (typically 20kHz) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a Logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at Pin 12 (A+) may be disconnected to conserve power. Normally the speech circuitry is powered by the voltage supplied at the V+ terminal (Pin 34) from the telephone lines. During this time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook," and V+ falls below 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a micrpprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook."

Equalization of Speech Network (KA2414 Only)

Resistors R17 and R18 are switched into the circuit when the voltage at the LR terminal exceeds the equalization threshold voltage (typically 1.65V). R17 reduces the transmit and receive gains for loop currents greater than the threshold (short loops) by attenuating signals at tip and ring. R18 reduces the sidetone level which would otherwise increase when R17 is switched into the circuit. The voltage V_{LR} at LR terminal is given by

$V_{LR} = (I_L - I_S) \times R4$.

where I_L = loop current

I_S = dummy load current (6.0 mA) + speech network current (4.0 mA).

Thus resistor R4 is selected to activate the equalization circuit at the desired loop current. However, R4 must be selected keeping in mind the fact that it also controls the dc resistance of the telephone. Capacitors C18 and C19 prevent dc current flow into the EV and ES terminals. This reduces clicks and also prevents changes in the dc characteristic of the telephone when the EV and ES terminals are switched to low impedance.

APPLICATION CIRCUIT 1

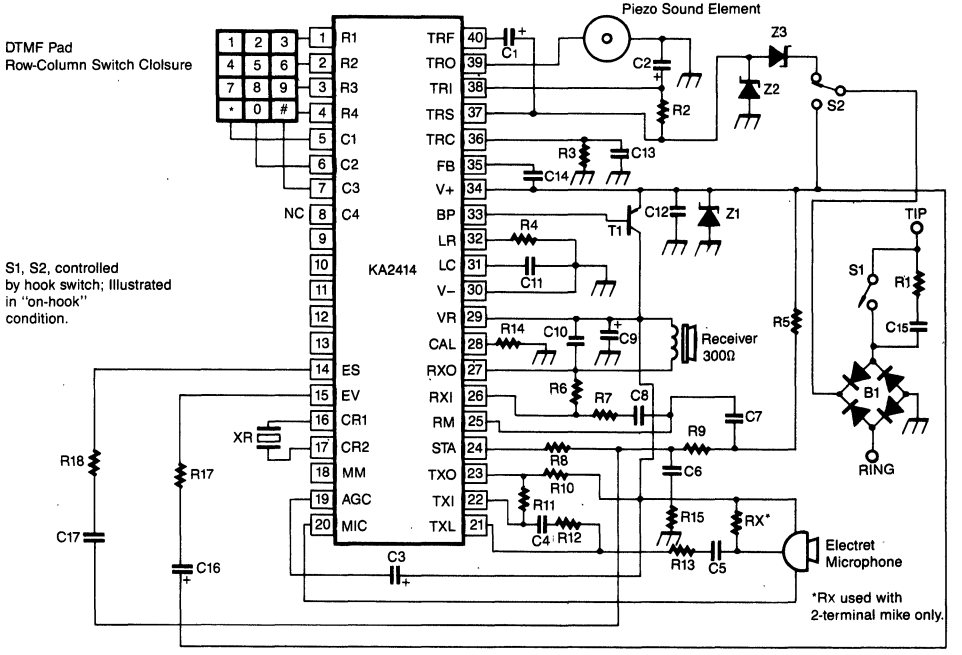


Fig. 12

APPLICATION CIRCUIT 2

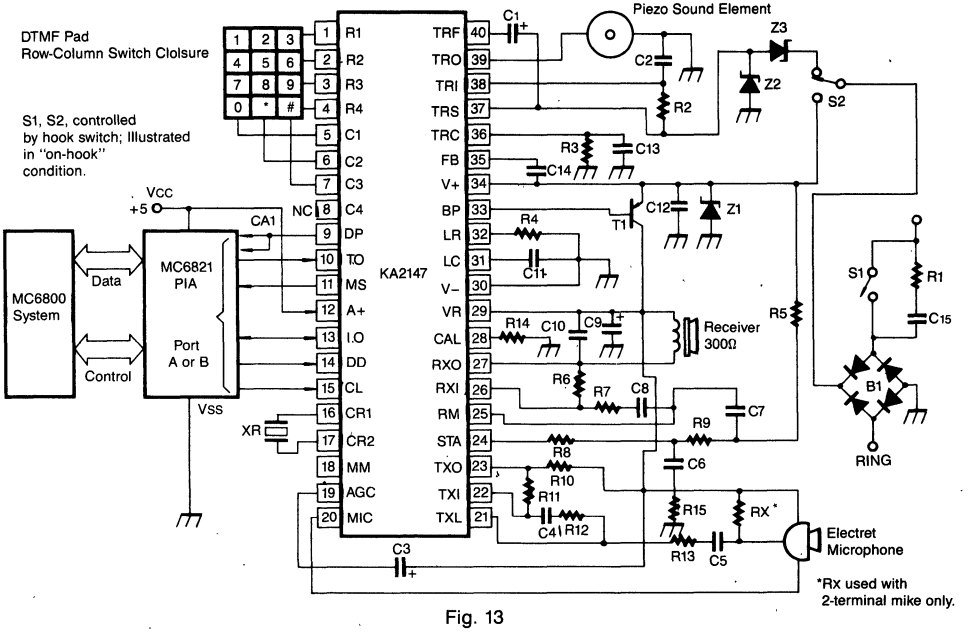


Fig. 13

EXTERNAL COMPONENTS

(Component labels referenced to Fig. 12, Fig. 13)

Capacitors	Nominal Value	Description
C1	1.0μF, 10V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C2	4.7μF, 25V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C3	1.0μF, 3.0V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuates low-frequency noise on microphone lead.
C6	0.05μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05μF	Receiver amplifier input capacitors: prevent dc current flow into FM terminal and attneuates low frequency noise on the telephone line.
C9	2.2μF, 3.0V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01μF	Telephone line by pass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1μF	DTMF output feed back capacitor: ac couples feed back around the DTMF output amplifier which reduces output impedance.
C15	1.0μF, 250Vac Non-Polarized	tone ringer line capacitor; ac couples the tone ringer to the telephone line partially controls the on-hook input impedance of telephone.
C16	25pF, 25V	Speech equalization coupling capacitor, prevents dc current flow into SPE terminal (optional)
C17	5.0μF, 3.0V	Side tone equalization coupling capacitor, prevents dc currents flow into STE terminal (optional)

EXTERNAL COMPONENTS (Continued)

(Component labels referenced to Fig. 12)

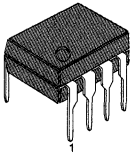
Resistors	Nominal Value	Description
R1	6.8K	Tone ringer input resistor: limits current into the tone ringe from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8K	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200K	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150K, 56K	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200K	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5K, 30K	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200K	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7K, 4.7K	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0K	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R17	600	Speech equalization resistor. Reduces transmit and receive gain when EV terminal switches on (optional)
R18	3.0K	Sidetone equalization resistor. Reduces sidetone level when ES terminal switches on. (optional)
R_X	3.0K	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; RX is not used with 3-terminal microphones.

Semiconductors	Electret Mic	Receiver
B1= MDA101A, or equivalent, or 4-IN4005 T1=KSA733 or equivalent Z1=18V, 1.5W, IN5931A Z2=30V, 1.5W, IN5936A Z3=4.7V, 1/2W, IN750 XR — Murata Erie CSB 500KHz Resonator or equivalent Piezo — PBL5030BC TOKO Buzzer or equivalent	2 Terminal, Primo EM-95 (use Rx) or equivalent 3 Terminal, Primo O7A 181P (Remove Rx) or equivalent	Prime Model DH-34 (300Ω) or equivalent

TONE RINGER WITH BRIDGE DIODE

The KA2418 is a monolithic integrated circuit designed to replace the mechanical bell in telephone sets, in connection with an electro acoustical converter. The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variation of the ringing signal cannot affect correct operation of the device.

8 DIP



FUNCTIONS

- Two oscillators
- Output amplifier
- Power supply control circuit.

FEATURES

- **Low current consumption, in order to allow the parallel operation of 4 devices.**
- **On-chip diode bridge and transient protection**
- **Little external circuitry**
- **Tone and switching frequencies adjustable by external components**
- **Integrated voltage and current hysteresis**
- **Activation voltage adjustable**

BLOCK DIAGRAM

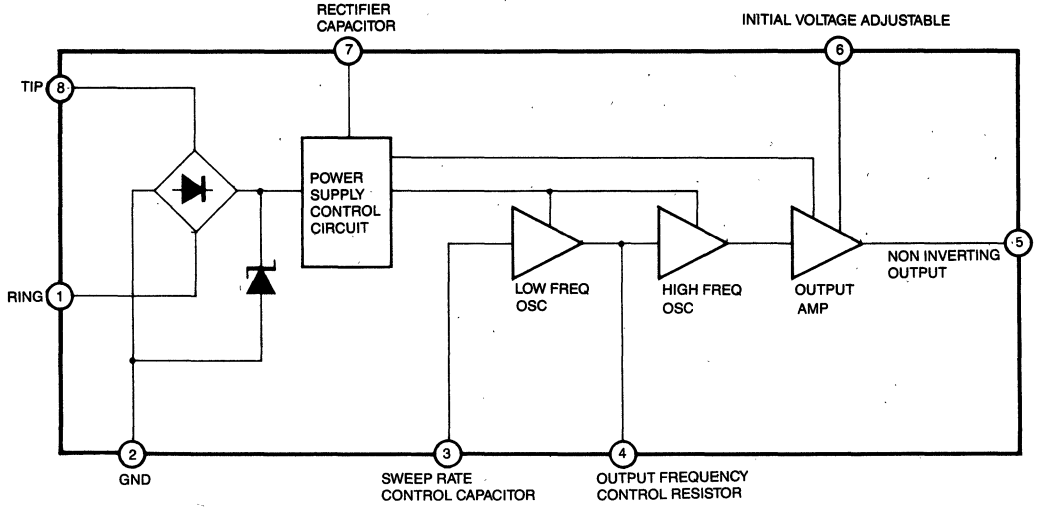


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Calling Voltage (f=50Hz) Continuous	V_{AB}	90	Vrms
Calling Voltage (f=50Hz) 5 Sec ON/10 Sec OFF	V_{AB}	110	Vrms
Supply Current	I_{CC}	22	mA
Operating Temeprature	T_{OP}	-20 ~ +70	°C
Storage and Junction Temeprature	T_{stg}	-65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

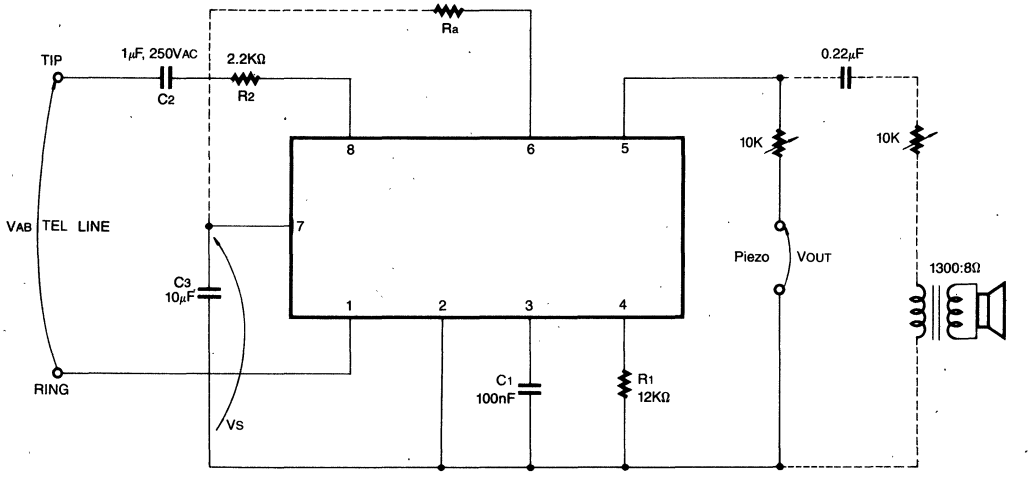
(T_a = 25°C unless otherwise specified)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}				26	V
Current Consumption without Load	I_B	V_S = 8.8 to 26V		1.5	1.8	mA
Activiation Voltage	V_{ON}		12.2		13	V
Activiation Voltage Range	V_{ONR}	R_A = 1kΩ	8		10	V
Sustaining Voltage	V_{OFF}		8		8.8	V
Differential Resistance in Off Condition	R_D		6.4			kΩ
Output Voltage Swing	$V_{OUT\,1}$			V_{CC} -3		V
Short Circuit Current	I_{OUT}			35		mA

AC OPERATION

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequencies		V_{CC} = 26V, R_1 = 14kΩ				
$f_{OUT\,1}$		V_{CC} = 0V		1,900		Hz
$f_{OUT\,2}$		V_{CC} = 6V		1,300		Hz
$f_{OUT\,1}$ Range		R_1 = 27kΩ to 1.7kΩ	0.1		15	KHz
Sweep Frequency		R_1 = 14kΩ, C_1 = 100nF		10		Hz

TEST AND APPLICATION CIRCUIT



$$f_1 = \frac{2.67 \cdot 10^4}{R_1(K\Omega)} \qquad f_2 = \frac{5}{7} f_1 \qquad f_{sweep} = \frac{1000}{C_1(nF)}$$

Fig. 2

DESCRIPTION

The KA2418 tone ringer derive its power supply by rectifying the AC ringing signal. It uses this power to activate two tone generators. The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker; both tone frequencies and the switching frequency can be externally adjusted.

The device can drive either directly a piezo ceramic converter (buzzer) or small loudspeaker. In case of using a loudspeaker, a transformer is needed.

An internal shunt voltage Regulator provides DC voltage to output stage, low frequency oscillator, an High frequency oscillator. To protect the IC from telephone line transients, a zener Diode is included.

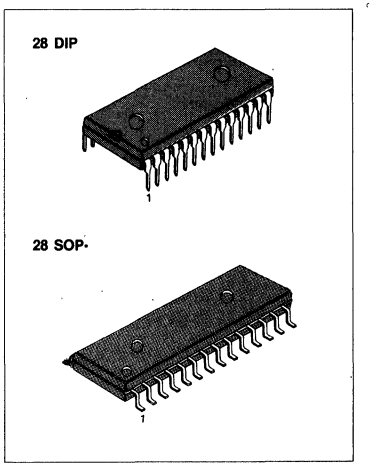
EXTERNAL COMPONENTS (refer to test circuit)

R_1 : Output frequency control resistor
C_1 : Sweep rate control capacitor
R_2 : Line input resistor. R_2affects the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients.
C_2 : Line input capacitor. C_2 AC couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies.
C_3 : Ringer supply capacitor, C_3 filters supply voltage for the tone generating circuits.
R_a : Activation voltage adjustable resistor

VOICE SWITCHED SPEAKER-PHONE

The KA2420 speaker phone chip includes amplifiers, attenuators, and control functions necessary to design a high quality speaker phone system. It also includes a microphone amplifier and audio power amplifier for speaker, background sound level monitoring system, attenuation control system, and the necessary regulated voltages for internal and the external circuits. This will permit operation from the mains with no additional power supply required.

The chip select pin will facilitate power down when the chip is not selected. The volume control may be implemented by using an external potentiometer. The KA2420 can be used in a wide variety of applications such as; intrecom systems, business, automotive or household telephones.



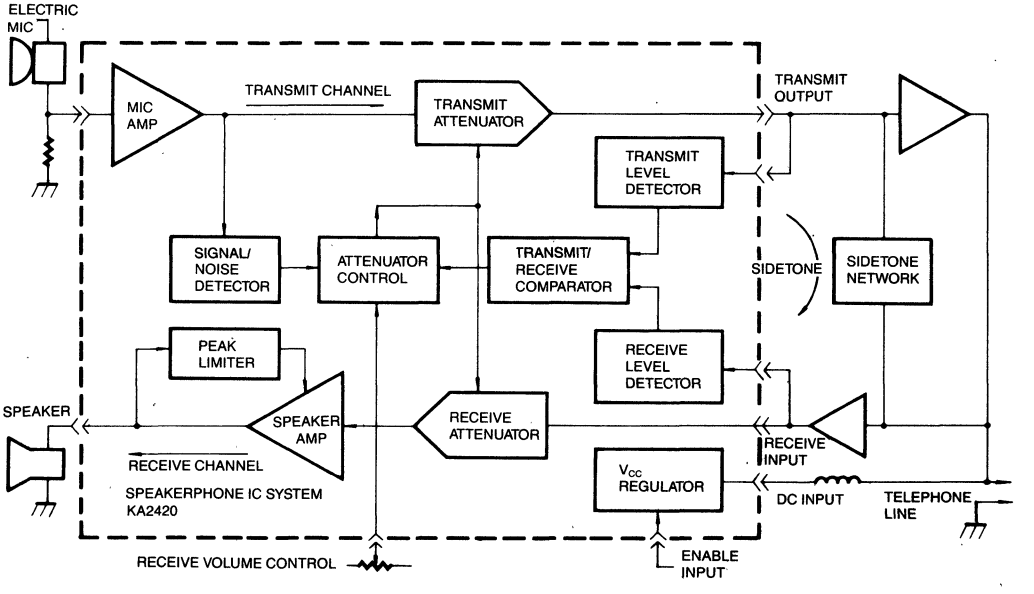
FEATURES

- **Level detection and attenuation controls on single chip**
- **Monitoring for background noise level with large time constant**
- **On-chip regulation for supply and reference voltages**
- **Wide range of operation due to signal compression**
- **Very low output power (10mW typ.) with peak limiting for minimizing distortion**
- **Chip Select allowing standby mode of operation**
- **Volume can be controlled linearly**
- **28 pin plastic DIP & SOP package**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA2420N	28 DIP	−20 ~ +60°C
KA2420D	28 SOP	

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Description
1	RR	A resistor to ground provides a reference current for the transmit and receive attenuators.
2	RTX	A resistor to ground determines the nominal gain of the transmit attenuator. The transmit channel gain is inversely proportional to the RTX resistance.
3	TXI	Input to the transmit attenuator. Input resistance is nominally 5.0KΩ.
4	TXO	Output of the transmit attenuator. The TXO output signal drives the input of the transmit level detector, as well as the external circuit which drives the telephone line.
5	TLI	Input of the transmit level detector. An external resistor ac coupled to the TLI pin sets the detection level. Decreasing this resistor increases the sensitivity to transmit channel signals.
6	TLO	Output of the transmit level detector. The external resistor and capacitor set the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Input of the receive level detector. An external resistor ac coupled to the RLI pin sets the detection level. Decreasing this resistor increases the sensitivity to receive channel signals.
8	RLO	Output of the receive level detector. The external resistor and capacitor set the time the comparator will hold the system in the receive mode after the receive signal ceases.
9	MCI	Microphone amplifier input. Input impedance is nominally 10KΩ and the dc bias voltage is approximately equal to V_B.
10	MCO	Microphone amplifier output. The mic amp gain is internally set at 34dB (50 V/V)
11	CP1	A parallel resistor and capacitor connected between this pin and V_{CC} holds a voltage corresponding to the background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	A capacitor at this pin peak detects the speech signals for comparison with the background noise level held at CP1.
13	XDI	Input to the transmit detector system. The microphone amplifier output is ac coupled to the XDI pin through an external resistor.
14	SKG	High current ground pin for the speaker amp output stage. The SKG voltage should be within 10mV of the ground voltage at pin 22.
15	SKO	Speaker amplifier output. The SKO pin will source and sink up to 100mA when ac coupled to the speaker. The speaker amp gain is internally set at 34dB (50 V/V)
16	V+	Input DC supply voltage. V+ can be powered from Tip and Ring if an ac decoupling inductor is used to prevent loading ac line signals. The required V+ voltage is 6.0 to 11V (7.5V nominal) at 7.0mA.
17	AGC	A capacitor from this pin to VB stabilizes the speaker amp gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SKO. The internal resistance at the AGC pin is nominally 110KΩ.
18	$\overline{CS}$	Digital chip select input. When at a logic "0" (<0.7V) the V_{CC} regulator is enabled. When at a logic "1" (>1.6V), the chip is in the standby mode drawing 0.5mA. An open $\overline{CS}$ pin is a logic "0". Input impedance is nominally 140KΩ. The input voltage should not exceed 11V.
19	SKI	Input to the speaker amplifier. Input impedance is nominally 20KΩ.
20	V_{CC}	A 5.4V regulated output which powers all circuits except the speaker amplifier output stage. V_{CC} can be used to power external circuitry such as a microprocessor (3.0mA max.). A filter capacitor is required. The KA2420 can be powered by a separate regulated supply by connecting V+ and V_{CC} to a voltage between 4.5V and 6.5V while maintaining $\overline{CS}$ at a logic "1".

PIN DESCRIPTION (Continued)

Pin	Name	Description
21	V_B	An output voltage equal to approximately $V_{CC}/2$ which serves as an analog ground for the speakerphone system. Up to 1.5mA of external load current may be sourced from V_B. Output impedance is 250Ω. A filter capacitor is required.
22	Gnd	Ground pin for the IC (except the speaker amplifier)
23	XDC	Transmit detector output. A resistor and capacitor at this pin hold the system in the transmit mode during pauses between words or phrases. When the XDC pin voltage decays to ground, the attenuators switch from the transmit mode to the idle mode. The internal resistor at XDC is nominally 2.6KΩ (see Fig. 1)
24	VLC	Volume control input. Connecting this pin to the slider of a variable resistor provides receive mode volume control. The VLC pin voltage should be less than or equal to V_B.
25	ACF	Attenuator control filter. A capacitor connected to this pin reduces noise transients as the attenuator control switches levels of attenuation.
26	RXO	Output of the receive attenuator. Normally this pin is ac coupled to the input of the speaker amplifier.
27	RXI	Input of the receive attenuator. Input resistance is nominally 5.0KΩ.
28	RRX	A resistor to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RRX resistance.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to Pin 22, T_a=25°C)

Characteristic	Value	Unit
Speaker Amp Ground (Pin 14)	+3.0, −1.0	V
V+ Terminal Voltage (Pin 16)	+12, −1.0	V
$\overline{CS}$ (Pin 18)	+12, −1.0	V
VLC (Pin 24)	V_{CC}, −1.0	V
Storage Temperature	−65~150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Electrical Characteristics" tables provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Value	Unit
Microphone Signal (Pin 9)	0~5.0	mVrms
Speaker Amp Ground (Pin 14)	−10~10	mV
V+ Terminal Voltage (Pin 16)	+6.0~11	V
$\overline{CS}$ (Pin 18)	0~11	V
I_{CC} (Pin 20)	0~3.0	mA
VLC (Pin 24)	$0.55V_B \sim V_B$	V
Receive Signal (Pin 27)	0~250	mVrms
Ambient Temperature	−20~60	°C

ELECTRICAL CHARACTERISTICS (Refer to Fig. 1)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
V+ Supply Current	I_V +	V+=11V, Pin 18=0.7V			9.0	mA
		V+=11V, Pin 18=1.6V			800	μA
V_{CC} Voltage	V_{CC}	V+=7.5V	4.9	5.4	5.9	V
V_{CC} Line Regulation	ΔV_{CC}	6.5V < V+ <11V		65	150	mV
V_{CC} Output Resistance	R_O	I_{CC}=3.0mA		6.0	20	Ω
V_{CC} Drop Voltage	V_{CC} D	V+=5.0V		80	300	mV
V_B Voltage	V_B	V+=7.5V	2.5	2.9	3.3	V
V_B Output Resistance	R_O	I_B = 1.7mA		250		Ω
ATTENUATORS						
Receive Attenuator Gain		1.0KHz				
Rx Mode	Arx	Pin 24=V_B, Pin 27=250mVrms	2.0	6.0	10	dB
Range	ΔArx	Rx to Tx Mode	40	44	48	dB
Idle Mode	Arxi	Pin 27=250mVrms	−20	−16	−12	dB
Rxo Voltage	Vrxo	Rx Mode	1.8	2.3	3.2	V
Rxo Voltage Change	ΔVrxo	From Rx to Tx Mode			100	mV
Rxo Sink Current	$I_R$sink	Rx Mode	75			μA
Rxo Source Current	$I_R$source	Rx Mode	1.0		3.0	mA
Rxi Input Resistance	Rrxi		3.5	5.0	8.0	KΩ
Volume Control Range	Vcon	Rx Attenuator Gain, Rx Mode, 0.6V_B < Pin 24 < V_B	24.5		32.5	dB
Transmit Attenuator Gain		1KHz				
Tx Mode	Atx	Pin 3=250mVrms	4.0	6.0	8.0	dB
Range	ΔAtx	Tx to Rx Mode	40	44	48	dB
Idle Mode	Atxi	Pin 3=250mVrms	−16.5	−13	−8.5	dB
Txo Voltage	Vtxo	Tx Mode	1.8	2.3	3.2	V
Txo Voltage Change	ΔVtxo	From Tx to Rx Mode			100	mV
Txo Sink Current	$I_T$sink	Tx Mode	75			μA
Txo Source Current	$I_T$source	Tx Mode	1.0		3.0	mA
Txi Input Resistance	Rtxi		3.5	5.0	8.0	KΩ
ACF Voltage	Vacf	V_{CC}-Pin 25 Voltage				
		Rx Mode		150		mV
		Tx Mode		6.0		mV
		Idle Mode		75		mV
SPEAKER AMPLIFIER						
Speaker Amp Gain	Aspk	Pin 19=20mVrms	33	34	35	dB
SKI Input Resistance	Rski		15	22	37	KΩ
SKO Voltage	Vsko	Capacitor Tied to GND	2.4	3.0	3.6	V
SKO High Voltage	Vskoh	Pin 19=0.1V, −100mA Load at Pin 15	5.5			V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
SKO Low Voltage	Vskol	Pin 19=−0.1V, +100mA Load at Pin 15			600	mV
MICROPHONE AMPLIFIER						
Mike Amp Gain	Amci	Pin 9=10mVrms 1KHz	32.5	34	35	dB
Mike Amp Input Resistance	Rmci		6.5	10	16	KΩ
LOG AMPLIFIER						
RLO Leakage Current	Ilkrlo	Pin 8=V_B+1.0V			2.0	μA
TLO Leakage Current	Ilktlo	Pin 6=V_B+1.0V			2.0	μA
Tx-Rx Switching Threshold	S, Th.	Ratio of I_{TLI} to I_{RLI} at 20μA to Switch Tx-Rx Comparator	0.8		1.2	
TRANSMIT DETECTOR						
XDC Voltage	Vxdc	Idle Mode		0		V
		Tx Mode		4.0		V
CP2 Current Source	Icp2		5.0	10	13	μA
DISTORTION						
Rx Mode-RXI to SKO	Rxd	Pin 27=10mVrms, 1KHz		1.5		%
Tx Mode-MCI to TXO	Txd	Pin 9=5.0mVrms, 1KHz		2.0		%

Note: 1. V+=7.5V, $\overline{CS}$=0.7V except where noted.
2. Rx Mode: Pin 7=−100μA, Pin 5=+100μA except where noted.
Tx Mode : Pin 5, 13=−100μA, Pin 7= + 100μA, Pin 11 = 0V
Idle Mode: Pin 5=−100μA, Pin 7, 13=+100μA
3. Current into a pin designated as +: current out of a pin designated as —
4. Voltage referred to Pin 22, Ta=+25°C.

TEMPERATURE CHARACTERISTICS (−20 to +60°C)

Characteristic	Pin	Typical Change	Unit
V+ Supply Current (V+=11V, Pin 18=0.7V)	16	−0.2	%/°C
V+ Supply Current (V+=11V, Pin 18=1.6V)	16	−0.4	%/°C
V_{CC} Voltage (V+=7.5V)	20	+0.1	%/°C
Attenuator Gain (Max and Min Settings)		±0.003	dB/°C
Delta RXO, TXO voltage	4, 26	±0.24	%/°C
Speaker Amp Gain	15, 19	±0.003	dB/°C
Microphone Amp Gain	9, 10	±0.001	dB/°C
Microphone Amp Input Resistance	9	+0.4	%/°C
Tx-Rx Switching Threshold (@20μA)	5, 7	±0.2	nA/°C

TEST CIRCUIT

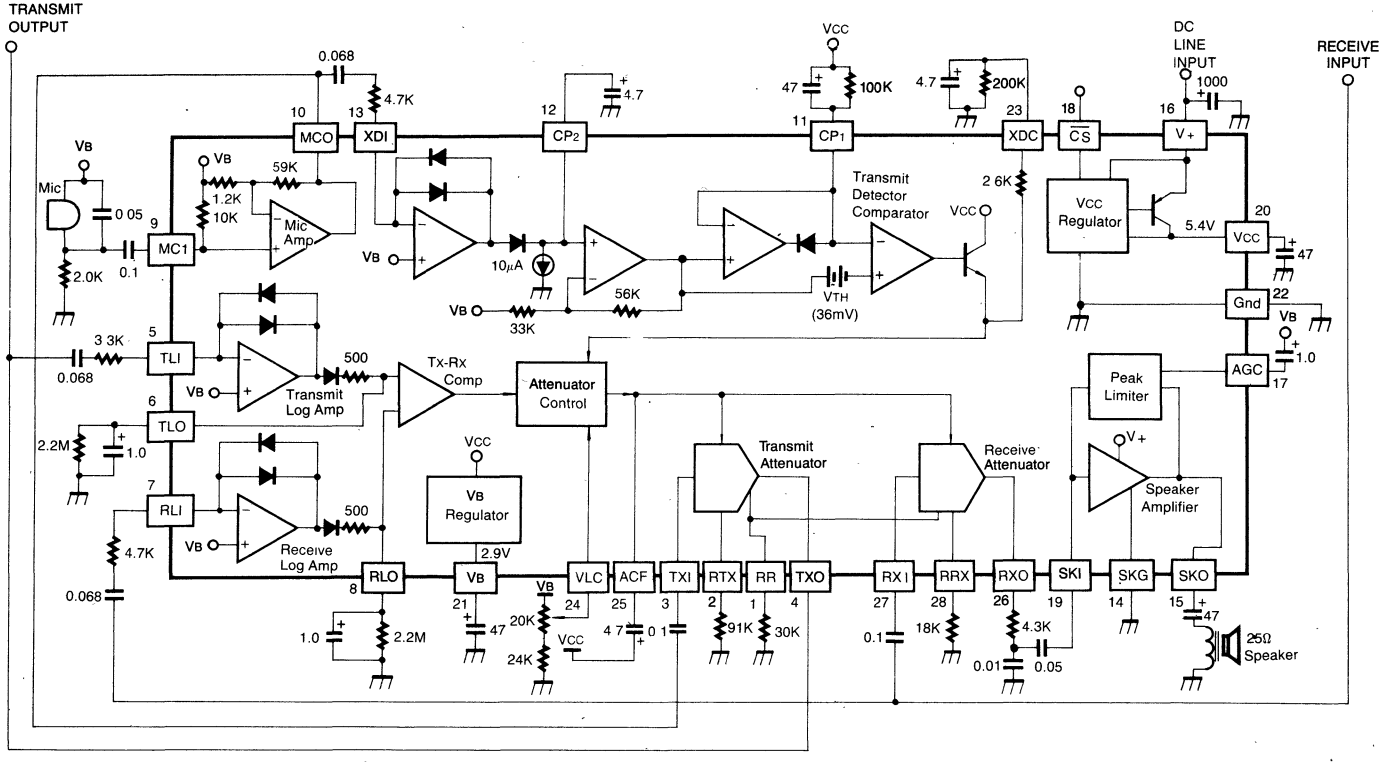


Fig. 1

TRANSMIT ATTENUATOR V_S RTX

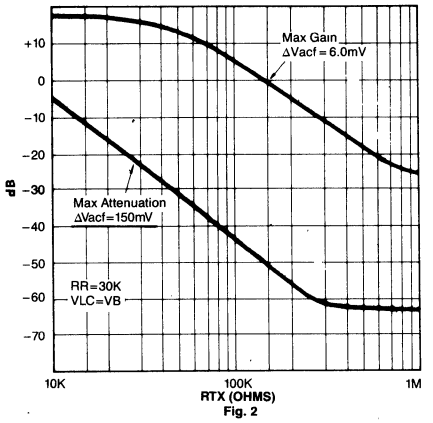


Fig. 2

RECEIVE ATTENUATOR V_S RRX

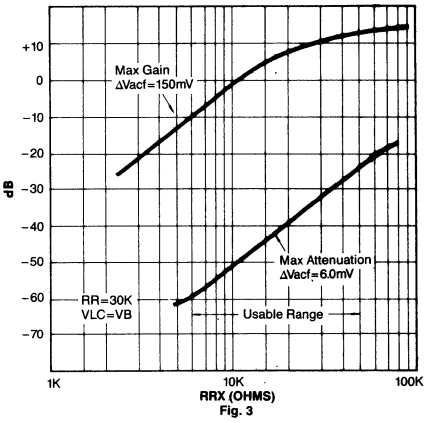


Fig. 3

GAIN AND ATTENUATION V_S RESISTOR RATIOS

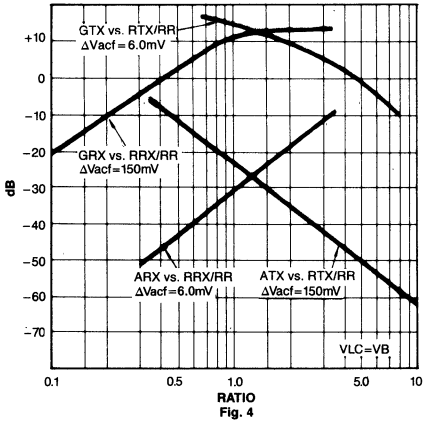


Fig. 4

ATTENUATOR GAIN V_S VLC

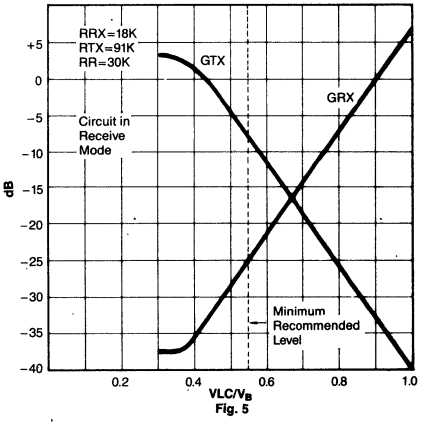


Fig. 5

ATTENUATOR GAIN V_S ΔVacf

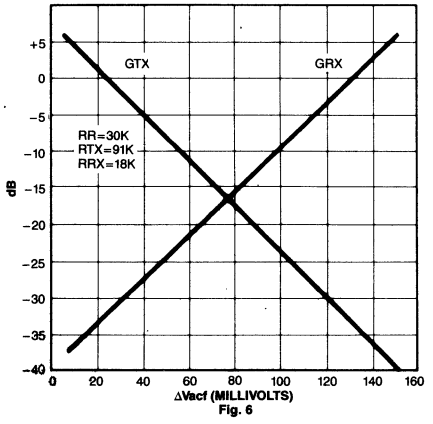


Fig. 6

LOG AMP TRANSFER CHARACTERISTICS

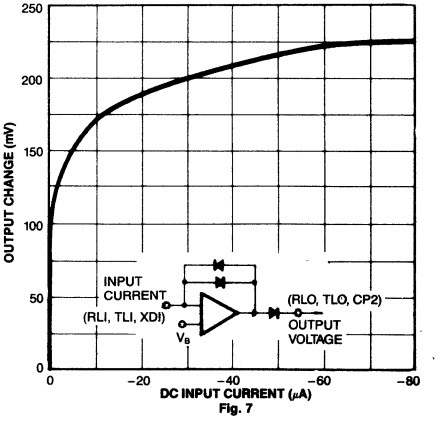


Fig. 7

LOG AMP TRANSFER CHARACTERISTICS

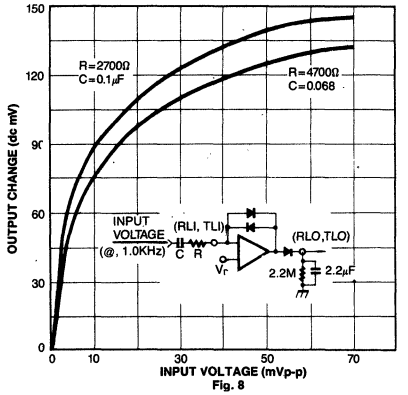


Fig. 8

SPEAKER AMP OUTPUT VS SUPPLY VOLTAGE

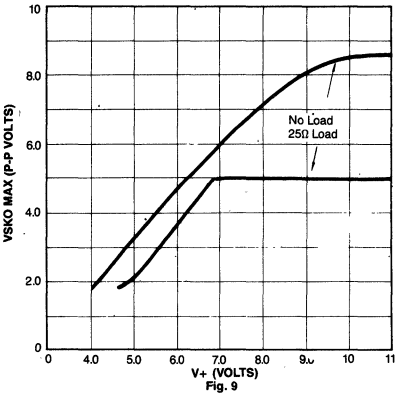


Fig. 9

RESPONSE AT CP2 AND CP1

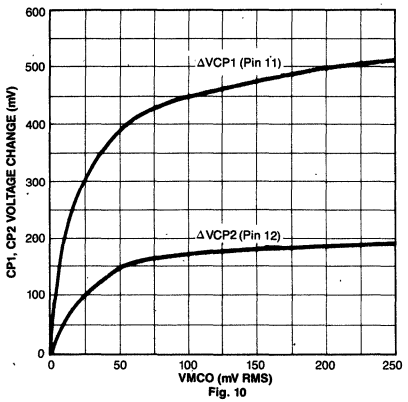


Fig. 10

TRANSMIT DETECTOR OPERATION

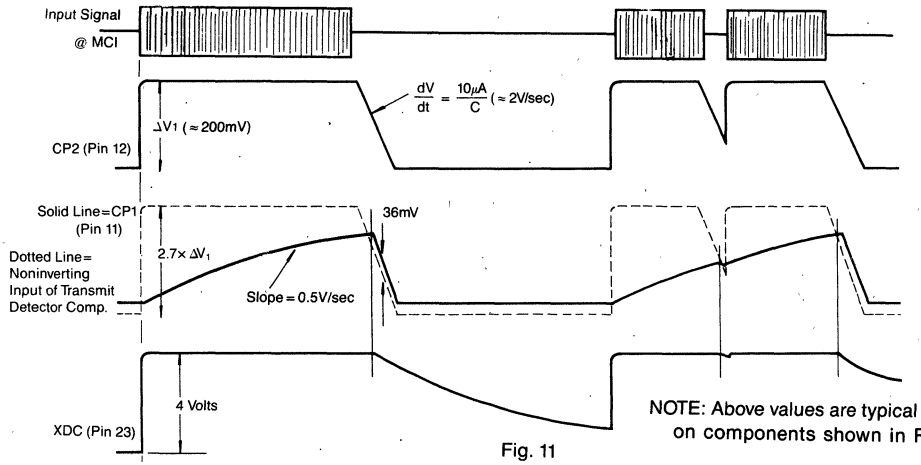


Fig. 11

NOTE: Above values are typical based on components shown in Fig. 1.

SUPPLY CURRENT Vs SUPPLY VOLTAGE

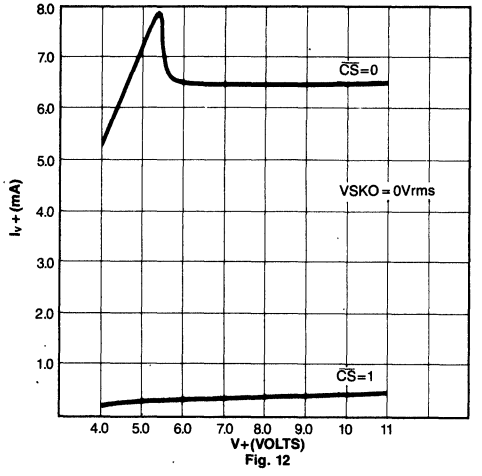


Fig. 12

SUPPLY CURRENT Vs SUPPLY VOLTAGE Vs SPEAKER POWER

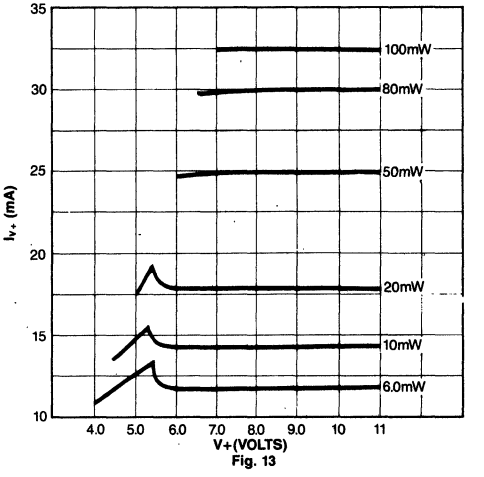


Fig. 13

ALTERNATE POWER SUPPLY CONFIGURATION

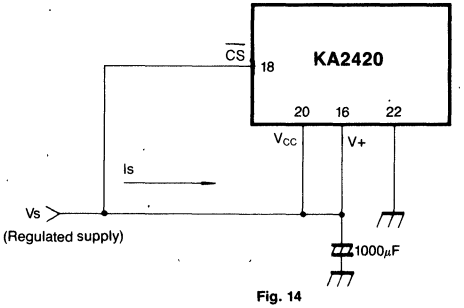


Fig. 14

SUPPLY CURRENT Vs SUPPLY VOLTAGE (see Fig. 14)

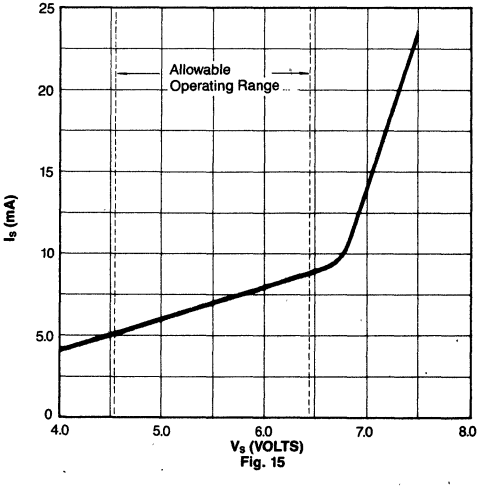


Fig. 15

SWITCHING TIME

The switching times of the speakerphone depends on the external components and the instantanious operating conditions at the time when a change takes place. For example, the switching time for changing between transmit and receive modes is much longer than that from idle to transmit.

The components connected at pin 5 "transimit turn-on", pin 6 "transmit-turn-off", pin 7 "receive-turn-on" and pin 8 "receive-turn-off" have major influence on the timing between the transmit and receive modes. The Tx-Rx comparator compares the relative and not the absolute values so the above referenced four timing functions interact with each other. The timing from transmit to idle is affected by the components at pins 11, 12, 13 and 23. The timing from idle to transmit is faster and hence the components have no major influence on it.

The table below indicates the degree of influence of various components on the switching time, including the volume control;

Additionally, the following should be noted:

1) The RCs at Pin 5 and Pin 7 affect the sensitivity of the respective log amplifiers, or how loud the speech must be for gain control of the speakerphone circuit.
2) The RC at Pin 13 controls the sensitivity of the transmit detector circuit.
3) The switching speed and the relative response to transmit signal are affected by the volume control, in manner as follows: When the volume control reduces, the signal at TXO increases, and consequently the signal to the TLI pin in the receive mode circuit.

Components	Rx to Tx	Tx to Rx	Tx to Idle
RC at Pin 5	high	medium	no influence
RC at Pin 6	medium	high	no influence
RC at Pin 7	medium	high	no influence
RC at Pin 8	high	medium	no influence
RC at Pin 11	low	no influence	medium
C at Pin 12	low	no influence	high
RC at Pin 13	low	no influence	low
RC at Pin 23	low	no influence	high
V at Pin 24	medium	no influence	no influence
C at Pin 25	medium	medium	low

Switching response times for the circuit of Fig. 1 are shown in the photographs of Fig. 16 and Fig. 17.

In Fig. 16, the circuit is supplied a continuous receive signal of 1.1mV$_{P-P}$ at RXI as shown Trace #3. MCI as shown Trace #1 operates a repetitive signal of 7.2mV$_{P-P}$ for 120msec, and repeated every 1sec. Trace #2 is the TXO output being about 650mV$_{P-P}$ at its maximum. Trace #4 is the RXO output being about 2.2mV$_{P-P}$ at its maximum.

The switching time from the receive mode to transmit mode is about 40msec required for TXO to turn on, and for RXO to turn off. After the signal at MCI is turned off, the switching time back to the receive mode is about 210msec.

In Fig. 17 a continuous signal of 7.6mV$_{P-P}$ is supplied to MCI as shown Trace #1, and a repetitive burst signal of 100mV$_{P-P}$ is supplied to RXI as shown Trace #3 for 120msec, and repeated every 1sec. Trace #2 is the TXO output and is about 90mV$_{P-P}$ at its maximum, and Trace #4 shows the RXO output being about 150mV$_{P-P}$ at its maximum, In this sequence, the circuit switches between the idle mode and the receive mode. The required switching time from idle to receive modes is about 70msec as shown in the first part of Trace #2 and Trace #4. After the receive signal is turned off, the switching time back to the idle mode is about 100msec.

All of above mentioned switching times can change significantly not only by varying the external components but also by varying the amplitude of input signals.

TRANSMIT-RECEIVE SWITCHING

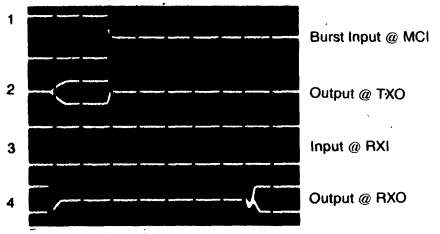


Fig. 16

IDLE-RECEIVE SWITCHING

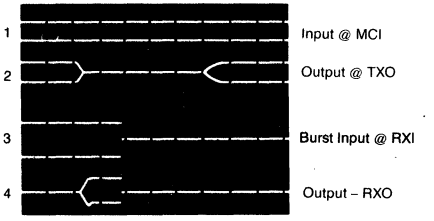
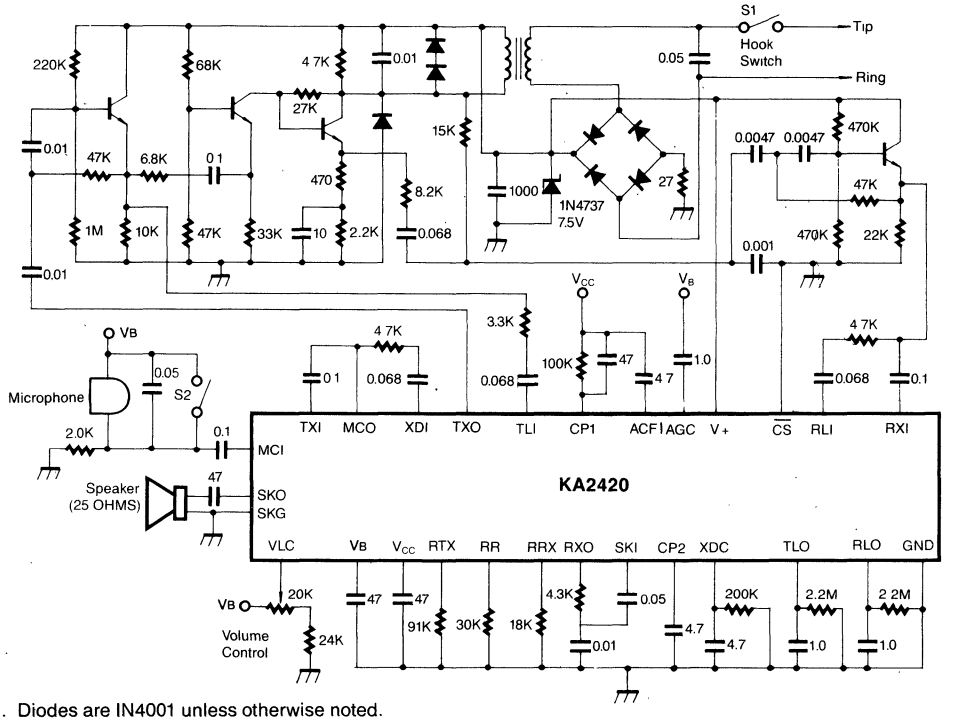


Fig. 17

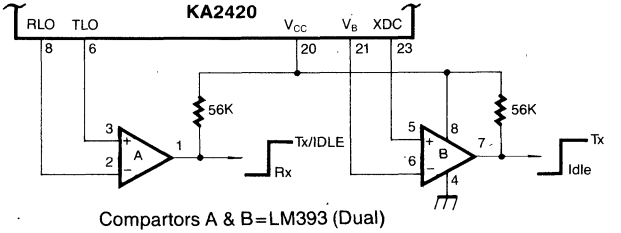
BASIC LINE POWERED SPEAKERPHONE



1. Diodes are IN4001 unless otherwise noted.
2. 4 Transistors are KSC945-Y
3. Recommended Transformer: Seoul Jupa SJ-019-2040

Fig. 18

DIGITAL TRANSMIT/IDLE/RECEIVE INDICATION



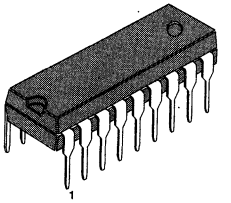
Compartors A & B=LM393 (Dual)

Fig. 19

TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The KA2425A/B is a Telephone Speech Network Integrated Circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization amp which compensates gains for line length variations. The conversion from 2 to 4 wire is accomplished with a supply voltage as low as 1.5 volts.

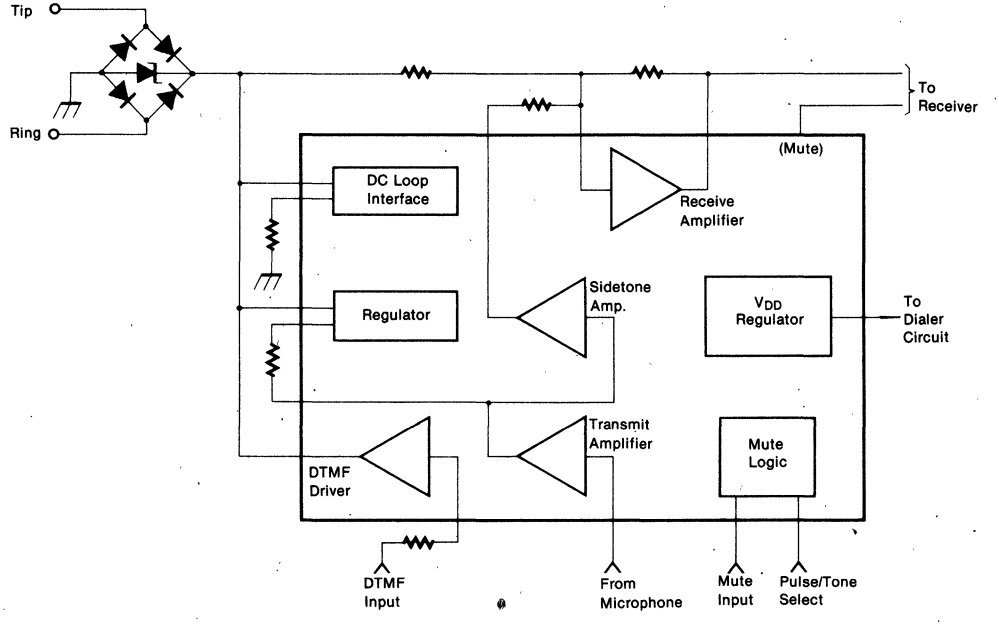
18 DIP



FEATURES

- **Transmit, Receive, and Sidetone Gain Set by External Resistors**
- **Loop Length Equalization for Transmit, Receive, and Sidetone Functions**
- **Low Voltage Operates Down to 1.5 volts (V+) in Speech Mode**
- **Provides Regulated Voltage for CMOS Dialer**
- **$\overline{\text{MUTE}}$: KA2425A, MUTE: KA2425B**
- **DTMF Output Level Adjustable with Single Resistor**
- **Compatible with 2-Terminal Electric Microphones (ECM)**
- **Compatible with Receiver impedances of 150Ω and Higher**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Voltage referred to V−, Ta = 25°C) (see Note 1.)

Characteristic	Value	Unit
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0 +6	Vdc
V_{LR}	−1.0, V+ −3.0	Vd
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

Note 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Value	Unit
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
LINE INTERFACE						
V+ Voltage	V+					V_{dc}
Speech/Pulse Mode		I_L = 20mA	2.6	3.2	3.8	
Speech/Pulse Mode		I_L = 30mA	3.0	3.7	4.4	
Speech/Pulse Mode		I_L = 120mA	7.0	8.2	9.5	
Tone Mode		I_L = 20mA	4.1	4.9	5.7	
Tone Mode		I_L = 30mA	4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	1+					mA
Speech Mode		V+ = 1.7V	4.5	7.1	9.0	
Speech/Pulse Modes		V+ = 12V	5.5	8.4	12.5	
Tone Mode		V+ = 12V	6.0	8.8	14.0	
LR Level Shift	$\triangle V_{LR}$					V_{dc}
Speech/Pulse Mode		V+ − V_{LR}	—	2.7	—	
Tone Mode		V+ − V_{LR}	—	4.3	—	
LC Terminal Resistance	R_{LC}		36	57	94	KΩ
VOLTAGE REGULATORS						
VR Voltage	V_R	(V+ = 1.7V)	1.1	1.2	1.3	V_{dc}
Load Regulation	$\triangle V_{RLD}$	0mA < I_R < 6.0mA	—	20	—	mV
Line Regulation	$\triangle V_{RLN}$	2.0V < V+ < 6.5V	—	25	—	mV
V_{DD} Voltage	V_{DD}	(V+ = 4.5V)	3.0	3.3	3.8	V_{dc}
Load Regulation(Dialing Mode)	$\triangle V_{DDLD}$	0 < I_{DD} < 1.6mA	—	0.25	—	V_{dc}
Line Regulation (All Modes)	$\triangle V_{DDLN}$	4.0V < V+ < 9.0V	—	50	—	mV
Max. Output Current	I_{DDSP}	Speech Mode	375	550	1000	μA
Max. Output Current	I_{DDDL}	Dialing Mode	1.6	2.0	3.6	mA
V_{DD} Leakage Current	I_{DDLK}	V+ = 0, V_{DD} = 3.0V		—	1.5	μA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SPEECH AMPLIFIERS						
Transmit Amplifier						
Gain	A_{TXO}	TXI to TXO	22	24	26	dB
TXO Bias Voltage	V_{TXOSP}	Speech/Pulse Mode	0.45	0.52	0.60	x V_R
TXO Bias Voltage	V_{TXODL}	Tone Mode	VR – 25	VR – 5.0	—	mV
TXO High Voltage	V_{TXOH}	Speech/Pulse Mode	VR – 25	VR – 5.0	—	mV
TXO Low Voltage	V_{TXOL}	Speech/Pulse Mode	—	125	250	mV
TXI Input Resistance	R_{TXI}		—	10	—	KΩ
Receive Amplifier						
RXO Bias Voltage	V_{RXO}	All Mode	0.45	0.52	0.60	x V_R
RXO Source Current	I_{RXOSP}	Speech Mode	1.5	2.0	—	mA
RXO Source Current	I_{RXODL}	Pulse/Tone Mode	200	400	—	μA
RXO High Voltage	V_{RXOH}	All Mode	VR – 100	VR – 50	—	mV
RXO Low Voltage	V_{RXOL}	All Mode	—	50	150	mV
MICROPHONE, RECEIVER CONTROLS						
MIC Saturation Voltage	V_{OLMIC}	Speech Mode, I = 500μA	—	50	125	mV
MIC Leakage Current	I_{MICLK}	Dialing Mode, Pin 1 = 3.0V	—	0	5.0	μA
RMT REsistance	R_{RMTSP}	Speech Mode	—	8.0	15	Ω
	R_{RMTDL}	Dialing Mode	5.0	10	18	KΩ
RMT Delay	t_{RMT}	Dialing to Speech	2.0	4.0	20	ms
SIDETONE AMPLIFIER						
Gain (TXO to STA)	A_{STA}					dB
Speech Mode		@V_{LR} = 0.5V	—	– 15	—	
Speech Mode		@V_{LR} = 2.5V	—	– 21	—	
Pulse Mode		@V_{LR} = 0.2V	—	– 15	—	
Pulse Mode		@V_{LR} = 1.0V	—	– 21	—	
STA Bias Voltage	V_{STA}	All Modes	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER						
Gain (V+ to EQ)	A_{EQ}					dB
Speech Mode		@V_{LR} = 0.5V	—	– 12	—	
Speech Mode		@V_{LR} = 2.5V	—	– 2.5	—	
Pulse Mode		@V_{LR} = 0.2V	—	– 12	—	
Pulse Mode		@V_{LR} = 1.0V	—	– 2.5	—	
EQ Bias Voltage	V_{EQ}					V_{dc}
Speech Mode		@V_{LR} = 0.5V	—	0.66	—	
Pulse Mode		@V_{LR} = 0.5V	—	1.3	—	
Speech, Pulse Mode		@V_{LR} = 2.5V	—	3.3	—	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
DIALING INTERFACE						
$\overline{MT}$ Input Resistance	R_{MT}		58	100	—	KΩ
MT Input Resistance			—	50	—	KΩ
$\overline{MT}$, MT Input High Voltage	V_{IHMT}		$V_{DD}-0.3$	—	—	V_{dc}
$\overline{MT}$, MT Input Low Voltage	V_{ILMT}		—	—	1.0	V_{dc}
MS Input Resistance	R_{MS}		280	600	—	KΩ
MS Input High Voltage	V_{IHMS}		2.0	—	—	V_{dc}
MS Input Low Voltage	V_{ILMS}		—	—	0.3	V_{dc}
TI Input Resistance	R_{TI}		—	1.25	—	KΩ
DTMF Gain	A_{DTMF}	See Figure 2 ($V+/V_{IN}$)	3.2	4.8	6.2	dB
SYSTEM SPECIFICATIONS (Refer to Fig. 1~ Fig. 4)						
Tip-Ring Voltage (including polarity guard bridge drop of 1.4V) (Speech Mode)		$I_L=5.0mA$ $I_L=10mA$ $I_L=20mA$ $I_L=40mA$ $I_L=60mA$	— — — — —	2.4 3.9 4.6 5.6 6.6	— — — — —	V_{dc}
Transmit Gain from V_S to V+ Gain Change Distortion Output Noise		Figure 3 ($I_L=20mA$) $I_L=60mA$	28 −6.0 — —	29.5 −4.5 2.0 11	31 −3.6 — —	dB dB % dBrnc
Receive V_{RXO}/V_S Receive Gain Change Distortion		$f=1.0KHz$, $I_L=20mA$ (See Figure 4) $I_L=60mA$	−16 −5.0 —	−15 −3.0 2.0	−13 −2.0 —	dB dB %
Sidetone Level $V_{RXO}/V+$ (Figure 3)		$I_L=20mA$ $I_L=60mA$	— —	−36 −21	— —	dB
Sidetone Cancellation $\{\frac{V_{RXO}}{V+}$ (Figure 4)$\}dB-\{\frac{V_{RXO}}{V+}$ (Figure 3)$\}dB$		$I_L=20mA$	20	26	—	dB
DTMF Driver $V+V_{IN}$ (Figure 2)		$I_L=20mA$	3.2	4.8	6.2	dB
AC Impedance Speech mode (incl. C_6, See Figure 4) $Z_{ac}=(600)V+/(V_S-V+)$ Tone Mode (including C_6)		$I_L=20mA$ $I_L=60mA$ $20mA<I_L<60mA$	— — —	750 300 1650	— — —	Ω

Note: Typicals are not tested or guaranteed.

PIN DESCRIPTION (See Fig. 1)

Pin No.	Name	Description
1	MIC	Microphone negative supply. Bias current from the electric microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off disabling the microphone.
2	TXI	Transmit amplifier input. Input impedance is 10KΩ. Signals from the microphone are input through capacitro C_5 to TXI
3	TXO	Transmit amplifier output. The AC signal current from this output flows through the V_R series pass transistor via R_9 to drive the line at V+. Increasing R_9 will decrease the signal at V+. The output is biased at≈0.65V to allow for maximum swing of AC signals. The closed loop from TXI to TXO is internally set at 26dB.
4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
5	CC	Compensation capacitor. A capacitor from CC to GND will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the AC impedance of the circuit to increase.
7	RXI	Receive amplifier input. Input impedance is >100KΩ. Signals from the line and sidetone amplifier are summed at RXI.
8	RXO	Receive amplifier output. RXO is biased by a 2.5mA current source. Feedback maintains the DC bias voltage at ≈ 0.65V. Increasing R_4 (between RXO and RXI) will increase the receive gain. C_4 stabilizes the amplifier. C_3 couples the signals to the receiver. The 2.5mA current source is reduced to 0.4mA when dialing.
9	RMT	Receiver Mute. The AC receiver current is returned to V− through an open collector NPN transistor and a parallel 10KΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10KΩ resistor in series with the receiver.
10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
11	VR	Regulated voltage output. The VR voltage is regulated at 1.2V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5V. Capacitor C_8 stabilizes the regulator.
12	LC	DC load capacitor. An external capacitor C_7 and an internal resistor form a low pass filter between V+ and LR to prevent AC signals from being loaded by the DC load resistor R_5. Forcing LC to V− will turn off the DC load current and increase the V+ voltage.

PIN DESCRIPTION (See Fig. 1) (Continued)

Pin No.	Name	Description
13	LR	DC load resistor. Resistor R_5 from LR to V− determines the DC resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode)
14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the KA2425A/B are powered by V+.
15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3V. The nominal output current is increased from 550μA to 2mA when dialing. Capacitor C_9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R_7. The current at TI is amplified to drive the line at V+. Increasing R_7 will reduce the DTMF output levels. The input impedance at TI is nominall 1.25KΩ.
17	MS	Mode select. This pin is connected through an internal 600KΩ resistor to base of an NPN transistor. A logic "1" (>2.0V) selects the pulse dialing mode. A logic "0" (<0.3V) selects the tone dialing mode.
18	$\overline{MT}$	Mute input for KA2425A. $\overline{MT}$ is connected through an internal 100KΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A logic "0" (<1.0V) will mute the network for either pulse or tone dialing. A logic "1" (>V_{DD} − 0.3V) puts the KA2425A into the speech mode.
	MT	Mute input for KA2425B. MT is connected through an internal 50KΩ to the base of a NPN transistor, with the collector to the base of a PNP transistor. A logic "1" (>V_{DD} − 0.3V) will mute the network for either pulse or tone dialing. A logic "0" (<1.0V) puts the KA2425B into the speech mode.

Fig. 1 Test Circuit

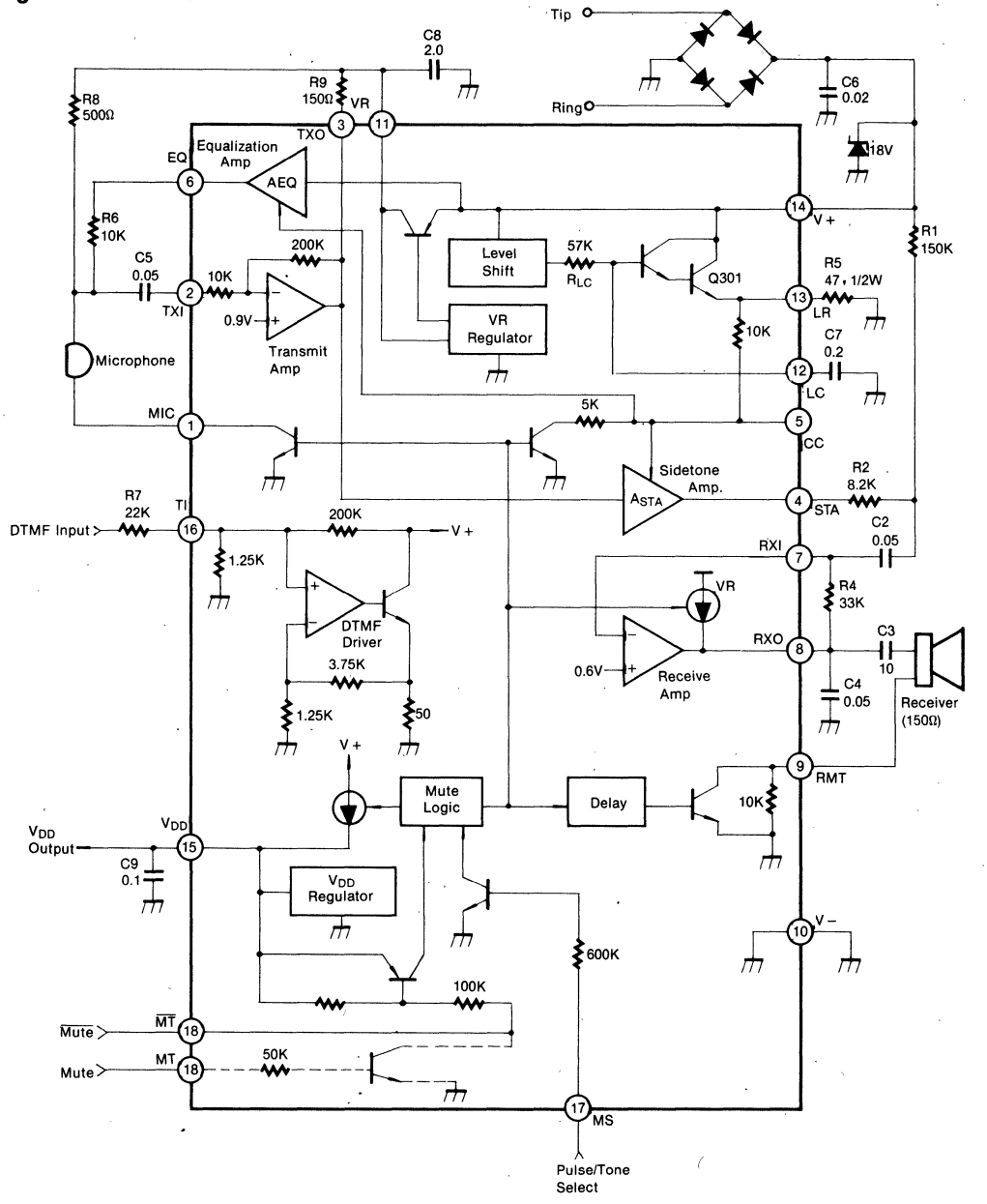


Fig. 2 DTMF Driver Test

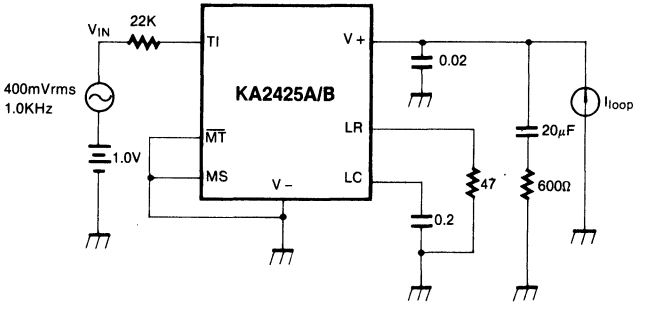


Fig. 3 Transmit and Sidetone Level Test

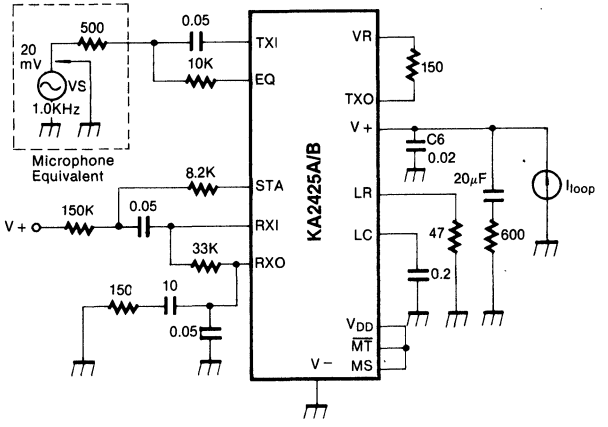
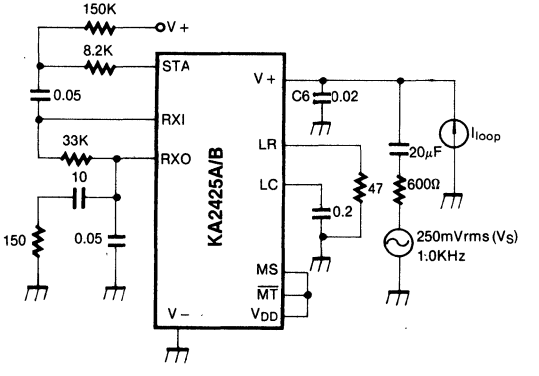
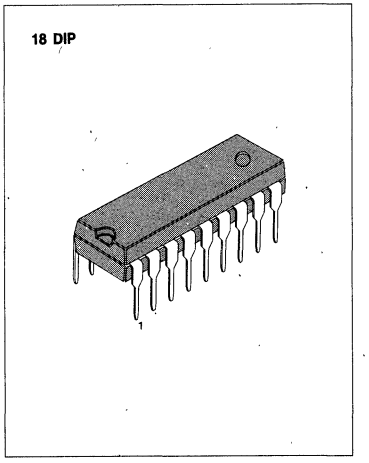


Fig. 4 AC Impedance, Receive and Sidetone Cancellation Test



TELEPHONE PULSE DIALER WITH REDIAL

The KS5805A/B is a monolithic CMOS integrated circuit and provides all the features required for implementing a pulse dialer with redial.



FUNCTIONS

- Mute output logic "0"
- Pulse output logic "0"
- RC oscillation for reference frequency
- Designed to operate directly from the telephone line
- Used CMOS technology for low voltage, low power operation
- Power up clear circuitry
- KS5805A pin 2: V_{REF}
- KS5805B pin 2: Tone out

FEATURES

- **Uses either a standard 2 of 7 matrix keyboard with negative true common or the inexpensive form A-type keyboard**
- **Make/Break ratio can be selected**
- **Redial with * or #**
- **Continuous MUTE**
- **Tone signal output or on-chip reference Voltage by bonding option on chip**
- **10 pps/20 pps can be selected**

TEST CIRCUIT

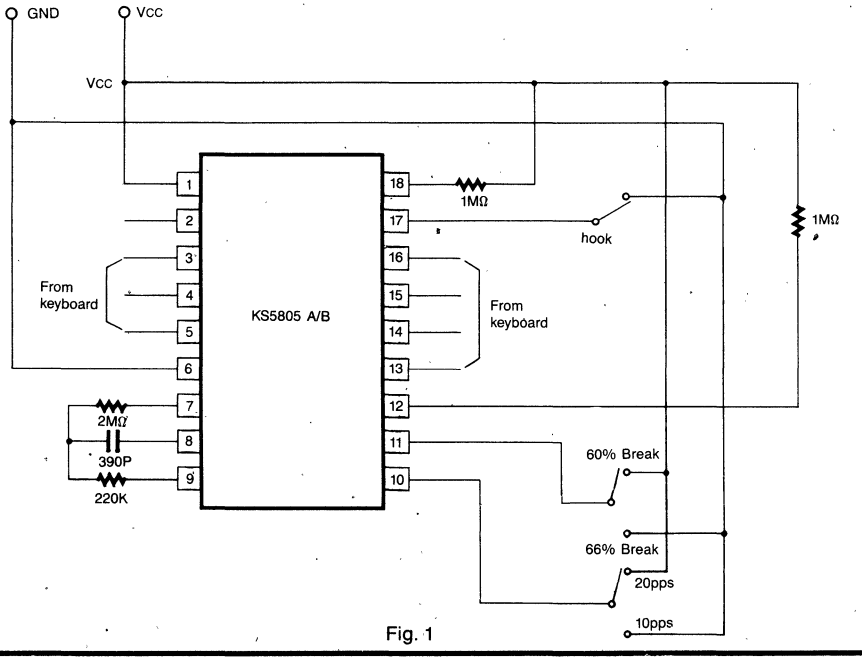


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	6.2	V
Voltage on Any Pin	V_{IN}	V_{CC} +0.3, Gnd−0.3	V
Power Dissipation	P_D	500.0	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

DC ELECTRICAL CHARACTERISTICS

(T_a =25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{CC}		2.5		6.0	V	
Key Contact Resistance	R_{KI}				1	KΩ	1
Keyboard Capacitance	C_{KI}				30	pF	
Key Input Voltage	K_{IH}	2 of 7 input mode	0.8V_{CC}		V_{CC}	V	1
	K_{IL}		Gnd		0.2V_{CC}		
Key Pull-Up Resistance	K_{IRU}	V_{CC} =6.0V		100		KΩ	
Key Pull-Down Resistance	K_{IRD}	V_{IN} =4.8V		4.0		KΩ	
Mute Sink Current	I_M	V_{CC} =2.5V V_O =0.5V	500			μA	2
Pulse Output Sink Current	I_P	V_{CC} =2.5V V_O =0.5V	1.0			mA	3
Tone Output Sink Current	I_{TL}	V_{CC} =2.5V V_O =0.5V	250			μA	4
Tone Output Source Current	I_{TH}	V_{CC} =2.5V V_O =0.5V	250			μA	4
Memory Retention Current	I_{MR}	All outputs under no load		0.7		μA	6
Operating Current	I_{OP}	All outputs under no load		100	150	μA	
Mute or Pulse Off Leakage	I_{LKG}	V_{CC} =6.0V V_O =6.0V		0.001	1.0	μA	2,3
V_{REF} Output Source Current	I_{REF}	V_{CC}-V_{REF} =6.0V	1.0	7.0		mA	5

Note 1) Applies to key input pin. (R_1-R_4, C_1-C_3)
2) Applies to $\overline{\text{MUTE}}$ output in.
3) Applies to $\overline{\text{PULSE}}$ output pin.
4) Applies to TONE pin (KS5805B)
5) Applies to V_{REF} pin (KS5805A)
6) Current necessary for memory to be maintained. All outputs unloaded.

* Typical values are to be used as a design aid are not subject to production testing.

AC ELECTRICAL CHARACTERISTICS (T_a = 25°C)

Charactistic	Symbol	Min	Typ	Max	Unit	Notes
Oscilator Frequency	F_{OSC}		4		KHz	1
Key Input Debounce Time	T_{DB}		10		ms	3,4
Key Down Time for Valid Entry	T_{KD}	40			ms	4,5
Key Down Time During Two-Key Roll Over	t_{KR}	5			ms	4
Oscillator Stat-Up Time (V_{CC} = 2.5V)	t_{os}		1		ms	
Mute Valid After Last Outpulse	t_{MO}		5		ms	3,4
Pulse Output Pulse Rate	P_R		10		PPS	2
On-Hook Time Required to Clear Memory	t_{OH}	300			ms	4
Pre-Digital Pause	T_{PDP}		800		ms	3,4
Inter-Digital Pause	T_{IDP}		800		ms	3,4
Frequency Stability . V_{CC} = 2.5 ~ 3.5V	Δf		±4		%	
Frequency Stability V_{CC} = 3.5 ~ 6.0V	Δf		±4		%	
Tone Output Frequency	F_{TONE}		1		KHz	4,6

Note: 1) R_S = 2MΩ, R = 220KΩ, C = 390pF.
2) If pin 10 is tied to V_{CC}, the output pulse rate will be 20pps.
3) If the 20pps option is selected, the time will be 1/2 these shown.
4) These times are directly proportional to the oscillator frequency.
5) Debounce plus oscillator start-up time ≤ 40ms.
6) If the 20pps option is selected, the tone output frequency will be 2KHz. (KS5805B ONLY)

PIN CONNECTIONS

Pin 1: V_{CC}
Pin 2: V_{ref} (KS5805A)/Pacifier tone (KS5805B)
Pin 3: $\overline{\text{Column 1}}$
Pin 4: $\overline{\text{Column 2}}$
Pin 5: $\overline{\text{Column 3}}$
Pin 6: GND
Pin 7: RC Oscillator
Pin 8: RC Oscillator
Pin 9: RC Oscillator
Pin 10: 10/20pps Select
Pin 11: Make/Break Select
Pin 12: $\overline{\text{Mute}}$ Output
Pin 13: $\overline{\text{ROW 4}}$
Pin 14: $\overline{\text{ROW 3}}$
Pin 15: $\overline{\text{ROW 2}}$
Pin 16: $\overline{\text{ROW 1}}$
Pin 17: On-Hook/Test
Pin 18: $\overline{\text{Pulse Output}}$

TIMING CHARACTERISTICS

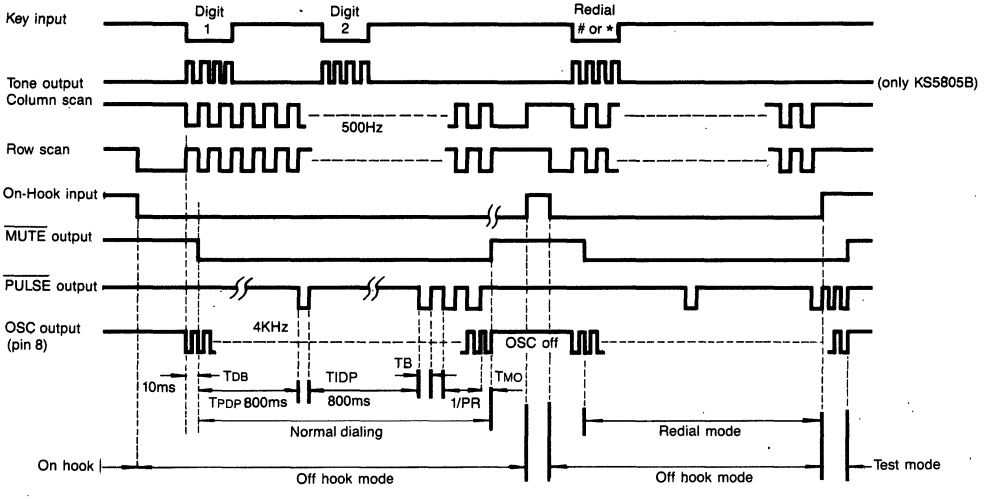


Fig. 2

PIN DESCRIPTIONS

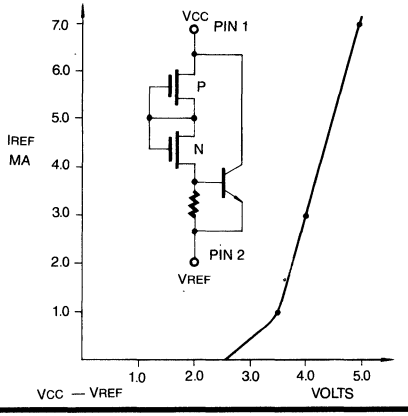
1. V_{CC} (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to Pin 6 and is supplied from a 150μA current source. This voltage must be regulated to less than 6.0 volts using on external form or regulation.

2. Tone signal output/V_{REF} (Pin 2)

Tone signal out pin is CMOS comperementaly output and drive on external bipolar transistor. This pin generates a tone signal when a key is depressed as its recognition. Tone signal frequency is 1KHz when 10pps pulse rate is selected. (the frequency is 2KHz when 20pps pulse rate is selected). Only the pin 2 of KS5805A is V_{REF} (on-chip reference voltage).

TYPICAL I-V CHARACTERISTICS



The V_{REF} output provides a reference voltage that tracks internal parameters of the KS5805A. V_{REF} provides a negative voltage reference to the V_{CC} supply. Its magnitude will be approximately 0.6 volt greater than the minimum operating voltage of each particular KS5805A

The typical application would be to connect the V_{REF} pin to the GND pin (Pin 6). The supply to the V_{CC} pin (Pin 1) should then be regulated to 150μA (I_{OP} max). With this amount of supply current, operation of the KS5805A is guaranteed.

The internal circuit of the V_{REF} function is shown in Figure 3 with its associated I-V characteristic.

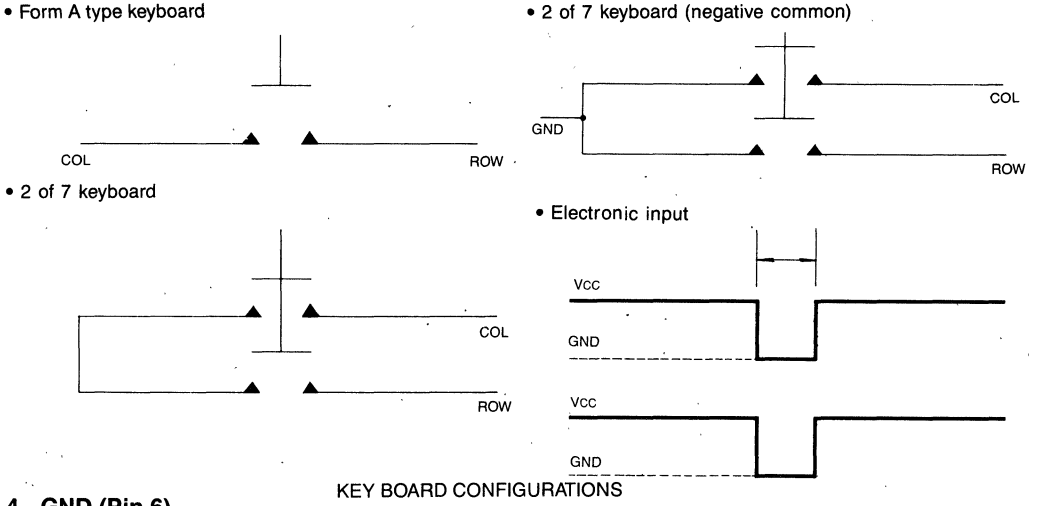
Fig. 3

3. Keyboard inputs (Pin 3, 4, 5, 13, 14, 15, 16,)

The KS5805A/B incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (form A) keyboard to be used.

A valied key entry is defined by either a single row being connected to a single column or GND being simutaneously presented to both a single row and column. When in the on-hook mode, the row and column inputs are held high and no keyboard inputs are accepted.

When off-hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is varied. The input must remain valid continuously for 10msec of debounce time to be accepted.



KEY BOARD CONFIGURATIONS

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

5. OSCILLATOR (Pins 7, 8, 9)

The KS5805A/B contains on-chip inverters to provide an oscillator which will operate with a minimum of external components.

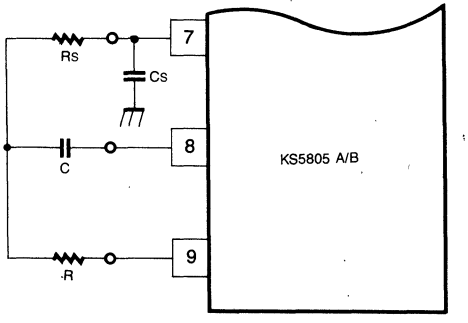
Following figure shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_S/R$ equal to 10.

The oscillator period is given by:

$$T=RC\ (1.386+(3.5KC_S)/C-(\pm K/(K+1))\ \ln\ (K/(1.5K+0.5))$$

Where C_S is the stray capacitance on Pin 7.

Accuracy and stability will be enhanced with this capacitance minimized.



6. 20/10 pps (Pin 10)

Connecting this pin to GND (pin 6) will select an output pulse rate of 10pps.
Connecting the pin V_{CC} (pin 1) will select an output pulse rate of 20pps.

7. MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connecting V_{CC} or GND to this pin as shown in the following table.

Input	Make	Break
V_{CC} (Pin 1)	34%	66%
GND (Pin 6)	40%	60%

8. $\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The mute output is an open-drain N-channel transistor designed to drive an external bipolar transistor.
This circuitry is usually used mute the receiver during outpulsing. As shown in Fig. 2 the KS5805 $\overline{\text{mute}}$ output turns on (pulls to the V_{GND}-supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break.
The delay from the end of the last break until the $\overline{\text{mute}}$ output turns off is mute overlap and is specified as t_{MO}.

9. ON-HOOK/TEST (Pin 17)

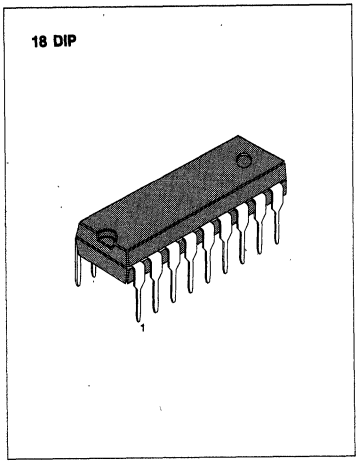
The "ON-HOOK" or "Test" input of the KS5805A/B has a 100KΩ pull-up to the positive supply. A V_{CC} input or allowing the pin to float sets the circuit in its on-hook or test mode while a V_{GND} input sets it in the off-hook or normal mode. When off-hook the KS5805A/B will accept key inputs and outputs the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.
Switching the KS5805A/B to on-hook while it is outpulsing causes the remaining digits to be outpulsed at 100x the normal rate (M/B ratio is then 50/50).
This feature provides a means of rapidly testing the device and is also on efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300msec, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and power-up-clear detect circuitry (refer to the electrical specifications).
Upon retuning off-hook, a negative transistion on the mute output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

10. $\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{pulse}}$ output is an open drain N-channel transistor designed to drive on external bipolar transistor. These transistor would normally be used to pulse the telephone line by disconnecting and connecting the network. The KS5805A/B $\overline{\text{pulse}}$ output is an open circuit during make and pulls to the GND supply during break.

TEN NUMBER REPERTORY DIALER WITH PACIFIER TONE

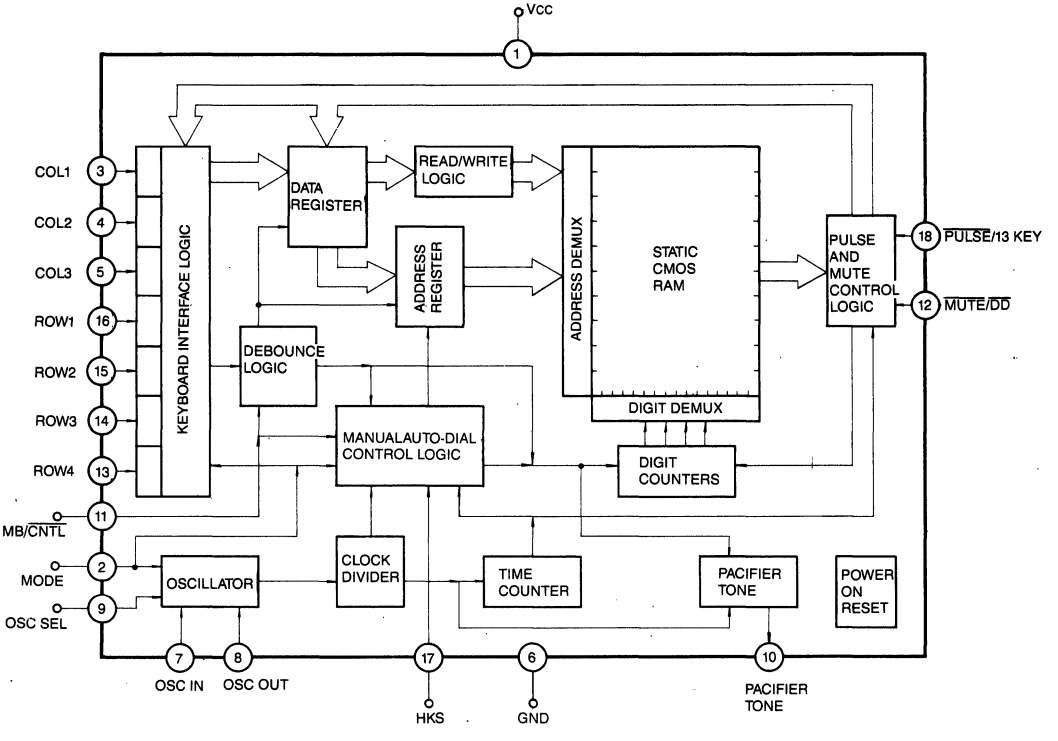
The KS5806 is a monolithic integrated ten-number repertory dialer manufactured using CMOS process. The circuit accepts keyboard inputs and provides the pulse and mute logic levels required for loop disconnect signaling.



FEATURES

- **Low-voltage (2 to 10V) and low power operation**
- **Low memory retention current of 1μ**
- **Auto-dials Ten 16 digit-numbers including Last Number Dialed (LND)**
- **Pacifier Tone Output**
- **Oscillator Selectable in pulse mode (RC or ceramic resonator)**
- **Stand-alone pulse dialer**
- **PABX pause key input**
- **Last number dialed memory**
- **Last number dialed may be copied into any one of nine other locations.**
- **Make/Break ratio is pin selectable in pulse mode**
- **Uses either the inexpensive Form-A type keyboard or the standard 2-of-7 matrix keyboard with common Gnd**
- **Optional use of 13th key input to control repertory functions in tone mode**
- **Power up circuit initializes RAM and logic**

BLOCK DIAGRAM



DESCRIPTION

The KS5806 is a ten-number repertory dialer manufactured using silicon Gate CMOS process. Pin 2, the "Mode select" input determines whether signaling will be pulse or tone. The interpretation of several inputs and outputs is dependent upon the mode selected.

In the pulse mode the time base for the circuit is selectable between a ceramic resonator and RC oscillator. In tone mode the circuit can only use the RC oscillator. An on chip RAM is capable of storing ten 16-digit telephone numbers including the last number dialed.

When used in a PABX system, a pause (# key) may be stored in the number sequence. The repertory dialer will recognize this pause when automatically dialing and stop until another key input is received.

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Caracteristic	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	10.5	V
Maximum Power Dissipation (25°C)	P_D	500	mW
Maximum Voltage on Any Pin	V_{IN}	V_{CC} +0.3, GND−0.3	V
Operating Temperature	T_{opr}	−30 ~ 60	°C
Storage Temperature	T_{stg}	−55 ~ 125	°C

DC ELECTRICAL CHARACTERISTICS

(T_a = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage[1]	V_{CC}		2.0		10.0	V
Operating Current (Tone)[2]	I_{OP}	V_{CC} = 2.5V		50	100	μA
Operating Current (Pulse)[2]	I_{OP}	V_{CC} = 2.5V		100	200	μA
Standby Current (V_{CC} = 2.5V)[3]	I_{SB}	No load		1.0	2.0	μA
Memory Retention Current[1]	I_{MR}			0.3	1.0	μA
Memory Retention Voltage[1]	V_{MR}		1.3	1.5		V
Mute Sink Current[4]	I_{ML}	V_{CC} = 2.5V, V_O = 0.5V	0.5	2.0		mA
Pulse Sink Current[4]	I_P	V_{CC} = 2.5V, V_O = 0.5V	1.0	4.0		mA
Pacifier Tone Source/Sink[4]	I_{PT}	Source V_O = 2.0V	200	500		μA
Mute and Pulse Leakage[5]	I_{LKG}	V_O = 10V		0.001	1.0	μA
Key Contact Resistance[6]	R_{KI}				1.0	KΩ
Keyboard Capacitance[6]	C_{KI}				30	pF
"O" Logic Level	K_{IL}		GND		0.2V_{CC}	V
"I" Logic Level	K_{IH}		0.8 V_{CC}		V_{CC}	V
Keyboard Pull Up[7]	K_{RU}			100		KΩ
Keyboard Pull Down[7]	K_{RD}			1.0		KΩ
CNT Pull Up (Pin 11)[8]	R_{CNT}	Tone mode only		100		KΩ

Notes:

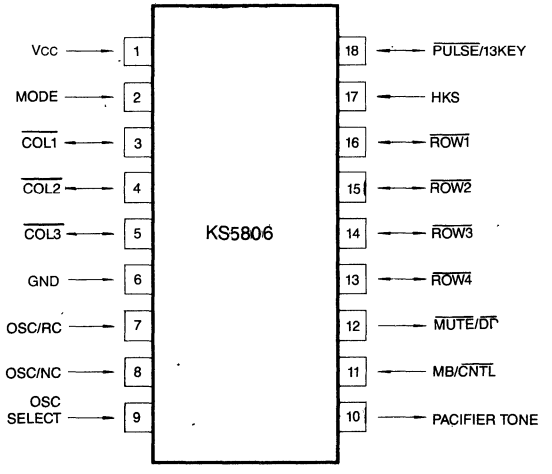
1. The memory will be retained at a lower voltage level than that required for circuit operation. If either I_{MR} or V_{MR} is maintained the memory contents will not be cleared.
2. Operating current with a valid key input at 2.5 volts.
3. Standby current on hook or off hook with all inputs unloaded.
4. For V+ = 2.5, Sink V_O = 0.5 Volts, Source V_O = 2.0 volts.
5. Leakage with V+, V_O = 10.0 Volts
6. Keyboard contact resistance and parasitic capacitance, maximum values.
7. Keyboard I/O pins will scan 250 Hz with oscillator enabled pulse mode and during $\overline{DD}$ in tone mode.
8. Tone mode only.

AC ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator (Cer, Res)[1]	F_{CR}		480		KHz
Oscillator (RC)[2]	F_{RC}		8	16	KHz
Oscillator Stability[3]	ΔF_{RC}	−3		+3	%
Debounce Time[4]	T_{DB}		32		mS
Valid Key Down Time	T_{KD}	40			mS
Oscillator Start Up Time	T_{OS}			8	mS
Key Rollover OVLP Time[5]	T_{ROL}	4			mS
Pulse Rate	P_R		10		PPS
Break Time (Pin 11 V_{CC}/GND)	T_B		60/68		mS
Predigital Pause Time[6]	T_{PDP}		170		mS
Mute Overlap Time	T_{MOL}		2		mS
Tone Rate	T_R		5		TPS
Pacifier Tone Burst Time[7]	T_{PT}		28		mS
Pacifier Tone Frequency[8]	F_{PT}		500		Hz
Interdigital Pause Time	T_{IDP}		940		mS

Notes:
1. Ceramic Resonator should have the following equivalent values: R < 20 Ohms. R_A > 70k Ohms, C_O < 500pF.
2. The RC values chosen determine frequency. The nominal frequency is 8kHz. To accelerate dialing the frequency may be increased to twice the nominal value. This would double signalling rate and half most timing specifications.
3. Voltage range of 2.5 to 6.0 volts, over temperature, and unit to unit variations.
4. Key entry must be present after 32 ms to be valid.
5. Rollover is the time key inputs must be invalid for successive entries to be recognized.
6. Time from initial key input till first break or tone output.
7. Tone burst will terminate if key released before 28 ms.
8. This is a square wave output.

PIN CONNECTION



PIN DESCRIPTION

1. V_{CC} (Pin 1)

Pin 1 is the positive supply input to the part and is measured relative to GND (pin 6). The voltage on this pin should not exceed 10 Volts. On chip Zener diodes will provide protection from supply transients in most applications. A low voltage detect circuit will perform a power up initialization whenever the supply voltage at this pin falls below a level necessary to guarantee proper circuit operation.

2. Mode (Pin 2)

The KS5806 will function in either tone or pulse mode, dependent upon the logic level presented to pin 2. For pulse mode operation, this pin must be tied to GND (pin 6). For tone mode, it should be tied to V_{CC} (pin 1). The interpretation of pins 7,8,11,12, and 18 are dependent upon the mode selected.

3. Keyboard Inputs (Pins 3, 4, 5, 13, 14, 15, 16)

The KS5806 incorporates a keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Fig. 1.

A valid key entry is defined by either a single row being connected to single column or V — being simultaneously presented to both a single row and column.

In the tone mode, the KS5806 features a bidirectional keyboard scheme. As the KS5806 passively monitors the key inputs (using the scan provided by the tone dialer), they are debounced, decoded, and stored in the on chip LND (Last Number Dialed) buffer. The keyboard inputs in tone mode are normally high impedance allowing the tone chip to scan the keyboard lines and begin signaling immediately upon detecting a key entry. A command key entry disables the tone chip and scanning is then controlled by the repertory dialer until the key is released. In tone mode auto-dialing is performed by the KS5806 which simulates key contact closures. The tone generator accepts these inputs as valid keyboard information and generates the proper DTMF frequencies.

In the pulse mode, the KS5806 keyboard inputs are static until an initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. Keyboard bounce is ignored for 32 ms after the initial key down is detected. A key input is accepted if it is valid after this initial debounce time. This scheme guarantees any valid key input to be recognized in less than 40 ms after the initial key closure.

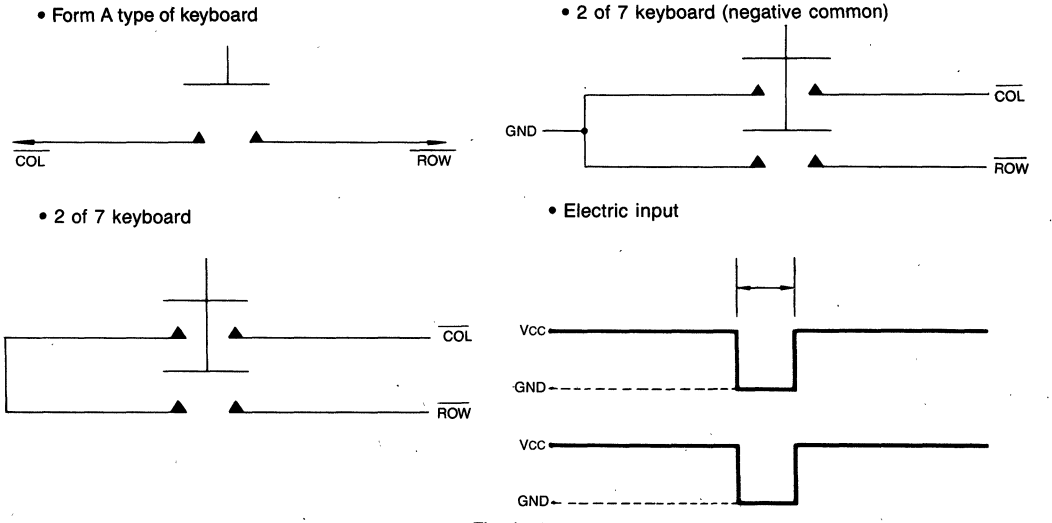


Fig. 1

4. GND (Pin 6)

This is the negative supply pin and is connected to the common part in the general applications.

5. Oscillator. (Pin 7 and Pin 8)

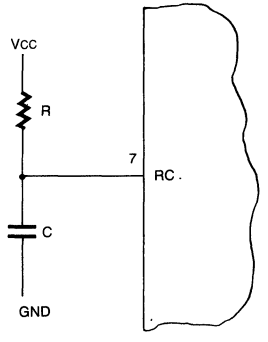
The RC oscillator (Figure 2a) requires a resistor and capacitor to provide the frequency reference for the KS5806. The resistor should be connected from Pin 7 (Osc/RC) to Pin 1 (V_{CC}) and the capacitor from Pin 7 to Pin 6 (GND). Pin 8 should be connected to V_{CC} for normal operation. The nominal frequency for standard operation is 8kHz. This provides for a tone rate of 100ms on and 100ms off and pulse rate of 10pps. The frequency of oscillation is approximated by the equation.

$$F_{OSC} = 1/(1.45\ RC).$$

The value suggested for the capacitor (C) should be 410pF or lower and resistor (R) may be adjusted for the desired signalling rate. 10PPS and 5TPS operation is achieved by selecting a 390 pF capacitor and a 220K Ohm resistor.

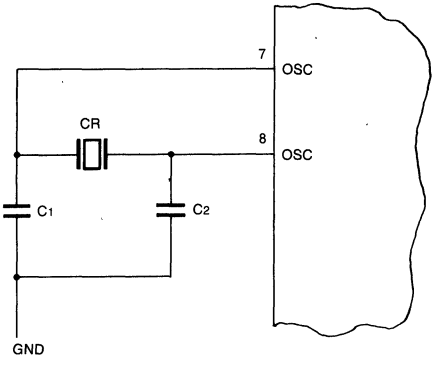
A more accurate and constant frequency reference in pulse mode is obtained using a 480 kHz ceramic resonator as shown in Figure 2b. The ceramic resonator is connected in parallel with an on-chip inverter. Two external capacitors to ground are also required.

a, RC OSC



NOMINAL FREQUENCY 8KHz

b, CERAMIC RESONATOR



FREQUENCY 480 KHz

Fig. 2

6. Oscillator Select. (Pin 9)

This pin determines the mode of oscillation used by the repertory dialer when in pulse mode. The ceramic resonator is chosen by tying this pin to Pin 1 (V_{CC}). The RC oscillator is chosen by tying this pin to Pin 6 (GND).

In tone mode this input must be tied either high or low but it will not affect the mode of oscillation which is always RC. The timing of the repertory dialer is independent of the tone chip which uses a 3.5795 MHz crystal as its frequency reference.

7. Pacifier Tone (Pin 10)

The pacifier tone consists of a burst of a 500 Hz square wave. The burst is initiated with the acceptance of a valid key input (following the debounce time) and terminates after 28ms or with the release of the key, whichever comes first. The output is high impedance when not active.

8. MB/$\overline{\text{CNTL}}$ (Pin 11)

The level on pin 18 determines the control key inputs required to implement the repertory dialer function. In the 13 key tone mode, Pin 18 can be used to "control" the repertory dialer functions of the phone with a momentary SPST switch to the negative supply connected to this input. This feature allows the basic keyboard to operate the same as in a standard telephone and only the closure of the 13th key will initiate a repertory dialer function. The * and # key inputs will be accepted as normal DTMF inputs (however they will not be stored in the LND buffer). In 12 key mode this pin should be connected to the positive supply (V_{CC}).

In pulse mode, the make break ratio may be selected by connecting this pin to either the V_{CC} or GND supply. Table 1 indicates the two ratios available.

9. $\overline{\text{Mute}}$/$\overline{\text{Dialer Disable}}$ (Pin 12)

Pin 12 is the output of an open drain N-channel transistor. In the tone mode, it is used to provide the tone dialer with a $\overline{\text{Dialer Disable}}$ signal which inhibits the generation of tones during command key entries. The timing characteristics in tone mode are shown in Figure 3a.

In the pulse mode, Pin 12 is the $\overline{\text{Mute}}$ output. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. Figure 3b shows the timing characteristics of the $\overline{\text{Mute}}$ output.

MB Input	% Break	% Make
V_{CC}	60	40
GND	68	32

Table 1

10. HKS (Pin 17)

The HKS (hook switch) input determines how the repertory dialer will handle key entries. When in the off-hook state (pin tied to GND) signalling is enabled and all entries will be stored in the LND buffer. A control key input in this state initiates the AUTODIAL function.

In the on-hook state (Pin 17 tied to V_{CC}), the dialer stores key information in the LND buffer as they are entered but will not pulse out or allow the DTMF generator to tone. A control key input is interpreted as a STORE command causing the information present in the LND buffer to be copied into the indicated location.

A hook switch transition terminates all dialer operations immediately and initializes all counters and latches. The dialer is then ready to accept a key entry which will be stored over previous data in the LND buffer.

11. $\overline{\text{Pulse}}$/13Key (Pin 18)

In the tone mode, a V+ level at Pin 18 allows the KS5806 to accept inputs from a control key (n.o. SPST) connected from $\overline{\text{CNTL}}$ (Pin 11) to GND. It is used to initiate all repertory functions. This is referred to as 13 key tone mode. With Pin 18 tied to GND, the KS5806 is set in the 12-key tone mode and the * and # keys are used in control functions. Pulse mode defaults to 12 key mode. Both 12 and 13 key tone modes are discussed in more detail in the Operations section of this data sheet.

In the pulse mode, Pin 18 is the $\overline{\text{Pulse}}$ output. It consists of an open drain N-channel transistor and provides the necessary timing for make, break, interdigital delay, and pulse rate to meet dialer specifications worldwide. The timing characteristics of the Pulse $\overline{\text{output}}$ are shown in Figure 3b.

GENERAL OPERATION

During normal dialing, each digit is stored in the LND (Last Number Dialed) buffer, location 0. The telephone number dialed can be left in this temporary LND buffer for later use or it can be copied into any of the other nine permanent memory locations (1-9).

The wrap-around feature of the buffer allows more than 16 digits to be dialed. Entries following the sixteenth input will be stored beginning with the first buffer location replacing the information originally stored there. Any number of digits may be entered and dialed correctly. In pulse mode, the user should not get more than 15 entries ahead of the digit being pulsed.

Keys entered while auto-dialing in pulse mode will be ignored and not affect the number dialed. In tone mode, if a key is entered while auto-dialing it will interfere with the keyboard outputs generated by the KS5806. The key entry is detected and auto-dialing is interrupted until the key is released. The keyboard entry generates a DTMF signal if valid.

The KS5806 repertory dialer will not store either a * or # entry in the buffer but will allow the tone generator to signal these digits as described below.

12. KEY OPERATION

Normal Dialing

In pulse mode digits 0-9 will result in the pulsing of that digit at the standard rate of 10 pps. If the RC oscillator is utilized this rate can be varied achieving a pulse rate of up to 20pps. The * and # keys enable the repertory functions listed below.

In tone mode operation, digits 0-9 causes the generation of respective DTMF signal. In order to tone a * or # key it must be entered twice. The second entry will generate the desired DTMF tone, although it will not be stored in memory.

Storage

Telephone numbers may be entered into the LND buffer while either on-hook or off-hook. However, the KS5806 must be in the on-hook mode for a number to be copied into a permanent memory location. The LND is copied by entering the key sequence **, followed by the address (1-9) of the desired memory location. This operation requires 300 ms before going off hook or initiating another store and does not change the data in the LND buffer. Information present in the LND buffer when new data is entered is replaced and cannot be recalled.

The storage operation may be performed with the telephone off-hook. If requires the addition of an additional switch providing an excellent "Scratchpad Memory". Numbers may be entered and copied without signalling the line making use of line current rather than battery current. Scratchapd memory is useful whenever the user has a need to record a telephone number such as when calling information.

Automatic Dialing

The automatic dialing function is implemented by going off-hook and entering a *, followed by the address (1-9) of the desired telephone number. Dialing will begin with the release of the address key and can be interrupted by initiating a new redial command or with a transition on the HKS pin. The LND buffer will contain the information last entered. A key sequence of * 0 will cause the last number entered to be redialed. More than one number sequence may be automatically dialed from memory without returning on-hook.

Pause/Continue Entries

The KS5806 has a feature which allows an indefinite pause to be programmed into the first 15 digits of a number sequence by entering a # key at the point in the sequence where a pause is desired. As the number is automatically dialed, the circuit will stop dialing when the pause is encountered. Any key entry, except for a * key, will cause the KS5806 to continue dialing the remainder of the number. If more than one pause was originally programmed into the number sequence, a corresponding number of continue commands must be made in order for the number to be completely dialed.

The continue input will not be recognized until one IDP period following the signalling of the digit preceeding the pause. This is approximately 940 ms in pulse mode and 100 ms in tone mode.

13. KEY MODE OPERATION

Normal Dialing

An additional mode of operation (tone mode only) is the ability to use the entire keyboard for normal signalling such that when any key is depressed once, including * or #, the proper DTMF signal is generated. This feature is activated by connecting Pin 18 to V_{CC}. The repertory dialer functions are then initiated by an extra control key (n.o. SPST) connected from Pin 11 (MB/$\overline{CNTL}$) to GND. This key will be referred to as "C".

Storage

The information in the LND buffer may be "copied" or stored into one of the nine permanent memory locations when the input to HKS is high. The control sequence for this function is C-N. The information will be copied yet leave the LND buffer information intact.

Automatic Dialing

Information stored in any of 10 memory locations may be autodialed by entering C-N when the input to HKS (Pin 17) is low. Autodialing may be initiated immediately following a hookswitch transition, manual key entries, or after the completion of a previous auto-dial number.

Pause/Continue

An indefinite pause may be inserted into the number sequence with a C # entry. This feature is quite useful when dialing through a PABX. When a number sequence with a pause is autodialed, signalling will stop when the pause is reached and will continue only when a valid key input is detected.

TONE MODE TIMING

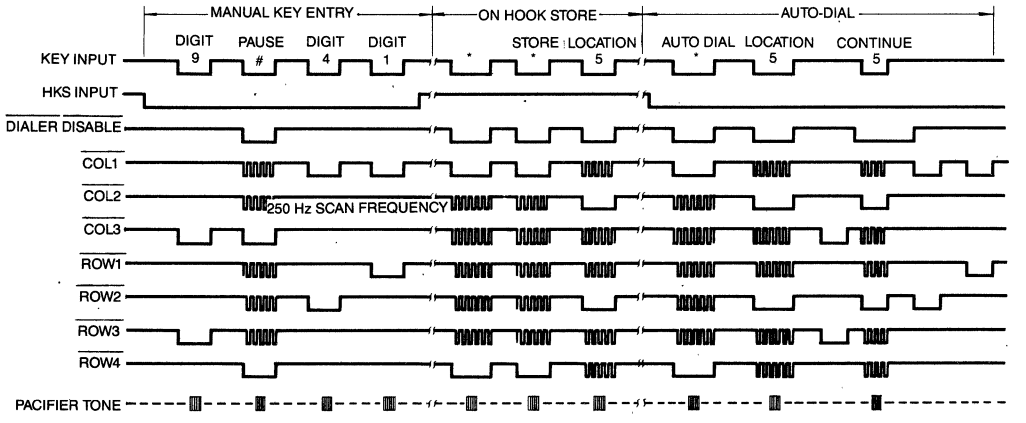


Fig. 3a

PULSE MODE TIMING

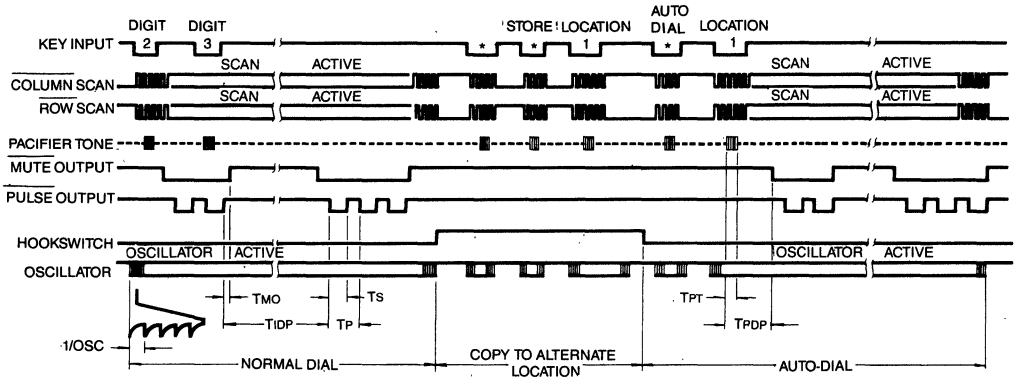
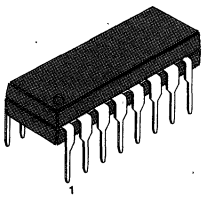


Fig 3b

DUAL TONE MULTI FREQUENCY DIALER

The KS5808 is a monolithic integrated circuit fabricated using CMOS process and is designed specifically for integrated tone dialer applications.

16 DIP



FUNCTIONS

- Fixed supply operation
- Negative-true keyboard input
- Tone disable input
- Stable-output level

FEATURES

- **Minimum number of external parts required.**
- **High accuracy tones.**
- **Digital divider logic, resistive ladder network and CMOS operational amplifier on single chip.**
- **Uses inexpensive 3.579545 MHz television color burst crystal.**
- **Invalid key entry can result in either single tone or no tone.**
- **Tone disable allows any key down output to function from keyboard input without generating tones.**

BLOCK DIAGRAM

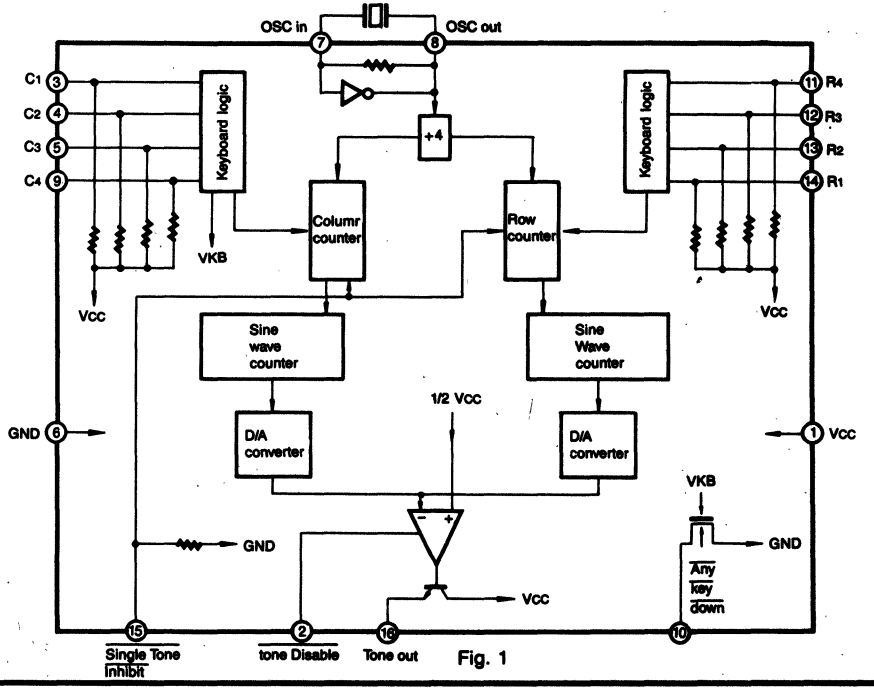


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10.5	V
Any Input Relative to V_{CC} (Except Pin 10)	V_N	0.3	V
Any Input Relative to GND (Except Pin 10)	V_N	−0.3	V
Power Dissipation	P_D	500	mW
Operating Temperature	Topr	−30 ~ +60	°C
Storage Temperature	Tstg	−65 ~ +150	°C

3

ELECTRICAL CHARACTERISTICS

(−30°C < T_a < 60°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		10	V
Input "0"	V_{IL}		0		0.3V_{CC}	V
Input "1"	V_{IH}		0.7V_{CC}		V_{CC}	V
Input Pull-Up Resister	R_I		20		100	KΩ
$\overline{\text{Tone Disable}}$	$\overline{TD}$	Note 4	0		0.3V_{CC}	V
Tone Output	V_{OUT}	Note 1	−10		−7	dBm
Preemphasis, High Band			2.4	2.7	3	dB
Output Distortion, Measured in Terms of Total Out-of-Band Power Relative to RMS sum of Row and Column fundamental Power		Note 2			−20	dB
Rise Time	T_{RISE}	Note 3		2.8	5	mS
$\overline{\text{Any Key Down}}$ Sink Current to GND	I_{AKD}	At V_{OUT} = 0.5V	500			uA
$\overline{\text{ADK}}$ Off Leakage Current	I_{AKDO}	At V_{OUT} = 5V			2	uA
Supply Current Operating	I_{SO}	At V_{CC} = 3.5V Note 6			2	mA
Supply Current Standby	I_{SST}	At V_{CC} = 10V Note 5			200	uA
Tone Output-No Key Down	NKD				−80	dBm

Note: 1. Single-tone, low-group. Any V_{CC} between 3.4V and 3.6V, odBm = 0.775V, R_{LOAD} = 10K see test circuit Fig 2.
2. Any dual-tone. Any V_{CC} between 3.4V to 10.0V.
3. Time from a valid keystroke with no bounce to allow the waveform to go from min to 90% of the final magnitude of either frequency. Crystal parameters defined as R_S = 100Ω L = 96mH, C = 0.02pF, and C_h = 5pF, $V_{CC} \geqq$ 3.4V, f = 3.57954MHz ± 0.02%.
4. Only tones will be disabled when $\overline{TD}$ is taken to logical "0". Other chip functions may activate. Pull-up resistor on $\overline{TD}$ input will meet same spec as other inputs. Logic 0 = GND
5. Stand-by condition is defined as no keys activated, $\overline{TD}$ = Logical 1, $\overline{\text{Single Tone Inhibit}}$ = Logical 0.
6. One key depressed only. Outputs unloaded.

PIN CONNECTIONS

PIN 1: Supply Voltage V_{CC}
PIN 2: $\overline{\text{Tone Disable}}$ Input
PIN 3: $\overline{\text{Column Input}}$ C_1
PIN 4: $\overline{\text{Column Input}}$ C_2
PIN 5: $\overline{\text{Column Input}}$ C_3
PIN 6: GND
PIN 7: OSC IN
PIN 8: OSC OUT
PIN 9: $\overline{\text{Column Input}}$ C_4
PIN 10: $\overline{\text{Any Key Down}}$
PIN 11: $\overline{\text{Row Input}}$ R_4
PIN 12: $\overline{\text{Row Input}}$ R_3
PIN 13: $\overline{\text{Row Input}}$ R_2
PIN 14: $\overline{\text{Row Input}}$ R_1
PIN 15: $\overline{\text{Single Tone Inhibit}}$
PIN 16: Tone Output

Tone Output Test Circuit

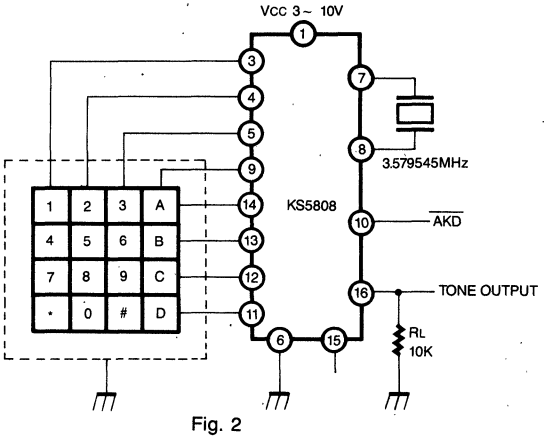


Fig. 2

FUNCTION DESCRIPTION

1. Oscillator

The network contains an on-board inverter with sufficient loop gain to provide oscillation when used with a low cost television color-burst crystal. The inverter's input is osc in (pin 7) and output is osc out (pin 8). The circuit is designed to work with a crystal cut to 3.579545MHz to give the frequencies in table 1. The oscillator is disabled whenever a keyboard input is not sensed.

Table 1: Standard DTMF and output frequencies of the KS5808

Item / Key	f	Standard DTMF Hz	Tone Output Frequency using 3.57954MHz Crystal Hz	Deviation from Standard %
ROW	f1	697	701.3	+0.62
	f2	770	771.4	+0.19
	f3	852	857.2	+0.61
	f4	941	935.1	−0.63
COL	f5	1209	1215.9	+0.57
	f6	1336	1331.7	−0.32
	f7	1477	1471.9	−0.35
	f8	1633	1645.0	+0.73

Most crystals don't vary more than 0.02%. Any crystal frequency deviation from 3.5795MHz will be reflected in the tone output frequency.

2. Output Waveform

The row and column output waveforms are shown in Figure 3. These waveforms are digitally synthesized using on-chip D/A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less. The on-chip operational amplifier of the KS5808 mixes the row and column tones together to result in a dual-tone waveform.

Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be -30dB down when referenced to the strongest fundamental (column tone). Figures 6 and 7 show a typical dual tone waveform and its spectral analysis.

Typical Sinewave Output

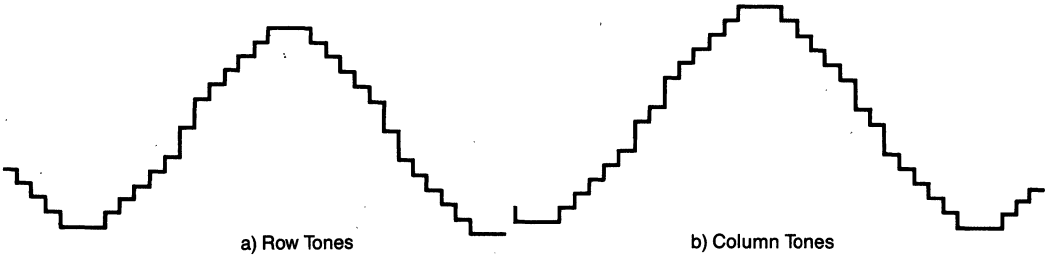


Fig. 3

3. Output Tone Level

The output tone level of the KS5808 is proportional to the applied DC supply voltage. Operation will normally be with a requlated supply. This results in enhanced temperature stability, since the supply voltage may be made temperature stable.

4. Keyboard Configuration

Each keyboard input is standard CMOS with a pull-up resistor to V_{CC}. These inputs may be controlled by a keyboard or electronic means. Open collector TTL or standard CMOS (operated off same supply as the KS5808) may be used for electronic control.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1KΩ as a valid key closure.

2 of 8 DTMF keyboard

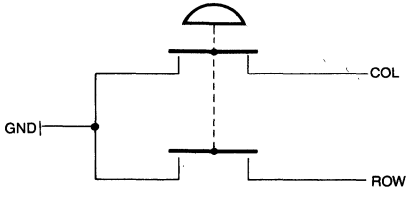


Fig. 4

Electronic Input Pulses

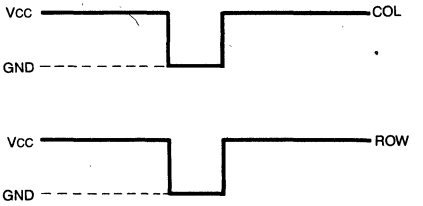


Fig. 5

TYPICAL DUAL TONE WAVEFORM

(ROW 1, Column 1)

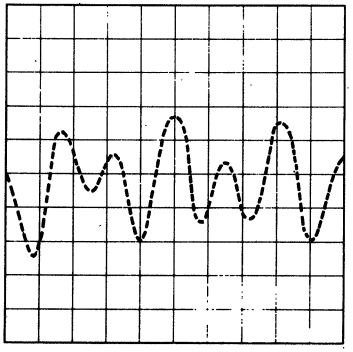


Fig. 6

SPECTRAL ANALYSIS OF WAVEFORM

(Vert: 10dB/Div, Hori: 1KHz/Div)

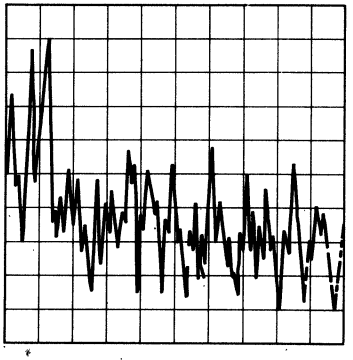


Fig. 7

POWER DISSIPATION VERSUS TEMPERATURE

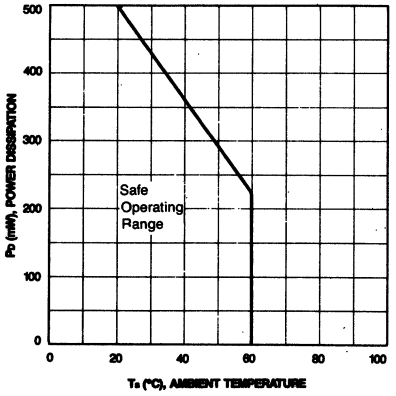


Fig. 8

PIN DESCRIPTIONS

1. Row and Column Input (Pin 3, 4, 5, 9, 11, 12, 13, 14)

With Single Tone Inhibit at V_{CC}, connection of GND to a single column will cause the generation of that column tone. Connection of GND to more than one column will result in no tones being generated. The application of GND to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to GND for row tones to be generated. If a single row tone is desired, it mey be generated by tying any two column pins and the desired row pin to GND. Dual tones will be generated if a single row pin and a single column pin are connected to GND.

2. Any Key Down Output (Pin10)

The any key down output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to GND when a keyboard button is pushed and is open circuited when not. The AKD output switches regardless of the tone disable and single tone inhibit inputs.

3. Tone Disable Input (Pin 2)

The Tone Disable input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaing. It has a pull-up to V_{CC} and when tied to GND tones are inhibited. All other chip functions operate normally.

4. Single Tone Inhibit Input (Pin 15)

The Single Tone Inhibit input is used to inhibit the generation of other than dual tones. It has a pull-down to GND and when floating or tied to GND, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

When forced to V_{CC} single or dual tones may be generated as described in the paragraph under row and column inputs.

5. Tone Output (Pin 16)

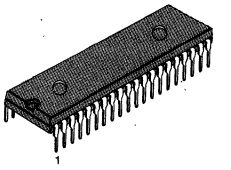
The tone output pin is connected internally in the KS5808 to the emitter of an NPN transistor whose collector is tied to V_{CC}. The input to this transistor is the on-chip operational ampifier which mixes the row and column tones together and provides output level regulation.

QUAD UNIVERSIAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5812, QUAD-UART, is a Si-Gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main system and subsystems.

The parallel data of the bus system is serially transmitted and by the asynchronous data interface with proper formatting and error checking. The KS5812 includes Transmit part, Receive part, Programmable control part, Status check part, and Select part. The control register that is programmed via the data bus during system initialization, provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control.

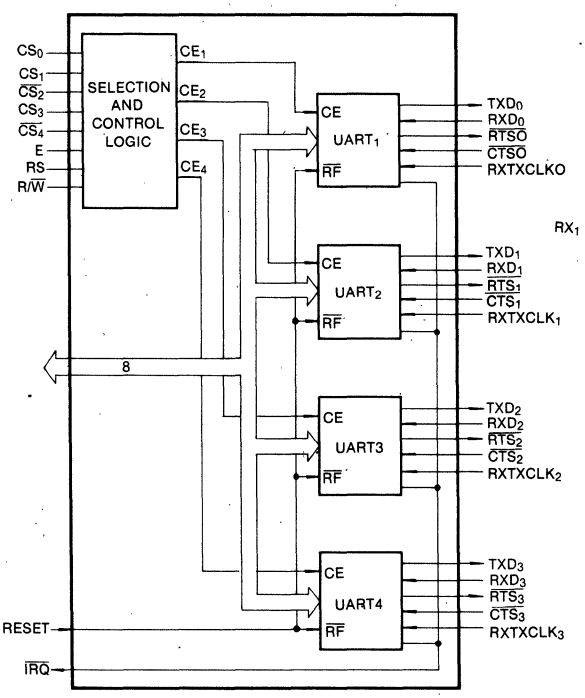
40 DIP



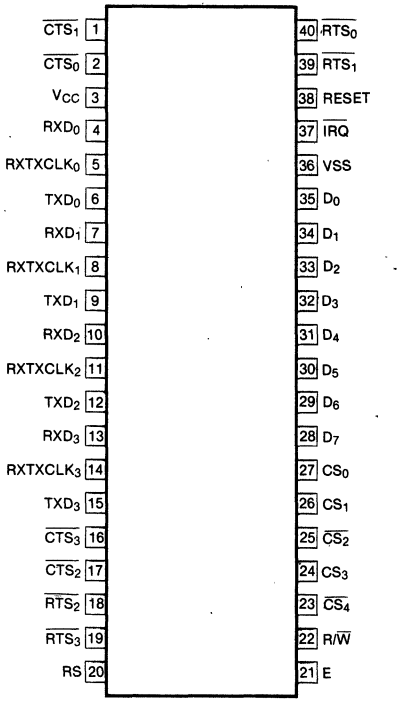
FEATURES

- **Low power, High speed CMOS process.**
- **Serial/Parallel conversion of Data**
- **8-and 9-bit Transmission**
- **Optional Even and Odd Parity**
- **Parity, Overrun and Framing Error Checking**
- **Programmable Control Register**
- **Optional ÷1, ÷16, and ÷64 Clock Modes**
- **Peripheral/Modern Control Functions**
- **Double Buffered**
- **One-or Two-Stop Bit Operation**

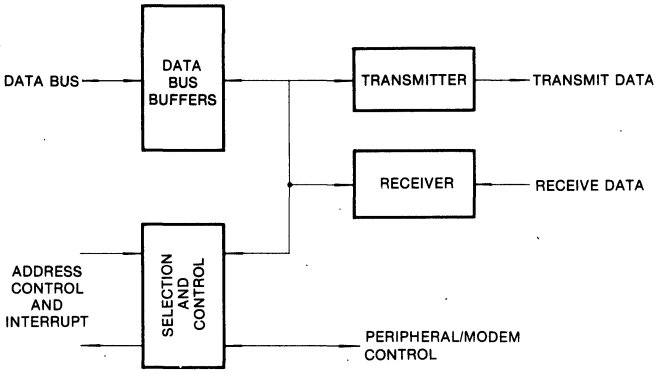
BLOCK DIAGRAM



PIN CONFIGURATION



UART BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{In}	−0.3 to 7.0	V
Maximum Output Current**	I_C	10	mA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

*With respect to V_{SS} (System GND)

**Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal ($D_0 \sim D_7$, $\overline{RTS}$, Tx Data, $\overline{IRQ}$)

(Note) Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions are exceeded, it could affect reliability of IC.

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	$D_0 \sim D_7$, RS, $\overline{CTS_i}$, RxD_i	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1 R/$\overline{W}$, E, CS_3, $\overline{CS_4}$, $RXTXCLK_i$		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (System GND)

DC CHARACTERISTICS (V_{CC} = +5V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	$D_0 \sim D_7$, RS, CTSi,	V_{IH}		2.0	—	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, CS_3, $\overline{CS_4}$ RXTXCLKi			2.2	—	V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3	—	0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, $\overline{CS_2}$, E, CS_3, $\overline{CS_4}$	I_{IN}	V_{IN} = 0 ~ V_{CC}	−2.5	—	2.5	μA
Three-State (Off State) Input Current	$D_0 \sim D_7$	I_{TSI}	V_{IN} = 0.4 ~ V_{CC}	−10	—	10	μA
Output "High" Voltage	$D_0 \sim D_7$	V_{OH}	I_{OH} = −400μA	4.1	—	—	V
			$I_{OH} \leq$ −10μA	V_{CC}-0.1	—	—	
	TXDi, $\overline{RTSi}$		I_{OH} = −400	4.1	—	—	
			$I_{OH} \leq$ −10μA	V_{CC}-0.1	—	—	
Output "Low" Voltage	All outputs	V_{OL}	I_{OH} = 1.6mA	—	—	0.4	V
Output Leakage Current (off state)	$\overline{IRQ}$	I_{LOH}	V_{OH} = V_{CC}	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_{IN}	V_{IN} = 0V, Ta = 25°C f = 1.0 MHz	—	—	12.5	pF
	E, RXTXCLKi, R/$\overline{W}$, RS, RXDi, CS_0, CS_1, $\overline{CS_2}$, CTS, CS_3, $\overline{CS_4}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, TXDi	C_{out}	V_{IN} = 0V, Ta = 25°C f = 1.0 MHz	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Supply Current	• Under transmitting and Receiving operation • 500 kbps • Data bus in R/$\overline{W}$ operation	I_{CC}	E = 1.0 MHz	—	—	3	mA
			E = 1.5 MHz	—	—	4	
			E = 2.0 MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = V_{CC} − 0.8V V_{IL} max = 0.8V		E = 1.0 MHz	—	—	200	μA
			E = 1.5 MHz	—	—	250	
			E = 2.0 MHz	—	—	300	

AC CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	KS5812 Min	KS5812 Max	Unit
Minimum Clock Pulse Width	÷1 Mode	PW_{CL}	Fig. 1	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	PW_{CH}	Fig. 2	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_C		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	—	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDSU}	Fig. 4	250	—	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	Fig. 5	250	—	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	—	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	—	560	ns
Rise Time and Fall Time	Except E	t_r, t_f		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	KS5812 Min	KS5812 Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 7	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	—	ns
Data Delay Time	t_{DDR}	Fig. 7	—	290	ns
Data Hold Time	t_H	Fig. 7	20	100	ns
Address Hold Time	t_{AH}	Fig. 7	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	KS5812		Unit
			Min	Max	
Enable Cycle Time	$t_{cyc}E$	Fig. 8	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	—	ns
Data Setup Time	t_{DSW}	Fig. 8	165	—	ns
Data Hold Time	t_H	Fig. 8	10	—	ns
Address Hold Time	t_{AH}	Fig. 8	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	—	25	ns

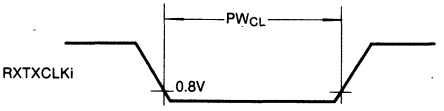


Fig. 1 Clock Pulse Width, "Low" State

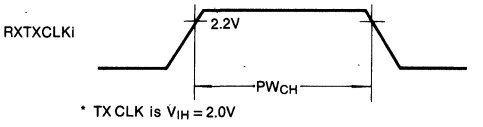


Fig. 2 Clock Pulse Width, "High" State

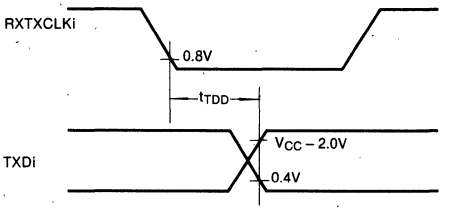


Fig. 3 Transmit Data Output Delay

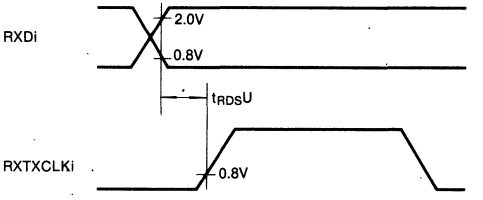


Fig. 4 Receive Data Setup Time (÷1 Mode)

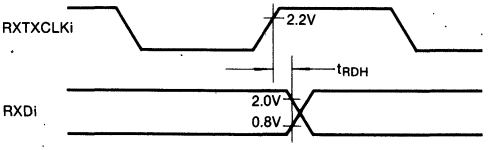
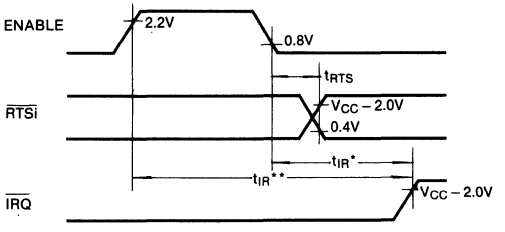


Fig. 5 Receive Data Hold Time (÷1 Mode)



* (1) $\overline{IRQ}$ Release Time applied to R_XDi Register read operation
(2) $\overline{IRQ}$ Release Time applied to T_XDi Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_X Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by DCD rising edge.

Note: Note that following take place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTSi}$ goes "High". (Refer to Figure 14)

Fig. 6 $\overline{RTSi}$ Delay and $\overline{IRQ}$ Release Time

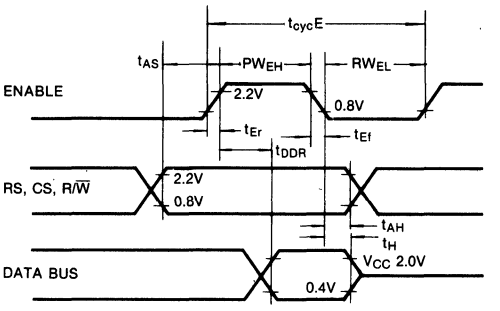


Fig. 7 Bus Read Timing Characteristics (Read information from UART)

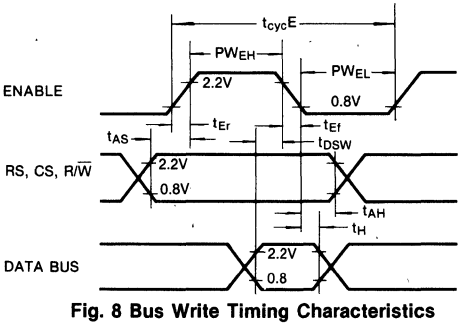


Fig. 8 Bus Write Timing Characteristics (Write information into UART)

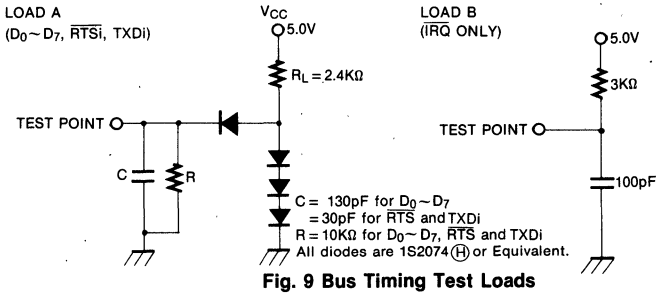


Fig. 9 Bus Timing Test Loads

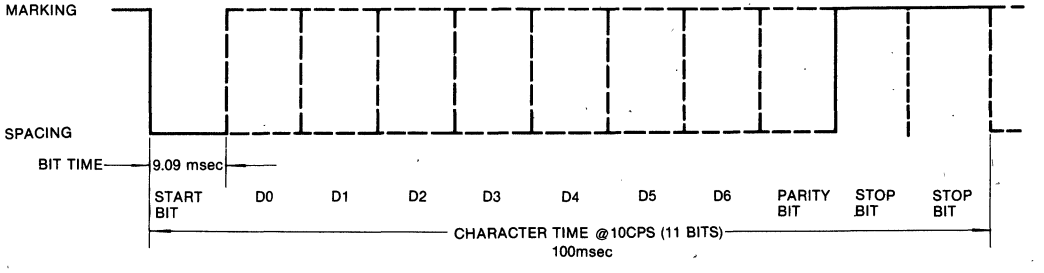


Fig. 10 110 Baud Serial ASCII Data Timing

DEVICE OPERATION

At the bus interface, the UARTi appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UARTi functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTSi}$ outputs are held at level 1. On all other master resets, the $\overline{RTSi}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTSi}$ whenever master reset is utilized. The UARTi also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UARTi. After master resetting the UARTi, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the UARTi. Status Register either as a result of an interrupt or in the UARTi's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the Register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divid-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UARTi bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

UART INTERFACE SIGNALS FOR MPU

The KS5812 interfaces to the MPU with an 8-bit bidirectional data bus, five chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5812.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5812 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UARTi read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus

input/output data buffers and clocks data to and from the KS5812.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UARTi's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5812 output drivers are turned on and a selected register is read. When it is low, the KS5812 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5812.

Chip Select (CS0, CS1, $\overline{CS2}$, CS3, $\overline{CS4}$) — These five high-impedance TTL-compatible input lines are to select and address the KS5812. Each UART can be enabled when $\overline{CS2}$ and CS3 are high and $\overline{CS4}$ is low. CS0 and CS1 are used to select individual UART.

CS0	CS1	CS2	CS3	CS4	UARTi
0	0	1	1	0	UART1
0	1	1	1	0	UART2
1	0	1	1	0	UART3
1	1	1	1	0	UART4

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the KS5812 is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UARTi. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•$\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTSi}$) being high or the UARTi being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTSi}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UARTi. Interrupts caused by Overrun is cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UARTi. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

High-impedance TTL-compatible inputs is provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

RECEIVE AND TRANSMITTER CLOCK (RXTXCLKi)

—The RXTXCLKi input are both used for the clocking of transmitted data and for synchronization of received data. (In the /1 mode, the clock and data must be synchronized extenally.) The transmitter initiates data on the negative transition of the clock and the receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (RXDi) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (TXDi) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The UARTi includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTSi}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTSi}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTSi}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTSi}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UARTi has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UARTi and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UARTi is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

CONTROL REGISTER

The UARTi Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UARTi. Additionally, these bits are used to provide a master reset for the UARTi which clears the Status Register (except for external conditions on $\overline{CTSi}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UARTi. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTSi}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTSi}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTSi}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTSi}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTSi}$ = low, Transmits Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Receive Data Register Full Overrun.

STATUS REGISTER

Information on the status of the UARTi is available to the MPU by reading the UARTi Status Register. This read only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the

status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UARTi

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

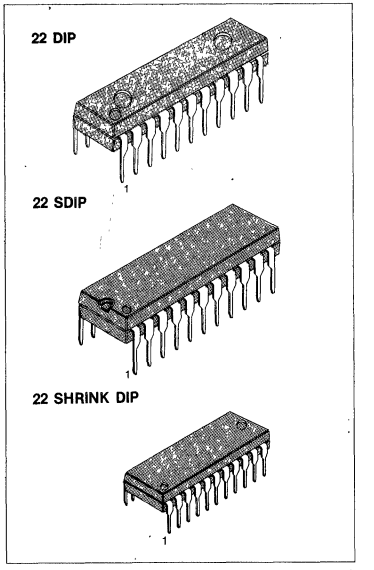
Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the HDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

TONE/PULSE DIALER WITH REDIAL

The KS5819/21 is a DTMF/PULSE switchable dialer with a 32-digit redial memory. Through pin selection, switching from pulse to DTMF mode can be done using slide switch or by depressing [T] key. All necessary dual-tone frequencies are derived from a 3.579545MHz TV crystal, providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7%). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet telephone industry specifications. CMOS technology is used to produce this device, resulting in very low power requirements high noise immunity, and easy interface to a variety of telephones requiring few external components.



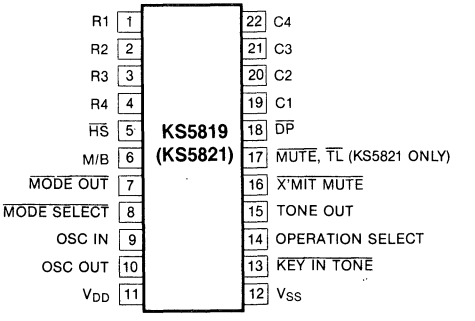
FEATURES

- **Tone/Pulse switchable (touch key or slide switch).**
- **32 digit capacity for redial**
- **Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause**
- **Key-in-tone output for valid key entry in pulse mode (Fkf = 1.8KHz, Tkf = 25mS).**
- **Low power CMOS process (2.0 to 5.5V)**
- **Numbers dialed Manually after redial are cascadable and stored as additional numbers for next redialing**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio (33 1/3~66 2/3 or 40/60) pin selectable**
- **Touch key hooking (580ms)**
- **Low standby current**
- **KS5821 Includes Telephone Locking Function**

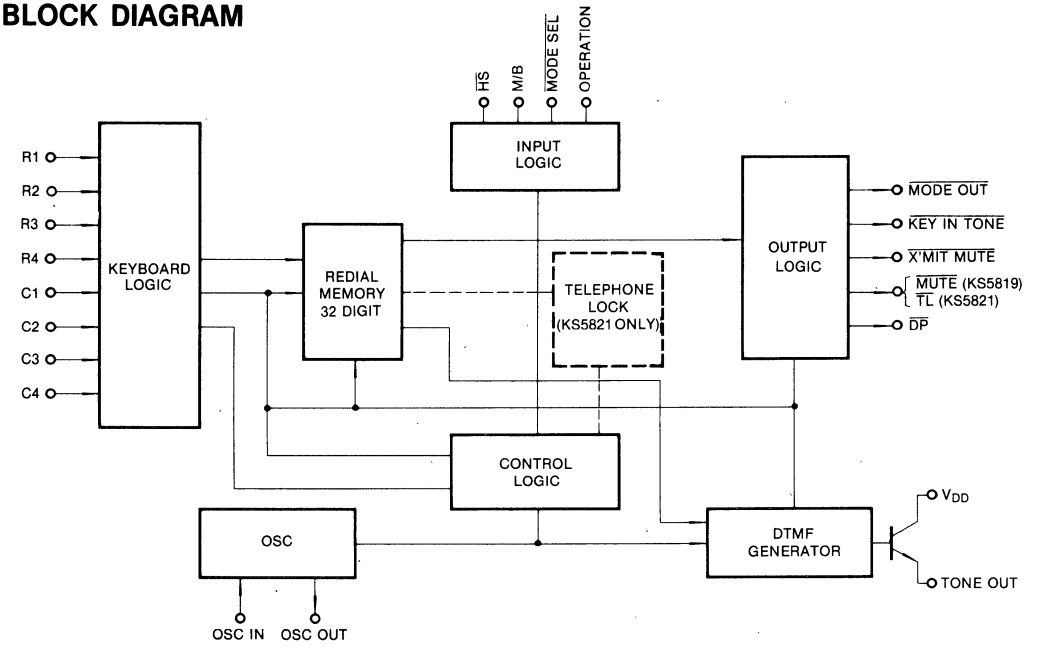
ORDERING INFORMATION

Package	KS5819	KS5821	Dial Pulse	PPS
300mil Width Normal Size	KS58A19N	KS58A21N	DP	10
	KS58B19N	KS58B21N	DP	20
	KS58C19N	KS58C21N	$\overline{DP}$	10
	KS58D19N	KS58D21N	$\overline{DP}$	20
400mil Width Size	KS58A19E	KA58A21E	DP	10
	KS58B19E	KA58B21E	DP	20
	KS58C19E	KA58C21E	$\overline{DP}$	10
	KS58D19E	KA58D21E	$\overline{DP}$	20
Shrink Package Type	KS58A19P	KA58A21P	DP	10
	KS58B19P	KA58B21P	DP	20
	KS58C19P	KA58C21P	$\overline{DP}$	10
	KS58D19P	KA58D21P	$\overline{DP}$	20

PIN CONFIGURATION



BLOCK DIAGRAM



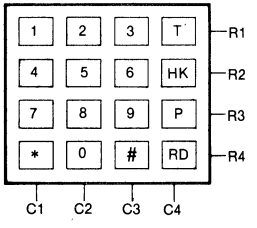
TONE DURATION & PAUSE IN REDIAL

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	74	mS
Minimum Pause	ITP	110	mS
Cycle Time	T_C	184	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.7	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35

ARRANGMENT OF KEYBOARD



T : PULSE-DTMF SWITCHING
HK : HOOKING (580ms)
P : PAUSE (3.6 second)
RD : REDIAL

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	1.2	V
Tone Output Current	I_{TONE}	50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, fx'tal = 3.579545MHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
Operating Voltage Range	$V_{DD}P$	Pulse Mode	All inputs connected to V_{DD} or V_{SS}		2.0		5.5	V
	$V_{DD}T$	Tone Mode			2.0		5.5	
Memory Retention Voltage	V_{DR}				1.0			V
Operating Supply Current	$I_{DD}P$	$\overline{MODE} = V_{DD}$	One key selected $\overline{HS} = V_{SS}$. All outputs unloaded			0.4	1.0	mA
	$I_{DD}T$	$\overline{MODE} = V_{SS}$				1.0	2.0	
Standby Current	$I_{SD}1$	$\overline{HS} = V_{DD} = 1.5V$	No key selected. All outputs unloaded			0.03	0.05	μA
	$I_{SD}2$	$\overline{HS} = V_{SS}$				70	140	
Output Current	$I_{OL}1$	$\overline{DP}$, $\overline{MUTE}$	$V_{OL} = 0.4V$	$V_{DD} = 3.5V$	1.7	5.0		mA
	$I_{OL}2$	$\overline{XMUTE}$, $\overline{TL}$(KS5821)		$V_{DD} = 2.5V$	0.5	1.5		
Input Leakage Current	I_{OFF}	$\overline{MODE\ OUT}$, $\overline{KT}$	$V_{OUT} = 2.5V$				1.0	μA
Input Voltage	V_{IH}	R1-R4, C1-C3, $\overline{HS}$, M/B			$0.8V_{DD}$		V_{DD}	V
	V_{IL}	OPERATION SELECT, $\overline{MODE\ SELECT}$			V_{SS}		$0.2V_{DD}$	
Input Current	$I_{IN}1$	$V_{DD} = 3.5V$ $V_{IN} = 0V$	R1-R4			116		μA
	$I_{IN}2$	$V_{DD} = 2.5V$ $V_{IN} = 0V$				50		
Valid Key Entry Time	T_{kd}				23		25.3	mS
Column and Row Scanning Frequency	F_{cr}					445		Hz
Key-In Tone Output Duration	T_{kt}					23		mS
Key-In Tone Frequency	F_{kt}					1.8		KHz
Auto Access Pause Time	T_{ap}					3.6		sec
Tone Output	V_{or}	$V_{DD} = 2.5V$, $R_L = 5K$	ROW TONE ONLY		−16.0		−12.0	dBV
		$V_{DD} = 3.5V$ $R_L = 5K$			−14.0		−11.0	
Ratio of Column to Row Tone	dB_{cr}	$V_{DD} = 3.5V$			1.0	2.0	3.0	dB
Distortion	%DIS	$V_{DD} = 3.5V$					10	%
Tone Output Delay Time	T_{psd}					1.5		mS

PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>1-4
15-22</td><td>R1-R4
C1-C4</td><td>Keyboard (R1, R2, R3, R4, C1, C2, C3, C4)
These inputs can be interfaced to an XY matrix keyboard. $C_1 \sim C_4$ & $R_1 \sim R_4$ are set to low at On Hook ($\overline{HS}$ = high). $C_1 \sim C_4$ key inputs are set to low and R1-R4 are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-input operation. Oscillator starts running when a key press is detected.
Scanning signals are presented at both column and row inputs (TYP: 445Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 23mS).</td></tr>
<tr><td>5</td><td>$\overline{HS}$</td><td>Hook Switch
This input detects the state of the hook switch contact.
"Off Hook" corresponds to V_{SS} condition.
"On Hook" corresponds to V_{DD} condition.</td></tr>
<tr><td>6</td><td>M/B</td><td>Make/Break Ratio
This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS}.</td></tr>
<tr><td>7</td><td>$\overline{\text{MODE OUT}}$</td><td>Mode Output
This output indicate whether the chip is operating in pulse or tone mode. Pulse/Tone mode corresponds to OFF/ON state (N channel open drain). Mode state is controlled with Operation Select, $\overline{\text{Mode Select}}$ and [T] key inputs.</td></tr>
<tr><td>8</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input
Pulse/DTMF mode is selected as shown in the following table.
Initial Mode means the state after going Off Hook ($\overline{HS} \rightarrow$ "V_{SS}")
<table>
<tr><th>OPERATION SELECT</th><th>$\overline{\text{MODE SELECT}}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th><th>NOTES</th></tr>
<tr><td rowspan="2">V_{DD}</td><td>V_{DD}</td><td>Pulse</td><td>[T] Key-In</td><td rowspan="2">$\overline{\text{MODE SELECT}}$ defines only initial mode after going Off Hook and is latched at first key entry.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
<tr><td rowspan="2">V_{SS}</td><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ input = V_{SS}</td><td rowspan="2">[T] key is disabled under this condition.</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table>
If choice of switching method is desired (either [T] key or $\overline{\text{MODE SELECT}}$). Operation select should be connected to $\overline{\text{MODE SELECT}}$ in order to avoid false operation.</td></tr>
<tr><td>9
10</td><td>OSC IN
OSC OUT</td><td>Oscillator Input/Output
These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF single are finished.</td></tr>
<tr><td>11
12</td><td>V_{DD}
V_{SS}</td><td>Power
These are the power supply inputs. This device is designed to operate on 2.0V to 5.5V.</td></tr>
</table>

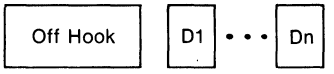
PIN DESCRIPTION (Continued)

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>13</td><td>$\overline{\text{KEY IN TONE}}$</td><td>Key In Tone Output
Key in tone signal is provided only in pulse mode for all Key-ins except [T] key-in. No $\overline{\text{KEY IN TONE}}$ generated in DTMF mode. Fkt: 1.8KHz, Tkt: 23mS.
(N channel open drain)</td></tr>
<tr><td>14</td><td>OPERATION SELECT</td><td>Operation Select Input
Mode switching (from Pulse to DTMF) entry is selectable with this input, i.e. whethere [T] key entry or $\overline{\text{MODE SELECT}}$ input entry is selectable via this pin.</td></tr>
<tr><td>15</td><td>TONE OUT</td><td>DTMF Signal Output
When a valid keypress is detected in DTMF mode Appropriate low group and high group frequencies are generated which hybrided the Dual Tone Output. Tone out is Off State in pulse mode.</td></tr>
<tr><td>16</td><td>$\overline{\text{X'MIT MUTE}}$</td><td>X'mit Mute Output
<table>
<tr><th>$\overline{\text{HS}}$</th><th>$\overline{\text{X'mit Mute Output}}$</th></tr>
<tr><td>V_{DD}</td><td>"OFF"</td></tr>
<tr><td>V_{SS}</td><td>Normally "OFF"
"ON" during pulse and DTMF dialing</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>17</td><td>$\overline{\text{MUTE}}$
$\overline{\text{TL}}$ (KS5821)</td><td>$\overline{\text{Mute Output/Telephone Lock Output}}$ (KS5821)
<table>
<tr><th>$\overline{\text{HS}}$ (KS5819)
Telephone (KS5821)</th><th>$\overline{\text{MUTE OUTPUT}}$ (KS5819)
Telephone Lock Output (KS5821)</th></tr>
<tr><td>V_{DD}
Locked (KS5821)</td><td>OFF (KS5819)
ON (KS5821)</td></tr>
<tr><td>V_{SS}
Unlocked (KS5821)</td><td>Normally "OFF" in DTMF mode.
"ON" during pulse dialing (KS5819)
Normally "OFF" (KS5821)</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>18</td><td>$\overline{\text{DP}}$, DP</td><td>Dial Pulse Out. $\overline{\text{DP}}$: C/D, DP: A/B</td></tr>
</table>

KEYBOARD OPERATION

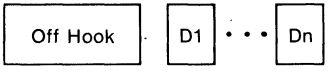
1. SINGLE MODE OPERATION

- **Pulse Mode Operation**

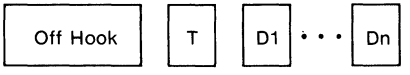


Pulse mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This is the condition under $\overline{\text{Mode Select}} = V_{DD}$.

- **Tone Mode Operation**

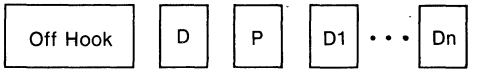


Tone mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This condition is under $\overline{\text{Mode Select}} = V_{SS}$.



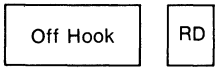
If initial mode is at pulse mode after going Off Hook and $\overline{\text{Mode Select}} = V_{DD}$, Operation Select $= V_{DD}$. Switching mode from pulse to tone can be done by [T] key entry and latched at [D1] key entry.

- **Manual Dialing with Automatic Access Pause**



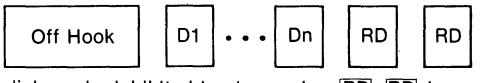
Multiple Pause key entries can be accepted and stored in the redial memory, each as on digit. Each [P] key provides 3.5 seconds pause time, but [P] key entry as first digit after going Off Hook is ignored. [*] key can also be used as pause key in pulse mode. Pause (s) can be cancelled with [P], [T] or [RD] key during pause time in redialing. [D] = Any numeric key.

- **Redialing**



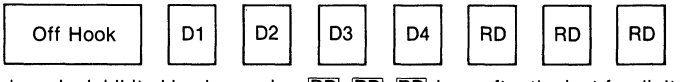
Up to 32 digits can be dialed with [RD] key. [RD] key is disabled while pulse or DTMF signals are transmitting. When more then 32 digits are stored in redial memory. Redial is also inhibited.
[#] key can be used as [RD] key in pulse mode.

- **Inhibiting Redial**



Redial can be inhibited by depressing [RD] [RD] keys after DTMF or pulse signals are transmitted.

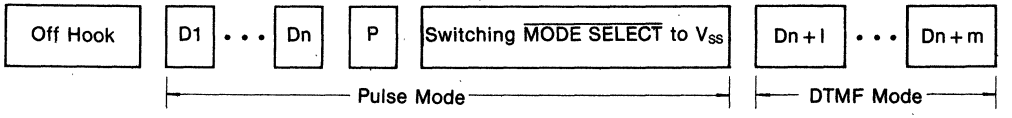
- **Inhibiting Dial (KS5821 only)**



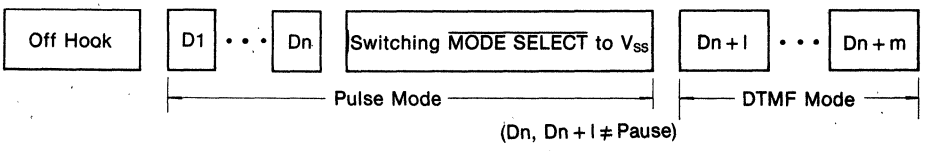
Dial can be inhibited by depressing [RD] [RD] [RD] keys after the just for digit keys's signals are transmitted. You must remember the four digit keys to release the Lock State. If you want to release the Lock State, you must depress [D1] [D2] [D3] [D4] keys which are the same sequence as the four digit keys. Otherwise, You must apply ⌐ (rising edge pulse) to the M/B input.

2. PULSE/TONE SWITCHABLE OPERATION

• **Mode Switching by $\overline{\text{MODE SELECT}}$ Input (OPERATION SELECT = V_{SS})**

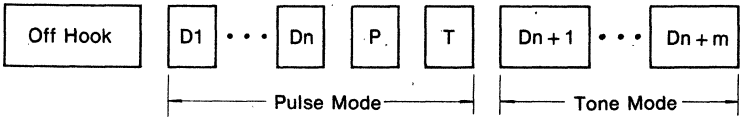


Pulse mode is initially defined $\overline{\text{MODE SELECT}} = V_{DD}$, mode switching to DTMF can be accepted by $\overline{\text{MODE SELECT}} = V_{SS}$, DTMF mode will be set up after pulse mode is finished. In this mode, digits [Dn+l] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys.
If no [P] key is contained serially before or after mode switching.

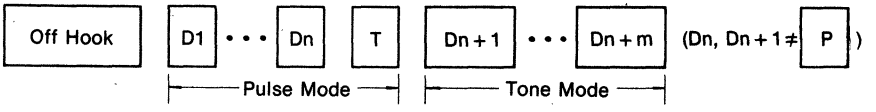


It results the next condition.
If digit [Dn+1] is depressed after pulse mode is finished, DTMF mode will be set up after last pulse signal (Dn) is output. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys. If digit [Dn+1] is depressed during dialing pulse signals. DTMF mode but in Hold State will be set up after last pulse signal [Dn] is finished. MODE OUT will flash to indicate this Hold State [Dn+1] ... [Dn+m] are stored in redial memory as DTMF data and not transmitted from Tone Out. When it is ready to transmit DTMF data in redial memory, [T], [RD] or [P] keys is depressed to reset this Hold State and [Dn+1] ... [Dn+m] data are serially transmitted.

• Mode Switching by [T] key (OPERATION SELECT = V_{DD})



Pulse mode is initially defined with $\overline{\text{MODE SELECT}} = V_{DD}$. Mode switching to DTMF can be accepted by [T] key. In DTMF mode, digits [Dn+1] ... [Dn+m] are transmitted from Tone Out as DTMF signals by depressing corresponded key. If no [P] key is contained serially before or after [T] key.



It results the next condition:
If digit [Dn+1] is depressed after pulse mode is finished DTMF mode will be set up after last pulse signal [Dn] is out. In this mode, digits [Dn+1] ... [Dn+m] are transmitted from TONE OUT as DTMF signals by depressing corresponded key.

If digit [Dn+1] is depressed during dialing pulse signal. DTMF mode but in Hold State will be set up after last pulse signal [Dn] is finished. When DTMF MODE is set up. MODE OUT will be flash to indicate this Hold State. Digits [Dn+1] ... [Dn+m] are stored in redial memory as DTMF data and not transmitted from Tone Out.
When it is ready to transmit DTMF data in redial memory, [T], [RD] or [P] keys is depressed to reset this Hold State and [Dn+1] ... [Dn+m] data are serially transmitted.

- Redial with Hold State Cancell

[Off Hook] [RD] [T] (or [P], [RD] key)

Pause time can be cancelled with [P], [T] or [RD] keys during pause time in redialing. Any pause in series with corresponding pause is also cancelled. When any pause is not stored before or after mode switching, chip will go into the Hold State when DTMF mode is set up. MODE OUT will flash to indicate this Hold State. DTMF data are stored in redial memory and not transmitted from tone out.
[T], [RD] or [P] keys is depressed to reset this Hold State and DTMF data are serially transmitted.

Single Tone Operation in DTMF Mode (Test mode)

The M/B pin is used to trig the chip into test made by applying a positive or negative pulse to this input after "Off Hook." Test mode is sustained until On Hook. The single tone is shown in the following table which contrast with normal mode.

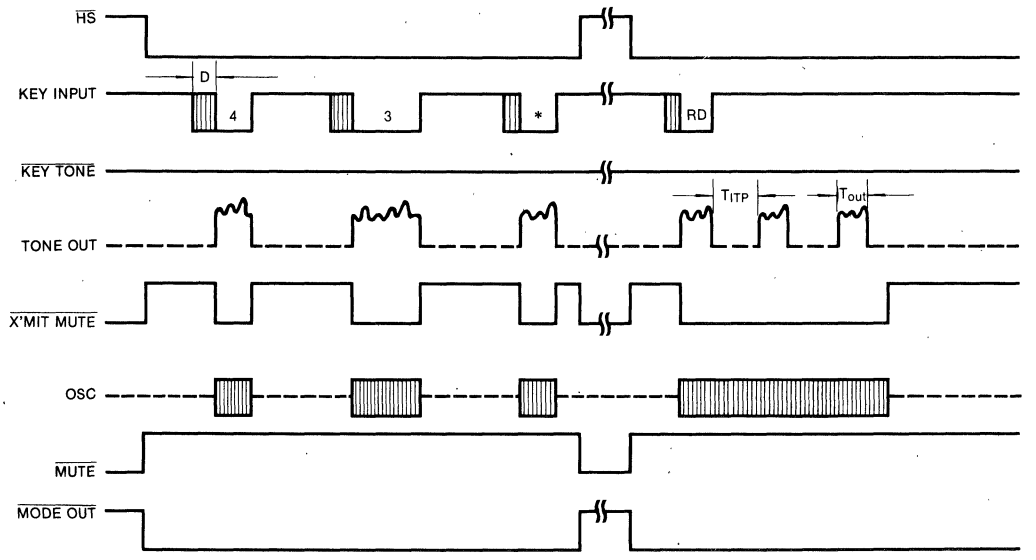
Normal mode

R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#
	C1	C2	C3

Single tone mode

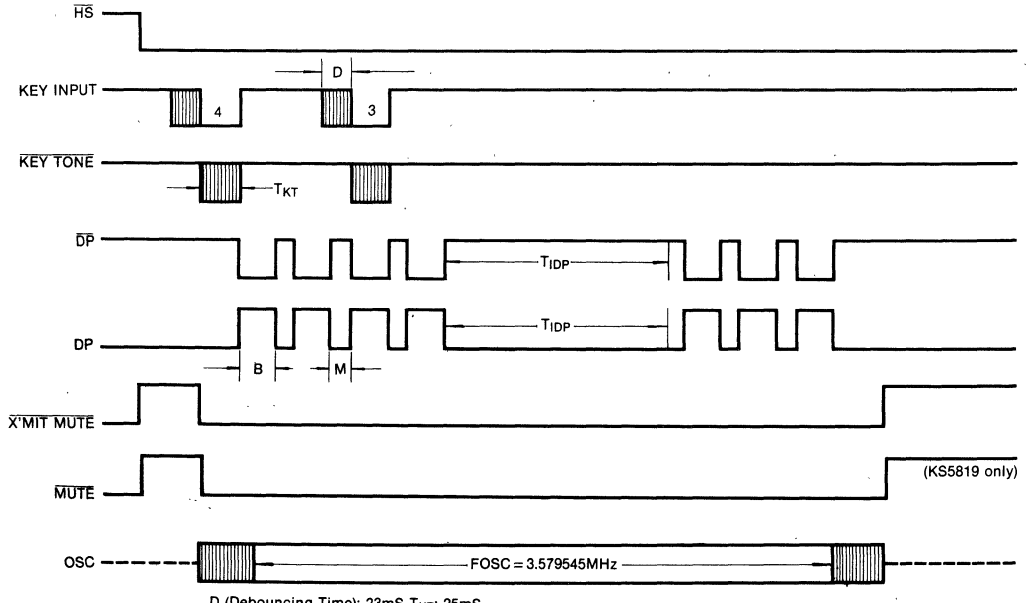
R1	R1	C2	C3
R2	C1	C2	R2
R3	R3	C2	C3
R4	C1	R4	C3

TONE MODE TIMING (MODE SELECT = V_{SS})



D: Debouncing time: 23mS
T_{ITP}: 146mS T_{out}: 146mS

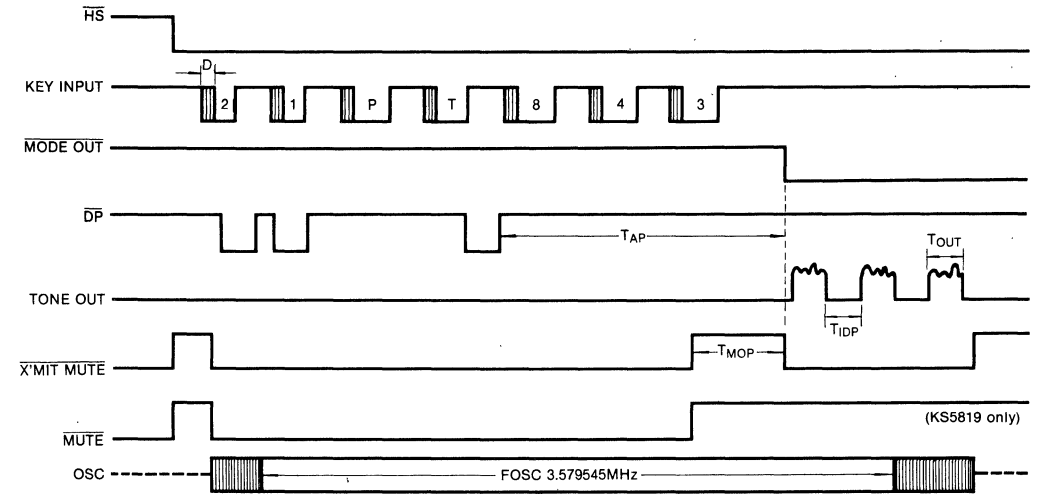
PULSE MODE TIMING ($\overline{\text{MODE SELECT}}$ = V_{DD})



D (Debouncing Time): 23mS T_{KT}: 25mS
T_{IDP}: 823mS f_{KT}: 1.75KHz

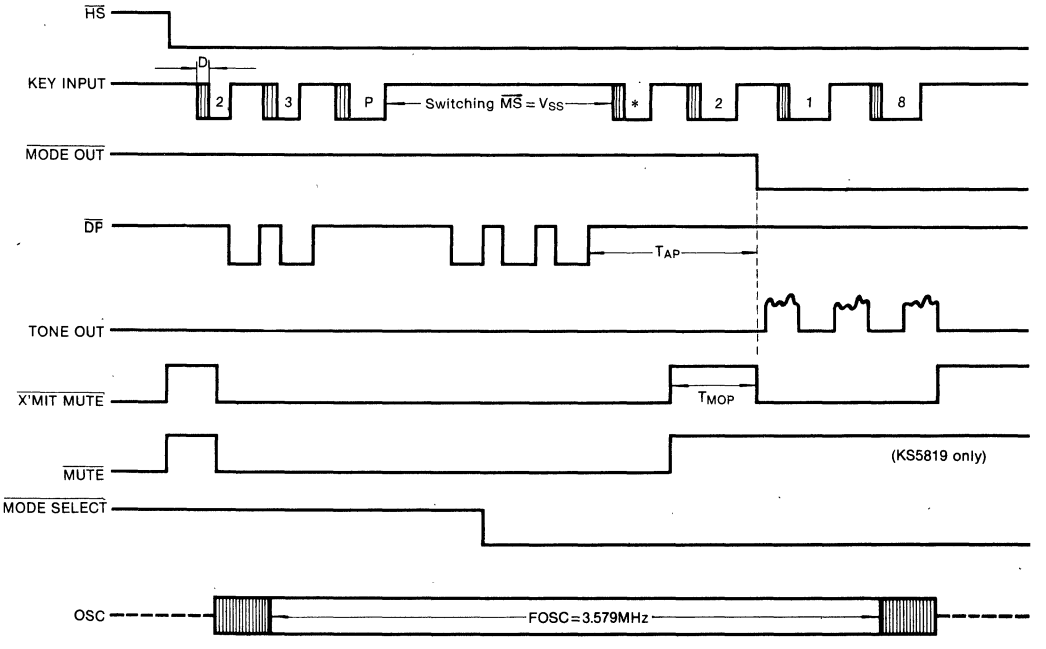
TIMING DIAGRAM

(for Switching Mode Operation by [T] key) (OPERATION SELECT, $\overline{\text{MODE SELECT}}$ = = V_{DD})



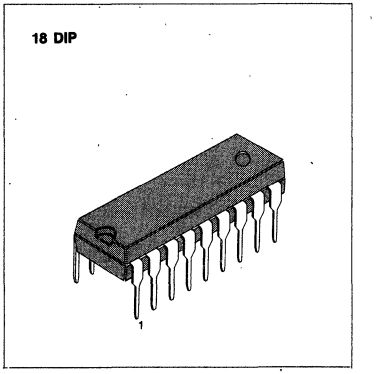
TIMING DIAGRAM

(for Switching Mode Operation by $\overline{\text{MODE SELECT}}$ Input) (OPERATION SELECT = V_{SS})



TONE/PULSE DIALER WITH REDIAL

The KS5820 is a DTMF/PULSE switchable dialer with a 32-digit redial memory. Through pin selection, switching from pulse to DTMF mode can be done using slide switch. All necessary dual-tone frequencies are derived from a 3.579545MHz TV crystal, providing very high accuracy and stability. The required sinusoidal wave form for each individual tone is digitally synthesized on the chip. The wave form so generated has very low total harmonic distortion (7% Max). A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the single levels of the dual tone to meet telephone industry specification. CMOS technology is used to produce this device, resulting very low power requirements high noise immunity, and easy interface to a variety of telephones requiring external components.



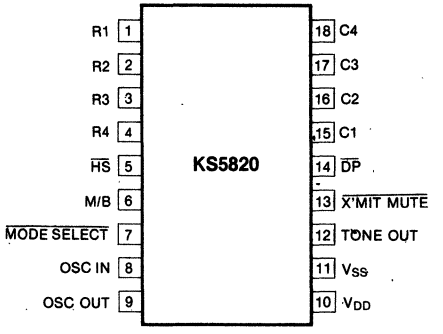
FEATURES

- **Tone/Pulse switchable (slide switch).**
- **32 digit capacity for redial**
- **Automatic mix redialing (last number dial) of PULSE→DTMF with multiple auto access pause**
- **PABX auto-pause for 3.6 sec.**
- **4 x 4 or (2 of 8) keyboard available**
- **Low power CMOS process (2.0 to 5.5V)**
- **Numbers dialed Manually after redial are cascadable and stored as additional numbers for next redialing**
- **Uses inexpensive TV crystal (3.579545MHz)**
- **Make/Break ratio (33 1/3 ~ 66 2/3 or 40/60) pin selectable**
- **Touch key hooking (580ms)**
- **Low standby current**

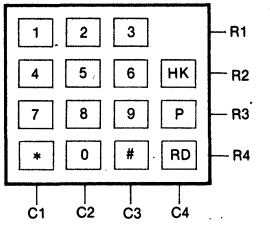
ORDERING INFORMATION

Type	Dial Pulse	Dial Pulse Rate	T_{idp}	Make/Break Ratio
KS58A20N	DP	10 (PPs)	823 (mS)	V_{DD}: 33.3/66.6
				V_{SS}: 40/60
KS58B20N	DP	20 (PPs)	823 (mS)	V_{DD}: 33.3/66.6
				V_{SS}: 40/60
KS58C20N	$\overline{DP}$	10 (PPs)	823 (mS)	V_{DD}: 33.3/16.6
				V_{SS}: 40/60
KS58D20N	$\overline{DP}$	20 (PPs)	823 (mS)	V_{DD}: 33.3/66.6
				V_{SS}: 40/60

PIN CONFIGURATION

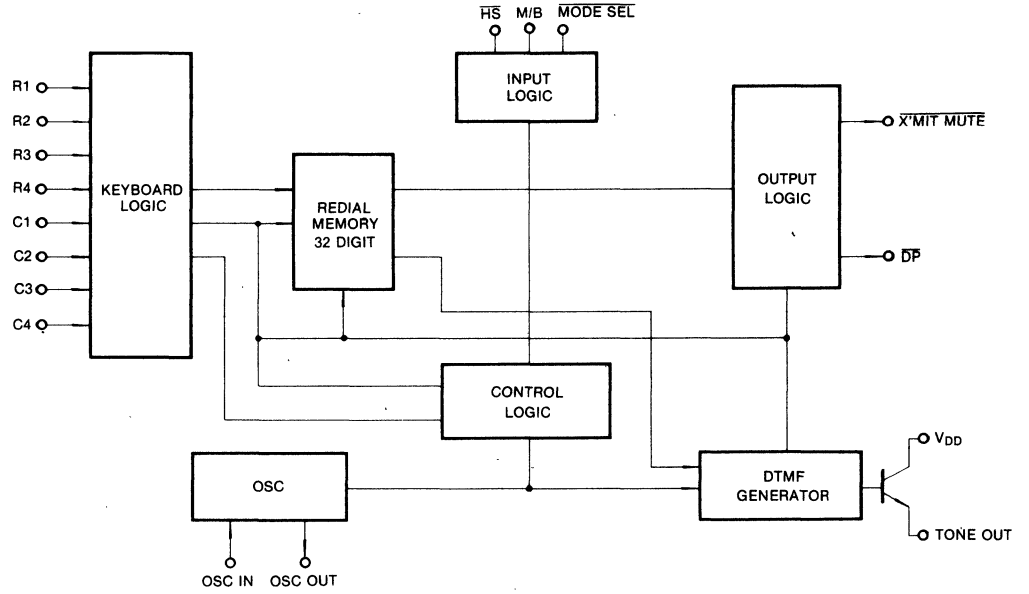


ARRANGEMENT OF KEYBOARD



HK : HOOKING (580ms)
P : PAUSE (3.6 second)
RD : REDIAL

BLOCK DIAGRAM



TONE DURATION & PAUSE IN REDIAL

Characteristic	Symbol	Typ	Unit
Tone Duration	T_D	74	mS
Minimum Pause	ITP	110	mS
Cycle Time	T_C	184	mS

TONE FREQUENCIES

Input	Specified	Actual	% Error
R1	697	699.1	+0.31
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.7	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	6.0	V
Input Voltage	V_{IN}	$V_{SS}-0.3$, $V_{DD}+0.3$	V
Output Voltage	V_{OUT}	$V_{SS}-0.3$, $V_{DD}+0.3$	
Output Voltage	V_{OUT}	1.2 ($\overline{DP}$, $\overline{X'MITMUTE}$)	V
Tone Output Current	I_{TONE}	50	mA
Power Dissipation	P_D	500	mW
Operating Temperature	T_{opr}	$-20 \sim +70$	°C
Storage Temperature	T_{stg}	$-40 \sim +125$	

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 3.5V, fx'tal = 3.579545MHz, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions			Min	Typ	Max	Unit
Operating Voltage Range	$V_{DD}P$	Pulse Mode	All inputs connected to V_{DD} or V_{SS}		2.0		5.5	V
	$V_{DD}T$	Tone Mode			2.0		5.5	
Memory Retention Voltage	V_{DR}				1.0			
Operating Supply Current	$I_{DD}P$	$\overline{MODE} = V_{DD}$	One key selected $\overline{HS} = V_{SS}$. All outputs unloaded			0.4	1.0	mA
	$I_{DD}T$	$\overline{MODE} = V_{SS}$				1.0	2.0	
Standby Current	$I_{SD}1$	$\overline{HS} = V_{DD} = 1.5V$	No key selected. All outputs unloaded			0.03	0.05	μA
	$I_{SD}2$	$\overline{HS} = V_{SS}$				70	140	
Output Current	$I_{OL}1$	$\overline{DP}$	$V_{OL} = 0.4V$	$V_{DD} = 3.5V$	1.7	5.0		mA
	$I_{OL}2$	$\overline{X'MIT\ MUTE}$		$V_{DD} = 2.5V$	0.5	1.5		
Input Voltage	V_{IH}	R1-R4. C1-C3. $\overline{HS}$. M/B			$0.8V_{DD}$		V_{DD}	V
	V_{IL}	$\overline{MODE\ SELECT}$			V_{SS}		$0.2V_{DD}$	
Input Current	$I_{IN}1$	$V_{DD} = 3.5V$ $V_{IN} = 0V$	R1-R4			116		μA
	$I_{IN}2$	$V_{DD} = 2.5V$ $V_{IN} = 0V$				50		
Valid Key Entry Time	T_{kd}				23		25.3	mS
Column and Row Scanning Frequency	F_{cr}					445		Hz
Auto Access Pause Time	T_{ap}					3.6		sec
Tone Output	V_{or}	ROW TONE ONLY	$V_{DD} = 2.5V$ $R_L = 5K$		−16.0		−12.0	dBV
			$V_{DD} = 3.5V$ $R_L = 5K$		−14.0		−11.0	
Ratio of Column to Row Tone	dB_{cr}	$V_{DD} = 3.5V$			1.0	2.0	3.0	dB
Distortion	%DIS	$V_{DD} = 3.5V$					10	%
Tone Output Delay Time	T_{psd}					1.5		mS

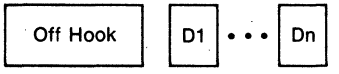
PIN DESCRIPTION

<table>
<tr><th>Pin</th><th>Name</th><th>Description</th></tr>
<tr><td>1-4
15-18</td><td>R1-R4
C1-C4</td><td>Keyboard (R1, R2, R3, R4, C1, C2, C3, C4)
These inputs can be interfaced to an XY matrix keyboard.
C1-C4 & R1-R4 are set to low at On Hook ($\overline{HS}$ = high). C1-C4 key inputs are set to low and R1-R4 are set to high at OFF HOOK ($\overline{HS}$ = low) which enables the key-input operation. Oscillator starts running when a keypress is detected. Scanning signals are presented at both column and row inputs (TYP: 445Hz) until the input key is released. Key inputs are compatible with standard 2-of-8 form or single-contact keyboard. Debouncing is provided to avoid false entry (TYP: 23mS).</td></tr>
<tr><td>5</td><td>$\overline{HS}$</td><td>Hook Switch
This input detects the state of the hook switch contact. "Off Hook" corresponds to V_{SS} condition.
"On Hook" corresponds to V_{DD} condition.</td></tr>
<tr><td>6</td><td>M/B</td><td>Make/Break Ratio
This input provides the selection of the Make/Break ratio (33.3: 66.6/40:60) when M/B is connected to V_{DD}/V_{SS}.</td></tr>
<tr><td>7</td><td>$\overline{\text{MODE SELECT}}$</td><td>Mode Select Input
Pulse/DTMF mode is selected as shown in the following table.
Initial Mode means the state after going Off Hook ($\overline{HS}$→"V_{SS}")
<table>
<tr><th>$\overline{\text{MODE SELECT}}$</th><th>INITIAL MODE</th><th>SWITCHING ENTRY MODE</th></tr>
<tr><td>V_{DD}</td><td>Pulse</td><td>$\overline{\text{MODE SELECT}}$ Input = V_{SS}</td></tr>
<tr><td>V_{SS}</td><td>Tone</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>8-9</td><td>OSC IN
OSC OUT</td><td>Oscillator Input/Output
These pins are provided to connect an external 3.58MHz crystal. Oscillator starts (at Off Hook) and is sustained until pulse or DTMF single are finished.</td></tr>
<tr><td>10-11</td><td>V_{DD}, V_{SS}</td><td>Power
These are the power supply inputs. This device is designed to operated on 2.0V to 5.5V.</td></tr>
<tr><td>12</td><td>TONE OUT</td><td>DTMF Signal Output
When a valid keypress is detected in DTMF mode Appropriate low group and high group frequencies are generated which hybrided the Dual Tone Output. Tone out is Off State in pulse mode.</td></tr>
<tr><td>13</td><td>$\overline{\text{X'MIT MUTE}}$</td><td>X'mit Mute Output
<table>
<tr><th>$\overline{HS}$</th><th>$\overline{\text{X'mit Mute Output}}$</th></tr>
<tr><td>V_{DD}</td><td>"OFF"</td></tr>
<tr><td>V_{SS}</td><td>Normally "OFF"
"ON" during pulse and DTMF dialing</td></tr>
</table>
(N channel open drain)</td></tr>
<tr><td>14</td><td>DP, DP</td><td>Dial Pulse Out</td></tr>
</table>

KEYBOARD OPERATION

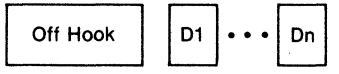
1. SINGLE MODE OPERATION

- **Pulse Mode Operation**



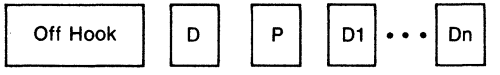
Pulse mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This is the condition under $\overline{\text{Mode Select}} = V_{DD}$.

- **Tone Mode Operation**



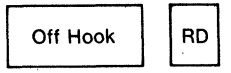
Tone mode is defined by the initial mode after going Off Hook and latched at [D1] key entry. This condition is under $\overline{\text{Mode Select}} = V_{SS}$.

- **Manual Dialing with Automatic Access Pause**



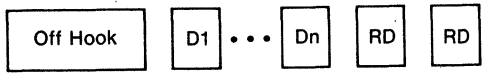
Multiple Pause key entries can be accepted and stored in the redial memory, each as on digit. Each [P] key provides 3.5 seconds pause time, but [P] key entry as first digit after going Off Hook is ignored. [*] key can also be used as pause key in pulse mode. Pause (s) can be cancelled with [P], or [RD] key during pause time in redialing.
[D] = Any numeric key.

- **Redialing**



Up to 32 digits can be dialed with [RD] key. [RD] key is disabled while pulse or DTMF signals are transmitting. When more then 32 digits are stored in redial memory, Redial is also inhibited.
[#] key can be used as [RD] key in pulse mode.

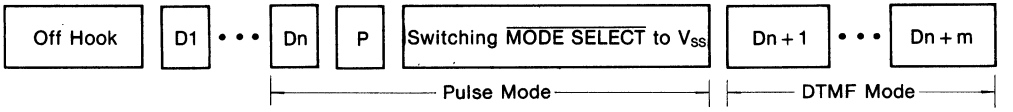
- **Inhibiting Redial**



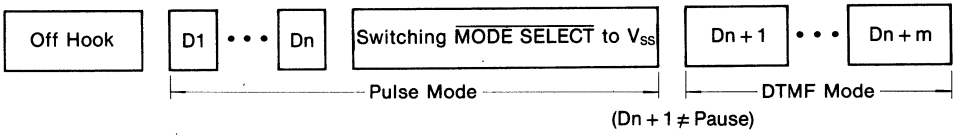
Redial can be inhibited by depressing [RD] [RD] keys after DTMF or pulse signals are transmitted.

2. PULSE/TONE SWITCHABLE OPERATION

• **Mode Switching by $\overline{\text{MODE SELECT}}$ Input**



Pulse mode is initially defined $\overline{\text{MODE SELECT}} = V_{DD}$, mode switching to DTMF can be accepted by $\overline{\text{MODE SELECT}} = V_{SS}$, DTMF mode will be set up after pulse mode is finished. In this mode, digits [Dn + 1] ... [Dn + m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys.
If no [P] key is contained serially before or after mode switching.



It results the next condition.
If digit [Dn + 1] is depressed after pulse mode is finished, DTMF mode will be set up after last pulse signal ([Dn]) is output. In this mode, digits [Dn + 1] ... [Dn + m] are transmitted from Tone Out as DTMF signals by depressing corresponded keys. If digit [Dn + 1] is depressed during dialing pulse signals. When DTMF mode is set up Hold State will be set up after last pulse signal [Dn] is finished. MODE OUT will flash to indicate this Hold State [Dn + 1] ... [Dn + m] are stored in redial memory as DTMF DATA and not transmitted from Tone Out. When it is ready to transmit DTMF data in redial memory, [RD] or [P] keys is depressed to reset this Hold State and [Dn + 1] ... [Dn + m] data are serially transmitted.

Single Tone Operation in DTMF Mode (Test mode)

The M/B pin is used to trig the chip into test made by applying a positive or negative pulse to this input after "Off Hook." Test mode is sustained until On Hook. The single tone is shown in the following table which contrast with normal mode.

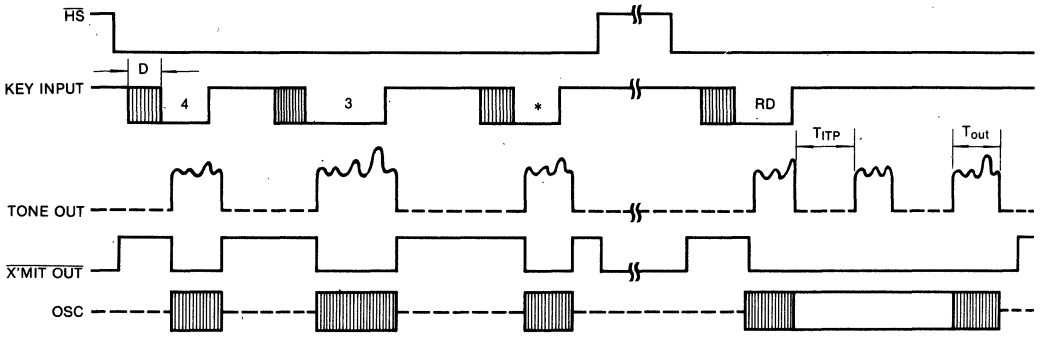
Normal mode

R1	1	2	3
R2	4	5	6
R3	7	8	9
R4	*	0	#
	C1	C2	C3

Single tone mode

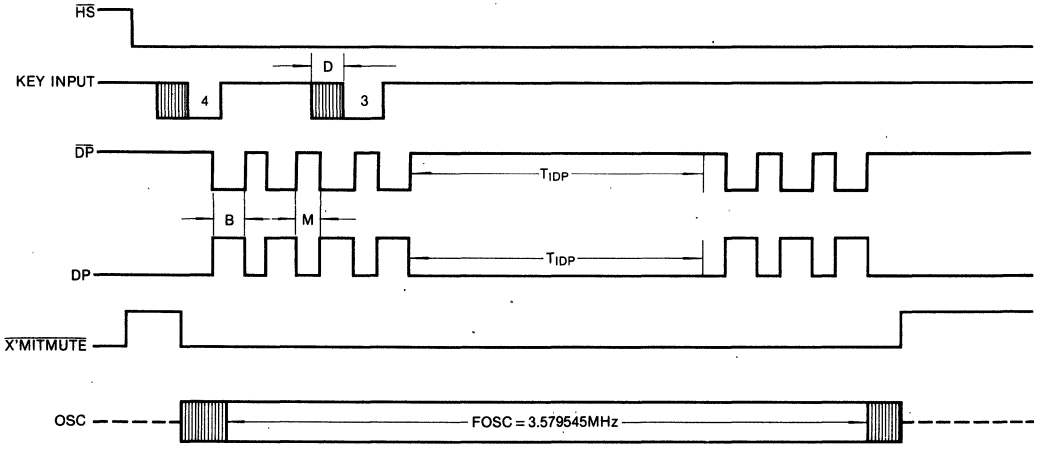
R1	R1	C2	C3
R2	C1	C2	R2
R3	R3	C2	C3
R4	C1	R4	C3
	C1	C2	C3

TONE MODE TIMING ($\overline{\text{MODE SELECT}} = V_{SS}$)



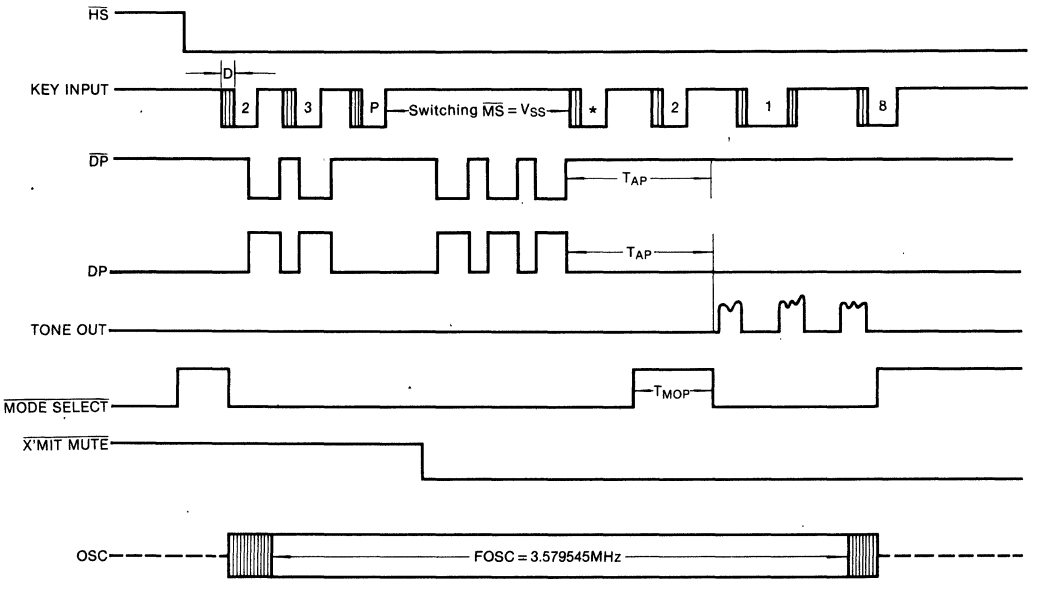
D: Debouncing Time: 23mS T_{out}: 146mS
T_{ITP}: 146mS RD

PULSE MODE TIMING ($\overline{\text{MODE SELECT}} = V_{DD}$)



D: Debouncing Time: 23mS
T_{IDP}: Inter Digit Pause: 823mS

TIMING DIAGRAM (for Switching Mode Operation by $\overline{\text{MODE SELECT}}$ Input)



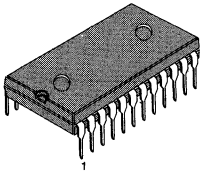
T_{AP}: Auto Pause Time

UNIVERSIAL ASYNCHRONOUS RECEIVER AND TRANSMITTER

The KS5824 UART, is a Si-gate CMOS IC which provides the data formatting and control to interface serial asynchronous data communications between main system and subsystems.

The bus interface of the KS5824 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially, transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the UART is programmed via the data bus during system initialization. A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. Exceeding Low Power dissipation is realized due to adopting CMOS process.

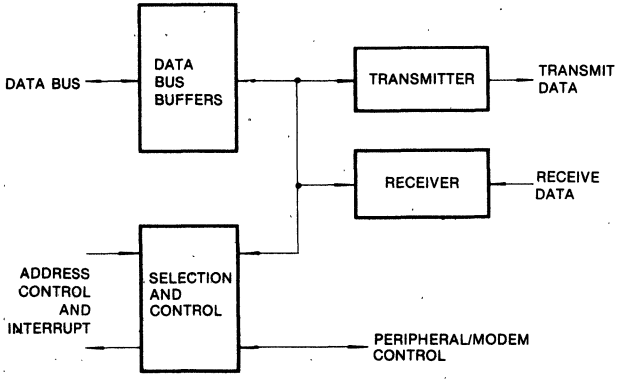
24 DIP



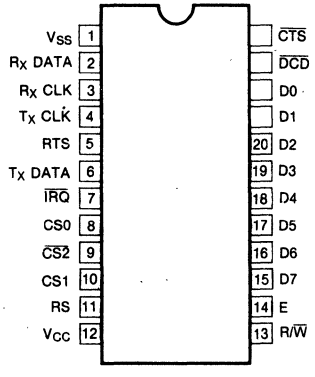
FEATURES

- **Low-power, high-speed, CMOS process**
- **Serial/parallel conversion of data**
- **8-and 9-bit transmission**
- **Optional even and odd parity**
- **Parity, overrun and framing error checking**
- **Programmable control register**
- **Optional ÷1, ÷16, and ÷64 clock modes**
- **Peripheral/modem control functions**
- **Double buffered**
- **One-or two-stop bit operation**

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 to −7.0	V
Input Voltage	V_{IN}*	−0.3 to +7.0	V
Maximum Output Current	I_O**	10	mA
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* With respect to V_{SS} (SYSTEM GND)

** Maximum output current is the maximum current which can flow out from one output terminal or I/O common terminal (D_0~D_7, $\overline{RTS}$, T_X Data, $\overline{IRQ}$).

Note: Permanent IC damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions are exceeded, it could affect reliability of IC.

3

RECOMMENDED OPERATING CONDITIONS

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}*	4.5	5.0	5.5	V
Input "Low" Voltage		V_{IL}*	0	—	0.8	V
Input "High" Voltage	D_0~D_7, RS, T_X CLK, $\overline{DCD}$, $\overline{CTS}$, R_X Data	V_{IH}*	2.0	—	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, R_X CLK		2.2	—	V_{CC}	
Operating Temperature		T_{opr}	−20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Input "High" Voltage	D_0~D_7, RS, Tx CLK, $\overline{DCD}$, $\overline{CTS}$, R_X Data	V_{IH}		2.0	—	V_{CC}	V
	CS_0, $\overline{CS_2}$, CS_1, R/$\overline{W}$, E, R_X CLK			2.2	—	V_{CC}	
Input "Low" Voltage	All inputs	V_{IL}		−0.3	—	0.8	V
Input Leakage Current	R/$\overline{W}$, CS_0, CS_1, $\overline{CS_2}$, E	I_{IN}	V_{IN} = 0 ~ V_{CC}	−2.5	—	2.5	μA
Three-State (Off State) Input Current	D_0~D_7	I_{TSI}	V_{IN} = 0.4 ~ V_{CC}	−10	—	10	μA
Output "High" Voltage	D_0~D_7	V_{OH}	I_{OH} = −400μA	4.1	—	—	V
			I_{OH} ≤ −10μA	V_{CC}-0.1	—	—	
	T_X data, $\overline{RTS}$		I_{OH} = −400μA	4.1	—	—	
			I_{OH} ≤ −10μA	V_{CC}-0.1	—	—	
Output "Low" Voltage	All outputs	V_{OL}	I_{OH} = 1.6mA	—	—	0.4	V

DC CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Leakage Current (Off State)	$\overline{IRQ}$	I_{LOH}	$V_{OH} = V_{CC}$	—	—	10	μA
Input Capacitance	$D_0 \sim D_7$	C_{IN}	$V_{IN} = 0V$, $Ta = 25°C$, $f = 1.0MHz$	—	—	12.5	pF
	E, T_X CLK, R_X CLK, R/$\overline{W}$, RS, R_X Data, CS_0, CS_1, $\overline{CS_2}$, $\overline{CTS}$, $\overline{DCD}$			—	—	7.5	
Output Capacitance	$\overline{RTS}$, T_X Data	C_{OUT}	$V_{IN} = 0V$, $Ta = 25°C$ $f = 1.0MHz$	—	—	10	pF
	$\overline{IRQ}$			—	—	5.0	
Supply Current	• Under transmitting and receiving operation • 500 kbps • Data bus in R/$\overline{W}$ operation	I_{CC}	E = 1.0MHz	—	—	3	mA
			E = 1.5MHz	—	—	4	
			E = 2.0MHz	—	—	5	
	• Chip is not selected • 500 kbps • Under non transmitting and receiving operation • Input level (Except E) V_{IH} min = $V_{CC} - 0.8V$ V_{IL} max = 0.8V		E = 1.0MHz	—	—	200	μA
			E = 1.5MHz	—	—	250	
			E = 2.0MHz	—	—	300	

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $Ta = -20 \sim +75°C$, unless otherwise noted.)

1. TIMING OF DATA TRANSMISSION

Characteristic		Symbol	Test Conditions	Min	Max	Unit
Minimum Clock Pulse Width	÷1 Mode	PW_{CL}	Fig. 1	900	—	ns
	÷16, ÷64 Modes			600	—	ns
	÷1 Mode	PW_{CH}	Fig. 2	900	—	ns
	÷16, ÷64 Modes			600	—	ns
Clock Frequency	÷1 Mode	f_C		—	500	KHz
	÷16, ÷64 Modes			—	800	KHz
Clock-to-Data Delay for Transmitter		t_{TDD}	Fig. 3	—	600	ns
Receive Data Setup Time	÷1 Mode	t_{RDSU}	Fig. 4	250	—	ns
Receive Data Hold Time	÷1 Mode	t_{RDH}	Fig. 5	250	—	ns
$\overline{IRQ}$ Release Time		t_{IR}	Fig. 6	—	1200	ns
$\overline{RTS}$ Delay Time		t_{RTS}	Fig. 6	—	560	ns
Rise Time and Fall Time	Except E	t_r, t_f		—	1000*	ns

* 1.0μs or 10% of the pulse width, whichever is smaller.

2. BUS TIMING CHARACTERISTICS

1) READ

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 7	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 7	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 7	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 7	80	—	ns
Data Delay Time	t_{DDR}	Fig. 7	—	290	ns
Data Hold Time	t_H	Fig. 7	20	100	ns
Address Hold Time	t_{AH}	Fig. 7	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 7	—	25	ns

2) WRITE

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Enable Cycle Time	$t_{cyc}E$	Fig. 8	1000	—	ns
Enable "High" Pulse Width	PW_{EH}	Fig. 8	450	—	ns
Enable "Low" Pulse Width	PW_{EL}	Fig. 8	430	—	ns
Setup Time, Address and R/$\overline{W}$ Valid to Enable Positive Transition	t_{AS}	Fig. 8	80	—	ns
Data Setup Time	t_{DSW}	Fig. 8	165	—	ns
Data Hold Time	t_H	Fig. 8	10	—	ns
Address Hold Time	t_{AH}	Fig. 8	10	—	ns
Rise and Fall Time for Enable Input	t_{Er}, t_{Ef}	Fig. 8	—	25	ns

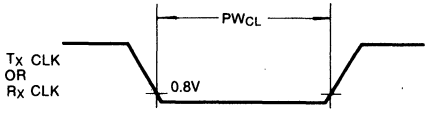


Fig. 1 Clock Pulse Width, "Low" State

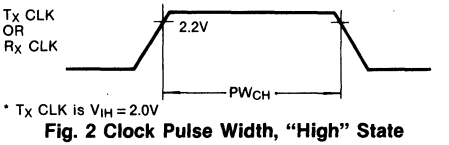


Fig. 2 Clock Pulse Width, "High" State

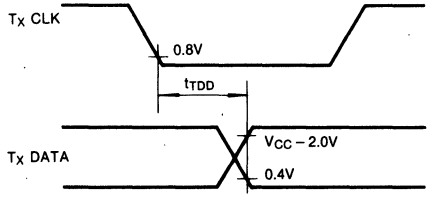


Fig. 3 Transmit Data Output Delay

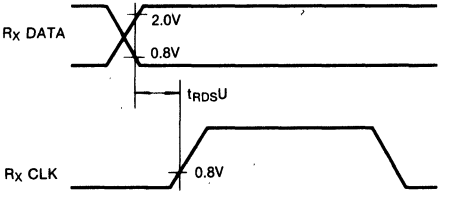


Fig. 4 Receive Data Setup Time (÷1 Mode)

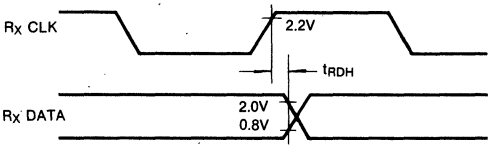


Fig. 5 Receive Data Hold Time (÷1 Mode)

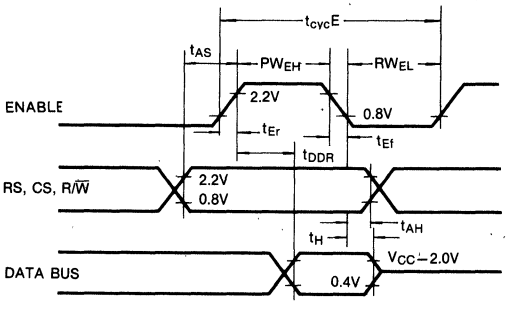
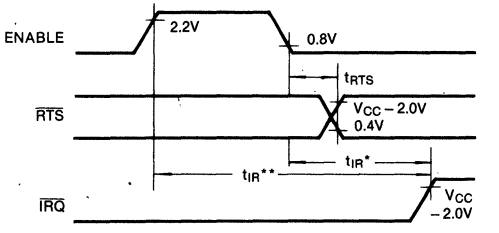


Fig. 7 Bus Read Timing Characteristics (Read information from UART)



* (1) $\overline{IRQ}$ Release Time applied to R_X Data Register read operation.
(2) $\overline{IRQ}$ Release Time applied to T_X Data Register write operation
(3) $\overline{IRQ}$ Release Time applied to control Register write TIE = 0, RIE = 0 operation.

** $\overline{IRQ}$ Release Time applied to R_X Data Register read operation right after read status register, when $\overline{IRQ}$ is asserted by $\overline{DCD}$ rising edge.

Note: Note that following take place when $\overline{IRQ}$ is asserted by the detection of transmit data register empty status. $\overline{IRQ}$ is released to "High" asynchronously with E signal when $\overline{CTS}$ goes "High". (Refer to Figure 14)

Fig. 6 $\overline{RTS}$ Delay and $\overline{IRQ}$ Release Time

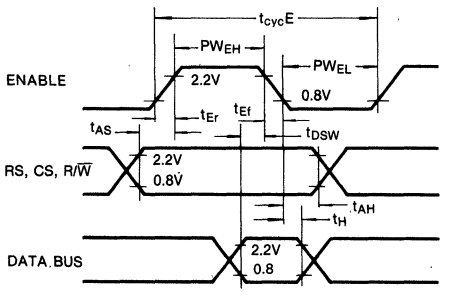


Fig. 8 Bus Write Timing Characteristics (Write information into UART)

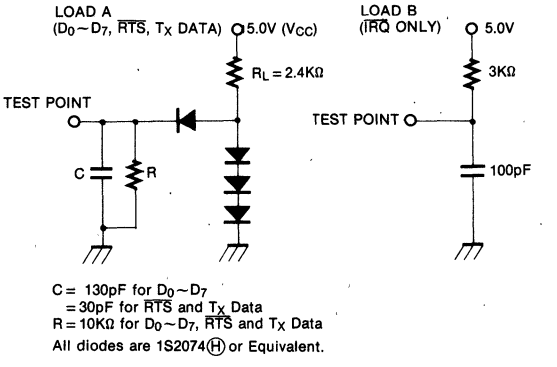


Fig. 9 Bus Timing Test Loads

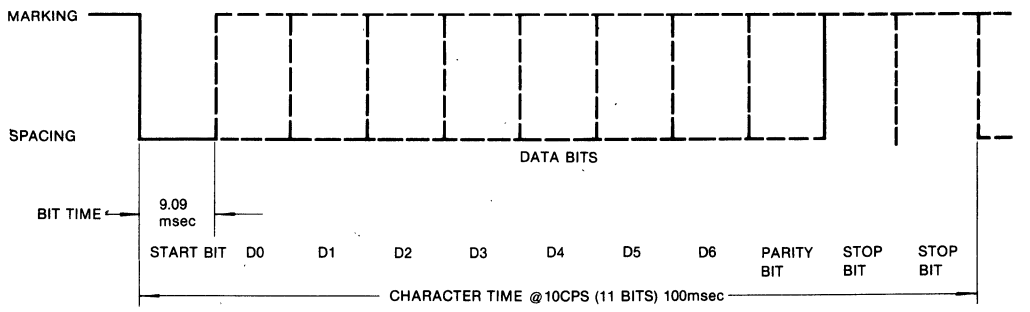


Fig. 10 110 Baud Serial ASCII Data Timing

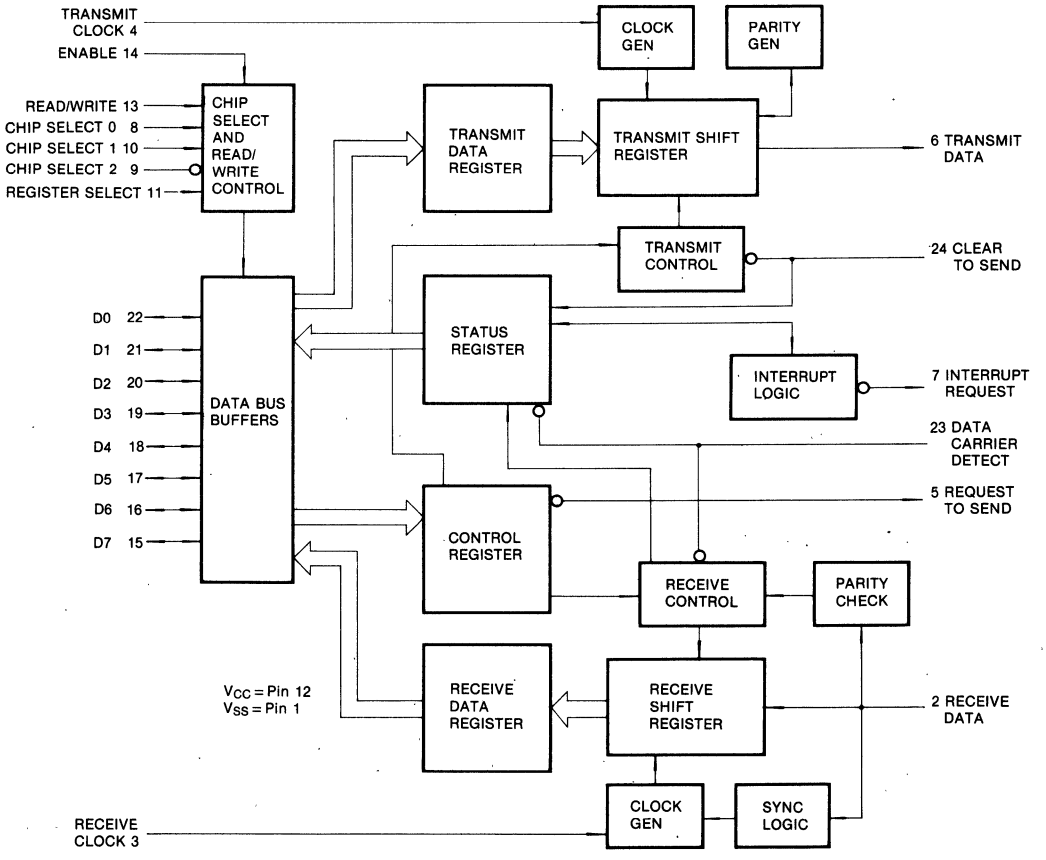


Fig. 11 Expanded Block Diagram

DEVICE OPERATION

At the bus interface, the UART appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the UART functional configuration when the communications channel is required. During the first master reset, the $\overline{IRQ}$ and $\overline{RTS}$ outputs are held at level 1. On all other master resets, the $\overline{RTS}$ output can be programmed high or low with the $\overline{IRQ}$ output held high. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The UART also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the UART. After master resetting the UART, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the UART. Status Register either as a result of an interrupt or in the UART's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divid-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of 8 or 32 low samples on the receive line in the divide-by-16 and 64 modes respectively. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit UART bus when a Read Data command is received from the MPU. When parity has been selected for a 7-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

UART INTERFACE SIGNALS FOR MPU

The KS5824 interfaces to the MPU with an 8-bit bidirectional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals permit the MPU to have complete control over the KS5824.

UART Bidirectional Data (D0-D7) — The bidirectional data lines (D0-D7) allow for data transfer between the KS5824 and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an UART read operation.

UART Enable (E) — The Enable signal, E, is a high-impedance TTL-compatible input that enables the bus input/output data buffers and clocks data to and from the KS5824.

Read/Write (R/$\overline{W}$) — The Read/Write line is a high-impedance input that is TTL compatible and is used to control the direction of data flow through the UART's input/output data bus interface. When Read/Write is high (MPU Read cycle), KS5824 output drivers are turned on and a selected register is read. When it is low, the KS5824 output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the KS5824.

Chip Select (CS0, CS1, $\overline{CS2}$) — These three high-impedance TTL-compatible input lines are used to address the KS5824. The KS5824 is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the KS5824, are then performed under the control of the Enable Signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high-impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) — Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the UART is set. The $\overline{IRQ}$ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the UART. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5•CR6), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the UART being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the UART. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the UART. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high-impedance TTL-compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16, or 64 times the data rate may be selected.

Transmit Clock (T_X CLK) —The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (R_X CLK) — The Receive Clock input is used for synchronization of received data. (In the ÷1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (R_X Data) — The Receive Data line is a high-impedance TTL-compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used.

Transmit Data (T_X Data) — The Transmit Data output line transfers serial data to a modem or other peripheral.

PERIPHERAL/MODEM CONTROL

The UART includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) — This high-impedance TTL-compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) — The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$; output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready (DTR).

Data Carrier Detect ($\overline{DCD}$) — This high-impedance TTL-compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the UART when high. A low-to-high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set. The Rx CLK must be running for proper $\overline{DCD}$ operation.

UART REGISTERS

The expanded block diagram for the UART indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the UART has been addressed with RS high and R/$\overline{W}$ low. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within 1-bit time of the training edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the UART and selecting the Receive Data Register with RS and R/$\overline{W}$ high when the UART is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

DEFINITION OF UART REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/$\overline{W}$ Transmit Data Register (Write Only)	**RS • R/$\overline{W}$ Receive Data Register (Read Only)**	**$\overline{RS}$ • R/$\overline{W}$ Control Register (Write Only)**	**$\overline{RS}$ • R/$\overline{W}$ Status Register (Read Only)**
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR1)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear-to-Send ($\overline{CTS}$)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request ($\overline{IRQ}$)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7 bit plus parity modes
*** Data bit is "don't care" in 7 bit plus parity modes.

CONTROL REGISTER

The UART Control Register consists of eight bits of write-only buffer that are selected when RS and R/$\overline{W}$ are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) — The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the UART. Additionally, these bits are used to provide a master reset for the UART which clears the Status Register (except for external conditions on $\overline{CTS}$ and $\overline{DCD}$) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the UART. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) — The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows;

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) — Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send ($\overline{RTS}$) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled.
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled.
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled.
1	1	$\overline{RTS}$ = low, Transmits Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) — The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full Overrun or a low-to-high transition on the Data Carrier Detect ($\overline{DCD}$) signal line.

STATUS REGISTER

Information on the status of the UART is available to the MPU by reading the UART Status Register. This read-only register is selected when RS is low and R/$\overline{W}$ is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the UART.

Receive Data Register Full (RDRF), Bit 0 — Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 — The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{DCD}$), Bit 2 — The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes and Interrupt Request to be generated when the Reoeive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read

status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 — The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send status bit.

Framing Error (FE), Bit 4 — Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the first stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 — Overrun is an error flag the indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 — The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{IRQ}$), Bit 7 — The $\overline{IRQ}$ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the $\overline{IRQ}$ bit will be high to indicate the interrupt or service request status. $\overline{IRQ}$ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

PCM MONOLITHIC FILTER

The KT3040J filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8KHz sampled systems.

The filter is manufactured using double-poly Si-Gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

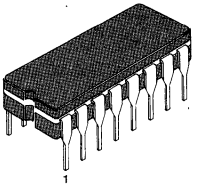
Transmit Filter Stage

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4KHz.

Receive Filter Stage

The receive filter is a fifth order elliptic lowpass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

16 CERDIP



FEATURES

- **Exceeds all D3/D4 and CCITT specifications**
- **+5V, −5V power supplies**
- **Low power consumption: 45mW (0 dBm0 into 600Ω)**
  30mW (power amps disabled)
- **Power down mode: 0.5mW**
- **20 dB gain adjust range**
- **No external anti-aliasing components**
- **Sin x/x correction in receive filter**
- **50/60Hz rejection in transmit filter**
- **TTL and CMOS compatible logic**
- **All inputs protected against static discharge due to handling**

BLOCK DIAGRAM

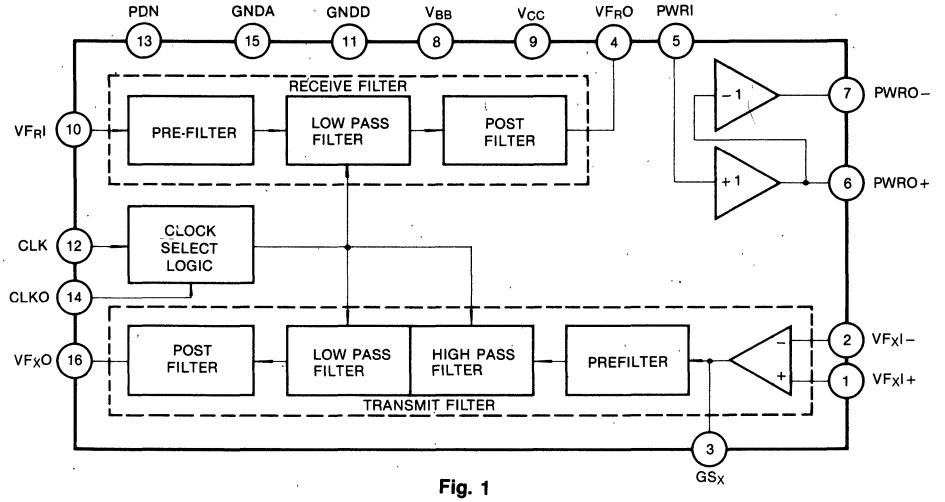
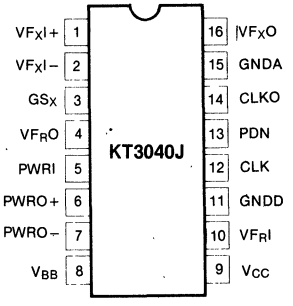


Fig. 1

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltages	V_S	±7	V
Power Dissipation	P_D	1	W/PKG
Input Voltage	V_{IN}	±7	V
Output Short-Circuit Duration	$T_{S.C\ OUT}$	Continuous	sec
Operating Temperature Range	Ta	−25 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Lead Temperature (Soldering 10 seconds)	T_L	300	°C

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, Ta = 0°C to 70°C, V_{CC} = +5.0V ± 5%, V_{BB} = −5.0V ± 5%, clock frequency is 2.048MHz. Typical parameters are specified at Ta = 25°C, V_{CC} = +5.0V, V_{BB} = −5.0V, digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
V_{CC} Standby Current	I_{CCO}	PDN = V_{DD}			400	μA
V_{BB} Standby Current	I_{BBO}	PDN = V_{DD}			400	μA
V_{CC} Operating Current	I_{CC1}	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
V_{BB} Operating Current	I_{BB1}	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
V_{CC} Operating Current	I_{CC2}	(Note 1)		4.6	6.4	mA
V_{BB} Operating Current	I_{BB2}	(Note 1)		4.6	6.4	mA
Digital Interface						
Input Current, CLK	I_{INC}	$V_{BB} \leq V_{IN} \leq V_{CC}$	−10		10	μA
Input Current, PDN	I_{INP}	$V_{BB} \leq V_{IN} \leq V_{CC}$	−100			μA
Input Current, CLKO	I_{INO}	$V_{BB} \leq V_{IN} \leq V_{CC} - 0.5V$	−10		−0.1	μA
Input Low Voltage, CLK, PDN	V_{IL}		0		0.8	V
Input High Voltage, CLK, PDN	V_{IH}		2.2		V_{CC}	V
Input Low Voltage, CLKO	V_{ILO}		V_{BB}		V_{BB} + 0.5	V
Input Intermediate Voltage, CLKO	V_{IIO}		−0.8		0.8	V
Input High Voltage, CLKO	V_{IHO}		V_{CC}-0.5		V_{CC}	V
Transmit Input OP Amp						
Input Leakage Current, V_{FXI}	I_{BXI}	$V_{BB} \leq V_{FXI} \leq V_{CC}$	−100		100	nA
Input Resistance, V_{FXI}	R_{IXI}	$V_{BB} \leq V_{FXI} \leq V_{CC}$	10			MΩ
Input Offset Voltage, V_{FXI}	V_{OSXI}	$-2.5V \leq V_{IN} \leq +2.5V$	−20		20	mV
Common Mode Range, V_{FXI}	V_{CM}		−2.5		2.5	V
Common Mode Rejection Ratio	CMRR	$-2.5V \leq V_{IN} \leq +2.5V$	60			dB
Power Supply Rejection of V_{CC} or V_{BB}	PSRR		60			dB
Open Loop Output Resistance, G_{SX}	R_{OL}			1		KΩ
Minimum Load Resistance, G_{SX}	R_L		10			KΩ
Maximum Load Capacitance, G_{SX}	C_L				100	pF
Output Voltage Swing, G_{SX}	V_{OXI}	$R_L \geq 10K$	±2.5			V
Open Loop Voltage Gain, G_{SX}	A_{VOL}	$R_L \geq 10K$	5000			V/V
Open Loop Unity Gain Bandwidth, G_{SX}	F_C			2		MHz

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta = 25°C. All parameters are specified for a signal level of 0dBm0 at 1KHz. The 0dBm0 level is assumed to be 1.54 V_{rms} measured at the output of the transmit or receive filter.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
TRANSMIT FILTER (Transmit filter input OP amp set to the non-inverting unity gain mode, with V_{FXI} = 1.09 V_{rms} unless otherwise noted.)						
Minimum Load Resistance, V_{FXO}	R_{LX}	$-2.5V < V_{OUT} < 2.5V$	3			KΩ
		$-3.2V < V_{OUT} < 3.2V$	10			KΩ
Load Capacitance, V_{FXO}	C_{LX}				100	pF
Output Resistance, V_{FXO}	R_{OX}			1	3	Ω
V_{CC} Power Supply Rejection, V_{FXO}	PSRR1	f = 1KHz, V_{FXI+} = 0 V_{rms}	30			dB
V_{BB} Power Supply Rejection, V_{FXO}	PSRR2	f = 1KHz, V_{FXI+} = 0 V_{rms}	35			dB
Absolute Gain	G_{AX}	f = 1KHz	2.875	3.0	3.125	dB
Gain Relative to G_{AX}	G_{RX}	Below 50Hz			−35	dB
		50Hz		−41	−35	dB
		60Hz		−35	−30	dB
		200Hz	−1.5		0.05	dB
		300Hz to 3KHz	−0.15		0.15	dB
		3.3KHz	−0.35		0.03	dB
		3.4KHz	−0.70		−0.1	dB
		4.0KHz		−15	−14	dB
		4.6KHz and above			−32	dB
Absolute Delay at 1KHz	D_{AX}				230	μs
Differential Envelope Delay from 1KHz to 2.6KHz	D_{DX}				60	μs
Single Frequency Distortion Products	D_{PX1}				−48	dB
Distortion at Maximum Signal Level	D_{PX2}	0.16 V_{rms}, 1KHz signal Applied to V_{FXI+}, Gain = 20dB, R_L = 10K			−45	dB
Total C Message Noise at V_{FXO}	N_{CX1}				6	dBrnc0
Total C Message Noise at V_{FXO}	N_{CX2}	Gain setting OP amp at 20dB, non-inverting, (Note 3) Ta = 0°C to 70°C			7	dBrnc0
Temperature Coefficient of 1KHz Gain	G_{AXT}			0.0004		dB/°C
Supply Voltage Coefficient of 1KHz Gain	G_{AXS}	V_{CC} = 5.0V ±5% V_{BB} = −5.0V ±5%		0.01		dB/V
Crosstalk, Receive to Transmit $20 \text{ Log } \frac{V_{FXO}}{V_{FRO}}$	C_{TRX}	Receive filter output = 2.2 V_{rms} V_{FXI+} = 0 V_{rms}, f = 0.2KHz to 3.4KHz measure V_{FXO}			−70	dB
Gaintracking Relative to G_{AX}	G_{RXL}	Output level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to +40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Filter (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 V_{rms}.)						
Input Leakage Current, V_{FRI}	I_{BR}	$-3.2V \leq V_{IN} \leq 3.2V$	−100		100	nA
Input Resistance, V_{FRI}	R_{IR}		10			MΩ
Output Resistance, V_{FRO}	R_{OR}			1	3	Ω
Load Capacitance, V_{FRO}	C_{LR}				100	pF
Load Resistance, V_{FRO}	R_{LR}		10			KΩ
Power Supply Rejection of V_{CC} or V_{BB}, V_{FRO}	PSRR3	V_{FRI} connected to GNDA f = 1KHz	35			dB
Output DC Offset, V_{FRO}	V_{OSRO}	V_{FRI} connected to GNDA	−200		200	mV
Absolute Gain	G_{AR}	f = 1KHz	−0.125	0	0.125	dB
Gain Relative to Gain at 1KHz	G_{RR}	Below 300Hz 300Hz to 3.0KHz 3.3KHz 3.4KHz 4.0KHz 4.6KHz and above	 −0.15 −0.35 −0.7		0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB
Absolute Delay at 1KHz	D_{AR}				100	μs
Differential Envelope Delay 1KHz to 2.6KHz	D_{DR}				100	μs
Single Frequency Distortion Products	D_{PR1}	f = 1KHz			−48	dB
Distortion at Maximum Signal Level	D_{PR2}	2.2 V_{rms} input to sin x/x filter, f = 1KHz, R_L = 10K			−45	dB
Total C-Message Noise at V_{FRO}	N_{CR}				6	dBrnc0
Temperature Coefficient of 1KHz Gain	G_{ART}			0.0004		dB/°C
Supply Voltage Coefficient of 1KHz Gain	G_{ARS}			0.01		dB/V
Crosstalk, Transmit to Receive $20 \text{ Log } \frac{V_{FRO}}{V_{FXO}}$	C_{TXR}	Transmit filter output = 2.2 V_{rms}, V_{FRI} = 0 V_{rms}, f = 0.3KHz to 3.4KHz Measure V_{FRO}			−70	dB
Gaintracking Relative to G_{AR}	G_{RRL}	Output level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

AC ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Receive Output Power Amplifier						
Input Leakage Current, P_{WRI}	I_{BP}	$-3.2V \leq V_{IN} \leq 3.2V$	0.1		3	μA
Input Resistance, P_{WRI}	R_{IP}		10			MΩ
Output Resistance, $P_{WRO}+$, $P_{WRO}-$	R_{OP1}	Amplifiers Active		1		Ω
Load Capacitance, $P_{WRO}+$, $P_{WRO}-$	C_{LP}				500	pF
Gain, P_{WRI} to $P_{WRO}+$ Gain, P_{WRI} to $P_{WRO}-$	$G_{AP}+$ $G_{AP}-$	$R_L = 600$ ohm connected between $P_{WRO}+$ and $P_{WRO}-$, input level = 0 dBm0 (Note 4)		1 −1		V/V V/V
Gaintracking Relative to 0 dBm0 Output Level, Including Receive Filter	G_{RPL}	$V = 2.05\ V_{rms}$, $R_L = 600Ω$ $V = 1.75\ V_{rms}$, $R_L = 300Ω$ (Notes 4, 5)	−0.1 −0.1		0.1 0.1	dB dB
Signal/Distortion	S/DP	$V = 2.05\ V_{rms}$, $R_L = 600Ω$ $V = 1.75\ V_{rms}$, $R_L = 300Ω$ (Notes 4, 5)			−45 −45	dB dB
Output DC Offset, $P_{WRO}+$, $P_{WRO}-$	V_{OSP}	P_{WRI} connected to GNDA	−50		50	mV
Power Supply Rejection of V_{CC} or V_{BB}	PSRR5	P_{WRI} connected to GNDA	45			dB

Note 1. Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0dBm is delivered to 600Ω connected from $P_{WRO}+$ to $P_{WRO}-$.
2. Voltage input to receive filter at 0V, V_{FRO} connected to P_{WRI}, 600Ω from $P_{WRO}+$ to $P_{WRO}-$, output measured from $P_{WRO}+$ to $P_{WRO}-$.
3. The 0dBm0 level for the filter is assumed to be 1.54 V_{rms} measured at the output of the XMIT or RCV filter.
4. The 0dBm0 level for the power amplifiers is load dependent. For $R_L = 600Ω$ to GNDA, the 0dBm0 level is 1.43 V_{rms} measured at the amplifier output. For $R_L = 300Ω$ the 0dBm0 level is 1.22 V_{rms}.
5. V_{FRO} connected to P_{WRI}, input signal applied to V_{FRI}.

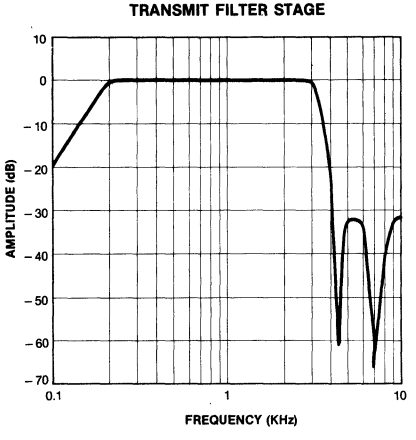
PIN DESCRIPTION

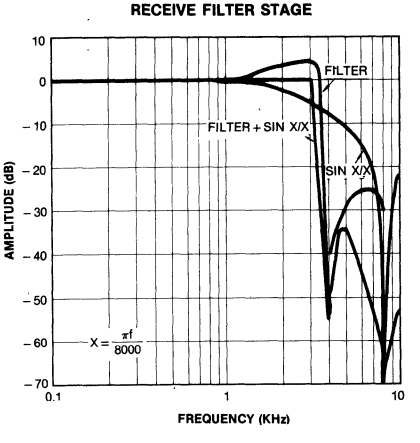
Pin	Name	Function
1	$V_{FXI}+$	The non-inverting input to the transmit filter stage.
2	$V_{FXI}-$	The inverting input to the transmit filter stage.
3	G_{SX}	The output used for gain adjustments for the transmit filter.
4	V_{FRO}	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	P_{WRI}	The input to the receive filter differential power amplifier.
6	$P_{WRO}+$	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	$P_{WRO}-$	The inverting output of the receive filter power amplifier. This output can be used with $P_{WRO}+$ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is −5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	V_{FRI}	The input pin for the receive filter stage.

PIN DESCRIPTION (Continued)

Pin	Name	Function
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048MHz, 1.544MHz or 1.536MHz.
13	PDN	The input pin used to power down the KT3040 during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLKO	This input pin selects internal counters in accordance with the CLK input clock frequency: C_{LK} — Connect CLKO to: 2048KHz — V_{CC} 1544KHz — GNDD 1536KHz — V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to G_{NDD}.
16	V_{FXO}	The output of the transmit filter stage.

TYPICAL PERFORMANCE CURVE





FUNCTION DESCRIPTION

The KT3040 monolithic filter contains four main sections; transmit filter, receive filter, receive filter power amplifier, and frequency divider/select logic (refer to Figure 1). A brief description of the circuit operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ, a voltage gain of greater than 10,000 low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10KΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by prefilter which is a two pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D_3 and D_4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10KΩ load in parallel with up to 25pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similiar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similiar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit. (SLIC).

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting lesistors, R_3, R_4 (refer to Fig. 2). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (Pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLKO (Pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (Pin 13) will reduce the total filter power consumption to less than 1mW. Connect PDN to GNDD for normal operation.

APPLICATION INFORMATION

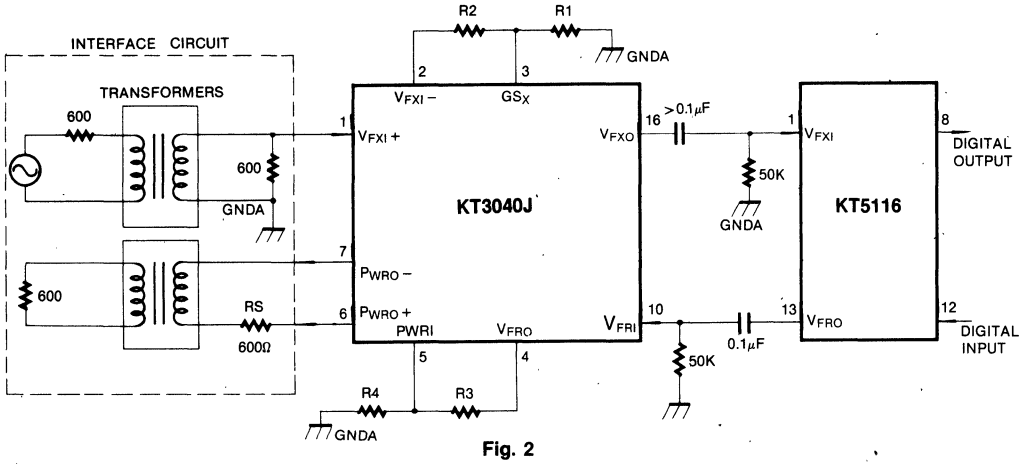


Fig. 2

Note 1: Transmit voltage gain $= \frac{R_1 + R_2}{R_2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain), $(R_1 + R_2 \geq 10K)$

Note 2: Receive Gain $= \frac{R_4}{R_3 + R_4}$ $(R_3 + R_4 \geq 10K)$

Note 3: In the configuration shown, the receive filter amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω lesistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

Gain Adjust

Fig. 2 shows the signal path interconnections between the KT3040 and KT5116 single-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the KT3040 filter when operated with system peak overload voltages of ±2.5 to ±3.2V at V_{FXO} and V_{FRO}. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the KT3040 filter can be used with the KT3000 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

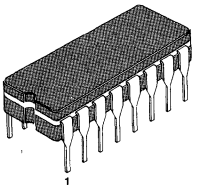
COMBO CODEC

The KT3054 consists of μ-law monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion and a serial PCM interface. The devices are fabricated using double-poly CMOS process (μ-process). The encode portion of each device consists of an input gain adjust amplifier, an active RC prefilter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200Hz and above 3,400Hz.

Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3,400Hz and is followed by a single-ended power amplifier capable of driving low impedance loads.

The devices require two 1.536MHz, 1.544MHz or 2.048MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64KHz to 2.048MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

16 CERDIP



FEATURES

- **Complete CODEC and filtering system (COMBO) including;**
  - **— Transmit high-pass and low-pass filtering**
  - **— Receive low-pass filter with sin x/x correction**
  - **— μ-law compatible COder and DECoder**
  - **— Internal precision voltage reference**
  - **— Active RC noise filters**
  - **— Serial I/O interface**
  - **— Internal auto-zero circuitry**
- **μ-law without signaling**
- **Meets or exceeds all D_3/D_4 and CCITT specifications**
- **Low operating power: typically 60mW**
- **Power-down standby mode: typically 3mW**
- **Automatic power-down**
- **$\pm$ 5V operation**
- **TTL or CMOS compatible digital interfaces**
- **Maximizes line interface card circuit density**

BLOCK DIAGRAMS

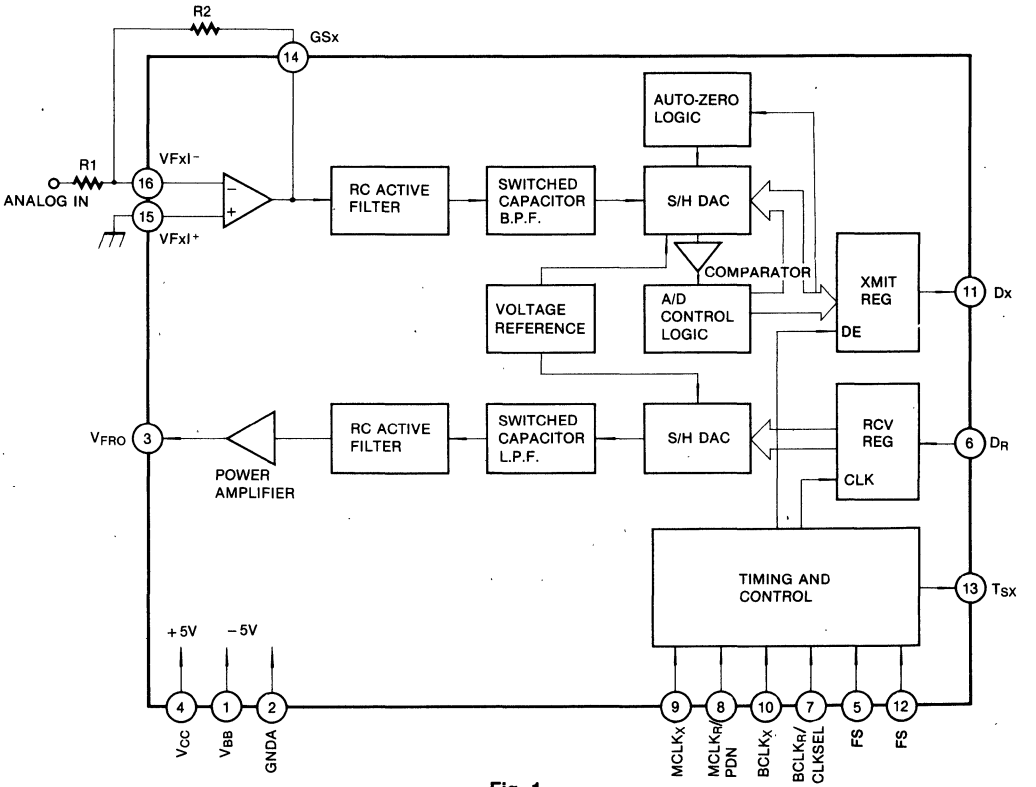


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Value	Unit
V_{CC} to GNDA	7	V
V_{BB} to GNDA	−7	V
Voltage at Any Analog Input or Output	V_{CC} + 0.3 to V_{BB} − 0.3	V
Voltage at Any Digital Input or Output	V_{CC} + 0.3 to GNDA − 0.3	V
Operating Temperature Range	−25 to +125	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (Soldering, 10 secs)	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted; $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, Ta = 25°C; all signals are referenced to GNDA.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Interface						
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, $I_L = 3.2mA$ $\overline{SIG_R}$, $I_L = 1.0mA$ $\overline{TS_X}$, $I_L = 3.2mA$, open drain			0.4 0.4 0.4	V V V
Output High Voltage	V_{OH}	D_X, $I_H = -3.2mA$ SIG_R, $I_H = -1.0mA$	2.4 2.4			V V
Input Low Current	I_{IL}	$GNDA \leq V_{IN} \leq V_{IL}$, all digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{CC}$	−10		10	μA
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA \leq V_O \leq V_{CC}$	−10		10	μA
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	R_IXA	$-2.5V \leq V \leq +2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	Ω
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L \leq 10K\Omega$	±2.8			V
Voltage Gain	A_VXA	VF_XI+ to GS_X	5,000			V/V
Unity Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	$V_{OS}XA$		−20		20	mV
Common-Mode Voltage	$V_{CM}XA$	CMRRXA > 60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB
Analog Interface with Receive Filter						
Outout Resistance	R_ORF	Pin VF_RO		1	3	Ω
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	600			Ω
Load Capacitance	C_LRF				500	pF
Output DC Offset Voltage	VOS_RO		−200		200	mV
Power Dissipation						
Power-Down Current	$I_{CC}0$	No Load		0.5	1.5	mA
Power-Down Current	$I_{BB}0$	No Load		0.05	0.3	mA
Active Current	$I_{CC}1$	No Load		6.0	9.0	mA
Active Current	$I_{BB}1$	No Load		6.0	9.0	mA

TIMING CHARACTERISTICS

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency of Master Clocks	$1/t_{PM}$	Depends on the device used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X	100			ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 488ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns
Holding Time from Bit Clock Low to Frame Sync	t_{HBFL}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long frame only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to $\overline{TS_X}$ Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DZC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	$C_L = 0pF$ to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSG}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	50			ns

TIMING CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long) (Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

TIMING DIAGRAM

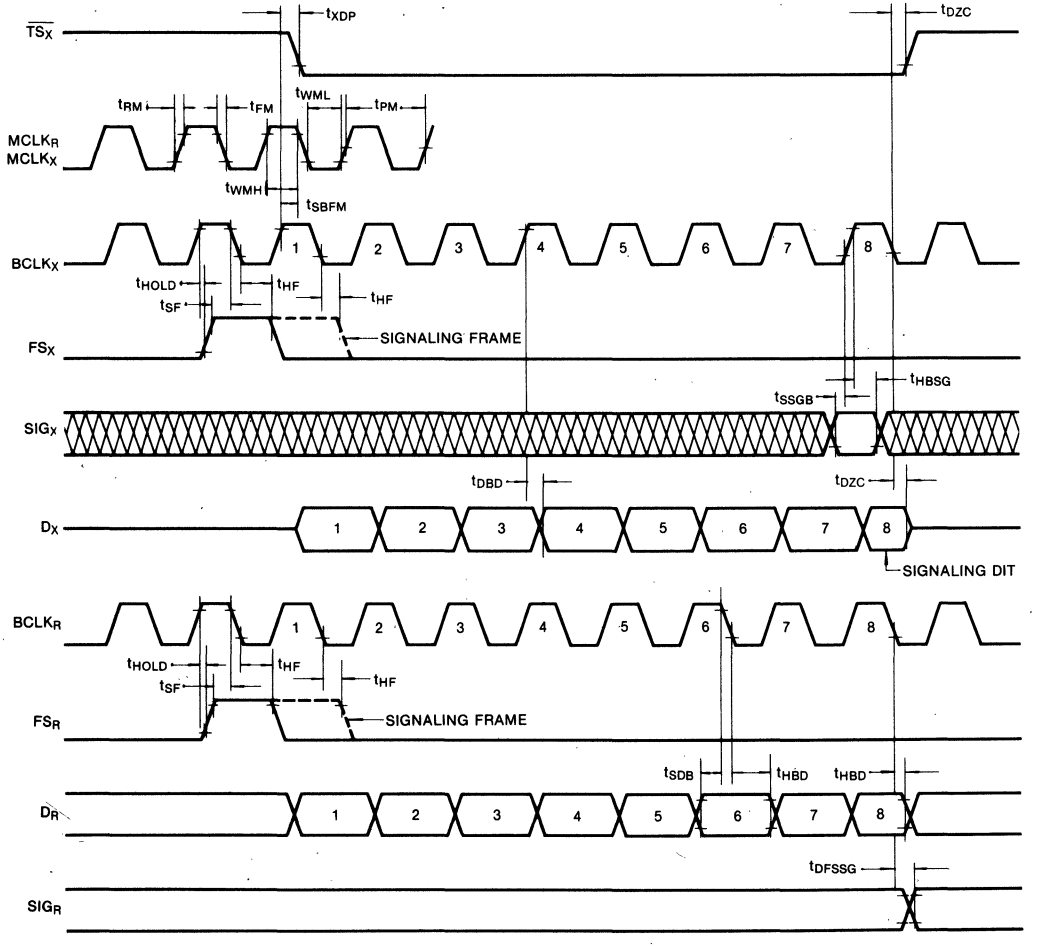


Fig. 2. Short Frame Sync Timing

TIMING DIAGRAM (Continued)

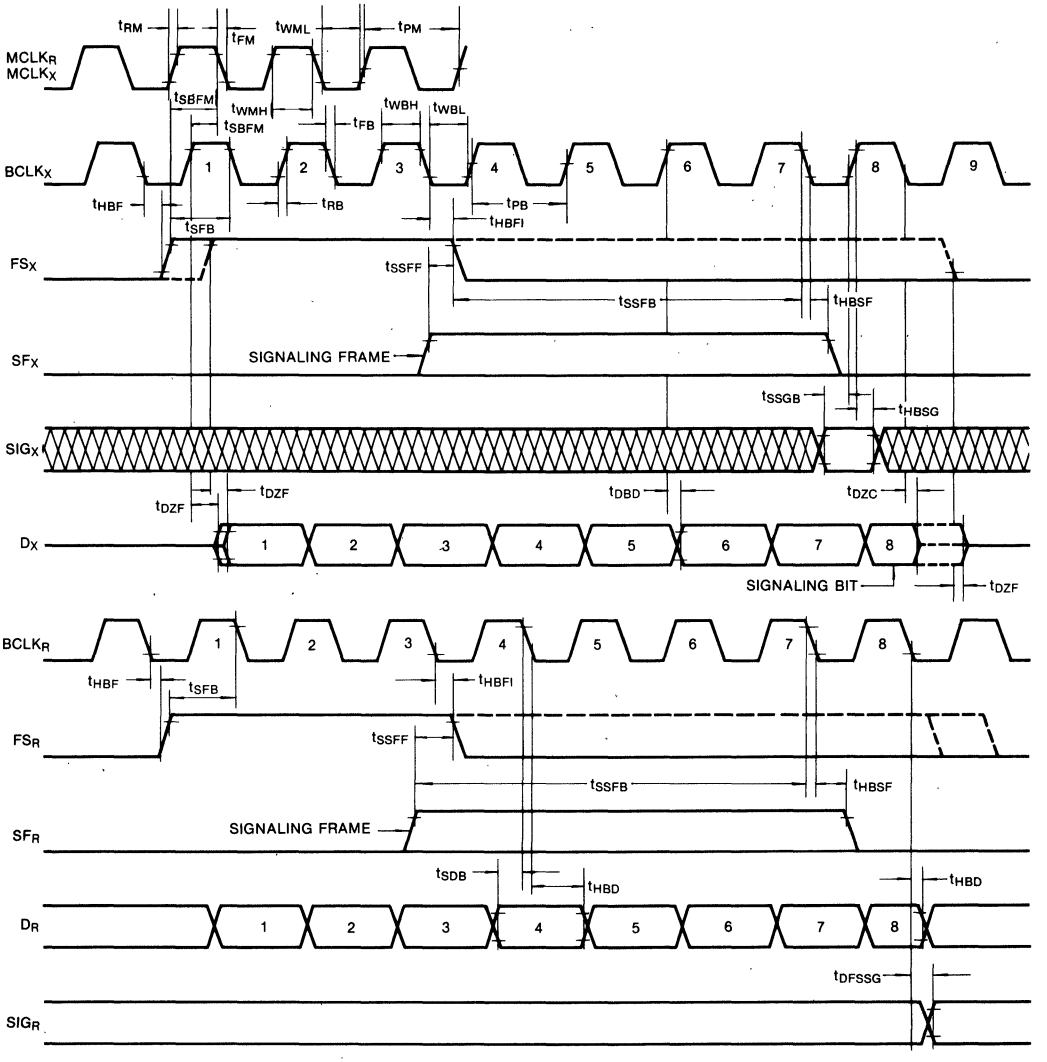


Fig. 3 Long Frame Sync Timing

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0, transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Amplitude Response						
Absolute Levels	A_L	Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		Vrms
Max Overload Level	t_{MAX}	Max overload level (3.17dBm0)		2.501		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40 dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an Ideally encoded—10dBm0 signal PCM level = −40dBm0 to +3 dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Output Drive Level	V_{RO}	R_L = 600Ω	−2.5		2.5	V

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz f = 600Hz – 800Hz f = 800Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz	– 40 – 30	– 25 – 20 70 100 145	 90 125 175	μs μs μs μs μs
Noise						
Transmit Noise, C Message Weighted	N_{XC}	$VF_XI+ = 0V$		12	15	dBrnC0
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero		8	11	dBrnC0
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0Vrms$			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0Vrms$, $V_{CC} = 5.0V_{DC} + 100mVrms$ f = 0KHz – 50KHz	40			dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0Vrms$, $V_{BB} = -5.0V_{DC} + 100mVrms$ f = 0KHz – 50KHz	40			dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100mVrms$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100mVrms$ f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, Measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 130dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk, 0dBm0 Transmit Level	CT_{X-R}	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk, 0dBm0 Receive Level	CT_{R-X}	f = 300Hz – 3400Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB

Note 1. CT_{R-X} is measured with a – 40dBm0 activating signal applied at VF_XI+

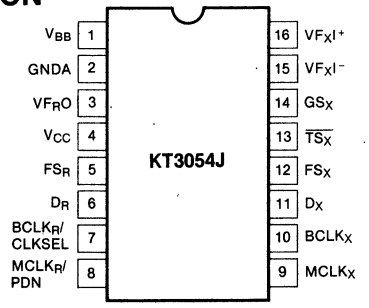
ENCODING FORMAT AT Dx OUTPUT

V_{IN} (at GS_X) = + Full – Scale	1 0 0 0 0 0 0 0
V_{IN} (at GS_X) = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} (at GS_X) = – Full – Scale	0 0 0 0 0 0 0 0

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8KHz pulse train.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. Many vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions.
8	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continously low, $MCLK_R$ is selected for all internal timing. When $MCLK_R$ is connected continuously high the device is powered down.
9	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8KHz pulse train.
13	$\overline{TS_X}$	Open drain ouptut which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
15	VF_XI-	Inverting input of the transmit input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

PIN CONNECTION



FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE 1. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected
Clocked	1.536MHz or 1.544MHz
0	2.048MHz
1 (or Open Circuit)	1.536MHz or 1.544MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 1.536MHz, 1.544MHz for the KT3054, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64KHz to 2.048MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2.* With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latgch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3.* Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64KHz operation, the frame sync pulse must be kept low for a minimum of 160ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256KHz. The decoder is A-law or μ-law (KT3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8KHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600Ω load to a level of 7.2dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is ~ 10μs (decoder update) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4.* The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (KT3054) or A-law coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

APPLICATION INFORMATION

POWER SUPPLIES

In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

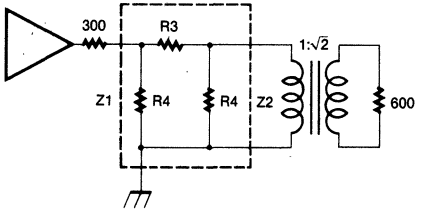
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to to 319Ω (assuming a perfect transformer).

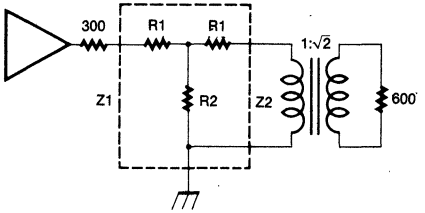
π-Pad Attenuator



$$R_3 = \sqrt{\frac{Z_1 \cdot Z_2}{2}} \left(\frac{N^2-1}{N}\right)$$

$$R_4 = Z_1 \left(\frac{N^2-1}{N^2-2NS+1}\right)$$

T-Pad Attenuator



$$R_1 = Z_1 \left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z_1 \cdot Z_2} \left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z_1 \cdot Z_2} \left(\frac{N}{N^2-1}\right)$$

Where: $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

$$S = \sqrt{\frac{Z1}{Z2}}$$

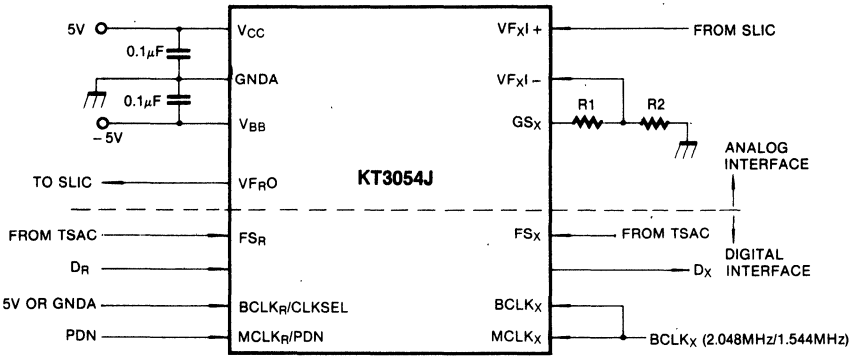
Also: $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC} = impedance with short circuit termination and Z_{OC} = impedance with open circuit termination

TABLE II. Attenuator Table for $Z_1 = Z_2 = 300\Omega$ (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26K	3.5	52K
0.2	3.5	13K	6.9	26K
0.3	5.2	8.7K	10.4	17.4K
0.4	6.9	6.5K	13.8	13K
0.5	8.5	5.2K	17.3	10.5K
0.6	10.4	4.4K	21.3	8.7K
0.7	12.1	3.7K	24.2	7.5K
0.8	13.8	3.3K	27.7	6.5K
0.9	15.5	2.9K	31.1	5.8K
1.0	17.3	2.61	34.6	5.2K
2	34.4	1.3K	70	2.6K
3	51.3	850	107	1.8K
4	68	650	144	1.3K
5	84	494	183	1.1K
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17K	386
20	246	61	1.5K	366

APPLICATION CIRCUITS

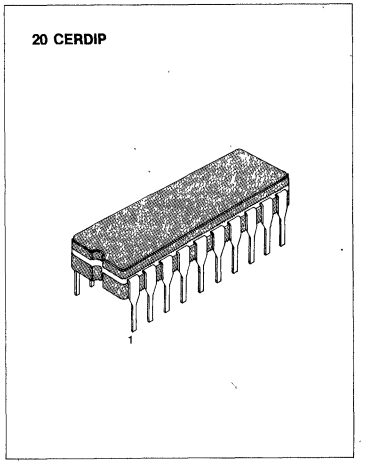


Note: XMIT gain $= 20 \times \log(\frac{R1 + R2}{R2})$, $(R1 + R2) > 10K\Omega$.

Fig. 4

COMBO CODEC

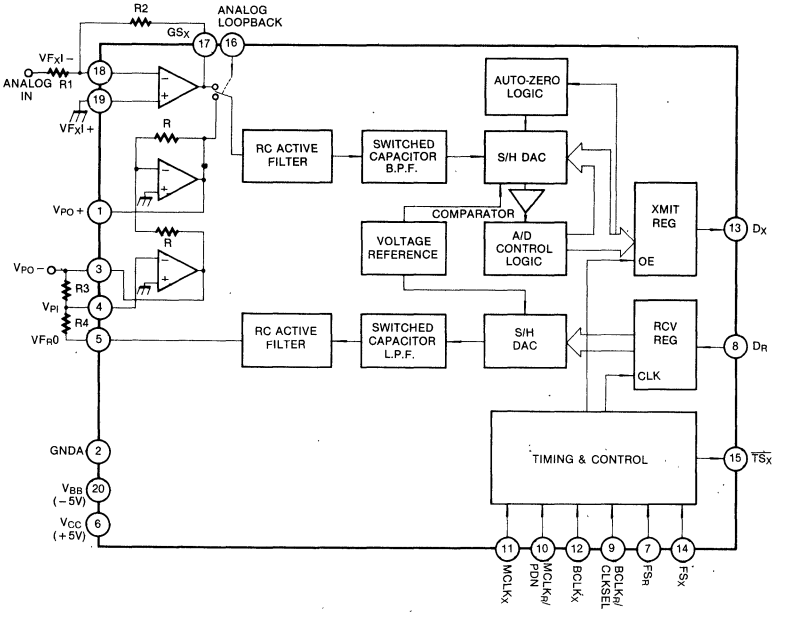
The KT3064 (μ-law), is monolithic PCM CODEC/ FILTERS utilizing the A/D and D/A conversion, a serial PCM interface. The devices are fabricated using double-poly CMOS process. The device feature an additional receive power amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6V across a balanced 600Ω load. The Analog Loopback switch and $\overline{TS}_X$ output is also included.



FEATURES

- **μ-law compatible**
- **Meets or exceeds all D3/D4 and CCITT specifications**
- **±5V operation**
- **Low operating power: typically 70mW**
- **Active RC noise filters**
- **Power-down standby mode: typically 3mW**
- **Automatic power-down**
- **Transmit high-pass and low-pass filtering**
- **Internal precision voltage reference**
- **Serial I/O interface**
- **Internal auto-zero circuitry**
- **TTL or CMOS compatible digital interface**
- **Maximizes line interface card circuit density**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
V_{CC} to GNDA	V_{CC}	7	V
V_{BB} to GNDA	V_{BB}	−7	V
Voltage at Any Analog Input or Output	Analoge I/O	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at Any Digital Input or Output	Digital I/O	$V_{CC}+0.3$ to GNDA − 0.3	V
Operating Temperature Range	T_a	−25 ~ +125	°C
Storage Temperature Range	T_s	−65 ~ +150	°C
Lead Temperature Soldering, 10 secs)	T_L	300	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: $V_{CC}=5.0V\pm5\%$, $V_{BB}=-5V\pm5\%$, GNDA = 0V, Ta = 0°C to 70°C; typical characteristics specified at $V_{CC}=5.0V$, Ta = 25°C; all signals are referenced to GNDA)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Power Dissipation						
Active Current	$I_{CC}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Active Current	$I_{BB}1$	Power amplifiers active, VPI = 0V		7.0	10.0	mA
Power-Down Current	I_{CCO}			0.5	1.5	mA
Power-Down Current	I_{BBO}			0.05	0.3	mA
Digital Interface						
Input Low Current	I_{IL}	$GNDA\leq V_{IN}\leq V_{IL}$, All digital inputs	−10		10	μA
Input High Current	I_{IH}	$V_{IH}\leq V_{IN}\leq V_{CC}$	−10		10	μA
Output Current in High Impedance State (TRI-STATE)	I_{OZ}	D_X, $GNDA\leq V_O\leq V_{CC}$	−10		10	μA
Input Low Voltage	V_{IL}				0.6	V
Input High Voltage	V_{IH}		2.2			V
Output Low Voltage	V_{OL}	D_X, $I_L=3.2mA$ SIG_R, $I_L=1.0mA$ $\overline{T_{SX}}$, $I_L=3.2mA$, Open Drain			0.4 0.4 0.4	V
Output High Voltage	V_{OH}	D_X, $I_H=-3.2mA$ SIG_R, $I_H=-1.0mA$	2.4 2.4			V
Analog Interface with Transmit Input Amplifier						
Input Leakage Current	I_IXA	$-2.5V\leq V\leq+2.5V$, VF_XI+ or VF_XI-	−200		200	nA
Input Resistance	R_IXA	$-2.5V\leq V\leq+2.5V$, VF_XI+ or VF_XI-	10			MΩ
Output Resistance	R_OXA	Closed loop, unity gain		1	3	MΩ
Load Resistance	R_LXA	GS_X	10			KΩ
Load Capacitance	C_LXA	GS_X			50	pF
Output Dynamic Range	V_OXA	GS_X, $R_L\geq10K\Omega$	±2.8			V

ELECTRICAL CHARACTERISTICS (Continued)

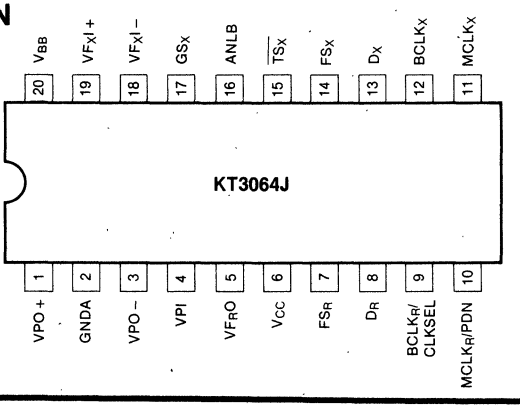
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Voltage Gain	A_VXA	VF_XI+ to GS_X	5000			V/V
Unit-Gain Bandwidth	F_UXA		1	2		MHz
Offset Voltage	$V_{OS}XA$		−20		20	mV
Common-Mode Voltage	$V_{CM}XA$	CMRRXA>60dB	−2.5		2.5	V
Common-Mode Rejection Ratio	CMRRXA	DC Test	60			dB
Power Supply Rejection Ratio	PSRRXA	DC Test	60			dB
Analog Interface with Receive Filter (All Devices)						
Output Resistance	R_ORF	Pin VF_RO		1	3	Ω
Output DC Offset Voltage	VOS_RO	Measure from VF_RO to GND A	−200		200	mV
Load Resistance	R_LRF	$VF_RO = \pm 2.5V$	10			KΩ
Load Capacitance	C_LRF	Connect from VF_RO to GND A			25	pF
Analog Interface with Power Amplifiers (All Devices)						
Input Leakage Current	IPI	$-1.0V \leq VPI \leq 1.0V \leq VPI \leq 1.0V$	−100		100	nA
Input Resistance	RIPI	$-1.0V \leq VPI \leq 1.0V$	10			MΩ
Input Offset Voltage	VI_{OS}		−25		25	mV
Output Resistance	ROP	Inverting unity gain at VPO+ or VPO−		1		Ω
Unit-Gain Bandwidth	F_C	Open loop (VPO−)		400		KHz
Load Capacitance	C_{LP}	$R_L \geq 1500\Omega$ VPO+ or $R_L = 600\Omega$ VPO− to $R_L = 300\Omega$ GNDA			100 500 1000	pF pF pF
Gain from VPO− to VPO+	GA_P+	$R_L = 300\Omega$ VPO+ to GNDA level at VPO− = −1.77Vrms (+3dBmo)		−1		V/V
Power Supply Rejection of V_{CC} or V_{BB}	$PSRR_P$	VPO− connected to VPI 0KHz−4KHz 0KHz−50KHz	 60 36			 dB dB
Frequency of Master Clock	I/t_{PM}	Depends on the device used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160			ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160			ns
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$			50	ns
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$			50	ns
Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First bit clock after the leading edge of FS_X	100			ns
Period of Bit Clock	t_{PB}		485	488	15,725	ns
Width of Bit Clock High	t_{WBH}	$V_{IH} = 2.2V$	160			ns
Width of Bit Clock Low	t_{WBL}	$V_{IL} = 0.6V$	160			ns
Rise Time of Bit Clock	t_{RB}	$t_{PB} = 480ns$			50	ns
Fall Time of Bit Clock	t_{FB}	$t_{PB} = 488ns$			50	ns

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Holding Time from Bit Clock Low to Frame Sync	t_{HBF}	Long frame only	0			ns
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short frame only	0			ns
Set-Up Time for Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80			ns
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load = 150pF plus 2 LSTTL loads	0		180	ns
Delay Time to TS_X Low	t_{XDP}	Load = 150pF plus 2 LSTTL loads			140	ns
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DEC}		50		165	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, whichever Comes Later	t_{DZF}	C_L = 0pF to 150pF	20		165	ns
Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50			ns
Hold Time from $BCLK_{R/X}$ Low to D_R Invalid	t_{HBD}		50			ns
Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	t_{DFSSF}	Load = 50pF plus 2 LSTTL loads			300	ns
Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	50			ns
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short frame sync pulse (1 or 2 bit clock periods long)(Note 1)	100			ns
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X of FS_R)	t_{HBFI}	Long frame sync pulse (from 3 to 8 bit clock periods long)	100			ns
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64K bit/s operating mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

PIN CONFIGURATION



TIMING DIAGRAM

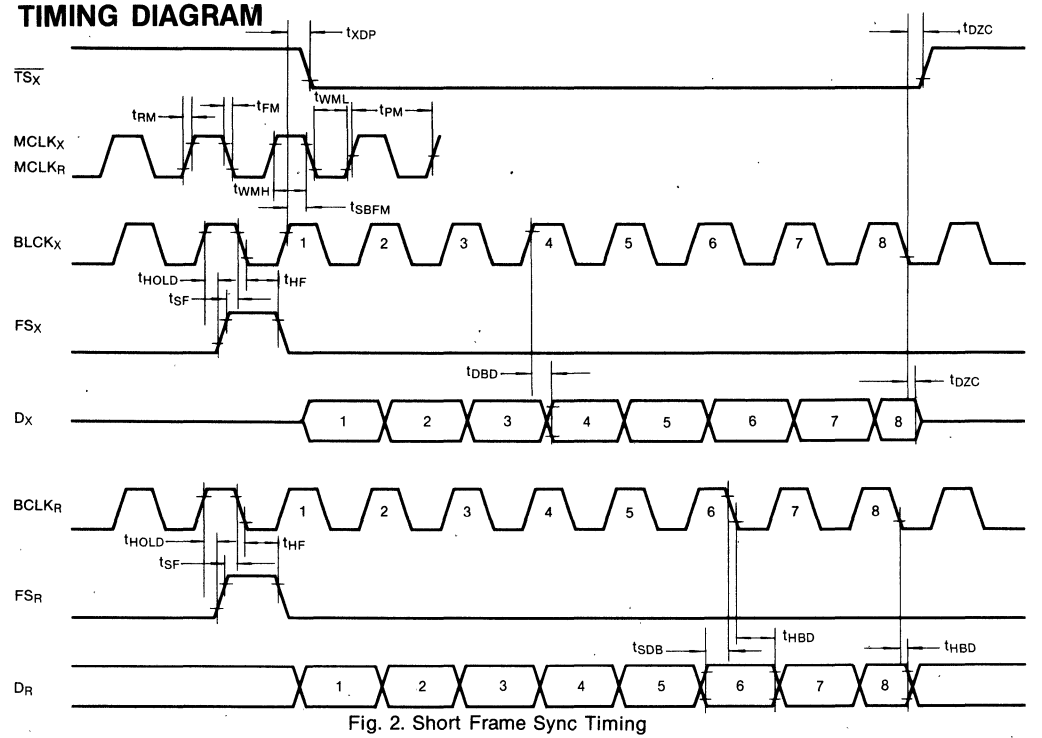


Fig. 2. Short Frame Sync Timing

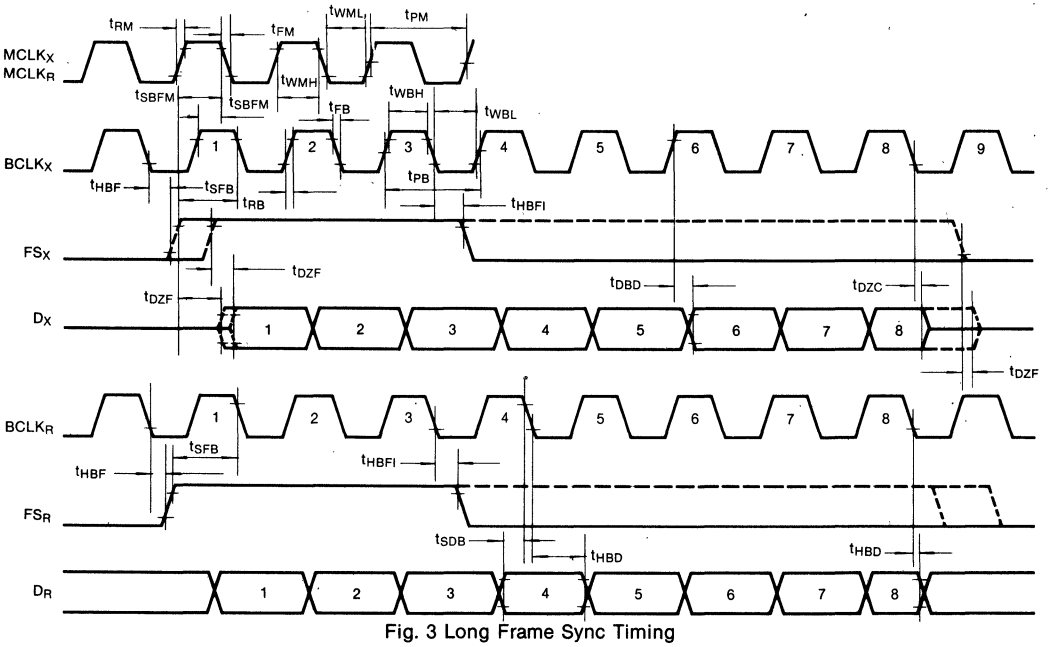


Fig. 3 Long Frame Sync Timing

PIN DESCRIPTION

Pin	Name	Function
1	VPO^+	The non-inverted output of the receive power amplifier.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VPO^-	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin $V_{CC} = +5V \pm 5\%$.
7	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R, FS_R is an 8KHz pulse train. (refer to Fig 2 and 3 for timing details)
8	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
9	$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64KHz to 2.048MHz. Alternatively, may be a logic input which selects either 1.536MHz/1.544MHz or 2.048MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions. (see Table 1)
10	$MCLK_R$/ PDN	Receive master clock. Must be 1.536MHz or 2.048MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
11	$MCLK_X$	Transmit master clock. Must be 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with $MCLK_R$.
12	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$.
13	D_X	The TRI-STATE PCM data output which is enabled by FS_X.
14	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data a on D_X, FS_X is an 8KHz pulse train. (refer to Fig 2, 3)
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is dis connected from the output of the preamplifier and connected to the VPO^+ output of the receive power, amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set again.
18	VF_XI^-	Inverting input of the transmit input amplifier.
19	VF_XI^+	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin $V_{BB} = -5V \pm 5\%$.

FUNCTIONAL DESCRIPTION

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X, VF_RO, VPO – and VPO + outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2-power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low-the device will power-down approximately 2ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. In synchronous mode, the bit clock, $BCLK_X$, may be from 64KHz to 2.048MHz, but must be synchronous with $MCLK_X$. Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE 1. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected
Clocked	1.536MHz or 1.544MHz
0	2.048MHz
1 (or Open Circuit)	1.544MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks maybe applied. $MCLK_X$ and $MCLK_R$ must be 1.536MHz, 1.544MHz for the KT3064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (refer to pin description). For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$, $BCLK_R$ must be a clock. $BCLK_X$ and $BCLK_R$ many operate from 64KHz to 2.048MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long (refer to Fig. 2). With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (KT5116-type) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long (refer to Fig. 3). Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64KHz operation, the frame sync pulse must be kept low for a minimum of 160ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth allow gains in excess of 20dB across the audio passband to be realized. The OP amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (KT3064) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{max}) of nominally 2.5V peak. The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165μs (due to the transmit filter) plus 125μs (due to encoding delay), which totals 290μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256KHz. The decoder is μ-law (KT3064) and 5th order low pass filter corrects for the sin x/x attenuation due to the 8KHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10μs later the decoder DAC output is updated. The total decoder delay is 210μs (decoder update) plus 110μs (filter delay) plus 62.5μs (1/2 frame), which gives approximately 180μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the $\pm$2.5V peak output signal from the receive filter upto $\pm$3.3V peak into an unbalanced 300Ω load, or $\pm$4.0V into an unbalanced 15KΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differently driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in Fig. 2. A total peak power of 15.6dBm can be delivered to the load plus termination. Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12mW of power.

ENCODING FORMAT AT Dx OUTPUT

V_{IN} = + Full – Scale	1 0 0 0 0 0 0 0
V_{IN} = 0V	1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1
V_{IN} = – Full – Scale	0 0 0 0 0 0 0 0

TRANSMISSION CHARACTERISTICS

(Unless otherwise specified: Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, GNDA = 0V, f = 1.02KHz, V_{IN} = 0dBm0 transmit input amplifier connected for unity-gain non-inverting.)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Amplitude Response						
Absolute Levels		Nominal 0dBm0 level is 4dBm (600Ω) 0dBm0		1.2276		Vrms
Max Transmit Overload Level	t_{MAX}	Max transmit overload level (3.17dBm0)		2.501		V_{PK}
Transmit Gain, Absolute	G_{XA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0dBm0 at 1020Hz	−0.15		0.15	dB
Transmit Gain, Relative to G_{XA}	G_{XR}	f = 16Hz f = 50Hz f = 60Hz f = 200Hz f = 300Hz − 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz f = 4600Hz and up, measure Response from 0Hz to 4000Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
Absolute Transmit Gain Variation with Temperature	G_{XAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Transmit Gain Variation with Supply Voltage	G_{XAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Transmit Gain Variations with Level	G_{XRL}	Sinusoidal test method Reference level = −10dBm0 VF_XI+ = −40dBm0 to +3dBm0 VF_XI+ = −50dBm0 to −40 dBm0 VF_XI+ = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Gain, Absolute	G_{RA}	Ta = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital code sequence for 0dBm0 signal at 1020Hz	−0.15		0.15	dB
Receive Gain, Relative to G_{RA}	G_{RR}	f = 0Hz to 3000Hz f = 3300Hz f = 3400Hz f = 4000Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
Absolute Receive Gain Variation with Temperature	G_{RAT}	Ta = 0°C to 70°C			±0.1	dB
Absolute Receive Gain Variation with Supply Voltage	G_{RAV}	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%			±0.05	dB
Receive Gain Variations with Level	G_{RRL}	Sinusoidal test method; reference input PCM code corresponds to an ideally encoded—10dBm0 signal PCM level = −40dBm0 to +3 dBm0 PCM level = −50dBm0 to −40dBm0 PCM level = −55dBm0 to −50dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
Receive Filter Output at VF_RO	V_{RO}	R_L = 10KΩ	−2.5		2.5	V

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Envelope Delay Distortion with Frequency						
Transmit Delay, Absolute	D_{XA}	f = 1600Hz		290	315	μs
Transmit Delay, Relative to D_{XA}	D_{XR}	f = 500Hz – 600Hz f = 600Hz – 800Hz f = 800Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz		195 120 50 20 55 80 130	220 145 75 40 75 105 155	μs μs μs μs μs μs μs
Receive Delay, Absolute	D_{RA}	f = 1600Hz		180	200	μs
Receive Delay, Relative to D_{RA}	D_{RR}	f = 500Hz – 1000Hz f = 1000Hz – 1600Hz f = 1600Hz – 2600Hz f = 2600Hz – 2800Hz f = 2800Hz – 3000Hz	– 40 – 30	– 25 – 20 70 100 145	 90 125 175	μs μs μs μs μs
Noise						
Transmit Noise, C Message Weighted	N_{XC}	$VF_XI+ = 0V$		12	15	dBrnC0
Receive Noise, C Message Weighted	N_{RC}	PCM code equals alternating positive and negative zero		8	11	dBrnC0
Noise, Single Frequency	N_{RS}	f = 0KHz to 100KHz, loop around measurement, $VF_XI+ = 0$Vrms			– 53	dBm0
Positive Power Supply Rejection, Transmit	$PPSR_X$	$VF_XI+ = 0$Vrms, $V_{CC} = 5.0V_{DC} + 100$mVrms f = 0KHz – 50KHz	40			dBC
Negative Power Supply Rejection, Transmit	$NPSR_X$	$VF_XI+ = 0$Vrms, $V_{BB} = -5.0V_{DC} + 100$mVrms f = 0KHz – 50KHz	40			dBC
Positive Power Supply Rejection, Receive	$PPSR_R$	PCM code equals positive zero $V_{CC} = 5.0V_{DC} + 100$mVrms f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB
Negative Power Supply Rejection, Receive	$NPSR_R$	PCM code equals positive zero $V_{BB} = -5.0V_{DC} + 100$mVrms f = 0Hz – 4000Hz f = 4KHz – 25KHz f = 25KHz – 50KHz	 40 40 36			 dBC dB dB

3

TRANSMISSION CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious Out-of-Band Signals at the Channel Output	SOS	Loop around measurement, 0dBm0, 300Hz – 3400Hz input applied to VF_XI+, measure individual image signals at VF_RO 4600Hz – 7600Hz 7600Hz – 8400Hz 8400Hz – 100,000Hz			 – 32 – 40 – 32	 dB dB dB
Distortion						
Signal to Total Distortion	STD_X	Sinusoidal test method				
Transmit or Receive Half-Channel	STD_R	Level = 3.0dBm0 = 0dBm0 to 130dBm0 = – 40dBm0 XMT RCV = – 55dBm0 XMT RCV	33 36 29 30 14 15			dBC dBC dBC dBC dBC dBC
Single Frequency Distortion, Transmit	SFD_X				– 46	dB
Single Frequency Distortion, Receive	SFD_R				– 46	dB
Intermodulation Distortion	IMD	Loop around measurement, VF_X+ = – 4dBm0 to – 21dBm0, two frequencies in the range 300Hz – 3400Hz			– 41	dB
Crosstalk						
Transmit to Receive Crosstalk	CT_{X-R}	f = 300Hz – 3400Hz D_R = Steady PCM code		– 90	– 75	dB
Receive to Transmit Crosstalk	CT_{R-X}	f = 300Hz – 3000Hz, VF_XI = 0V		– 90	– 70 (Note 1)	dB
Power Amplifiers						
Maximum 0dBm0 Level for Better than ±0.1dB Linearity Over the Range – 10dBm0 to + 3dBm0	V_{OL}	Balanced load, R_L connected between VPO+ and VPO– R_L = 600Ω R_L = 1200Ω R_L = 30KΩ	 3.3 3.5 4.0			 Vrms Vrms Vrms
Signal/Distortion	S/Dp	R_L = 600Ω, 0dBm0	50			dB

Note 1. CT_{R-X} is measured with a – 40dBm0 activating signal applied at VF_XI+.

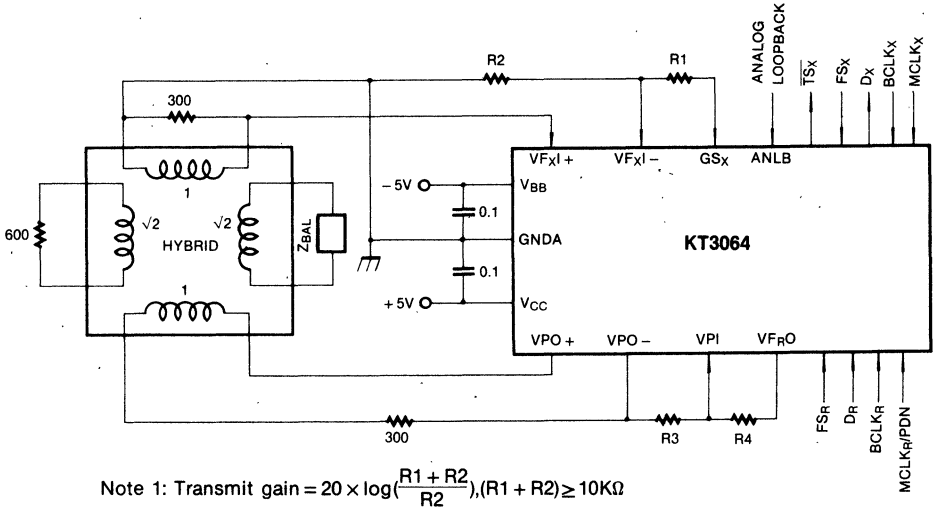
APPLICATION INFORMATION

POWER SUPPLY

While the pins of the KT3064 are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}. For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in start formation, rather tha via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10μF capacitors.

APPLICATION CIRCUIT



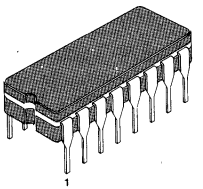
Note 1: Transmit gain $= 20 \times \log(\frac{R1+R2}{R2})$, $(R1+R2) \geq 10K\Omega$

Note 2: Receive gain $= 20 \times \log(\frac{2 \times R3}{R4})$, $R4 \geq 10K\Omega$

μ-LAW COMPANDING CODEC

The KT5116 is a monolithic CMOS companding CODEC which contains two parts: (1) an analog-to-digital converter (2) a digital to-analog converter which have transfer characteristics conforming to the μ-Law companding code.
These two parts form a coder-decoder function designed to meet the needs of the telecommunications industry for per-channel voice-frequency codes used in telephone digital switching and transmission systems.
Digital input and output are in serial format using sign-plus-amplitude coding.
A sync pulse input is provided for reception of multichannel information being multiplexed and synchronizing transmission over a single transmission line.
Practical transmission and reception of 8bit data words which contain the analog information is done from 64Kb/s to 2.1Mb/s rate with analog signal sampling occuring at an 8KHz rate.

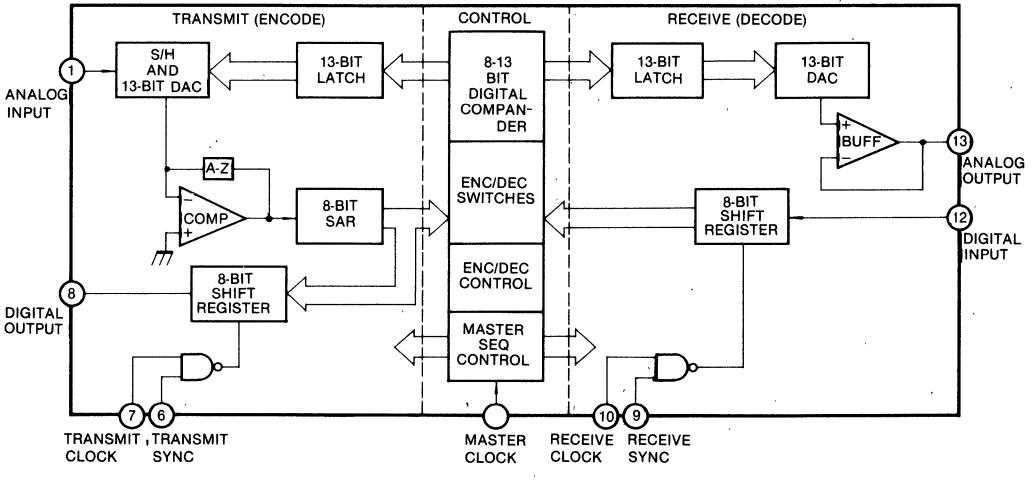
16 CERDIP



FEATURES

- **The simple ±5V power supply operation**
- **Typically 30mW low power dissipation**
- **Follows the μ-255 companding law**
- **Synchronous and asynchronous operation**
- **On-chip offset null circuit eliminates long term drift, drift error and need for trimming**
- **Minimum external circuitry required**
- **Serial data output 64Kb/s to 2.1Mb/s at 8KHz sampling rate**
- **Separate analog and digital grounding pins reduce system noise problems**
- **On-chip sample and hold.**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

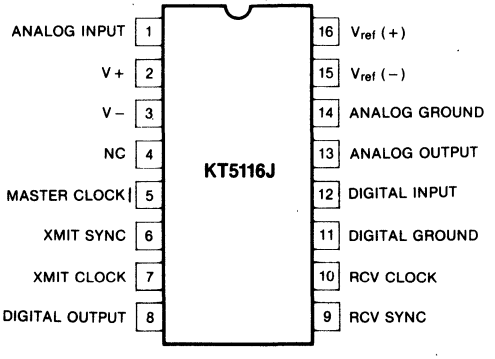
Characteristics	Symbol	Value	Unit
DC Power Supply	V+ (V−)	+6 (−6)	V
Ambient Operating Temperature	T_a	0 to 70	°C
Storage Temperature	T_s	−55 to 125	°C
Package Dissipation at 25°C	P_D	500	mW
Digital Input Voltage	V_{DI}	−0.5 to 6	V
Analog Input Voltage	V_{AI}	−6 to 6	V
Positive Reference Voltage	V_{ref+}	−0.5 to 6	V
Negative Reference Voltage	V_{ref-}	−6 to 0.5	V

DIGITAL OUTPUT CODE μ-LAW

No	Chord Code	Chord Value	Step Value
1	0 0 0	0.0mV	0.613mV
2	0 0 1	10.11mV	1.226mV
3	0 1 0	30.3mV	2.45mV
4	0 1 1	70.8mV	4.90mV
5	1 0 0	151.7mV	9.81mV
6	1 0 1	313mV	19.61mV
7	1 1 0	637mV	39.2mV
8	1 1 1	1284mV	78.4mV

EXAMPLE;
1 0 1 1 0 0 1 0 = +70.8mV+ (2×4.90mV)
sign bit chord step bit = 80.6mV
If the sign bit were a zero, then both pulse signs would be changed to minus signs

PIN CONFIGURATION



DC CHARACTERISTICS

(Condition; $V^+ = 5V$, $V^- = -5V$, $V_{ref+} = 2.5V$, $V_{ref-} = -2.5V$)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Input Resistance During Sampling	R_{INAS}		2		KΩ
Analog Input Resistance Non-Sampling	R_{INANS}		100		MΩ
Analog Input Capacitance	C_{INA}		150	250	pF
Analog Input Offset Voltage	V_{offINA}		±1	±8	mV
Analog Output Resistance	R_{OUTA}		20	50	Ω
Analog Output Current	$I_{out/A}$	0.25	0.5		mA
Analog Output Offset Voltage	$V_{off/O}$		±20	±850	mV
Logic Input Low Current ($V_{IN} = 0.8V$) Digital Input, Clock Input, SYNC Input	I_{IL}		±0.1	±10	μA
Logic Input High Current ($V_{IN} = 2.4V$)	I_{IH}		−0.25	−0.8	mA
Digital Output Capacitance	$C_{D/O}$		8	12	pF
Digital Output Leakage Current	I_{DOL}		±0.1	±10	μA
Digital Output Low Voltage	V_{OL}			0.4	V
Digital Output High Voltage	V_{OH}	3.9			V
Positive Supply Current	I^+		4	10	mA
Negative Supply Current	I^-		2	6	mA
Positive Reference Current	I_{ref+}		4	20	μA
Negative Reference Current	I_{ref-}		4	20	μA

AC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Frequency	f_m	1.5	1.544	2.1	MHz
RCV, XMIT Clock Frequency	f_r, f_x	0.064	1.544	2.1	MHz
Clock Pulse Width (MASTER, XMIT, RCV)	PW_{CLK}	200			ns
Clock Rise, Fall Time (MASTER, XMIT, RCV)	t_{rc}, t_{fc}			25% of PW_{CLK}	ns
SYNC Rise, Fall Time (XMIT, RCV)	t_{rs}, t_{fs}			25% of PW_{CLK}	ns
SYNC Pulse Width (XMIT, RCV)			$\frac{8}{f \times (fr)}$		μs
Data Input Rise, Fall Time	t_{DIR}, t_{DIF}			25% of PW_{CLK}	ns
SYNC Pulse Period (XMIT, RCV)	t_{ps}		125		μs
XMIT Clock-to-XMIT SYNC Delay	t_{xcs}	50% of t_{fc} (t_{rs})			ns
XMIT Clock-to-XMIT SYNC (Negative Edge) Delay	t_{xcsn}	200			ns
XMIT SYNC Set-Up Time	t_{xss}	200			ns
XMIT Data Delay	t_{xdd}	0		200	ns
XMIT Data Present	t_{xdp}	0		200	ns
XMIT Data Three State	t_{xdt}			150	ns
Digital Output Fall Time	t_{dof}		50	100	ns
Digital Output Rise Time	t_{dor}		50	100	ns
RCV SYNC-to-RCV Clock Delay	t_{src}	50% t_{rc} (t_{fs})			ns
RCV Data Set-Up Time	t_{rds}	50			ns
RCV Data Hold Time	t_{rdh}	200			ns
RCV Clock-to-RCV SYNC Delay	t_{rcs}	200			ns
RCV SYNC Set-Up Time	t_{rss}	200			ns
RCV SYNC-to-Analog Output Delay	t_{sao}		7		μs
Analog Output Positive Slew Rate	Slew +		1		V/μs
Analog Output Negative Slew Rate	Slew −		1		V/μs
Analog Output Drop Rate	Droop		25		μV/μs

POWER SUPPLY REQUIREMENTS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	$V+$	4.75	5.0	5.25	V
Negative Supply Voltage	$V-$	−5.25	−5.0	−4.75	V
Positive Reference Voltage	V_{ref}^{+}	2.375	2.5	2.625	V
Negative Reference Voltage	V_{ref}^{-}	−2.625	−2.5	−2.375	V

SYSTEM CHARACTERISTICS

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Signal-to-Distortion	Analog Input: 0 ~ −30dBmo Analog Input: −40dBmo Analog Input: −45dBmo	S/D	35 29 24	39 34 29		dB dB dB
Gain Tracking	Analog Input: +3 ~ −37dBmo Analog Input: −37 ~ −50dBmo Analog Input: −50 ~ −55dBmo	GT		±0.1 ±0.1 ±0.2	±0.4 ±0.8 ±2.5	dB dB dB
Idle Channel Noise	Analog Input = 0V	N_{IC}		10	18	dBrnCO
Transmission Level Point	600Ω	T_{LP}		+4		dB

PIN DESCRIPTION

1. Analog Input (Pin 1)

At this pin, employs voice-frequency analog signals which are bandwidth-limited to 4KHz. Then, they are sampled at an 8KHz rate. The Analog Input must remain between V_{ref} (+) and V_{ref} (−) for accurate conversion.

2. Positive Supply Voltage and Negative Supply Voltage (Pin 2, 3)

Pin 2, 3 is a pin which employs supply voltage. Typically, the voltages of these pins are ±5V.

3. NC (Pin 4)

This pin is a pin of non-connection.

4. Master Clock (Pin 5)

This signal provides the basic timing and control signals required for all internal conversions. It is not necessary for synchronizing with RCV SYNC, RCV Clock, XMIT SYNC or XMIT Clock. It is not internally related to them.

5. XMIT SYNC (Pin 6)

This input is synchronized with XMIT Clock. If XMIT SYNC goes High, the Digital Output is activated and the A/D conversion begins on the next positive edge of Master Clock. Otherwise, if XMIT SYNC goes Low, the Digital Output become 3 state. XMIT SYNC must go Low for at least 1 Master Clock prior to the transmission of the next digital word.

6. XMIT Clock (Pin 7)

The on-chip 8-bit output shift register of the KT5116 is unloaded at the clock rate present on this pin. Clock rates of 64KHz to 2.1MHz can be used for XMIT Clock. When the positive edge of XMIT SYNC occurs after the positive edge of XMIT Clock, XMIT SYNC will determine when the first positive edge of the internal clock will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

7. Digital Output (Pin 8)

The Digital Output is composed of a sign bit, 3 chord bits and 4 step bits. The sign bit indicates the polarity of the Analog Input while the chord and step bits indicate the magnitude. The KT5116 output register stores the 8 bit encoded sample of the Analog Input. The 8 bit-word is shifted out under control of XMIT SYNC and XMIT CLOCK. If XMIT SYNC is Low, the Digital Output is an open circuit, otherwise when XMIT SYNC is High, the state of the Digital Output is determined by the value of the output bit in the serial shift register.

8. RCV SYNC (Pin 9): Refer to Figure 3

This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV pulse is approximately eight RCV Clock periods. The conversion from digital to analog starts after the negative edge of RCV SYNC pulse (see Fig. 6). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 Master Clocks (minimum) before the digital word is to be received (see Fig. 11).

9. RCV Clock (Pin 10): Refer to Figure 3

Valid data should be applied to the digital input before the positive edge of the internal clock. (refer to Fig. 3) This SYNC pulse is approximately eight RCV CLOCK periods. The conversion from digital to analog starts after the negative the internal clock transfers the data to the slave of the master-slave flip-flop. A hold time, t_{rdh}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of internal clock will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

10. Digital Ground (Pin 11)

11. Digital Input (Pin 12)

The KT5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK (refer to Figure 3). When RCV SYNC goes High, the KT5116 uses RCV CLOCK to clock to clock the serial data into its input register RCV SYNC goes Low to indicate the end of serial input data. The eight bits of the input data have the same functions described for the Digital Output.

12. Analog Output (Pin 13)

The Analog Output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This wave form is then filtered with an external low-pass filter with sin x/x correction to recreate the sample voice signal.

13. Analog Ground (Pin 14)

14. Positive and Negative Reference Voltages, (Pin 15, 16) V_{ref} (−), V_{ref} (+)

These inputs provide the conversion reference for the digital-to-analog converter in the KT5116. V_{ref} (+) and V_{ref} (−) must maintain 100ppm/°C regulation over the operating temperature. Variation of the reference directly affects system again.

RECOMMENDED ANALOG INPUT CIRCUIT

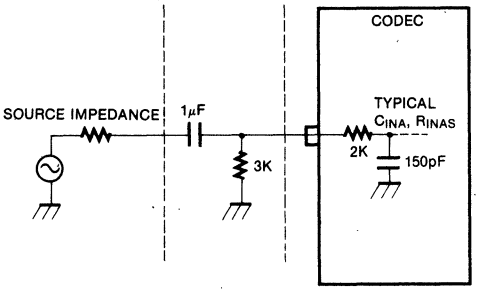


Fig. 1

TRANSMITTER SECTION TIMING

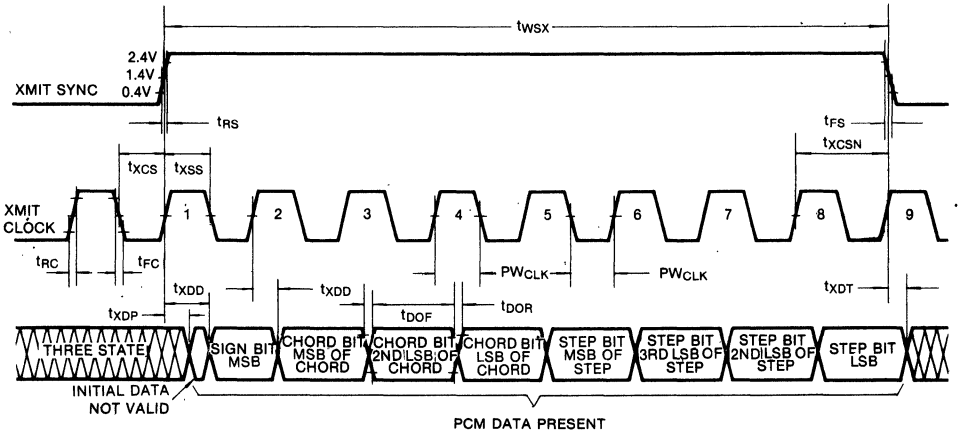


Fig. 2

RECEIVER SECTION TIMING

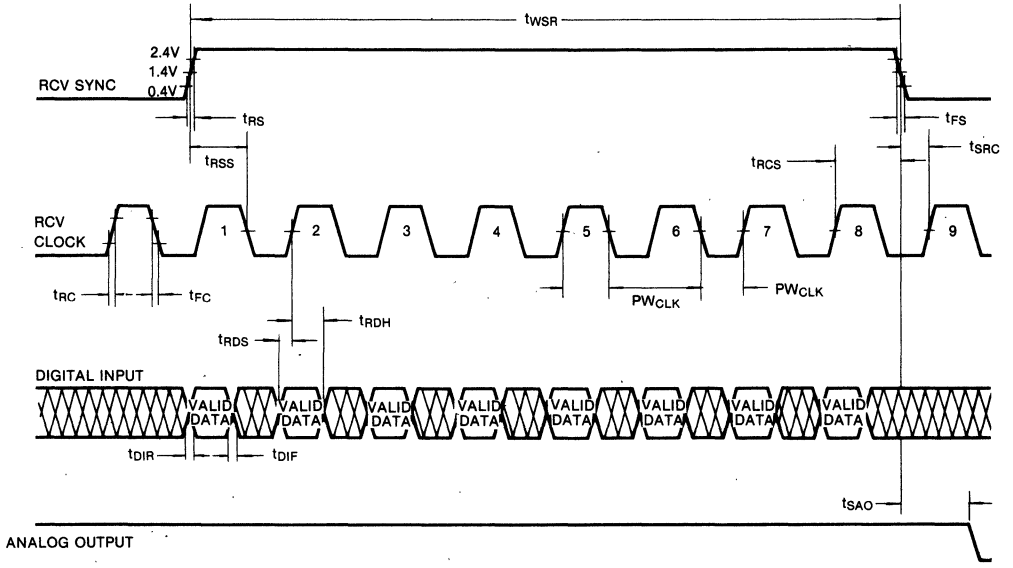


Fig. 3

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

S/D RATIO VS INPUT LEVEL

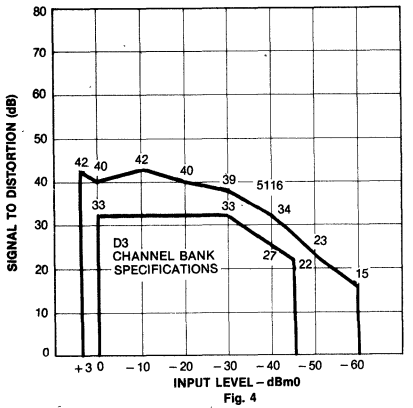


Fig. 4

GAIN TRACKING PERFORMANCE

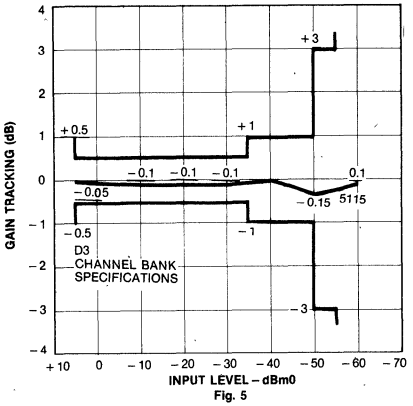


Fig. 5

A/D, D/A CONVERSION TIMING

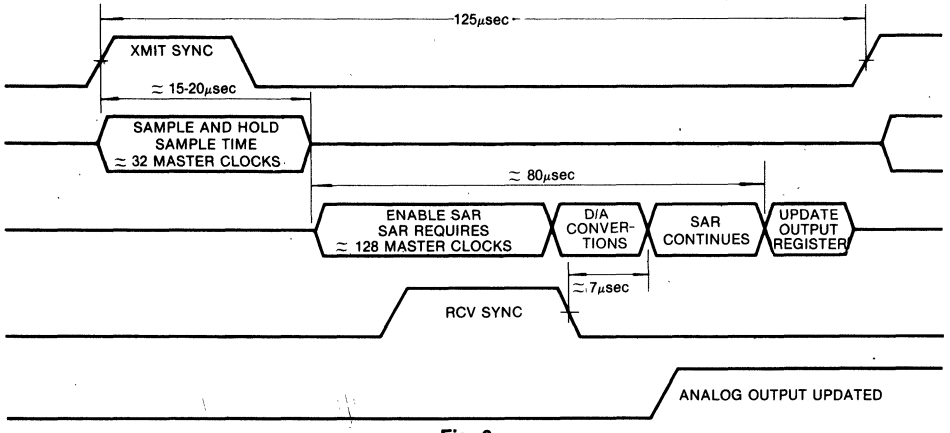


Fig. 6

DATA INPUT/OUTPUT TIMING

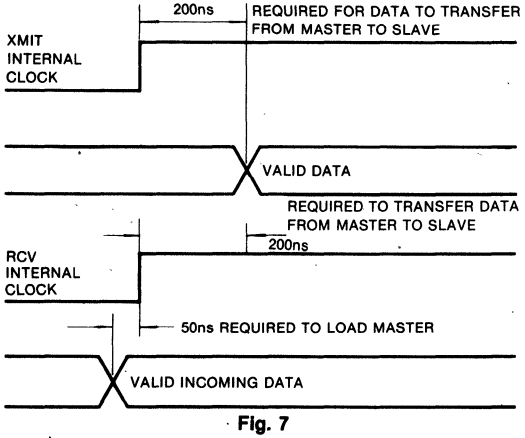
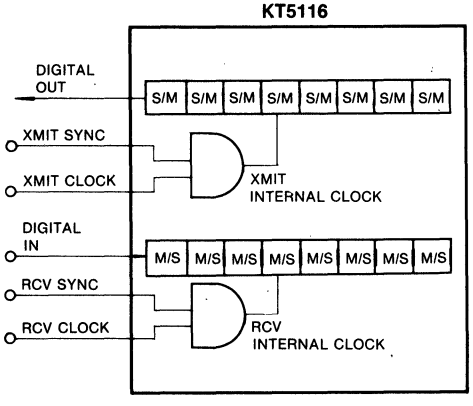


Fig. 7



KT5116 A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

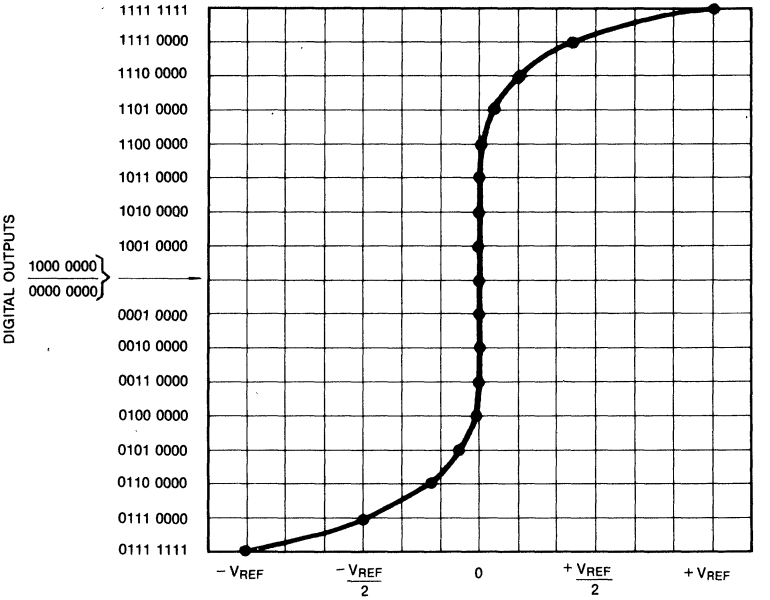


Fig. 8 ANALOG INPUT (VOLTS)

D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

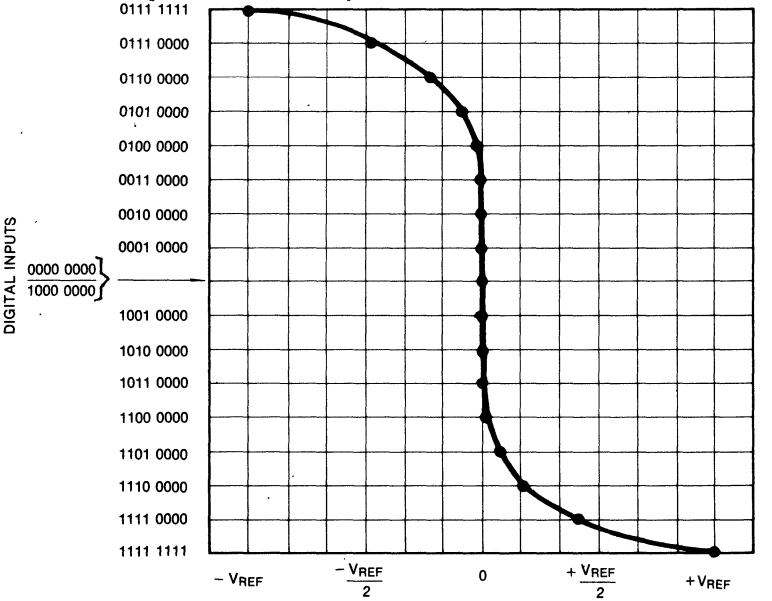


Fig. 9 ANALOG OUTPUT (VOLTS)

64KHz OPERATION, TRANSMITTER SECTION TIMING

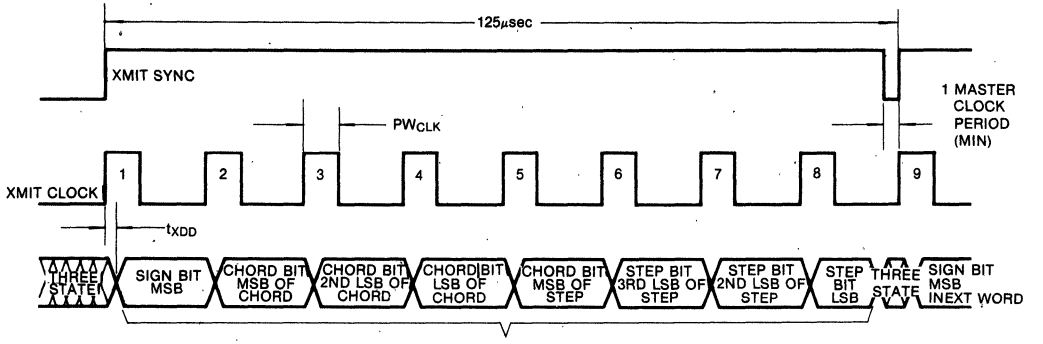


Fig. 10 PCM DATA PRESENT

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64KHz OPERATION, RECEIVER SECTION TIMING

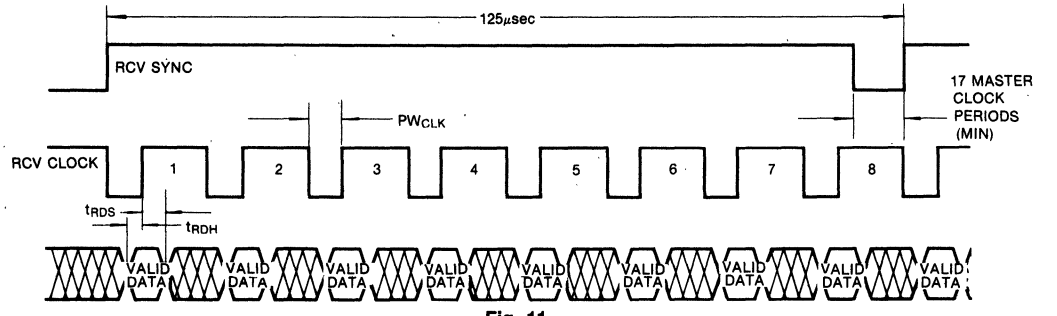
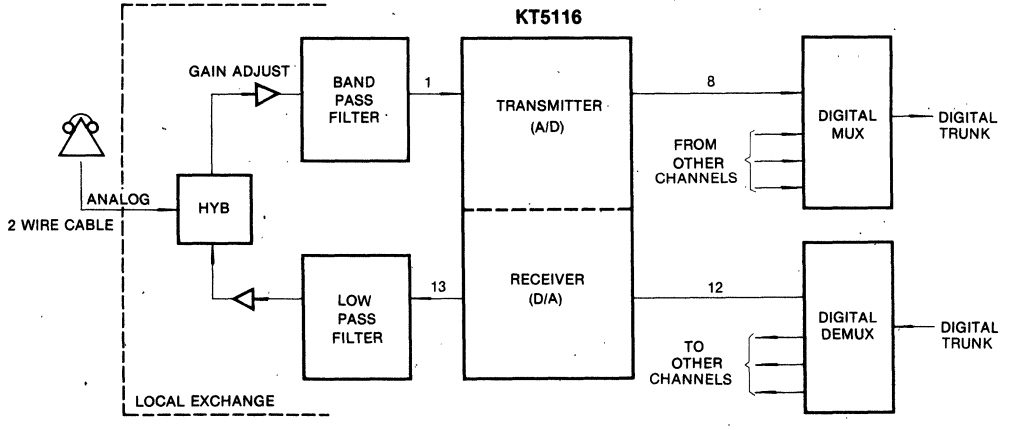


Fig. 11

Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

PCM SYSTEM BLOCK DIAGRAM



SYSTEM CHARACTERISTICS TEST CONFIGURATION

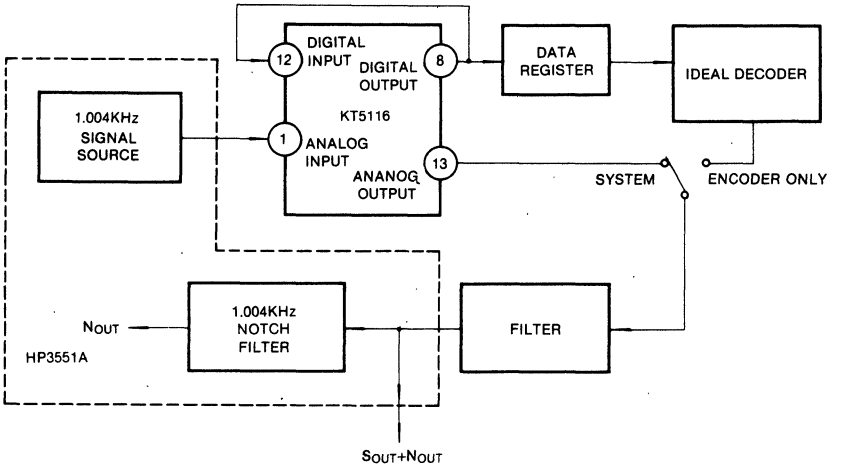


Fig. 12

Note: The ideal decoder consists of a digital decomponder and a 13-bit precision DAC.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 12 can be used to evaluate the performance of the KT5116. An analog signal provided by the HP3551 a transmission test set is connected to the Analog Input (Pin 1) of the KT5116. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A.

Remaining pins of the KT5116 are connected as follows:

1. RCV SYNC is tied to XMIT SYNC.
2. XMIT CLOCK is tied to Master CLOCK. The signal is inverted and tied to RCV clock.

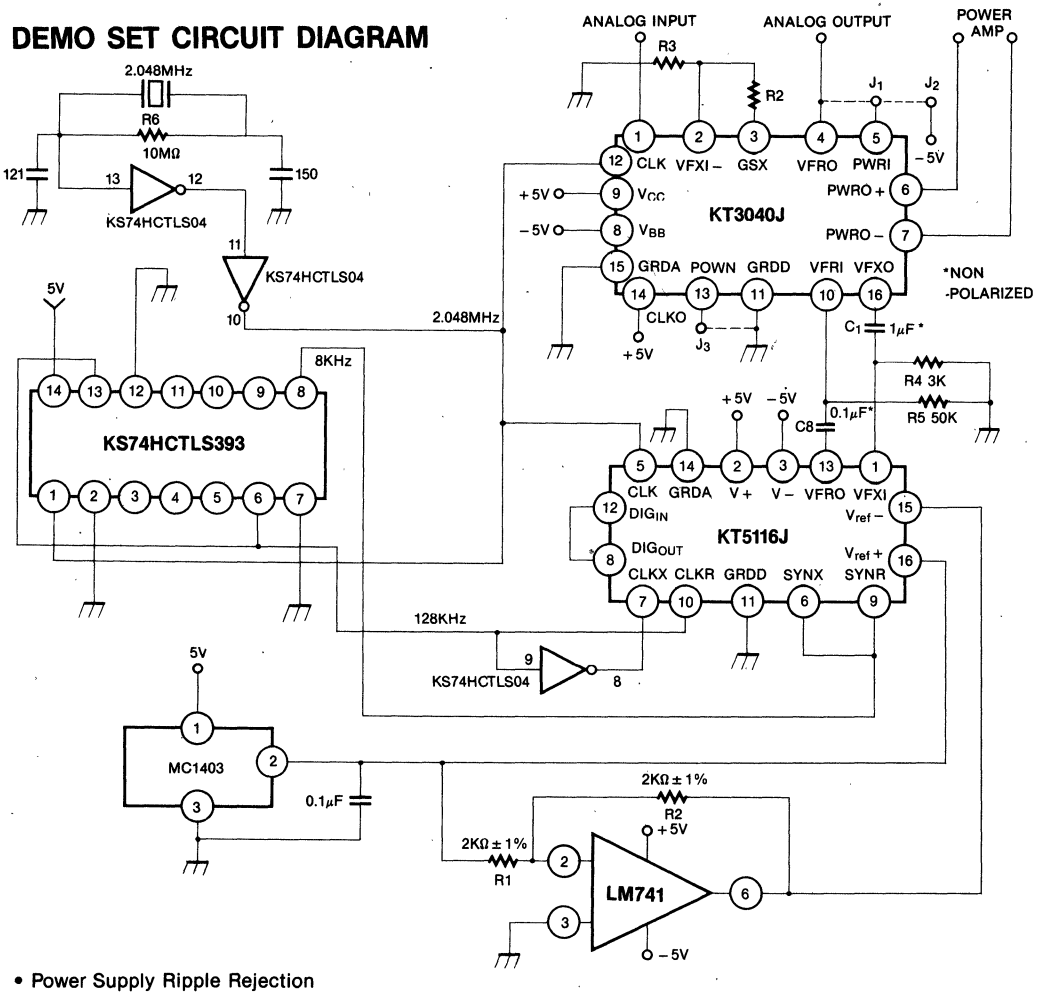
The following timing signals are required:

1. Master CLOCK=2.048MHz
2. XMIT SYNC repetition rate=8KHz
3. XMIT SYNC width=8 XMIT CLOCK periods.

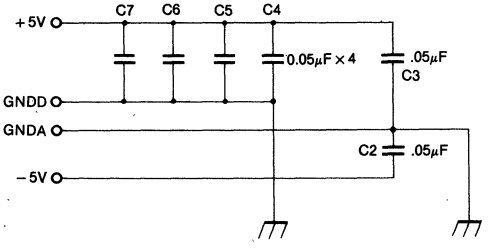
when all the above requirements are met, the set-up of Figure 12 permits the measurement of synchronous system performance over a wide range of Analog Inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the KT5116 independently of the decoder section. To test the system in the asynchronous mode, Master CLOCK should be separated from RCV CLOCK. XMIT CLOCK and RCV CLOCK are separated also separated.

DEMO SET CIRCUIT DIAGRAM



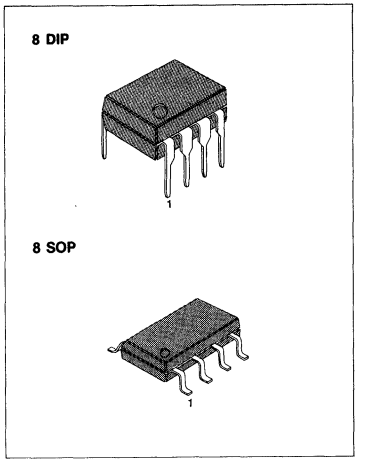
• Power Supply Ripple Rejection



NOTE: All unused input connected to GNDD or V_{CC}, only in HCT series.

TONE DECODER

The LM567C is a monolithic phase locked loop system designed to provide a saturated transistor switch to GND, when an input signal is present within the passband. External components are used to independently set center frequency bandwidth and output delay.



FEATURES

- **Wide frequency range (0.01Hz — 500kHz).**
- **Bandwidth adjustable from 0 to 14%**
- **Logic compatible output with 100mA current sinking capability.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by an external resistor.**

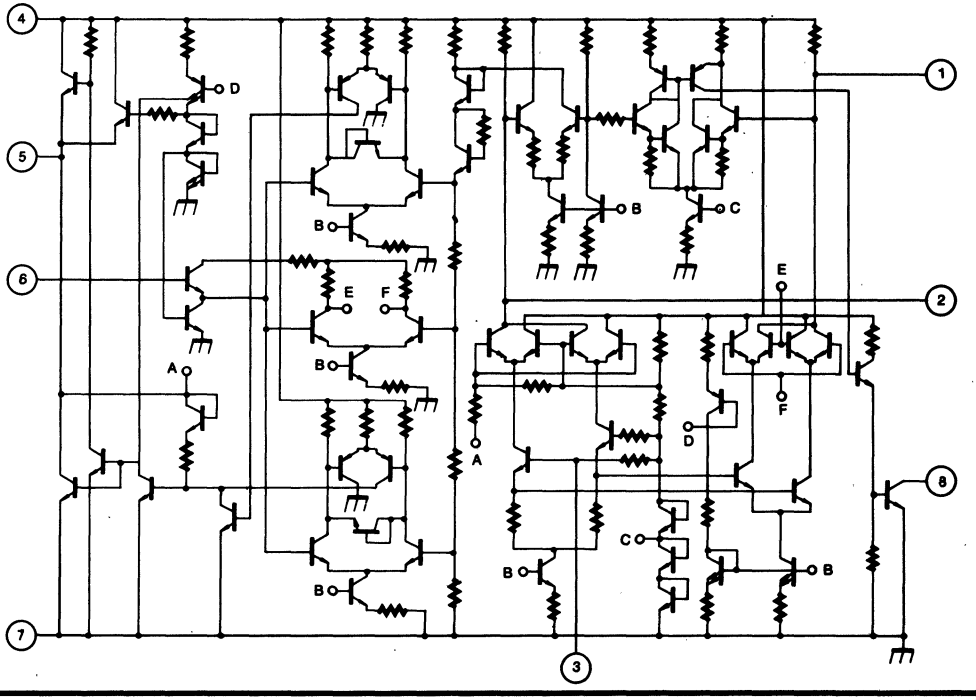
APPLICATIONS

- Touch Tone Decoder
- Wireless Intercom.
- Communications paging decoders
- Frequency monitoring and control.
- Ultrasonic controls (remote TV etc.)
- Carrier current remote controls.
- Precision oscillator.

ORDERING INFORMATION

Device	Package	Operating Temperature
LM567CN	8 DIP	0 ~ +70°C
LM567CD	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{CC}	10	V
Input Voltage	V_{IN}	−10 ~ V_{CC} +0.5	V
Output Voltage	V_O	15	V
Power Dissipation	Pd	300	mW
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, T_a=25°C unless other wise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}		4.75	5.0	9.0	V
Supply Current Quiescent	I_{CC}-1	R_L=20K		7	10	mA
Supply Current Activated	I_{CC}-2			12	15	mA
Quiescent Power Dissipation	P_{QD}			35		mW
Highest Center Frequency	H_{FO}	R_L=20K	100	500		KHz
Center Frequency Stability	F_{SE}	0°C to 70°C		35 ± 60		ppm/°C
Center Frequency Shift With Supply Voltage	F_{CS}			0.7	2	%/V
Largest Detection Bandwidth	B.W		10	14	18	% of fo
Largest Detection B.W Skew	B.Ws			2	3	% of fo
Largest Detection Bandwidth Variation With Supply Voltage	B.Wv	4.75 ~ 6.75V		±1	±5	%/V
Largest Detection Bandwidth Variation With Temperature	B.Wt			±0.1		%/°C
Input Resistance	R_{IN}			20		Kohm
Smallest Detectable Input Voltage	V_{IN}-1	I_L=100mA, fi=fo		20	25	mVrms
Largest No Output Input Voltage	V_{IN}-2		10	15		mVrms
Greatest Simultaneous Outband Signal To Inband Signal Ratio	S1/Sd	R_L=20k V_{IN}=300mV_{RMS} fi=fo=100KHz		+6		dB
Minimum Input Signal to Wideband Noise Ratio	S2/Sd	f_{i1}=140KHz f_{i2}=60KHz		−6		dB
Fastest On-Off Cycling Rate	F_{OUT}	R_L=20K		fo/20		
Output Leakage Current	I_{CO}	V_{IN}=25mV_{RMS}		0.01	25	μA
Output Saturaton Voltage	V_{SAT}-1	I_L=30mA, V_{IN}=25mVrms		0.2	0.4	V
	V_{SAT}-2	I_L=100mA, V_{IN}=25mVrms		0.6	1.0	V
Output Fall Time	T_F	R_L=50		30		nS
Output Rise Time	T_R	R_L=50		150		nS

CIRCUIT DESCRIPTION

The LM567C monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

BLOCK DIAGRAM

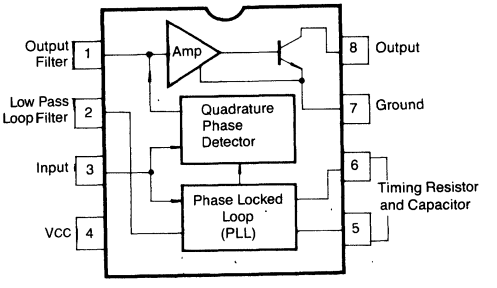


Fig. 1

DEFINITION OF LM567C PARAMETERS

CENTER FREQUENCY f_O

f_O is the free-running frequency of the C_L controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground f_O can be approximated by

$$f_O = \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BANDWIDTH (BW)

The detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically 20mVrms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_O, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_O C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

DETECTION BAND SKEW

The detection band skew is a measure of how accurately the largest detection band is centered about the center frequency, f_O. It is defined as $(f_{max} + f_{min} - 2f_O)/f_O$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment.

PIN DESCRIPTION

OUTPUT FILTER — C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not entical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be $\geq 2\ C_2$, where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

LOOP FILTER — C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567C The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements. For additional information see section on "Definition of LM567C Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_O, with a slope of approximately 20 mV/% frequency deviation.

INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} — 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 avoid disturbing the temperature stability or duty cycle of the oscillator.

LOGIC OUTPUT (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ $\leq$ 20 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the LM567C is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_O = 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_OC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200mV$ rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_OC_2 product.
3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminales spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. a typical minimum value of C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The LM567C is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. the system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

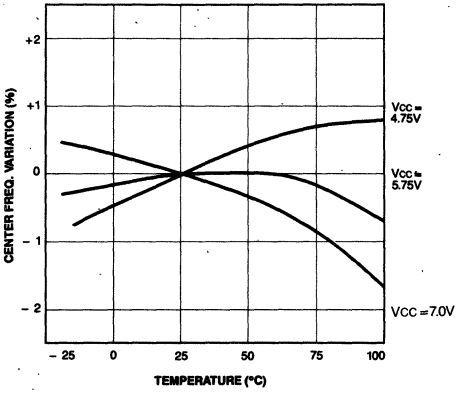
When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

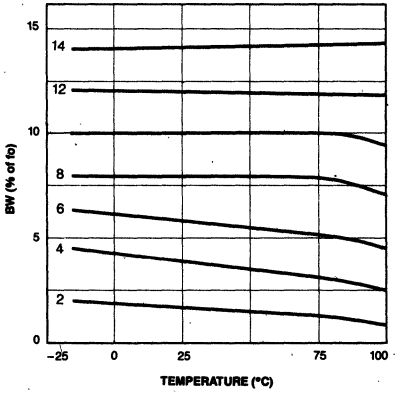
The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_O, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3

TYPICAL CHARACTERISTICS (Fig. 2)

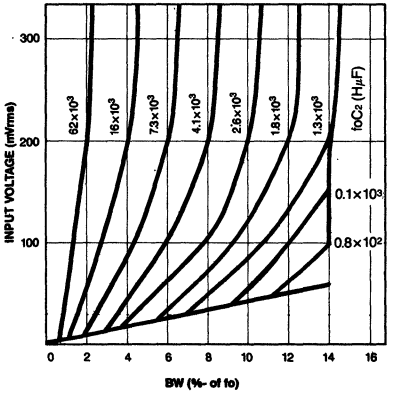
CENTER FREQ. VS TEMPERATURE



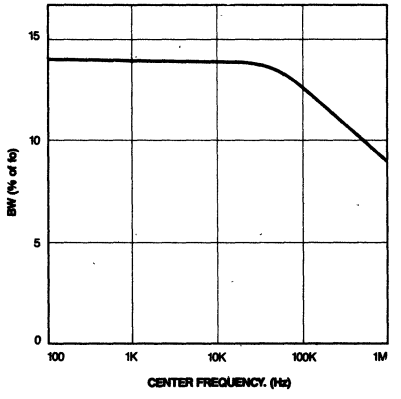
TYP. BW VS TEMPERATURE



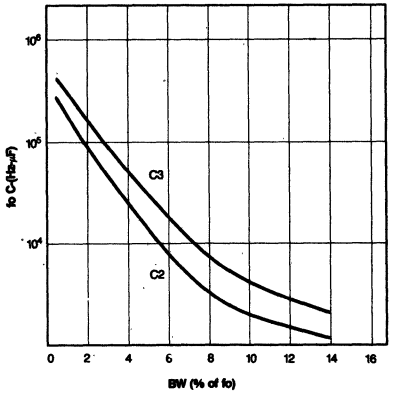
BW VS INPUT VOLTAGE.



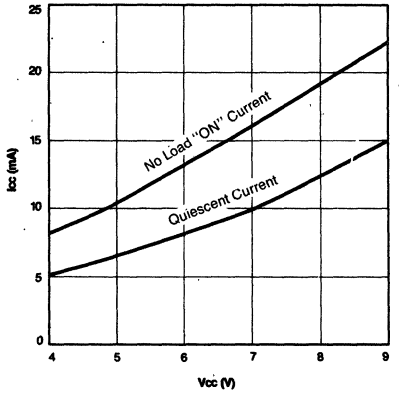
BW VS CENTER FREQUENCY



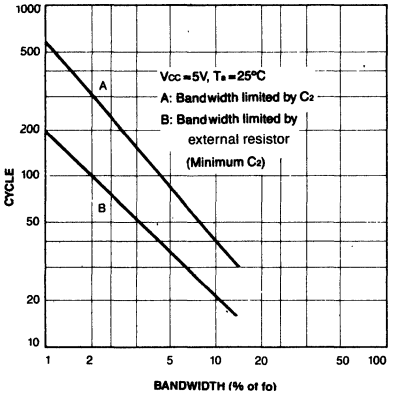
BW (C2, C3 CHARCT.)



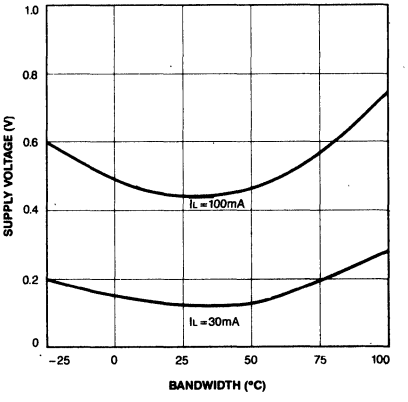
CURRENT DRAIN VS. VCC



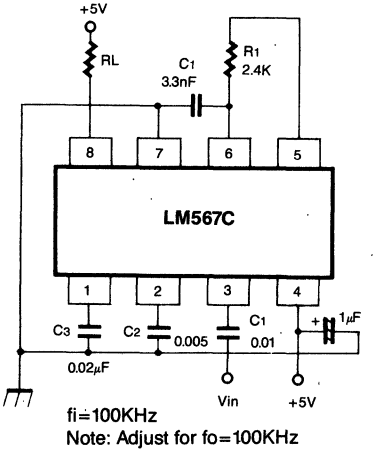
OPERATING CYCLE VS BANDWIDTH



OUTPUT SATURATION VOLTAGE VS AMBIENT TEMPERATURE



AC TEST CIRCUIT

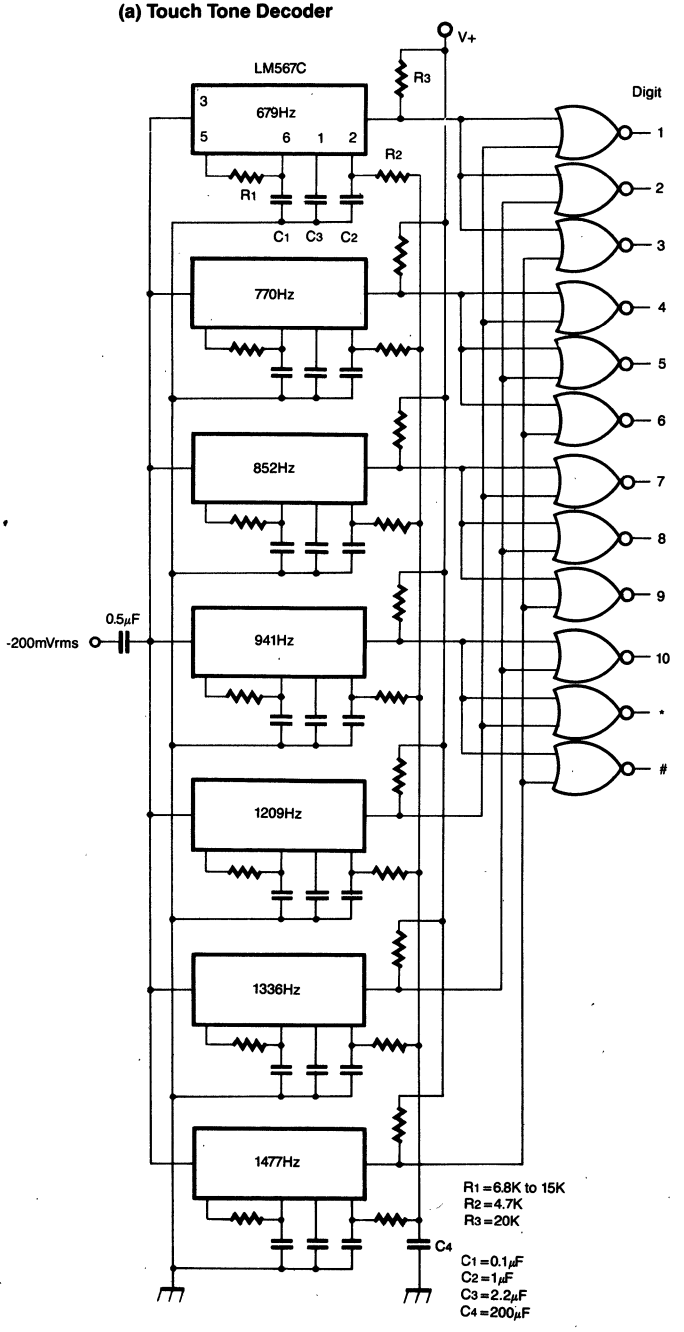


fi=100KHz
Note: Adjust for fo=100KHz

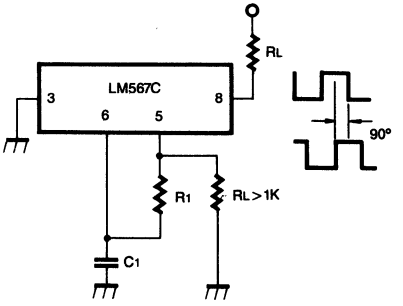
Fig. 2

APPLICATION CIRCUIT

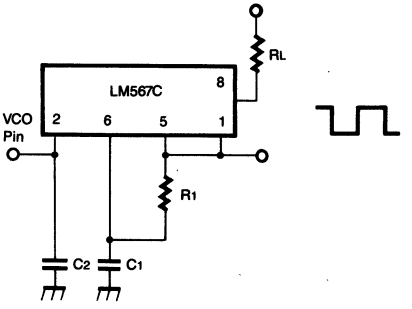
(a) Touch Tone Decoder



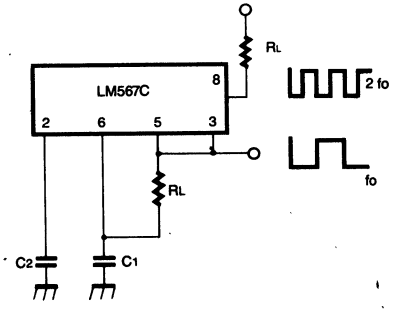
(b) 2-Phase Oscillator



(c) Variable Oscillator

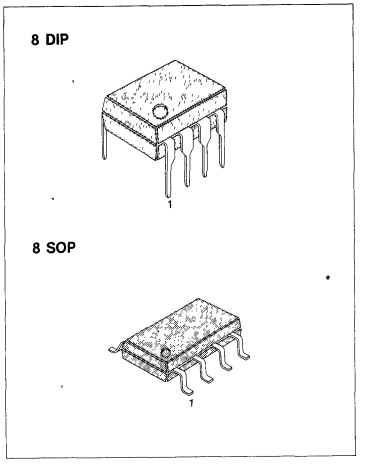


(d) Frequency Doubler



MICROPOWER TONE DECODER

The LM567L is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the LM567L can replace the popular 567 type decoder with only minor component value changes. The LM567L offers approximately 1/10th the power dissipation of the conventional 567 type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4mW at 5 volts.



FEATURES

- **Very low power dissipation (4mW at 5V)**
- **Bandwidth adjustable from 0 to 14% of f_o**
- **Logic compatible output with 10mA current sinking capability.**
- **Highly stable center frequency.**
- **Center frequency adjustable from 0.01Hz to 60KHz.**
- **Inherent immunity to false signals.**
- **High rejection of out-of-band signals and noise.**
- **Frequency range adjustable over 20:1 range by external resistor.**

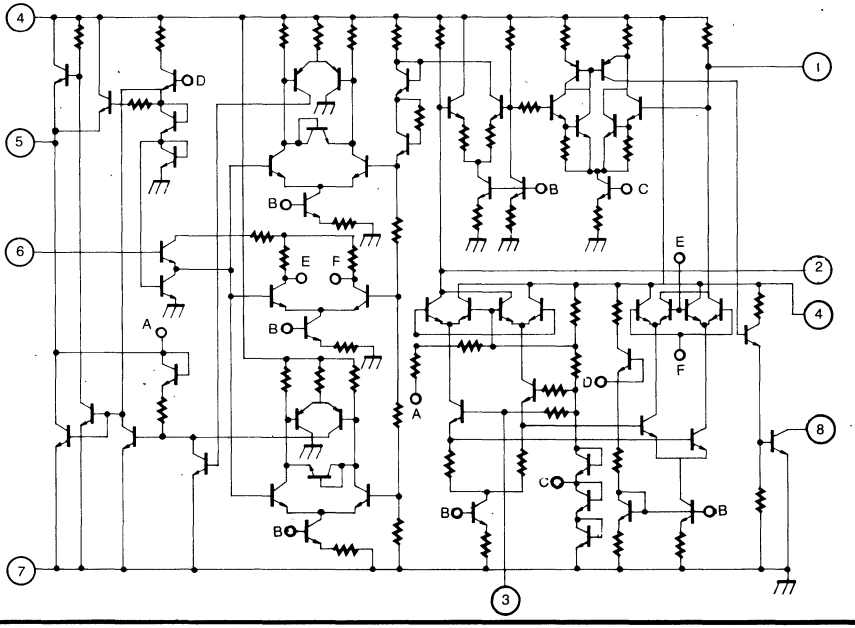
APPLICATIONS

- **Battery-operated tone detection**
- **Sequential tone decoding**
- **Ultrasonic remote-control**
- **Touch-tone decoding**
- **Communications paging**
- **Telemetric decoding**

ORDERING INFORMATION

Device	Package	Operating Temperature
LM567LN	8 DIP	0 ~ +70°C
LM567LD	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

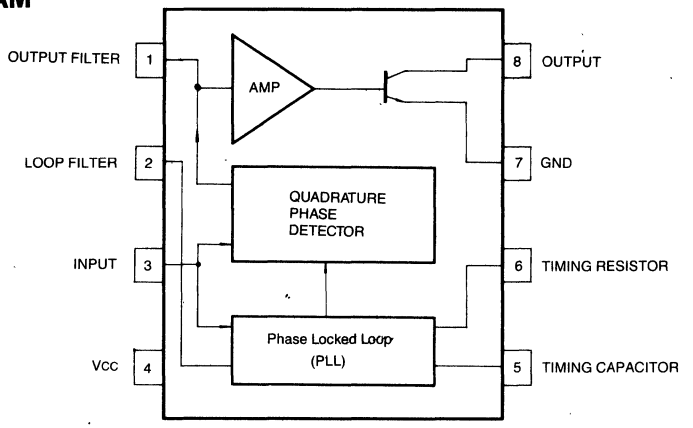
Characteristic	Symbol	Value	Unit
Power Supply	V_{CC}	10	V
Power Dissipation			
Plastic Package	P_d	300	mW
Derate Above +25°C		2.5	mW/°C
Operating Temperature	Topr	0 ~ +70	°C
Storage Temperature	Tstg	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_a = 25°C, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}		4.75		8.0	V
Supply Current/Quiescent	I_{CC-1}	R_L = 20KΩ,		0.6	1.0	mA
Supply Current/Activated	I_{CC-2}	R_L = 20KΩ, V_{IN} = 300mV, $f_i = f_o$		0.8	1.4	mA
Highest Center Frequency	H_{fo}	R1 = 3KΩ − 5KΩ	10	60		KHz
Center Frequency Drift Temperature						
0 < T_a < 70°C		See Figures 15 and 16		−150		ppm/°C
Supply Voltage		f_o = 10KHz, V_{CC} = 4.75−5.75		0.5	3.0	%/V
Largest Detection Bandwidth	B.W	f_o = 10KHz, V_{IN} = 300mV_{rms} R_L = 20KΩ	10	14	18	% of f_o
Largest Detection Bandwidth Skew	B.Ws	See Figure 4 for Definition		2	3	% of f_o
Largest Detection Bandwidth Variation With Temperature	B.Wt	V_{IN} = 300mV_{rms}, R_L = 20KΩ		±0.1		%/°C
Largest Detection Bandwidth Variation With Supply Voltage	B.Wv	V_{IN} = 300mV_{rms}, R_L = 20KΩ		±0.2		%/V
Input Resistance	R_{IN}			100		KΩ
Smallest Detectable Input Voltage	V_{IN-1}	I_L = 10mA, $f_i = f_o$ = 10KHz		20	25	mV_{rms}
Largest No-Output Input Voltage	V_{IN-2}	IL = 10mA, $f_i = f_o$ = 10KHz	10	15		mV_{rms}
Greatest Simultaneous Outband Signal to Inband Signal Ratio	S_1/S_d	V_{IN} = 300mV, f_i'1 = 6KHz $f_i = f_o$ = 10KHz		+6		dB
Minimum Input Signal to Wideband Noise Ratio	S_2/S_d	V_{IN} = 300mV, f_i'2 = 14KHz $f_i = f_o$ = 10KHz		−6		dB
Output Saturation Voltage	V_{SAT-1}	IL = 2mA, V_{IN} = 25mV_{rms}		0.2	0.4	V
	V_{SAT-2}	IL = 10mA, V_{IN} = 25mV_{rms}		0.3	0.6	V
Output Leakage Current	I_{CO}			0.01	25	μA
Fastest On/Off Cycling Rate	F_{OUT}	fi = fo = 10KHz	f_o/20			
Output Rise Time	T_r	R_L = 1KΩ		780		nS
Output Fall Time	T_f	R_L = 1KΩ		100		nS

BLOCK DIAGRAM



TEST CIRCUIT

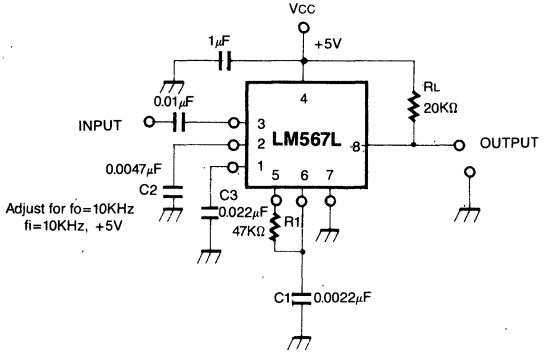


Fig. 1

TYPICAL APPLICATION CIRCUIT

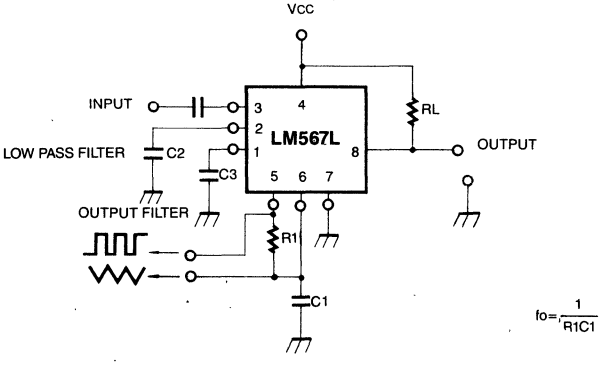


Fig. 2

CIRCUIT DESCRIPTION

The LM567L monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillater which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100KΩ nominal input resistance). Free running frequency is controlled by an RC network at pins 5 and 6. A capacitor on pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependent upon the circuitry here. Pin 4 is $+V_{CC}$ (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The LM567L is pin-for-pin compatible with the standard LM567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

PRINCIPLES OF OPERATION

The LM567L is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature detector, a voltage comparator, and an output logic driver.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the DC voltage at the output of the detector is shifted. This DC level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic output at Pin 8 is an "open-collector" NPN transistor stage capable of switching 10mA current loads.

The logic output at Pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at Pin 8 goes to a "low" state.

Fig 3 shows the typical output response of the circuit for a tone-burst applied to the input, within the detection band.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R1 and C1 connected to Pins 5 and 6, as shown in Fig 2.

The detection bandwidth is determined by the size of the PLL filter capacitor, C2 (see Fig 10); and the output response speed is controlled by the output filter capacitor, C3.

DEFINITION OF DEVICE PARAMETERS

CENTER FREQUENCY f_O

f_O is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R1 between Pins 5 and 6, and capacitor C1 from Pin 6 to ground, f_O can be approximated by

$$f_O = \frac{1}{R1C1}\ \text{Hz}$$ where R1 is in ohms and C1 is in farads.

DETECTION BANDWIDTH (BW)

The largest detection bandwidth is the frequency range centered about f_O, within which an input signal larger than the threshold voltage (typically $20mV_{rms}$) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass loop filter at Pin 2. Typical dependence of detection bandwidth on the filter capacitance and the input signal amplitude is shown in Figs 10 and 11, or may be calculated by the approximation.

$$B{\cdot}W\ (\%) = 338\sqrt{\frac{V_i\ (RMS)}{f_O\ (Hz){\cdot}C_2\ (\mu F)}}$$

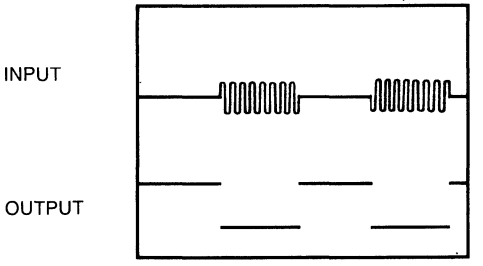
LARGEST DETECTION BANDWIDTH

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BANDWIDTH SKEW

The detection bandwidth skew is a measure of how accurately the largest detection band is centered about the center frequency f_o. This parameter is graphically illustrated in Fig 4. In the figure, f_{min} and f_{max} correspond to the lower and the upper ends of the largest detection band, and f1 corresponds to the apparent center of the detection band, and is defined as the arithmetic average of fmin and fmax and f_O is the free running frequency of the LM567L oscillator section. The bandwidth skew Δf_X is the difference between these frequencies. Normalized to f_o, this bandwidth skew can be expressed as:

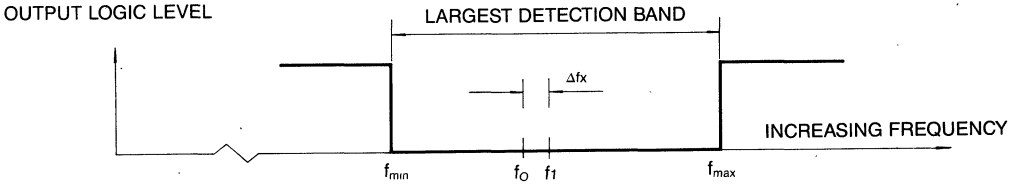
$$\text{Bandwidth Skew} = \frac{\Delta fx}{f_O} = \frac{(fmax + fmin - 2\,f_O)}{2\,f_O}$$



Response to $100mV_{rms}$ tone burst. $R_L = 1K\Omega$

Fig. 3. Typical Output Response to 100mV Input Tone-Burst

If necessary, the detection bandwidth skew can be reduced to zero by an optional centering adjustment. (see optional controls.)



f_O = PLL free-running frequency
f1 = Center freq of detection band = $(f_{max} + f_{min})/2$

Fig. 4. Definition of Bandwidth Skew

PIN DESCRIPTION AND EXTERNAL COMPONENTS

PIN 3: INPUT

The input signal is applied to Pin 3 through a coupling capacitor. This terminal is internally biased at a DC level 2 volts above ground, and has an input impedance level of approximately 100KΩ.

PIN 5 and 6: TIMING RESISTOR R1 and CAPACITOR C1

The center frequency of the decoder is set by resistor R1 between Pins 5 and 6, and capacitor C1 from Pin 6 to ground, as shown in Fig 2.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC}-1.4V and an average DC level of V_{CC}/2.A 5KΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of=(V_{CC}-1.3)/3.5 volts and an average DC level of V_{CC}/2. Only high impedance loads should be connected to Pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

PIN 2: LOOP FILTER-C2

Capacitor C2 connected from Pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the LM567L. The filter time constant is given by T2=R2C2, where R2 (100KΩ) is the impedance at Pin 2.

The selection of C2 is determined by the detection bandwidth requirements, as shown in Fig 10. For additional information see section on "Definition of Device Parameters."

The voltage at Pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 f_O to 1.05 f_O, with a slope of approximately 20mV/% frequency deviation.

PIN 1: OUTPUT FILTER-C3

Capacitor C3 connected from Pin 1 to ground forms a simple low-pass post detection filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as T3=R3C3, where R3 (47KΩ) is the internal impedance at Pin 1.

If the value of C3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output (Pin 8).

The average voltage (during lock) at Pin 1 is a function of the in-band input amplitude in accordance with the given transfer characteristic.

PIN 8: LOGIC OUTPUT

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, open-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, RL, connected from Pin 8 to the positive supply.

When an in-band signal is present the output transistor at Pin 8 saturates with a collector voltage of less than 0.6V at full rated output current of 10mA. If large output voltage swings are needed, RL can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤15 volts.

OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the LM567L is shown in Fig 2. For most applications, the following procedure will be sufficient for determination of the external components R1, C1, C2, and C3.

1. R1 and C1 should be selected for the desired center frequency by the expression $f_O \approx 1/R1C2$. For optimum temperature stability, R1 should be selected such that 20KΩ ≤ R1 ≤200KΩ, and the R1C1 product should have sufficient stability over the projected operating temperature range.
2. Low-pass capacitor, C2, can be determined from the bandwidth versus input signal amplitude graph of Fig 10. One approach is to select an area of operation from the graph, and then adjust the input level and value of C2 accordingly. Or if the input amplitude variation is known, the required f_O C2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200mV_{rms}$. Then, as noted on the graph, bandwidth will be controlled solely by the f_O C2 product.
3. Capacitor C3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C3 is 2 C2.

   Conversely, if C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C3 passes the threshold value.

PRECAUTIONS

1. The LM567L will lock on signals near (2n+1) f_O and produce an output for signals near (4n+1) f_O, for n=0, 1, 2 etc. Signals at 5 f_O and 9 f_O can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.
2. Operating the LM567L in a reduced bandwidth mode of operation at input levels less than $200mV_{rms}$ results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Fig 13.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the LM567L in the high input level mode, above 200mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit becomes sensitive to signals at $f_O/3$, $f_O/5$ etc.
4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

OPTIONAL CONTROLS

PROGRAMMING

Varying the value of resistor R1 and/or capacitor C1 will change the center frequency. The value of R1 can be changed either mechanically or by solid state switches. Additional C1 capacitors can be added by grounding them through saturated npn transistors.

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transients becomes greater. Thus maximum operating speed is obtained when the value of capacitor C2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C2 and C3, in microfarads, which allow the maximum operating speeds for various center frequencies where f_O is Hz.

$$C2 = \frac{13}{f_O}, \quad C3 = \frac{26}{f_O} \ \mu F$$

The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_O/10$ baud. In situations where minimum turn-off is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Fig 5 can be used to bring the quiescent C3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

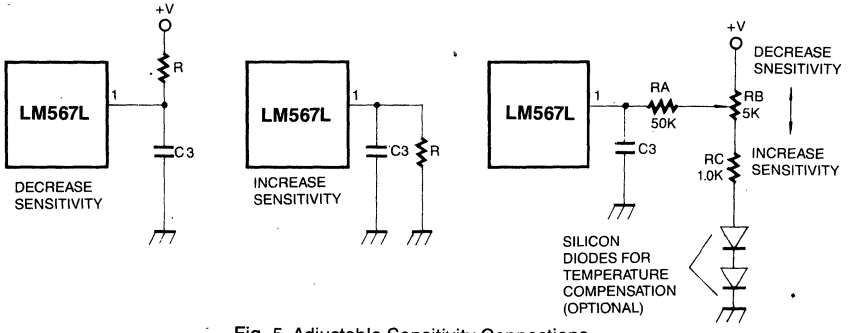


Fig. 5. Adjustable Sensitivity Connections

CHATTER

When the value of C3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (Pin 1) or, by increasing the size of capacitor C3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Fig 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

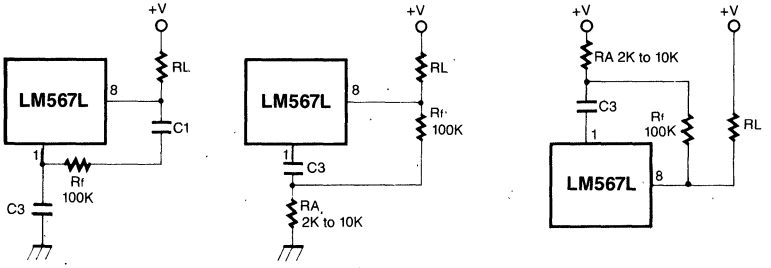


Fig. 6. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Fig 7 can be used to change the position of the detection band (capture range) within the largest detection band (lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only, since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

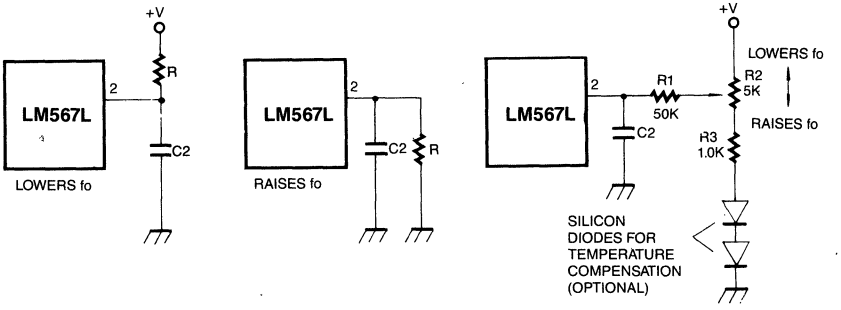


Fig. 7. Detection Band Skew Adjustment

TYPICAL PERFORMANCE CHARACTERISTICS

FIG 8. SUPPLY CURRENT
V_S SUPPLY VOLTAGE

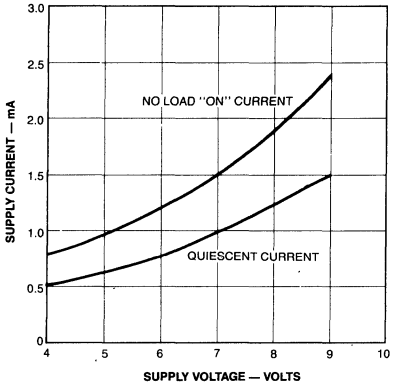


FIG 9. LARGEST DETECTION BANDWIDTH
V_S OPERATING FREQUENCY

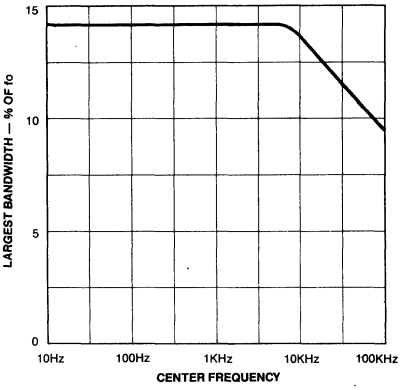


FIG 10. DETECTION BANDWIDTH
V_S A FUNCTION OF C2 AND C3

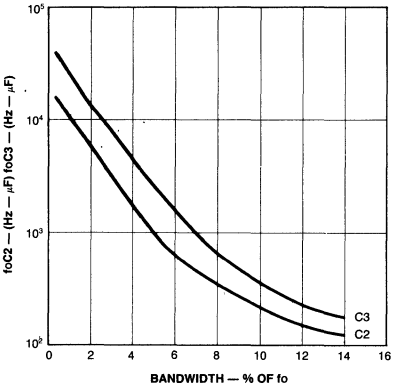


FIG 11. BANDWIDTH V_S INPUT SIGNAL
AMPLITUDE (C2 IN μF)

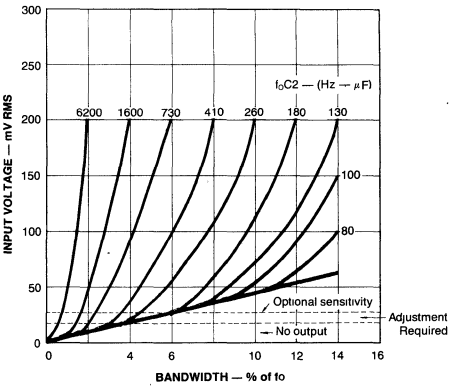


FIG 12. BANDWIDTH VARIATION
WITH TEMPERATURE

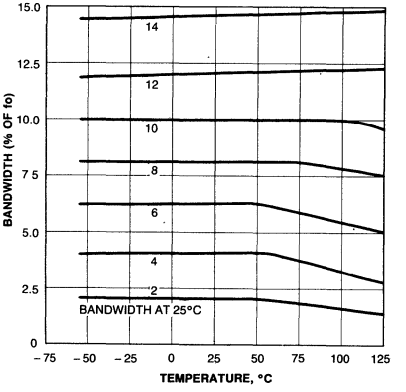


FIG 13. GREATEST NUMBER OF
CYCLES BEFORE OUTPUT

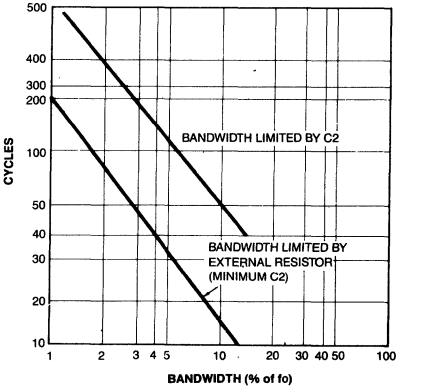


FIG 14. POWER SUPPLY DEPENDENCE OF CENTER FREQUENCY

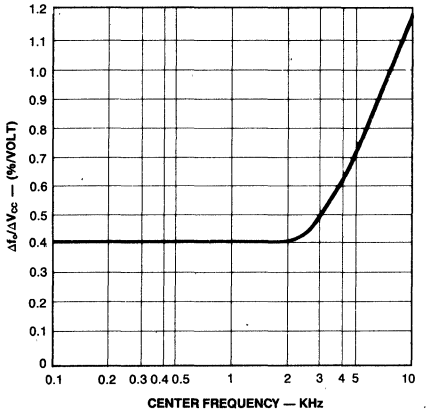


FIG 15. TYPICAL CENTER FREQUENCY DRIFT WITH TEMPERATURE(V_{CC} = 5V, R1 = 80kΩ, fo = 1KHz)

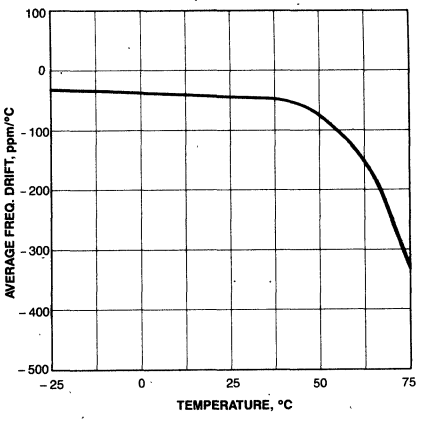
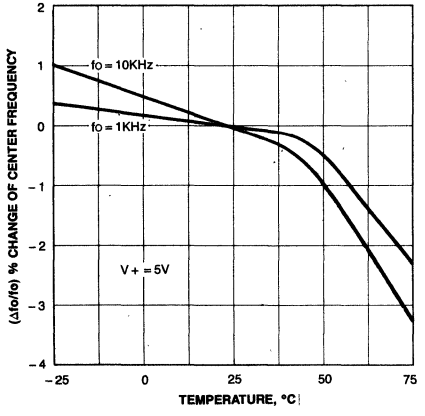
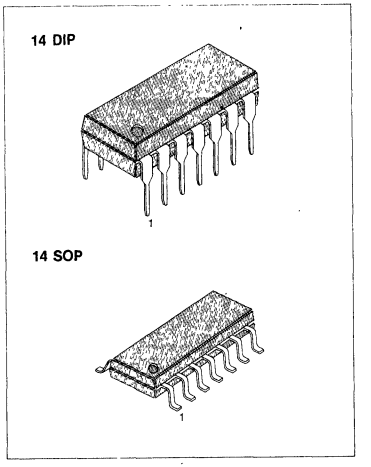


FIG 16. TYPICAL FREQUENCY DRIFT AS A FUNCTION OF TEMPERATURE



QUAD LINE DRIVER

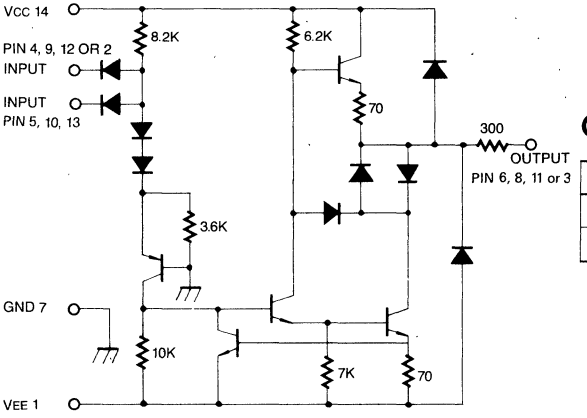
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.



FEATURES

- **Current Limited Output: ± 10mA typ**
- **Power-Off Source Impedance: 300 Ohms (min)**
- **Simple Slew Rate Control with External Capacitor**
- **Flexible Operating Supply Range**
- **Compatible with DTL and TTL, HCTLS Families**

SCHEMATIC DIAGRAM (1/4 of Circuit Shown)



ORDERING INFORMATION

Device	Package	Operating Temperature
MC1488N	14 DIP	0 ~ + 70°C
MC1488D	14 SOP	

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C unless otherwise noted)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+ 15 − 15	V_{DC}
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	V_{DC}
Output Signal Voltage	V_D	± 15	V_{DC}
Power Dissipation	P_D	1000	mW
Derate Above T_a = + 25°C	$1/R\theta_{JA}$	6.7	mW/°C
Operating Temperature Range	T_a	0 ~ + 70	°C
Storage Temperature Range	Tstg	− 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 9.0±1%V, V_{EE} = −9.0 ± 1%V, T_a = 0 ~ 70°C unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Input Current 1	I_{IL}	Low Logic State (V_{IL} = 0)		1.0	1.6	mA	1
Input Current 2	I_{IH}	High Logic State (V_{IH} = 5.0V)			10	μA	1
Output Voltage-High Logic State	V_{OH}	V_{IL} = 0.8V, R_L = 3.0KΩ V_{CC} = 9.0V, V_{EE} = −9.0V	6	7		V	2
		V_{IL} = 0.8V, R_L = 3.0KΩ V_{CC} = 13.2V, V_{EE} = −13.2V	9	10.5			
Output Voltage-Low Logic State	V_{OL}	V_{IH} = 1.9V, R_L = 3.0KΩ V_{CC} = 9.0V, V_{EE} = −9.0V	−6	−7		V	2
		V_{IH} = 1.9V, R_L = 3.0KΩ V_{CC} = 13.2V, V_{EE} = −13.2V	−9	−10.5			
Output Short Circuit Current	I_{OS+}	Positive	6	10	12	mA	3
Output Short Circuit Current	I_{OS-}	Negative	−6	−10	−12	mA	3
Output Resistance	R_O	V_{CC} = V_{EE} = 0, V_O = ±2.0V	300			Ω	
Positive Supply Current (RL=∞)	I_{CC}	V_{IH} = 1.9V, V_{CC} = +9.0V		15	20	mA	5
		V_{IL} = 0.8V, V_{CC} = +9.0V		4.5	6		
		V_{IH} = 1.9V, V_{CC} = +12V		19	25		
		V_{IL} = 0.8V, V_{CC} = +12V		5.5	7		
		V_{IH} = 1.9V, V_{CC} = +15V			34		
		V_{IL} = 0.8V, V_{CC} = +15V			12		
Negative Supply Current (RL=∞)	I_{EE}	V_{IH} = 1.9V, V_{EE} = −9.0V		−13	−17	mA	5
		V_{IL} = 0.8V, V_{EE} = −9.0V			−15	μA	
		V_{IH} = 1.9V, V_{EE} = −12V		−18	−23	mA	
		V_{IL} = 0.8V, V_{EE} = −12V			−15	μA	
		V_{IH} = 1.9V, V_{EE} = −15V			−34	mA	
		V_{IL} = 0.8V, V_{EE} = −15V			−2.5	mA	
Power Consumption	P_C	V_{CC} = 9.0V, V_{EE} = −9.0V			333	mW	
		V_{CC} = 12V, V_{EE} = −12V			576		

* Maximum package power dissipation may be exceeded if all outputs are shorted simultaneously.

SWITCHING CHARACTERISTICS

(V_{CC} = 9.0±1%V, V_{EE} = −9±1%V, T_a = 0 ~ 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit	Fig
Propagation Delay Time	t_{PLH}	Z_L = 3.0K and 15pF		275	350	nS	6
Fall Time	t_{THL}	Z_L = 3.0K and 15pF		45	75	nS	6
Rise Time	t_{TLH}	Z_L = 3.0K and 15pF		55	100	nS	6
Propugation Delay Time	t_{PHL}	Z_L = 3.0K and 15pF		110	175	nS	6

DC TEST CIRCUIT

FIGURE 1 INPUT CURRENT

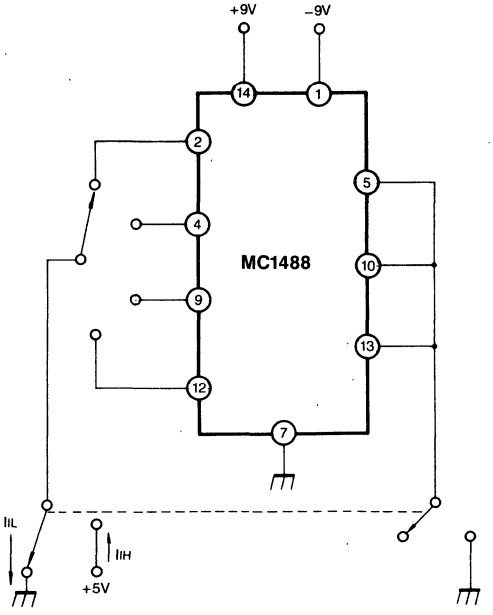


FIGURE 2 OUTPUT VOLTAGE

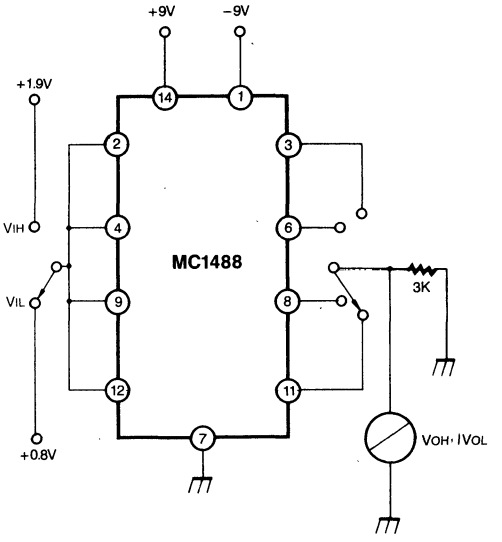


FIGURE 3 OUTPUT SHORT CIRCUIT CURRENT

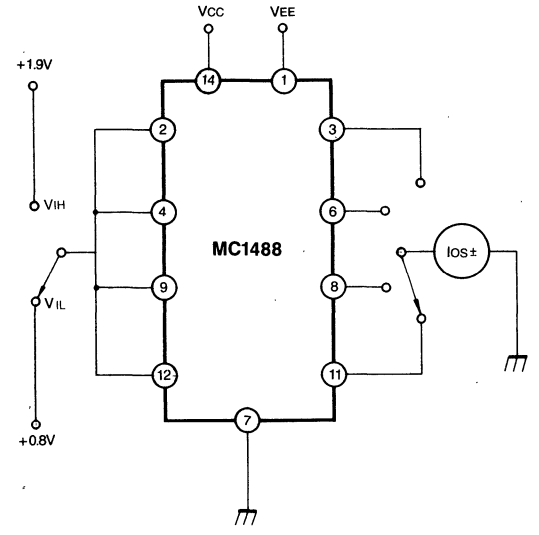


FIGURE 4 OUTPUT RESISTANCE (POWER OFF)

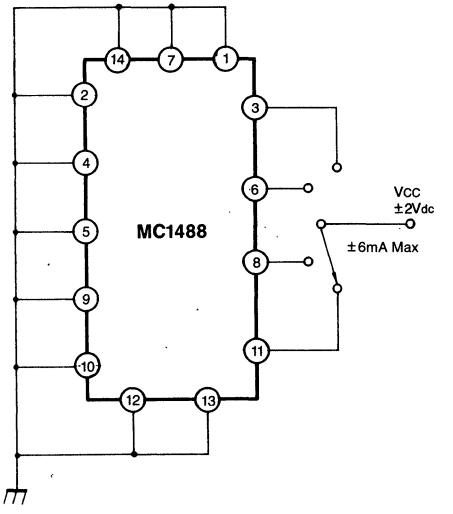


FIGURE 5 POWER SUPPLY CURRENTS

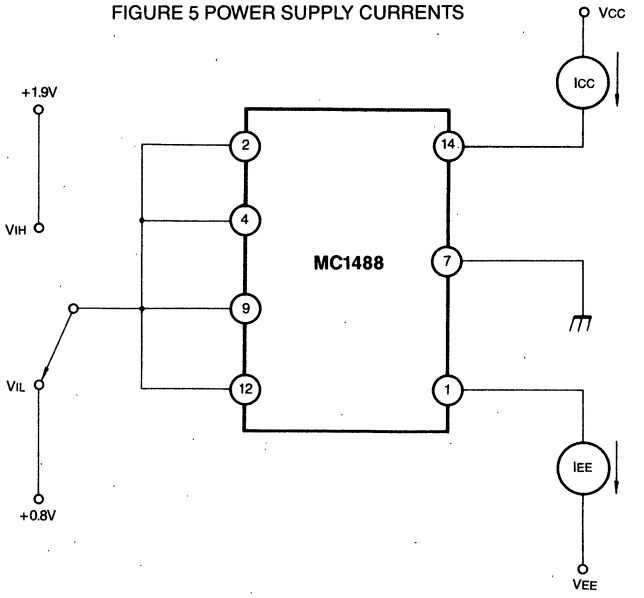
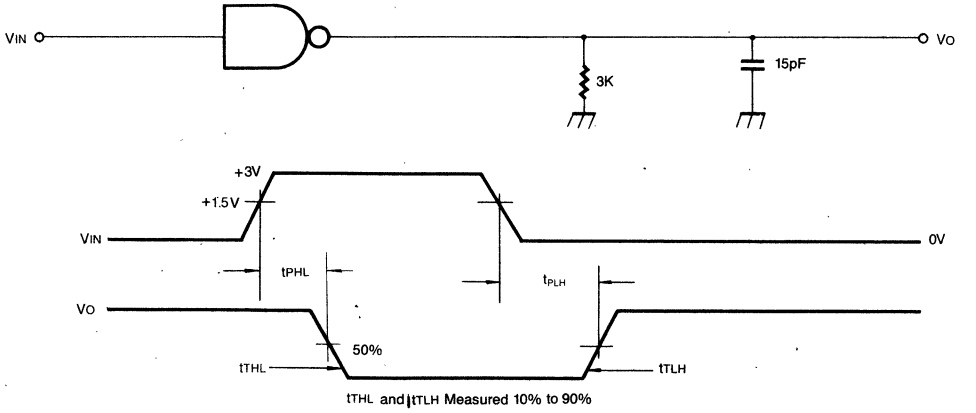


FIGURE 6 SWITCHING RESPONSE



TYPICAL PERFORMANCE CHARACTERISTICS

FIGURE 7 — TRANSFER CHARACTERISTICS V_S POWER-SUPPLY VOLTAGE

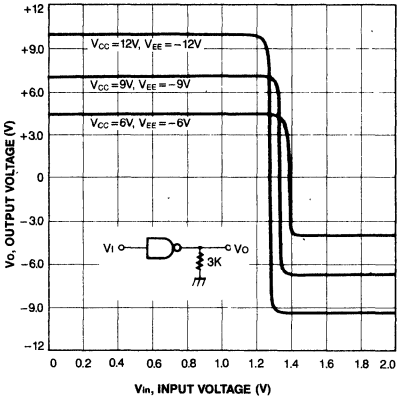


FIGURE 8 — SHORT CIRCUIT OUTPUT CURRENT V_S TEMPERATURE

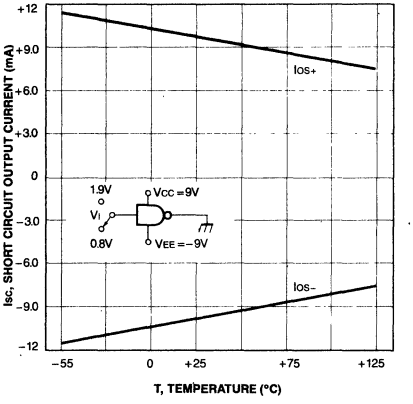


FIGURE 9 — OUTPUT SLEW RATE V_S LOAD CAPACITANCE

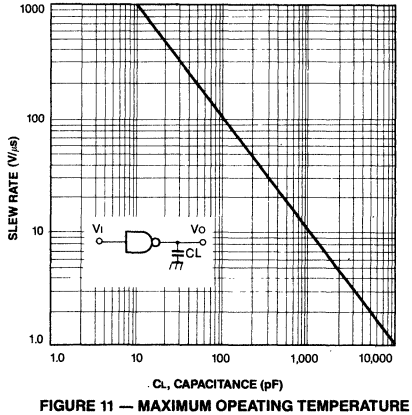


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT LIMITING CHARACTERISTICS

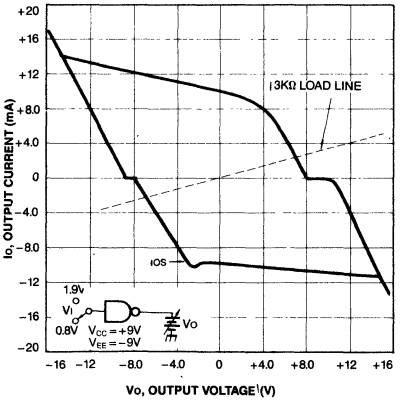
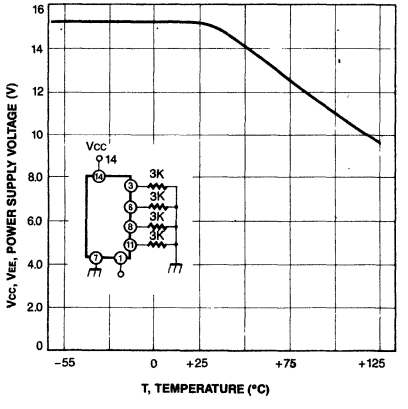


FIGURE 11 — MAXIMUM OPEATING TEMPERATURE V_S POWER SUPPLY VOLTAGE



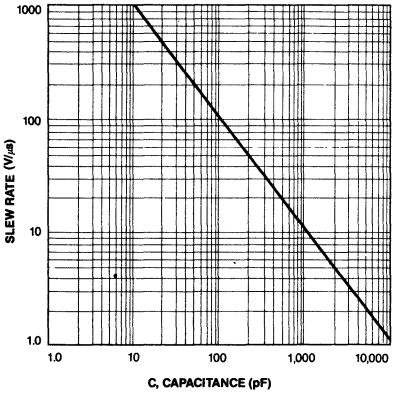
APPLICATION INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489/A quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the

FIGURE 12 — SLEW RATE Vs CAPACITANCE FOR I_{SC} = 10mA



device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate or 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V:$V_{EE} \leq -9.0$V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low

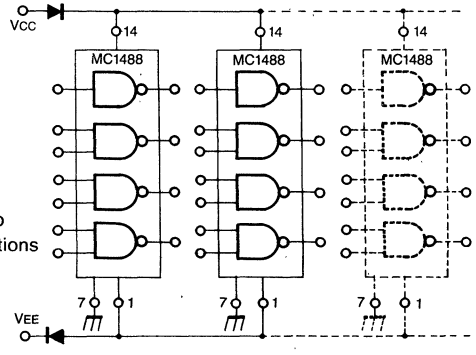


Fig. 13 — Power supply protection to meet power-off fault conditions

impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 8, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300mV above ground MOS input level limit.

2. Power-Supply Range — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately −2.5 volts to the minimum specified the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation.Figure 15 shows one such combination.

FIGURE 14 DTL/TTL-TO-MOS TRANSLATOR

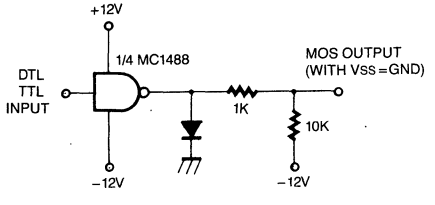
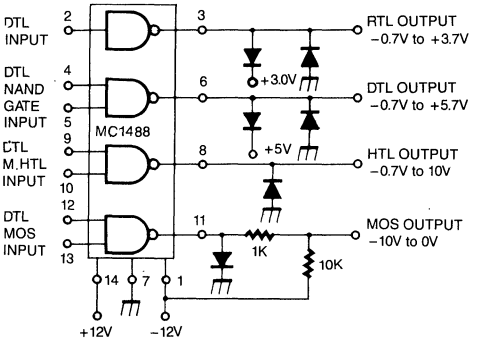
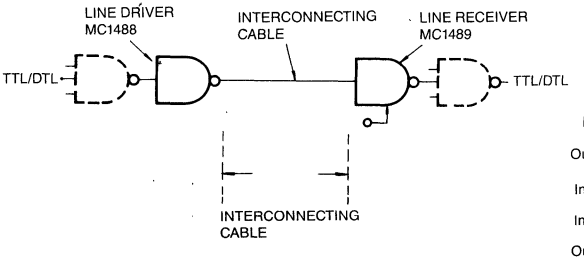


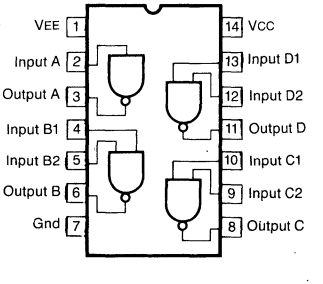
FIGURE 15 LOGIC TRANSLATOR APPLICATIONS



TYPICAL APPLICATION

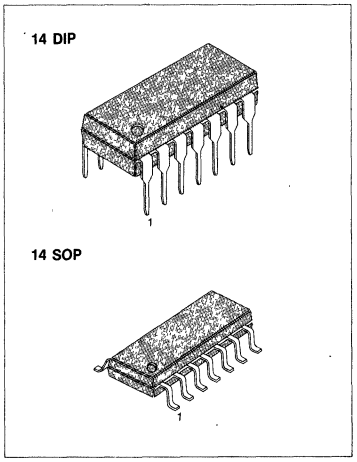


PIN CONNECTIONS



QUAD LINE RECEIVER

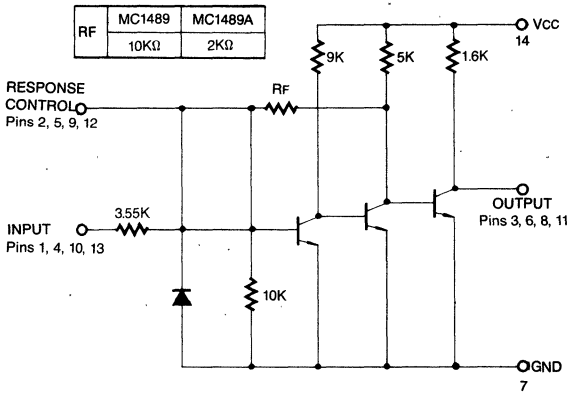
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.



FEATURES

- **Input Resistance — 3.0KΩ to 7.0KΩ**
- **Input Signal Range — ±30 Volts**
- **Response Control**
  - **a) Logic Threshold Shifting**
  - **b) Input Noise Filtering**
- **Input Threshold Hysteresis Built in**

SCHEMATIC DIAGRAM
(1/4 OF CIRCUIT SHOWN)



ORDERING INFORMATION

Device	Package	Operating Temperature
MC1489N	14 DIP	0 ~ +70°C
MC1489AN		
MC1489D	14 SOP	
MC1489AD		

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	V_{DC}
Input Voltage Range	V_{IR}	±30	V_{DC}
Output Load Current	I_L	20	mA
Power Dissipation Derate Above T_a = +25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Temperature	T_a	0 to +70	°C
Storage Temperature	Tstg	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 10%V, T_a = 0 ~ 70°C unless otherwise noted)

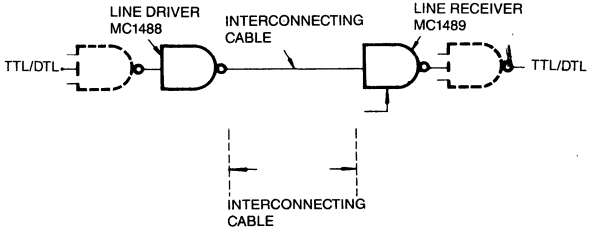
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Input Current	I_{IH}	V_{IH} = 25Vdc	3.6		8.3	mA
		V_{IH} = 3.0Vdc	0.43			
Negative Input Current	I_{IL}	V_{IL} = −25Vdc	−3.6		−8.3	mA
		V_{IL} = −3.0Vdc	−0.43			
Input Turn-On Thereshold Voltage MC1489 MC1489A	V_{IH}	T_a = 25°C, $V_{OL} \leq$ 0.45V	 1.0 1.75	 1.95	 1.5 2.25	Vdc
Input Turn-Off Threshold Voltage	V_{IL}	T_a = 25°C, $V_{OH} \geq$ 2.5V, I_L = 0.5mA	0.75		1.25	Vdc
Output Voltage High	V_{OH}	V_{IH} = 0.75V, I_L = −0.5mA	2.5	4.0	5.0	Vdc
		Input Open, I_L = −0.5mA	2.5	4.0	5.0	
Output Voltage Low	V_{OL}	V_{IL} = 3.0V, I_L = 10mA		0.2	0.45	Vdc
Output Short Circuit Current	I_{OS}			−3.0	−4.0	mA
Power Supply Current	I_{CC}	All gates "on", I_{OUT} = 0mA, V_{IH} = 5.0V		16	26	mA
Power Consumption	P_C	V_{IH} = 5.0V		80	130	mW

SWITCHING CHARACTERISTICS

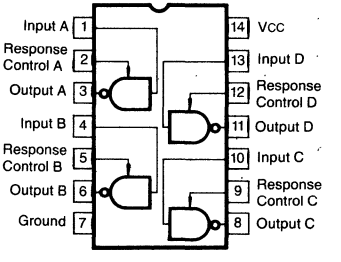
(V_{CC} = 5.0 ± 1%V, T_a = 25°C, See Fig. 1)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PLH}	R_L = 3.9KΩ		25	85	nS
Rise Time	t_{TLH}	R_L = 3.9KΩ		120	175	nS
Propagation Delay Time	t_{PHL}	R_L = 390Ω		25	50	nS
Fall Time	t_{THL}	R_L = 390Ω		10	20	nS

TYPICAL APPLICATION

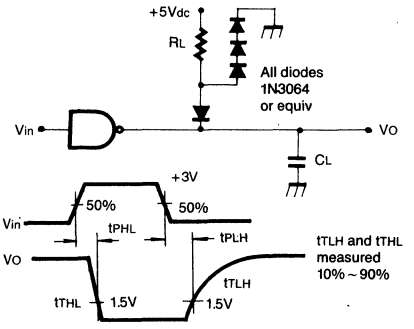


PIN CONNECTIONS



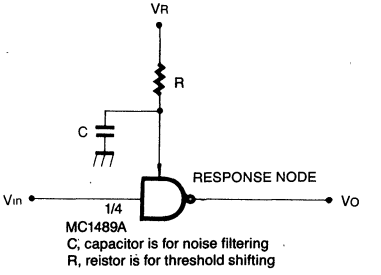
TEST CIRCUIT

Fig 1 — SWITCHING RESPONSE



CL=15pF=total parasitic capacitance, which includes probe and wiring capacitances

Fig 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering
R, reistor is for threshold shifting

TYPICAL PERFORMANCE CHARACTERISTICS

(VCC=5.0 Vdc Ta=+25°C unless otherwise noted)

Fig. 3 — TYPICAL TURN-ON THRESHOLD V_S CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

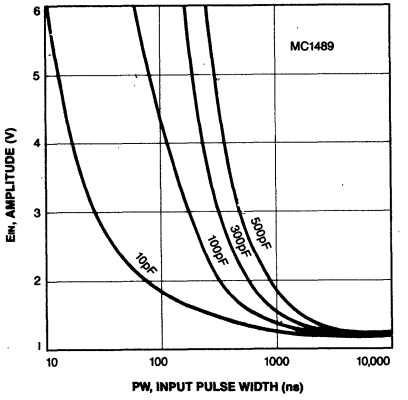


Fig. 4 — TYPICAL TURN-ON THRESHOLD V_S CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

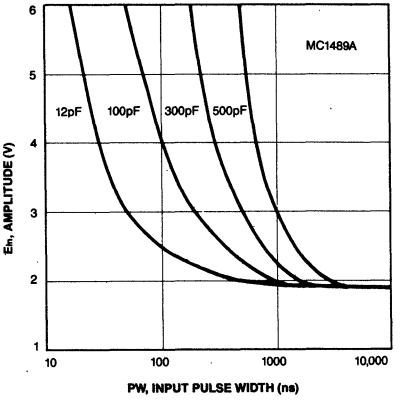


Fig. 5 — INPUT CURRENT

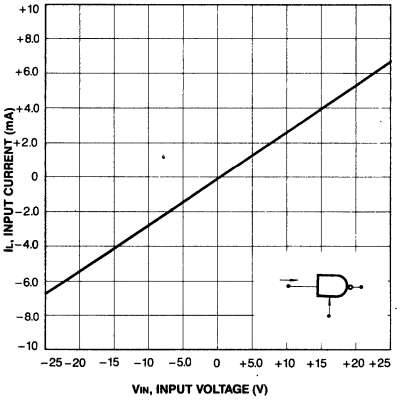


Fig. 6 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

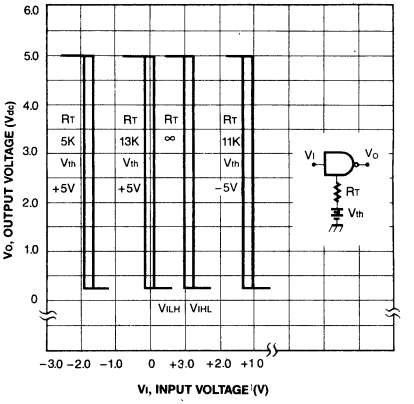


Fig. 7 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

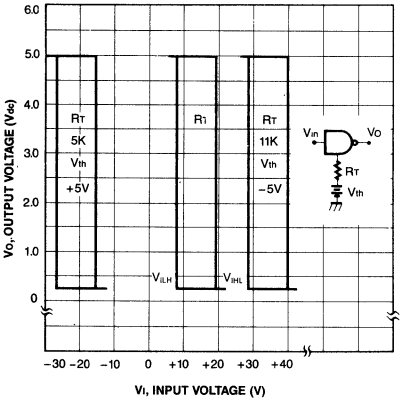


Fig. 8 — INPUT THRESHOLD VOLTAGE Vs. TEMPERATURE

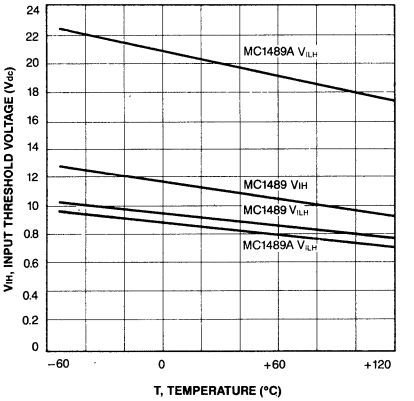
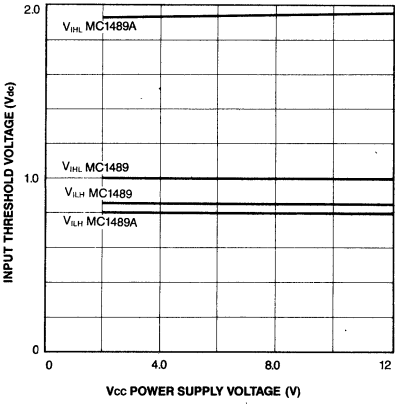


Fig. 9 — INPUT THRESHOLD Vs. POWER SUPPLY VOLTAGE



3

APPLICATION INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0". On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1". For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for typical hysteresis of 250mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 6 and 7 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 3 and 4 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and DTL/TTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 9).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure10 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

Fig. 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

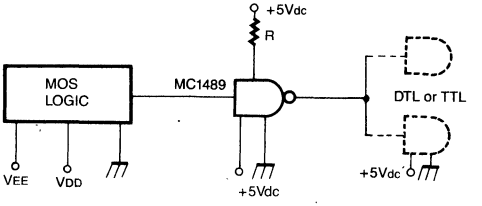
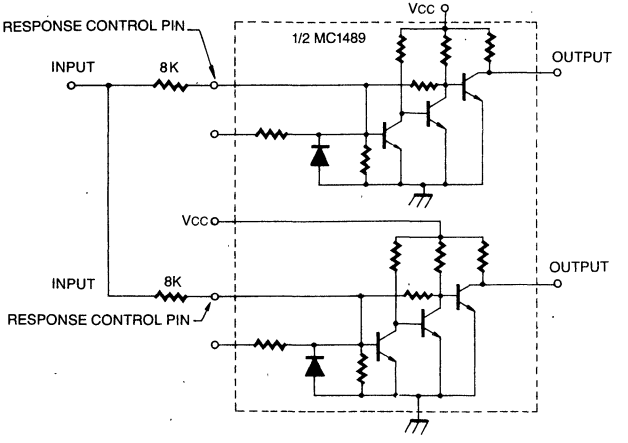


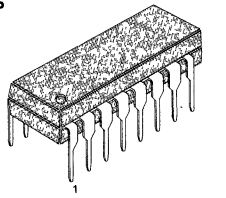
Fig. 11 — TYPICAL PARALLELING OF TWO MC1489/A RECEIVERS TO MEET RS-232C



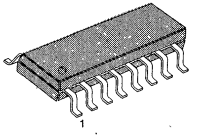
LOW POWER NARROW BAND FM IF

The MC3361 is designed for use in FM dual conversion communication equipment. It contains a complete narrow band FM demodulation system operable to less than 2.5V supply voltage.

16 DIP



16 SOP



FEATURES

- **Includes: Oscillator, Mixer, Limiting Amp, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch**
- **Stable operation with wide supply voltage (2.5V to 7.0V)**
- **Low drain current (4.0mA Typ. at V_{CC}=4.0V)**
- **Excellent Input Sensitivity (−3dB limiting, 2.0μVrms Typ.)**
- **Minimum number of external parts required.**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC3361N	16 DIP	−20 ~ +70°C
MC3361D	16 SOP	

BLOCK DIAGRAM

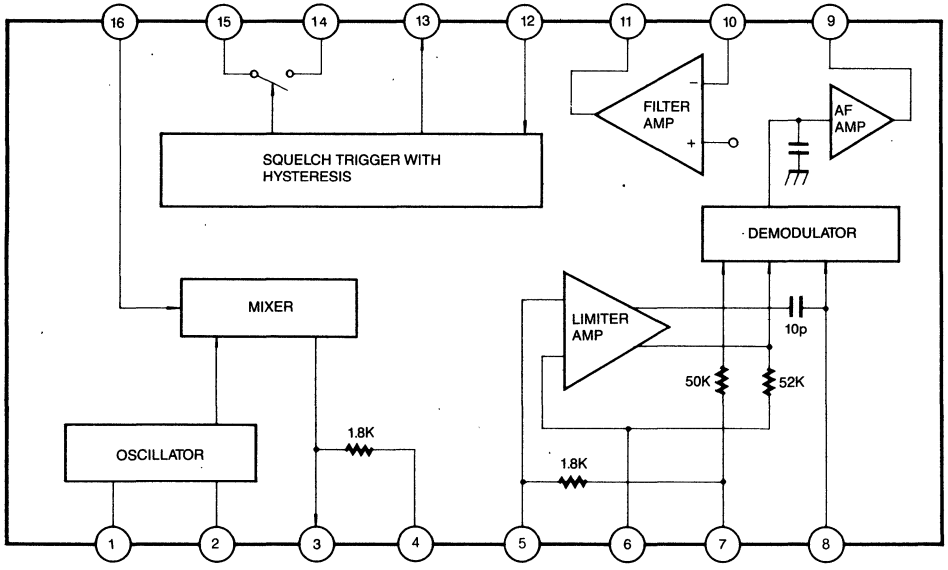


Fig. 1

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Detector Input Voltage	V_D	1.0	V_{P-P}
Input Voltage ($V_{CC} \geq 4.0V$)	V_{16}	1.0	Vrms
Mute Function	V_{14}	−0.5 ~ +5.0	Vpeak
Operating Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

3

ELECTRICAL CHARACTERISTICS

(V_{CC}=4.0V, fo=10.7MHz, Δf= ±3KHz, f_{mod}=1KHz, T_a=25°C, Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	I_{CC}	Squelch Off Squelch On		4.0 6.0		mA
Input Limiting Voltage	V_{INL}	−3dB Limiting		2.0		μV
Detector Output Voltage	V_7			2.0		V
Detector Output Impedance	Z_{OD}			400		ohm
Recovered Audio Output Voltage	V_O	V_{IN}=10mV	100	150		mVrms
Filter Gain	A_{VF}	f=10KHz, V_{IN}=5mV	40	48		dB
Filter Output Voltage	V_{OF}			1.5		V
Trigger Hysteresis	V_{TH}			50		mV
Mute Function Low	R_{OL}			10		ohm
Mute Function High	R_{OH}			10		Mohm
Scan Function Low	V_{13L}	Mute Off (V_{12}=2V)			0.5	V
Scan Function High	V_{13H}	Mute On (V_{12}=GND)	3.0			V
Mixer Conversion Gain	A_{VM}			24		dB
Mixer Input Resistance	R_I			3.3		Kohm
Mixer Input Capacitance	C_I			2.2		pF

PIN CONNECTIONS

Pin 1: Oscillator
Pin 2: Oscillator
Pin 3: Mixer Output
Pin 4: Vcc
Pin 5: Limiter Input
Pin 6: Decoupling
Pin 7: Limiter Output
Pin 8: Quad Coil
Pin 9: Recovered Audio Output
Pin 10: Filter Input
Pin 11: Filter Output
Pin 12: Squelch In
Pin 13: Scan Control
Pin 14: Mute
Pin 15: GND
Pin 16: Mixer Input

TEST CIRCUIT

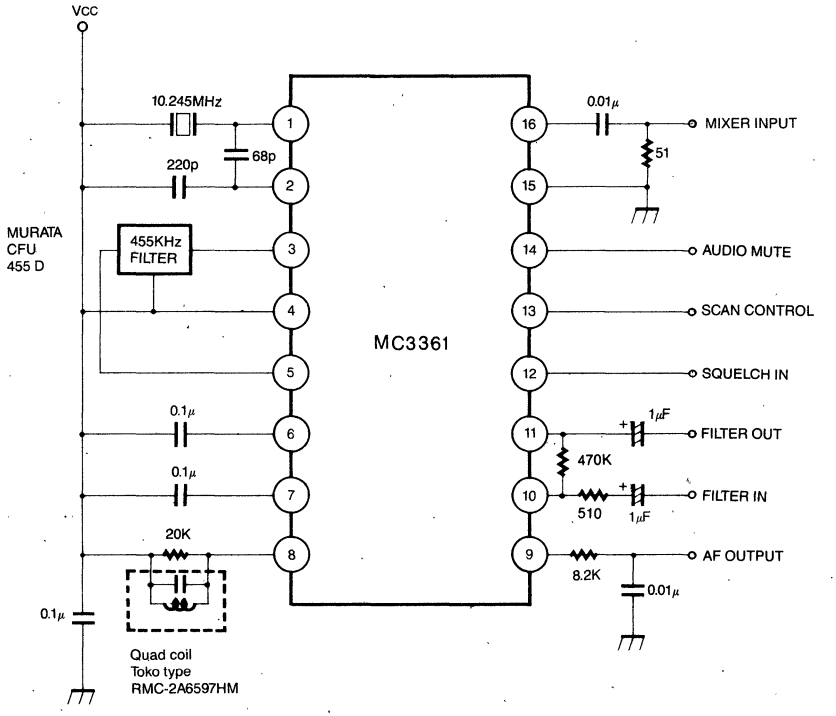


Fig. 2

CIRCUIT DESCRIPTION (see block diagram)

The MC3361 functions include an Oscillator, Mixer, FM IF limiting amplifier, FM demodulator, OP-amp, Scan control and Mute switch.

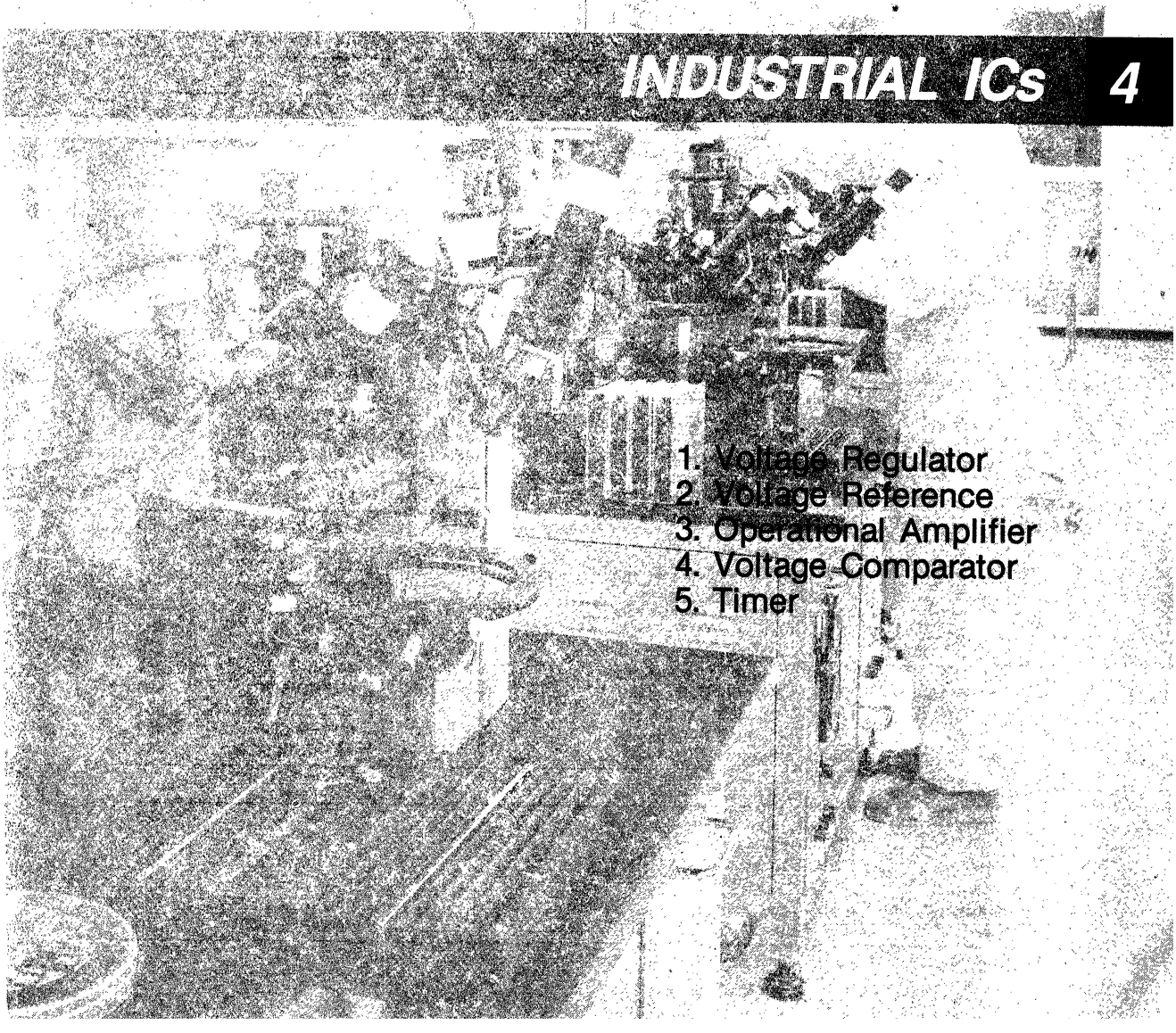
The mixer combines the crystal controlled oscillator to convert the input frequency from 10.7MHz to an intermediate frequency of 455KHz, where, after external bandpass filtering, most of the amplification is done. A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple affects on the audio output. Increasing the Q increases output level because of nonlinearities in the tank phase characteristic.

After detection and de-emphasis, the audio output at pin 9 is partially filtered, then buffered by an emitter follower. The signal still requires volume control and further amplification before driving loudspeaker.

The op amp inverting input (pin 10) which is internally referenced to 0.7V, receives DC bias from the output of pin 11 through the external feedback network. It is normally utilized as either a bandpass filter to extract a specific frequency from th audio output, such as a ring or dial-tone, or as a highpass filter to detect noise due to no input at the mixer. This information is applied to pin 12. An external positive bias to pin 12 sets up the squelch trigger circuit such that pin 13 is low and the audio mute (pin 14) is open circuit. If pin 12 is pulled down to 0.5Vdc by the noise or tone detector, pin 13 will rise to approximately 0.5Vdc below V_{CC} and pin 14 is internally short circuited to ground. There is 50mV of hysteresis at pin 112 to prevent jitter. Audio muting is accomplished by connecting pin 14 to a high-impedance ground-reference point in the audio path between pin 9 and the audio amplifier.

NOTE

INDUSTRIAL ICs 4



1. Voltage Regulator
2. Voltage Reference
3. Operational Amplifier
4. Voltage Comparator
5. Timer

Voltage Regulator

Device	Function	Package	Page
KA350	3 AMP Adjustable Positive Voltage Regulator	TO-3P	277
KA3524	Regulator Pulse Width Modulator	16 DIP	285
LM317	3-Terminal Positive Adjustable Regulator	TO-220	291
LM323	3-Terminal Positive Voltage Regulator	14 DIP/14 SOP	423
LM723	Precision Voltage Regulator	14 DIP/14 SOP	300
KA78S40	Switching Regulator	16 DIP	306
KA78TXX	3A Positive Voltage Regulator	TO-220	312
MC78XX	3-Terminal 1A Positive Voltage Regulator	TO-220	323
MC78LXX	3-Terminal Positive Voltage Regulator	TO-92	353
MC78MXX	3-Terminal 0.5A Positive Voltage Regulator	TO-220	364
MC79XX	3-Terminal Negative Voltage Regulator	TO-220	377
MC79MXX	3-Terminal 0.5A Negative Voltage Regulator	TO-220	387

Voltage Reference

KA336-5.0	Voltage Reference Diode	TO-92	393
KA385-1.2	Micropower Voltage Reference Diode	TO-92	397
KA431	Programmable Precision Reference	TO-92/8 DIP/8 SOP	401

Operational Amplifier

KA201A	Single Operational Amplifier	8 DIP/8 SOP	407
KA301A	Single Operational Amplifier	8 DIP/8 SOP	407
KA733C	Differential Video Amplifier	14 DIP/14 SOP	412
KA9256	Dual Power Operational Amplifier	10 SIP H/S	419
KF351	Single Operational Amplifier	8 DIP/8 SOP	421
LM224/A	Quad Operational Amplifier	14 DIP/14 SOP	423
LM248	Quad Operational Amplifier	14 DIP/14 SOP	432
LM258/A	Quad Operational Amplifier	8 DIP/8 SOP/9 SIP	438
LM324/A	Dual Operational Amplifier	14 DIP/14 SOP	423
LM348	Dual Operational Amplifier	14 DIP/14 SOP	432
LM358/A/S	Quad Operational Amplifier	8 DIP/8 SOP/9 SIP	438
LM741C/E/I	Single Operational Amplifier	8 DIP/8 SOP	446
LM2902	Quad Operational Amplifier	14 DIP/14 SOP	423
LM2904	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	438
MC1458/C/S/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	452
MC3303	Quad Operational Amplifier	14 DIP/14 SOP	456
MC3403	Quad Operational Amplifier	14 DIP/14 SOP	456
MC4558C/AC/I	Dual Operational Amplifier	8 DIP/8 SOP/9 SIP	463

Voltage Comparator

KA319	Dual High Speed Voltage Comparator	14 DIP/14 SOP	468
KA361	High Speed Voltage Comparator	14 DIP/14 SOP	472
KA710C	High Speed Voltage Comparator	14 DIP/14 SOP	474
LM211	Voltage Comparator	8 DIP/8 SOP	476
LM239/A	Quad Differential Comparator	14 DIP/14 SOP	481
LM293/A	Dual Differential Comparator	8 DIP/8 SOP	489
LM311	Voltage Comparator	8 DIP/8 SOP	476
LM339/A	Quad Differential Comparator	14 DIP/14 SOP	481
LM393/A/S	Dual Differential Comparator	8 DIP/8 SOP	489
LM2901	Quad Differential Comparator	14 DIP/14 SOP	481
LM2903	Dual Differential Comparator	8 DIP/8 SOP	489
LM3302	Quad Differential Comparator	14 DIP/14 SOP	481

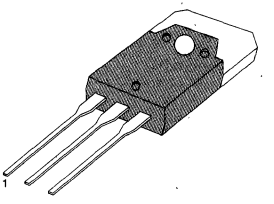
Timer

KS555	CMOS Timer	8 DIP/8 SOP	496
KS555H	CMOS Timer	8 DIP/8 SOP	501
KS556	CMOS Timer	14 DIP/14 SOP	505
NE555	Timer	8 DIP/8 SOP	509
NE556	Dual Timer	14 DIP/14 SOP	513
NE558	Dual Timer	16 DIP/16 SOP	516

3 AMP ADJUSTABLE POSITIVE VOLTAGE REGULATOR

The KA350 is adjustable 3-terminal positive voltage regulator capable of supplying in excess of 3.0A over an output voltage range of 1.2V to 33V. This voltage regulator is exceptionally easy to use and require only two external resistors to set the output voltage. Further, they employ internal current limiting, thermal shutdown and safe area compensation, making them essentially blow-out proof. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

TO-3P



1: Adj 2: Output 3: Input

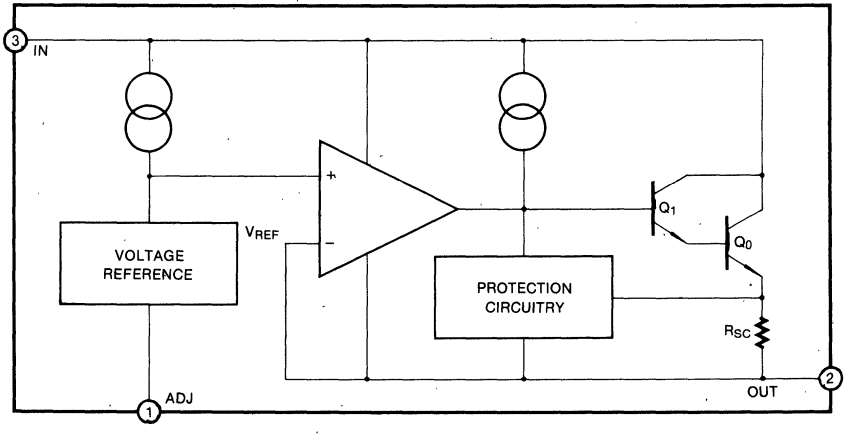
FEATURES

- **Output adjustable between 1.2V and 33V**
- **Guranteed 3A output current**
- **Internal thermal overload protection**
- **Load regulation typically 0.1%**
- **Line regulation typically 0.005%/V**
- **Internal short-circuit current limiting constant with temperature.**
- **Output transistor safe-area compensation**
- **Floating operation for high voltage application**
- **Standard 3-lead transistor package**
- **Eliminates stocking many fixed voltages**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA350H	TO-3P	0 ~ 125°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	V_I-V_o	35	V_{DC}
Soldering Lead Temperature (10 Seconds)	T_{lead}	300	°C
Power Dissipation	P_D	Internally limited	
Operating Temperature Range	T_j	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

($V_I - V_O = 5V$, $I_O = 1.5A$, $T_j = 0°C$ to $125°C$; P_{max}, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	$\triangle V_o$	$Ta = 25°C$, $3V \leq V_I$-$V_o \leq 35V$ (Note 1)		0.005	0.03	%/V
Load Regulation	$\triangle V_o$	$Ta = 25°C$, $10mA \leq I_o \leq 3A$ $V_o \leq 5V$ (Note 1) $V_o \geq 5V$ (Note 1)		 5 0.1	 25 0.5	 mV %/V_o
Adjustment Pin Current	I_{adj}			50	100	μA
Adjustment Pin Current Change	$\triangle I_{adj}$	$3V \leq V_I - V_o \leq 35V$, $10mA \leq I_L \leq 3A$, $P_D \leq P_{MAX}$		0.2	5.0	μA
Thermal Regulation	V_{TRG}	Pulse = 20mS, $Ta = 25°C$		0.002		%/W
Reference Voltage	V_{REF}	$3V \leq V_I - V_o \leq 35V$, $10mA \leq I_O \leq 3A$	1.2	1.25	1.30	V
Line Regulation	$\triangle V_o$	$3.0V \leq V_I - V_o \leq 35V$		0.02	0.07	%/V
Load Regulation	$\triangle V_o$	$10mA \leq I_O \leq 3.0A$ $V_o \leq 5.0V$ $V_O \geq 5.0V$		 20 0.3	 70 1.5	 mV %V_O
Temperature Stability	T_S	$T_j = 0°C$ to $125°C$		1.0		%V_O
Maximum Output Current	I_{MAX}	$V_I - V_o \leq 10V$, $P_D \leq P_{MAX}$	3.0	4.5		A
		$V_I - V_o = 30V$, $P_D \leq P_{MAX}$, $Ta = 25°C$	0.25	1.0		A
Minimum Load Current to Maintain Regulation	I_{LMIN}	$V_I - V_o = 35V$		3.5	10	mA
RMS Noise, % of V_o	V_N	$10Hz \leq f \leq 10KHz$, $Ta = 25°C$		0.003		%V_O
Ripple Rejection	RR	$V_o = 10V$, $f = 120Hz$, without C_{ADJ} $C_{ADJ} = 10\mu F$	 66	 65 80	 	 dB dB
Long-Term Stability	S	$T_j = 125°C$		0.3	1	%

Note 1: Regulation is measured at constant junction temperature. Changes in output voltage due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TYPICAL PERFORMANCE CHARACTERISTIC

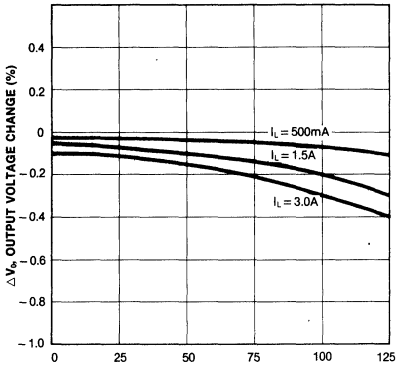


Fig. 1

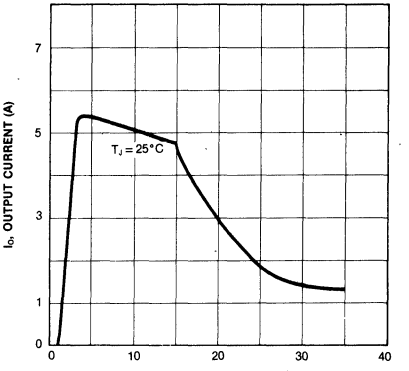


Fig. 2

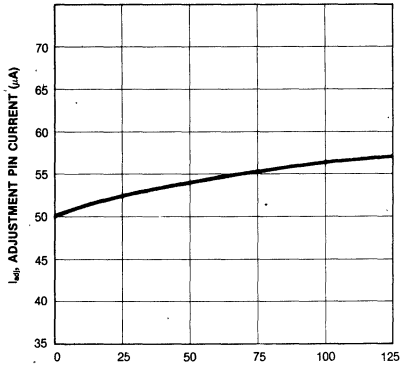


Fig. 3

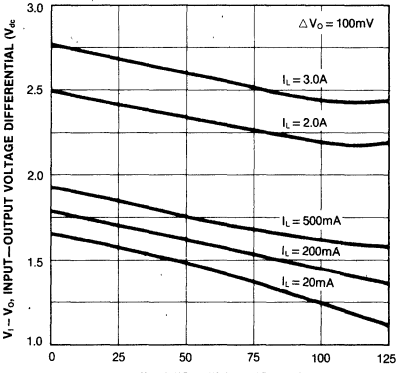


Fig. 4

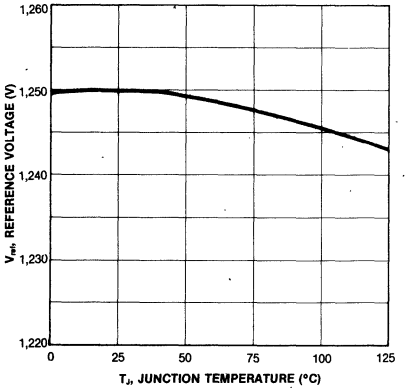


Fig. 5

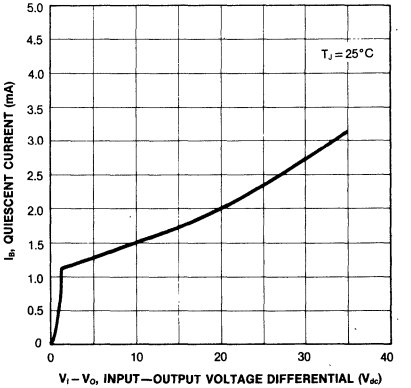


Fig. 6

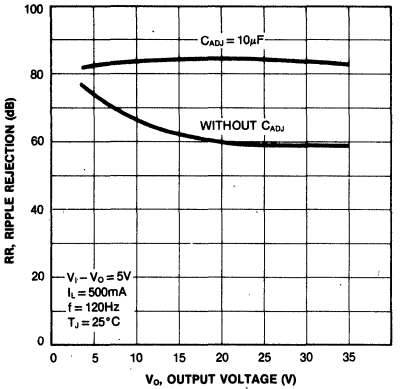


Fig. 7

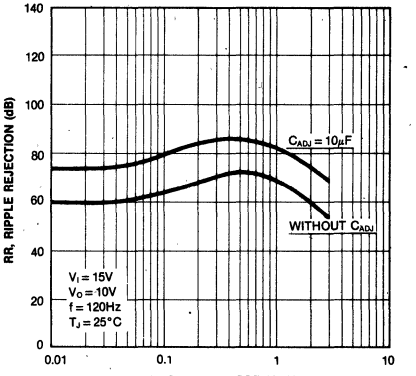


Fig. 8

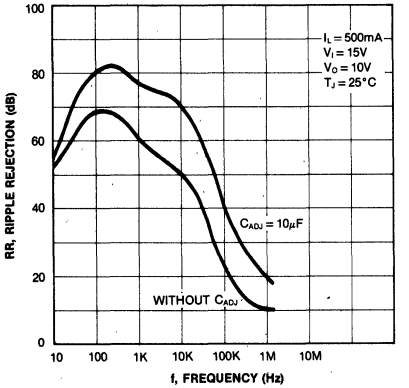


Fig. 9

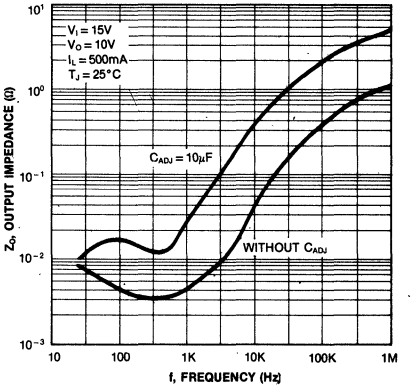


Fig. 10

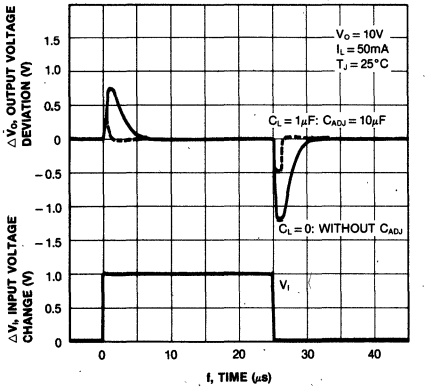


Fig. 11

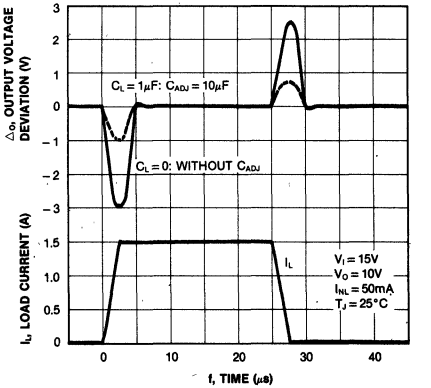


Fig. 12

APPLICATION INFORMATION

STANDARD APPLICATION

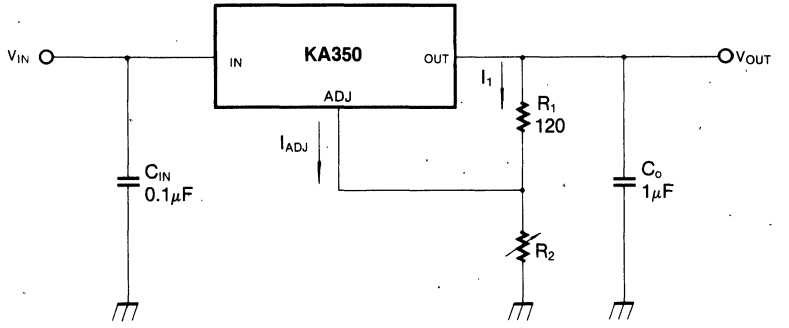


Fig. 13

C_{in}: C_{in} is required if regulator is located an appreciable distance from power supply filter.
C_o: Output capacitors in the range of 1μF to 100μF of aluminum or tantalum electrontic are commonly used to provide improved output impedance and rejection of transients.

In operation, KA350 develops a nominal 1.25V reference voltage, V_{ref}, between the output and adjustment terminal. The reference voltage is impressed across program resistor R_1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R_2, giving an output voltage of

$$V_{out} = 1.25V\ (1 + \frac{R_2}{R_1}) + I_{ADJ}\ R_2$$

Since I_{ADJ} current (less than 100μA) from the adjustment terminal represents an error term, the KA350 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output voltage will rise.

Since the KA350 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltage with respect to ground is possible.

TYPICAL APPLICATIONS

LIGHT CONTROLLER

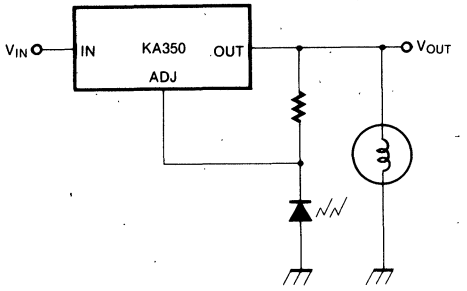
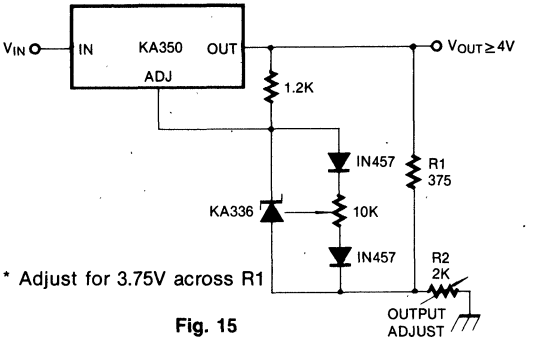


Fig. 14

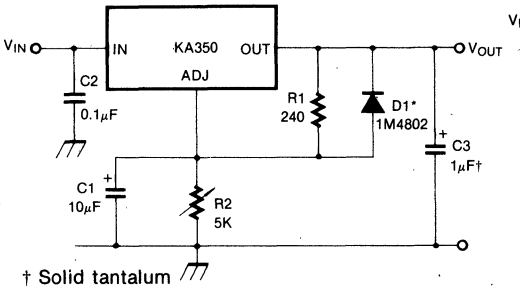
PRECISION POWER REGULATOR WITH LOW TEMPERATURE COEFFICIENT



* Adjust for 3.75V across R1

Fig. 15

ADJUSTABLE REGULATOR WITH IMPROVED RIPPLE REJECTION



† Solid tantalum

* Discharges C1 if output is shorted to ground

Fig. 16

SLOW TURN-ON 15V REGULATOR

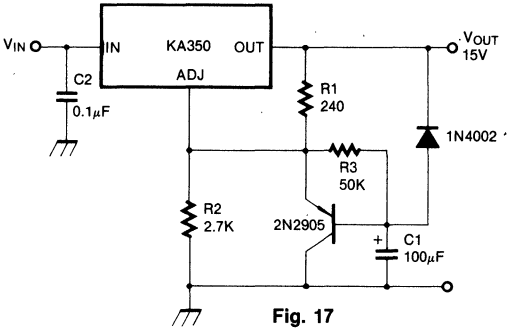


Fig. 17

0 TO 30V REGULATOR

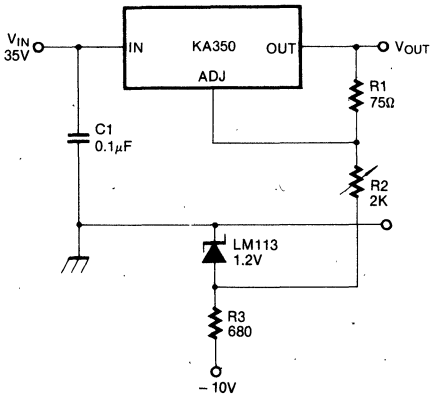
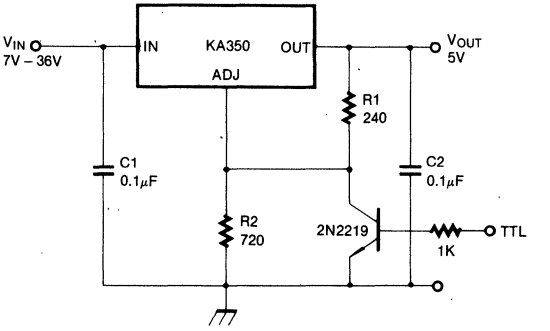


Fig. 18

5V LOGIC REGULATOR WITH ELECTRONIC SHUTDOWN*

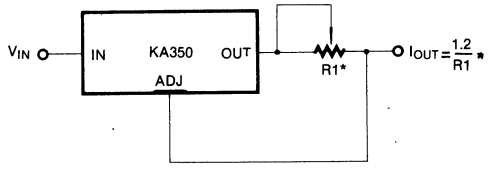


* Min output = 1.2V

Fig. 19

TYPICAL APPLICATIONS (Continued)

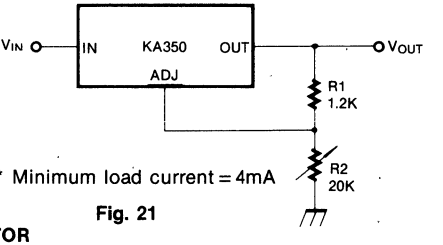
PRECISION CURRENT LIMITER



* $0.4 \leq R1 \leq 120\Omega$

Fig. 20

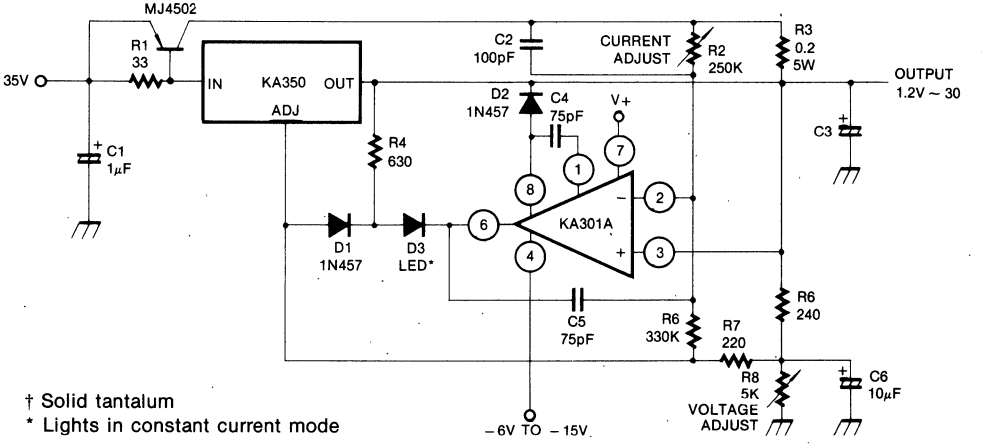
1.2V – 20V REGULATOR WITH MINIMUM PROGRAM CURRENT



* Minimum load current = 4mA

Fig. 21

5A CONSTANT VOLTAGE/CONSTANT CURRENT REGULATOR



† Solid tantalum

* Lights in constant current mode

Fig. 22

12V BATTERY CHARGER

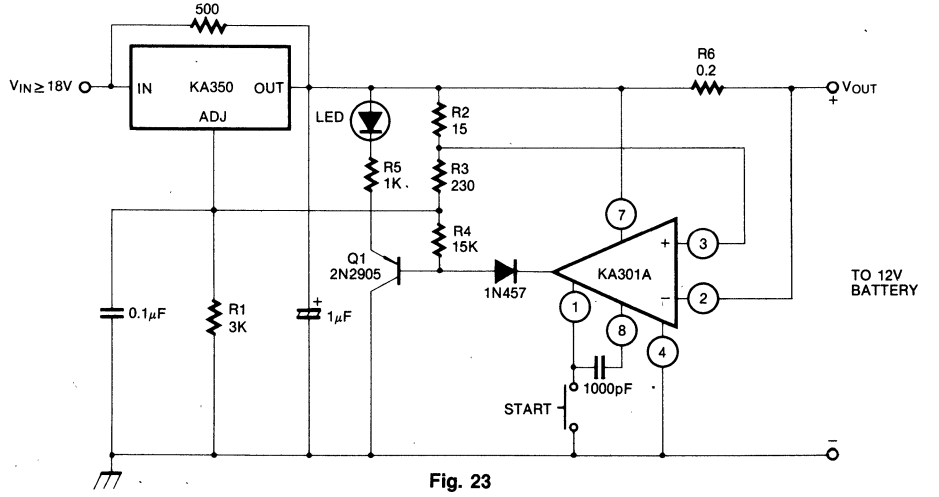


Fig. 23

TRACKING PREREGULATOR

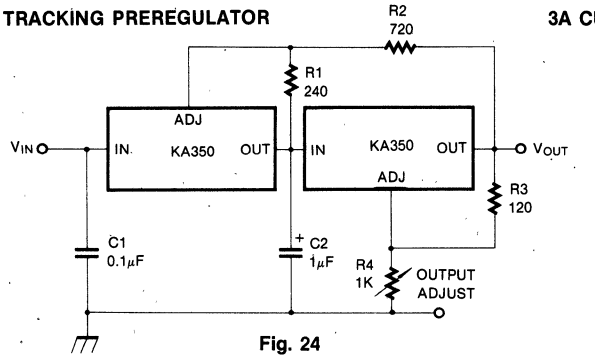


Fig. 24

3A CURRENT REGULATOR

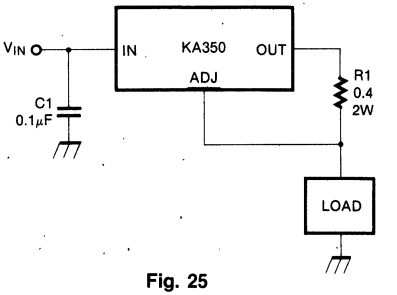
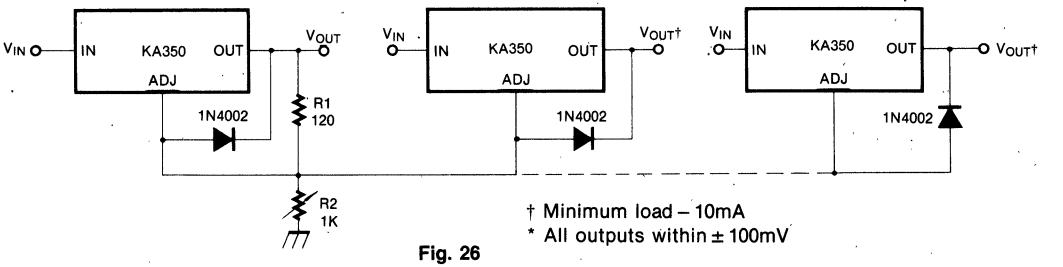


Fig. 25

ADJUSTING MULTIPLE ON-CARD REGULATORS WITH SINGLE CONTROL*



† Minimum load – 10mA
* All outputs within ± 100mV

Fig. 26

AC VOLTAGE REGULATOR

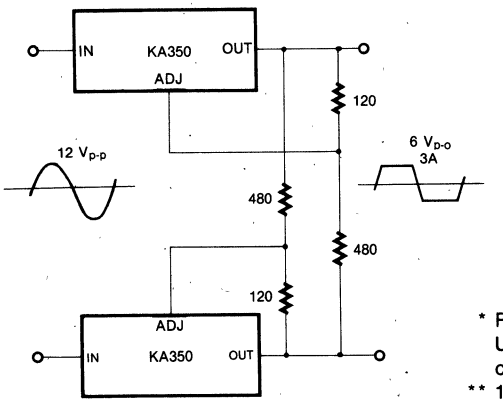
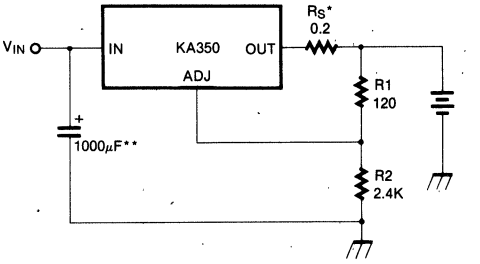


Fig. 27

SIMPLE 12V BATTERY CHARGER



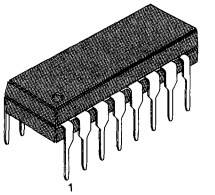
* R_S – sets output impedance of charger $Z_{OUT} = R_S\,(1 + \frac{R_2}{R_1})$
Use of R_S allows low charging rates with fully charged battery.
** 1000μF is recommended to filter out any input transients.

Fig. 28

REGULATOR PULSE WIDTH MODULATOR

The KA3524 regulating pulse width modulator contains all of the control circuitry necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50mA to external circuitry, a control amplifier, an oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shut-down circuitry. Both the regulator output transistor and each output switch are internally current limiting and, to limit junction temperature, an internal thermal shutdown circuit is employed.

16 DIP



FEATURES

- **Complete PWM power control circuitry**
- **Frequency adjustable to greater than 100KHz**
- **2% frequency stability with temperature**
- **Total quiescent current less than 10mA**
- **Dual alternating output switchs for both push-pull or single-ended applications**
- **Current limit amplifier provides external component protection**
- **On-chip protection against excessive junction temperature and output current**
- **5V, 50mA linear regulator output available to user**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA3524N	16 DIP	0 ~ 70°C

BLOCK DIAGRAM

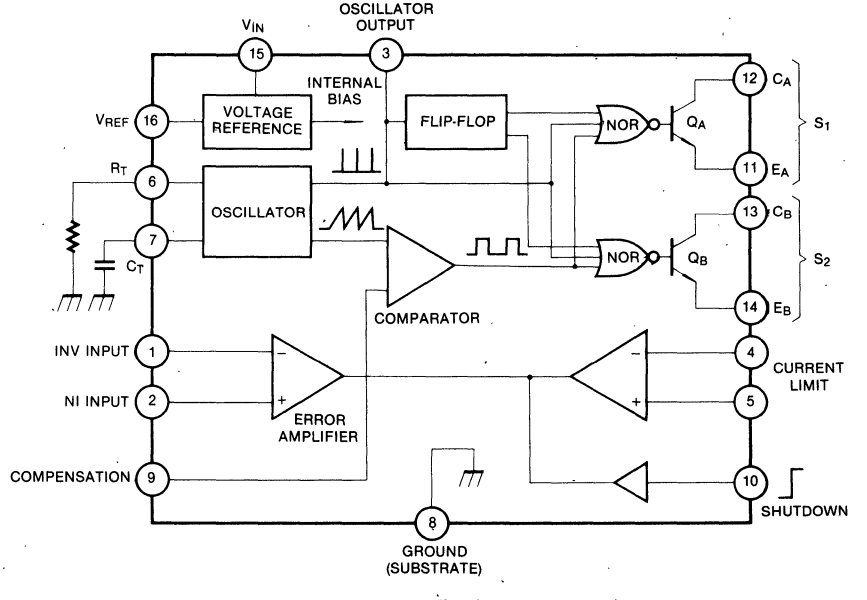


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Reference Output Current	I_{ref}	50	mA
Output Current (Each Output)	I_O	100	mA
Oscillator Changing Current (pin 6 or 7)	I_{charge}	5	mA
Lead Temperature (Soldering, 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	1000	mW
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 20V, f = 20KHz, Ta = 0 to 70°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
REFERENCE SECTION						
Output Voltage	V_{ref}		4.6	5.0	5.4	V
Line Regulation	V_{line}	V_{IN} = 8 ~ 40V		10	30	mV
Load Regulation	V_{load}	I_L = 0 ~ 20mA		20	50	mV
Ripple Rejection	V_{RR}	f = 120Hz, Ta = 25°C		66		dB
Short-Circuit Output Current	I_{SC}	V_{ref} = 0, Ta = 25°C		100		mA
Temperature Stability				0.3	1	%
Long Term Stability		Ta = 25°C		20		mV/Khr
OSCILLATOR SECTION						
Maximum Frequency	f_{MAX}	CT = 0.001μF, RT = 2KΩ		350		KHz
Initial Accuracy		RT and CT constant		5		%
Frequency Change with Voltage	△f	V_{IN} = 8 ~ 40V, Ta = 25°C			1	%
Frequency Change with Temperature	△f	Over operating temperature range			2	%
Output Amplitude (Pin 3)	VA3	Ta = 25°C		3.5		V
Output Pulse Width (Pin 3)	V3PW	CT = 0.01μF, Ta = 25°C		0.5		μs
ERROR AMPLIFIER SECTION						
Input Offset Voltage	V_{IO}	VCM = 2.5V		2	10	mV
Input Bias Current	I_{IB}	VCM = 2.5V		2	10	μA
Open Loop Voltage Gain	A_{VO}		60	80		dB
Common-Mode Input Voltage Range	V_{CR}	Ta = 25°C	1.8		3.4	V
Common-Mode Rejection Ratio	CMRR	Ta = 25°C		70		dB
Small Signal Bandwidth	BW	A_V = 0dB, Ta = 25°C		3		MHz
Output Voltage Swing	V_{OSW}	Ta = 25°C	0.5		3.8	V

ELECTRICAL CHARACTERISTICS (Continued)

(V_{IN} = 20V, f = 20KHz, Ta = 0 ~ 70°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
COMPARATOR SECTION						
Maximum Duty Cycle	DC_{max}	% Each output on	45			%
Input Threshold (Pin 9)	V_{TH1}	Zero duty cycle		1		V
Input Threshold (Pin 9)	V_{TH2}	Maximum duty cycle		3.5		V
Input Bias Current	I_B			1		μA
CURRENT LIMITING SECTION						
Sense Voltage	V_{sense}	V(Pin 2) – V(Pin 1) ≥ 50mV Pin 9 = 2V, Ta = 25°C	180	200	220	mV
Sense Voltage T.C.				0.2		mV/°C
Common-Mode Current			0.7		1	V
OUTPUT SECTION (EACH OUTPUT)						
Collector-Emitter Voltage	V_{CEO}		40			V
Collector Leakage Current	I_{LKg}	V_{CE} = 40V		0.1	50	μA
Saturation Voltage	V_{SAT}	IC = 50mA		1	2	V
Emitter Output Voltage	V_E	V_{IN} = 20V,	17	18		V
Rise Time (10% to 90%)	t_r	RC = 2KΩ, Ta = 25°C		0.2		μs
Fall Time (90% to 10%)	t_f	RC = 2KΩ, Ta = 25°C		0.1		μs
Total Standby Current	I_{STD}	V_{IN} = 40V, PINS 1, 4, 7, 8, 11 and 14 are grounded, Pin 2 = 2V All other inputs and outputs open		5	10	mA

APPLICATION INFORMATION

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher current with an external PNP as shown in Figure 2.

EXPANDED REFERENCE CURRENT CAPABILITY

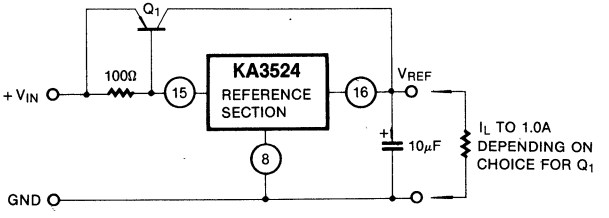


Fig. 2

Oscillator

The oscillator in the KA3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to $3.6V \div R_T$ and should be kept within the range of approximately 30μA to 2mA, i.e., $1.8K < R_T < 100K$. The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 6. A pulse width below approximately 0.5 microseconds may allow faise triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (= 100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 7 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the KA3524 to an external clock, a pulse of = +3 volts may be applied to the oscillator output terminal with $R_T C_T$ set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more KA3524s must be synchronized together, one must be designated as master with its $R_T C_T$ set for the correct period. The slaves should each have an $R_T C_T$ set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L = 5M\Omega$). The gain is

$$A_V = gmR_L = \frac{8I_C R_L}{2K_T} = .002\ R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 8.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 5 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly power frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50KΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 3. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the KA3524 is shown in Figure 4.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1:

$$\text{Threshold} = V_{BE}(Q1) + I_1R_2 - V_{BE}(Q2)$$
$$= I_1R_2 = 200mV$$

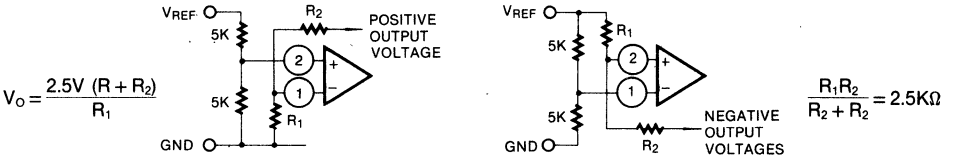
Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limitting can be provided with the network of Figure 5. This circuit can reduce the shortcircuit current (I_{SC}) to approximately onethird the maximum available output current (I_{MAX}).

4

ERROR AMPLIFIER BIASING CIRCUITS



$$V_O = \frac{2.5V\ (R + R_2)}{R_1} \qquad \frac{R_1R_2}{R_2 + R_2} = 2.5K\Omega$$

Note change in input connections for opposite polarity outputs.

Fig. 3

CURRENT LIMITING CIRCUITRY OF THE KA3524

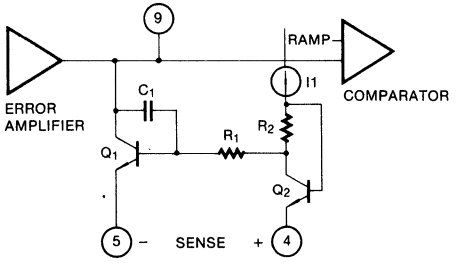
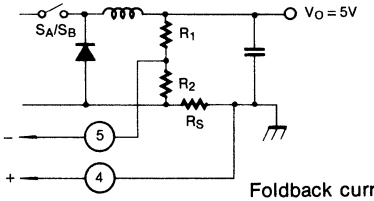


Fig. 4

FOLDBACK CURRENT LIMITING



$$I_{MAX} = \frac{1}{R_S}\ V_{TH} + \frac{V_OR_2}{R_1 + R_2}$$

$$I_{SC} = \frac{V_{TH}}{R_S} \text{ where}$$

$$V_{TH} = 200mV$$

Foldback current limiting can be used to reduce power dissipation under shorted output conditions

Fig. 5

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT STAGE DEAD TIME AS A FUNCTION OF THE TIMING CAPACITOR VALUE

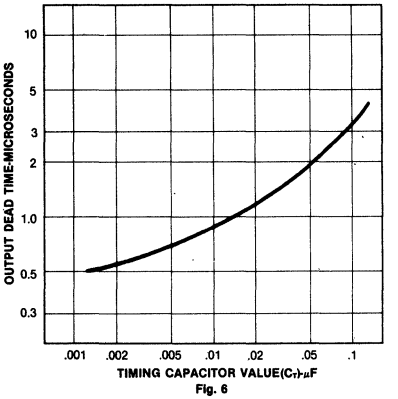


Fig. 6

OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

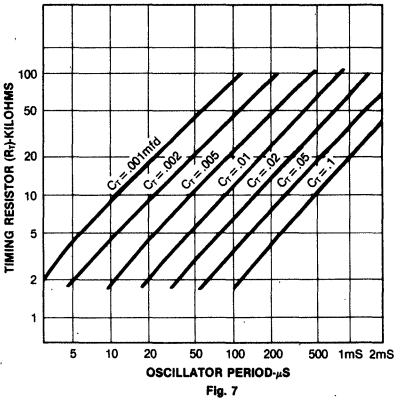


Fig. 7

AMPLIFIES OPEN-LOOP GAIN AS A FUNCTION OF FREQUENCY AND LOADING ON PIN 9

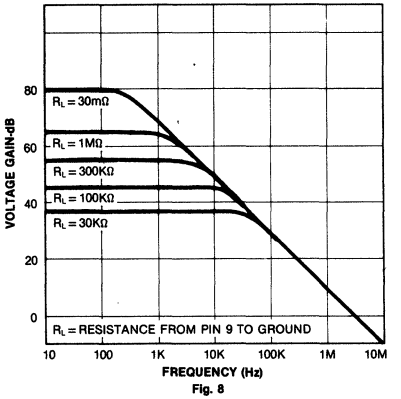
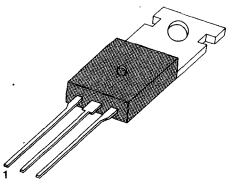


Fig. 8

3-TERMINAL POSITIVE ADJUSTABLE REGULATOR

The LM317 is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 1.5A over an output voltage range of 1.2V to 37V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current-limiting, thermal-shutdown and safe area compensation, making it essentially blow-out proof. The LM317 serves a wide variety of applications including local, on-card regulation. This device also makes an especially simple adjustable switching regulator, and a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

TO-220



1: Adj 2: Output 3: Input

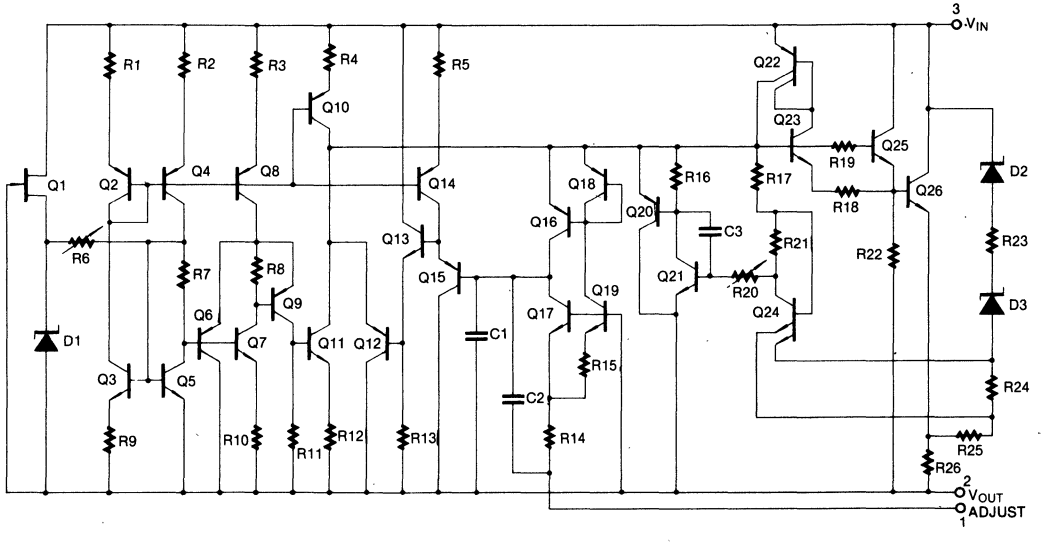
FEATURE

- **Output current in excess of 1.5A**
- **Output adjustable between 1.2V and 37V**
- **Internal thermal-overload protection**
- **Internal short-circuit current-limiting constant with temperature**
- **Output transistor safe-area compensation**
- **Floating operation for high-voltage applications**
- **Standard 3-pin transistor packages**

ORDERING INFORMATION

Device	Package	Operating Temperature
LM317T	TO-220	0 ~ 125°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	$V_{IN} - V_{OUT}$	40	V_{DC}
Lead Temperature	T_{lead}	230	°C
Power Dissipation	P_D	Internally limited	—
Operating Temperature Range	T_j	0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS

($V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 0.5A$, $0°C \leq T_j \leq 125°C$, $I_{max} = 1.5A$, $P_{max} = 20W$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	$\triangle V_o$	Ta = 25°C $3V \leq V_{IN} - V_{OUT} \leq 40V$		0.01	0.04	%/V
		$3V \leq V_{IN} - V_{OUT} \leq 40V$		0.02	0.07	%/V
Load Regulation	$\triangle V_o$	Ta = 25°C, $10mA \leq I_{OUT} \leq I_{MAX}$ $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$		5 0.1	25 0.5	mV $\%V_o$
		$10mA \leq I_{OUT} \leq I_{MAX}$ $V_{OUT} \leq 5V$ $V_{OUT} \geq 5V$		20 0.3	70 1.5	mV $\%V_o$
Adjustable Pin Current	I_{ADJ}			50	100	μA
Adjustable Pin Current Change	$\triangle I_{ADJ}$	$2.5V \leq V_{IN} - V_{OUT} \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$ $P \leq P_{MAX}$		0.2	5	μA
Reference Voltage	V_{REF}	$3V \leq V_{IN} - V_{OUT} \leq 40V$ $10mA \leq I_{OUT} \leq I_{MAX}$ $P_D \leq P_{MAX}$	1.20	1.25	1.30	V
Temperature Stability	T_S			0.7		$\%V_o$
Minimum Load Current to Maintain Regulation	I_L (min)	$V_{IN} - V_{OUT} = 40V$		3.5	10	mA
Maximum Output Current	I_{MAX}	$V_{IN} - V_{OUT} \leq 15V$, $P_D \leq P_{MAX}$ $V_{IN} - V_{OUT} = 40V$, $P_D \leq P_{MAX}$	1.5 0.15	2.2 0.4		A
RMS Noise, % of V_{OUT}	e_N	Ta = 25°C, $10Hz \leq f \leq 10KHz$		0.003		$\%V_o$
Ripple Rejection	RR	$V_{OUT} = 10V$, f = 120Hz without C_{ADJ} $C_{ADJ} = 10\mu F$	 66	65 80		dB
Long-Term Stability, $T_j = T_{high}$	S	Ta = 25°C for end point measurements		0.3	1	%1KHRS
Thermal Resistance Junction to Case	$R_{\theta JC}$			5		°C/W

TYPICAL PERFORMANCE CHARACTERISTICS

LOAD REGULATION

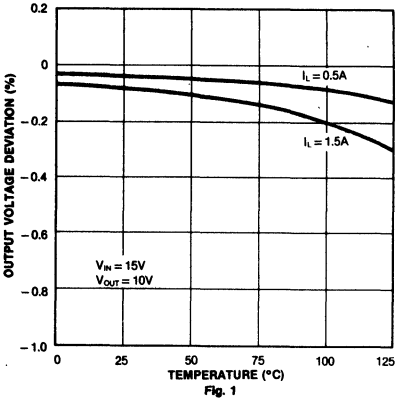


Fig. 1

ADJUSTMENT CURRENT

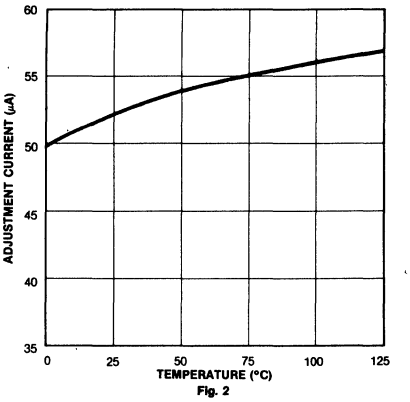


Fig. 2

DROPOUT VOLTAGE

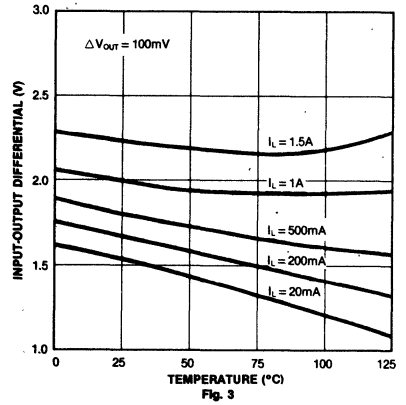


Fig. 3

TEMPERATURE STABILITY

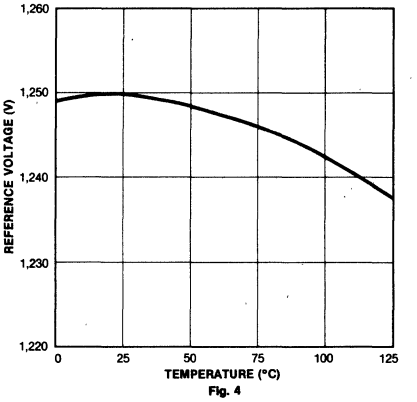


Fig. 4

RIPPLE REJECTION

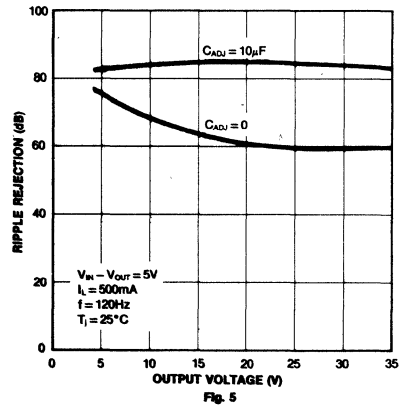


Fig. 5

RIPPLE REJECTION

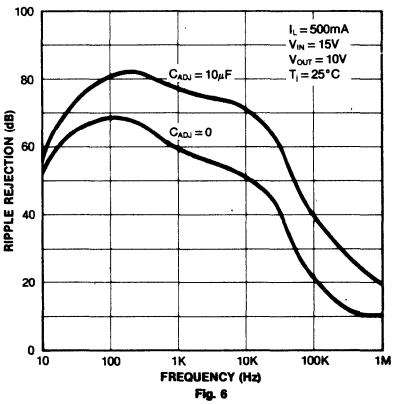


Fig. 6

RIPPLE REJECTION

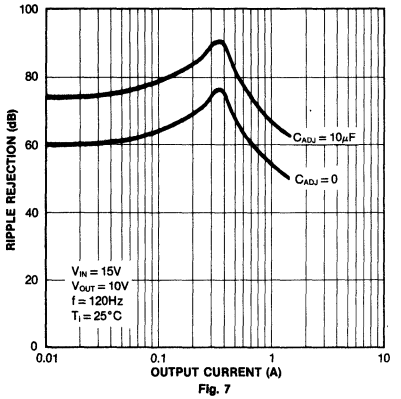


Fig. 7

OUTPUT IMPEDANCE

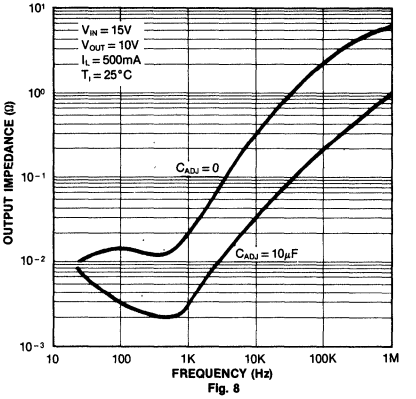


Fig. 8

LINE TRANSIENT RESPONSE

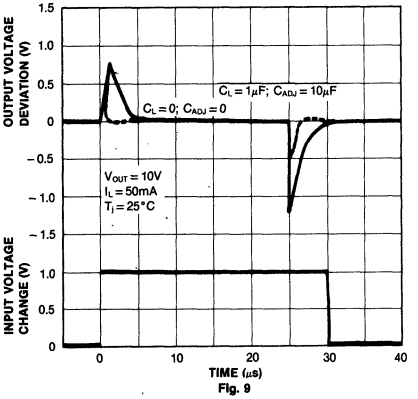


Fig. 9

LOAD TRANSIENT RESPONSE

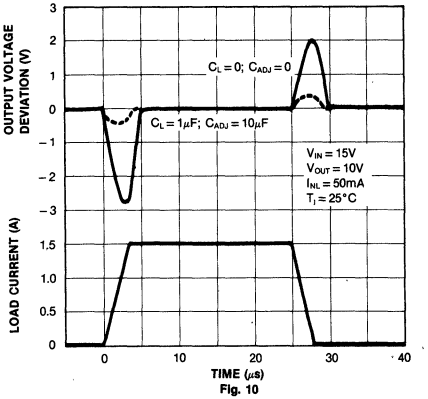


Fig. 10

TYPICAL APPLICATIONS

AC Voltage Regulator

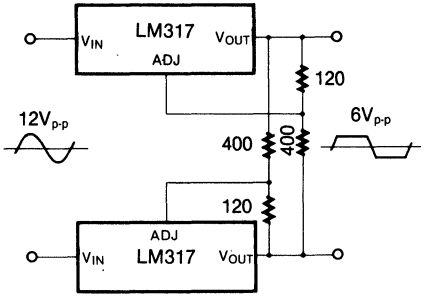
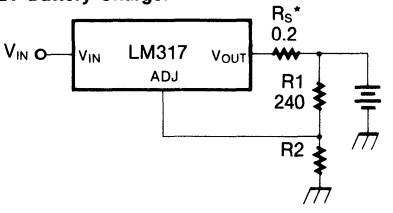


Fig. 11

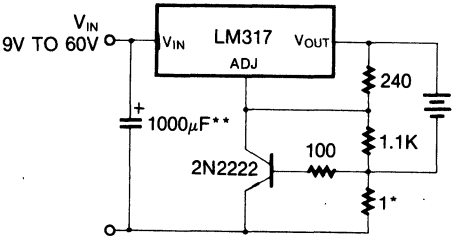
12V Battery Charger



* R_S—sets output impedance of charger $Z_{OUT} = R_S (1 + \frac{R2}{R1})$
Use of R_S allows low charging rates with fully charged battery.

Fig. 13

Current Limited 6V Charger



* Sets peak current (0.6A for 1Ω)
** The 1000μF is recommended to filter out input transients

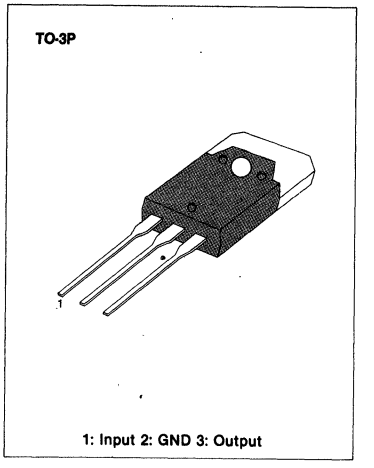
Fig. 12

4

3-TERMINAL POSITIVE VOLTAGE REGULATOR

The LM323 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 Amps.

New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.



1: Input 2: GND 3: Output

FEATURES

- **3 Amp output current**
- **Internal current and thermal limiting**
- **0.01Ω typical output impedance**
- **7.5 minimum input voltage**

ORDERING INFORMATION

Device	Package	Operating Temperature
LM323H	TO-3P	0 ~ 125°C

SCHEMATIC DIAGRAM

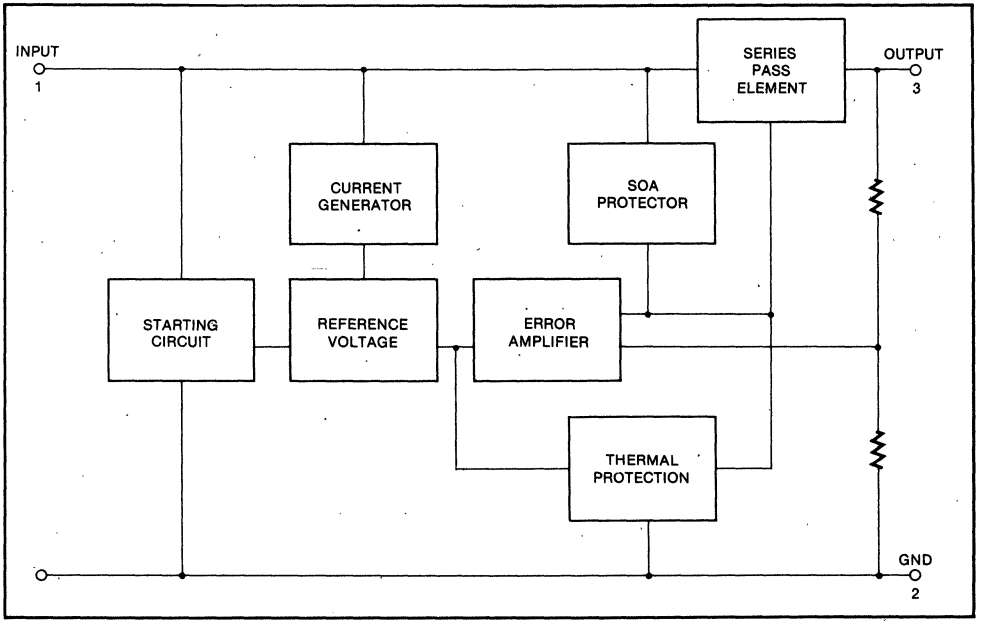


Fig. 1

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage	V_C	20	V
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(0°C ≤ T_J ≤ 125°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_O	T_J = 25°C V_{IN} = 7.5V, I_{OUT} = 0	4.8	5	5.2V	
		7.5V ≤ V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A, P ≤ 30W	4.75		5.25	V
Line Regulation	ΔV_O	T_J = 25°C 7.5V ≤ V_{IN} ≤ 15V		5	25	mV
Load Regulation	ΔV_O	T_J = 25°C, V_{IN} = 7.5V 0 ≤ I_{OUT} ≤ 3A		25	100	mV
Quiescent Current	I_d	7.5V ≤ V_{IN} ≤ 15V 0 ≤ I_{OUT} ≤ 3A		12	20	mA
Output Noise Voltage	V_N	T_J = 25°C, 10Hz ≤ f ≤ 100KHz		40		μV_{rms}
Short Circuit Current	I_{SC}	T_J = 25°C, V_{IN} = 15V		3		A
		T_J = 25°C, V_{IN} = 7.5V		4		A
Thermal Resistance Junction to Case	Θ_{JC}			3		°C/W

Fig. 2 MAXIMUM AVERAGE POWER DISSIPATION

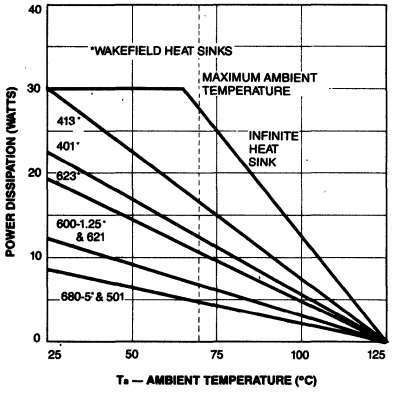


Fig. 3 OUTPUT IMPEDANCE

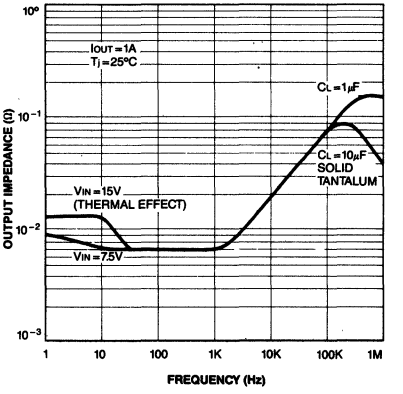


Fig. 4 PEAK AVAILABLE OUTPUT CURRENT

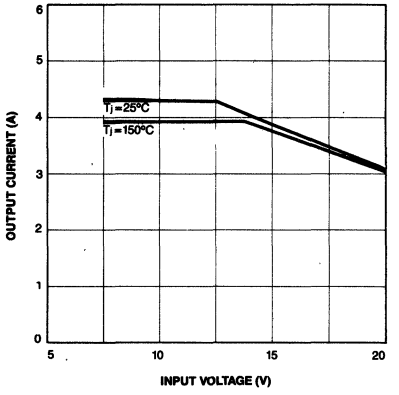


Fig. 5 SHORT CIRCUIT CURRENT

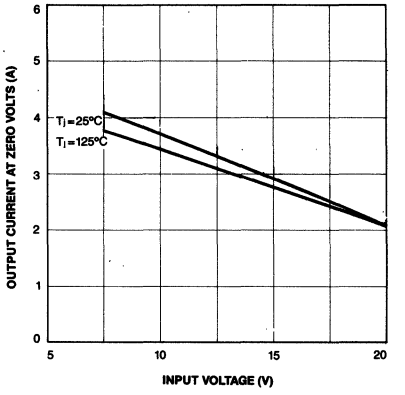


Fig. 6 RIPPLE REJECTION

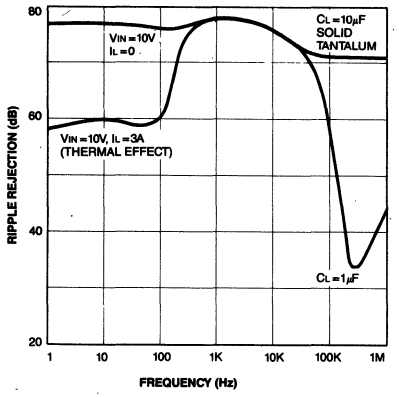


Fig. 7 DROPOUT VOLTAGE

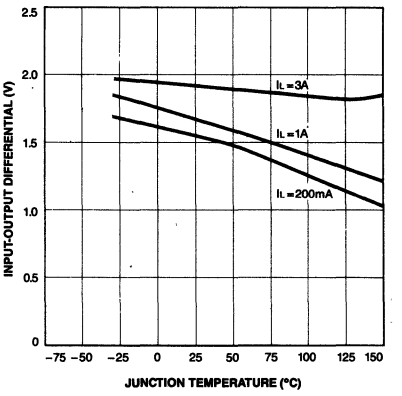


Fig. 8 LINE TRANSIENT RESPONSE

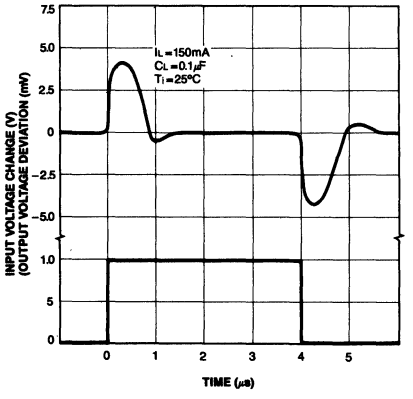


Fig. 9 OUTPUT VOLTAGE

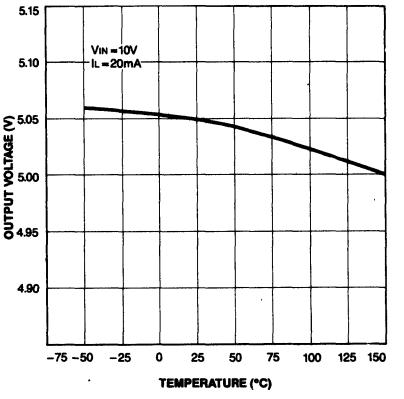


Fig. 10 QUIESCENT CURRENT

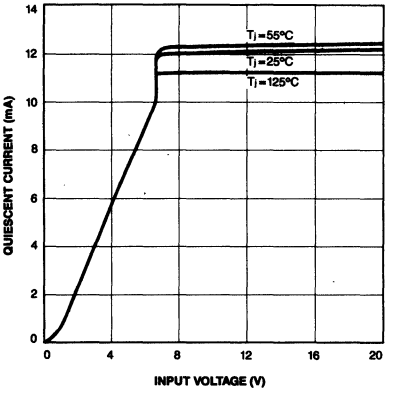


Fig. 11 LOAD TRANSIENT RESPONSE

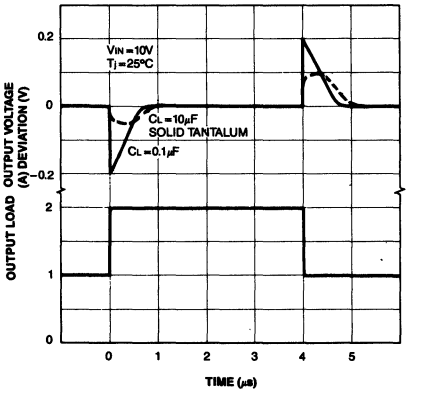
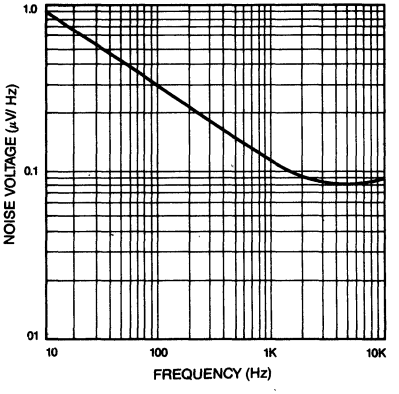
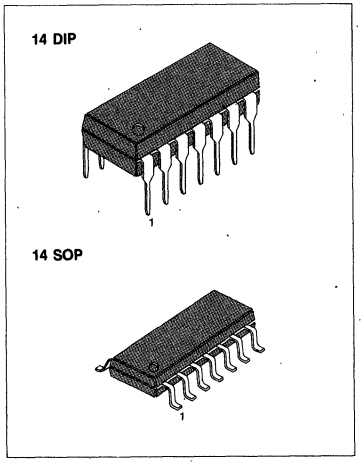


Fig. 12 OUTPUT NOISE VOLTAGE



PRECISION VOLTAGE REGULATOR

The LM723 is a monolithic integrated circuit voltage regulator featuring high ripple rejection, excellent output and load regulation, excellent temperature stability, and low standby current.



FEATURES

- **Positive or Negative Supply Operation.**
- **0.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts.**
- **Output current to 150mA without external pass transistor**

BLOCK DIAGRAM

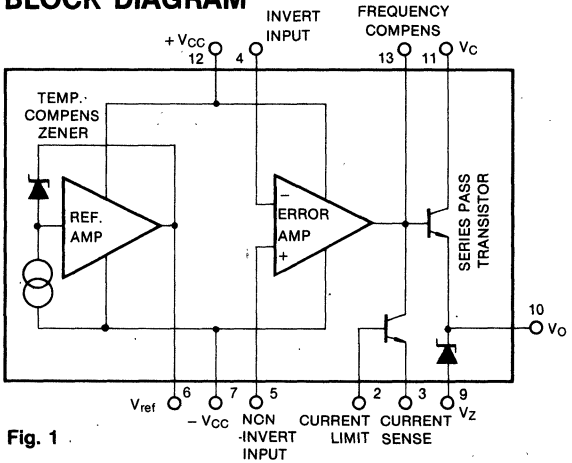


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
LM723CN	14 DIP	0 ~ +70°C
LM723CD	14 SOP	
LM723IN	14 DIP	– 25 ~ +85°C
LM723ID	14 SOP	

SCHEMATIC DIAGRAM

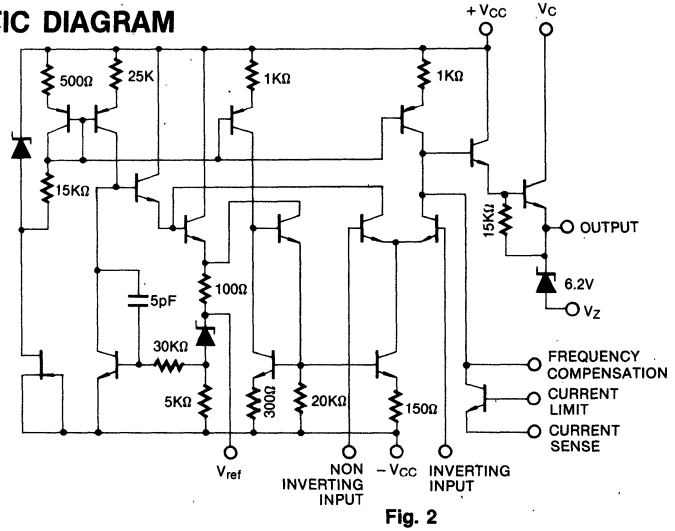


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic		Symbol	Value	Unit
Pulse Voltage from V+ to V− (50ms)		$V_{IN(P)}$	50	V_{peak}
Continus Voltage from V+ to V−		V_{IN}	40	V
Input-Output Voltage Differential		V_{IN}-V_O	40	V
Maximum Output Current		I_O	150	mA
Differential Input Voltage		V_{ID}	±5	V
Voltage Between Non-Inverting Input and V−		V_{IE}	8	V
Current from V_Z		I_Z	25	mA
Current from V_{REF}		I_{REF}	15	mA
Power Dissipation		P_D	1000	mW
Operating Temperature Range	LM723I	T_{opr}	−25 ~ +85	°C
	LM723C		0 ~ +70	°C
Storage Temperature Range		T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(unless otherwise specified, Ta = 25°C, $V_I = V_{CC} = V_C = 12V$, $V_O = +5V$, $I_L = 1.0mA$, $R_{SC} = 0$, $C_I = 100pF$, $C_{ref} = 0$ and devider impedance as seen by error Amplifier ≤ 10KΩ connected as shown in figure 3)

Characteristic	Symbol	Test Conditions	LM7231/LM723C			Unit
			Min	Typ	Max	
Line Regulation	$\triangle V_O$	$V_I = 12V$ to $15V$		0.01	0.1	%
		$V_I = 12V$ to $40V$		0.1	0.5	
		$T_{MIN} \leq T_A \leq T_{MAX}$, $V_I = 12V$ to $15V$			0.3	
Load Regulation	$\triangle V_O$	$I_O = 1mA$ to $50mA$		0.03	0.2	%
		$T_{MIN} \leq T_A \leq T_{MAX}$, $I_O = 1$ to $50mA$			0.6	
Ripple Rejection	RR	f = 100Hz to 10KHz, $C_{REF} = 0$		74		dB
		f = 100Hz to 10KHz, $C_{REF} = 5\mu F$		86		
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	$T_{MIN} \leq T_A \leq T_{MAX}$		0.003	0.015	%/°C
Short Circuit Current Limit	I_{SC}	$R_{SC} = 10\Omega$, $V_O = 0$		65		mA
Reference Voltage	V_{REF}		6.80	7.15	7.50	V
Output Noise Voltage	V_N	f = 100Hz to 10KHz, $C_{REF} = 0$		20		μV_{rms}
		f = 100Hz to 10KHz, $C_{REF} = 5\mu F$		2.5		
Long-term Stability	V_O/T			0.1		%/1000HR
Standby Current Drain	I_D	$I_L = 0$, $V_{IN} = 30V$		2.3	4.0	mA
Input Voltage Range	V_I		9.5		40	V
Output Voltage Range	V_O		2.0		37	V
Input-Output Voltage Differential	V_D		3.0		38	V

* Note: $T_{MIN} = 0°C$ for LM723C, $= -25°C$ for LM723I; $T_{MAX} = 70°C$ for LM723C, $= 85°C$ for LM723I

Table 1 — Resistor values (KΩ) for standard output voltage

Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10%			Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10%		
		R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3	3, 6	4.12	3.01	1.8	0.5	1.2	−6*	5	3.57	2.43	1.2	0.5	0.75
+5	3, 6	2.15	4.99	0.75	0.5	2.2	−9	5	3.48	5.36	1.2	0.5	2
+6	3, 6	1.15	6.04	0.5	0.5	2.7	−12	5	3.57	8.45	1.2	0.5	3.3
+9	4, 6	1.87	7.15	0.75	1	2.7	−15	5	3.65	11.5	1.2	0.5	4.3
+12	4, 6	4.87	7.15	2	2	3	−28	5	3.57	24.3	1.2	0.5	10
+15	4, 6	7.87	7.15	3.3	1	3							
+28	4, 6	21	7.15	5.6	1	2							

Note: *V_{CC} must be connected to a +3V or greater supply.

Table II — Formulae for intermediate output voltages

Outputs from +2 to +7 volts Fig. 3 $V_o = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Foldback Current Limiting $I_{KNEE} = [\frac{V_o R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts Fig. 4, 6 $V_o = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Output from −6 to −250 volts Fig. 5 $V_o = [\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	

APPLICATION INFORMATION

Basic low voltage regulator (V_O = 2 to 7V)

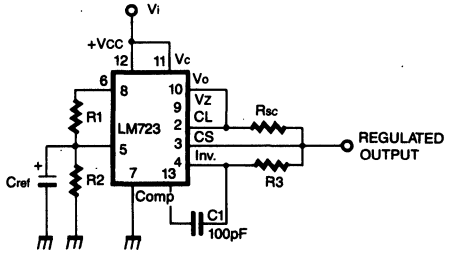


Fig. 3

Note: R3=R1 • R2/(R1+R2) for minimum temperature drift.
R3 may be eliminated for minimum component count.

Typical performance
Regulated Output Voltage 5V
Line Regulation (ΔV_i = 3V) 0.5mV
Load Regulation (ΔI_o = 50mA) 1.5mV

Basic high voltage regulator (V_O = 7 to 37V)

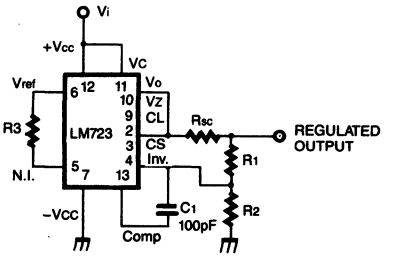


Fig. 4

Note: R1•R2/(R1+R2)for minimum temperature drift.
R3 may be eliminated for minimum component count.

Typical performance
Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V) 1.5mV
Load Regulation (ΔI_o = 50mA) 4.5mV

Negative voltage regulator

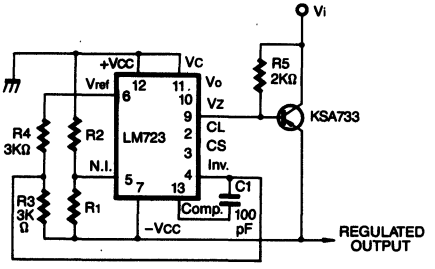


Fig. 5

Typical performance
Regulated output Voltage ..... -15V
Line Regulation (ΔV_i = 3V) 1mV
Load Regulation (ΔI_o = 100mA) 2mV

Positive voltage regulator
(Extenal NPN Pass Transistor)

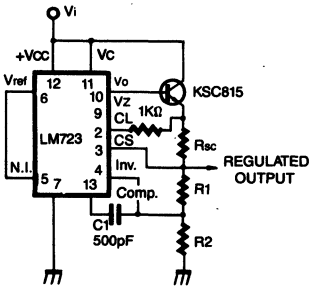


Fig. 6

Typical performance
Regulated Output Voltage ..... +15V
Line Regulation (ΔV_i = 3V) 1.5mV
Load Regulation (ΔI_o = 1A) 15mV

Maximum output current vs. voltage drop

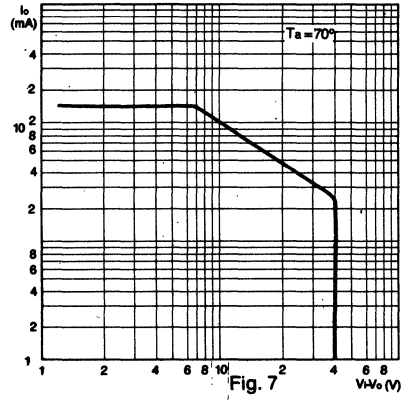


Fig. 7

Current limiting characteristics

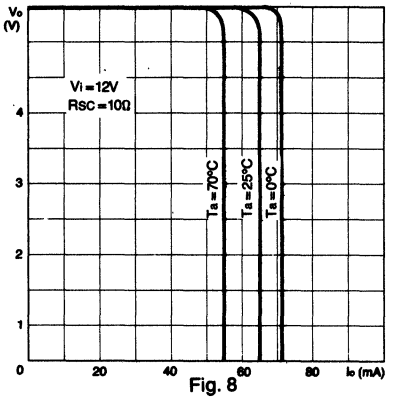


Fig. 8

Current limiting characteristics vs. junction temperature

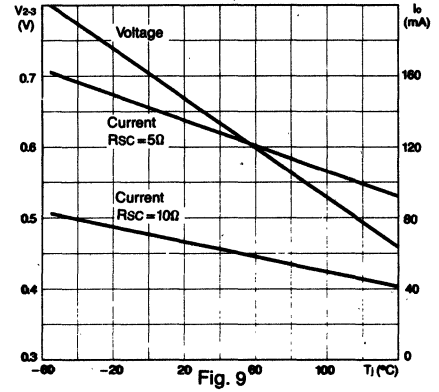


Fig. 9

Load regulation characteristics without current limiting

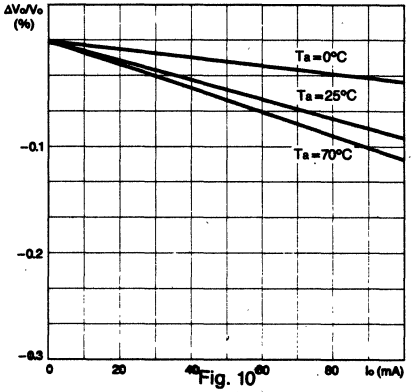


Fig. 10

Load regulation characteristics with current limiting

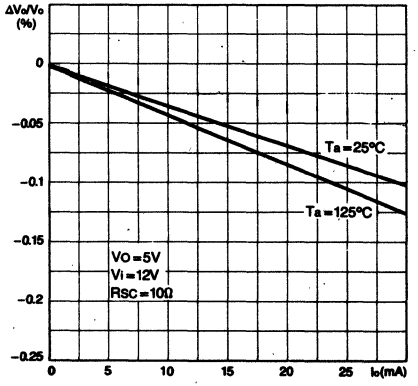


Fig. 11

Load regulation characteristic with current limiting

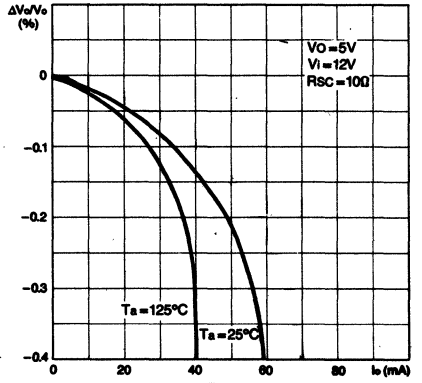


Fig. 12

Line regulation — voltage drop

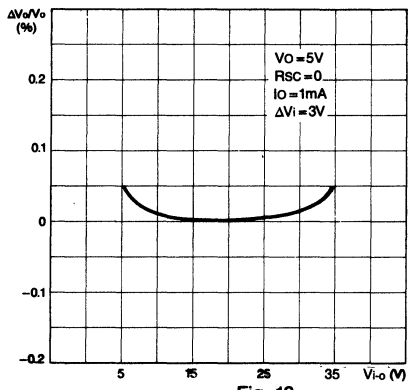


Fig. 13

Load regulation — voltage drop

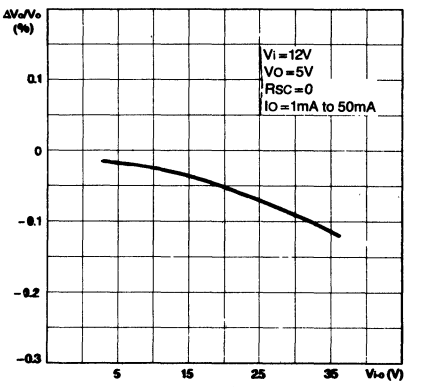


Fig. 14

Quiescent drain current vs. input voltage

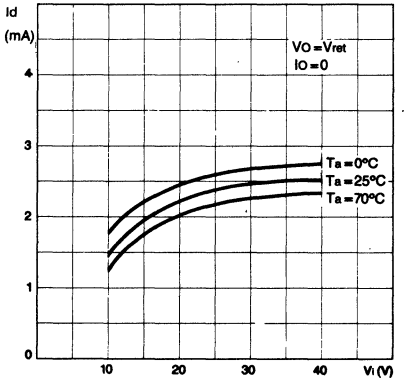


Fig. 15

Line transient response

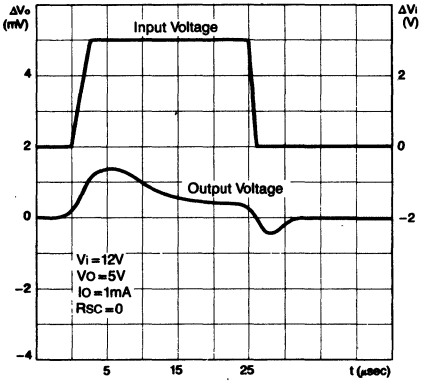


Fig. 16

Load transient response

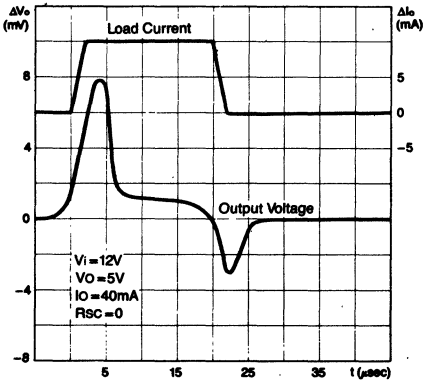


Fig. 17

Output impedance vs. frequency

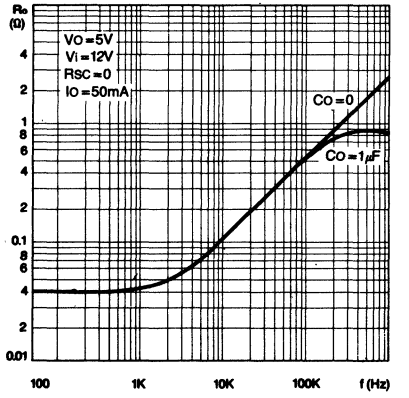
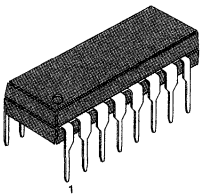


Fig. 18

SWITCHING REGULATOR

The KA78S40 is a monolithic switching regulator subsystem consisting of all the active building blocks necessary for switching regulator systems.

16 DIP



FUNCTIONS

- High-current, high-voltage output switch a power transistor and a diode
- A temperature compensated voltage reference
- A comparator
- A duty cycle controllable oscillator with an active current limit circuit
- Independent operational amplifier.

FEATURES

- **Step-up, step-down or inverting switching regulators**
- **Output current to 1.5A without external transistors**
- **Output adjustable from 1.3 to 40V**
- **Operation from 2.5 to 40V input**
- **80dB line and load regulation**
- **Low standby current drain**
- **High gain, high current independent OP Amp.**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA78S40N	16 DIP	0~70°C

BLOCK DIAGRAM

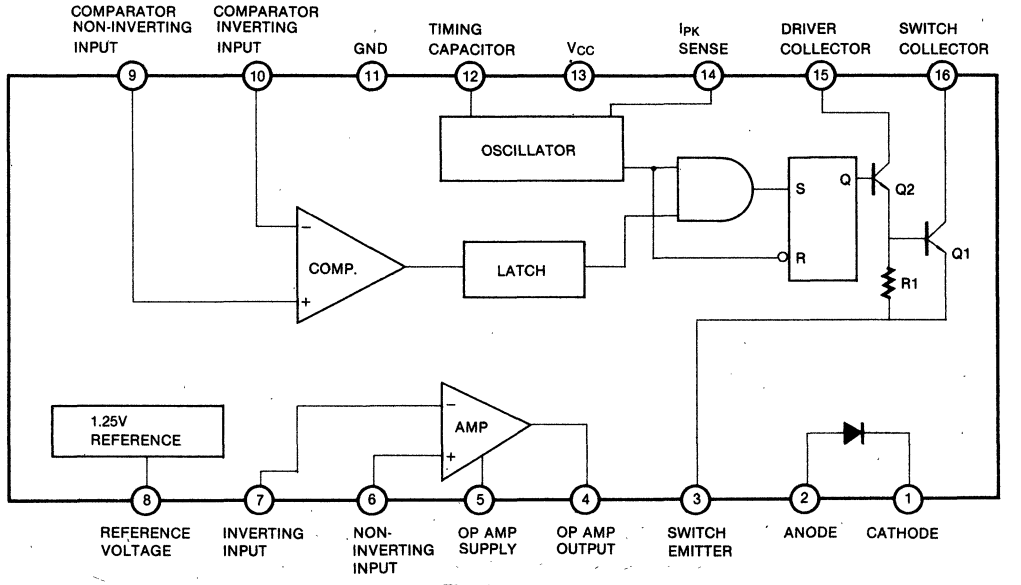


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
OP Amp Power Supply Voltage	V_{OP}	40	V
Common Mode Input Voltage Range	V_{ICM}	$-0.3 \sim V_{CC}$	V
Differential Input Voltage Range (Note)	V_{ID}	$-30 \sim 30$	V
Output Short Circuit Duration (OP Amp)	I_{SC}	Continuous	
Current from V_{REF}	I_{REF}	10	mA
Voltage from Switch Collector to GND	V_{CG}	40	V
Voltage from Switch Emitter to GND	V_{EG}	40	V
Voltage from Switch Collector to Emitter	V_{CE}	40	V
Voltage from Power Diode to GND	V_{DG}	40	V
Reverse Power Diode Voltage	V_{DR}	40	V
Current Through Power Switch	I_{SW}	1.5	A
Current Through Power Diode	I_D	1.5	A
Power Dissipation	P_D	1500	mW
Lead Temperature (Soldering for 10 Sec)	T_{lead}	260	°C
Operating Temperature Range	T_{opr}	0 +70	°C
Storage Temperature Range	T_{stg}	−65 +150	°C

NOTE: For supply voltage less than 30V, the absolute maximum voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, $V_{OP\ Amp}$ = 5.0V, 0° < Ta < 70°, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
General Characteristic						
Supply Voltage	V_{CC}		2.5		40	V
Supply Current Disconnected OP Amp	I_{CC1}	V_{CC} = 5.0V		1.8	3.5	mA
		V_{CC} = 40V		2.3	5.0	
Supply Current Connected OP Amp	I_{CC2}	V_{CC} = 5.0V			4.0	mA
		V_{CC} = 40V			5.5	
Reference Section						
Reference Voltage	V_{REF}	I_{REF} = 1.0mA	1.180	1.245	1.310	V
Reference Voltage Line Regulation	$\triangle V_{REF}$	V_{CC} = 3.0V to 40V I_{REF} = 1.0mA, Ta = 25°C		0.04	0.2	mV/V
Reference Voltage Load Regulation	$\triangle V_{REF}$	I_{REF} = 1.0mA to 10mA Ta = 25°C		0.2	0.5	mV/mA
Oscillation Section						
Charging Current	I_{CHG}	V_{CC} = 5.0V, Ta = 25°C	20		50	μA
		V_{CC} = 40V, Ta = 25°C	20		70	μA
Discharging Current	I_{DCH}	V_{CC} = 5.0V, Ta = 25°C	150		250	μA
		V_{CC} = 40V, Ta = 25°C	150		350	μA

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillator Voltage Swing	V_{OSC}	V_{CC} = 5.0V, Ta = 25°C		0.5		V
t_{on}/t_{off}	t_r			6.0		μS/μS
Current Limit Section						
Current Limit Sense Voltage	V_{SEN}	Ta = 25°C	250		350	mV
Output Switch Section						
Output Saturation Voltage	V_{SAT}	I_{SW} = 1.0A, step-down		1.1	1.3	V
		I_{SW} = 1.0A, step-up		0.45	0.7	V
Output Transistor h_{FE}	h_{FE}	I_C = 1.0A, V_{CE} = 5.0V, Ta = 25°C		70		
Output Leakage Current	I_{leak}	V_{OUT} = 40V, Ta = 25°C		10		nA
Power Diode						
Forward Voltage Drop	V_D	I_D = 1.0A		1.25	1.5	V
Diode Leakage Current	I_{leak}	V_D = 40V, Ta = 25°C		10		nA
Comparator						
Input Offset Voltage	V_{IO}	$V_{CM} = V_{REF}$		1.5	15	mV
Input Bias Current	I_B	$V_{CM} = V_{REF}$		35	200	nA
Input Offset Current	I_{IO}	$V_{CM} = V_{REF}$		5.0	75	nA
Common Mode Voltage Range	V_{CM}	Ta = 25°C	0		V_{CC}-2	V
Power Supply Rejection Ratio	PSRR	V_{CC} = 3.0V to 40V, Ta = 25°C	70	96		dB
Operational Amplifier						
Input Offset Voltage	V_{IO}	V_{CM} = 2.5V		4.0	15	mV
Input Bias Current	I_{IB}	V_{CM} = 2.5V		30	200	nA
Input Offset Current	I_{IO}	V_{CM} = 2.5V		5.0	75	nA
Voltage Gain (Positive)	A_{VOL+}	R_L = 2.0 kΩ to GND, V_0 = 1.0 to 2.5V, Ta = 25°C	25	250		V/mV
Voltage Gain (Negative)	V_{VOL-}	R_L = 2.0 kΩ to V_+ OP Amp V_0 = 1.0 to 2.5V, Ta = 25°C	25	250		V/mV
Common Mode Voltage Range	V_{CM}	Ta = 25°C	0		V_{CC}-2	V
Common Mode Rejection Ratio	CMRR	V_{CM} = 0 to 3.0V, Ta = 25°C	76	100		dB
Power Supply Rejection Ratio	PSRR	V_{op} = 3.0 to 40V, Ta = 25°C	76	100		dB
Output Source Current	I_{SOUR}	Ta = 25°C	75	150		mA
Output Sink Current	I_{SINK}	Ta = 25°C	10	35		mA
Slew rate	S.R	Ta = 25°C		0.6		V/μS
Output Low Voltage	V_{OL}	I_L = −5.0mA, Ta = 25°C			1.0	V
Output High Voltage	V_{OH}	I_L = 50mA, Ta = 25°C	V_{op} − 3.0			V

APPLICATION INFORMATION

Design Formulas

Characteristic	Step Down	Step Up	Inverting	Unit
I_{pk}	$2\ I_{OUT(Max)}$	$2\ I_{OUT(Max)} \bullet \frac{V_{OUT}+V_D-V_{sat}}{V_{IN}-V_{sat}}$	$2 I_{OUT(Max)} \bullet \frac{V_{IN}+\lvert V_{OUT}\rvert+V_D-V_{sat}}{V_{IN}-V_{sat}}$	A
R_{SC}	$0.33/I_{pk}$	$0.33/I_{pk}$	$0.33/I_{pk}$	Ω
$\frac{t_{on}}{t_{off}}$	$\frac{V_{OUT}+V_D}{V_{IN}-V_{sat}-V_{OUT}}$	$\frac{V_{OUT}+V_D-V_{IN}}{V_{IN}-V_{sat}}$	$\frac{\lvert V_{OUT}\rvert+V_D}{V_{IN}-V_{sat}}$	
L	$\frac{V_{OUT}+V_D}{I_{pk}} \bullet t_{off}$	$\frac{V_{OUT}+V_D-V_{IN}}{I_{pk}} \bullet t_{off}$	$\frac{\lvert V_{OUT}\rvert+V_D}{I_{pk}} \bullet t_{off}$	μH
t_{off}	$\frac{I_{pk} \bullet L}{V_{OUT}+V_D}$	$\frac{I_{pk} \bullet L}{V_{OUT}+V_D-V_{IN}}$	$\frac{I_{pk} \bullet L}{\lvert V_{OUT}\rvert+V_D}$	μs
C_T (μF)	$45 \times 10^{-5}\ t_{off}$ (μs)	$45 \times 10^{-5}\ t_{off}$ (μs)	$45 \times 10^{-5}\ t_{off}$ (μs)	μF
C_O	$\frac{I_{pk} \bullet (t_{on}+t_{off})}{8\ V_{ripple}}$	$\frac{(I_{pk}-I_{OUT})^2 \bullet t_{off}}{2\ I_{pk} \bullet V_{ripple}}$	$\frac{(I_{pk}-I_{OUT})^2 \bullet t_{off}}{2\ I_{pk} \bullet V_{ripple}}$	μF
Efficiency	$\frac{V_{IN}-V_{sat}+V_D}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT}+V_D}$	$\frac{V_{IN}-V_{sat}}{V_{IN}} \bullet \frac{V_{OUT}}{V_{OUT}+V_D-V_{sat}}$	$\frac{V_{IN}-V_{sat}}{V_{IN}} \bullet \frac{\lvert V_{OUT}\rvert}{V_{OUT}+V_D}$	
I_{IN}(Avg) (Max load condition)	$\frac{I_{pk}}{2} \bullet \frac{V_{OUT}+V_D}{V_{IN}-V_{sat}+V_D}$	$\frac{I_{pk}}{2}$	$\frac{I_{pk}}{2} \bullet \frac{\lvert V_{OUT}\rvert+V_D}{V_{IN}+\lvert V_{OUT}\rvert+V_D-V_{sat}}$	A

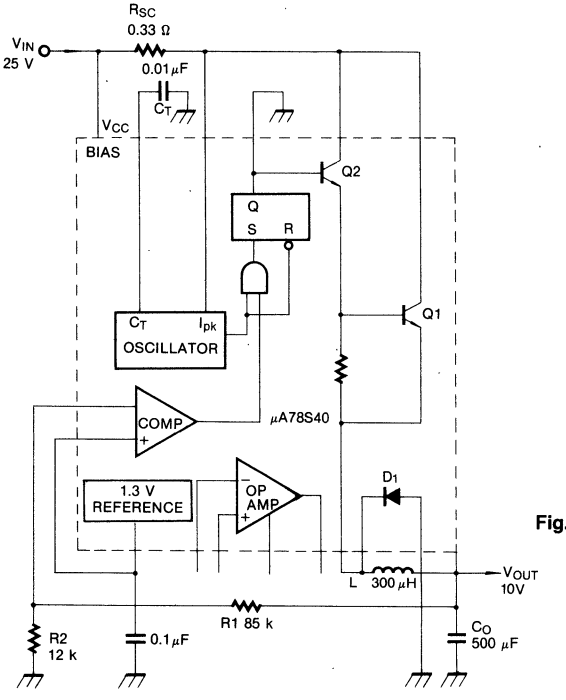


Fig. 2. Typical step-down operation (Ta = 25°C)

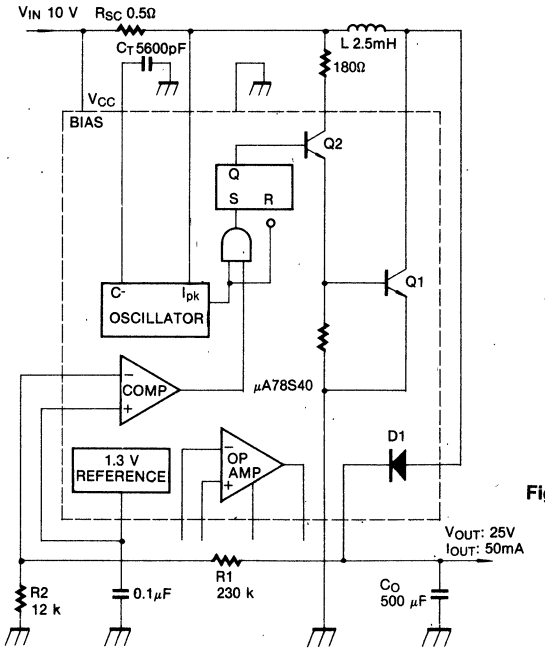


Fig. 3. Typical step-up operation (Ta = 25°C)

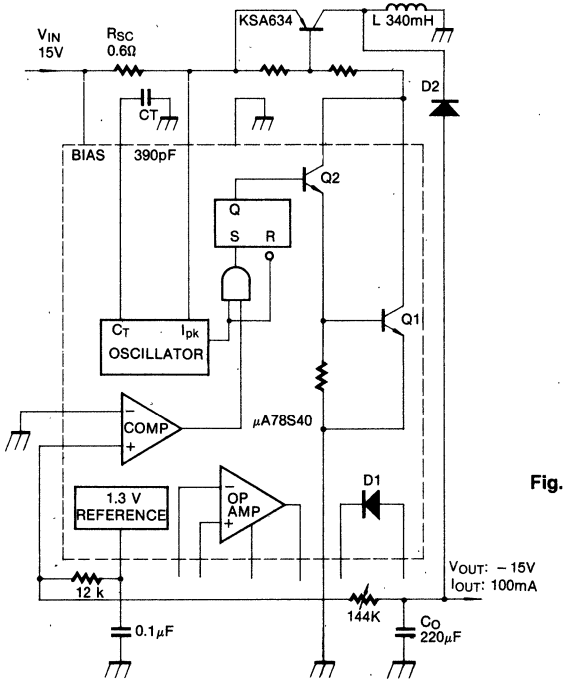


Fig. 4. Typical inverting operation (Ta = 25°C)

TYPICAL CHARACTERISTICS

Fig. 5. C_T V_S t_{off}

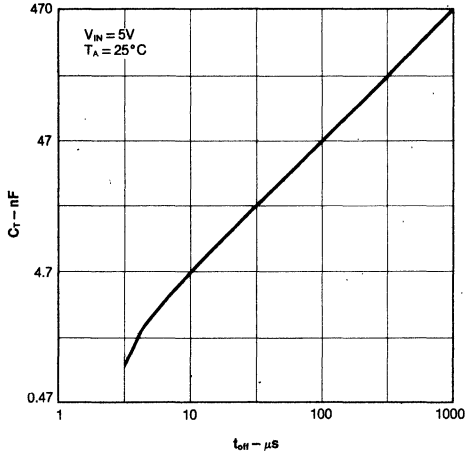


Fig. 6. V_{REF} V_S T_j

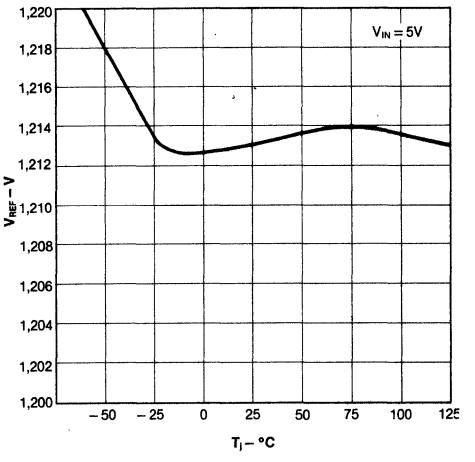


Fig. 7. Idischarge V_S V_{IN}

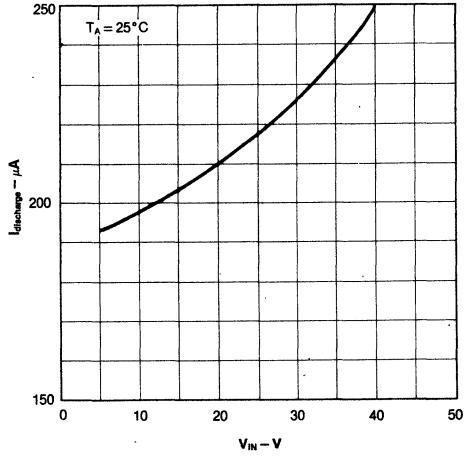
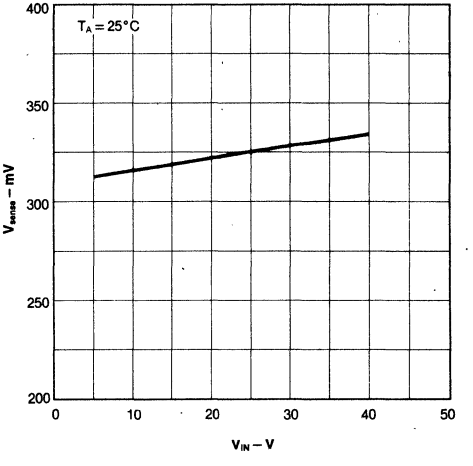


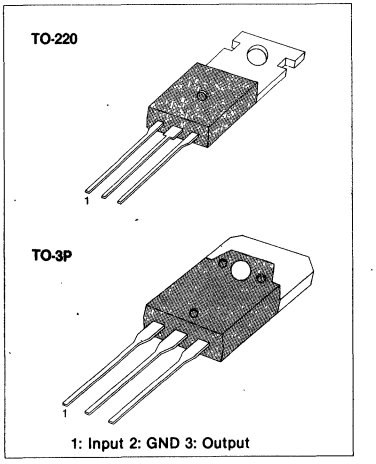
Fig. 8. V_{sense} V_S V_{IN}



4

3A POSITIVE VOLTAGE REGULATOR

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 amperes. These three-terminal regulators employ internal current limiting, thermal shutdown, and safe-area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance on A- suffix 5, 12 and 15 volts device types.
Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



1: Input 2: GND 3: Output

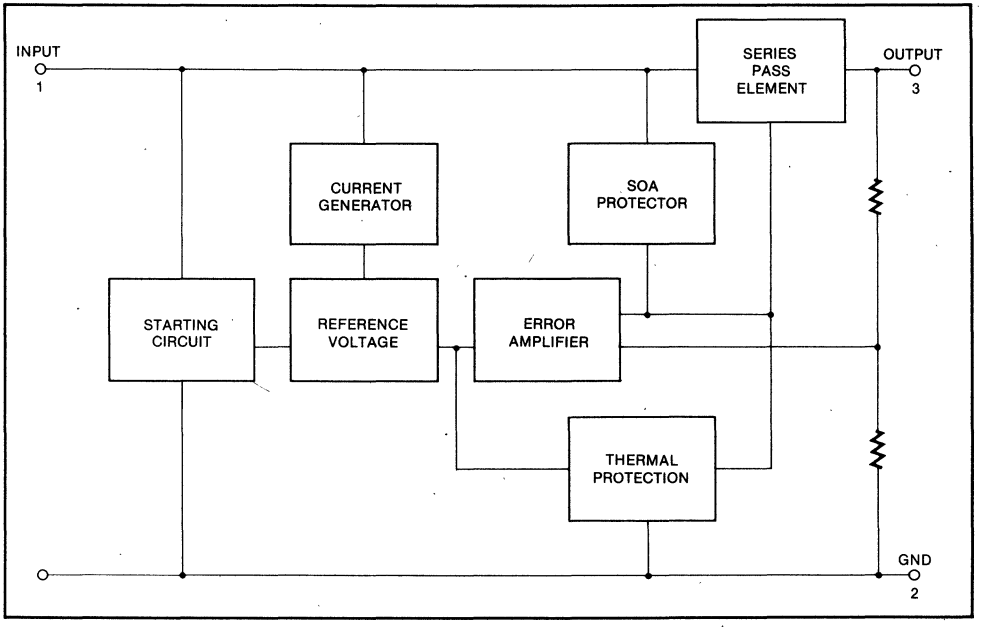
FEATURES

- **Output current in excess of 3.0 ampere**
- **Output transistor safe-area compensation**
- **Power dissipation: 25W (To-220)**
- **Internal short-circuit current limiting**
- **Internal thermal overload protection**
- **Output voltage offered in 2% and 4% tolerance (2% regulators are available in 5, 12 and 15 volt devices)**
- **No external components required**
- **Thermal regulation is specified**
- **Output voltage of 5; 6; 8; 12; 15; 18; 24V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA78TXXCT	TO-220	0 ~ 125°C
KA78TXXACT		
KA78TXXCH	TO-3P	
KA78TXXACH		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (5.0V – 12V) (15V – 24V)	V_{IN}	35 40	V_{DC} V_{DC}
Power Dissipation	P_D	Internally limited	
Thermal Resistance, Junction to Air Tc = 25°C	Θ_{JA}	65	°C/W
Thermal Resistance, Junction to Case	Θ_{JC}	2.5	°C/W
Operating Temperature Range	T_{opr}	0 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

4

KA78T05C, KA78T05AC ELECTRICAL CHARACTERISTICS

(V_{IN} = 10V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T05AC			KA78T05C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	5mA ≤ I_o ≤ 3.0A, T_j = 25°C 5mA ≤ I_o ≤ 3A; 7.3V_{DC} ≤ V_{IN} ≤ 20V_{DC}, 5mA ≤ I_o ≤ 2A	4.9 4.8	5 5	5.1 5.2	4.8 4.75	5.0 5.0	5.2 5.25	V_{DC}
Line Regulation	$\triangle V_o$	7.2V_{DC} ≤ V_{IN} ≤ 35V_{DC}, I_o = 5mA, T_j = 25°C 7.2V_{DC} ≤ V_{IN} ≤ 35V, I_o = 1.0A, T_j = 25°C 7.5V ≤ V_{IN} ≤ 20V, I_o = 2.0A 8.0V ≤ V_{IN} ≤ 12V, I_o = 3.0A		3.0	10		3.0	25	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3.0A, T_j = 25°C 5mA ≤ I_o ≤ 3.0A		10 15	25 50		10 15	30 80	mV mV
Thermal Regulation	Regthe	Pulse = 10mS, P = 20W, Ta = 25°C		0.001	0.01		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = 25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0		3.5 4.0	5.0 6.0	mA mA
Quiescent Current Change	$\triangle I_d$	7.2V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = 25°C; 7.5V ≤ V_{IN} ≤ 20V, I_o = 2A; 5mA ≤ I_o ≤ 3A		0.1	0.5		0.1	0.8	mA
Ripple Rejection	RR	8V ≤ V_{IN} ≤ 18V, f = 120Hz, I_o = 2.0A	68	75		65	75		dB
Dropout Voltage	V_D	I_o = 3A, T_j = 25°C		2.2	2.5		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = 25°C		10			10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0			2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = 25°C		1.5	2.5		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = 25°C		5.0			5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.2			0.2		mV/°C

KA78T06C ELECTRICAL CHARACTERISTICS

(V_{IN} = 11V, I_o = 3.0V, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T06C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 8.3V ≤ V_{IN} ≤ 21V, 5mA ≤ I_o ≤ 2A	5.75 5.7	6.0 6.0	6.25 6.3	V
Line Regulation	$\triangle V_o$	8.25V ≤ V_{IN} ≤ 35V I_o = 5.0mA, T_j = +25°C; 8.25V ≤ V_{IN} ≤ 35V I_o = 1.0A, T_j = +25°C; 8.6V ≤ V_{IN} ≤ 21V I_o = 2.0A 9.0V ≤ V_{IN} ≤ 13V I_o = 3.0A		4.0	30	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	Regthe	Pulse = 10mS, P = 20W, Ta = 25°C		0.002	0.03	% V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	8.25V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = +25°C; 8.6V ≤ V_{IN} ≤ 21V, I_o = 2A; 5mA ≤ I_o ≤ 3.0A		0.1	0.8	mA
Ripple Rejection	RR	9V ≤ V_{IN} ≤ 19V, f = 120Hz, I_o = 2A	61	71		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = +25°C		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Cofficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.3		mV/°C

KA78T08C ELECTRICAL CHARACTERISTICS

(V_{IN} = 14V, I_o = 3.0V, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T08C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 10.4V ≤ V_{IN} ≤ 23V, 5mA ≤ I_o ≤ 2A	7.7 7.6	8.0 8.0	8.3 8.4	V_{DC}
Line Regulation	$\triangle V_o$	10.3V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = +25°C 10.3V ≤ V_{IN} ≤ 35V, I_o = 1.0A, T_j = +25°C 10.7V ≤ V_{IN} ≤ 23V, I_o = 2.0A 11V ≤ V_{IN} ≤ 17V, I_o = 3.0A		4.0	35	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	Regthe	Pulse = 10mS, P = 20W, Ta = 25°C		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	10.3V ≤ V_{IN} ≤ 35V, I_o = 5mA, T_j = +25°C 10.7V ≤ V_{IN} ≤ 23V, I_o = 2A 5mA ≤ I_o ≤ 3A		0.1	0.8	mA
Ripple Rejection	RR	11V ≤ V_{IN} ≤ 21V, f = 120Hz, I_o = 2A	61	71		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = +25°C		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Cofficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.3		mV/°C

KA78T12C, KA78T12AC ELECTRICAL CHARACTERISTICS

(V_{IN} = 19V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise noted)

Characteristic	Symbol	Test Conditions	KA78T12AC			KA78T12C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	5mA≤I_o≤3A, T_j = 25°C 5mA≤I_o≤3A; 5mA≤I_o≤2A, 14.5V≤V_{IN}≤27V	11.75 11.5	12 12	12.25 12.5	11.5 11.4	12 12	12.5 12.6	V_{DC}
Line Regulation	$\triangle V_o$	14.5V_{DC}≤V_{IN}≤35V_{DC}, I_o = 5mA, T_j = +25°C; 14.5V_{DC}≤V_{IN}≤35V_{DC}, I_o = 1.0A, T_j = +25°C; 14.9V_{DC}≤V_{IN}≤27V_{DC}, I_o = 2.0A; 16V_{DC}≤V_{IN}≤22V_{DC}, I_o = 3.0A		6.0	18		6.0	45	mV
Load Regulation	$\triangle V_o$	5mA≤I_o≤3A, T_j = +25°C 5mA≤I_o≤3A		10 15	25 50		10 15	30 80	mV
Thermal Regulation	Regth	Pulse = 10mS, P = 20W, Ta = 25°C		0.001	0.01		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA≤I_o≤3A, T_j = +25°C 5mA≤I_o≤3A		3.5 4.0	5.0 6.0		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	14.5V_{DC}≤V_{IN}≤35V_{DC}, I_o = 5mA, T_j = 25°C; 14.9V_{DC}≤V_{IN}≤27V_{DC}, I_o = 2A; 5.0mA≤I_o≤3.0A		0.1	0.5		0.1	0.8	mA
Ripple Rejection	RR	15V_{DC}≤V_{IN}≤25V_{DC}, f = 120Hz, I_o = 2.0A	61	67		57	67		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz≤f≤100KHz, T_j = +25°C		10			10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0			2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 35V, T_j = +25°C		1.5	2.5		1.5	2.5	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0			5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.5			0.5		mV/°C

KA78T15C, KA78T15AC ELECTRICAL CHARACTERISTICS

(V_{IN} = 23V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise noted)

Characteristic	Symbol	Test Conditions	KA78T15AC			KA78T15C			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A; 17.5V_{DC} ≤ V_{IN} ≤ 30V_{DC}, 5mA ≤ I_o ≤ 2A	14.7 14.4	15 15	15.3 15.6	14.4 14.25	15 15	15.6 15.75	V_{DC}
Line Regulation	$\triangle V_o$	17.6V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C 17.6V ≤ V_{IN} ≤ 40V, I_o = 1A, T_j = +25°C; 18V ≤ V_{IN} ≤ 30V, I_o = 2.0A; 20V ≤ V_{IN} ≤ 26V, I_o = 3.0A		7.5	22		7.5	55	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	25 50		10 15	30 80	mV
Thermal Regulation	Regth	Pulse = 10mS, P = 20W, Ta = 25°C		0.001	0.01		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	17.6V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 18V ≤ V_{IN} ≤ 30V, I_o = 2A; 5mA ≤ I_o ≤ 3A		0.1	0.5		0.1	0.8	mA
Ripple Rejection	RR	18.5V_{DC} ≤ V_{IN} ≤ 28.5V_{DC}, f = 120Hz, I_o = 2.0A	60	65		55	65		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10			10		$\mu V/V_o$
Output Resistance	R_o	f = 1.0KHz		2.0			2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 40V, T_j = +25°C		1.0	2.0		1.0	2.0	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0			5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.6			0.6		mV/°C

KA78T18C ELECTRICAL CHARACTERISTICS

(V_{IN} = 27V, I_o = 3.0V, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T18C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA≤I_o≤3A, T_j = +25°C 5.0mA≤I_o≤3A; 20.6V≤V_{IN}≤33V, 5mA≤I_o≤2A	17.3 17.1	18 18	18.7 18.9	V_{DC}
Line Regulation	$\triangle V_o$	20.7V≤V_{IN}≤40V, I_o = 5mA, T_j = +25°C; 20.7V≤V_{IN}≤40V, I_o = 1A, T_j = +25°C; 21.2V≤V_{IN}≤33V, I_o = 2.0A 24V≤V_{IN}≤30V, I_o = 3A		9.0	80	mV
Load Regulation	$\triangle V_o$	5mA≤I_o≤3A, T_j = +25°C 5mA≤I_o≤3A		10 15	30 80	mV
Thermal Regulation	Regthe	Pulse = 10mS, P = 20W, Ta = 25°C		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA≤I_o≤3A, T_j = +25°C 5mA≤I_o≤3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	20.7V≤V_{IN}≤40V, I_o = 5mA, T_j = +25°C; 21.2V≤V_{IN}≤33V, I_o = 2.0A; 5mA≤I_o≤3.0A		0.1	0.8	mA
Ripple Rejection	RR	22V≤V_{IN}≤32V, f = 120Hz, I_o = 2.0A	54	64		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz≤f≤100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_O	f = 1.0KHz		2.0		mΩ
Output Circuit Current Limit	I_{SC}	V_{IN} = 40V, T_j = +25°C		1.0	2.0	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		0.7		mV/°C

KA78T24C ELECTRICAL CHARACTERISTICS

(V_{IN} = 33V, I_o = 3.0A, T_j = 0°C to 125°C, $P_o \leq P_{max}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	KA78T24C			Unit
			Min	Typ	Max	
Output Voltage	V_o	5.0mA ≤ I_o ≤ 3A, T_j = +25°C 5.0mA ≤ I_o ≤ 3A; 27.3V ≤ V_{IN} ≤ 39V, 5mA ≤ I_o ≤ 2A	23 22.8	24 24	25 25.2	V_{DC}
Line Regulation	$\triangle V_o$	27V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 27V ≤ V_{IN} ≤ 40V, I_o = 1.0A, T_j = +25°C; 27.5V ≤ V_{IN} ≤ 39V, I_o = 2.0A; 30V ≤ V_{IN} ≤ 36V, I_o = 3.0A		12	90	mV
Load Regulation	$\triangle V_o$	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		10 15	30 80	mV
Thermal Regulation	Regthe	Pulse = 10mS, P = 20W, Ta = 25°C		0.002	0.03	%V_o/W
Quiescent Current	I_d	5mA ≤ I_o ≤ 3A, T_j = +25°C 5mA ≤ I_o ≤ 3A		3.5 4.0	5.0 6.0	mA
Quiescent Current Change	$\triangle I_d$	27V ≤ V_{IN} ≤ 40V, I_o = 5mA, T_j = +25°C; 27.5V ≤ V_{IN} ≤ 39V, I_o = 2A; 5mA ≤ I_o ≤ 3A		0.1	0.8	mA
Ripple Rejection	RR	28V ≤ V_{IN} ≤ 38V, f = 120Hz, I_o = 2.0A	51	61		dB
Dropout Voltage	V_D	I_o = 3A, T_j = +25°C		2.2	2.5	V_{DC}
Output Noise Voltage	V_N	10Hz ≤ f ≤ 100KHz, T_j = +25°C		10		$\mu V/V_o$
Output Resistance	R_O	f = 1.0KHz		2.0		mΩ
Short Circuit Current Limit	I_{SC}	V_{IN} = 40V, T_j = +25°C		1.0	2.0	A
Peak Output Current	I_{peak}	T_j = +25°C		5.0		A
Average Temperature Coefficient of Output Voltage	$\triangle V_O/\triangle T$	I_o = 5.0mA		1.0		mV/°C

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 TEMPERATURE STABILITY

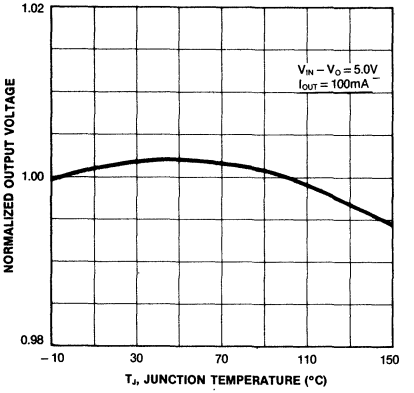


Fig. 2 OUTPUT IMPEDANCE

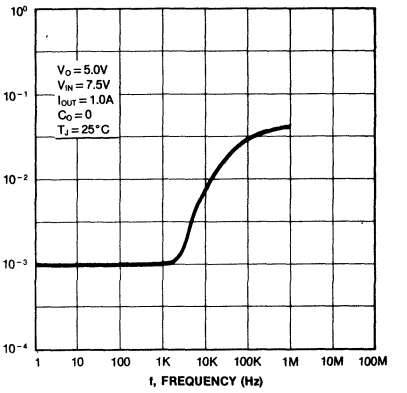


Fig. 3 RIPPLE REJECTION V_S FREQUENCY

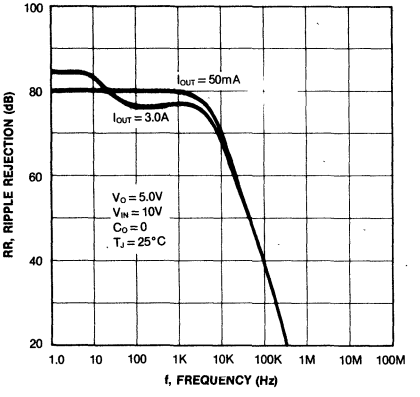


Fig. 4 RIPPLE REJECTION V_S OUTPUT CURRENT

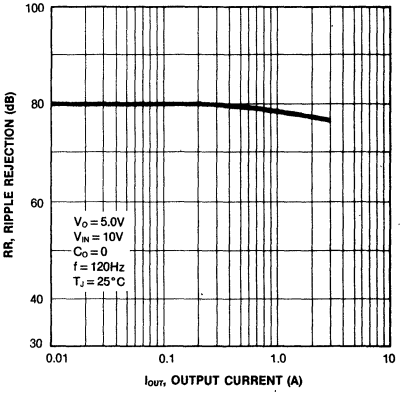


Fig. 5 QUIESCENT CURRENT V_S INPUT VOLTAGE

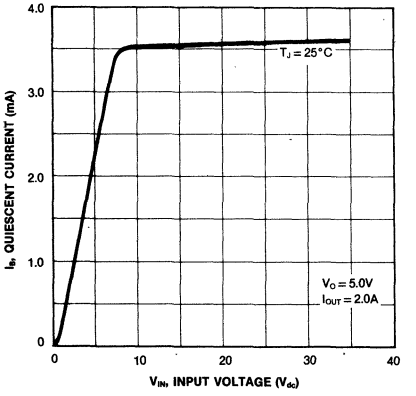


Fig. 6 QUIESCENT CURRENT V_S OUTPUT CURRENT

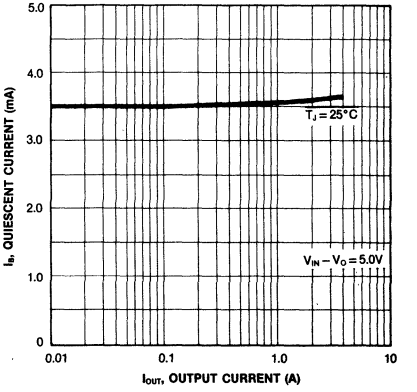


Fig. 7 DROPOUT VOLTAGE

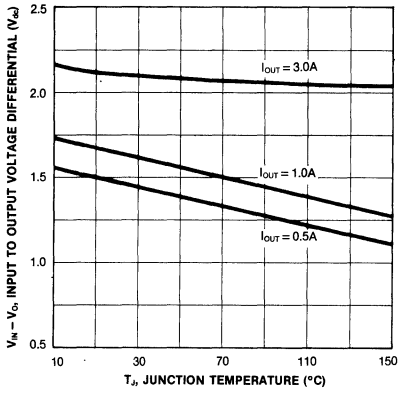


Fig. 8 PEAK OUTPUT CURRENT

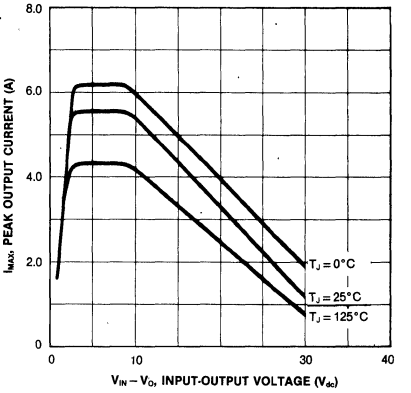


Fig. 9 LINE TRANSIENT RESPONSE

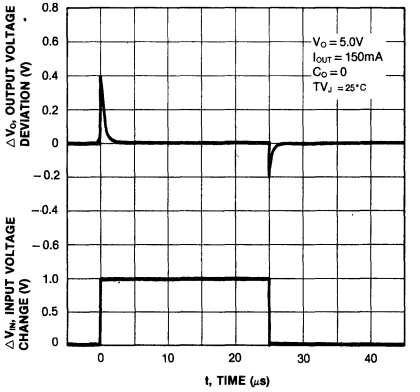


Fig. 10 LOAD TRANSIENT RESPONSE

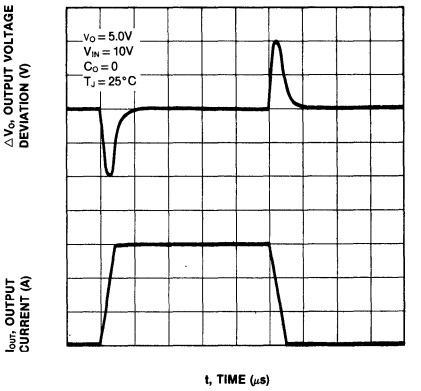
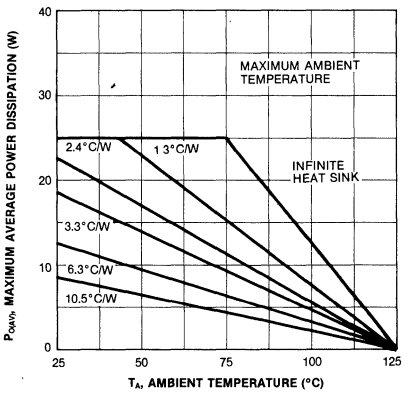


Fig. 11 MAXIMUM AVERAGE POWER DISSIPATION



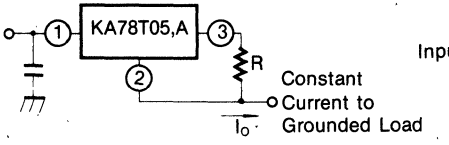
4

APPLICATION INFORMATIONS

The KA78T00,A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provided good high-frequency characteristics to insure stable operation under all load conditions. A 0.33μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Fig. 12—CURRENT REGULATOR



The KA78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation, the KA78T05 is chosen in this application. Resistor R determines the current as follows:

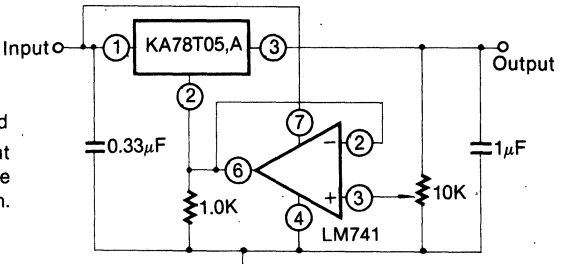
$$I_O = \frac{5.0V}{R} + I_B$$

$\triangle I_B = 0.7mA$ over line, load and temperature changes

$I_B = 3.5mA$

For example, a 2-ampere current source would require R to be a 2.5 ohm, 15W resistor and the output voltage compliance would be the input voltage less 7.5 volts.

Fig. 13—ADJUSTABLE OUTPUT REGULATOR

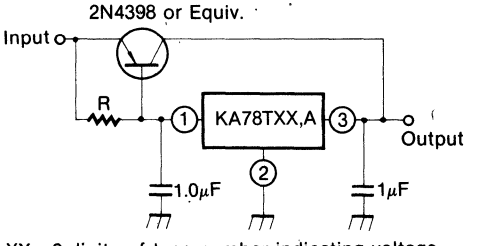


V_O, 8.0V to 20V

$V_{IN} - V_O \geq 2.5V$

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 volts greater than the regulator voltage.

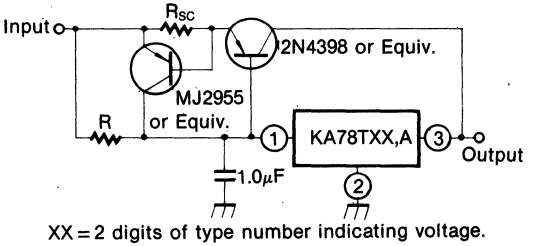
Fig. 14—CURRENT BOOST REGULATOR



XX = 2 digits of type number indicating voltage.

The KA78T00,A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 amperes. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short-circuit proof. Input-output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Fig. 15—CURRENT BOOST WITH SHORT-CIRCUIT PROTECTION



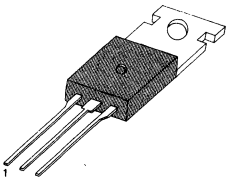
XX = 2 digits of type number indicating voltage.

The circuit of Figure 18 can be modified to provide supply protection against short circuits by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, an eight-ampere power transistor is specified.

3-TERMINAL 1A POSITIVE VOLTAGE REGULATORS

The MC78XX/MC78XXA series of three-terminal positive regulators are available in TO-220 package and with several fixed output voltages, making it useful in a wide range of applications. These Regulators can provide local oncard regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



1: Input 2: GND 3: Output

FEATURES

- **Output Current up to 1.5A**
- **Output voltages of 5; 6; 8; 8.5; 9; 10; 11; 12; 15; 18; 24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC78XXIT	TO-220	−40°C ~ +125°C
MC78XXCT	TO-220	0°C ~ +125°C
MC78XXACT	TO-220	

BLOCK DIAGRAM

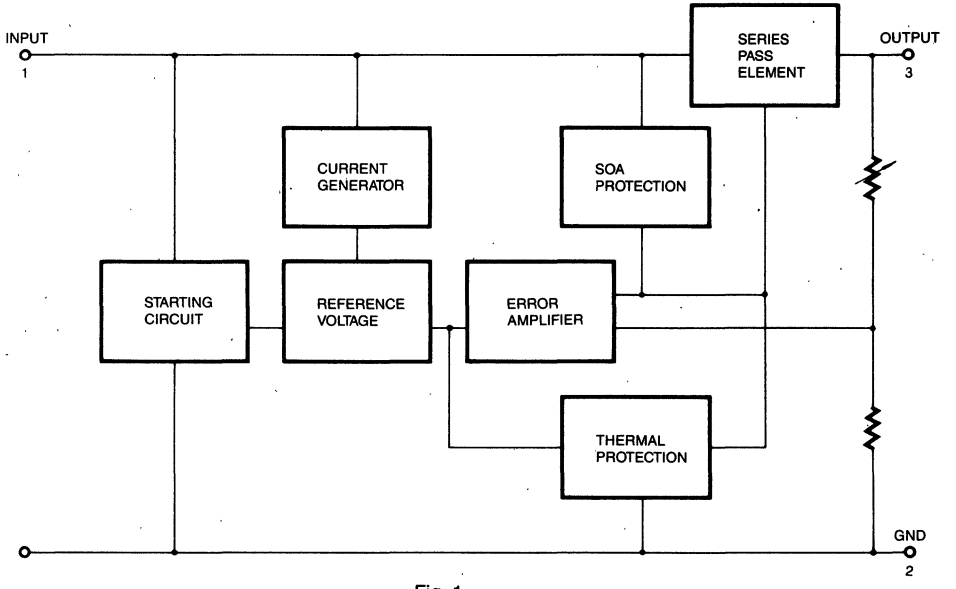


Fig. 1

SCHEMATIC DIAGRAM

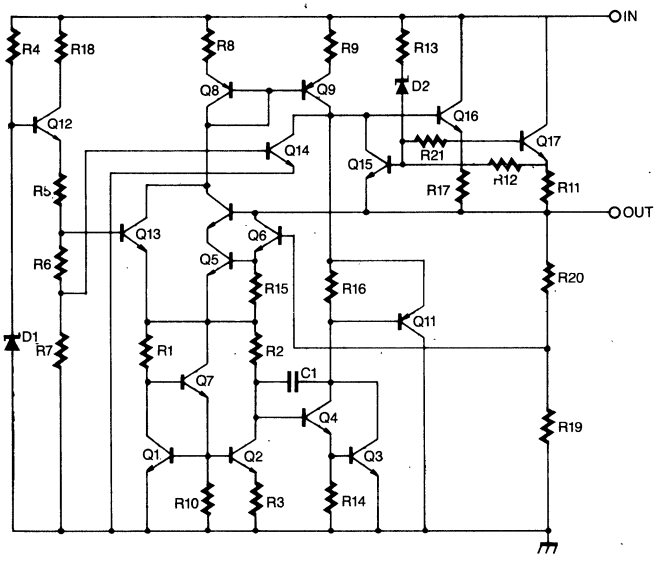


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o = 5V to 18V)	V_i	35	V
(for V_o = 24V)	V_i	40	V
Thermal Resistance Junction-Cases	Θ_{JC}	5	°C/W
Thermal Resistance Junction-Air	Θ_{JA}	65	°C/W
Operating Temperature Range MC78XXI	T_{opr}	−40 ~ +125	°C
MC78XXC/AC		0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS MC7805

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 10V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7805I			MC7805C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		4.8	5.0	5.2	4.8	5.0	5.2	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 7V$ to $20V$ $V_i = 8V$ to $20V$		4.75	5.0	5.25	4.75	5.0	5.25	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 7V$ to $25V$		3.0	100		3.0	100	mV
			$V_i = 8V$ to $12V$		1.0	50		1.0	50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		15	100		15	100	mV
			$I_o = 250mA$ to $750mA$		5	50		5	50	
Quiescent Current	I_d	$T_j = 25°C$			4.2	8		4.2	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 7V$ to $25V$							1.3	
		$V_i = 8V$ to $25V$				1.3				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1.1			-1.1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			40			40		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 8$ to $18V$		62	78		62	78		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			750			750		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

4

ELECTRICAL CHARACTERISTICS MC7806

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 11V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7806I			MC7806C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		5.75	6.0	6.25	5.75	6.0	6.25	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 8.0V$ to $21V$ $V_i = 9.0V$ to $21V$		5.7	6.0	6.3	5.7	6.0	6.3	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 8V$ to $25V$		5	120		5	120	mV
			$V_i = 9V$ to $13V$		1.5	60		1.5	60	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		14	120		14	120	mV
			$I_o = 250mA$ to $750mA$		4	60		4	60	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 8V$ to $25V$							1.3	
		$V_i = 9V$ to $25V$				1.3				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−0.8			−0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			45			45		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 9$ to $19V$		59	75		59	75		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			19			19		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			550			550		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7808

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 14V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7808I			MC7808C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		7.7	8.0	8.3	7.7	8.0	8.3	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 10.5V$ to $23V$ $V_i = 11.5V$ to $23V$		7.6	8.0	8.4	7.6	8.0	8.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 10.5V$ to $25V$		6.0	160		6.0	160	mV
			$V_i = 11.5V$ to $17V$		2.0	80		2.0	80	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		12	160		12	160	mV
			$I_o = 250mA$ to $750mA$		4.0	80		4.0	80	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 10.5V$ to $25V$							1.0	
		$V_i = 11.5V$ to $25V$				1.0				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−0.8			−0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			52			52		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 11.5V$ to 21.5		56	72		56	72		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			16			16		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			450			450		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7885

(Refer to test circuit $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 14.5V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7885I			MC7885C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		8.15	8.5	8.85	8.15	8.5	8.85	V
		$I_o = 5mA$ to $1.0A$, $P_D \leq 15W$ $V_i = 11V$ to $23.5V$					8.1	8.5	8.9	
		$V_i = 12V$ to $23.5V$		8.1	8.5	8.9				
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 11V$ to $25V$		12	170		12	170	mV
			$V_i = 11.5V$ to $18V$		5.0	85		5.0	85	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		45	170		45	170	mV
			$I_o = 250mA$ to $750mA$		16	85		16	85	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8.0		4.3	8.0	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 11V$ to $25V$							1.0	
		$V_i = 12V$ to $25V$				1.0				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			−1.0			−1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$, $Ta = 25°C$			55			55		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = 12V$ to $22V$		56	72		56	72		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$			2.0			2.0		V
Output Resistance	R_0	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{sc}	$V_i = 35V$, $T_j = 25°C$			450			450		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
  MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
  MC78XXC: $T_{min} = 0°C$, $T_{max} = 125°C$
* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7809

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 15V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7809I			MC7809C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		8.65	9	9.35	8.65	9	9.35	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 11.5V$ to $24V$ $V_i = 12.5V$ to $24V$		8.6	9	9.4	8.6	9	9.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 11.5V$ to $25V$		6	180		6	180	mV
			$V_i = 12V$ to $25V$		2	90		2	90	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	180		12	180	mV
			$I_o = 250mA$ to $750mA$		4	80		4	90	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8.0	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 11.5V$ to $26V$							1.3	
		$V_i = 12.5V$ to $26V$				1.3				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			58			58		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 13V$ to $23V$		56	71		56	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			450			450		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7810

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 16V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7810I			MC7810C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		9.6	10	10.4	9.6	10	10.4	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 12.5V$ to $25V$ $V_i = 13.5V$ to $25V$		9.5	10	10.5	9.5	10	10.5	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 12.5V$ to $25V$		10	200		10	200	mV
			$V_i = 13V$ to $20V$		3	100		3	100	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	200		12	200	mV
			$I_o = 250mA$ to $750mA$		4	100		4	100	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 12.5V$ to $29V$							1.0	
		$V_i = 13.5V$ to $29V$				1.0				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1			−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			58			58		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 14V$ to $23V$		56	71		56	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			17			17		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			420			420		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7811

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 18V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7811I			MC7811C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		10.6	11	11.4	10.6	11	11.4	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 13.5V$ to $26V$					10.5	11	11.5	
		$V_i = 14.5V$ to $26V$		10.5	11	11.5				
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 13.5$ to $25V$		10	220		10	220	mV
			$V_i = 14$ to $21V$		3.0	110		3.0	110	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		12	220		12	220	mV
			$I_o = 250mA$ to $750mA$		4	110		4	110	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 13.5V$ to $29V$							1.0	
		$V_i = 14.5V$ to $29V$				1.0				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1			-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			70			70		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 14V$ to $24V$		55	71		55	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			18			18		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			390			390		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7812

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 19V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7812I			MC7812C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		11.5	12	12.5	11.5	12	12.5	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_{in} = 14.5V$ to $27V$ $V_i = 15.5V$ to $27V$		11.4	12	12.6	11.4	12	12.6	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 14.5$ to $30V$		10	240		10	240	mV
			$V_i = 16$ to $22V$		3.0	120		3.0	120	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	240		12	240	mV
			$I_o = 250mA$ to $750mA$		4.0	120		4.0	120	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 14.5V$ to $30V$							1.0	
		$V_i = 15V$ to $30V$				1.0				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			−1			−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			75			75		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 15V$ to $25V$		55	71		55	71		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			18			18		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			350			350		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7815

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 23V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7815I			MC7815C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		14.4	15	15.6	14.4	15	15.6	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 17.5V$ to $30V$ $V_i = 18.5V$ to $30V$		14.25	15	15.75	14.25	15	15.75	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 17.5$ to $30V$		11	300		11	300	mV
			$V_i = 20$ to $26V$		3	150		3	150	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $1.5A$		12	300		12	300	mV
			$I_o = 250mA$ to $750mA$		4	150		4	150	
Quiescent Current	I_d	$T_j = 25°C$			4.4	8		4.4	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1.0A$				0.5			0.5	mA
		$V_i = 17.5V$ to $30V$							1.0	
		$V_i = 18.5V$ to $30V$				1.0				
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			−1			−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			90			90		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 18.5V$ to $28.5V$		54	70		54	70		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			19			19		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			230			230		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7818

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 27V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7818I			MC7818C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		17.3	18	18.7	17.3	18	18.7	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 21V$ to $33V$ $V_i = 22V$ to $33V$		17.1	18	18.9	17.1	18	18.9	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 21$ to $33V$		15	360		15	360	mV
			$V_i = 24$ to $30V$		5	180		5	180	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	360		12	360	mV
			$I_o = 250mA$ to $750mA$		4.0	180		4.0	180	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 21V$ to $33V$							1	
		$V_i = 22V$ to $33V$				1				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1			−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			110			110		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 22V$ to $32V$		53	69		53	69		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			22			22		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			200			200		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
  MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
  MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$
* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC7824

(Refer to test circuit, $T_{min} < T_j < T_{max}$, $I_o = 500mA$, $V_i = 33V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC7824I			MC7824C			Unit
				Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$		23	24	25	23	24	25	V
		$5.0mA \leq I_o \leq 1.0A$, $P_D \leq 15W$ $V_i = 27V$ to $38V$ $V_i = 28V$ to $38V$		22.8	24	25.2	22.8	24	25.2	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = 27V$ to $38V$		18	480		18	480	mV
			$V_i = 30V$ to $36V$		6	240		6	240	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5mA$ to $1.5A$		12	480		12	480	mV
			$I_o = 250mA$ to $750mA$		4	240		4	240	
Quiescent Current	I_d	$T_j = 25°C$			4.3	8		4.3	8	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$				0.5			0.5	mA
		$V_i = 27V$ to $38V$							1	
		$V_i = 28V$ to $38V$				1				
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1.5			-1.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			170			170		μV
Ripple Rejection	RR	$f = 120Hz$ $V_i = 28V$ to $38V$		50	66		50	66		dB
Dropout Voltage	V_D	$I_o = 1A$, $T_j = 25°C$			2			2		V
Output Resistance	R_O	$f = 1KHz$			28			28		mΩ
Short Circuit Current	I_{SC}	$V_i = 35V$, $T_j = 25°C$			150			150		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2			2.2		A

* $T_{min} < T_j < T_{max}$
MC78XXI: $T_{min} = -40°C$, $T_{max} = 125°C$
MC78XXC, $T_{min} = 0°C$, $T_{max} = 125°C$

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

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ELECTRICAL CHARACTERISTICS MC7805AC

(Refer to the test circuits, T_j=0 to 125°C, I_o=1A, V_i=10V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	4.9	5	5.1	V
		I_o=5mA to 1A, $P_D \leq$ 15W, V_i=7.5 to 20V	4.8	5	5.2	
*Line Regulation	ΔV_o	V_i=7.5 to 25V, I_o=500mA		7	50	mV
		V_i=8 to 12V		10	50	
		T_j=25°C, V_i=7.3 to 25V		7	50	
		T_j=25°C, V_i=8 to 12V		2	25	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		25	100	mV
		I_o=5mA to 1A		25	100	
		I_o=250 to 750mA		8	50	
Quiescent Current	I_d	T_j=25°C		4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=8 to 25V, I_o=500mA			0.8	
		V_i=7.5 to 20V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		-1.1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz: T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA, V_i=8 to 18V		68		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		750		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7806AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=11V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	5.88	6	6.12	V
		I_o=5mA to 1A, $P_D \leq$15W V_i=8.6 to 21V	5.76	6	6.24	
*Line Regulation	ΔV_o	V_i=8.6 to 25V, I_o=500mA		9	60	mV
		V_i=9 to 13V		11	60	
		T_j=25°C, V_i=8.3 to 21V		9	60	
		T_j=25°C, V_i=9 to 13V		3	30	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		43	100	mV
		I_o=5mA to 1A		43	100	
		I_o=250 to 750mA		16	50	
Quiescent Current	I_d	T_j=25°C		4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=9 to 25V, I_o=500mA			0.8	
		V_i=8.6 to 21V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		-0.8		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=9 to 19V		65		dB
Dropout Voltage	V_d	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		17		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		550		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7808AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=14V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C		7.84	8	8.16	V
		I_o=5mA to 1A, $P_D \leq$ 15W V_i=10.6 to 23V		7.7	8	8.3	
*Line Regulation	ΔV_o	V_i=10.6 to 25V, I_o=500mA			12	80	mV
		V_i=11 to 17V			15	80	
		T_j=25°C	V_i=10.4 to 23V		12	80	
			V_i=11 to 17V		5	40	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A			45	100	mV
		I_o=5mA to 1A			45	100	
		I_o=250 to 750mA			16	50	
Quiescent Current	I_d	T_j=25°C			4.3	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A				0.5	mA
		V_i=11 to 25V, I_o=500mA				0.8	
		V_i=10.6 to 23V, T_j=25°C				0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA			−0.8		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C			10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=11.5 to 21.5V			62		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C			2		V
Output Resistance	R_o	f=1KHz			18		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C			450		mA
Peak Current	I_{peak}	T_j=25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7885AC

(Refer to the test circuits, $T_j = 0$ to 125°C, $I_o = 1A$, $V_i = 14V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		8.33	8.5	8.67	V
		$I_o = 5mA$ to 1.0A, $P_D \leq 15W$ $V_i = 11.2V$ to 23.5V		8.15	8.5	8.85	
Line Regulation	$\triangle V_o$	$V_i = 11.2V$ to 25V $I_o = 500mA$			12	85	mV
		$V_i = 11.5V$ to 18V			15	43	
		$T_j = 25°C$	$V_i = 11V$ to 23.5V		12	85	
			$V_i = 11.5V$ to 18V		5.0	43	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to 1.5A			45	100	mV
		$I_o = 5mA$ to 1.0A			45	100	
		$I_o = 250mA$ to 750mA			16	50	
Quiescent Current	I_d	$T_j = 25°C$			4.3	6.0	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to 1.0A				0.5	mA
		$V_i = 11.5V$ to 25V, $T_j = 25°C$				0.8	
		$V_i = 11.2V$ to 23.5V, $I_o = 500mA$				0.8	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1.0		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, Ta = 25°C			10		$\mu V/V_o$
Ripple Rejection	RR	f = 120Hz, $V_i = 12V$ to 22V $I_o = 500mA$			62		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$			2.0		V
Output Resistance	R_o	f = 1KHz			17		m
Short Circuit Current	I_{short}	$V_i = 35V$, $T_a = 25°C$			450		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7809AC

(Refer to the test circuits, $T_j = 0$ to 125°C, $I_o = 1A$, $V_i = 15V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		8.82	9.0	9.18	V
		$I_o = 5mA$ to 1.0A, $P_D \leq 15W$ $V_i = 11.2V$ to 24V		8.65	9.0	9.35	
Line Regulation	$\triangle V_o$	$V_i = 11.7V$ to 25V $I_o = 500mA$			12	90	mV
		$V_i = 12.5V$ to 19V			15	45	
		$T_j = 25°C$	$V_i = 11.5V$ to 24V		12	90	
			$V_i = 12.5V$ to 19V		5.0	45	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to 1.0A			46	100	mV
		$I_o = 5mA$ to 1.0A			46	100	
		$I_o = 250mA$ to 750mA			17	50	
Quiescent Current	I_d	$T_j = 25°C$			4.3	6.0	mA
Quiescent Current Change	$\triangle I_d$	$V_i = 11.7V$ to 24V, $T_j = 25°C$				0.8	mA
		$V_i = 12V$ to 25V, $I_o = 500mA$				0.8	
		$I_o = 5mA$ to 1.0A				0.5	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1.0		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, Ta = 25°C			10		$\mu V/V_o$
Ripple Rejection	RR	f = 120Hz, $V_i = 12V$ to 22V $I_o = 500mA$			62		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$			2.0		V
Output Resistance	R_o	f = 1KHz			17		m
Short Circuit Current	I_{short}	$V_i = 35V$, $T_j = 25°C$			420		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7811AC

(Refer to the test circuits, $T_j = 0$ to 125°C, $I_o = 1A$, $V_i = 18V$, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$ unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		10.8	11.0	11.2	V
		$I_o = 5mA$ to $1.0A$, $P_D \leq 15W$ $V_i = 13.8V$ to $26V$		10.6	11.0	11.4	
Line Regulation	$\triangle V_o$	$V_i = 13.8V$ to $27V$ $I_o = 500mA$			13	110	mV
		$V_i = 15V$ to $21V$			16	55	
		$T_j = 25°C$	$V_i = 13.5V$ to $26V$		13	110	
			$V_i = 15V$ to $21V$		6.0	5.5	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			46	100	mV
		$I_o = 5mA$ to $1.0A$			46	100	
		$I_o = 250mA$ to $750mA$			17	50	
Quiescent Current	I_d	$T_j = 25°C$			4.4	6.0	mA
						6.0	
Quiescent Current Change	$\triangle I_d$	$V_i = 13.8V$ to $26V$, $T_j = 25°C$				0.8	mA
		$V_i = 14V$ to $27V$, $I_o = 500mA$				0.8	
		$I_o = 5mA$ to $1.0A$				0.5	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			−1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$, $Ta = 25°C$			10		$\mu V/V_o$
Ripple Rejection	RR	$f = 120Hz$, $V_i = 14V$ to $24V$ $I_o = 500mA$			61		dB
Dropout Voltage	V_D	$I_o = 1.0A$, $T_j = 25°C$			2.0		V
Output Resistance	R_o	$f = 1KHz$			18		m
Short Circuit Current	I_{short}	$V_i = 35V$, $T_j = 25°C$			390		mA
Peak Current	I_{peak}	$T_j = 25°C$			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7812AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=19V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C		11.75	12	12.25	V
		I_o=5mA to 1A, $P_D \leq$ 15W V_i=14.8 to 27V		11.5	12	12.5	
*Line Regulation	ΔV_o	V_i=14.8 to 30V, I_o=500mA			13	120	mV
		V_i=16 to 22V			16	120	
		T_j=25°C	V_i=14.5 to 27V		13	120	
			V_i=16 to 22V		6	60	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A			46	100	mV
		I_o=5mA to 1A			46	100	
		I_o=250 to 750mA			17	50	
Quiescent Current	I_d	T_j=25°C			4.4	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A				0.5	mA
		V_i=15 to 30V, I_o=500mA				0.8	
		V_i=14.8 to 27V, T_j=25°C				0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA			−1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C			10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=15 to 25V			60		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C			2		V
Output Resistance	R_o	f=1KHz			18		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C			350		mA
Peak Current	I_{peak}	T_j=25°C			2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7815AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=23V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	14.7	15	15.3	V
		I_o=5mA to 1A, $P_D \leq$ 15W, V_i=17.7 to 30V	14.4	15	15.6	
*Line Regulation	ΔV_o	V_i=17.9 to 30V, I_o=500mA		13	150	mV
		V_i=20 to 26V		16	150	
		T_j=25°C, V_i=17.5 to 30V		13	150	
		T_j=25°C, V_i=20 to 26V		6	75	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		52	100	mV
		I_o=5mA to 1A		52	100	
		I_o=250 to 750mA		20	50	
Quiescent Current	I_d	T_j=25°C		4.4	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=17.5 to 30V, I_o=500mA			0.8	
		V_i=17.5 to 30V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		−1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz, T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA, V_i=18.5 to 28.5V		58		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		230		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7818AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=27V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	17.64	18	18.36	V
		I_o=5mA to 1A, $P_D \leq$ 15W, V_i=21 to 33V	17.3	18	18.7	
*Line Regulation	ΔV_o	V_i=21 to 33V, I_o=500mA		25	180	mV
		V_i=24 to 30V		28	180	
		T_j=25°C, V_i=20.6 to 33V		25	180	
		T_j=25°C, V_i=24 to 30V		10	90	
*Load Regulation	ΔV_o	T_j=25°C, I_o=5mA to 1.5A		55	100	mV
		I_o=5mA to 1A		55	100	
		I_o=250 to 750mA		22	50	
Quiescent Current	I_d	T_j=25°C		4.5	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=21 to 33V, I_o=500mA			0.8	
		V_i=21 to 33V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=5mA		−1		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz, T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA, V_i=22 to 32V		57		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		19		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		200		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS MC7824AC

(Refer to the test circuits, T_j=0 to 150°C, I_o=1A, V_i=33V, C_i=0.33μF, C_o=0.1μF unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	T_j=25°C	23.5	24	24.5	V
		I_o=5mA to 1A, $P_D \leq$ 15W V_i=27.3 to 38V	23	24	25	
*Line Regulation	ΔV_o	V_i=27 to 38V, I_o=500mA		31	240	mV
		V_i=30 to 36V		35	240	
		T_j=25°C, V_i=26.7 to 38V		31	240	
		T_j=25°C, V_i=30 to 36V		14	120	
*Load Regulation	ΔV_o	T_j=25°C I_o=5mA to 1.5A		60	100	mV
		I_o=5mA to 1A		60	100	
		I_o=250 to 750mA		25	50	
Quiescent Current	I_d	T_j=25°C		4.6	6	mA
Quiescent Current Change	ΔI_d	I_o=5mA to 1A			0.5	mA
		V_i=27.3 to 38V, I_o=500mA			0.8	
		V_i=27.3 to 38V, T_j=25°C			0.8	
Output Voltage Drift	$\frac{\Delta V_o}{\Delta T}$	I_o=1mA		−1.5		mV/°C
Output Noise Voltage	V_N	f=10Hz to 100KHz T_a=25°C		10		$\frac{\mu V}{V_o}$
Ripple Rejection	RR	f=120Hz, I_o=500mA V_i=28 to 38V		54		dB
Dropout Voltage	V_D	I_o=1A, T_j=25°C		2		V
Output Resistance	R_o	f=1KHz		20		mΩ
Short Circuit Current	I_{sc}	V_i=35V, T_a=25°C		150		mA
Peak Current	I_{peak}	T_j=25°C		2.2		A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

TEST CIRCUIT

DC parameters

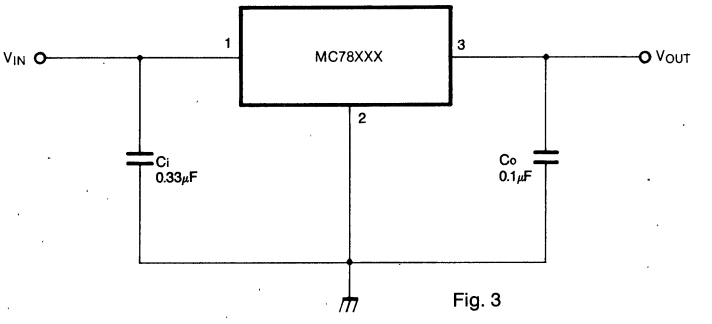


Fig. 3

Load regulation

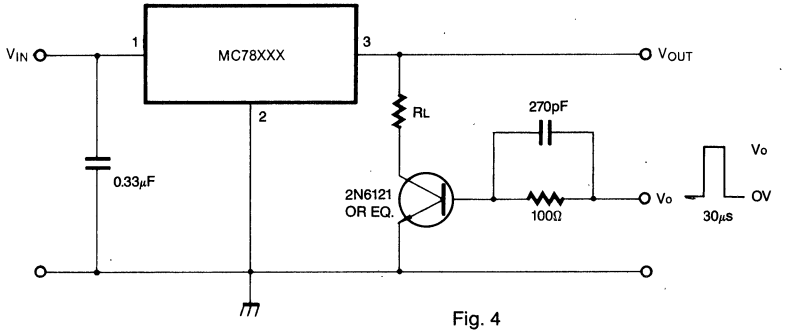


Fig. 4

Ripple rejection

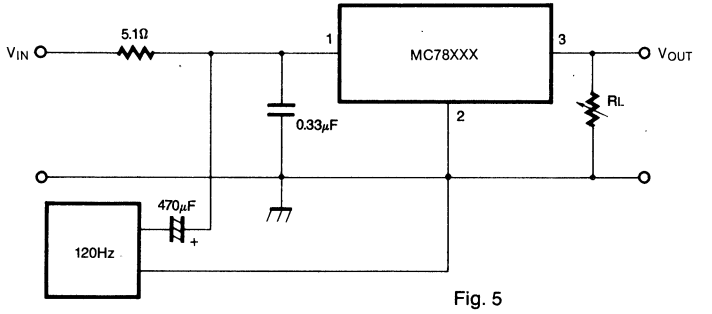


Fig. 5

APPLICATION CIRCUIT

Fixed output regulator

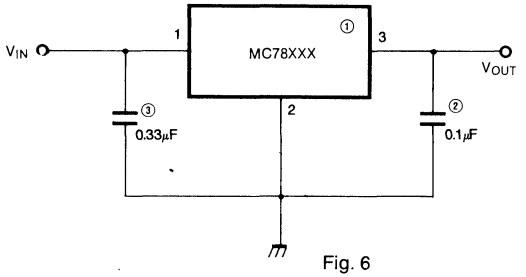


Fig. 6

Constant current regulator

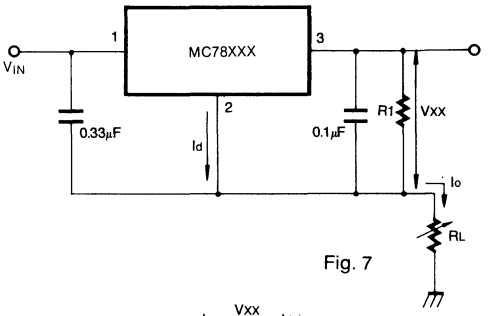


Fig. 7

$$I_o = \frac{V_{XX}}{R_1} + I_d$$

Notes:
(1) To specify an output voltage, substitute voltage value for "XX."
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Circuit for increasing output voltage

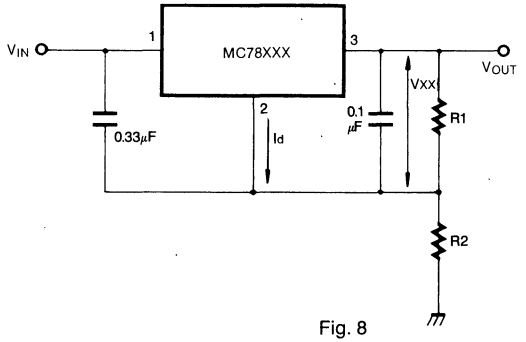


Fig. 8

$I_{R1} \geq 5I_d$
$V_O = V_{XX}(1+R_2/R_1)+I_d R_2$

Adjustable output regulator (7 to 30V)

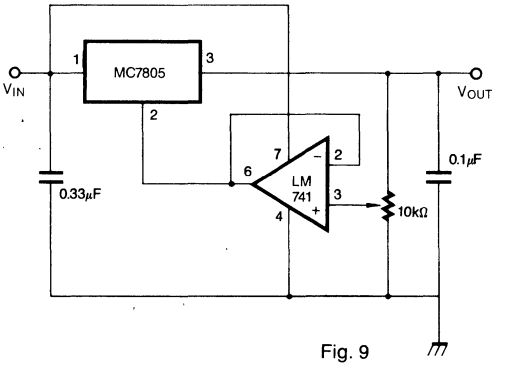


Fig. 9

APPLICATION CIRCUIT (continued)

0.5 to 10V regulator

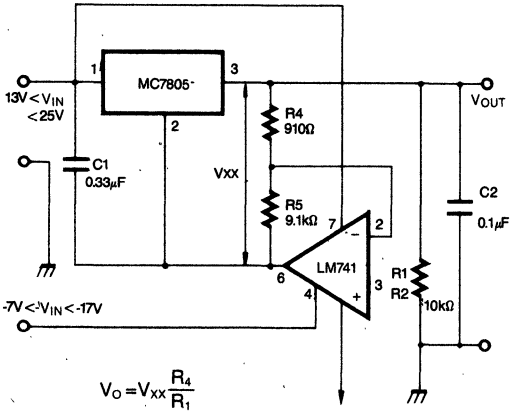


Fig. 10

High current voltage regulator

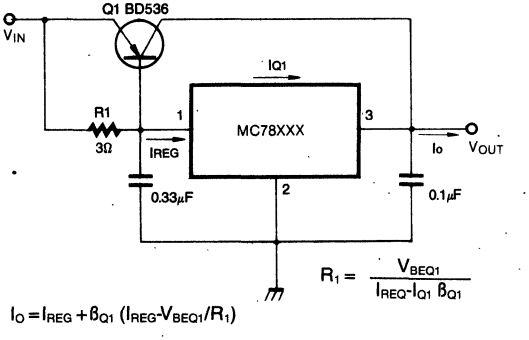


Fig. 11

High output current with short circuit protection

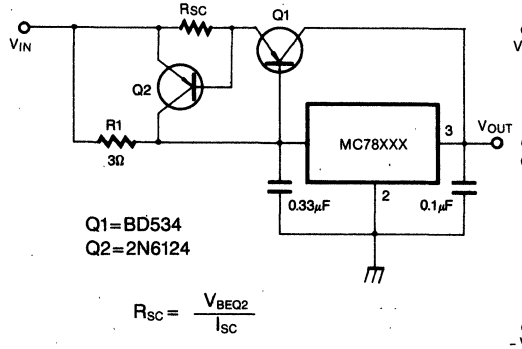


Fig. 12

Tracking voltage regulator

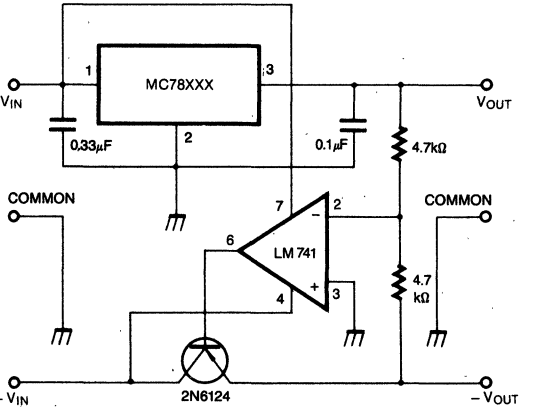


Fig. 13

Split power supply (± 15V — 1A)

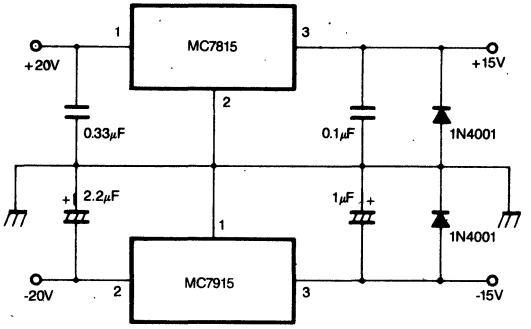


Fig. 14

Negative output voltage circuit

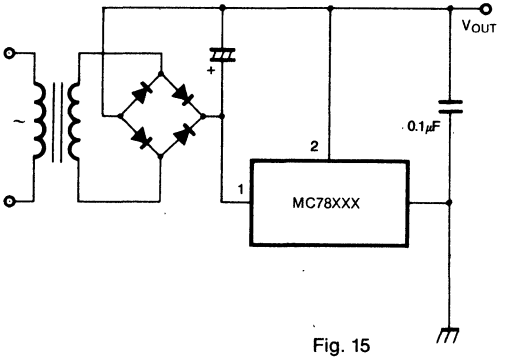


Fig. 15

Switching regulator

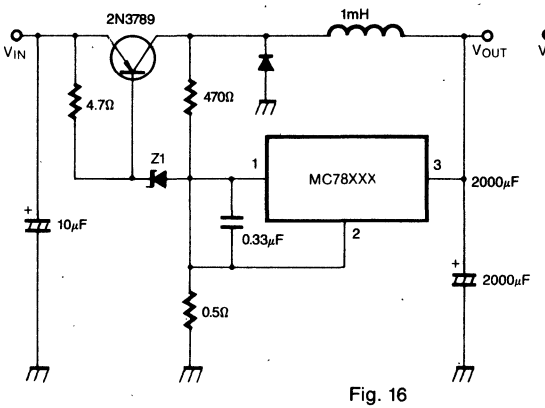
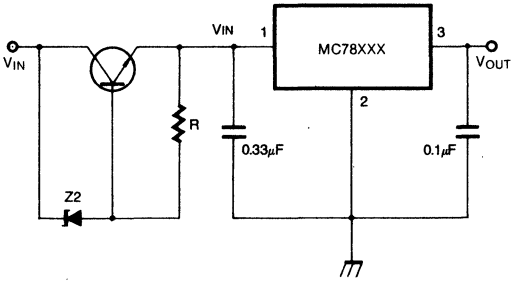


Fig. 16

High input voltage circuit



$V_{IN} = V_i - (V_Z + V_{BE})$

Fig. 17

APPLICATION CIRCUIT (continued)

High input voltage circuit

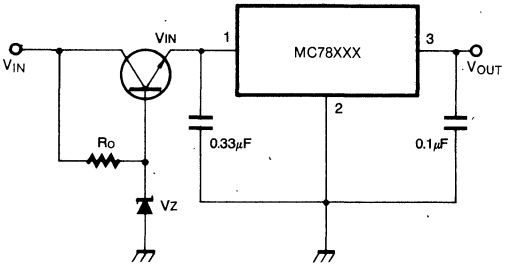


Fig. 18

$V_{IN} = V_Z - V_{BE}$

High output voltage regulator

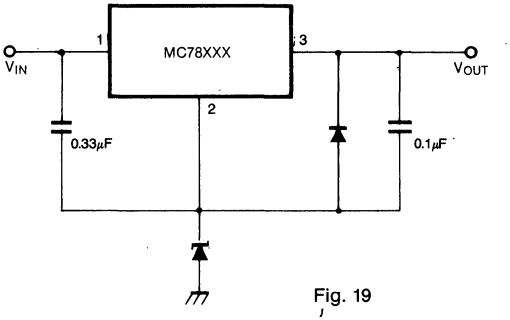
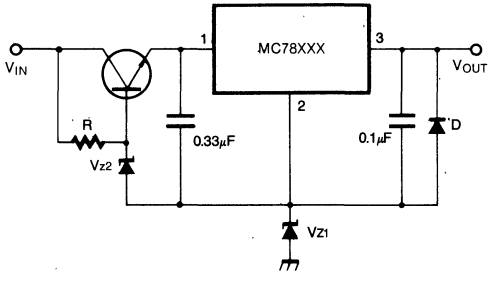


Fig. 19

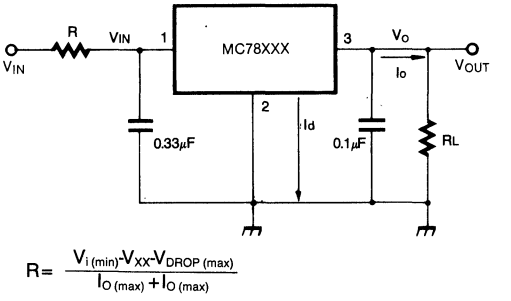
High input and output voltage



$V_O = V_{XX} + V_{Z1}$

Fig. 20

Reducing power dissipation with dropping resitor



$$R = \frac{V_{i\,(min)} - V_{XX} - V_{DROP\,(max)}}{I_{O\,(max)} + I_{O\,(max)}}$$

Fig. 21

APPLICATION CIRCUIT (continued)

Remote shuntdown

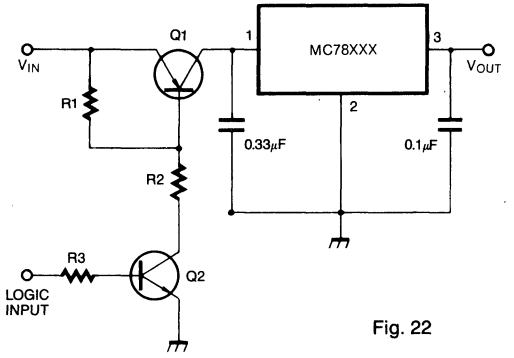


Fig. 22

Power AM modulator
(unity voltage gain, $I_O \leq 1A$)

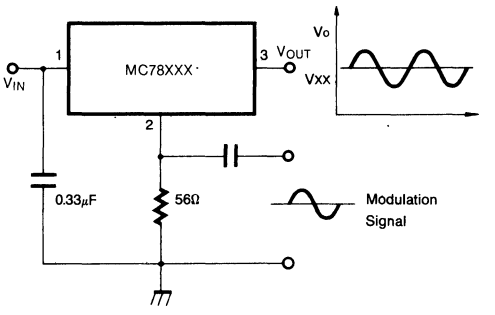


Fig. 23

Note: The circuit performs well up to 100 KHz.

Adjustable output voltage with temperature compensation

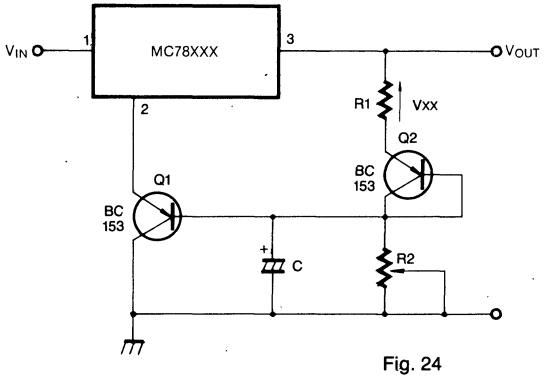


Fig. 24

Note: Q2 is connected as a diode in order to compensate the variation of the Q1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

4

Light controllers (V_O min=V_{XX} +V_{BE})

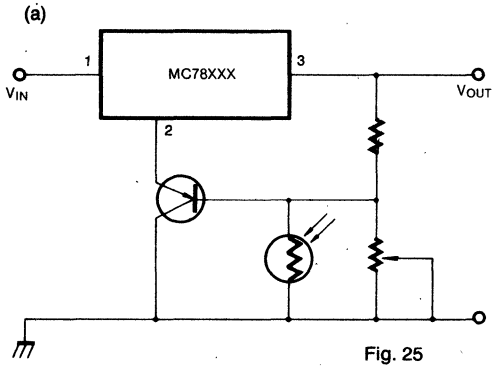
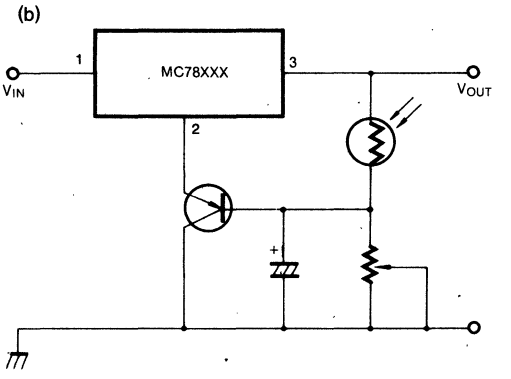


Fig. 25

V_O falls when the light goes up



V_O rises when the light goes up

Protection against input short-circuit with high capacitane loads

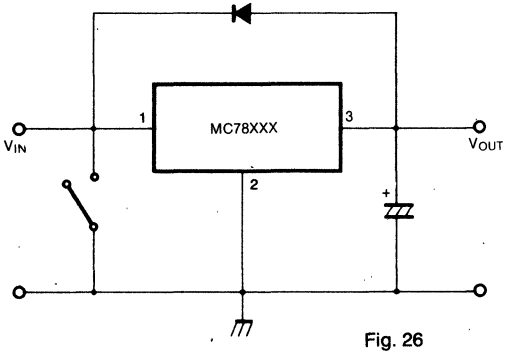


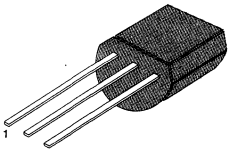
Fig. 26

Applications with high capacitance loads and an output voltage greater than 6 volts need an external diode (see fig. 26) to protect the device against input short circuit. In this case the input voltage falls rapidly while the output voltage decreases showly. The capacitance discharges by means of the Base-Emitter junction of the series pass transistor in the regulator. If the energy is sufficiently high, the transistor may be destroyed. The external diode by-passes the current from the IC to ground.

3-TERMINAL POSITIVE VOLTAGE REGULATORS

These regulators employ internal current-limiting and thermal-shutdown, making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 100mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators. The MC78LXXAC used as a Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnitude, along with lower quiescent current and lower noise.

TO-92



1: Output 2: GND 3: Input

FEATURES

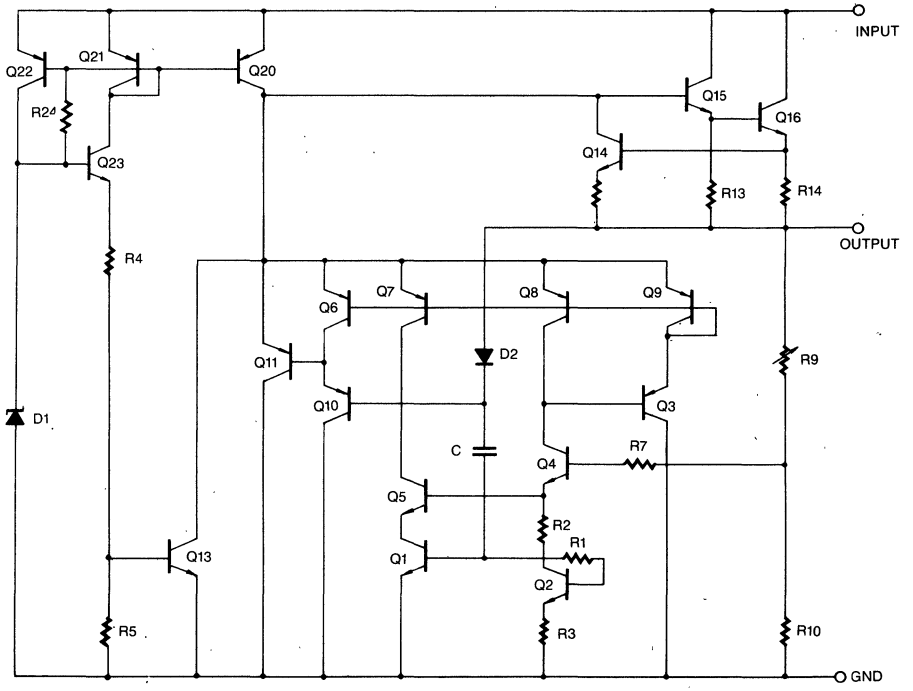
- **Output current up to 100mA.**
- **No external components.**
- **Internal thermal overload protection.**
- **Internal short circuit current limiting.**
- **Available in JEDEC TO-92.**
- **Output voltage of 2.6V, 5V, 6.2V, 8V, 8.2V, 9V, 12V, 15V, 18V, and 24V.**
- **Output voltage tolerances of ±5% over the temperature range.**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC78LXXACZ	TO-92	0°C ~ +125°C
**MC78LXXAIZ	TO-92	−40°C ~ +125°C

** Under Development

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

Characteristic	Symbol	Value	Unit
Input Voltage (2.6V-9V)	V_i	30	V
(12V-18V)		35	V
(24V)		40	V
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

MC78L26AC ELECTRICAL CHARACTERISTICS

V_{IN}=9V, I_{OUT}=40mA, 0°C≤Tj≤125°C, C_{IN}=0.33μF, C_{OUT}=0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		2.5	2.6	2.7	V
Line Regulation		ΔV_O	T_j=25°C	4.75V≤V_{IN}≤20V		40	100	mV
				5V≤V_{IN}≤20V	30	75		mV
Load Regulation		ΔV_O	T_j=25°C	1mA≤I_{OUT}≤100mA		10	50	mV
				1mA≤I_{OUT}≤40mA		4.0	25	mV
Output Voltage		V_O	4.75V≤V_{IN}≤20V	1mA≤I_{OUT}≤40mA	2.45		2.75	V
			4.75V≤V_{IN}≤V_{max} (Note 2)	1mA≤I_{OUT}≤70mA	2.45		2.75	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	5V≤V_{IN}≤20V				2.5	mA
	with load	ΔI_d	1mA≤I_{OUT}≤40mA				0.1	mA
Output Noise Voltage		$\overline{V_N}$	T_a=25°C, 10Hz≤f≤100KHz			30		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT}=5mA			−0.4		mV/°C
Ripple Rejection		RR	f=120Hz, 6V≤V_{IN}≤16V, Tj=25°C		43	51		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L05AC ELECTRICAL CHARACTERISTICS

V_{IN} =10V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j =25°C		4.8	5.0	5.2	V
Line Regulation		ΔV_O	T_j =25°C	7V ≤ V_{IN} ≤ 20V		55	150	mV
				8V ≤ V_{IN} ≤ 20V		45	100	mV
Load Regulation		ΔV_O	T_j =25°C	1mA ≤ I_{OUT} ≤ 100mA		11	60	mV
				1mA ≤ I_{OUT} ≤ 40mA		5.0	30	mV
Output Voltage		V_O	7V ≤ V_{IN} ≤ 20V	1mA ≤ I_{OUT} ≤ 40mA	4.75		5.25	V
			7V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	4.75		5.25	V
Quiescent Current		I_d	T_j =25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	8V ≤ V_{IN} ≤ 20V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a =25°C, 10Hz ≤ f ≤ 100KHz			40		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−0.65		mV/°C
Ripple Rejection		RR	f=120Hz, 8V ≤ V_{IN} ≤ 18V, Tj=25°C		41	49		dB
Dropout Voltage		V_D	T_j =25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j =25°C			140		mA

MC78L62AC ELECTRICAL CHARACTERISTICS

V_{IN} =12V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j =25°C		5.95	6.2	6.45	V
Line Regulation		ΔV_O	T_j =25°C	8.5V ≤ V_{IN} ≤ 20V		65	175	mV
				9V ≤ V_{IN} ≤ 20V		55	125	mV
Load Regulation		ΔV_O	T_j =25°C	1mA ≤ I_{OUT} ≤ 100mA		13	80	mV
				1mA ≤ I_{OUT} ≤ 40mA		6.0	40	mV
Output Voltage		V_O	8.5V ≤ V_{IN} ≤ 20V	1mA ≤ I_{OUT} ≤ 40mA	5.90		6.5	V
			8.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	5.90		6.5	V
Quiescent Current		I_d	T_j =25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	8V ≤ V_{IN} ≤ 20V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a =25°C, 10Hz ≤ f ≤ 100KHz			50		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−0.75		mV/°C
Ripple Rejection		RR	f=120Hz, 10V ≤ V_{IN} ≤ 20V, Tj=25°C		40	46		dB
Dropout Voltage		V_D	T_j =25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j =25°C			140		mA

MC78L08AC ELECTRICAL CHARACTERISTICS

V_{IN} =14V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		7.7	8.0	8.3	V
Line Regulation		ΔV_O	T_j=25°C	10.5 ≤ V_{IN} ≤ 23V		80	17.5	mV
				11V ≤ V_{IN} ≤ 23V		70	125	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		15	80	mV
				1mA ≤ I_{OUT} ≤ 40mA		8.0	40	mV
Output Voltage		V_O	10.5V ≤ V_{IN} ≤ 23V	1mA ≤ I_{OUT} ≤ 40mA	7.6		8.4	V
			10.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	7.6		8.4	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	11V ≤ V_{IN} ≤ 23V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			60		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} =5mA			−0.8		mV/°C
Ripple Rejection		RR	f=120Hz, 11V ≤ V_{IN} ≤ 21V, T_j = 25°C		39	45		dB
Dropout Voltage		V_D	Tj=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	Tj=25°C			140		mA

MC78L82AC ELECTRICAL CHARACTERISTICS

V_{IN} =14V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		7.87	8.2	8.53	V
Line Regulation		ΔV_O	T_j=25°C	11V ≤ V_{IN} ≤ 23V		80	175	mV
				12V ≤ V_{IN} ≤ 23V		70	125	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		15	80	mV
				1mA ≤ I_{OUT} ≤ 40mA		8.0	40	mV
Output Voltage		V_O	11V ≤ V_{IN} ≤ 23V	1mA ≤ I_{OUT} ≤ 40mA	7.8		8.6	V
			11V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	7.8		8.6	V
Quiescent Current		I_d	T_j=25°C			2.0	5.5	mA
Quiescent Current Change	with line	ΔI_d	12V ≤ V_{IN} ≤ 23V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			60		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−0.8		mV/°C
Ripple Rejection		RR	f=120Hz, 12V ≤ V_{IN} ≤ 22V, Tj=25°C		39	45		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L09AC ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, I_{OUT} = 40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j = 25°C		8.64	9.0	9.36	V
Line Regulation		ΔV_O	T_j = 25°C	11.5V ≤ V_{IN} ≤ 24V		90	200	mV
				13V ≤ V_{IN} ≤ 24V		100	150	mV
Load Regulation		ΔV_O	T_j = 25°C	1mA ≤ I_{OUT} ≤ 100mA		20	90	mV
				1mA ≤ I_{OUT} ≤ 40mA		10	45	mV
Output Voltage		V_O	11.5V ≤ V_{IN} ≤ 24V	1mA ≤ I_{OUT} ≤ 40mA	8.55		9.45	V
			11.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	8.55		9.45	V
Quiescent Current		I_d	T_j = 25°C			2.1	6.0	mA
Quiescent Current Change	with line	ΔI_d	13V ≤ V_{IN} ≤ 24V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a = 25°C, 10Hz ≤ f ≤ 100KHz			70		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−0.9		mV/°C
Ripple Rejection		RR	f = 120Hz, 12V ≤ V_{IN} ≤ 22V, T_j = 25°C		38	44		dB
Dropout Voltage		V_D	T_j = 25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j = 25°C			140		mA

MC78L12AC ELECTRICAL CHARACTERISTICS

V_{IN} = 19V, I_{OUT} = 40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j = 25°C		11.5	12	12.5	V
Line Regulation		ΔV_O	T_j = 25°C	14.5V ≤ V_{IN} ≤ 27V		120	250	mV
				16V ≤ V_{IN} ≤ 27V		100	200	mV
Load Regulation		ΔV_O	T_j = 25°C	1mA ≤ I_{OUT} ≤ 100mA		20	100	mV
				1mA ≤ I_{OUT} ≤ 40mA		10	50	mV
Output Voltage		V_O	14.5V ≤ V_{IN} ≤ 27V	1mA ≤ I_{OUT} ≤ 40mA	11.4		12.6	V
			14.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	11.4		12.6	V
Quiescent Current		I_d	T_j = 25°C			2.1	6.0	mA
Quiescent Current Change	with line	ΔI_d	16V ≤ V_{IN} ≤ 27V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a = 25°C, 10Hz ≤ f ≤ 100KHz			80		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−1.0		mV/°C
Ripple Rejection		RR	f = 120Hz, 15V ≤ V_{IN} ≤ 25V, Tj = 25°C		37	42		dB
Dropout Voltage		V_D	T_j = 25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j = 25°C			140		mA

MC78L15AC ELECTRICAL CHARACTERISTICS

V_{IN} =23V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		14.4	15	15.6	V
Line Regulation		ΔV_O	T_j=25°C	17.5V ≤ V_{IN} ≤ 30V		130	300	mV
				20V ≤ V_{IN} ≤ 30V		110	250	nV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		25	150	mV
				1mA ≤ I_{OUT} ≤ 40mA		12	75	mV
Output Voltage		V_O	17.5V ≤ V_{IN} ≤ 30V	1mA ≤ I_{OUT} ≤ 40mA	14.25		15.75	V
			17.5V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	14.25		15.75	V
Quiescent Current		I_d	T_j=25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_d	20V ≤ V_{IN} ≤ 30V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			90		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			– 1.3		mV/°C
Ripple Rejection		RR	f=120Hz, 18.5V ≤ V_{IN} ≤ 28.5V, Tj=25°C		34	39		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L18AC ELECTRICAL CHARACTERISTICS

V_{IN} =27V, I_{OUT} =40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} =0.33μF, C_{OUT} =0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		17.3	18	18.7	V
Line Regulation		ΔV_O	T_j=25°C	21V ≤ V_{IN} ≤ 33V		145	300	mV
				22V ≤ V_{IN} ≤ 33V		135	250	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		30	170	mV
				1mA ≤ I_{OUT} ≤ 40mA		15	85	mV
Output Voltage		V_O	21V ≤ V_{IN} ≤ 33V	1mA ≤ I_{OUT} ≤ 40mA	17.1		18.9	V
			21V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	17.1		18.9	V
Quiescent Current		I_d	T_j=25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_d	21V ≤ V_{IN} ≤ 33V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			150		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			– 1.8		mV/°C
Ripple Rejection		RR	f=120Hz, 23V ≤ V_{IN} ≤ 33V, Tj=25°C		34	48		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

MC78L24AC ELECTRICAL CHARACTERISTICS

V_{IN} = 33V, I_{OUT} = 40mA, 0°C ≤ Tj ≤ 125°C, C_{IN} = 0.33μF, C_{OUT} = 0.1μF, unless otherwise specified. (Note 1)

Characteristic		Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage		V_O	T_j=25°C		23	24	25	V
Line Regulation		ΔV_O	T_j=25°C	27V ≤ V_{IN} ≤ 38V		160	300	mV
				28V ≤ V_{IN} ≤ 38V		150	250	mV
Load Regulation		ΔV_O	T_j=25°C	1mA ≤ I_{OUT} ≤ 100mA		40	200	mV
				1mA ≤ I_{OUT} ≤ 40mA		20	100	mV
Output Voltage		V_O	27V ≤ V_{IN} ≤ 38V	1mA ≤ I_{OUT} ≤ 40mA	22.8		25.2	V
			27V ≤ V_{IN} ≤ V_{max} (Note 2)	1mA ≤ I_{OUT} ≤ 70mA	22.8		25.2	V
Quiescent Current		I_d	T_j=25°C			2.2	6.0	mA
Quiescent Current Change	with line	ΔI_d	28V ≤ V_{IN} ≤ 38V				1.5	mA
	with load	ΔI_d	1mA ≤ I_{OUT} ≤ 40mA				0.1	mA
Output Noise Voltage		V_N	T_a=25°C, 10Hz ≤ f ≤ 100KHz			200		μV
Temperature Coefficient of V_{OUT}		$\frac{\Delta V_O}{\Delta T}$	I_{OUT} = 5mA			−2.0		mV/°C
Ripple Rejection		RR	f=120Hz, 28V ≤ V_{IN} ≤ 38V, Tj=25°C		34	45		dB
Dropout Voltage		V_D	T_j=25°C			1.7		V
Peak Output/Short-Circuit Current		I_{SC}	T_j=25°C			140		mA

Notes

1. The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The date above represent pulse test conditions with junction temperatures as indicated at the initiation of tests.
2. Power dissipation ≤ 0.75W.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 QUIESCENT CURRENT vs A FUNCTION OF INPUT VOLTAGE

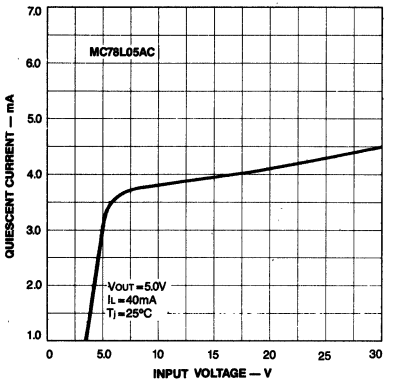


Fig. 2 DROPOUT VOLTAGE vs A FUNCTION O FJUNCTION TEMPERATURE

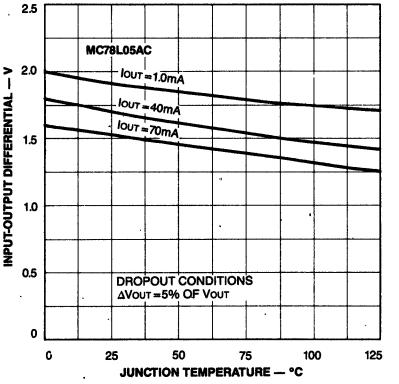


Fig. 3 QUIESCENT CURRENT vs A FUNCTION OF TEMPERATURE

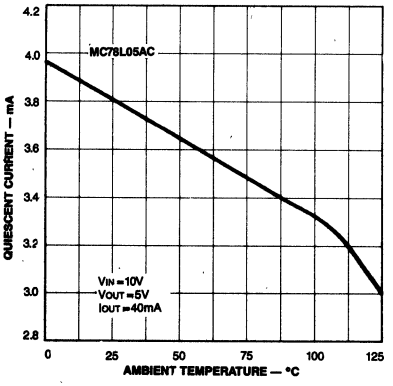


Fig. 4 · DROPOUT CHARACTERISTICS

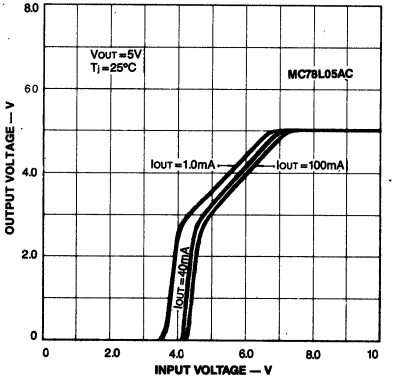


Fig. 5 RIPPLE REJECTION vs A FUNCTION OF FREQUENCY

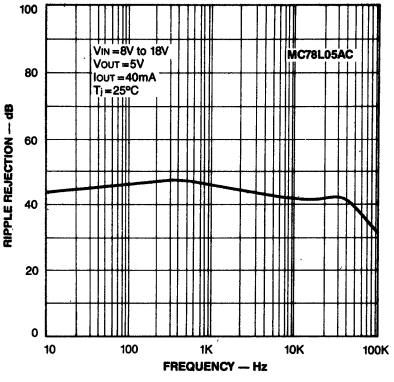


Fig. 6 LINE TRANSIENT RESPONSE

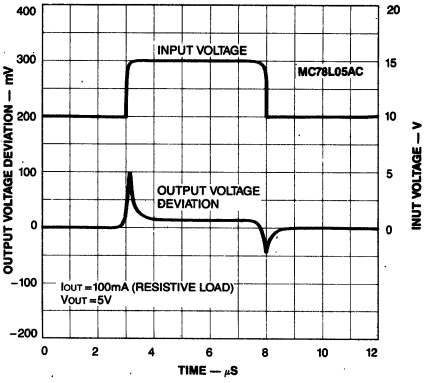


Fig. 7 LOAD TRANSIENT RESPONSE

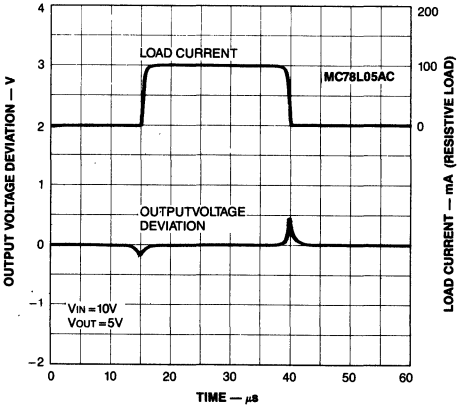
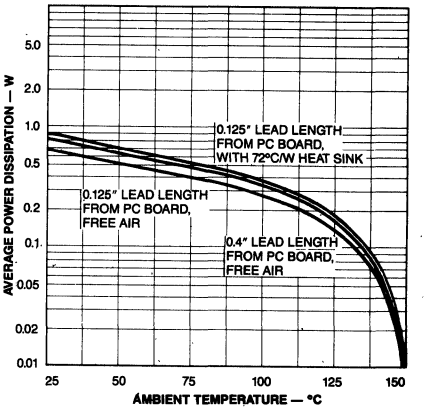


Fig. 8 TO-92 WORST CASE POWER DISSIPATION vs AMBIENT TEMPERATURE



4

APPLICATION INFORMATION

The MC78L series regulators have thermal overload protection from excessive power, internal short-circuit protection which limits each circuit's maximum current, and output transistor safe-area protection for reducing the output current as the voltage across each pass transistor is increased.

Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature (125°C) in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, the following thermal resistance values should be used:

Thermal Considerations

The TO-92 molded package manufactured by SST is capable of unusually high power dissipation due to the lead frame design. However, its thermal capabilities are generally overlooked because of a lack of understanding of the thermal paths from the semiconductor junction to ambient temperature. While thermal resistance is normally specified for the device mounted 1cm above an infinite heat sink, very little has been mentioned of the options available to improve on the conservatively rated thermal capability.

An explanation of the thermal paths of the TO-92 will allow the designer to determine the thermal stress he is applying in any given application.

The TO-92 Package

The TO-92 package thermal paths are complex. In addition to the path through the molding compound to ambient temperature, there is another path through the pins, in parallel with the case path, to ambient temperature, as shown in Figure 1.

The total thermal resistance in this model is then:

$$\theta_{JA} = \frac{(\theta_{JC} + \theta_{CA})(\theta_{JL} + \theta_{LA})}{\theta_{JC} + \theta_{CA} + \theta_{JL} + \theta_{LA}}$$

Where: θ_{JC} = thermal resistance of the case between the regulator die and a point on the case directly above the die location.
θ_{CA} = thermal resistance between the case and air at ambient temperature.
θ_{JL} = thermal resistance from transistor die through the collector lead to a point 1/16 inch below the regulator case.
θ_{LA} = total thermal resistance of the collector-base-emitter pins to ambient temperature.
θ_{JA} = junction to ambient thermal resistance.

TO-92 Thermal Equivalent Circuit

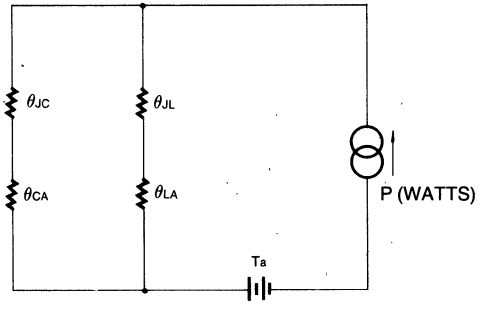


Fig. 9

TO-92 Thermal Equivalent Circuit (PIN at Other Than Ambient Temperature)

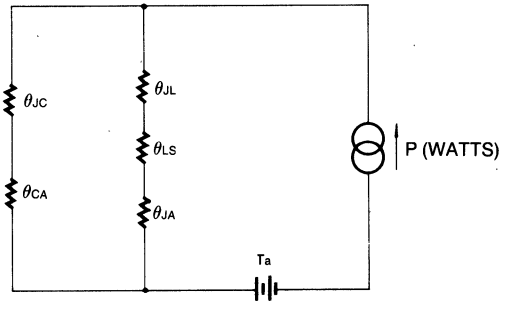


Fig. 10

Methods of Heat Sinking

With two external thermal resistances in each leg of a parallel network available to the circuit designer as variables, he can choose the method of heat sinking most applicable to his particular situation. To demonstrate, consider the effect of placing a small 72°C/W flag type heat sink, such as the Staver F1-7D-2, on the 78LXX molded case. The heat sink effectively replaces the θ_{CA} (Figure 2) and the new thermal resistance, $\theta_{JA} = 145°C/W$ (assuming, 0.125 inch led length).

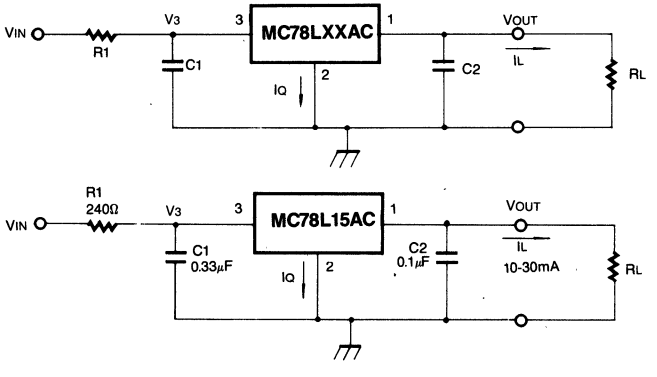
The net change of 15°C/W increases the allowable power dissipation to 0.86W with an inserted cost of 1-2 cents. A still further decrease in θ_{JA} could be achieved by using a heat sink rated at 46°C/W, such as the Staver FS-7A. Also, if the case sinking does not provide an adequate reduction in total θ_{JA}, the other external thermal resistance, θ_{LA}, may be reduced by shortening the lead length from package base to mounting medium. However, one point must be kept in mind. The lead thermal path includes a thermal resistance, θ_{SA}, from the pins at the mounting points to ambient, that is, the mounting medium, θ_{LA} is then equal to $\theta_{LS} + \theta_{SA}$. The new model is shown in Figure 2.

In the case of a socket, θ_{SA} could be as high as 270°C/W, thus causing a net increase in θ_{JA} and a consequent decrease in the maximum dissipation capability. Shortening the lead length may return the net θ_{JA} to the original value, but pin sinking would not be accomplished.

In those cases where the regulator is inserted into a copper clad printed circuit board, it is advantageous to have a maximum area of copper at the entry points of the pins. While it would be desirable to rigorously define the effect of PC board copper, the real world variables are too great to allow anything more than a few general observations.

The best analogy for PC board copper is to compare it with parallel resistors. Beyond some point, additional resistors are not significantly effective; beyond some point, additional copper area is not effective.

High Dissipation Applications



When it is necessary to operate a MC78LXXAC regulator with a large input-output differential voltage, the addition of series resistor R1 will extend the output current range of the device by sharing the total power dissipation between R1 and the regulator.

$$R1 = \frac{V_{IN\,(MIN)} - V_{OUT} - 2.0V}{I_{L\,(MAX)} + I_Q}$$

Where I_o is the regulator quiescent current.

Regulator power dissipation at maximum input voltage and maximum load current is now

$$P_{D\,(MAX)} = (V_3 - V_{OUT})\, I_{L\,(MAX)} + V_3 I_Q$$

where $V_3 = V_{IN\,(MAX)} - (I_{C\,(MAX)} + I_Q)\, R_1$

The presence of R1 will affect load regulation according to the equation:

load regulation (at constant V_{IN})
=load regulation (at constant V_3)
+(line regulation, mV per V)
×(R1)×(ΔIL).

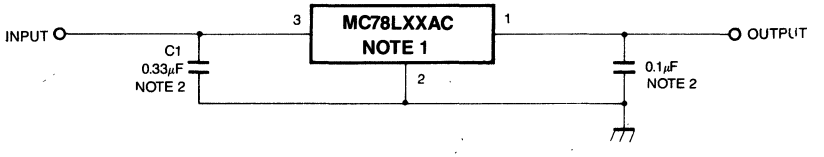
As an example, consider a 15V regulator with a supply voltage of 30±5V, required to supply a maximum load current of 30mA. I_Q is 4.3mA, and minimum load current is to be 10mA.

$$R_1 = \frac{25 - 15 - 2}{30 + 4.3} = \frac{34.3}{8} = 240\Omega$$

$V_3 = 35 - (30 + 4.3) \times 0.24 = 35.82 = 26.8V$
$P_{D\,(MAX)} = (26.8 - 15)\, 30 + 26.8\, (4.3)$
$= 354 + 115$
=470mW, which permit operation up to 70°C
in most applications.

Line regulation of this circuit is typically 110mV for an input range of 25 ~ 35V at a constant load current; i.e. 11mV/V
Load regulation=constant V_1 load regulation (typically 10mV, 10 ~ 30mA I_L)
+(11mV/V×0.24×20mA (typically 53mV)
=63mV for a load current change of 20mA at a constant V_{IN} of 30V.

Typical Application



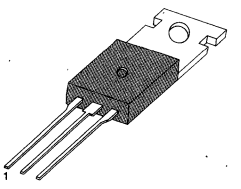
Notes

1. To specify an output voltage, substitute voltage value for "xx".
2. Bypass Capacitors are recommended for optimum stability and transient response and should be locate as close as possible to the regulator.

3-TERMINAL 0.5A POSITIVE VOLTAGE REGULATOR

The MC78MXXC series of three-terminal positive regulators is available TO-220 package with several fixed output voltages, making it useful in a wide range of applications. These reglators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 0.5A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



1: Input 2: GND 3: Output

FEATURES

- **Output Current up to 0.5A**
- **Output Voltages of 5; 6; 8; 10; 12; 15; 18; 20; 24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC78MXXIT	TO-220	– 40 ~ + 125°C
MC78MXXCT	TO-220	0°C ~ + 125°C

BLOCK DIAGRAM

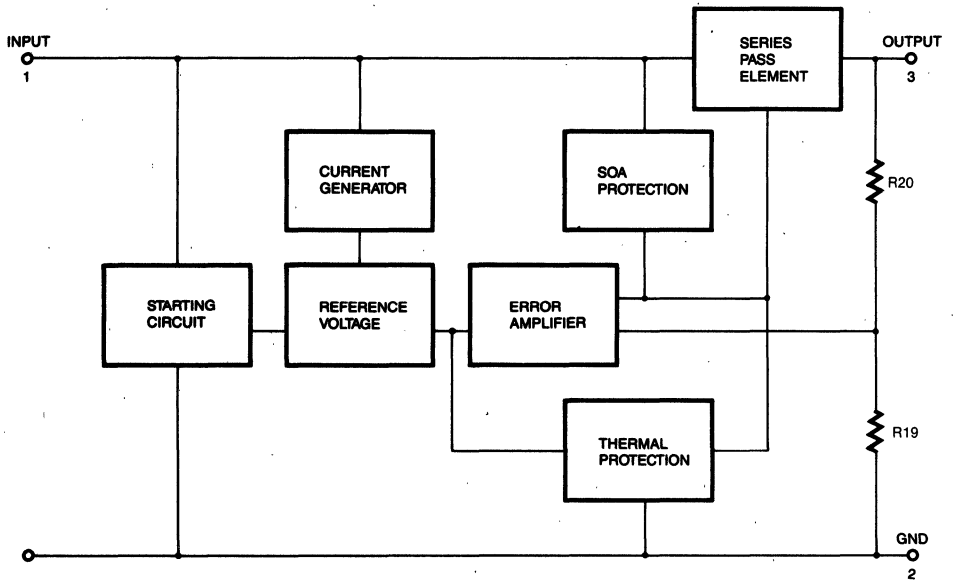


Fig. 1

SCHEMATIC DIAGRAM

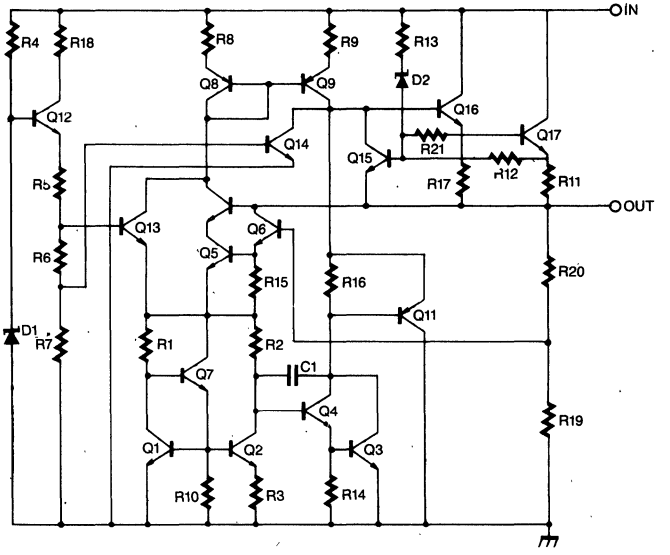


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o = 5V to 18V)	V_i	35	V
(for V_o = 24V)	V_i	40	V
Thermal Resistance Junction-Cases	Θ_{JC}	5	°C/W
Thermal Resistance Junction-Air	Θ_{JA}	65	°C/W
Operating Temperature Range MC78XXI	T_{opr}	−40 ~ +125	°C
MC78XXC/AC		0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS MC78M05C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 10V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		4.8	5	5.2	V
		$I_o = 5$ to $350mA$ $V_i = 7$ to $20V$		4.75	5	5.25	
Line Regulation	$\triangle V_o$	$I_o = 200mA$	$V_i = 7$ to $25V$			100	mV
			$V_i = 8$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$				100	mV
		$I_o = 5mA$ to $200mA$				50	
Quiescent Current	I_d					6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 8$ to $25V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			-0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			40		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 8$ to $18V$		62			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			300		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M06C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 11V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	5.75	6	6.25	V
		$I_o = 5$ to $350mA$ $V_i = 8$ to $21V$	5.7	6	6.3	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $V_i = 8$ to $25V$			100	mV
		$I_o = 200mA$, $V_i = 9$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$			120	mV
		$I_o = 5mA$ to $200mA$			60	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 9$ to $25V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		−0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		45		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 9$ to $19V$	59			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		270		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

4

ELECTRICAL CHARACTERISTICS MC78M08C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 14V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	7.7	8	8.3	V
		$I_o = 5$ to $350mA$ $V_i = 10.5$ to $23V$	7.6	8	8.4	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $V_i = 10.5$ to $25V$			100	mV
		$I_o = 200mA$, $V_i = 11$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$			160	mV
		$I_o = 5mA$ to $200mA$			80	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 10.5$ to $25V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		-0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		52		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 11.5$ to $21.5V$	56			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		250		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M10C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 17V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		9.6	10	10.4	V
		$I_o = 5$ to $350mA$ $V_i = 12.5$ to $25V$		9.5	10	10.5	
Line Regulation	$\triangle V_o$	$I_o = 200mA$	$V_i = 12.5$ to $25V$			100	mV
			$V_i = 13$ to $25V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$				200	mV
		$I_o = 5mA$ to $200mA$				100	
Quiescent Current	I_d	$T_j = 25°C$				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 12.5$ to $25V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			-0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			65		μV
Ripple Rejection	RR	$f = 120Hz$, $I_o = 300mA$ $V_i = 13$ to $23V$		55			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			250		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

4

ELECTRICAL CHARACTERISTICS MC78M12C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 19V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		11.5	12	12.5	V
		$I_o = 5$ to $350mA$ $V_i = 14.5$ to $27V$		11.4	12	12.6	
Line Regulation	$\triangle V_o$	$I_o = 200mA$	$V_i = 14.5$ to $30V$			100	mV
			$V_i = 16$ to $30V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$				240	mV
		$I_o = 5mA$ to $200mA$				120	
Quiescent Current	I_d	$T_j = 25°C$				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$				0.5	mA
		$I_o = 200mA$ $V_i = 14.5$ to $30V$				0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$			−0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$			75		μV
Ripple Rejection	RR	$f = 120Hz$, $I_o = 300mA$ $V_i = 15$ to $25V$		55			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$			2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$			240		mA
Peak Current	I_{peak}	$T_j = 25°C$			700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M15C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 23V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	14.4	15	15.6	V
		$I_o = 5$ to $350mA$, $V_i = 17.5$ to $30V$	14.25	15	15.75	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $V_i = 17.5$ to $30V$			100	mV
		$I_o = 200mA$, $V_i = 20$ to $30V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$			300	mV
		$I_o = 5mA$ to $200mA$			150	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$, $V_i = 17.5$ to $30V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$, $T_j = 0$ to $125°C$		-1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		90		μV
Ripple Rejection	RR	$f = 120Hz$, $I_o = 300mA$, $V_i = 18.5$ to $28.5V$	54			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		240		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M18C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 26V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	17.3	18	18.7	V
		$I_o = 5$ to $350mA$ $V_i = 20.5$ to $33V$	17.1	18	18.9	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $V_i = 21$ to $33V$			100	mV
		$I_o = 200mA$, $V_i = 24$ to $33V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$			360	mV
		$I_o = 5mA$ to $200mA$			180	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 21$ to $33V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		−1.1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		100		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 22$ to $32V$	53			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		240		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

ELECTRICAL CHARACTERISTICS MC78M20C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 29V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	19.2	20	20.8	V
		$I_o = 5$ to $350mA$, $V_i = 23$ to $35V$	19	20	21	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $V_i = 23$ to $35V$			100	mV
		$I_o = 200mA$, $V_i = 24$ to $35V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$			400	mV
		$I_o = 5mA$ to $200mA$			200	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$, $V_i = 23$ to $35V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$, $T_j = 0$ to $125°C$		-1.1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		110		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$, $V_i = 24$ to $34V$	53			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$, $V_i = 35V$		240		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

4

ELECTRICAL CHARACTERISTICS MC78M24C

(Refer to the test circuits, $T_{min} \leq T_j \leq 125°C$, $I_o = 350mA$, $V_i = 33V$, unless otherwise specified, $C_i = 0.33\mu F$, $C_o = 0.1\mu F$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	
Output Voltage	V_o	$T_j = 25°C$	23	24	25	V
		$I_o = 5$ to $350mA$ $V_i = 27$ to $38V$	22.8	24	25.2	
Line Regulation	$\triangle V_o$	$I_o = 200mA$, $V_i = 27$ to $38V$			100	mV
		$I_o = 200mA$, $V_i = 28$ to $38V$			50	
Load Regulation	$\triangle V_o$	$I_o = 5mA$ to $0.5A$			480	mV
		$I_o = 5mA$ to $200mA$			240	
Quiescent Current	I_d				6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $350mA$			0.5	mA
		$I_o = 200mA$ $V_i = 27$ to $38V$			0.8	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$ $T_j = 0$ to $125°C$		−1.2		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$		170		μV
Ripple Rejection	RR	$f = 120Hz$ $I_o = 300mA$ $V_i = 28$ to $38V$	50			dB
Dropout Voltage	V_D	$T_j = 25°C$, $I_o = 500mA$		2		V
Short Circuit Current	I_{sc}	$V_i = 35V$		240		mA
Peak Current	I_{peak}	$T_j = 25°C$		700		mA

* T_{min}
MC78MXXI: $T_{min} = -40°C$
MC78MXXC: $T_{min} = 0°C$

APPLICATION CIRCUIT

Fixed output regulator

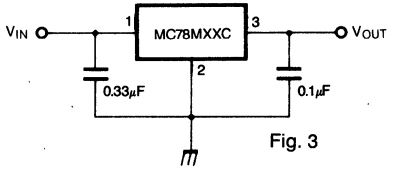


Fig. 3

Notes:
(1) To specify an output voltage, substitute voltage value for "XX".
(2) Although no output capacitor is needed for stability, it does improve transient response.
(3) Required if regulator is located an appreciable distance from power supply filter.

Constant current regulator

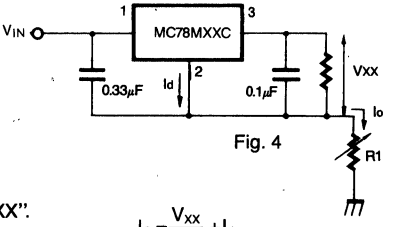


Fig. 4

$$I_O = \frac{V_{XX}}{R_1} + I_d$$

Circuit for increasing output voltage

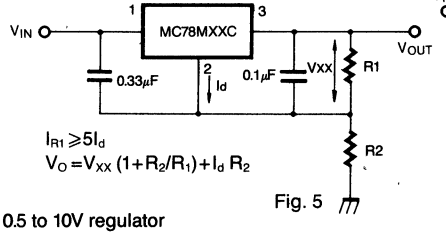


Fig. 5

Adjustable output regulator (7 to 30V)

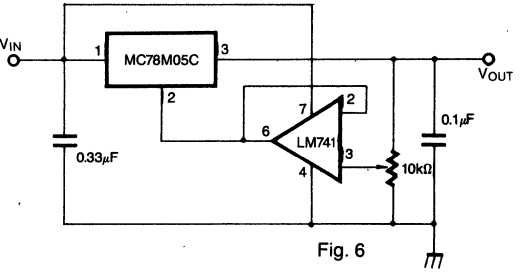


Fig. 6

0.5 to 10V regulator

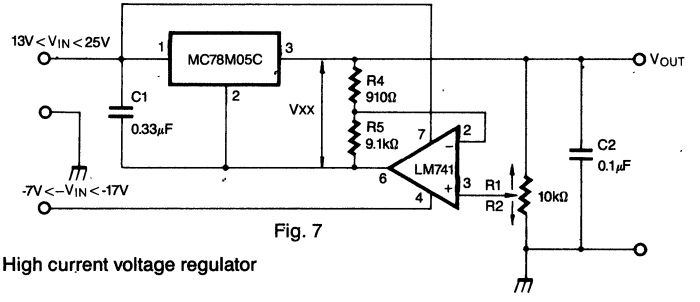


Fig. 7

$$V_O = V_{XX}\frac{R_4}{R_1}$$

High current voltage regulator

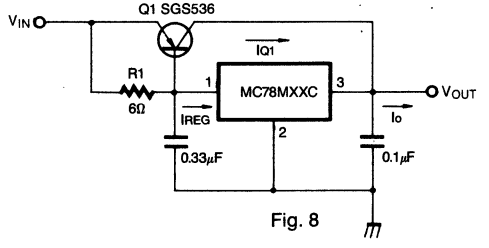


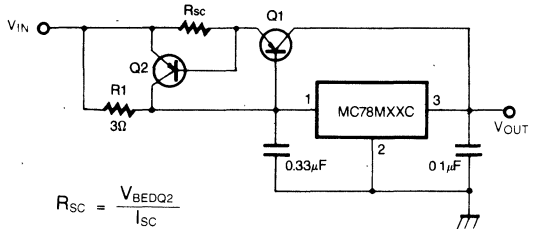
Fig. 8

$$R_1 = \frac{V_{BEQ1}}{I_{REQ} - \frac{I_{Q1}}{\beta_{Q1}}}$$

$$I_O = I_{REG} + \beta_{Q1}\left(I_{REG} - \frac{V_{BEQ1}}{R_{R1}}\right)$$

APPLICATION CIRCUIT (continued)

High output current with short circuit protection



$$R_{SC} = \frac{V_{BEDQ2}}{I_{SC}}$$

Fig. 9

Tracking voltage regulator

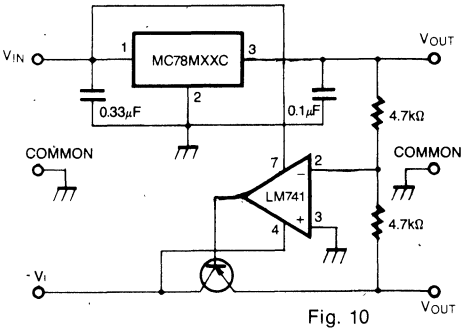
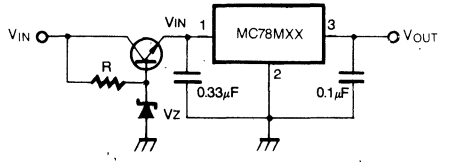


Fig. 10

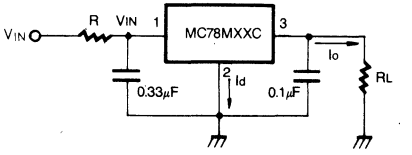
High input voltage circuit



$$V_{IN} = V_Z - V_{BE}$$

Fig. 11

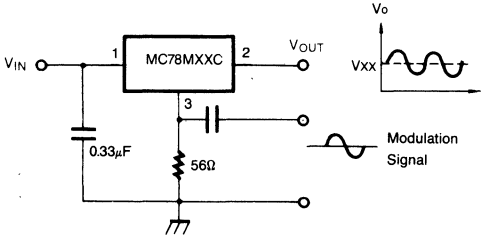
Reducing power dissipation with dropping resistor



$$R = \frac{V_I(\min) - V_{XX} - V_{DROP}(\max)}{I_O(\max) + I_d(\max)}$$

Fig. 12

Power AM modultor (unity voltage gain, $I_o \leqslant 0.5$)



Note: The circuit performs well up to 100 KHz.

Fig. 13

Adjustable output voltage with temperature compensation

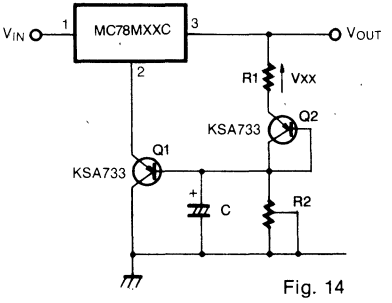


Fig. 14

Note: Q2 is connected as a diode in order to compensate the variation of the Q1 V_{BE} with the temperature. C allows a slow rise-time of the V_O

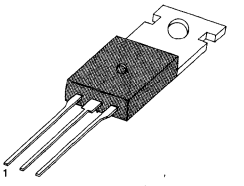
$$V_O = V_{XX}\left(1 + \frac{R_2}{R_1}\right) + V_{BE}$$

3-TERMINAL NEGATIVE VOLTAGE REGULATOR

The MC79XXC series of three-terminal negative regulators is available in TO-220 package and with several output voltages. They can provides local on-card regulation, eliminating the distribution problems associated with single point regulation; furthermore, having the same voltage options as the MC78XXC positive standard series, they are particularly suited for split power supplies.

If adequate heat sinking is provided, the MC79XXC series can deliver an output current in excess of 1.5A. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

TO-220



1: GND 2: Input 3: Output

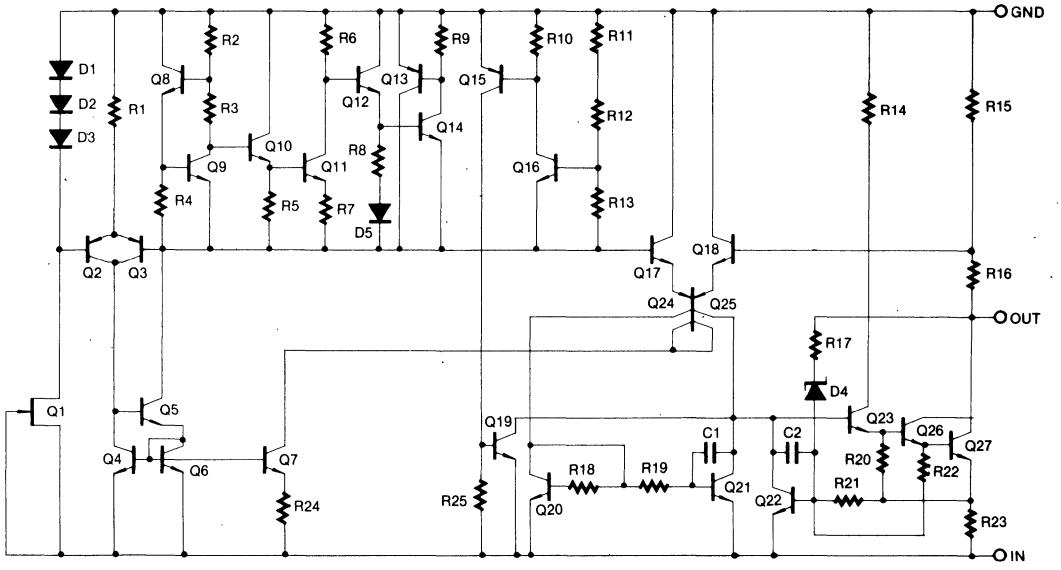
FEATURES

- **Output Current up to 1.5A**
- **Ouput Voltages of −2V, −5V, −6V, −8V, −12V, −15V, −18V, −24V**
- **Thermal Overload Protection**
- **Short Circuit Protection**
- **Output Transistor SOA Protection**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC79XXCT	TO-220	0 ~ 125°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o= −2 to −18V)	V_i	−35	V
(for V_o = −24V)	V_i	−40	V
Thermal Resistance Junction-Case	Θ_{JC}	5	°C/W
Junction-Air	Θ_{JA}	65	°C/W
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +125	°C

ELECTRICAL CHARACTERISTICS MC7902C

(C_i = 2.2μF, C_o = 1μF, T_j = 0 to 125°C, I_o = 500mA, V_i = 10V, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	T_j = 25°C		−1.92	−2	−2.08	V
		I_o = 5mA to 1A $P_D \leq$ 15W V_i = −7 to −20V		−1.9	−2	−2.1	
Line Regulation	$\triangle V_o$	T_j = 25°C	V_i = −7 to −25V			40	mV
			V_i = −8 to −12V			20	
Load Regulation	$\triangle V_o$	T_j = 25°C I_o = 5mA to 1.5A			70	120	mV
		T_j = 25°C I_o = 250 to 750mA			20	60	
Quiescent Current	I_d	T_j = 25°C			3	6	mA
Quiescent Current Change	$\triangle I_d$	I_o = 5mA to 1A				0.5	mA
		V_i = −7 to −25V				1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	I_o = 5mA			−0.4		mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz T_j = 25°C			40		μV
Ripple Rejection	RR	f=120Hz $\triangle V_i$ = 10V		54	60		dB
Dropout Voltage	V_D	T_j = 25°C I_o = 1A			3.5		V
Short Circuit Current	I_{sc}	T_j = 25°C			2.2		A
Peak Current	I_{peak}	T_j = 25°C			2.5		A

ELECTRICAL CHARACTERISTICS MC7905C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 10V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−4.8	−5	−5.2	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -8$ to $-20V$	−4.75	−5	−5.25	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -7$ to $-25V$			100	mV
		$T_j = 25°C$, $V_i = -8$ to $-12V$			50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			100	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$			50	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -8$ to $-25V$			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.4		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		100		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		2.1		A
Peak Current	I_{peak}	$T_j = 25°C$		2.5		A

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ELECTRICAL CHARACTERISTICS MC7906C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 11V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−5.75	−6	−6.25	V
		$I_o = 5mA$ to 1A, $P_o \leq 15W$ $V_i = -9$ to $-21V$	−5.7	−6	−6.3	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -8$ to $-25V$			120	mV
		$T_j = 25°C$, $V_i = -9$ to $-13V$			60	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to 1.5A			120	mV
		$T_j = 25°C$ $I_o = 250$ to 750mA			60	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to 1A			0.5	mA
		$V_i = -9$ to $-25V$			1.3	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.5		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		130		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		1.8		A
Peak Current	I_{peak}	$T_j = 25°C$		2.5		A

ELECTRICAL CHARACTERISTICS MC7908C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 14V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−7.7	−8	−8.3	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -11.5$ to $-23V$	−7.6	−8	−8.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -10.5$ to $-25V$			160	mV
		$T_j = 25°C$, $V_i = -11$ to $-17V$			80	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			160	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$			80	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -11.5$ to $-25V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.6		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		175		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		1.5		A
Peak Current	I_{peak}	$T_j = 25°C$		2.5		A

ELECTRICAL CHARACTERISTICS MC7912C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 18V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−11.5	−12	−12.5	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -15.5$ to $-27V$	−11.4	−12	−12.6	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -14.5$ to $-30V$			240	mV
		$T_j = 25°C$, $V_i = -16$ to $-22V$			120	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			240	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$			120	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -15$ to $-30V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		200		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		1.5		A
Peak Current	I_{peak}	$T_j = 25°C$		2.5		A

ELECTRICAL CHARACTERISTICS MC7915C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 23V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−14.4	−15	−15.6	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -18$ to $-30V$	−14.25	−15	−15.75	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -17.5$ to $-30V$			300	mV
		$T_j = 25°C$, $V_i = -20$ to $-26V$			150	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			300	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$			150	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -18.5$ to $-30V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−0.9		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		250		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		1.3		A
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

ELECTRICAL CHARACTERISTICS MC7918C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 27V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−17.3	−18	−18.7	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -22.5$ to $-33V$	−17.1	−18	−18.9	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -21$ to $-33V$			360	mV
		$T_j = 25°C$, $V_i = -24$ to $-30V$			180	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			360	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$			180	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -22$ to $-33V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		300		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		1.1		A
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

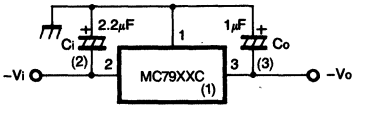
ELECTRICAL CHARACTERISTICS MC7924C

($C_i = 2.2\mu F$, $C_o = 1\mu F$, $T_j = 0$ to $125°C$, $I_o = 500mA$, $V_i = 33V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$	−23	−24	−25	V
		$I_o = 5mA$ to $1A$, $P_o \leq 15W$ $V_i = -27$ to $-38V$	−22.8	−24	−25.2	
Line Regulation	$\triangle V_o$	$T_j = 25°C$, $V_i = -27$ to $-38V$			480	mV
		$T_j = 25°C$, $V_i = -30$ to $-36V$			240	
Load Regulation	$\triangle V_o$	$T_j = 25°C$ $I_o = 5mA$ to $1.5A$			480	mV
		$T_j = 25°C$ $I_o = 250$ to $750mA$			240	
Quiescent Current	I_d	$T_j = 25°C$		3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5mA$ to $1A$			0.5	mA
		$V_i = -27$ to $-38V$			1	
Output Voltage Drift	$\frac{\triangle V_o}{\triangle T}$	$I_o = 5mA$		−1		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$		400		μV
Ripple Rejection	RR	$f = 120Hz$ $\triangle V_i = 10V$	54	60		dB
Dropout Voltage	V_D	$T_j = 25°C$ $I_o = 1A$		2		V
Short Circuit Current	I_{sc}	$T_j = 25°C$		1.1		A
Peak Current	I_{peak}	$T_j = 25°C$		2.2		A

APPLICATION INFORMATION

Fig. 1 — Fixed output regulator



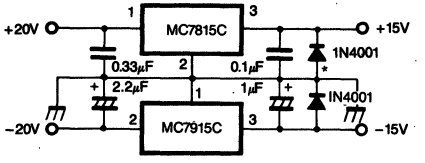
Notes:

(1) To specify an output voltage, substitute voltage value for "XXC".

(2) Required for stability. For value given, capacitor must be solid tantalum. If aluminium electrolitics are used, at least ten times value shown should be selected. Ci is required if regulator is located an appreciable distance from power supply filter.

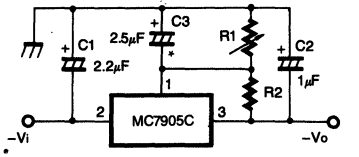
(3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N4001 or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 2 — Split power supply (±15V/1A)



* Against potential latch-up problems.

Fig. 3 — Circuit for increasing output voltage



$V_o = V_{XX} \cdot \frac{R1 + R2}{R2}$

$V_{XX}/R2 > 3\ I_d$

* C3 optional for improved transient response and ripple rejection.

Fig. 4 — High current negative regulator (−5V/4A with 5A current limiting)

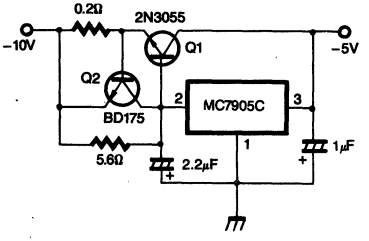
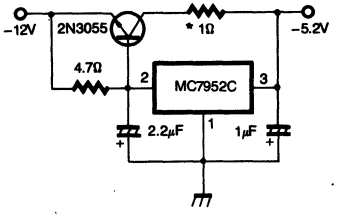


Fig. 5 — Typical ECL system power supply (−5.2V/4A)

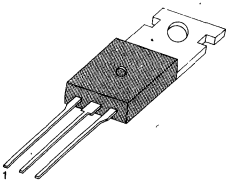


* Optional dropping resistor to reduce the power dissipated in the boost transistor.

3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATOR

The MC79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially indestructible. If adequate heat sinking is provided, they can deliver up to 500mA output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

TO-220



1: GND 2: Input 3: Output

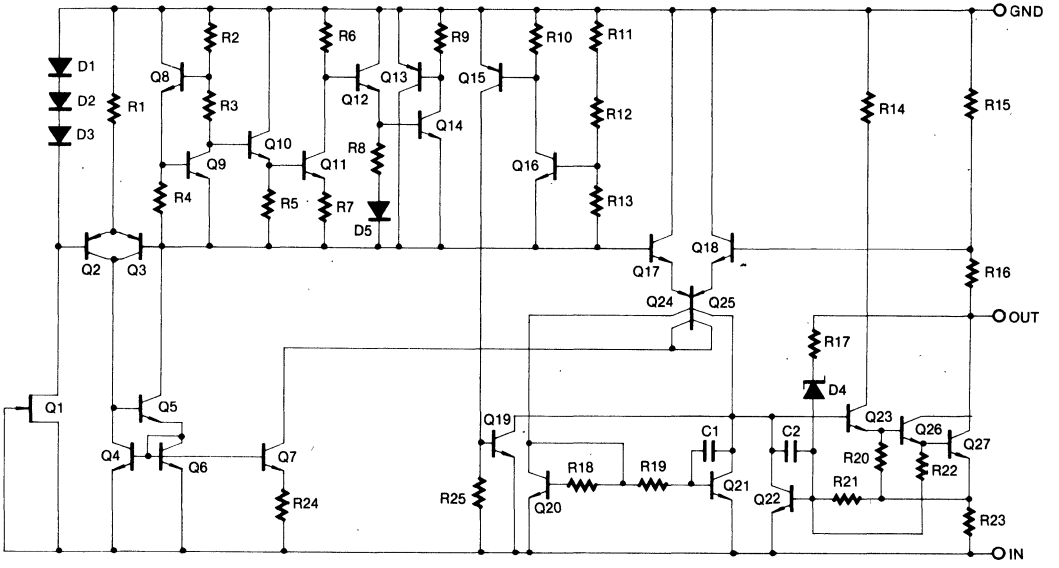
FEATURES

- **Output current in excess of 0.5A**
- **Internal thermal-overload protection**
- **Internal short circuit current limiting**
- **Output transistor safe-area compensation**
- **Available in JEDEC TO-220**
- **Output voltages of −5V, −6V, −8V, −12V, −15V, −18V, −24V**

ORDERING INFORMATION

Device	Package	Operating Temperature
MC79MXXCT	TO-220	0 ~ 125°C

SCHEMATHIC DIAGRAM



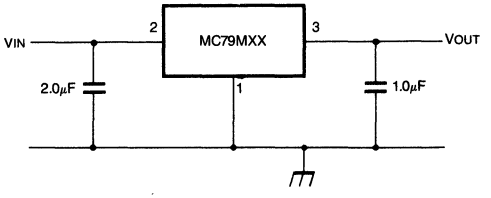
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Input Voltage (for V_o = −5V to −1.8V)	V_I	−35	V
(for V_o = 24V)	V_I	−40	V
Thermal Resistance			
Junction-Case	Θ_{JC}	5	°C/W
Junction-Air	Θ_{JA}	65	°C/W
Operating Temperature Range	T_{opr}	0 ~ +125	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

TYPICAL APPLICATION

Bypass capacitors are recommended for stable operation of the MC79MXXC series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.
The bypass capacitors, (2μF on the input, 1μF on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electrolytics are used, their values should be 10μF or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fixed Output Regulator



ELECTRICAL CHARACTERISTICS MC79M05C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -10V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-4.8	-5.0	-5.2	V
		$5.0mA \leq I_o \leq 350mA$, $V_i = -7V$ to $-25V$		-4.75	-5.0	-5.25	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -7V$ to $-25V$		7.0	50	mV
			$V_i = -8V$ to $-18V$		2.0	30	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	100	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -8V$ to $-25V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			0.2		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			40		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -8$ to $-18V$		54	60		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

ELECTRICAL CHARACTERISTICS MC79M06C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -11V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-5.75	-6.0	-6.25	V
		$5.0mA \leq I_o \leq 350mA$, $V_i = -8.0V$ to $-25V$		-5.7	-6.0	-6.3	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -8V$ to $-25V$		7.0	60	mV
			$V_i = -9V$ to $-19V$		2.0	40	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	120	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -8.0V$ to $-25V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			0.4		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			50		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -9$ to $-19V$		54	60		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC79M08C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -14V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-7.7	-8.0	-8.3	V
		$5.0mA \leq I_o \leq 350mA$, $V_i = -10.5V$ to $-25V$		-7.6	-8.0	-8.4	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -10.5V$ to $-25V$		7.0	80	mV
			$V_i = -11V$ to $-21V$		2.0	50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to 500mA		30	160	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to 350mA				0.4	mA
		$V_i = -10.5V$ to $-25V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-0.6		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			60		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -11.5V$ to $-21.5V$		54	59		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

ELECTRICAL CHARACTERISTICS MC79M12C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -19V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-11.5	-12	-12.5	V
		$5.0mA \leq I_o \leq 350mA$, $V_i = -14.5V$ to $-30V$		-11.4	-1.2	-12.6	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -14.5V$ to $-30V$		8.0	80	mV
			$V_i = -15V$ to $-25V$		3.0	50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to 500mA		30	240	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to 350mA				0.4	mA
		$V_i = -14.5V$ to $-30V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-0.8		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			75		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -15V$ to $-25V$		54	60		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC79M15C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -23V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-14.4	-15	-15.6	V
		$5.0mA \leq I_o \leq 350mA$, $V_i = -17.5V$ to $-30V$		-14.25	-15	-15.75	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -17.5V$ to $-30V$		9.0	80	mV
			$V_i = -18V$ to $-28V$		5.0	50	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	240	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -17.5V$ to $-28V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			90		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -18.5V$ to $-28.5V$		54	59		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

ELECTRICAL CHARACTERISTICS MC79M18C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -27V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-17.3	-18	-18.7	V
		$5.0mA \leq I_o \leq 350mA$, $V_i = -21V$ to $-33V$		-17.1	-18	-18.9	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -21V$ to $-33V$		9.0	80	mV
			$V_i = -24V$ to $-30V$		5.0	60	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	360	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -21V$ to $-33V$				0.4	
Output Voltage Drift	$\triangle V_o/\triangle T$	$I_o = 5mA$			-1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			110		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -22V$ to $-32V$		54	59		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

* Load and line regulation are specified at constant junction temperature changes in V_o due to heating effects must be taken into account separately pulse testing with low duty is used.

ELECTRICAL CHARACTERISTICS MC79M24C

(Refer to test circuit, $0°C < T_j < 125°C$, $I_o = 350mA$, $V_i = -33V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage	V_o	$T_j = 25°C$		-23	-24	-25	V
		$5.0mA \leq I_o \leq 350mA$ $V_i = -27V$ to $-38V$		-22.8	-24	-25.2	
Line Regulation	$\triangle V_o$	$T_j = 25°C$	$V_i = -27V$ to $-38V$		9.0	80	mV
			$V_i = -30V$ to $-36V$		5.0	70	
Load Regulation	$\triangle V_o$	$T_j = 25°C$	$I_o = 5.0mA$ to $500mA$		30	300	mV
Quiescent Current	I_d	$T_j = 25°C$			3	6	mA
Quiescent Current Change	$\triangle I_d$	$I_o = 5.0mA$ to $350mA$				0.4	mA
		$V_i = -27V$ to $-38V$				0.4	
Output Voltage Drift	$\triangle V_o / \triangle T$	$I_o = 5mA$			-1.0		mV/°C
Output Noise Voltage	V_N	$f = 10Hz$ to $100KHz$ $T_j = 25°C$			180		μV
Ripple Rejection	RR	$f = 120Hz$, $V_i = -28V$ to $-38V$		54	58		dB
Dropout Voltage	V_D	$I_o = 500mA$, $T_j = 25°C$			1.1		V
Short Circuit Current	I_{SC}	$V_i = -35V$, $T_j = 25°C$			140		mA
Peak Current	I_{peak}	$T_j = 25°C$			650		mA

VOLTAGE REFERENCE DIODE

The KA336-5.0 integrated circuit is precision 5.0V shunt regulator diodes. The monolithic IC voltage reference operates as a low temperature coefficient 5.0V zener with 0.6 ohm dynamic impedance. A third terminal on the KA336-5.0 allows the reference voltage and temperature coefficient to be trimmed easily.
KA336-5.0 is useful as a precision 5.0V low voltage references for digital voltmeters, power supplies or OP amp circuitry. The 5.0V make it convenient to obtain a stable reference from low voltage supplies. Further, since the KA336-5.0 operates as a shunt regulators, it can be used as either a positive or negative voltage reference.

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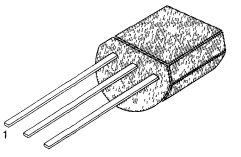


1: Adj 2: Cathode 3: Anode

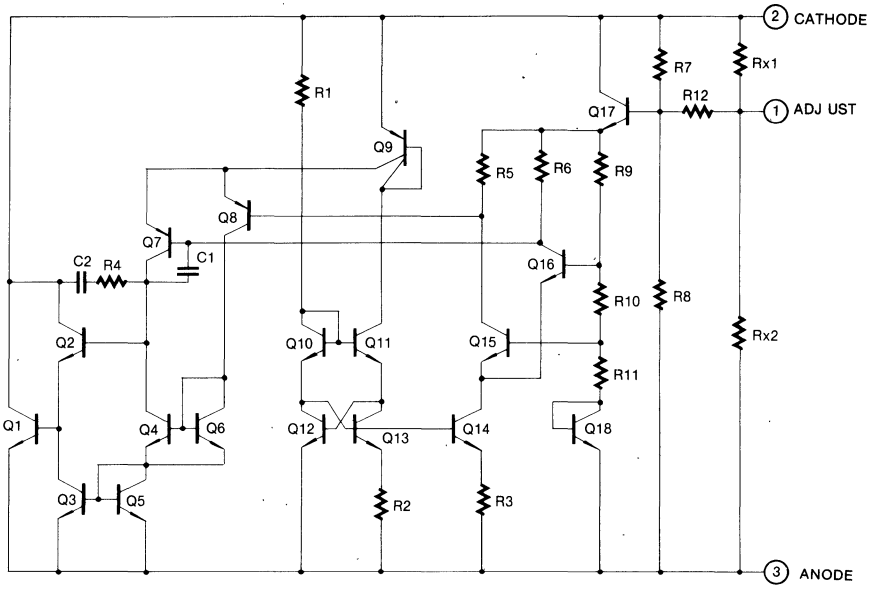
FEATURES

- **Low temperature coefficient**
- **Adjustable 4V to 6V**
- **Wide operating range current of 400μA to 10mA**
- **Three lead transistor package (To-92)**
- **0.6 ohm dynamic impedance**
- **$\pm$1.0% initial tolerance available**
- **Guaranteed temperature stability**
- **Easily trimmed for minimum temperature drift**
- **Fast turn on**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA336Z-5	TO-92	0~70°C

SCHEMATIC DIAGRAM



Rx1, Rx2: External Resistors

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Reverse Current	I_R	15	mA
Forward Current	I_F	10	mA
Storage Temperature Range	T_{stg}	−60 ~ 150	°C
Operating Temperature Range	T_{opr}	0 ~ 70	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Breakdown Voltage	V_R	$I_R = 1mA$	4.8	5.0	5.2	V
Reverse Breakdown Change with Current	$\triangle V_R$	$600\mu A \leq I_R \leq 10mA$		6	20	mV
Reverse Dynamic Impedance	Z_D	$I_R = 1mA$		0.6	2	Ω
Temperature Stability	$\triangle V_R T_1$	$V_R = 5V$, $I_R = 1mA$ $0°C \leq Ta \leq 70°C$		4	12	mV
Reverse Breakdown Change with Current	$\triangle V_R T_2$	$600\mu A \leq I_R \leq 10mA$ $0°C \leq Ta \leq 70°C$		6	24	mV
Adjustment Range	V_A			±1		V
Reverse Dynamic Impedance	Z_{DT}	$I_R = 1mA$, $0°C \leq Ta \leq 70°C$		0.8	2.5	Ω
Long Term Stability	S	$I_R = 1mA$		20		ppm

TYPICAL PERFORMANCE CHARACTERISTICS

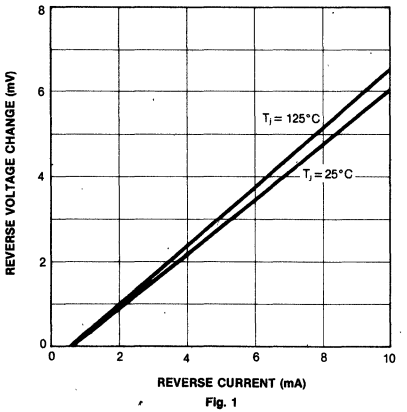


Fig. 1

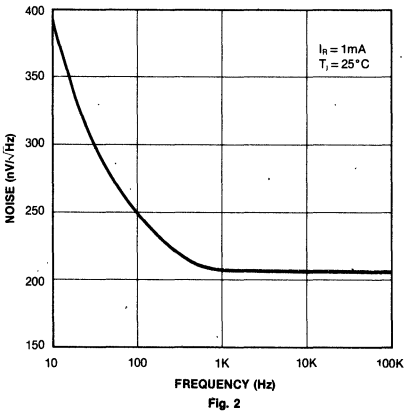


Fig. 2

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

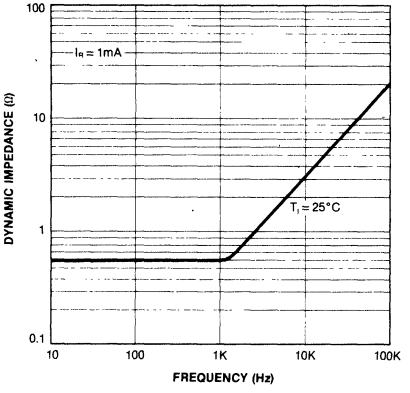


Fig. 3

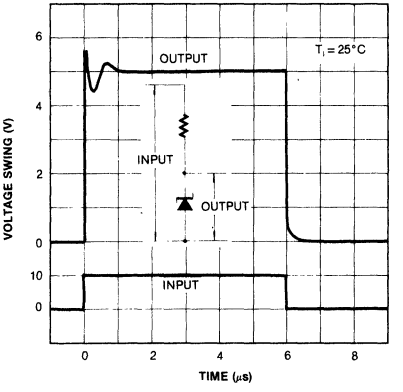


Fig. 4

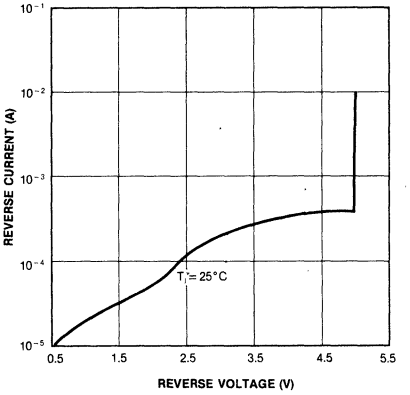


Fig. 5

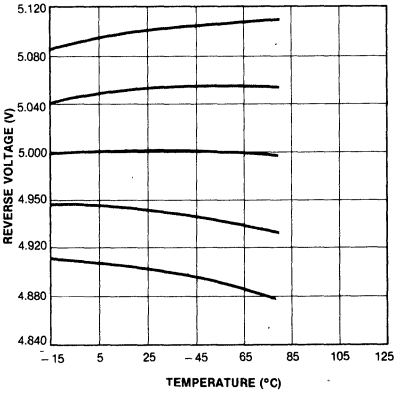


Fig. 6

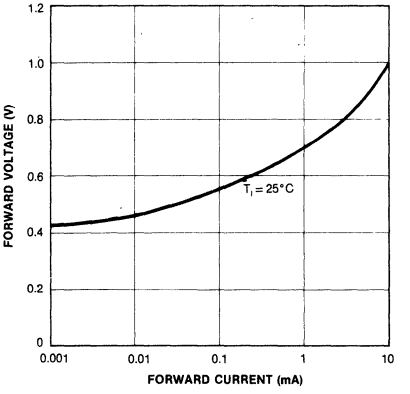


Fig. 7

4

TYPICAL APPLICATIONS

5.0V REFERENCE

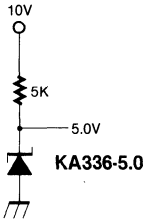
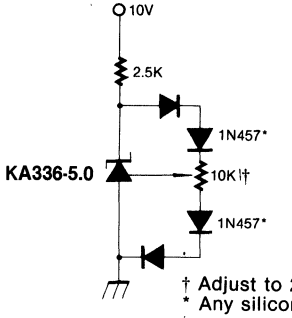


FIGURE 8

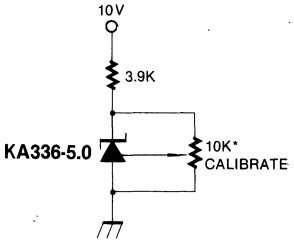
5.0V REFERENCE WITH MINIMUM TEMPERATURE COEFFICIENT



† Adjust to 2.490V
* Any silicon signal diode

FIGURE 9

TRIMMED 4V TO 6V REFERENCE WITH TEMPERATURE COEFFICIENT OF BREAKDOWN VOLTAGE INDEPENDENT



* Does not affect temperature coefficient

FIGURE 10

PRECISION POWER REGULATOR WITH LOW TEMPERATURE COEFFICIENT

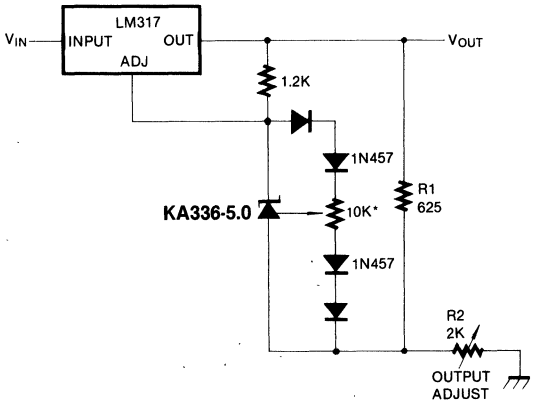


FIGURE 11

5V CROWBAR

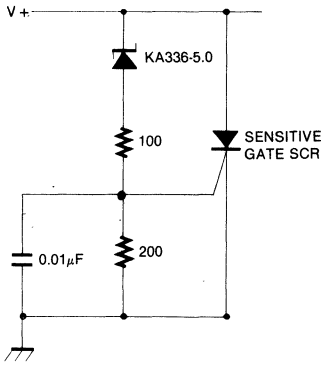


FIGURE 12

MICROPOWER VOLTAGE REFERENCE DIODE

The KA385 is micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10μA to 20mA current range, it features exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the KA385-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result. Careful design of the KA385-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

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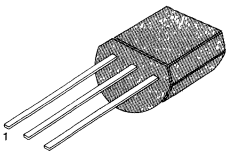


1: N.C. 2: Cathode 3: Anode

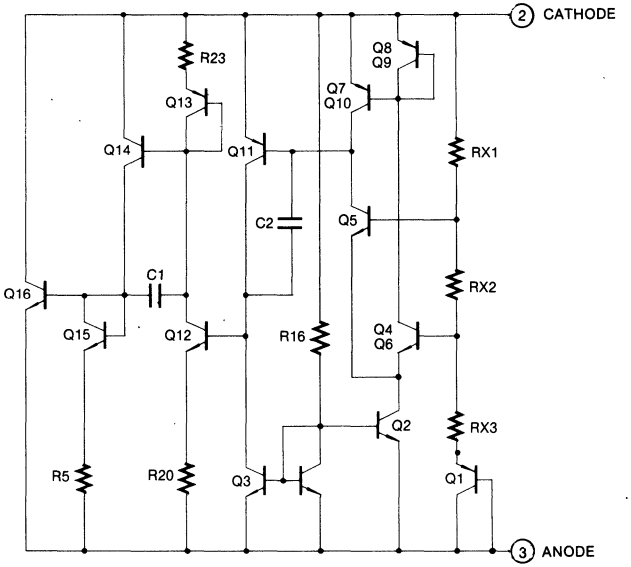
FEATURES

- **Operating current of 10μA to 20mA**
- **1% and 2% initial tolerance**
- **1Ω dynamic impedance**
- **Low temperature coefficient**
- **Low voltage reference – 1.235V**

ORDERING INFORMATION

Device	Package	Operating Temperature
KA385Z-1.2	TO-92	0 ~ 70°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Temperature Range	T_{opr}	0 ~ 70	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Breakdown Voltage	V_R	$I_{min} \leq I_R \leq 20mA$	1.205	1.235	1.260	V
Minimum Operating Current	I_{min}	$0°C \leq Ta \leq 70°C$		8	15	μA
Reverse Breakdown Voltage Change with Current	$\triangle V_R$	$0°C \leq Ta \leq 70°C$, $I_{min} \leq I_R \leq 1mA$ $0°C \leq Ta \leq 70°C$, $1mA \leq I_R \leq 20mA$			1.5 25	mV mV
		$I_{min} \leq I_R \leq 1mA$ $1mA \leq I_R \leq 20mA$			1 20	mV
Reverse Dynamic Impedance	Z_D	$0°C \leq Ta \leq 70°C$, $I_R = 100\mu A$		0.4	1.5	Ω
		$I_R = 100\mu A$		0.4	1	Ω
Average Temperature Coefficient		$0°C \leq Ta \leq 70°C$, $10\mu A \leq I_R \leq 20mA$		20		ppm/°C
Wide Band Noise (RMS)	E_N	$I_R = 100\mu A$, $10Hz \leq f \leq 10KHz$ $0°C \leq Ta \leq 70°C$		60		μV
Long Term Stability	S	$I_R = 100\mu A$		20		ppm/KHR

TYPICAL PERFORMANCE CHARACTERISTICS

TEMPERATURE DRIFT

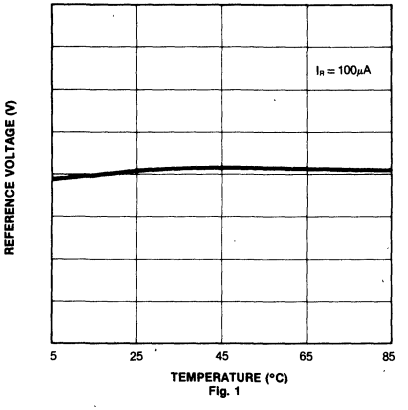


Fig. 1

REVERSE DYNAMIC IMPEDANCE

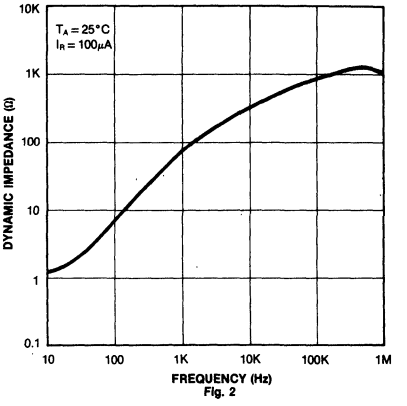


Fig. 2

NOISE VOLTAGE

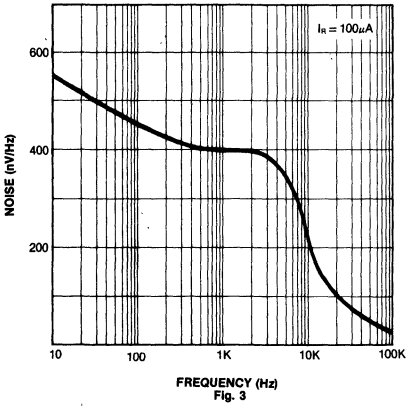


Fig. 3

FILTERED OUTPUT NOISE

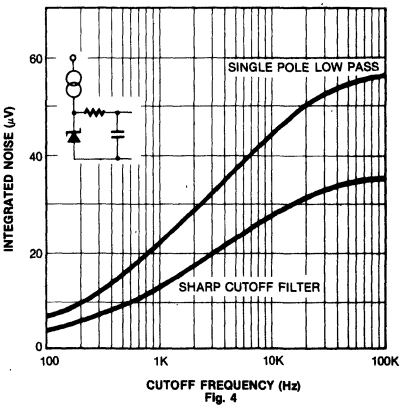


Fig. 4

RESPONSE TIME

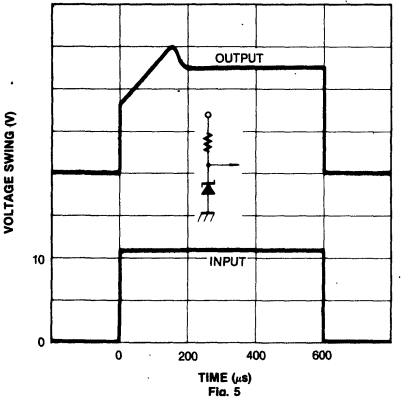
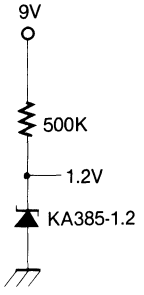


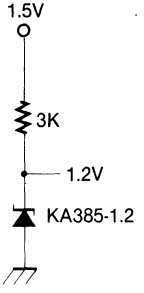
Fig. 5

STANDARD APPLICATIONS

MICROPOWER REFERENCE FROM 9V BATTERY



REFERENCE FROM 1.5V BATTERY



PROGRAMMABLE PRECISION REFERENCES

The KA431 is a three-terminal adjustable regulator series with guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 volts) and 36 volts with two external resistors. These devices have a typical dynamic output impedance of 0.2Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacement for zener diodes in many applications.

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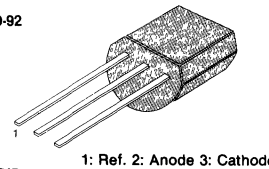
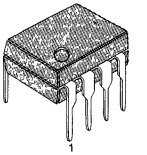


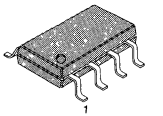
1: Ref. 2: Anode 3: Cathode

8 DIP



1: Cathode 6: Anode 8: Ref. 2, 3, 4, 7: N.C.

8 SOP

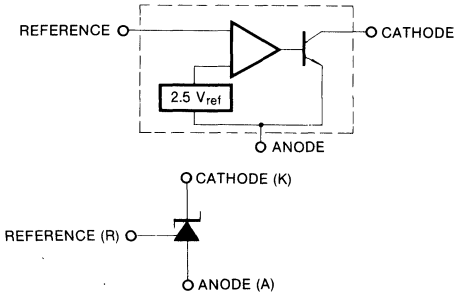


1: Cathode 2, 3, 6, 7: Anode 8: Ref. 4, 5: N.C.

FEATURES

- **Programmable output voltage to 36 volts**
- **Low dynamic output impedance 0.2Ω typical**
- **Sink current capability of 1.0 to 100mA**
- **Equivalent full-range temperature coefficient of 50ppm/°C typical**
- **Temperature compensated for operation over full rated operating temperature range**
- **Low output noise voltage**

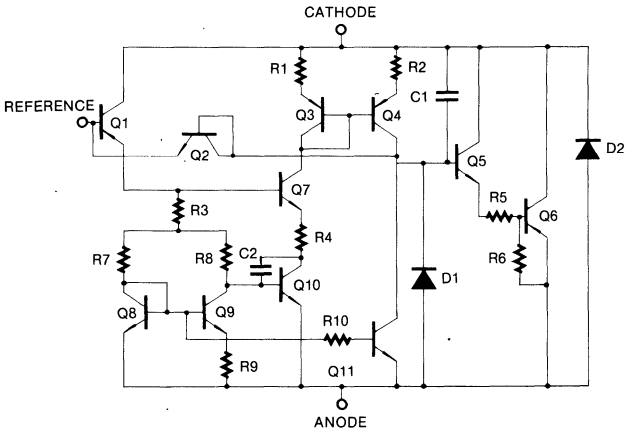
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature	Package
KA431CZ	0 ~ +70°C	TO-92
KA431CN	0 ~ +70°C	8 DIP
KA431CD	0 ~ +70°C	8 SOP
KA431IZ	−40 ~ +85°C	TO-92
KA431IN	−40 ~ +85°C	8 DIP

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operating temperature range applies unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Cathode Voltage	V_{KA}	37	V
Cathode Current Range (Continuous)	I_K	$-100 \sim +150$	mA
Reference Input Current Range	I_{ref}	$0.05 \sim +10$	mA
Power Dissipation	P_D		
D, Z Suffix Package		770	mW
N Suffix Package		1000	mW
Operating Temperature	T_{opr}		
KA431CZ, KA431CN, KA431CD		$0 \sim +70$	°C
KA431IZ, KA431IN		$-40 \sim +85$	°C
Operating Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS

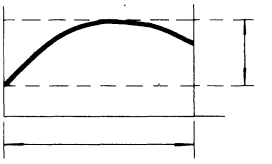
Characteristic	Symbol	Min	Typ	Max	Unit
Cathode Voltage	V_{KA}	V_{ref}		36	V
Cathode Current	I_K	1.0		100	mA

ELECTRICAL CHARACTERISTICS (Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit	*T/C
Reference Input Voltage	V_{ref}	$V_{KA} = V_{ref}$, $I_K = 10mA$	Ta = 25°C	2.440	2.495	2.550	V	1
			Ta = 0°C to 70°C	2.423		2.567		
Deviation of Reference Input Voltage Over Temperature 1	$V_{ref(dev)}$	$V_{KA} = V_{ref}$, $I_K = 10mA$, Ta = 0°C to 70°C			8	17	mV	1
Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	$\frac{V_{ref}}{V_{KA}}$	$I_K = 10mA$	$V_{KA} = V_{ref}$ to 10V		−1.4	−2.7	mV/V	2
			V_{KA} = 10V to 36V		−1.0	−2.0		
Reference Input Current	I_{ref}	$I_K = 10mA$, R1 = 10KΩ, R2 = ∞	Ta = 25°C		1.8	4.0	μA	2
			Ta = 0°C to 70°C			5.2		
Reference Input Current Deviation Over Temperature Range	I_{ref}	$I_K = 10mA$, R1 = 10KΩ, R2 = ∞, Ta = 0°C to 70°C			0.4	1.2	μA	2
Minimum Cathode Current for Regulation	I_{Kmin}	$V_{KA} = V_{ref}$			0.5	1.0	mA	1
Off-State Cathode Current	I_{Koff}	$V_{KA} = 36V$, $V_{ref} = 0V$			2.6	1000	nA	3
Dynamic Impedance 2	Z_{KA}	$V_{KA} = V_{ref}$, $I_K = 1.0$ to 100mA, $f \leq 1.0KHz$			0.22	0.5	Ω	1

* Test Circuit

Note: 1. The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The equivalent full-range temperature coefficient of the reference input voltage, aV_{ref}, is defined as:



Max V_{ref} Min V_{ref} $\triangle T_A$ $V_{ref(dev)}$

$$aV_{ref}\ (\frac{ppm}{°C}) = \frac{(\frac{V_{ref(dev)}}{V_{ref}@25°C}) \times 10^6}{\triangle T_A}$$

where $\triangle T_A$ is the rated operating free-air temperature range of the device.
aV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature

Example: Max V_{ref} = 2500mV@30°C, Min V_{ref} = 2492mV@0°C, V_{ref} = 2495mV@25°C, $\triangle T_A$ = 70°C for KA431C

$$aV_{ref} = \frac{(\frac{8mV}{2495mV}) \times 10^6}{70°C} = 46ppm/°C$$

Because minimum V_{ref} occurs at the lower temperature, the coefficient is positive.

2. The dynamic impedance is defined as:

$$Z_{KA} = \frac{\triangle V_{KA}}{\triangle I_K}$$

When the device is operated with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$Z' = \frac{\triangle V}{\triangle I} = Z_{KA}\ (1 + \frac{R1}{R2})$$

TEST CIRCUIT

Fig. 1 Test Circuit for $V_{KA} = V_{ref}$

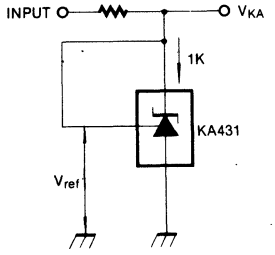


Fig. 2 Test Circuit for $V_{KA} \geq V_{ref}$

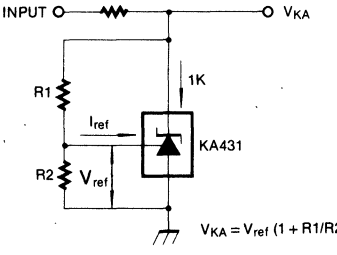
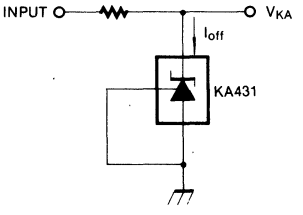


Fig. 3 Test Circuit for I_{off}



TYPICAL PERFORMANCE CHARACTERISTICS

CATHODE CURRENT VS CATHODE VOLTAGE

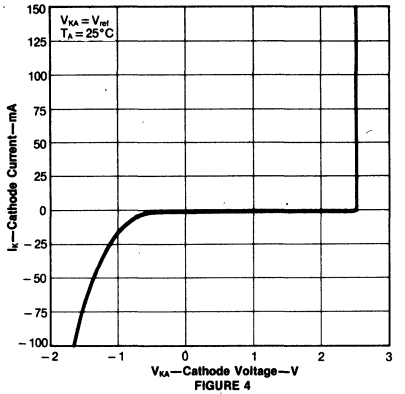


FIGURE 4

CATHODE CURRENT VS CATHODE VOLTAGE

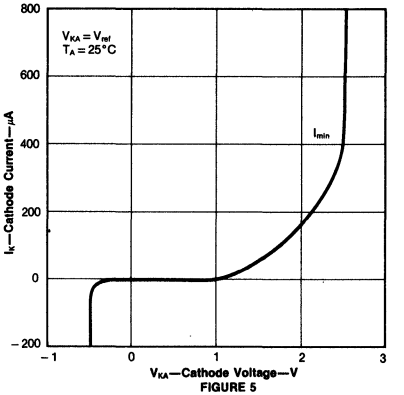


FIGURE 5

CHANGE IN REFERENCE INPUT VOLTAGE VS CATHODE VOLTAGE

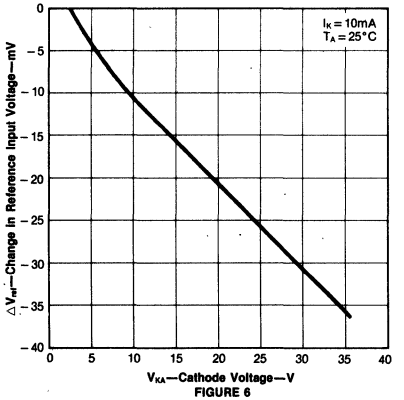


FIGURE 6

NOISE VOLTAGE VS FREQUENCY

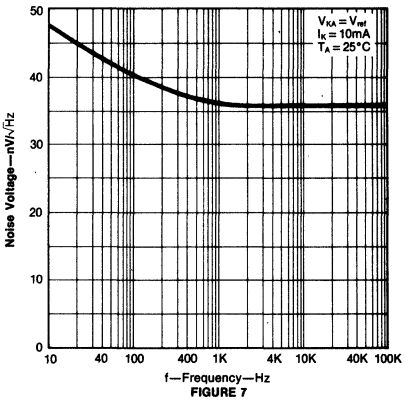


FIGURE 7

DYNAMIC IMPEDANCE VS FREQUENCY

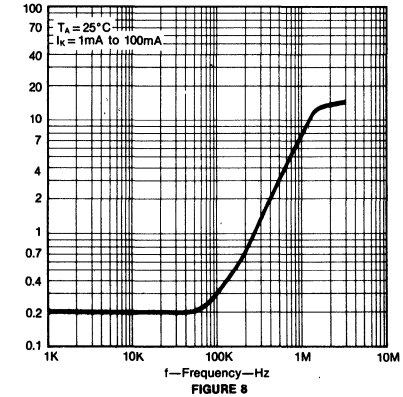


FIGURE 8

SMALL SIGNAL VOLTAGE AMPLIFICATION VS FREQUENCY

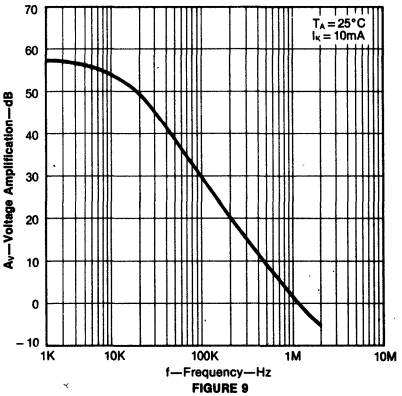


FIGURE 9

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

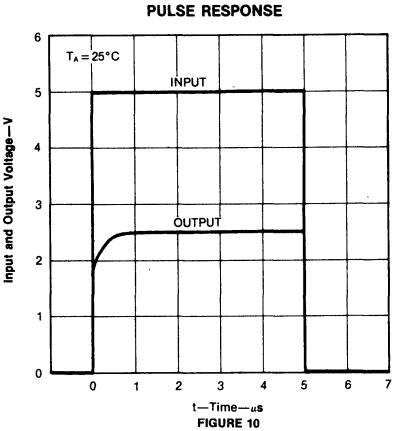
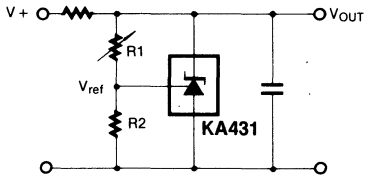


FIGURE 10

TYPICAL APPLICATIONS

FIGURE 11—SHUNT REGULATOR



$$V_{out} = (1 + \frac{R1}{R2})V_{ref}$$

FIGURE 12—SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD

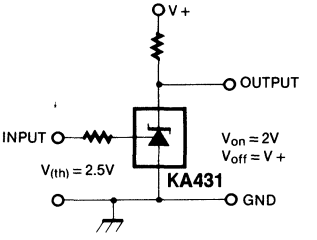
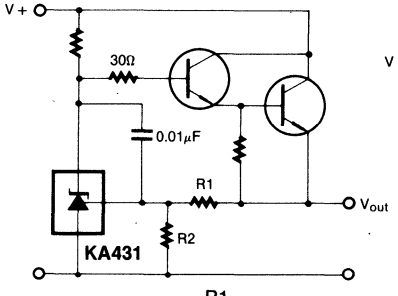
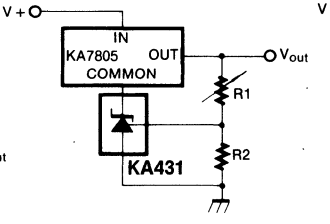


FIGURE 13—SERIES REGULATOR



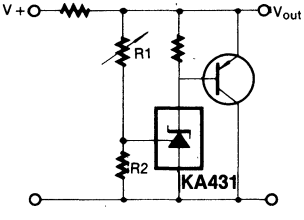
$$V_{out} = (1 + \frac{R1}{R2})V_{ref}$$

FIGURE 14—OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR



$$V_{out} = V_{ref}(1 + \frac{R1}{R2})$$

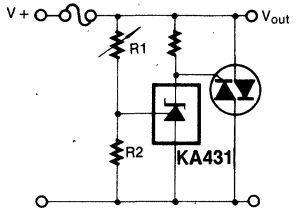
FIGURE 15—HIGHER-CURRENT SHUNT REGULATOR



$$V_{out} = (1 + \frac{R1}{R2})V_{ref}$$

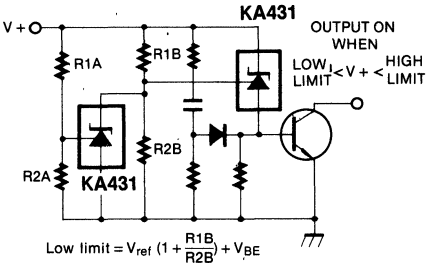
TYPICAL APPLICATIONS (Continued)

FIGURE 16—CROW BAR



$$V_{limit} = (1 + \frac{R1}{R2})V_{ref}$$

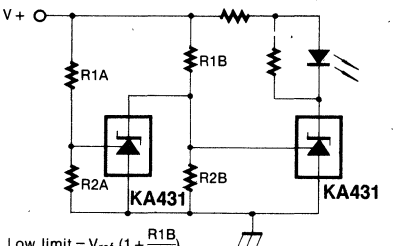
FIGURE 17—OVER-VOLTAGE/UNDER-VOLTAGE PROTECTION CIRCUIT



$$\text{Low limit} = V_{ref}(1 + \frac{R1B}{R2B}) + V_{BE}$$

$$\text{High limit} = V_{ref}(1 + \frac{R1A}{R2A})$$

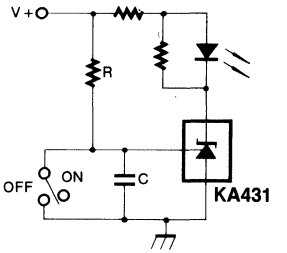
FIGURE 18—VOLTAGE MONITOR



$$\text{Low limit} = V_{ref}(1 + \frac{R1B}{R2B})$$

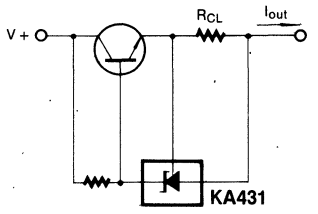
$$\text{High limit} = V_{ref}(1 + \frac{R1A}{R2A})$$

FIGURE 19—DELAY TIMER



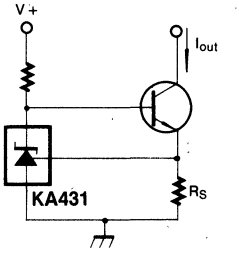
$$\text{Delay} = R\text{-}C\text{-}\ln\frac{V+}{(V+) - V_{ref}}$$

FIGURE 20—CURRENT LIMITER OR CURRENT SOURCE



$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

FIGURE 21—CONSTANT-CURRENT SINK

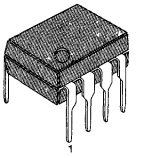


$$I_{out} = \frac{V_{ref}}{R_S}$$

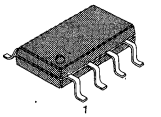
SINGLE OPERATIONAL AMPLIFIER

The KA201A and KA301A are general-purpose operational amplifiers which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain: unity-gain compensation can be obtained with a single 30pF capacitor.

8 DIP



8 SOP

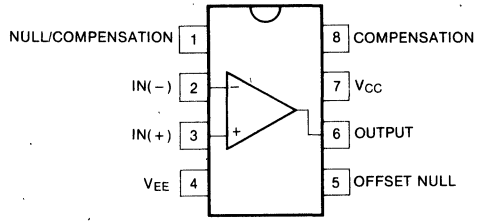


FEATURES

- **Unity-gain phase compensation with a single 30pF**
- **Short-circuit protection and latch-free operation**
- **Slew rate of 10V/μs as a summing amplifier**
- **Class AB output provides excellent linearity**

4

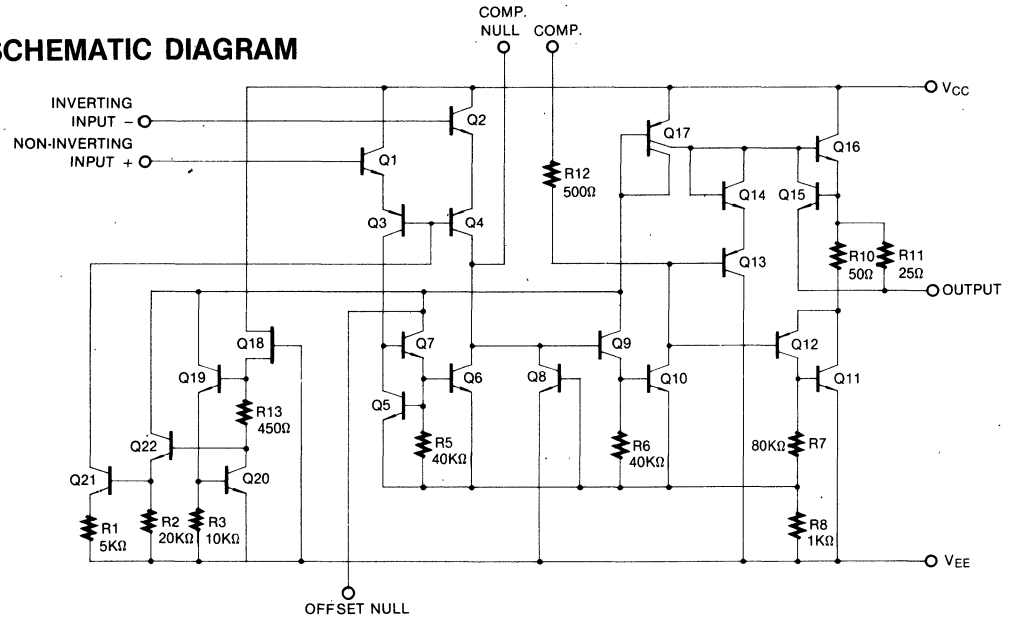
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA201AN	8 DIP	−25°C ~ +85°C
KA301AN		0°C ~ 70°C
KA201AD	8 SOP	−25°C ~ +85°C
KA301AD		0°C ~ +70°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	KA201A	KA301A	Unit
Supply Voltage	V_S	±22	±18	V
Differential Input Voltage	V_{ID}	±30	±30	V
Input Voltage	V_I	±15	±15	V
Output Short Circuit Duration		Continuous	Continuous	
Power Dissipation	P_D	500	500	mW
Operating Temperature Range	T_{opr}	−25 ~ +85	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(−25°C≤Ta≤+85°C for the KA201A, 0°C≤Ta≤+70°C for the KA301A, unless otherwise specified)

Characteristic	Symbol	Test Conditions		KA201A			KA301A			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S≤50KΩ			0.7	2.0		2.0	7.5	mV
			T_{amin}≤T_a≤T_{amax}			3			10	mV
Input Offset Current	I_{IO}				1.5	10		3	50	nA
			T_{amin}≤T_a≤T_{amax}			20			70	nA
Input Bias Current	I_{IB}				30	75		70	250	nA
			T_{amin}≤T_a≤T_{amax}			100			300	nA
Supply Current	I_S	V_S = ±20V			1.8	3.0				mA
		V_S = ±15V						1.8	3.0	mA
		V_S = ±20V, T_a = T_{amax}			1.2	2.5				mA
Large Signal Voltage Gain	A_V	V_{CC} = ±15V, R_L≥2KΩ, V_o = ±10V		50	160		25	160		V/mV
			T_{amin}≤T_a≤T_{amax}	25			15			V/mV
Average Temperature Coefficient of Input Offset Voltage	$\triangle V_{IO}/\triangle T$	T_{amin}≤T_a≤T_{amax}			3.0	15		6.0	30	μV/°C
Average Temperature Coefficient of Input Offset Current	$\triangle I_{IO}/\triangle T$	25°C≤T_a≤T_{amax}			0.01	0.1		0.01	0.3	nA/°C
		T_{amin}≤T_a≤25°C			0.02	0.2		0.02	0.6	nA/°C
Input Voltage Range	V_{ICR}	V_S = ±20V	T_{amin}≤T_a≤T_{amax}	±15						V
		V_S = ±15V	T_{amin}≤T_a≤T_{amax}				±12			V
Common-Mode Rejection Ratio	CMRR	R_S≤50KΩ	T_{amin}≤T_a≤T_{amax}	80	96		70	90		dB
Power Supply Rejection Ratio	PSRR	R_S≤50KΩ	T_{amin}≤T_a≤T_{amax}	80	96		70	96		dB
Output Voltage Swing	V_{OUT}	V_S = ±15V	R_L = 10KΩ	±12	±14		±12	±14		V
			R_L = 2.0KΩ	±10	±13		±10	±13		V
Input Resistance	R_i			1.5	4.0		0.5	2.0		MΩ
Slew Rate	SR				0.5			0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT

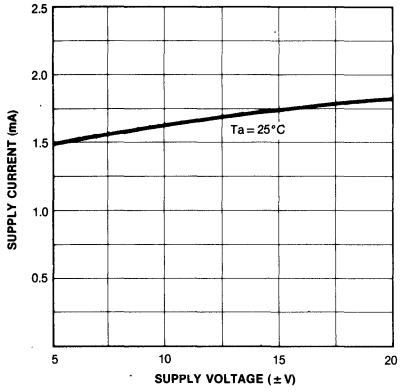


Fig. 1

VOLTAGE GAIN

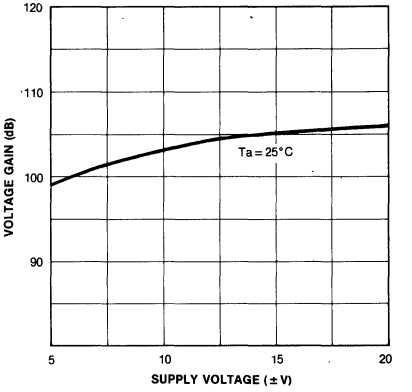


Fig. 2

CURRENT LIMITING

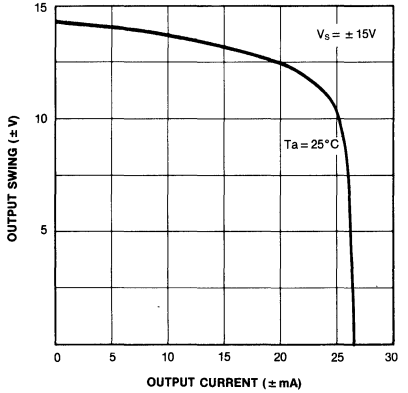


Fig. 3

COMMON MODE REJECTION

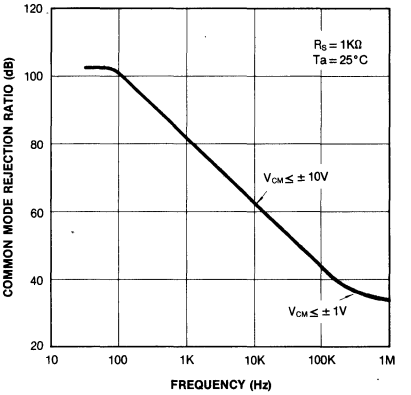


Fig. 4

POWER SUPPLY REJECTION

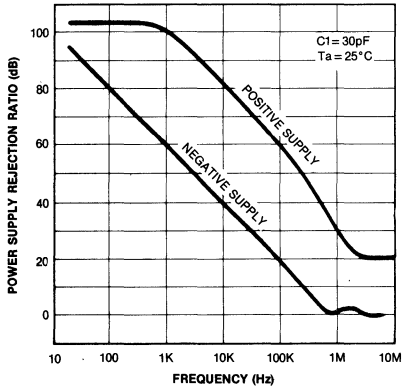
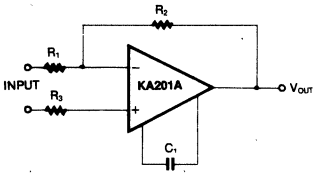


Fig. 5

4

SINGLE POLE COMPENSATION



$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$

$C_S \geq 30pF$

Fig. 6

OPEN LOOP FREQUENCY RESPONSE

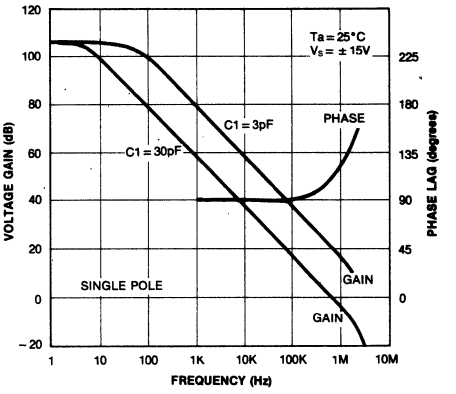


Fig. 7

LARGE SIGNAL FREQUENCY RESPONSE

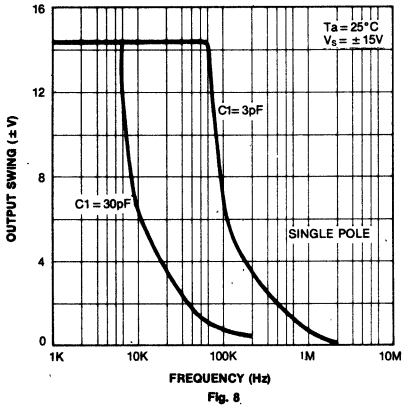


Fig. 8

VOLTAGE FOLLOWER PULSE RESPONSE

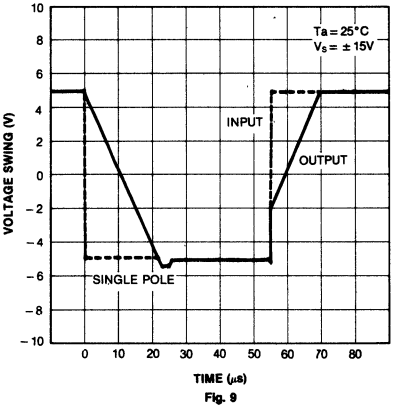
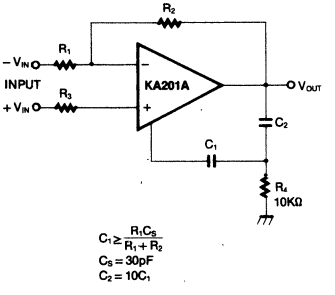


Fig. 9

TWO POLE COMPENSATION



$C_1 \geq \frac{R_1 C_S}{R_1 + R_2}$

$C_S = 30pF$

$C_2 = 10C_1$

Fig. 10

OPEN LOOP FREQUENCY RESPONSE

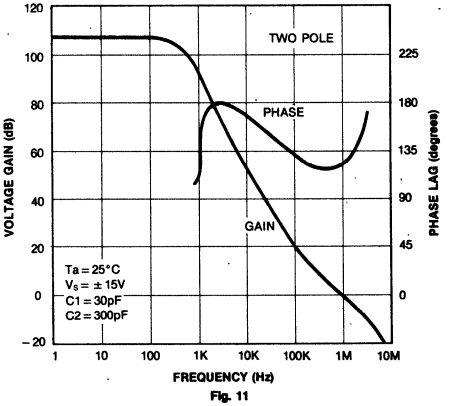


Fig. 11

LARGE SIGNAL FREQUENCY RESPONSE

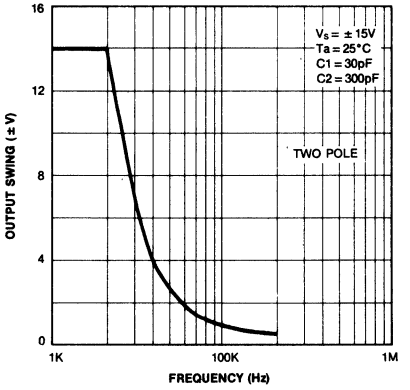


Fig. 12

VOLTAGE FOLLOWER PULSE RESPONSE

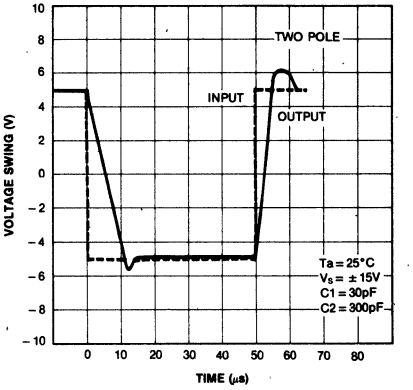


Fig. 13

FEEDFORWARD COMPENSATION

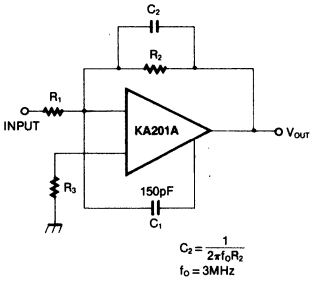


Fig. 14

OPEN LOOP FREQUENCY RESPONSE

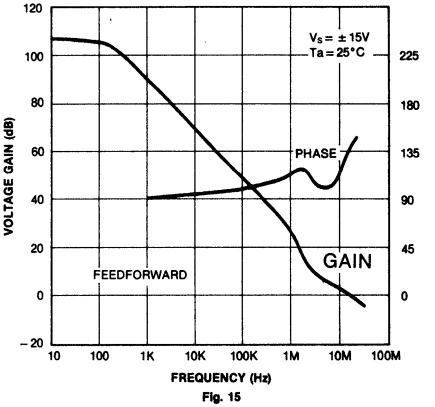


Fig. 15

LARGE SIGNAL FREQUENCY RESPONSE

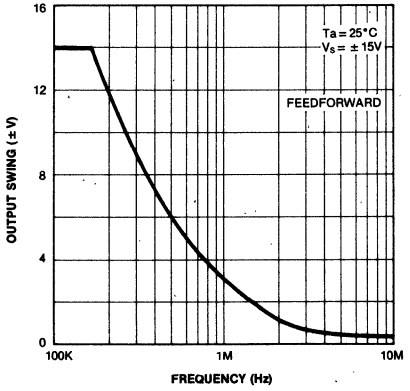


Fig. 16

INVERTER PULSE RESPOSE

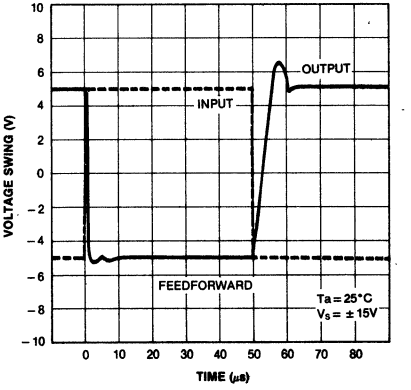
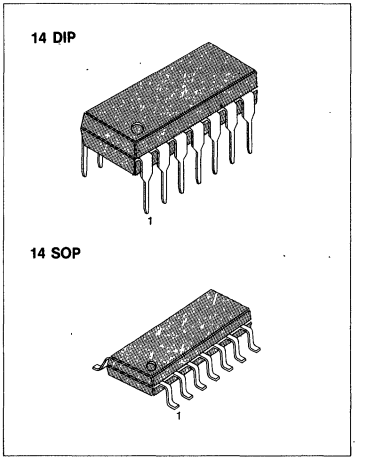


Fig. 17

DIFFERENTIAL VIDEO AMPLIFIER

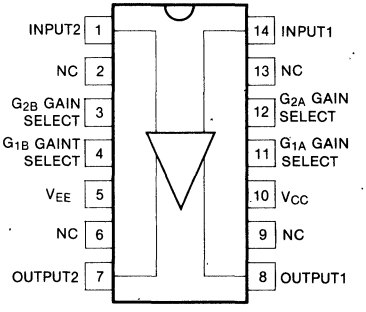
The KA733C is a monolithic differential input, differential output, wideband video amplifier.
The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. The KA733C offers fixed gains 10,100,400 without external components, and adjustable gains from 10 to 400 by use of an external resistor.
The KA733C is intended for use as a high performance video and pluse amplifier in communications, magnetic memories, displays and video recorder systems.



FEATURES

- **120MHz bandwidth**
- **250KΩ input resistance**
- **Selectable gains of 10,100,400**
- **No frequency compensation required**

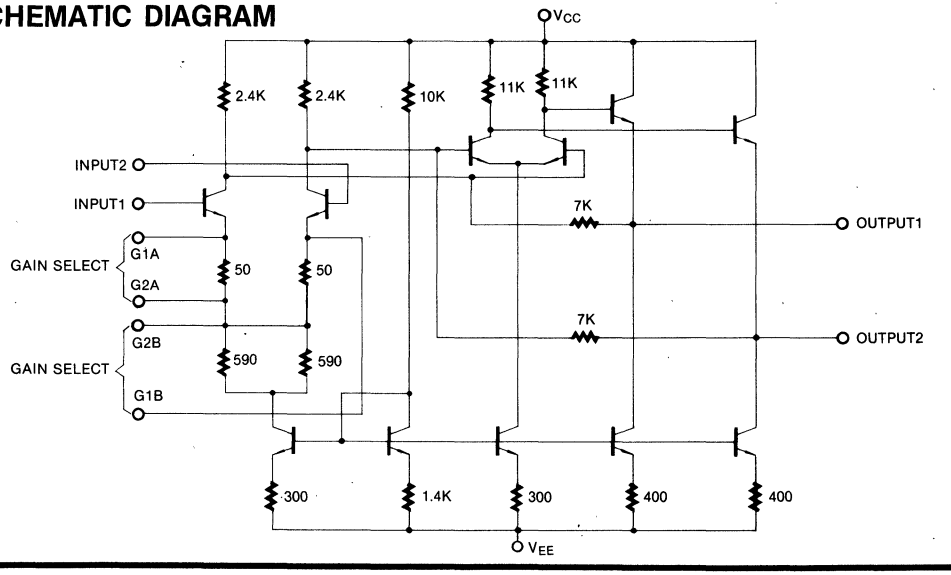
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA733CN	14 DIP	0 ~ +70°C
KA733CD	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Differential Input Voltage	V_{ID}	±5	V
Common mode input Voltage	V_I	±6	V
Power Supply Voltage	V_S	±8	V
Output Current	I_O	10	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +6V, V_{EE} = −6V, Ta = 25°C, unless otherwise specified)

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Voltage Gain Gain 1 (Note 1) Gain 2 (" 2) Gain 3 (" 3)	1	A_V	R_L = 2KΩ, V_{out} = $3V_{p-p}$	 250 80 8	 400 100 10	 600 120 12	V/V
Bandwidth Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	2	BW	R_S = 50Ω		 40 90 120		MHz
Rise Time Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	2	t_r	R_S = 50Ω V_{OUT} = $1V_{p-p}$		 10.5 4.5 2.5	 12	ns
Propagation Delay Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	2	t_{pd}	R_S = 50Ω V_{OUT} = $1V_{p-p}$		 7.5 6.0 3.6	 10	ns
Input Resistance Gain 1 (" 1) Gain 2 (" 2) Gain 3 (" 3)	3	R_i	$V_{OD} \leq 1V$	 10	 4.0 30 250		KΩ
Input Offset Current		I_{IO}			0.4	5	μA
Input Bias Current		I_{IB}			9	30	μA
Input Voltage Range	1	V_{ICR}		±1			V
Common Mode Rejection Ratio Gain 2 Gain 2	4	CMRR	V_{CM} = ±1V, f ≤ 100KHz V_{CM} = ±1V, f = 5MHz	 60	 86 60		dB dB
Power Supply Rejection Ratio Gain 2	1	PSRR	$\triangle V_S$ = ±0.5V	50	70		dB
Output Offset Voltage Gain 1 Gain 2 and 3	1	V_{OO}	R_L = ∞		 0.6 0.35	 1.5 1.5	 V V
Input Capacitance			Gain 2		2.0		pF

ELECTRICAL CHARACTERISTIC (Continued)

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Common Mode Voltage	1	V_{OCM}	$R_L = \infty$	2.4	2.9	3.4	V
Output Voltage Swing	1	V_{OUT}	$R_L = 2K\Omega$	3.0	4.0		V
Output Sink Current		I_{sink}		2.5	3.6		mA
Power Supply Current	1	I_S	$R_L = \infty$		18	24	mA
Output Resistance		R_o			20		Ω

ELECTRICAL CHARACTERISTICS

The following specifications apply over the range of $0°C \leq Ta \leq 70°C$ $V_{CC} = +6V$, $V_{EE} = -6V$

Characteristic	Test Figure	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Voltage Gain Gain 1 (Note 1) Gain 2 (Note 2) Gain 3 (Note 3)	1	A_V	$R_L = 2K\Omega$ $V_{out} = 3V_{p\text{-}p}$	 250 80 80		 600 120 12	V/V
Input Bias Current		I_{IB}				40	μA
Input Offset Current		I_{IO}				6.0	μA
Input Voltage Range	1	V_{ICR}		±1.0			V
Input Impedance (Gain 2)	3	R_i		8.0			KΩ
Common Mode Rejection Ratio Gain 2 (Note 2)	4	CMRR	$V_{CM} = \pm 1V$, $f \leq 100KHz$	50			dB
Power Supply Rejection Ratio Gain 2 (Note 2)	1	PSRR	$\triangle V_{CC} = \pm 0.5V$ $\triangle V_{EE} = \pm 0.5V$	50			dB
Output Offset Voltage Gain 1 (Note 1) Gain 2 and Gain 3 (Note 2, 3)	1	V_{OO}				 1.5 1.5	V
Output Voltage Swing	1	V_{OP}		2.8			V
Output Sink Current		I_{sink}		2.5			mA
Power Supply Current		I_S				27	mA

Notes 1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUITS

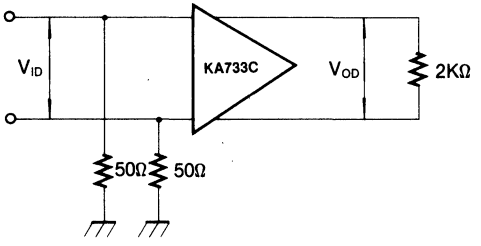


Fig. 1

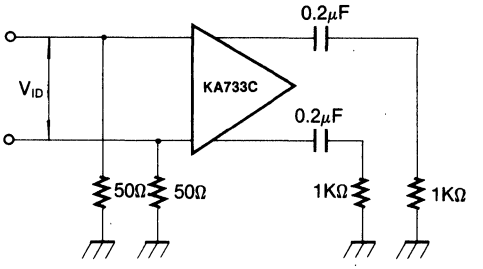


Fig. 2

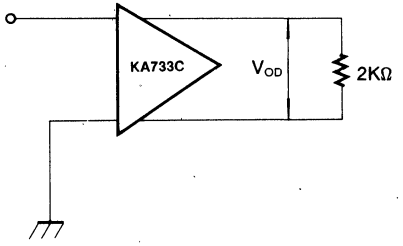


Fig. 3

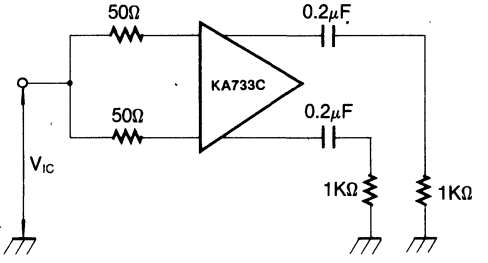


Fig. 4

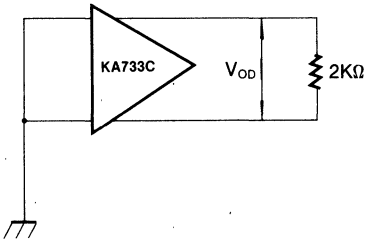
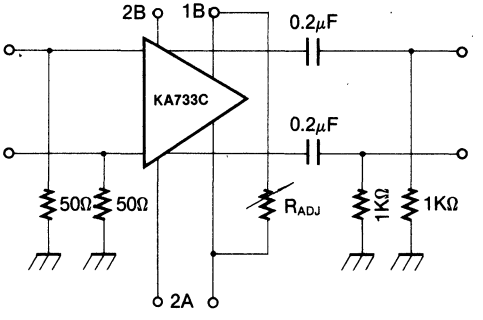


Fig. 5



VOLTAGE AMPLIFICATION ADJUSMENT

Fig. 6

TYPICAL PERFORMANCE CHARACTERISTICS

PHASE SHIFT vs FREQUENCY

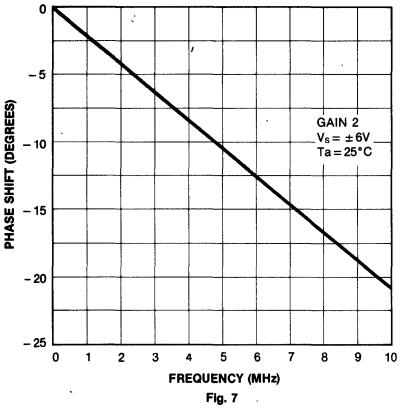


Fig. 7

PHASE SHIFT vs FREQUENCY

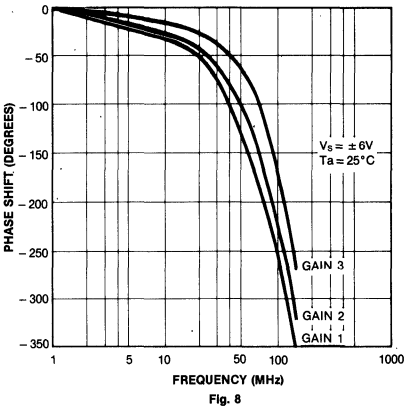


Fig. 8

VOLTAGE GAIN vs FREQUENCY

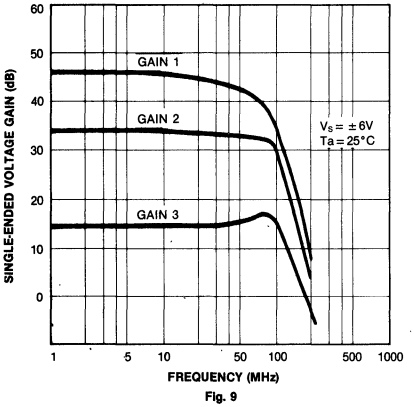


Fig. 9

PULSE RESPONSE

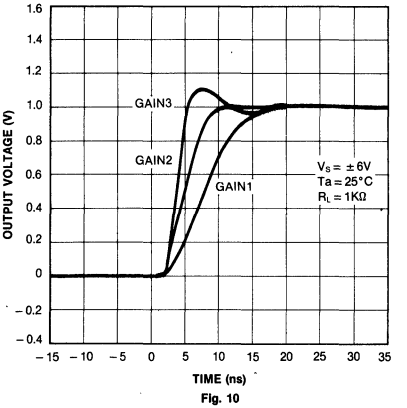


Fig. 10

PULSE RESPONSE vs SUPPLY VOLTAGE

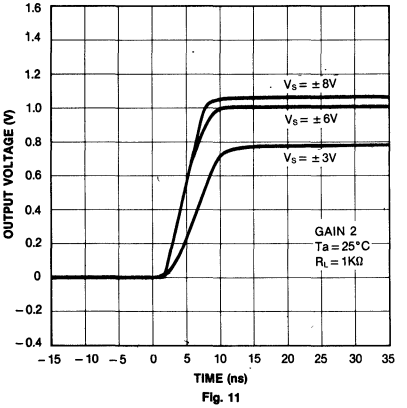


Fig. 11

PULSE RESPONSE vs TEMPERATURE

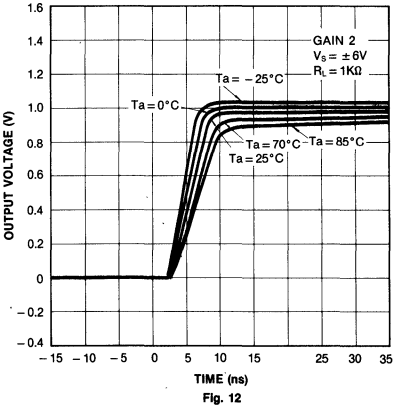


Fig. 12

COMMON MODE REJECTION RATIO vs FREQUENCY

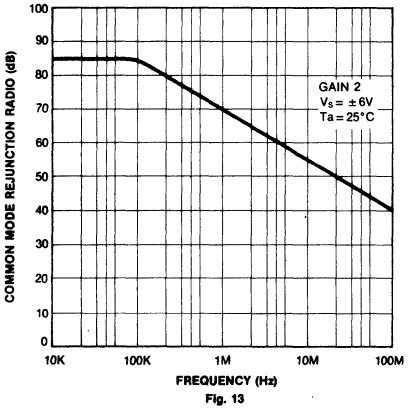


Fig. 13

OUTPUT VOLTAGE SWING vs FREQUENCY

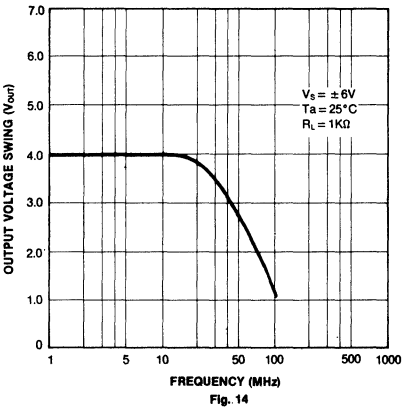


Fig. 14

DIFFERENTIAL OVERDRIVE RECOVERY TIME

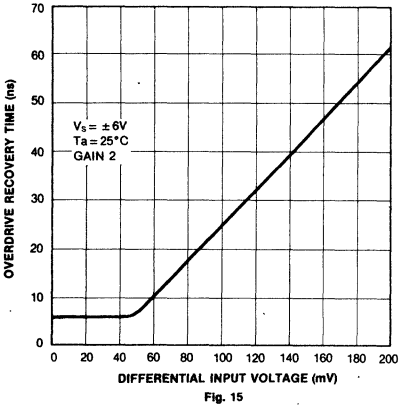


Fig. 15

VOLTAGE GAIN vs SUPPLY VOLTAGE

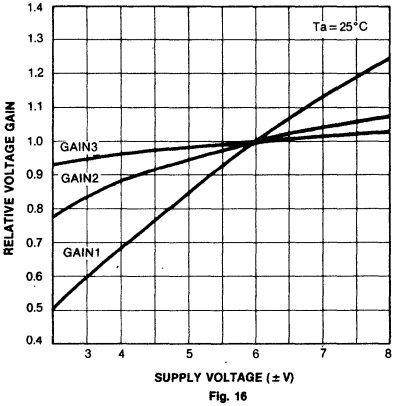


Fig. 16

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

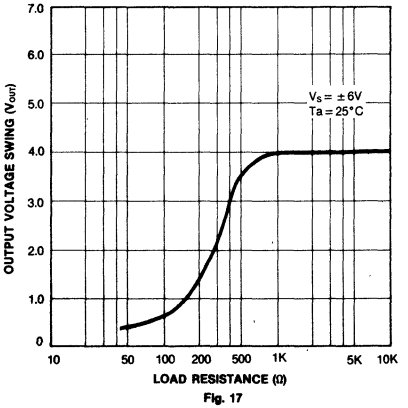


Fig. 17

GAIN vs FREQUENCY vs SUPPLY VOLTAGE

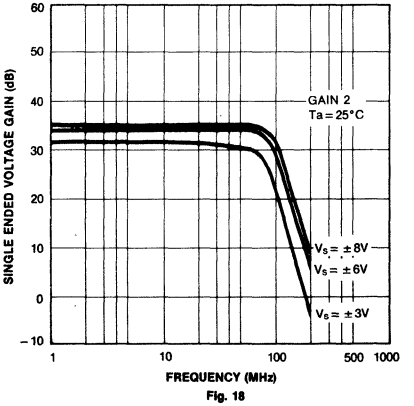


Fig. 18

4

SUPPLY CURRENT vs TEMPERATURE

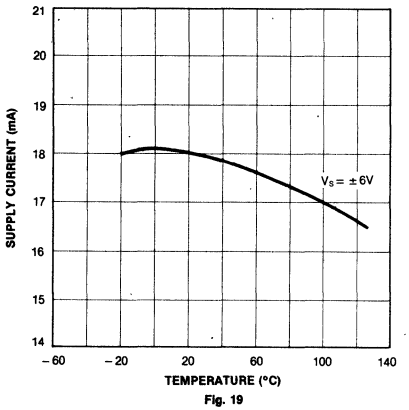


Fig. 19

SUPPLY CURRENT vs SUPPLY VOLTAGE

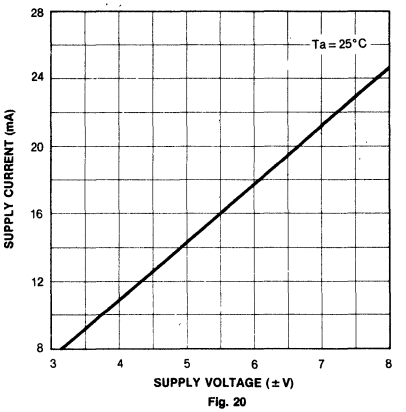


Fig. 20

VOLTAGE GAIN vs R_{ADJ}

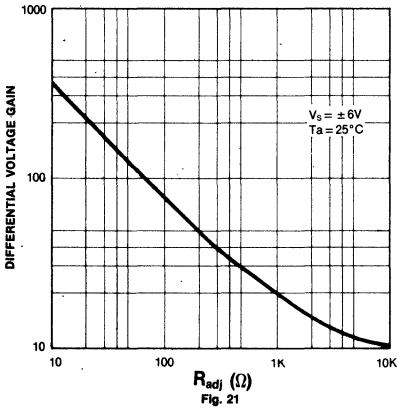
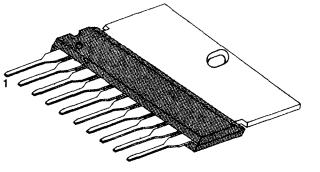


Fig. 21

DUAL POWER OPERATIONAL AMPLIFIER

The KA9256 is a dual power operational amplifier and it is output maximum current is 1.0A ($V_S = \pm 15V$). It can be used in arm driver for player, driver for brush motors forward and reverse rotation control and CD output driver for hole motor.

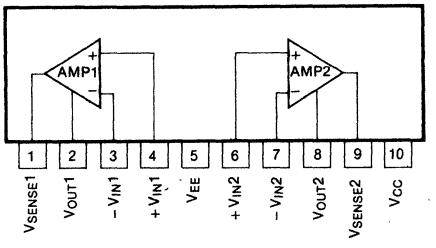
10 SIP



FEATURES

- **Interal current limiting: $I_{SC} = 350mA$ ($R_{SC} = 2.2\Omega$)**
- **High output current: $I_o = 500mA$ max**
- **10 SIP H/S package**
- **Internal phase compensated**

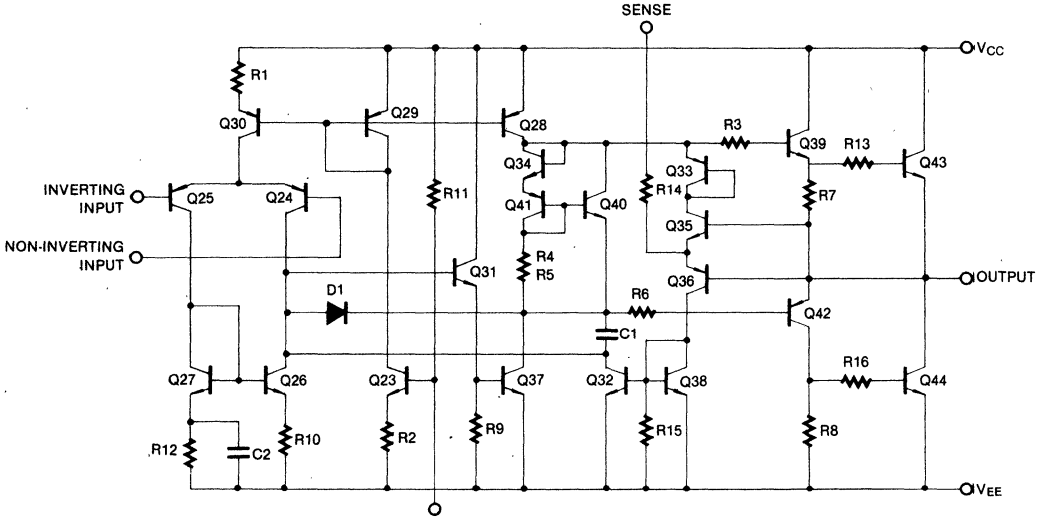
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA9256	10 SIP H/S	– 20 ~ + 70°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_S	± 18	V
Output Current	I_o	1.0	A
Power Dissipation	P_D	12.5	W
Operating Temperature Range	T_{opr}	− 20 ~ + 70	°C
Storage Temperature Range	T_{stg}	− 65 ~ + 150	°C

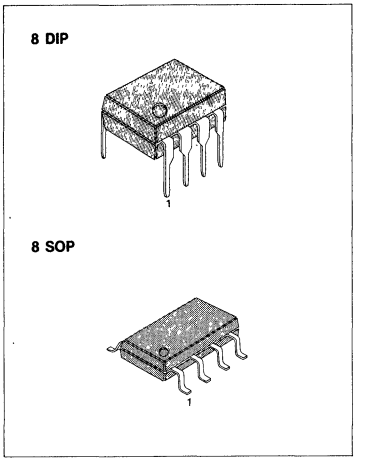
ELECTRICAL CHARACTERISTICS

(V_{CC} = + 15V, V_{EE} = − 15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}			2	6	mV
Input Offset Current	I_{IO}			10	200	nA
Input Bias Current	I_{IB}			100	700	nA
Supply Current	I_S			10	20	mA
Output Voltage Swing	V_{OUT}	R_L = 33Ω	± 12	± 13		V
Large Signal Voltage Gain	A_V			100		dB
Input Voltage Range	V_{ICR}		± 12	± 14		V
Common Mode Rejection Ratio	CMRR		70	90		dB
Power Supply Rejection Ratio	PSRR			50	150	μV/V
Bandwidth	BW			1.0		MHz
Slew Rate	SR	A_V = 1, R_L = 33Ω, R = 10Ω, C = 0.1μF		0.15		V/μs
Limiting Current	I_{OS}	R_{SC} = 2.2Ω		0.35		A
Cross Talk	CT	R_L = 33Ω, V_o = $1V_{p-p}$		60		dB

SINGLE OPERATIONAL AMPLIFIER

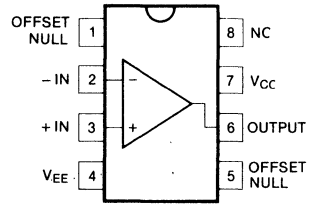
The KF351 is JFET input operational amplifier with an internally trimmed input offset voltage. The JFET input device provides wide bandwidth, low input bias currents and offset currents.



FEATURES

- **Internally trimmed offset voltage: 10mV**
- **Low input bias current: 50pA**
- **Wide gain bandwidth: 4MHz**
- **High slew rate: 13V/μs**
- **Low supply current: 1.8mA**
- **High input impedance: $10^{12}\Omega$**

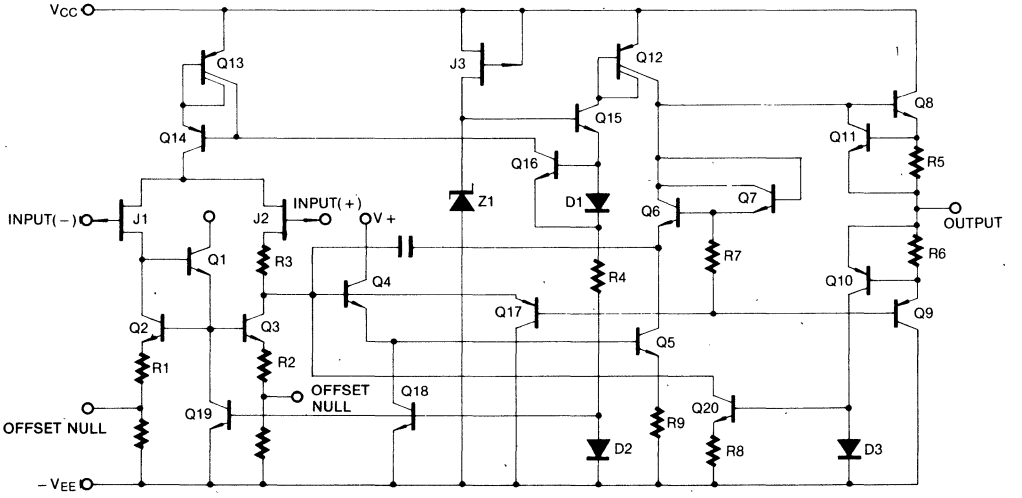
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KF351N	8 DIP	0 ~ +70°C
KF351D	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_S	±18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range	V_I	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	500	mV
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

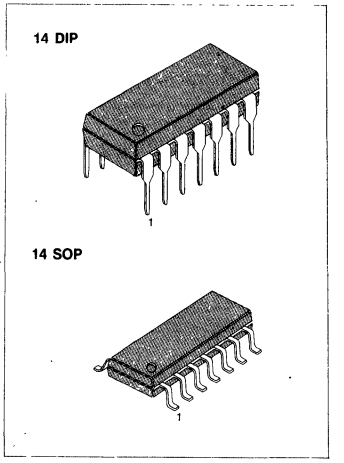
Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	R_S = 10K			5.0	10	mV
			0°C≤Ta≤+70°C			13	
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	R_S = 10K	0°C≤Ta≤+70°C		10		μV/°C
Input Offset Current	I_{IO}				25	100	pA
			0°C≤Ta≤+70°C			4	nA
Input Bias Current	I_{IB}				50	200	pA
			0°C≤Ta≤+70°C			8	nA
Input Resistance	R_i				10^{12}		Ω
Large Signal Voltage Gain	A_V	V_O = ±10V, R_L = 2KΩ		25	100		V/mV
			0≤Ta≤+70°C	15			
Output Voltage Swing	V_{OUT}	R_L = 10KΩ		±12	±13.5		V
Input Voltage Range	V_{ICR}			±11	+15		V
Common Mode Rejection Ratio	CMRR	R_S≤10KΩ		70	100		dB
Power Supply Rejection Ratio	PSRR	R_S≤10KΩ		70	100		dB
Power Supply Current	I_S				1.8	3.4	mA
Slew Rate	SR	A_V = 1			13		V/μs
Gain-Bandwidth Product	GBW				4		MHz

QUAD OPERATIONAL AMPLIFIERS

The LM224 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

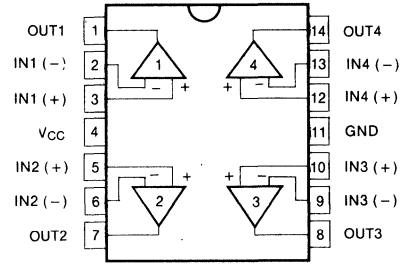
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.



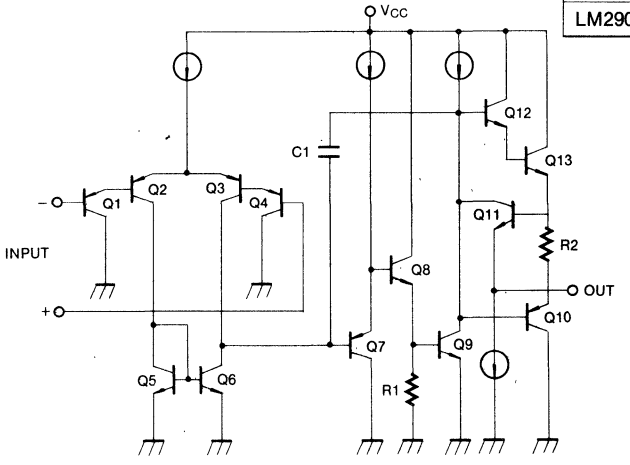
FEATURES

- **Internally frequency compensated for unity gain**
- **Large DC voltage gain: 100dB**
- **Wide power supply range: LM224/A, LM324/A: 3V ~ 32V (or ±1.5V ~ 16V)**
  LM2902: 3V ~ 26V (or ±1.5V ~ 13V)
- **Input common-mode voltage range includes ground**
- **Large output voltage swing: 0V DC to V_{CC}-1.5V DC**
- **Power drain suitable for battery operation.**

BLOCK DIAGRAM



SCHEMATIC DIAGRAM (One Section Only)



ORDERING INFORMATION

Device	Package	Operating Temperature
LM324N LM324AN	14 DIP	0 ~ +70°C
LM324D LM324AD	14 SOP	
LM224N LM224AN	14 DIP	−25 ~ +85°C
LM224D LM224AD	14 SOP	
LM2902N	14 DIP	−40 ~ +85°C
LM2902D	14 SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM224/LM224A	LM324/LM324A	LM2902	Unit
Power Supply Voltage	V_S	± 18 or 32	± 18 or 32	± 13 or 26	V
Differential Input Voltage	V_{ID}	32	32	26	V
Input Voltage	V_I	−0.3 to +32	−0.3 to +32	−0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq 15V$ Ta = 25°C (One Amp)		Continuous	Continuous	Continuous	
Power Dissipation	P_D	570	570	570	mW
Operating Temperature Range	T_{opr}	−25 ~ +85	0 ~ +70	−40 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM224			LM324			LM2902			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_o = 1.4V, R_S = 0Ω		2.0	5.0		2.0	7.0		2.0	7.0	mV
Input Offset Current	I_{IO}			3	30		5	50		5	50	nA
Input Bias Current	I_{IB}			45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (V_{CC} = 26V for LM2902)	0		V_{CC} -1.5	0	V_{CC} -1.5		0		V_{CC} -1.5	V
Supply Current	I_{CC}	$R_L = \infty$ V_{CC} = 30V(all Amps) (V_{CC} = 26V for LM2902)		1.5	3		1.5	3		1.5	3	mA
		$R_L = \infty$ V_{CC} = 5V(all Amps)		0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$	50	100		25	100			100		V/mV
Output Voltage Swing	V_{OUT}	R_L = 2KΩ(LM2902, $R_L \geq 10K\Omega$)	0		V_{CC} -1.5	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Common-Mode Rejection Ratio	CMRR		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120			120		dB
Short Circuit to GND	I_{OS}			40	60		40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V	20	40		20	40		20	40		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V	10	20		10	20		10	20		mA
		V_{in+} = 0V, V_{in-} = 1V V_o = 200mV	12	50		12	50					μA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM224; and the $0°C \leq Ta \leq +70°C$ for the LM324; and the $-40°C \leq Ta \leq +85°C$ for the LM2902

Characteristic	Symbol	Test Conditions	LM224			LM324			LM2902			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V, V_o = 1.4V, R_S = 0Ω			7.0			9.0			10.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$			7.0			7.0			7.0		μV/°C
Input Offset Current	I_{IO}				100			150			200	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$			10			10			10		pA/°C
Input Bias Current	I_{IB}				300			500			500	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (LM2902: V_{CC} = 26V)	0		V_{CC} -2.0	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2.0K\Omega$ (for large V_o swing)	25			15			15			V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V, R_L = 2KΩ	26			26			22			V
	V_{OH}	V_{CC} = 26V for 2902, R_L = 10KΩ	27	28		27	28		23	24		V
	V_{OL}	V_{CC} = 5V, $R_L \leq 10K\Omega$		5	20		5	20		5	100	mV
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V, V_{CC} = 15V	10	20		10	20		10	20		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V, V_{CC} = 15V	10	15		5	8		5	8		mA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM224A			LM324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V R_S = 0		1.0	3.0		2.0	3.0	mV
Input Offset Current	I_{IO}			2	15		5	30	nA
Input Bias Current	I_{IB}			40	80		45	100	nA
Input Comm-Mode Voltage Range	V_{ICR}	V_{CC} = 30V	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current (All Amps)	I_{CC}	R_L = ∞ V_{CC} = 30V		1.5	3		1.5	3	mA
		R_L = ∞ V_{CC} = 5V		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V $R_L \geq 2K\Omega$	50	100		25	100		V/mV
Output Voltage Swing	V_{OUT}	R_L = 2KΩ	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I_{OS}			40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V V_{in-} = 0V V_{CC} = 15V	20	40		20	40		mA
	I_{sink}	V_{in+} = 0V V_{in-} = 1V V_{CC} = 15V	10	20		10	20		mA
		V_{in+} = 0V V_{in-} = 1V V_O = 200mV	12	50		12	50		μA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM224A; and the $0°C \leq Ta \leq +70°C$ for the LM324A

Characteristic	Symbol	Test Conditions	LM224A			LM324A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V R_S = 0Ω			4.0			5.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$			7.0	20		7.0	30	μV/°C
Input Offset Current	I_{IO}				30			75	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$			10	200		10	300	pA/°C
Input Bias Current	I_{IB}			40	100		40	200	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V $R_L \geq 2.0K\Omega$	25			15			V/mV
Output Voltage Swing	V_{OH} V_{OL}	V_{CC} = 30V R_L = 2KΩ	26			26			V
		R_L = 10KΩ	27	28		27	28		
		V_{CC} = 5V $R_L \leq 10K\Omega$		5	20		5	20	mV
Output Current	I_{source}	V_{in+} = 1V V_{in-} = 0V V_{CC} = 15V	10	20		10	20		mA
	I_{sink}	V_{in+} = 0V V_{in-} = 1V V_{CC} = 15V	5	8		5	8		mA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}	V

4

APPLICATION NOTE

The LM224 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger the V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case noninverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM224 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. in general, introducing a pseudo-ground (a bias voltage reference of $V_{CC}/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT VOLTAGE RANGE

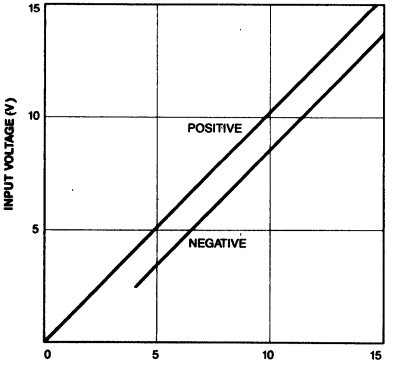


Fig. 1 POWER SUPPLY VOLTAGE (±V)

INPUT CURRENT

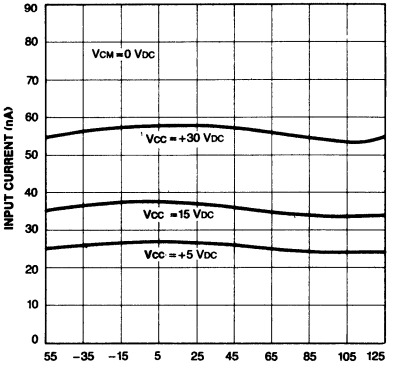


Fig. 2 TEMPERATURE (°C)

SUPPLY CURRENT

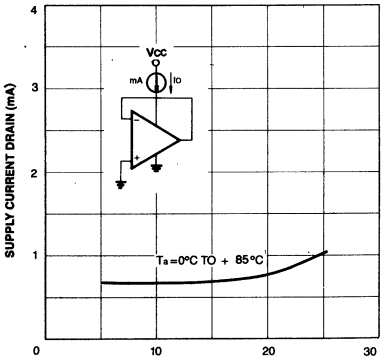


Fig. 3 SUPPLY VOLTAGE (V)

VOLTAGE GAIN

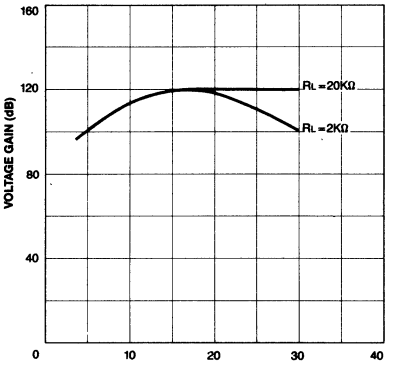


Fig. 4 SUPPLY VOLTAGE (V)

OPEN LOOP FREQUENCY RESPONSE

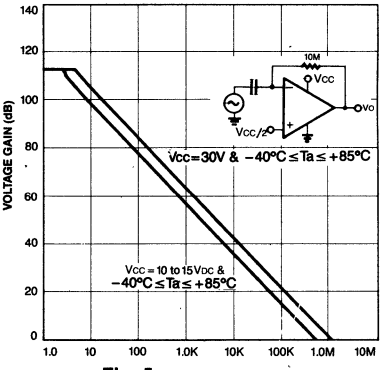


Fig. 5 FREQUENCY (Hz)

COMMON MODE REJECTION RATIO

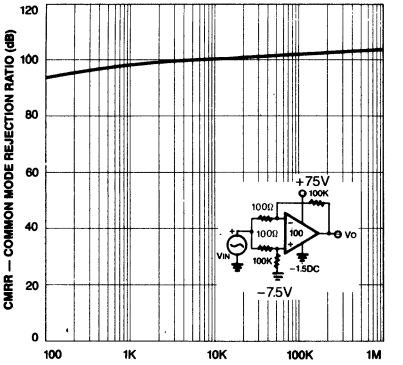


Fig. 6 FREQUENCY (Hz)

VOLTAGE FOLLOWER PULSE RESPONSE

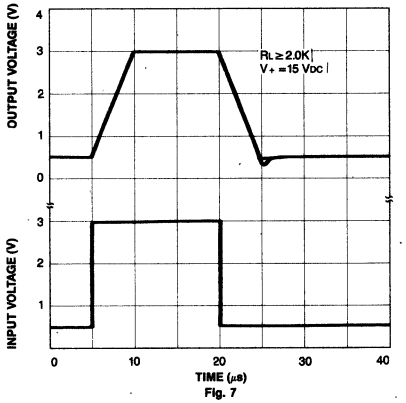


Fig. 7

VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

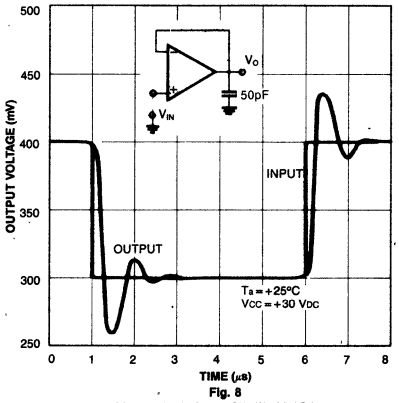


Fig. 8

LARGE SIGNAL FREQUENCY RESPONSE

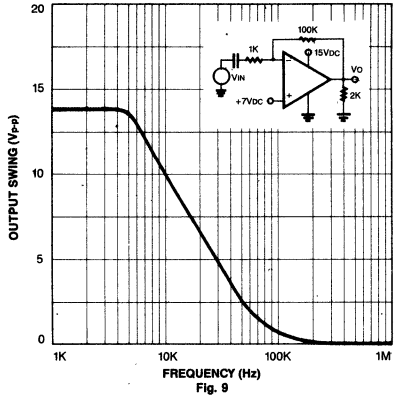


Fig. 9

OUTPUT CHARACTERISTICS CURRENT SOURCING

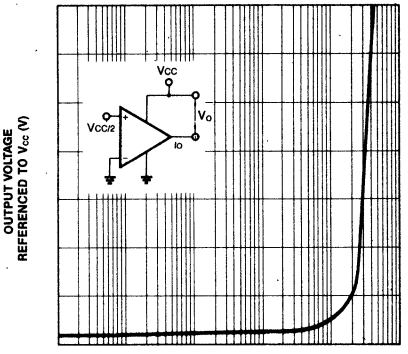


Fig. 10

OUTPUT CHARACTERISTICS CURRENT SINKING

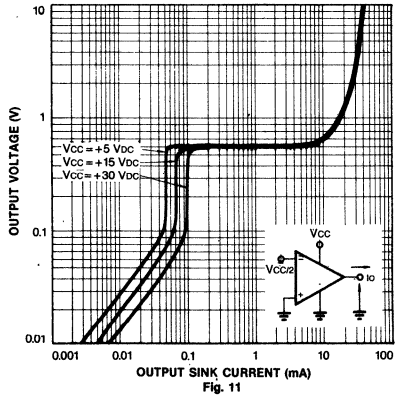


Fig. 11

CURRENT LIMITING

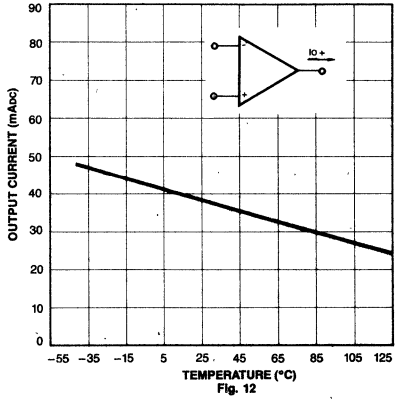


Fig. 12

TYPICAL APPLICATIONS (V_{CC} = 5.0V)

Voltage Reference

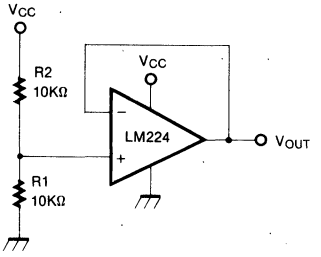


Fig. 13

Non-Inverting DC Gain

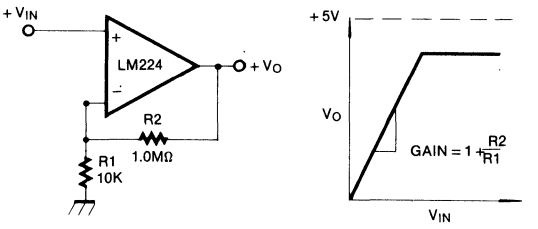


Fig. 14

AC Coupled Non-Inverting Amplifier

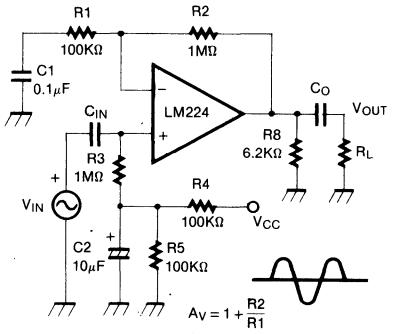


Fig. 15

Pulse Generator

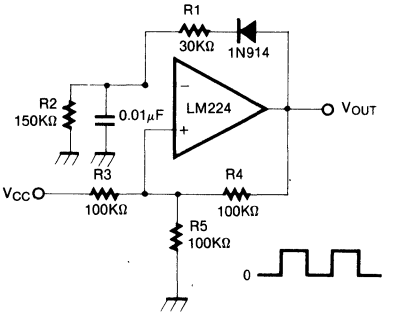
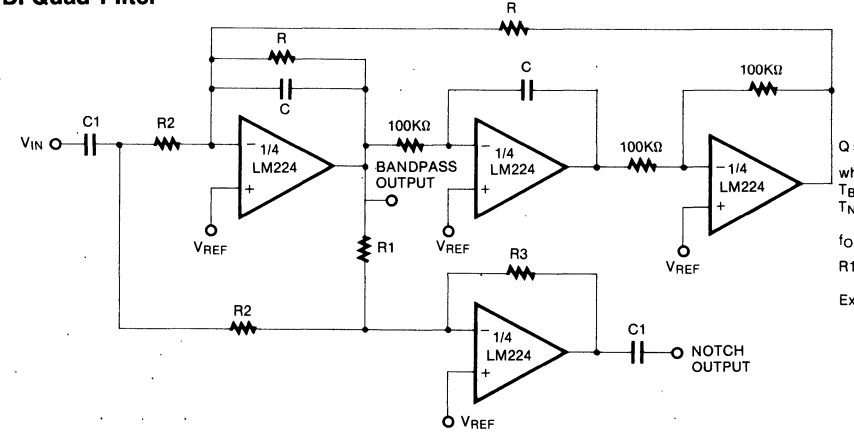


Fig. 16

Bi-Quad Filter



$Q = \frac{BW}{f_O}$

where

T_{BP} = Center frequency gain

T_N = Bandpass notch gain

$f_O = \frac{1}{2\pi RC}$ $R2 = \frac{R1}{T_{BP}}$

$R1 = QR$ $R3 = T_N R2$

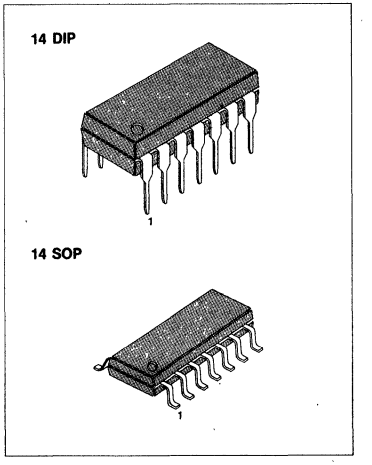
$C1 = 10C$

Example: f_O = 1000Hz
BW = 100Hz
T_{BP} = 1
T_N = 1
R = 160KΩ
R1 = 1.6MΩ
R2 = 1.6MΩ
R3 = 1.6MΩ
C = 0.01μF

Fig. 17

QUAD OPERATIONAL AMPLIFIERS

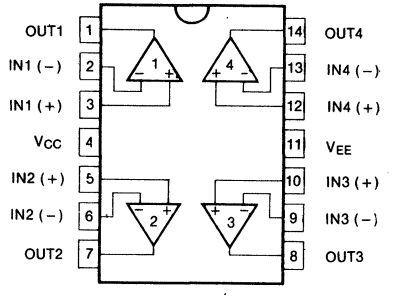
The LM248/LM348 is a true quad LM741. It consists of four independent, high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single LM741 type OP Amp. Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.



FEATURES

- **LM741 OP Amp operating characteristics**
- **Low supply current drain**
- **Class AB output stage-no crossover distortion**
- **Pin compatible with the LM324 & MC3403**
- **Low input offset voltage-1mV Typ.**
- **Low input offset current-4nA Typ.**
- **Low input bias current-30nA Typ.**
- **Gain bandwidth product for LM348 (unity gain)-1.0MHz Typ.**
- **Channel seperation 120dB**
- **Overload protection for outputs**

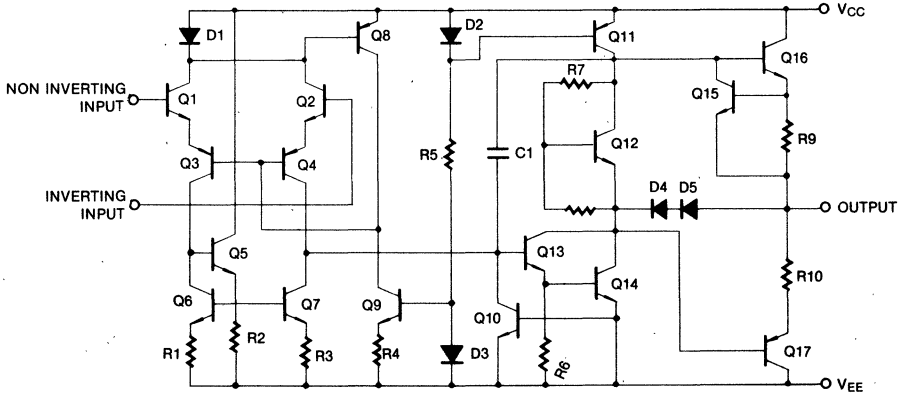
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM348N	14 DIP	0 ~ +70°C
LM348D	14 SOP	
LM248N	14 DIP	−25 ~ +85°C
LM248D	14 SOP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	±18	V
Differential Input Voltage	V_{ID}	±36	V
Input Voltage	V_I	±18	V
Output Short Circuit Duration		Continuous	
Operating Temperature LM248	T_{opr}	−25 ~ +85	°C
LM348		0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM248			LM348			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$		1.0	6.0		1.0	6.0	mV
		$T_{amin} \leq T_a \leq T_{amax}$			7.5			7.5	
Input Offset Current	I_{IO}			4	50		4	50	nA
		$T_{amin} \leq T_a \leq T_{amax}$			125			100	
Input Bias Current	I_{IB}			30	200		30	200	nA
		$T_{amin} \leq T_a \leq T_{amax}$			500			400	
Input Resistance	R_i		0.8	2.5		0.8	2.5		MΩ
Supply Current (all Amplifiers)	I_S			2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	A_V	$R_L \geq 2K\Omega$	25	160		25	160		V/mV
		$T_{amin} \leq T_a \leq T_{amax}$	15			15			
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Common Mode Input Voltage Range	V_{ICR}	$T_{amin} \leq T_a \leq T_{amax}$	±12			±12			V
Small Signal Bandwidth	BW	$A_V = 1$		1.0			1.0		MHz
Phase Margin	ϕ_m	$A_V = 1$		60			60		Degrees
Slew Rate	SR	$A_V = 1$		0.5			0.5		V/μs
Output Short Circuit Current	I_{OS}			25			25		mA
Output Voltage Swing	V_{OUT}	$R_L \geq 10K\Omega$, $T_{amin} \leq T_a \leq T_{amax}$	±12	±13		±12	±13		V
		$R_L \geq 2K\Omega$, $T_{amin} \leq T_a \leq T_{amax}$	±10	±12		±10	±12		
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K$, $T_{amin} \leq T_a \leq T_{amax}$	70	90		70	90		dB
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10K$, $T_{amin} \leq T_a \leq T_{amax}$	77	96		77	96		dB

* $T_{amin} \leq T_a \leq T_{amax}$
LM248: T_{amin} = −25°C, T_{amax} = +85°C
LM348: T_{amin} = 0°C, T_{amax} = +70°C

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT

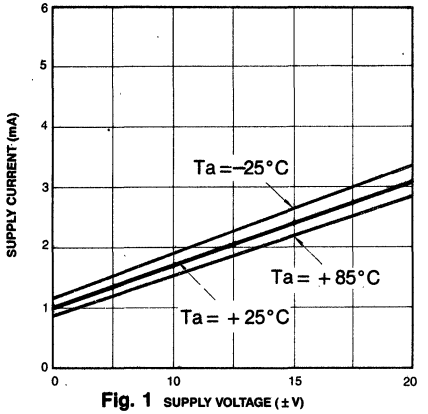


Fig. 1 SUPPLY VOLTAGE (±V)

VOLTAGE SWING

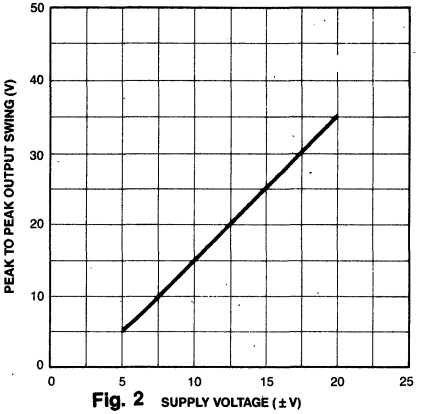


Fig. 2 SUPPLY VOLTAGE (±V)

SOURCE CURRENT LIMIT

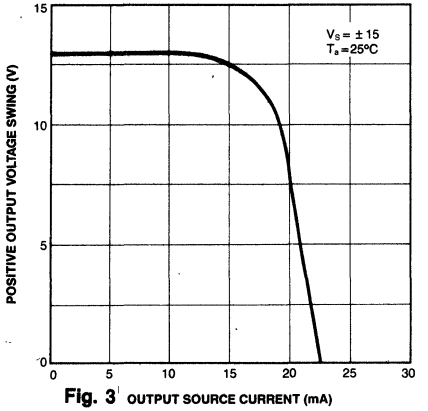


Fig. 3 OUTPUT SOURCE CURRENT (mA)

SINK CURRENT LIMIT

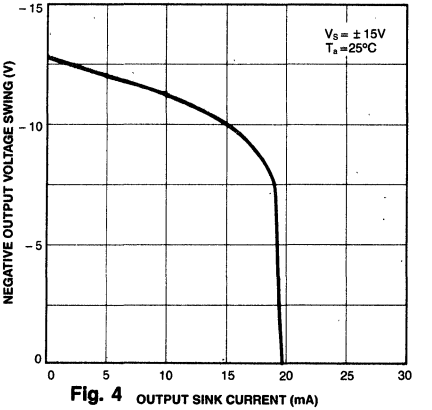


Fig. 4 OUTPUT SINK CURRENT (mA)

OUTPUT IMPEDANCE

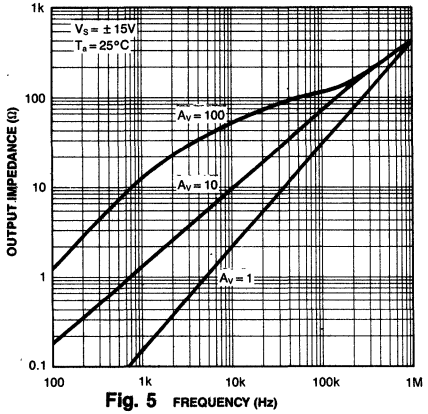


Fig. 5 FREQUENCY (Hz)

COMMON-MODE REJECTION RATIO

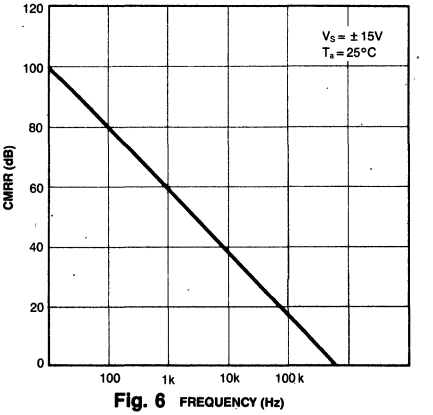


Fig. 6 FREQUENCY (Hz)

OPEN LOOP FREQUENCY RESPONSE

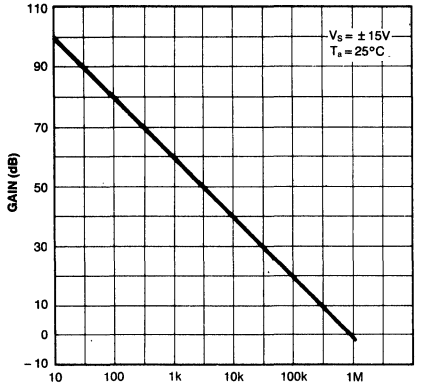


Fig. 7 FREQUENCY (Hz)

BODE PLOT

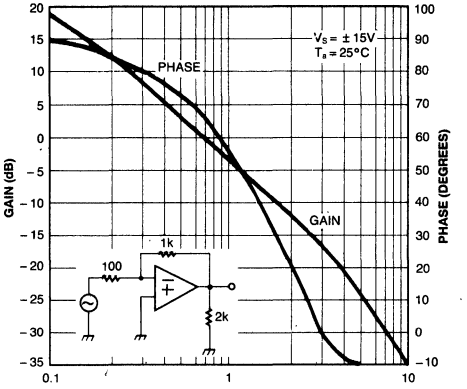


Fig. 8 FREQUENCY (MHz)

LARGE SIGNAL PULSE RESPONSE

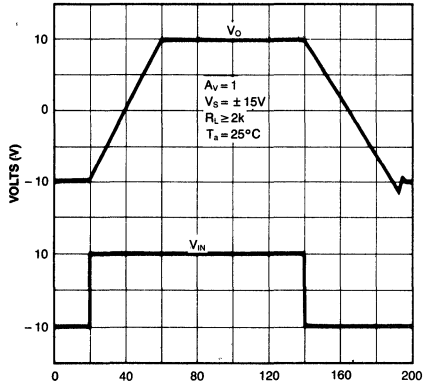


Fig. 9 TIME (μs)

SMALL SIGNAL PULSE RESPONSE

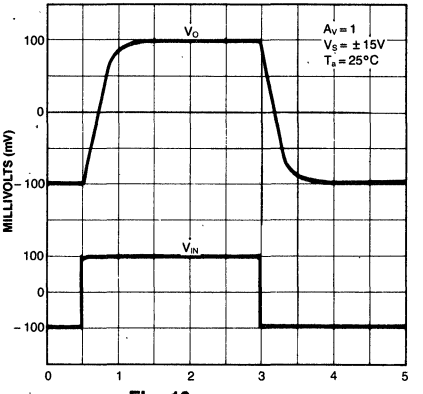


Fig. 10 TIME (μs)

UNDISTORTED OUTPUT VOLTAGE SWING

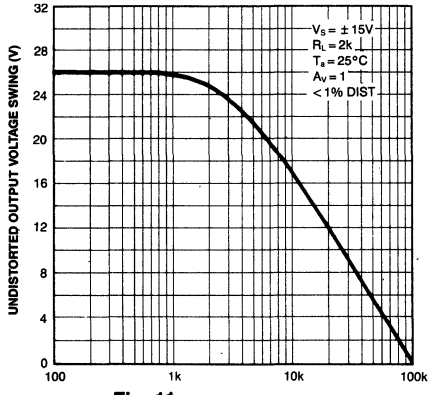


Fig. 11 FREQUENCY (Hz)

INVERTING LARGE SIGNAL PULSE RESPONSE

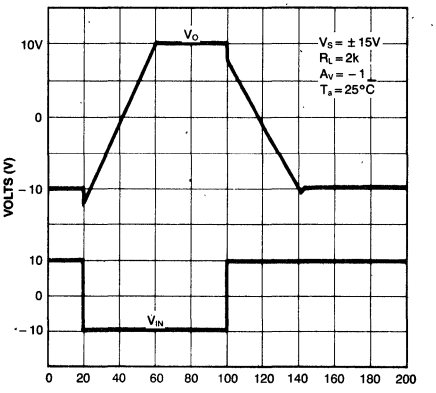


Fig. 12 TIME (μs)

INPUT NOISE VOLTAGE AND NOISE CURRENT

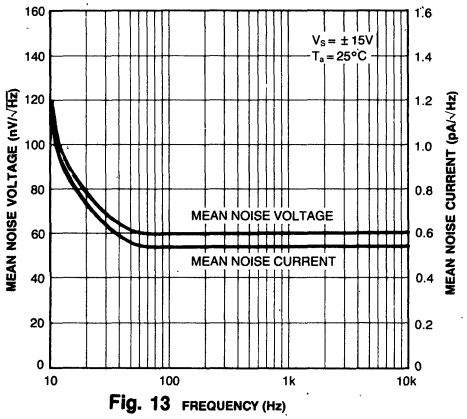


Fig. 13 FREQUENCY (Hz)

POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

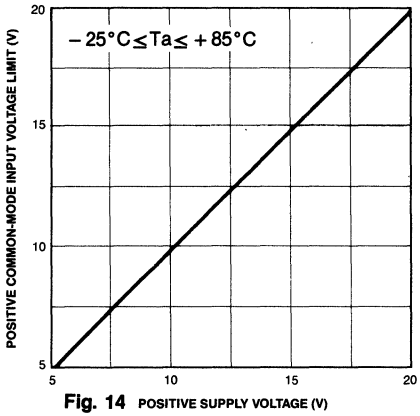


Fig. 14 POSITIVE SUPPLY VOLTAGE (V)

NEGATIVE COMMON — MODE INPUT VOLTAGE LIMIT

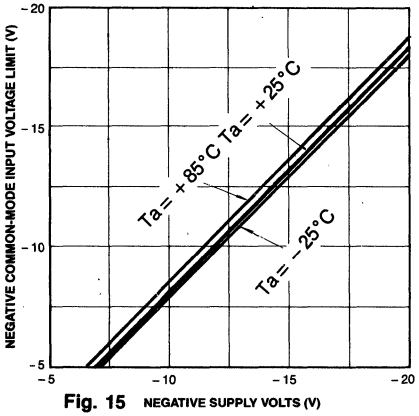


Fig. 15 NEGATIVE SUPPLY VOLTS (V)

TYPICAL APPLICATIONS

Function Generator

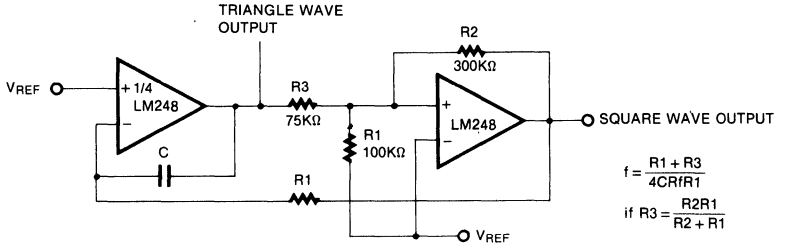


Fig. 16

Bi-Quad Filter

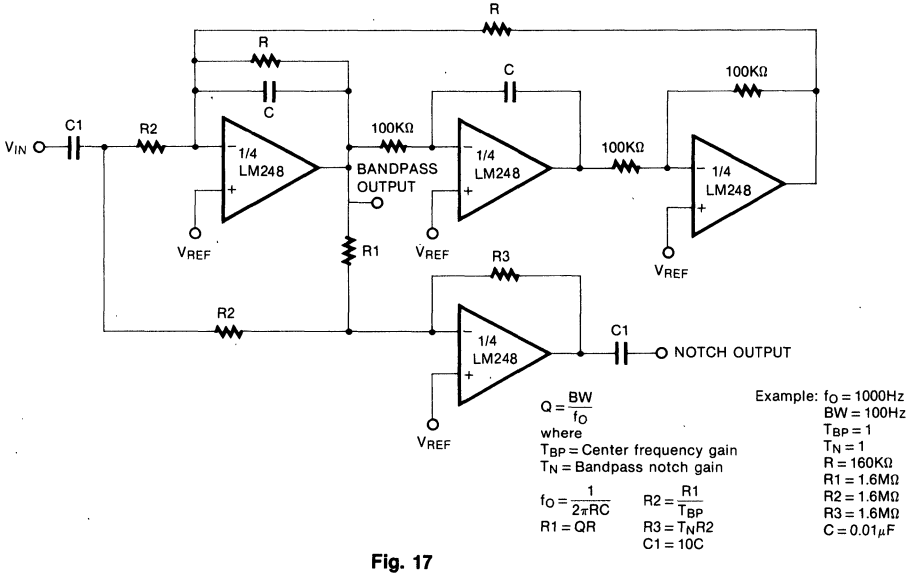


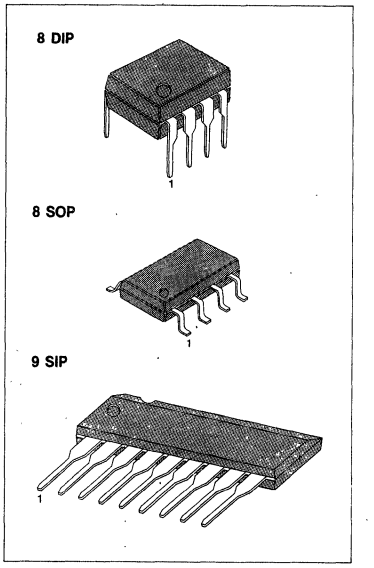
Fig. 17

QUAD OPERATIONAL AMPLIFIERS

The LM258 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

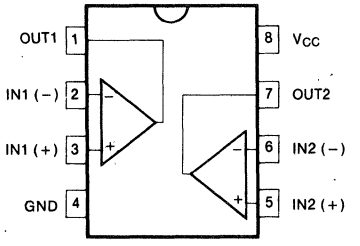
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

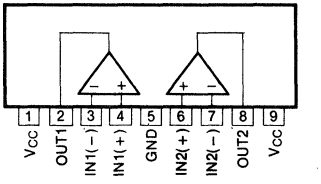


FEATURES

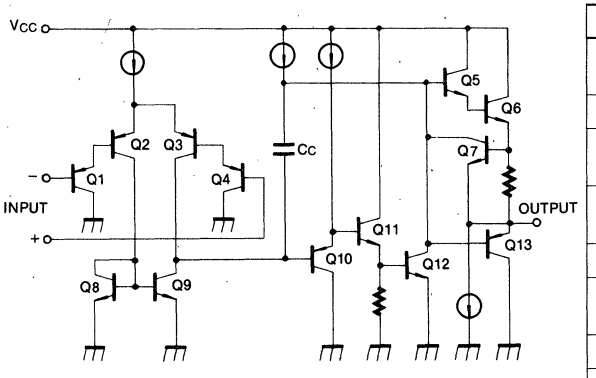
- **Internally frequency compensated**
- **Large DC voltage gain: 100dB**
- **Wide power supply range: LM258/A, LM358/A: 3V ~ 32V (or ± 1.5V ~ 16V)**
  LM2904: 3V ~ 26V (or ± 1.5V ~ 13V)
- **Input common-mode voltage range includes ground**
- **Large output voltage swing: 0V DC to V_{CC} – 1.5V DC**
- **Power drain suitable for battery operation.**

BLOCK DIAGRAM





SCHEMATIC DIAGRAM (One section only)



ORDERING INFORMATION

Device	Package	Operating Temperatur
LM358N LM358AN	8 DIP	0 ~ +70°C
LM358S	9 SIP	
LM358D LM358AD	8 SOP	
LM258N LM258AN	8 DIP	– 25 ~ +85°C
LM258S	9 SIP	
LM258D LM258AD	8 SOP	
LM2904N	8 DIP	– 40 ~ +85°C
LM2904D	8 SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM258/LM258A	LM358/LM358A	LM2904	Unit
Power Supply Voltage	V_S	±16 or 32	±16 or 32	±13 or 26	V
Differential Input Voltage	V_{ID}	±32	±32	±26	V
Input Voltage	V_I	−0.3 to +32	−0.3 to +32	−0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq 15V$ Ta = 25°C (One Amp)		Continuous	Continuous	Continuous	
Operating Temperature Range	T_{opr}	−25 ~ +85	0 ~ +70	−40 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM258			LM358			LM2904			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_S = 0Ω		±2.0	±5.0		±2.0	±7.0		±2.0	±7.0	mV
Input Offset Current	I_{IO}			±3	±30		±5	±50		±5	±50	nA
Input Bias Current	I_{IB}			45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (LM2904, V_{CC} = 26V)	0		V_{CC} -1.5	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	$R_L = \infty$ V_{CC} = 30V (LM2902, V_{CC} = 26V)		1.0	2.0		1.0	2.0		1.0	2.0	mA
		$R_L = \infty$ over full temperature range		0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$	50	100		25	100			100		V/mV
Output Voltage Swing	V_{OUT}	R_L = 2KΩ (LM2904, $R_L \geq 10K\Omega$)	0		V_{CC} -1.5	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Common-Mode Rejection Ratio	CMRR		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120			120		dB
Short Circuit to GND	I_{OS}			40	60		40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V, V_{CC} = 15V	20	40		20	40		20	40		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V, V_{CC} = 15V	10	20		10	20		10	20		mA
		V_{in+} = 0V, V_{in-} = 1V, V_o = 200mV	12	50		12	50					μA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM258; and the $0°C \leq Ta \leq +70°C$ for the LM358; and the $-40°C \leq Ta \leq +85°C$ for the LM2904

Characteristic	Symbol	Test Conditions	LM258			LM358			LM2904			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_o = 1.4V, R_S = 0			±7.0			±9.0			±10.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	R_S = 0Ω		7.0			7.0			7.0		μV/°C
Input Offset Current	I_{IO}				±100			±150		±45	±200	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$			10			10			10		pA/°C
Input Bias Current	I_{IB}			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (LM2904, V_{CC} = 26V)	0		V_{CC} -2.0	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2.0K\Omega$	25			15			15			V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V R_L = 2KΩ	26			26			22			V
		V_{CC} = 26V for 2904 R_L = 10KΩ	27	28		27	28		23	24		
	V_{OL}	V_{CC} = 5V $R_L \leq 10K\Omega$		5	20		5	20		5	100	mV
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V	10	20		10	20		10	20		mA
	I_{sink}	V_{in+} = 0V V_{in-} = 1V V_{CC} = 15V	5	8		5	8		5	8		mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM258A			LM358A			
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V R_S = 0		1.0	3.0		2.0	3.0	mV
Input Offset Current	I_{IO}			2	15		5	30	nA
Input Bias Current	I_{IB}			40	80		45	100	nA
Input Comm-Mode Voltage Range	V_{ICR}	V_{CC} = 30V	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞ V_{CC} = 30V		1.0	2.0		1.0	2.0	mA
		R_L = ∞ over full temperature range		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V $R_L \geq 2K\Omega$	50	100		25	100		V/mV
Output Voltage Swing	V_{OUT}	R_L = 2KΩ	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I_{OS}			40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V V_{in-} = 0V V_{CC} = 15V	20	40		20	40		mA
	I_{sink}	V_{in+} = 0V V_{in-} = 1V V_{CC} = 15V	10	20		10	20		mA
		V_{in+} = 0V V_{in-} = 1V V_O = 200mV	12	50		12	50		mA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}	V

4

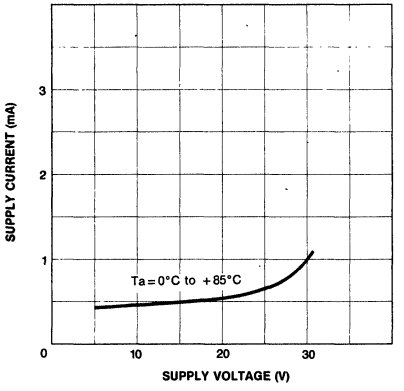
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)

The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM258A; and the $0°C \leq Ta \leq +70°C$ for the LM358A

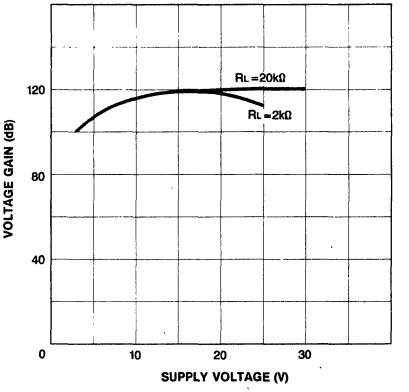
Characteristic	Symbol	Test Conditions	LM258A			LM358A			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V o V_{CC}-1.5V V_O = 1.4V R_S = 0Ω			4.0			5.0	mV
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$	R_S = 0Ω		7.0	15		7.0	20	μV/°C
Input Offset Current	I_{IO}				30			75	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$			10	200		10	300	PA/°C
Input Bias Current	I_{IB}			40	100		40	200	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V $R_L \geq 2.0K\Omega$	25			15			V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V R_L = 20KΩ	26			26			V
		R_L = 10KΩ	27	28		27	28		V
	V_{OL}	V_{CC} = 5V $R_L \leq 10K\Omega$		5	20		5	20	mV
Output Current	I_{source}	V_{in+} = 1V V_{in-} = 0V V_{CC} = 15V	10	20		10	20		mA
	I_{sink}	V_{in+} = 0V V_{in-} = 1V V_{CC} = 15V	5	8		5	8		mA
Differential Input Voltage	V_{ID}				V_{CC}			V_{CC}	V

TYPICAL PERFORMANCE CHARACTERISTICS

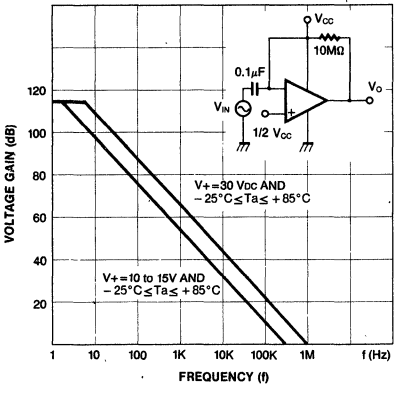
SUPPLY CURRENT



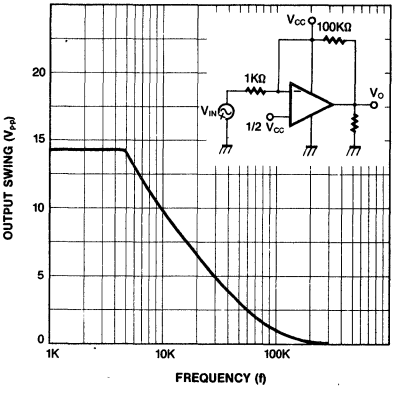
VOLTAGE GAIN



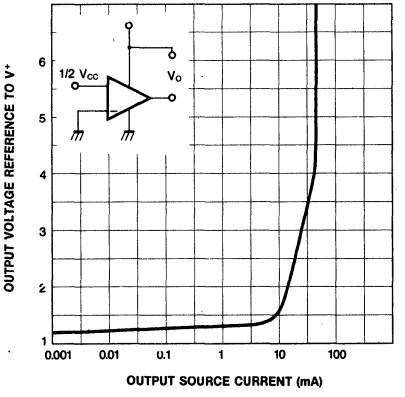
OPEN LOOP FREQUENCY RESPONSE



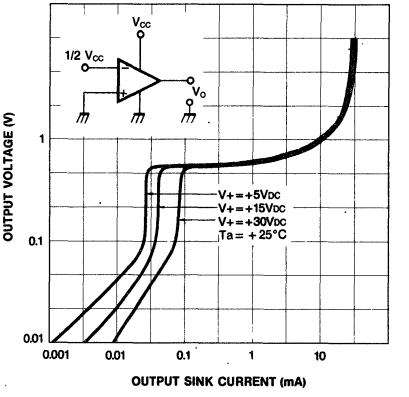
LARGE SIGNAL FREQUENCY RESPONSE



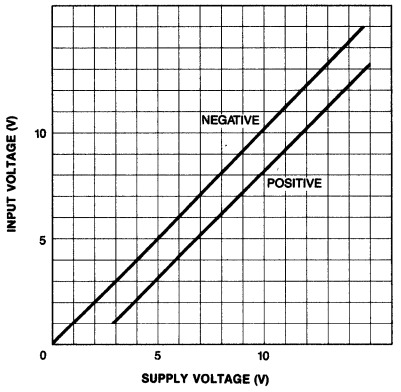
OUTPUT CURRENT SOURCE



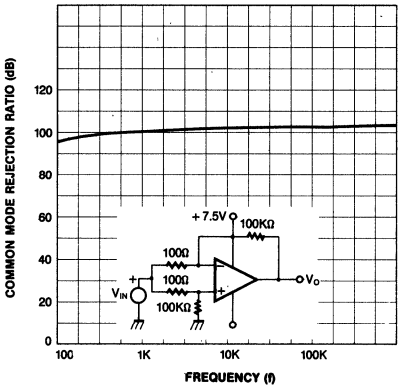
OUTPUT SINK CURRENT



INPUT COMMON-MODE VOLTAGE RANGE

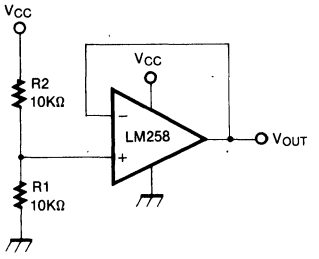


COMMON-MODE REJECTION RATIO

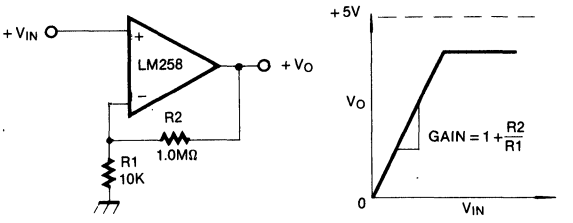


TYPICAL APPLICATIONS (V_{CC} = 5.0V)

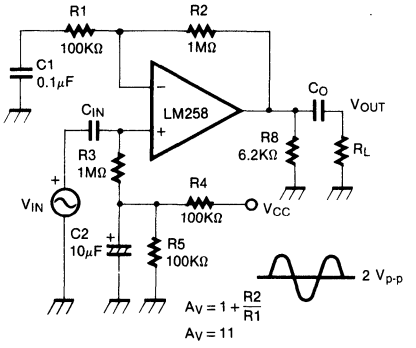
Voltage Reference



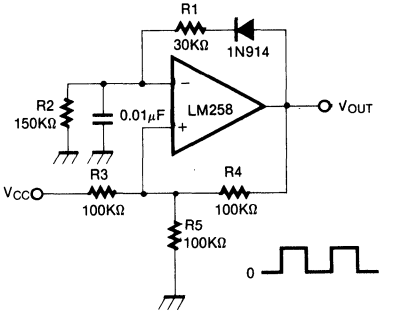
Non-Inverting DC Gain



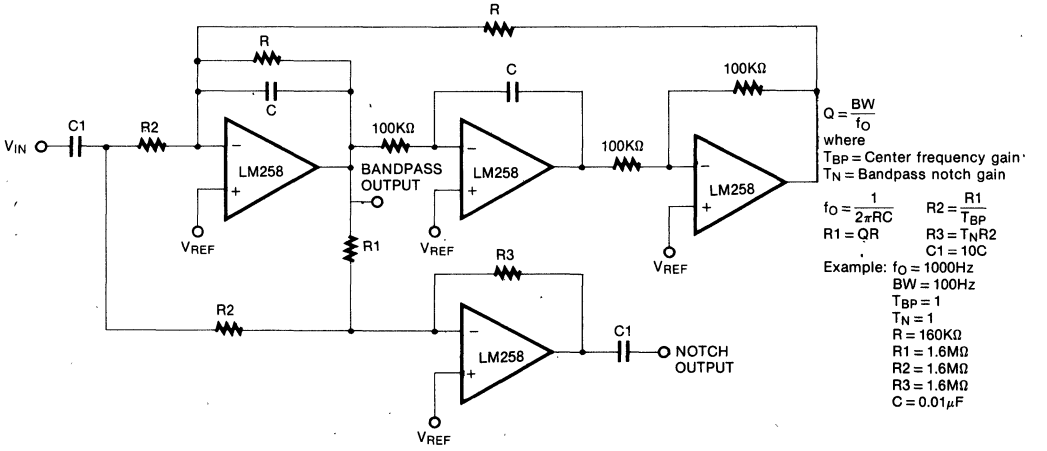
AC Coupled Non-Inverting Amplifier



Pulse Generator



Bi-Quad Filter



$Q = \frac{BW}{f_O}$

where

T_{BP} = Center frequency gain

T_N = Bandpass notch gain

$f_O = \frac{1}{2\pi RC}$ $R2 = \frac{R1}{T_{BP}}$

$R1 = QR$ $R3 = T_N R2$

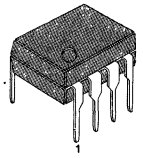
$C1 = 10C$

Example: f_O = 1000Hz
BW = 100Hz
T_{BP} = 1
T_N = 1
R = 160KΩ
R1 = 1.6MΩ
R2 = 1.6MΩ
R3 = 1.6MΩ
C = 0.01μF

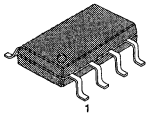
SINGLE OPERATIONAL AMPLIFIERS

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications.
The high gain and wide range of operating voltage provide superior performance in intergrator, summing amplifier, and general feedback applications.

8 DIP



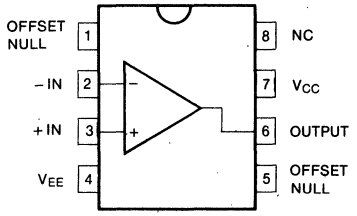
8 SOP



FEATURES

- **Short circuit protection**
- **Excellent temperature stability**
- **Internal frequency compensation**
- **High input voltage range**
- **Null of offset**

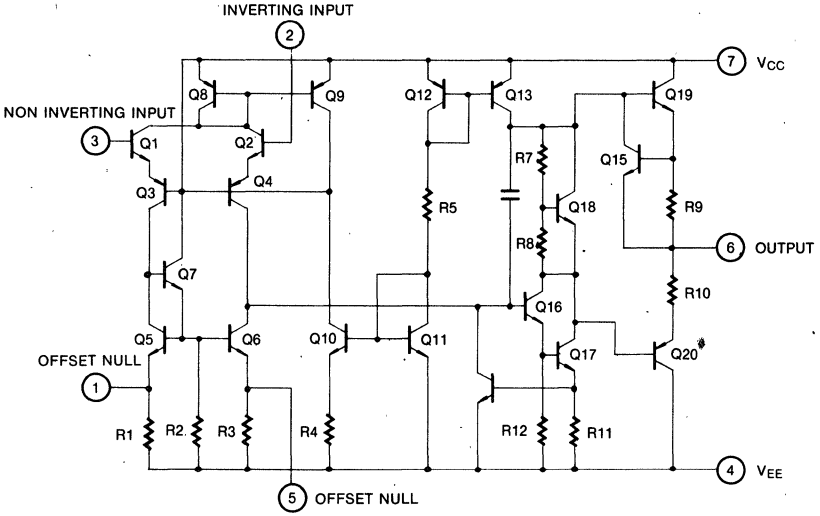
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM741EN LM741CN	8 DIP	0 ~ +70°C
LM741ED LM741CD	8 SOP	
LM741IN	8 DIP	-40 ~ +85°C
LM741ID	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	LM741C	LM741E	LM741I	Unit
Power Supply Voltage	V_S	±18	±22	±18	V
Differential Input Voltage	V_{ID}	±30	±30	±30	V
Input Voltage	V_I	±15	±15	±15	V
Output Short Circuit Duration		Indefinite	Indefinite	Indefinite	
Power Dissipation	P_D	500	500	500	mW
Operating Temperature Range	T_{opr}	0 ~ +70	0 ~ +70	−40 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	−65 ~ +150	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM741E			LM741C/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$						2.0	6.0	mV
		$R_S \leq 50\Omega$			0.8	3.0				
Input Offset Voltage Adjustment Range	V_{IOR}	$V_S = \pm 20V$		±10				±15		mV
Input Offset Current	I_{IO}				3.0	30		20	200	nA
Input Bias Current	I_{IB}				30	80		80	500	nA
Input Resistance	R_i	$V_S = \pm 20V$		1.0	6.0		0.3	2.0		MΩ
Input Voltage Range	V_{ICR}			±12	±13		±12	±13		V
Large Signal Voltage Gain	A_V	$R_L \geq 2K\Omega$	$V_S = \pm 20V$, $V_O = \pm 15V$	50						V/mV
			$V_S = \pm 15V$, $V_O = \pm 10V$				20	200		
Output Short Circuit Current	I_{OS}			10	25	35		25		mA
Output Voltage Swing	V_{OUT}	$V_S = \pm 20V$	$R_L \geq 10K\Omega$	±16						V
			$R_L \geq 2K\Omega$	±15						
		$V_S = \pm 15V$	$R_L \geq 10K\Omega$				±12	±14		
			$R_L \geq 2K\Omega$				±10	±13		
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$, $V_{CM} = \pm 12V$					70	90		dB
		$R_S \leq 50K\Omega$, $V_{CM} = \pm 12V$		80	95					
Power Supply Rejection Ratio	PSRR	$V_S = \pm 20V$ to $V_S = \pm 5V$, $R_S \leq 50\Omega$		80	96					dB
		$V_S = \pm 15V$ to $V_S = \pm 5V$, $R_S \leq 10K\Omega$					77	96		

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Test Conditions	LM741E			LM741C/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Transient Response	Rise Time	t_r	Unity Gain		0.25	0.8		0.3		μs
	Overshoot	OS			6.0	20		5		%
Bandwidth		BW		0.43	1.5			1.0		MHz
Slew Rate		SR	Unity Gain	0.3	0.7			0.5		V/μs
Supply Current		I_S	$R_L = \infty\ \Omega$					1.7	2.8	mA
Power Consumption		P_C	$V_S = \pm 20V$		80	150				mW
			$V_S = \pm 15V$					50	85	

ELECTRICAL CHARACTERISTICS

($-25°C \leq Ta \leq 85°C$ for the LM7411, $0°C \leq Ta \leq 70°C$ for the LM741C, LM741E, $V_{CC} = +15V$, $V_{EE} = -15V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM741E			LM741C/LM741I			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 50\Omega$				4.0				mV
		$R_S \leq 10K\Omega$							7.5	
Input Offset Voltage Drift	$\triangle V_{IO}/\triangle T$				15					μV/°C
Input Offset Current	I_{IO}					70			300	nA
Input Offset Current Drift	$\triangle I_{IO}/\triangle T$					0.5				nA/°C
Input Bias Current	I_{IB}					0.21			0.8	nA
Input Resistance	R_i	$V_S = \pm 20V$		0.5						MΩ
Input Voltage Range	V_{ICR}			±12	±13		±12	±13		V
Output Voltage Swing	V_{OUT}	$V_S = \pm 20V$	$R_L \geq 10K\Omega$	±16						V
			$R_L \geq 2K\Omega$	±15						
		$V_S = \pm 15V$	$R_L \geq 10K\Omega$				±12	±14		
			$R_L \geq 2K\Omega$				±10	±13		
Output Short Circuit Current	I_{OS}			10		40				mA
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$, $V_{CM} = \pm 12V$					70	90		dB
		$R_S \leq 50K\Omega$, $V_{CM} = \pm 12V$		80	95					
Power Supply Rejection Ratio	PSRR	$V_S = \pm 20V$ to $\pm 5V$	$R_S \leq 50\Omega$	86	96					dB
			$R_S \leq 10K\Omega$				77	96		
Large Signal Voltage Gain	A_V	$R_L \geq 2K\Omega$	$V_S = \pm 20V$, $V_o = \pm 15V$	32						V/mV
			$V_S = \pm 15V$, $V_O = \pm 10V$					15		
			$V_S = \pm 15$, $V_O = 2V$	10						

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

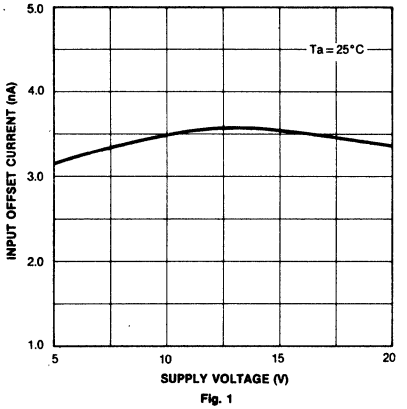


Fig. 1

POWER CONSUMPTION vs SUPPLY VOLTAGE

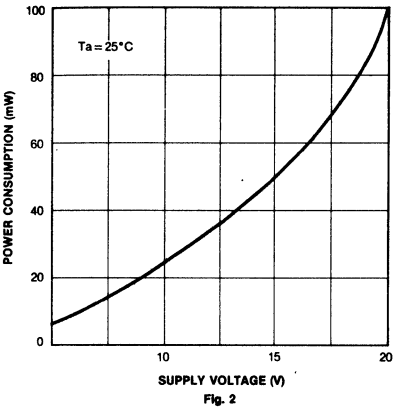


Fig. 2

OPEN LOOP VOLTAGE GAIN vs FREQUENCY

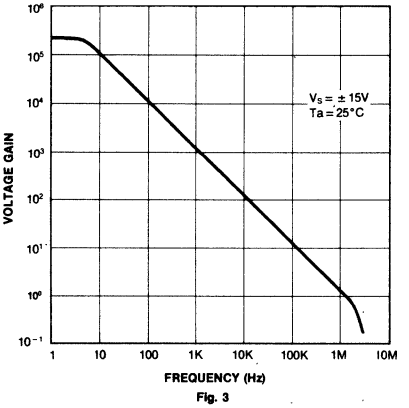


Fig. 3

OPEN LOOP PHASE RESPONSE vs FREQUENCY

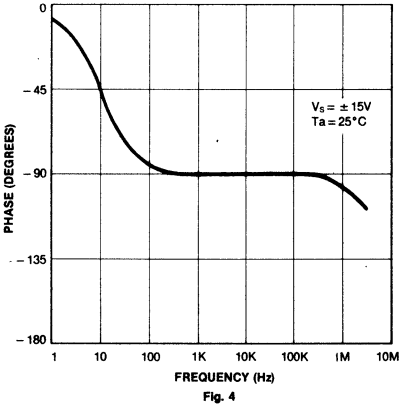


Fig. 4

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

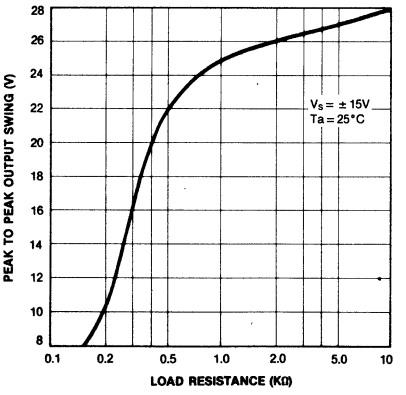


Fig. 5

OUTPUT VOLTAGE SWING vs FREQUENCY

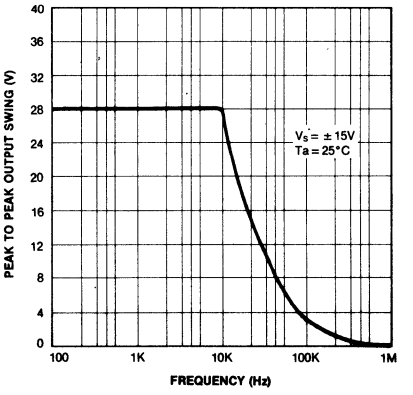


Fig. 6

OUTPUT RESISTANCE vs FREQUENCY

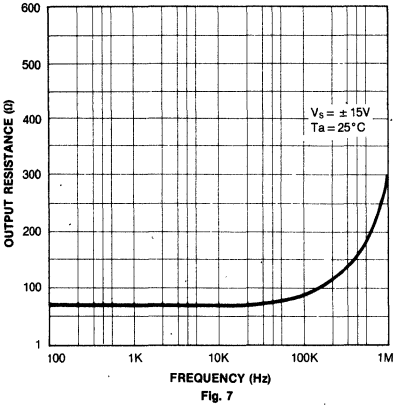


Fig. 7

INPUT RESISTANCE AND INPUT CAPACITANCE vs FREQUENCY

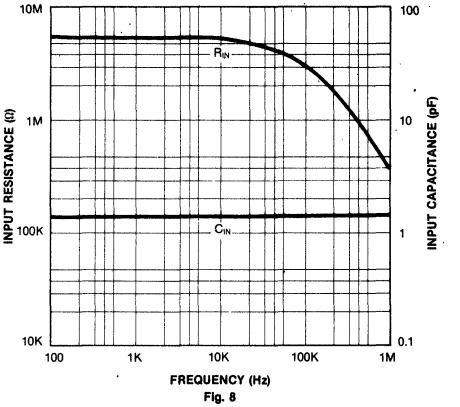


Fig. 8

INPUT BIAS CURRENT vs AMBIENT TEMPERATURE

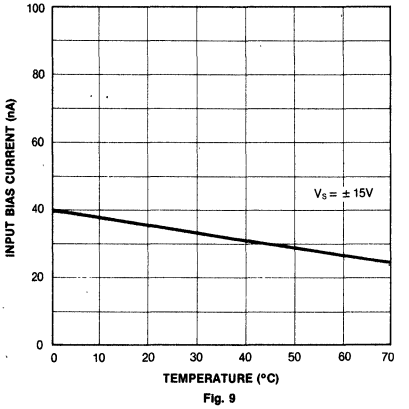


Fig. 9

INPUT RESISTANCE vs AMBIENT TEMPERATURE

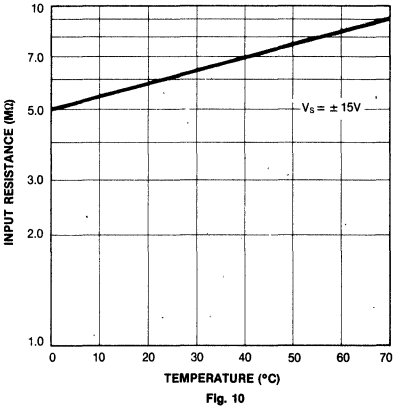


Fig. 10

INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE

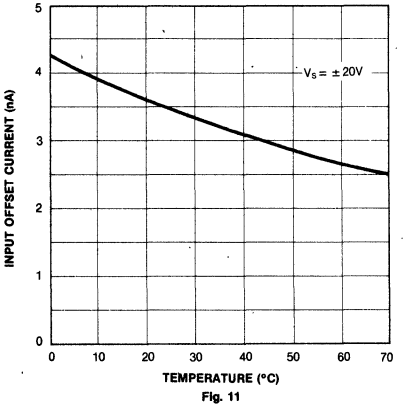


Fig. 11

POWER CONSUMPTION vs AMBIENT TEMPERATURE

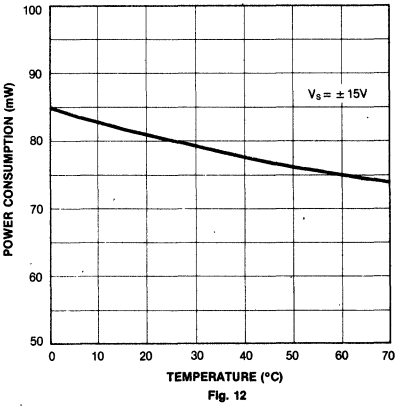


Fig. 12

OUTPUT SHORT CIRCUIT CURRENT
vs AMBIENT TEMPERATURE

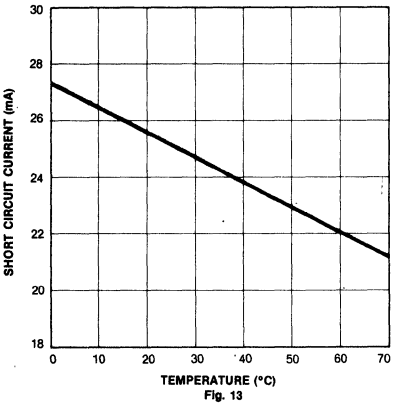


Fig. 13

TRANSIENT RESPONSE

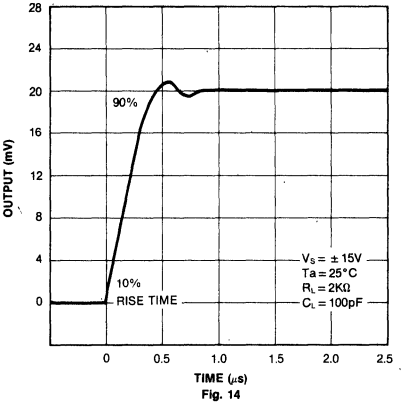


Fig. 14

VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE

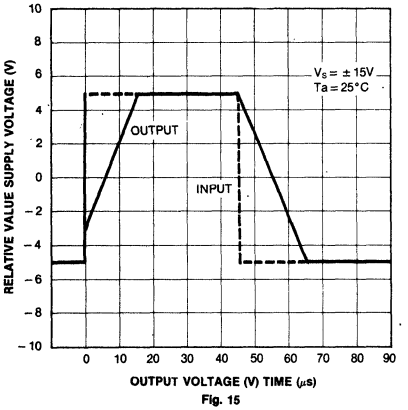


Fig. 15

COMMON MODE REJECTION RATIO
vs FREQUENCY

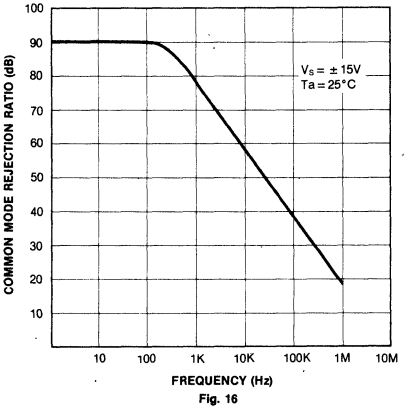
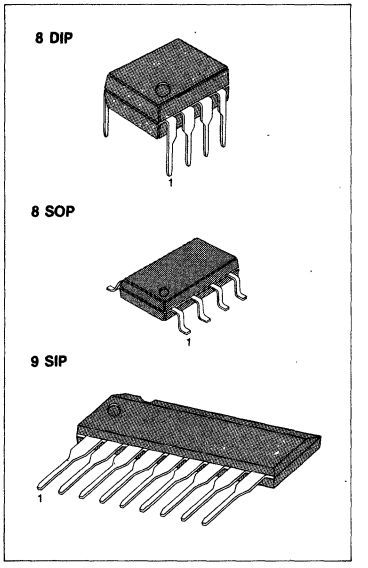


Fig. 16

4

DUAL OPERATIONAL AMPLIFIERS

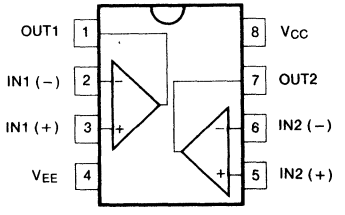
The MC1458 series is a dual general purpose operational amplifier. The MC1458 series is a short circuit protected and require no external components for frequency compensation.
High common mode voltage range and absence of "latch up" make the MC1458 ideal for use as voltage followers.
The high gain and wide range of operating voltage provides superior performance in intergrator, summing amplifier and general feedback applications.

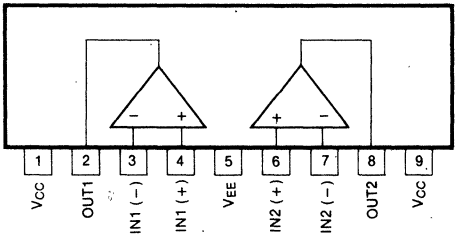


FEATURES

- **Interal frequency compensation**
- **Short circuit protection**
- **Large common mode and differential voltage range**
- **No latch up**
- **Low power consumption**

BLOCK DIAGRAM

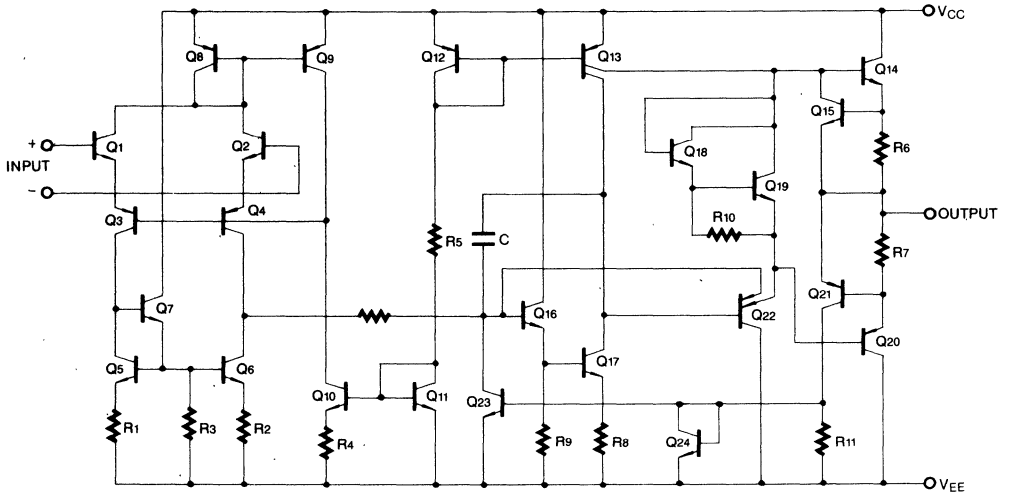




ORDERING INFORMATION

Device	Package	Operating Temperature
MC1458CN MC1458N	8 DIP	0 ~ +70°C
MC1458S	9 SIP	
MC1458D MC1458CD	8 SOP	0 ~ +70°C
MC1458IN	8 DIP	−25 ~ +85°C
MC1458ID	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_S	± 18	V
Input Differential Voltage	V_{ID}	± 30	V
Input Voltage	V_I	± 15	V
Operating Temperature Range MC1458I	T_{opr}	− 25 ~ + 85	°C
MC1458/C		0 ~ + 70	°C
Storage Temperature Range	T_{stg}	− 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

($V_S = \pm 15V$, $Ta = 25°C$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC1458/MC1458I			MC1458C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$		2.0	6.0		2.0	10	mV
Input Offset Current	I_{IO}			20	200		20	300	nA
Input Bias Current	I_{IB}			80	500		80	700	nA
Large Signal Voltage Gain	A_V	$V_o = \pm 10V$, $R_L \geq 2.0K\Omega$	20	100		20	100		V/mV
Input Voltage Range	V_{ICR}		± 12	± 13		± 11	± 13		V
Input Resistance	R_I		0.3	1.0			1.0		MΩ
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$	70	90		60	90		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10K\Omega$	77	90		77	90		dB
Supply Current (Both Amplifier)	I_S			2.3	5.6		2.3	8.0	mA
Output Voltage Swing	V_{OUT}	$R_L = 10K\Omega$	± 12	± 14		± 11	± 14		V
		$R_L = 2K\Omega$	± 10	± 13		± 9	± 13		
Output Short Circuit Current	I_{OS}			20			20		mA
Power Consumption	P_C	$V_o = 0V$		70	170		70	240	mA
Transient Response (Unity Gain)									
Rise Time	t_r	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$		0.3			0.3		μs
Overshoot	OS	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$		15			15		%
Slew Rate	SR	$V_i = 10V$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$		0.8			0.8		$V/\mu s$

ELECTRICAL CHARACTERISTICS

($T_{amin} \leq T_a \leq T_{amax}$, $V_S = \pm 15V$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC1458/MC1458I			MC1458C			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$			7.5			12	mV
Input Offset Current	I_{IO}				300			400	nA
Input Bias Current	I_{IB}				800			1000	nA
Large Signal Voltage Gain	A_V	$V_o = \pm 10V$, $R_L \geq 2.0K$	15			15			V/mV
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K$	70	90		70	90		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10K$	77	90		77	90		dB
Output Voltage Swing	V_{OUT}	$R_L = 10K$	± 12	± 14		± 11	± 14		V
		$R_L = 2K$	± 10	± 13		± 9	± 13		
Input Voltage Range	V_{ICR}		± 12			± 12			V

* $T_{amin} \leq T_a \leq T_{amax}$
MC1458I: $T_{amin} = -25°C$, $T_{amax} = +85°C$
MC4558/C: $T_{amin} = 0°C$, $T_{amax} = 70°C$

TYPICAL PERFORMANCE CHARACTERISTICS

OPEN-LOOP VOLTAGE GAIN vs POWER SUPPLY VOLTAGES

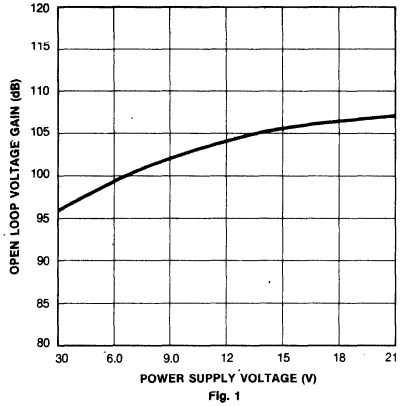


Fig. 1

OPEN-LOOP FREQUENCY RESPONSE

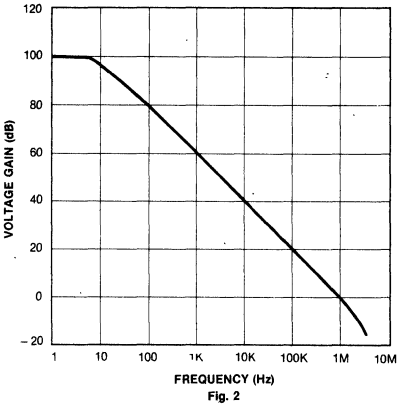


Fig. 2

POWER BANDWIDTH (LARGE SIGNAL SWING vs FREQUENCY)

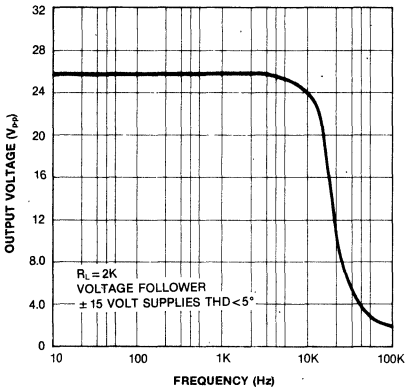


Fig. 3

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

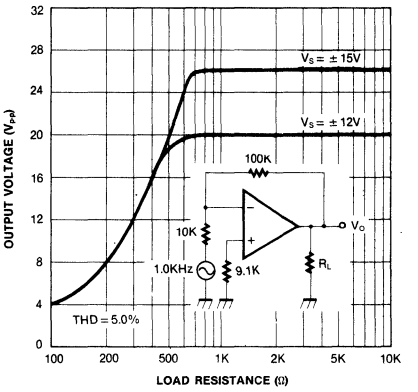
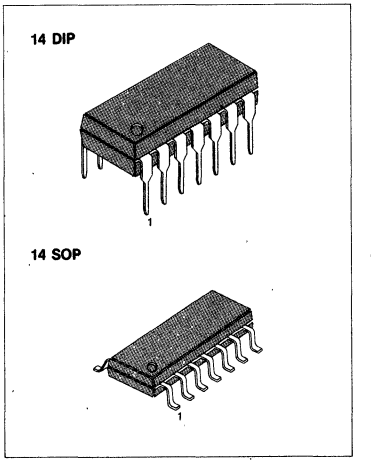


Fig. 4

QUAD OPERATIONAL AMPLIFIER

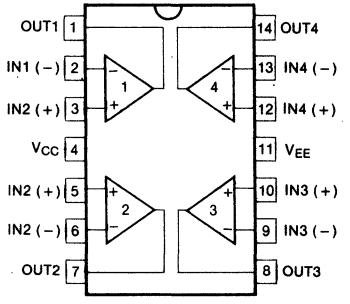
The MC3303 series is a monolithic Quad operational amplifier consisting of four independent amplifiers. The device has high gain, internally frequency, compensated operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common made input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.



FEATURES

- **Output voltage can swing to GND or negative supply**
- **Wide power supply range;**
  Single supply of 3.0V to 36V
  Dual supply of ±1.5V to ±18V
- **Electrical characteristics similar to the popular LM741**
- ***CLASS AB output stage for minimal crossover distortion***
- **Short circuit protected output.**

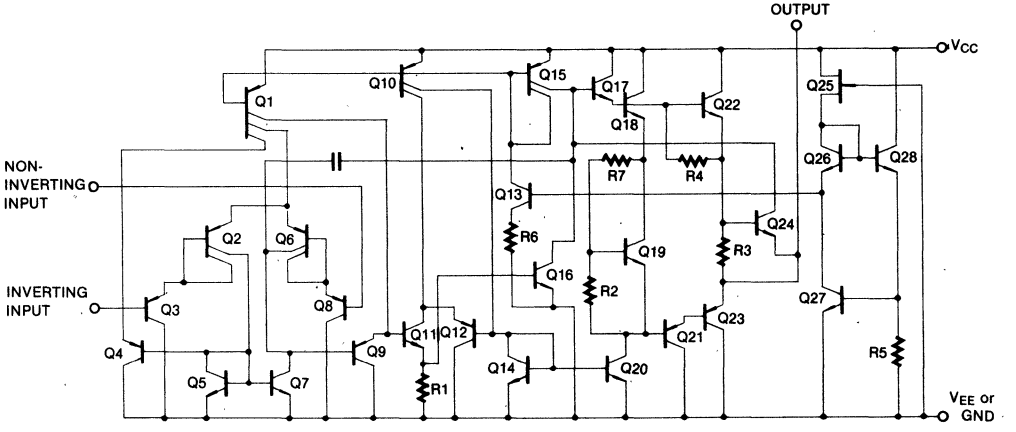
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
MC3303N	14 DIP	−40 ~ +85°C
MC3403N	14 DIP	0 ~ +70°C
MC3403D	14 SOP	

SCHEMATHIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	±18 or 36	V
Differential Input Voltage	V_{ID}	±36	V
Input Voltage	V_i	±18	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	670	mW
Operating Temperature MC3303	T_{opr}	−40 ~ +85	°C
MC3403		0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V for MC3403, V_{CC} = +14V, V_{EE} = GND for MC3303, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC3303			MC3403			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}			2.0	8.0		2.0	10	mV
		$T_{amin} \leq T_a \leq T_{amax}$			10			12	
Input Offset Current	I_{IO}			30	75		30	50	nA
		$T_{amin} \leq T_a \leq T_{amax}$			250			200	
Input Bias Current	I_{IB}			0.2	0.5		0.2	0.5	μA
		$T_{amin} \leq T_a \leq T_{amax}$			1.0			0.8	
Large Signal Voltage Gain	A_V	V_o = ±10V, R_L = 2KΩ	20	200		20	200		V/mV
		$T_{amin} \leq T_a \leq T_{amax}$	15			15			
Input Impedance	R_i		0.3	1		0.3	1.0		MΩ
Output Voltage Swing	V_{OUT}	R_L = 10KΩ	12	12.5		±12	±13.5		V
		R_L = 2KΩ	10	12		±10	±13		
		R_L = 2KΩ, $T_{amin} \leq T_a \leq T_{amax}$	±10			±10			
Input Common Mode Voltage Range	V_{ICR}		12V-V_{EE}	12.5V-V_{EE}		13V-V_{EE}	13.5V-V_{EE}		V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$	70	90		70	90		dB
Power Supply Current	I_S	V_o = 0, R_L = ∞		2.8	7.0		2.8	7.0	mA
Output Short Circuit Current	I_{OS}	Each amplifier	±10	±30	±45	±10	±20	±45	mA
Positive Supply Rejection Ratio	$PSRR^+$			30	150		30	150	μV/V
Negative Supply Rejection Ratio	$PSRR^-$						30	150	μV/V
Average Temperature Coefficient of Input Offset Current	$\Delta I_{io}/\Delta T$			50			50		pA/°C

ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = +15V, V_{EE} = −15V for MC3403, V_{CC} = +14V, V_{EE} = GND for MC3303, unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC3303			MC3403			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage Drift	$\triangle V_{io}/\triangle T$			10			10		μV/°C
Power Bandwidth	GBW	A_V = 1, R_L = 2KΩ, V_o = $20V_{p-p}$, THD = 5%		9.0			9.0		KHz
Small Signal Bandwidth	BW	A_V = 1, R_L = 10KΩ, V_o = 50mV		1.0			1.0		MHz
Slew Rate	SR	A_V = 1, V_{IN} = −10V to +10V		0.6			0.6		V/μs
Rise Time	t_r	A_V = 1, R_L = 10KΩ, V_o = 50mV		0.35			0.35		μs
Fall Time	t_f	A_V = 1, R_L = 10KΩ, V_o = 50mV		0.35			0.35		μs
Over Shoot	OS	A_V = 1, R_L = 10KΩ, V_O = 50mV		20			20		%
Phase Margin	ϕ_m	A_V = 1, R_L = 2KΩ, C_L = 200pF		60			60		Degrees
Crossover Distortion	CD	V_{IN} = $30mV_{p-p}$, V_o = $2.0V_{p-p}$, f = 10KHz		1.0			1.0		%

* $T_{amin} < Ta < T_{amax}$
MC3303: T_{amin} = −40°C, T_{amax} = +85°C
MC3403: T_{amin} = 0°C, T_{amax} = +70°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	MC3303			MC3403			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}				10		2.0	10	mV
Input Offset Current	I_{IO}				75		30	50	nA
Input Bias Current	I_{IB}				500		200	500	nA
Large Signal Open Loop Voltage Gain	A_V	R_L = 2.0KΩ	10	200		10	200		V/mV
Power Supply Rejection Ratio	PSRR				150			150	μV/V
Output Voltage Range	V_{OUT}	R_L = 10K, V_{CC} = 5.0V	3.3	3.5		3.3	3.5		V
		R_L = 10K, 5.0V ≤ V_{CC} ≤ 30V	V_{CC}-2.0	V_{CC}-1.7		V_{CC}-2.0	V_{CC}-1.7		
Supply Current	I_{CC}			2.5	7.0		2.5	7.0	mA
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1. Large Signal Open Loop Voltage Gain V_S Frequency

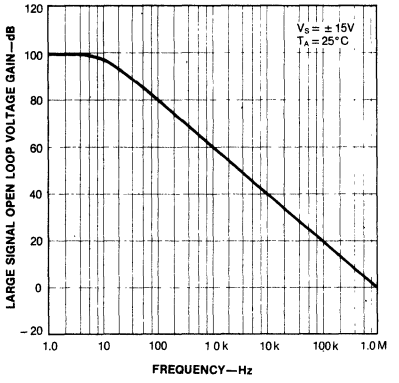


Fig. 2. Wave Response

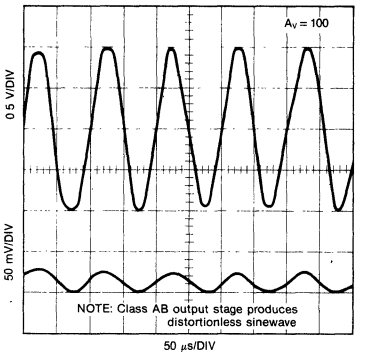


Fig. 3. Output Voltage V_S Frequency

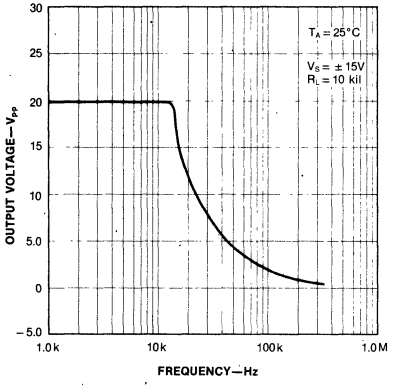


Fig. 4. Output Voltage V_S Supply Voltage

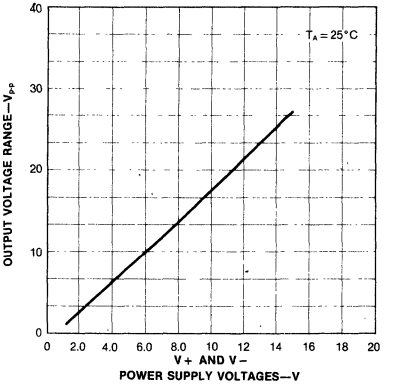


Fig. 5. Input Bias Voltage V_S Temperature

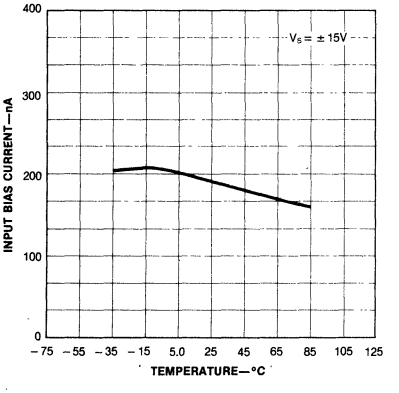
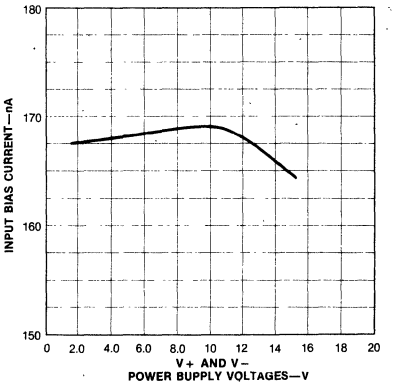
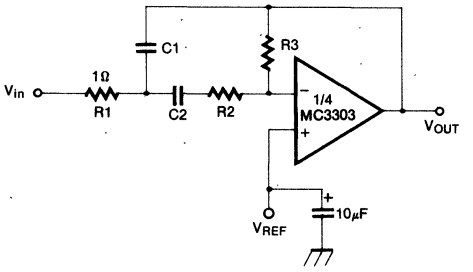


Fig. 6. Input Bias Current V_S Supply Voltage



TYPICAL APPLICATIONS

Fig. 7. Multiple feedback bandpass filter



f_o = center frequency

BW = Bandwidth

R in kΩ

C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

$$\left.\begin{aligned} R1 &= R2 = 1 \\ R8 &= 9Q^2 - 1 \end{aligned}\right\}$$ Use scaling factors in these expressions.

If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:

given: $Q = 5$, $f_o = 1$ kHz

Let $R1 = R2 = 10$ kΩ

then $R3 = 9(5)^2 - 10$

$R3 = 215$ kΩ

$$C = \frac{5}{3} = 1.6 \text{ nF}$$

Fig. 8. Wein bridge oscillator

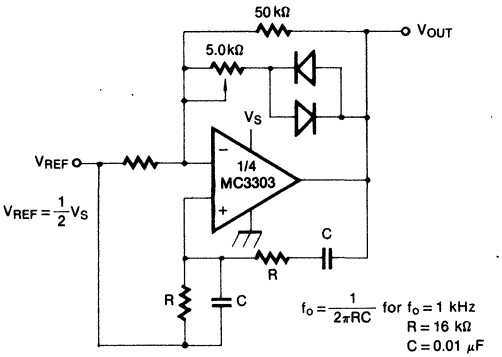
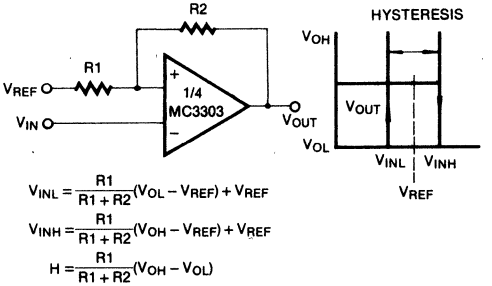


Fig. 9. Comparator with hysteresis



$$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Fig. 10. High impedance differential amplifier

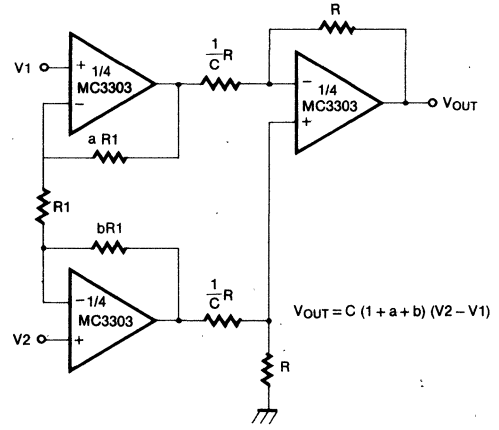


Fig. 11. AC Coupled inverting amplifier

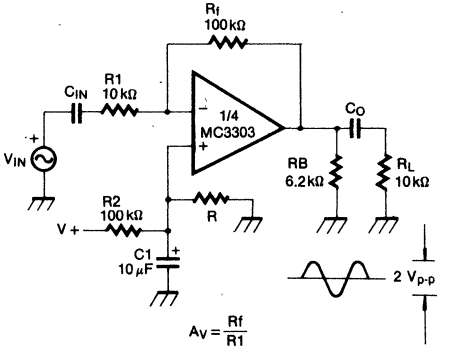


Fig. 12. Ground referencing a differential input signal

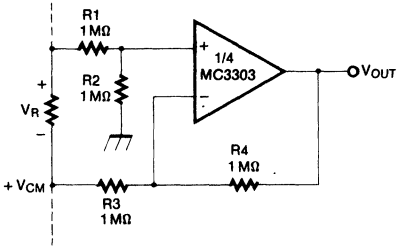


Fig. 13. Voltage reference

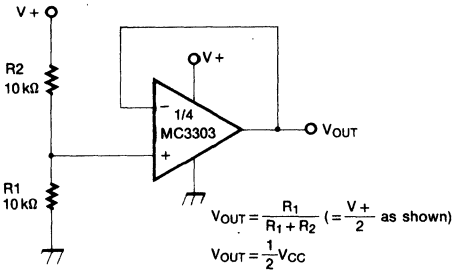


Fig. 14. AC Coupled non-inverting amplifier

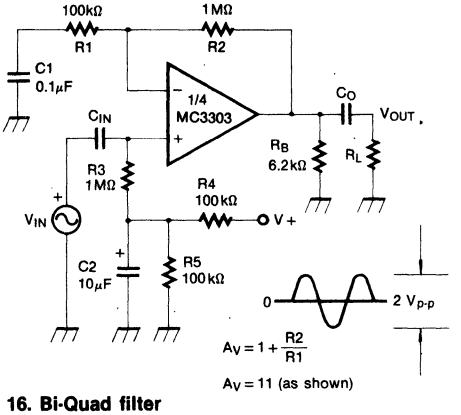


Fig. 15. Pulse generator

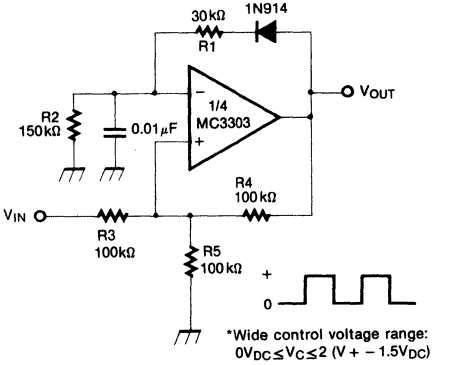


Fig. 16. Bi-Quad filter

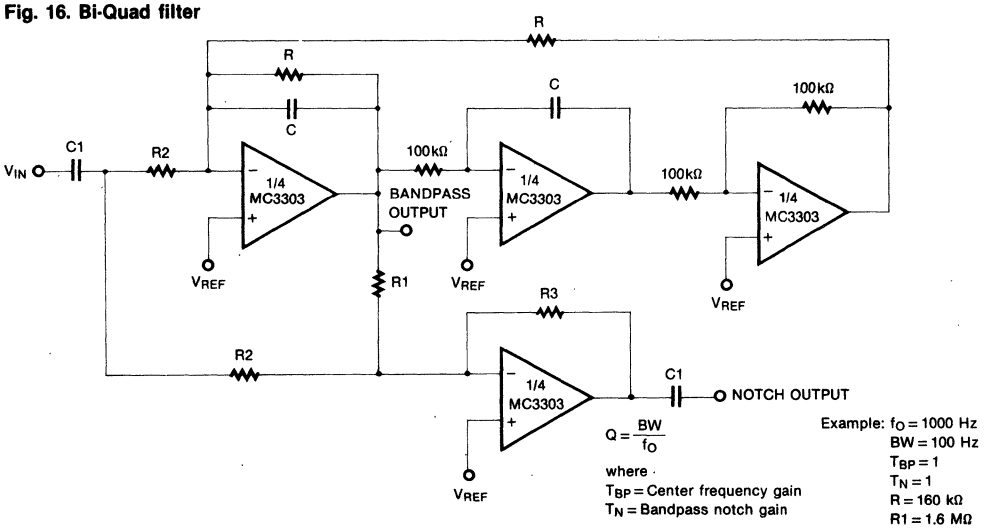


Fig. 17. Voltage controlled oscillator

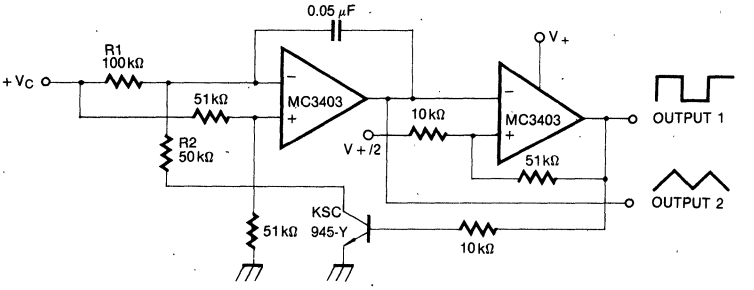
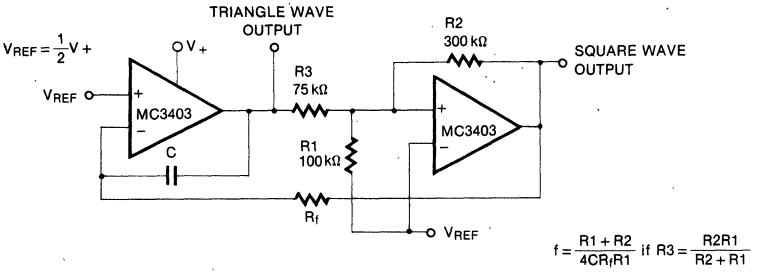
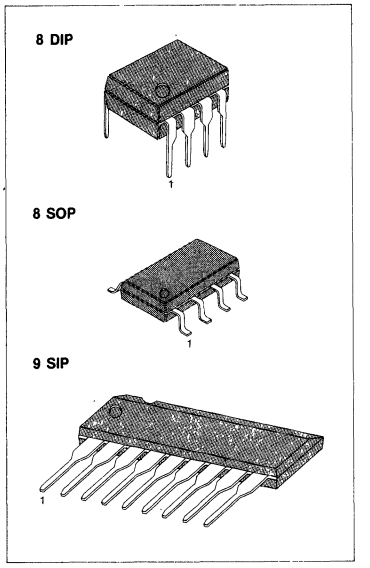


Fig. 18. Function generator



DUAL OPERATIONAL AMPLIFIER

The MC4558 series is a monolithic integrated circuit designed for dual operational amplifier.

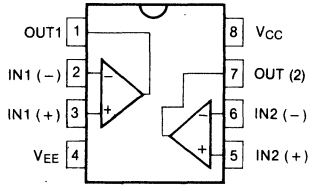


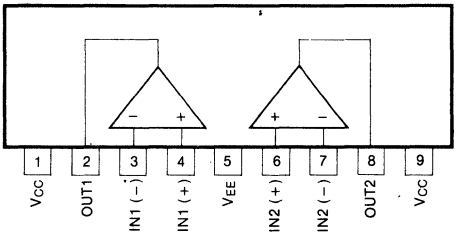
FEATURES

- **No frequency compensation required.**
- **No latch-up.**
- **Large common mode and differential voltage range.**
- **Parameter tracking over temperature range.**
- **Gain and phase match between amplifiers.**
- **Internally frequency compensated.**
- **Low noise input transistors.**

4

BLOCK DIAGRAM

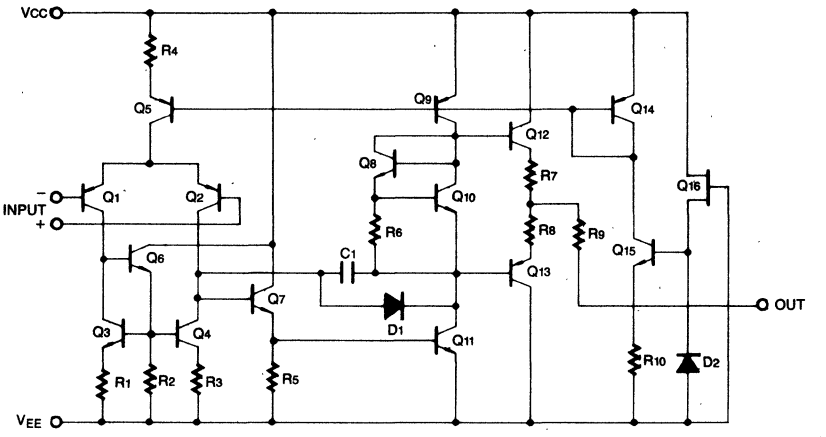




ORDERING INFORMATION

Device	Package	Operating Temperature
MC4558IN	8 DIP	−40 ~ +85°C
MC4558ID	8 SOP	
MC4558ACN	8 DIP	0 ~ +70°C
MC4558ACD	8 SOP	
MC4558CN	8 DIP	
MC4558CD	8 SOP	
MC4558S	9 SIP	

SCHEMATIC DIAGRAM (One Section Only)



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage MC4558AC/ MC4558C MC4558I	V_S	±22 ±18	V V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage	V_i	±15	V
Power Dissipation	P_D	400	mW
Operating Temperature Range MC4558I MC4558AC/MC4558C	T_{opr}	−40 ~ +85 0 ~ 70	°C °C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		MC4558I/MC4558AC			MC4558C			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 10K\Omega$			1	5		2	6	mV
			$T_{amin} \leq T_a \leq T_{amax}$		1	6			7.5	
Input Offset Current	I_{IO}				20	200		20	200	nA
			$T_a = T_{amax}$		70	200			300	
			$T_a = T_{amin}$		85	500			300	
Input Bias Current	I_{IB}				80	500		80	500	nA
			$T_a = T_{amax}$		30	500			800	
			$T_a = T_{amin}$		300	1500			800	
Large Signal Voltage Gain	A_V	$V_O = \pm 10V$ $R_L \geq 2.0K\Omega$		50	200		20	200		V/mV
			$T_{amin} \leq T_a \leq T_{amax}$	25			15			
Common Mode Input Voltage Range	V_{ICR}			±12	±13		±12	±13		V
			$T_{amin} \leq T_a \leq T_{amax}$	±12	±13					
Common Mode Rejection Ratio	CMRR	$R_S \leq 10K\Omega$		70	90		70	90		dB
			$T_{amin} \leq T_a \leq T_{amax}$	70	90					
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10K\Omega$		76	90		76	90		dB
			$T_{amin} \leq T_a \leq T_{amax}$	76	90		76	90		
Output Voltage Swing	V_{OUT}	$R_L \geq 10K\Omega$	$T_{amin} \leq T_a \leq T_{amax}$	±12	±14		±12	±14		V
		$R_L \geq 2K\Omega$		±10	±13		±10	±13		
Supply Current (Both Amplifiers)	I_S				2.3	5.0		2.3	5.6	mA
			$T_a = T_{amax}$			4.5			5.0	
			$T_a = T_{amin}$			6.0			6.7	
Power Consumption (Both Amplifiers)	P_C				70	150		70	170	mV
			$T_a = T_{amax}$			135			150	
			$T_a = T_{amin}$			180			200	
Slew Rate	SR	$V_i = 10V$, $R_L \geq 2K\Omega$ $C_L \leq 100pF$		1.0			1.0			V/μs
Rise Time	t_r	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$			0.3			0.3		μs
Overshoot	OS	$V_i = 20mV$, $R_L \geq 2K\Omega$, $C_L \leq 100pF$			15			15		%

* MC4558I: $T_{amin} = -40°C$, $T_{amax} = +85°C$
MC4558AC/MC4558C: $T_{amin} = 0°C$, $T_{amax} = +70°C$

TYPICAL PERFORMANCE CHARACTERISTICS

BURST NOISE V_S SOURCE RESISTANCE

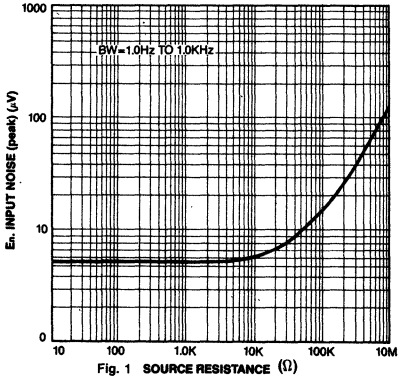


Fig. 1 SOURCE RESISTANCE (Ω)

RMS NOISE V_S SOURCE RESISTANCE

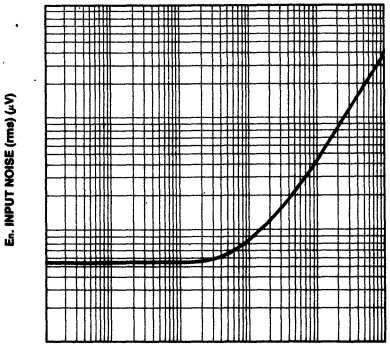


Fig. 2 SOURCE RESISTANCE (Ω)

OUTPUT NOISE V_S SOURCE RESISTANCE

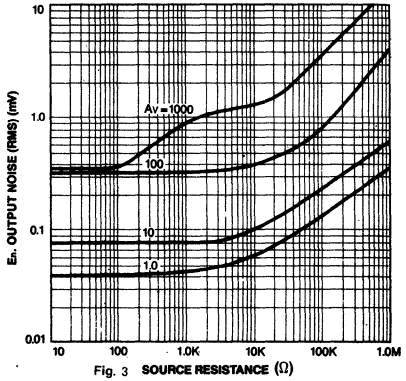


Fig. 3 SOURCE RESISTANCE (Ω)

SPECTRAL NOISE DENSITY

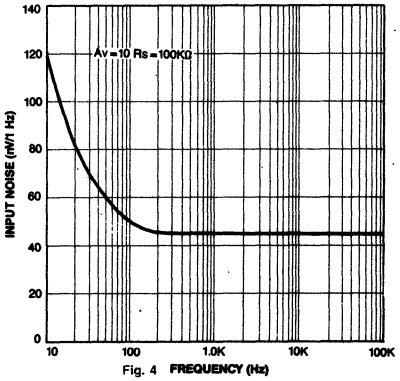


Fig. 4 FREQUENCY (Hz)

OPEN LOOP FREQUENCY RESPONSE

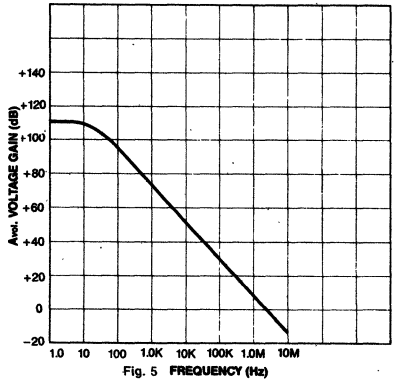


Fig. 5 FREQUENCY (Hz)

PHASE MARGIN V_S FREQUENCY

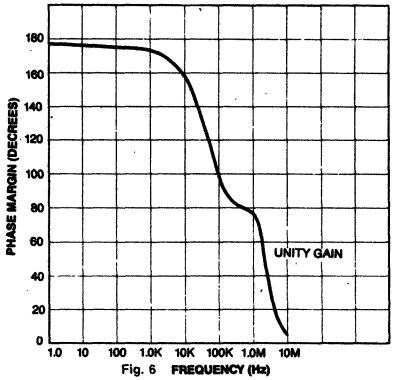


Fig. 6 FREQUENCY (Hz)

POSITIVE OUTPUT VOLTAGE SWING
V_S LOAD RESISTANCE

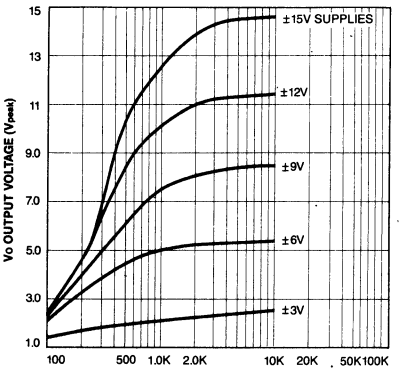


Fig. 7 LOAD RESISTANCE (Ω)

NEGATIVE OUTPUT VOLTAGE SWING
V_S LOAD RESISTANCE

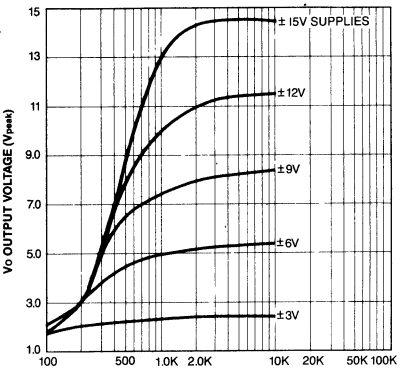


Fig. 8 LOAD RESISTANCE (Ω)

POWER BANDWIDTH
(LARGE SIGNAL SWING VERSUS FREQUENCY)

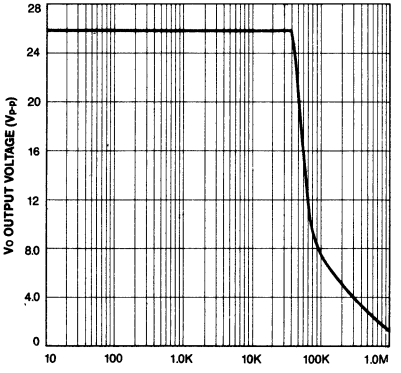


Fig. 9 FREQUENCY (Hz)

TRANSIENT RESPONSE TEST CIRCUIT

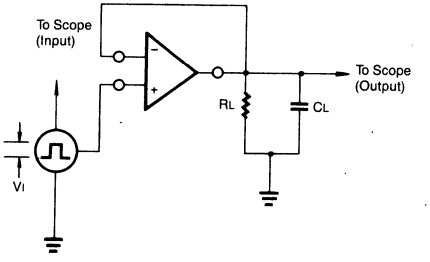
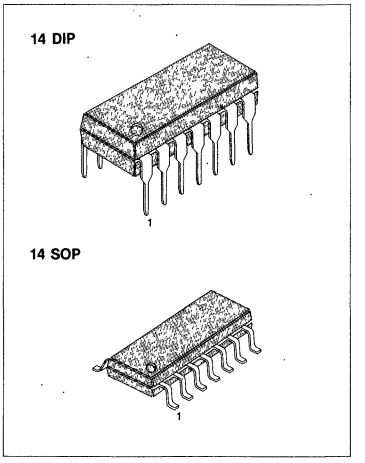


Fig. 10

DUAL HIGH SPEED VOLTAGE COMPARATOR

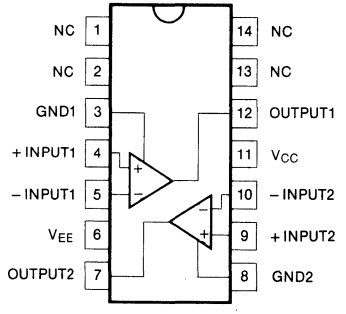
The KA319 is a dual high speed voltage comparator designed to operate from a single +5V supply up to ±15V dual supplies.
Open collector of the output stage makes the KA319 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA. Typical response time of 80ns with ±15V power supplies makes the KA319 ideal for application in fast A/D converts, level shifters, oscillaters, and multivibrators.



FEATURES

- **Operates form a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Open collector outputs: up to +35V**
- **High output drive current: 25mA**
- **Inputs and outputs can be isolated from system ground**
- **Minimum fan-out of 2 (each side)**
- **Two independent compators**

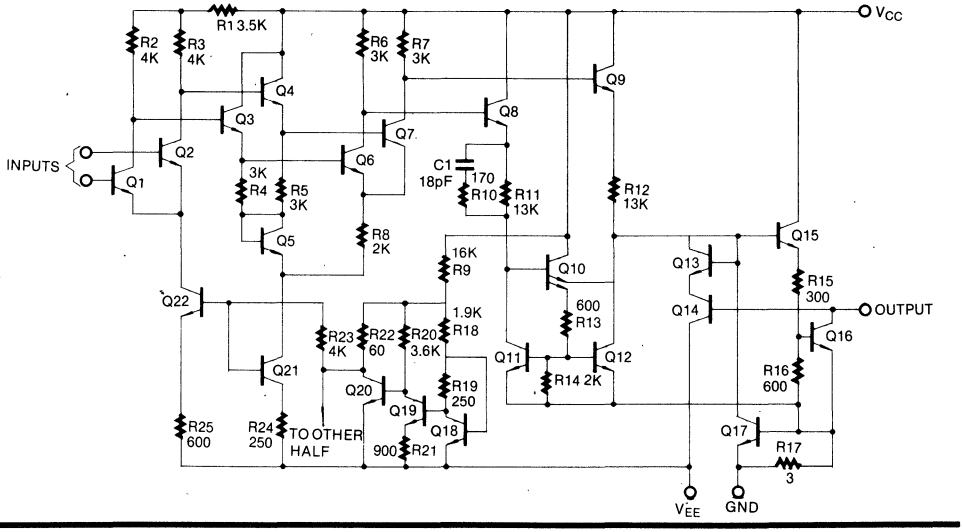
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA319N	14 DIP	0 ~ +70°C
KA319D	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_S	36	V
Output to Negative Supply Voltage	$V_o - V_{EE}$	36	V
Ground to Negative Supply Voltage	$GND - V_{EE}$	25	V
Ground to Positive Supply Voltage	$GND - V_{CC}$	18	V
Differential Input Voltage	V_{ID}	±5	V
Input Voltage	V_I	±15	V
Output Short Circuit Duration		10	sec
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage (Note 1)	V_{IO}	$R_S \leq 5K$			2.0	8.0	mV
			$T_{amin} \leq T_a \leq T_{amax}$			10	
Input Offset Current (Note 1)	I_{IO}				80	200	nA
			$T_{amin} \leq T_a \leq T_{amax}$			300	
Input Bias Current	I_{IB}				250	1000	nA
			$T_{amin} \leq T_a \leq T_{amax}$			1200	
Voltage Gain	A_V			8	40		V/mV
Response Time (Note 2)	t_r	$V_S = \pm 15V$			80		ns
Saturation Voltage	V_{OL}	$V_{in} \leq -10mV$, $I_{out} = 25mA$			0.75	1.5	V
		$V_{CC} \geq 4.5V$, $V_{EE} = 0$, $V_{IN} \leq -10mV$, $I_{SINK} \leq 3.2mA$			0.3	0.4	V
			$T_{amin} \leq T_a \leq T_{amax}$				
Output Leakage Current	I_{OL}	$V_{in} \geq 10mV$, $V_{out} = 35V$			0.2	2	μA
Input Voltage Range	V_{ICR}	$T_{amin} \leq T_a \leq T_{amax}$	$V_S = \pm 15V$		±13		V
			$V_{CC} = 5V$, $V_{EE} = 0V$	1		3	
Differential Input Voltage	V_{ID}					±5	V
Positive Supply Current	I_{CC1}	$V_{CC} = 5V$, $V_{EE} = 0V$			4.3		mA
Positive Supply Current	I_{CC2}	$V_S = \pm 15V$			8	12.5	mA
Negative Supply Current	I_{EE}	$V_S = \pm 15V$			3	5	mA

Note: 1. The offset voltage and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impeance.
2. The response time specified is for a 100mV input step with 5mV overdrive.
3. $T_{amin} \leq T_a \leq T_{amax}$
KA319: $T_{amin} = 0°C$, $T_{amax} = 70°C$

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT CURRENTS vs TEMPERATURE

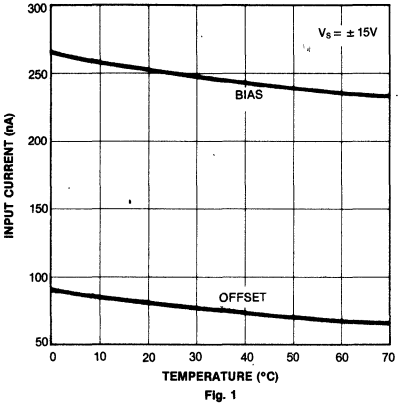


Fig. 1

SUPPLY CURRENTS vs TEMPERATURE

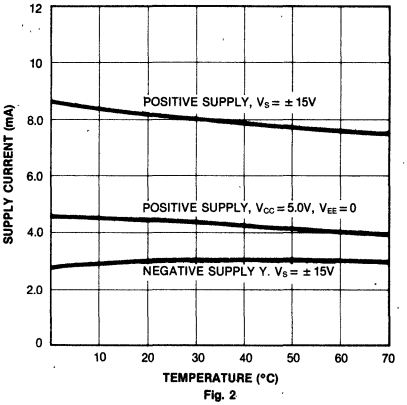


Fig. 2

TRANSFER FUNCTION

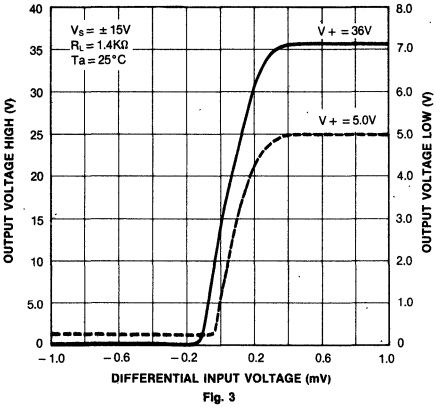


Fig. 3

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

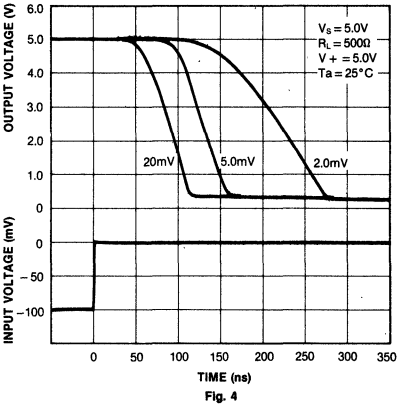


Fig. 4

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

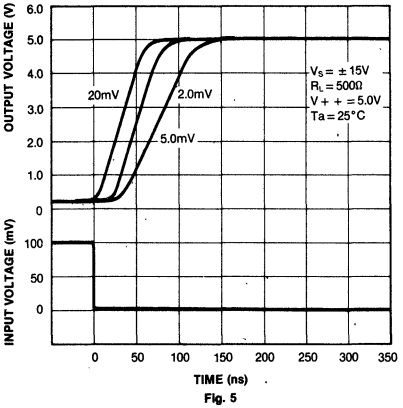


Fig. 5

INPUT CHARACTERISTICS vs DIFFERENTIAL INPUT VOLTAGE

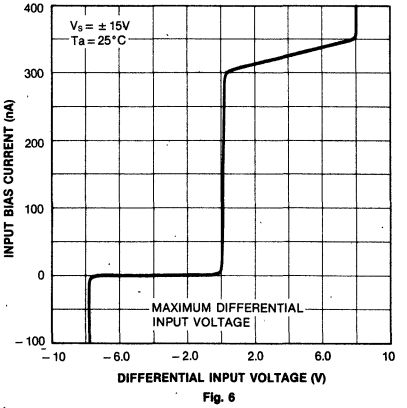


Fig. 6

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

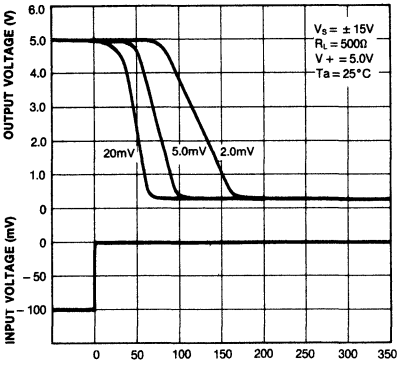


Fig. 7

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

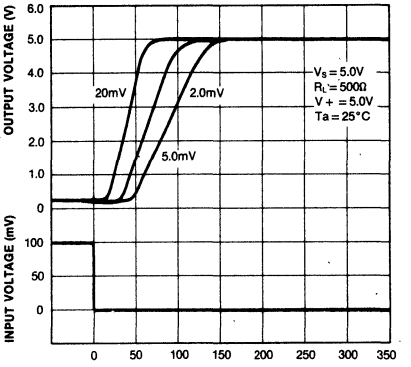


Fig. 8

OUTPUT SATURATION VOLTAGE vs OUTPUT VOLTAGE

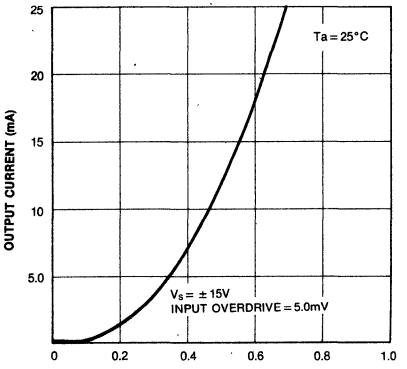


Fig. 9

SUPPLY CURRENT vs SUPPLY VOLTAGE

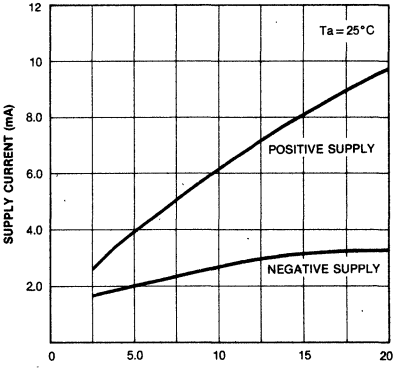


Fig. 10

OUTPUT LIMITING CHARACTERISTICS vs OUTPUT VOLTAGE

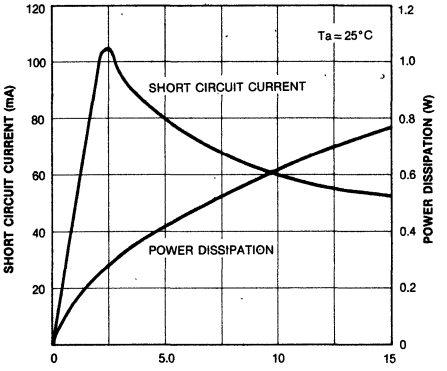
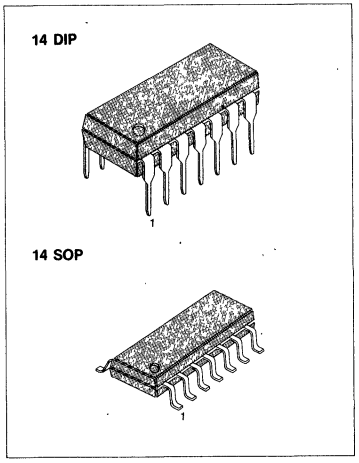


Fig. 11

HIGH SPEED VOLTAGE COMPARATOR

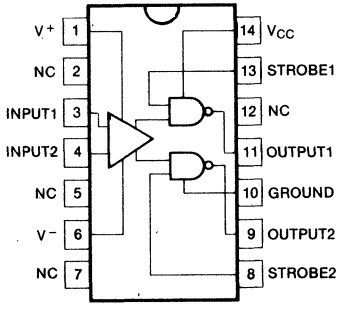
The KA361 is a very high speed differential input, complementary TTL output voltage comparator. Applications involve high speed A/D converts and zero-crossing detectors in disc file systems.



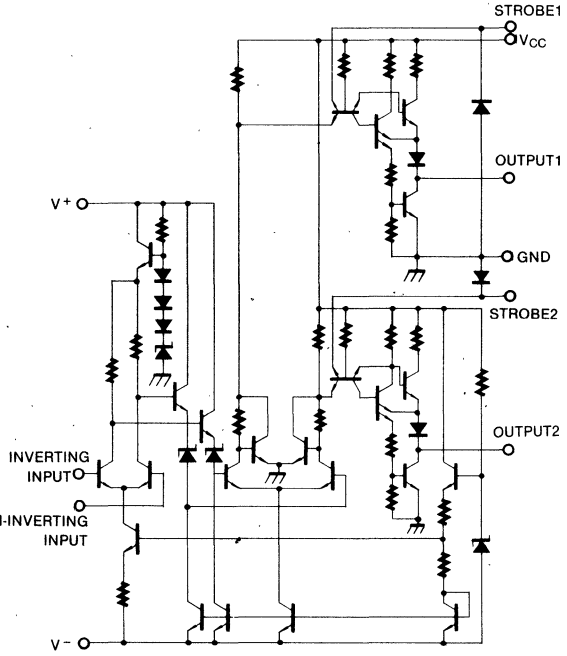
FEATURES

- **Complementary TTL outputs**
- **Independent strobes**
- **High speed: 20ns (max)**
- **Operates from OP amp supplies: ±15V**
- **Low input offset voltage**
- **Versatile supply voltage range**

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA361N	14 DIP	0 ~ +70°C
KA361D	14 SOP	

OPERATING CONDITIONS

Supply Voltage	Min	Typ	Max	Unit
V+	5		15	V
V−	−6		−15	V
V_{CC}	4.75		5.25	V

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V+	+16	V
Negative Supply Voltage	V−	−16	V
Gate Supply Voltage	V_{CC}	+7	V
Output Voltage	V_{OUT}	+7	V
Differential Input Voltage	V_{ID}	±5	V
Input Voltage Range	V_I	±6	V
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

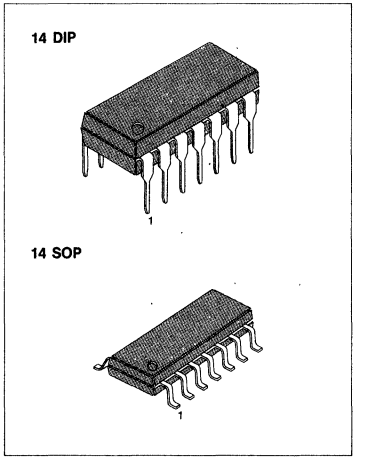
(V+ = +10V, V_{CC} = +5V, V− = −10V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	0°C ≤ Ta ≤ 70°C		1	5	mV
Input Bias Current	I_{IB}			10	30	μA
Input Offset Current	I_{IO}			2	5	μA
Voltage Gain	A_V			3		V/mV
Input Resistance	R_i	f = 1KHz		20		KΩ
Logical "1" Output Voltage	V_{OH}	V_{CC} = 4.75V, I_{source} = −5mA	2.4	3.3		V
Logical "0" Output Voltage	V_{OL}	V_{CC} = 4.75V, I_{sink} = 6.4mA			0.4	V
Strobe Input "1" Current	I_{stH}	V_{CC} = 5.25V, V_{strobe} = 2.4V			200	μA
Strobe Input "0" Current	I_{stL}	V_{CC} = 5.25V, V_{strobe} = 0.4V			−1.6	mA
Strobe Input "0" Voltage	V_{stL}	V_{CC} = 4.75V			0.8	V
Strobe Input "1" Voltage	V_{stH}	V_{CC} = 4.75V	2			V
Output Short Circuit Current	I_{OS}	V_{CC} = 5.25V, V_{OUT} = 0V, V^+ = 10V, V^- = −10V	18		−55	mA
Supply Current	I+	V_{CC} = 5.25V, $T_{amin} \leq T_a \leq T_{amax}$			5	mA
Supply Current	I−	V_{CC} = 5.25V, $T_{amin} \leq T_a \leq T_{amax}$			10	mA
Supply Current	I_{CC}	V_{CC} = 5.25V, $T_{amin} \leq T_a \leq T_{amax}$			20	mA
Propagation Delay Time	t_{pd} (0)	V_{IN} = 50mV overdrive		14	20	ns
Propagation Delay Time	t_{pd} (1)	V_{IN} = 50mV overdrive		14	20	ns
Delay Between Output A and B	t_d	V_{IN} = 50mV overdrive		2	5	ns
Strobe Delay Time (t_{pd} (0))	t_d	V_{IN} = 50mV overdrive		8		ns
Strobe Delay Time (t_{pd} (1))	t_d	V_{IN} = 50mV overdrive		8		ns

4

HIGH SPEED VOLTAGE COMPARATOR

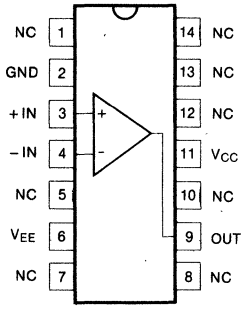
The KA710C is a high speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance.
The output of the comparator is compatible with all intergrated logic forms.
The KA710C is useful as pulse height disciminators, a variable threshold schmitt trigger, voltage comparators in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver.



FEATURES

- **Low offset voltage: 5mV**
- **High gain: 1000 (Min)**
- **High speed: 40ns Typ**

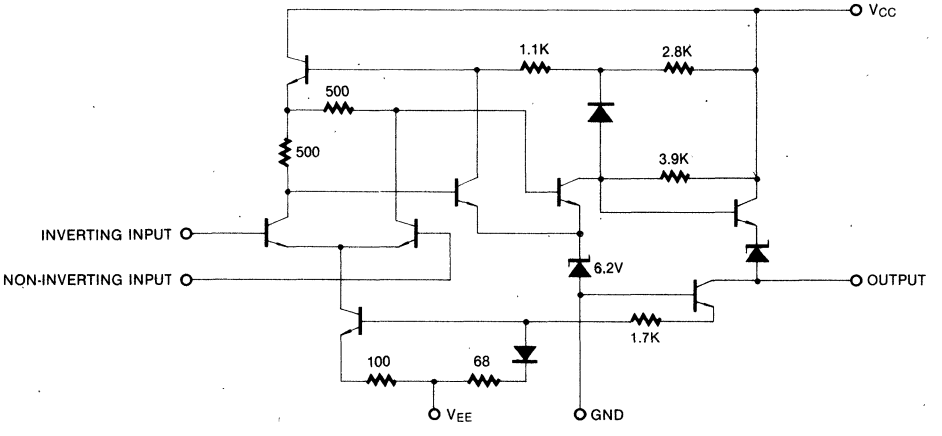
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
KA710CN	14 DIP	0 ~ +70°C
KA710CD	14 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+14	V
Negative Supply Voltage	V_{EE}	−7	V
Peak Output Current	I_{peak}	10	mA
Output Short Circuit Duration		10	Sec
Differential Input Voltage	V_{ID}	±5	V
Input Voltage	V_I	±7	V
Power Dissipation	P_D	200	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = −6V, Ta = 25°C, unless otherwise specified)

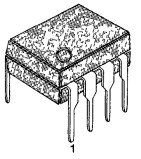
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 200\Omega$		1.6	5.0	mV
		$0 \leq Ta \leq 70°C$			6.5	
Input Offset Current	I_{IO}	V_{OUT} = 1.4V		1.8	5.0	μA
		$0 \leq Ta \leq 70°C$			7.5	
Input Bais Current	I_{IB}			16	25	μA
		Ta = 0°C		25	40	
Large Signal Voltage Gain	A_V		1000	1500		V/V
Input Voltage Range	V_{ICR}	V_{EE} = −7.0V	±5.0			V
Common Mode Rejection Ratio	CMRR	$R_S \leq 200\Omega$	70	98		dB
Differential Input Voltage Range	V_{IDR}		±5.0			V
Output Voltage (High)	V_{OH}	$V_{IN} \geq 5mV$, $0 < I_{OUT} < 5mA$	2.5	3.2	4.0	V
Output Voltage (Low)	V_{OL}	$V_{IN} \geq 5mV$	−1.0	−0.5	0	V
Output Sink Current	I_{sink}	$V_{IN} \geq 10mV$, $V_o = 0V$	0.5			mA
Positive Supply Current	I_{CC}	$V_o = 0V$, $V_{IN} \geq 10mV$		5.2	9.0	mA
Negative Supply Current	I_{EE}	$V_o = 0V$, $V_{IN} \leq 10mV$		4.6	7.0	mA
Power Consumption	P_D	$V_o = 0V$, $V_{IN} \geq 10mV$			150	mW
Response Time	t_r	(NOTE1)		40		ns

Note: 1. The response time specified is for a 100mV input step with 10mV overdrive.

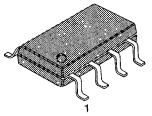
VOLTAGE COMPARATOR

The LM211 series is a monolithic, low input current voltage comparator.

8 DIP



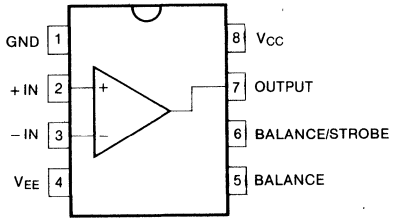
8 SOP



FEATURE

- **Low input bias current: MAX 250nA.**
- **Low input offset current: MAX 50nA.**
- **Differential Input Voltage: ±30V.**
- **Power supply voltage: single 5.0V supply to ±15V.**
- **Offset voltage null capability.**
- **Strobe capability.**

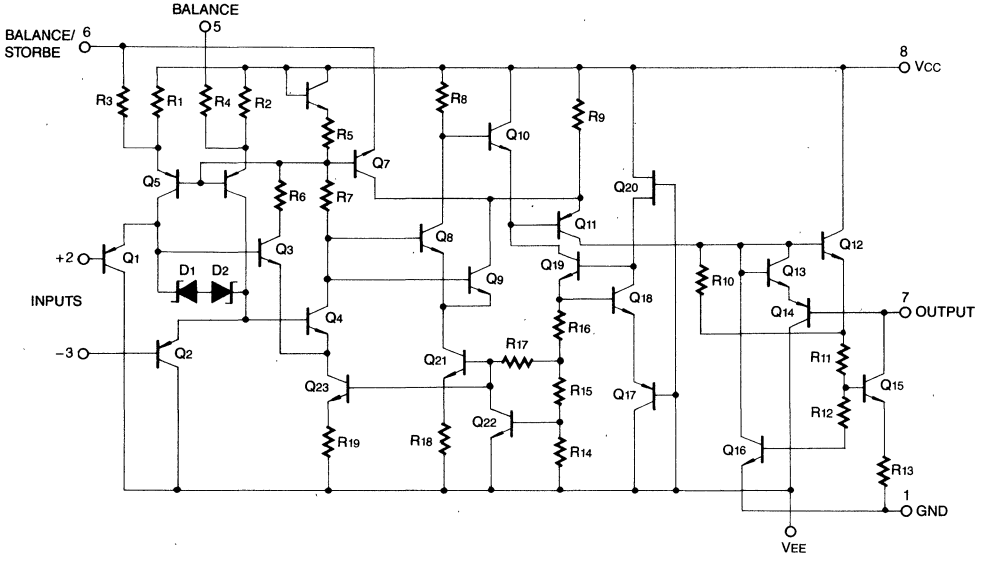
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM211N	8 DIP	-25 ~ +85°C
LM211D	8 SOP	
LM311N	8 DIP	0 ~ +70°C
LM311D	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Total Supply Voltage	V_S	36	V
Output to Negative Supply Voltage LM211	$V_O - V_{EE}$	50	V
LM311		40	V
Ground to Negative Supply Voltage	V_{EE}	30	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage	V_{IN}	±15	V
Output Short Circuit Duration		10	sec
Voltage at Strobe Pin		V_{CC} to V_{CC}-5.0	V
Power Dissipation	P_D	500	mW
Operating Temperature LM211	T_{opr}	−25 ~ +85	°C
LM311		0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, V_{EE} = −15V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions	LM211			LM311			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (NOTE1)	V_{IO}	$R_S \leq 50K\Omega$		0.7	3.0		2.0	7.5	mV
		$T_{amin} \leq T_a \leq T_{amax}$			4.0			10	
Input Offset Current (NOTE1)	I_{IO}			4.0	10		6	50	nA
		$T_{amin} \leq T_a \leq T_{amax}$			20			70	
Input Bias Current	I_{IB}			60	100		100	250	nA
		$T_{amin} \leq T_a \leq T_{amax}$			150			300	
Voltage Gain	A_V		40	200		40	200		V/mV
Response Time (NOTE2)	t_r			200			200		nS
Saturation Voltage	V_{sat}	$V_{id} \leq -5.0mV$, $I_o = 50mA$		0.75	1.5				V
		$V_{id} = -10.0mV$, $I_o = 50mA$					0.75	1.5	
		$V_{CC} \geq 4.5V$, $V_{EE} = 0V$, $I_{sink} \leq 8.0mA$ $V_{id} \leq -6.0mV$ $T_{amin} \leq T_a \leq T_{amax}$		0.23	0.4				
		$V_{id} \leq -10.0mV$					0.23	0.4	
Strove "ON" Current	I_S			3			3		mA
Output Leakage Current	I_{leak}	$V_{id} \geq 5.0mV$ $V_o = 35V$		0.2	10				nA
		$V_{id} \geq 10mV$ $V_o = 35V$					0.2	50	
		$V_{id} \geq 5.0mV$, $V_o = 35V$, $T_{amin} < T_a < T_{amax}$		0.1	0.5				μA
Input Voltage Range	V_{ICR}	$T_{amin} \leq T_a \leq T_{amax}$	−14.5	−14.7 to 13.8	13.0	−14.5	−14.7 to 13.8	13.0	V
Positive Supply Current	I_{CC}			2.4	6.0		2.4	7.5	mA
Negative Supply Current	I_{EE}			−1.3	−5.0		−1.3	−5.0	mA
Strobe Current	I_{strobe}			3			3		mA

NOTE 1 $T_{amin} \leq T_a \leq T_{amax}$
LM211: T_{amin} = −25°C, T_{amax} = +85°C LM311: T_{amin} = 0°C, T_{amax} = +70°C
NOTE 2 The response time specified is for a 100mV input step with 5mV over drive

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT BIAS CURRENT V_S TEMPERATURE

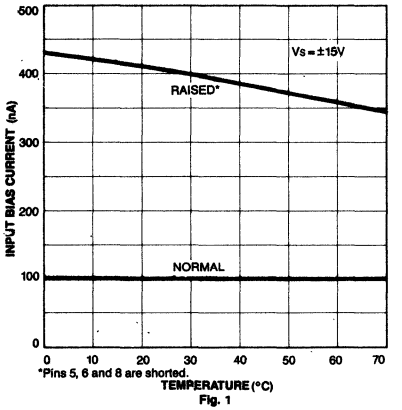


Fig. 1

INPUT OFFSET CURRENT V_S TEMPERATURE

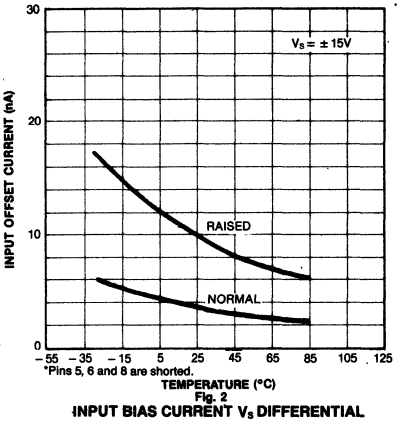


Fig. 2

OFFSET VOLTAGE V_S INPUT RESISTANCE

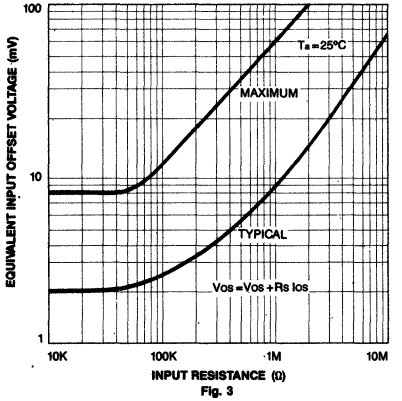


Fig. 3

INPUT BIAS CURRENT V_S DIFFERENTIAL INPUT VOLTAGE

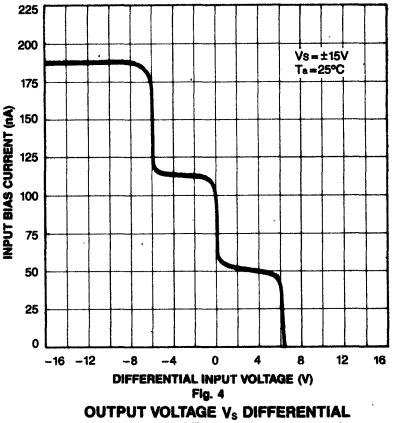


Fig. 4

COMMON MODE LIMITS V_S TEMPERATURE

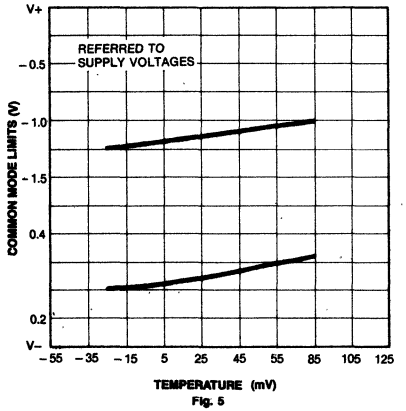


Fig. 5

OUTPUT VOLTAGE V_S DIFFERENTIAL INPUT VOLTAGE

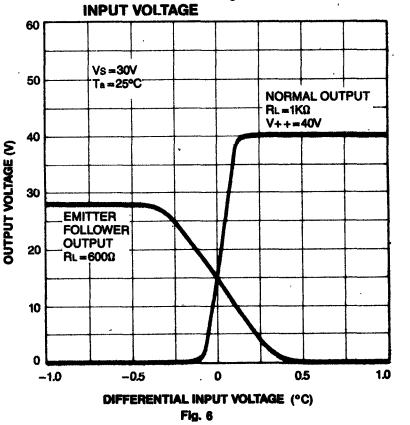


Fig. 6

SATURATION VOLTAGE V_S CURRENT

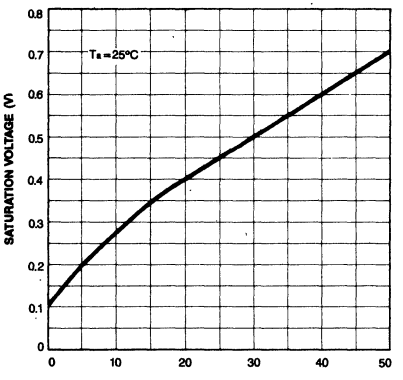


Fig. 7

SUPPLY CURRENT V_S TEMPERATURE

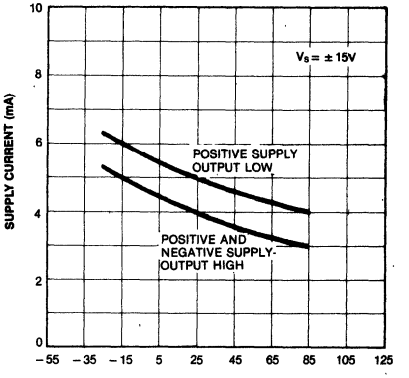


Fig. 8

LEAKAGE CURRENTS V_S TEMPERATURE

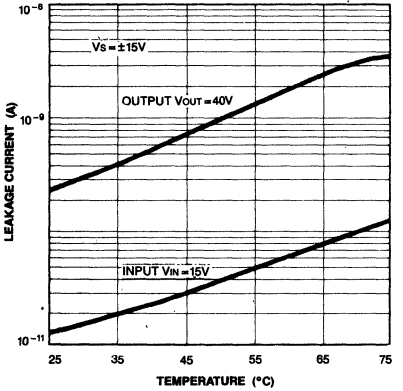


Fig. 9

TYPICAL APPLICATIONS

Switching Power Amplifier

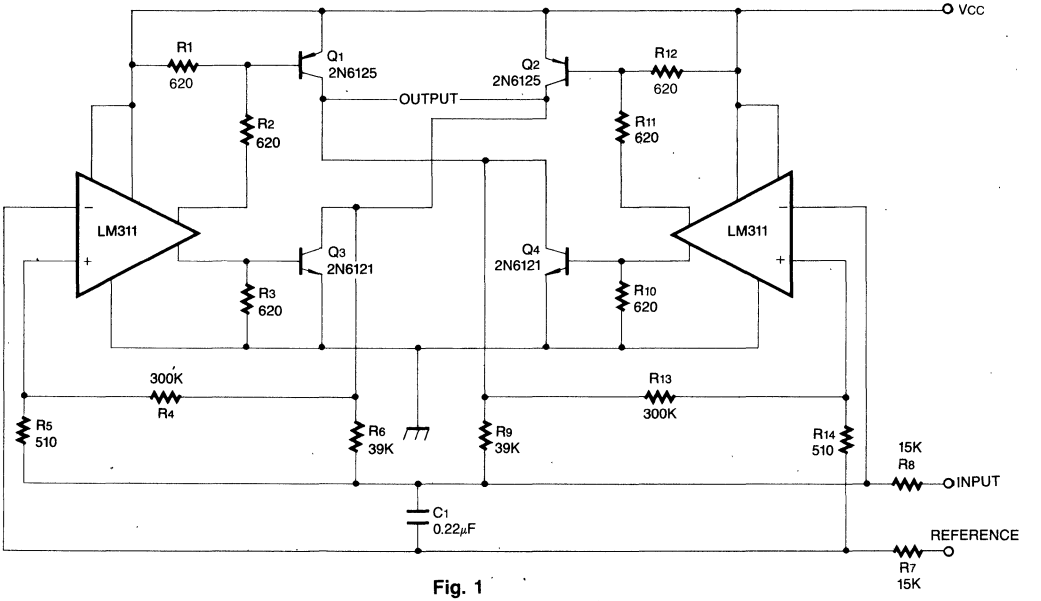


Fig. 1

Relay Driver with Strobe

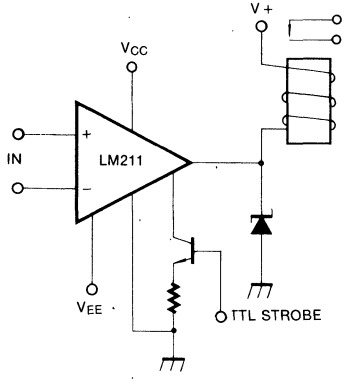


Fig. 2

Digital Transmission Isolator

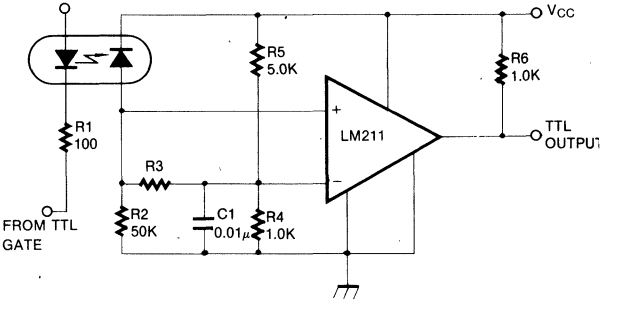
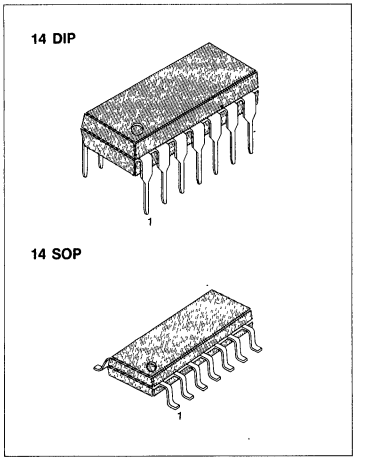


Fig. 3

QUAD DIFFERENTIAL COMPARATOR

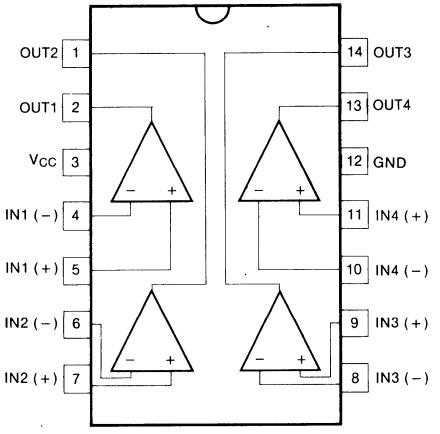
The LM239 series consists of four independent voltage comparators that one designed to operate from single power supply over a wide range of voltage.



FEATURES

- **Single or dual supply operation**
- **Wide range of supply voltages LM239/A, LM339/A: 2 ~ 36V (or ±1 ~ ±18V)**
  LM2901, LM3302: 2 ~ 28V (or ±1 ~ ±14V)
- **Low supply current drain 800μA Typ.**
- **Open collector outputs for wired and connectors**
- **Low input bias current 25nA Typ.**
- **Low input offset current ±5nA Typ.**
- **Low input offset voltage ±2mV Typ.**
- **Common mode input voltage range includes ground.**
- **Low output saturation voltage**
- **Output compatible with TTL, DTL and MOS logic system**

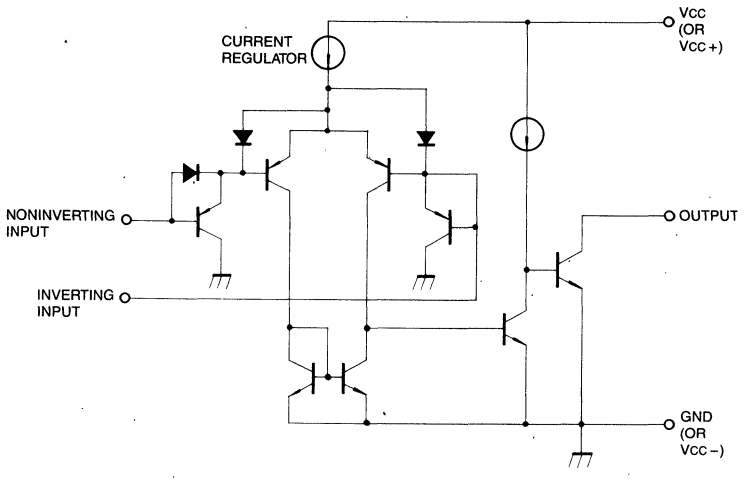
BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Operating Temperature
LM239N LM239AN	14 DIP	−25 ~ +85°C
LM239D LM239AD	14 SOP	
LM339N LM339AN	14 DIP	0 ~ 70°C
LM339D LM339AD	14 SOP	
LM2901N LM2901D LM3302N	14 DIP 14 SOP 14 DIP	−45 ~ +85°C

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_S	±18 or 36	V
Power Supply Voltage Only LM3302	V_S	±14 or 28	V
Differential Input Voltage	V_{ID}	36	V
Differential Input Voltage Only LM3302	V_{ID}	28	V
Input Voltage	V_I	−0.3 to +36	V
Input Voltage Only LM3302	V_I	−0.3 to +28	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM239/LM239A	T_{opr}	−25 ~ +85	°C
LM339/LM339A		0 ~ +70	°C
LM2901/LM3302		−40 ~ +85	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristics	Symbol	Test Condition		LM239A/LM339A			LM239/LM339			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V V_o = 1.4V, R_S = 0			±1	±2		±1	±5	mV
			$T_{amin} \leq T_a \leq T_{amax}$			±4.0			±9.0	
Input Offset Current	I_{IO}				±5	±50		±5	±50	nA
			$T_{amin} \leq T_a \leq T_{amax}$			±150			±150	
Input Bias Current	I_B				25	250		25	250	nA
			$T_{amin} \leq T_a \leq T_{amax}$			400			400	
Input Common Mode Voltage Range	V_{ICR}			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			$T_{amin} \leq T_a \leq T_{amax}$	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}		$R_L = \infty$,		0.8	2.0		0.8	2.0	mA
			$R_L = \infty$ V_{CC} = 36V		1.0	2.5		1.0	2.5	
Voltage Gain	A_{VOL}	V_{CC} = 15V, $R_L \geq 15K\Omega$ (for large swing)		50	200			200		V/mV
Large Signal Response Time	t_{RES}	V_{IN} = TTL Logic Swing V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ			300			300		ns
Response Time	t_{RES}	V_{RL} = 5V, R_L = 5.1KΩ			1.3			1.3		μs
Output Sink Current	I_{sink}	$V_{IN}^- \geq 1V$, $V_{IN}^+ = 0V$, $V_o \leq 1.5V$		6	16		6	16		mA
Output Saturation Voltage	V_{sat}	$V_{IN}^- \geq 1V$, $V_{IN}^+ = 0V$ I_{sink} = 4mA			250	400		250	400	mV
			$T_{amin} \leq T_a \leq T_{amax}$			700			700	
Output Leakage Current	I_{leak}	$V_{in}^- = 0$ V_{in} = 1V	V_o = 5V		0.1			0.1		nA
			V_o = 30V			1.0			1.0	μA

* $T_{amin} \leq T_a \leq T_{amax}$
LM239/LM239A: T_{amin} = −25°C, T_{amax} = +85°C
LM339/LM339A: T_{amin} = 0°C, T_{amax} = +70°C
LM2901/LM3302: T_{amin} = −40°C, T_{amax} = +85°C

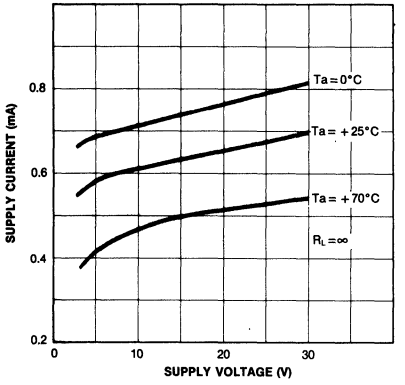
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristics	Symbol	Test Condition	LM2901			LM3302			Unit
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_S = 0		±2	±7		±3	±20	mV
		$T_{amin} \leq T_a \leq T_{amax}$		9	±15			±40	
Input Offset Current	I_{IO}			±5	±50		±3	±100	nA
		$T_{amin} \leq T_a \leq T_{amax}$		±50	±200			±300	
Input Bias Current	I_B			25	250		25	250	nA
		$T_{amin} \leq T_a \leq T_{amax}$		200	500			1000	
Input Common Mode Voltage Range	V_{ICR}		0		V_{CC}-1.5	0		V_{CC}-1.5	V
		$T_{amin} \leq T_a \leq T_{amax}$	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}	$R_L = \infty$		0.8	2.0		0.8	2.0	mA
		$R_L = \infty$, V_{CC} = 36V, LM3302, V_{CC} = 28V		1.0	2.5				
Voltage Gain	A_{VOL}	V_{CC} = 15V, $R_L \geq 15K\Omega$ (for large swing)	25	100		2	30		V/mV
Large Signal Response Time	t_{RES1}	V_{IN} = TTL Logic Swing, V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ		300			300		ns
Response Time	t_{RES2}	V_{RL} = 5V, R_L = 5.1KΩ		1.3			1.3		μs
Output Sink Current	I_{sink}	$V_{IN}^- \geq 1V$, $V_{IN}^+ = 0V$, $V_o \leq 1.5V$	6	16		6	16		mA
Output Saturation Voltage	V_{sat}	$V_{IN}^- \geq 1V$, $V_{IN}^+ = 0V$, I_{sink} = 4mA		250	400		250	400	mV
		$T_{amin} < T_a < T_{amax}$			700			700	
Output Leakage Current	I_{leak}	$V_{in}^- = 0$, V_o = 5V		0.1			0.1		nA
		V_{in} = 1V, V_o = 30V LM3302, V_o = 28V			1.0			1.0	μA

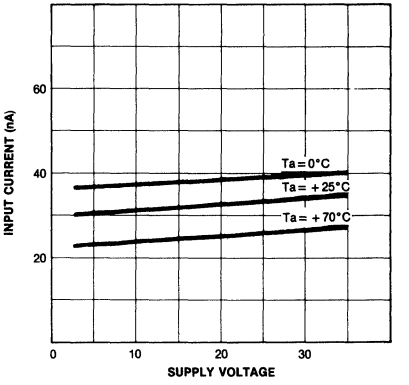
* $T_{amin} < T_a < T_{amax}$
LM239/LM239A: T_{amin} = − 25°C, T_{amax} = + 85°C
LM339/LM339A: T_{amin} = 0°C, T_{amax} = + 70°C
LM2901/LM3302: T_{amin} = − 40°C, T_{amax} = + 85°C

TYPICAL PERFORMANCE CHARACTERISTICS

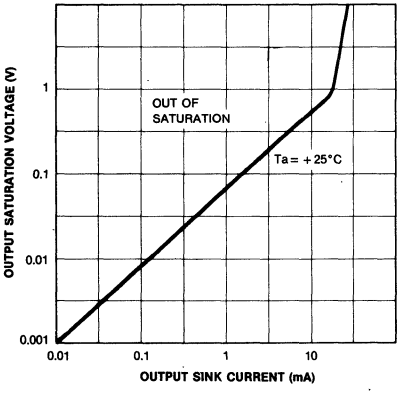
SUPPLY CURRENT V_S SUPPLY VOLTAGE



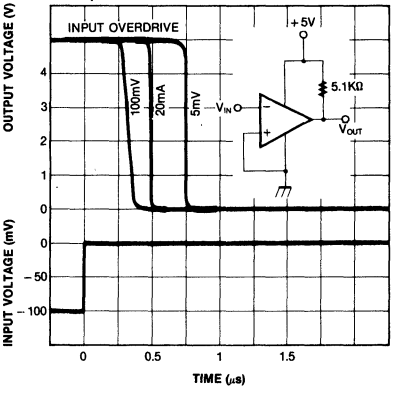
INPUT CURRENT V_S SUPPLY VOLTAGE



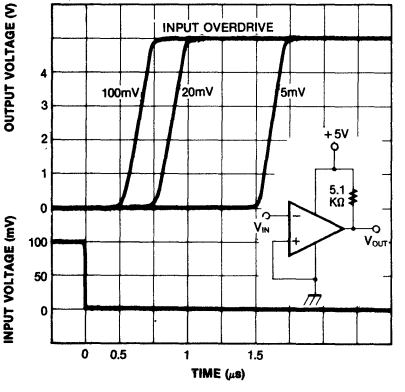
OUTPUT SATURATION VOLTAGE



RESPONSE TIME



RESPONSE TIME



APPLICATION INFORMATION

The LM239 series includes four high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input output coupling; reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

It is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than −0.3V should not be used: an input clamping diode can be used as protection.

The output LM339 is the uncommitted collector of a NPN transistor with grounded emitter. This allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16 mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltage will rise very rapidly.

Under this limit, the output saturation voltageis limited by the approximatively 60Ω r_{sat} of the output transistor.

TYPICAL APPLICATIONS (V_{CC} = +15V)

Basic comparator

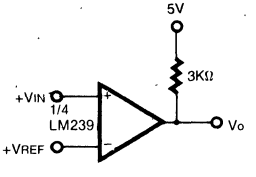


Fig. 6

Non-inverting comparator with Hysteresis

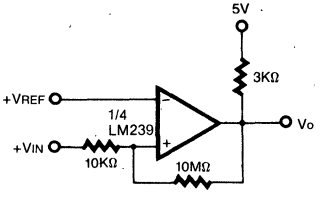


Fig. 7

Inverting comparator with Hysteresis

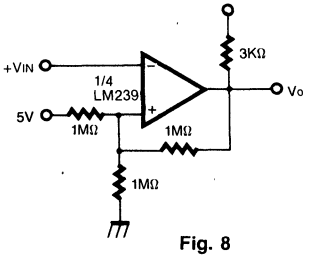


Fig. 8

Driving C/MOS

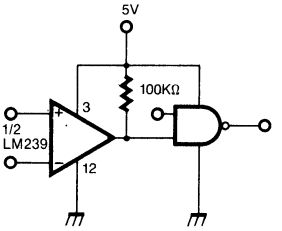


Fig. 9

Driving TTL

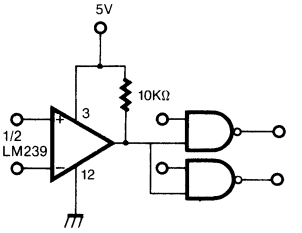


Fig. 10

AND gate

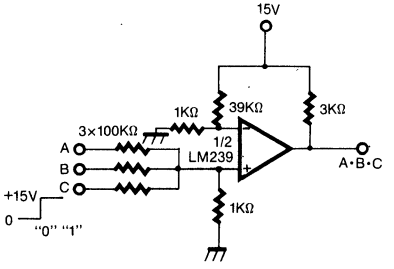


Fig. 11

OR gate

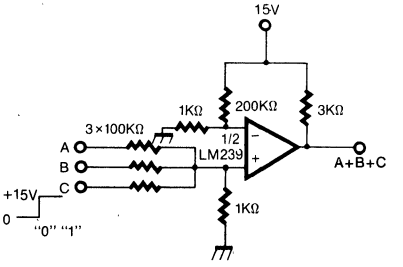


Fig. 12

Large fan-in AND gate

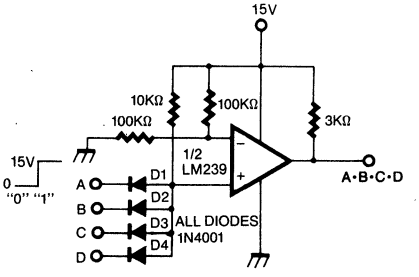


Fig. 13

Squarewave oscillator

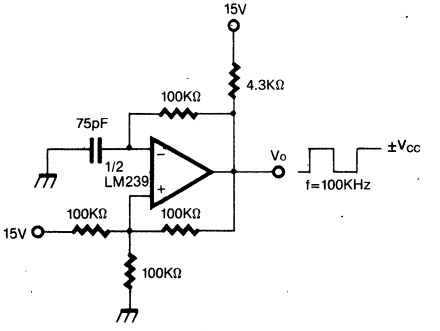


Fig. 14

ORing the outputs

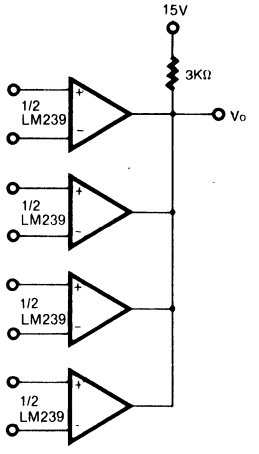


Fig. 15

Peak audio level display

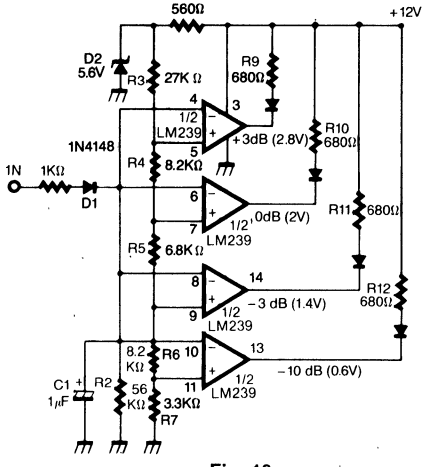


Fig. 16

Zero crossing detector (single supply)

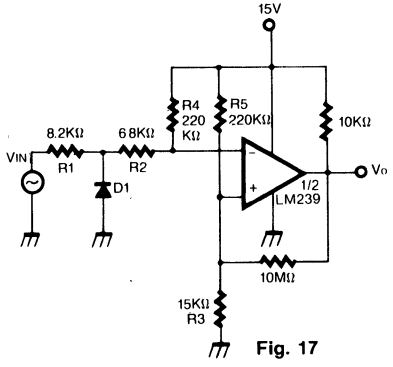


Fig. 17

Zero crossing detector (split supplies)

$V_{INmin} \approx 0.4V$ peak for 1% phase distortion ($\Delta\theta$)

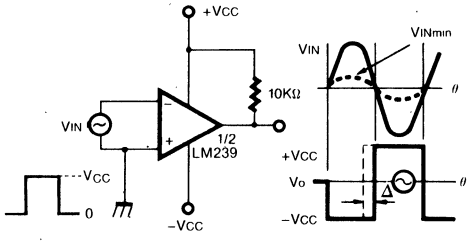


Fig. 18

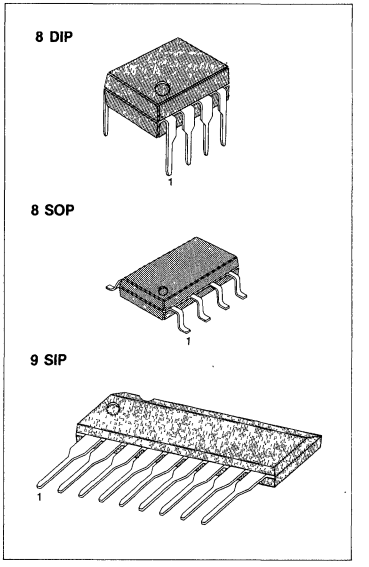
D1 prevents input from going negative by more than 0.6V:

$$R1+R2=R3$$

$R3 \leqslant R5/10$ for smaller error in zero crossing

DUAL DIFFERENTIAL COMPARATOR

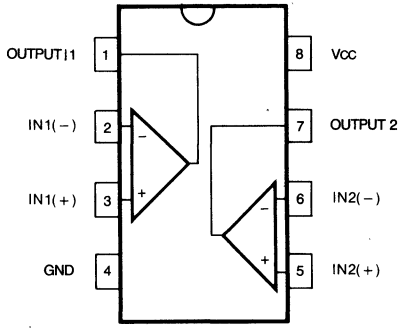
The LM293 series consists of two independent voltage comparators that one designed to operate from a single power supply over a wide range of voltage.

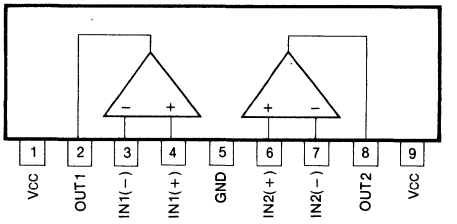


FEATURES

- **Single Supply Operation: 2V to 36V**
- **Dual Supply Operation: ±1V to ±18V**
- **Allow Comparison of Voltages Near Ground Potential**
- **Low Current Drain 800μA Typ**
- **Compatible with all Forms of Logic**
- **Low Input Bias Current 25nA Typ**
- **Low Input Offset Current ±5nA Typ**
- **Low Offset Voltage ±2mV Typ**

BLOCK DIAGRAM

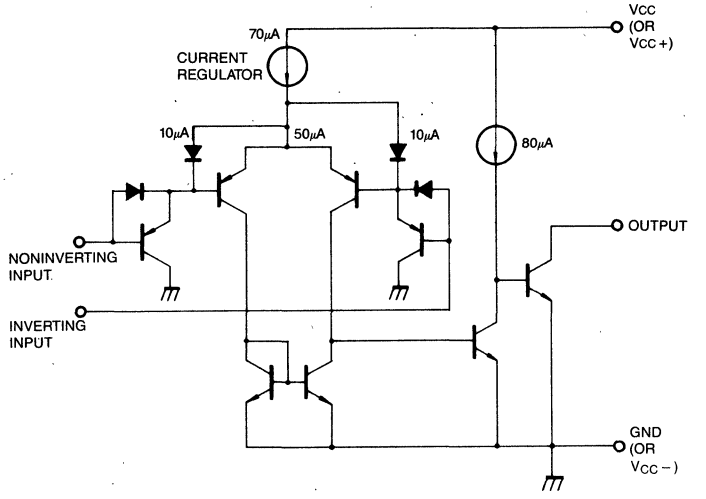




ORDERING INFORMATION

Device	Package	Operating Temperatur
LM293N LM293AN	8 DIP	−25 ~ +85°C
LM293S	9 SIP	
LM293D LM293AD	8 SOP	
LM393N LM393AN	8 DIP	0 ~ +75°C
LM393S	9 SIP	
LM393D LM393AD	8 SOP	
LM2903N	8 DIP	−40 ~ +85°C
LM2903D	8 SOP	

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_S	±18 or 36	V
Differential Input Voltage	V_{ID}	36	V
Input Voltage	V_I	−0.3 to +36	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P_D	570	mW
Operating Temperature LM293/LM293A LM393/LM393A LM2903	T_{opr}	 −25~+85 0~+70 −40~+85	 °C °C °C
Storage Temperature	T_{stg}	−65~+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM293A/LM393A			LM293/LM393			Unit
				Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_s = 0			±1	±2		±1	±5	mV
			$T_{amin} \leq T_a \leq T_{amax}$			±4.0			±9.0	
Input Offset Current	I_{IO}				±5	±50		±5	±50	nA
			$T_{amin} \leq T_a \leq T_{amax}$			±150			±150	
Input Bias Current	I_B				25	250		25	250	nA
			$T_{amin} \leq T_a \leq T_{amax}$			400			400	
Input Common Mode Voltage Range	V_{ICR}			0		V_{CC}-1.5	0		V_{CC}-1.5	V
			$T_{amin} \leq T_a \leq T_{amax}$	0		V_{CC}-2	0		V_{CC}-2	
Supply Current	I_{CC}	R_L = ∞			0.4	1		0.4	1	mA
		R_L = ∞ V_{CC} = 36V			1	2.5		1	2.5	
Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq$ 15KΩ(for large V_o swing)		50	200		50	200		V/mV
Large Signal Response Time	t_{RES1}	V_{IN} = TTL Logic Swing, V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ			300			300		nS
Response Time	t_{RES2}	V_{RL} = 5V, R_L = 5.1KΩ			1.3			1.3		μS
Output Sink Current	I_{sink}	$V_{IN}^- \geq$ 1V, V_{IN}^+ = 0V, $V_o \leq$ 1.5V		6	16		6	16		mA
Output Saturation Voltage	V_{sat}	$V_{IN}^- \geq$ 1V, V_{IN}^+ = 0V, I_{sink} = 4mA			250	400		250	400	mV
			$T_{amin} \leq T_a \leq T_{amax}$			700			700	
Output Leakage Current	I_{leak}	V_{IN}^- = 0, V_{in}^+ = 1V	V_o = 5V		0.1			0.1		nA
			V_o = 30V			1.0			1.0	μA

* $T_{amin} \leq T_a \leq T_{amax}$
LM293/LM293A: T_{amin} = −25°C, T_{amax} = +85°C
LM393/LM393A: T_{amin} = 0°C, T_{amax} = +70°C
LM2903: T_{amin} = −45°C, T_{amax} = +85°C

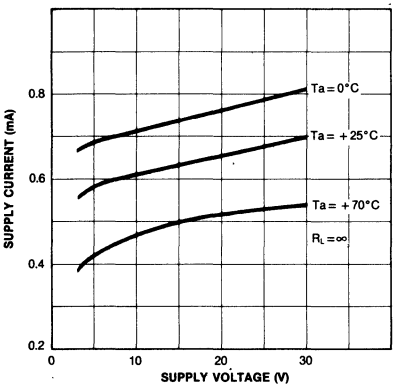
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM2903 Min	LM2903 Typ	LM2903 Max	Unit
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V, V_o = 1.4V, R_s = 0			±2	±7	mV
			$T_{amin} \leq T_a \leq T_{amax}$		±9	±15	
Input Offset Current	I_{IO}				±5	±50	nA
			$T_{amin} \leq T_a \leq T_{amax}$		±50	±200	
Input Bias Current	I_B				25	250	nA
			$T_{amin} \leq T_a \leq T_{amax}$			500	
Input Common Mode Voltage Range	V_{ICR}	V_{CC} = 30V		0		V_{CC}-1.5	V
			$T_{amin} \leq T_a \leq T_{amax}$	0		V_{CC}-2	
Supply Current	I_{CC}	$R_L = \infty$			0.4	1	mA
		$R_L = \infty$ V_{CC} = 36V			1	2.5	
Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq$ 15KΩ (for large V_o swing)		25	100		V/mV
Large Signal Response Time	t_{RES1}	V_{IN} = TTL Logic Swing, V_{ref} = 1.4V, V_{RL} = 5V, R_L = 5.1KΩ			300		nS
Response Time	t_{RES2}	V_{RL} = 5V, R_L = 5.1KΩ			1.5		μS
Output Sink Current	I_{sink}	$V_{IN}^- \geq$ 1V, V_{IN}^+ = 0V, $V_o \leq$ 1.5V		6	16		mA
Output Saturation Voltage	V_{sat}	$V_{IN}^- \geq$ 1V, V_{IN}^+ = 0V, I_{sink} = 4mA			250	400	mV
			$T_{amin} \leq T_a \leq T_{amax}$			700	
Output Leakage Current	I_{leak}	V_{IN}^- = 0,	V_o = 5V		0.1		nA
		V_{in}^+ = 1V	V_o = 30V			1.0	μA

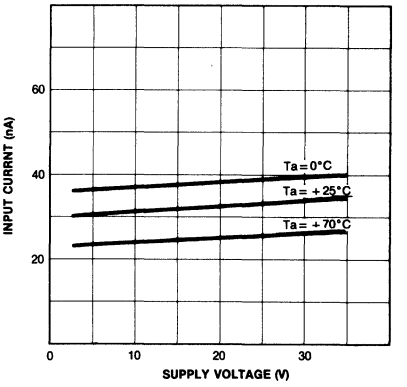
* $T_{amin} \leq T_a \leq T_{amax}$
LM293/LM293A: T_{amin} = −25°C, T_{amax} = +85°C
LM393/LM393A: T_{amin} = 0°C, T_{amax} = +70°C
LM2903: T_{amin} = −45°C, T_{amax} = +85°C

TYPICAL PERFORMANCE CHARACTERISTICS

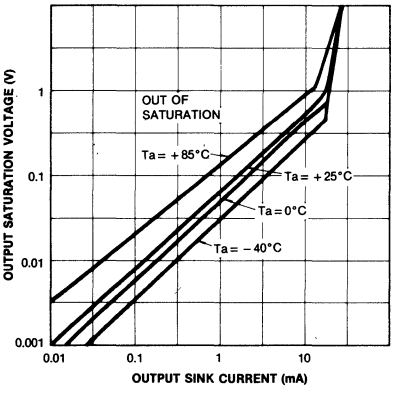
SUPPLY CURRENT V_S SUPPLY VOLTAGE



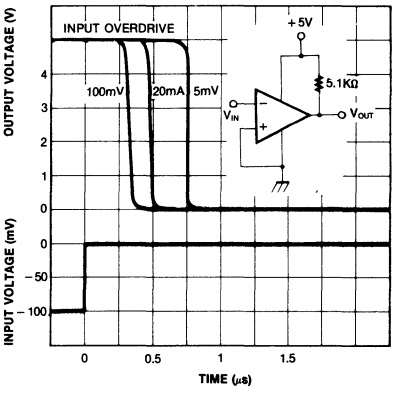
INPUT CURRENT V_S SUPPLY VOLTAGE



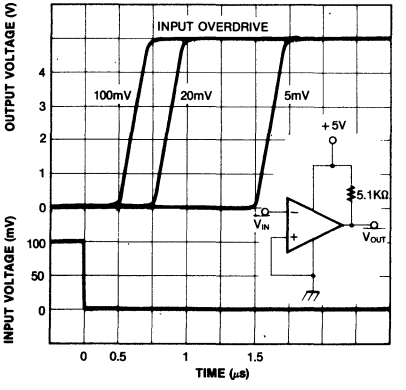
OUTPUT SATURATION VOLTAGE



RESPONSE TIME



RESPONSE TIME



APPLICATION INFORMATION

The LM293 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output is inadvertently allowed to capacitively couple to the inputs via stray capacitance. That occurs during the output voltage transitions, when the comparator changes state.

To minimize this problem, PC board layout should be designed to reduce stray input-output coupling, reducing the input resistors to less than 10KΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible.

If is good design practice to ground all unused pins.

The differential input voltage may be larger than positive supply without damaging the device. Note that voltages more negative than −0.3V should not used: an input clamping diode can be used as protection.

The output of the LM239 series is the uncommitted collector of a NPN transistor with grounded emitter. The allows the device to be used like any open-collector gate providing the OR-wide facility.

The output sink current capability is approximately 16mA; if this limit is exceeded, the output transistor will come out of saturation and the output voltate will rise very rapidly.
Under this limit, the output saturation voltage is limited by the approximatively 60Ω r_{sat} of the output transistor.

TYPICAL APPLICATIONS (V_{CC} = + 15V)

Basic comparator

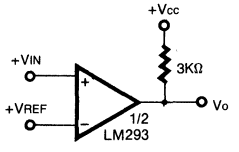


Fig. 3

Non-inverting comparator with Hysteresis

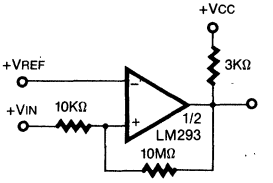


Fig. 4

Inverting comparator with Hysteresis

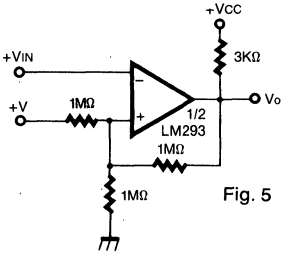


Fig. 5

Driving C-MOS

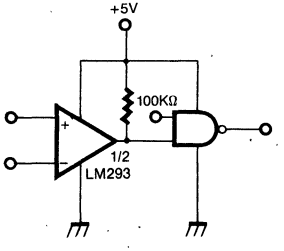


Fig. 6

Driving TTL

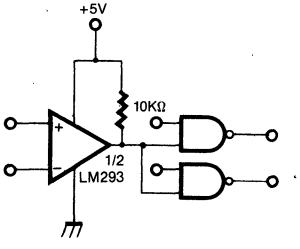


Fig. 7

APPLICATION INFORMATION (continued)

AND gate

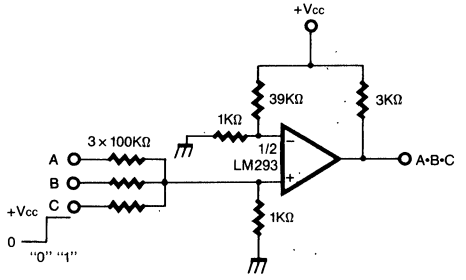


Fig. 8

OR gate

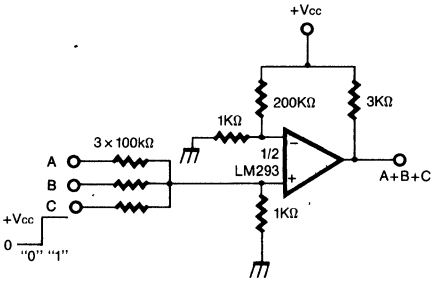


Fig. 9

Large fan-in AND gate

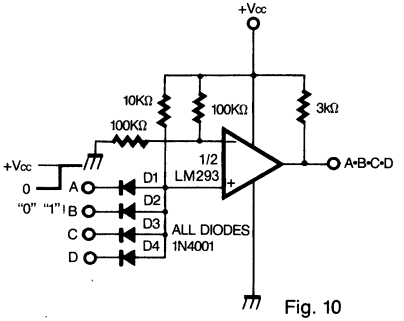


Fig. 10

Squarewave oscillator

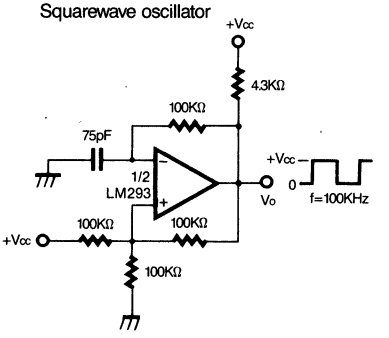


Fig. 11

Pulse generator

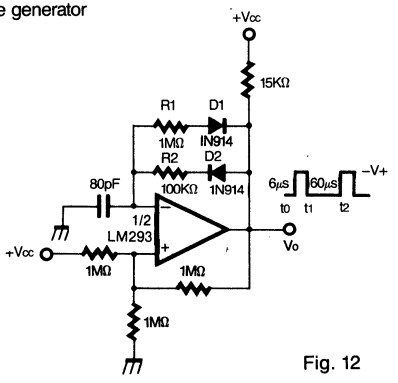


Fig. 12

One-shot multivibrator

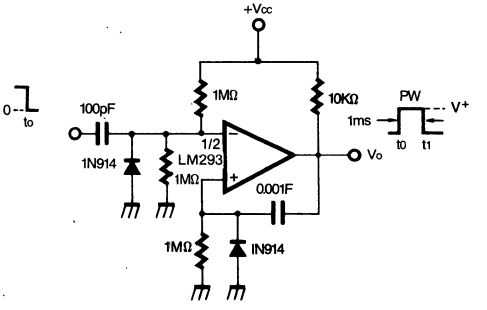


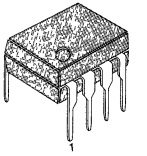
Fig. 13

CMOS TIMER

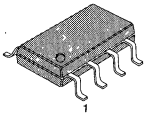
The KS555 is CMOS RC timer providing significantly improved performance over the standard NE555, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the KS555 is stable controller capable of producing accurate time delays or frequencies. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555 device, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuit is triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

8 DIP



8 SOP



FEATURES

- **Exact equivalent in most cases for NE555.**
- **Low Supply Current: 80μA Typ.**
- **Extremely low trigger, threshold and reset current: 20pA Typ.**
- **High speed operation: 500KHz**
- **Wide operation supply voltage range: 2 to 18 Volts**
- **Normal reset function: No crowbarring of supply during output transition.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Highly immunized to static charge**

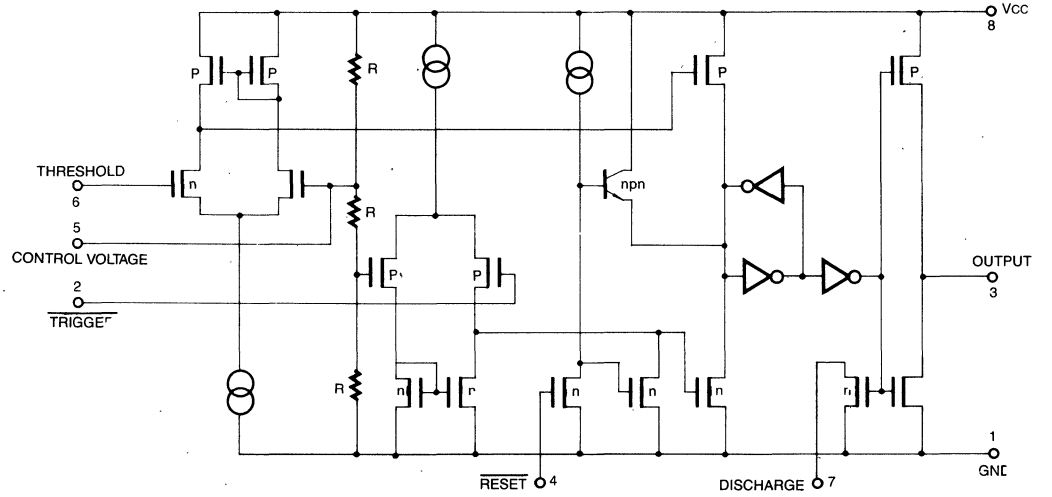
APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

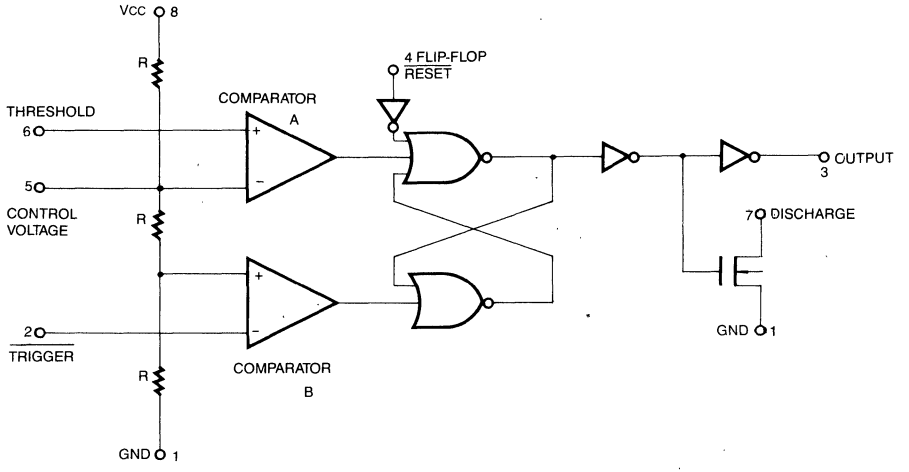
ORDERING INFORMATION

Device	Package	Operating Temperature
KS555N	8 DIP	−20 ~ +85°C
KS555D	8 SOP	

SCHEMATIC DIAGRAM



BLOCK DIAGRAM



This block diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.
R = 100KΩ ± 20% Typ.

TRUTH TABLE

Threshold Voltage	Trigger Voltage	Reset	Output	Discharge Switch
Don't Care	Don't Care	Low	Low	On
> 2/3 (V_{CC})	> 1/3 (V_{CC})	High	Low	On
< 1/3(V_{CC}) ~ 2/3(V_{CC})	> 1/3(V_{CC}) ~ 2/3(V_{CC})	High	Stable	Stable
Don't Care	< 1/3 (V_{CC})	High	High	Off

Note: $\overline{\text{RESET}}$ will dominate all other input.$\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Voltage ($\overline{\text{Trigger}}$, Control Voltage, Threshold and $\overline{\text{Reset}}$)	V_{IN}	−0.3 ~ V_{CC} + 0.3	V
Output Current	I_{OUT}	100	mA
Power Dissipation	P_D	200	mW
Operating Temperature Range	T_{opr}	−20 ~ +85	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

Note 1: Stresses above those listed under absolute maximum rating may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 2 to 15 Volts unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}	$-20°C < T_a < +70°C$	2		18	V
Supply Current	I_{CC}	V_{CC} = 2V		60	200	μA
		V_{CC} = 18V		120	300	μA
Timing Error	MT	$R_a = R_b$ = 1KΩ to 100KΩ C = 0.1μF, $5V \leq V_{CC} \leq 15V$				
Initial Accuracy				2.0	5.0	%
Drift With Temperature		V_{CC} = 5V		50		ppm/°C
		V_{CC} = 10V		75		ppm/°C
		V_{CC} = 15V		100		ppm/°C
Drift With Supply Voltage		V_{CC} = 5V		1.0	3.0	%/V
Threshold Voltage	V_{TH}	V_{CC} = 5V	0.63	0.66	0.67	V_{CC}
Trigger Voltage	V_{TR}	V_{CC} = 5V	0.29	0.33	0.34	V_{CC}
Trigger Current	I_{TR}	V_{CC} = 18V		50		pA
		V_{CC} = 5V		10		pA
		V_{CC} = 2V		1		pA
Threshold Current	I_{TH}	V_{CC} = 18V		50		pA
		V_{CC} = 5V		10		pA
		V_{CC} = 2V		1		pA
Reset Current	I_{RE}	V_{RST} = GND V_{CC} = 18V		100		pA
		V_{RST} = GND V_{CC} = 5V		20		pA
		V_{RST} = GND V_{CC} = 2V		2		pA
Reset Voltage	V_{RE}	V_{CC} = 18V	0.4	0.7	1.0	V
		V_{CC} = 2V	0.4	0.7	1.0	V
Control Voltage	V_C	V_{CC} = 5V	0.62	0.66	0.67	V_{CC}
Output Voltage Drop	V_{OL}	V_{CC} = 18V, I_{SINK} = 3.2mA		0.1	0.4	V
		V_{CC} = 5V, I_{SINK} = 3.2mA		0.15	0.4	V
	V_{OH}	V_{CC} = 18V, I_{source} = 1.0mA	17.25	17.8		V
		V_{CC} = 5V, I_{source} = 1.0mA	4.0	4.5		V
Rise Time of Output	T_r	R_L = 10MΩ, C_L = 10pF, V_{CC} = 5V	35	40	75	ns
Fall Time of Output	T_f		35	40	75	ns
Guaranteed Max Osc. Freq.	F_{max}	Astable Operation	500			KHz

APPLICATION NOTES

General

The KS555 device is, in most instances, a direct replacement for the NE555 device. However, it is possible to effect economies in the external component count using the KS555. Because the bipolar 555 device produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The KS555 device produce no such transients. See Figure 1.

The KS555 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an KS555.

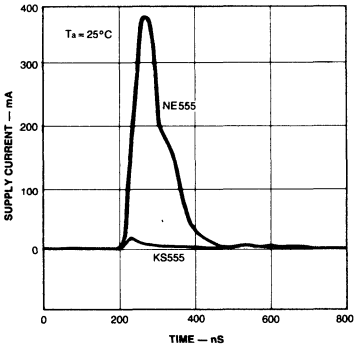


Fig 1. Supply current transient compared with a standard bipolar 555 during an output transition

Power Supply Considerations

Although the supply current consumed by the KS555 device is very low, the total system can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 2. and 3.

Output Drive Capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the KS555 will drive at least 2 standard TTL loads.

Astable Operating

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 2. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4RC}$$

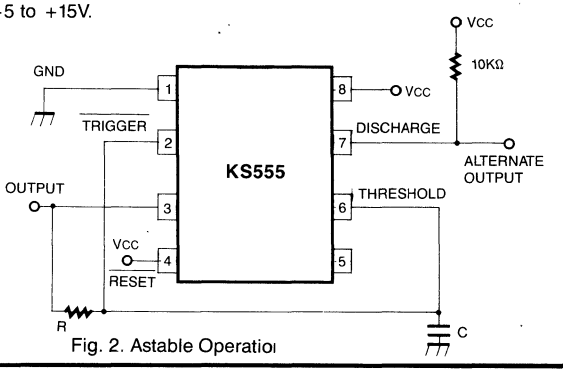


Fig. 2. Astable Operatio

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharaged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant t=RaC.

When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip flop, which in turn discharge the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

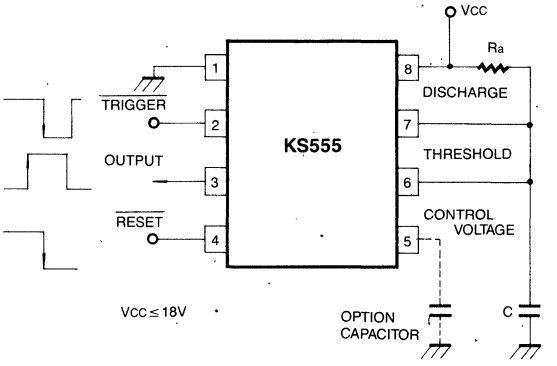


Fig. 3. Monostable Operation

Control Voltage

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

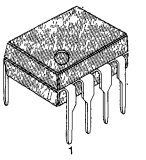
$\overline{\text{Reset}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

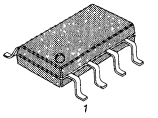
CMOS TIMER

The KS555H is monolithic integrated circuit fabricated using CMOS process. Due to its high impedance inputs (threshold, trigger, reset), it is capable of producing accurate time delay and oscillation using less expensive, smaller timing capacitors than NE555.
Another features are very low power consumption and high speed astable operation and very low voltage operation.

8 DIP



8 SOP



FEATURES

- **Very low power consumption: 1.2mW**
- **Very high speed operation: 2MHz**
- **Complementary CMOS output capable of switching rail-to-rail**
- **Output fully CMOS-, TTL-, and MOS- compatible**
- **Exactly equivalent in most cases for NE555 or 556 (dual timer) or the 355**
- **Well behaved reset function**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **Highly immuned to static charge**

APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

BLOCK DIAGRAM

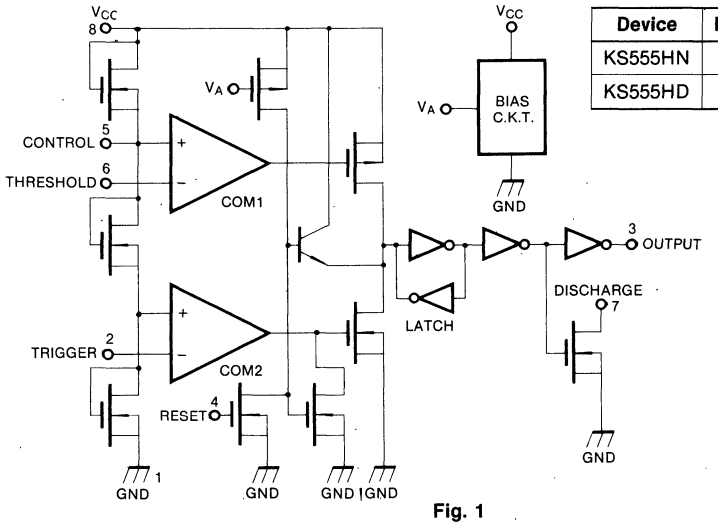


Fig. 1

ORDERING INFORMATION

Device	Package	Operating Temperature
KS555HN	8 DIP	0 ~ +70°C
KS555HD	8 SOP	

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Voltage (Trigger, Reset, Threshold)	V_{IN}	$-0.3 \sim V_{CC}$	V
Lead Temperature (Soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{opr}	$0 \sim 70$	°C
Storage Temperature Range	T_{stg}	$-65 \sim 150$	°C

ELECTRICAL CHARACTERISTICS

($Ta = 25°C$, $V_{CC} = 5V$, refer to application circuit unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		18	V
Supply Current	I_{CC}			240		μA
		$V_{CC} = 15V$		480		μA
Control Voltage	V_C			3.33		V
		$V_{CC} = 15V$		10		V
Threshold Voltage	V_{TH}			3.33		V
		$V_{CC} = 15V$		10		V
Threshold Current	I_{TH}	$V_{CC} = 5V$		50		PA
Trigger Voltage	V_{TR}			1.67		V
		$V_{CC} = 15V$		5		V
Trigger Current	I_{TR}			50		PA
Reset Voltage	V_{RE}			0.7	1	V
Reset Current	I_{RE}			50		PA
Low Level Output Voltage	V_{OL}	$I_{OL} = 5mA$		0.1		V
		$I_{OL} = 8mA$		0.15		V
		$V_{CC} = 15V$				
		$I_{OL} = 10mA$		0.1		V
		$I_{OL} = 50mA$		0.5		V
		$I_{OL} = 100mA$		1		V
High Level Output Voltage	V_{OH}	$I_{OH} = -1mA$		4.5		V
		$I_{OH} = -2mA$		4		V
		$V_{CC} = 15V$				
		$I_{OH} = -1mA$		14.8		V
		$I_{OH} = -5mA$		14		V
		$I_{OH} = -10mA$		12.7		V

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Initial Error of Timing Interval	T_{EI}	V_{CC} = 5 to 15V, $R_A = R_B$ = 1 to 100K, C_T = 0.1μF		1		%
Timing Error Due to Supply Drift	T_{ES}			0.1		%/V
Rise Time of Output	T_r	R_l = 10MΩ, C_l = 10pF		20		nS
Fall Time of Output	T_f			20		nS
Maximum Astable Oscillation	F_{MAX}	R_A = 470Ω, R_B = 200Ω, C_T = 200pF		2.1		MHz

4

APPLICATION CIRCUIT

1) ASTABLE

The circuit can be connected to trigger itself and free run as multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}.
As in the trigger mode, the charging and discharging times, and therefore the frequency are essentially independently of the supply voltage.
The frequency of oscillation is given by

$f = 1/T = 1.44/(R_A + 2 \times R_B)/C$

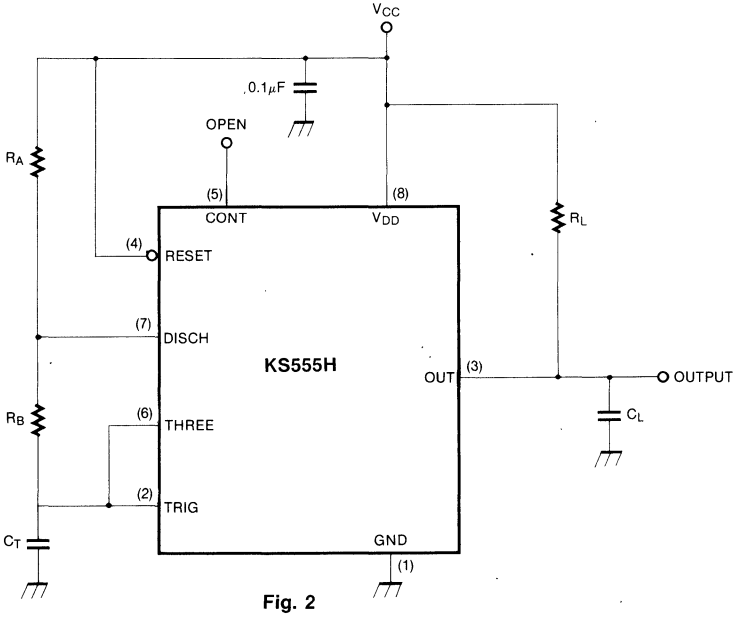


Fig. 2

2) MONOSTABLE

In this mode of operation, the timer functions as one shot. Initially, the external capacitor C is held discharged by a transistor inside timer. Upon application of negative trigger pulse to pin 2, the flip flop is set which releases the short circuit across the external capacitor and drives the output high.
The voltage across the external capacitor now increases exponentially with a time constant T = RA*C. When the voltage across the external capacitor equals 2/3*V_{CC}, the comparator resets the flip flop, which in turn discharges the capacitor repidly and also drives the output to its state.

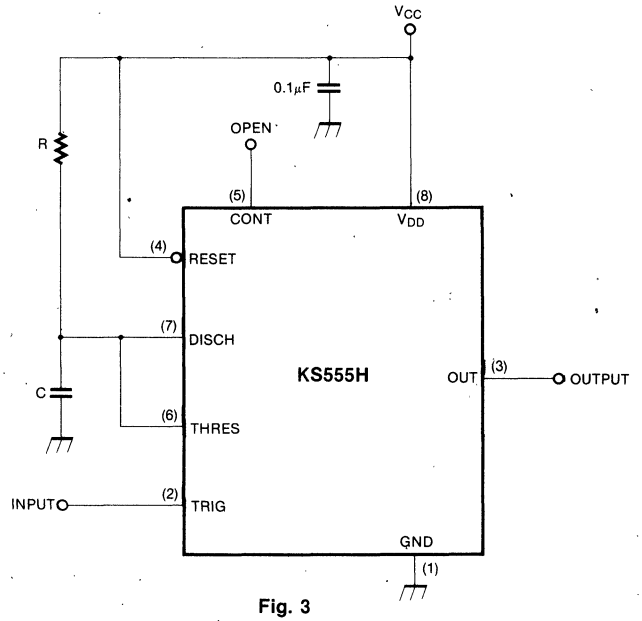
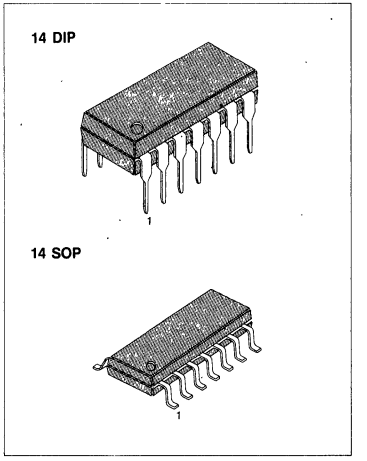


Fig. 3

CMOS TIMER

The KS556 is monolithic integrated circuit fabricated using C-MOS process. Due to high impedance inputs (Trigger, Threshold, Reset), it is capable of producing accurate time delay using less expensive, smaller timing capacitor than NE556.

Another features one very low power consumption and high speed astable operation and very low voltage operation.



FEATURES

- **Very low power consumption: 2.4mW**
- **Very high speed operation: 2MHz**
- **Output fully CMOS, TTL, and MOS compatible**
- **Timing from microseconds through hours**
- **Adjustable duty cycle**

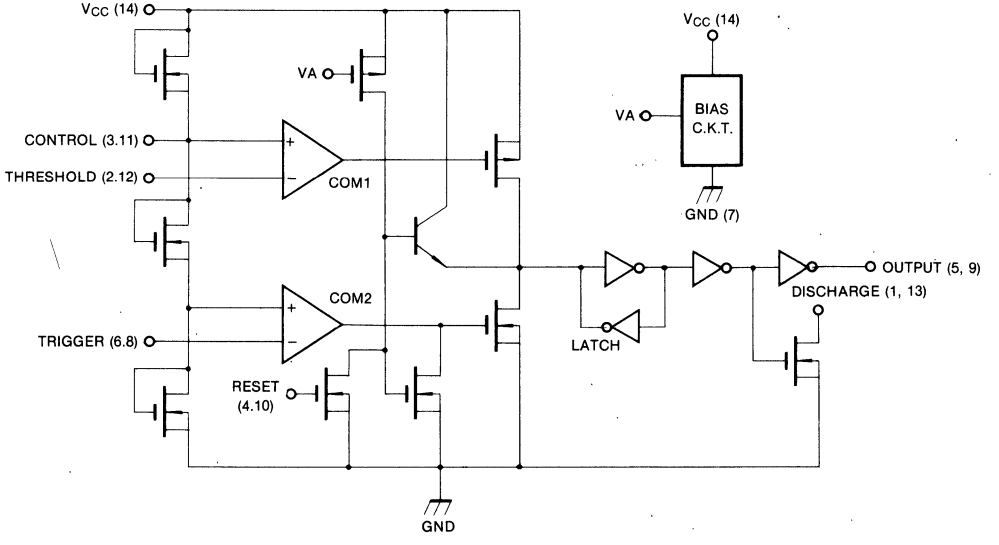
APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation

ORDERING INFORMATION

Device	Package	Operating Temperature
KS556N	14 DIP	0 ~ +70°C
KS556D	14 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Input Voltage (Trigger, Reset, Threshold)	V_{IN}	$-0.3 \sim V_{CC}$	V
Lead Temperature (Soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{opr}	$0 \sim +70$	°C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

ELECTRICAL CHARACTERISTICS

($Ta = 25°C$, $V_{CC} = 5V$, refer to application circuit unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		3		18	V
Supply Current	I_{CC}			240		μA
		$V_{CC} = 15V$		480		
Control Voltage	V_C			3.33		V
		$V_{CC} = 15V$		10		
Threshold Voltage	V_{TH}			3.33		V
		$V_{CC} = 15V$		10		
Threshold Current	I_{TH}			50		pA
Trigger Voltage	V_{TR}			1.67		V
		$V_{CC} = 15V$		5		
Trigger Current	I_{TR}			50		pA
Reset Voltage	V_{RE}			0.7		V
Reset Current	I_{RE}			50		pA
Low Level Output Voltage	V_{OL}	$I_{OL} = 5mA$		0.1		V
		$I_{OL} = 8mA$		0.15		
		$V_{CC} = 15V$ $I_{OL} = 10mA$		0.1		
		$V_{CC} = 15V$ $I_{OL} = 50mA$		0.5		
		$V_{CC} = 15V$ $I_{OL} = 100mA$		1		
High Level Output Voltage	V_{OH}	$I_{OH} = -1mA$		4.5		V
		$I_{OH} = -2mA$		4		
		$V_{CC} = 15V$ $I_{OH} = -1mA$ $I_{OH} = -5mA$ $I_{OH} = -10mA$		14.8 14 12.7		

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Initial Error of Timing Interval	T_{EI}	V_{CC} = 5 to 15V $R_A = R_B$ = 1 to 100K C_T = 0.1μF		1		%
Supply Voltage Sensitivity of Timing Interval	T_{ES}			0.1		%/V
Rise Time	T_r	R_L = 10MΩ, C_L = 10pF		20		nS
Fall Time	T_f	R_L = 10MΩ, C_L = 10pF		20		nS
Maximum Astable Oscillation	F_{max}	R_A = 470Ω, R_B = 200Ω C_T = 200pF		2		MHz

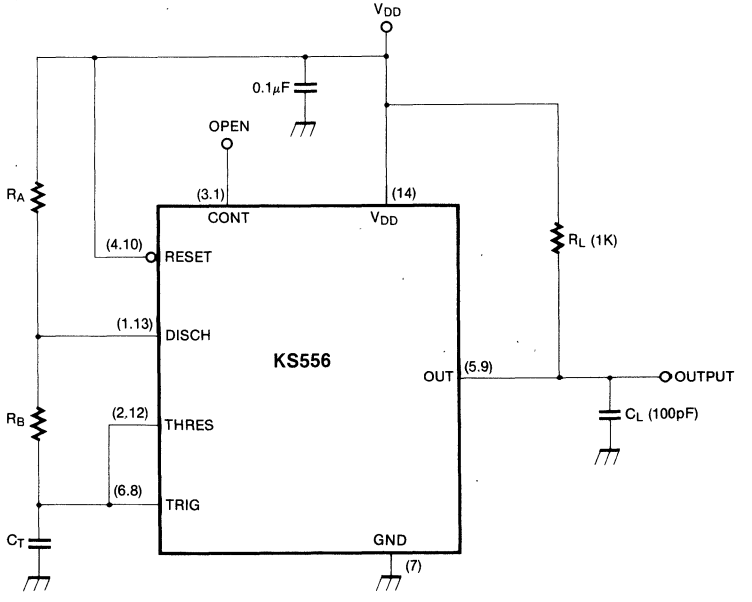
4

APPLICATION CIRCUIT

1) Astable

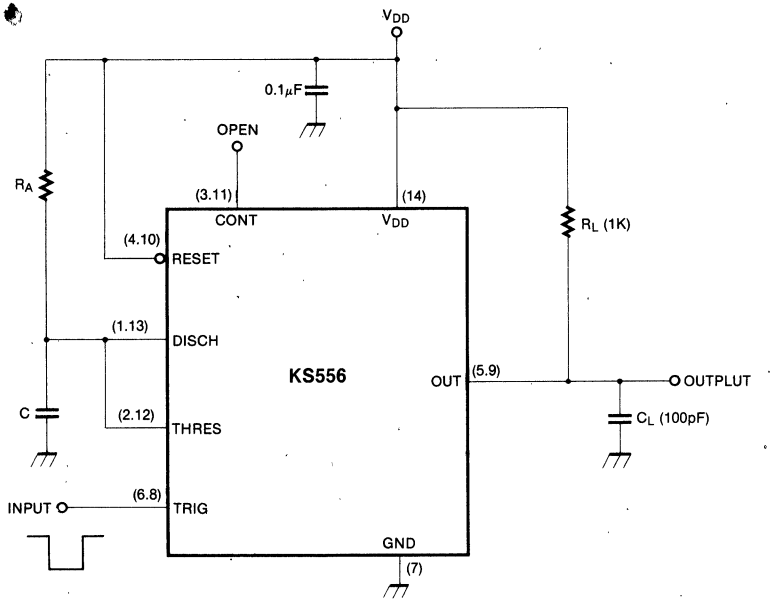
The circuit can be connected to trigger itself and free runs as multivibrator. The external capacitor chrages through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}.
As in the trigger mode, the charging and discharging times, and therefore the frequency, are essentially independently of the supply voltage. These frequency of oscillation is given by

$$F = 1/T = 1.44/(R_A + 2*R_B)/C$$



2) Monostable

In this mode of operation, the timer functions as one shot. Initially, the external capacitor (C) is held discharged by a transistor inside timer. Upon application of negative trigger pulse to trigger pin the flip flop is set which releases the short circuit across the external capacitor and drives the output high.
The voltage across the external capacitor now increases exponentially with time constant $T = R_A \times C$. When the voltage across the external capacitor equals $2/3 \times V_{CC}$, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the output to its state.

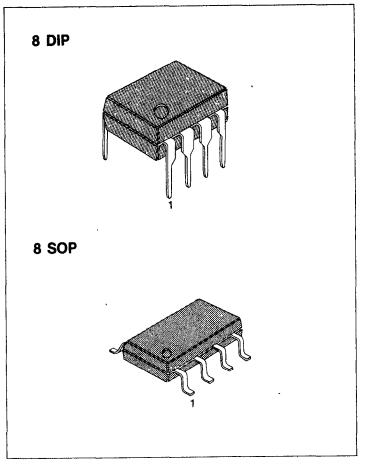


TIMER

The NE555 series are a monolithic integrated circuit and high stable device for generating accurate time delay or oscillation.

FEATURES

- **Turn off time less than 2μs**
- **Maximum operating frequency greater than 500KHz**
- **Timing from microseconds to hours**
- **Operates in both astable and monostable modes**
- **High output current**
- **Adjustable duty cycle**
- **Temperature stability of 0.005% per °C**



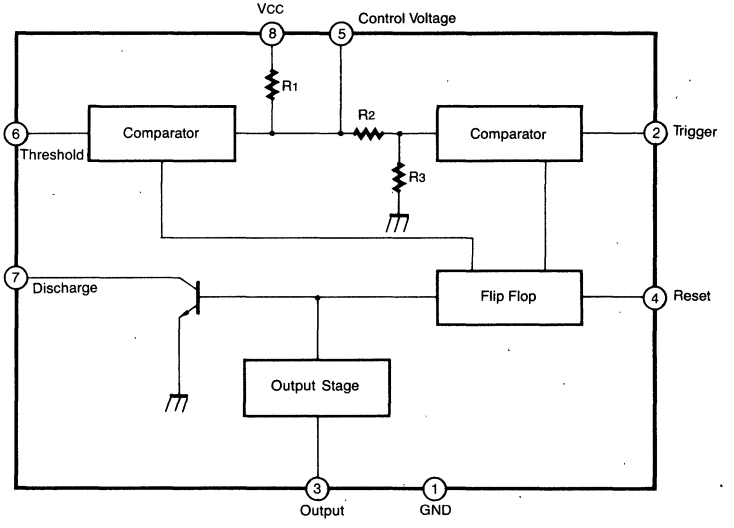
APPLICATIONS

- Precision timing
- Time delay generation
- Pulse generation
- Pulse position modulation
- Sequential timing
- Missing pulse detector

ORDERING INFORMATION

Device	Package	Operating Temperature
NE555IN	8 DIP	– 40 ~ + 85°C
NE555ID	8 SOP	
NE555CN	8 DIP	0 ~ + 70°C
NE555CD	8 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range NE555I	T_{opr}	−40 ~ +85	°C
NE555C		0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 5 ~ 15V, unless otherwise specified)

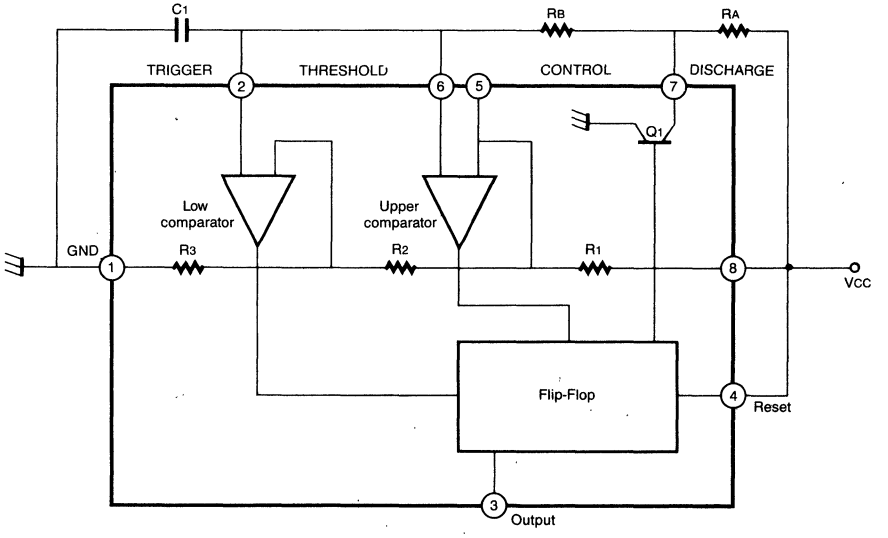
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current *1(low stable)	I_{CC}	V_{CC} = 5V, R_L = ∞		3	6	mA
		V_{CC} = 15V, R_L = ∞		10	15	mA
*Timing Error (Monsotable)	MT_1					
[2]Initial Accurary		R_A = 1KΩ to 100KΩ		1.0	3.0	%
Drift with Temperature		C = 0.1μF		50		ppm/°C
Drift with Supply Voltage				0.1	0.5	%/V
*Timing Error (astable)	MT_2					
[2]Initial Accurary		R_A = 1K to 100KΩ		2.25		%
Drift with Temperature		C = 0.1μF		150		ppm/°C
Drift with Supply Voltage				0.3		%/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V		10.0		V
		V_{CC} = 5V		3.33		V
*[3]Threshold Current	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_{TR}	V_{CC} = 5	1.1	1.67	2.2	V
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5	5.6	V
Trigger Current	I_{TR}	V_T = 0V		0.5	2.0	μA
Reset Voltage	V_{RE}		0.4	0.7	1.0	V
Reset Current	I_{RE}			0.1	0.4	mA

ELECTRICAL CHARACTERISTICS

(T_a=25°C, V_{CC}=5~15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (low)	V_{OL}	V_{CC}=15V I_{sink}=10mA I_{sink}=50mA		0.1 0.4	0.25 0.75	V V
		V_{CC}= 5V I_{sink}=5mA		0.25	0.35	V
Output Voltage (high)	V_{OH}	V_{CC}=15V I_{source}=200mA I_{source}=100mA	 12.75	12.5 13.3		V V
		V_{CC}=5V I_{source}=100mA	2.75	3.3		V
Rise Time of Output	T_r			100		nsec
Fall Time of Output	T_f			100		nsec
Discharge Leakage Current	I_D			20	100	nA

APPLICATION CIRCUIT



Notes:

1. Supply current when output is high is typically 1mA less at V_{CC}=5V.
2. Tested at V_{CC}=5.0V and V_{CC}=15V
3. This will determine the maximum value of R_A+R_B for 15V operation, the max total R=20MΩ, and for 5V operation the max total R=6.7MΩ.

APPLICATION NOTE

The application circuit shows astable mode.
The pin 6 (threshold) tied to the pin 2 (trigger) and pin 4 (reset) tied to V_{CC} (pin 8).
The external capacitor C_1 of pin 6 and pin 2 charges through R_A, R_B and discharges through R_B only.
In the internal circuit of the NE555 one input of upper comparator is the 2/3 V_{CC} ($^*R_1 = R_2 = R_3$), another input of it connected pin 6.
As soon as charging C_1 is higher than 2/3 V_{CC}, discharge transistor Q_1 turn on and C_1 discharges to collector of transistor Q_1.
Therefore flip-flop circuit is reset and output is low.
One input of lower comparator is the 1/3 V_{CC}, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B.
Therefore flip-flop circuit is set and output is high.
So to say, when C_1 charges through R_A and R_B output is high and when C_1 discharges through R_b output is low
The charge time (output is high) T_1 is 0.693 $(R_A + R_B)$ C_1 and the discharge time (output is low) T_2 is 0.693 $(R_B C_1)$.

$$\left(\ln \frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}} = 0.693\right)$$

Thus the total period time T is given by
$T = T_1 + T_2 = 0.693\,(R_A + 2R_B).\,C_1$.
Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C_1}$$

The duty cycle is given by

$$D.C = \frac{T_2}{T} = \frac{R_B}{R_A + 2R_B}$$

If you make use of the NE556 you can make two astable mode.
If you want another application note, request information on our timer IC application circuit designer.

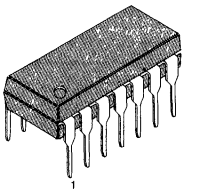
DUAL TIMER

The NE556 series dual monolithic timing circuits are a highly stable controller capable of producing accurate time delays or oscillation.

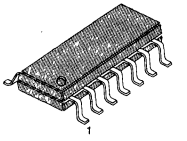
The NE556 is a dual NE555. Timing is provided an external resistor and capacitor for each timing function.

The two timers operate independently of each other, sharing only V_{CC} and ground.
The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

14 DIP



14 SOP



FEATURES

- **Direct replacement for NE556**
- **Replace two NE555 timers**
- **Operates in both astable and monostable modes**
- **High output current**
- **TTL compatible**
- **Timing from microsecond to hours**
- **Adjustable duty cycle**
- **Temperature stability of 0.005% per °C**

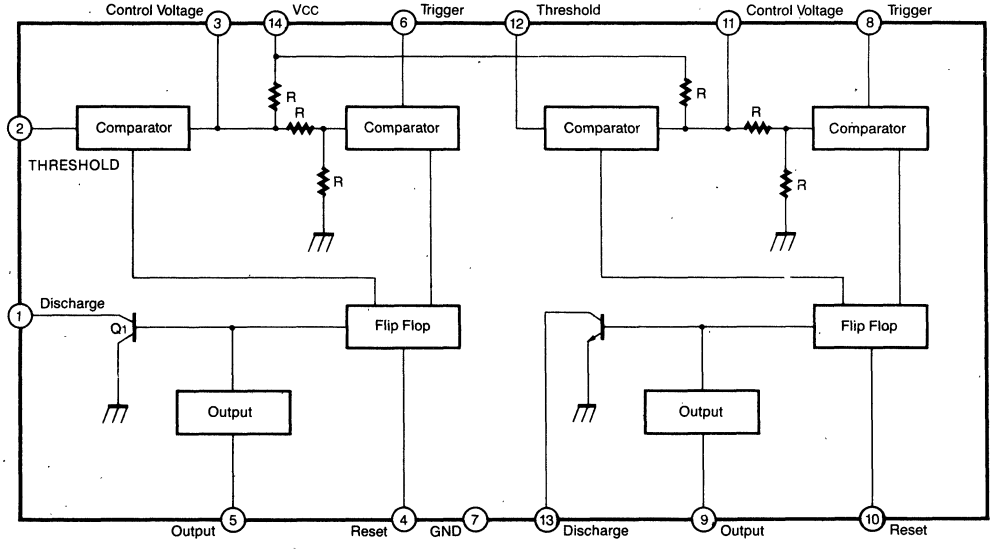
APPLICATIONS

- Precision timing
- Pulse shaping
- Pulse width modulation
- Frequency division
- Traffic light control
- Sequential timing
- Pulse generator
- Time delay generator
- Touch tone encoder
- Tone burst generator

ORDERING INFORMATION

Device	Package	Operating Temperature
NE556IN	14 DIP	−40 ~ +85°C
NE556ID	14 SOP	
NE556CN	14 DIP	0 ~ +70°C
NE556CD	14 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range NE556I	T_{opr}	−40 ~ +85	°C
NE556C		0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V to +15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
*1 Supply Current (Two timers) (low state)	I_{CC}	V_{CC} = 5V, $R_L = \infty$ V_{CC} = 15V, $R_L = \infty$		6 20	12 30	mA mA
*2 Timing Error (monostable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	MT_1	R_A = 2KΩ to 100KΩ C = 0.1μF T = 1.1R_C		 0.75 50 0.1		 % % %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V		10.0		V
		V_{CC} = 5V		3.33		V
*3 Threshold Current	I_{TH}			30	250	nA
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5.0	5.6	V
		V_{CC} = 5V	1.1	1.67	2.2	V
Trigger Current	I_{TR}	V_T = 0V		0.5	2.0	μA
*5 Reset Voltage	V_{RE}		0.4	0.7	1.0	V
Reset Current	I_{RE}			0.1	0.6	mA
Output Voltage Low	V_{OL}	V_{CC} = 15V I_{sink} = 10mA I_{sink} = 50mA I_{sink} = 100mA I_{sink} = 200mA V_{CC} = 5V I_{sink} = 8mA I_{sink} = 5mA		 0.1 0.4 2.0 2.5 0.25 0.15	 0.25 0.75 2.75 0.35 0.25	 V V V V V V

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V to +15V, unless otherwise specified)

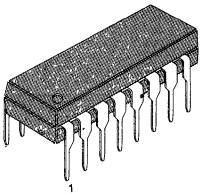
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (high)	V_{OH}	V_{CC} = 15V I_{source} = 200mA I_{source} = 100mA	 12.75	 12.5 13.3		 V V
		V_{CC} = 5V I_{source} = 100mA	2.75	3.3		V
Rise Time of Output	T_r			100		nsec
Fall Time of Output	T_f			100		nsec
Discharge Leakage Current	I_D			20	100	nA
*4 Matching Characteristics Initial Accuracy Drift with Temperature Drift with Supply Voltage	M_{CH}			 1.0 10 0.2	 2.0 0.5	 % ppm/°C %/V
*2 Timing Error (astable) Initial Accuracy Drift with Temperature Drift with Supply Voltage	MT_2	R_A, R_B = 1kΩ to 100kΩ C = 0.1μF V_{CC} = 15V		 2.25 150 0.3		 % ppm/°C %/V

Notes:
1. Supply current when output is high is typically 1.0mA less at V_{CC} = 5V.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. This will determine the maximum value of $R_A + R_B$ for 15V operation.
   The maximum total R = 20MΩ, and for 5V operation the maximum total R = 6.6MΩ.
4. Matching characteristic refer to the difference between performance characteristics of each timer section in the monostable mode.
5. As reset voltage lowers, timing is inhibited and then the output goes low.

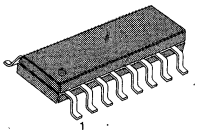
QUAD TIMER

The NE558 series are a monolithic Quad Timers which can be used to produce four entirely independent timing functions. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. The time is precisely controlled by one external resistor and one capacitor in the time delay mode. A stable mode can be operated by using two of four timer sections.

16 DIP



16 SOP



FEATURES

- **Wide supply voltage range: 4.5V to 16V**
- **100mA output current per section**
- **Edge triggered without coupling capacitor**
- **Time period equals RC**
- **Output independent of trigger conditions.**

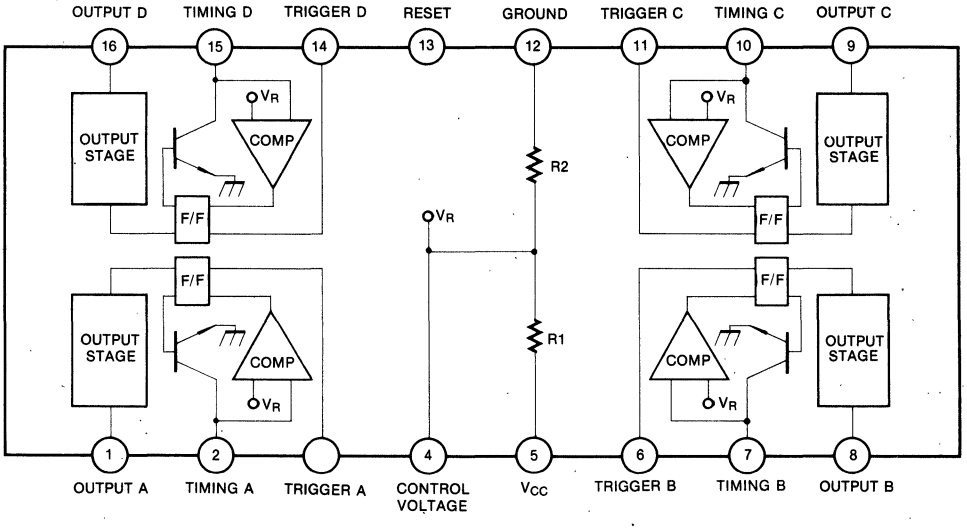
APPLICATIONS

- Quad one-shot
- Sequential timing
- Precision timing
- **Time delay generation**

ORDERING INFORMATION

Device	Package	Operating Temperature
NE558IN	14 DIP	−45 ~ +85°C
NE558CN	14 DIP	0 ~ +70°C
NE558CD	14 SOP	

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range NE556I	T_{opr}	−40 ~ +85	°C
NE556C		0 ~ 70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ~ 15V, Ta = 25°C unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current	I_{CC}	V_{CC} = 15V, reset voltage = 15V		16	36	mA
Timing Error (T = RC) Initial Accuracy	M_T	R = 2KΩ to 100KΩ, C = 1μF		±2	5	%
Drift with Temperature				30	150	PPM/°C
Drift with Supply Voltage				0.1	0.9	%/V
[1]Trigger Voltage	V_{TR}	V_{CC} = 15V	0.8	1.5	2.4	V
[1]Trigger Current	I_{TR}	Trigger voltage = 0V		50	100	μA
[2]Reset Voltage	V_{RE}	Reset	0.8		2.4	V
[2]Reset Current	I_{RE}	Reset		50	500	μA
Threshold Voltage	V_{TH}			0.63 × V_{CC}		V
Threshold Current	I_{TL}			15		nA
[3]Output Voltage	V_{OUT}	I_L = 10mA		0.1	0.4	V
		I_L = 100mA		1.0	2.0	
Output Leakage Current	I_{OL}			10	500	nA
Propagation Delay Time	T_P			1.0		μS
Rise Time	T_r	I_L = 100mA		100		nS
Fall Time	T_f	I_L = 100mA		100		nS

NOTES: 1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8V, outputs set low and trigger inhibited.
3. Output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is nomally low sinking current.

APPLICATIONS

- **Long-Time Delay**

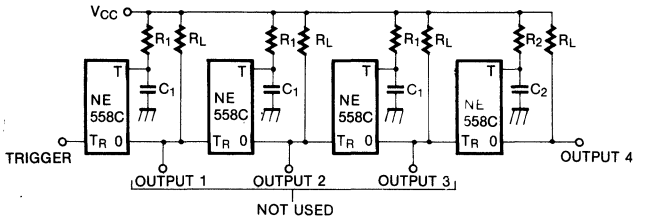


Fig. 1. Circuit

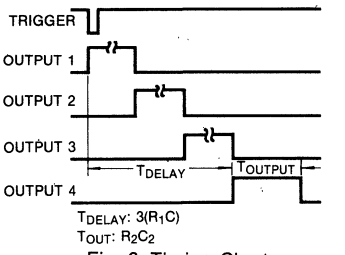


Fig. 2. Timing Chart

- **Ring Counter**

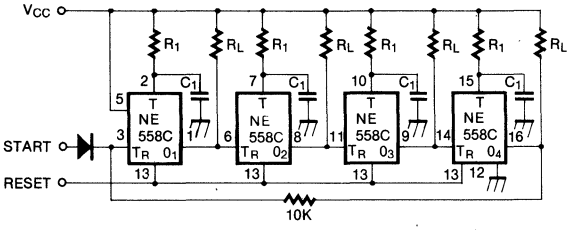


Fig. 3. Circuit

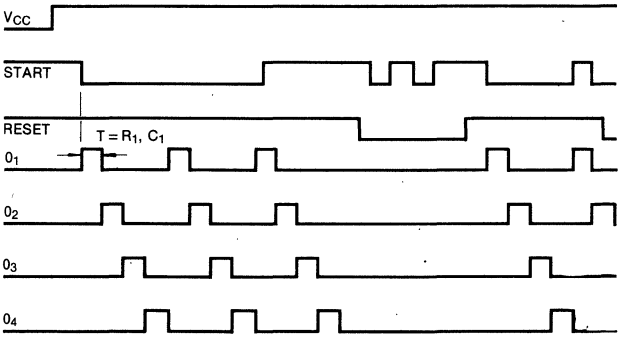
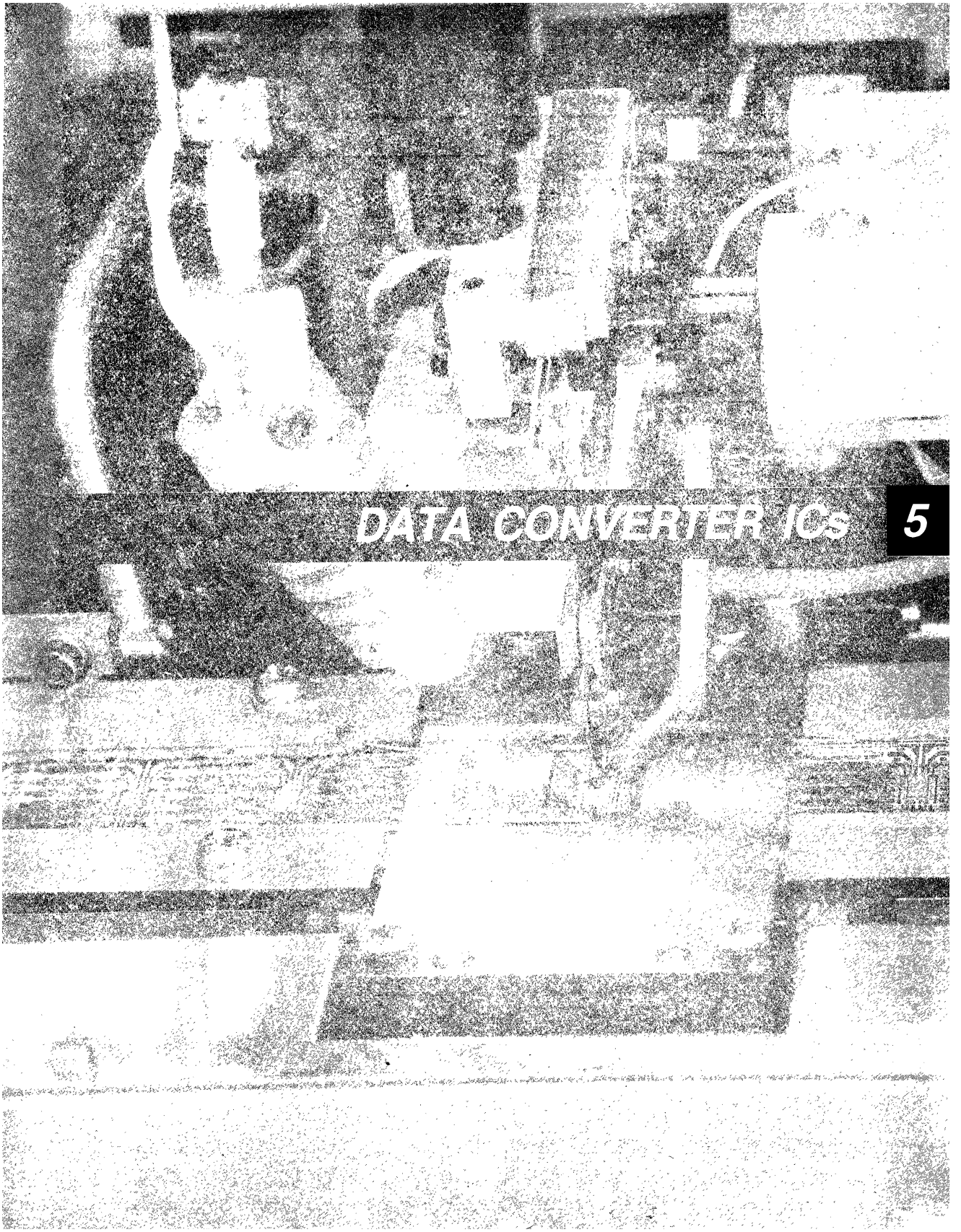


Fig. 4. Timing Chart



DATA CONVERTER ICs

5

Data Converter Application

Device	Function	Package	Page
KSV3100A	High-Speed A/D-DA Converter	40 DIP	521
KSV3110	High-Speed A/D-DA Converter	40 DIP	531
KSV3208	High-Speed A/D Converter	28 DIP	541
KAD0808	8 Bit μp-Compatible A/D Converter with 8-Channel Multiplexer	28 DIP	549
KAD0809	8 Bit μp-Compatible A/D Converter with 8-Channel Multiplexer	28 DIP	549
KAD0820A/B	8 Bit High Speed μp Compatible A/D Converter with Track/Hold Function	20 DIP	560
KDA0800	8 Bit D/A Converter	16 DIP	580
KDA0801	8 Bit D/A Converter	16 DIP	580
KDA0802	8 Bit D/A Converter	16 DIP	580
KS25C02	8 Bit CMOS Successive Approximation Register	16 DIP	586
KS25C03	8 Bit CMOS Successive Approximation Register	16 DIP	586
KS25C04	12 Bit CMOS Successive Approximation Register	24 SDIP	586
KS7126	3 1/2 Digit A/D Converter	40 DIP	568

HIGH-SPEED A/D-D/A CONVERTER

Samsung KSV3100A, VLSI circuit in CI (Collector Implanted) technology, consists of a high-speed flash-type 8-bit A/D converter and a high-speed low-glitch 10-bit D/A converter designed as an R-2R network with switched current sources. Also, the various auxiliary circuits, as reference voltage sources, pre-amplifier, input clamping circuit and feed-in output amplifier are integrated on the single chip.

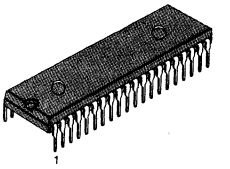
KSV3100A has been developed for use in all applications which call for a high-speed A/D-D/A converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcast.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although KSV3100A was initially designed as high-speed codecs for the video range, it can be used with equal benefits for lower frequencies, even down to zero.

40 DIP



5

BLOCK DIAGRAM

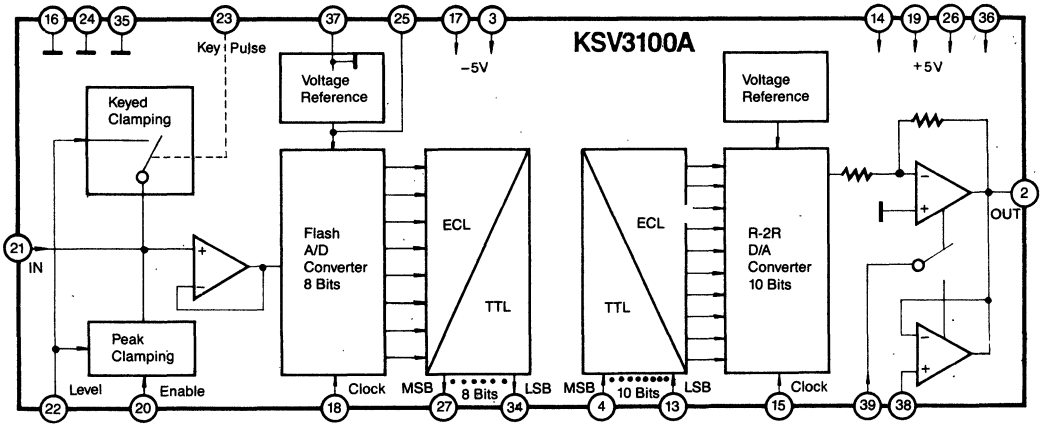


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input, in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping or peak clamping or without clamping. Also the D/A converter's reference voltage is generated on-chip, and a gated amplifier is arranged at the output of the D/A converter so that an external analog signal can be fed-in instead of the signal delivered by the D/A converter.

Separate clock inputs are provided for the A/D converter and the D/A converter thus enabling the application of time compression procedures.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	No Connection	21	Analog Input A/D Converter
2	Analog Output D/A Converter	22	Clamping Level Input
3	−5V Supply D/A Converter-Analog	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	−5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	No Connection

RECOMMENDED OPERATING CIRCUIT

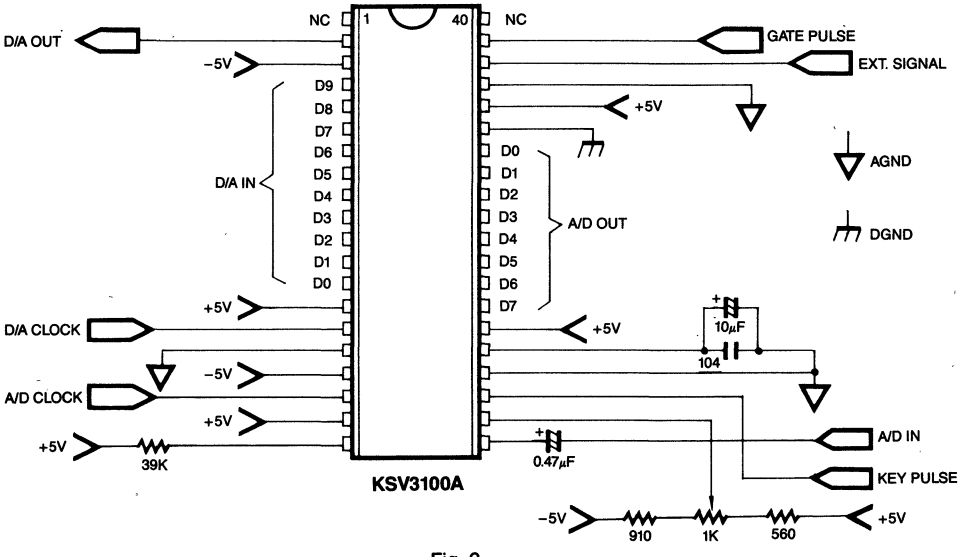


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	6	V
Negative Supply Voltage	V_{EE}	−6	V
Input Voltages (Digital)	V_I	−0.5 ~ V_{CC} +0.5	V
Input Voltages (Analog)	V_I	−0.5 ~ V_{CC} +0.5	V
Output Current Pin 2	I_o	± 10	mA
Ambient Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5	−5.25	V
A/D Converter					
Analog Input Voltage	V_I	0	—	2	V
Input Frequency, Analog Input	f_I	—	—	$f_{cl}/2$	—
Clock Amplitude	V_{18H}	2.0	—	V_{CC}	V
	V_{18L}	0	—	0.8	V
Conversion Rate	f_{18}	0	—	20	MSPS*
Clock High Time (See Fig. 3)	t_H	15	—	—	ns
Clock Low Time (See Fig. 3)	t_L	35	—	—	ns
A/D Output Voltage	V_{OH}	2.4	—	V_{CC}	V
	V_{OL}	0	—	0.4	V
Clamping Level	V_{22}	−1	—	+2	V
Clamping Pulse	V_{23H}	2.0	—	V_{CC}	V
	V_{23L}	0	—	0.8	V
Activation of Peak Clamping	—	Resistor of 20 to 60KΩ from Pin 20 to +5V			—
D/A Converter					
Clock Amplitude	V_{15H}	2.0	—	V_{CC}	V
	V_{15L}	0	—	0.8	V
Conversion Rate	f_{15}	0	—	20	MSPS*
Digital Input Voltage	V_{IH}	2.0	—	V_{CC}	V
	V_{IL}	0	—	0.8	V
Analog Input Voltage at Pin 38	V_{38}	−1	—	+3	V
Output Signal Switch Over Input					
for the D/A Converter Out	V_{39}	0	—	0.8	V
for the Ext. Signal (from Pin 38) Out	V_{39}	2	—	V_{CC}	V

* MSPS (Mega Sample Per Second)

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{EE} = −5V, f_{15} = 20MHz, f_{18} = 20MHz, Ta = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC} I_{EE}	— —	90 −80	120 −110	mA mA
Power Dissipation	P_{TOT}	—	—	1.2	W
Total Transfer Time A/D-D/A	t_{TOT}	See Fig. 3			—
A/D Converter					
Input Current Pin 21	I_I	—	2	—	μA
Input Capacitance Pin 21	C_I	—	10	—	pF
Input Impedance Pin 21					
at f = 1KHz	Z_I	—	20	—	MΩ
at f = 10MHz	Z_I	—	100	—	KΩ
3dB Bandwidth of the Input Amp.	—	—	50	—	MHz
Keyed Clamping Active Level	V_{23}	2.0	—	V_{CC}	V
On Resistance of the Clamping Switch Between Pin 21 and 22	R_{ON}	—	300	—	Ohm
Input Current of the Clamping Level Input Pin 22 (V_{20} = 3V, V_{22} = 2V)	I_{22}	—	150	—	μA
Aperture Delay (② in Fig. 3)	t_{AD}	—	—	10	ns
Digital Output Delay (③ in Fig. 3)	t_{DV}	—	25	—	ns
Transfer Time (⑥ in Fig. 3)	t_W	One clock period			—
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	8	—	—
Code of the Digital Output Signal	—	Binary			—
Output CODE at the Input with V_{21} = 0V with V_{21} = V_{ref}	 — —	 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1			 — —
Internal Reference Voltage	V_{25}	1.8	2.0	2.2	V
D/A Converter					
Output Impedance Pin 2	Z_O	—	15	—	Ω
Input Current Pin 38 (V_{38} = 2V)	I_{ID}	—	0.6	—	mA
Internal Reference Voltage	V_{ref}	1.8	2.0	2.2	V
Input Resister Hold Time (⑦ in Fig. 3)	t_{IH}	6.0	—	—	ns
Input Resister Setup Time (⑧ in Fig. 3)	t_{IH}	20	—	—	ns
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	10	—	—
Code of the Digital Input Signal	—	Binary			—
Output Signal at the Input with 0 0 0 0 0 0 0 0 0 0 with 1 1 1 1 1 1 1 1 1 1	 V_2 V_2	 — —	 0 2	 — —	 V V
Settling Time	t_S	—	50	—	ns

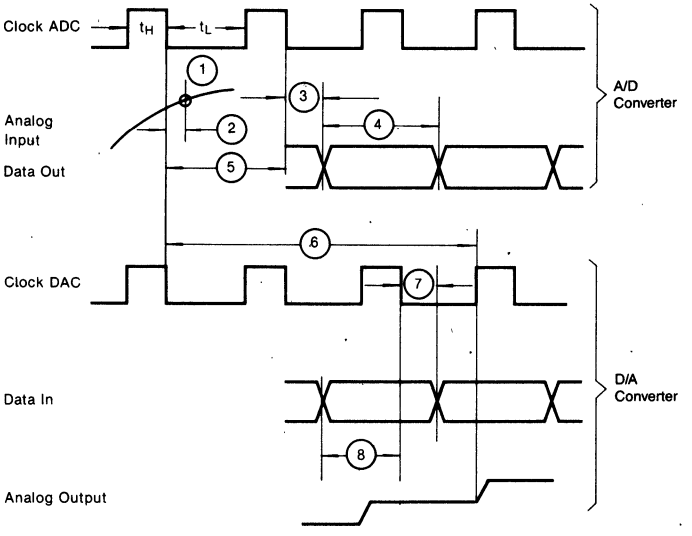
ORDERING INFORMATION

KSV3100A has four kind of version according to the accuracy bit (so called 'Precision') of D/A Converter, and their marking specifications are as follow;

Device	Package	Temperature Range	D/A Converter		A/D Converter
			Accurary Bit	Diff. Nonlinearity	Diff. Nonlinearity
KSV3100ACN-10	40 DIP	0 ~ +70°C	10 bit	± 1/2 LSB	± 1/2 LSB
KSV3100ACN-9			9 bit	± 1 LSB	
KSV3100ACN-8			8 bit	± 2 LSB	
KSV3100ACN-7			7 but	± 4 LSB	

* The accuracy of A/D Converter can be guaranteed as '8 bit' (differential nonlinearity = ± 1/2 LSB) regardless of the D/A Converter's accuracy.

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D
⑥ Total Transfer Time A/D-D/A with Common Clock
⑦ Input Register Hold Time
⑧ Input Register Setup Time

Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

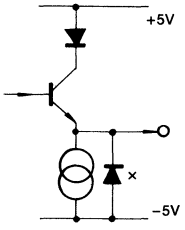


Fig. 4: Pin 2, Output

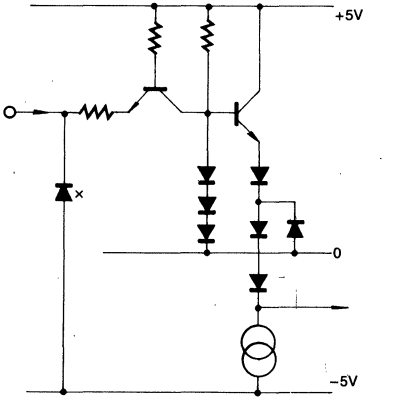


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

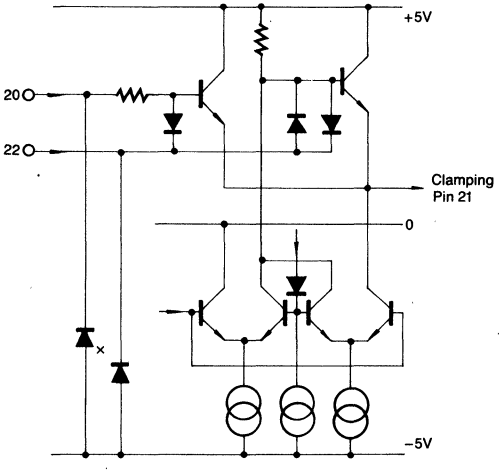


Fig. 6: Pins 20 and 22, Inputs

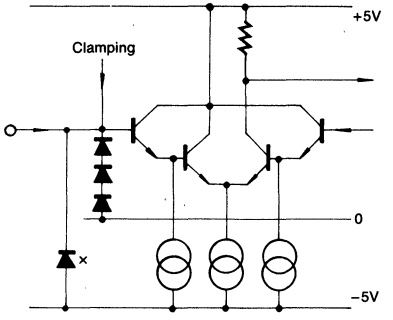


Fig. 7: Pin 21, Input

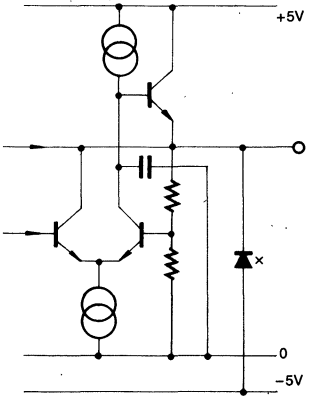


Fig. 8: Pin 25, Reference Voltage Pin

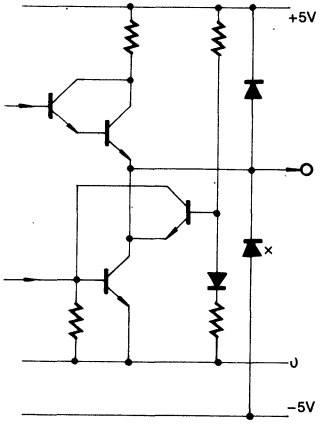


Fig. 9: Pins 27 to 34, Outputs

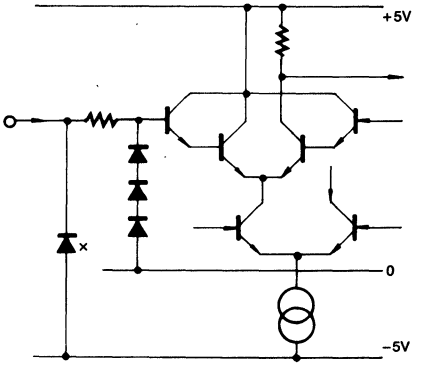


Fig. 10: Pin 38, Input
x = protection diode

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	No Connection
Pin 2	Analog Output D/A Converter This pin whose diagram is shown in Fig. 4, is the output for the processed analog signal either originating from the D/A converter or from the external analog input pin 38.
Pin 3	−5 Volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+5 Volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin whose diagram is shown in Fig. 5 must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.
Pin 17	−5 Volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5. Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+5 Volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via pin 20 whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS (Continued)

Pin No.	Description
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Fig. 5 is the diagram of this input. Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as ground pin for the analog part of the A/D converter.
Pin 25	Reference Voltage A/D Converter This pin whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to pin 37.
Pin 26	+5 Volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 9 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+5 Volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference Voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3100A instead of the D/A-converted signal originating from pin 4 to 13.
Pin 39	Output Signal Switchover Input This pin whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to pin 38.
Pin 40	No Connection

APPENDIX: APPLICATION CIRCUITS

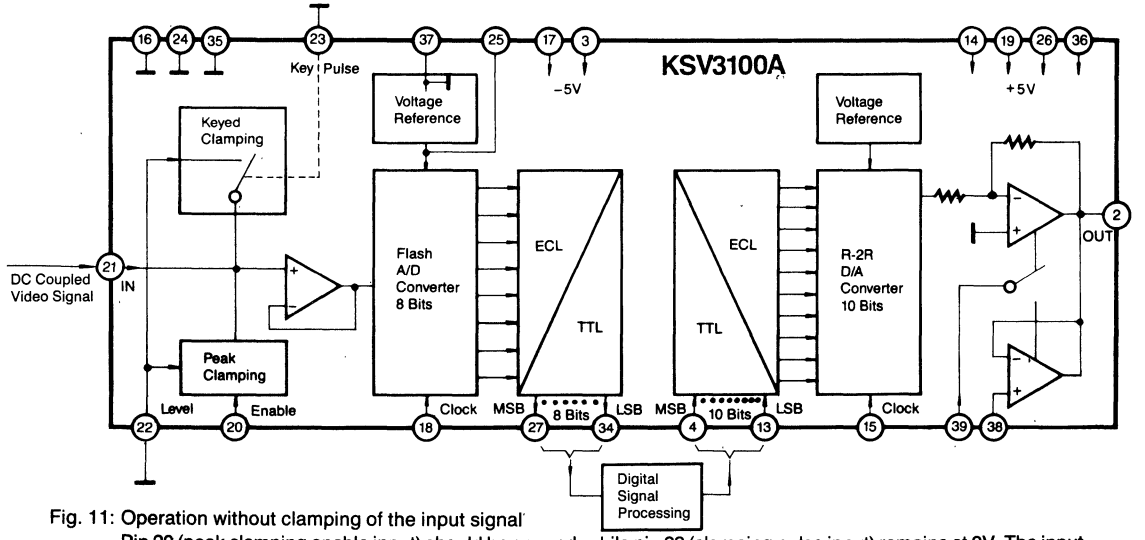


Fig. 11: Operation without clamping of the input signal
Pin 20 (peak clamping enable input) should be opened, while pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 21, without coupling capacitor such that it lies between 0 and +2V.

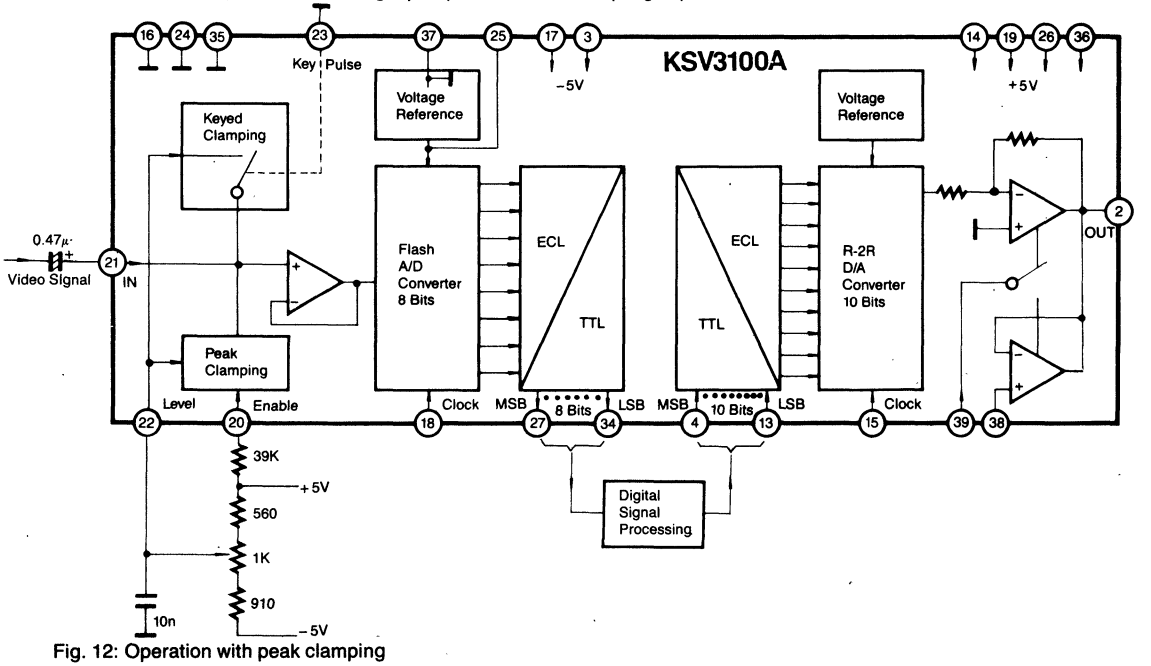


Fig. 12: Operation with peak clamping
The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and pin 22 (clamping level input) is connected, as desired, to zero or a voltage between −1 and +2V. The input signal is fed to pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

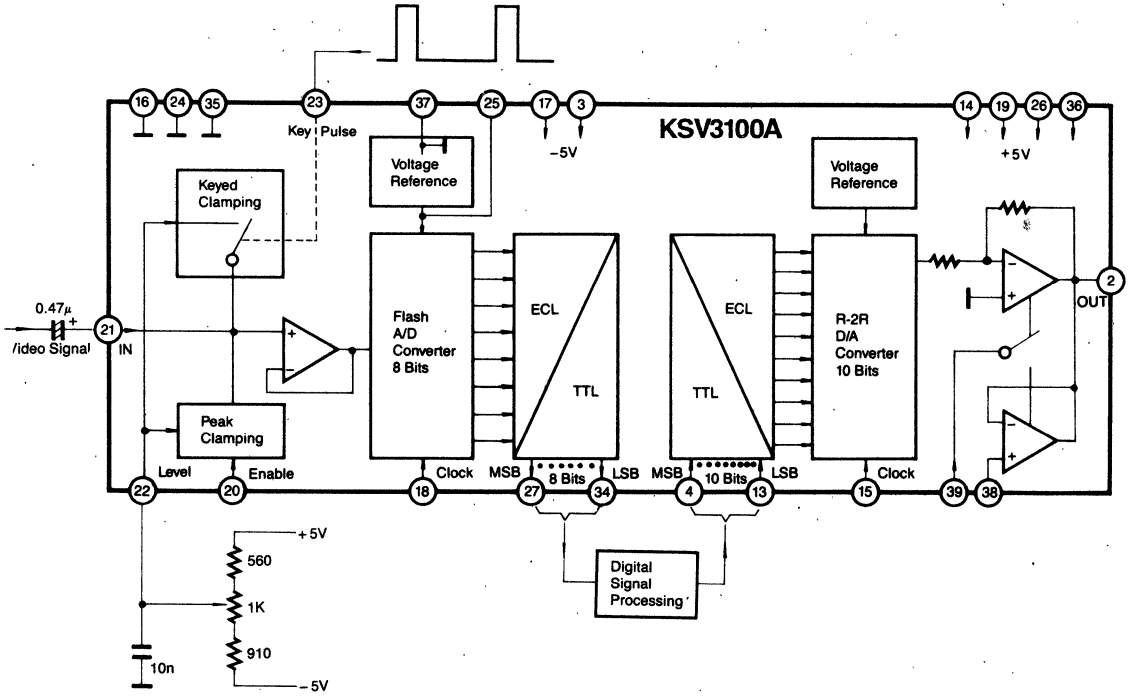


Fig. 13: Operation with keyed clamping

The input signal is applied to pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 23. By this means the clamping switch in the KSV3100A connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between -1 and $+2$V.

HIGH-SPEED A/D-D/A CONVERTER

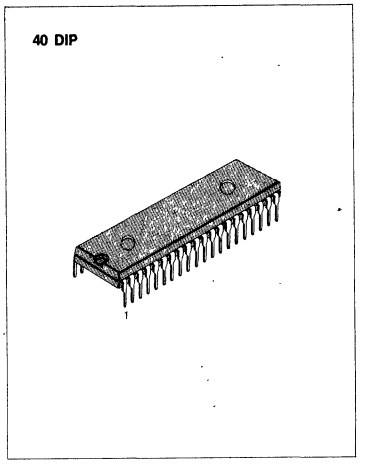
Samsung KSV3110, VLSI circuit in CI (Collector Implanted) technology consists of a high-speed flash-type 8-bit A/D converter and a high-speed low-glitch 10-bit D/A converter designed as an weighted current sources. Also, the various auxiliary circuits, as reference voltage voltage sources, pre-amplifier, input clamping circuit and feed-in output amplifier are integrated on the single chip.

KSV3110 has been developed for use in all applications which call for a high-speed A/D-D/A converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcast.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although KSV3110 was initially designed as high-speed codecs for the video range, it can be used with equal benefits for lower frequencies, even down to zero.



BLOCK DIAGRAM

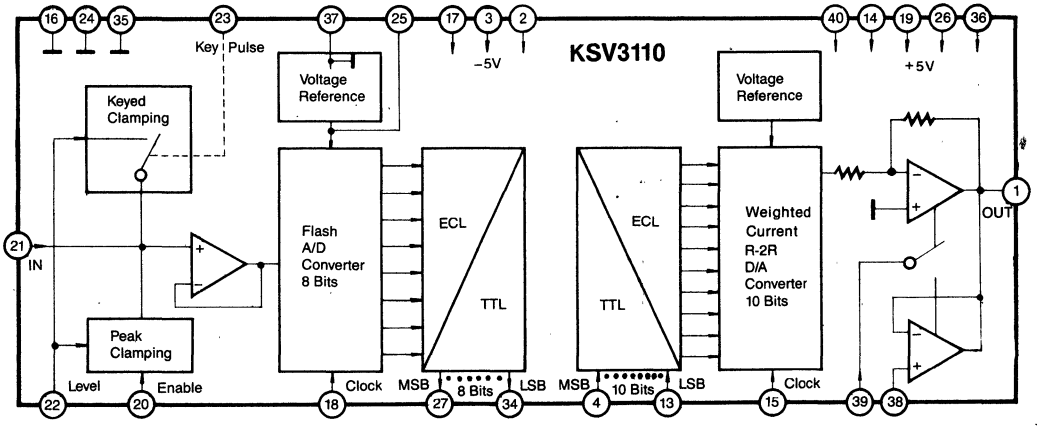


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input, in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping or peak clamping or without clamping. Also the D/A converter's reference voltage is generated on-chip, and a gated amplifier is arranged at the output of the D/A converter so that an external analog signal can be fed-in instead of the signal delivered by the D/A converter.

Separate clock inputs are provided for the A/D converter and the D/A converter thus enabling the application of time compression procedures.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description	Pin No.	Description
1	Analog Output D/A Converter	21	Analog Input A/D Converter
2	−5V Supply D/A-Analog	22	Clamping Level Input
3	−5V Supply D/A Converter-Digital	23	Clamping Pulse Input
4	Digital Input Bit 9 (MSB)	24	Analog Ground A/D Converter
5	Digital Input Bit 8	25	Reference Voltage A/D Converter
6	Digital Input Bit 7	26	+5V Supply A/D Converter-Digital
7	Digital Input Bit 6	27	Digital Output Bit 7 (MSB)
8	Digital Input Bit 5	28	Digital Output Bit 6
9	Digital Input Bit 4	29	Digital Output Bit 5
10	Digital Input Bit 3	30	Digital Output Bit 4
11	Digital Input Bit 2	31	Digital Output Bit 3
12	Digital Input Bit 1	32	Digital Output Bit 2
13	Digital Input Bit 0 (LSB)	33	Digital Output Bit 1
14	+5V Supply D/A Converter-Analog-Digital	34	Digital Output Bit 0 (LSB)
15	Clock Input D/A Converter	35	Digital Ground A/D Converter
16	GND D/A Conv. & Clock A/D Converter	36	+5V Supply A/D Converter-Analog
17	−5V Supply A/D Converter-Analog	37	GND of Ref. Voltage A/D Converter
18	Clock Input A/D Converter	38	External Analog Input
19	+5V Supply A/D Converter	39	Output Signal Switchover Input
20	Peak Clamping Enable Input	40	+5V Supply D/A-Analog

RECOMMENDED OPERATING CIRCUIT

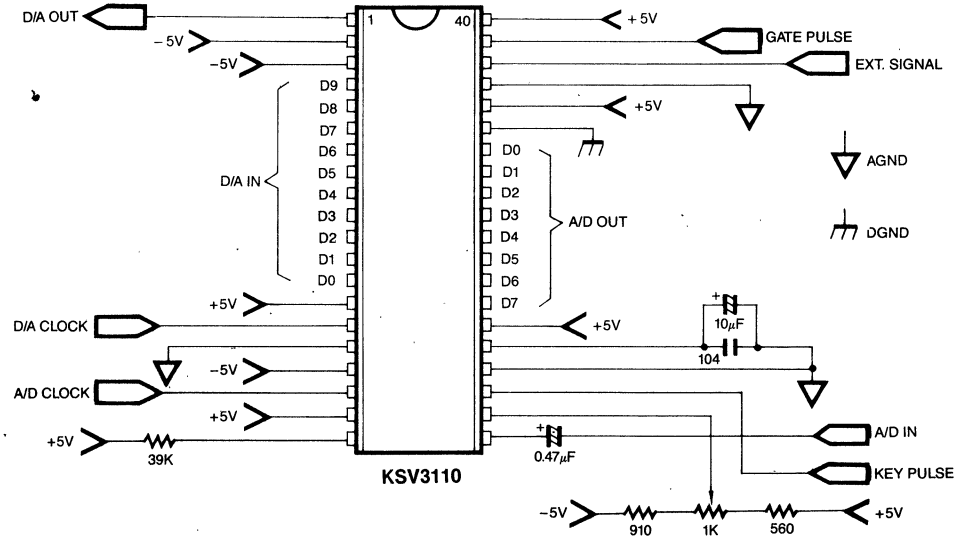


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	6	V
Negative Supply Voltage	V_{EE}	−6	V
Input Voltages (Digital)	V_I	−0.5 ~ V_{CC} +0.5	V
Input Voltages (Analog)	V_I	−0.5 ~ V_{CC} +0.5	V
Output Current Pin 2	I_o	±10	mA
Ambient Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5	−5.25	V
A/D Converter					
Analog Input Voltage	V_I	0	—	2	V
Input Frequency, Analog Input	f_I	—	—	$f_{cl}/2$	—
Clock Amplitude	V_{18H}	2.0	—	V_{CC}	V
	V_{18L}	0	—	0.8	V
Conversion Rate	f_{18}	0	—	20	MSPS*
Clock High Time (See Fig. 3)	t_H	15	—	—	ns
Clock Low Time (See Fig. 3)	t_L	35	—	—	ns
A/D Output Voltage	V_{OH}	2.4	—	V_{CC}	V
	V_{OL}	0	—	0.4	V
Clamping Level	V_{22}	−1	—	+2	V
Clamping Pulse	V_{23H}	2.0	—	V_{CC}	V
	V_{23L}	0	—	0.8	V
Activation of Peak Clamping	—	Resistor of 20 to 60KΩ from Pin 20 to +5V			—
D/A Converter					
Clock Amplitude	V_{15H}	2.0	—	V_{CC}	V
	V_{15L}	0	—	0.8	V
Conversion Rate	f_{15}	0	—	20	MSPS*
Digital Input Voltage	V_{IH}	2.0	—	V_{CC}	V
	V_{IL}	0	—	0.8	V
Analog Input Voltage at Pin 38	V_{38}	−1	—	+3	V
Output Signal Switch Over Input					
for the D/A Converter Out	V_{39}	0	—	0.8	V
for the Ext. Signal (from Pin 38) Out	V_{39}	2	—	V_{CC}	V

* MSPS (Mega Sample Per Second)

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{EE} = −5V, f_{15} = 20MHz, f_{18} = 20MHz, Ta = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC} I_{EE}	— —	90 −80	120 −110	mA mA
Power Dissipation	P_{TOT}	—	—	1.2	W
Total Transter Time A/D-D/A	t_{TOT}	See Fig. 3			—
A/D Converter					
Input Current Pin 21	I_I	—	2	—	μA
Input Capacitance Pin 21	C_I	—	10	—	pF
Input Impedance Pin 21					
at f = 1KHz	Z_I	—	20	—	MΩ
at f = 10MHz	Z_I	—	100	—	KΩ
3dB Bandwidth of the Input Amp.	—	—	50	—	MHz
Keyed Clamping Active Level	V_{23}	2.0	—	V_{CC}	V
On Resistance of the Clamping Switch Between Pin 21 and 22	R_{ON}	—	300	—	Ohm
Input Current of the Clamping Level Input Pin 22	I_{22}	—	200	—	μA
Aperture Delay (② in Fig. 3)	t_{AD}	—	—	10	ns
Digital Output Delay (③ in Fig. 3)	t_{DV}	—	18	—	ns
Transfer Time (⑥ in Fig. 3)	t_W	One clock period			—
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	8	—	—
Code of the Digital Output Signal	—	Binary			—
Output CODE at the Input with V_{21} = 0V with V_{21} = V_{ref}	 — —	 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1			 — —
Internal Reference Voltage	V_{25}	1.8	2.0	2.2	V
D/A Converter					
Output Impedance Pin 2	Z_O	—	15	—	Ω
Input Current Pin 38	I_{ID}	—	2	—	μA
Internal Reference Voltage	V_{ref}	1.8	2.0	2.2	V
Input Resister Hold Time (⑦ in Fig. 3)	t_{IH}	6.0	—	—	ns
Input Resister Setup Time (⑧ in Fig. 3)	t_{IH}	20	—	—	ns
Differential Non-Linearity	—	See "Ordering Information"			—
Absolute Non-Linearity	—	—	1	—	%
Number of Bits	—	—	10	—	—
Code of the Digital Input Signal	—	Binary			—
Output Signal at the Input with 0 0 0 0 0 0 0 0 0 0 with 1 1 1 1 1 1 1 1 1 1	 V_2 V_2	 — —	 0 2	 — —	 V V

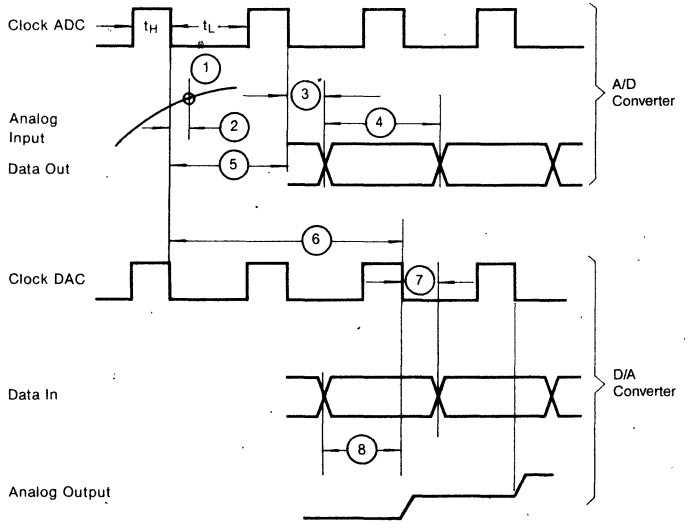
ORDERING INFORMATION

KSV3110 has four kind of version according to the accuracy bit (so called 'Precision') of D/A Converter, and their marking specifications are as follow;

Device	Package	Temperature Range	D/A Converter		A/D Converter
			Accurary Bit	Diff. Nonlinearity	Diff. Nonlinearity
KSV3110CN-10	40 DIP	0 ~ +70°C	10 bit	± 1/2 LSB	± 1/2 LSB
KSV3110CN-9			9 bit	± 1 LSB	
KSV3110CN-8			8 bit	± 2 LSB	
KSV3110CN-7			7 but	± 4 LSB	

* The accuracy of A/D Converter can be guaranteed as '8 bit' (differential nonlinearity = ± 1/2 LSB) regardless of the D/A Converter's accuracy.

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D
⑥ Total Transfer Time A/D-D/A with Common Clock
⑦ Input Register Hold Time
⑧ Input Register Setup Time

Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

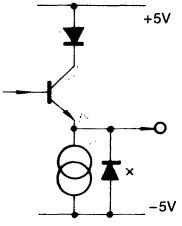


Fig. 4: Pin 1, Output

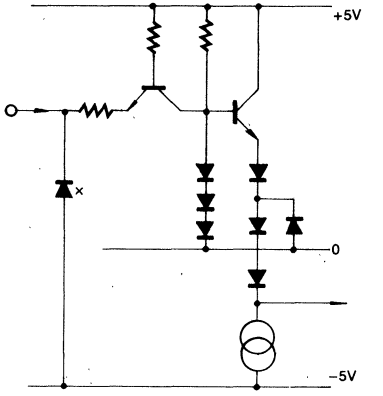


Fig. 5: Pins 4 to 13, 15, 18, 23 and 39, Inputs

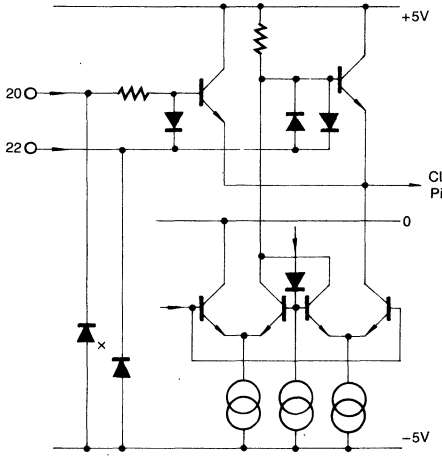


Fig. 6: Pins 20 and 22, Inputs

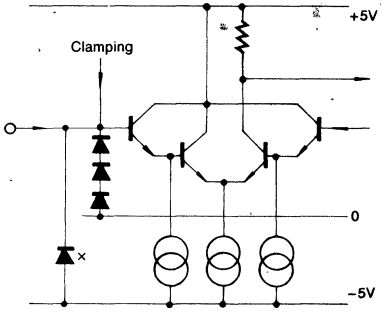


Fig. 7: Pin 21, Input

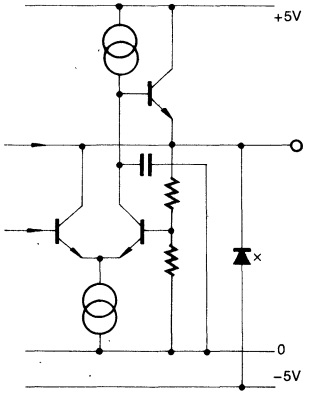


Fig. 8: Pin 25, Reference Voltage Pin

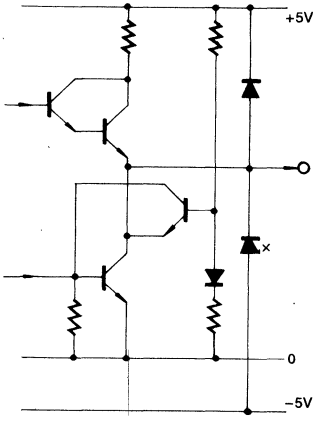


Fig. 9: Pins 27 to 34, Outputs

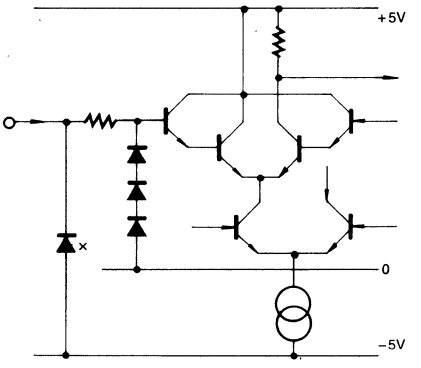


Fig. 10: Pin 38, Input
x = protection diode

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	Analog Output D/A Converter This pin whose diagram is shown in Fig. 4, is the output for the processed analog signal either originating from the D/A converter or from the external analog input pin 38.
Pin 2	−5 Volt Supply D/A Converter, Analog This pin gets the negative supply for the analog part of the D/A converter
Pin 3	−5 Volt Supply D/A Convetter, Digital This pin gets the negative supply for the digital part of the D/A converter.
Pin 4 to 13	Digital Inputs Bit 9 to Bit 0 This diagram of these pins is shown in Fig. 5. They are the inputs of the D/A converter and not-used inputs should be connected to the ground.
Pin 14	+5 Volt Supply D/A Converter, Digital This pin gets the positive supply for the digital part of the D/A converter.
Pin 15	Clock Input D/A Converter This pin whose diagram is shown in Fig. 5 must be supplied with the clock signal for the D/A converter.
Pin 16	Ground D/A Converter and Clock A/D Converter This pin serves as ground pin for the D/A converter and for the clock of the A/D converter.
Pin 17	−5 Volt Supply A/D Converter, Analog This pin is the negative supply pin for the analog part of the A/D converter.
Pin 18	Clock Input A/D Converter The diagram of this pin is shown in Fig. 5. Pin 18 is supplied with the clock of the A/D converter.
Pin 19	+5 Volt Supply A/D Converter Via this pin the A/D converter gets its positive supply.
Pin 20	Peak Clamping Enable Input Via pin 20 whose diagram is shown in Fig. 6, the peak clamping facility can be enabled.

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS (Continued)

Pin No.	Description
Pin 21	Analog Input A/D Converter Fig. 7 is the diagram of this input. To pin 21 is applied the analog signal to be converted into digital.
Pin 22	Clamping Level Input Via this pin whose diagram is shown in Fig. 6, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Clamping Pulse Input Fig. 5 is the diagram of this input. Pin 23 must be supplied with the key pulse if keyed clamping is required.
Pin 24	Analog Ground A/D Converter This pin serves as ground pin for the analog part of the A/D converter.
Pin 25	Reference Voltage A/D Converter This pin whose diagram is shown in Fig. 8, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage, the other end of this capacitor to pin 37.
Pin 26	+5 Volt Supply A/D Converter, Digital This pin is the positive supply pin for the digital part of the A/D converter.
Pin 27 to 34	Digital Outputs Bit 7 to Bit 0 Fig. 9 shows the diagram of these outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 35	Digital Ground A/D Converter This pin is the ground connection for the digital part of the A/D converter.
Pin 36	+5 Volt Supply A/D Converter, Analog This pin is the positive supply pin for the analog part of the A/D converter.
Pin 37	Ground of Reference Voltage A/D Converter To this pin must be connected the ground end of the decoupling which is at pin 25.
Pin 38	External Analog Input The diagram of this input is shown in Fig. 10. Pin 38 serves for feeding an external analog signal into the output amplifier of the KSV3110 instead of the D/A-converted signal originating from pin 4 to 13.
Pin 39	Output Signal Switchover Input This pin whose diagram is shown in Fig. 5, is intended for enabling the external analog signal fed to pin 38.
Pin 40	+ 5 Volt Supply D/A Converter, Analog This pin is the negative supply pin for the analog parts of the D/A converter

APPENDIX: APPLICATION CIRCUITS

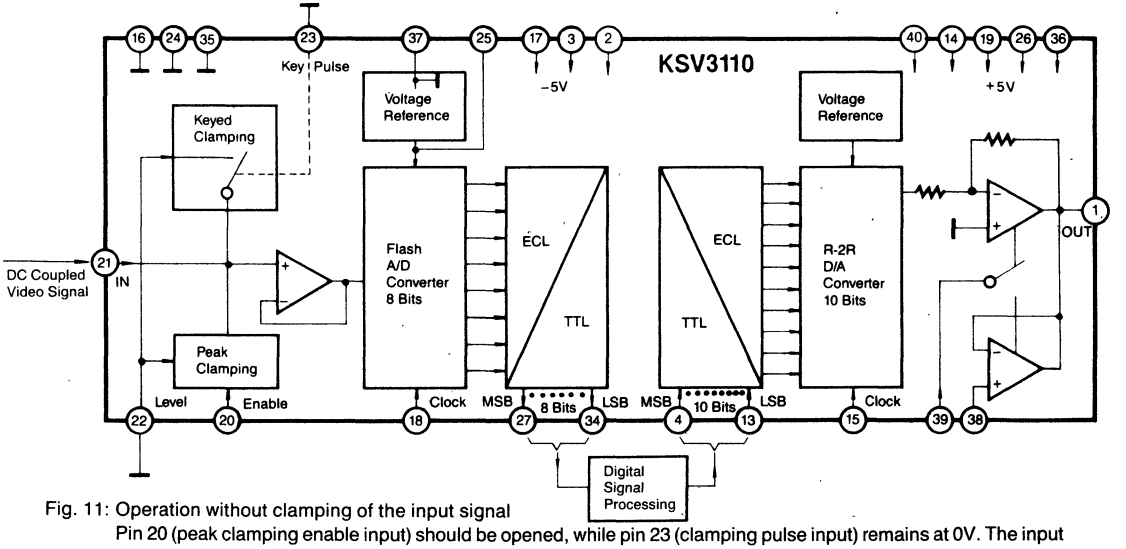


Fig. 11: Operation without clamping of the input signal

Pin 20 (peak clamping enable input) should be opened, while pin 23 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 21, without coupling capacitor such that it lies between 0 and +2V.

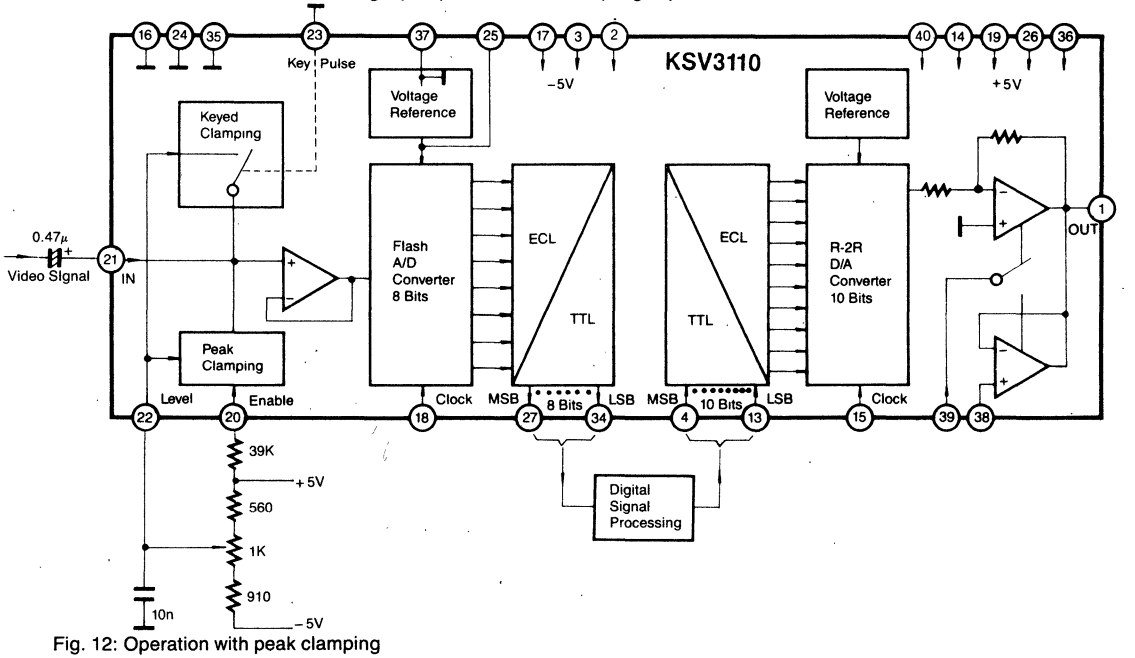


Fig. 12: Operation with peak clamping

The input signal is clamped automatically to the negative peak value. Pin 20 is connected to +5V via a 39KΩ resistor, and pin 22 (clamping level input) is connected, as desired, to zero or a voltage between −1 and +2V. The input signal is fed to pin 21 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

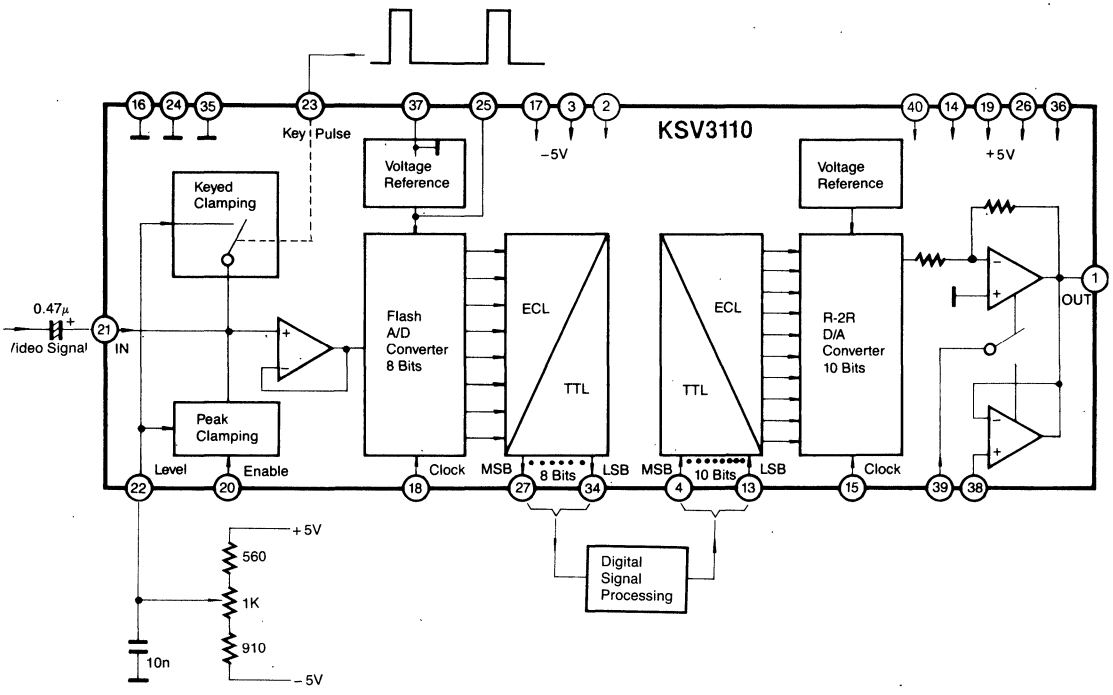


Fig. 13: Operation with keyed clamping

The input signal is applied to pin 21 through a coupling capacitor. Pin 20 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 23. By this means the clamping switch in the KSV3110 connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between – 1 and + 2V.

HIGH-SPEED A/D CONVERTER

Samsung KSV3208, VLSI circuit in CI (Collector Implanted) technology, consists of a high-speed flash-type 8-bit A/D converter. Also, the various auxiliary circuits, as reference voltage sources, pre-amplifier, input clamping circuits are integrated on the single chip.

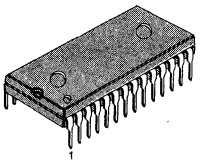
KSV3208 has been developed for use in all applications which call for a high-speed A/D converter.

For instance, this VLSI circuit can be used to advantage to decode television signals in Pay-TV converters or for MAC converters used in direct satellite broadcast.

Other promising applications can be seen in industrial electronics, e.g. in conjunction with signal processing.

Although KSV3208 was initially designed as high-speed converter for video frequency range, it can be used with equal benefits for lower frequencies, even down to zero.

28 DIP



ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KSV3208CN	28 DIP	0 ~ +70°C	± 1/2 LSB

5

BLOCK DIAGRAM

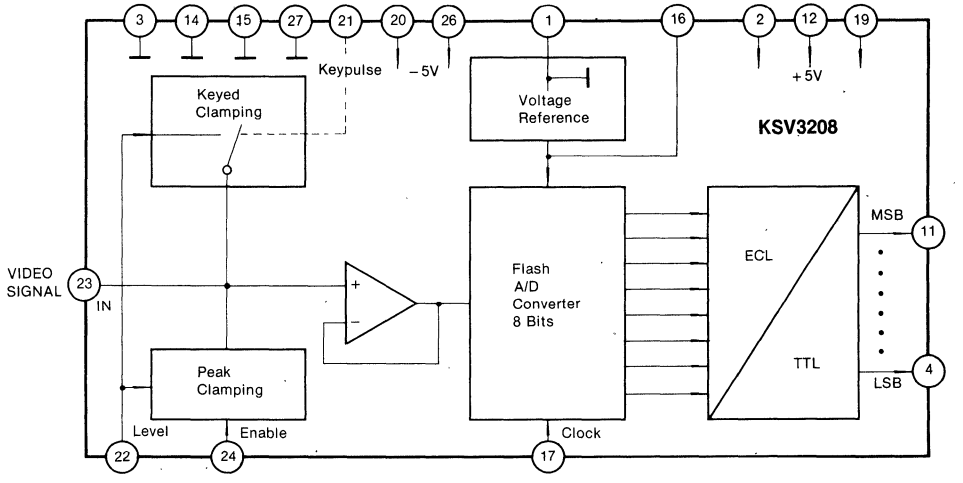


Fig. 1

The auxiliary circuits contained on-chip provide versatile potential applications needing a minimum of external components. For example, an impedance converter is connected upstream of the A/D converter to provide a high-impedance signal input in spite of the high input capacitance of the A/D converter. The reference voltage for the A/D converter is generated on-chip, but both the ground of the circuit and the reference voltage are fed to pins, so that an external filter capacitor may be connected.

Further, the input is equipped with switches which optionally provide operation with keyed clamping of peak clamping or without clamping.

All inputs and outputs are TTL compatible.

PIN DESCRIPTION

Pin No.	Description
1	GND of Reference Resistor String
2	+5V Supply of ECL Logic Part, Digital
3	GND of ECL to TTL Translator Part, Digital
4	Digital Output Bit 0 (LSB)
5	Digital Output Bit 1
6	Digital Output Bit 2
7	Digital Output Bit 3
8	Digital Output Bit 4
9	Digital Output Bit 5
10	Digital Output Bit 6
11	Digital Output Bit 7 (MSB)
12	+5V Supply of TTL Output Part, Digital
13	No Connection
14	GND of ECL Logic Part, Digital
15	GND of Input Stage, Analog
16	$+V_{REF}$, Reference Voltage Point of Resistor String
17	Clock Input
18	No Connection
19	+5V Supply of Input Stage, Analog
20	−5V Input Stage, Analog
21	Clamping Pulse Input
22	Clamping Level Input
23	Analog Signal Input
24	Peak Clamp Enable Input
25	No Connection
26	No Connection
27	GND of ECL Clock Part, Digital
28	−5V Supply of ECL Logic Part, Digital

RECOMMENDED OPERATING CIRCUIT

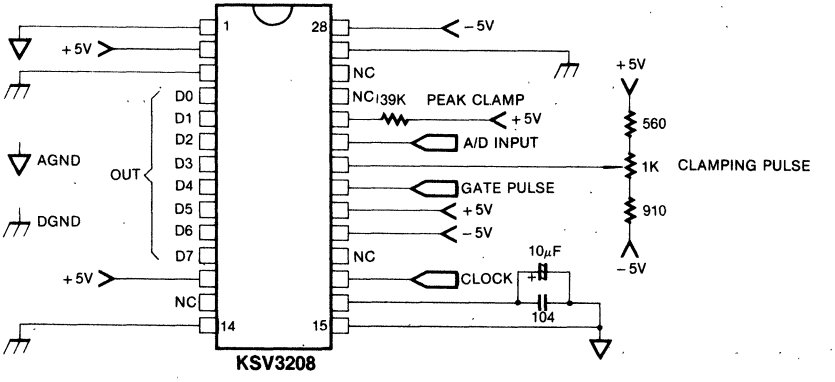


Fig. 2

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	6	V
Negative Supply Voltage	V_{EE}	−6	V
Input Voltages (Digital)	V_I	−0.5 ~ V_{CC} +0.5	V
Input Voltages (Analog)	V_I	−0.5 ~ V_{CC} +0.5	V
Ambient Operating Temperature Range	T_a	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−40 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Positive Supply Voltage	V_{CC}	4.75	5	5.25	V
Negative Supply Voltage	V_{EE}	−4.75	−5	−5.25	V
Analog Input Voltage	V_I	0	—	2	V
Input Frequency, Analog Input	f_I	—	—	$f_{cl}/2$	—
Clock Amplitude	V_{17H}	2.0	—	V_{CC}	V
	V_{17L}	0	—	0.8	V
Conversion Rate	f_{17}	0	—	20	MSPS*
Clock High Time (See Fig. 3)	t_H	15	—	—	ns
Clock Low Time (See Fig. 3)	t_L	35	—	—	ns
Clamping Level	V_{22}	−1	—	+2	V
Clamping Pulse (High)	V_{21H}	2.0	—	V_{CC}	V
Clamping Pulse (Low)	V_{21L}	0	—	0.8	V
Activation of Peak Clamping	—	Resistor of 20 to 60Kohm from Pin 24 to +5V			—

* MSPS (Mega Sample Per Second)

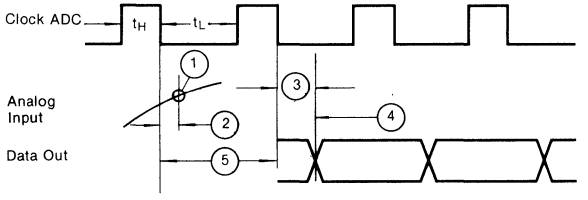
5

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{EE} = 5V, f_{17} = 20MHz, Ta = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption	I_{CC} I_{EE}	— —	— —	100 – 80	mA mA
Power Dissipation	P_{tot}	—	—	0.9	W
Total Transter Time A/D	T_{tot}	See Fig. 3			—
Input Current Pin 23	I_I	—	1	—	μA
Input Capacitance Pin 23	C_I	—	10	—	pF
3dB Bandwidth of the Input Amp.	—	—	50	—	MHz
Keyed Clamping Active Level	V_{21}	2.0	—	V_{CC}	V
On Resistance of the Clamping Switch Between Pin 23 and 23	R_{ON}	—	300	—	Ohm
Input Current of the Clamping Level Input Pin 22	122	—	200	—	μA
Aperture Delay (② in Fig. 3)	t_{sd}	—	—	10	ns
Digital Output Delay (③ in Fig. 3)	t_{dv}	—	—	14	ns
Transfer Time (⑤ in Fig. 3)	T_{tr}	On Clock Period			—
Differential Non-Linearity	—	—	—	± 1/2	LSB
Absolute Non-Linearity		—	1	—	%
Number of Bits	—	—	8	—	—
Code of the Digital Output Signal	—	Binary			—
Output CODE at the Input with V_{23} = 0V with V_{23} = V_{ref}	 — —	 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1			 — —
Internal Reference Voltage	V_{ref}	1.8	2.0	2.2	V

TIMING DIAGRAM



① Sample
② Aperture Delay
③ Digital Output Delay
④ Data Valid (after Sample ①)
⑤ Transfer Time A/D

Fig. 3

INNER CONFIGURATION OF THE CONNECTION PINS

The following figures schematically show the circuitry at the various pins.

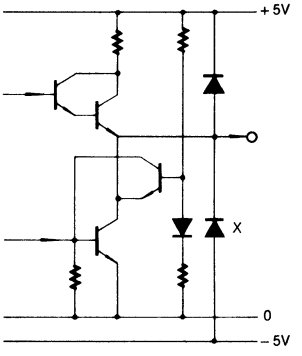


Fig. 4: Pin 4 to 11, Outputs

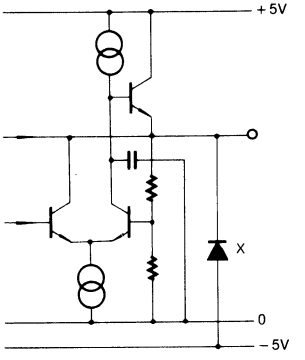


Fig. 5: Pin 16, Reference Voltage

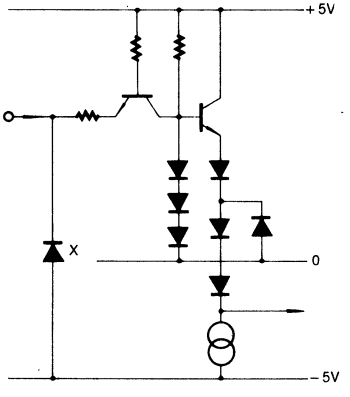


Fig. 6: Pin 17, 21 Input

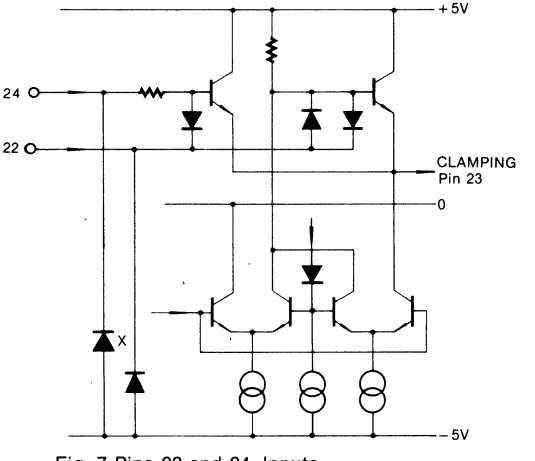


Fig. 7 Pins 22 and 24, Inputs

x: Protection Diode

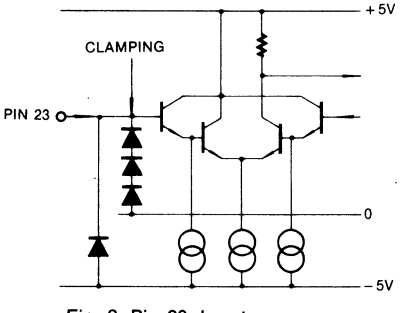


Fig. 8: Pin 23, Input

DESCRIPTION OF THE CONNECTIONS AND THE SIGNALS

Pin No.	Description
Pin 1	GND of Reference Resistor String This pin must be connected to the ground of the decoupling capacitor whitch is at pin 16.
Pin 2	+5 Volt Supply of ECL Logic Part, Digital This pin is the positive supply pin for the ECL logic part.
Pin 3	Digital Ground of ECL to TTL Translator Part. This pin is the digital ground connection for the TTL output stage where ECL level is translated to TTL level.
Pin 4 to Pin 11	Digital Outputs Bit 0 to Bit 7. Fig. 4 shows the diagram of there outputs which supply the digitized analog signal in parallel 8-bit code.
Pin 12	+5 Volt Supply off TTL Output Part, Digital This pin is the digital positive supply pin for the TTL output stage where ECL level is translated to TTL level.
Pin 14	Digital GND of ECL Logic Part This pin serves as the digital ground for the ECL logic part.
Pin 15	Analog GND of Input Stage This pin serves as the analog ground for the input stage; buffer amp, bandgap reference, clamp block.
Pin 16	$+V_{REF}$, Reference Voltage Point of Resistor String This pin whose diagram is shown is Fig. 5, is intended for connecting a decoupling capacitor to the A/D converter's reference voltage. The other end of this capacitor is connected to pin 1. (GND of Reference Resistor String).
Pin 17	Clock Input The diagram of this pin is shown in Fig. 6. Pin 17 is supplied with the clock of A/D converter.
Pin 19	+5 Volt Supply of Input Stage, Analog This pin is the analog positive supply pin for the input stage; bandgap reference.
Pin 20	−5 Volt Supply of Input Stage, Analog This pin is the analog negative supply pin for the input stage; buffer amp, bandgap reference, clamp block.
Pin 21	Clamping Pulse Input Fig. 6 is diagram of this pin. Pin 21 must be supplied with the key pulse if keyed clamping is required.
Pin 22	Clamping Level Input Via this pin whose diagram is shown is Fig. 7, the input of the A/D converter is supplied with the desired clamping level.
Pin 23	Analog Signal Input Fig. 8 is the diagram of this input. To pin 23 is applied the analog signal to be converted into digital.
Pin 24	Peak Clamp Enable Input Via pin 24 whose diagram is shown in Fig. 7, the peak clamping facilities can be enable.
Pin 27	Digital GND of ECL Clock Part This pin serves as the digital ground for the ECL clock block.
Pin 28	−5 Volt Supply of ECL Logic Part, Digital This pin is the digital negative supply for the ECL logic part.

APPENDIX: APPLICATION CIRCUITS

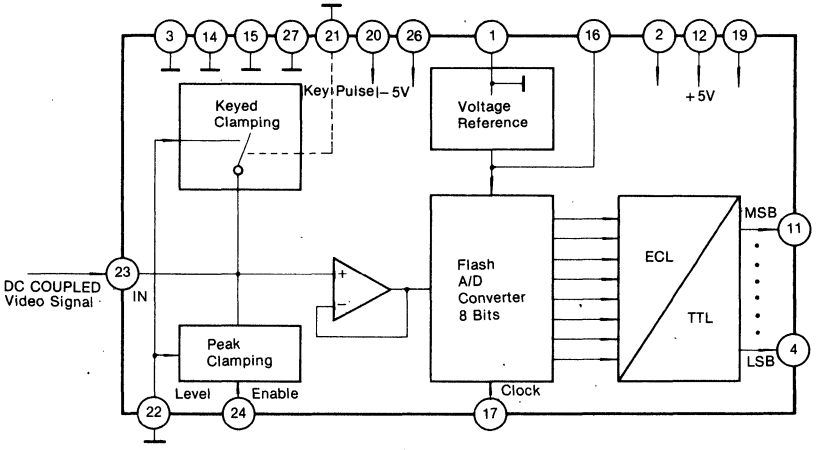


Fig. 9: Operation without clamping of the input signal
Pin 24 (peak clamping enable input) should be opened, while pin 21 (clamping pulse input) remains at 0V. The input signal is applied to the analog input, pin 23, without coupling capacitor such that it lies between 0 and +2V

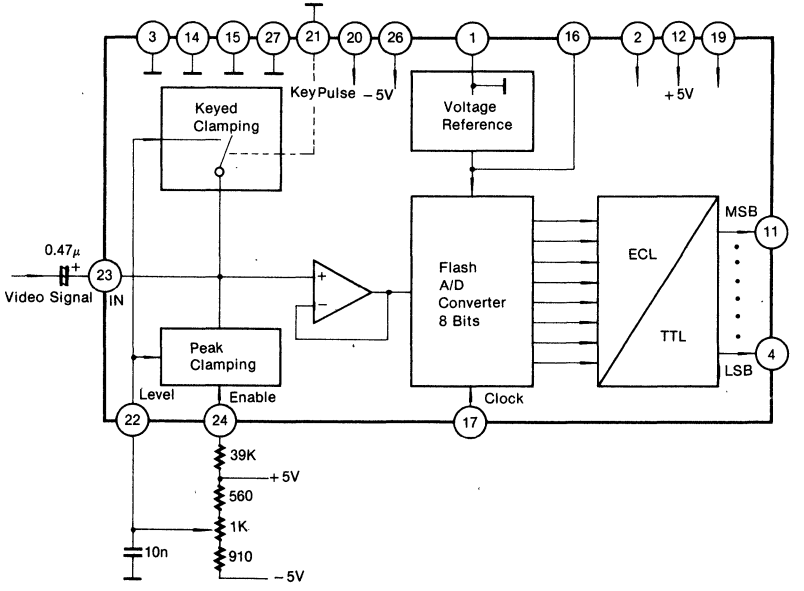


Fig. 10: Operation with peak clamping
The input signal is clamped automatically to the negative peak value. Pin 24 is connected to +5V via a 39Kohm resistor and pin 22 (clamping level input) is connected, as desired, to zero or a voltage betgween −1 and +2V. The input signal is fed to pin 23 by way of a coupling capacitor, and no key pulse (clamping pulse) is needed.

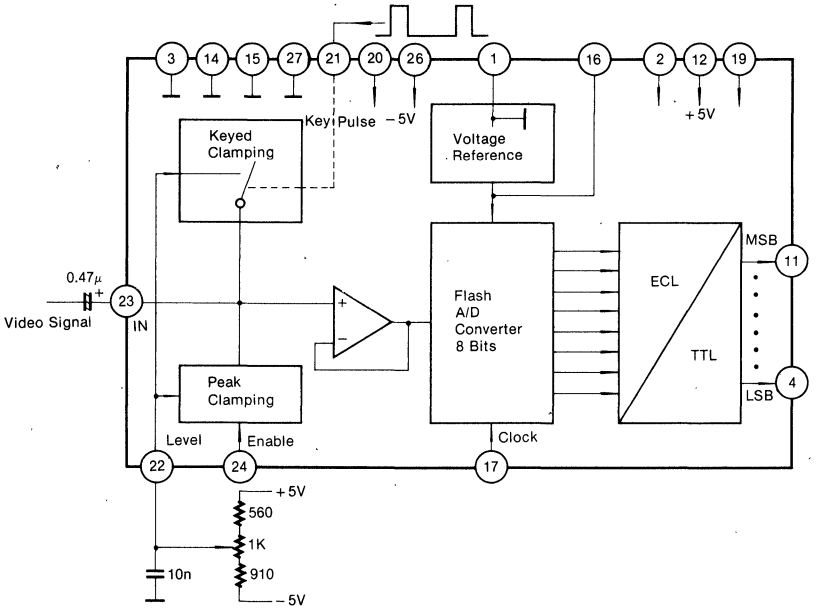
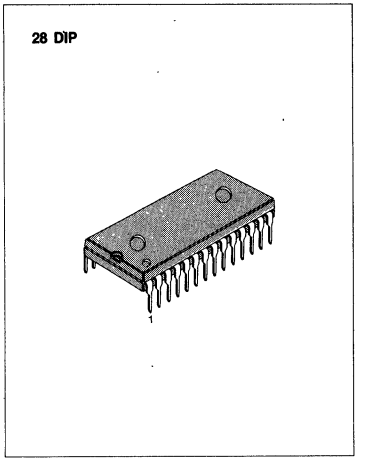


Fig. 11: Operation with keyed clamping

The input signal is applied to pin 23 through a coupling capacitor. Pin 24 must not be connected. While the input signal is at the desired clamping level, an high-level is applied at the clamping pulse input, pin 21. By this means the clamping switch in the KSV3208 connects the input with the clamping level at pin 22 and recharges the coupling capacitor accordingly. The clamping level can be set to zero or, by means of an external voltage devider, to any desired value between −1 and +2V.

8-BIT μP-COMPATIBLE A/D CONVERTERS WITH 8-CHANNEL MULTIPLEXER



The KAD0808/KAD0809 Analog to Digital converter is a monolithic CMOS device with an 8-bit resolution, 8-channel input multiplexer and microprocessor compatible control logic. It uses successive approximation as the conversion technique.

The design of the KAD0808/KAD0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The KAD0808/KAD0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power.

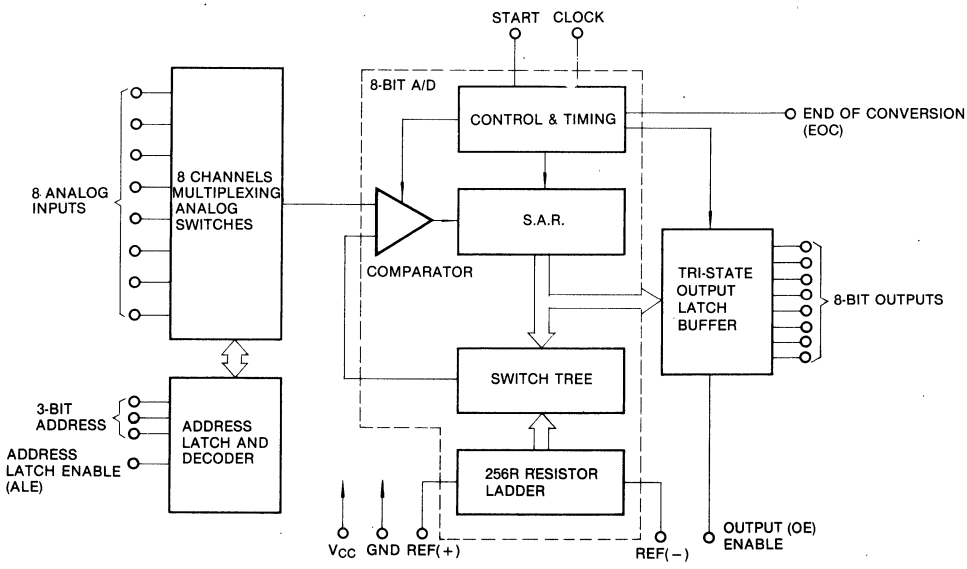
FEATURES

- **Total unadjusted error— ±1/2 LSB or ±1 LSB**
- **Resolution—8-bits**
- **Conversion time—100μS**
- **No missing codes**
- **Latched TRI-STATE output**
- **Easy interface to all microprocessors, or operates "stand alone"**
- **Single supply—5 V_{DC}**
- **8-channel multiplexer with latched control logic**
- **Outputs meet TTL voltage level specifications**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero or full-scale adjust required**
- **Standard 28-pin DIP package**

ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KAD0808IN	28 DIP	−40°C ~ +85°C	±1/2 LSB
KAD0809IN			±3/4 LSB

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristic	Symbol	Value	Unit
Supply Voltage (Note 3)	V_{CC}	6.5	V
Voltage at Any Pin Except Control Inputs	V_I	$-0.3V \sim (V_{CC}+0.3V)$	V
Voltage at Control Inputs	V_I	$-0.3V \sim +15V$	V
Package Dissipation at Ta = 25°C	P_D	875	mW
Operating Temperature	T_{opr}	$-40°C \sim +85°C$	°C
Storage Temperature Range	T_{stg}	$-65°C \sim +125°C$	°C

ELECTRICAL CHARACTERISTICS

Converter Specifications: $V_{CC}=5$ $V_{DC}=V_{ref(+)}$, $V_{ref(-)}=GND$, $T_f=T_r=20ns$ and $f_{CLK}=640KHz$ unless otherwise stated.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
KAD0808 Total Unadjusted Error (Note 5)		 25°C $-40°C \sim 85°C$	 — —	 — —	 ±1/2 ±3/4	 LSB LSB
KAD0809 Total Unadjusted Error (Note 5)		$0°C \sim 70°C$ $-40°C \sim 85°C$	— —	— —	±1 $\pm 1\frac{1}{4}$	LSB LSB
Input Resistance	R_{ref}	From Ref(+) to Ref(−)	1.0	2.5	—	KΩ
Analog Input Voltage Range	V_{in}	(Note 4) V(+) or V(−)	GND − 0.10	—	$V_{CC}+0.10$	V
Comparator Input Current	I_{on}	$f_C=640KHz$, (Note 6)	−2	±0.5	2	μA
Analog Multiplexer						
OFF Channel Leakage Current	$I_{OFF(+)}$	$V_{CC}=5V$, $V_{IN}=5V$, Ta = 25°C	—	10	200	nA
OFF Channel Leakage Current	$I_{OFF(-)}$	$V_{CC}=5V$, $V_{IN}=0$, Ta = 25°C	−200	−10	—	nA
Control Inputs						
Logical "1" Input Voltage	V_{IH}		$V_{CC}-1.5$	—	V_{CC}	V
Logical "0" Input Voltage	V_{IL}		0	—	0.4	V
Supply Current	I_{CC}	$f_{CLK}=640KHz$	—	0.3	3.0	mA
Logical "1" Output Voltage	V_{OH}	$I_O=-360\mu A$	$V_{CC}-0.4$	—	V_{CC}	V
Logical "0" Output Voltage	V_{OL}	$I_O=1.6mA$	0	—	0.45	V
Logical "0" Output Voltage EOC	$V_{OUT(0)}$	$I_O=1.2mA$	0	—	0.45	V
TRI-STATE Output Current	I_{OUT}	$V_O=5V$ $V_O=0$	— −3	— —	3 —	μA μA

ELECTRICAL CHARACTERISTICS

Timing Specifications $V_{CC} = V_{ref(+)} = 5V$, $V_{ref(-)} = GND$, $t_r = t_f = 20ns$ and $Ta = 25°C$ unless otherwise noted.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Minimum Start Pulse Width	t_{WS}	(Figure 5)	—	100	200	ns
Minimum ALE Pulse Width	t_{WALE}	(Figure 5)	—	100	200	ns
Minimum Address Set-Up Time	t_s	(Figure 5)	—	25	50	ns
Minimum Address Hold Time	t_h	(Figure 5)	—	25	50	ns
Analog MUX Delay Time From ALE	t_d	$R_S = 0\Omega$ (Figure 5)	—	1	2.5	μS
OE Control to Q Logic State	t_{H1}, t_{H0}	$C_L = 50pF$, $R_L = 10K$ (Figure 8)	—	125	250	ns
OE Control to Hi-Z	t_{1H}, t_{0H}	$C_L = 10pF$, $R_L = 10K$ (Figure 8)	—	125	250	ns
Conversion Time	t_{CON}	$f_c = 640KHz$, (Figure 5)	90	100	116	μS
Clock Frequency	f_{CLK}		10	640	1280	KHz
Input Capacitance	C_{IN}	At Control Inputs	—	10	15	pF
TRI-STATE Output Capacitance	C_{OUT}	At TRI-STATE Outputs	—	10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, Internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See Figure 3. None of those A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See Figure 13.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (Figure 6).

5

FUNCTIONAL DESCRIPTION

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

Selected Analog Channel	Address Line		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (Figure 1) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in Figure 1 are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + 1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. Figure 2 shows a typical example of a 3-bit converter. In the KAD0808, KAD0809 the approximation technique is extended to 8 bits using the 256R network.

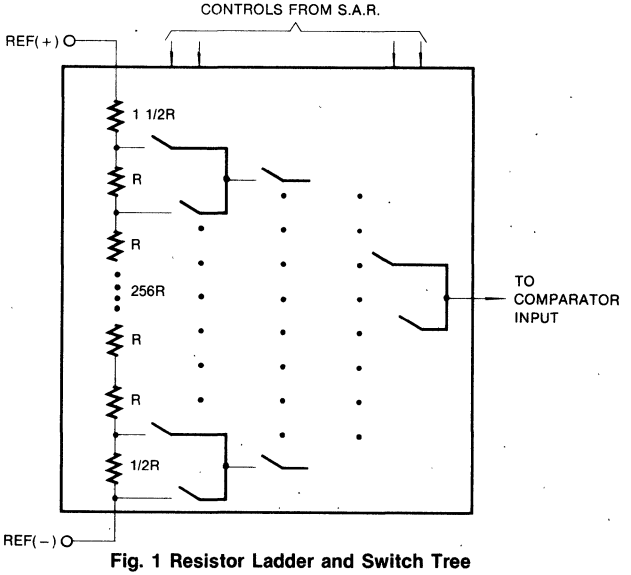


Fig. 1 Resistor Ladder and Switch Tree

FUNCTIONAL DESCRIPTION (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed throught a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the KAD0808.

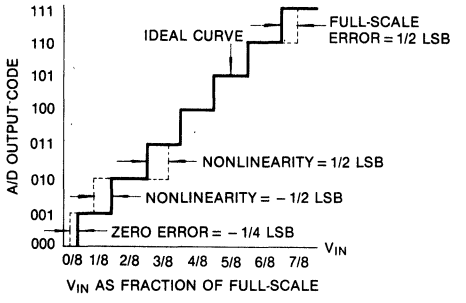


Fig. 2 3-Bit A/D Transfer Curve

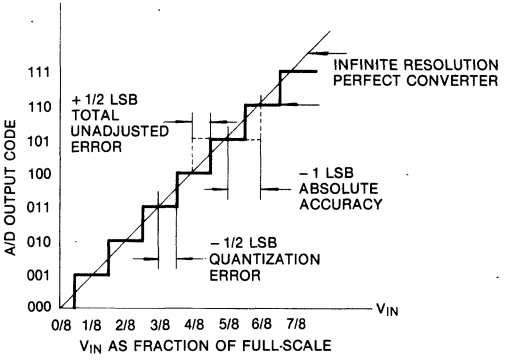


Fig. 3 3-Bit A/D Absolute Accuracy Curve

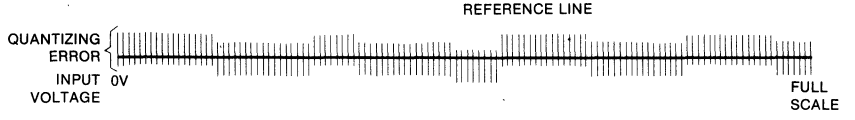
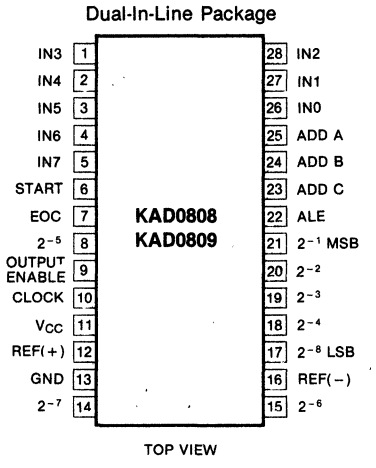


Fig. 4 Typical Error Curve

PIN CONFIGURATION



TIMING DIAGRAM

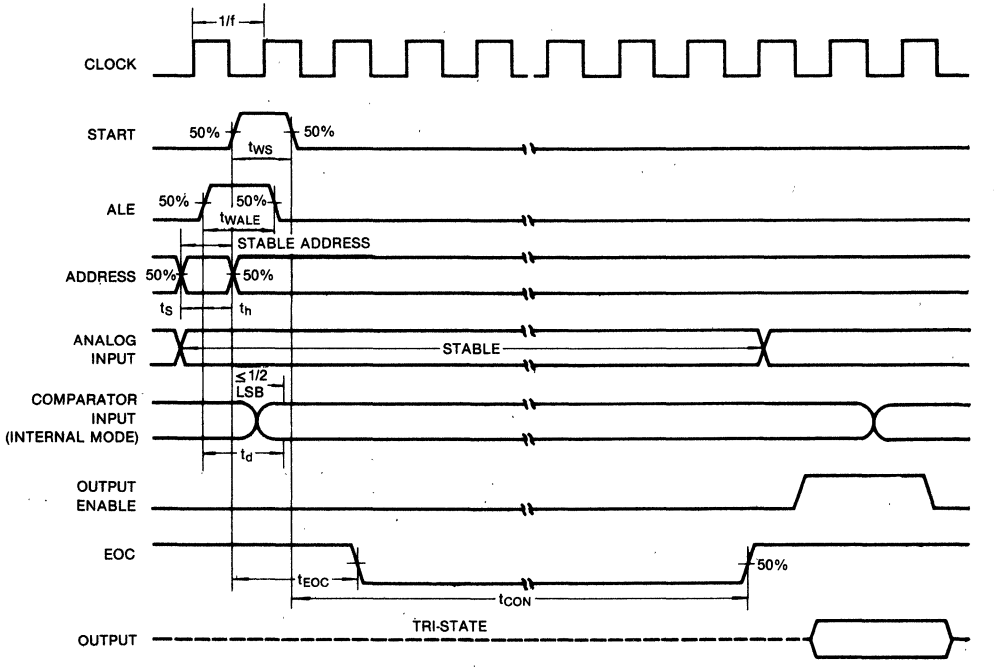


Fig. 5

TYPICAL PERFORMANCE CHARACTERISTICS

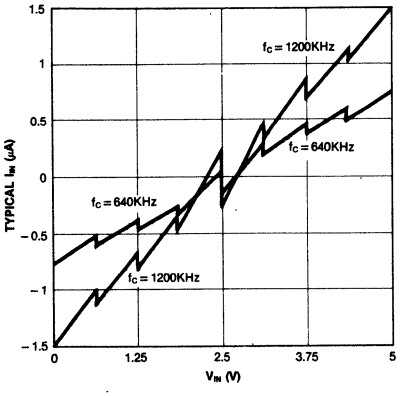


Fig. 6 Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

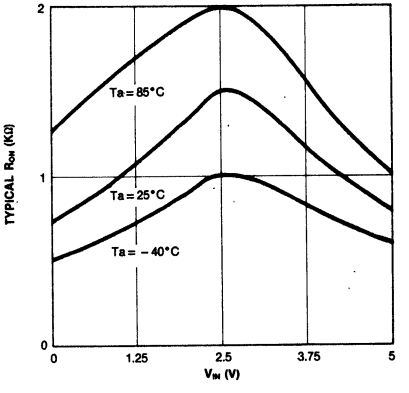


Fig. 7 Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE TEST CIRCUITS AND TIMING DIAGRAMS

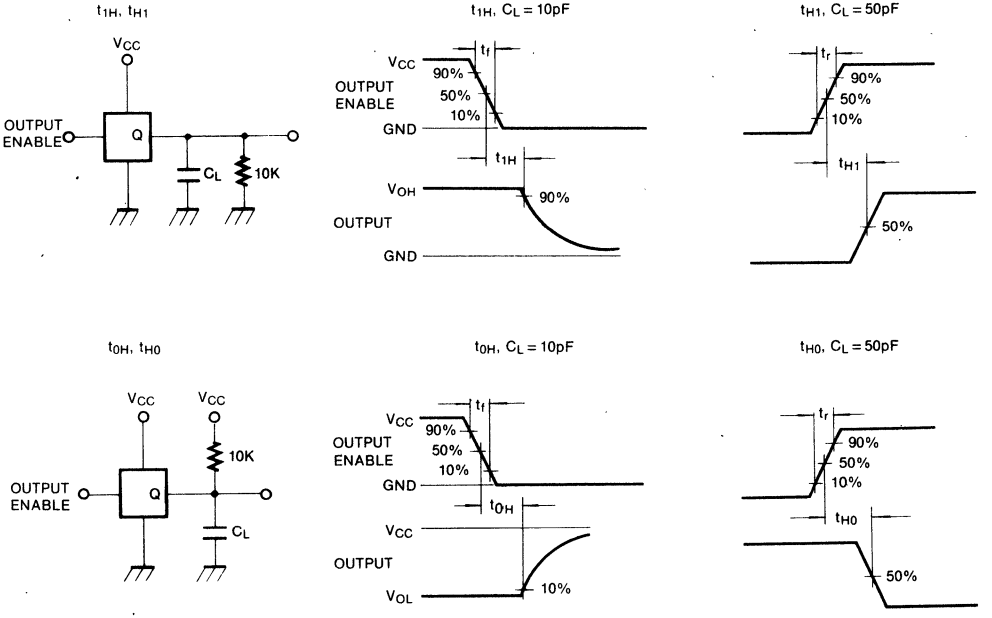


Fig. 8

APPLICATIONS INFORMATION

OPERATION

1.0 Ratiometric Conversion

The KAD0808, KAD0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the KAD0808 is expressed by the equation.

$$\frac{V_{IN}}{V_{fs} - V_Z} = \frac{D_X}{D_{max} - D_{min}}$$

V_{IN} = Input voltage into the KAD0808
V_{fs} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{max} = Maximum data limit
D_{min} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the KAD0808, KAD0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and thier outputs connected directly into the multiplexer inputs, (Figure 9).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is a LSB which is then 20mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

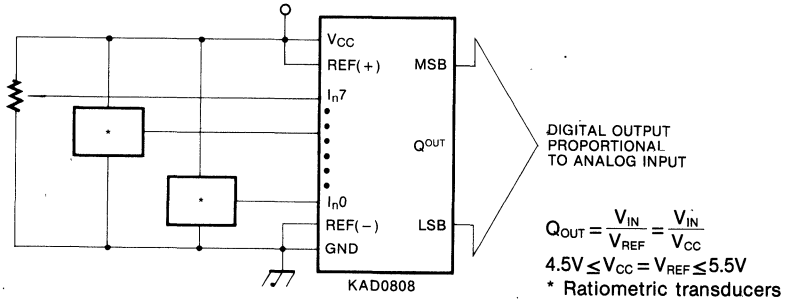


Fig. 9 Ratiometric Conversion System

APPLICATIONS INFORMATION (Continued)

The KAD0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In Figure 11 a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in Figure 12. The KA301A is overcompensated to insure stability when loaded by the 10μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. Sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In Figure 13, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

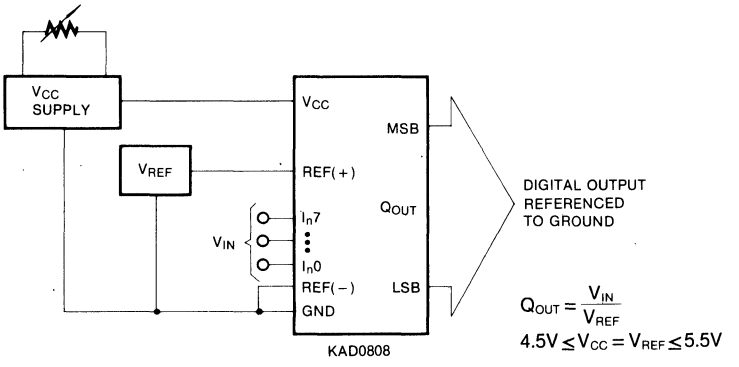


Fig. 10 Ground Referenced Conversion System Using Trimmed Supply

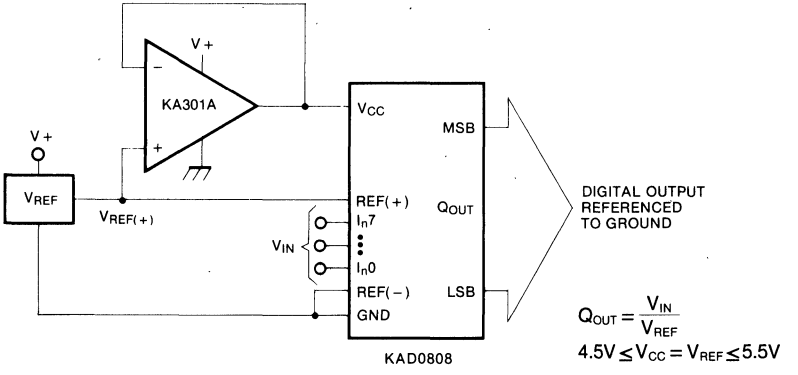


Fig. 11 Ground Referenced Conversion System with Reference Generating V_{CC} Supply

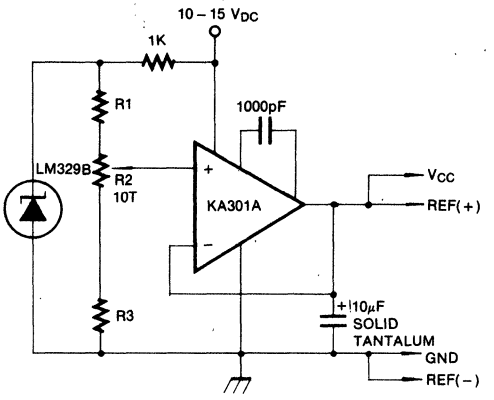


Fig. 12 Typical Reference and Supply Circuit

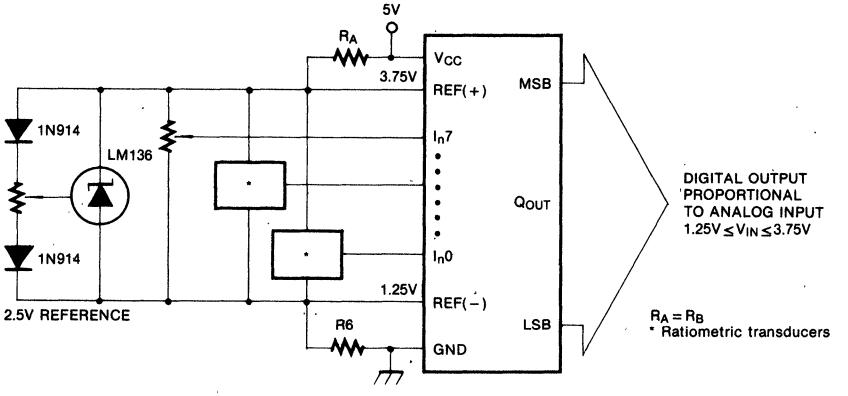


Fig. 13 Symmetrically Centered Reference

3.0 Converter Equations

The transition between adjacent codes N and N + 1 is givn by:

$$V_{IN} = \{(V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\} + V_{REF(-)}$$

The center of an output code N is given by:

$$V_{IN}\{(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\} + V_{REF(-)}$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy}$$

Where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(–)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 Analog Comparator Inputs

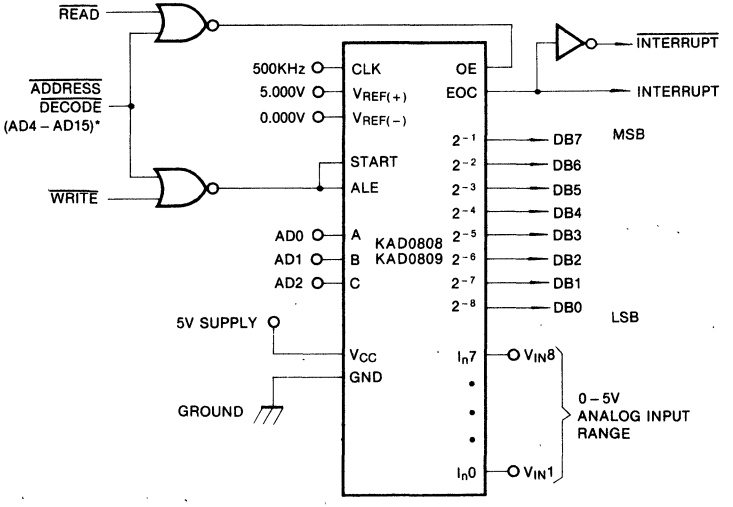
The dynamic comparator input current is caused by the pariodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in Figure 6.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduced converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. I will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

TYPICAL APPLICATION

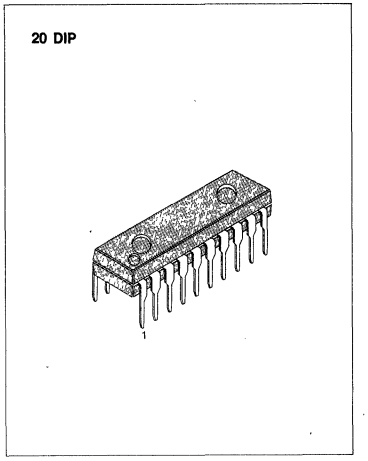


* Address latches needed for 8085 and SC/MP interfacing the KAD0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

Processor	$\overline{\text{Read}}$	$\overline{\text{Write}}$	Interrupt (Comment)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA• ϕ 2•R/W	VMA• ϕ •$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

8-BIT HIGH SPEED μP-COMPATIBLE A/D CONVERTER WITH TRACK/HOLD FUNCTION



By using a half-flash conversion technique, the 8-bit KAD0820A/B CMOS A/D offers a 1.5μs conversion time and dissipates only 75mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the KAD0820A/B is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100mV/μs.

For ease of interface to microprocessors, the KAD0820A/B has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

FEATURES

- **Built-in track-and-hold function**
- **No missing codes**
- **No external clocking**
- **Single supply $+5V_{DC}$**
- **Easy interface to all microprocessors, or operates stand-alone**
- **Latched TRI-STATE output**
- **Logic inputs and outputs meet both CMOS and TTL voltage level specifications**
- **Operates ratiometrically or with any reference value equal to or less than V_{CC}**
- **0V to 5V analog input voltage range with single 5V supply**
- **No zero or full-scale adjust required**
- **Overflow output available for cascading**
- **0.3″ standard width 20-pin DIP**

ORDERING INFORMATION

Device	Package	Temperature Range	Diff. Nonlinearity
KAD0820AIN	20 DIP	−40°C ~ +85°C	±1/2 LSB
KAD0820BIN			±1 LSB

BLOCK DIAGRAMS

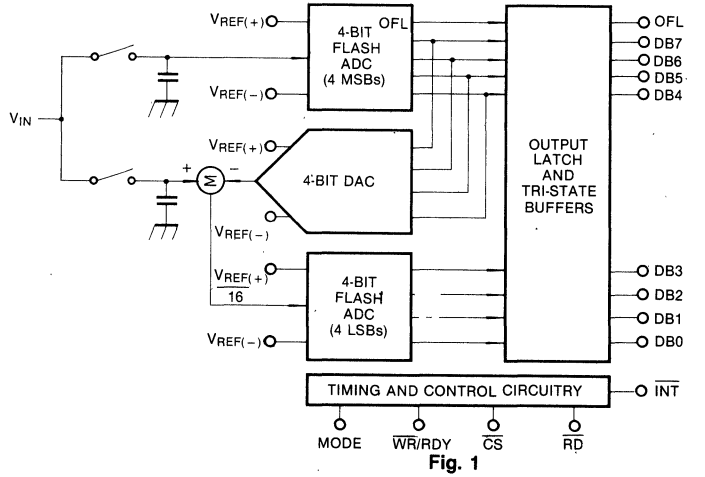


Fig. 1

ABSOLUTE MAXIMUM RATINGS (Note 1 & 2)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Package Dissipation at Ta = 25°C	P_D	875	mW
Logic Control Inputs	V_I	$-0.2 \sim V_{CC}+0.2$	V
Voltage at Other Inputs and Output	V_I	$-0.2 \sim V_{CC}+0.2$	V
Operating Temperature Range	T_{opr}	$-40 \sim +85$	°C
Storage Temperature Range	T_{stg}	$-65 \sim +150$	°C

ELECTRICAL CHARACTERISTICS

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = +5V, $V_{REF(+)}$ = +5V, and $V_{REF(-)}$ = GND, Ta = 25°C unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Resolution			—	8	8	Bits
Total Unadjusted Error (Note 3)	INL	KAD0820A KAD0820B	—	±1/2 ±1	±1/2 ±1	LSB LSB
Reference Resistance	R_{REF}		1.4	2.3	5.3	KΩ
Maximum $V_{REF(+)}$ Input Voltage		$V_{REF(+)max}$	—	V_{CC}	V_{CC}	V
Minimum $V_{REF(-)}$ Input Voltage		$V_{REF(-)min}$	—	GND	GND	V
Minimum $V_{REF(+)}$ Input Voltage		$V_{REF(+)min}$	—	$V_{REF(-)}$	$V_{REF(-)}$	V
Maximum $V_{REF(-)}$ Input Voltage		$V_{REF(-)max}$	—	$V_{REF(+)}$	$V_{REF(+)}$	V
V_{IN} Input Voltage	V_{IN}		GND-0.1	—	$V_{CC}+0.1$	V
Maximum Analog Input Leakage Current	I_L	$\overline{CS} = V_{CC}$ $V_{IN} = V_{CC}$ V_{IN} = GND	—	0.3 −0.3	3 −3	μA μA
Power Supply Sensitivity	I_S	V_{CC} = 5V ± 5%	—	±1/16	±1/4	LSB

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DC ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC} = 5V$, $Ta = 25°C$ unless otherwise specified.

Characteristic	Symbol	Test Conditions		Min	Typ	Max	Units
Logical "1" Input Voltage	$V_{IN(1)}$	$V_{CC} = 5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.0	—	V_{CC}	V
			Mode	3.5	—	V_{CC}	V
Logical "0" Input Voltage	$V_{IN(0)}$	$V_{CC} = 4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$	0	—	0.8	V
			Mode	0	—	1.5	V
Logical "1" Input Current	$I_{IN(1)}$	$V_{IN(1)} = 5V$; $\overline{CS}$, $\overline{RD}$		—	0.1	1	μA
		$V_{IN(1)} = 5V$; $\overline{WR}$		—	0.1	1	μA
		$V_{IN(1)} = 5V$; Mode		—	50	170	μA
Logical "0" Input Current	$V_{IN(0)}$	$V_{IN(0)} = 0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		—	0.1	1	μA
Logical "1" Output Voltage	$V_{OUT(1)}$	$V_{CC} = 4.75V$, $I_{OUT} = -360\mu A$; DB0 – DB7, $\overline{OFL}$, $\overline{INT}$		—	2.4	2.8	V
		$V_{CC} = 4.75V$, $I_{OUT} = -10\mu A$; DB0 – DB7, $\overline{OFL}$, $\overline{INT}$		—	4.5	4.6	V
Logical "0" Output Voltage	$V_{OUT(0)}$	$V_{CC} = 4.75V$, $I_{OUT} = 1.8mA$; DB0 – DB7, $\overline{OFL}$, $\overline{INT}$, RDY		—	0.34	0.4	V
TRI-STATE Output Current	I_{OUT}	$V_{OUT} = 5V$; DB0 – DB7, RDY		—	0.1	1	μA
		$V_{OUT} = 0V$; DB0 – DB7, RDY		—	−0.1	−1	μA
Output Source Current	I_{SOURCE}	$V_{OUT} = 0V$; DB0 – DB7, OFL		−7.2	−12	—	mA
		$\overline{INT}$		−5.3	−9	—	mA
Output Sink Current	I_{SINK}	$V_{OUT} = 5V$; DB0 – DB7, OFL, $\overline{INT}$, RDY		8.4	14	—	mA
Supply Current	I_{CC}	$\overline{CS} = \overline{WR} = \overline{RD} = 0$		—	7.5	13	mA

AC ELECTRICAL CHARACTERISTICS

The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20ns$, $V_{REF(+)} = 5V$, $V_{REF(-)} = GND$ and $Ta = 25°C$ unless otherwise specified.

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
Conversion Time for $\overline{RD}$ Mode		t_{CRD}	Pin 7 = 0, (Figure 2)	—	1.6	2.5	μs
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		t_{RCCO}	Pin 7 = 0, (Figure 2)	—	$t_{CRD} + 20$	$t_{CRD} + 50$	ns
Conversion Time for WR-RD Mode		t_{CWR-RD}	Pin 7 = V_{CC}; $t_{WR} = 600ns$, $t_{RD} = 600ns$; (Figures 3a and 3b)	—	1.52	—	μs
Write Time	Min	t_{WR}	Pin 7 = V_{CC}; (Figures 3a and 3b)	—	—	600	ns
	Max		(Note 4) See Graph	—	50	—	μs
Read Time	Min	t_{RD}	Pin 7 = V_{CC}; (Figures 3a and 3b) (Note 4) See Graph	—	—	600	ns

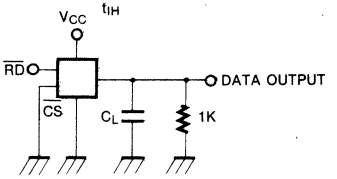
AC ELECTRICAL CHARACTERISTICS (Continued) The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20ns$, $V_{REF(+)} = 5V$, $V_{REF(-)} = 0V$ and $Ta = 25°C$ unless otherwise specified.

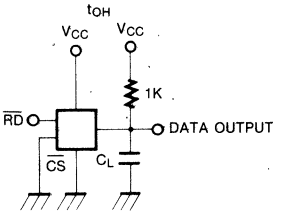
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	t_{ACC1}	Pin 7 = V_{CC}, $t_{RD} < t_I$; (Figure 3a) $C_L = 15pF$	—	190	280	ns
		$C_L = 100pF$	—	210	320	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	t_{ACC2}	Pin 7 = V_{CC}, $t_{RD} > t_I$; (Figure 3b) $C_L = 15pF$	—	70	120	ns
		$C_L = 100pF$	—	90	150	ns
Internal Comparison Time	t_I	Pin 7 = V_{CC}; (Figure 3b and 4) $C_L = 50pF$	—	800	1300	ns
TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	t_{1H}, t_{0H}	$R_L = 1K$, $C_L = 10pF$	—	100	200	ns
Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	$\overline{t_{INTL}}$	Pin 7 = V_{CC}, $C_L = 50pF$ $t_{RD} > t_I$; (Figure 3b) $t_{RD} < t_I$; (Figure 3a)	—	$t_{RD} + 200$	t_I ns $t_{RD} + 290$ ns	
Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	$\overline{t_{INTH}}$	(Figure 2, 3a and 3b) $C_L = 50pF$	—	125	225	ns
Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	$\overline{t_{INTHWR}}$	(Figure 4), $C_L = 50pF$	—	175	270	ns
Delay from $\overline{CS}$ to RDY	t_{RDY}	(Figure 2), $C_L = 50pF$, Pin 7 = 0	—	50	100	ns
Delay from $\overline{INT}$ to Output Valid	t_{ID}	(Figure 4)	—	20	50	ns
Delay from $\overline{RD}$ to $\overline{INT}$	t_{RI}	Pin 7 = V_{CC}, $t_{RD} < t_I$ (Figure 3a)	—	200	290	ns
Delay from End of Conversion to Next Conversion	t_P	(Figure 2, 3a, 3b and 4) (Note 4) See Graph	—	—	500	ns
Slew Rate, Tracking			—	0.1	—	V/μs
Analog Input Capacitance	C_{VIN}		—	45	—	pF
Logic Output Capacitance	C_{OUT}		—	5	—	pF
Logic Input Capacitance	C_{IN}		—	5	—	pF

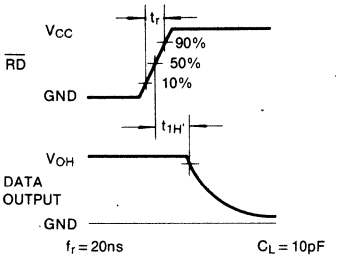
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
Note 2: All voltages are measured with respect to GND, unless otherwise specified.
Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.
Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RP} graphs.

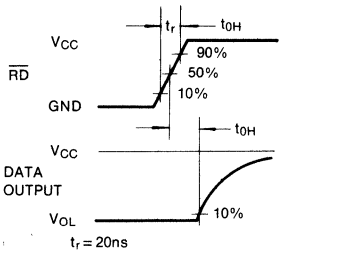
5

TRI-STATE TEST CIRCUITS AND TIMING DIAGRAMS









TIMING DIAGRAMS

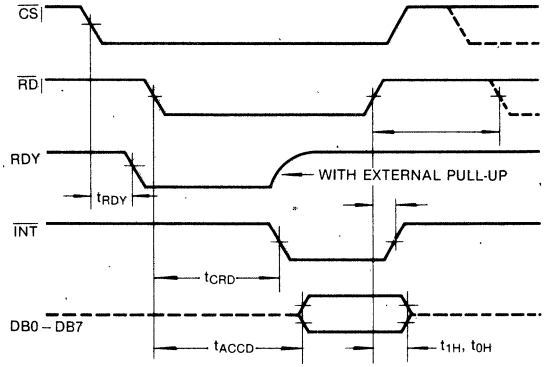


Fig. 2 RD Mode (Pin 7 is Low)

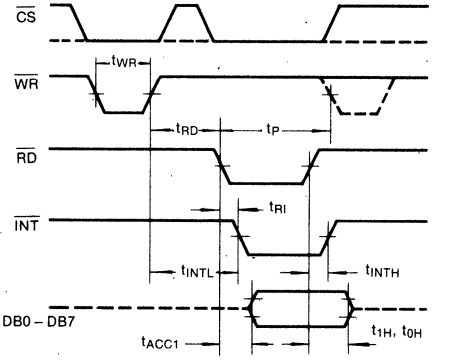


Fig. 3a WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)

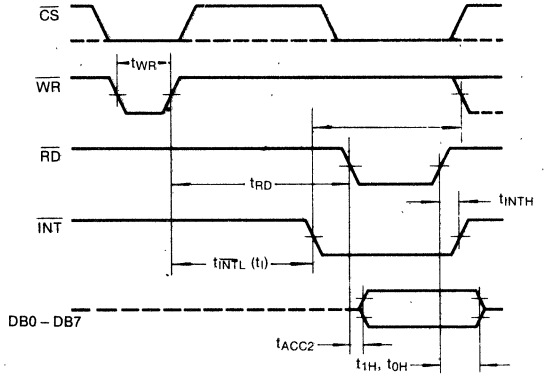


Fig. 3b WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

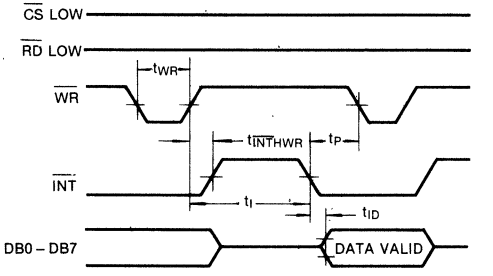
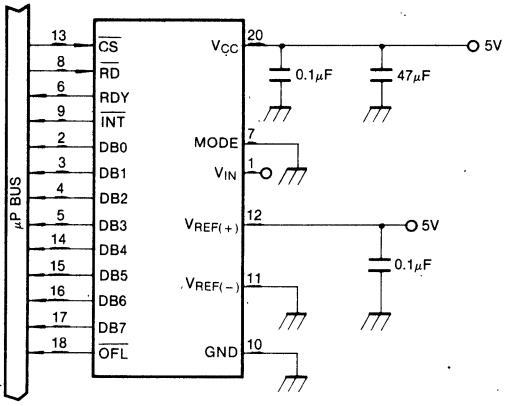
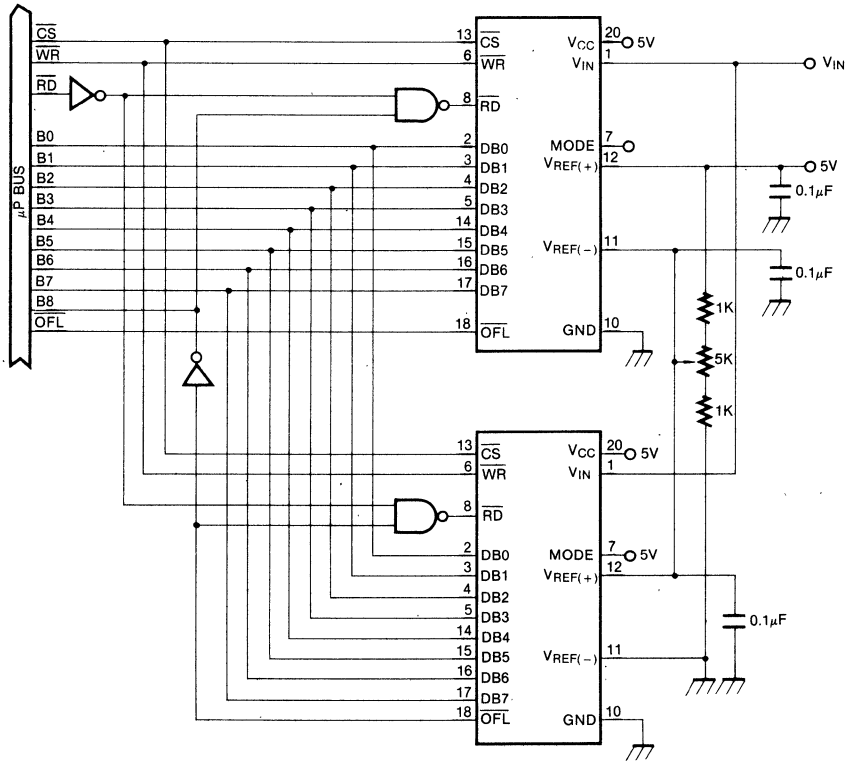


Fig. 4 WR-RD Mode (Pin 7 is High)
Stand-Alone Operation

TYPICAL APPLICATIONS

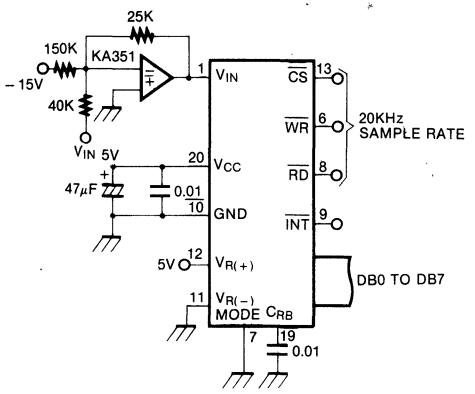


8-Bit Resolution Configuration

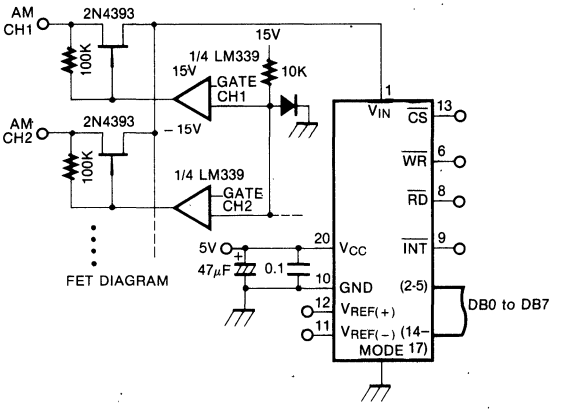


9-Bit Resolution Configuration

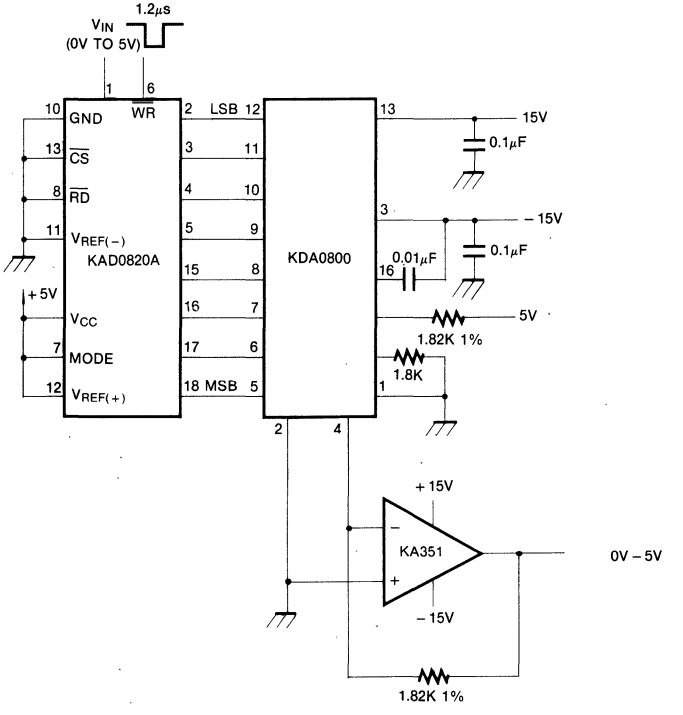
TYPICAL APPLICATIONS (Continued)



Telecom A/D Converter



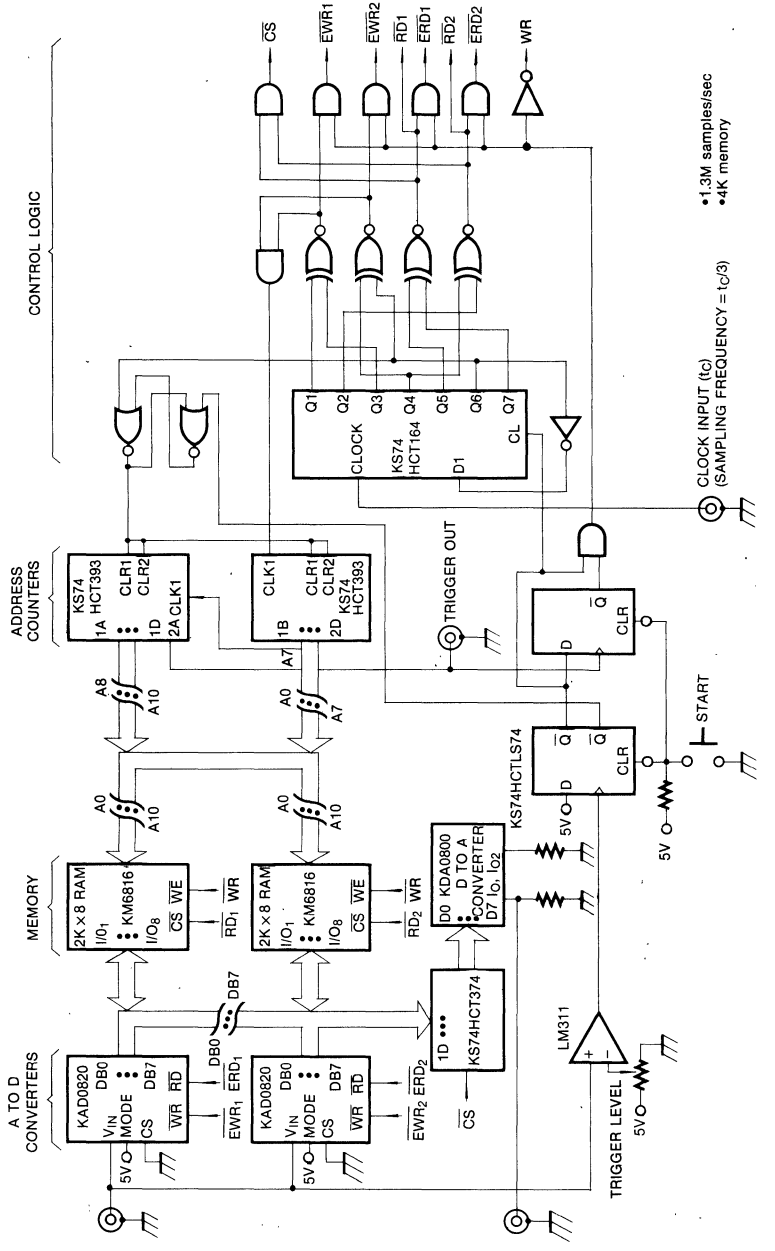
Multiple Input Channels



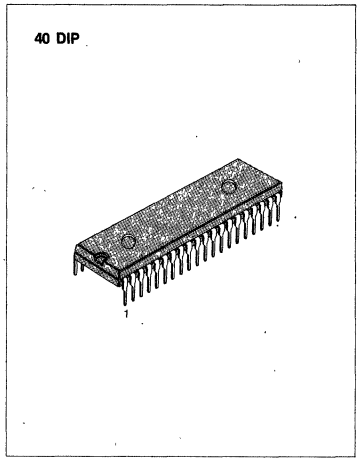
Fast Infinite Sample-and-Hold

TYPICAL APPLICATIONS (Continued)

Digital Waveform Recorder



3 1/2 DIGIT A/D CONVERTER



The single chip CMOS KS7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution-0.05%-indicating meter requires only a display, four resistors, four capacitors and 9V battery.

The KS7126 dual slope conversion technique rejects interference signal when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 40Hz line frequency signals are present. With an auto-zero error less than 10μV, zero drift less than 1μV/°C, input bias current of 10pA max and rollover error of less than one count, the KS7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power KS7126 can be used as a plug-in replacement for existing 7106 based systems by changing only the values of seven passive components.

FEATURES

- **Long Battery Life: 800 Hours Typical**
- **Auto-Zero Cycle**
- **Guaranteed Zero Reading With Zero Input**
- **Low Noise: 15μVp-p**
- **High Resolution (0.05%) and Wide Dynamic Range (72dB)**
- **Low Input Leakage Current: 1pA Typical, 10pA Maximum**
- **Direct LCD Display Drive-No External Components**
- **Precision Null Detection With True Polarity at Zero**
- **High Impedance Differential Input**
- **Convenient 9V Battery Operation With Low Power Dissipation: 500μW Typical, 900μW Maximum**
- **Internal Clock Circuit**
- **Drop-In Replacement for TSC7126, ICL7126**

ORDERING INFORMATION

Device	Package	Temperature Range
KS7126CN	40 DIP	0 ~ +70°C

TYPICAL APPLICATIONS

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid/flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	V
Analog Input Voltage (Either Input) (1)	V_{IN}	$V_{CC} \sim V_{EE}$	V
Reference Input Voltage (Either Input)	V_{REF}	$V_{CC} \sim V_{EE}$	V
Clock Input	V_{CL}	Test $\sim V_{CC}$	V
Power Dissipation	P_d	800	mW
Lead Temperature (Soldering, 60 Sec)	T_l	300	°C
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +160	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditons	Min	Typ	Max	Unit
Zero Input Reading	—	$V_{IN} = 0.0V$ Full scale = 200.0mV	−000.0	+000.0	+000.0	Digital Reading
Zero Rading Drift	—	$V_{IN} = 0$, 0°C<Ta<70°C		0.2	1	μV/°C
Ratiometric Reading	—	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999 1000	1000	Digital Reading
Linearity (Max. deviation from straight line fit)	NL	Full scale = 200mV or full scale = 2,000V	−1	+0.2	+1	Counts
Rollover Error (Difference in reading for equal positive and negative reading near full scale)	—	$-V_{IN} = +V_{IN}$ = 200.0mV	−1	+0.2	+1	Counts
Noise (Pk-Pk value not exceed 95% of time)	E_N	$V_{IN} = 0V$	—	—	15	μV
Leakage Current @ Input	I_L	$V_{IN} = 0V$		1	10	pA
Common Mode Rejection Ratio	CMRR	$V_{CM} = +1V$; $V_{IN} = 0V$ Full scale = 200.0mV	—	50	—	μV/V
Scale Factor Temperature Coefficient	—	V_{IN} = 199.0mV 0<Ta<70°C (Ext. Ref. 0 ppm/°C)	—	1	5	ppm/°C
Temp. Coeff. of Analog Common (with respect to positive supply)	V_{CTL}	250KΩ between common and positive supply	—	80	—	ppm/°C
Analog Common Voltage (with respect to positive supply)	V_C	250KΩ between common and positive supply	2.4	2.8	3.2	V
Pk-Pk Segment Drive Voltage (Note 5)	V_{SO}	V_{CC} to V_{EE} = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V_{BD}	V_{CC} to V_{EE} = 9V	4	5	6	V
Power Supply Current	I_S	$V_{IN} = 0V$, V_{CC} to V_{EE} = 9V	—	55	100	μA

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Notes

1) Input voltage may exceed the supply voltage provided the input current is limited to ± 100μA
2) Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3) Unless otherwise noted, specifications apply T_a =25°C, f_{CLOCK} =16KHz and are tested in the circuit of Figure 1.
4) Refer to "Differential Input" discussion on page 7.
5) Backplane drive is in phase with segment drive for 'off' segment, 180 out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6) During auto-zero phase, current is 10 ~ 20μA higher, 48KHz oscillator, Figure 2, increases current by 8μA (Typ.)

TYPICAL OPERATING CIRCUITS

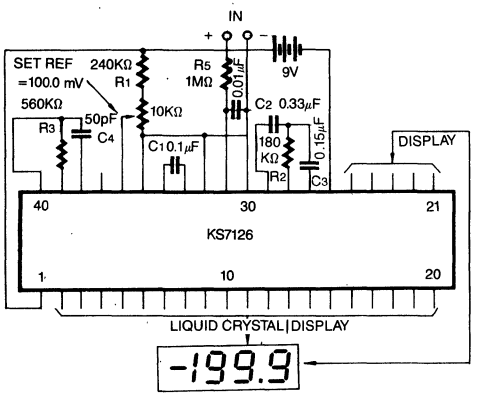


Figure 1: KS7126 Clock Frequency 16 KHz (1 reading/sec.)

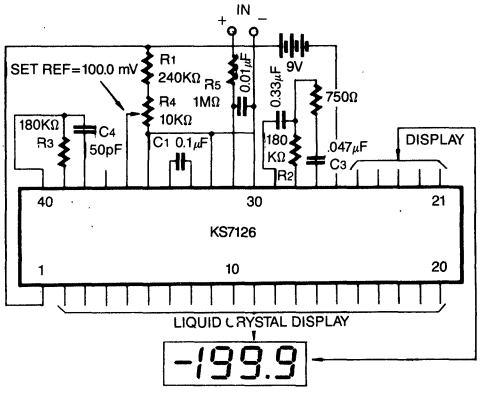
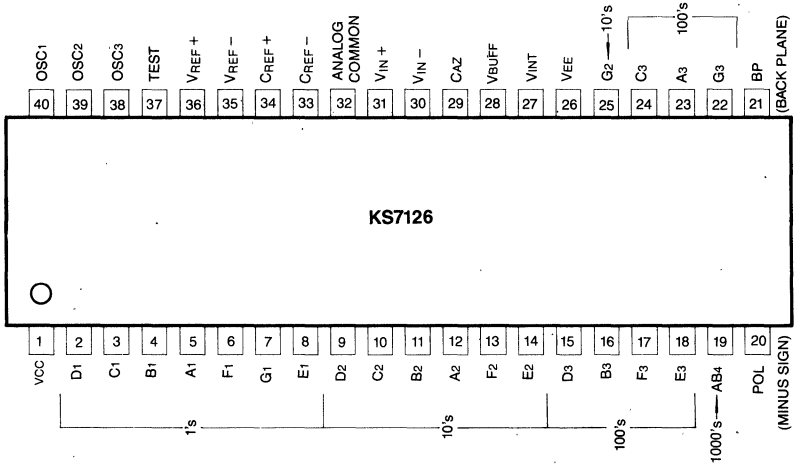


Figure 2: KS7126 Clock Frequency 48 KHz (3 readings/sec.)

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	Name	Description
1	V_{CC}	Positive supply voltage.
2	D_1	Activates the D section of the units display.
3	C_1	Activates the C section of the units display.
4	B_1	Activates the B section of the units display.
5	A_1	Activates the A section of the units display.
6	F_1	Activates the F section of the units display.
7	G_1	Activates the G section of the units display.
8	E_1	Activates the E section of the units display.
9	D_2	Activates the D section ofthe tens display.
10	C_2	Actatives the C section of the tens display.
11	B_2	Activates the B section of the tens display.
12	A_2	Activates the A section of the tens display.
13	F_2	Activates the F section of the tens display.
14	E_2	Activates the E section of the tens display.
15	D_3	Activates the D section of the hundreds display.
16	B_3	Activates the B section of the hundreds display.
17	F_3	Activates the F section of the hundreds display.
18	E_3	Activates the E section of the hundreds display.
19	AB_4	Activates both halves of the 1 in the thousands display.
20	POL	Activates the negative polarity display.
21	BP	Backplane drive output
22	G_3	Activates the G section of the hundreds display.
23	A_3	Activates the A section of the hundreds display.
24	C_3	Activates the C section ofthe hundreds display.
25	G_2	Activates the G section of the tens display.
26	V_{EE}	Negative power supply voltage.
27	V_{INT}	The integrating capacitor should be selected to give maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 reading per second, a 0.047μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	V_{BUFF}	Integration resistor connection. Use a 180KΩ fr a 200mV full-scale range and a 1.8MΩ for 2V full-scale range.
29	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33μF capacitor for a 200mV full-scale, and 0.033μF capacitor for a 2V full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.

PIN DESCRIPTION (Continued)

Pin Number	Name	Description
30	$V_{IN}-$	The low input is connected to this pin.
31	$V_{IN}+$	The high input signal is connected to this pin.
32	ANALOG COMMON	This pin is primarily used to set the analog common-mode voltage for battery operation or in sytem where the input signal is referenced to the power supply. See paragraph for ANALOG COMMON for more details. It also acts as a reference voltage source.
33	$C_{REF}-$	See pin 34
34	$C_{REF}+$	A 0.1μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200mV scale is used, a 1.0μF is recommended and will hold the rollover error to 0.5 count.
35	$V_{REF}-$	See pin 36.
36	$V_{REF}+$	The analog input required to generate a full-scale output (1.999 counts). Place 100mV between pins 35 and 36 for 199.9mV full-scale. Place 1.000 volt between pins 35 and 36 for 2V full-scale. See paragraph on REFERENCE VOLTAGE.
37	TEST	Lamp test. When pulled high (to V_{CC}) all segments will be turned ON and the display should read −1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	OSC_3	See pin 40.
39	OSC_2	See pin 40.
40	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48KHz clock (3 readings per second) connect pin 40 the junction of a 180KΩ resistor an a 50pF capacitor. The 180K resistor is tied to pin 39 an the 50pF capacitor is tied to pin 38.

DETAILED DESCRIPTION

ANALOG SECTION

Fig. 3 shows the Block Diagram of the Analog Section for the KS7126. Each measurement cycle is divided into three phases. They are (1) Auto-zero (A-Z), (2) Signal integrate (INT) and (3) De-Integrate (DE).

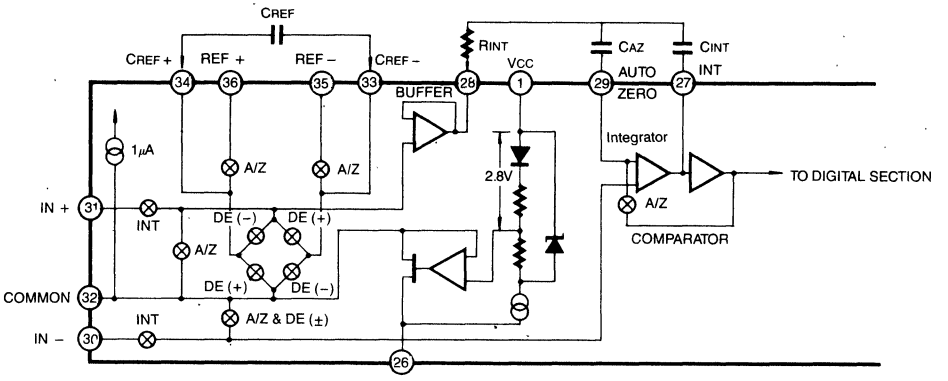


Fig. 3 Analog Section of KS7126

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN+ and IN– for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN– can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000(\frac{V_{IN}}{V_{REF}})$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its modes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error However, by selecting the reference capacitor large enough in comparision to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (See component Value Section)

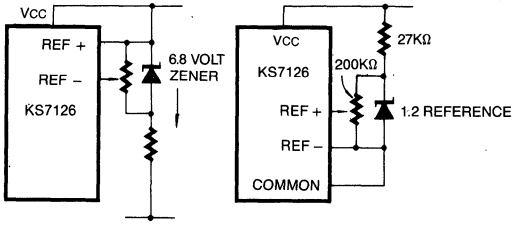


Fig. 4: Using an External Reference

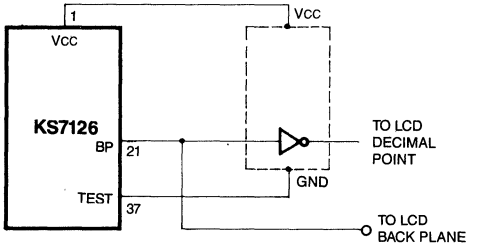


Figure 5: Simple Inverter for Fixed Decimal Point

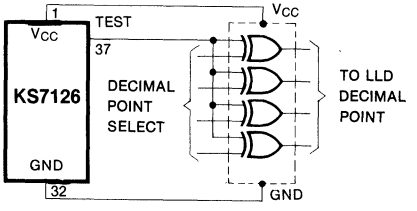


Figure 6: Exclusive-OR Gate for Decimal Point

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≅15Ω), and a temperature coefficient typically less than 80 ppm/°C.

The limitations of the on-chip reference should be also recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Fig. 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN− is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN− will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 100μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display Fig. 5 and Fig. 6 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test". When TEST is pulled high (to V_{CC}) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

DIGITAL SECTION

Fig. 7 shows the digital section for the KS7126. An internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive current when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN− and IN+ are reversed, this indication can be reversed also, if desired.

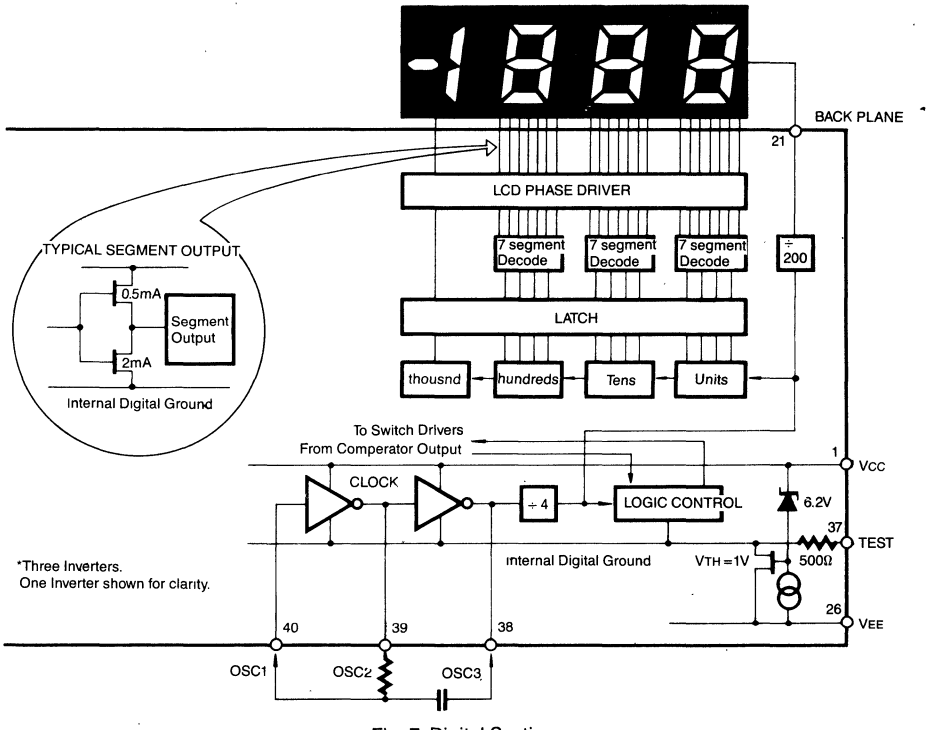


Fig. 7: Digital Section

System Timing

Fig. 8 shows the clocking arrangement used in the KS7126. Three basic clocking arrangements can be used.

1. An external oscillator connected to pin 40
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins

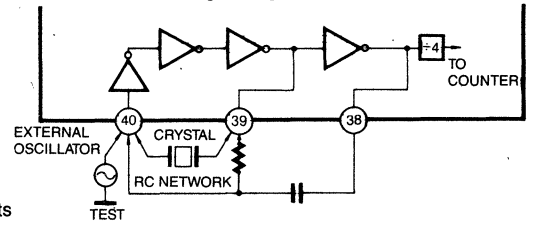


Fig. 8: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counts. It is then futher divided to form the three convert — cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto — zero (1000 to 3000 counts). For signals less than full scale, auto — zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (1,600 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 KHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequency of 60KHz, 48KHz, 33⅓KHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔KHz, 50KHz, 40KHz, etc. would be suitable. Note that 40KHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz)

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~ 1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8MΩ is near optimum and similarly 180KΩ for a 200.0mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integral swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine.For three readings/second (48KHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16KHz) 0.15μF of course, it different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost. At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF– pin is not analog COMMON) and a 200mV scale is used, a large value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \approx \frac{45}{RC}$ For 48KHz clock (3 readings/second) R=18KΩ

TYPICAL APPLICATIONS

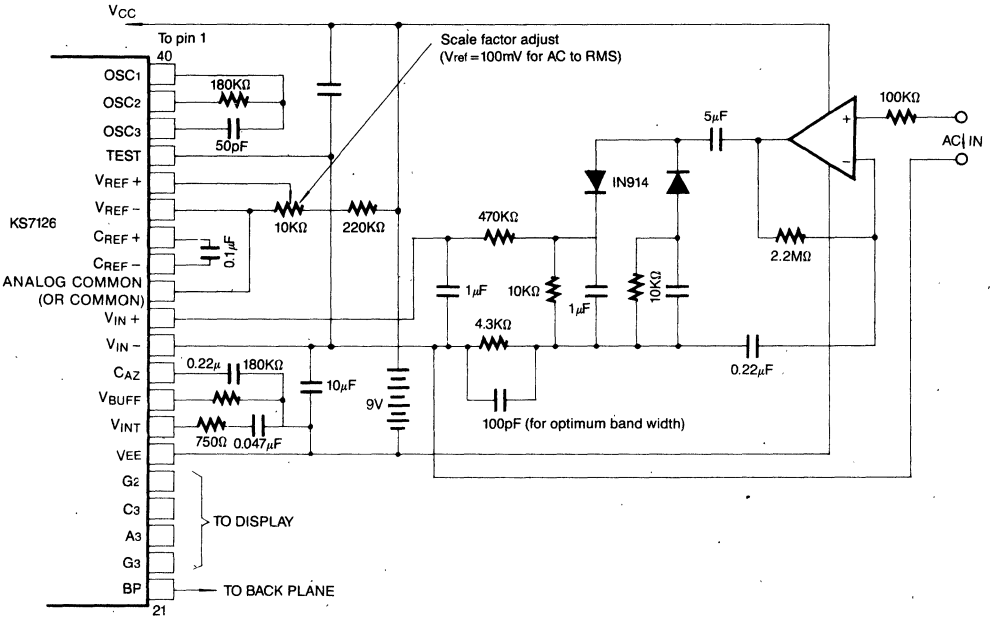


Figure 9: AC to DC Converter with KS7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-Amps.

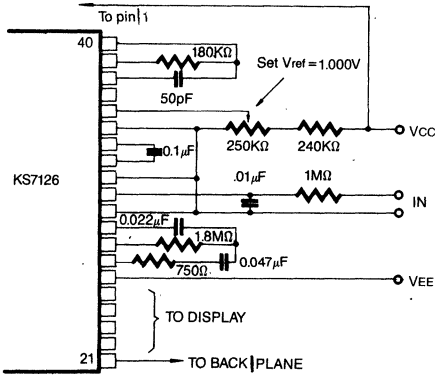


Figure 10: Recommended Values for 2.000V Full-Scale, Three Readings Per Second.

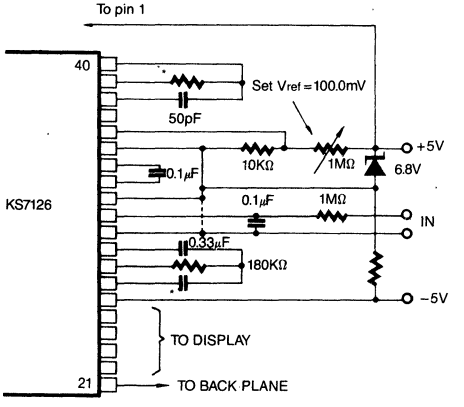


Figure 11: KS7126 with Zener Diode Reference.

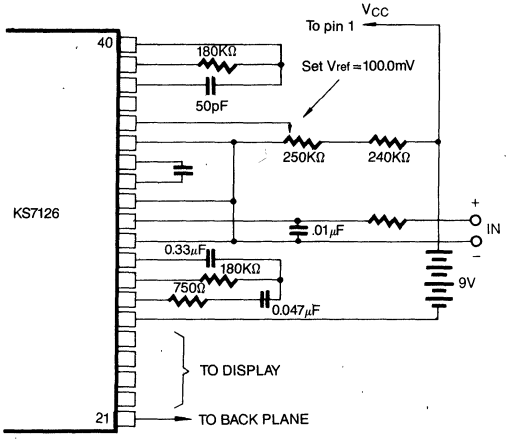


Figure 12: KS7126 Using the Internal Reference. 200.0mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9V Battery).

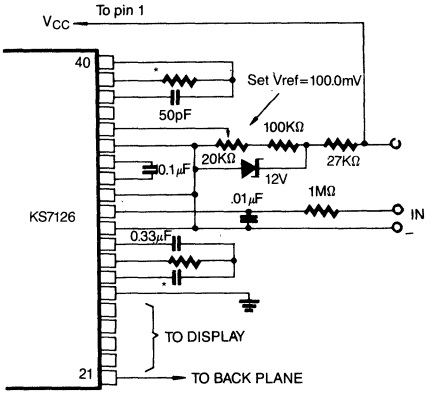
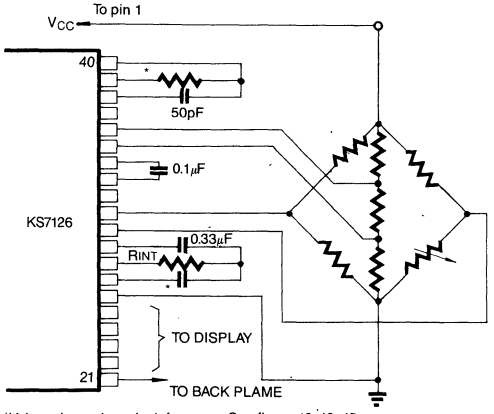


Figure 13: KS7126 Operated From Single +5V Supply. An External Reference Must Be Used.



*Values depend on clock frqeucny. See figure 10, 12, 15.

Figure 14: KS7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within theBridge are Determined by the Desired Sensitivity.

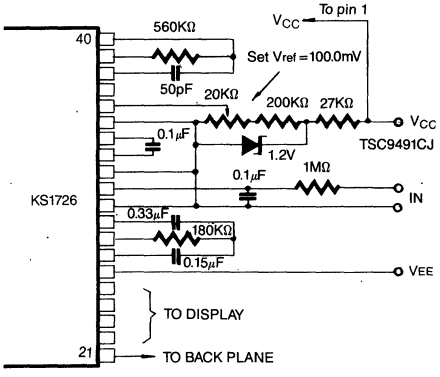


Figure 15: KS7126 with an External Band-Gap Reference (1.2V Typ) IN− is tied to Common. Values Shown are for One Reading Per Second.

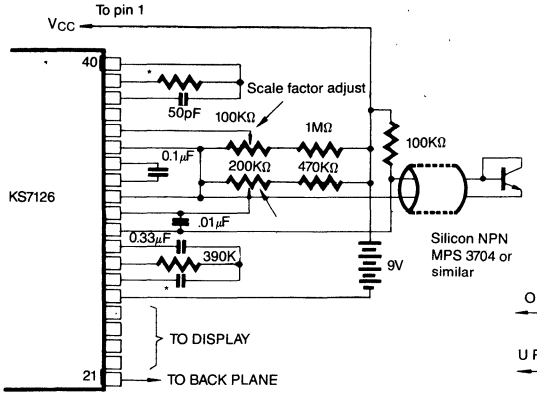


Figure 16: KS7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2mV/°C.

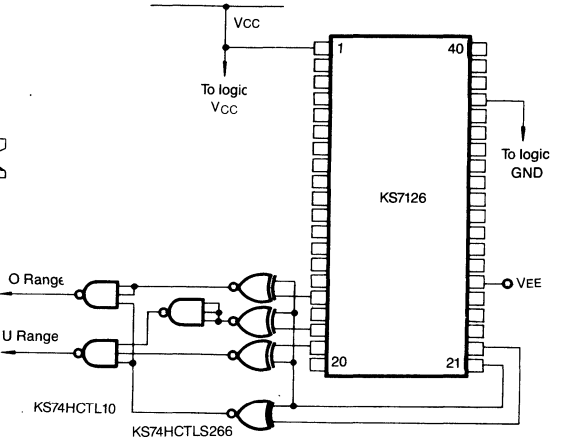


Figure 17: Circuit for Developing Underrange and Overrange Signals from KS7126 Outputs.

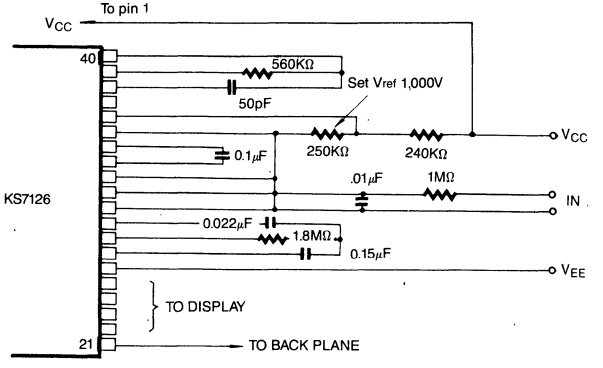


Figure 18: Recommended Component Values for 2.00V Full-Scale, One Reading Per Second.

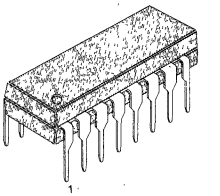
*Values depend on clock frequency. See Figure 10, 12,15

8-BIT D/A CONVERTER

The KDA0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The KDA0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 V_{p-p} with simple resistor loads. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the KDA0800 series will accept TTL levels with the logic threshold pin, V_{LC}, potential allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33mW with ±5V supplies and is independent of the logic input states.

16 DIP



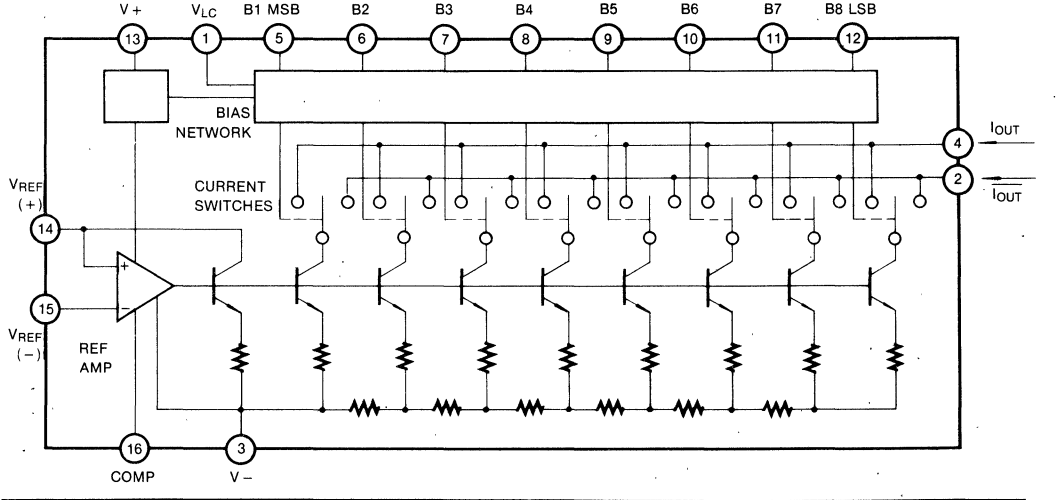
FEATURES

- **Fast settling output time: 100ns**
- **Full scale error: ±1 LSB**
- **Nonlinearity over temperature: ±0.1%**
- **Full scale current drift: ±10 ppm/°C**
- **High output compliance: −10V to +18V**
- **Complementary current outputs**
- **Interface directly with TTL, CMOS, PMOS and others**
- **2 quadrant wide range multiplying capability**
- **Wide power supply range: ±4.5V to ±18V**
- **Low power consumption: 33mW at ±5V**
- **Low cost**
- **Standard 16 DIP package**

ORDERING INFORMATION

Device	Package	Temperature Range	Nonlinearity
KDA0800CN	16 DIP	0 ~ +70°C	±0.19%FS
KDA0801CN			±0.39%FS
KDA0802CN			±0.1%FS

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	± 18V or 36V	V
Power Dissipation	P_D	500mW	mW
Reference Input Differential Voltage (V14 to V15)	V_{IN}	$V_- \sim V_+$	V
Reference Input Common-Mode Range (V14, V15)	V_{IN}	$V_- \sim V_+$	V
Reference Input Current	I_{ref}	5mA	mA
Logic Inputs	V_{IN}	$V_- \sim V_- + 36V$	V
Operating Temperature	T_{opr}	0°C ~ +70°C	°C
Storage Temperature	T_{stg}	−65°C ~ +150°C	°C

ELECTRICAL CHARACTERISTICS

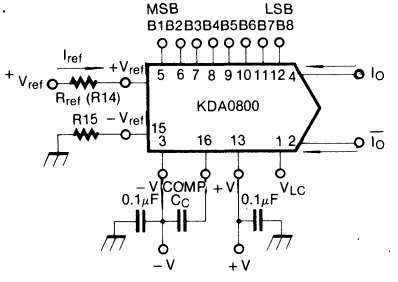
($V_S = \pm 15V$, $I_{ref} = 2mA$, $T_{min} \leq Ta \leq T_{max}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Characteristic	Symbol	Test Conditions	KDA0800			Unit
			Min	Typ	Max	
Resolution			8	8	8	Bits
Monotonicity			8	8	8	Bits
Nonlinearity		KDA0802 KDA0800 KDA0801	—	—	±0.1 ±0.19 ±0.39	%FS
Settling Time	t_S	To ± 1/2 LSB, all bits switched "ON" or "OFF", Ta = 25°C	—	100	150	ns
Propagation Delay Each Bit All Bits Switched	t_{PLH}, t_{PHL}	Ta = 25°C	 — —	 35 35	 60 60	 ns ns
Full Scale Tempco	TCI_{FS}			± 10	± 50	ppm/°C
Output Voltage Compliance	V_{OC}	Full scale current change < 1/2 LSB, R_{OUT} > 20MΩ Typ	−10	—	18	V
Full Scale Current	I_{FS4}	$V_{ref} = 10V$, R14 = 5KΩ R15 = 5KΩ, Ta = 25°C	1.94	1.99	2.04	mA
Full Scale Symmetry	I_{FSS}	$I_{FS4} - I_{FS2}$	—	± 1	± 8.0	μA
Zero Scale Current	I_{ZS}		—	0.2	2.0	μA
Output Current Range	I_{FSR}	V− = −5V V− = −8V to −18V	0 0	2.0 2.0	2.1 4.2	mA mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	$V_{LC} = 0V$	 0 2.0	 — —	 0.8 V_{CC}	 V V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	$V_{LC} = 0V$ $-10V \leq V_{IN} \leq +0.8V$ $2V \leq V_{IN} \leq +18V$	 — —	 −2.0 0.002	 −10 10	 μA μA
Logic Input Swing	V_{IS}	V− = −15V	−10	—	18	V
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$	−10	—	13.5	V
Reference Bias Current I_{15}			—	−1.0	μA	μA
Reference Input Slew Rate	dI/dt		4.0	8.0	—	mA/μs
Power Supply Sensitivity	$PSSI_{FS+}$	$4.5V \leq V+ \leq 18V$	—	0.0001	0.01	%/%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	Test Conditions	KDA0800			Unit
			Min	Typ	Max	
	$PSSI_{FS-}$	$-4.5V \leq V- \leq 18V$ $I_{ref} = 1mA$	—	0.0001	0.01	%/%
Power Supply Current		$V_S = \pm 5V$, $I_{ref} = 1mA$				
	I+		—	2.3	3.8	mA
	I−		—	−4.3	−5.8	mA
		$V_S = 5V, -15V$, $I_{ref} = 2mA$				
	I+		—	2.4	3.8	mA
	I−		—	−6.4	−7.8	mA
		$V_S = \pm 15V$, $I_{ref} = 2mA$				
	I+		—	2.5	3.8	mA
	I−		—	−6.5	−7.8	mA
Power Dissipation	P_D	$\pm 5V$, $I_{ref} = 1mA$	—	33	48	mW
		$5V, -15V$, $I_{ref} = 2mA$	—	108	136	mW
		$\pm 15V$, $I_{ref} = 2mA$	—	135	174	mW

TYPICAL APPLICATIONS



$$I_{FS} \cong \frac{+V_{ref}}{R_{ref}} \times \frac{255}{256}$$

$I_O + \overline{I_O} = I_{FS}$ for all logic states

For fixed reference, TTL operation, typical values are:

$V_{ref} = 10V$

$R_{ref} = 5K\Omega$

$R15 \cong R_{ref}$

$C_C = 0.01\mu F$

$V_{LC} = 0V$ (Ground)

Fig. 1 Basic Positive Reference Operation

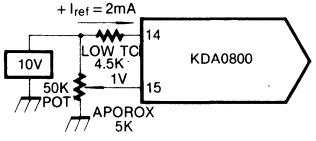
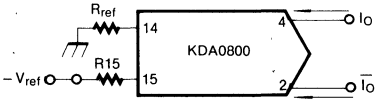


Fig. 2 Recommended Full Scale Adjustment Circuit

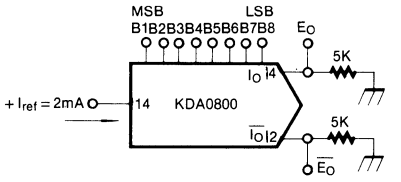


$$I_{FS} \cong \frac{-V_{ref}}{R_{ref}} \times \frac{255}{256}$$

Note: R_{ref} sets I_{FS}: R15 is for bias current cancellation

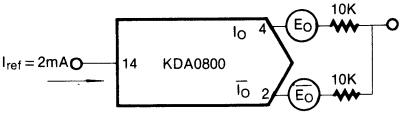
Fig. 3 Basic Negative Reference Operation

TYPICAL APPLICATIONS (Continued)



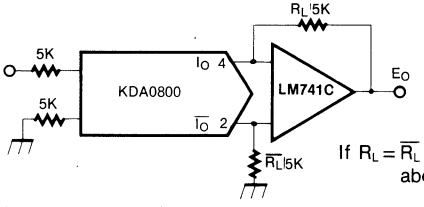
	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	0.000
Full Scale − LSB	1	1	1	1	1	1	1	0	1.984	0.008	−9.920	−0.040
Half Scale + LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale − LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

Fig. 4 Basic Unipolar Negative Operation



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos. Full Scale	1	1	1	1	1	1	1	1	−9.920	+10.000
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	−9.840	+9.920
Zero Scale + LSB	1	0	0	0	0	0	0	1	−0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale − LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	+9.920	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	−9.920

Fig. 5 Basic Diploar Output Operation

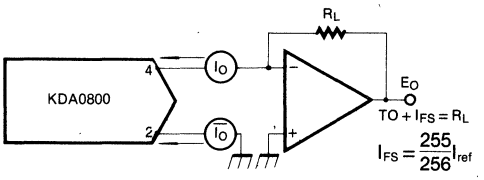


If $R_L = \overline{R_L}$ within ±0.05%, output is symmetrical about ground

	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.920
Pos. Full Scale − LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero Scale	1	0	0	0	0	0	0	0	+0.040
(−) Zero Scale	0	1	1	1	1	1	1	1	−0.040
Neg. Full Scale + LSB	0	0	0	0	0	0	0	1	−9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	−9.920

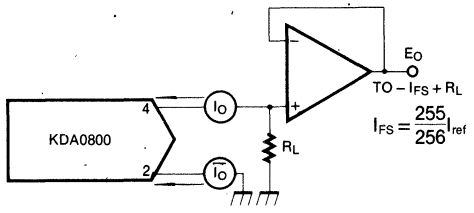
Fig. 6 Symmetrical Offset Binary Operation

TYPICAL APPLICATIONS (Continued)



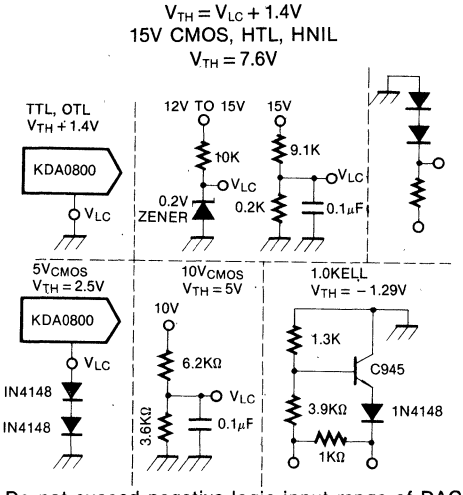
For complementary output (operation as negative logic DAC), connect inverting input of op amp to $\overline{I_O}$ (pin 2), connect I_O (pin 4) to ground.

Fig. 7 Positive Low Impedance Output Operation



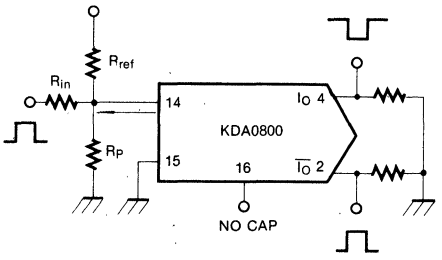
For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to I_O (pin 2); connect I_O (pin 2); connect I_O (pin 4) to ground.

Fig. 8 Negative Low Impedance Output Operation



Do not exceed negative logic input range of DAC.

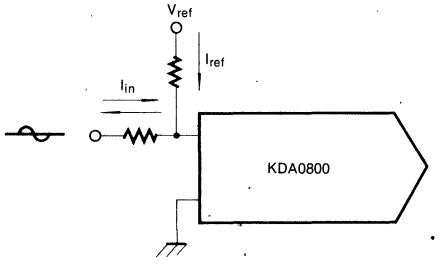
Fig. 9 Interfacing with Various Logic Families



Typical values: $R_{IN} = 5K_1 + V_{IN} = 10V$

Fig. 10 Pulsed Reference Operation

(a) $I_{ref} \geq$ peak negative swing of I_{IN}



(b) $+V_{ref}$ must be above peak positive swing of V_{IN}

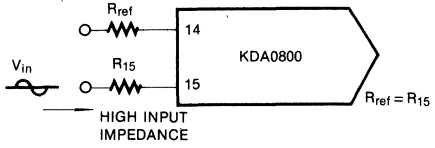


Fig. 11. Accommodating Bipdlar References

TYPICAL APPLICATIONS (Continued)

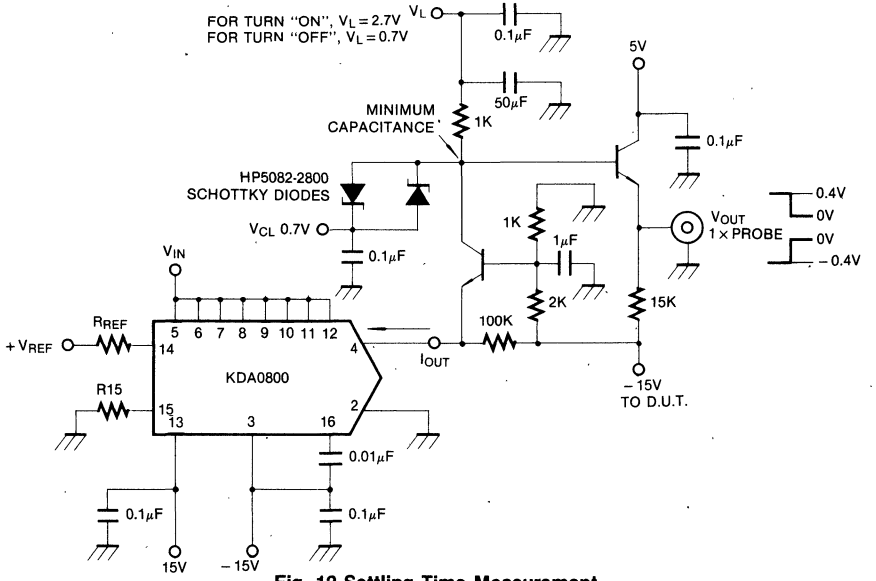
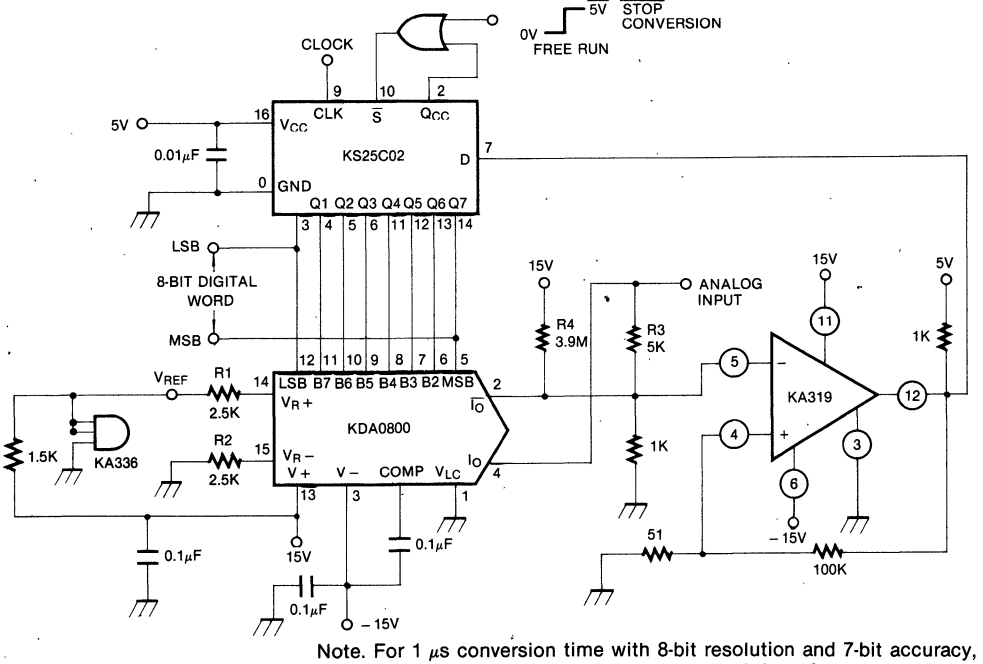


Fig. 12 Settling Time Measurement



Note. For 1 μs conversion time with 8-bit resolution and 7-bit accuracy, an KA361 comparator replaces the KA319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5KΩ and R4 to 2MΩ.

Fig. 13 A Complete 2 μs Conversion Time, 8-Bit A/D Converter

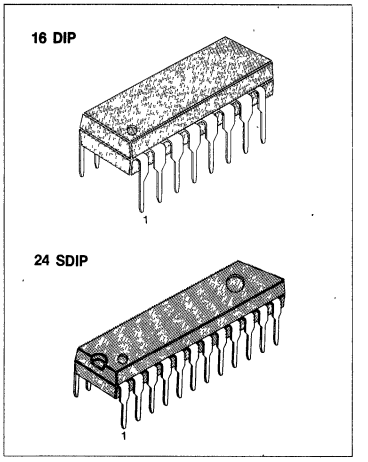
8-BIT AND 12-BIT CMOS SUCCESSIVE APPROXIMATION REGISTERS

These are 8-bit and 12-bit CMOS registers designed for use in successive approximation A/D converters. They contain all the logic and control circuits necessary in combination with the A/D converter to perform successive approximation analog-to-digital conversions.

The KS25C02 has 8 bits with serial capability and is not expandable. The KS25C03 has 8 bits and is expandable without serial capability. The KS25C04 has 12 bits with serial capability and expandibility.

Fabricated using a 2μm, dual-layer metal CMOS process, these parts deliver speeds and drive capability equivalent to their TTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.



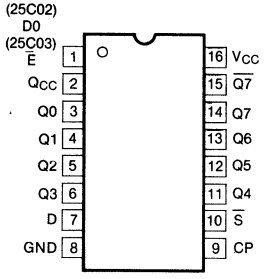
ORDERING INFORMATION

Device	Package	Temperature Range	Registers
KS25C02IN	16 DIP	−40°C ~ +85°C	4 bit
KS25C03IN	16 DIP		8 bit
KS25C04IN	24SDIP		12 bit

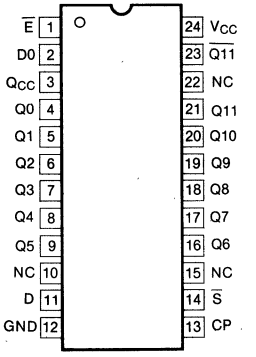
FEATURES

- **Complete logic for successive approximation A/D converters**
- **8-bit and 12-bit registers**
- **Capable of short cycle or expanded operation**
- **Continuous or start-stop operation**
- **Compatible with D/A converters using any logic code**
- **Active low or active high logic outputs**
- **Use as general purpose serial-to-parallel converter or ring counter**
- **Low power consumption characteristics of CMOS**
- **Inputs and outputs interface directly with TTL, NMOS and TTL devices.**

PIN CONFIGURATIONS

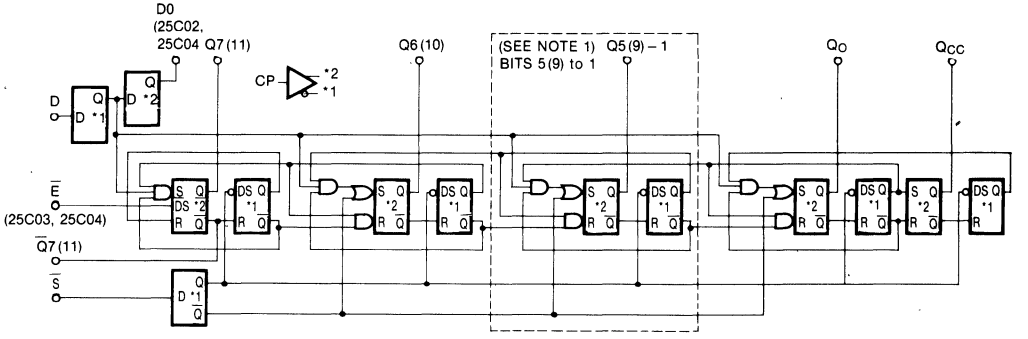


KS25C02 AND KS25C03



KS25C04

LOGIC DIAGRAM



NOTE 1: Cell logic is repeated for register stages Q5 to Q1 KS25C02, KS25C03
2: Numbers in parenthesis are for KS25C04

TRUTH TABLE

Time	Inputs			Outputs[1]									
t_n	D	$\overline{S}$	$\overline{E}$[2]	D0[3]	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

NOTES:
1: Truth table for KS25C04 is extended to include 12 outputs.
2: Truth table for KS25C02 does not include $\overline{E}$ column or last line in truth table shown.
3: Truth table for KS25C03 does not include D0 column.
H = High Voltage Level
L = Low Voltage Level
X = Don't Care
NC = No Change

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 ~ +7	V
DC Input Diode Current	I_{IK}	±20	mA
DC Output Diode Current	I_{OK}	±20	mA
Continuous Output Current Per Pin	I_O	±35	mA
Continuous Current Through V_{CC} or GND Pins	I_{CON}	±125	mA
Power Dissipation Per Package	P_D	500	mW
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	−55 ~ +125	°C

DC ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions)

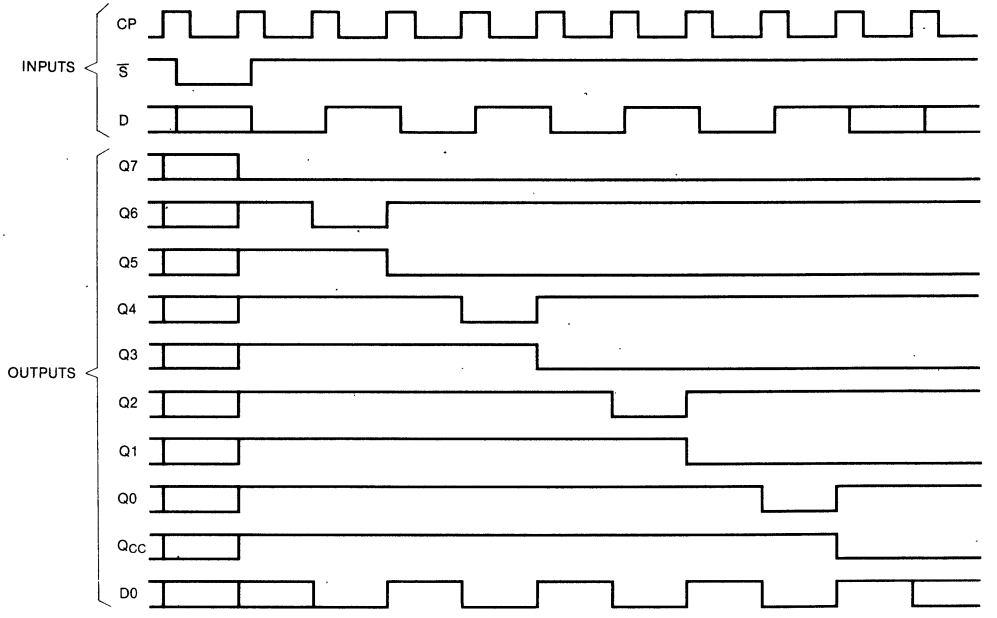
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage	V_{CC}		4.5	5.0	5.5	V
High-Level Input Voltage	V_{IH}	V_{CC} = Min	2.0	—	V_{CC}	V
Low-Level Input Voltage	V_{IL}	V_{CC} = Min	0	—	0.8	V
High-Level Output Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_O = −20μA I_O = −4mA	 V_{CC}-0.1 2.4	 — —	 V_{CC} V_{CC}	 V V
Low-Level Output Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_O = 20μA I_O = 9.6mA	 0 0	 — —	 0.1 0.4	 V V
Low-Level Input Current	I_{IL}	V_{CC} = Max, V_{IL} = 0.4V	—	0.5	1.0	μA
High-Level Input Current	I_{IH}	V_{CC} = Max, V_{IH} = 2.4V	—	0.5	1.0	μA
Supply Current	I_{CC}	V_{CC} = Max, V_{IN} = V_{CC} or GND	—	1.0	10.0	μA

AC ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions), C_L = 15pF

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay to a Logical "0" from CP to any Output	t_{PD0}		10	18	28	ns
Propagation Delay to a Logical "0" from $\overline{E}$ to Q7(Q11) Output	t_{PD0}	CP high, $\overline{S}$ low, KS25C03, KS25C04 only	—	15	24	ns
Propagation Delay to a Logical "1" from CP to Any Output	t_{PD1}		10	20	38	ns
Propagation Delay to a Logical "1" from $\overline{E}$ to Q7(Q11) Output	t_{PD1}	CP high, $\overline{S}$ low, KS25C03, KS25C04 only	—	12	19	ns
Data Input Setup Time	$t_{S(D)}$		−10	4	8	ns
Start Input Setup Time	$t_{S(S)}$		0	5	10	ns
Minimum Low CP Width	t_{PWL}		—	5	20	ns
Minimum High CP Width	t_{PWH}		—	15	20	ns
Maximum Clock Frequency	f_{MAX}		—	—	25	MHz

TIMING DIAGRAMS

KS25C02, KS25C03, KS25C04



APPLICATION INFORMATION

Operation

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the D0 output on the KS25C02 and KS25C04 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7(11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ signal must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7(11) register bit and the Q6(10) register bit and Q5(9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The KS25C02, KS25C03 and KS25C04 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

Logic Codes

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator 1/2 full range + 1/2 LSB and using the complement of the MSB ($\overline{Q7}$ or $\overline{Q11}$) with a binary D/A

APPLICATION INFORMATION (Continued)

converter. Offset binary is used in the same manner but with the MSB ($\overline{Q}7$ or $\overline{Q}11$). BCD D/A converters can be used with the addition of illegal code suppression logic.

Active High or Active Low Logic

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

Expanded Operation

An active low enable input, $\overline{E}$, on the KS25C03 and KS25C04 allows registers to be connected together to form a longer register by connecting the clock, D, and S inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start resets the register, the $\overline{E}$ signal goes high, forcing the Q7(11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

Short Cycle

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

Comparator Bias

To minimize the digital error below ±1/2 LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased + 1/2 LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased − 1/2 LSB.

Definition of Terms

CP: The clock input of the register.

D: The serial data input of the register.

D0: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7(11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_I I = 7(11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

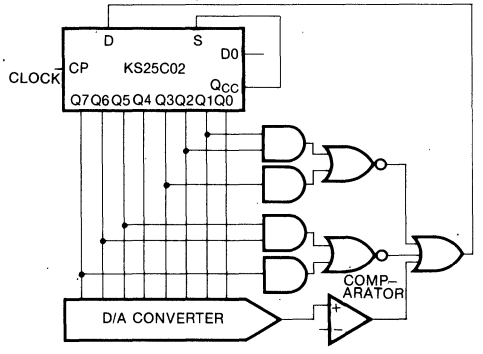
Q7(11): The true output of the MSB of the register.

$\overline{Q7}$(11): The complement output of the MSB of the register.

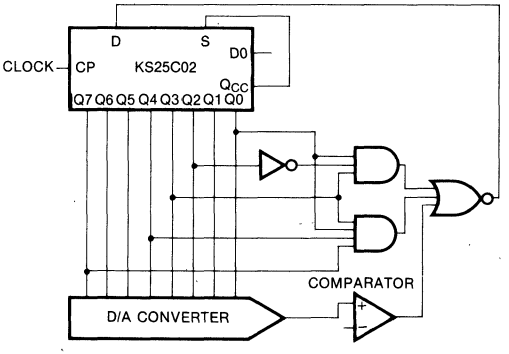
$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7(11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the S input.

TYPICAL APPLICATIONS

BCD ILLEGAL CODE SUPPRESSION

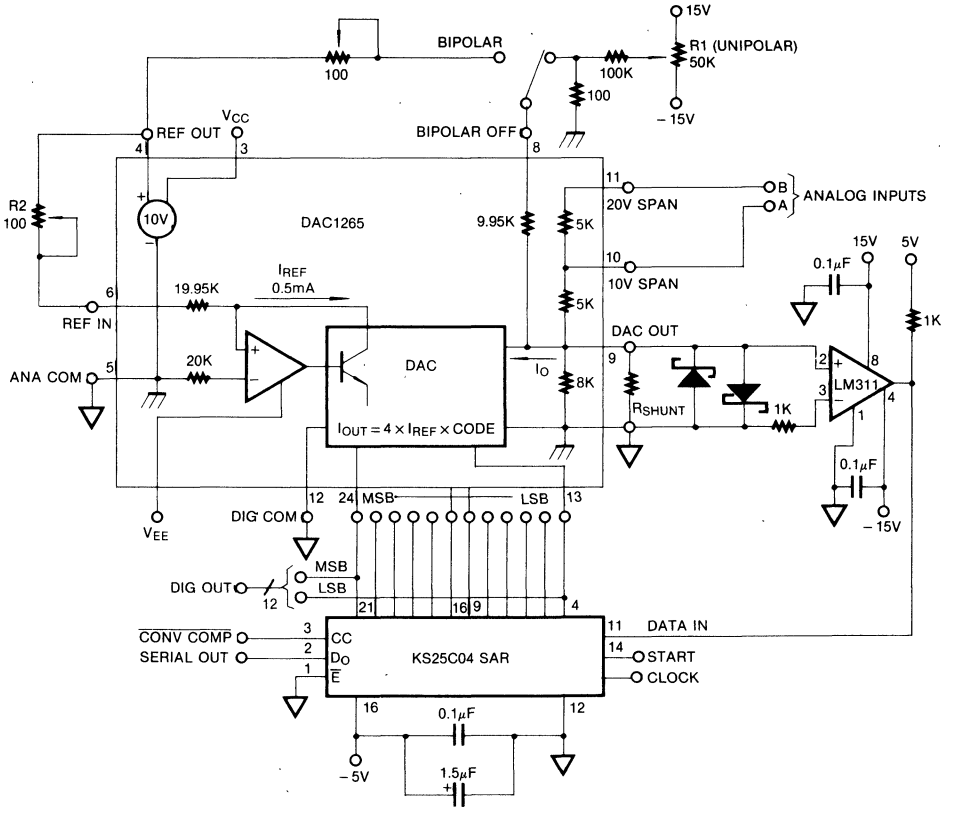


ACTIVE HIGH



ACTIVE LOW

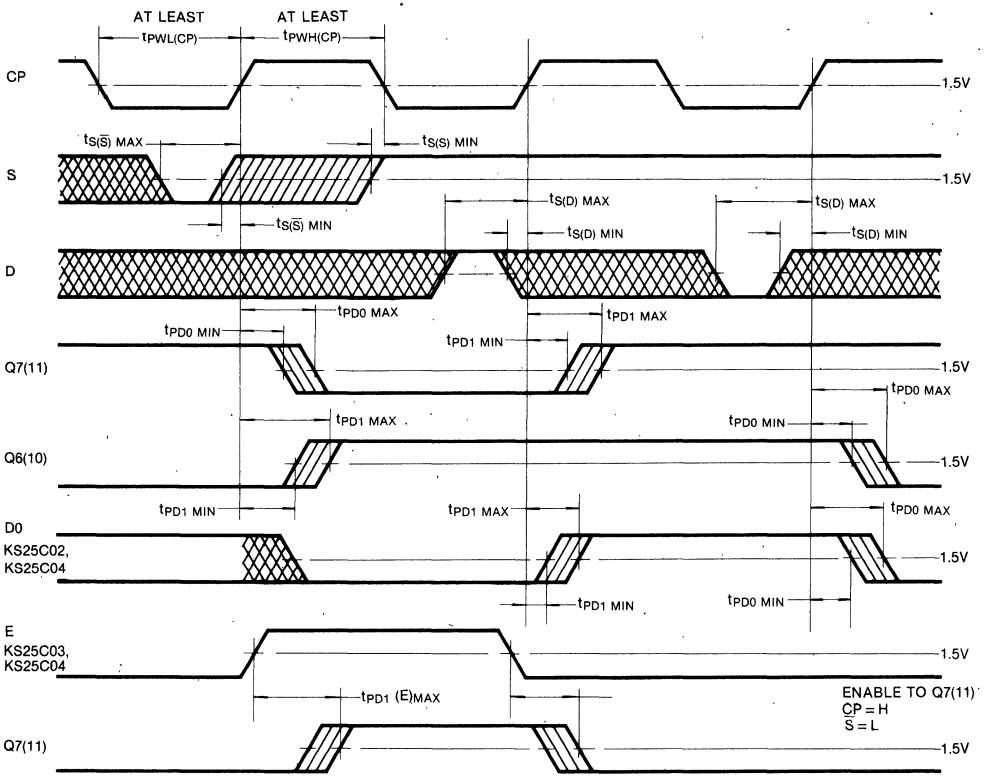
FAST PRECISION A/D CONVERTER



INPUT RANGES

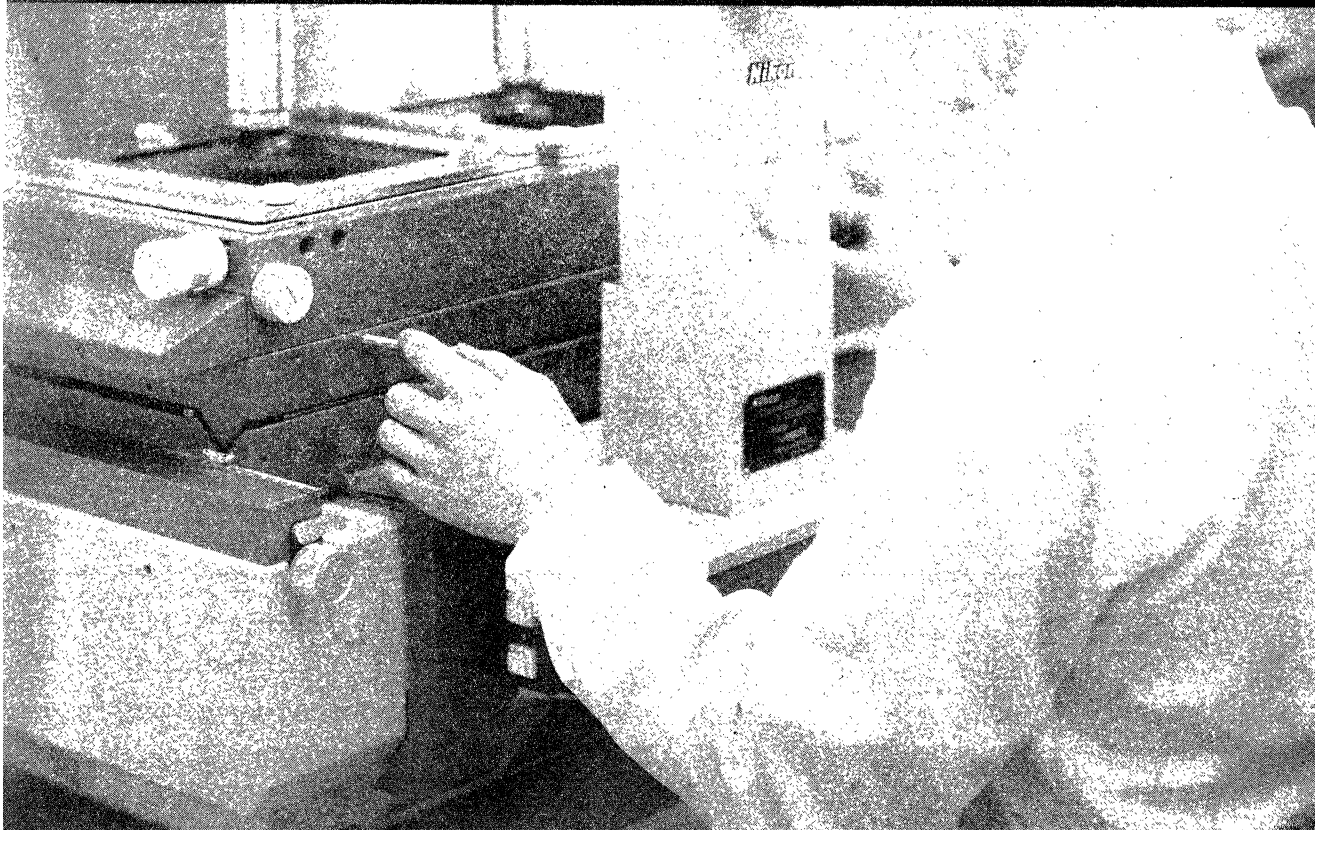
UNIPOLAR	BIPOLAR	CONNECT	EQUIV. DAC Z_{OUT}
0 to 10	±5	Input to A	2.36KΩ
0 to 5	±2.5	Input to A	1.90KΩ
0 to 20	±10	Input to B B to DAC OUT	3.08KΩ

SWITCHING TIME WAVEFORMS



WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care: any change permitted	Changing: state unknown

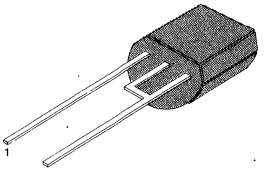
MISCELLANEOUS ICs 6



SILICON MONOLITHIC BIPOLAR INTEGRATED CIRCUIT VOLTAGE STABILIZAER FOR ELECTRONIC TUNER

The KA33V is a monolithic integrated voltage stabilizer especially designed as voltage supplier for electronic tuners.

TO-92



1: Anode 2: Cathode

FEATURES

- **Low Temperature Coefficient**
- **Low Dynamic Resistance**
- **Typical Reference Voltage of 33V**

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

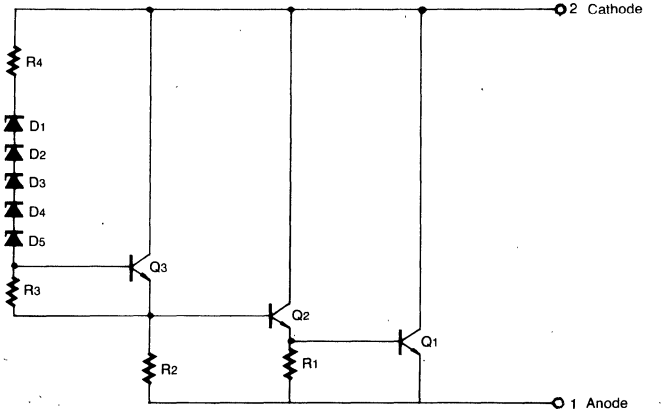
Characteristic	Symbol	Value	Unit
Zener Current	I_Z	10	mA
Power Dissipation (T_a =75°C)	P_D	200	mW
Operating Ambient Temperature-Range	T_{opr}	−20 ~ 75	°C
Storage Temperature Range	T_{stg}	−40 ~ 125	°C

6

ELECTRICAL CHARACTERISTICS (T_a =25°C)

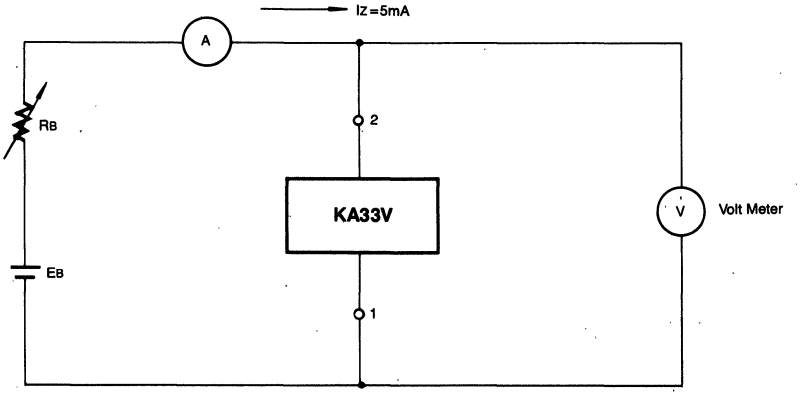
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Stabilized Voltage	V_Z	I_Z=5mA	31		35	V
Stabilized Voltage-Temperature Drift	$\triangle V_Z/\triangle T$	I_Z=5mA T_a=−20 to 75°C	−1	0	1	mV/°C
Dynamic Resistance	r_Z	I_Z=5mA, f=1KHz		10	25	

SCHEMATIC DIAGRAM

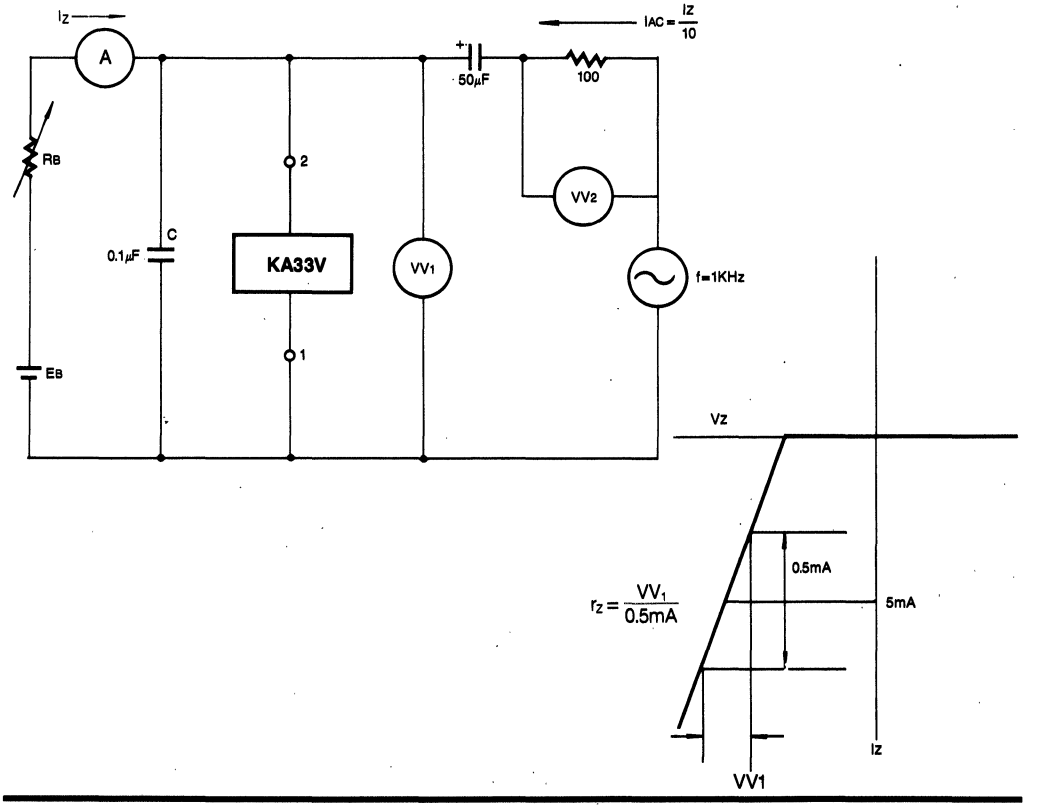


MEASURING CIRCUITS

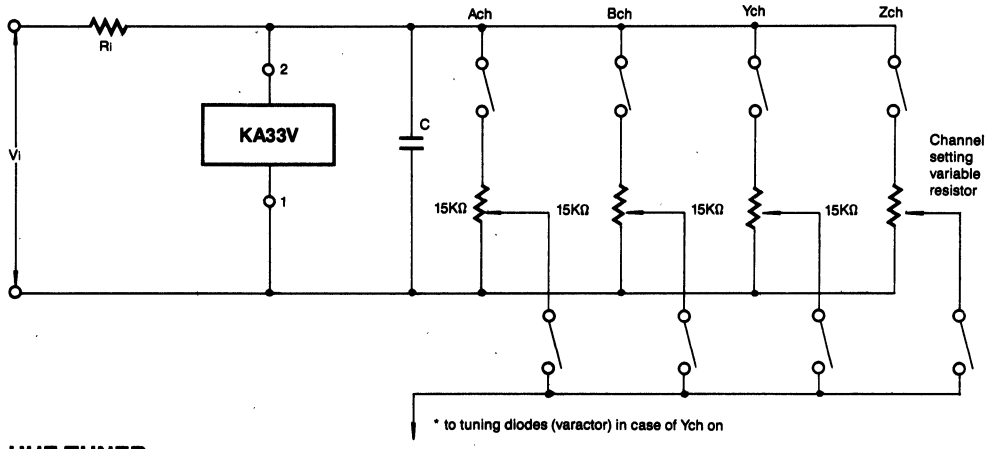
Measuring Circuit for Stabilized Voltage V_Z



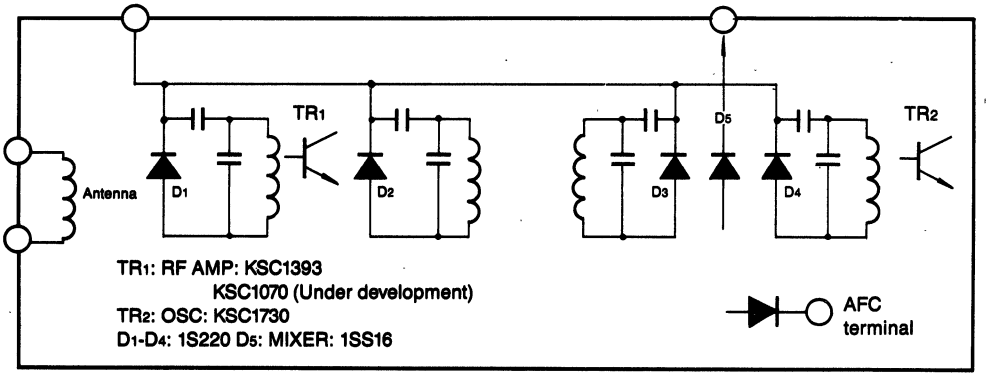
Measuring Circuit for Dynamic Resistance



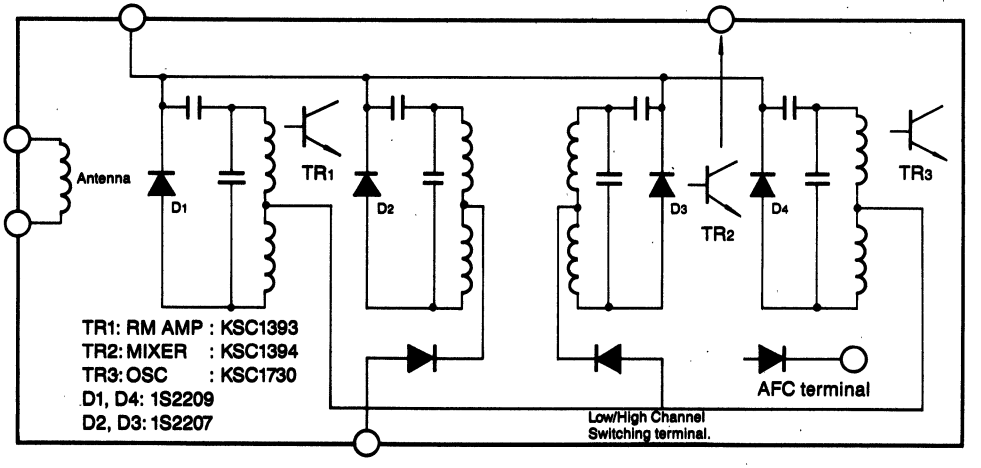
TYPICAL APPLICATION



(1) UHF TUNER

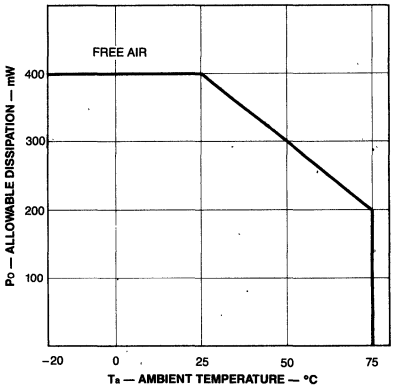


(2) VHF TUNER



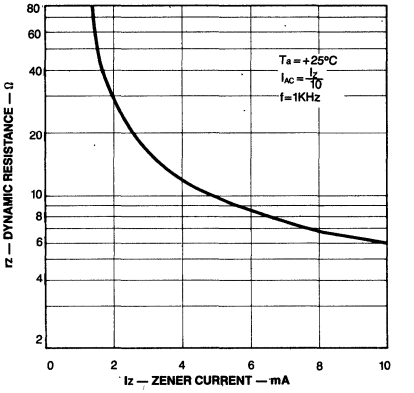
POWER-TEMPERATURE DERATING CURVE

ALLOWABLE DISSIPATION vs. AMBIENT TEMPERATURE

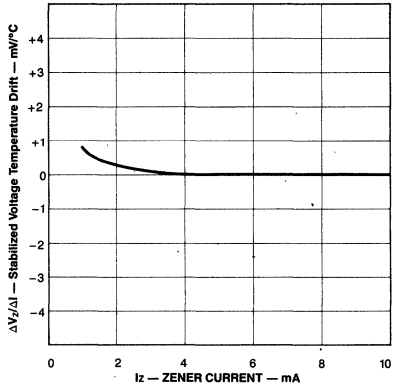


TYPICAL CHARACTERISTIC CURVES (T_a=25°C)

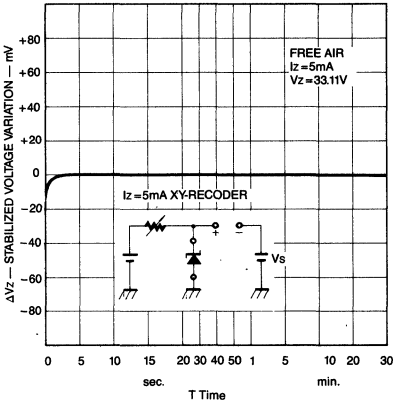
DYNAMIC RESISTANCE vs. ZENER CURRENT



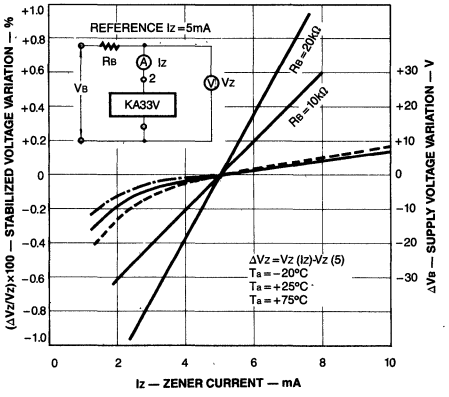
STABILIZED VOLTAGE TEMPERATURE DRIFT vs. ZENER CURRENT



STABILIZED VOLTAGE VARIATION vs. TIME



STABILIZED VOLTAGE VARIATION & SUPPLY VOLTAGE VARIATION vs. ZENER CURRENT



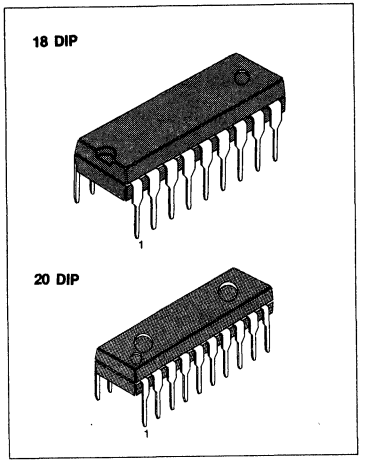
8-CHANNEL SOURCE DRIVERS

These integrated circuits, rated for operation with output voltages of up to 50V and designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic-and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

KA2580A is a high current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

KA2588A is a high-current source driver similar to KA2580A, has separated logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, MOS) or negative logic (NMOS) and either negative or split-load supplies.

KA2580A is furnished in 18-pin dual in-line plastic package; KA2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.

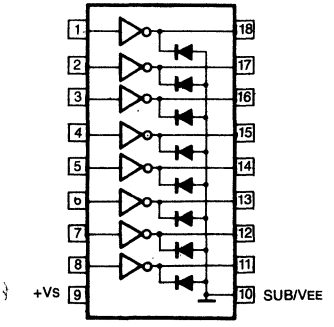


FEATURES

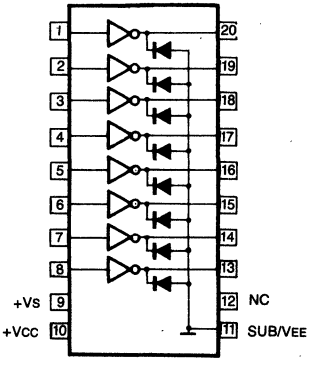
- **TTL, CMOS, PMOS, NMOS Compatible**
- **High Output Current Ratings**
- **Internal Transient Suppression**
- **Efficient Input/Output Pin Structure**

6

SCHEMATIC DIAGRAM



KA2580A



KA2588A

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C, for Any One Driver unless otherwise noted)

Characteristic	Symbol	Value	Unit
Output Voltage	V_{CE}	50	V
Supply Voltage (ref, sub)	V_S	50	V
Supply Voltage (ref, sub, KA2588A)	V_{CC}	50	V
Input Voltage (ref, Vs)	V_{IN}	−30	V
Total Current	$I_{CC}+I_S$	−500	mA
Substrate Current	I_{SUB}	3.0	A
Power Dissipation (single output)	Pd	1.0	W
(total Package)*		2.2	W
Operating Temperature	T_a	−20 ~ +85	°C
Storage Temperature	Tstg	−65 ~ +150	°C

* Derate at the rate of 18mW/°C above 25°C

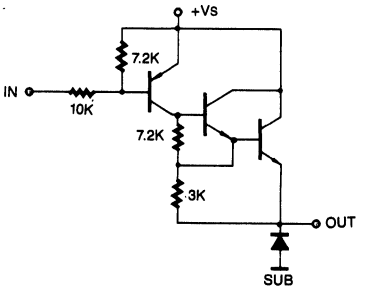
TYPICAL OPERATING VOLTAGE

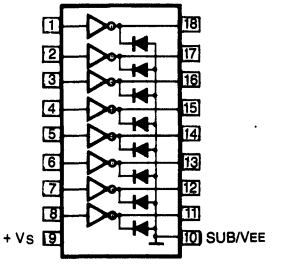
V_S	V_{IN} (on)	V_{IN} (off)	V_{CC}	V_{CC} (max)	DVC Type
0V	−15V ~ −3.6V	−0.5V ~ 0V	NA	−50V	KA2580A
+5V	0V ~ +1.4V	+4.5V ~ +5V	NA ≤5V	−45V −45V	KA2580A KA2588A
+12V	0V ~ +8.4V	+11.5V ~ +12V	NA ≤12V	−38V −38V	KA2580A KA2588A
+15V	0V ~ +11.4V	+14.5V ~ +15V	NA ≤15V	−35V −35V	KA2580A KA2588A

Notes

1) For simplication, these devices are characterized to the above with specific voltages for inputs, logic supply (V_s), load supply (V_{EE}), and collector supply (V_{CC}).
2) Typical use of the KA2580A is with negative referenced logic. The more common application of the KA2588A is with positive referenced logic supplies.
3) In application, the devices are capable of operation over a wide range of logic and supply voltage levels.
4) The substrate must be tied to the most negative point in the external circuit to maintain isolation drivers and to provide for normal circuit operation.

PARTIAL SCHEMATIC (KA2580A)





ELECTRICAL CHARACTERISTICS (KA2580A)

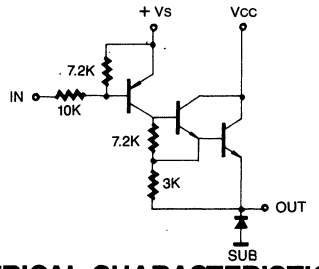
(T_a=25°C, V_S=0V, V_{EE}=−45V unless otherwise noted)

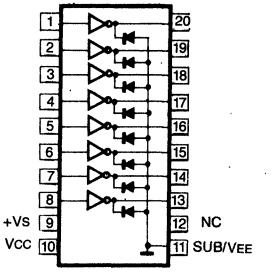
Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	V_{in}=−0.5V, V_{OUT}=V_{EE}=−50V		50	μA
		V_{IN}= −0.4V, V_{OUT}=V_{EE}= −50V T_a=70°C		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	V_{IN}=−0.4V, I_{OUT}=−25mA	35		V
Output Saturation Voltage	V_{CE} (sat)	V_{IN}=−2.4V, I_{OUT}=−100mA		1.8	V
		V_{IN}=−3.0V, I_{OUT}=−225mA		1.9	V
		V_{IN}=−3.6V, I_{OUT}=−350mA		2.0	V
Input Current	I_{IN} (on)	V_{IN}=−3.6V, I_{OUT}=−350mA		−500	μA
		V_{IN}=−15V, I_{OUT}=−350mA		−2.1	mA
	I_{IN} (off)	I_{OUT}= −500μA, T_a=70°C (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	I_{OUT}=−100mA, V_{CE}≤1.8V		−2.4	V
		I_{OUT}=−225mA, V_{CE}≤1.9V		−3.0	V
		I_{OUT}=−350mA, V_{CE}≤2.0V		−3.6	V
	V_{IN} (off)	I_{OUT}=−500μA, T_a=70°C	−0.2		V
Clamp Diode Leakage Current	I_R	V_R=50V, T_a=70°C		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS

Notes

1) Pulsed test, tp≤300uS, duty cycle≤2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.

PARTIAL SCHEMATIC (KA2588A)





ELECTRICAL CHARACTERISTICS (KA2588A)

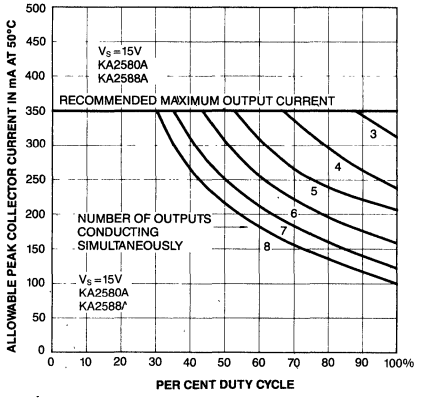
(T_a = 25°C, V_S = V_{CC} = 5.0V, V_{EE} = −40V unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5V$, $V_{OUT} = V_{EE} = -45V$		50	μA
		$V_{IN} \geq 4.6V$, $V_{OUT} = V_{EE} = -45V$ $T_a = 70°C$		100	μA
Output Sustaining Voltage (Note 1, 2)	V_{CE} (sus)	$V_{IN} \geq 4.6V$, $I_{OUT} = -25mA$	35		V
Output Saturation Voltage	V_{CE} (sat)	$V_{IN} = 2.6V$, $I_{OUT} = -100mA$ Ref. V_{CC}		1.8	V
		$V_{IN} = 2.0V$, $I_{OUT} = -225mA$ Ref. V_{CC}		1.9	V
		$V_{IN} = 1.4V$, $I_{OUT} = -350mA$ Ref. V_{CC}		2.0	V
Input Current	I_{IN} (on)	$V_{IN} = 1.4V$, $I_{OUT} = -350mA$		−500	μA
		$V_S = 15V$, $V_{EE} = -30V$, $V_{IN} = 0V$, $I_{OUT} = -350mA$		−2.1	mA
	I_{IN} (off)	$I_{OUT} = -500\mu A$, $T_a = 70°C$ (Note 3)	−50		μA
Input Voltage (Note 4)	V_{IN} (on)	$I_{OUT} = -100mA$, $V_{CE} \leq 1.8V$		2.6	V
		$I_{OUT} = -225mA$, $V_{CE} \leq 1.9V$		2.0	V
		$I_{OUT} = -350mA$, $V_{CE} \leq 2.0V$		1.4	V
	V_{IN} (off)	$I_{OUT} = -500\mu A$, $T_A = 70°C$	4.8		V
Clamp Diode Leakage Current	I_R	$V_R = 50V$, $T_a = 70°C$		50	μA
Clamp Diode Forward Voltage	Vf	If=350mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn-On Delay	t_{PHL}	0.5 V_{IN} to 0.5 Vout		5.0	μS
Turn-Off Delay	t_{PLH}	0.5 V_{IN} to 0.5 Vout		5.0	μS

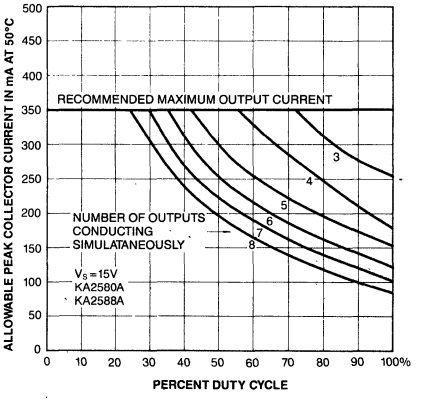
Notes

1) Pulsed test, tp ≤ 300uS, duty cycle ≤ 2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.
6) V_{CC} must never be more positive than V_S.

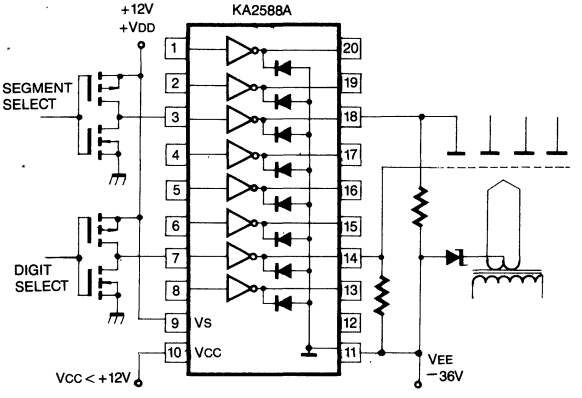
ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE



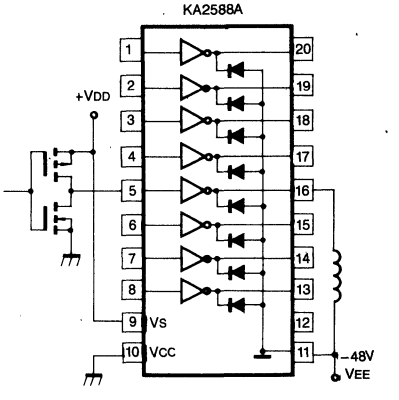
ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE



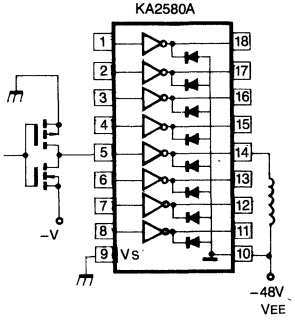
TYPICAL APPLICATIONS



Vacuum Fluorescent Display Driver (Split Supply)



Telecommunicaiton Relay Driver (Positive Logic)

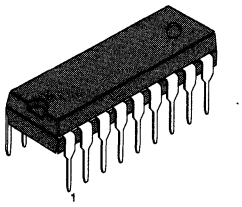


Telecommunication Relay Driver (Negative Logic)

FLUORESCENT DISPLAY DRIVERS

Consisting of eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. KA2651 is capable of driving the digits and/or segments of these displays and is designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications.

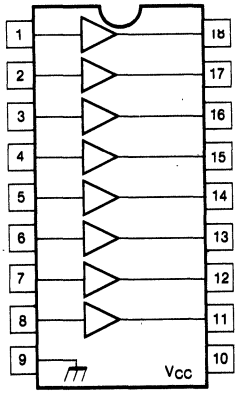
18 DIP



FEATURES

- **Digit or Segment Drivers**
- **Low Input Current**
- **Internal Output Pull-Down Resistors**
- **High Output Breakdown Voltage**
- **Single or Split Supply Operation**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C, Voltage are with reference to ground unless otherwise noted)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	65	V
Input Voltage	V_{IN}	20	V
Output Current	I_{Out}	−40	mA
Operating Temperature	Ta	−20 +85	°C
Storage Temperature	T_{stg}	−55 +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	5.0 ~ 50	V
Input ON Voltage	V_{IN}	2.4 ~ 15	V
Output ON Current*	I_{outON}	−25	mA

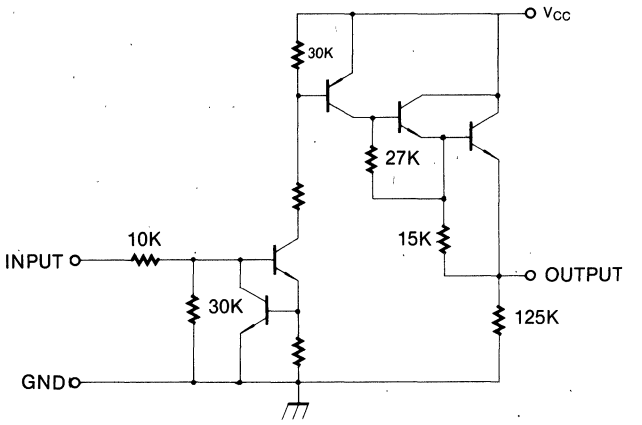
* Positive (negative) current is defined as going into (coming out of) the specified device pin.

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 60V, V_{EE} = 0V unless otherwise noted.)

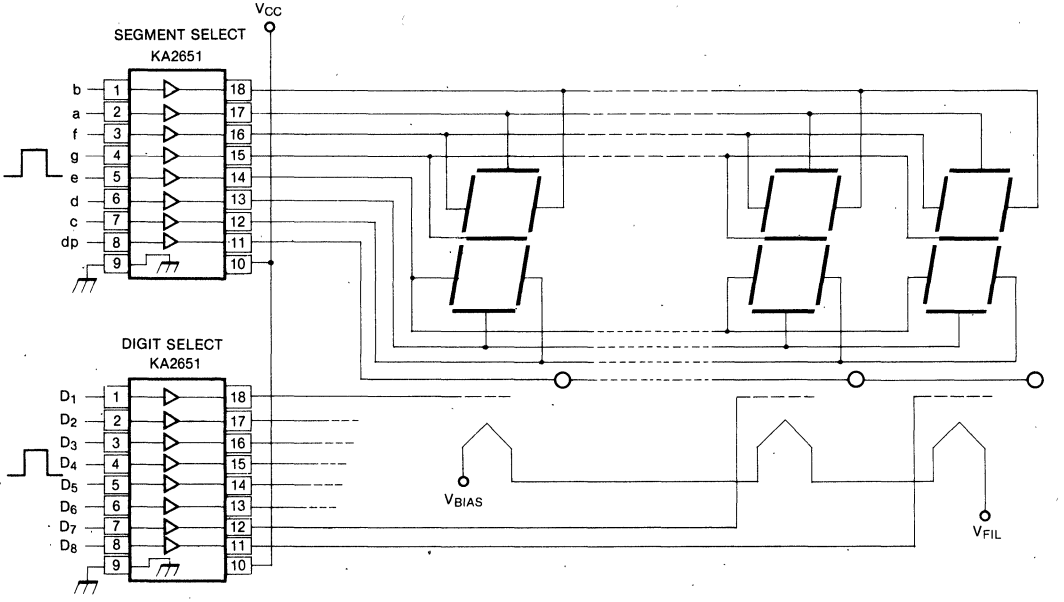
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Leakage Current	I_{OUTLK}	V_{IN} = 0.4V			15	μA
Output OFF Voltage	V_{OUTOFF}	V_{IN} = 0.4V			1.0	V
Output Pull-Down Current	I_{OUTPD}	Input Open, $V_{OUT} = V_{CC}$	350	500	775	μ
Output ON Voltage	V_{OUTON}	V_{IN} = 2.4V I_{OUT} = −25mA	57	58		V
Input ON Current	I_{IN}	V_{IN} = 2.4V		120	225	μA
		V_{IN} = 5.0V		375	650	μA
Supply Current	I_{CC}	All Inputs Open		10	100	μA
		All Inputs = 2.4V		5.5	8.0	mA

PARTIAL SCHEMATIC



(One Driver)

TYPICAL MULTIPLEXED FLUORESCENT DISPLAY

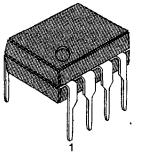


LOW POWER CONSUMPTION EARTH LEAKAGE DETECTOR

The KA2803 is designed for use in earth leakage circuit interrupters, for operation directly off the AC line in breakers. The input of the differential amplifier is connected to the secondary coil of ZCT (Zero Current Transformer). The amplified output of differential amplifier is integrated at external capacitor to gain adequate time delay that is specified in KSC4613.

The level comparator generates high level when earth leakage current is greater than some level.

8 DIP



FUNCTIONS

- Differential amplifier
- Level camparator
- Latch circuit

FEATURES

- **Low power consumption (P_d=5mW, 100V/200V)**
- **Built-in voltage regulator**
- **High gain differential amplifier (V_T=13.5mV)**
- **1mA output current pulse to trigger SCR'S**
- **Low external part count, economic**
- **Mini-dip package (8 Dip), high packing density**
- **High noise immunity, large surge margin**
- **Super temperature characteristic of input sensitivity**
- **Wide operating temperature range (T_a=−25°C ~ +80°C)**

APPLICATION CIRCUIT

1. Full Wave Application Circuit

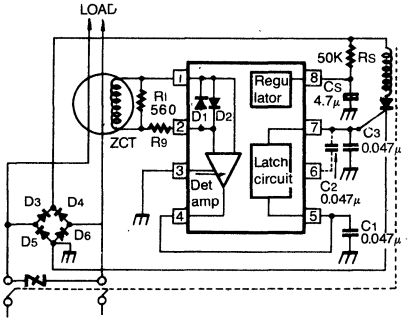


Fig. 1

2. Half Wave Application Circuit

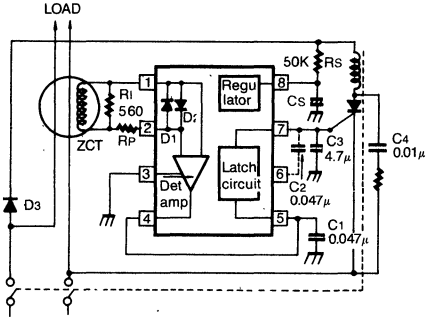


Fig. 2

ABSOLUTE MAXIMUM RATINGS (T_a =25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	20	V
Supply Current	I_S	8	mA
Power Dissipation	P_D	300	mW
Lead Temperature (soldering 10 sec)	T_{lead}	260	°C
Operating Temperature	T_{opr}	−25 ~ +80	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS (T_a =25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current 1	I_{S1}	V_{CC} =12V (−25°C) V_R-V_I =300mV (25°C) (80°C)		400	580 530 480	μA μA μA
Trip Voltage		V_{CC} =16V (−25°C ~ 80°C) V_R-V_I =X	10	13.5	17	mVrms
Differential Amplifier Output Current 1	I_{TDI}	V_{CC} =16V (25°C) V_R-V_I =30mV V_{OD} =1.2V	12		30	μA
Differential Amplifier Output Current 2	I_{TD2}	V_{CC} =16V (25°C) V_{OD} =0.6V V_R, V_1 short	17		37	μA
Output Current	I_O	V_{SC} = 1.4V V_{OS} =0.8V V_{CC} = 12V (−25°C) (+25°C) (+80°C)	 −200 −100 −75			 μA μA μA
Latch on Voltage	V_{scon}	V_{CC} = 16V (25°C)	0.7		1.4	V
Latch Input Current	I_{scon}	V_{CC} =12V (25°C)			5	μA
Output Low Current	I_{OSL}	V_{CC} =12V (−25 ~ 80°C) V_{OSL} =0.2V	200			μA
Diff. Input Clamp Voltage	V_{IDC}	I_{IDC} =100mA (−25 ~ 80°C)	0.4		2	V
Maximum Current Voltage	V_{SM}	I_{SM} =7mA (−25°C)	20		28	V
Supply Current 2	I_{S2}	V_R-V_I =X (25 ~ 80°C) V_{OS} =0.6			900	μA
Latch Off Supply Voltage	V_{soff}	V_{os} =high (25°C)	7.0			V
Response Time	T_{on}	V_{CC} =16V (25°C) V_R-V_I =0.3V	2		4	msec

APPLICATION NOTE

(refer to full wave application circuit Fig. 1)

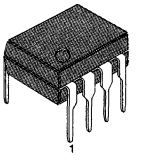
The Fig 1 shows the KA2803 connected in a typical leakage current detector system.
The power is applied to the V_{CC} terminal (Pin 8) of the KA2803 directly from the power line.
The resistor R_S and capacitor C_S are chosen so that pin 8 voltage is at least 12V.
The value of C_S is recommended above 1μF at this time.
If the leakage current is at the load, it is detected by the zero current transformer (ZCT).
The output voltage signal of ZCT is amplified by the differential amplifier of the KA2803 internal circuit and appears as half-cycle sine wave signal referred to input signal at the output of the amplifier.
The amplifier closed loop gain is fixed about 1000 times with internal feedback resistor to compensate for zero current transformer (ZCT) Variations.
The resistor R_L should be selected so that the breaker satisfies the required sensing current.
The protection resistor R_P is not usually used put when the high current is injected at the breaker, this resistor should be used to protect the earth leakage detector IC the KA2803.
The range of R_P is from several hundred Ω to several kΩ.
The capacitor C_1 is for the noise canceller and standard value of C_1 is 0.047μF. Also the capacitor C_2 is noise canceller capacitance but it is not usually used.
When high noise is only appeared at this system 0.047μF capacitor may be connected between pin 6 and pin 7.
The amplified signal is finally appeared to the Pin 7 with pulse signal through the internal latch circuit of the KA2803.
This signal drivies the gate of the external SCR which energizes the trip coil which opens the circuit breaker.
The trip time of breaker is decided by the capacitor C_3 and the mechanism breaker.
This capacitor should be selected under 1μF for the required the trip time.
The full wave bridge supplies power to the KA2803 during both the positive and negative half-cycles of the line voltage.
This allows the hot and neutral lines to be interchanged.
If your application want the detail information, request it on our application circuit designer of KA2803.

ZERO VOLTAGE SWITCH

The KA2804 is a TRIAC controller providing a complete solution for temperature controlled electric panel heaters, cookers, film processing baths etc.

Switching occurs at the zero voltage point in order to minimize radio frequency interference. The device is suitable for mains-on-line operation and requires minimal components.

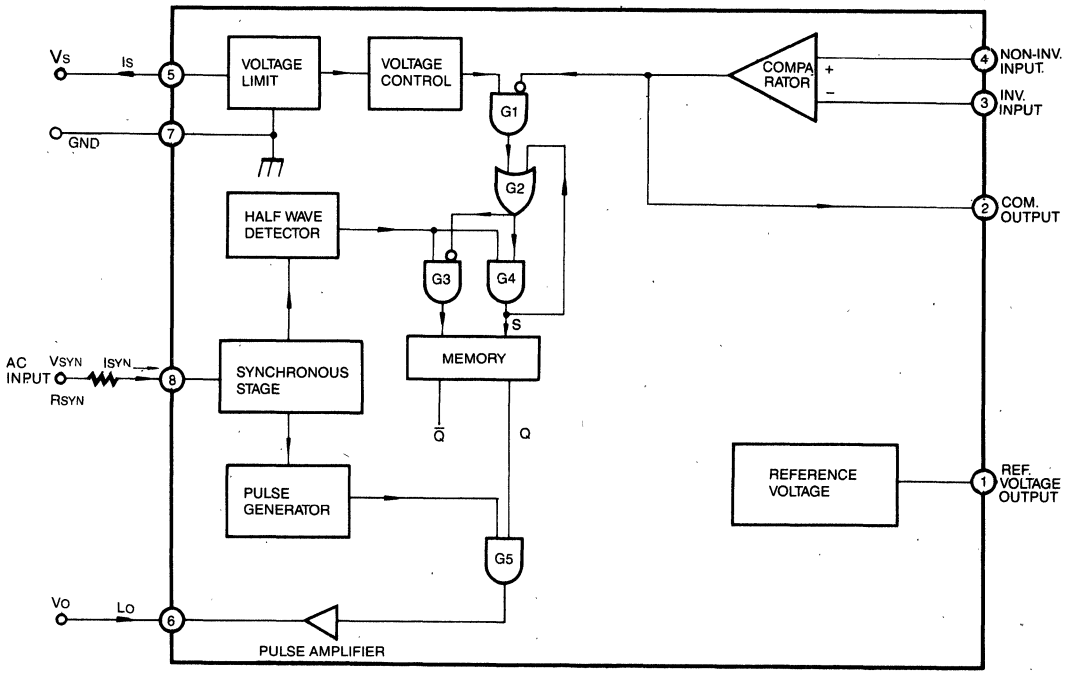
8 DIP



FEATURES

- **Easy operation either through the AC line or a DC supply.**
- **Supply voltage control.**
- **Very few external components.**
- **Symmetrical burst control — No DC current components in the load circuit.**
- **Negative output current pulse up to 250mA-short circuit protection.**
- **Reference voltage output.**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	$-V_S$	8.2	V
Supply Current	$-I_S$	40 (average)	mA
Synchronous Current	I_{SYN}	5.0 (rms)	mA
Input Voltage	V_I	$\leqq \lvert V_S \rvert$	V
Power Dissipation	P_D	350	mW
Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_{opr}	−20 ~ +70	°C
Storage Temperature	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

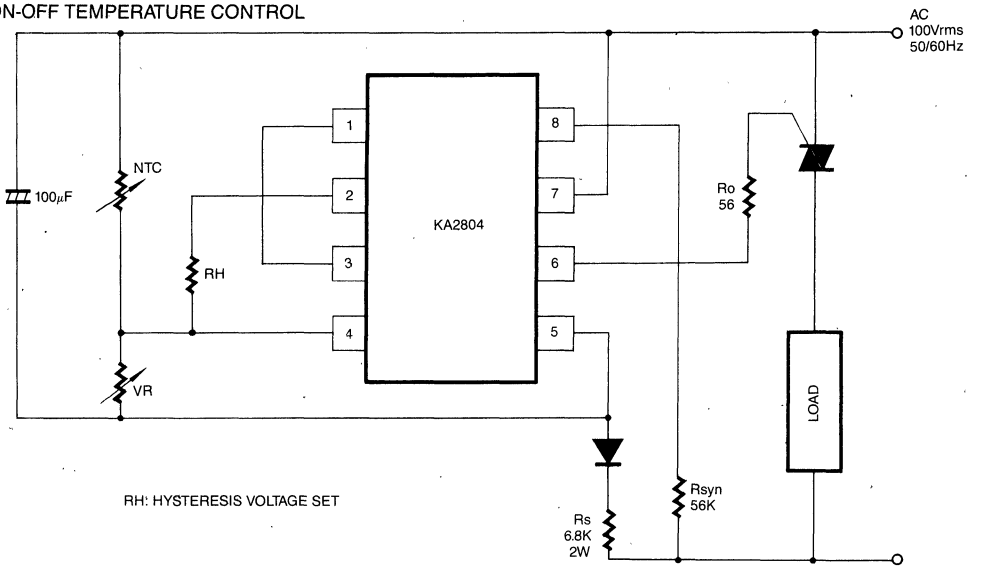
(V_S = 8.0V, V_{SYN} = 100 to 115V_{rms}, T_a = 25°C, f = 50/60Hz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Circuit Current	$-I_S$	Pin 5, R_{SYN} = 56K	—	2.0	2.5	mA
Supply Voltage 1	$-V_S$ 1	Pin 5, I_S = 2.5mA R_{SYN} = 56K	7.2	—	8.4	V
Supply Voltage 2	$-V_S$ 2	Pin 5, I_S = 20mA R_{SYN} = 56K	7.2	—	8.6	V
Synchronous Current	I_{SYN}	Pin 8	0.3	—	—	mA
Output Pulse Width	T_P	Pin 6, R_{SYN} = 56K	—	200	—	μS
Output Voltage	V_O	Pin 6, $I_O \leqq$ 200mA	4.2	5.2	—	V
Output Current	I_O	Pin 6, $R_O \leqq$ 25	200	250	—	mA
Output Leakage Current	I_{LO}	Pin 6	—	—	2.0	μA
Input Offset Voltage	V_{IO}	Pin 3, 4	—	2.0	5.0	mV
Input Bias Current	I_I	Pin 3, 4	—	0.5	1.0	μA
Common Mode Input Voltage Range	$-V_{ICM}$	Pin 3, 4	0	—	5.7	V
Output Leakage Current	I_{LC}	Pin 2	—	—	0.2	μA
Reference Voltage	$-V_R$	Pin 1, $I_R \leqq$ 1uA	—	3.6	—	V

6

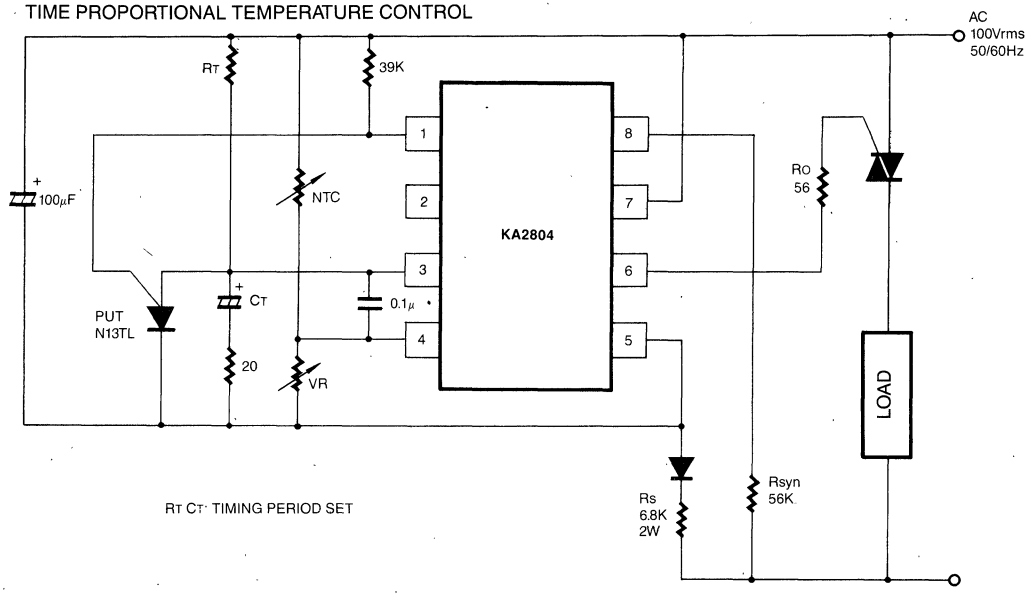
APPLICATIONS

ON-OFF TEMPERATURE CONTROL



RH: HYSTERESIS VOLTAGE SET

TIME PROPORTIONAL TEMPERATURE CONTROL

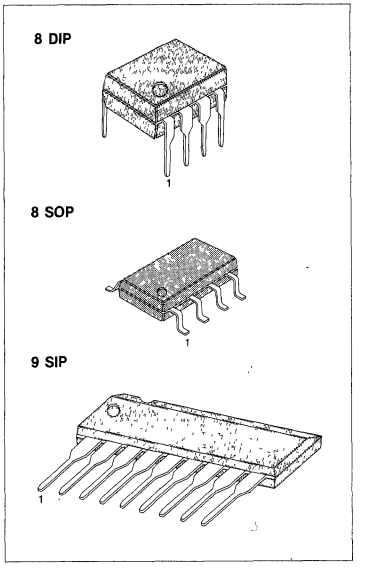


RT CT: TIMING PERIOD SET

LOW VOLTAGE AUDIO POWER AMPLIFIER

The LM386/S/D is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 30 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.



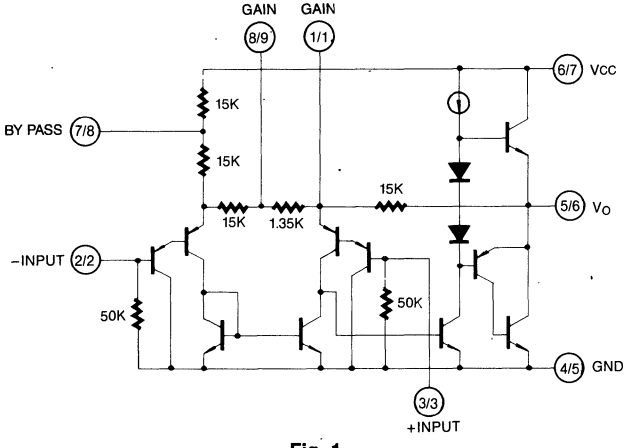
FEATURES

- **Battery operation.**
- **Minimum external parts.**
- **Wide supply voltage range: 4V ~ 12V (LM386)**
  4V ~ 9V (LM386S/D)
- **Low quiescent current drain (4mA.)**
- **Voltage gains : 20 ~ 200.**
- **Ground referenced input.**
- **Self-centering output quiescent voltage.**
- **Low distortion.**
- **3 kinds of package types**
  LM386 (8 Dip), LM386S (9 Sip), LM386D (8 Sop)

ORDERING INFORMATION

Device	Package	Operating Temperature
LM386N	8 DIP	– 20°C ~ + 70°C
LM386S	9 SIP	
LM386D	8 SOP	

SCHEMATIC DIAGRAMS



⊘ : LEFT (LM386/D)
RIGHT (LM386S)

Fig. 1

CONNECTION DIAGRAM

(LM386/D)

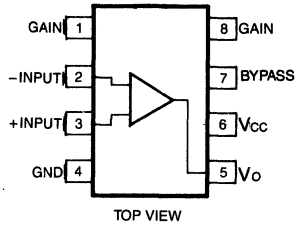


Fig. 2

(LM386S)

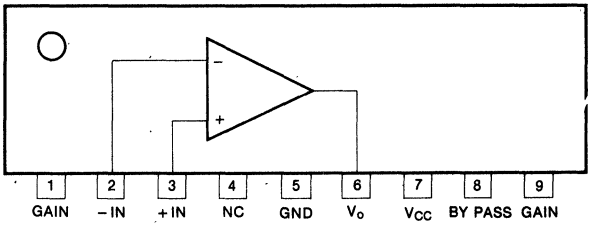


Fig. 3

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic		Symbol	Value	Unit
Supply Voltage		V_{CC}	15	V
Power Dissipation	LM386	P_d	660	mW
	LM386S		500	
	LM386D		300	
Input Voltage		V_i	±0.4	V
Operating Temperature		T_{opr}	−20 ~ +70	°C
Storage Temperature		T_{stg}	−40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(T_a = 25°C, V_{CC} = 6V, R_L = 8Ω, f = 1KHz, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescient Circuit Current	I_{CC}	V_i = 0		4	8	mA
Output Power	P_o	V_{CC} = 6V, THD = 10%	250	325		mW
		V_{CC} = 9V, THD = 10%	500	700		mW
Voltage Gain (D-Type)	A_V	Pins 1 and 8 Open		26		dB
		10μF from Pin 1 to 8		46		
Bandwidth (D-Type)	BW	Pins 1 and 8 Open		300		KHz
		10μF from Pin 1 to 8		60		
Total Harmonic Distortion (D-Type)	THD	P_o = 125mW, Pins 1 and 8 Open		0.2		%
Input Resistance	R_i			50		KΩ
Input Bias Current	I_b	Pins 1 and 8 Open		250		nA

TYPICAL APPLICATIONS (LM386/D)

Amplifier with Gain=50 (34 dB)

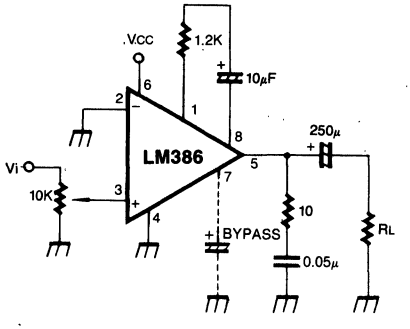


Fig. 4

Low Distortion Power Wienbridge Oscillator

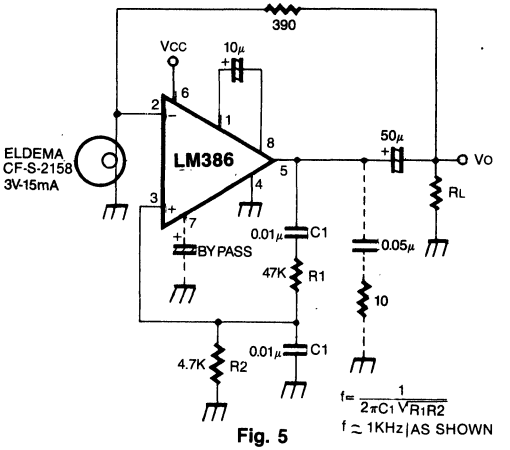


Fig. 5

Square Wave Oscillator

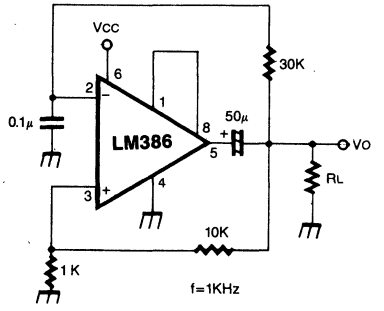


Fig. 6

Amplifier with Bass Boost

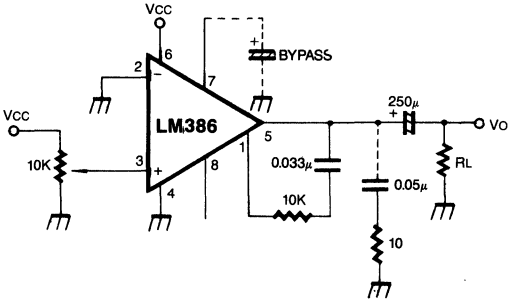


Fig. 7

AM Radio Power Amplifier

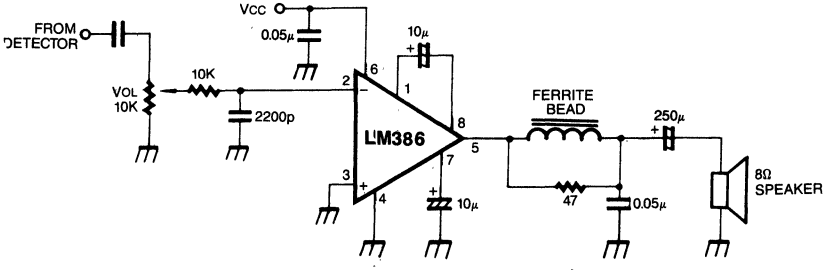
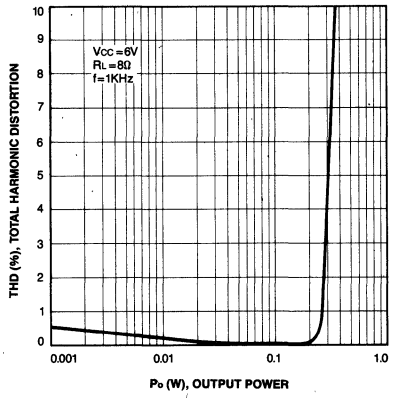
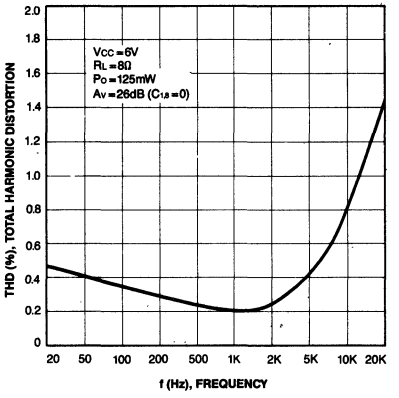


Fig. 8

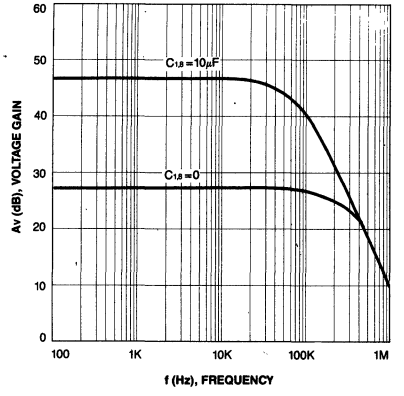
TOTAL HARMONIC DISTORTION-OUTPUT POWER



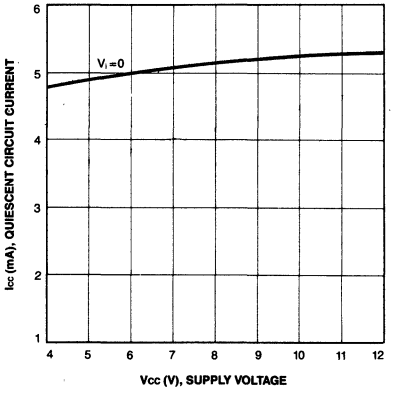
TOTAL HARMONIC DISTORTION-FREQUENCY



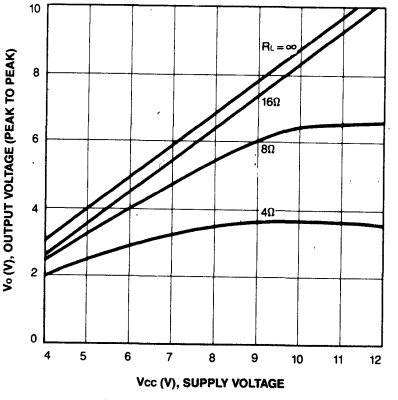
VOLTAGE GAIN—FREQUENCY



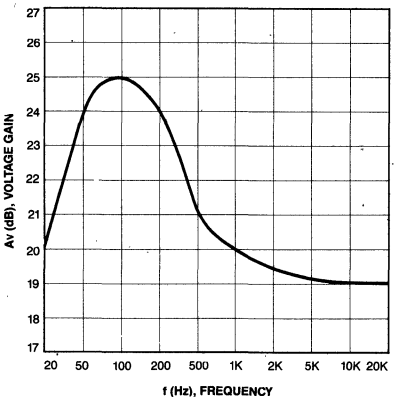
QUIESCENT CIRCUIT CURRENT-SUPPLY VOLTAGE

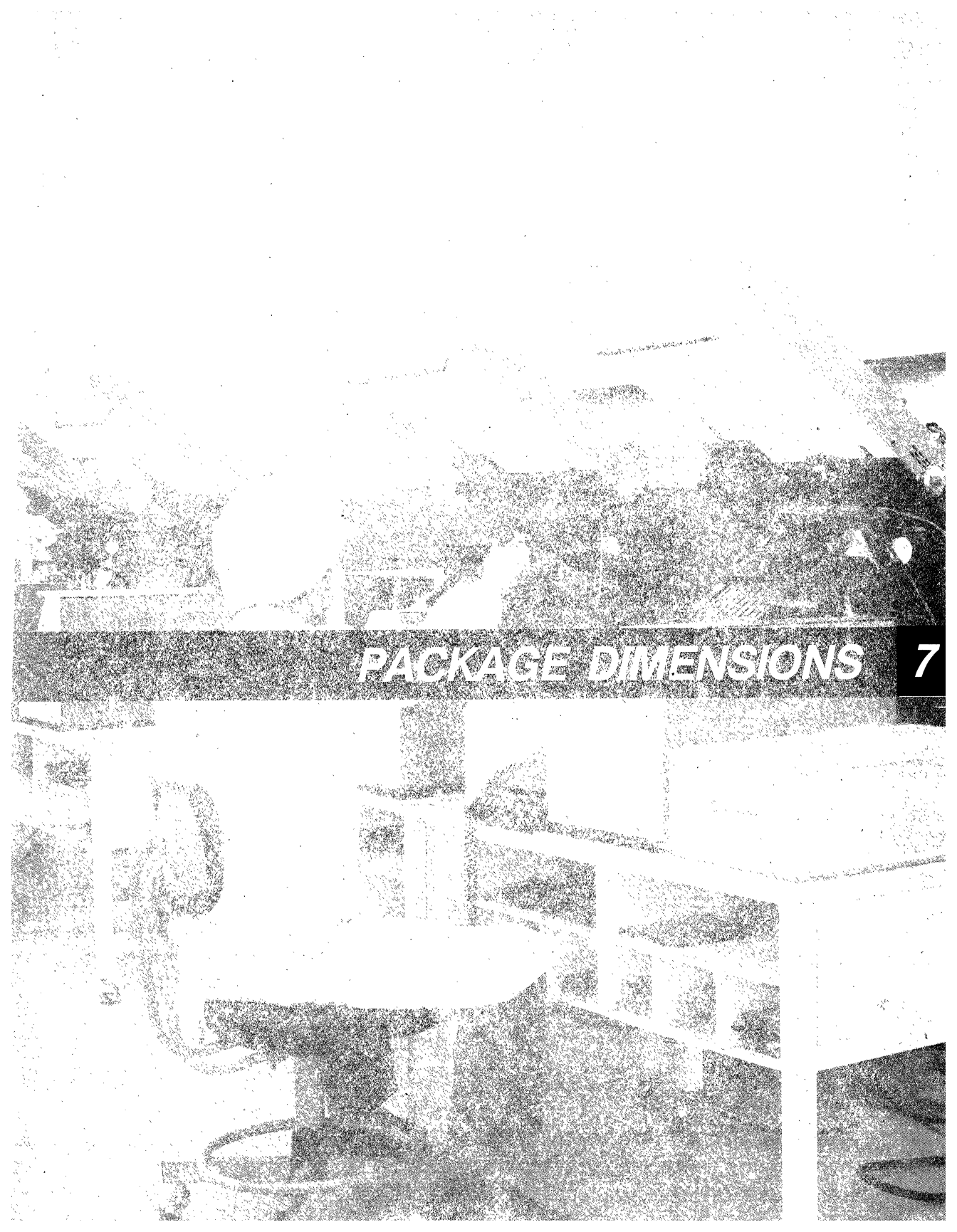


OUTPUT VOLTAGE SWING-SUPPLY VOLTAGE



FREQUENCY RESPONSE WITH BASS BOOST



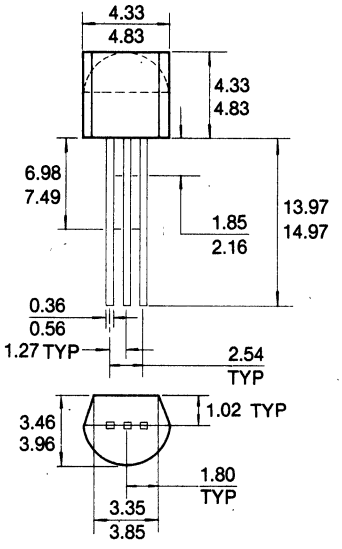


PACKAGE DIMENSIONS

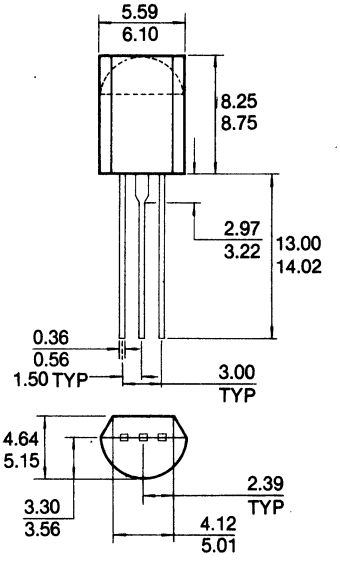
7

PACKAGE DIMENSIONS

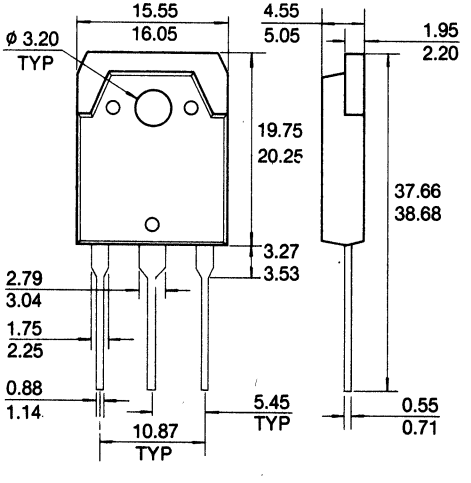
TO-92 Unit: mm



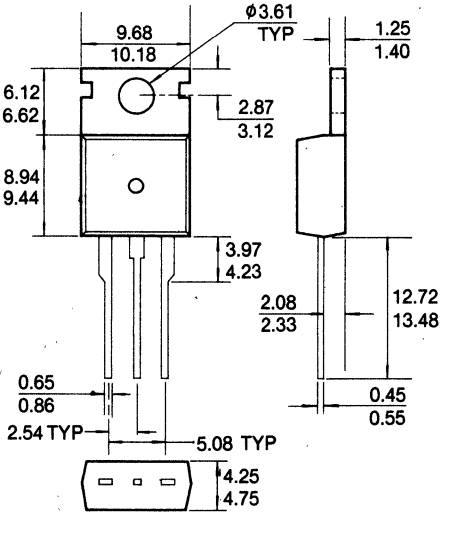
TO-92L Unit: mm



TO-3P Unit: mm



TO-220 Unit: mm

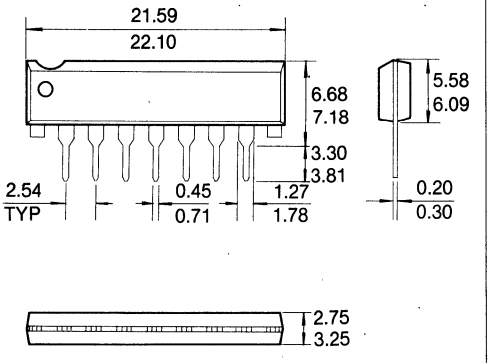


7

PACKAGE DIMENSIONS

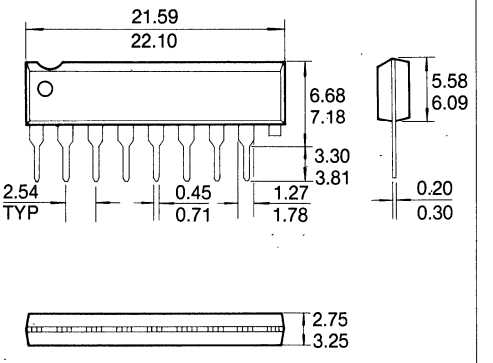
7 SIP

Unit: mm



8 SIP

Unit: mm



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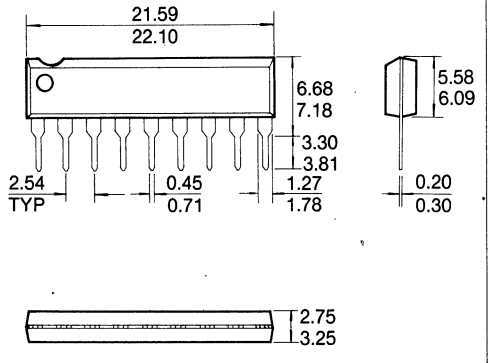
Unit: mm



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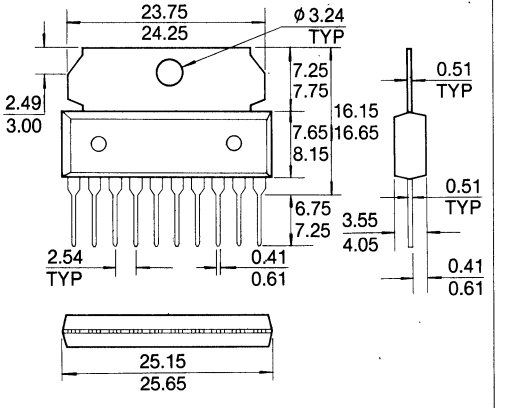
Unit: mm



PACKAGE DIMENSIONS

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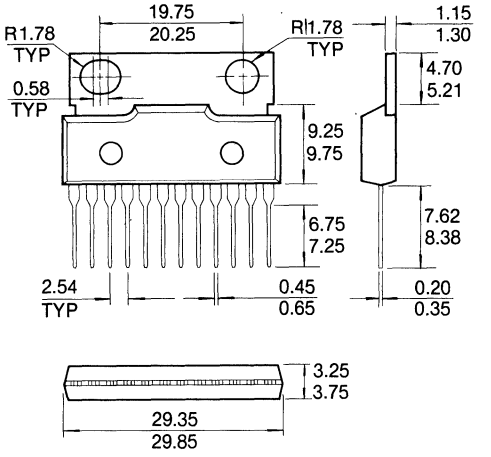
Unit: mm



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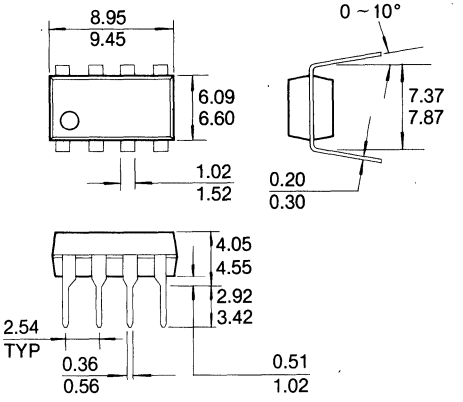

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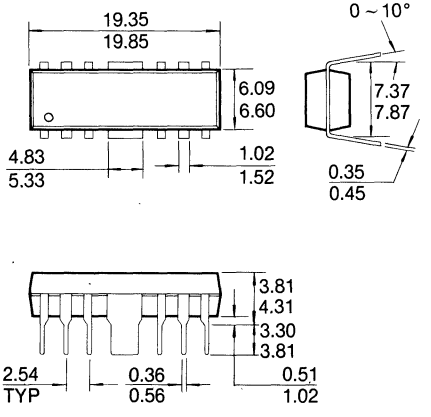

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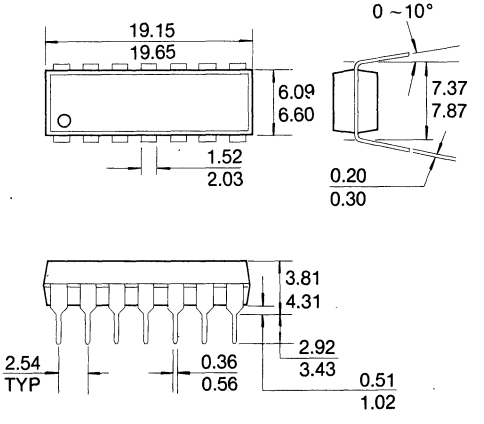
Unit: mm



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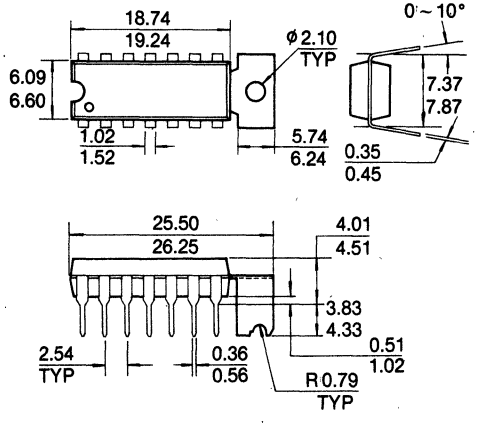
PACKAGE DIMENSIONS

14 DIP H/S

Unit: mm



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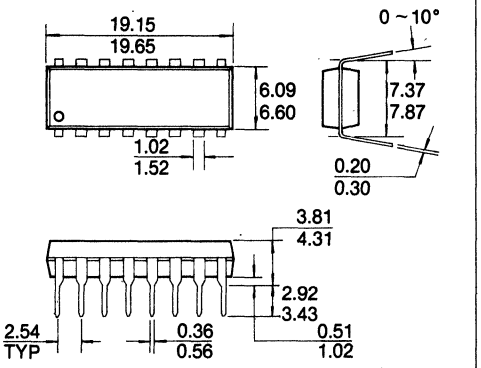

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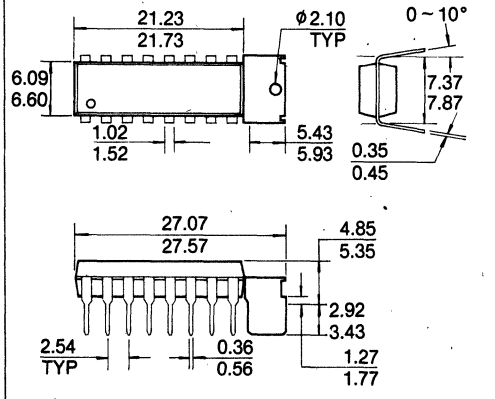

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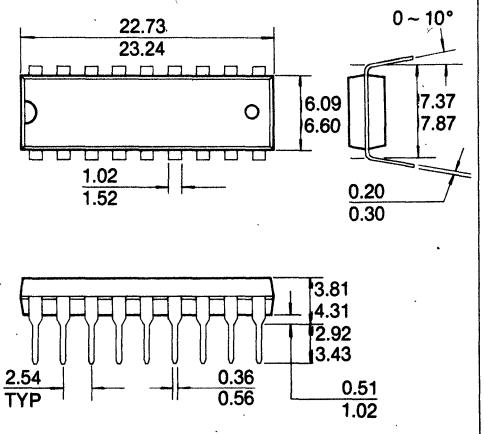

PACKAGE DIMENSIONS

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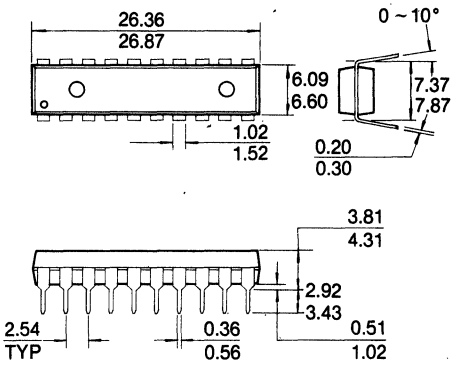
Unit: mm



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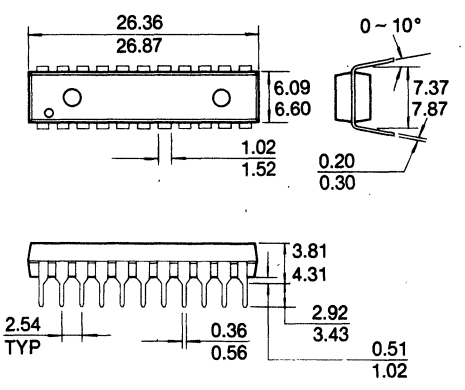
Unit: mm



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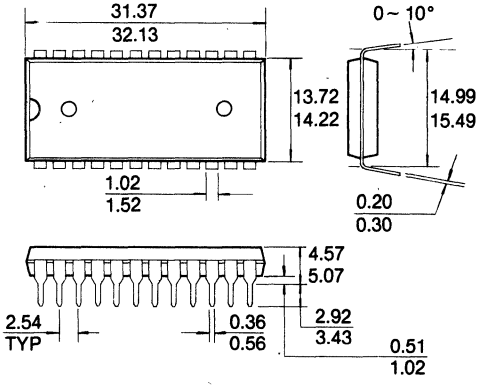

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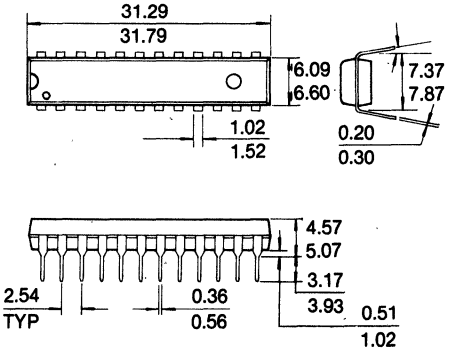

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PACKAGE DIMENSIONS

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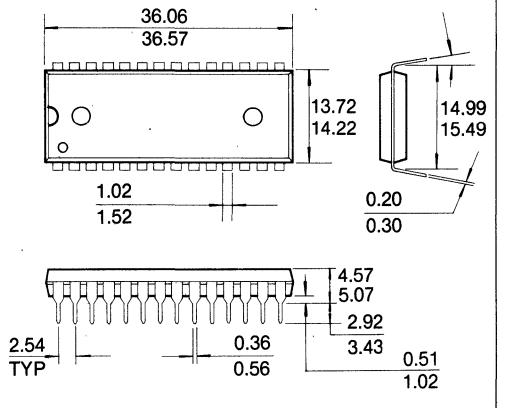
Unit: mm



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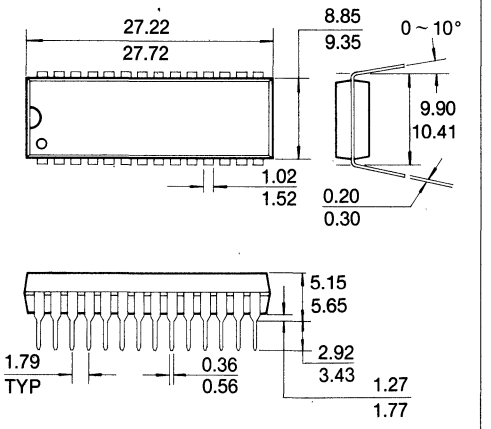

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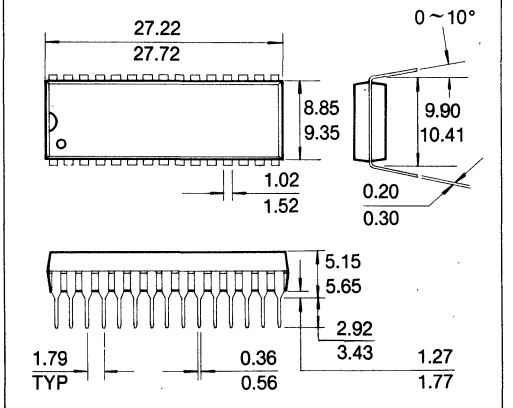

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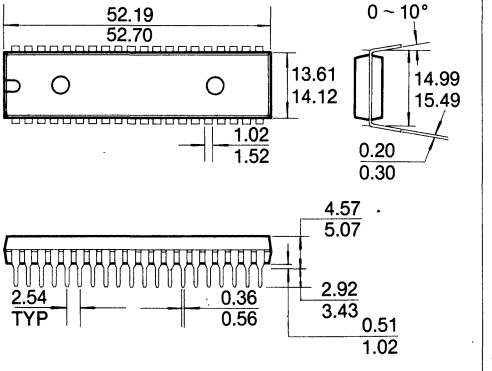

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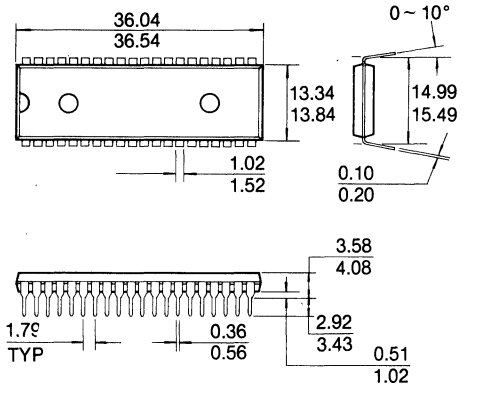

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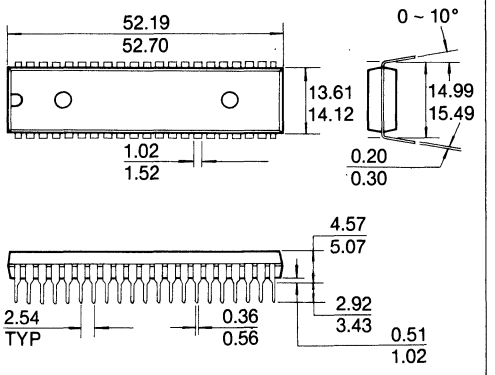
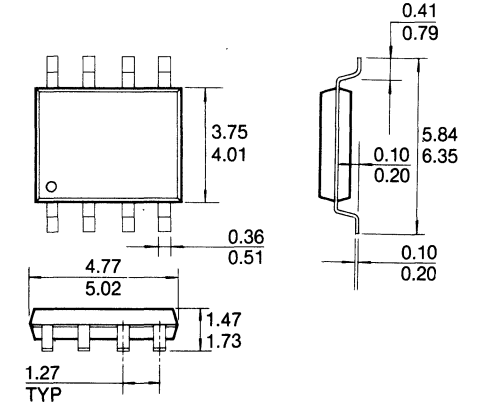


8 SOP

Unit: mm



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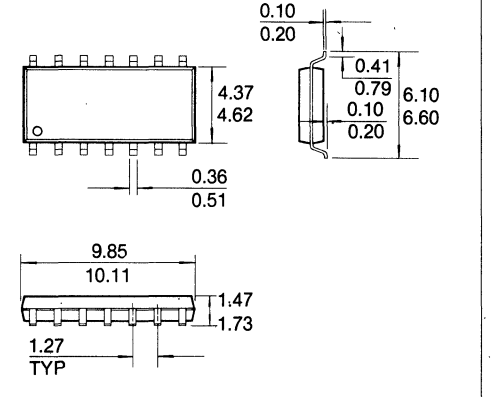

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PACKAGE DIMENSIONS

16 SOP

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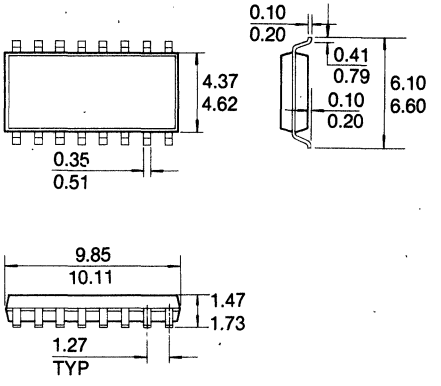

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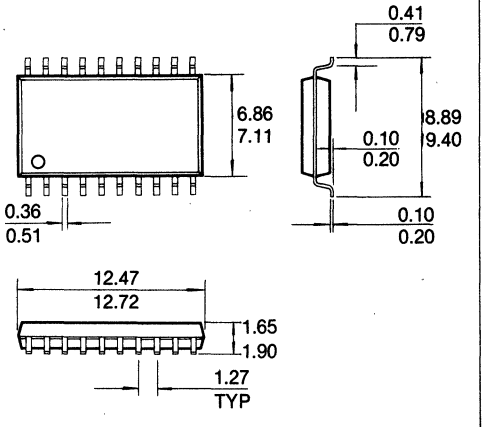

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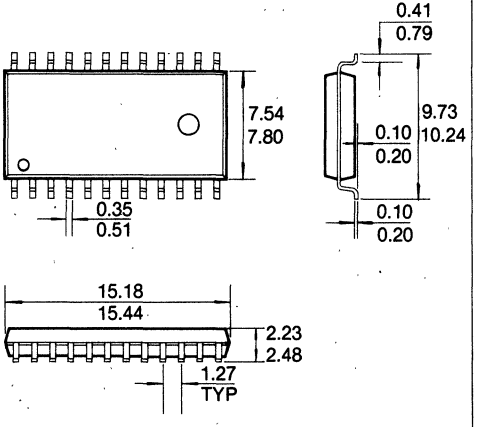

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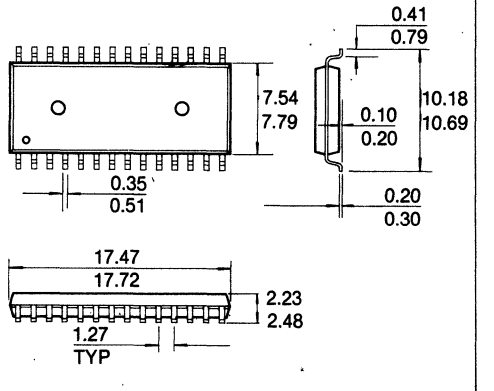
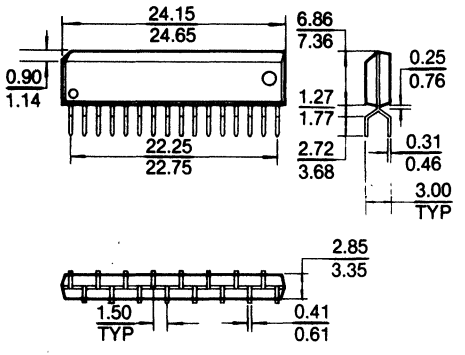


PACKAGE DIMENSIONS

16 ZIP **Unit: mm**



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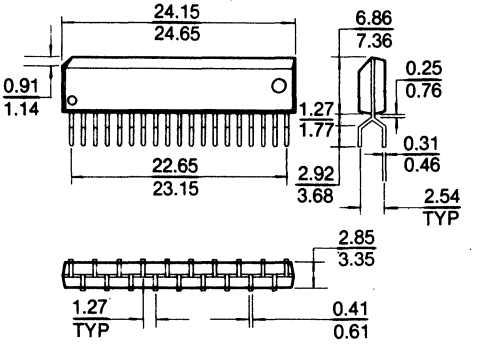
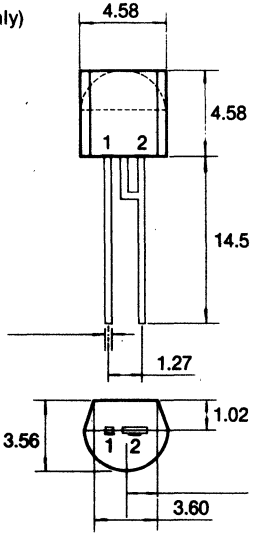


TO-92 **Unit: mm**

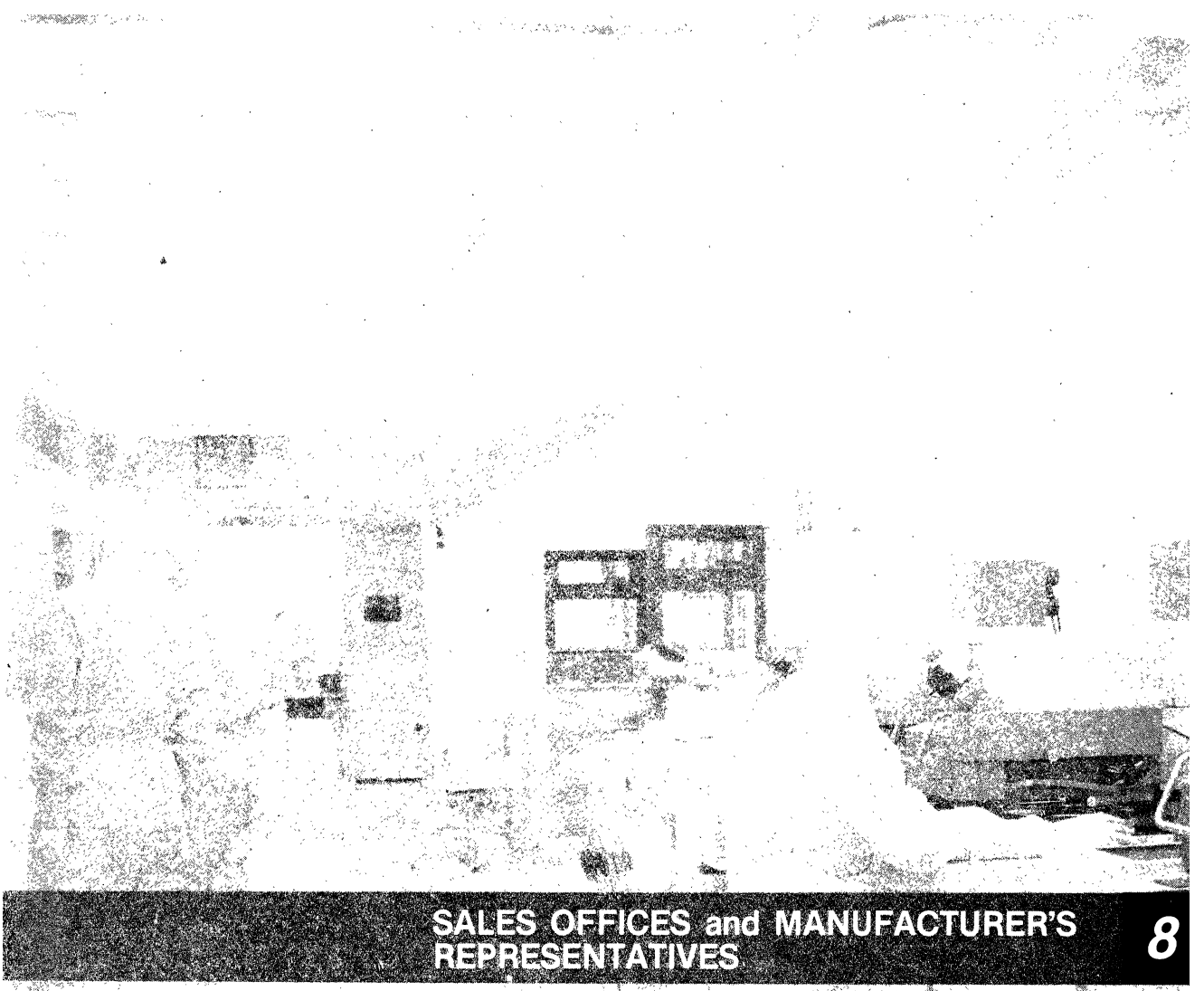
(KA33V Only)



1. Anode 2. Cathode

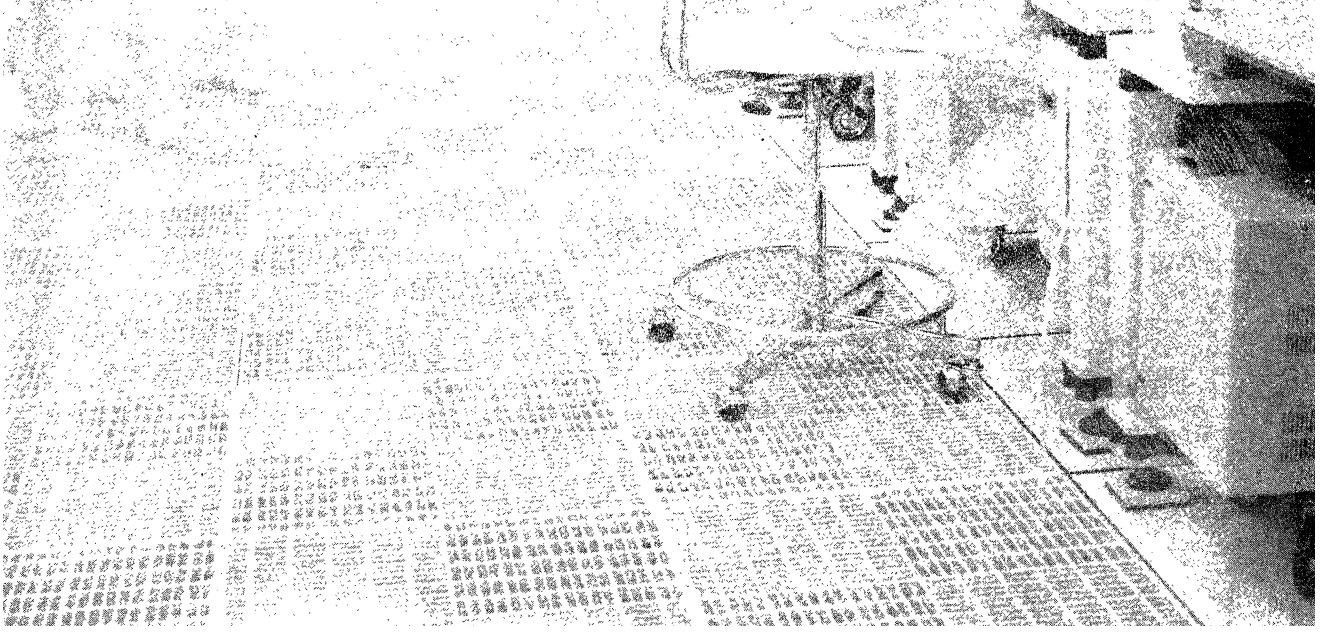
7

NOTE



SALES OFFICES and MANUFACTURER'S REPRESENTATIVES

8



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