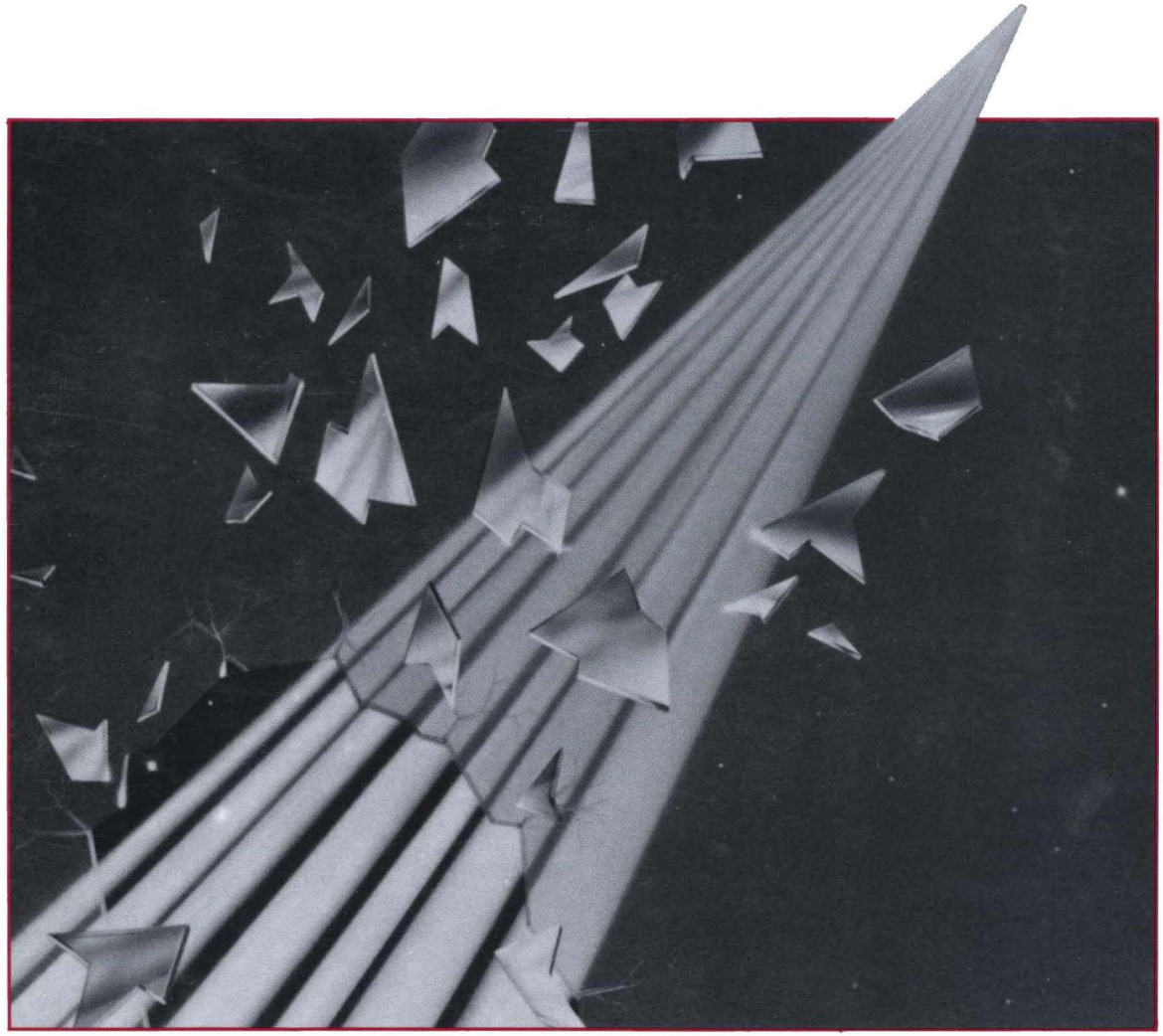
HIGH PERFORMANCE CMOS PRODUCTS

DATA BOOK 1988



WAFERSCALE INTEGRATION, INC.

HIGH PERFORMANCE CMOS PRODUCTS

1988

WSI

WaferScale Integration, Inc.

High Performance CMOS Products Databook

1988

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SHATTERING BARRIERS THAT LIMIT GROWTH

In its short history, WaferScale Integration, Inc. (WSI) has made commonplace the breaking of traditional barriers that limit high-performance system evolution. Company "breakthroughs":

- First company to patent a self-aligned split-gate single transistor EPROM cell and place it in high volume production.
- First company to produce a 55 ns 8K × 8 CMOS EPROM.
- First company to produce a 43 MHz 4-bit CMOS bit slice processor.
- First company to produce monolithic 16-bit and 32-bit CMOS bit slice processors, both as stand-alone products and as cell library macros.
- First company to produce a 128K CMOS re-programmable non-volatile memory with bipolar PROM pinouts.
- First company to produce a 30 ns 16 × 16 CMOS Multiplier Accumulator.
- First company to produce a 55 ns × 16 (wordwide) CMOS EPROM.
- First company to produce 55 ns 32K × 8 CMOS EPROMs.
- First company to combine high-performance EPROM, SRAM and logic all on the same circuit.
- First company to have 33 re-programmable CMOS EPROM products compliant to MIL-STD-883C.
- First company to produce user-configurable high-performance CMOS re-programmable board-replacement system controllers.
- First company to produce a family of 16K to 64K CMOS RPROMs™ with sub-35 ns access time.
- First company to produce address mappable memory circuits that combine EPROM, SRAM and logic.

As WSI moves into faster sub-micron CMOS technologies in 1988 and continues to develop new programmable solutions for higher performance system markets, additional barriers will continue to be broken in our drive for leadership in high-performance next-generation programmable semiconductor products that integrate both memory and logic. WSI thus enables its customers to achieve faster market entry, higher performance systems and more easily producible end products.

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

GENERAL INFORMATION

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

WAFERSCALE INTEGRATION, INC.

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INTRODUCTION

WaferScale Integration, Inc. (WSI) has achieved marked increases in sales of its programmable CMOS memory, logic and semicustom products. These increased sales have resulted in a solid financial position including profitability. WSI is leveraging its proprietary CMOS technology and circuit architectures with strategic alliances involved in technology, manufacturing and distribution. This partnership structure has resulted in WSI's rapid emergence as the leader in high-performance next-generation user-programmable semiconductor products integrating both memory and logic.

WSI serves its customers with the industry's fastest family of non-volatile CMOS EPROM and RPROM™ memory circuits, high-speed CMOS bit-slice processors and peripherals and programmable board-replacement cell-based custom circuits. WSI continues to build on its unique technology by bringing to market fast new user-programmable controllers and specialized memory products that combine high-performance EPROM, SRAM and logic on one circuit. WSI supports these new products with a complete system development environment including software assemblers, simulators and utilities as well as the MagicPro™ programmer. These development tools are used by customer design engineers during system development. Derived customer benefits from using the new user-programmable products include faster time to market, higher levels of integration resulting in smaller, more efficient products and higher system performance.

THE COMPANY

WSI was founded in August, 1983, to develop integrated circuit technologies and products tailored specifically to meet the needs of high-performance systems developers. The company is headquartered in a 66,000 square foot facility in Fremont, California and employs 100 people.

The company's leveraging of its partnerships with Sharp Corporation, GE Solid State, Altera Corporation, Intergraph Corporation, and Kyocera Corporation enables WSI to invest its capital into advancing its technology, serving its customers, and realigning products to match market shifts.

Sharp Corporation and GE Solid State have invested in WSI through equity positions, and both companies hold WSI technology licenses. Altera Corporation and Intergraph Corporation are two additional strategic alliances involving either equity and/or technology. The Kyocera alliance involves equity and distribution of WSI product in Japan.

In its first round of financing in February, 1984, the company secured $16.1 million in equity, equipment loans, leaselines, and facilities leasehold improvements. Investments were received from private sources, venture capital groups, and corporate investment funds.

After achieving significant milestones in its first year of operation, the company secured its second round of equity financing in October, 1984, for $8.5 million. WSI completed its third round financing in January, 1986 raising an additional $13 million in equity and licensing of its CMOS and EPROM technology. All of WSI's previous institutional investors participated in the third round.

A fourth round of financing with Kyocera Corporation as an added investor has been completed, exceeding $8 million. This round brings the company's total financing to over $30 million. Corporate investors cornerstoned and contributed over 60% of the fourth round.

MARKETING STRATEGY

Today's rapidly expanding systems markets demand semiconductor products that provide exceptionally high speed, high reliability, high levels of integration, low power, a high electrostatic discharge protection, low to moderate cost, and in the case of semicustom circuits, the ability to tailor or program the product to achieve unique customer defined functions.

WSI focuses on high-performance markets that include telecommunications, minicomputers, local area networking, digital signal processing, array processing, high resolution color graphics, and military avionics and communications. The company's products are used where system designers are pushing the limits of system performance. These high-speed requirements often involve real time data manipulation and control.

Major market involvement of WSI's products presently include 55% office automation, 25% telecommunication, 15% military, and 5% other. Marketing direction has been established to balance office automation, telecommunication, and military to roughly 30% each by 1990.

To fulfill the needs of these markets, WSI has focused its attention on customer service. The company's product-development teams rely heavily on first-hand input from its customer base regarding new products. WSI provides extensive technical information to customers in the form of printed product data, application notes, and personal design assistance. WSI is supplying an engineering programmer (dubbed "MagicPro" for Memory And loGIC PROgrammer) which will enable customer engineers to incorporate new WSI products into their designs without having to wait until the algorithms are commercially published for production use.

WSI has a CBIC (Cell-Based-Integrated-Circuit) program through which customers can combine a variety of proven macro-cell functions and produce a unique high-performance programmable integrated circuit tailored to exact customer specifications.

SALES NETWORK

WSI's products are sold worldwide through a sales network that includes a combination of regional and direct sales managers, manufacturers' representative companies, and component distributors.

WSI has direct sales offices in Boston, MA; Huntsville, AL; Philadelphia, PA; Los Angeles and Fremont, CA; and Chicago, IL. Over 25 manufacturers' representative companies sell WSI products to major accounts on a nationwide basis. WSI's U.S. distributors include Time Electronics, Wyle Laboratories, Pioneer Technologies, and Pioneer Standard.

WSI has expanded its sales coverage in Europe and Japan. The company's European sales representatives include Tekelec Airtronic GmbH (Germany), Micro Call Ltd (England), REA (France), Silverstar (Italy), Traco AB (Sweden), Bacher GmbH (Austria, Switzerland), OY Comdax AB (Finland), OTE A/S (Norway), Distributoren Interelko, A/S (Denmark), Unitronics, S.A. (Spain), Inelco (Belgium and Luxembourg), Components & Systems Electronics B.V. (Holland), and Vectronics (Israel). In the Orient, Kyocera Corporation recently has been named as a WSI sales representative for Japan along with Nippon Imex Corporation (Japan), Components Agent Ltd (Hong Kong), Sertec International, Inc. (Taiwan), and Eastern Electronics, Inc. (Korea).

MANUFACTURING STRATEGY

A key ingredient for success in leading-edge semiconductors is a world-class fabrication facility that ensures high volume capacity and prompt delivery of highly reliable and high yielding VLSI circuits. To this end, WSI has licensed its proprietary CMOS logic and EPROM process to Sharp Corporation of Osaka, Japan and GE Solid State in Somerville, NJ.

WSI's semicustom and standard products are manufactured at Sharp's highly automated manufacturing facility where it produces 5-inch wafers with 1.2 micron CMOS VLSI circuits in a Class 1 clean room environment. The Sharp facility employs the most advanced manufacturing equipment available including ion implantation, reactive ion etch, and wafer stepper lithographic systems.

The WSI-GE Solid State alliance provides WSI with a state-side second source. The GE Solid State Class 10 facility in Findley, Ohio provides 1.0 micron CMOS circuits on 5-inch wafers, and includes wafer stepper lithography and dry etch capability. As a self-contained unit, wafer fabrication, assembly, and test can all be performed at this facility.

The benefits derived from this WSI multi-fab strategy include product manufactured with very high quality, high wafer yields which enable low customer prices, and on-time delivery to meet demanding customer schedules . . . all at low fixed cost to WSI.

PRODUCTS

WSI is the innovative leader in the high-speed EPROM arena. WSI began shipping the world's first CMOS 8K x 8 RPROM™ in the first quarter of 1986. RPROMs (UV erasable re-programmable PROMs) provide bipolar PROM pin-out and matching speed as well as CMOS low-power operation.

In mid-1987, WSI introduced the world's fastest pair of 256K CMOS EPROMs using its newly patented, self-aligned split gate EPROM technology. These EPROMs feature access times of just 55 ns and provide one- and two-chip program-store solutions for 16- and 32-bit MPU and DSP applications.

In addition to producing the world's fastest family of CMOS EPROMs, WSI supplies very high-speed CMOS bit-slice processors and peripheral circuits that operate faster than bipolar products while using only a small fraction of the power.

WSI's ability to combine EPROM, SRAM, and complex system logic functions on a single high-performance integrated circuit is unique among semiconductor companies. Examples of this capability are seen in the Microprogrammable Controller (PAC™) family, the MAP™ family of mappable memory products and the Stand-Alone Microsequencer (SAM™) series. This same capability is used to develop powerful cell-based semicustom circuits that are unique to customer requirements. A re-programmable semicustom circuit provides flexibility in software, system configuration, and commonality of use among many customer projects.

The WSI CMOS macro-block cell library provides VLSI EPROM and SRAM memory and logic cells. When coupled with WSI's advanced CAD system, it enables WSI to build specially designed integrated circuits for its customers. The use of pre-characterized and pre-proven macro cells greatly insures the early success of each project. By using these powerful LSI functions, in addition to common logic elements, the cell library enables programmable subsystems or even complete system designs to be integrated on a single piece of silicon.

The macro-block CMOS cell library contains a family of high-performance bit-slice processor cells (from 4-bit to 32-bit) with better than bipolar LSI performance. Also included are bit-slice processor peripheral cells including microprogram controllers, variable pipelines, FIFOs, multipliers, bus registers, and register files. The library also contains high-density, very fast CMOS EPROM memory cell arrays, high-performance cell compilers for fast static RAM arrays, ROM arrays, and PLA cell arrays. High-speed random logic cells, which are functionally compatible with the popular 7400/4000 series, are also included in the library.

Many of the macro-cells developed for the cell library are excellent as stand-alone standard products. By providing these high-performance standard products, WSI can assist its customers in achieving enhanced system performance either in discrete design configurations or as design aids in advance of a full semicustom solution.

QUALITY AND RELIABILITY

WSI has designed, developed and implemented a Quality and Reliability System whose mission is to continually produce Commercial and Military products that meet, and most often exceed, the customers' requirements.

WSI is deeply committed to product excellence. This begins with proper management attitude and direction and through this focus the Quality and Reliability Program is able to operate efficiently. As a result, product quality becomes part of each employee's responsibilities.

Quality and Reliability begin with the proper product and process designs and is supported by material and process controls. Examples are products manufactured on an epitaxial silicon layer to reduce latch-up sensitivity, all pins are designed to withstand >2,000 volts ESDS, numerous ground taps are used which increases product noise immunity, metal traces are designed to carry a current density of $>2.0 \times 10^5$ amps/cm^2, top passivation extends over into the scribe lane to seal the die edges, data retention is performed 100% on re-programmable products (T_A = +200°C, T = 48 hours), automated die attach and bonding is used extensively, wafers are fabricated in a ≤Class 10 clean room, raw materials, chemicals and gases are inspected before use, and statistical controls are used to keep the process on course.

Product and process introductions or changes are routinely evaluated for worthiness. Life Tests are conducted at higher than typical stress levels (T_A = +150°C, V_{CC} = +6.5V) and even at these stress levels, WSI products have demonstrated low failure rates (see the Quality and Reliability section in this databook).

WSI is active in Military programs and its Quality and Reliability System supports Compliant Non-Jan products. WSI also supports DESC's (Defense Electronics Supply Center) Standardized Military Drawings (SMD) program. As of February, 1988, WSI is on three SMDs, two are pending and more are in process. See the Military section in this databook.

For additional information, call 800-TEAM-WSI (800-832-6974). In California, call 415-656-5400.

WSI CMOS TECHNOLOGY

Each generation of systems involved with data processing, digital communications, and real-time data analysis and control historically require faster and more efficient system elements to accomplish greater productivity. Issues of performance, reliability, integration, power and cost must be successfully addressed to insure the successful development of highly competitive end products. WSI's CMOS technology forms the foundation on which successful, high-performance next-generation systems may be realized.

The basic WSI CMOS process is a 1.2 micron N-well epi technology with double poly and single metal. This process enables the combining of non-volatile memory, static random access memory and logic functions all on the same low power circuit.

WSI's core EPROM technology begins with its patented self-aligned single transistor split-gate EPROM cell (Patent Number #4,639,893). This advancement beyond the traditional "stacked gate" EPROM cell provides much higher read current at comparable cell size. Proprietary EPROM array design enhancements such as clocked differential sensing, address-transition detection and the use of low resistance tungsten silicide in the second poly layer result in very high-speed memory products. Manufacturability is also improved as fewer EPROM cells are needed to complete a fast memory array, thus more conservative photolithography may be used.

WSI's use of epi wafers and design innovations result in products that exhibit immunity to latch-up and provide ESD protection far in excess of that specified by MIL-STD-883C.

The WSI EPROM technology has proliferated into families of high-performance EPROMs, bipolar PROM replacement products, user-configurable system products and cell-based custom capabilities described in this databook. When the high-speed split-gate EPROM technology is combined with high-performance cell-based logic functions, new user-configurable CMOS circuits such as the 20 MHz Microprogrammable Controller (PAC™) series are realized. An additional family of 40 ns mappable (MAP™) memory products combine EPROM, SRAM and logic on a single chip. WSI's fast CMOS logic has yielded a market leading 30 ns 16 × 16 CMOS Multiplier Accumulator and a 33 MHz 32-bit CMOS bit slice processor . . . both the fastest in their class.

WSI's ability to rapidly combine any of these completed or modified macro memory or logic functions into a custom high-performance cell-based board-replacement circuit for special customer applications makes WSI unique among semiconductor companies.

WAFERSCALE'S 256-K EPROM RUNS SUPERFAST

Speed or density? Density or speed? Thanks to WaferScale Integration Inc., systems designers no longer must compromise. The Fremont, Calif., company has just unleashed a pair of high-speed, 256-Kbit ultraviolet-erasable CMOS programmable read-only memories. With 50- to 55-ns access times, they are the fastest nonvolatile memories on the market at 256 Kbits and beyond—at least two to three times quicker than comparably sized PROMs, and coming within range, at twice the density, of the largest commercial bipolar PROM [*Electronics*, Feb. 10, 1986, p. 35]. And active power dissipation is a comfortable 325 milliwatts, just half that of its closest bipolar rival, sinking to 75 mW on standby.

With their combination of speed and density, the word-wide 16-K-by-16-bit WS57C257 and byte-wide 32-K-by-8-bit WS57C256F are tailored to one- and two-chip program storage for 16- and 32-bit microprocessors and digital signal processing. Conventionally, anywhere from 4 to 16 nonvolatile memories are needed. Current plans call for the byte-wide memory to hit the streets in July in standard 28-pin ceramic dual in-line packages and 32-pin ceramic leadless chip carriers. The word-wide part will follow sometime in the third quarter, in 40-pin Cerdips and 44-lead ceramic leadless chip carriers. Both are priced at $94 per unit in 100-unit sample quantities.

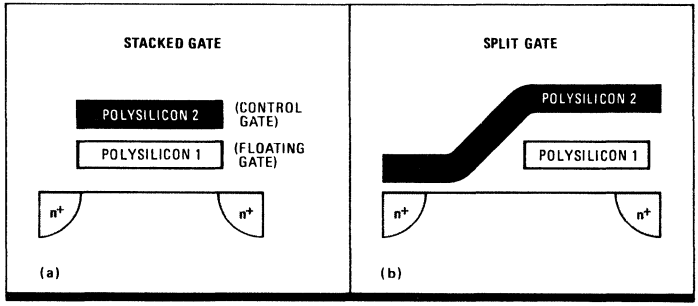
To achieve this unprecedented combination of speed and density, engineers at WaferScale Integration refined the company's process technology and fine-tuned the circuit design. On the process side, a slimmed-down, second-generation 1.2-μm CMOS process, a scaled version of the company's patented split-gate EPROM cell, and tungsten silicide word lines were the keys to success. On the circuit-design side, clocked differential sensing and a novel precharge technique, a special two-step ac signal scheme, and address-transition detection were the key developments. "These two devices disprove the traditional belief that you could have speed or size, but not both, in your microcontrol store," says Jerry Banks, marketing manager for standard products. "These large-architecture CMOS EPROMs are ideally suited for modems, real-time control, guidance systems, digital signal processing, and other real-time or complex processing applications."

WaferScale Integration first boiled down its CMOS process—from 1.5 to 1.2 μm—and then used the refined technology to whip up a scaled version of its proprietary split-gate EPROM cell. Just 6.5 μm on a side, the latest split-gate incarnation is roughly half the size of its predecessor. There's more to the new cell than just size, but the company won't go any further than saying that it adopted tungsten silicide.

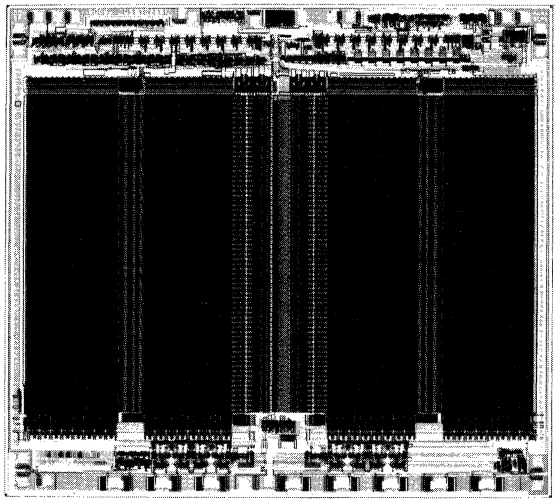
The main problem with the traditonal stacked-gate cell, notes Boaz Eitan, manager of the PROM program, is that it forces a tradeoff between the necessarily high read current and efficient programmability. "In traditional implementations, chip designers have had to make a choice," he says. "If they wanted speed, they had to implement a PROM cell with three to four transistors, separating the read, write, and select functions. If they wanted density, all three functions could be incorporated into a single-stacked PROM cell, but only at considerable sacrifice in speed."

The heart of the trouble lies in rapidly sensing the word- and bit-line voltages after address decoding. "The bit-line capacitance plays a big part in the equation," explains Syed Ali, manager of memory design. "If the capacitance remains fixed, a higher read current is needed to achieve greater speed. However, if the capacitance can be lowered, the speed can be boosted without increasing the read current."

The split-gate structure weds the best of the multiple-transistor and single-stacked cell approaches, requiring none of the compromises inherent in either. It consists of a MOS transistor linked in series with a floating-gate transistor that has been merged into a composite device (see fig. 1). In this design, says Eitan, the second polysilicon layer acts as the control gate and directly covers part of the channel area. "This eliminates drain turn-on and source-drain punchthrough, which adversely affects the stan-



1. SPLITS. Unlike the stacked-gate transistor (a), the split-gate transistor (b) has a second poly control gate that partly covers the channel, preventing drain turn-on and source-drain punchthrough.



2. DELAY KILLER. Tungsten-silicide deposition helps WaferScale's 256-Kbit EPROM achieve its 45-ns access time.

dard stacked-gate EPROM cell." As a result, bit-line read currents in excess of 150 μA can be achieved, compared with the 50 μA typical of conventional stacked-gate cells, giving the speed of the multiple-transistor EPROM cell without its attendant die size.

The memory array (see fig. 2) is divided into two planes, each consisting of two blocks separated by a mid-word-line repeater. Tungsten silicide is deposited over the second polysilicon layer to reduce word-line RC delays, further improving access time. With a resistance of only 3 Ω per square μm, tungsten silicide helps reduce the delay to 60% of that incurred with traditional aluminum metallization. The 512 columns of the array are divided into blocks of eight columns, each block with its own dedicated source lines.

The higher bit-line voltage and read current established by the split-gate structure allow the company to employ a differential-sensing scheme that does not require a separate bit line, thus eliminating bit-line capacitance. In this scheme, the sense amplifier is designed to work in conjunction with a trip inverter. During precharge, the outputs of the differential amplifier and the inverter are precharged to the inverter trip point, enabling the inverter to move rapidly in either direction after a signal has been detected. The relative difference in the rate of discharge between the bit line and a column of reference cells provides just enough differential voltage for high-speed sensing.

To ensure that signal levels are high enough for sensing—a key consideration in all memories, as density increases and interconnects get longer—a two-step ac signal-development scheme has been incorporated into the circuits. In the first step of the proprietary approach, a small ac signal is generated by using a capacitor-imbalancing technique. This 100-mV signal is rapidly read out by a differential sense amplifier. In the second step, the on-chip circuitry converts this signal to a 300-mV dc signal that is used to increase programmed cell margins by as much as 25%.

As a result, says Eitan, the design senses bit-line voltages more than five times faster than previous devices. The scheme also makes for fast programming. Typically, it takes only 0.1 ms to program a byte, compared with 1 ms for older technologies.

Address-transition detection also contributes to the improved access times. Normally associated with static random-access memories, it helps precharge the bit lines and to equalize the gain of the critical sense amplifiers. When an address transition is detected, an enable pulse is generated that precharges the bit-lines and critical sense-amplifier nodes. This eliminates the setup time normally encountered in PROMs. To further reduce the precharge time, the bit-line voltage swing is kept within narrow limits. More time is saved by performing the address decoding in parallel with the bit-line precharge, then ending them simultaneously.

To keep power dissipation down, only 25% of the cells in the array have access to the supply voltage during a read. This dramatically decreases the supply current to no more than 40 mA at 20 MHz, about half that of other designs.

WaferScale Integration is also using its high-speed process for a 64-Kbit PROM, the 8-K-by-8-bit WS57C49B, a direct pin-for-pin replacement for a bipolar PROM (called a reprogrammable ROM, or RPROM). At 35 ns it matches most high-speed CMOS SRAMs in access time. Another device for which it is using the high-speed process is a pin-for-pin CMOS relacement for the Am27C51, a 128-Kbit bipolar PROM from Advanced Micro Devices Inc., Sunnyvale, Calif. The WS57C51 is a 16-K-by-8-bit RPROM with an access time of only 55 ns and a chip area of only 32,000 mils^2, 60% smaller than the AMD device.

The company is now working on its next-generation CMOS PROM process, which at 1.0 μm will enable it to build 64-Kbit memories that access in only 25 ns and 128-Kbit and 256-Kbit devices that access in 35 ns. The same process will also allow WaferScale Integration to extend its speed challenge up into the megabit range. "There is nothing in our process that I can see that will prevent us from building 1-Mbit EPROMs with access times as low as 55 ns," Ali says. *–Bernard C. Cole*

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

PART NUMBER	DESCRIPTION	SPEED	PACKAGE
One-Time Programmable (OTP) CMOS PROMs			
WS57C191	2K x 8 CMOS PROM	45/55 ns	24 PDIP
WS57C191B	2K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C291	2K x 8 CMOS PROM	45/55 ns	24 PDIP
WS57C291B	2K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C45	2K x 8 Registered CMOS PROM	20/25/35 ns	24 PDIP 24 CERDIP
WS57C43B	4K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C49	8K x 8 CMOS PROM	55/70 ns	24 PDIP
WS57C49B	8K x 8 CMOS PROM	35/45 ns	24 PDIP
Re-Programmable CMOS PROMs (RPROMs)			
WS57C191	2K x 8 CMOS RPROM™(1)	45/55 ns	24 CERDIP 28 CLLCC
WS57C191B	2K x 8 CMOS RPROM™(1)	35/45 ns	24 CERDIP 28 CLLCC
WS57C291	2K x 8 CMOS RPROM™(1)	45/55 ns	24 CERDIP 28 CLLCC
WS57C291B	2K x 8 CMOS RPROM™(1)	35/45 ns	24 CERDIP 28 CLLCC
WS57C45	2K x 8 CMOS Registered RPROM™(1)	20/25/35 ns	24 Flatpack 24 CERDIP
WS57C43	4K x 8 CMOS RPROM™(1)	55/70 ns	24 CERDIP 28 CLLCC
WS57C43B	4K x 8 CMOS RPROM™(1)	35/45/55 ns	24 CERDIP 28 CLLCC
WS57C49	8K x 8 CMOS RPROM™(1)	55/70 ns	24 CERDIP 28 CLLCC
WS57C49B	8K x 8 CMOS RPROM™(1)	35/45/55 ns	24 CERDIP 28 CLLCC
WS57C51	16K x 8 CMOS RPROM™(1)	70 ns	28 CERDIP
WS57C51B	16K x 8 CMOS RPROM™(1)	40/45/55/70 ns	28 CERDIP 32 CLLCC
High-Speed Byte-Wide CMOS EPROMs			
WS57C64F	8K x 8 CMOS High Speed EPROM	55/70 ns	28 CERDIP 32 CLLCC
WS57C128F	16K x 8 CMOS High Speed EPROM	55/70 ns	28 CERDIP 32 CLLCC
WS57C256F	32K x 8 CMOS High Speed EPROM	55/70 ns	28 CERDIP 32 CLLCC

PRODUCT SUMMARY (Continued)

PART NUMBER	DESCRIPTION	SPEED	PACKAGE
High-Speed Byte-Wide CMOS EPROMs (Continued)			
WS57C256F	32K × 8 CMOS High Speed EPROM	35/45 ns	28 CERDIP 32 CLLCC
WS27C256L	32K × 8 CMOS High Speed LP EPROM	90/120 ns	28 CERDIP 28 PDIP 32 CLLCC
WS27C256F	32K × 8 CMOS High Speed LP EPROM	90/120 ns	28 CERDIP 32 CLLCC
WS27C512F	64K × 8 CMOS High Speed LP EPROM	70/90 ns	28 CERDIP 32 CLLCC
WS27C010L	128K × 8 CMOS High Speed LP EPROM	90/120/150 ns	32 CERDIP
WS57C010F	128K × 8 CMOS High Speed EPROM	55/70 ns	32 CERDIP
Military Low Power CMOS EPROMs			
WS27C64F	8K × 8 Military CMOS LP EPROM	90/120/150 ns	28 CERDIP 32 CLLCC
WS27C128F	16K × 8 Military CMOS LP EPROM	90/120/150 ns	28 CERDIP 32 CLLCC
WS27C256F	32K × 8 Military CMOS LP EPROM	90/120/150 ns	28 CERDIP 32 CLLCC
High-Speed Word-Wide CMOS EPROMs			
WS57C65	4K × 16 CMOS EPROM	55/70 ns	40 CERDIP 44 CLLCC
WS57C66	4K × 16 CMOS EPROM (Multiplexed Address/Data)	55/70 ns	40 CERDIP 44 CLLCC
WS57C257	16K × 16 CMOS EPROM	55/70 ns	40 CERDIP 44 CLLCC
WS57C210F	64K × 16 CMOS EPROM	55/70 ns	40 CERDIP
Mapped-Address Programmable Products			
WSMAP162	128K EPROM/32K SRAM MAP™ Memory	40 ns	40 CERDIP
WSMAP161	128K EPROM/32K SRAM MAP™ Memory	40 ns	40 CERDIP
WSMAP168	128K EPROM/32K SRAM MAP™ Memory	40 ns	44 CPGA 44 CLLCC 44 PLDCC
CMOS Bit-Slice Processors and Peripherals			
WS5901	4-Bit CMOS Bit-Slice Processor	C, D	40 PDIP
WS59016	16-Bit CMOS Bit-Slice Processor	C, D	64 SDBRZ DIP 68 PLDCC 68 CLDCC
WS59032	32-Bit CMOS Bit-Slice Processor	D, E	101 CPGA
WS5910A	12-Bit CMOS Variable Sequencer	A	40 CERDIP 40 PDIP

PRODUCT SUMMARY (Continued)

PART NUMBER	DESCRIPTION	SPEED	PACKAGE
CMOS Bit-Slice Processors and Peripherals (Continued)			
WS5910B	12-Bit CMOS Variable Sequencer	B	40 CERDIP 40 PDIP
WS59520	CMOS Variable Pipeline Register	—	24 CERDIP 24 PDIP
WS59521	CMOS Variable Pipeline Register	—	24 CERDIP 24 PDIP
WS59510	CMOS 16-Bit Multiplier Accumulator	30/40/50 ns	68 PLDCC 68 CPGA 64 PDIP
WS59820	CMOS Bi-Directional Bus Register	23 ns	68 PLDCC 68 CPGA
Programmable Logic Products			
WSPAC116	CMOS Programmable Stand-Alone Controller	20 MHz	88 CPGA
WS444	CMOS Programmable Stand-Alone Microsequencer (SAM)	32 MHz	24 CERDIP
WS448	CMOS Programmable Stand-Alone Microsequencer (SAM)	32 MHz	24 CERDIP

NOTES: 1) RPROM™: Re-Programmable PROM
CMOS Replacement for Bipolar PROM's

2) LP EPROM: Low Power EPROM

PART NUMBER	DESCRIPTION	SPEED	PACKAGE
WS444	CMOS Programmable Stand-Alone Microsequencer (SAM)	32 MHz	24 CERDIP
WS448	CMOS Programmable Stand-Alone Microsequencer (SAM)	32 MHz	24 CERDIP
WS27C64F	8K x 8 Military CMOS LP EPROM	90/120/150 ns	28 CERDIP 32 CLLCC
WS27C010L	128K x 8 CMOS High Speed LP EPROM	90/120/150 ns	32 CERDIP
WS27C128F	16K x 8 Military CMOS LP EPROM	90/120/150 ns	28 CERDIP 32 CLLCC
WS27C256F	32K x 8 Military CMOS LP EPROM	90/120/150 ns	28 CERDIP 32 CLLCC
WS27C256F	32K x 8 CMOS High Speed LP EPROM	90/120 ns	28 CERDIP 32 CLLCC
WS27C256L	32K x 8 CMOS High Speed LP EPROM	90/120 ns	28 CERDIP 28 PDIP 32 CLLCC
WS27C512F	64K x 8 CMOS High Speed LP EPROM	70/90 ns	28 CERDIP 32 CLLCC
WS57C43	4K x 8 CMOS RPROM™(1)	55/70 ns	24 CERDIP 28 CLLCC
WS57C43B	4K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C43B	4K x 8 CMOS RPROM™(1)	35/45/55 ns	24 CERDIP 28 CLLCC
WS57C45	2K x 8 CMOS Registered RPROM™(1)	20/25/35 ns	24 Flatpack 24 CERDIP
WS57C45	2K x 8 CMOS Registered PROM	20/25/35 ns	24 PDIP 24 CERDIP
WS57C49	8K x 8 CMOS PROM	55/70 ns	24 PDIP
WS57C49	8K x 8 CMOS RPROM™(1)	55/70 ns	24 CERDIP 28 CLLCC
WS57C49B	8K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C49B	8K x 8 CMOS RPROM™(1)	35/45/55 ns	24 CERDIP 28 CLLCC
WS57C51	16K x 8 CMOS RPROM™(1)	70 ns	28 CERDIP
WS57C51B	16K x 8 CMOS RPROM™(1)	40/45/55/70 ns	28 CERDIP 32 CLLCC
WS57C64F	8K x 8 CMOS High Speed EPROM	55/70 ns	28 CERDIP 32 CLLCC
WS57C65	4K x 16 CMOS EPROM	55/70 ns	40 CERDIP 44 CLLCC

NUMERICAL LISTING (Continued)

PART NUMBER	DESCRIPTION	SPEED	PACKAGE
WS57C66	4K x 16 CMOS EPROM (Multiplexed Address/Data)	55/70 ns	40 CERDIP 44 CLLCC
WS57C010F	128K x 8 CMOS High Speed EPROM	55/70 ns	32 CERDIP
WS57C128F	16K x 8 CMOS High Speed EPROM	55/70 ns	28 CERDIP 32 CLLCC
WS57C191	2K x 8 CMOS PROM	45/55 ns	24 PDIP
WS57C191	2K x 8 CMOS RPROM™(1)	45/55 ns	24 CERDIP 28 CLLCC
WS57C191B	2K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C191B	2K x 8 CMOS RPROM™(1)	35/45 ns	24 CERDIP 28 CLLCC
WS57C210F	64K x 16 CMOS EPROM	55/70 ns	40 CERDIP
WS57C256F	32K x 8 CMOS High Speed EPROM	55/70 ns	28 CERDIP 32 CLLCC
WS57C256F	32K x 8 CMOS High Speed EPROM	35/45 ns	28 CERDIP 32 CLLCC
WS57C257	16K x 16 CMOS EPROM	55/70 ns	40 CERDIP 44 CLLCC
WS57C291	2K x 8 CMOS PROM	45/55 ns	24 PDIP
WS57C291	2K x 8 CMOS RPROM™(1)	45/55 ns	24 CERDIP 28 CLLCC
WS57C291B	2K x 8 CMOS PROM	35/45 ns	24 PDIP
WS57C291B	2K x 8 CMOS RPROM™(1)	35/45 ns	24 CERDIP 28 CLLCC
WS5901	4-Bit CMOS Bit-Slice Processor	C, D	40 PDIP
WS5910A	12-Bit CMOS Variable Sequencer	A	40 CERDIP 40 PDIP
WS5910B	12-Bit CMOS Variable Sequencer	B	40 CERDIP 40 PDIP
WS59016	16-Bit CMOS Bit-Slice Processor	C, D	64 SDBRZ DIP 68 PLDCC 68 CLDCC
WS59032	32-Bit CMOS Bit-Slice Processor	D, E	101 CPGA
WS59510	CMOS 16-Bit Multiplier Accumulator	30/40/50 ns	68 PLDCC 68 CPGA 64 PDIP
WS59520	CMOS Variable Pipeline Register	—	24 CERDIP 24 PDIP
WS59521	CMOS Variable Pipeline Register	—	24 CERDIP 24 PDIP
WS59820	CMOS Bi-Directional Bus Register	23 ns	68 PLDCC 68 CPGA

NUMERICAL LISTING (Continued)

PART NUMBER	DESCRIPTION	SPEED	PACKAGE
WSMAP162	128K EPROM/32K SRAM MAP™ Memory	40 ns	40 CERDIP
WSMAP161	128K EPROM/32K SRAM MAP™ Memory	40 ns	40 CERDIP
WSMAP168	128K EPROM/32K SRAM MAP™ Memory	40 ns	44 CPGA 44 CLLCC
WSPAC116	CMOS Programmable Stand-Alone Controller	20 MHz	88 CPGA

NOTES: 1) RPROM™: Re-Programmable PROM
CMOS Replacement for Bipolar PROMs

2) LP EPROM: Low Power EPROM

AMD	WSI
AM27S191	WS57C191
AM27PS191	WS57C191
AM27S291	WS57C291
AM27PS191	WS57C291
AM27S43	WS57C43
AM27PS43	WS57C43
AM27S49	WS57C49
AM27S49A	WS57C49B
AM27S51	WS57C51 or WS57C51B
AM2901	WS5901
AM2910A	WS5910A
AM29520	WS59520
AM29521	WS59521
AM29C101	WS59016*
AM29510	WS59510

ATMEL	WSI
27HC64	WS57C64F
27HC641	WS57C49 or WS57C49B

CYPRESS	WSI
CY7C291	WS57C191
CY7C292	WS57C291
CY7C264	WS57C49
CY7C901	WS5901
CY7C910	WS5910A
CY7C9101	WS59016*
CY7C510	WS59510
CY7C263	WS57C49B
CY7C264	WS57C49B
CY7C254	WS57C51

FAIRCHILD	WSI
93Z511	WS57C191
93Z565	WS57C49 or WS57C49B
29F01	WS5901
29F10	WS5910A

FUJITSU	WSI
MB7138	WS57C191
MB7138-SK	WS57C291
MB7142	WS57C43
MB7144	WS57C49

HARRIS	WSI
HM-76161	WS57C191
HM-76321	WS57C43
HM-76641	WS57C49 or WS57C49B

IDT	WSI
IDT39C01	WS5901
IDT39C10	WS5910A
IDT49C401	WS59016*
IDT7210	WS59510

LDI	WSI
L29C520	WS59520
L29C521	WS59521

MMI	WSI
63S1681	WS57C191
63S3281	WS57C43 or WS57C43B**

NATIONAL	WSI
DM87S191	WS57C191
DM87S291	WS57C291
DM87S321	WS57C43 or WS57C43B**

SIGNETICS	WSI
N82S191	WS57C191
N82S191__-3	WS57C291
N82S321	WS57C43
N82HS321	WS57C43 or WS57C43B**
N82HS641	WS57C49
N27HC641	WS57C49 or WS57C49B

T.I.	WSI
TBP38S166__W	WS57C191
TBP38L166__W	WS57C191
TBP38SA166__W	WS57C191
TBP38S166__T	WS57C291
TBP38L166__T	WS57C291
TBP38SA166__T	WS57C291

MILITARY ONLY

AMD	WSI
AM2764	WS27C64F
AM27128	WS27C128F
AM27256	WS27C256F

INTEL	WSI
M2764	WS27C64F
M27128	WS27C128F
M27256	WS27C256F
M27C64	WS27C64F
M27C128	WS27C128F
M27C256	WS27C256F

* Functional Equivalent **Available Q1 '88

HIGH-PERFORMANCE CMOS PRODUCTS

WS57C----- — **S** **P** **MP**

Basic Part Number

Manufacturing Process:

(blank) = WSI Standard Commercial Product Manufacturing Process

M = Military Operating Range
— Temperature: −55 to +125°C
— Voltage: +5 Volts, ±10%

CB = Commercial Burned-In (enhanced commercial reliability)

MB = MIL-STD-883C

Package:

		Window
A	= Plastic Pin Grid Array	No
B	= Ceramic SDBRZD DIP, 0.9″	No
C	= CLLCC	Yes
D	= CERDIP, 0.6″	Yes
F	= Ceramic Flatpack	Yes
G	= Ceramic Pin Grid Array	No
H	= Ceramic Flatpack	No
J	= PLDCC	No
K	= CERDIP, 0.6″	No
L	= CLDCC	No
M	= Plastic DIP, 0.9″	No
P	= Plastic DIP, 0.6″	No
S	= Plastic DIP, 0.3″	No
T	= CERDIP, 0.3″	Yes
W	= Waffle Packed Dice	—
X	= Ceramic Pin Grid Array	Yes
Y	= CERDIP, 0.6″	No
Z	= CLLCC	No

Speed:

−35 = 35 ns
−55 = 55 ns
−70 = 70 ns
Etc.

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

PROGRAMMABLE MEMORY PRODUCTS

PROM Memory:

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

2K x 8 CMOS PROM

KEY FEATURES

- **Fast Access Time**
  — 45 ns
- **Low Power Consumption**
  — 225 mW Active Power
- **Fast Programming**
- **Pin Compatible with AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

GENERAL DESCRIPTION

The WS57C191/291 is now available as a PROM. It utilizes the same design as the previously released RPROM™ from WSI. The difference is the PROM version is available in plastic packages and is not re-programmable. The plastic packaging is ideal for high volume applications which require automatic insertion. The plastic packaging also provides an economic benefit when compared to a windowed cerdip package. For applications requiring reprogrammability, contact your WSI sales representative for information on the WSI family of RPROMs.

The WS57C191/291 is a High Performance 16K-bit CMOS PROM. It is manufactured in an advanced CMOS EPROM process which enables it to operate at bipolar speeds while consuming only 25% of the power of bipolar.

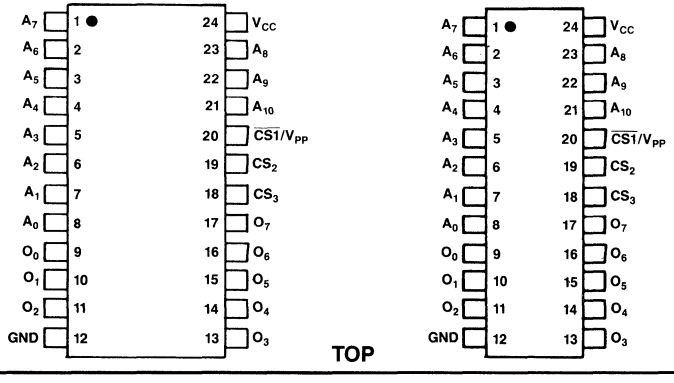
The WS57C191/291's patented CMOS EPROM technology enables the entire memory array to be fully programmed and erased prior to assembly. This capability ensures nearly 100% programming yield. Devices manufactured with other types of technologies utilize various types of fuses which cannot be tested without permanently programming the fuse. This results in a relatively high programming fallout at the packaged level.

Other testability features were designed into the 57C191/291 which enable it to be tested for speed after assembly without programming the memory array. This feature insures that the device will meet all A.C. as well as D.C. data sheet parameters.

Another feature of the WS57C191/291 is its uniquely designed output structure. When compared with other high speed devices, the output structure of the WS57C191/291 virtually eliminates the introduction of switch related noise into the system environment.

The WS75C191/291 is configured in the standard Bipolar PROM pinout. The WS57C191 is offered in a 600 mil wide Dip and the WS57C291 is offered in a 300 mil wide Dip.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191/291-45	WS57C191/291-55
Address Access Time (Max)	45 ns	55 ns
Output Enable Time (Max)	20 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65° C to +150° C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l.	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

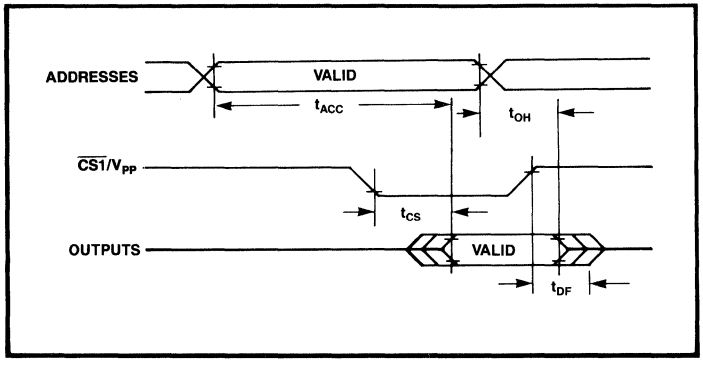
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		20	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		25	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		110	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

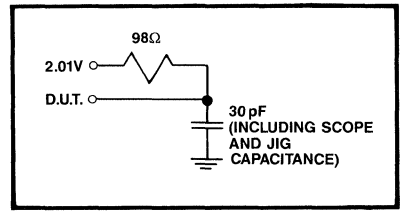
PARAMETER	SYMBOL	WS57C191/291-45		WS57C191/291-55		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		45		55	ns
CS to Output Delay	t_{CS}		20		30	
Output Disable to Output Float	t_{DF}		20		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = -4mA)	V_{OH}	2.4		V

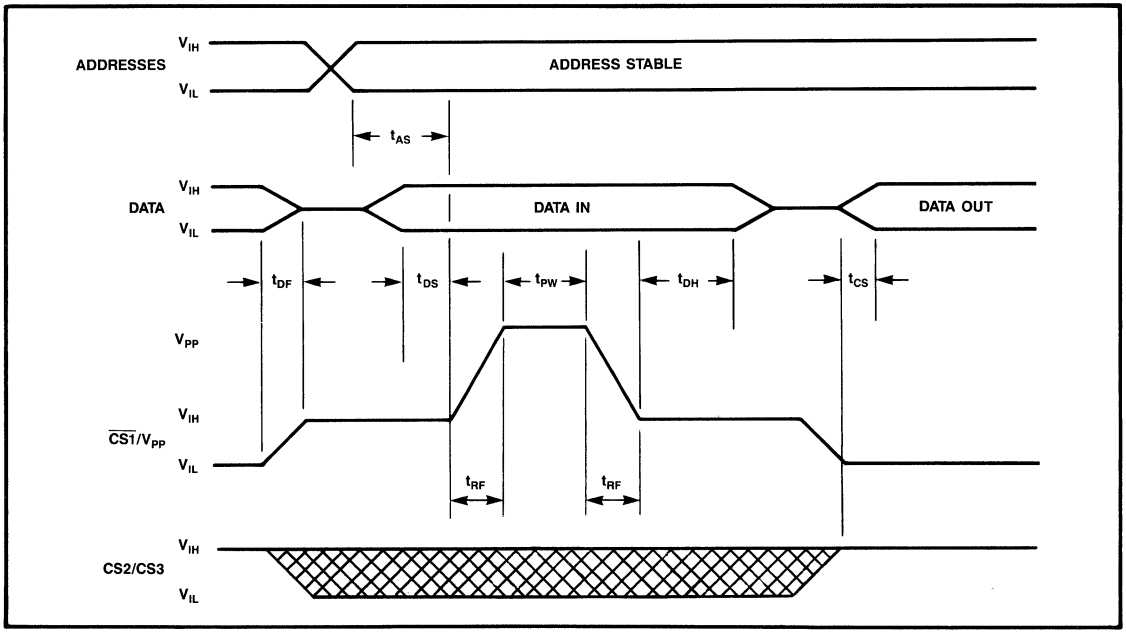
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Set Up	t_{DS}	2			μs
Program Pulse Width (Note 6)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTE: 6) For programmers utilizing a one shot programming pulse, a 10 ms pulse width should be used.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc., the WS57C191/291 has all 2048x8 bits in the "1," or high state. "0's" are loaded into the WS57C191/291 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by temoving the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, family/pinout code 7B/21; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191-45P	45	24 Pin PDIP, 0.6"	P2	Comm'l	Standard
WS57C291-45S	45	24 Pin PDIP, 0.3"	S1	Comm'l	Standard
WS57C191-55P	55	24 Pin PDIP, 0.6"	P2	Comm'l	Standard
WS57C291-55S	55	24 Pin PDIP, 0.3"	S1	Comm'l	Standard

2K × 8 CMOS PROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
  — 225 mW Active Power
- **Fast Programming**
- **Pin Compatible with AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
  — ESD Protection Exceeds 2000V
- **Plastic Dip Package**

GENERAL DESCRIPTION

The WS57C191B/291B is an extremely HIGH PERFORMANCE 16K Electrically Programmable Read Only Memory. It is specifically designed to replace bipolar PROMs in existing applications.

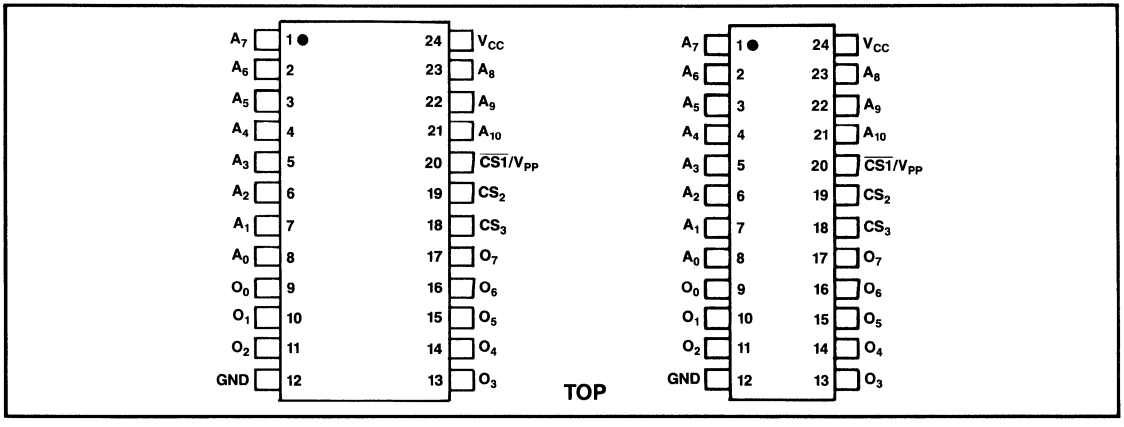
The WS57C191B/291B is manufactured using WSI's patented CMOS EPROM technology. As a result, the entire memory array can be fully programmed and erased prior to assembly. This capability ensures nearly 100% programming yield. Devices manufactured with other types of technologies utilize various types of fuses which cannot be tested without permanently programming the fuse. This results in relatively high programming fallout when compared to a WSI PROM.

Other testability features were designed into the WS57C191B/291B which enable it to be tested for speed after assembly without programming the memory array. This capability insures that the product will meet all A.C. as well as D.C. data sheet parameters.

Another feature of the WS57C191B/291B is its uniquely designed output structure. When compared with other high speed devices, the output structure of the WS57C191B/291B virtually eliminates the introduction of switch related noise into the system environment.

The WS57C191B/291B is configured in the standard Bipolar PROM pinout. The WS57C191B is offered in a 600 mil wide Dip and the WS57C291B is offered in a 300 mil wide Dip.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191B/291B-35	WS57C191B/291B-45
Address Access Time (Max)	45 ns	55 ns
Output Enable Time (Max)	20 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

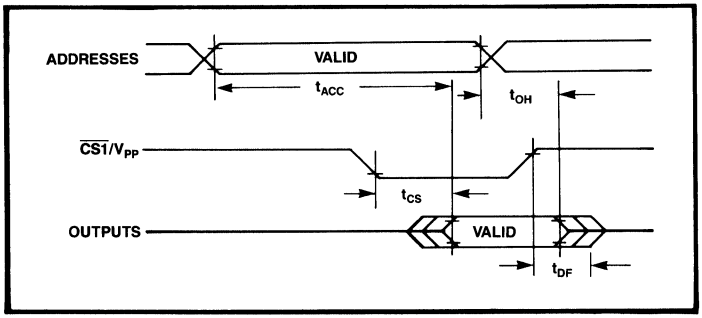
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

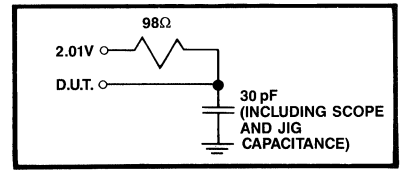
PARAMETER	SYMBOL	WS57C191B/291B-35		WS57C191B/291B-45		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45	ns
CS to Output Delay	t_{CS}		20		20	
Output Disable to Output Float	t_{DF}		20		20	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

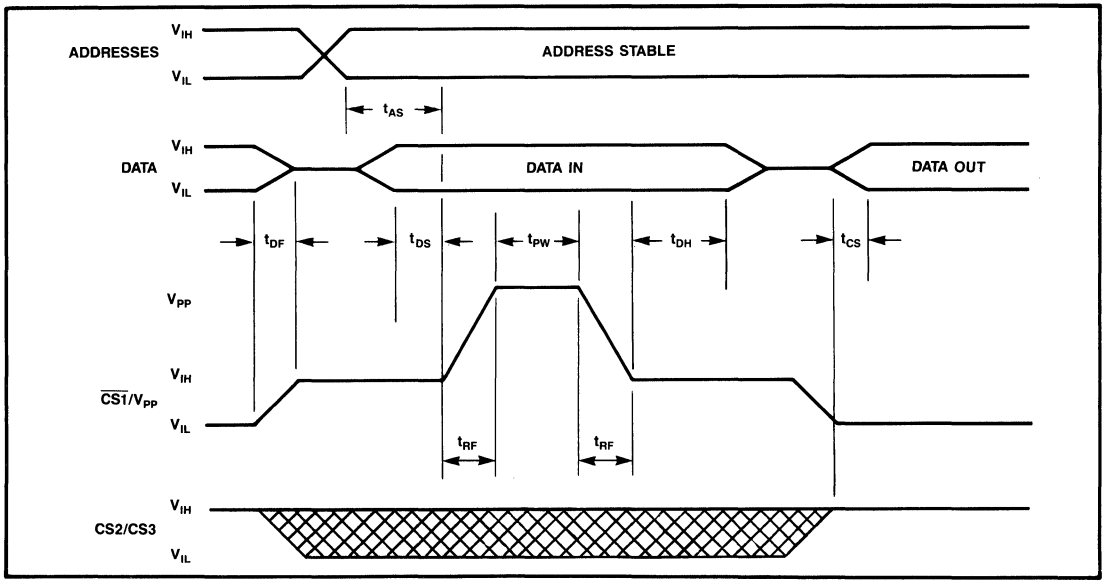
NOTE: 4) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Set Up	t_{DS}				µs
Program Pulse Width (Note 5)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: 5) For programmers utilizing a one shot programming pulse, a 10 ms pulse width should be used.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc., the WS57C191B/291B has all 2048×8 bits in the "1," or high state. "0's" are loaded into the WS57C191B/291B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, family/pinout code 7B/21; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191B-35P	35	24 Pin PDIP, 0.6″	P2	Comm'l	Standard
WS57C291B-35S	35	24 Pin PDIP, 0.3″	S1	Comm'l	Standard
WS57C191B-45P	45	24 Pin PDIP, 0.6″	P2	Comm'l	Standard
WS57C291B-45S	45	24 Pin PDIP, 0.3″	S1	Comm'l	Standard

HIGH-SPEED 2K × 8 REGISTERED CMOS PROM

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 20 ns Setup
  - — 10 ns Clock to Output
- **Low Power Consumption**
  - — 225 mW Active Power
- **Fast Programming**
- **Programmable Synchronous or Asynchronous Output Enable**
- **Pin Compatible with AM27S45 and CY7C245**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Programmable Asynchronous Initialize Register**

2

GENERAL DESCRIPTION

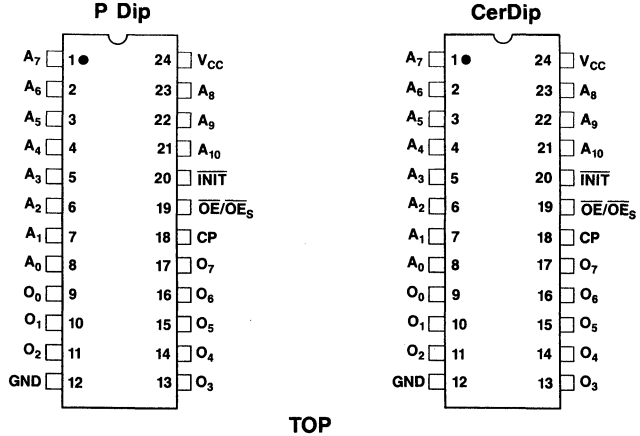
The WS57C45 is an extremely HIGH PERFORMANCE 16K Registered CMOS PROM. It is a direct drop-in replacement for such devices as the AM27S45 and CY7C245.

To meet the requirements of systems which execute and fetch instructions simultaneously, an 8-bit parallel data register has been provided at the output which allows PROM data to be stored while other data is being addressed.

An asynchronous initialization feature has been provided which allows a user programmable 2049th word to be placed on the outputs independent of the system clock. This feature can be used to force an initialize word or provide a preset or clear function.

A further advantage of the WS57C45 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. Unlike devices which cannot be erased, every WS57C45 is 100% tested with worst case test patterns, switching characteristics, and functionality before assembly.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C45-20	WS57C45-25	WS57C45-35
Address Access Time (Max)	20 ns	25 ns	35 ns
Output Enable Time (Max)	10 ns	12 ns	15 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

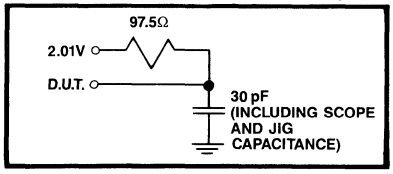
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		30	mA
			Military		35	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 3 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C45-20		WS57C45-25		WS57C45-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Setup to Clock HIGH	t_{SA}	20		25		35		ns
Address Hold From Clock HIGH	t_{HA}	0		0		0		
Clock HIGH to Valid Output	t_{CO}		10		12		15	
Clock Pulse Width	t_{PWC}	12		15		20		
$\overline{OE}_S$ Setup to Clock HIGH	t_{SOES}	10		12		15		
$\overline{OE}_S$ Hold From Clock HIGH	t_{HOES}	5		5		5		
Delay From $\overline{INIT}$ to Valid Output	t_{DI}		20		20		20	
$\overline{INIT}$ Recovery to Clock HIGH	t_{RI}	15		15		20		
$\overline{INIT}$ Pulse Width	t_{PWI}	15		15		20		
Active Output From Clock HIGH	t_{LZC}		15		15		20	
Inactive Output From Clock HIGH	t_{HZC}		15		15		20	
Active Output From $\overline{OE}$ LOW	t_{LZOE}		15		15		20	
Inactive Output From $\overline{OE}$ HIGH	t_{HZOE}		15		15		20	

TEST LOAD (High Impedance Systems)

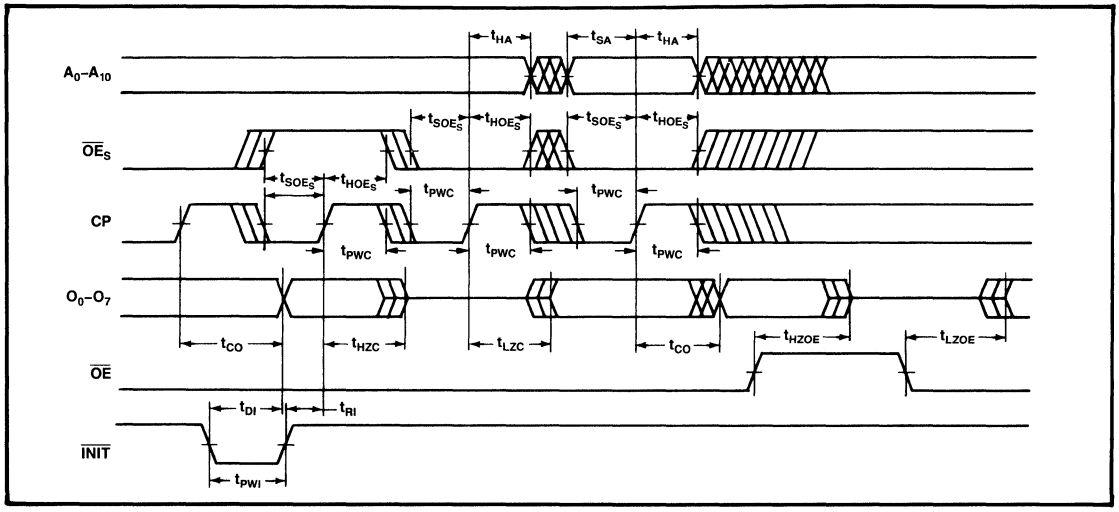


TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

AC READ TIMING DIAGRAM



PROGRAMMERS

Data I/O Unipak 2 or 2B; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C45-20S	20	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS57C45-20K	20	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS57C45-25S	25	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS57C45-25K	25	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS57C45-25KMB	25	24 Pin CERDIP, 0.3″	K1	Military	MIL-STD-883C
WS57C45-35S	35	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS57C45-35K	35	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS57C45-35KMB	35	24 Pin CERDIP, 0.3″	K1	Military	MIL-STD-883C

4K × 8 CMOS PROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
  — 300 mW Active Power (20 MHz)
- **Fast Programming**
- **Pin Compatible with AM27S43 and N82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Available in 300 Mil Dip**

GENERAL DESCRIPTION

The WS57C43B is now available as a PROM. It utilizes the same design as the previously released RPROM™ from WSI. The difference is the PROM version is available in plastic packages and is not re-programmable. The plastic packaging is ideal for high volume applications which require automatic insertion. The plastic packaging also provides an economic benefit when compared to a windowed cerdip package. For applications requiring reprogrammability, contact your WSI sales representative for information on the WSI family of RPROMs.

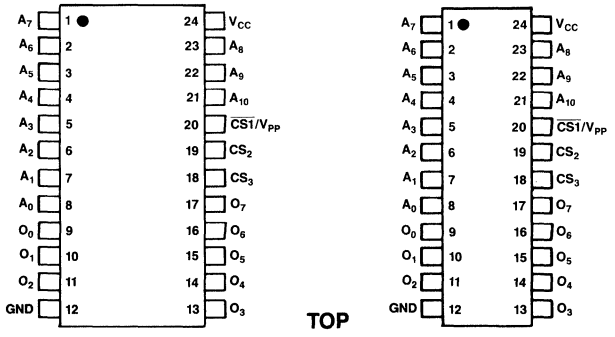
The WS57C43B is a High Performance 32K-bit CMOS PROM. It is manufactured in an advanced CMOS EPROM process which enables it to operate at bipolar speeds while consuming only 25% of the power of bipolar.

The WS57C43B's patented CMOS EPROM technology enables the entire memory array to be fully programmed and erased prior to assembly. This capability ensures nearly 100% programming yield. Devices manufactured with other types of technologies utilize various types of fuses which cannot be tested without permanently programming the fuse. This results in a relatively high programming fallout at the packaged level.

Other testability features were designed into the WS57C43B which enable it to be tested for speed after assembly without programming the memory array. This feature insures that the product will meet all A.C. as well as D.C. data sheet parameters.

The WS57C43B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs. It also uses the same programming algorithm as its predecessor the WS57C43.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C43B-35	WS57C43B-45	WS57C43B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	25 ns	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

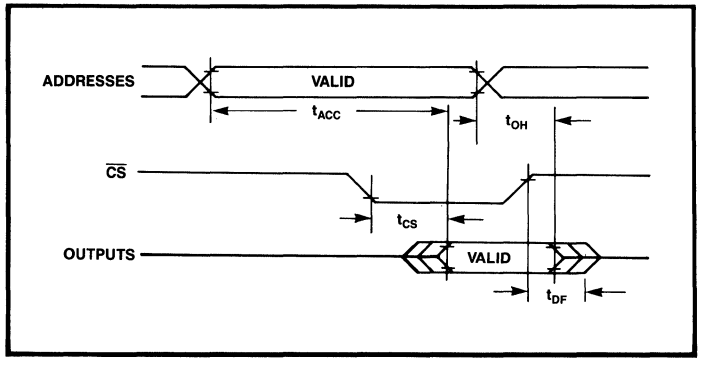
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

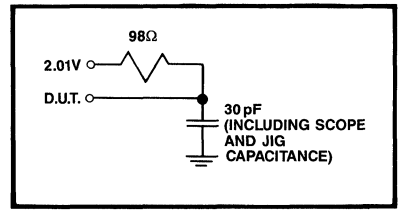
PARAMETER	SYMBOL	WS57C43B-35		WS57C43B-45		WS57C43B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
CS to Output Delay	t_{CS}		20		25		25	
Output Disable to Output Float	t_{DF}		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		30	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = -4mA)	V_{OH}	2.4		V

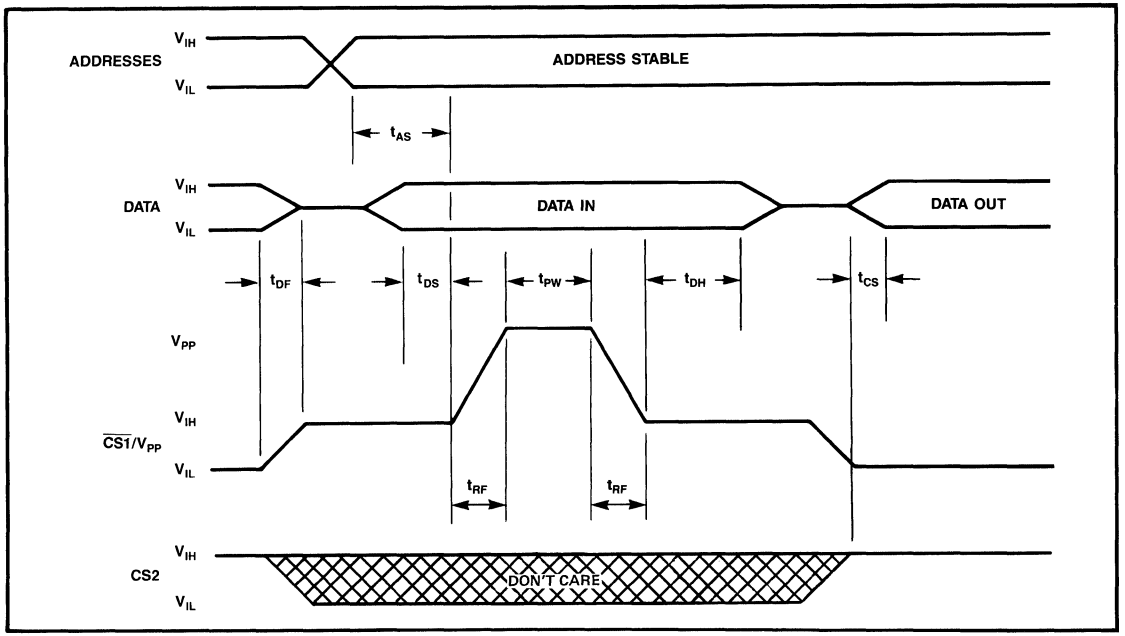
NOTES: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Set Up	t_{DS}	2			μs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTES: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc., the WS57C43B has all 4096 × 8 bits in the "1," or high state. "0's" are loaded into the WS57C43B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 11 or later, family/pinout code 7B/63; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43B-35S	35	24 Pin PDIP, 0.3″	S1	Comm'l	Standard
WS57C43B-35P	35	24 Pin PDIP, 0.6″	P2	Comm'l	Standard
WS57C43B-45S	45	24 Pin PDIP, 0.3″	S1	Comm'l	Standard
WS57C43B-45P	45	24 Pin PDIP, 0.6″	P2	Comm'l	Standard
WS57C43B-55S	55	24 Pin PDIP, 0.3″	S1	Comm'l	Standard
WS57C43B-55P	55	24 Pin PDIP, 0.6″	P2	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

8K x 8 CMOS PROM

KEY FEATURES

- **Very-Fast Access Time**
  — 55 ns
- **Low Power Consumption**
  — 300 mW Active Power (Full Speed)
- **Fast Programming**
- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
  — ESD Protection Exceeds 2000V
- **Plastic Dip Package**

GENERAL DESCRIPTION

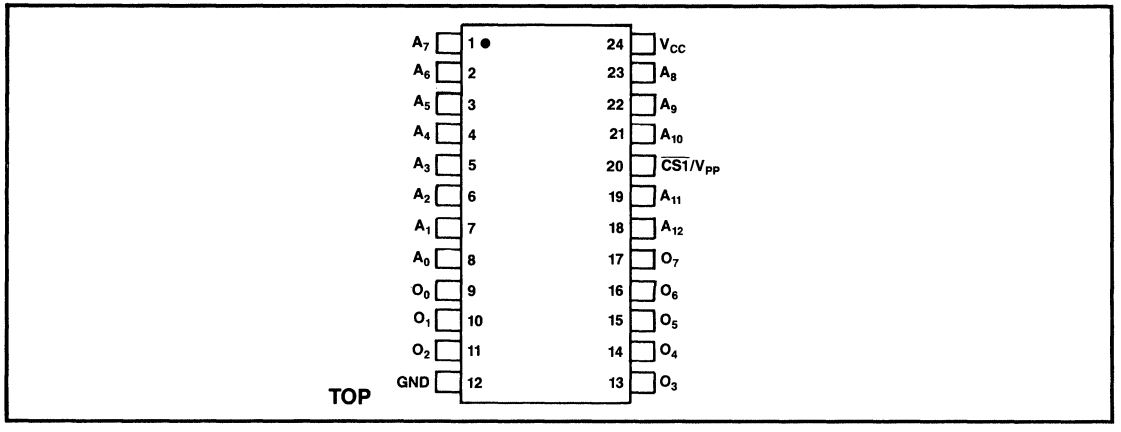
The WS57C49 is an extremely HIGH PERFORMANCE 64K Electrically Programmable Read Only Memory. It is specifically designed to replace bipolar PROMs in existing applications.

The WS57C49 is manufactured using WSI's patented CMOS EPROM technology. As a result, the entire memory array can be fully programmed and erased prior to assembly. This capability ensures nearly 100% programming yield. Devices manufactured with other types of technologies utilize various types of fuses which cannot be tested without permanently programming the fuse. This results in relatively high programming fallout when compared to a WSI PROM.

Other testability features were designed into the WS57C49 which enable it to be tested for speed after assembly without programming the memory array. This capability insures that the product will meet all A.C. as well as D.C. data sheet parameters.

The WS57C49 is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49-55	WS57C49-70
Address Access Time (Max)	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

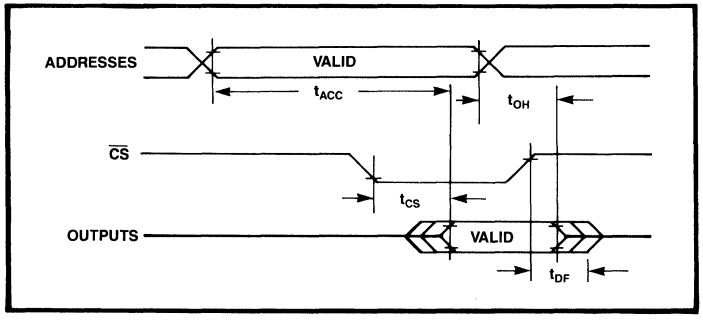
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		20	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		25	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

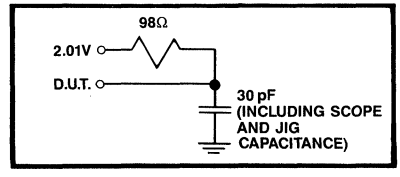
PARAMETER	SYMBOL	WS57C49-55		WS57C49-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
CS to Output Delay	t_{CS}		20		25	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} +0.3	V
Output Low Voltage During Verify (I_{OL} = 16 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4 mA)	V_{OH}	2.4		V

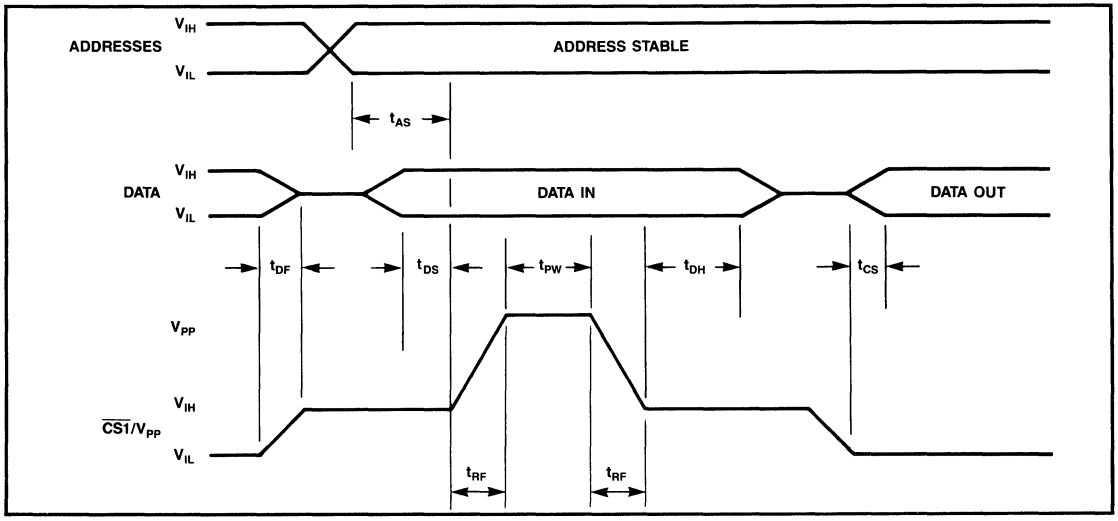
NOTE: 4) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Chip Disable Setup Time	t_{DF}			30	ns
Data Set Up	t_{DS}	2			µs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			µs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			µs

NOTE: Single shot programming algorithms should use one 10 ms pulse per word.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc., the WS57C49 has all 8192×8 bits in the "1," or high state. "0's" are loaded into the WS57C49 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 3C/67; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49-55P	55	24 Pin PDIP, 0.6"	P2	Comm'l	Standard
WS57C49-70P	70	24 Pin PDIP, 0.6"	P2	Comm'l	Standard

8K × 8 CMOS PROM

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
  — 300 mW Active Power (20 MHz)
- **Fast Programming**
- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Available in 300 Mil Dip**

GENERAL DESCRIPTION

The WS57C49B is now available as a PROM. It utilizes the same design as the previously released RPROM™ from WSI. The difference is the PROM version is available in plastic packages and is not re-programmable. The plastic packaging is ideal for high volume applications which require automatic insertion. The plastic packaging also provides an economic benefit when compared to a windowed cerdip package. For applications requiring reprogrammability, contact your WSI sales representative for information on the WSI family of RPROMs.

The WS57C49B is a High Performance 64K-bit CMOS PROM. It is manufactured in an advanced CMOS EPROM process which enables it to operate at bipolar speeds while consuming only 25% of the power of bipolar.

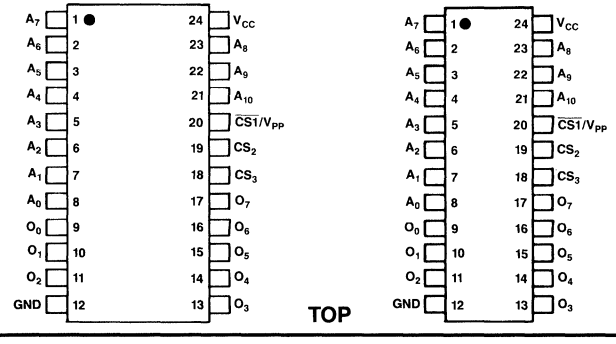
The WS57C49B's patented CMOS EPROM technology enables the entire memory array to be fully programmed and erased prior to assembly. This capability ensures nearly 100% programming yield. Devices manufactured with other types of technologies utilize various types of fuses which cannot be tested without permanently programming the fuse. This results in a relatively high programming fallout at the packaged level.

Other testability features were designed into the WS57C49B which enable it to be tested for speed after assembly without programming the memory array. This capability insures that the device will meet all A.C. as well as D.C. data sheet parameters.

Another feature of the WS57C49B is its uniquely designed output structure. When compared with other high-speed devices, the output structure of the WS57C49B virtually eliminates the introduction of switch-related noise into the system environment.

The WS57C49B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C49B-35	WS57C49B-45
Address Access Time (Max)	35 ns	45 ns
Output Enable Time (Max)	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65° C to +150° C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

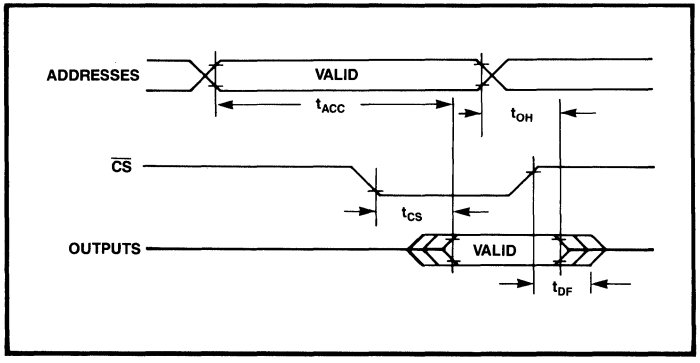
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

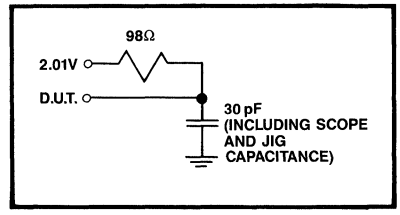
PARAMETER	SYMBOL	WS57C49B-35		WS57C49B-45		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20	
Output Disable to Output Float	t_{DF}		20		20	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

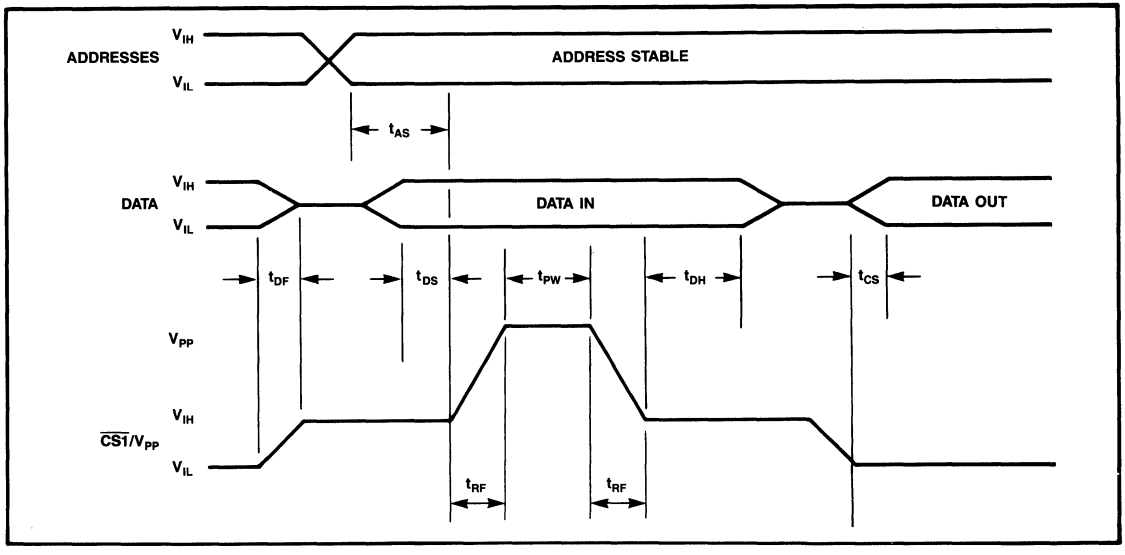
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5° C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup	t_{DS}	2			μs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{pp} Rise and Fall Time	t_{RF}	1			μs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc., the WS57C49B has all 8192 x 8 bits in the "1," or high state. "0's" are loaded into the WS57C49B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 3C/67; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49B-35S	35	24 Pin PDIP, 0.3"	S1	Comm'l	Standard
WS57C49B-35P	35	24 Pin PDIP, 0.6"	P2	Comm'l	Standard
WS57C49B-45S	45	24 Pin PDIP, 0.3"	S1	Comm'l	Standard
WS57C49B-45P	45	24 Pin PDIP, 0.6"	P2	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

RE-PROGRAMMABLE MEMORY PRODUCTS

RPROM Memory:

EPROM Memory (×8):

EPROM Memory (×16):

Mappable Memory Products:

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 2K × 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 45 ns
- **Low Power Consumption**
  — 225 mW Active Power
- **Fast Programming**
- **Pin Compatible With AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

3

GENERAL DESCRIPTION

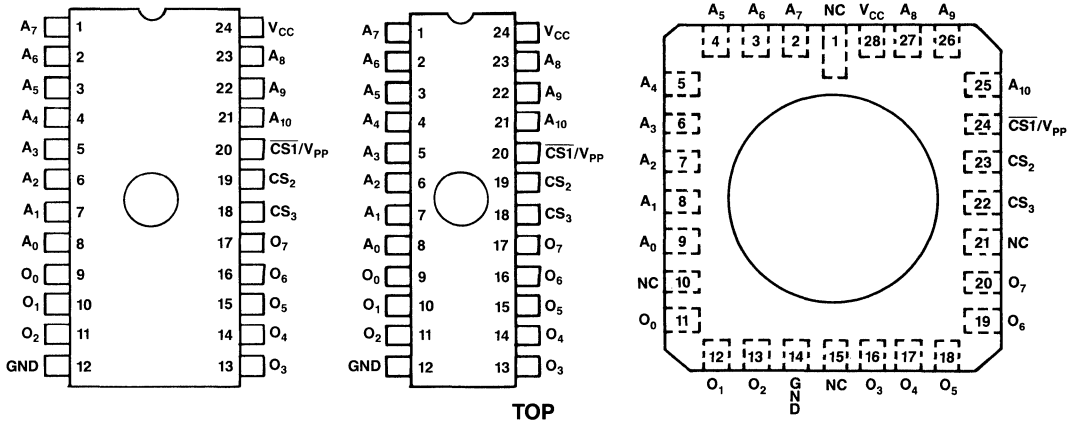
The WS57C191/291 is an extremely HIGH PERFORMANCE 16K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power of its Bipolar counterparts.

A further advantage of the WS57C191/291 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C191/291 is 100% tested with worst case test patterns both before and after assembly.

Another feature of the WS57C191/291 is its uniquely designed output structure. When compared with other high speed devices, the output structure of the WS57C191/291 virtually eliminates the introduction of switch related noise into the system environment.

The WS57C191/291 is configured in the standard Bipolar PROM pinout. The WS57C191 is offered in a 600 mil wide Dip and the WS57C291 is offered in a 300 mil wide Dip. Both are offered in a Leadless Ceramic Chip Carrier.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191/291-45	WS57C191/291-55
Address Access Time (Max)	45 ns	55 ns
Output Enable Time (Max)	20 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

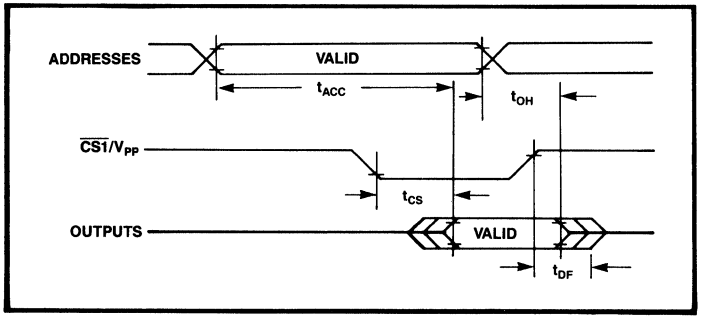
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		20	mA
			Military		30	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		25	
			Military		35	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

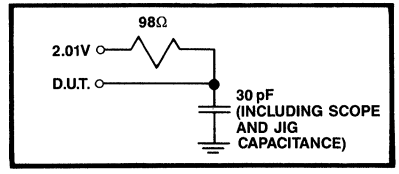
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C191/291-45		WS57C191/291-55		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		45		55	ns
CS to Output Delay	t_{CS}		20		30	
Output Disable to Output Float	t_{DF}		20		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = -4mA)	V_{OH}	2.4		V

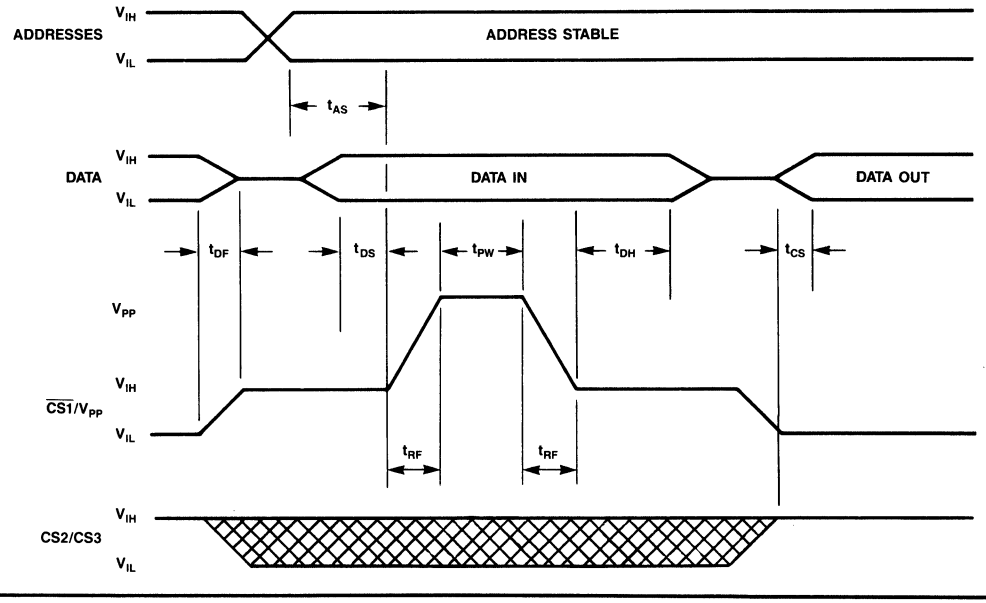
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Set Up	t_{DS}				μs
Program Pulse Width (Note 6)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTE: 6) For programmers utilizing a one shot programming pulse, a 10 ms pulse width should be used.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C191/291 has all 2048 x 8 Bits in the "1," or high state. "0's" are loaded into the WS57C191/291 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

PROGRAMMERS

Data I/O Unipak 2 or 2B, family/pinout code 7B/21; WSI's MagicPro™ IBM PC Compatible Engineering Program.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C191/291 to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase a WS57C191/291.

This dosage can be obtained by exposure to an ultra-violet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000µ W/cm^2 for 15 to 20 minutes. The WS57C191/291 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C191/291 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C191/291 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191-45D	45	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C291-45T	45	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C191-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C291-55T	55	24 Pin CERDIP, 0.3"	T1	Comm'l	Standard
WS57C191-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191-55DMB	55	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C
WS57C291-55TMB	55	24 Pin CERDIP, 0.3"	T1	Military	MIL-STD-883C

HIGH SPEED 2K × 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
  — 300 mW Active Power
- **Fast Programming**
- **Pin Compatible with AM27S191/291 and N82S191 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

3

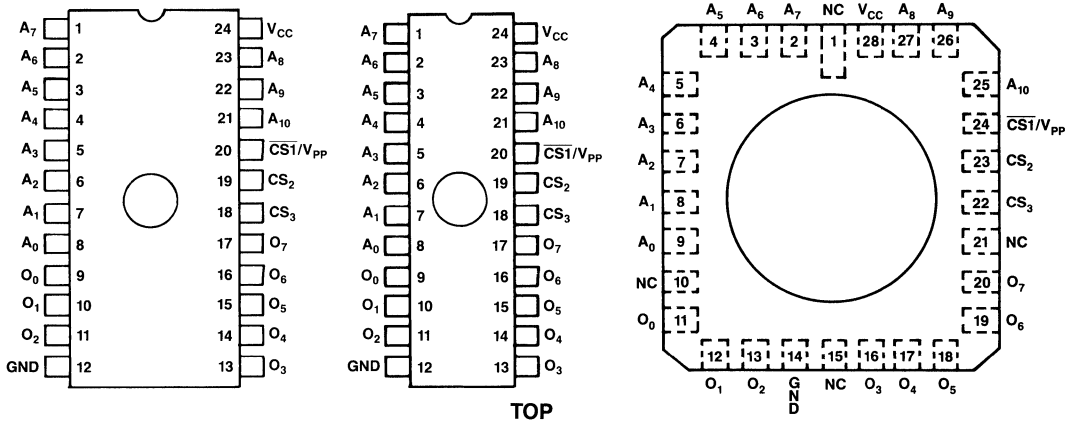
GENERAL DESCRIPTION

The WS57C191B/291B is an extremely HIGH PERFORMANCE 16K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power of its Bipolar counterparts.

A further advantage of the WS57C191B/291B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C191B/291B is 100% tested with worst case test patterns both before and after assembly.

The WS57C191B/291B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C191B/291B-35	WS57C191B/291B-45
Address Access Time (Max)	35 ns	45 ns
Output Enable Time (Max)	20 ns	20 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

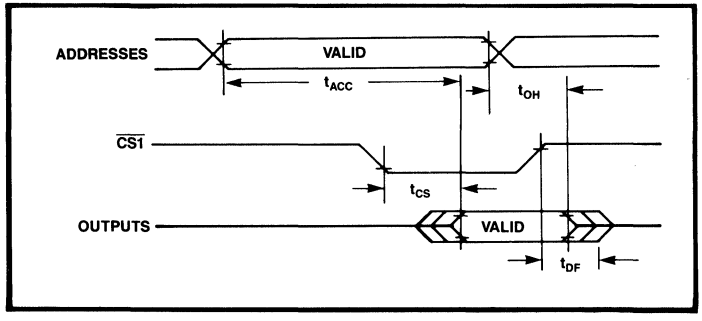
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		30	mA
			Military		35	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 3 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.

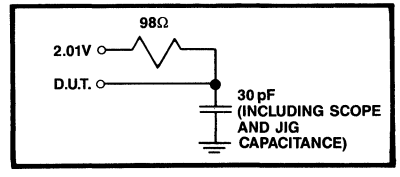
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C191B/291B-35		WS57C191B/291B-45		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45	ns
$\overline{CS}$ to Output Delay	t_{CE}		20		20	
Output Disable to Output Float	t_{DF}		20		20	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

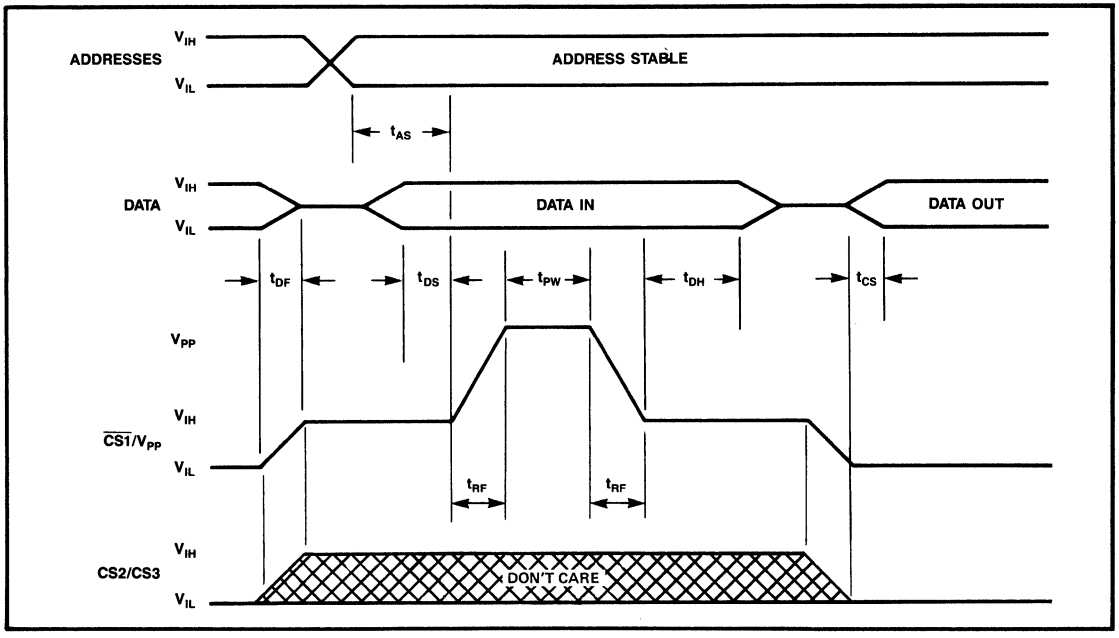
NOTES: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}	2		30	ns
Data Set Up	t_{DS}				μs
Program Pulse Width (Note 6)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTES: 6) For programmers utilizing a one shot programming pulse, a 10ms pulse width should be used.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C191B/291B has all 2048×8 bits in the "1," or high state. "0's" are loaded into the WS57C191B/291B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS}1/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C191B/291B to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C191B/291B. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 15 or 20 minutes. The WS57C191B/291B should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C191B/291B and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C191B/291B and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 7B/21; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C191B-35D	35	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C291B-35T	35	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C191B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C191B-45D	45	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C191B-45DMB	45	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C291B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C291B-45T	45	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS59C291B-45TMB	45	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C

HIGH-SPEED 2K × 8 REGISTERED CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  - — 20 ns Setup
  - — 10 ns Clock to Output
- **Low Power Consumption**
  - — 225 mW Active Power
- **Fast Programming**
- **Programmable Synchronous or Asynchronous Output Enable**
- **Pin Compatible with AM27S45 and CY7C245**
- **Immune to Latch-Up**
  - — Up to 200 mA
- **ESD Protection Exceeds 2000V**
- **Programmable Asynchronous Initialize Register**

3

GENERAL DESCRIPTION

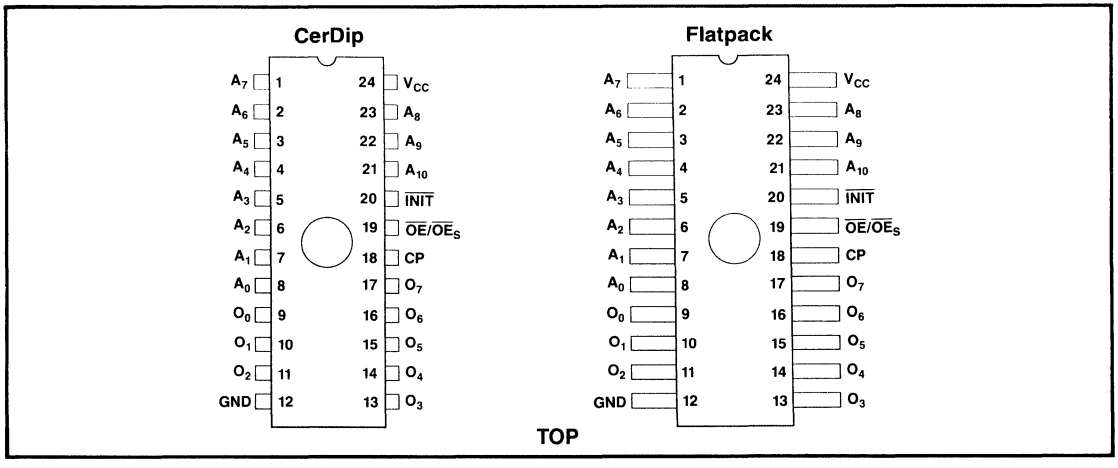
The WS57C45 is an extremely HIGH PERFORMANCE 16K UV Erasable Registered CMOS RPROM. It is a direct drop-in replacement for such devices as the AM27S45 and CY7C245.

To meet the requirements of systems which execute and fetch instructions simultaneously, an 8-bit parallel data register has been provided at the output which allows RPROM data to be stored while other data is being addressed.

An asynchronous initialization feature has been provided which allows a user programmable 2049th word to be placed on the outputs independent of the system clock. This feature can be used to force an initialize word or provide a preset or clear function.

A further advantage of the WS57C45 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C45 is 100% tested with worst case test patterns both before and after assembly.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C45-20	WS57C45-25	WS57C45-35
Address Access Time (Max)	20 ns	25 ns	35 ns
Output Enable Time (Max)	10 ns	12 ns	15 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

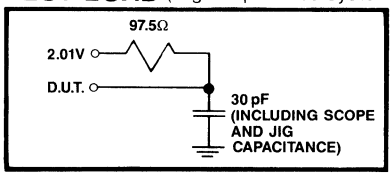
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		20	mA
			Military		30	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 4	Comm'l.		25	
			Military		35	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or Vcc ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 2 mAMHz.
4) A.C. Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C45-20		WS57C45-25		WS57C45-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address Setup to Clock HIGH	t_{SA}	20		25		35		ns
Address Hold From Clock HIGH	t_{HA}	0		0		0		
Clock HIGH to Valid Output	t_{CO}		10		12		15	
Clock Pulse Width	t_{PWC}	12		15		20		
$\overline{OE}_S$ Setup to Clock HIGH	t_{SOES}	10		12		15		
$\overline{OE}_S$ Hold From Clock HIGH	t_{HOES}	5		5		5		
Delay From $\overline{INIT}$ to Valid Output	t_{DI}		20		20		20	
$\overline{INIT}$ Recovery to Clock HIGH	t_{RI}	15		15		20		
$\overline{INIT}$ Pulse Width	t_{PWI}	15		15		20		
Active Output From Clock HIGH	t_{LZC}		15		15		20	
Inactive Output From Clock HIGH	t_{HZC}		15		15		20	
Active Output From $\overline{OE}$ LOW	t_{LZOE}		15		15		20	
Inactive Output From $\overline{OE}$ HIGH	t_{HZOE}		15		15		20	

TEST LOAD (High Impedance Systems)

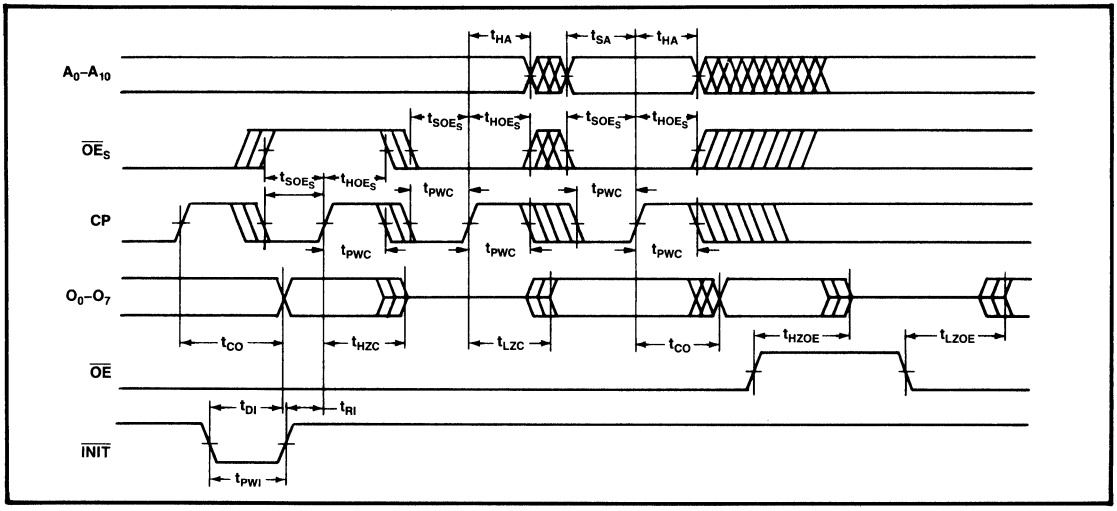


TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

AC READ TIMING DIAGRAM



ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C45 to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C45. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WS57C45 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C45 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C45 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C45-20T	20	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C45-25FMB	25	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C45-25T	25	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C45-25TMB	25	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C
WS57C45-35FMB	35	24 Pin Ceramic Flatpack	F1	Military	MIL-STD-883C
WS57C45-35T	35	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C45-35TMB	35	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 4K x 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 55 ns
- **Low Power Consumption**
  — 225 mW Active Power
- **Fast Programming**
- **Pin Compatible with AM27S43, MB7142 and 82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

3

GENERAL DESCRIPTION

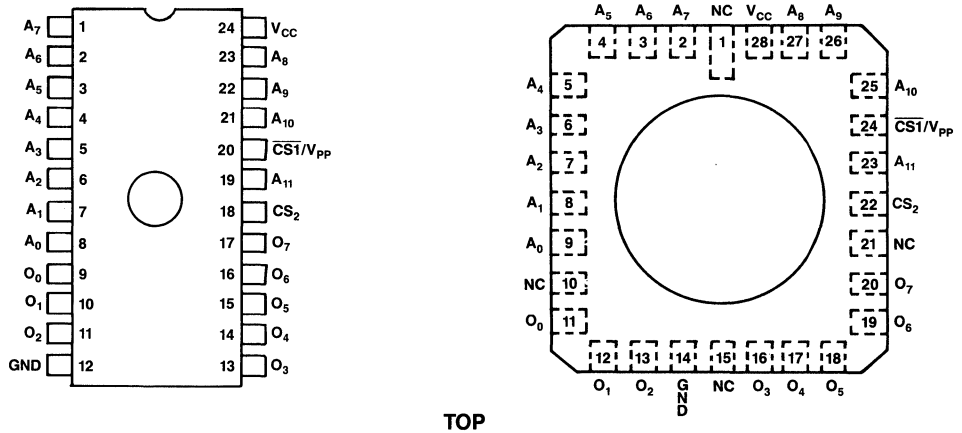
The WS57C43 is an extremely HIGH PERFORMANCE 32K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power of its Bipolar counterparts.

A further advantage of the WS57C43 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C43 is 100% tested with worst case test patterns both before and after assembly.

Another feature of the WS57C43 is its uniquely designed output structure. When compared with other high speed devices, the output structure of the WS57C43 virtually eliminates the introduction of switch related noise into the system environment.

The WS57C43 is configured in the standard Bipolar PROM pinout. Packaging options include both 300 and 600 mil wide Dips as well as a Leadless Chip Carrier.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C43-55	WS57C43-70
Address Access Time (Max)	55ns	70ns
Output Enable Time (Max)	25ns	30ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

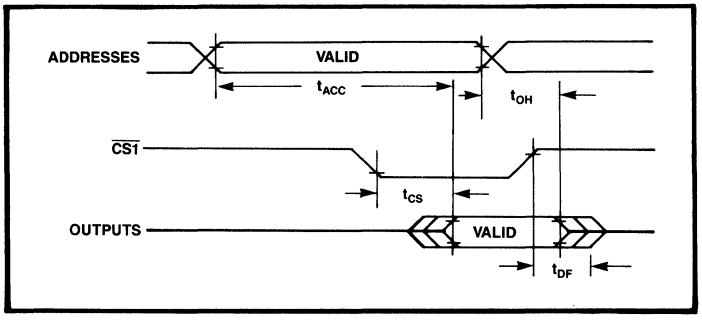
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		20	mA
			Military		30	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		25	
			Military		35	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

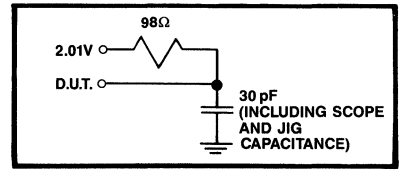
AC READ CHARACTERISTICS Over operating Range. (See above)

PARAMETER	SYMBOL	WS57C43-55		WS57C43-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		25		30	
Output Disable to Output Float	t_{DF}		25		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{pp} = 13.5 ± 0.5V)

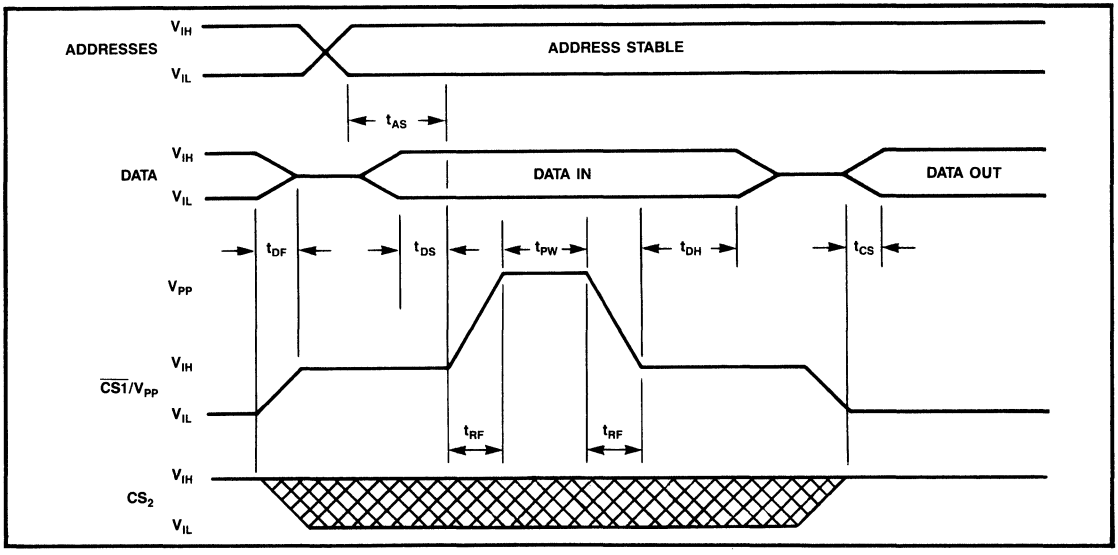
PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = -4mA)	V_{OH}	2.4		V

NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Address Setup Time	t_{AS}	2		μS
Chip Disable Setup Time	t_{DF}		30	ns
Data Setup	t_{DS}	2		μS
Program Pulse Width	t_{PW}	5		ms
Data Hold Time	t_{DH}	2		μS
Chip Select Delay	t_{CS}		30	ns
V_{pp} Rise and Fall Time	t_{RF}	1		μS

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C43 has all 4096x8 bits in the "1," or high state. "0's" are loaded into the WS57C43 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C43 to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C43. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WS57C43 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C43 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C43 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43-55D	55	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C43-55T	55	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C43-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C43-70D	70	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C43-70DM	70	24 Pin CERDIP, 0.6″	D1	Military	Standard
WS57C43-70DMB	70	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C43-70T	70	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C43-70TM	70	24 Pin CERDIP, 0.3″	T1	Military	Standard
WS57C43-70TMB	70	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C

HIGH SPEED 4K × 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
  — 300 mW Active Power (20 MHz)
- **Fast Programming**
- **Pin Compatible with AM27S43 and N82S321 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Available in 300 Mil Dip**

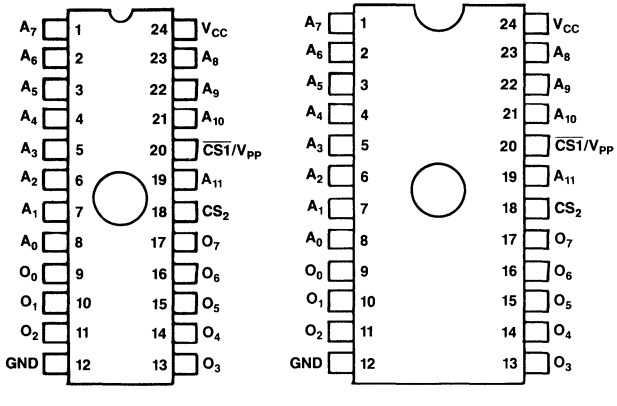
GENERAL DESCRIPTION

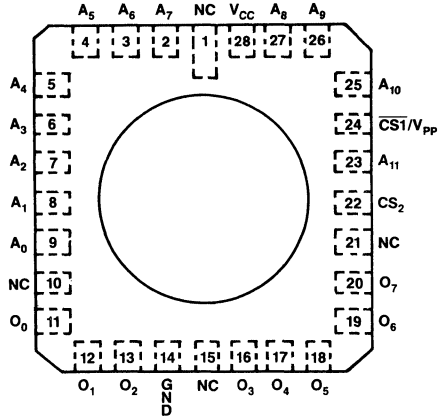
The WS57C43B is an extremely HIGH PERFORMANCE 32K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C43B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C43B is 100% tested with worst case test patterns both before and after assembly.

The WS57C43B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs. It also uses the same programming algorithm as its predecessor the WS57C43.

PIN CONFIGURATION





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PRODUCT SELECTION GUIDE

PARAMETER	WS57C43B-35	WS57C43B-45	WS57C43B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

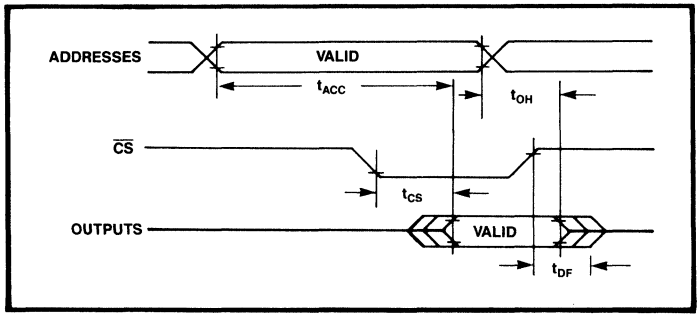
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		30	mA
			Military		35	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 3 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.

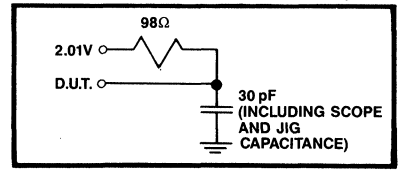
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C43B-35		WS57C43B-45		WS57C43B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
CS to Output Delay	t_{CS}		20		25		25	
Output Disable to Output Float	t_{DF}		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		30	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

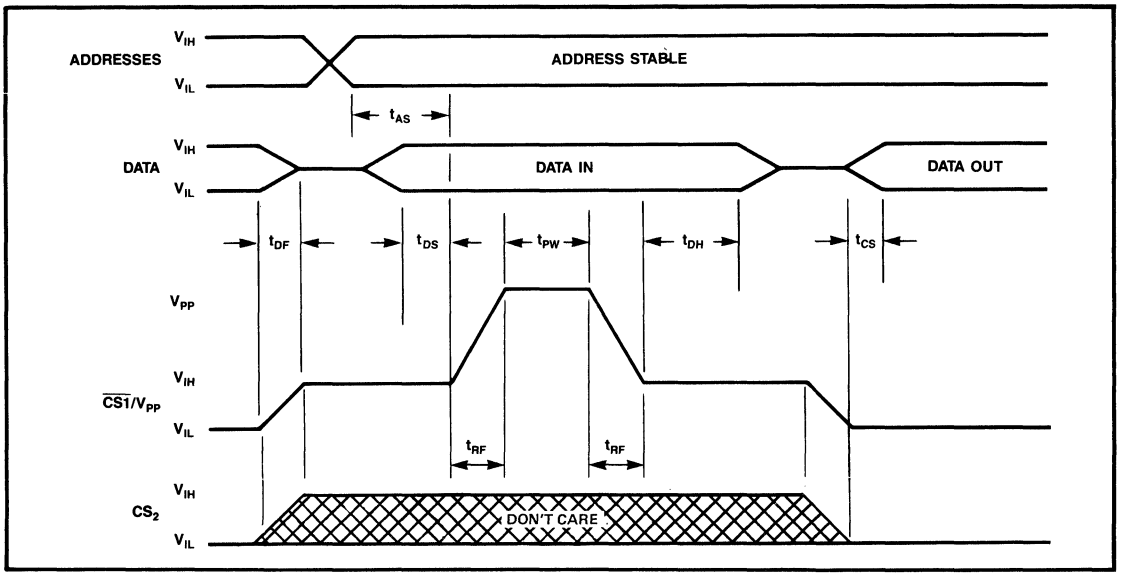
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup	t_{DS}	2			μs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{pp} Rise and Fall Time	t_{RF}	1			μs

NOTE: A single shot programming algorithm should use one 10ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C43B has all 4096×8 bits in the "1," or high state. "0's" are loaded into the WS57C43B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS}1/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C43B to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C43B. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 15 to 20 minutes. The WS57C43B should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C43B and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C43B and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 11 or later, family/pinout code 7B/63; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C43B-35D	35	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C43B-35T	35	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C43B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C43B-45D	45	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C43B-45DMB	45	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C43B-45T	45	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C43B-45TMB	45	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C
WS57C43B-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C43B-55D	55	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C43B-55DMB	55	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C43B-55T	55	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C43B-55TMB	55	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 8K x 8 CMOS RPROM™

KEY FEATURES

- **Very-Fast Access Time**
  — 55 ns
- **Low Power Consumption**
  — 300 mW Active Power (Full Speed)
- **Fast Programming**
- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **Commercial and Military Availability**

3

GENERAL DESCRIPTION

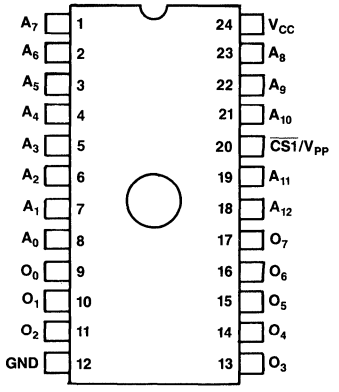
The WS57C49 is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Re-Programmable Read Only Memory. It is specifically designed to replace bipolar PROMs in existing applications.

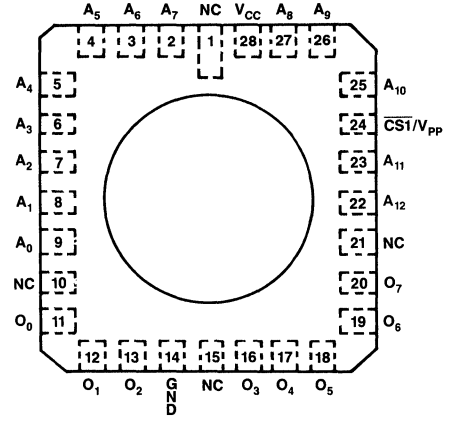
An advantage of the WS57C49 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49 is 100% tested with worst case test patterns both before and after assembly.

The WS57C49 is manufactured using WSI's patented CMOS EPROM technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

The WS57C49 is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

PIN CONFIGURATION





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PRODUCT SELECTION GUIDE

PARAMETER	WS57C49-55	WS57C49-70
Address Access Time (Max)	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

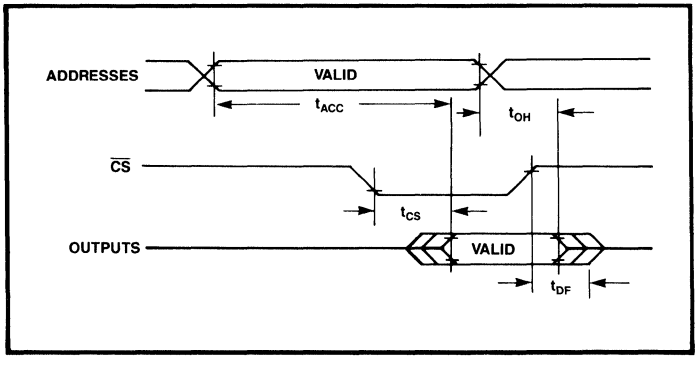
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		20	mA
			Military		30	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		25	
			Military		35	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) AC Power component adds 3 mA/MHz.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

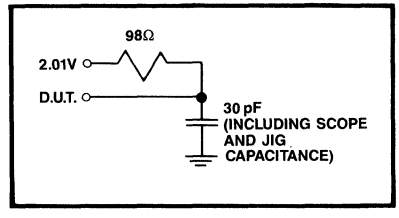
PARAMETER	SYMBOL	WS57C49-55		WS57C49-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		25	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

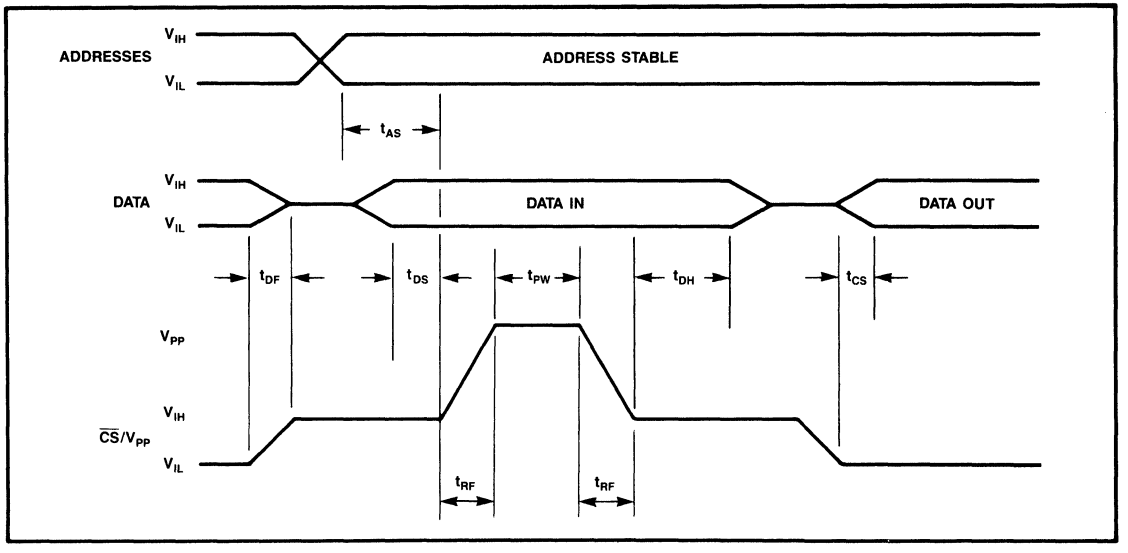
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5° C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup	t_{DS}	2			μs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTE: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C49 has all 8192x8 bits in the "1," or high state. "0's" are loaded into the WS57C49 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C49 to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C49. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WS57C49 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C49 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C49 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 3C/67; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49-55D	55	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49-70CMB	70	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49-70D	70	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49-70DMB	70	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C

HIGH SPEED 8K x 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 35 ns
- **Low Power Consumption**
  — 300 mW Active Power (20 MHz)
- **Fast Programming**
- **Pin Compatible with AM27S49 and MB7144 Bipolar PROMs**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

3

GENERAL DESCRIPTION

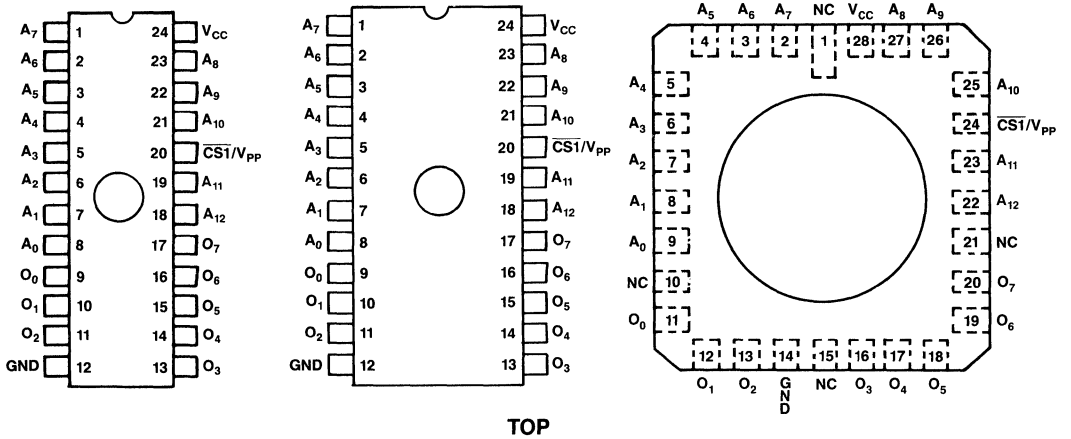
The WS57C49B is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C49B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C49B is 100% tested with worst case test patterns both before and after assembly.

A unique feature of the WS57C49B is a designed-in output hold from address change. This allows the WS57C49B to be run at a cycle time equal to the address access time. While addresses are changing, output data is held long enough to be latched into external circuitry.

The WS57C49B is configured in the standard Bipolar PROM pinout which provides an easy upgrade path for systems which are currently using Bipolar PROMs.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C49B-35	WS57C49B-45	WS57C49B-55
Address Access Time (Max)	35 ns	45 ns	55 ns
Output Enable Time (Max)	20 ns	25 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65° C to +150° C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70° C	+5V ± 5%
Military	−55° to +125° C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See above)

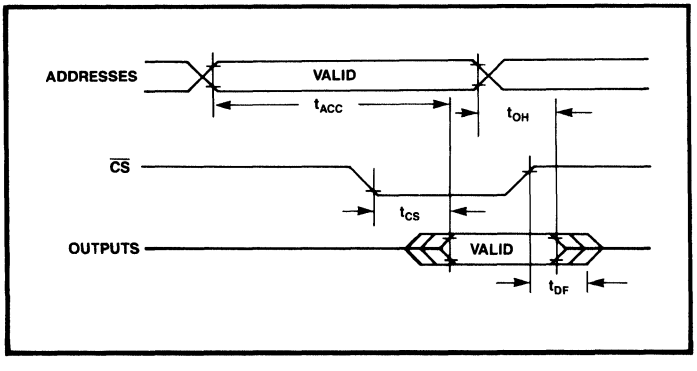
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA		2.4		
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l.		30	mA
			Military		35	
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l.		40	
			Military		40	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 3 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.

AC READ CHARACTERISTICS Over Operating Range. (See Above)

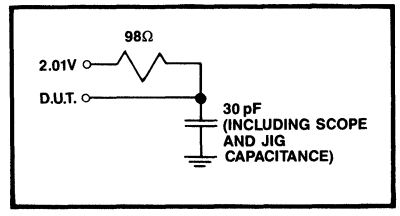
PARAMETER	SYMBOL	WS57C49B-35		WS57C49B-45		WS57C49B-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45		55	ns
CS to Output Delay	t_{CS}		20		25		25	
Output Disable to Output Float	t_{DF}		20		25		25	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		35	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

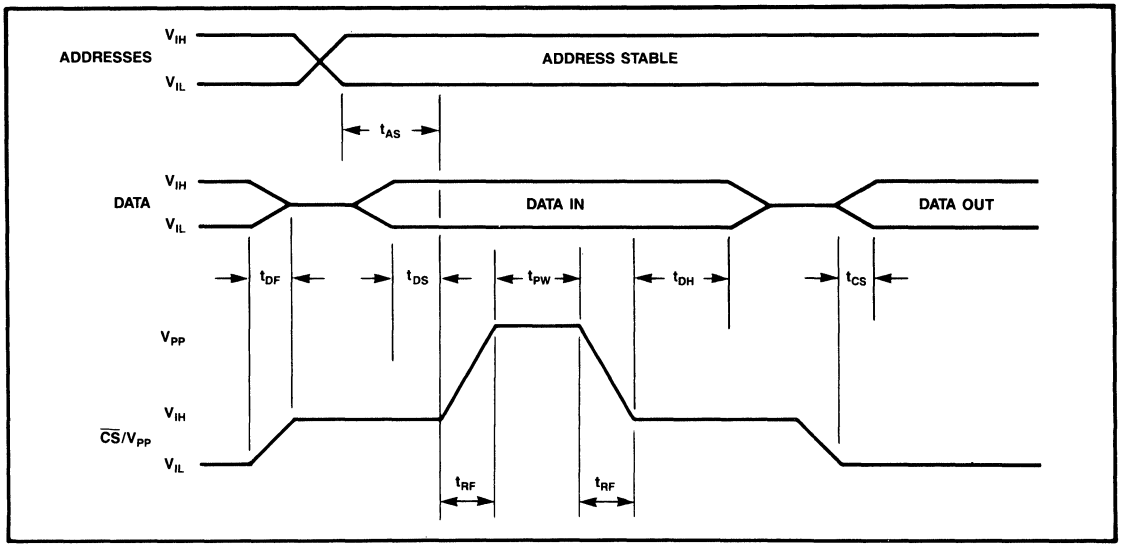
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5° C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup	t_{DS}	2			μs
Program Pulse Width	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{pp} Rise and Fall Time	t_{RF}	1			μs

NOTES: A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C49B has all 8192×8 bits in the "1," or high state. "0's" are loaded into the WS57C49B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.5V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS}1/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C49B to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C49B. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 15 to 20 minutes. The WS57C49B should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C49B and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C49B and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 3C/67; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C49B-35D	35	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49B-35T	35	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-45CMB	45	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-45D	45	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C49B-45DMB	45	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C49B-45FMB	45	24 Pin Flatpack	F1	Military	MIL-STD-883C
WS57C49B-45T	45	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-45TMB	45	24 Pin CERDIP, 0.3″	T1	Comm'l	MIL-STD-883C
WS57C49B-55CMB	55	28 Pad CLLCC	C1	Military	MIL-STD-883C
WS57C49B-55DMB	55	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C49B-55FMB	55	24 Pin Flatpack	F1	Military	MIL-STD-883C
WS57C49B-55T	55	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C49B-55TMB	55	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 16K × 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 70 ns
- **Low Power Consumption**
  — 200 mW Active Power (10 MHz)
- **Fast Programming**
- **Pin Compatible with AM27S51**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

3

GENERAL DESCRIPTION

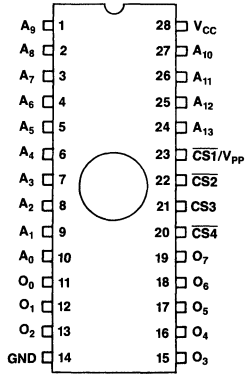
The WS57C51 is an extremely High Performance 128K UV Erasable electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C51 over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C51 is 100% tested with worst case test patterns both before and after assembly.

The WS57C51 provides a low power alternative to those designs which are committed to a bipolar PROM footprint. It is a direct drop-in replacement for a bipolar PROM of the same architecture (16K x 8). No software, hardware or layout changes need be performed.

The WS57C51 is configured in the standard Bipolar PROM pinout which provides an easy crossover path for systems which are currently using Bipolar PROMs.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C51-70
Address Access Time (Max)	70 ns
Output Enable Time (Max)	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

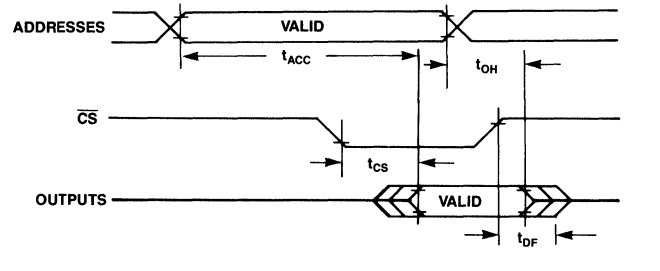
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		20 (Note 3)	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		25 (Note 3)	
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

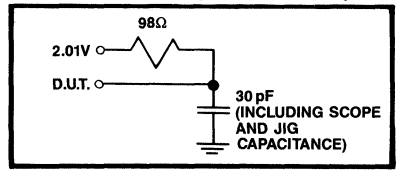
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C51-70		UNITS
		MIN	MAX	
Address to Output Delay	t_{ACC}		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		25	
Output Disable to Output Float	t_{DF}		25	
Address to Output Hold	t_{OH}	0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

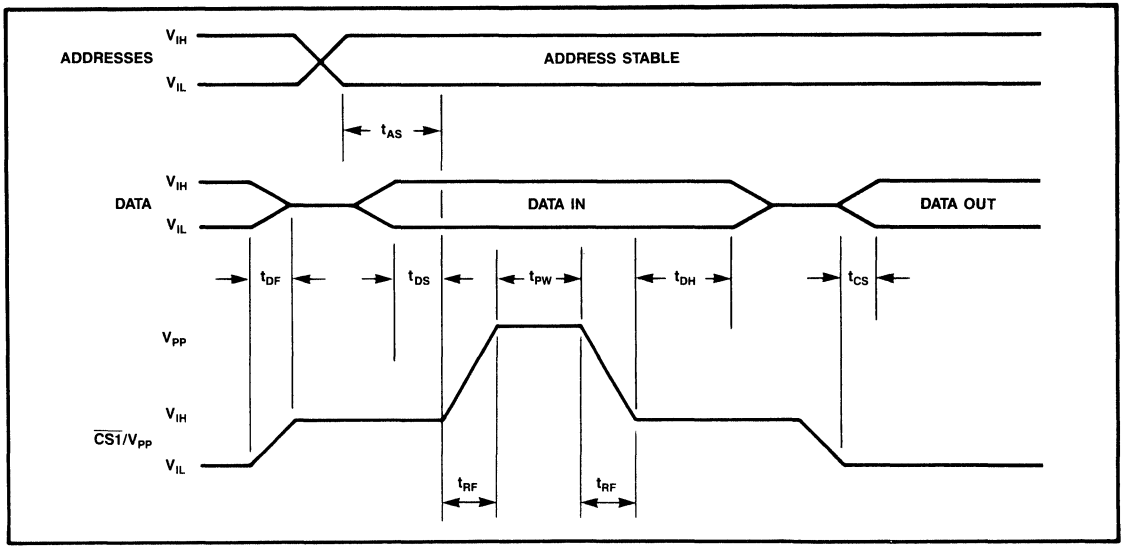
NOTE: 5) V_{pp} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup	t_{DS}	2			μs
Program Pulse Width (Note 6)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{pp} Rise and Fall Time	t_{RF}	1			μs

NOTE: 6) 10 ms is the pulse width required for simple, one pulse only, programming routines.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C51 has all 16K×8 bits in the "1," or high state. "0's" are loaded into the WS57C51 through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 13.5V pulse to the $\overline{CS}1/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C51 to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C51. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WS57C51 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C51 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C51 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2B, software version 13 or later, family/pinout code 7B/71; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C51-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 16K X 8 CMOS RPROM™

KEY FEATURES

- **Ultra-Fast Access Time**
  — 40 ns
- **Low Power Consumption**
  — 250 mW Active Power (10 MHz)
- **Fast Programming**
- **Pin Compatible with AM27S51**
- **Immune to Latch-Up**
  — Up to 200 mA
- **ESD Protection Exceeds 2000V**

3

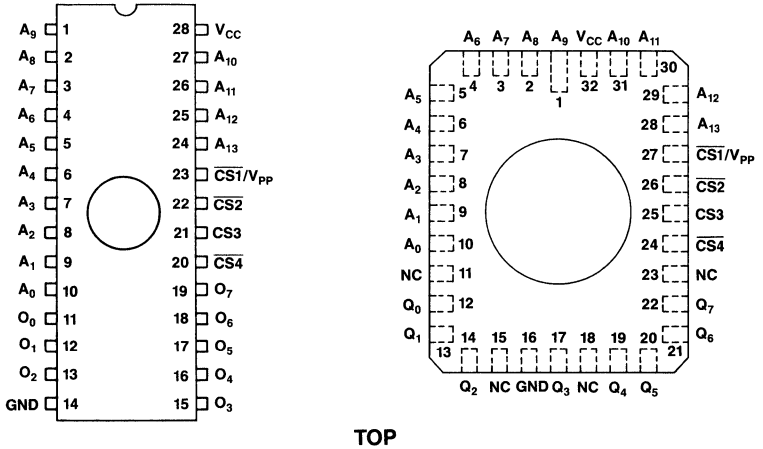
GENERAL DESCRIPTION

The WS57C51B is an extremely High Performance 128K UV Erasable electrically Re-Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar PROM speeds while consuming only 25% of the power required by its Bipolar counterparts.

A further advantage of the WS57C51B over Bipolar PROM devices is the fact that it utilizes a proven EPROM technology. This allows the entire memory array to be tested for switching characteristics and functionality after assembly. Unlike devices which cannot be erased, every WS57C51B is 100% tested with worst case test patterns both before and after assembly.

The WS57C51B provides a low power alternative to those designs which are committed to a bipolar PROM footprint. It is a direct drop-in replacement for a bipolar PROM of the same architecture (16K x 8). No software, hardware or layout changes need be performed.

PIN CONFIGURATION



TOP

PRODUCT SELECTION GUIDE

PARAMETER	WS57C51B-40	WS57C51B-45	WS57C51B-55	WS57C51B-70
Address Access Time (Max)	40 ns	45 ns	55 ns	70 ns
Output Enable Time (Max)	20 ns	20 ns	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....-65° to +150°C
Voltage on any pin with respect to GND .....-0.6V to +7V
VPP with respect to GND .....-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

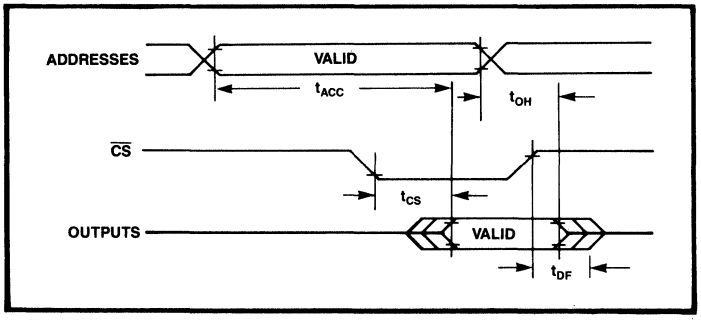
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX		UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4		V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4			
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l		30	Note 3	mA
			Military		35		
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l		40	Note 3	
			Military		40		
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10		µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10		

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

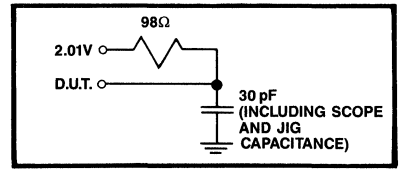
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C51B-40		WS57C51B-45		WS57C51B-55		WS57C51B-70		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		40		45		55		70	ns
$\overline{CS}$ to Output Delay	t_{CS}		20		20		20		25	
Output Disable to Output Float	t_{DF}		20		20		20		25	
Address to Output Hold	t_{OH}	0		0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 1.5V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or Gnd	I_{LI}	−10	10	μA
V_{PP} Supply Current During Programming Pulse	I_{PP}		60	mA
V_{CC} Supply Current (Notes 2 and 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

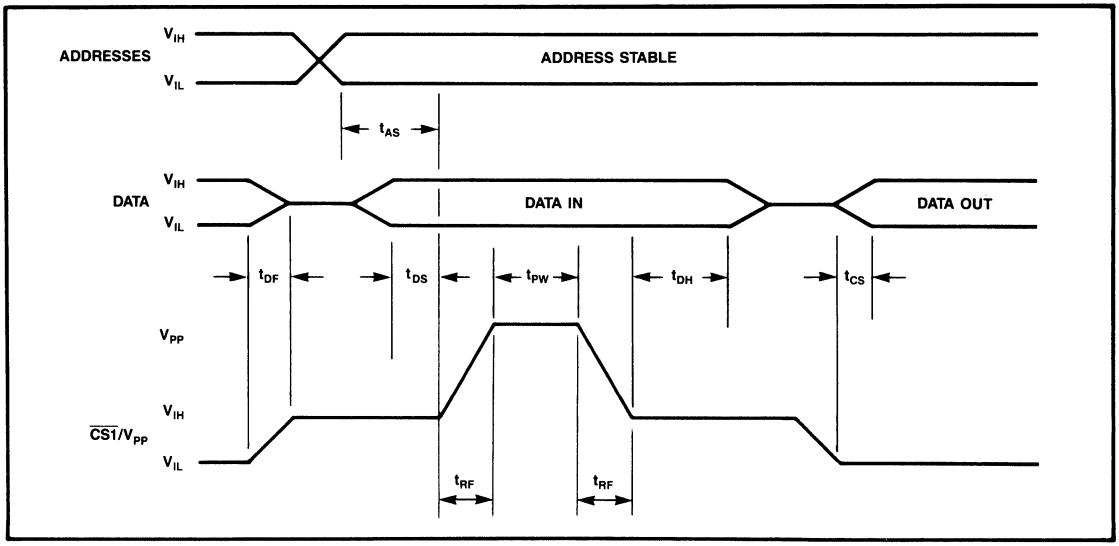
NOTE: 5) V_{PP} must not be greater than 14 volts including overshoot.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Disable Setup Time	t_{DF}			30	ns
Data Setup	t_{DS}	2			μs
Program Pulse Width (Note 6)	t_{PW}	1	3	10	ms
Data Hold Time	t_{DH}	2			μs
Chip Select Delay	t_{CS}			30	ns
V_{PP} Rise and Fall Time	t_{RF}	1			μs

NOTE: 6) 10 ms is the pulse width required for simple, one pulse only, programming routines.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C51B has all 16K×8 bits in the "1," or high state. "0's" are loaded into the WS57C51B through the procedure of programming.

Programming is performed by raising V_{CC} to 5.75V, disabling the outputs, addressing the byte to be programmed, presenting the data to be programmed onto the data pins, and applying a 12.5V pulse to the $\overline{CS1}/V_{PP}$ pin for 5 ms. The byte is then verified by removing the input data and reading the programmed byte as in the read operation. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C51B to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C51B. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WS57C51B should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C51B and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C51B and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2B, software version 13 or later, family/pinout code 7B/71; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C51B-40D	40	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C51B-40T	40	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C51B-45CMB	45	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-45D	45	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C51B-45DMB	45	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C51B-45T	45	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C51B-45TMB	45	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C
WS57C51B-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-55D	55	24 Pin CERDIP, 0.6″	D1	Comm'l	Standard
WS57C51B-55DMB	55	24 Pin CERDIP, 0.6″	D1	Military	MIL-STD-883C
WS57C51B-55T	55	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard
WS57C51B-55TMB	55	24 Pin CERDIP, 0.3″	T1	Military	MIL-STD-883C
WS57C51B-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C51B-70DM	70	24 Pin CERDIP	T1	Military	Standard
WS57C51B-70T	70	24 Pin CERDIP, 0.3″	T1	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

MILITARY 8K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 90 ns
- **Low Power Consumption**
  - 1 mW During Power Down
  - 240 mW Active Power (Max)
- **EPI Processing**
  - Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Military Temperature Operating Range**

3

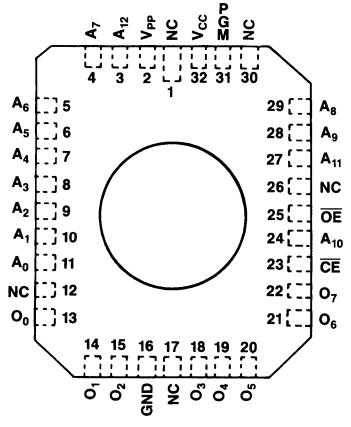
GENERAL DESCRIPTION

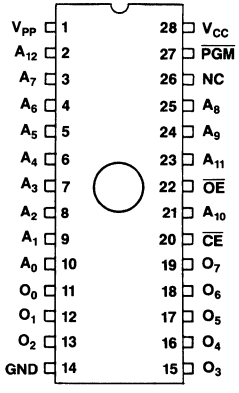
The WS27C64F is a HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at high speeds and very low power over the Military operating range.

The WS27C64F is a direct drop-in replacement for the industry standard 27C64 and/or 2764 EPROMs. It was developed specifically for this purpose and requires no board or software modifications to complete the change.

The WS27C64F is configured in the standard EPROM pinout which provides an easy upgrade path to the WS27C128F and WS27C256F.

PIN CONFIGURATION





TOP

PRODUCT SELECTION GUIDE

PARAMETER	WS27C64F-90	WS27C64F-12	WS27C64F-15
Address Access Time (Max)	90 ns	120 ns	150 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns
Output Enable Time (Max)	30 ns	30 ns	35 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....-65° to +150°C
Voltage on any pin with
respect to GND .....-0.6V to +7V
VPP with respect to GND ...-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Military	−55° to +125°C	+5V ±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

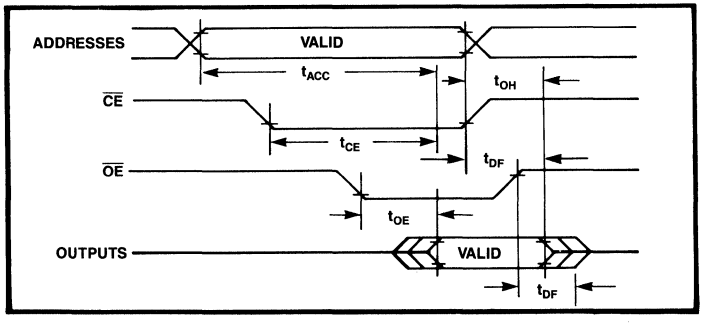
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = − 1mA	2.4		V
I_{SB1}	Vcc Standby Current CMOS	Note 1		200	μA
I_{SB2}	Vcc Standby Current TTL	Note 2		10	mA
I_{CC1}	Active Current (CMOS)	Notes 1 and 3		25	mA
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3		35	mA
I_{pp}	Vpp Supply Current	Vpp = Vcc		100	μA
V_{pp}	Vpp Read Voltage		Vcc − 0.4	Vcc	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	− 10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	− 10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Active power component is 3 mA/MHz (Power = AC + DC).

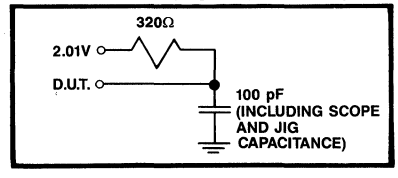
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C64F-90		WS27C64F-12		WS27C64F-15		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		120		150	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		120		150	
$\overline{OE}$ to Output Delay	t_{OE}		30		30		35	
Output Disable to Output Float	t_{DF}		30		30		35	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: .45 and 2.4V
Reference Levels: .8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse (CE = PGM = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		50	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

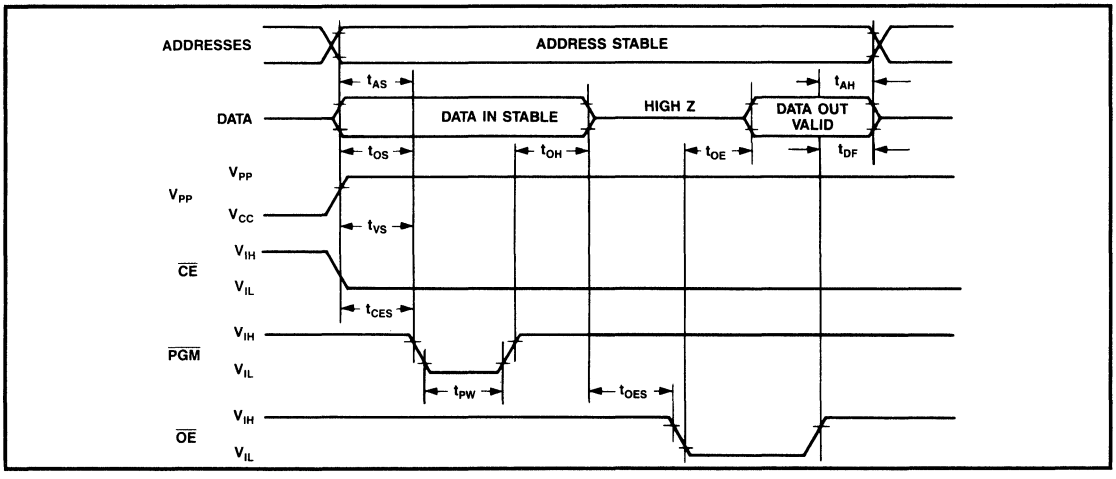
NOTES: 5) V_{CC} must be applied either coincidentally or before V_{pp} and removed either coincidentally or after V_{pp}.
6) V_{pp} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{pp} must not be switched from 5 volts to 13.5 volts or vice-versa.
7) During power up the PGM pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{pp}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2	-		μs
Chip Enable Setup Time	t_{CES}	2	-		μs
Output Enable Setup Time	t_{OES}	2	-		μs
Data Setup Time	t_{OS}	2	-		μs
Address Hold Time	t_{AH}	0	-		μs
Data Hold Time	t_{OH}	2	-		μs
Chip Disable to Output Float Delay	t_{DF}	0	-	130	ns
Data Valid from Output Enable	t_{OE}		-	130	ns
Vpp Setup Time	t_{VS}	2	-		μs
PGM Pulse Width	t_{PW}	1	3	10	ms

NOTE: 8) Single pulse programming algorithms should use one 10 ms PGM pulse per byte.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C64F has all 8192x8 bits in the "1," or high state. "0's" are loaded into the WS27C64F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C64F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS27C64F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS27C64F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C64F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C64F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 3C/33; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C64F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C64F-12CMB	120	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C64F-15CMB	150	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C64F-15DMB	150	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 8K X 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  —55ns
- **Low Power Consumption**
  —90mW During Power Down (18 MHz)
  —280mW Active Power (18 MHz)
- **EPI Processing**
  —Latch-up Immunity up to 200mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

3

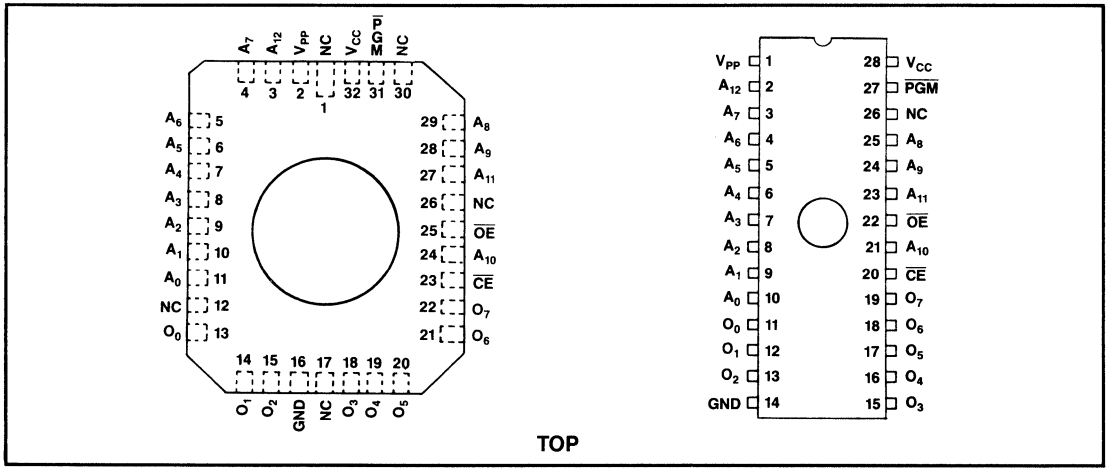
GENERAL DESCRIPTION

The WS57C64F is an extremely HIGH PERFORMANCE 64K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming very little power.

Two major features of the WS57C64F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

The WS57C64F is configured in the standard EPROM pinout which provides an easy upgrade path to higher density EPROMs.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C64F-55	WS57C64F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	20ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65° C to +150° C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70° C	+5V ± 5%
Military	−55° to +125° C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

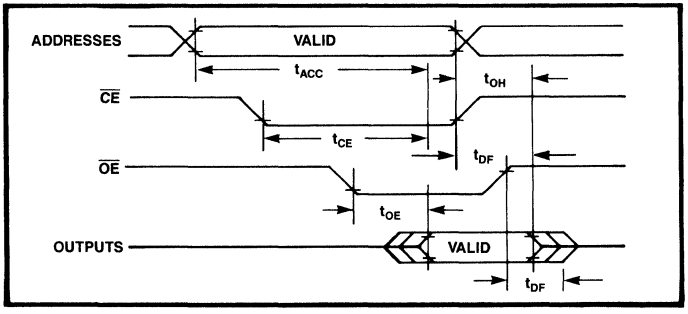
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= −4mA		2.4		V
I_{SB1}	Vcc Standby Current (CMOS)	CE=Vcc ± 0.3V. Notes 1 and 3			500	μA
I_{SB2}	Vcc Standby Current(TTL)	CE=V_{IH}. Notes 2 and 3			15	mA
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 4	Comm'l.		20	mA
			Military		30	mA
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 4	Comm'l.		25	mA
			Military		35	mA
I_{PP}	Vpp Supply Current	V_{PP}= Vcc			100	μA
V_{PP}	Vpp Read Voltage			Vcc-0.4	Vcc	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 1 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$. 4) A.C. Power component adds 3 mA/MHz.

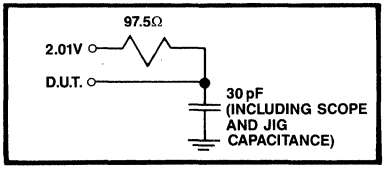
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C64F-55		WS57C64F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		20		25	
Output Disable to Output Float	t_{DF}		20		25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	MAX.	UNIT
Input Leakage Current V_{IN} = V_{CC} or Gnd	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse (CE = PGM = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current (Note 4)	I_{CC}		25	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = -4mA)	V_{OH}	2.4		V

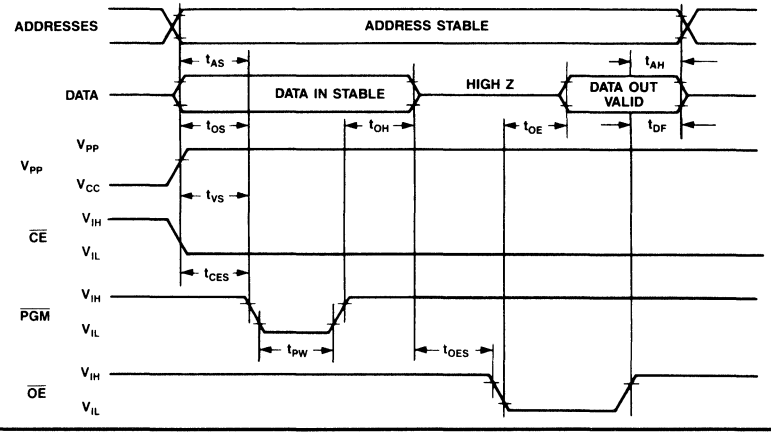
NOTES: 6) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7) V_{PP} must not be greater than 14 volts including overshoot. During CE = PGM = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
8) During power up the PGM pin must be brought high (≥V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{OS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{OH}	2			μs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			μs
PGM Pulse Width	t_{PW}	1	3	10	ms

NOTE: 9) For simple, one pulse only, programming algorithms, use a 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C64F has all 8192×8 bits in the "1," or high state. "0's" are loaded into the WS57C64F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin and $\overline{CE}$ is taken to V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C64F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C64F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS57C64F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C64F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C64F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 9 or later, family/pinout code 3C/33; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C64F-55D	55	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C64F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C64F-70D	70	24 Pin CERDIP, 0.6"	D1	Comm'l	Standard
WS57C64F-70DMB	70	24 Pin CERDIP, 0.6"	D1	Military	MIL-STD-883C

MILITARY 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 90/120/150 ns
- **Low Power Consumption**
  - 1 mW During Power Down
  - 300 mW Active Power
- **EPI Processing**
  - Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Military Operating Range**

3

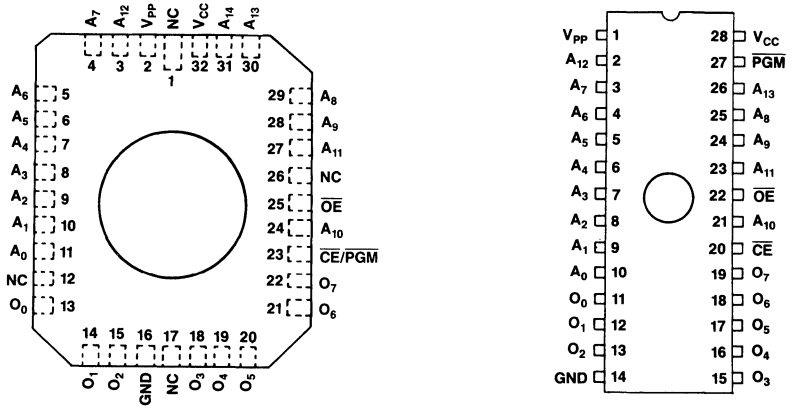
GENERAL DESCRIPTION

The WS27C128F is an extremely HIGH PERFORMANCE 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at high speeds and very low power over the full Military temperature operating range.

The WS27C128F was specifically designed to replace standard EPROMs in military environments. No hardware or software changes are required to replace standard military 27128 EPROMs with the WSI WS27C128F.

The WS27C128F is configured in the standard EPROM pinout which provides an easy upgrade path for the WS27C64F and the 256K bit WS27C256F.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS27C128F-90	WS27C128F-12	WS27C128F-15
Address Access Time (Max)	90 ns	120 ns	150 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns
Output Enable Time (Max)	30 ns	30 ns	35 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....-65° to +150°C
Voltage on any pin with
respect to GND .....-0.6V to +7V
VPP with respect to GND ...-0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Military	−55° to +125°C	+5V ±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	$I_{OL} = 4mA$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1mA$	2.4		V
I_{SB1}	Vcc Standby Current CMOS	Notes 1 and 3		200	μA
I_{SB2}	Vcc Standby Current TTL	Notes 2 and 3		10	mA
I_{CC1}	Active Current (CMOS)	Notes 1 and 4		25	mA
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 4		35	mA
I_{pp}	Vpp Supply Current	Vpp = Vcc		100	μA
V_{pp}	Vpp Read Voltage		Vcc − 0.4	Vcc	V
I_{LI}	Input Load Current	$V_{IN} = 5.5V$ or Gnd	−10	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$ or Gnd	−10	10	μA

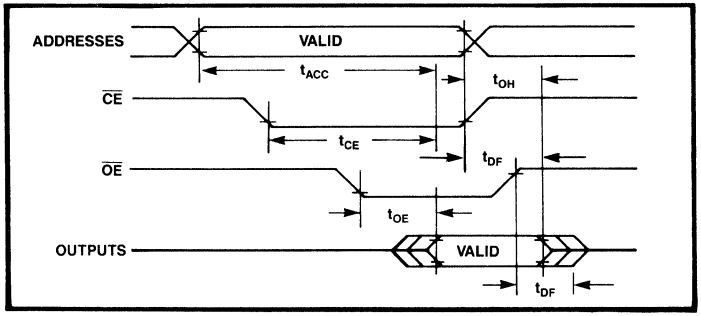
NOTES: 1) CMOS inputs: GND ± 0.3V or Vcc ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. standby power component is 1mA/MHz.
4) A.C. Active power component is 3mA/MHz (Power = AC + DC).

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

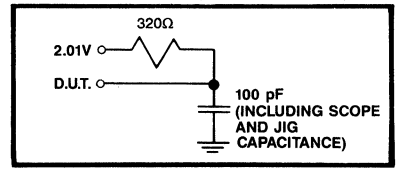
PARAMETER	SYMBOL	WS27C128F-90		WS27C128F-12		WS27C128F-15		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		120		150	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		120		150	
$\overline{OE}$ to Output Delay	t_{OE}		30		30		35	
Output Disable to Output Float	t_{DF}		30		30		30	
Address to Output Hold	t_{OH}	0		0		0		

NOTE: Single shot programming algorithms should use one 10 ms PGM pulse per word.

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: .45 and 2.4V
Reference Levels: .8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	µA
Vpp Supply Current During Programming Pulse (CE = PGM = V_{IL})	I_{pp}		30	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

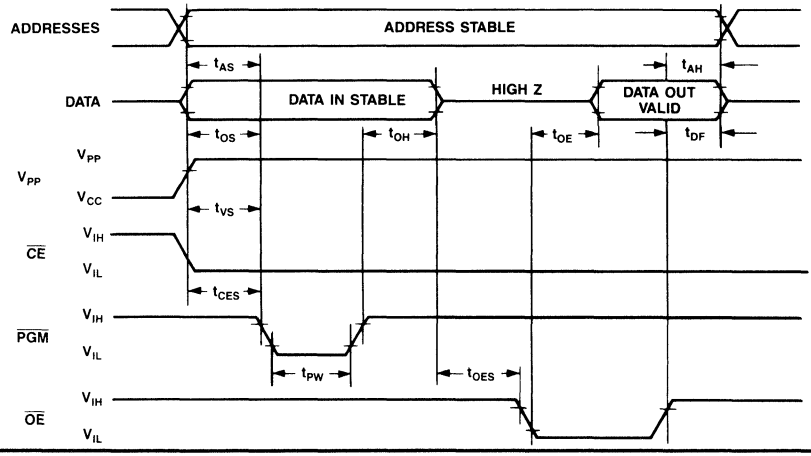
NOTES: 6) V_{CC} must be applied either coincidentally or before V_{pp} and removed either coincidentally or after V_{pp}.
7) V_{pp} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{pp} must not be switched from 5 volts to 13.5 volts or vice-versa.
8) During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{pp}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2	-		µs
Chip Enable Setup Time	t_{CES}	2	-		µs
Output Enable Setup Time	t_{OES}	2	-		µs
Data Setup Time	t_{OS}	2	-		µs
Address Hold Time	t_{AH}	0	-		µs
Data Hold Time	t_{OH}	2	-		µs
Chip Disable to Output Float Delay	t_{DF}	0	-	130	ns
Data Valid from Output Enable	t_{OE}		-	130	ns
Vpp Setup Time	t_{VS}	2	-		µs
PGM Pulse Width (Note 9)	t_{PW}	1	5		ms

NOTE: 9) For single pulse programming algorithms, use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C128F has all 16,384x8 bits in the "1," or high state. "0's" are loaded into the WS27C128F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin and $\overline{CE}$ is taken to V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C128F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS27C128F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS27C128F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C128F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C128F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 12 or later, family/pinout code 3C/51; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C128F-90CM	90	32 Pad CLLCC	C2	Military	Standard
WS27C128F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C128F-90DM	90	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS27C128F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C128F-12CM	120	32 Pad CLLCC	C2	MIlitary	Standard
WS27C128F-12CMB	120	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C128F-12DM	120	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS27C128F-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C128F-15CM	150	32 Pad CLLCC	C2	Military	Standard
WS27C128F-15CMB	150	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C128F-15DM	150	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS27C128F-15DMB	150	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  —55ns
- **Low Power Consumption**
  —90mW During Power Down (18 MHz)
  —305mW Active Power (18 MHz)
- **EPI Processing**
  —Latch-up Immunity up to 200mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

3

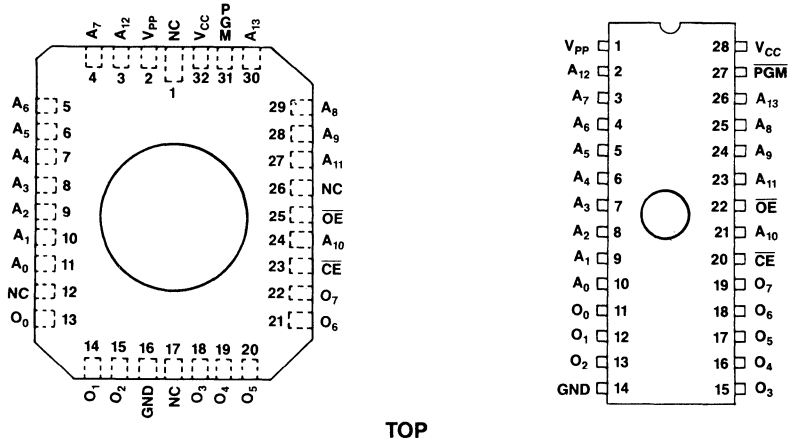
GENERAL DESCRIPTION

The WS57C128F is an extremely HIGH PERFORMANCE 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at Bipolar speeds while consuming only 60mA.

Two major features of the WS57C128F are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited. Examples of these applications are modems, secure telephones, servo controllers, and industrial controllers.

The WS57C128F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C128F-55	WS57C128F-70
Address Access Time (Max)	55ns	70ns
Chip Select Time (Max)	55ns	70ns
Output Enable Time (Max)	25ns	25ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

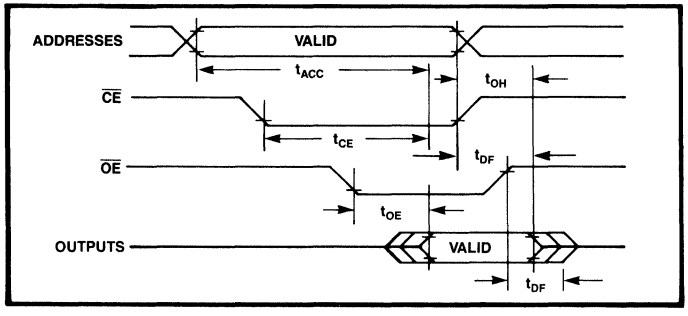
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4		V
I_{SB1}	V_{CC} Standby Current (CMOS)	Notes 1 and 3			500	µA
I_{SB2}	V_{CC} Standby Current (TTL)	Notes 2 and 3			20	mA
I_{CC1}	Active Current (CMOS)	Notes 1 and 4	Comm'l		25	mA
			Military		30	
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 4	Comm'l		35	mA
			Military		40	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Standby power component is 1 mA/MHz (Power = AC + DC).
4) A.C. Active power component is 3 mA/MHz (Power = AC + DC).

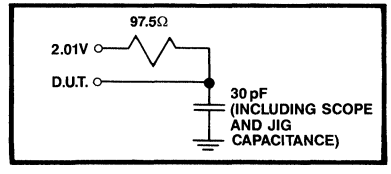
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C128F-55		WS57C128F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		25		25	
Output Disable to Output Float	t_{DF}		25	0	25	
Address to Output Hold	t_{OH}	10		10		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	μA
V_{PP} Supply Current During Programming Pulse (CE = PGM = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current Notes 2 & 4	I_{CC}		30	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

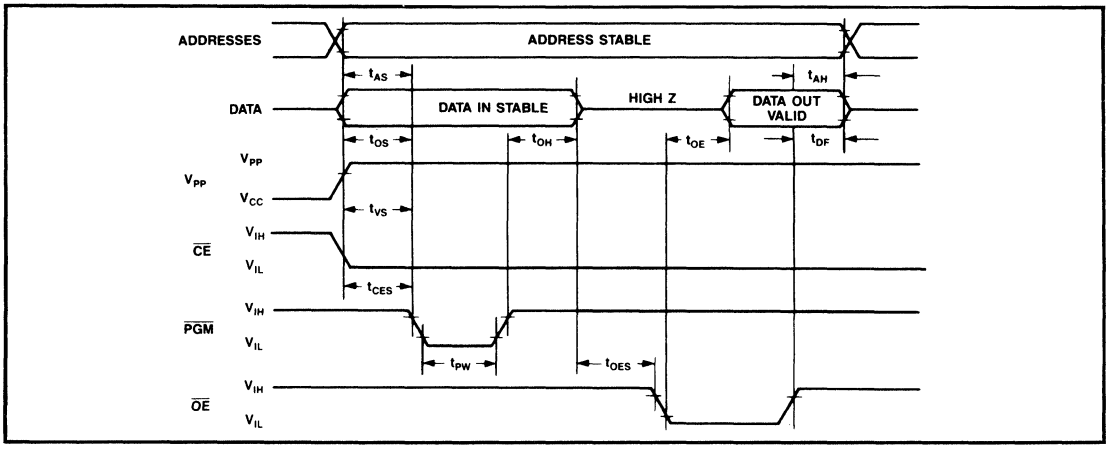
NOTES:
6) V_{CC} must be applied either coincidentally or before V_{pp} and removed either coincidentally or after V_{pp}.
7) V_{pp} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{pp} must not be switched from 5 volts to 13.5 volts or vice-versa.
8) During power up the PGM pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{pp}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2	-		μs
Chip Enable Setup Time	t_{CES}	2	-		μs
Output Enable Setup Time	t_{OES}	2	-		μs
Data Setup Time	t_{OS}	2	-		μs
Address Hold Time	t_{AH}	0	-		μs
Data Hold Time	t_{OH}	2	-		μs
Chip Disable to Output Float Delay	t_{DF}	0	-	130	ns
Data Valid from Output Enable	t_{OE}		-	130	ns
Vpp Setup Time	t_{VS}	2	-		μs
PGM Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C128F has all 16,384×8 bits in the "1," or high state. "0's" are loaded into the WS57C128F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin, and $\overline{CE}$ is at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C128F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C128F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS57C128F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C128F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C128F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 11 or later, family/pinout code 3C/51; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C128F-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883c
WS57C128F-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C128F-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

MILITARY 32K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 90 ns (Military)
- **Low Power Consumption**
  - 1 mW During Power Down
  - 325 mW Active Power
- **EPI Processing**
  - Latch-Up Immunity Up to 200 mA
- **Military High Rel Processing**
- **Drop-In Replacement for**
  - M27256

3

GENERAL DESCRIPTION

The WS27C256F is a HIGH PERFORMANCE 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at speeds as fast as 90 ns Access Time over the full military operating range. (If faster speeds are required, contact your WSI sales representative.

Two major features of the WS27C256F are its Low Power and High Speed. While operating in a TTL environment it consumes only 65 mA while cycling at full speed. Additionally, the WS27C256F can be placed in a standby mode which drops operating current below 30 mA in a TTL environment and 200 µA in a CMOS environment.

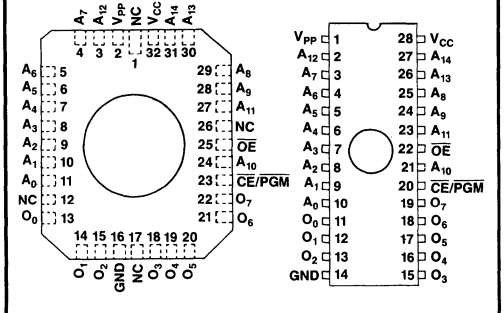
The WS27C256F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other address are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE A8H.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-90	WS27C256F-12	WS27C256F-15
Address Access Time (Max)	90 ns	120 ns	150 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

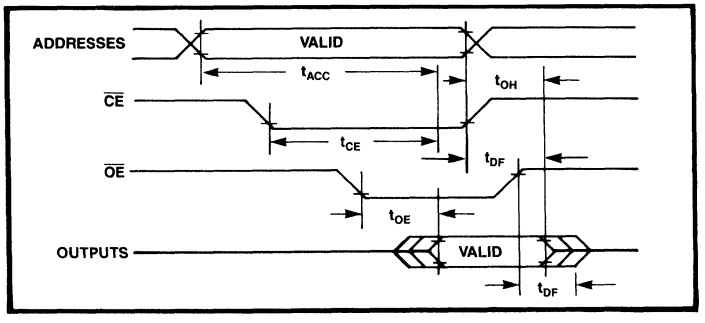
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC} \pm 0.3V$ (Note 1)		250	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = V_{IH}$ (Note 2)		5	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Note 1		30 (Note 3)	mA
I_{CC2}	V_{CC} Active Current (TTL)	Note 2		40 (Note 3)	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		100	µA
V_{PP}	V_{PP} Read Voltage		$V_{CC}-0.4$	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	−10	10	µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Active power component is 3 mA/MHz (Total Power = AC + DC).

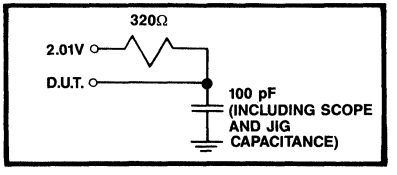
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C256F-90		WS27C256F-12		WS27C256F-15		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		120		150	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		120		150	
$\overline{OE}$ to Output Delay	t_{OE}		30		35		40	
Output Disable to Output Float	t_{DF}		30		35		40	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: .45 and 2.4
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 10%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	μA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		30	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL}=4mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH}=−1mA)	V_{OH}	2.4		V

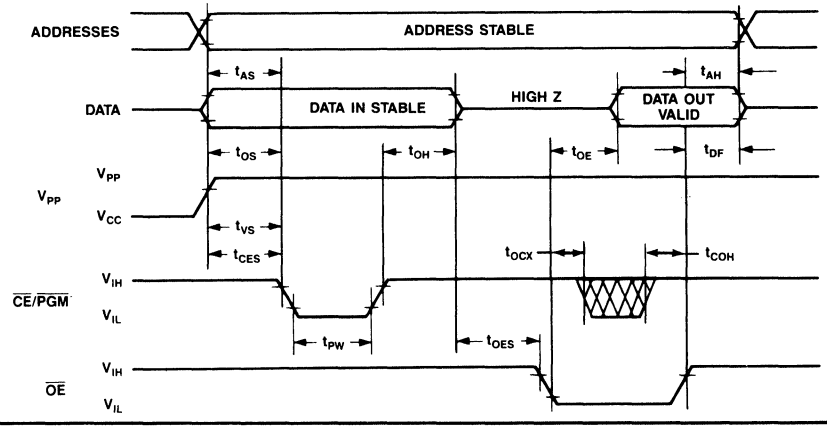
NOTES: 5) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
6) V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
7) During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 10%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{OS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{OH}	2			μs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time	t_{VS}	2			μs
PGM Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			μs

NOTE: 8) Single pulse programming algorithms should use one 10 ms PGM pulse per byte.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C256F has all 32,768×8 bits in the "1," or high state. "0's" are loaded into the WS27C256F through the procedure of programming.

The programming mode is entered when +12.5V is applied to the V_{PP} pin, and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C256F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS27C256F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS27C256F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C256F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C256F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 12 or later, family/pinout code 3C/32; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-12CMB	120	32 Pad CLLCC	C2	Military	MIL-STD-883c
WS27C256F-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256F-15CMB	150	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256F-15DMB	150	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

HIGH SPEED 32K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 55 ns
- **Low Power Consumption**
  - — 75 mW During Power Down
  - — 325 mW Active Power
- **EPI Processing**
  - — Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

GENERAL DESCRIPTION

The WS57C256F is an extremely HIGH PERFORMANCE 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at speeds as fast as 55 ns Access Time.

Two major features of the WS57C256F are its Low Power and High Speed. While operating in a TTL environment it consumes only 65 mA while cycling at full speed. Additionally, the WS57C256F can be placed in a standby mode which drops operating current below 15 mA in a TTL environment and 200 µA in a CMOS environment.

The WS57C256F also has exceptional output drive capability. It can source 4 mA and sink 16 mA per output.

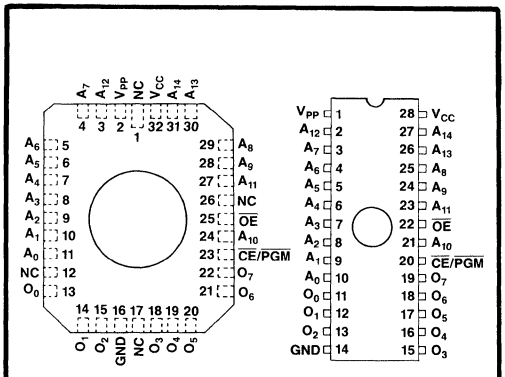
The WS57C256F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, $A_9 = 12V$, A_0 is toggled, and all other address are at TTL low. $A_0 = V_{IL}$ = MFGR 23H, $A_0 = V_{IH}$ = DEVICE A8H.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C256F-55	WS57C256F-70
Address Access Time (Max)	55 ns	70 ns
Chip Select Time (Max)	55 ns	70 ns
Output Enable Time (Max)	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....-65° to +150°C
Voltage on any pin with
respect to GND .....-0.6V to +7V
VPP with respect to GND ...-0.6V to +13.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l	0° to +70°C	+5V ± 5%
Military	-55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range With Vpp= Vcc.

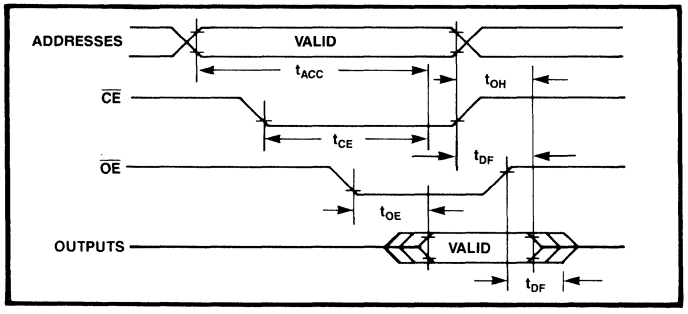
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}=16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}=-4mA		2.4		V
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$=Vcc ± 0.3V. Note 1 & 3			500	µA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$=V_{IH}. Note 2 & 3			15	mA
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 4	Comm'l		30	mA
			Military		40	mA
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 4	Comm'l		35	mA
			Military		45	mA
I_{pp}	Vpp Supply Current	Vpp=Vcc			100	µA
V_{pp}	Vpp Read Voltage			Vcc-0.4	Vcc	V
I_{LI}	Input Load Current	V_{IN}=5.5V or Gnd		-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT}=5.5V or Gnd		-10	10	µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 1 mA/MHz.
4) A.C. Power component adds 3 mA/MHz.

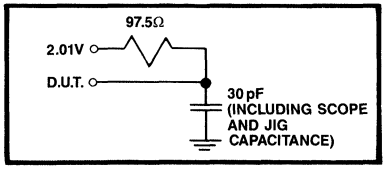
AC READ CHARACTERISTICS Over Operating Range with V_{PP} = V_{CC}.

PARAMETER	SYMBOL	WS57C256F-55		WS57C256F-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		50		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		25		30	
Output Disable to Output Float	t_{DF}		25		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 12.5 \pm 0.5V$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd)	I_{LI}	-10	10	μA
V_{CC} Supply Current During Programming Pulse ($\overline{CE} = \overline{PGM} = V_{IL}$)	I_{CC}		60	mA
V_{CC} Supply Current (Note 4)	I_{CC}		35	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify ($I_{OL} = 16mA$)	V_{OL}		0.45	V
Output High Voltage During Verify ($I_{OH} = -4mA$)	V_{OH}	2.4		V

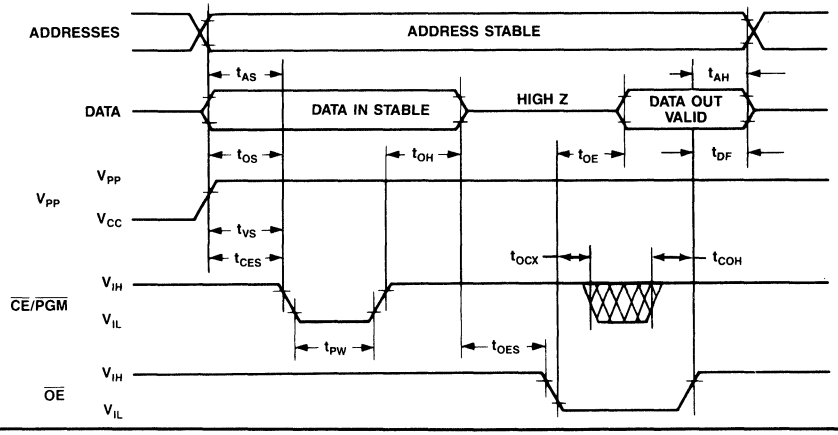
NOTES: 6) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7) V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8) During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			μs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{OS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{OH}	2			μs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			μs
PGM Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			μs

NOTE: 9) A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C256F has all 32,768×8 bits in the "1," or high state. "0's" are loaded into the WS57C256F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During Programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C256F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C256F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS57C256F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C256F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C256F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 12 or later; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C256F-55D	55	28 Pin CERDIP, 0.6″	D2	Comm'l	Standard
WS57C256F-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-70D	70	28 Pin CERDIP, 0.6″	D2	Comm'l	Standard
WS57C256F-70DMB	70	28 Pin CERDIP, 0.6″	D2	Military	MIL-STD-883C

HIGH SPEED 32K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - — 35 ns
- **Low Power Consumption**
  - — 75 mW During Power Down
  - — 325 mW Active Power
- **EPI Processing**
  - — Latch-Up Immunity Up to 200 mA
  - — ESD Protection Exceeds 2000V
- **Standard EPROM Pinout**

GENERAL DESCRIPTION

The WS57C256F is a 32K x 8 CMOS EPROM which has been speed-enhanced from 55 ns to 35 ns. It is based upon WaferScale's patented CMOS Split Gate EPROM technology.

The 35 ns access time of the WS57C256F is a key parameter. Traditionally, as memory densities increase, memory access times become slower. This forces microprocessors to insert Wait States which negatively impact system throughput. Real Time applications cannot afford Wait States regardless of memory density. WaferScale's unique memories can keep pace with the fastest microprocessors. The combination of speed and density available in the WS57C256F enables the use of more complex and comprehensive algorithms in Real Time applications.

WaferScale's patented CMOS Split-Gate EPROM technology not only enables the development of fast and dense memory products, it also provides a higher level of Quality and Reliability. Tests have proven that WSI EPROM products program very efficiently and quickly. Also, the WSI EPROM retains its data an order of magnitude better than traditional EPROM technologies. This combination of speed, density, quality and reliability make WSI the obvious choice when selecting a non-volatile memory supplier.

The WS57C256F is configured in the JEDEC standard EPROM pin configuration. It is also easily programmed on popular EPROM programmers as well as the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

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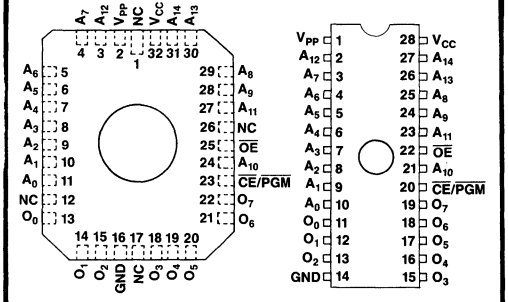
MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, $A_9 = 12V$, A_0 is toggled, and all other address are at TTL low. $A_0 = V_{IL}$ = MFGR 23H, $A_0 = V_{IH}$ = DEVICE A8H.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS57C256F-35	WS57C256F-45
Address Access Time (Max)	35 ns	45 ns
Chip Select Time (Max)	35 ns	45 ns
Output Enable Time (Max)	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature .....-65° to +150°C
Voltage on any pin with
respect to GND .....-0.6V to +7V
VPP with respect to GND ...-0.6V to +13.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l	0° to +70°C	+5V ± 5%
Military	-55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

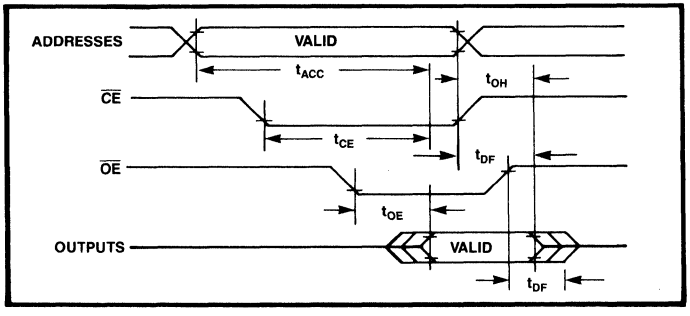
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}=16mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}=-4mA		2.4		V
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$=Vcc ± 0.3V. Note 1			500	µA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$=V_{IH}. Note 2			5	mA
I_{CC1}	Vcc Active Current (CMOS)	Notes 1 and 3	Comm'l		30	mA
			Military		40	mA
I_{CC2}	Vcc Active Current (TTL)	Notes 2 and 3	Comm'l		35	mA
			Military		45	mA
I_{pp}	Vpp Supply Current	Vpp=Vcc			100	µA
V_{pp}	Vpp Read Voltage			Vcc-0.4	Vcc	V
I_{LI}	Input Load Current	V_{IN}=5.5V or Gnd		-10	10	µA
I_{LO}	Output Leakage Current	V_{OUT}=5.5V or Gnd		-10	10	µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Power component adds 3 mA/MHz.

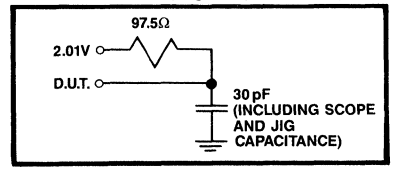
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C256F-35		WS57C256F-45		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		35		45	ns
$\overline{CE}$ to Output Delay	t_{CE}		35		45	
$\overline{OE}$ to Output Delay	t_{OE}		15		20	
Output Disable to Output Float	t_{DF}		15		20	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

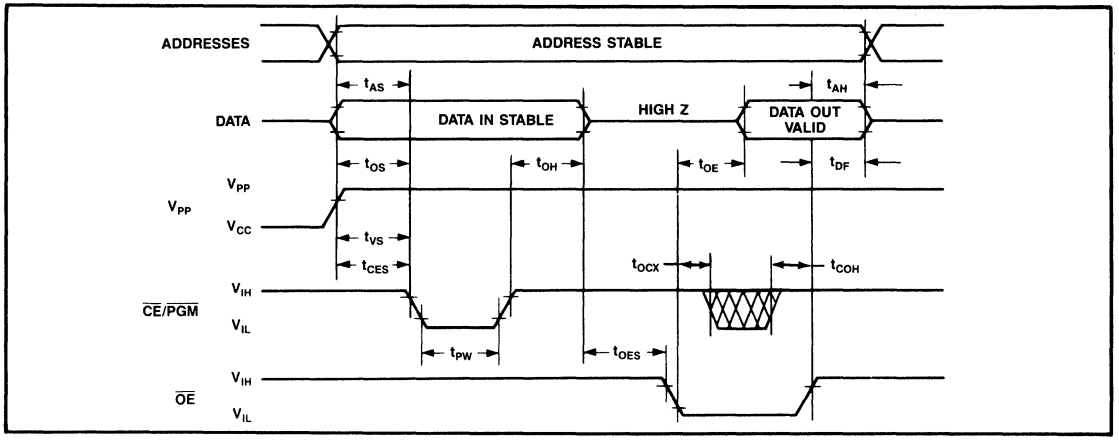
PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current (Note 4)	I_{CC}		35	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 16mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −4mA)	V_{OH}	2.4		V

NOTES: 6) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7) V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
8) During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
PGM Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C256F has all 32,768x8 Bits in the "1," or high state. "0's" are loaded into the WS57C256F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During Programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C256F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C256F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS57C256F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C256F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C256F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C256F-35D	35	28 Pin CERDIP, 0.6″	D2	Comm'l	Standard
WS57C256F-45CMB	45	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-45D	45	28 Pin CERDIP, 0.6″	D2	Comm'l	Standard
WS57C256F-45DMB	45	28 Pin CERDIP, 0.6″	D2	Military	MIL-STD-883C
WS57C256F-55CMB	55	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C256F-55DMB	55	28 Pin CERDIP, 0.6″	D2	Military	MIL-STD-883C

32K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 90 ns
- **Low Power Consumption**
  - 0.5 mW During Power Down
  - 150 mW Active Power @ 5 MHz
- **Drop-In Replacement for 27C256 or 27256**
- **300 Mil Dip or Standard 600 Mil Dip**
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000V

3

GENERAL DESCRIPTION

The WS27C256L is a HIGH PERFORMANCE 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in WSI's latest CMOS EPROM technology which enables it to operate at speeds as fast as 90 ns access time over the full operating range. (If faster speeds are required, contact your WSI sales representative.)

The WS27C256L can directly replace any 32K × 8 EPROM which conforms to the JEDEC standard. Examples of this would be as follows: 27256, 27C256, or 27C256F. It can be easily programmed using standard EPROM programmers or the MagicPro™ IBM PC compatible engineering programmer offered by WSI.

The WS27C256L is also available in a 300 mil Dip. The pin configuration remains the same as the 600 mil wide package and the programming algorithms are unchanged. This allows for a simple PCB layout change to take advantage of a 50% reduction in required board space. An upgrade path to a 512K product (WS27C512F) is provided.

The high-speed (90 ns access time) of the WS27C256L enables it to run in a "No Wait State" environment with such microprocessors as the 16 MHz 80286. Slower speed versions are also available for lower performance applications.

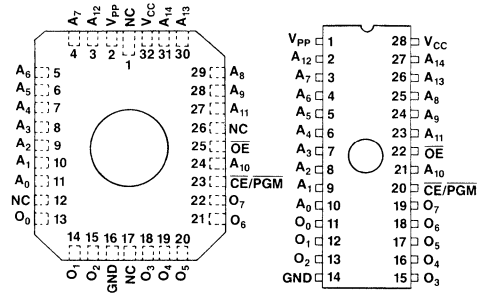
The WS27C256L is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}.

PIN CONFIGURATION



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PRODUCT SELECTION GUIDE

PARAMETER	WS27C256L-90	WS27C256L-12
Address Access Time (Max)	90 ns	120 ns
Chip Select Time (Max)	90 ns	120 ns
Output Enable Time (Max)	30 ns	35 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65° C to +150° C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Military	−55°C to +125°C	+5V ± 10%
Commercial	0° to +70°C	

DC READ CHARACTERISTICS Over Operating Range With Vpp= Vcc.

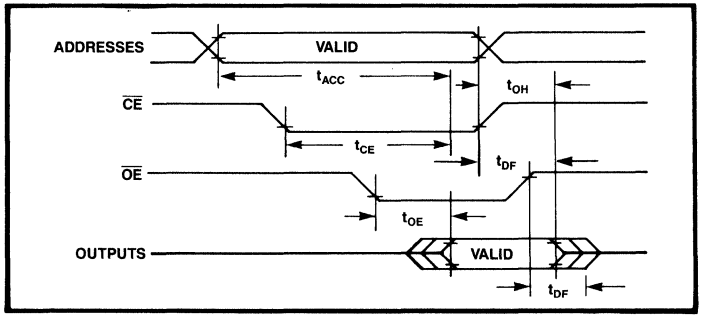
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL}= 4mA		0.4	V
V_{OH}	Output High Voltage	I_{OL}=-1mA	2.4		V
I_{SB1}	Vcc Standby Current CMOS	$\overline{CE}$=Vcc ± 0.3V. Note 1		100	μA
I_{SB2}	Vcc Standby Current TTL	$\overline{CE}$=V_{IH}. Note 2		3	mA
I_{CC1}	Vcc Active Current (CMOS)	Note 1		17 (Note 3)	mA
I_{CC2}	Vcc Active Current (TTL)	Note 2		33 (Note 3)	mA
I_{pp}	Vpp Supply Current	V_{pp}= Vcc		100	μA
V_{pp}	Vpp Read Voltage		Vcc - 0.4	Vcc	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd	- 10	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd	- 10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Active power component is 2.5 mA/MHz (Total Power = AC + DC).

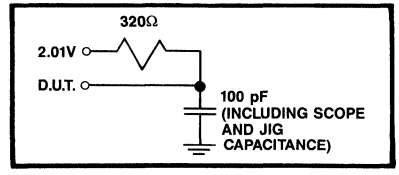
AC READ CHARACTERISTICS Over Operating Range with V_{PP} = V_{CC}.

PARAMETER	SYMBOL	WS27C256L-90		WS27C256L-12		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		120	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		120	
$\overline{OE}$ to Output Delay	t_{OE}		30		35	
Output Disable to Output Float	t_{DF}		30		35	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: .45 and 2.4
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 10%, V_{pp} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		33	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL}=4mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH}=-1mA)	V_{OH}	2.4		V

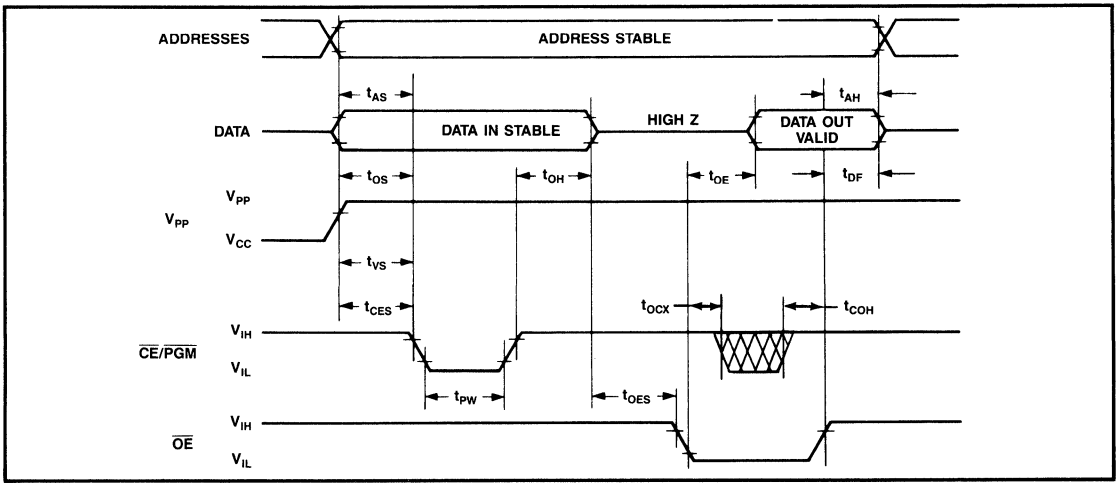
NOTES: 5) V_{CC} must be applied either coincidentally or before V_{pp} and removed either coincidentally or after V_{pp}.
6) V_{pp} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{pp} must not be switched from 5 volts to 12.5 volts or vice-versa.
7) During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{pp}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 10%, V_{pp} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid from Output Enable	t_{OE}			55	ns
V_{PP} Setup Time	t_{VS}	2			µs
PGM Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

NOTE: 8) Single pulse programming algorithms should use one 10 ms PGM pulse per byte.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C256L has all 32,768x8 Bits in the "1," or high state. "0's" are loaded into the WS27C256L through the procedure of programming.

The programming mode is entered when +12.5V is applied to the V_{PP} pin and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During Programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C256L to an ultra-violet light source. A dosage of 15W second/cm^3 is required to completely erase a WS27C256L. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms and intensity of 12000µ W/cm^3 for 20 minutes. The WS27C256L should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C256L and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C256L and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256L-90D	90	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256L-90DMB	90	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256L-90P	90	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS27C256L-90S	90	28 Pin Plastic DIP, 0.3"	S2	Comm'l	Standard
WS27C256L-90T	90	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS27C256L-90TMB	90	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C
WS27C256L-12CMB	120	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C256L-12D	120	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256L-12DMB	120	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C
WS27C256L-12P	120	28 Pin Plastic DIP, 0.6"	P3	Comm'l	Standard
WS27C256L-12S	120	28 Pin Plastic DIP, 0.3"	S2	Comm'l	Standard
WS27C256L-12T	120	28 Pin CERDIP, 0.3"	T2	Comm'l	Standard
WS27C256L-12TMB	120	28 Pin CERDIP, 0.3"	T2	Military	MIL-STD-883C

COMMERCIAL 32K × 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 90 ns
- **Low Power Consumption**
  - 1 mW During Power Down
  - 325 mW Active Power
- **EPI Processing**
  - Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Compatible with WS57C256F**

3

The WS27C256F is an extremely HIGH PERFORMANCE 256K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at speeds as fast as 90 ns Access Time. (If faster speeds are required, contact your WSI sales representative.)

Two major features of the WS27C256F are its Low Power and High Speed. While operating in a TTL environment it consumes only 65 mA while cycling at full speed. Additionally, the WS27C256F can be placed in a standby mode which drops operating current below 1 mA in a TTL environment and 100 µA in a CMOS environment.

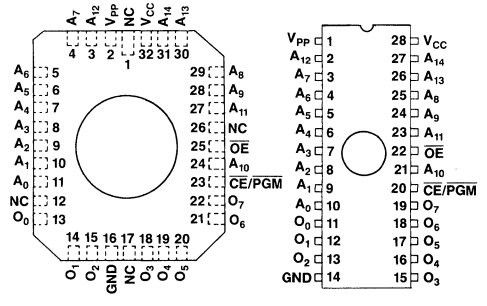
The WS27C256F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

PINS / MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, $A_9 = 12V$, A_0 is toggled, and all other address are at TTL low. $A_0 = V_{IL}$ = MFGR 23H, $A_0 = V_{IH}$ = DEVICE A8H.

PIN CONFIGURATION



TOP

PRODUCT SELECTION GUIDE

PARAMETER	WS27C256F-90	WS27C256F-12
Address Access Time (Max)	90 ns	120 ns
Chip Select Time (Max)	90 ns	120 ns
Output Enable Time (Max)	30 ns	35 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range With Vpp= Vcc.

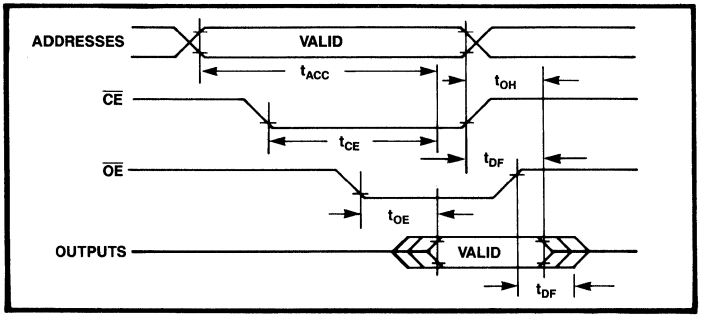
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA		2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} ± 0.3V (Note 1)			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = V_{IH} (Note 2)			1	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Note 1	Comm'l		30 (Note 3)	mA
I_{CC2}	V_{CC} Active Current (TTL)	Note 2	Comm'l		35 (Note 3)	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Active power component is 3 mA/MHz (Total Power = AC + DC).

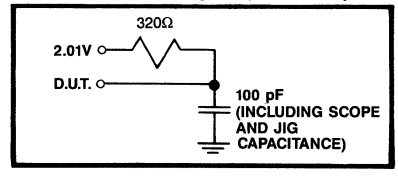
AC READ CHARACTERISTICS Over operating Range with Vpp = Vcc.

PARAMETER	SYMBOL	WS27C256F-90		WS27C256F-12		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		90		120	ns
$\overline{CE}$ to Output Delay	t_{CE}		90		120	
$\overline{OE}$ to Output Delay	t_{OE}		30		35	
Output Disable to Output Float	t_{DF}		30		35	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: .45 and 2.4
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 10%, V_{pp} = 13.5 ± 0.5V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		35	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL}=4mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH}=-1mA)	V_{OH}	2.4		V

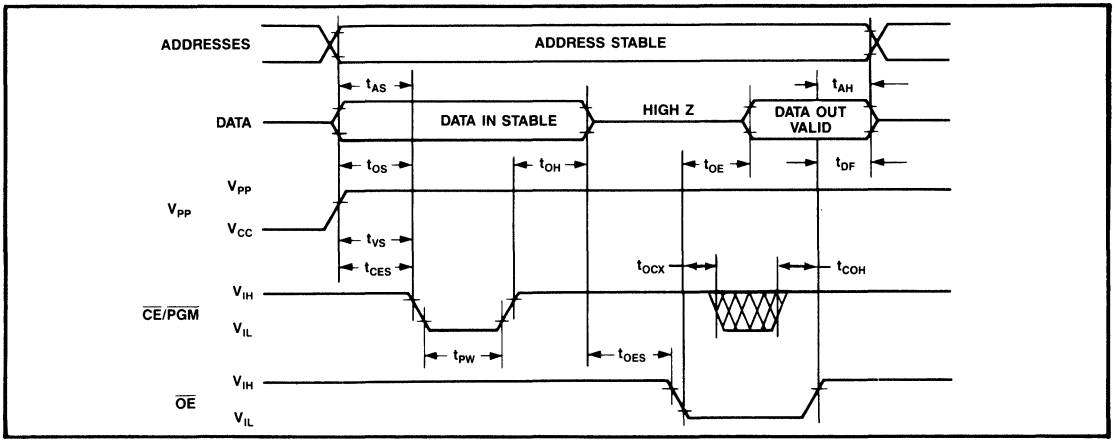
NOTES: 5) V_{CC} must be applied either coincidentally or before V_{pp} and removed either coincidentally or after V_{pp}.
6) V_{pp} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{pp} must not be switched from 5 volts to 13.5 volts or vice-versa.
7) During power up the $\overline{PGM}$ pin must be brought high (≥ V_{IH}) either coincident with or before power is applied to V_{pp}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 13.5 ± 0.5V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time	t_{VS}	2			µs
PGM Pulse Width	t_{PW}	1	3	10	ms
$\overline{OE}$ Low to $\overline{CE}$ "Don't Care"	t_{OCX}	2			µs

NOTE: 8) Single pulse programming algorithms should use one 10 ms PGM pulse per byte.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C256F has all 32,768×8 bits in the "1," or high state. "0's" are loaded into the WS27C256F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin, and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During Programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C256F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS27C256F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS27C256F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C256F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C256F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2 or 2B, software version 12 or later, family/pinout code 3C/32; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C256F-90D	90	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS27C256F-12D	120	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard

HIGH SPEED 64K x 8 CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 70 ns
- **Low Power Consumption**
  - 75 mW During Power Down
  - 325 mW Active Power
- **EPI Processing**
  - Latch-Up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **Bipolar Speeds**

GENERAL DESCRIPTION

The WS27C512F is an extremely HIGH PERFORMANCE 512K UV Erasable Electrically Programmable Read Only Memory. It is manufactured in an advanced CMOS technology which allows it to operate at speeds as fast as 70 ns Access Time.

Two major features of the WS27C512F are its Low Power and High Speed. While operating in a TTL environment it consumes only 72 mA while cycling at full speed. Additionally, the WS27C512F can be placed in a standby mode which drops operating current below 2 mA in a TTL environment and 200 µA in a CMOS environment.

The WS27C512F also have exceptional output drive capability. It can source 1 mA and sink 4 mA per output.

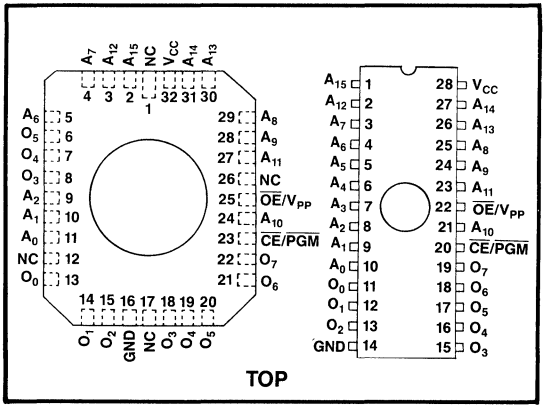
The WS27C512F is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$/V_{PP}	Vcc	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Output Disable	C	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	High Z
Program	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, A_9 = 12V, A_0 is toggled, and all other address are at TTL low. A_0 = V_{IL} = MFGR 23H, A_0 = V_{IH} = DEVICE AAH.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS27C512F-70	WS27C512F-90
Address Access Time (Max)	70 ns	90 ns
Chip Select Time (Max)	70 ns	90 ns
Output Enable Time (Max)	25 ns	30 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +13.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	V_{CC}
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP}=V_{CC}$.

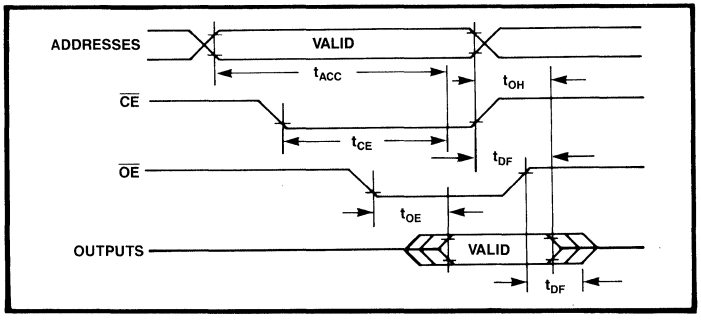
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA		2.4		V
I_{SB1}	V_{CC} Standby Current CMOS	CE=V_{CC} ± 0.3V. Note 1			200	μA
I_{SB2}	V_{CC} Standby Current TTL	CE=V_{IH}. Note 2			2	mA
I_{CC1}	V_{CC} Active Current (CMOS)	Notes 1 and 3	Comm'l.		30	mA
			Military		40	mA
I_{CC2}	V_{CC} Active Current (TTL)	Notes 2 and 3	Comm'l.		35	mA
			Military		45	mA
I_{PP}	V_{PP} Supply Current	$V_{PP}=V_{CC}$			100	μA
V_{PP}	V_{PP} Read Voltage			V_{CC}−0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN}=5.5V or Gnd		−10	10	μA
I_{LO}	Output Leakage Current	V_{OUT}=5.5V or Gnd.		−10	10	μA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V. 3) A.C. Power component adds 3 mA/MHz.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.

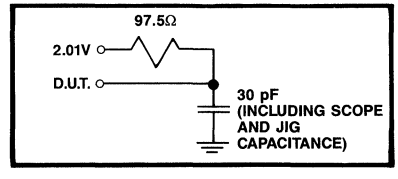
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS27C512F-70		WS27C512F-90		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		25		30	
Output Disable to Output Float	t_{DF}		25		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0.4 and 2.4V

Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{CC} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{CC}		60	mA
V_{CC} Supply Current (Note 3)	I_{CC}		25	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 4 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −1 mA)	V_{OH}	2.4		V

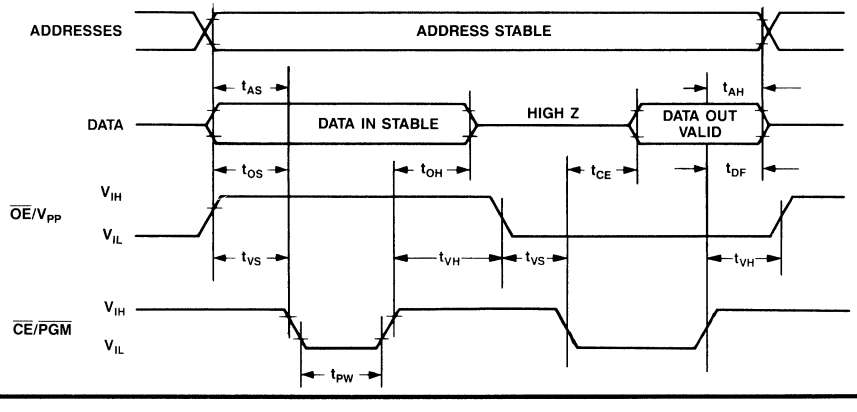
NOTES: 4) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
5) V_{PP} must not be greater than 14 volts including overshoot. During CE = PGM = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
6) During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.5V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µS
V_{PP} Hold Time	t_{VH}	2			µS
Data Setup Time	t_{OS}	2			µS
Address Hold Time	t_{AH}	0			µS
Data Hold Time	t_{OH}	2			µS
Chip Disable to Output Float Delay	t_{DF}	0		70	ns
Data Valid From Chip Enable	t_{CE}			70	ns
V_{PP} Setup Time	t_{VS}	2			µS
PGM Pulse Width	t_{PW}	1	35		ms

NOTES: 7. A single shot programming algorithm should use one 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS27C512F has all 65,536×8 bits in the "1," or high state. "0's" are loaded into the WS27C512F through the procedure of programming.

The programming mode is entered when +13.5V is applied to the $\overline{OE}/V_{PP}$ pin and $\overline{CE}/\overline{PGM}$ is taken to V_{IL}. During Programming, $\overline{CE}/\overline{PGM}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS27C512F to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS27C512F. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS27C512F should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS27C512F and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS27C512F and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2B; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C512F-70C	70	32 Pad CLLCC	C2	Comm'l	Standard
WS27C512F-70D	70	28 Pin CERDIP, 0.6″	D2	Comm'l	Standard
WS27C512F-90C	90	32 Pad CLLCC	C2	Comm'l	Standard
WS27C512F-90CM	90	32 pad CLLCC	C2	Military	Standard
WS27C512F-90CMB	90	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS27C512F-90D	90	28 Pin CERDIP, 0.6″	D2	Comm'l	Standard
WS27C512F-90DM	90	28 Pin CERDIP, 0.6″	D2	Military	Standard
WS27C512F-90DMB	90	28 Pin CERDIP, 0.6″	D2	Military	MIL-STD-883C

1 Meg (128K × 8) BYTE-WIDE EPROM

KEY FEATURES

- **Compatible with JEDEC 27256 and 27512 EPROMs**
- **Simplified Upgrade Path**
  - — V_{PP} and PGM Are "Don't Care" During Normal Read Operation
- **EPI Processing**
  - — Latch-Up Immunity to 200 mA
  - — ESD Protection Exceeds 2000 Volts
- **Fast Programming**
  - — 15 Seconds Typical
- **High Performance CMOS**
  - — 90 ns Access Time
  - — 65 mA Active Power
- **JEDEC Standard Pin Configuration**
  - — 32 Pin Dip Package

3

GENERAL DESCRIPTION

The WS27C010L is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs allows upgrades from 16K through 512K EPROMs. The "Don't Care" feature during read operations allows memory expansions up to 8M bits with no printed circuit board changes.

The WS27C010L can directly replace lower density 28-pin EPROMs by adding an A_{16} address line and V_{CC} jumper. During the normal read operation PGM and V_{PP} are in a "don't care" state which allows higher order addresses, such as A_{17}, A_{18}, and A_{19} to be connected without affecting the normal read operation. This allows memory upgrades to 8M bits without hardware changes. The WS27C010L will also be offered in a 32-pin plastic Dip with the same upgrade path.

The WS27C010L provides microprocessor-based systems with extensive storage capacity for large portions of operating system and application software. Its 90-ns access time provides no-wait-state operation with high-performance CPUs such as the 16-MHz 80186. The WS27C010L offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The WS27C010L is one of a three product megabit EPROM family. Other family members are the WS57C010F and WS57C210F. The WS57C010F is the high-speed version of the WS27C010L. The WS57C210F is organized in a 64K × 16 configuration which is optimal for wordwide systems.

The WS27C010L is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS27C010L-90	WS27C010L-12	WS27C010L-15
Address Access Time (Max)	90 ns	120 ns	150 ns
Chip Select Time (Max)	90 ns	120 ns	150 ns
Output Enable Time (Max)	30 ns	40 ns	50 ns

NOTE: Plastic Dip will be available in the second half of 1988.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltages on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

DC CHARACTERISTICS $0°C \leq T_A \leq +70°C$; V_{CC} (Comm'l/Military) = +5V ± 10%

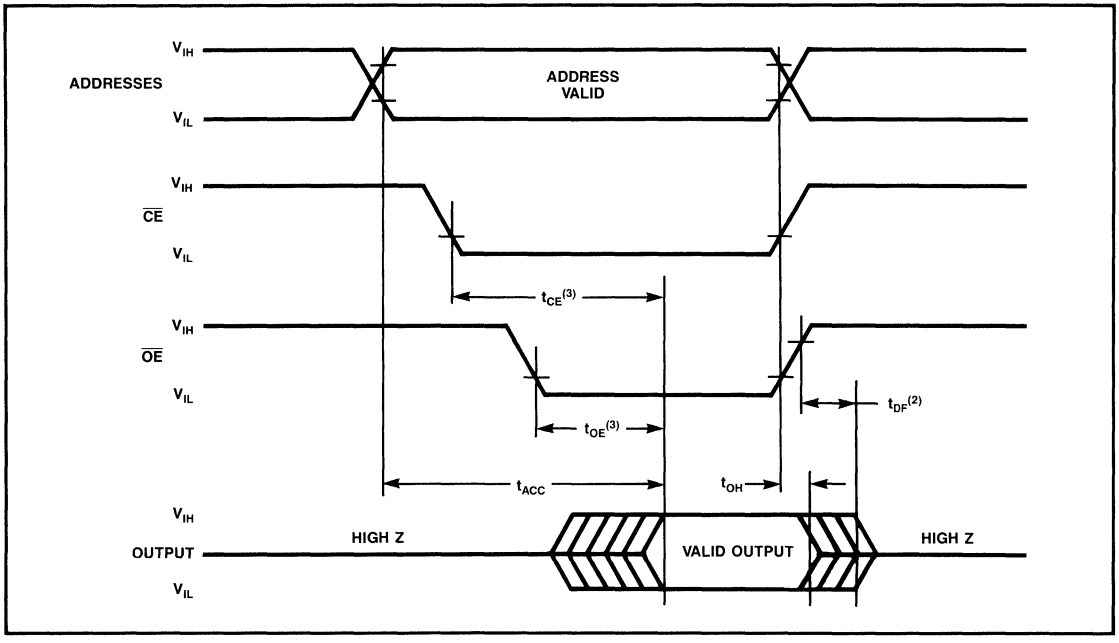
SYMBOL	PARAMETER	CONDITIONS	LIMITS		
			MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP1}(1)	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} (TTL)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		2	mA
I_{SB} (CMOS)	V_{CC} Current Standby	$\overline{CE}$ = V_{CC}		100	µA
I_{CC1}(1)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		40	mA
I_{CC2} (CMOS)	V_{CC} Active Current (Note 3)	$\overline{CE}$ = $\overline{OE}$ = 0V		14	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} +1	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.4		V
V_{PP}(1)	V_{PP} Read Voltage	V_{CC} = 5.0V ± 0.25	−0.1	V_{CC} +1	V

AC CHARACTERISTICS $0°C \leq T_A \leq +70°C$

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	WS27C010L-90		WS27C010L-12		WS27C010L-15		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		90		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		90		120		150	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		30		40		50	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	30	0	40	0	50	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		0		

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. A.C. current component adds 2.5 mA per MHz.

A.C. WAVEFORMS

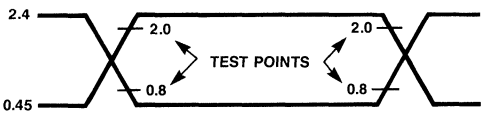


NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE(2) T_A = 25°C, f = 1 MHz

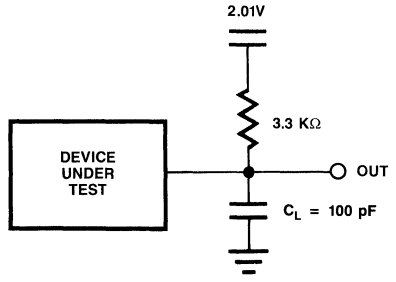
SYMBOL	PARAMETER	CONDITIONS	TYP(1)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

MODE SELECTION

The modes of operation of the WS27C010L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for device signature.

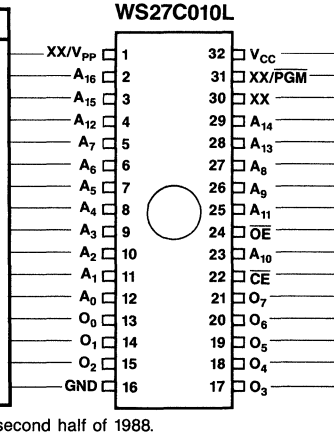
Table 1. Modes Selection

MODE \ PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[1]	X	X	X	5.0V	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	V_{CC}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	V_{CC}	High Z
Signature	Manufacturer[3]	V_{IL}	V_{IL}	X	V_H[2]	V_{IL}	X	5.0V	23 H
	Device[3]	V_{IL}	V_{IL}	X	V_H[2]	V_{IH}	X	5.0V	C1 H

NOTES:
1. X can be V_{IL} or V_{IH}
2. V_H = 12.0V ±0.5V
3. A_1–A_8, A_{10}–A_{16} = V_{IL}

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27512	27256
A_{19}	XX/V_{PP}	XX/V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



27256	27512	2 Mbit	4 Mbit	8 Mbit
		V_{CC}	V_{CC}	V_{CC}
		XX/$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTES: 1. Plastic Dip will be available in the second half of 1988.
2. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C010L pins.

PIN NAMES

A_0–A_{19}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS27C010L-90D	90	32 Pin CERDIP, 0.6″	D4	Comm'l	Standard
WS27C010L-12D	120	32 Pin CERDIP, 0.6″	D4	Comm'l	Standard
WS27C010L-12DMB	120	32 Pin CERDIP, 0.6″	D4	Military	MIL-STD-883C
WS27C010L-15D	150	32 Pin CERDIP, 0.6″	D4	Comm'l	Standard
WS27C010L-15DMB	150	32 Pin CERDIP, 0.6″	D4	Military	MIL-STD-883C

1 Meg (128K x 8) BYTE-WIDE EPROM

KEY FEATURES

- **Ultra-High Performance**
  - 55 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **Pin Compatible with WS27C010L**
- **Fast Programming**
  - 15 Seconds Typical
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 32 Pin Dip Package

GENERAL DESCRIPTION

The WS57C010F is an ultra-high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128 K-words of 8 bits each. The 55 ns access time of the WS57C010F enables it to operate in high performance systems. The "Don't Care" feature during read operations allows memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require sub-70 ns memory access times to operate at or near full speed. The WS57C010F enables such systems to incorporate operating systems and/or applications software into EPROM. This enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS57C010F pin configuration was established to enable memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 31 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins (see Figure 2). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS57C010F is part of a three product megabit EPROM family. Other family members are the WS27C010L and WS57C210F. The WS27C010L is the standard speed version of the WS57C010F. The WS57C210F is organized in a 64K x 16 configuration which is optimal for a word-wide system.

The WS57C010F is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS57C010F-55	WS57C010F-70
Address Access Time (Max)	55 ns	70 ns
Chip Select Time (Max)	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +125°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.6V to +7V
V_{PP} with Respect to Ground . . . . . −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground . . . . . −0.6V to +7V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

DC CHARACTERISTICS $0°C \leq T_A \leq +70°C$; V_{CC} (Comm'l/Military) = +5V ± 10%.

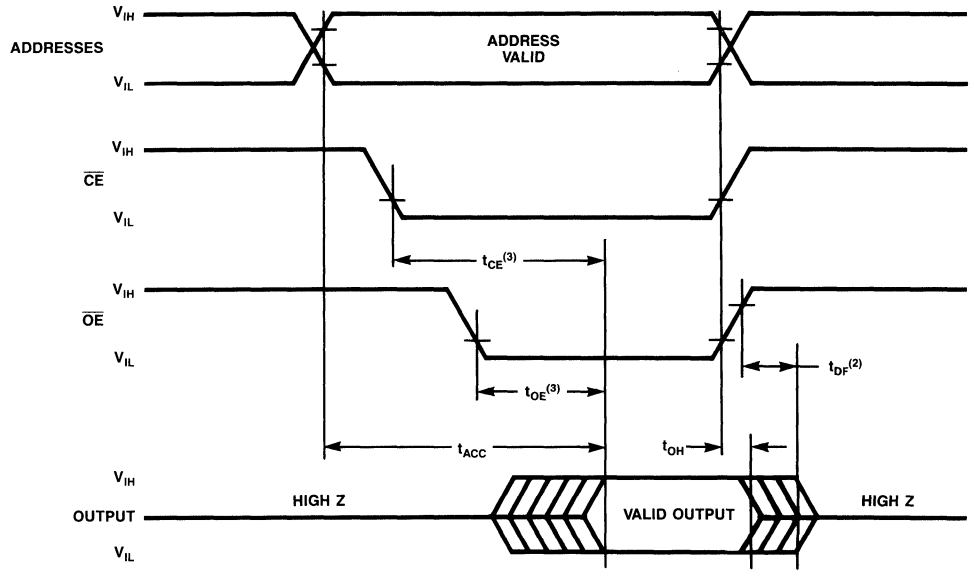
SYMBOL	PARAMETER	CONDITIONS	LIMITS		
			MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP1}(1)	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} TTL	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		2	mA
I_{SB} CMOS	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		500	µA
I_{CC1}(1)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		60	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 16 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA	2.4		V
V_{PP}(1)	V_{PP} Read Voltage	V_{CC} = 5.0V ± 0.25	−0.1	V_{CC}+1	V

AC CHARACTERISTICS $0°C \leq T_A \leq +70°C$

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	WS57C010F-55		WS57C010F-70		UNITS
			MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	20	0	25	ns
t_{OH}	Output Hold From Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		ns

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

A.C. WAVEFORMS

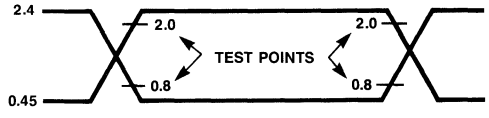


NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE[2] T_A = 25°C, f = 1 MHz

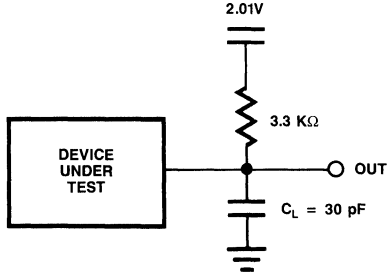
SYMBOL	PARAMETER	CONDITIONS	TYP[1]	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

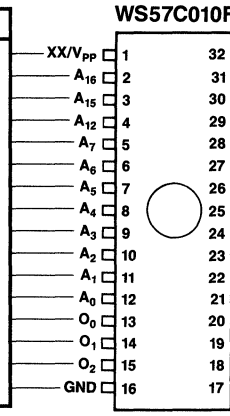
A.C. TESTING LOAD CIRCUIT



C_L = 30 pF
C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	27512	27256
A_{19}	XX/V_{PP}	XX/V_{PP}		
A_{16}	A_{16}	A_{16}		
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



27256	27512	2 Mbit	4 Mbit	8 Mbit
		V_{CC}	V_{CC}	V_{CC}
		XX/PGM	A_{18}	A_{18}
V_{CC}	V_{CC}	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
OE	OE/V_{PP}	OE	OE	OE/V_{PP}
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
CE	CE	CE	CE	CE
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

NOTES: 1. Plastic Dip will be available in the second half of 1988.
2. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS57C010F pins.

PIN NAMES

A_0–A_{19}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C010F-55D	55	32 Pin CERDIP, 0.6″	D4	Comm'l	Standard
WS57C010F-70D	70	32 Pin CERDIP, 0.6″	D4	Comm'l	Standard
WS57C010F-70DMB	70	32 Pin CERDIP, 0.6″	D4	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

HIGH SPEED 4K x 16 WORDWIDE CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  — 55ns
- **Low Power Consumption**
- **Ideal for 16/32 bit Processors**
  — TMS320, 68000, 80386, etc.
- **2 to 1 Package Reduction**
- **30% + Space Savings**
- **Single Chip Solution**
- **Compatible with JEDEC pinout**

GENERAL DESCRIPTION

The WS57C65 is an extremely High Performance EPROM based memory with a 4K x 16 architecture. It is manufactured in an advanced CMOS process which consumes very little power while operating at speeds which rival that of bipolar PROMs.

The major features of the WS57C65 are its 4K x 16 architecture and its high speed. This combination makes the WS57C65 an ideal solution for applications which utilize 16/32 bit data paths. Examples include systems which are based on such processors as the TMS320 family of DSP processors as well as high performance general purpose processors such as the MC68000 family and the 80286 and 80386 microprocessors.

The word wide architecture of the WS57C65 results in a 2 to 1 savings in EPROM component count and a minimum 30% savings in board space.

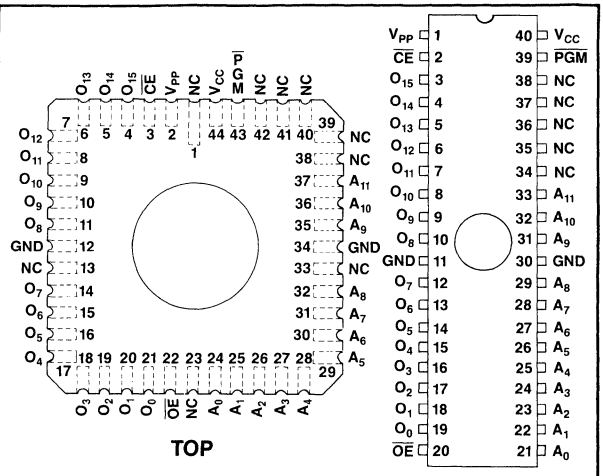
The pin configuration utilized is upward compatible with the JEDEC standard pinout for word wide EPROMs. This allows an easy upgrade path to higher density memories such as the WS57C257. No board changes or jumper wires are required to complete the upgrade.

MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.
*For Signature, $A_9 = 12V$, A_0 is toggled, and all other address are at TTL low. $A_0 = V_{IL}$ = MFGR 0023H, $A_0 = V_{IH}$ = DEVICE 00B1H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C65-55	WS57C65-70
Address Access Time	55ns	70ns
Chip Select Time	55ns	70ns
Output Enable Time	25ns	30ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65° to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
V_{PP} with Respect to GND . . . . . −0.6V to +14V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range. (See Above)

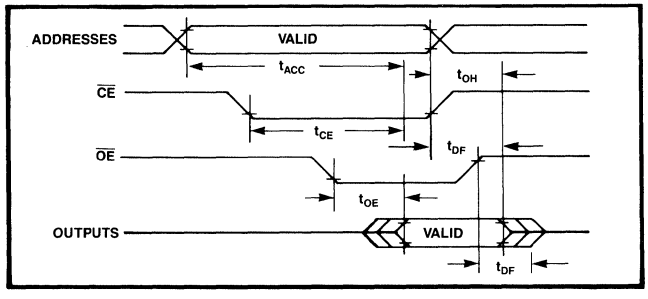
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX		UNITS
V_{OL}	Output Low Voltage	I_{OL} = 16 mA			0.4		V
V_{OH}	Output High Voltage	I_{OH} = −4 mA		2.4			V
I_{SB1}	V_{CC} Standby Current (CMOS)	Notes 1 and 3			500		µA
I_{SB2}	V_{CC} Standby Current (TTL)	Notes 3 and 3			20		mA
I_{CC1}	Active Current (CMOS)	Note 1	Comm'l		35	(Note 4)	mA
			Military		45		
I_{CC2}	V_{CC} Active Current (TTL)	Note 2	Comm'l		45	(Note 4)	mA
			Military		55		
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100		µA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}		V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−10	10		µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10		µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. Standby power component is 1 mA/MHz (Power = AC + DC).
4) A.C. Active power component is 3 mA/MHz (Power = AC + DC).

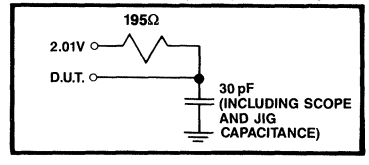
AC READ CHARACTERISTICS Over Operating Range. (See Above)

PARAMETER	SYMBOL	WS57C65-55		WS57C65-70		WS57C65-90		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70		90	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70		90	
$\overline{OE}$ to Output Delay	t_{OE}		20		25		30	
Output Disable to Output Float	t_{DF}		20		25		30	
Address to Output Hold	t_{OH}	0		0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	-10	10	μA
Vpp Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		50	mA
V_{CC} Supply Current	I_{CC}		35 (Note 4)	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 8mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −2mA)	V_{OH}	2.4		V

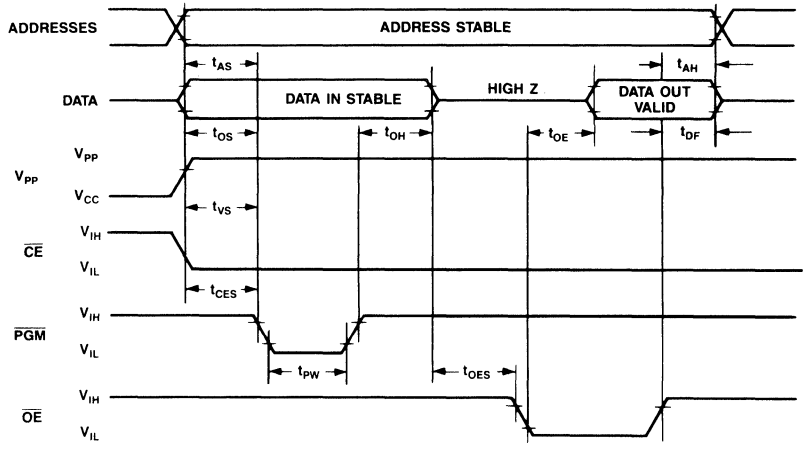
NOTES:
6) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
7) V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 13.5 volts or vice-versa.
8) During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2	-		μs
Chip Enable Setup Time	t_{CES}	2	-		μs
Output Enable Setup Time	t_{OES}	2	-		μs
Data Setup Time	t_{OS}	2	-		μs
Address Hold Time	t_{AH}	0	-		μs
Data Hold Time	t_{OH}	2	-		μs
Chip Disable to Output Float Delay	t_{DF}	0	-	130	ns
Data Valid from Output Enable	t_{OE}		-	130	ns
Vpp Setup Time	t_{VS}	2	-		μs
PGM Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single shot programming algorithms should use a single 10 ms pulse.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C65 has all 4096×16 bits in the "1," or high state. "0's" are loaded into the WS57C65 through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin, +5.75V is applied to V_{CC}, and $\overline{CE}$ is at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C65 to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C65. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000µ W/cm^2 for 20 minutes. The WS57C65 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C65 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C65 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C65-55D	55	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WS57C65-70CMB	70	44 Pad CLLCC	C3	Military	MIL-STD-883C
WS57C65-70D	70	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WS57C65-70DMB	70	40 Pin CERDIP, 0.6″	D3	Military	MIL-STD-883C

HIGH-SPEED 4K × 16 CMOS EPROM WITH MUX I/O

KEY FEATURES

- **Fast Access Time**
  - — 55 ns — Commercial
  - — 70 ns — Military
- **Multiplexed I/O**
  - — Interfaces Directly to a 16-Bit Multiplexed Bus
  - — Address Latched on Chip
- **4 to 1 Package Reduction**
- **Low Power Consumption**
- **Chip Select Can be Latched (FT = 0) or Unlatched (FT = 1)**
- **28-Pin Cerdip Package**
- **Supported by the WSI MagicPro™ Engineering Programmer**

3

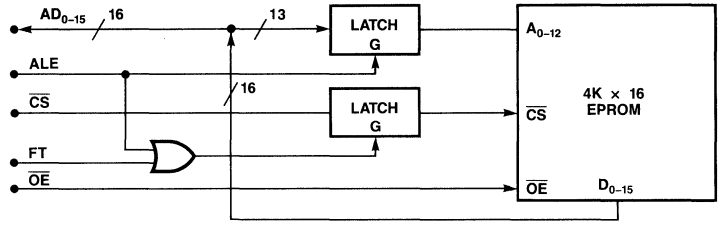
GENERAL DESCRIPTION

The WS57C66 is a high-performance CMOS EPROM memory in a 4K × 16 architecture that interfaces directly to a multiplexed bus. The address and data are multiplexed enabling the circuit to be housed in a 28 pin DIP package. The ALE input latches the address in the input latches when low. The latches are transparent when the ALE is high.

The $\overline{CS}$ to the WS57C66 can be latched for a maximum savings of 4 packages (FT = 0) or 2 packages when FT = 1.

The WS57C66 is an ideal solution for microprocessors or microcontrollers with multiplexed address and data busses.

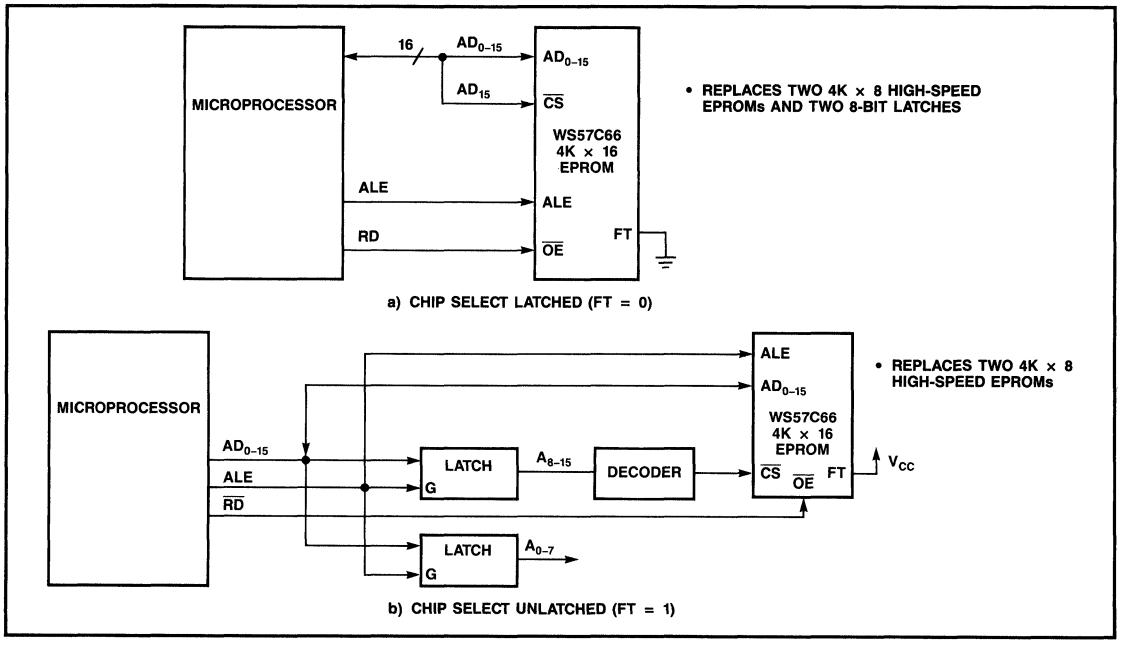
FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTION GUIDE

PARAMETER	WS57C66-55	WS57C66-70	UNITS
Address Access Time	55	70	ns
Chip Select Time	55	70	ns
Output Enable Time	20	25	ns

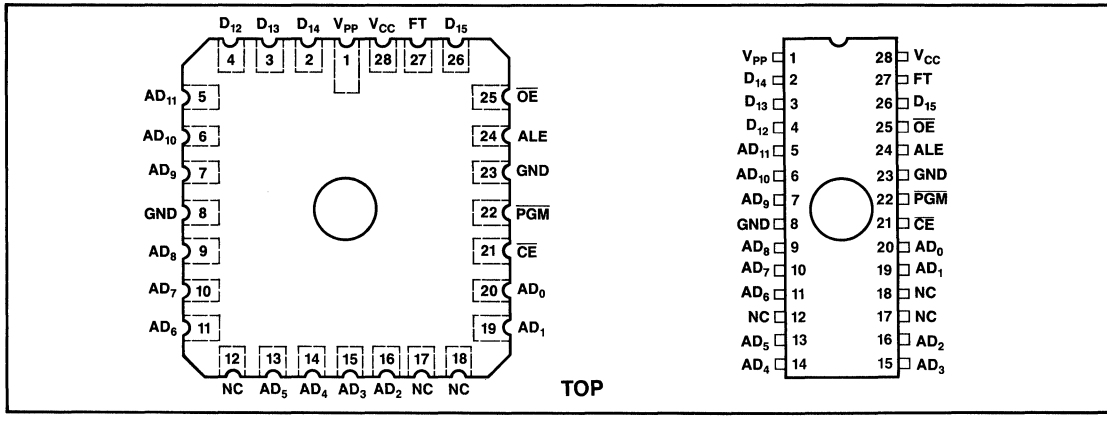
SYSTEM INTERFACE



MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z

WS57C66 PIN ASSIGNMENTS



ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . . −65°C to +150°C
Voltage to any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14.0V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

3

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

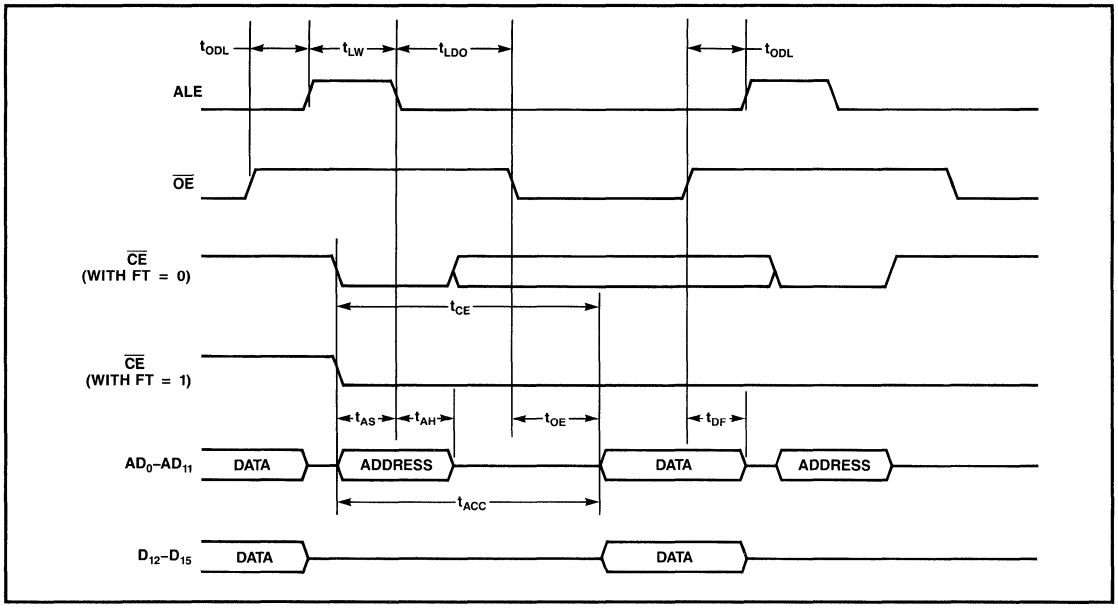
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX		UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4		V
V_{OH}	Output High Voltage	I_{OH} = −2 mA		2.4			V
I_{SB1}	V_{CC} Standby Current (CMOS)	Note 1			15 (Note 3)		mA
I_{SB2}	V_{CC} Standby Current (TTL)	Note 2			20 (Note 3)		mA
I_{CC1}	Active Current (CMOS)	Note 1	Comm'l		35	(Note 4)	mA
			Military		45		
I_{CC2}	V_{CC} Active Current (TTL)	Note 2	Comm'l		45	(Note 4)	mA
			Military		55		
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			100		µA
V_{PP}	V_{PP} Read Voltage			$V_{CC}-0.4$	V_{CC}		V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−10	10		µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10		µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. standby power component is 1 mA/MHz (Power = AC + DC).
4) A.C. active power component is 3 mA/MHz (Power = AC + DC).

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$

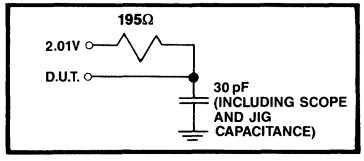
PARAMETER	SYMBOL	WS57C66-55		WS57C66-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	ns
$\overline{OE}$ to Output Delay	t_{OE}		20		25	ns
Output Disable to Output Float	t_{DF}		20		25	ns
Address Setup Time	t_{AS}	6		8		ns
Address Hold Time	t_{AH}	10		12		ns
Latch Pulse Width	t_{LW}	10		12		ns
Output Disable to Latch Enable	t_{ODL}	0		0		ns
Latch Disable to Output Enable	t_{LDO}	10		12		ns

AC READ TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: .8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Leakage Current $V_{IN} = V_{CC}$ or GND	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse (CE = PGM = V_{IL})	I_{PP}		40	mA
V_{PP} Supply Current	I_{CC}		35 (Note 5)	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 8 mA)	V_{OL}		0.45	V
Output High Voltage During Verify (I_{OH} = −2 mA)	V_{OH}	2.4		V

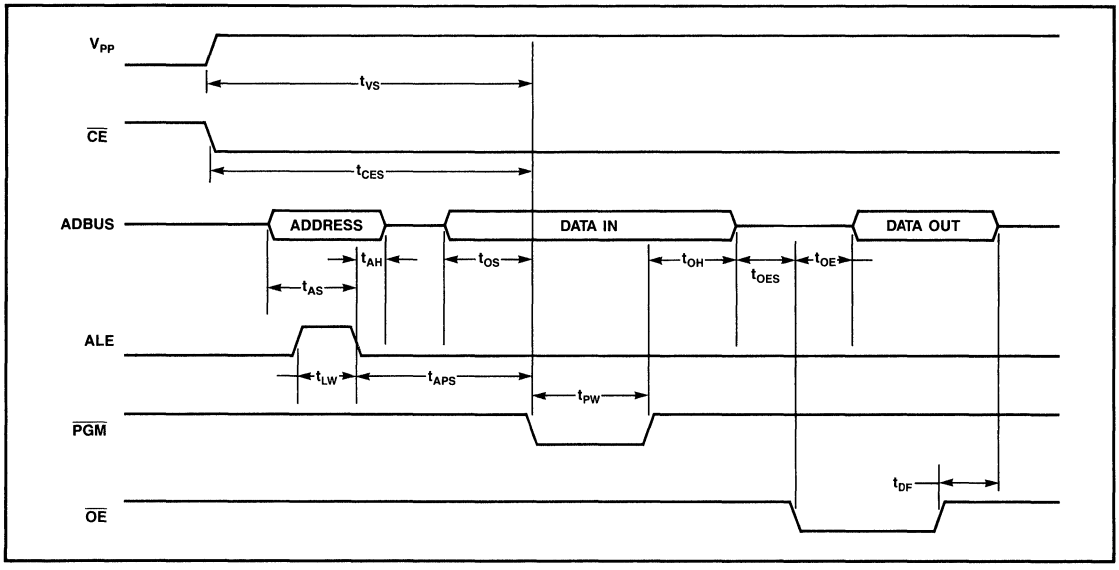
NOTES: 5) V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
6) V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
7) During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 5.50V ± 5%, V_{PP} = 12.5 ± 0.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	10			ns
Address Hold Time	t_{AH}	14			ns
Latch Pulse Width	t_{LW}	14			ns
Address Setup Time to PGM	t_{APS}	2			µs
Chip Enable Setup Time	t_{CES}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Data Hold Time	t_{OH}	2			µs
Output disable to Output Float	t_{DF}	0		130	ns
Data Valid From Output Enable	t_{OE}			130	ns
V_{PP} Setup Time	t_{VS}	2			µs
PGM Pulse Width	t_{PW}	1	5		ms

3

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C66 has all 8192 x 8 bits in the "1" or high state. "0's" are loaded into the WS57C66 through the procedure of programming.

The programming mode is entered when +12.5V is applied to the V_{PP} pin and $\overline{CE}$ is at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C66 to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase a WS57C66. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstroms (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WS57C66 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C66 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C66 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C66-55D	55	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C66-70CMB	70	32 Pad CLLCC	C2	Military	MIL-STD-883C
WS57C66-70D	70	28 Pin CERDIP, 0.6"	D2	Comm'l	Standard
WS57C66-70DM	70	28 Pin CERDIP, 0.6"	D2	Military	Standard
WS57C66-70DMB	70	28 Pin CERDIP, 0.6"	D2	Military	MIL-STD-883C

HIGH SPEED 16K X 16 WORDWIDE CMOS EPROM

KEY FEATURES

- **Fast Access Time**
  - 55 ns
- **Low Power Consumption**
- **Ideal for 16/32 Bit Processors**
  - TMS320, 68000, 80386, etc.
- **16 Bit Data Bus**
- **Simplifies Board Routing**
- **Single Chip Solution**
- **Compatible with JEDEC pinout**

GENERAL DESCRIPTION

The WS57C257 is an extremely High Performance EPROM based memory with a 16K x 16 architecture. It is manufactured in an advanced CMOS process which consumes very little power while operating at speeds which rival that of bipolar PROMs.

The major features of the WS57C257 are its 16K x 16 architecture and its high speed. This combination makes the WS57C257 an ideal solution for applications which utilize 16/32 bit data paths. Examples include systems which are based on such processors as the TMS320 family of DSP processors as well as high performance general purpose processors such as the MC68000 family and the 80286 and 80386 microprocessors.

The wordwide architecture of the WS57C257 results in a 4 to 1 savings in EPROM component count and a minimum 60% savings in board space.

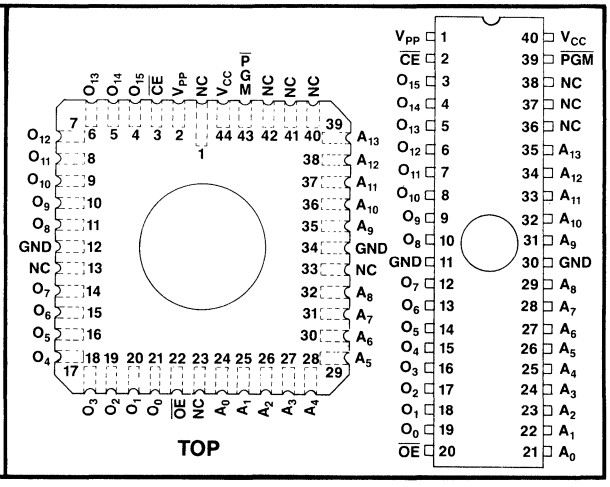
The pin configuration utilized is upward compatible with the JEDEC standard pinout for word wide EPROMs. This allows an easy upgrade path from lower density memories such as the WS57C65. No board changes or jumper wires are required to complete the upgrade.

MODE SELECTION

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	X	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}
*For signature, $A_9 = 12V$, A_0 is toggled, and all other address are at TTL low. $A_0 = V_{IL}$ = MFGR 0023H. $A_0 = V_{IH}$ = DEVICE 00B2H.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

PARAMETER	WS57C257-55	WS57C257-70
Address Access Time	55ns	70ns
Chip Select Time	55ns	70ns
Output Enable Time	25ns	30ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -65°C to +150°C
Voltage on any pin with
respect to GND.....-0.6V to +7V
VPP with respect to GND ..... -0.6V to +14.0V
ESD Protection .....>2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

Range	Temperature	Vcc
Comm'l.	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

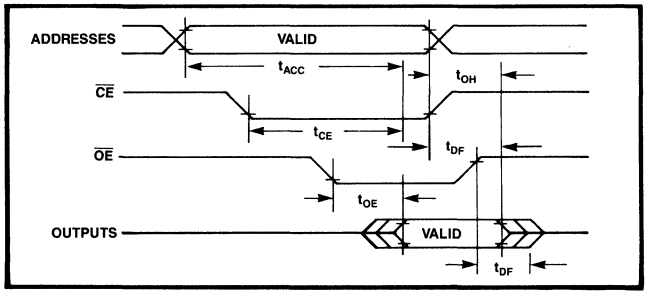
SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX		UNIT
V_{OL}	Output Low Voltage	I_{OL}= 8mA			0.4		V
V_{OH}	Output High Voltage	I_{OH}= – 2mA		2.4			V
I_{SB1}	Vcc Standby Current (CMOS)	Notes 1 and 3			500		µA
I_{SB2}	Vcc Standby Current (TTL)	Notes 2 and 3			20		mA
I_{CC1}	Active Current (CMOS)	Note 1	Comm'l.		40	(Note 4)	mA
			Military		50		
I_{CC2}	Vcc Active Current (TTL)	Note 2	Comm'l.		50	(Note 4)	mA
			Military		60		
I_{PP}	Vpp Supply Current	V_{PP}= Vcc			100		µA
V_{PP}	Vpp Read Voltage			Vcc - 0.4	Vcc		V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		- 10	10		µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		- 10	10		µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$.
3) A.C. standby power component is 1 mA/MHz.
4) A.C. active power component is 3 mA/MHz (Power = AC + DC).

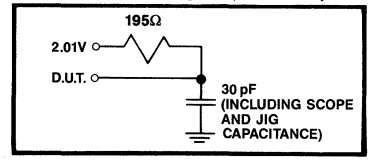
AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

PARAMETER	SYMBOL	WS57C257-55		WS57C257-70		UNITS
		MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		55		70	ns
$\overline{CE}$ to Output Delay	t_{CE}		55		70	
$\overline{OE}$ to Output Delay	t_{OE}		25		30	
Output Disable to Output Float	t_{DF}		25		30	
Address to Output Hold	t_{OH}	0		0		

AC READ TIMING DIAGRAM



TEST LOAD (High Impedance Systems)



TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 0.8 and 2.0V

PROGRAMMING INFORMATION

DC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{pp} = 12.5 \pm 0.5V$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd)	I_{LI}	-10	10	μA
Vpp Supply Current During Programming Pulse ($\overline{CE} = \overline{PGM} = V_{IL}$)	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		35 (Note 4)	mA
Input Low Level	V_{IL}	-0.1	0.8	V
Input High Level	V_{IH}	2.0	$V_{CC} + 0.3$	V
Output Low Voltage During Verify ($I_{OL} = 8mA$)	V_{OL}		0.45	V
Output High Voltage During Verify ($I_{OH} = -2mA$)	V_{OH}	2.4		V

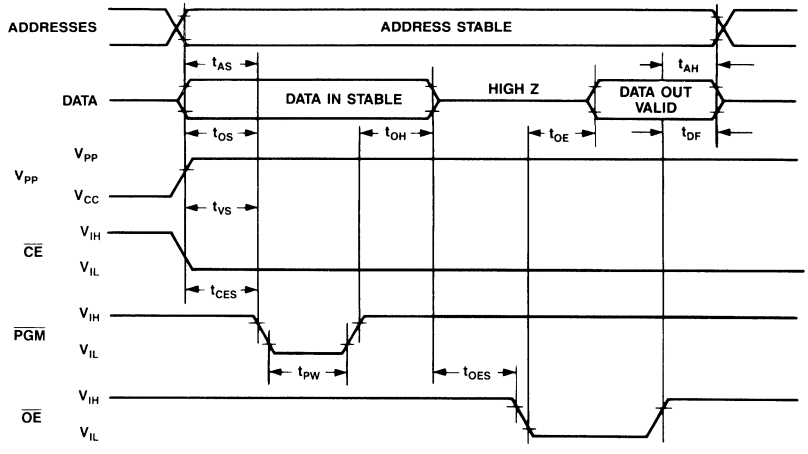
NOTES: 6) Vcc must be applied either coincidentally or before Vpp and removed either coincidentally or after Vpp.
7) Vpp must not be greater than 14 volts including overshoot. During $\overline{CE} = \overline{PGM} = V_{IL}$, Vpp must not be switched from 5 volts to 13.5 volts or vice-versa.
8) During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to Vpp.

AC CHARACTERISTICS ($T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{pp} = 12.5 \pm 0.5V$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Setup Time	t_{AS}	2	-		μs
Chip Enable Setup Time	t_{CES}	2	-		μs
Output Enable Setup Time	t_{OES}	2	-		μs
Data Setup Time	t_{OS}	2	-		μs
Address Hold Time	t_{AH}	0	-		μs
Data Hold Time	t_{OH}	2	-		μs
Chip Disable to Output Float Delay	t_{DF}	0	-	130	ns
Data Valid from Output Enable	t_{OE}		-	130	ns
Vpp Setup Time	t_{VS}	2	-		μs
PGM Pulse Width	t_{PW}	1	3	10	ms

NOTE: Single shot programming algorithms should use one 10 ms pulse per word.

PROGRAMMING WAVEFORM



PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WS57C257 has all 16,384×16 bits in the "1," or high state. "0's" are loaded into the WS57C257 through the procedure of programming.

The programming mode is entered when +13.5V is applied to the V_{PP} pin, +5.5V is applied to V_{CC}, and $\overline{CE}$ is taken to V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 16-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WS57C257 to an ultra-violet light source. A dosage of 15W second/cm^2 is required to completely erase a WS57C257. This dosage can be obtained by exposure to an ultra-violet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000µ W/cm^2 for 20 minutes. The WS57C257 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WS57C257 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WS57C257 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMERS

Data I/O Unipak 2B, software version 13 or later, family/pinout code 1F/E1; WSI's MagicPro™ IBM PC Compatible Engineering Programmer.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C257-55D	55	40 Pin CERDIP, 0.6"	D3	Comm'l	Standard
WS57C257-70CMB	70	44 Pad CLLCC	C3	Military	MIL-STD-883C
WS57C257-70D	70	40 Pin CERDIP, 0.6"	D3	Comm'l	Standard
WS57C257-70DMB	70	40 Pin CERDIP, 0.6"	D3	Military	MIL-STD-883C

1 Meg (64K × 16) WORD-WIDE EPROM

KEY FEATURES

- **Ultra-High Performance**
  - 55 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **Fast Programming**
  - 15 Seconds Typical
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 40 Pin Dip Package

GENERAL DESCRIPTION

The WS57C210F is an ultra-high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 64 K-words of 16 bits each. The 55 ns access time of the WS57C210F enables it to operate in high performance systems. The "Don't Care" feature during read operations allows memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require sub-70 ns memory access times to operate at or near full speed. The WS57C210F enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS57C210F pin configuration was established to allow memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 39 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins (see Figure 2). When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS57C210F is part of a three product megabit EPROM family. Other family members are the WS27C010L and WS57C010F. The standard speed WS27C010L is organized in a 128K × 8 configuration. The WS57C010F is the high-speed version of the WS27C010L.

The WS57C210F is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	WS57C210F-55	WS57C210F-70
Address Access Time (Max)	55 ns	70 ns
Chip Select Time (Max)	55 ns	70 ns
Output Enable Time (Max)	20 ns	25 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +125°C
Voltages on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7V
ESD Protection ..... >2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ OPERATION

DC CHARACTERISTICS $0°C \leq T_A \leq +70°C$; V_{CC} (Comm'l/Military) = +5V ± 10%

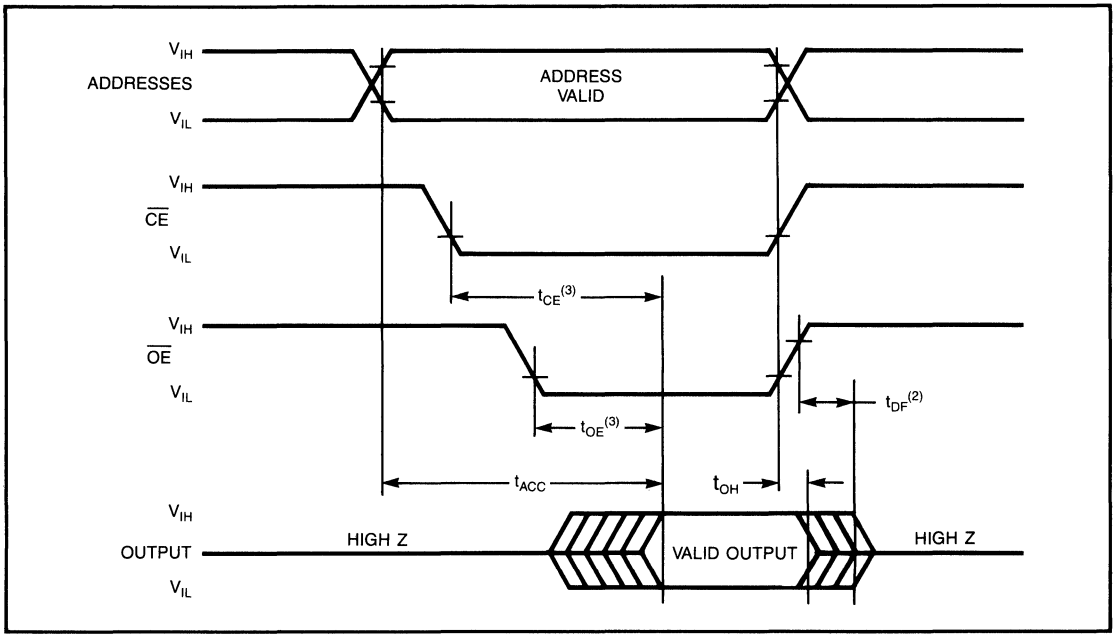
SYMBOL	PARAMETER	CONDITIONS	LIMITS		
			MIN	MAX	UNITS
I_{LI}	Input Load Current	V_{IN} = 5.5V		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V		10	µA
I_{PP1}(1)	V_{PP} Load Current	$V_{PP} \leq V_{CC}$		10	µA
I_{SB} (TTL)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		2	mA
I_{SB} (CMOS)	V_{CC} Current Standby	$\overline{CE}$ = V_{IH}		500	µA
I_{CC1}(1)	V_{CC} Current Active	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		75	mA
V_{IL}	Input Low Voltage		−0.1	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2 mA	2.4		V
V_{PP}(1)	V_{PP} Read Voltage	V_{CC} = 5.0V ± 0.25	−0.1	V_{CC}+1	V

AC CHARACTERISTICS $0°C \leq T_A \leq +70°C$

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	WS57C210F-55		WS57C210F-70		UNITS
			MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		55		70	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		55		70	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25	ns
t_{DF}(2)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}	0	20	0	25	ns
t_{OH}	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0		0		ns

NOTES:
1. V_{PP} should be at a TTL level except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

A.C. WAVEFORMS

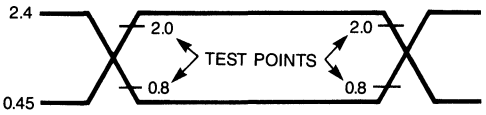


NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE(2) T_A = 25°C, f = 1 MHz

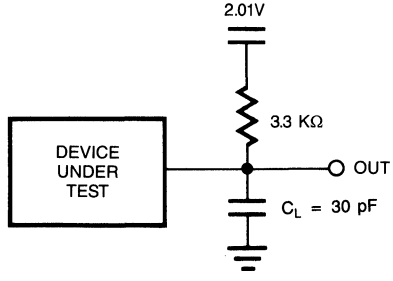
SYMBOL	PARAMETER	CONDITIONS	TYP(1)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

A.C. TESTING INPUT/OUTPUT WAVEFORM



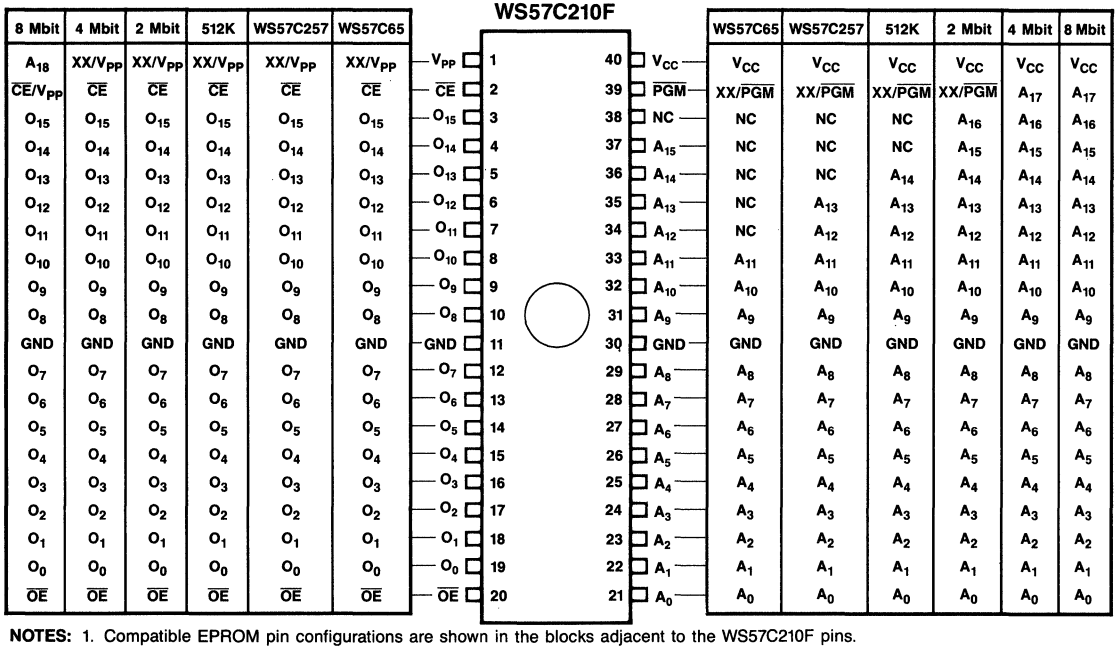
A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 30 pF
C_L includes Jig Capacitance

DIP PIN CONFIGURATIONS



NOTES: 1. Compatible EPROM pin configurations are shown in the blocks adjacent to the WS57C210F pins.
2. Plastic Dip Availability is scheduled for second half 1988.

PIN NAMES

A_0–A_{19}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
NC	No Connection
XX	Don't Care (During Read)

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS57C210F-55D	55	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WS57C210F-70D	70	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WS57C210F-70DMB	70	40 Pin CERDIP, 0.6″	D3	Military	MIL-STD-883C

HIGH-SPEED MAPPABLE MEMORY (MAP™)

KEY FEATURES

- **Super Fast Access Time**
  - — EPROM/SRAM: 40 ns (including decode)
  - — Chip Select Outputs: 22 ns
- **High Density UV Erasable EPROM**
  - — 128K Bits
- **High Density 6-Transistor Static RAM**
  - — 32K Bits
- **On-Board Programmable Address Decoder**
  - — Eliminates External Chip-Select Decode Components and Delay
- **Code Security**
  - — Contains Programmable Security Bit
- **Addressable Range**
  - — 512K Bytes or 256K Words
- **Block Resolution**
  - — 2K Bytes or 1K Words
- **Eight Chip Select Outputs**
  - — Control I/O and Other System Devices
- **Fully User Configurable**
  - — Byte or Word Operation
- **Reduces Board Space**
  - — Simplifies Routing
  - — Replaces 2 or more EPROMs, 2 or more SRAMs and One Decoder

GENERAL DESCRIPTION

The WSMAP162 and WSMAP161 are Mapped Address Programmable (MAP™) memory products that integrate 128K bits of EPROM, 32K bits of SRAM and a Programmable Mapping Decoder (PMD™) into a single 40-pin package. With a wide input addressing range, these memory products are compatible with large address space processor systems. The on-board PMD™ enables the placement of physical 16K bytes or 8K words of EPROM and 4K bytes or 2K words of SRAM anywhere in a total address space of 512K bytes or 256K words respectively. The PMD™ reduces system component count as well as board space, enhances performance and increases data security. The major feature of this product is the integration of high speed, high density UV erasable EPROM and a CMOS SRAM along with decoding logic on a single chip.

The WSMAP162 is ideal for use with digital signal processors such as the TMS320XX series. Its data path can be programmed as either 8 or 16 bits. With the provision of Pin 2 programmable as either Chip Select ($\overline{CSI}$) or the highest address bit, its address range is from 128K to 256K words or 256K to 512K bytes. The EPROM architecture is 16K × 8 (byte operations) or 8K × 16 (word operations). The SRAM architecture is 4K × 8 (byte operations) or 2K × 16 (word operations).

The 16-bit data path WSMAP161 is used with microcontrollers and microprocessors using a 16-bit data bus. With Pin 39 as $\overline{BHE}$ (Byte High Enable), the WSMAP161 can accomodate either full word or byte operations (for those 16-bit processors capable of byte operations). Its addressing range is from 64K words to 128K words (see pin 2 above). Its EPROM is 8K × 16 and its SRAM is 2K × 16.

Refer to Application Note 002 in this databook for additional information.

BLOCK DIAGRAM

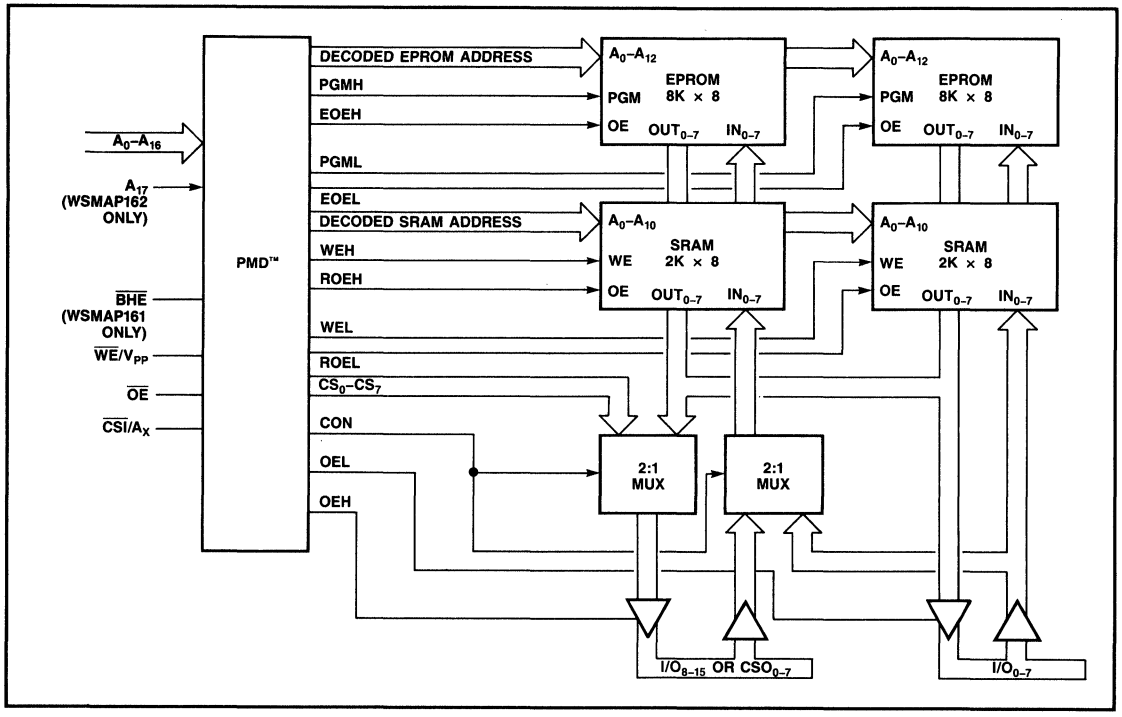


TABLE 1. PRODUCT SELECTION GUIDE

PARAMETER	WSMAP162-40 WSMAP161-40	WSMAP162-45 WSMAP161-45	WSMAP162-55 WSMAP161-55	UNITS
Address Access Time (Max.)	40	45	55	ns
Chip Select ($\overline{CSI}$) Access Time (Max.)	40	45	55	ns
Output Enable ($\overline{OE}$) Access Time (Max.)	18	21	23	ns
Chip Select Output Delay (Max)	22	25	27	ns

TECHNICAL DESCRIPTION

Internally the memory is organized as two 8K x 8 EPROMs and two 2K x 8 SRAMs. The MAP™ memory can be configured for byte or wordwide operations during the EPROM and PMD™ programming operation by programming the configuration (CON) bit. In the wordwide operation, the I/Os of the two EPROMs and two SRAMs are common and are brought out in parallel. In the byte wide operation, the 8 most significant bits of the I/O are multiplexed with the 8 least significant bits using a multiplexer controlled by address bit A_0. An important feature offered with the byte wide configuration is the 8 most significant I/O bits are replaced by 8 individual chip select outputs (CSO_0–CSO_7) which can be programmed to select and control other devices (I/O, SRAM, DRAM, etc.).

The PMD™ enables the WSMAP162/WSMAP161 to directly interface with high speed microprocessors and digital signal processors which require 16K bytes (or 8K words) of EPROM program store and 4K bytes (or 2K words) of SRAM data store in a non-contiguous address space.

In the byte wide configuration, it is possible (by programming the PMD™) to subdivide and selectively access 8 blocks of EPROM each configured in a 2K x 8 architecture. Any one of these eight EPROM blocks can be mapped into any of the 256 available 2K deep blocks in a 512K byte address space. Similarly, the two blocks of SRAM configured as 2K x 8 can be mapped into any of the 256 2K blocks in a 512K byte address space (not occupied by the EPROM).

The physical blocks of EPROM and SRAM can be concatenated together to form a continuous sequentially addressable section of memory, placed in non-sequential addressable individual blocks or any combination of the two.

In the wordwide configuration, the EPROM and SRAM are organized as 1K × 16. The PMD™ is used to map the 8 blocks of EPROM and 2 blocks of SRAM into any of the 256 1K blocks in a 256K word address space.

Pin 2 can be configured as a normal address input ("A_X" or highest address bit) or as a chip select input ($\overline{CSI}$). This is done during the programming of the PMD™. When configured as an address input, this pin goes directly to the PMD™ and effectively doubles the address space. When configured as a chip select ($\overline{CSI}$), this pin provides a very low power stand-by mode when the chip is deselected.

In the WSMAP162, pin 39 is an address input (A_{17}) and in the WSMAP161 it is Byte High Enable ($\overline{BHE}$). As A_{17}, it functions as a normal address input. As $\overline{BHE}$, it is used in the ×16 (wordwide) configuration if byte operations are required. The combination of $\overline{BHE}$ and A_0 control the memory access for a word, upper byte, or lower byte operation. See table 4. This feature reduces the logic required in 16-bit microprocessors and microcontrollers capable of byte operations. If only word operations are required, $\overline{BHE}$ and A_0 should be connected to ground.

A security bit (SEC) bit is provided that functions as a "bridge" bit. After completion of programming the PMD™ and EPROM, this bit can be programmed (the "bridge" can be "burned"). This prevents external access to the PMD™ contents and inhibits duplication of the PMD™ data by routine copying.

The WSMAP162/WSMAP161 pin out is derived from the JEDEC standard WSI WS57C257 16K × 16 high speed EPROM, i.e., it is read compatible. This pinout enables memory expansion with future WSI mapped address products up to 512K bytes of physical memory. The process technology used in the WSMAP162/WSMAP161 is common to all of WSI's current family of high speed EPROM and RPROM™ memory products. Both the PMD™ and EPROM blocks are programmed using the WSI MagicPro™ IBM PC compatible engineering programmer. A menu driven software package for the IBM PC is provided from WSI to support the special PMD™ address mapping and configuration.

TABLE 2. MAP™ MEMORY CONFIGURATIONS

	WSMAP162 × 8		**WSMAP162 × 16**		**WSMAP161 × 16**	
Pin 2 Configured as	$\overline{CSI}$	A_X	$\overline{CSI}$	A_X	$\overline{CSI}$	A_X
Address Space	256K Bytes	512K Bytes	128K Words	256K Words	64K Words	128K Words
Block Size	2K Bytes	2K Bytes	1K Words	1K Words	1K Words	1K Words
Addressable Blocks	128	256	128	256	64	128
Available EPROM Blocks	8	8	8	8	8	8
Available SRAM Blocks	2	2	2	2	2	2
Number of Chip Select Outputs	8	8	0	0	0	0
EPROM Size Configuration	16K × 8	16K × 8	8K × 16	8K × 16	8K × 16	8K × 16
SRAM Size Configuration	4K × 8	4K × 8	2K × 16	2K × 16	2K × 16	2K × 16
Number of I/Os	8	8	16	16	16	16
Low Power Standby	Yes	No	Yes	No	Yes	No
Protected Mode	Yes	Yes	Yes	Yes	Yes	Yes
Byte Operations	N/A	N/A	No	No	Yes	Yes

NOTE: A_X is Highest Address Bit

TABLE 3. MODE SELECTION

PIN / MODE	$\overline{CSI}$	$\overline{OE}$	$\overline{WE}/V_{PP}$	ADDRESS	I/O CONFIGURED ×16, I/O_{0-15} CONFIGURED ×8, I/O_{0-7}	CHIP SELECTS CONFIGURED ×8, $\overline{CS0_0}$–$\overline{CS0_7}$
Read EPROM/SRAM	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Selected	D_{OUT}	CS_{OUT}
Read External	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Not Selected	High Z	CS_{OUT}
Output Disable	X	V_{IH}	X	X	High Z	CS_{OUT}
Stand-By	V_{IH}	X	X	X	High Z	CS_{OUT}
Write SRAM	V_{IL}	X	V_{IL}	SRAM Selected	D_{IN}	CS_{OUT}
Write External	V_{IL}	X	V_{IL}	No SRAM Selected	X	CS_{OUT}
Program EPROM	V_{IL}	V_{IH}	V_{PP}	EPROM Program Address	D_{IN}	D_{IN}
Program Verify EPROM	V_{IL}	V_{IL}	V_{IH}	EPROM Program Address	D_{OUT}	CS_{OUT}
Program PMD™	V_{IL}	V_{IH}	V_{PP}	PMD Program Address	D_{IN}	D_{IN}
Program Verify PMD™	V_{IL}	V_{IL}	V_{IH}	PMD Program Address	D_{OUT}	CS_{OUT}

TABLE 4. HIGH/LOW BYTE SELECTION TRUTH TABLE (IN ×16 CONFIGURATION ONLY)

$\overline{BHE}$ (PIN 39)	A_0	OPERATION
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

NOTE: $\overline{WR}$ and $\overline{BHE}$ are used for SRAM Functions

TABLE 5. DC READ CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX		UNITS
Output Low Voltage	V_{OL}	I_{OL} = 16 mA			0.4		V
Output High Voltage	V_{OH}	I_{OH} = −4 mA		2.4			V
V_{CC} Standby Current CMOS	I_{SB1}	Notes 1 and 3	Comm'l		10		mA
			Military		20		mA
V_{CC} Standby Current TTL	I_{SB2}	Notes 2 and 3	Comm'l		40		mA
			Military		50		mA
					Configured ×16	×8	
Active Current (CMOS) No Blocks Selected	I_{CC} 1A	Notes 1 and 4	Comm'l		10	10	mA
			Military		20	20	mA
Active Current (CMOS) EPROM Block Selected	I_{CC} 1B	Notes 1 and 4	Comm'l		55	30	mA
			Military		65	40	mA
Active Current (CMOS) SRAM Block Selected	I_{CC} 1C	Notes 1 and 4	Comm'l		65	40	mA
			Military		75	50	mA
Active Current (TTL) No Blocks Selected	I_{CC} 2A	Notes 2 and 4	Comm'l		40	40	mA
			Military		50	50	mA
Active Current (TTL) EPROM Block Selected	I_{CC} 2B	Notes 2 and 4	Comm'l		85	60	mA
			Military		95	70	mA
Active Current (TTL) SRAM Block Selected	I_{CC} 2C	Notes 2 and 4	Comm'l		95	70	mA
			Military		105	80	mA
Input Load Current	I_{LI}	V_{IN} = 5.5V or GND		−10	10		µA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5 or GND		−10	10		µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V
2) TTL inputs: $V_{IL} \leqslant 0.8V$, $V_{IH} \geqslant 2.0V$
3) A.C. power component is 1.5 mA/MHz (Power = AC + DC)
4) A.C. power component is 3.5 mA/MHz (Power = AC + DC)

3

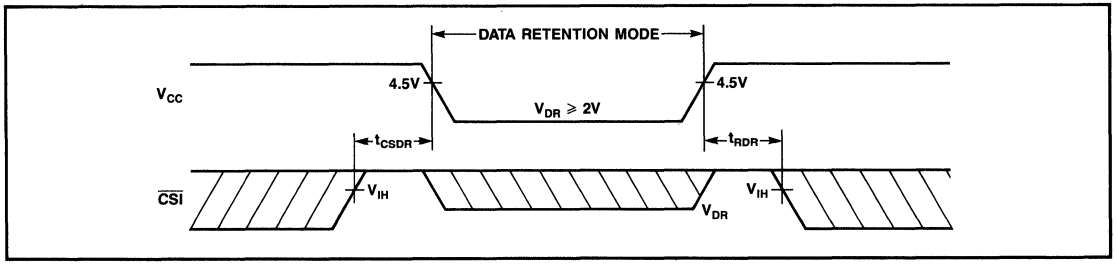
TABLE 6. AC EPROM/SRAM READ AND SRAM WRITE CHARACTERISTICS

PARAMETER	SYMBOL	WSMAP162-40 WSMAP161-40		WSMAP162-45 WSMAP161-45		WSMAP162-55 WSMAP161-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	40		45		55		ns
Address to Output Delay	t_{ACC}		40		45		55	ns
$\overline{CSI}$ to Output Delay	t_{CE}		40		45		55	ns
$\overline{OE}$ to Output Delay	t_{OE}		18		21		23	ns
Output Disable to Output Float	t_{OEF}		18		21		23	ns
Chip Disable to Output Float ($\overline{CSI}$)	t_{CSF}		18		21		23	ns
Address to Output Hold	t_{OH}	10		10		10		ns
Address to $\overline{CSO}$ Valid	t_{CSO}		22		25		27	ns
SRAM Write Cycle Time	t_{WC}	40		45		55		ns
Chip Enable to Write End	t_{CSW}	40		45		55		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Address Valid to Write End	t_{AW}	40		45		55		ns
SRAM Write Enable Pulse Width	t_{PWE}	25		30		35		ns
Data Setup Time	t_{DS}	20		20		30		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Data Float	t_{WEF}		18		21		23	ns
Write Disable to Data Low Z	t_{WELZ}	3		3		3		ns

TABLE 7. DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Minimum V_{CC} for Data Retention	V_{DR}	V_{CC} = 2.0V, $\overline{CSI} \geq V_{CC}$ −0.2V, $V_{IN} \geq V_{CC}$ −0.2V or $V_{IN} \leq$ 0.2V	2.0		V
Current When in Data Retention Mode	I_{CCDR}			100	µA
Chip Deselect to Data Retention	t_{CSDR}		0		ns
Recovery Time From Data Retention	t_{RDR}		t_{RC}		ns

DATA RETENTION WAVEFORM



ABSOLUTE MAXIMUM RATINGS*

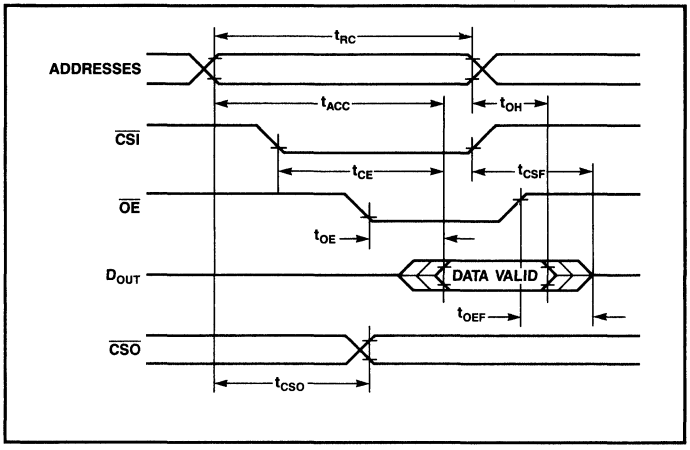
Storage Temperature . . . . . −65°C to +150°C
Voltage to any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14.0V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

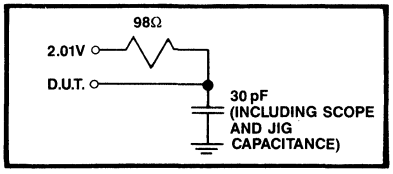
RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

READ CYCLE TIMING DIAGRAM



TEST LOAD

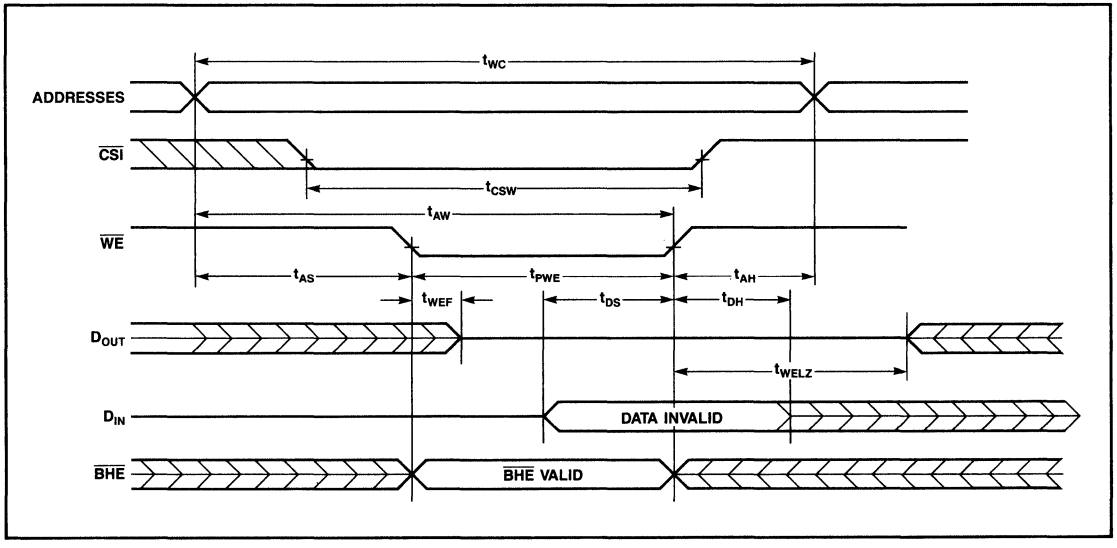
(High Impedance Test Systems)



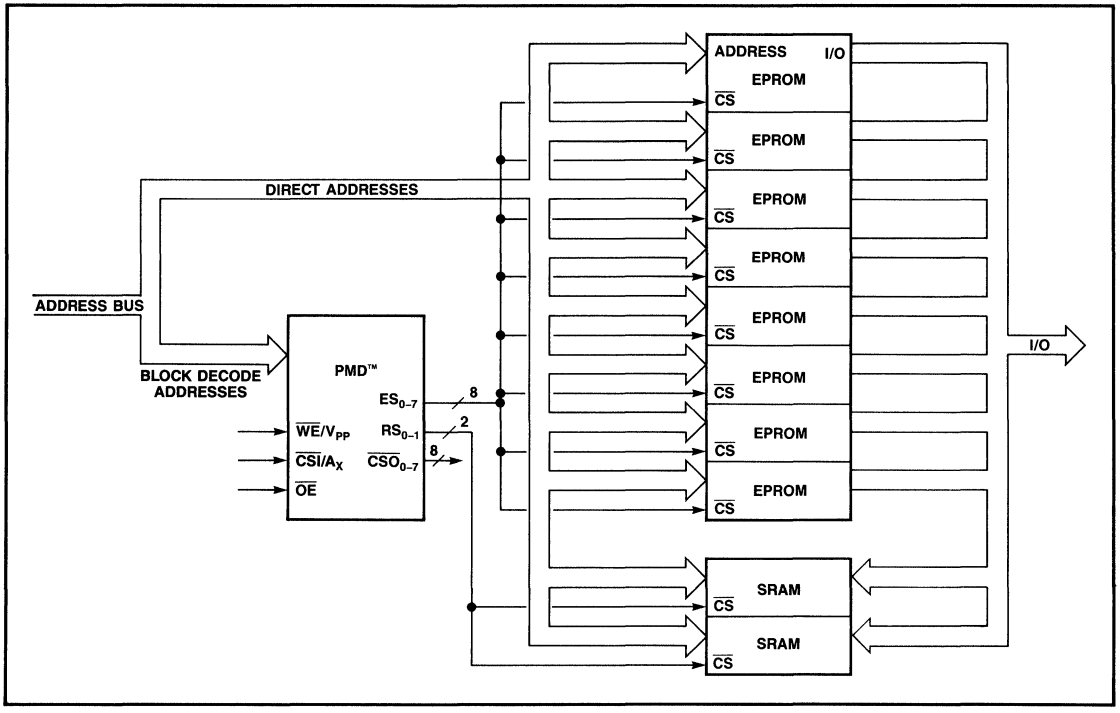
TIMING LEVELS

Input Levels: 0 and 3V
Reference Levels: 1.5V

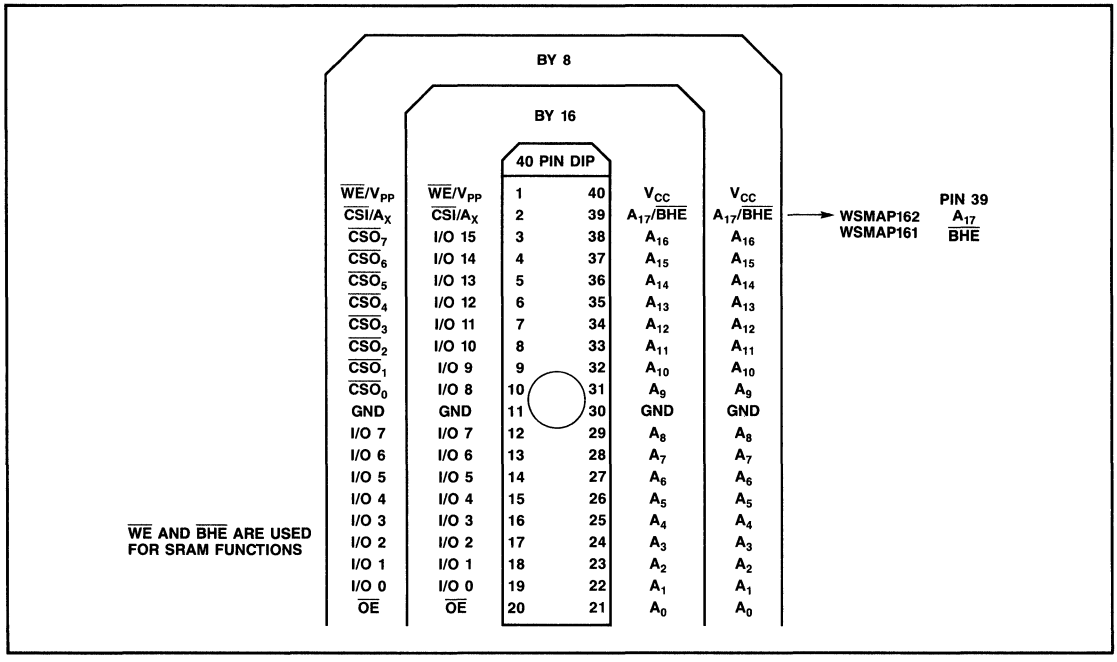
WRITE CYCLE TIMING DIAGRAM



MAP™ MEMORY ARCHITECTURE



WSMAP162/WSMAP161 PIN ASSIGNMENTS



WE/VPP	WE/VPP	1	40	VCC	VCC
CSI/AX	CSI/AX	2	39	A17/BHE	A17/BHE
CSO7	I/O 15	3	38	A16	A16
CSO6	I/O 14	4	37	A15	A15
CSO5	I/O 13	5	36	A14	A14
CSO4	I/O 12	6	35	A13	A13
CSO3	I/O 11	7	34	A12	A12
CSO2	I/O 10	8	33	A11	A11
CSO1	I/O 9	9	32	A10	A10
CSO0	I/O 8	10	31	A9	A9
GND	GND	11	30	GND	GND
I/O 7	I/O 7	12	29	A8	A8
I/O 6	I/O 6	13	28	A7	A7
I/O 5	I/O 5	14	27	A6	A6
I/O 4	I/O 4	15	26	A5	A5
I/O 3	I/O 3	16	25	A4	A4
I/O 2	I/O 2	17	24	A3	A3
I/O 1	I/O 1	18	23	A2	A2
I/O 0	I/O 0	19	22	A1	A1
OE	OE	20	21	A0	A0

PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WSMAP162/WSMAP161 has all bits in the PMD™ and EPROM in the "1" or high state. "0's" are loaded through the procedure of programming.

Information for programming the PMD™ and EPROM is available directly from WSI. Please contact your local sales representative.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MAP™ Memory to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase the part. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 Angstrom (Å) with intensity of 12000μ W/cm^2 for 15 to 20 minutes. The WSMAP162/161 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WSMAP162/161 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WSMAP162/161 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WSMAP162-40D	40	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WSMAP162-40P	40	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WSMAP161-40D	40	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WSMAP161-40P	40	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WSMAP162-45D	40	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WSMAP162-45P	40	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WSMAP161-45D	40	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WSMAP161-45P	40	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WSMAP162-55D	55	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WSMAP162-55DMB	55	40 Pin CERDIP, 0.6″	D3	Military	MIL-STD-883C
WSMAP162-55P	55	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WSMAP161-55D	55	40 Pin CERDIP, 0.6″	D3	Comm'l	Standard
WSMAP161-55DMB	55	40 Pin CERDIP, 0.6″	D3	Military	MIL-STD-883C
WSMAP161-55P	55	40 Pin Plastic Dip, 0.6″	P1	Comm'l	Standard

HIGH SPEED MAPPABLE MEMORY (MAP™)

KEY FEATURES

- **Super Fast Access Time**
  - — EPROM/SRAM: 40 ns (including decode)
  - — Chip Select Outputs: 22 ns
  - — Fast Chip Select Output: 17 ns
- **High Density UV Erasable EPROM**
  - — 128K Bits
- **High Density 6-Transistor Static RAM**
  - — 32K Bits
- **On-Board Programmable Address Decoder**
  - — Eliminates External Chip-Select Decode Components and Delay
- **Code Security**
  - — Contains Programmable Security Bit
- **Addressable Range**
  - — 2M Bytes or 1M Words
- **Block Resolution**
  - — 2K Bytes or 1K Words
- **Chip Select Outputs**
  - — Control I/O and Other Devices
  - — 9 in Byte Wide Mode
  - — 1 in Word Wide Mode
- **Fully User Configurable**
  - — Byte or Word Operation
- **Reduces Board Space**
  - — Simplifies Routing
  - — Replaces 2 or more EPROMs, 2 or more SRAMs and One Decoder

3

GENERAL DESCRIPTION

The WSMAP168 is a Mapped Address Programmable (MAP™) memory product that integrates 128K bits of EPROM, 32K bits of SRAM and a Programmable Mapping Decoder (PMD™) into a single 44-pin package. With a wide input addressing range, this memory product is compatible with large address space processor systems. The on-board PMD™ enables the placement of physical 16K bytes or 8K words of EPROM and 4K bytes or 2K words of SRAM anywhere in a total address space of 2M bytes or 1M words respectively. The PMD™ reduces system component count as well as board space, enhances performance and increases data security. The major feature of this product is the integration of high speed, high density UV erasable EPROM and a 6-transistor full CMOS SRAM along with decoding logic on a single chip.

The WSMAP168 combines the features of the WSMAP162 and WSMAP161 MAP™ products into a single 44 pin package.

The WSMAP168 is ideal for use with digital signal processors like the TMS320XX series, high-performance microcontrollers and microprocessors using a 16-bit data bus. Its data path can be programmed as either 8 or 16 bits. With the provision of Pin 3 programmable as either Chip Select ($\overline{CSI}$) or the highest address bit, its address range is from 512K to 1M words or 1M to 2M bytes. The EPROM architectures are 16K x 8 (byte operations) or 8K x 16 (word operations). The SRAM architectures are 4K x 8 (byte operations) or 2K x 16 (word operations).

With $\overline{BHE}$ (Byte High Enable) in the 16-bit mode, the WSMAP168 can accommodate either full word or byte operations (for those 16-bit processors capable of byte operations).

Refer to Application Note 002 in this databook for additional information.

BLOCK DIAGRAM

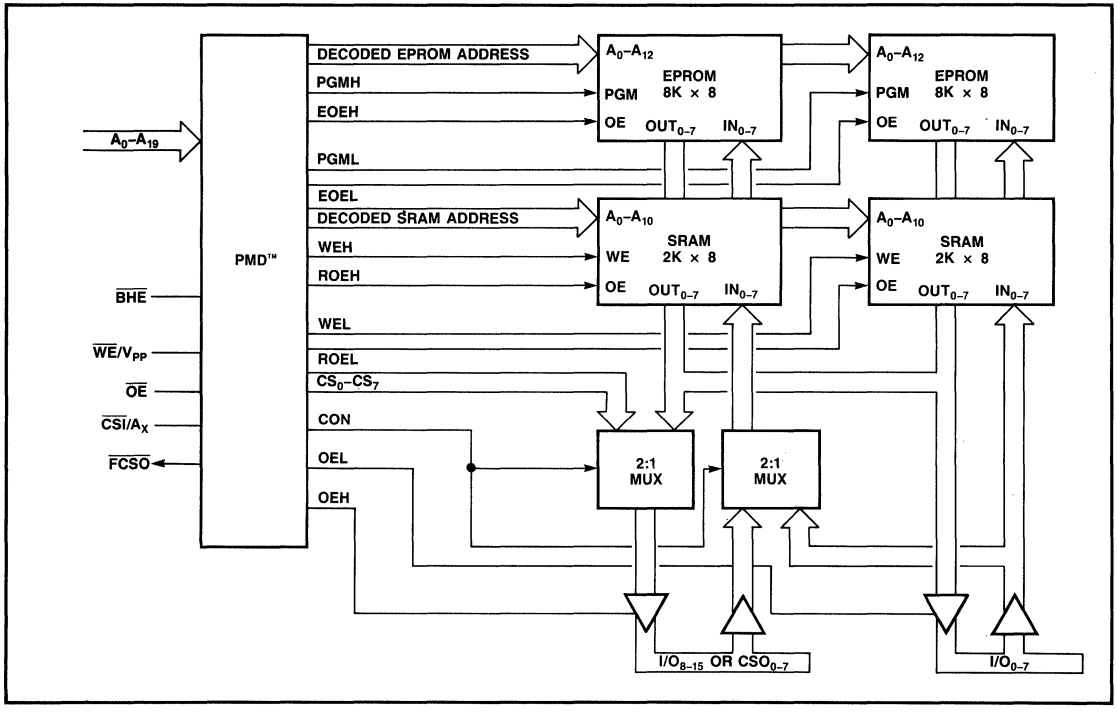


TABLE 1. PRODUCT SELECTION GUIDE

PARAMETER	WSMAP168-40	WSMAP168-45	WSMAP168-55	UNITS
Address Access Time (Max.)	40	45	55	ns
Chip Select ($\overline{CSI}$) Access Time (Max.)	40	45	55	ns
Output Enable ($\overline{OE}$) Access Time (Max.)	18	21	23	ns
Chip Select Output ($\overline{CSO_0}$–$\overline{CSO_7}$)	22	25	27	ns
Fast Chip Select ($\overline{FCSO}$) Output Time (Max.)	17	20	22	ns

TECHNICAL DESCRIPTION

Internally the memory is organized as two 8K x 8 EPROMs and two 2K x 8 SRAMs. The WSMAP168 can be configured for byte or wordwide operations during the EPROM and PMD™ programming operation by programming the configuration (CON) bit. In the wordwide operation, the I/Os of the two EPROMs and two SRAMs are common and are brought out in parallel. In the byte wide operation, the 8 most significant bits of the I/O are multiplexed with the 8 least significant bits using a multiplexer controlled by address bit A_0. An important feature offered with the byte wide configuration is the 8 most significant I/O bits are replaced by 8 individual chip select outputs (CSO_0–CSO_7) which can be programmed to select and control other devices (I/O, SRAM, DRAM, etc.). A single fast chip select output ($\overline{FCSO}$) is provided regardless of byte or wordwide mode selection.

The PMD™ enables the WSMAP168 to directly interface with high speed microprocessors and digital signal processors which require 16K bytes (or 8K words) of EPROM program store and 4K bytes (or 2K words) of SRAM data store in a non-contiguous address space.

In the byte wide configuration, it is possible (by programming the PMD™ to subdivide and selectively access 8 blocks of EPROM each configured in a 2K x 8 architecture. Any one of these eight EPROM blocks can be mapped into any of the 1024 available 2K deep blocks in a 2M byte address space. Similarly, the two blocks of SRAM configured

as 2K x 8 can be mapped into any of the 1024 2K blocks in the 2M byte address space (not occupied by the EPROM). The physical blocks of EPROM and SRAM can be concatenated together to form a continuous sequentially addressable section of memory, placed in non-sequential addressable individual blocks or any combination of the two.

In the wordwide configuration, the EPROM and SRAM are organized as 1K x 16. The PMD™ is used to map the 8 blocks of EPROM and 2 blocks of SRAM into any of the 1024 blocks in a 1M word address space.

Pin 3 ($\overline{CSI}/A_X$) is a dual function input. It is always an address (MSB) input. Optionally, it can be programmed to be a chip select input as well which enables the EPROM and SRAM memory when active low. In a system application, usually one or the other modes is employed but rarely both even though it is possible to employ both modes simultaneously. $\overline{CSO}$s are not powered down since they are a function of the address input and the (always powered up) PMD™.

In the x16 (wordwide) configuration, pin 1 is used as a Byte High Enable ($\overline{BHE}$) control (if byte operations are required). The combination of $\overline{BHE}$ and A_0 control the memory access for a word, upper byte, or lower byte operation. See table 4. This feature reduces the logic required in 16-bit microprocessors and microcontrollers capable of byte operations. If only word operations are required, $\overline{BHE}$ and A_0 should be connected to ground.

A security bit (SEC) is provided that functions as a "bridge" bit. After completion of programming the PMD™ and EPROM, this bit can be programmed (the "bridge" can be "burned"). This prevents external access to the PMD™ contents and inhibits duplication of the PMD™ data by routine copying.

The WSMAP168 pinout is derived from the JEDEC standard WSI WS57C257 16K x 16 high-speed EPROM, i.e., it is read compatible. This pinout enables memory expansion with future WSI mapped address products up to 2M bytes of physical memory. The process technology used in the WSMAP168 is common to all of WSI's current family of high-speed EPROM and RPROM™ memory products. Both the PMD™ and EPROM blocks are programmed using the WSI MagicPro™ (or other) programmer. A menu driven software package for the IBM PC is provided from WSI to support the special PMD™ address mapping and configuration.

TABLE 2. WSMAP168 CONFIGURATIONS

	WSMAP168 x 8		**WSMAP168 x 16**	
Pin 2 Configured as	$\overline{CSI}$	A_X	$\overline{CSI}$	A_X
Address Space	1M Bytes	2M Bytes	512K Words	1M Words
Block Size	2K Bytes	2K Bytes	1K Words	1K Words
Addressable Blocks	512	1024	512	1024
Available EPROM Blocks	8	8	8	8
Available SRAM Blocks	2	2	2	2
Number of Chip Select Outputs	9	9	1	1
EPROM Size Configuration	16K x 8	16K x 8	8K x 16	8K x 16
SRAM Size Configuration	4K x 8	4K x 8	2K x 16	2K x 16
Number of I/Os	8	8	16	16
Low Power Standby	Yes	No	Yes	No
Protected Mode	Yes	Yes	Yes	Yes
Byte Operations	N/A	N/A	Yes	Yes

TABLE 3. MODE SELECTION

PIN / MODE	$\overline{CSI}$	$\overline{OE}$	$\overline{WE}/V_{PP}$	ADDRESS	CONFIGURED ×16 I/O_{0-15} CONFIGURED ×8 I/O_{0-7}	CONFIGURED ×16 $\overline{FCSO}$ CONFIGURED ×8 $\overline{FCSO}$, $\overline{CSO_0}$–$\overline{CSO_7}$
Read EPROM/SRAM	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Selected	D_{OUT}	CS_{OUT}
Read External	V_{IL}	V_{IL}	V_{IH}	EPROM/SRAM Not Selected	High Z	CS_{OUT}
Output Disable	X	V_{IH}	X	X	High Z	CS_{OUT}
Stand-By	V_{IH}	X	X	X	High Z	CS_{OUT}
Write SRAM	V_{IL}	X	V_{IL}	SRAM Selected	D_{IN}	CS_{OUT}
Write External	V_{IL}	X	V_{IL}	No SRAM Selected	X	CS_{OUT}
Program EPROM	V_{IL}	V_{IH}	V_{PP}	EPROM Program Address	D_{IN}	D_{IN}
Program Verify EPROM	V_{IL}	V_{IL}	V_{IH}	EPROM Program Address	D_{OUT}	CS_{OUT}
Program PMD™	V_{IL}	V_{IH}	V_{PP}	PMD Program Address	D_{IN}	D_{IN}
Program Verify PMD™	V_{IL}	V_{IL}	V_{IH}	PMD Program Address	D_{OUT}	CS_{OUT}

TABLE 4. HIGH/LOW BYTE SELECTION TRUTH TABLE (IN ×16 CONFIGURATION ONLY)

$\overline{BHE}$ (PIN 1)	A_0	OPERATION
0	0	Whole Word
0	1	Upper Byte From/To Odd Address
1	0	Lower Byte From/To Even Address
1	1	None

NOTE: $\overline{WR}$ and $\overline{BHE}$ are used for SRAM Functions

TABLE 5. DC READ CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX		UNITS
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.45		V
Output High Voltage	V_{OH}	I_{OH} = −2 mA		2.4			V
V_{CC} Standby Current CMOS	I_{SB1}	Notes 1 and 3	Comm'l		10		mA
			Military		20		mA
V_{CC} Standby Current TTL	I_{SB2}	Notes 2 and 3	Comm'l		40		mA
			Military		50		mA
					Configured ×16	×8	
Active Current (CMOS) No Blocks Selected	I_{CC} 1A	Notes 1 and 4	Comm'l		10	10	mA
			Military		20	20	mA
Active Current (CMOS) EPROM Block Selected	I_{CC} 1B	Notes 1 and 4	Comm'l		55	30	mA
			Military		65	40	mA
Active Current (CMOS) SRAM Block Selected	I_{CC} 1C	Notes 1 and 4	Comm'l		65	40	mA
			Military		75	50	mA
Active Current (TTL) No Blocks Selected	I_{CC} 2A	Notes 2 and 4	Comm'l		40	40	mA
			Military		50	50	mA
Active Current (TTL) EPROM Block Selected	I_{CC} 2B	Notes 2 and 4	Comm'l		85	60	mA
			Military		95	70	mA
Active Current (TTL) SRAM Block Selected	I_{CC} 2C	Notes 2 and 4	Comm'l		95	70	mA
			Military		105	80	mA
Input Load Current	I_{LI}	V_{IN} = 5.5V or GND		−10	10		µA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V or GND		−10	10		µA

NOTES: 1) CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V
2) TTL inputs: $V_{IL} \leq 0.8V$, $V_{IH} \geq 2.0V$
3) A.C. power component is 1.5 mA/MHz (Power = AC + DC)
4) A.C. power component is 3.5 mA/MHz (Power = AC + DC)

3

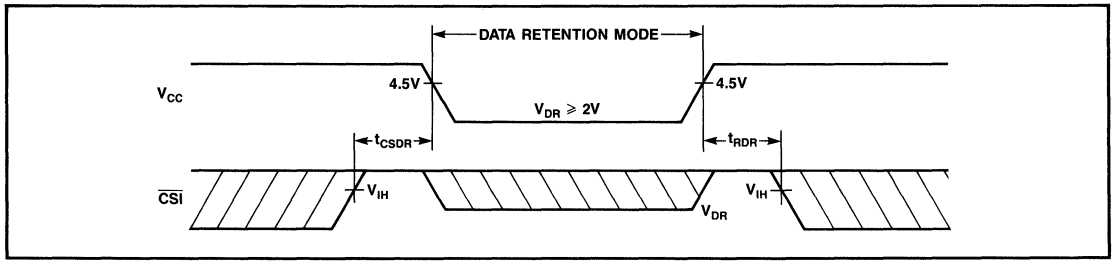
TABLE 6. AC EPROM/SRAM READ AND SRAM WRITE CHARACTERISTICS

PARAMETER	SYMBOL	WSMAP168-40		WSMAP168-45		WSMAP168-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	40		45		55		ns
Address to Output Delay	t_{ACC}		40		45		55	ns
$\overline{CSI}$ to Output Delay	t_{CE}		40		45		55	ns
$\overline{OE}$ to Output Delay	t_{OE}		18		21		23	ns
Output Disable to Output Float	t_{OEF}		18		21		23	ns
Chip Disable to Output Float	t_{CSF}		18		21		23	ns
Address to Output Hold	t_{OH}	10		10		10		ns
Address to $\overline{CSO}_{0-7}$ True	t_{CSO}		22		25		27	ns
Address to $\overline{FCSO}$ True	t_{FCSO}		17		20		22	ns
SRAM Write Cycle Time	t_{WC}	40		45		55		ns
Chip Enable to Write End	t_{CSW}	40		45		55		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Address Valid to Write End	t_{AW}	40		45		55		ns
SRAM Write Enable Pulse Width	t_{PWE}	25		30		35		ns
Data Setup Time	t_{DS}	20		20		30		ns
Data Hold Time	t_{DH}	0		0		0		ns
Write Enable to Data Float	t_{WEF}		18		21		23	ns
Write Disable to Data Low Z	t_{WELZ}	3		3		3		ns

TABLE 7. DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Minimum V_{CC} for Data Retention	V_{DR}	V_{CC} = 2.0V, $\overline{CSI} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
Current in Data Retention Mode	I_{CCDR}			100	mA
Chip Deselect to Data Retention	t_{CSDR}		0		ns
Recovery Time From Data Retention	t_{RDR}		t_{RC}		ns

DATA RETENTION WAVEFORM



ABSOLUTE MAXIMUM RATINGS*

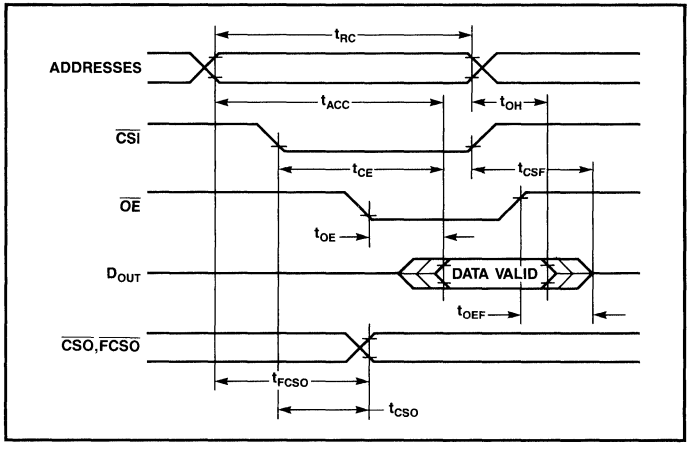
Storage Temperature . . . . . −65°C to +150°C
Voltage to any pin with
respect to GND . . . . . −0.6V to +7V
V_{PP} with respect to GND . . . . . −0.6V to +14.0V
ESD Protection . . . . . >2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

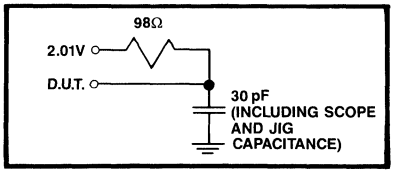
RANGE	TEMPERATURE	V_{CC}
Comm'l	0° to +70°C	+5V ± 5%
Military	−55° to +125°C	+5V ± 10%

READ CYCLE TIMING DIAGRAM



TEST LOAD

(High Impedance Test Systems)

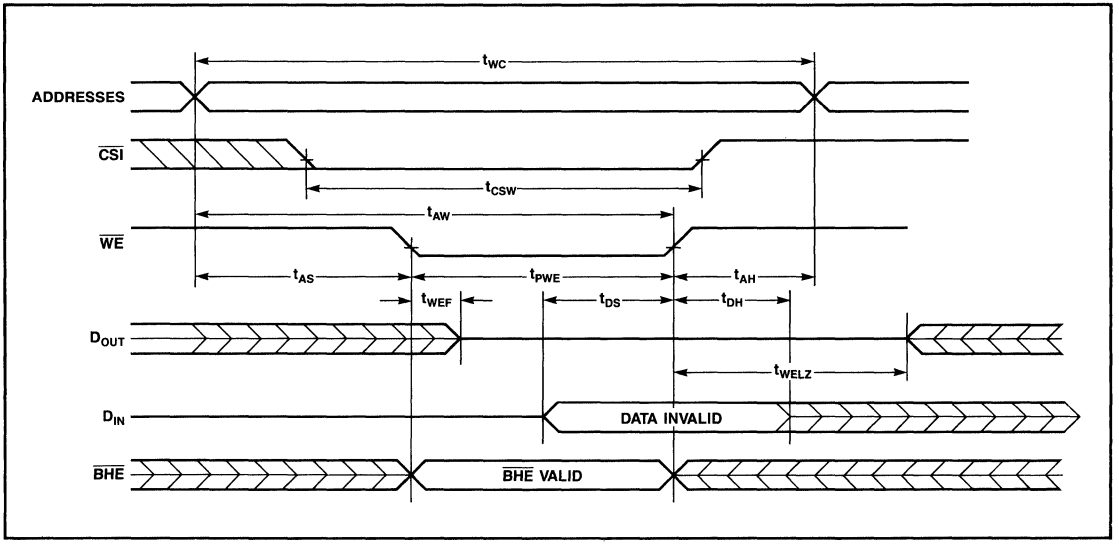


TIMING LEVELS

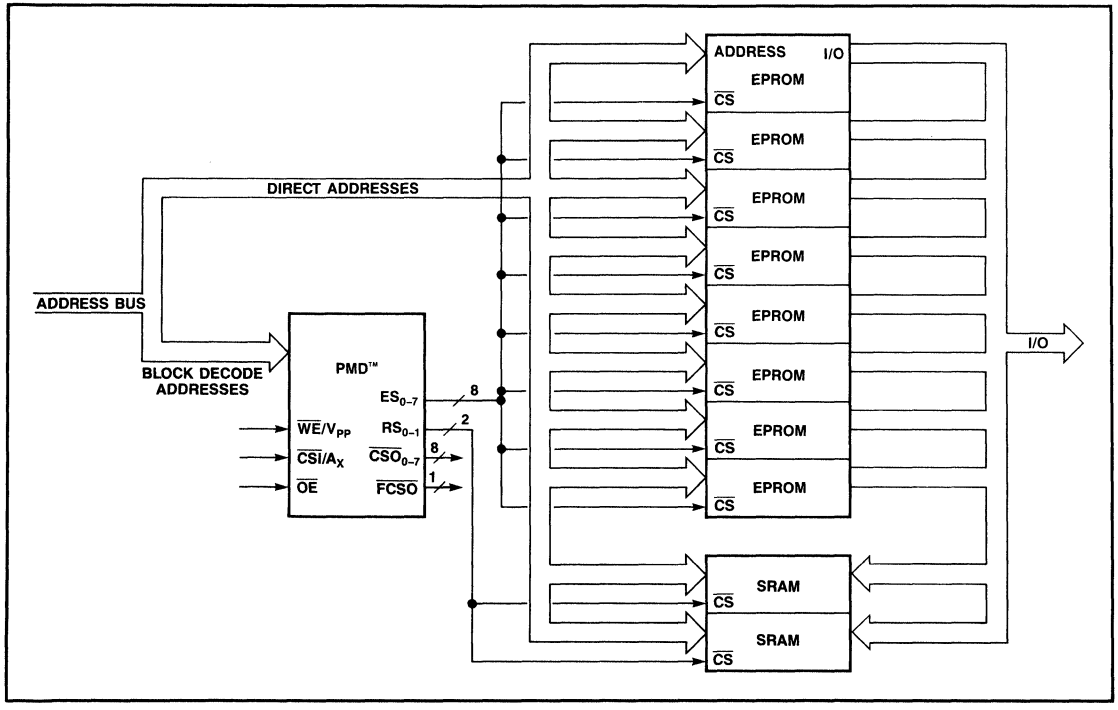
Input Levels: 0 and 3V

Reference Levels: 1.5V

WRITE CYCLE TIMING DIAGRAM



MAP™ MEMORY ARCHITECTURE



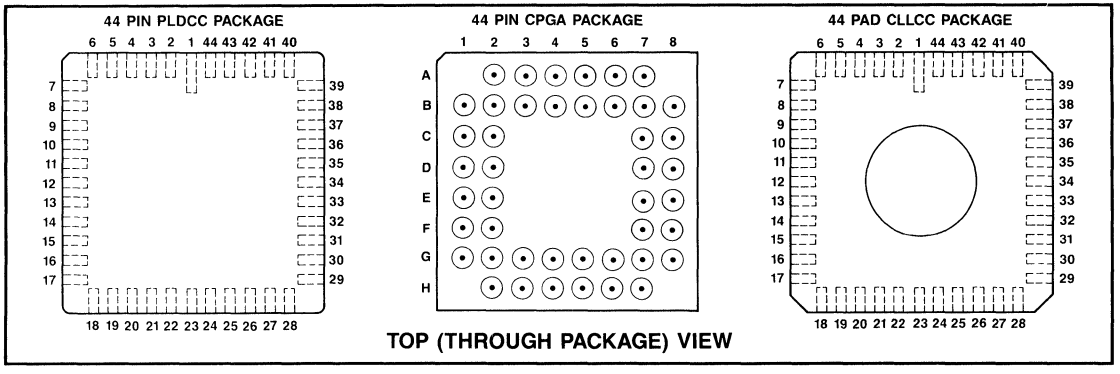
WSMAP168 PIN ASSIGNMENTS

44 PIN PLDCC PACKAGE 44 PAD CLLCC PACKAGE		
PIN NO.	×8	×16
1	GND	$\overline{BHE}$
2	$\overline{WE}/V_{PP}$	$\overline{WE}/V_{PP}$
3	$\overline{CSI}/A_X$	$\overline{CSI}/A_X$
4	$\overline{CSO}_7$	I/O_{15}
5	$\overline{CSO}_6$	I/O_{14}
6	$\overline{CSO}_5$	I/O_{13}
7	$\overline{CSO}_4$	I/O_{12}
8	$\overline{CSO}_3$	I/O_{11}
9	$\overline{CSO}_2$	I/O_{10}
10	$\overline{CSO}_1$	I/O_9
11	$\overline{CSO}_0$	I/O_8
12	GND	GND
13	$\overline{FCSO}$	$\overline{FCSO}$
14	I/O_7	I/O_7
15	I/O_6	I/O_6
16	I/O_5	I/O_5
17	I/O_4	I/O_4
18	I/O_3	I/O_3
19	I/O_2	I/O_2
20	I/O_1	I/O_1
21	I/O_0	I/O_0
22	$\overline{OE}$	$\overline{OE}$
23	A_0	A_0
24	A_1	A_1
25	A_2	A_2
26	A_3	A_3
27	A_4	A_4
28	A_5	A_5
29	A_6	A_6
30	A_7	A_7
31	A_8	A_8
32	A_9	A_9
33	A_{10}	A_{10}
34	GND	GND
35	A_{11}	A_{11}
36	A_{12}	A_{12}
37	A_{13}	A_{13}
38	A_{14}	A_{14}
39	A_{15}	A_{15}
40	A_{16}	A_{16}
41	A_{17}	A_{17}
42	A_{18}	A_{18}
43	A_{19}	A_{19}
44	V_{CC}	V_{CC}

44 PIN CPGA PACKAGE		
PIN NO.	×8	×16
A_5	GND	$\overline{BHE}$
A_4	$\overline{WE}/V_{PP}$	$\overline{WE}/V_{PP}$
B_4	$\overline{CSI}/A_X$	$\overline{CSI}/A_X$
A_3	$\overline{CSO}_7$	I/O_{15}
B_3	$\overline{CSO}_6$	I/O_{14}
A_2	$\overline{CSO}_5$	I/O_{13}
B_2	$\overline{CSO}_4$	I/O_{12}
B_1	$\overline{CSO}_3$	I/O_{11}
C_2	$\overline{CSO}_2$	I/O_{10}
C_1	$\overline{CSO}_1$	I/O_9
D_2	$\overline{CSO}_0$	I/O_8
D_1	GND	GND
E_1	$\overline{FCSO}$	$\overline{FCSO}$
E_2	I/O_7	I/O_7
F_1	I/O_6	I/O_6
F_2	I/O_5	I/O_5
G_1	I/O_4	I/O_4
G_2	I/O_3	I/O_3
H_2	I/O_2	I/O_2
G_3	I/O_1	I/O_1
H_3	I/O_0	I/O_0
G_4	$\overline{OE}$	$\overline{OE}$
H_4	A_0	A_0
H_5	A_1	A_1
G_5	A_2	A_2
H_6	A_3	A_3
G_6	A_4	A_4
H_7	A_5	A_5
G_7	A_6	A_6
G_8	A_7	A_7
F_7	A_8	A_8
F_8	A_9	A_9
E_7	A_{10}	A_{10}
E_8	GND	GND
D_8	A_{11}	A_{11}
D_7	A_{12}	A_{12}
C_8	A_{13}	A_{13}
C_7	A_{14}	A_{14}
B_8	A_{15}	A_{15}
B_7	A_{16}	A_{16}
A_7	A_{17}	A_{17}
B_6	A_{18}	A_{18}
A_6	A_{19}	A_{19}
B_5	V_{CC}	V_{CC}

NOTE: $\overline{WR}$ and $\overline{BHE}$ functions are for SRAM functions.

WSMAP168 PIN ASSIGNMENTS



TOP (THROUGH PACKAGE) VIEW

PROGRAMMING

Upon delivery from WaferScale Integration, Inc. or after each erasure (see Erasure section), the WSMAP168 has all bits in the PMD™ and EPROM in the "1" or high state. "0's" are loaded through the procedure of programming.

Information for programming the PMD™ and EPROM is available directly from WSI. Please contact your local sales representative.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the WSMAP168 to an ultra-violet light source. A dosage of 15W-second/cm^2 is required to completely erase a WSMAP168. This dosage can be obtained by exposure to an ultra-violet lamp with wavelength of 2537 (Å) with intensity of 1200μ W/cm^2 for 15 to 20 minutes. The WSMAP168 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the WSMAP168 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, the exposure to fluorescent light and sunlight will eventually erase the WSMAP168 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WSMAP168-40C	40	44 Pad CLLCC	C3	Comm'l	Standard
WSMAP168-40CMB	40	44 Pad CLLCC	C3	Military	MIL-STD-883C
WSMAP168-40J	40	44 Pin PLDCC	J2	Comm'l	Standard
WSMAP168-40X	40	44 Pin Ceramic PGA	X2	Comm'l	Standard
WSMAP168-40XMB	40	44 Pin Ceramic PGA	X2	Military	MIL-STD-883C
WSMAP168-45C	45	44 Pad CLLCC	C3	Comm'l	Standard
WSMAP168-45CMB	45	44 Pad CLLCC	C3	Military	MIL-STD-883C
WSMAP168-45J	45	44 Pin PLDCC	J2	Comm'l	Standard
WSMAP168-45X	45	44 Pin Ceramic PGA	X2	Comm'l	Standard
WSMAP168-45XMB	45	44 Pin Ceramic PGA	X2	Military	MIL-STD-883C
WSMAP168-55C	55	44 Pad CLLCC	C3	Comm'l	Standard
WSMAP168-55CMB	55	44 Pad CLLCC	C3	Military	MIL-STD-883C
WSMAP168-55J	55	44 Pin PLDCC	J2	Comm'l	Standard
WSMAP168-55X	55	44 Pin Ceramic PGA	X2	Comm'l	Standard
WSMAP168-55XMB	55	44 Pin Ceramic PGA	X2	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

CMOS BIT SLICE PRODUCTS

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

WAFERSCALE INTEGRATION, INC.

CMOS 4-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **2901 Architecture in CMOS**
- **Drop-In Replacement for 2901C**
- **Expandable in 4-Bit Increments**
- **High Speed**
  — Maximum Clock Frequency of 43 MHz (23 ns)
- **Very Low Power**
  — 30 mA Maximum (Commercial Temperature)
- **EPI Processing**
  — Latch-Up Immunity Over 200 mA

4

GENERAL DESCRIPTION

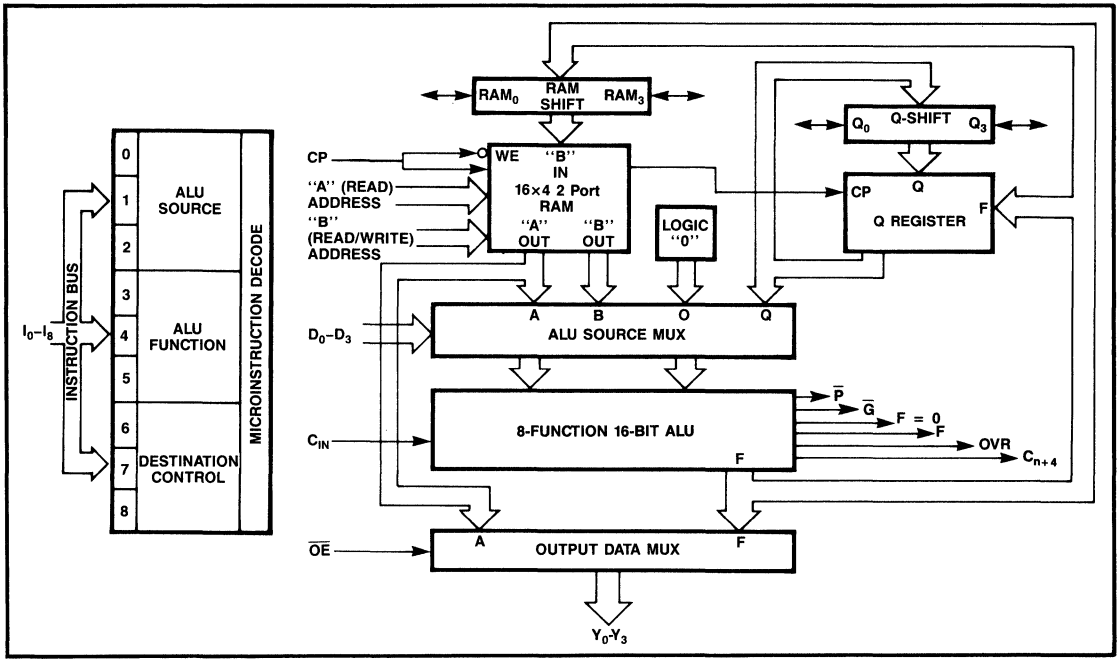
The WS5901 is a 4-bit high-speed microprocessor which contains the logic of a Bipolar 2901 bit slice processor.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the 5901 is manufactured, provides significant performance improvements over its counterpart. While operating as fast as a 2901C based system, the WS5901C requires less than 8% of the power consumed by its Bipolar equivalent. The WS5901D is a 25% speed enhancement over the "C" speed.

The WS5901 is also a macro cell in the WaferScale cell library. As such it can be combined with other cells to build High Performance CMOS Application Specific Integrated Circuits.

FUNCTIONAL BLOCK DIAGRAM

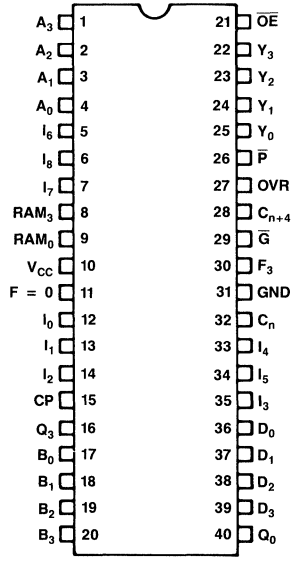


PIN DESCRIPTION

Signal Name	I/O	Description
A0-3	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-3	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low.
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678).
Q3, RAM3	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 3 pin and the MSB of the Q-register is available on the Q3 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Qo, RAMo	I/O	Shift lines similar to Q3 and RAM3. However the description is applied to the LSB of RAM and the Q-register.
D0-D3	I	These four direct data inputs can be selected as a data source for the ALU. DO is the LSB.
Y0-Y3	O	These four three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678.
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state. When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y3, as determined by I678.
$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the ALU.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F = 0	O	This output, when high, indicates the result of an ALU operation is zero.
F3	O	The most significant ALU output bit.
Cn	I	The carry-in to the ALU.
Cn + 4	O	The carry-out of the ALU.
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board 16 x 4 RAM, including set-up time for the A and B port registers. The A and B port and Q-register outputs change on the clock low-to-high transition.

PIN DESIGNATOR

Plastic Package



TOP

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
Latch-Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC READ CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	Y_0–Y_3	I_{OL} = 20 mA Comm'l		0.5	V
			All Others	I_{OL} = 16 mA			
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max (Note 2)	Comm'l (0°C to +70°C)			30	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) 100 ns System Cycle

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals, G, P, C_{n+4} and OVR are designed to indicate carry and overflow conditions when the WS5901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	R ∧ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R}_i$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$ equations, but substitute $\overline{R}_i$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3+G_2+G_1+G_0$	$P_3G_2+P_3P_2G_1+P_3P_2P_1G_0$	$\overline{G_3+P_3G_2+P_3P_2G_1}$ $+P_3P_2P_1P_0(G_0+\overline{C_n})$	See note 1

NOTES: 1) $(P_2 + G_2P_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n) \forall (\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n)$
2) + = OR

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1: ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EXOR	R ▽ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q - A - 1 Q - A	B - A - 1 B - A	Q - 1 Q	B - 1 B	A - 1 A	A - D - 1 A - D	Q - D - 1 Q - D	- D - 1 - D
2	C_n = L R Minus S C_n = H	A - Q - 1 A - Q	A - B - 1 A - B	- Q - 1 - Q	- B - 1 - B	- A - 1 - A	D - A - 1 D - A	D - Q - 1 D - Q	D - 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ▽ Q	A ▽ B	Q	B	A	D ▽ A	D ▽ Q	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; - = Minus; ∨ = OR; ∧ = AND; ▽ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1, and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4, and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS5901 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \veebar Q$
6 1		$A \veebar B$
6 5		$D \veebar A$
6 6		$D \veebar Q$
7 0	EX-NOR	$\overline{A \veebar Q}$
7 1		$\overline{A \veebar B}$
7 5		$\overline{D \veebar A}$
7 6		$\overline{D \veebar Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

4

WS5901C COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901C over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	31ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	32MHz
Minimum Clock Low Time	15ns
Minimum Clock High Time	15ns
Minimum Clock Period	31ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	23ns
From $\overline{OE}$ High to output disable	23ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	40	40	40	37	40	40	40	–	ns
D0-D3	30	30	30	30	38	30	30	–	
C_n	22	22	20	–	25	22	25	–	
I_{012}	35	35	35	37	37	35	35	–	
I_{345}	35	35	35	35	38	35	35	–	
I_{678}	25	–	–	–	–	–	26	26	
A BYPASS ALU (I = 2XX)	35	–	–	–	–	–	–	–	
CLOCK	35	35	35	35	35	35	35	28	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	1 (Note 3)	30 (Note 4)	1	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		1	
D0-D3	–	–	25	0	
C_n	–	–	20	0	
I_{012}	–	–	30	0	
I_{345}	–	–	30	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	–	–	12	0	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS5901D COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	23ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	43MHz
Minimum Clock Low Time	11ns
Minimum Clock High Time	11ns
Minimum Clock Period	23ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	14ns
From $\overline{OE}$ High to output disable	16ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	30	30	30	28	30	30	30	-	ns
D0-D3	21	20	20	20	24	21	22	-	
C_n	17	17	14	-	19	16	18	-	
I_{012}	26	25	24	24	25	24	25	-	
I_{345}	26	24	24	24	26	24	26	-	
I_{678}	16	-	-	-	-	-	21	21	
A BYPASS ALU (I = 2XX)	24	-	-	-	-	-	-	-	
CLOCK	24	23	23	23	24	24	24	19	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	10	0 (Note 3)	21 (Note 4)	1	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		1	
D0-D3	-	-	16	0	
C_n	-	-	13	0	
I_{012}	-	-	19	0	
I_{345}	-	-	19	0	
I_{678}	7	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	-	-	9	1	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS5901CP	C	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WS5901DP	D	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

CMOS 16-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **Four CMOS 2901 Type Devices in a Single Package**
- **On Board Look-Ahead Carry Generator**
- **Low CMOS Power**
  — 225 mW
- **High Speed Operation**
  — 31 ns Read-Modify-Write
- **Fully Firmware Compatible with the Bipolar Device Configuration of Four 2901s and One 2902A**

GENERAL DESCRIPTION

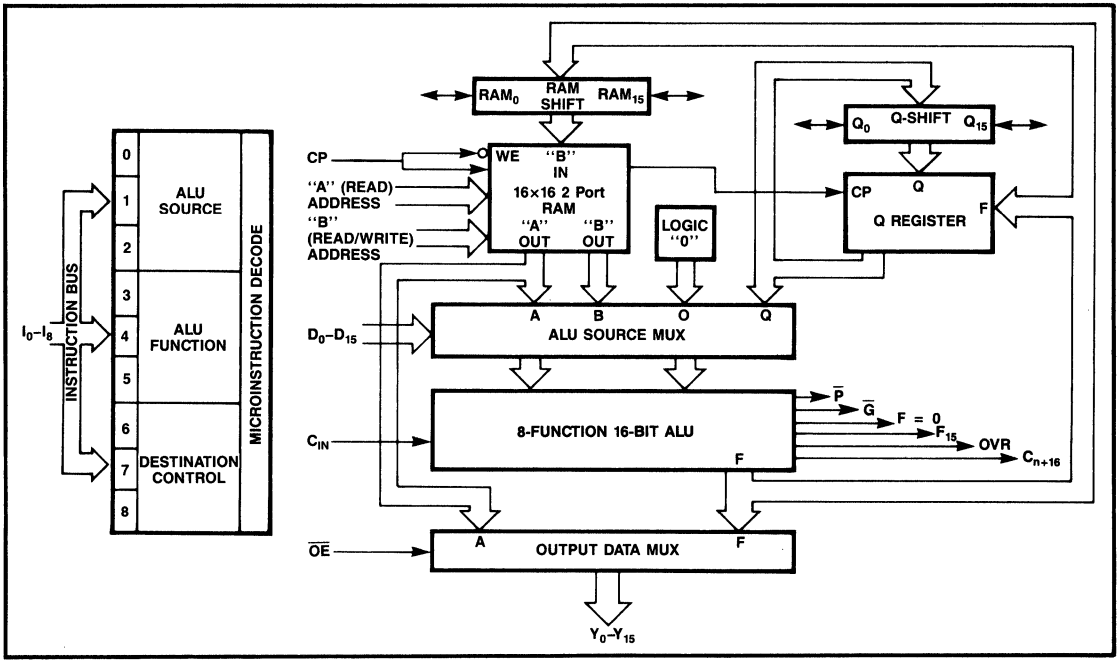
The WS59016 is a 16-bit high-speed microprocessor which combines the functions of four 2901 4-bit slice processors and distributed look-ahead carry generation on a single High Performance CMOS device.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the WS59016 is manufactured, provides significant performance improvements over an equivalent Bipolar device configuration. While operating faster than a 2901C based system, the WS59016 requires less than 3% of the power consumed by an equivalent Bipolar system.

The WS59016 is also available as a macro cell in the WaferScale cell library. As such it can be combined with other cells to build Application Specific Integrated Circuits.

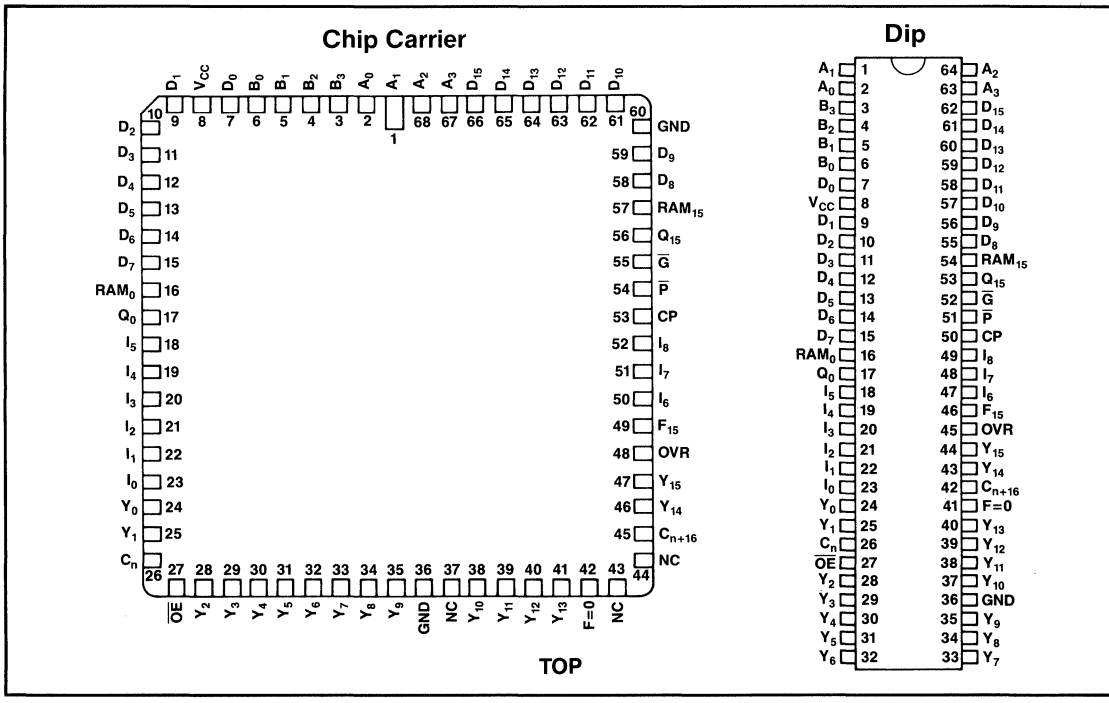
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Signal Name	I/O	Description
A0-3	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-3	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low.
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678).
Q15, RAM15	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 15 pin and the MSB of the Q-register is available on the Q15 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Qo, RAMo	I/O	Shift lines similar to Q15 and RAM15, however the description is applied to the LSB of RAM and the Q-register.
D0-D15	I	These sixteen direct data inputs can be selected as a data source for the ALU. DO is the LSB.
Y0-Y15	O	These sixteen three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678.
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state. When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y15, as determined by I678.
$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the ALU.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F = 0	O	This output, when high, indicates the result of an ALU operation is zero.
F15	O	The most significant ALU output bit.
Cn	I	The carry-in to the ALU.
Cn + 16	O	The carry-out of the ALU.
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board dual port RAM, including set-up time for the A and B-port registers. The A and B-port outputs change while the clock is high. The Q-register is latched on the clock low-to-high transition.

PIN ORIENTATION



ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
Latch-Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC READ CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OL} = 12 mA Comm'l I_{OL} = 8 mA Mil		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	Comm'l (0°C to +70°C)			45	mA
			Mil (−55°C to +125°C)			60	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+16}, and OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+16}, and OVR are designed to indicate carry and overflow conditions when the WS59016 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions

$P_i = R_i + S_i$
$G_i = R_i \cdot S_i$

$P_{0-3} = P_0 \cdot P_1 \cdot P_2 \cdot P_3$ $\quad G_{0-3} = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0$
$P_{4-7} = P_4 \cdot P_5 \cdot P_6 \cdot P_7$ $\quad G_{4-7} = G_7 + P_7 \cdot G_6 + P_7 \cdot P_6 \cdot G_5 + P_7 \cdot P_6 \cdot P_5 \cdot G_4$
$P_{8-11} = P_8 \cdot P_9 \cdot P_{10} \cdot P_{11}$ $\quad G_{8-11} = G_{11} + P_{11} \cdot G_{10} + P_{11} \cdot P_{10} \cdot G_9 + P_{11} \cdot P_{10} \cdot P_9 \cdot G_8$
$P_{12-15} = P_{12} \cdot P_{13} \cdot P_{14} \cdot P_{15}$ $\quad G_{12-15} = G_{15} + P_{15} \cdot G_{14} + P_{15} \cdot P_{14} \cdot G_{13} + P_{15} \cdot P_{14} \cdot P_{13} \cdot G_{12}$
$C_{n+15} = G_{12-14} + P_{12-14} \cdot G_{8-11} + P_{12-14} \cdot P_{8-11} \cdot G_{4-7} + P_{12-14} \cdot P_{8-11} \cdot P_{4-7} \cdot G_{0-3}$
$P_{12-14} = P_{12} \cdot P_{13} \cdot P_{14}$ $\quad G_{12-14} = G_{14} + P_{14} \cdot G_{13} + P_{14} \cdot P_{13} \cdot G_{12}$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+16}	OVR
0	R + S	$\overline{P_{0-3} \cdot P_{4-7} \cdot P_{8-11} \cdot P_{12-15}}$	$\overline{G_{12-15} + P_{12-15} \cdot G_{8-11} + P_{12-15} \cdot P_{8-11} \cdot G_{4-7} + P_{12-15} \cdot P_{8-11} \cdot P_{4-7} \cdot G_{0-3}}$	P·C_n + G	$C_{n+15} \oplus C_{n+16}$
1	S − R	← Same as R + S Equations except substitute $\overline{R}_i$ for R_i in definitions →			
2	R − S	← Same as R + S Equations except substitute $\overline{S}$ for S in definitions →			
3	R ∨ S	LOW	HIGH	LOW	LOW
4	R ∧ S	LOW	$\overline{G_{12-15} + G_{8-11} + G_{4-7} + G_{0-3}}$	HIGH	LOW
5	$\overline{R}$ ∧ S	LOW	Same as R ∧ S except substitute $\overline{R}$ for R in definition	HIGH	LOW
6	R ⊕ S	$\overline{P_{0-3} \cdot P_{4-7} \cdot P_{8-11} \cdot P_{12-15}}$	HIGH	LOW	LOW
7	$\overline{R \oplus S}$	Same as R⊕S except Substitute $\overline{R}$ for R in Definitions	HIGH	LOW	LOW

Note: 1) + = OR

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1: ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EXOR S	R ▽ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ▽ Q	A ▽ B	Q	B	A	D ▽ A	D ▽ Q	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ▽ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1 and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4 and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS59016 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (CN = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \triangledown Q$
6 1		$A \triangledown B$
6 5		$D \triangledown A$
6 6		$D \triangledown Q$
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

COMPETITIVE TIMING ANALYSIS

The following analysis compares the critical timing paths of a WS59016D vs. the equivalent Bipolar circuit implementation using four 2901C's and one 2902A.

As can be seen from this comparison, the WS59016 operates faster than even the theoretically achievable values of the Bipolar implementation. The actual values for the Bipolar circuit will be lengthened by the layout dependent interconnect delays between the individual devices. When these delays are taken into account, the WS59016 speed advantage becomes even greater.

TIMING COMPARISON
WS59016D vs 2901C w/2902A (Comm'l)

DATA PATH	CONTROL PATH
2901C w/ 2902A	2901C w/ 2902A
A, B Address → $\overline{P}$ or $\overline{G}$ = 37ns	I_{012} → $\overline{P}$ or $\overline{G}$ = 37ns
$\overline{P}$ or $\overline{G}$ → C = 9ns	$\overline{P}$ or $\overline{G}$ → C = 9ns
C → F = 0, $RAM_{0,15}$ = 25ns	C → F = 0, $RAM_{0,15}$ = 25ns
interconnect delay → = Xns	interconnect delay → = Xns
Total Delay → > 71ns	Total Delay → > 71ns
59016D	59016D
A, B Address → F = 0, $RAM_{0,15}$ = 46ns	I_{012} → F = 0, $RAM_{0,15}$ = 41ns
interconnect delay → = 0ns	interconnect delay → = 0ns
Total Delay → ≤ 46ns	Total Delay → ≤ 41ns

TIMING COMPARISON
WS59016D vs 2901C w/2902A (Military)

DATA PATH	CONTROL PATH
2901C w/ 2902A	2901C w/ 2902A
A, B Address → $\overline{P}$ or $\overline{G}$ = 44ns	I_{012} → $\overline{P}$ or $\overline{G}$ = 44ns
$\overline{P}$ or $\overline{G}$ → C = 11.5ns	$\overline{P}$ or $\overline{G}$ → C = 11.5ns
C → F = 0, $RAM_{0,15}$ = 28ns	C → F = 0, $RAM_{0,15}$ = 28ns
interconnect delay → = Xns	interconnect delay → = Xns
Total Delay → > 83.5ns	Total Delay → > 83.5ns
59016D	59016D
A, B Address → F15, $RAM_{0,15}$ = 56ns	I_{012} → F15, $RAM_{0,15}$ = 49ns
interconnect delay → = 0ns	interconnect delay → = 0ns
Total Delay → ≤ 56ns	Total Delay → ≤ 49ns

NOTE: This competitive analysis holds true for any 16 bit system which performs arithmetic operations. If arithmetic operations are not used, the Bipolar circuit can run faster than noted above.

COMMERCIAL RANGE AC CHARACTERISTICS (WS59016C)

The tables shown here specify the guaranteed performance of the WS59016C over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	67ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	15MHz
Minimum Clock Low Time	33ns
Minimum Clock High Time	33ns
Minimum Clock Period	67ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	25ns
From $\overline{OE}$ High to output disable	25ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM15	Q0, Q15	UNITS
A, B ADDRESS	69	69	60	68	71	69	71	–	ns
D0-D15	55	55	45	50	55	55	55	–	
C_n	38	38	27	–	42	38	42	–	
I_{012}	60	60	55	55	60	60	60	–	
I_{345}	60	60	55	55	60	60	60	–	
I_{678}	30	–	–	–	–	–	27	26	
A BYPASS ALU (I = 2XX)	45	–	–	–	–	–	–	–	
CLOCK	65	65	65	65	55	65	70	30	

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	2 (Note 3)	65 (Note 4)	1	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		1	
D0-D15	–	–	50	0	
C_n	–	–	34	0	
I_{012}	–	–	55	0	
I_{345}	–	–	55	0	
I_{678}	15	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	–	–	20	4	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here.

MILITARY RANGE AC CHARACTERISTICS (WS59016C)

The tables shown here specify the guaranteed performance of the WS59016C over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	80ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	12.5MHz
Minimum Clock Low Time	39ns
Minimum Clock High Time	39ns
Minimum Clock Period	80ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30ns
From $\overline{OE}$ High to output disable	30ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM15	Q0, Q15	UNITS
A, B ADDRESS	83	83	72	82	83	83	83	–	ns
D0-D15	66	66	54	60	66	66	66	–	
C_n	46	46	33	–	53	46	53	–	
I_{012}	72	72	66	66	72	72	72	–	
I_{345}	72	72	66	66	72	72	72	–	
I_{678}	36	–	–	–	–	–	31	31	
A BYPASS ALU (I = 2XX)	55	–	–	–	–	–	–	–	
CLOCK	78	78	78	78	66	78	78	36	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	20	2 (Note 3)	78 (Note 4)	2	ns
B Destination Address	20	DO NOT CHANGE (Note 2)		2	
D0-D15	–	–	60	0	
C_n	–	–	41	0	
I_{012}	–	–	66	0	
I_{345}	–	–	66	0	
I_{678}	20	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	–	–	25	5	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

COMMERCIAL RANGE AC CHARACTERISTICS (WS59016D)

The tables shown here specify the guaranteed performance of the WS59016D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select) of A, B registers to end of cycle)	31 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock Low Time	14 ns
Minimum Clock High Time	14 ns
Minimum Clock Period	40 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	24 ns
From $\overline{OE}$ High to output disable	22 ns

COMBINATION PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15	UNITS
A, B ADDRESS	46	46	44	43	46	46	44	—	ns
D0-D15	36	32	34	32	36	34	36	—	
C_n	32	29	24	—	32	28	32	—	
I_{012}	39	39	37	38	39	38	41	—	
I_{345}	39	38	37	37	39	38	41	—	
I_{678}	28	—	—	—	—	—	34	34	
A BYPASS ALU (I = 2XX)	34	—	—	—	—	—	—	—	
CLOCK	38	37	38	34	38	38	38	38	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H→L	Hold after H→L	Set Up before L→H	Hold after L→H	UNITS
A, B, Source Address	12	0 (Note 3)	23 (Note 4)	1	ns
B Destination Address	12	DO NOT CHANGE (Note 2)		1	
D0-D15	—	—	19	0	
C_n	—	—	16	0	
I_{012}	—	—	22	0	
I_{345}	—	—	22	0	
I_{678}	12	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	—	—	17	3	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here.

MILITARY RANGE AC CHARACTERISTICS (WS59016D)

The tables shown here specify the guaranteed performance of the WS59016D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select) of A, B registers to end of cycle)	36 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	27 MHz
Minimum Clock Low Time	17 ns
Minimum Clock High Time	17 ns
Minimum Clock Period	47 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30 ns
From $\overline{OE}$ High to output disable	27 ns

COMBINATION PROPAGATION DELAYS (C_L = 50PF)

FROM OUTPUT \ TO OUTPUT	Y	F15	C_{n+16}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15	UNITS
A, B ADDRESS	56	56	53	52	56	56	53	—	ns
D0-D15	43	39	42	39	43	42	43	—	
C_n	39	36	30	—	39	34	39	—	
I_{012}	48	48	46	47	48	47	49	—	
I_{345}	48	47	46	46	48	47	49	—	
I_{678}	34	—	—	—	—	—	42	42	
A BYPASS ALU (I = 2XX)	42	—	—	—	—	—	—	—	
CLOCK	47	46	47	42	47	47	47	47	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H→L	Hold after H→L	Set Up before L→H	Hold after L→H	UNITS
A, B, Source Address	16	0 (Note 3)	29 (Note 4)	2	ns
B Destination Address	16	DO NOT CHANGE (Note 2)		2	
D0-D15	—	—	23	0	
C_n	—	—	20	0	
I_{012}	—	—	27	0	
I_{345}	—	—	27	0	
I_{678}	16	DO NOT CHANGE (Note 2)		0	
RAM0, 15 and Q0, 15	—	—	21	4	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here.

ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59016CB	C	64 Pin Ceramic Sidebrazed DIP, 0.9″	B1	Comm'l	Standard
WS59016CBMB	C	64 Pin Ceramic Sidebrazed DIP, 0.9″	B1	Military	MIL-STD-883C
WS59016CJ	C	68 Pin PLDCC	J1	Comm'l	Standard
WS59016CL	C	68 Pin CLDCC	L1	Comm'l	Standard
WS59016CLMB	C	68 Pin CLDCC	L1	Military	MIL-STD-883C
WS59016DB	D	64 Pin Ceramic Sidebrazed DIP, 0.9″	B1	Comm'l	Standard
WS59016DBMB	D	64 Pin Ceramic Sidebrazed DIP, 0.9″	B1	Military	MIL-STD-883C
WS59016DJ	D	68 Pin PLDCC	J1	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

CMOS 32-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **Eight CMOS 2901 Type Devices in a Single Package**
- **32 x 32 Dual Port RAM**
- **Low CMOS Power**
  — 350 mW
- **High Speed Operation**
  — 23 MHz Read-Modify-Write Cycle
- **Fully Firmware Compatible with the 2901**
- **On Board Carry Look-Ahead**

GENERAL DESCRIPTION

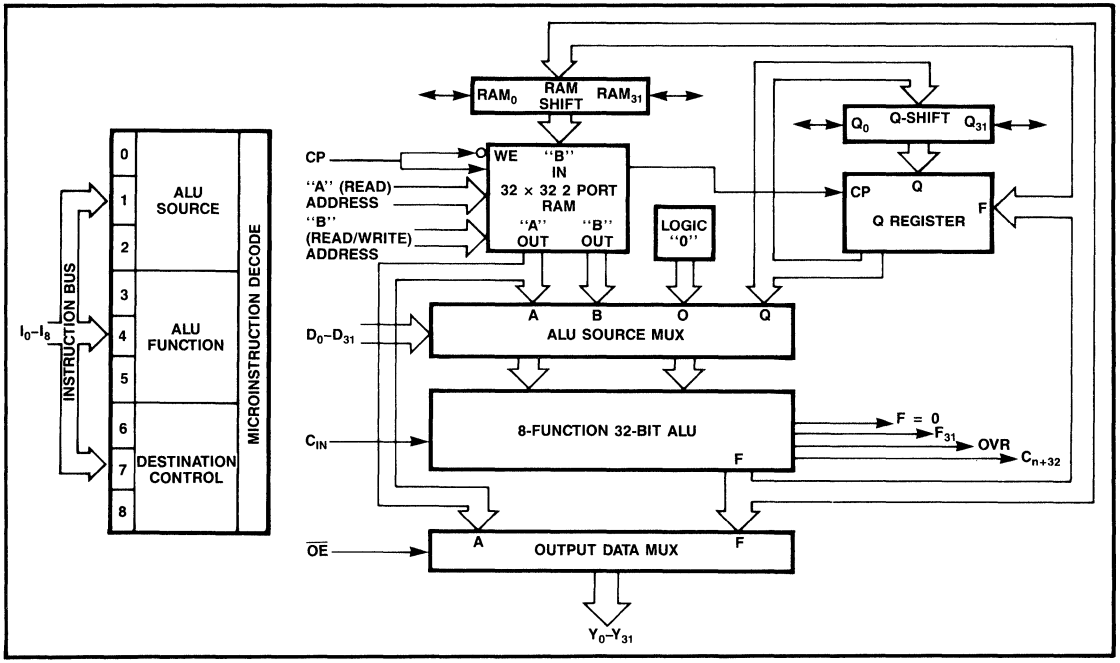
The WS59032 is a 32-bit High-Speed microprocessor which combines the functions of eight 2901 4-bit slice processors and distributed look-ahead carry generation on a single High Performance CMOS device. The WS59032 dual port RAM is 32-bits wide and 32 words deep. This architecture provides greater flexibility and eases the task of generating new microcode while maintaining 100% compatible with existing 2901 based microcode.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the WS59032 is manufactured, provides significant performance improvements over an equivalent Bipolar device configuration. While operating faster than a 2901C based system, the WS59032 requires less than 3% of the power consumed by an equivalent Bipolar system.

The WS59032 is also available as a macro cell in the WaferScale cell library. As such it can be combined with other cells to build Application Specific Integrated Circuits.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Signal Name	I/O	Description
A0-4	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-4	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low.
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678).
Q31, RAM31	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM31 pin and the MSB of the Q-register is available on the Q31 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Q0, RAM0	I/O	Shift lines similar to Q31 and RAM31. however the description is applied to the LSB of RAM and the Q-register.
D0-D31	I	These thirty two direct data inputs can be selected as a data source for the ALU. DO is the LSB.
Y0-Y31	O	These thirty two three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678.
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state. When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y31. as determined by I678.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F=0	O	This output, when high, indicates the result of an ALU operation is zero.
F31	O	The most significant ALU output bit.
Cn	I	The carry-in to the ALU.
Cn+32	O	The carry-out of the ALU.
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board dual port RAM, including set-up time for the A and B-port registers. The A and B-port outputs change while the clock is high. The Q-register is latched on the clock low-to-high transition.

PIN DESIGNATOR

PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #
VCC	N1	B3	N2	D23	B1	Y7	K12
VCC	A1	B4	M3	D24	B2	Y8	K13
GND	N7	D0	N6	D25	B3	Y9	J12
GND	G13	D1	M6	D26	A2	Y10	J13
GND	A12	D2	L6	D27	A3	Y11	H11
GND	C6	D3	N5	D28	B4	Y12	H12
RAM0	M7	D4	M5	D29	A4	Y13	H13
RAM31	B6	D5	N4	D30	B5	Y14	G12
Q0	L7	D6	M4	D31	A5	Y15	G11
Q31	A6	D7	N3	I0	N8	Y16	F13
CLK	A7	D8	H3	I1	M8	Y17	F12
CIN	N13	D9	H2	I2	L8	Y18	F11
CN+32	A9	D10	H1	I3	N9	Y19	E13
OVR	C8	D11	G1	I4	M9	Y20	E12
F=0	C13	D12	G3	I5	N10	Y21	D13
F31	B8	D13	G2	I6	A8	Y22	D12
OEN	M12	D14	F1	I7	B7	Y23	B13
A0	J1	D15	F2	I8	C7	Y24	C12
A1	J2	D16	F3	Y0	M10	Y25	A13
A2	K1	D17	E1	Y1	N11	Y26	B12
A3	K2	D18	E2	Y2	N12	Y27	B11
A4	L1	D19	D1	Y3	M11	Y28	A11
B0	M1	D20	D2	Y4	M13	Y29	B10
B1	L2	D21	C1	Y5	L12	Y30	A10
B2	M2	D22	C2	Y6	L13	Y31	B9

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... −55°C to +125°C
Storage Temp. (No bias) ... −65°C to +150°C
Voltage on any pin with
respect to GND ..... −0.6V to +7V
Latch Up Protection ..... >200 mA
ESD Protection ..... > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

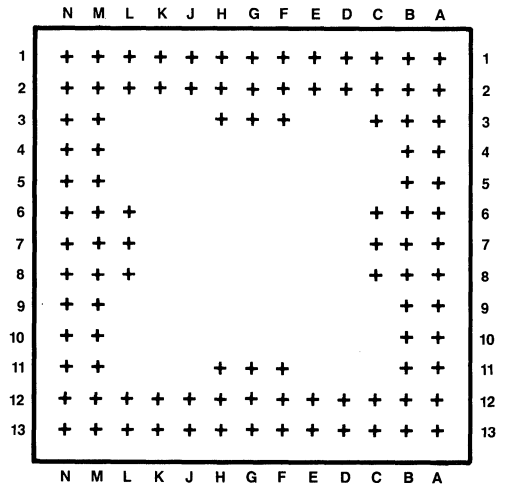
DC CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{oh}	Output High Voltage	V_{CC} = Min. V_{in} = V_{ih} or V_{il}	All outputs	I_{oh} = −1.6mA	2.4		V
V_{ol}	Output Low Voltage	V_{CC} = Min V_{in} = V_{ih} or V_{il}	Y0-Y31	I_{ol} = 12mA Com'l		0.5	V
				I_{ol} = 9mA Mil			
			All others	I_{ol} = 8mA			
V_{ih}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{il}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{ix}	Input Load Current	V_{CC} = Max, V_{in} = Gnd or V_{CC}			−10	10	µA
I_{oz}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{cc}	Power Supply Current	V_{CC} = Max	Comm'l (0°C to +70°C)			70	mA
			Mil (−55°C to +125°C)			85	mA

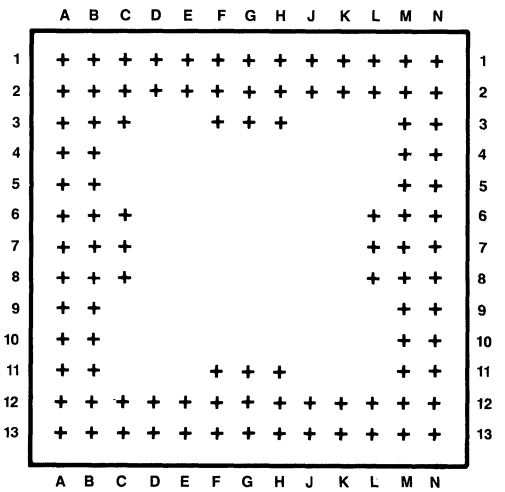
NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

PACKAGE ORIENTATION

101 PIN PGA PACKAGE



TOP VIEW
(THROUGH PACKAGE VIEW)



BOTTOM VIEW

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1 : ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EXOR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NORS	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; $\veebar$ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1, and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4, and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS59032 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \veebar Q$
6 1		$A \veebar B$
6 5		$D \veebar A$
6 6		$D \veebar Q$
7 0	EX-NOR	$\overline{A \veebar Q}$
7 1		$\overline{A \veebar B}$
7 5		$\overline{D \veebar A}$
7 6		$\overline{D \veebar Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

4

WS59032D COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	51ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	26.4 MHz
Minimum Clock Low Time	22ns
Minimum Clock High	26ns
Minimum Clock Period	48ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30ns
From $\overline{OE}$ High to output disable	25ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F=0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	66	66	58	66	62	75	—	ns
D0-D31	45	45	35	45	35	48	—	
C_n	36	36	18	36	32	42	—	
I_{012}	46	46	35	46	41	58	—	
I_{345}	51	51	41	51	46	53	—	
I_{678}	22	—	—	—	—	22	20	
A BYPASS ALU (I = 2XX)	46	—	—	—	—	—	—	
CLOCK	51	51	42	51	46	59	22	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	20	1 (Note 3)	53 (Note 4)	0	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		0	
D0-D31	—	—	20	0	
C_n	—	—	22	0	
I_{012}	—	—	28	0	
I_{345}	—	—	30	0	
I_{678}	7	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	7	3	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032D MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	60ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	23.6 MHz
Minimum Clock Low Time	28ns
Minimum Clock High	30ns
Minimum Clock Period	60ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	36ns
From $\overline{OE}$ High to output disable	30ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	72	72	63	69	69	81	—	ns
D0-D31	51	51	40	52	42	52	—	
C_n	41	41	21	39	36	36	—	
I_{012}	48	48	40	48	44	63	—	
I_{345}	54	54	46	56	51	57	—	
I_{678}	27	—	—	—	—	21	20	
A BYPASS ALU (I = 2XX)	51	—	—	—	—	—	—	
CLOCK	58	58	50	58	53	66	29	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	25	1 (Note 3)	63 (Note 4)	1	ns
B Destination Address	25	DO NOT CHANGE (Note 2)		1	
D0-D31	—	—	30	0	
C_n	—	—	30	0	
I_{012}	—	—	36	0	
I_{345}	—	—	42	0	
I_{678}	13	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	10	5	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032E COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032E over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	42ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	33 MHz
Minimum Clock Low Time	18ns
Minimum Clock High	21ns
Minimum Clock Period	40ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	25ns
From $\overline{OE}$ High to output disable	20ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT / TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	55	55	48	55	51	62	—	ns
D0-D31	37	37	29	37	29	40	—	
C_n	30	30	15	30	26	35	—	
I_{012}	38	38	29	38	34	48	—	
I_{345}	42	42	34	42	38	44	—	
I_{678}	18	—	—	—	—	18	16	
A BYPASS ALU (I = 2XX)	38	—	—	—	—	—	—	
CLOCK	42	42	35	42	38	49	18	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT / CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	20	0 (Note 3)	44 (Note 4)	0	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		0	
D0-D31	—	—	18	0	
C_n	—	—	20	0	
I_{012}	—	—	26	0	
I_{345}	—	—	29	0	
I_{678}	5	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	5	3	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032E MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032E over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	50ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	29 MHz
Minimum Clock Low Time	23ns
Minimum Clock High	25ns
Minimum Clock Period	50ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30 ns
From $\overline{OE}$ High to output disable	30 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	60	60	52	57	57	67	—	ns
D0-D31	42	43	33	43	35	43	—	
C_n	34	34	17	32	30	30	—	
I_{012}	40	40	33	40	36	52	—	
I_{345}	45	45	38	46	42	47	—	
I_{678}	22	—	—	—	—	17	16	
A BYPASS ALU (I = 2XX)	42	—	—	—	—	—	—	
CLOCK	48	48	41	48	44	55	24	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	23	0 (Note 3)	52 (Note 4)	1	ns
B Destination Address	23	DO NOT CHANGE (Note 2)		1	
D0-D31	—	—	25	0	
C_n	—	—	25	0	
I_{012}	—	—	30	0	
I_{345}	—	—	35	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	7	5	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

COMPETITIVE TIMING ANALYSIS

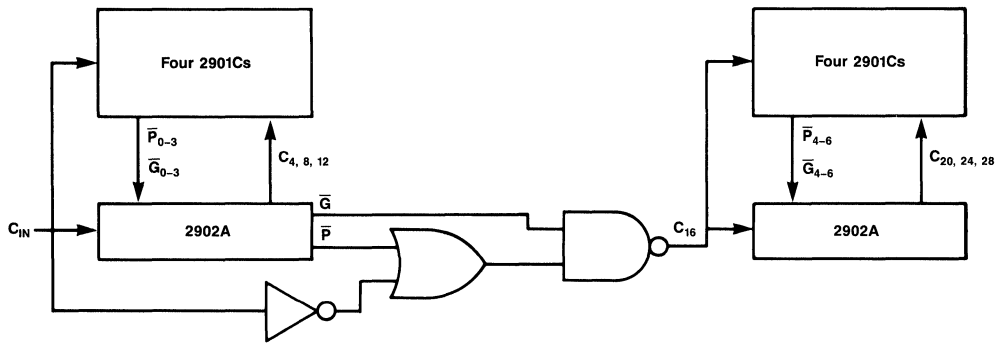
The following analysis compares the critical timing paths of a WS59032E vs. the equivalent Bipolar circuit implementation using eight 2901C's, two 2902A's and three high speed logic gates (See Figure).

As can be seen from the following comparison, the Data Path of the WS59032E is 44% faster than the Data Path of the Bipolar/ECL functional equivalent circuit. Additionally, the Control Path of the WS59032E is 50% faster than the Bipolar/ECL implementation. The actual values for the Bipolar/ECL circuit will be lengthened by the layout dependent interconnect delays between the individual devices. When these delays are taken into account, the WS59032E speed advantage becomes even greater.

TIMING COMPARISON
WS59032D vs Eight 2901C's, Two 2902A's Plus High Speed Logic

DATA PATH		CONTROL PATH	
WS59032E		**WS59032E**	
A,B Address	F = Ø = 55ns	I 012	F = Ø = 48ns
interconnect delay	= Øns	interconnect delay	= Øns
Total Delay	≤ 55ns	Total Delay	≤ 48ns
DISCRETE IMPLEMENTATION (See Figure)		DISCRETE IMPLEMENTATION (See Figure)	
A,B	$\overline{P}_3,\overline{G}_3$ = 37ns	I 012	F = Ø = 37ns
$\overline{P}_3,\overline{G}_3$	$\overline{P},\overline{G}$ = 11ns	$\overline{P}_3,\overline{G}_3$	$\overline{P},\overline{G}$ = 11ns
$\overline{P},\overline{G}$	C_{16} = 10ns	$\overline{P},\overline{G}$	C_{16} = 10ns
C_{16}	C_{28} = 14ns	C_{16}	C_{28} = 14ns
C_{28}	F = Ø = 25ns	C_{28}	F = Ø = 25ns
interconnect delay	= Xns	interconnect delay	= Xns
Total Delay	> 97ns	Total Delay	> 97ns

Look-Ahead Carry Using Discrete Components



ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59032DG	D	101 Pin Ceramic PGA	G2	Comm'l	Standard
WS59032DGMB	D	101 Pin Ceramic PGA	G2	Military	MIL-STD-883C
WS59032EG	E	101 Pin Ceramic PGA	G2	Comm'l	Standard
WS59032EGMB	E	101 Pin Ceramic PGA	G2	Military	MIL-STD-883C

CMOS MICROPROGRAM CONTROLLER

KEY FEATURES

- **High Speed Operation**
  — 50% Faster Than Bipolar
- **Low Power**
  — 225 mW
- **On-Board Stack**
  — 9 Words Deep
- **Bipolar Replacement**
  — Fully Compatible with AM2910A
- **Immune to Latch-Up**
  — Over 200 mA
- **ESD Protection**
  — Exceeds 2000 Volts

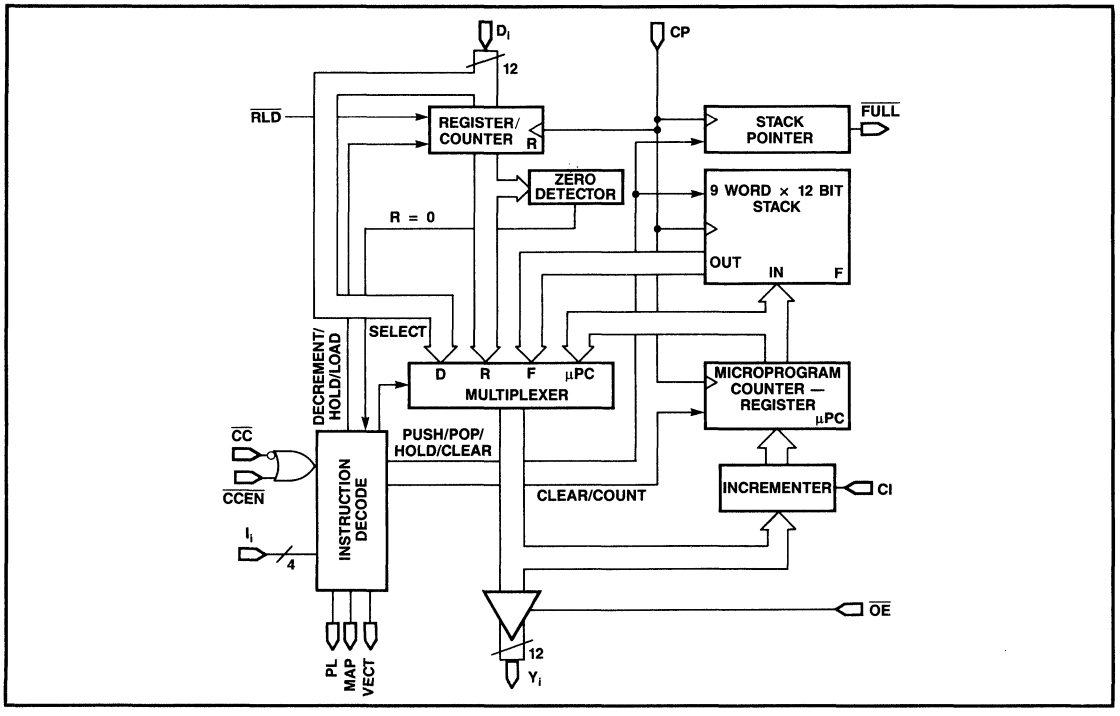
GENERAL DESCRIPTION

The WS5910A/B microprogram controller is an address sequencer which provides addresses to a control store memory. These addresses can come from one of four internal sources: 1) the Microprogram Counter, 2) the 9 word × 12 bit stack, 3) the 12-bit Register/Counter, or 4) the Direct Data Input. The address source selected is dependent upon the instruction applied to the WS5910A/B.

The device can sequentially address memory or it can provide a conditional branch address anywhere within its addressing range. In addition, the WS5910A/B also contains a last-in, first-out stack which provides capabilities for looping as well as providing the microsubroutine return linkage. The on-board register/counter provides loop count control with a count capacity of 4096.

The CMOS WS5910A/B is a form, fit and function replacement for the bipolar/ECL AM2910A. A.C. performance and output drive capability, meet or exceed the specifications of its bipolar counterpart. The WS5910A/B is also available as a macro cell in the WSI cell library.

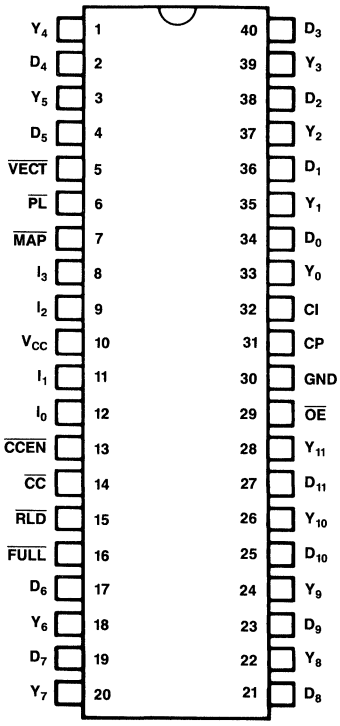
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SIGNAL NAME	I/O	DESCRIPTION
Di	I	Direct Input to Register/Counter and Multiplexer. D_0 is LSB.
Ii	I	Instruction Inputs to the WS5910A/B
$\overline{CC}$	I	Condition Code Input. Pass Test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	I	When HIGH, $\overline{CC}$ Input is Ignored and Internally Forced LOW
CI	I	Carry Input to the LSB of the Microprogram Counter
$\overline{RLD}$	I	When LOW, Register/Counter is Loaded Regardless of Instruction or Condition
$\overline{OE}$	I	Three State Control of Yi Outputs
Yi	O	Address to Microprogram Memory. Y_0 is LSB.
CP	I	All Internal States Change at LOW-to-HIGH Edge
$\overline{FULL}$	O	Stack Full Indicator. (Stack is Nine Levels Deep.)
$\overline{PL}$	O	Active LOW Signal Used to Select the Pipeline Register as the Direct Input Source
$\overline{MAP}$	O	Active LOW Signal Used to Select the Mapping PROM (or PLA) as the Direct Input Source
$\overline{VECT}$	O	Active LOW Signal Used to Select the Interrupt Vector as the Direct Input Source

PIN CONFIGURATION



TOP

INTRODUCTION

The WS5910A/B is a high performance CMOS microprogram controller that produces a sequence of addresses which control the execution of a microprogram. These 12-bit addresses are selected from one of the four sources which feed into a 12-bit 4 to 1 multiplexer. The source selected can be 1) the direct data inputs (D_0-D_{11}), 2) the Register/Counter, 3) the Microprogram Counter, or 4) the stack register. Selection is dependent upon which of the sixteen instructions is being executed as well as other external inputs. The selected source is used to drive the Y_0-Y_{11} three state output buffers.

External Inputs: D_0-D_{11}

The external inputs can be used to supply the jump address for conditional branch types of instructions. They can also be used to load the register counter.

Register Counter

The RC is an edge triggered 12-bit register which is clocked on the LOW-to-HIGH (positive) transition of the clock, CP. The RC is loaded synchronously from the D inputs when the load control input, RLD, is LOW. The output of RC is referred to as R in the table of instructions.

The RC operates as a 12-bit down counter and is decremented and tested for a zero result during instructions 8, 9, and 15. If the RC is loaded with a number N, the sequence will be executed N + 1 times. This allows microinstructions to be repeated up to 4096 times.

THE STACK AND STACK POINTER

The last-in-first-out stack, which is 9 levels deep by 12-bits wide, provides return addresses from micro-subroutine or from loops. Integral to it is the stack pointer which points to the last word written. This allows data on the top of the stack to be referenced without having to perform a POP operation.

There are five microinstructions during which a POP operation may occur (8, 10, 11, 13, 15). A POP decrements the stack pointer at the next rising clock edge following the microinstruction causing the POP. The stack pointer points to zero when the stack is empty. A POP from an empty stock may place unknown data on the Y outputs. The stack pointer remains at zero if a POP is attempted on an empty stack.

There are three operations during which a PUSH operation may occur (1, 3, and 5). A PUSH increments the stack pointer and the return linkage is then written into the stack at the location pointed to by the just incremented stack pointer. RESET (instruction 0) forces the stack pointer to zero, effectively emptying the stack. Each PUSH increments the stack pointer by one, each POP decrements the stack pointer by one. When the stack reaches the level of nine (stack pointer equals nine), the FULL flag goes low. This flag indicates that a POP should occur prior to the next PUSH. If a PUSH does occur on a full stack, the data is overwritten at the top of the stack (location nine) but the stack pointer remains unchanged. The operation will usually destroy useful information and is normally avoided.

TABLE OF INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CONTENTS	RESULT					
				FAIL $\overline{CCEN}$=L and $\overline{CC}$=H		PASS $\overline{CCEN}$=H or $\overline{CC}$=L		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	Note 1	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠ 0	F	Hold	F	Hold	Dec	PL
			= 0	PC	Pop	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠ 0	PC	Hold	D	Hold	Dec	PL
			= 0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠ 0	F	Hold	PC	Pop	Dec	PL
			= 0	D	Pop	PC	Pop	Hold	PL

NOTE: 1) If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load. H = HIGH L = LOW X = Don't Care

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
Latch Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Temperature Range (See Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OL} = 12 mA		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	V
I_{BC}	Input Load Current	V_{CC} = Max, V_{IN} = GND or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = GND or V_{CC}			−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	0°C to +70°C (Comm'l)			45	mA
			−55°C to +125°C (Mil)			70	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

WS5910A
COMMERCIAL RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910A over the commercial operating range of 0°C to +70°C and a power supply range of 5V ± 5%.

Inputs are switching between 0 and 3V with rise and fall times of 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	20	ns
Minimum Clock HIGH Time	20	
Minimum Clock Period	50	
Maximum Clock Frequency	20	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	20	—	—	ns
I_0-I_3	35	30	—	
CC	30	—	—	
CCEN	30	—	—	
CP	40	—	31	

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	25	ns
From $\overline{OE}$ HIGH to Y Output Disable	27	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di → R	16	0	ns
Di → PC	30	0	
I_0-I_3	35	0	
CC	24	0	
CCEN	24	0	
CI	18	0	
RLD	19	0	

WS5910A
MILITARY RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910A over the military operating range of −55°C to +125°C and a power supply range of 5V ± 10%.

Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	25	ns
Minimum Clock HIGH Time	25	
Minimum Clock Period	51	
Maximum Clock Frequency	19.6	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	25	—	—	ns
I_0-I_3	40	35	—	
CC	36	—	—	
CCEN	36	—	—	
CP	46	—	35	

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	25	ns
From $\overline{OE}$ HIGH to Y Output Disable	30	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di → R	16	0	ns
Di → PC	30	0	
I_0-I_3	38	0	
CC	35	0	
CCEN	35	0	
CI	18	0	
RLD	20	0	

WS5910B
COMMERCIAL RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910B over the commercial operating range of 0°C to +70°C and a power supply range of 5V ± 5%.

Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	13	ns
Minimum Clock HIGH Time	13	
Minimum Clock Period	33	
Maximum Clock Frequency	30	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	18	—	—	ns
I_0-I_3	24	—	—	
CC	21	—	—	
CCEN	21	—	—	
CP	27	—	20	

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	21	ns
From $\overline{OE}$ HIGH to Y Output Disable	22	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di → R	11	0	ns
Di → PC	20	0	
I_0-I_3	23	0	
CC	16	0	
CCEN	16	0	
CI	12	0	
RLD	12	0	

WS5910B
MILITARY RANGE
AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5910B over the military operating range of −55°C to +125°C and a power supply range of 5V ± 10%.

Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

Minimum Clock LOW Time	17	ns
Minimum Clock HIGH Time	17	
Minimum Clock Period	35	
Maximum Clock Frequency	29	MHz

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

INPUT	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$	UNITS
D_0-D_{11}	22	—	—	ns
I_0-I_3	26	23	—	
CC	24	—	—	
CCEN	24	—	—	
CP	30	—	24	

OUTPUT ENABLE/DISABLE TIME

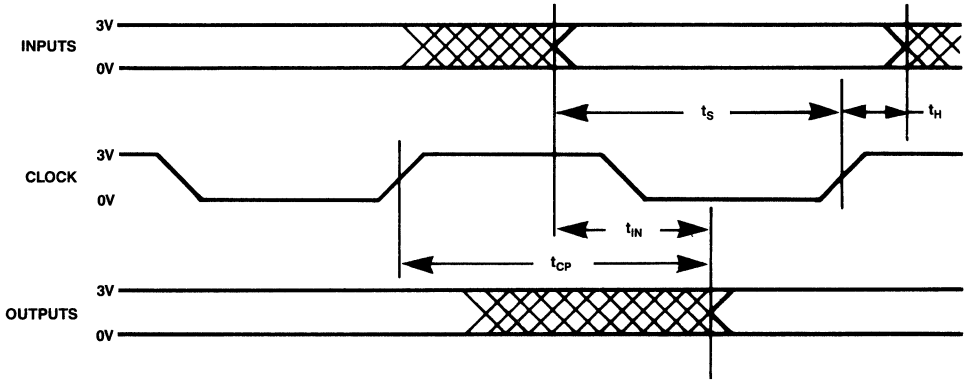
Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ LOW to Y Output Enable	24	ns
From $\overline{OE}$ HIGH to Y Output Disable	25	

SET UP AND HOLD TIMES

INPUT	t_S	t_H	UNITS
Di → R	11	0	ns
Di → PC	20	0	
I_0-I_3	25	0	
CC	23	0	
CCEN	23	0	
CI	12	0	
RLD	13	0	

SWITCHING WAVEFORMS



ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS5910AP	20 MHz	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WS5910ADMB	20 MHz	40 Pin CERDIP, 0.6″	Y1	Military	MIL-STD-883C
WS5910BP	30 MHz	40 Pin Plastic DIP, 0.6″	P1	Comm'l	Standard
WS5910BDMB	30 MHz	40 Pin CERDIP, 0.6″	Y1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

16 X 16 MULTIPLIER ACCUMULATOR

KEY FEATURES

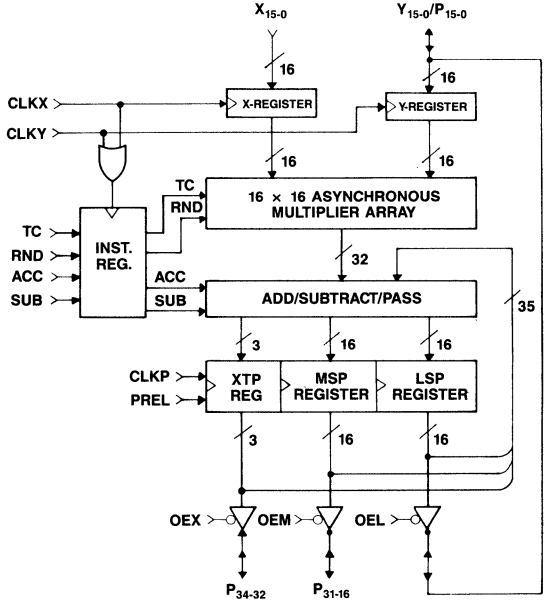
- **16 X 16 Bit Parallel Multiplication with Accumulation to 35-Bit Result**
- **Fast**
  — 30 ns Multiply Accumulate Time
- **Low Power**
  — I_{CC} = 100 mA (10 MHz)
- **Two's complement or unsigned magnitude operation**
- **Immune to latch-up**
  — Over 200 mA
- **Pin compatible and functionally equivalent to Am29510 and TDC1010**

FUNCTIONAL DESCRIPTION

The WS59510 is a high-speed 16 x 16 parallel multiplier accumulator which operates at 30 ns clocked multiply accumulate (MAC) time (33 MHz multiply accumulate rate). The operands may be specified as either two's complement or unsigned magnitude 16-bit numbers. The accumulator functions include loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, or preloading the accumulator from the external world.

All inputs (data and instructions) and outputs are registered. These independently clocked registers are positive edge triggered D-type flip-flops. The 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most significant product (MSP), and a 16-bit least significant product (LSP). The XTP and MSP have dedicated ports for three-state output; the LSP is multiplexed with the Y-input. The 35-bit accumulator/output register may be preloaded through the bidirectional output ports.

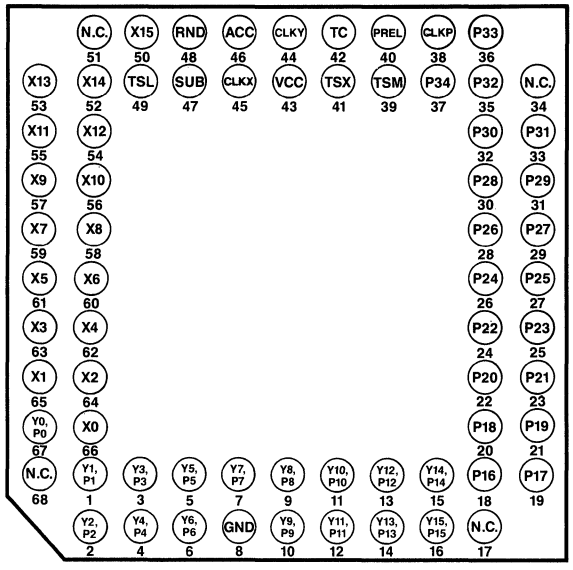
FUNCTIONAL BLOCK DIAGRAM



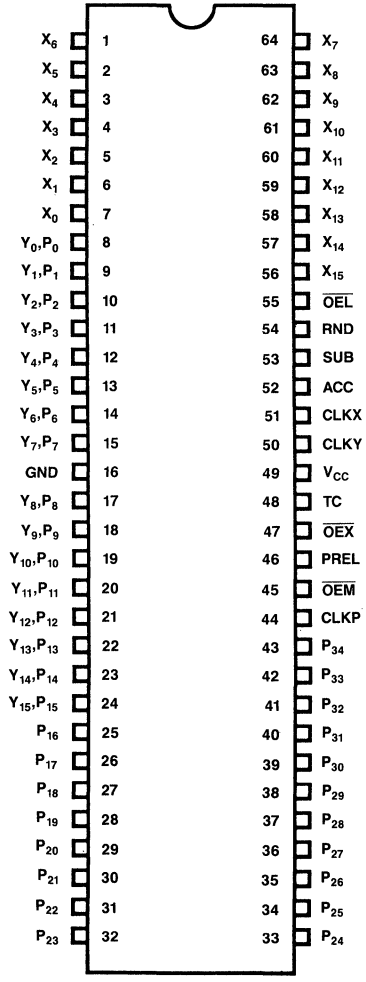
PRODUCT SELECTION GUIDE

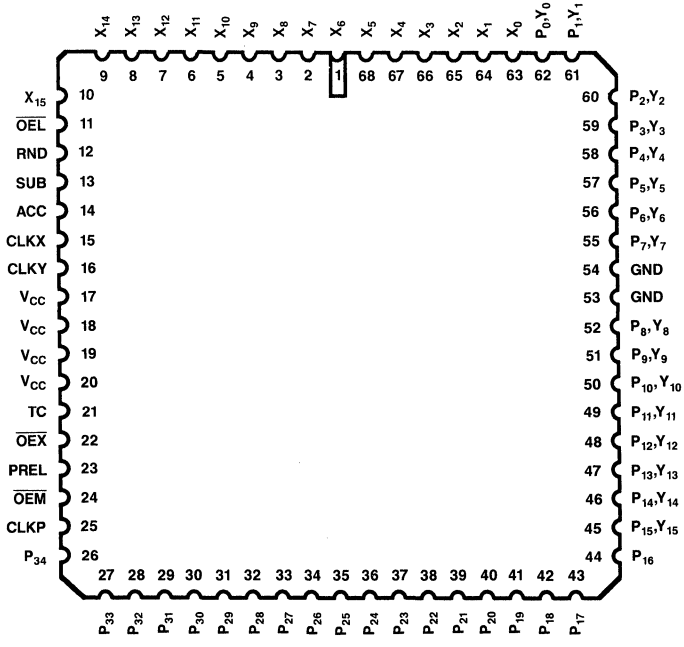
		59510-30	59510-40	59510—50
Maximum Multiply-Accumulate Time (ns)	Commercial	30	40	—
	Military	—	40	50

PIN CONFIGURATIONS



TOP
(Through Package View)





TOP VIEW

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
54	RND	I	Round When RND is High, a bit with a weight of P_{15} is added to the multiplier product. RND is loaded on the rising edge of CLKx or CLKy.
48	TC	I	Two's Complement When High, the X and Y inputs are defined as two's complement data, or as unsigned data when Low. The TC control is loaded on the rising edge of CLKx or CLKy.
46	PREL	I	Preload When High, data is preloaded into the specific output register when its respective Load Enable is High. When Low, the accumulator register is available at the P-port when the Output Enables are Low.
47	LEx/$\overline{OE}$x	I	Load Enable Extended/Output Enable Extended Active High Load Enable for the XTP port during preloading. Active Low three-state control for the XTP port during normal operation (see Preload Function). (TSX)**
45	LEm/$\overline{OE}$m	I	Load Enable Most/Output Enable Most Active High Load Enable for the MSP port during preloading. Active Low three-state control for the MSP port during normal operation (see Preload Function). (TSM)**
55	LEL/$\overline{OE}$L	I	Load Enable Least/Output Enable Least Active High Load Enable for the LSP port during preloading. Active Low three-state control for the LSP port during normal operation (see Preload Function). (TSL)**
51, 50	CLK_x, CLK_y	I	CLOCKS Load X and Y data respectively and TC, RND, ACC and SUB/$\overline{ADD}$ on the rising edge.
44	CLK_P	I	CLOCK Loads data into the XTP, MSP and LSP registers on the rising edge.
1-7, 56-64	X_{15}-X_0	I	Multiplier Data Input Data is loaded into the X register on the rising edge of CLK_x.
8-15, 17-24	Y_{15}-Y_0 P_{15}-P_0	I/O	Bidirectional Port Data is loaded into the Y register on the rising edge of CLK_y. Product output for least Significant Product (LSP) and input to preload LSP register.
41-43	P_{34}-P_{32}	I/O	Bidirectional Port Product output for extended Product (XTP) and input to preload XTP register.
25-40	P_{31}-P_{16}	I/O	Bidirectional Port Product output for the Most Significant Product (MSP) and input to preload MSP register.
52	ACC	I	Accumulate When High, the multiplier product is accumulated in the accumulator. When Low, the multiplier product is written into the accumulator (see Accumulator Function Table). The ACC control is loaded on the rising edge of CLKx or CLKy.
53	SUB/$\overline{ADD}$	I	Subtraction/Addition When High, the accumulator contents are subtracted from the multiplier product and the result written back into the accumulator. When Low, the multiplier product is added into the accumulator (see Accumulator Function Table). The SUB/$\overline{ADD}$ control is loaded on the rising edge of CLKx or CLKy.

*DIP Configuration
**TRW TDC1010 Pin Designation

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... -55°C to +125°C
Storage Temp. (No bias) ..... -65°C to +150°C
Voltage on any pin with
respect to GND ..... -0.6V to +7V
Latch Up Protection ..... >200 mA
ESD Protection ..... > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{oh}	Output High Voltage	V_{cc}=Min. V_{in}=V_{ih} or V_{il}	All outputs	I_{oh} = -1.6mA	2.4		V
V_{ol}	Output Low Voltage	V_{cc}=Min V_{in}=V_{ih} or V_{il}	Y0-Y31	I_{ol}=12mA Comm'l		0.5	V
			Y0-Y31	I_{ol}=9mA Mil			
			All others	I_{ol}=8mA			
V_{ih}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{il}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{ix}	Input Load Current	V_{cc} = Max, V_{in} = Gnd or V_{cc}			-10	10	μA
I_{oz}	High Impedance Output Current	V_{cc} = Max, V_o = Gnd or V_{cc}			-50	50	μA
I_{cc}	Power Supply Current	V_{cc} = Max	Comm'l. (0°C to +70°C)			100	mA
			Mil (−55°C to +125°C)			110	

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to +70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

DETAILED DESCRIPTION

The WS59510 is a high-speed 16 x 16-bit multiplier accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. All inputs (data and instructions) and outputs are registered. The WS59510 is divided into four sections: the input section, the 16 x 16 asynchronous multiplier array, the accumulator, and the output/preload section.

The input section has two 16-bit operand input registers for the X and Y operands, clocked by the rising edge of CLKX and CLKY, respectively. The four-bit instruction register (TC, RND, ACC, SUB) is clocked by the rising edge of the logical OR of CLKX, CLKY.

The 16 x 16 asynchronous multiplier array produces the 32-bit product of the input operands. Either two's complement or unsigned magnitude operation is selected, based on control TC. If rounding is selected, (RND = 1), a "1" is added to the MSB of the LSP (position P_{15}). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator function is controlled by ACC, SUB, and PREL. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be preloaded from the bidirectional ports.

The output/preload section contains the accumulator/output register and the bidirectional ports. This section is controlled by the signals PREL, $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$. When PREL is HIGH, the output buffers are in high impedance state. When the controls $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are also high, data present at the output pins will be preloaded into the appropriate accumulator register at the rising edge of CLKP. When PREL is LOW, the signals $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are enable controls for their respective three-state output ports.

WS59510
Input Formats

Fractional Two's Complement Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
(Sign)															

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15
(Sign)															

Integer Two's Complement Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
(Sign)															

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
(Sign)															

Unsigned Fractional Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16

Unsigned Integer Input

XIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

YIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

WS59510
Output Formats

Two's Complement Fractional Output

XTP			MSP														LSP														
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-24	23	22	21	20	2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16	2-17	2-18	2-19	2-20	2-21	2-22	2-23	2-24	2-25	2-26	2-27	2-28	2-29	2-30
(Sign)																																		

Two's Complement Integer Output

XTP			MSP																LSP													
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-234	233	232	231	230	229	228	227	226	225	224	223	222	221	220	219	218	217	216	215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20
(Sign)																																		

Unsigned Fractional Output

XTP			MSP																LSP													
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
221	220		2-1	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	2-12	2-13	2-14	2-15	2-16	2-17	2-18	2-19	2-20	2-21	2-22	2-23	2-24	2-25	2-26	2-27	2-28	2-29	2-30	2-31	2-32

Unsigned Integer Output

XTP			MSP																LSP													
34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-234	233	232	231	230	229	228	227	226	225	224	223	222	221	220	219	218	217	216	215	214	213	212	211	210	29	28	27	26	25	24	23	22	21	20

SWITCHING CHARACTERISTICS Over Operating Range

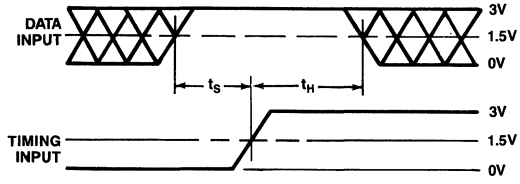
DESCRIPTION		PARAMETERS	WS59510-30		WS59510-40		WS59510-50		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
Multiply Accumulate Time		t_{MA}		30		40		50	ns
Setup Time (X_{IN},Y_{IN},RND,TC,ACC,SUB)		t_{S1}	5		5		5		ns
Setup Time (PREL,$\overline{OEX}$,$\overline{OEM}$,$\overline{OEL}$)		t_{S2}	15		15		15		ns
Hold Time		t_H	2		2		2		ns
Clock Pulse Width		t_{PW}	10		10		15		ns
Output Clock to P		t_{PDP}		20		25		30	ns
Output Clock to Y		t_{PDY}		20		25		30	ns
$\overline{OEX}$, $\overline{OEM}$ to P;	High to Z	t_{PHZ}		20		25		30	ns
$\overline{OEL}$ to Y (Disable Time)	Low to Z	t_{PLZ}		20		25		30	ns
$\overline{OEX}$, $\overline{OEM}$ to P;	Z to High	t_{PZH}		20		25		30	ns
$\overline{OEL}$ to Y (Enable Time)	Z to Low	t_{PZL}		20		25		30	ns
Relative Hold Time		t_{HCL}	0		0		0		ns

NOTE: Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All inputs have maximum DC load.

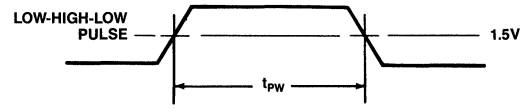
TEST WAVEFORMS

Test	V_X	OUTPUT WAVEFORM - MEASUREMENT LEVEL
All t_{PD}'s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, 0.5V, V_{OL}
t_{PZH}	0.0V	V_{OH}, 1.5V, 0.0V
t_{PZL}	2.6V	2.6V, 1.5V, V_{OL}

Setup and Hold Time

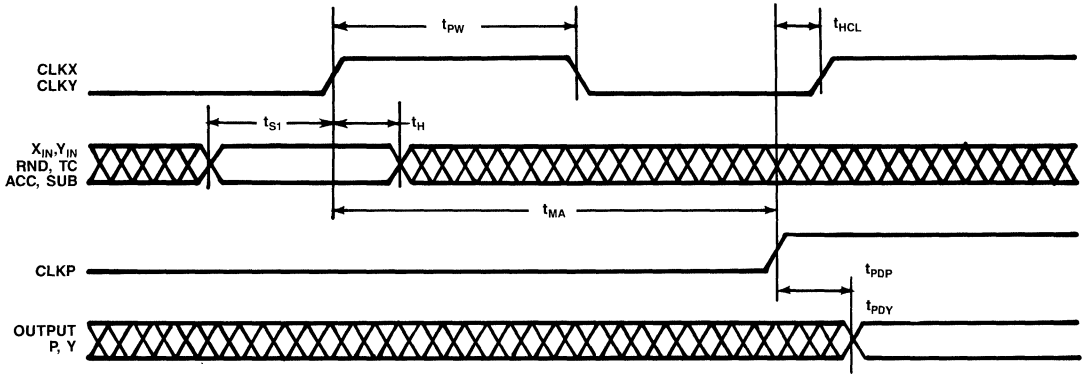


Pulse Width



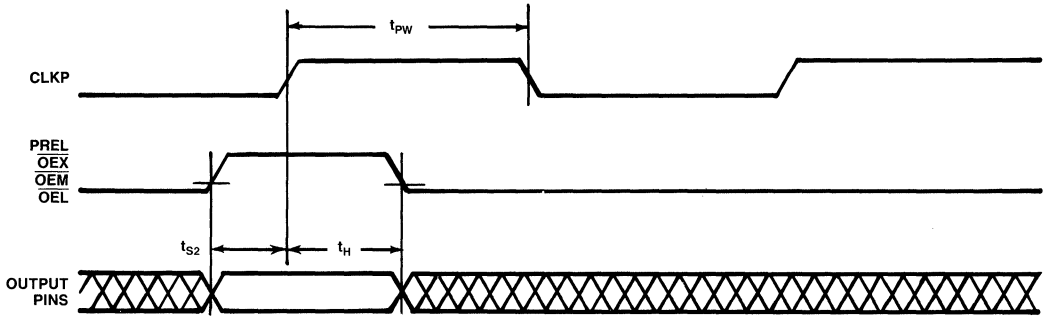
Notes:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

WS59510 TIMING DIAGRAM

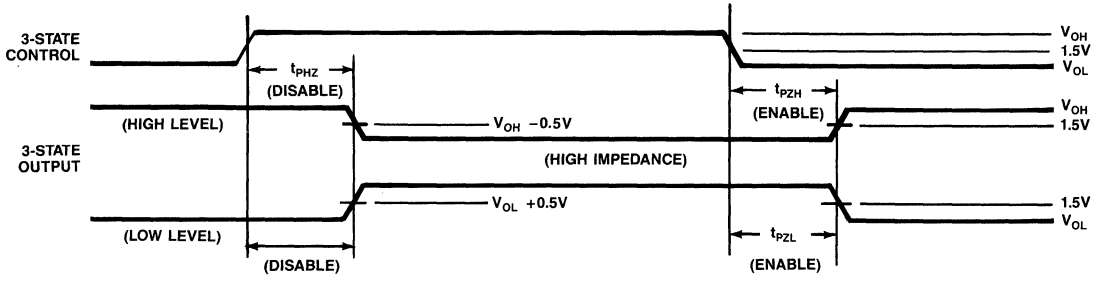


4

PRELOAD TIMING DIAGRAM



THREE-STATE TIMING DIAGRAM



ACCUMULATOR FUNCTION TABLE

PREL	ACC	SUB/$\overline{ADD}$	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

PRELOAD FUNCTION

PREL	LEx/$\overline{OE_X}$	LEm/$\overline{OE_M}$	LEL/$\overline{OE_L}$	Output Register XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = output buffers at High impedance (disabled).
Q = output buffers at Low impedance. Contents of output register available through output ports.
PL = output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKp.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59510-30J	30	68 Pin PLDCC	J1	Comm'l	Standard
WS59510-40G	40	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59510-40GMB	40	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C
WS59510-40J	40	68 Pin PLDCC	J1	Comm'l	Standard
WS59510-40P	40	64 Pin Plastic DIP, 0.9″	M1	Comm'l	Standard
WS59510-50G	50	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59510-50GMB	50	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C
WS59510-50J	50	68 Pin PLDCC	J1	Comm'l	Standard
WS59510-50P	50	64 Pin Plastic DIP, 0.9″	M1	Comm'l	Standard

WAFERSCALE INTEGRATION, INC.

MULTILEVEL PIPELINE REGISTER

KEY FEATURES

- Four 8-Bit Registers
- Contents of Each Register Available at Output
- 24-Pin 300 Mil Package
- Dual Two Stage or Single Four Stage Push Only Stack Operation
- Hold, Transfer and Load Instructions
- High Performance CMOS
- TTL Compatible

4

GENERAL DESCRIPTION

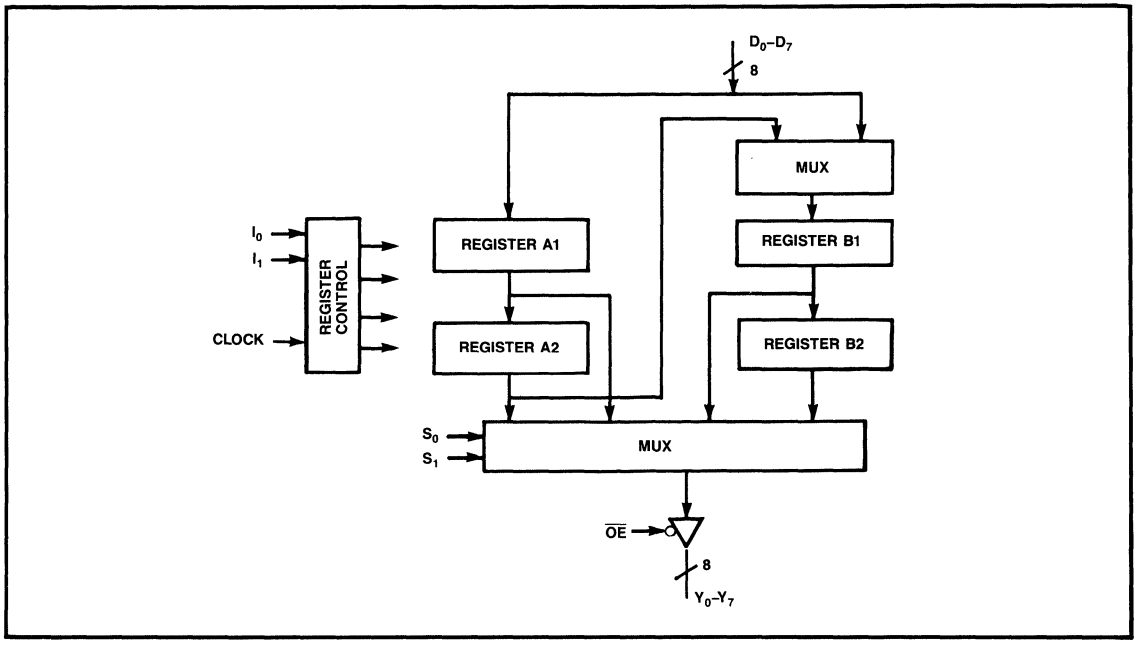
The WS59520 and WS59521 are CMOS drop-in replacements for the bipolar AM29520 and AM29521 devices offered by Advanced Micro Devices. The high performance CMOS process with which these products are manufactured enables them to operate at bipolar speeds while consuming one tenth the power of the bipolar circuits.

The WS59520/521 consists of four 8-bit registers which can be configured as a single four level pipeline or two dual level pipelines. The architectural configuration is determined by the instruction inputs (I_0 and I_1).

Each of the four registers contents is available at the multiplexed output. The register to be used as the output register is determined by the control inputs (S_0 and S_1). The output is 8-bits wide and is enabled by the $\overline{OE}$ input.

The WS59520 and WS59521 differ only in the dual two level stack mode of operation.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

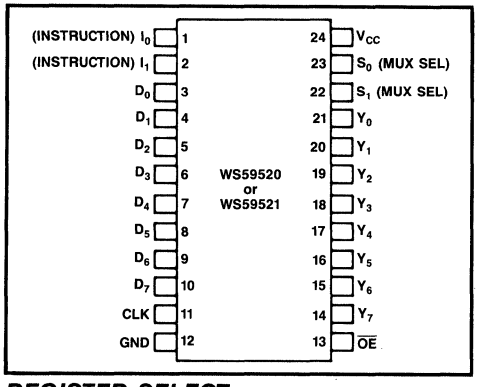
Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... −55°C to +125°C
Storage Temp. (No bias) .... −65°C to +150°C
Voltage on any pin with
respect to GND ..... −0.6V to +7V
Latch Up Protection .....>200 mA
ESD Protection ..... > ±2000V

* **Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may effect device reliability.

PIN DESCRIPTION

SIGNAL NAME	I/O	DESCRIPTION
D_0–D_7	I	Data input port
Y_0–Y_7	0	Data output port
CLK	I	Data Latches on Low-to-High Transition
I_0–I_1	I	Instruction inputs. Refer to Instruction Control Tables.
S_0, S_1	I	Selects one of four registers to be read at the output port.
$\overline{OE}$	I	Active Low, output enable. A high signal disables the output port.

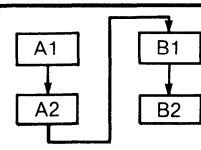
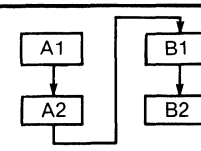
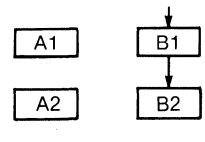
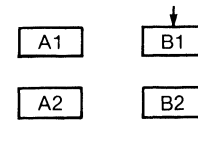
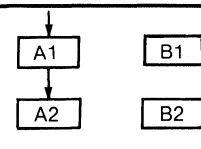
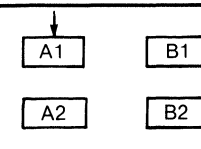
PIN CONFIGURATION



REGISTER SELECT

S1	S0	WS59520 or WS59521
0	0	B2
0	1	B1
1	0	A2
1	1	A1

INSTRUCTION CONTROL

I1	I0	WS59520	WS59521
0	0		
0	1		
1	0		
1	1	ALL REGISTERS HOLD	ALL REGISTERS HOLD

DC CHARACTERISTICS Over Operating Range (See Notes)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{oh}	Output High Voltage	V_{CC} = Min. V_{in} = V_{ih} or V_{il}	I_{oh} = −6.5mA	2.4		V
V_{ol}	Output Low Voltage	V_{CC} = Min. V_{in} = V_{ih} or V_{il}	I_{OL} = 20 mA Comm'l		0.5	V
			I_{OL} = 16 mA Mil			
V_{ih}	Input High Voltage	Guaranteed Input High Voltage		2.0		V
V_{il}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	V
I_{ix}	Input Load Current	V_{CC} = Max, V_{in} = Gnd or V_{CC}		−10	10	µA
I_{oz}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}		−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	Comm'l (0° + 70°C)		12	mA
			Mil (−55° to +125°C)		15	mA

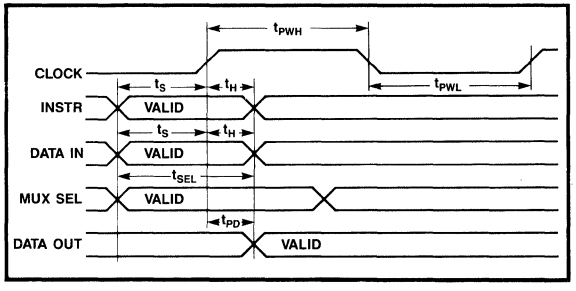
NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.
3) C_L = 50 pF except for t_{DF} where C_L = 5 pF.

4

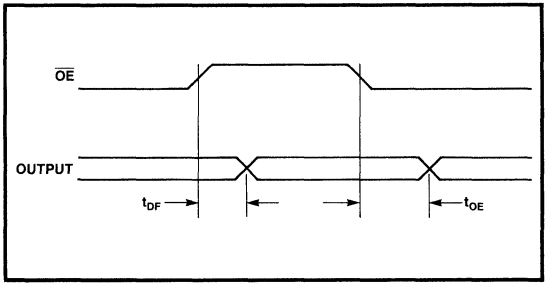
SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

		WS59520/WS59521				
		COMMERCIAL		MILITARY		
PARAMETER	DESCRIPTION	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Clock to Data Out		22		24	ns
t_{SEL}	Mux Select to Data Out		20		22	ns
t_S	Input (Data/Instr.) Set Up	10		10		ns
t_H	Input (Data/Instr.)Hold	3		3		ns
t_{DF}	Output Disable		15		16	ns
t_{OE}	Output Enable		21		22	ns
t_{PWH}	Clock Pulse Width High	10		10		ns
t_{PWL}	Clock Pulse Width Low	10		10		ns

TIMING DIAGRAM



OUTPUT TIMING DIAGRAM



Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59520S	22	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS59520T	22	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS59520TMB	24	24 Pin CERDIP, 0.3″	K1	Military	MIL-STD-883C
WS59521S	22	24 Pin Plastic DIP, 0.3″	S1	Comm'l	Standard
WS59521T	22	24 Pin CERDIP, 0.3″	K1	Comm'l	Standard
WS59521TMB	24	24 Pin CERDIP, 0.3″	K1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

BI-DIRECTIONAL BUS INTERFACE REGISTERS

KEY FEATURES

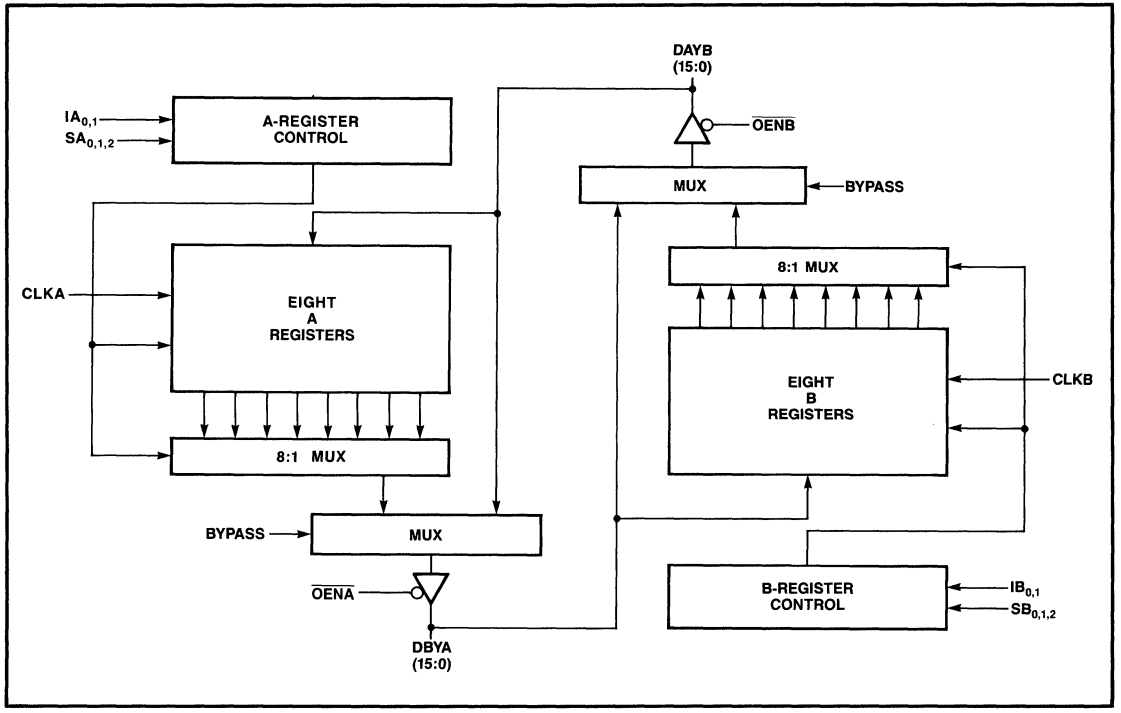
- **Two Banks of 8 x 16 Registers**
- **Contents of Each Register Available at Output**
- **Provides Temporary Address or Data Storage Between Two Processor Ports or Buses**
- **Bi-Directional Buses Interface — Dual 4-Deep or 8-Deep Registers in Each Direction**
- **Separate Control for Each Register Bank**
- **Direct Processor Bus-to-Bus Interface**
- **TTL Compatible**
- **Replaces Eight WS59520's**

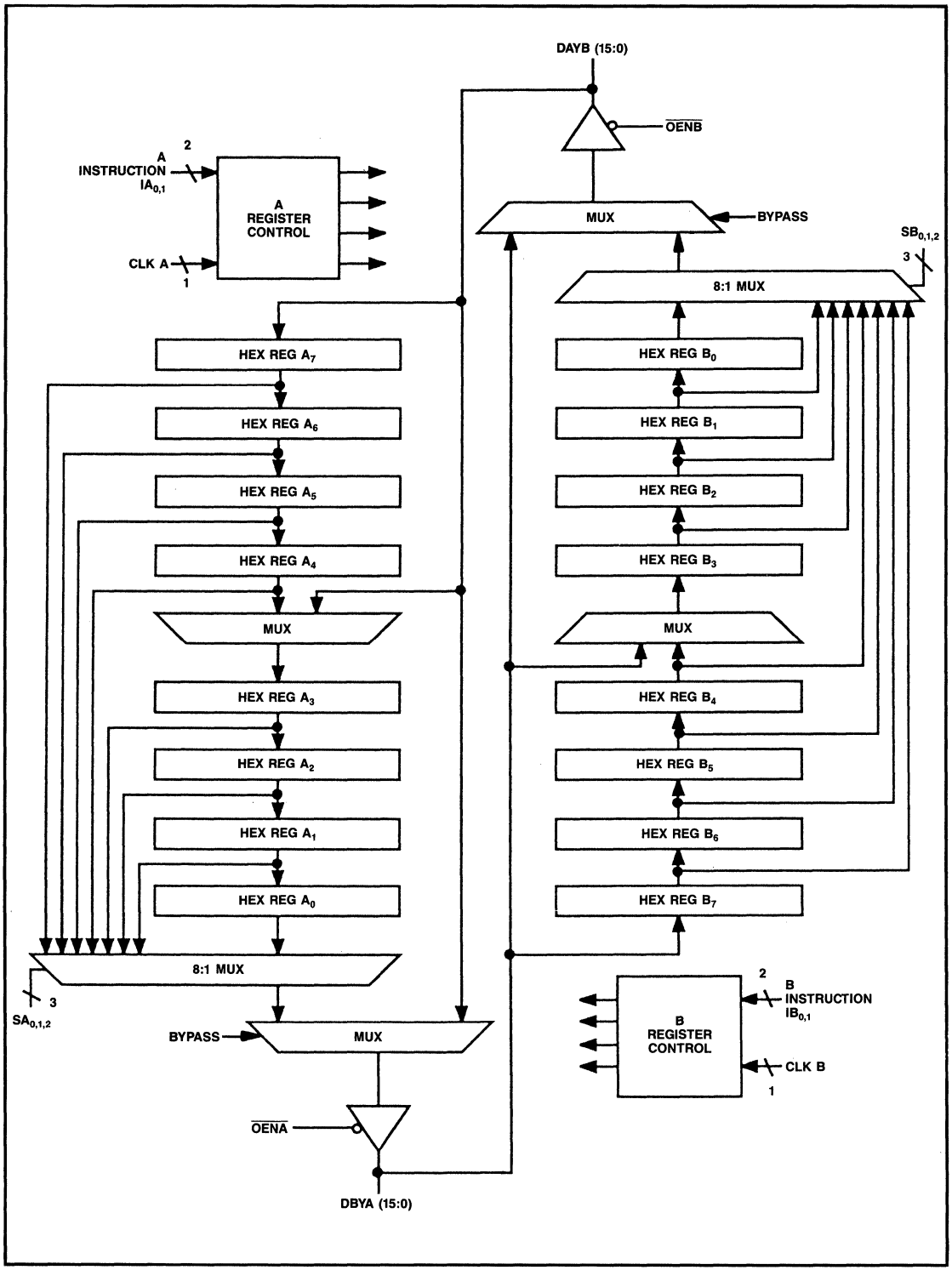
GENERAL DESCRIPTION

The WS59820 consists of two banks of registers, eight registers in each bank, each register 16 bits wide. A single bank can be configured as an eight level pipeline or two each four level pipelines. The architectural configuration is determined by the instruction inputs (I0 and I1) for each register bank.

Each of the eight registers in each bank is available at the multiplex output. The output register is determined by the control inputs (S0, S1, and S2) for each register bank. The multiplexed ouput is 16 bits wide and is enabled by the -OEN signal. Each bank of registers has its own clock (CLK), instruction inputs (I0-1) and multiplex controls.

BLOCK DIAGRAM



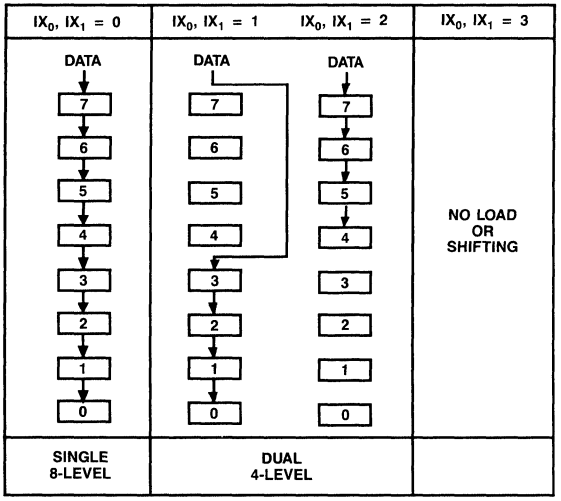

DAYB (15:0)
OENB
2
A
INSTRUCTION
IA0,1
A
REGISTER
CONTROL
CLK A
1
MUX
BYPASS
SB0,1,2
3
8:1 MUX
HEX REG A7
HEX REG A6
HEX REG A5
HEX REG A4
MUX
HEX REG A3
HEX REG A2
HEX REG A1
HEX REG A0
8:1 MUX
3
SA0,1,2
BYPASS
MUX
OENA
DBYA (15:0)
HEX REG B0
HEX REG B1
HEX REG B2
HEX REG B3
MUX
HEX REG B4
HEX REG B5
HEX REG B6
HEX REG B7
2
B
INSTRUCTION
IB0,1
B
REGISTER
CONTROL
CLK B
1

SELECTION TABLE FOR REGISTER A OR B

SX2	SX1	SX0	REGISTER SELECTED
0	0	0	REG 0
0	0	1	REG 1
0	1	0	REG 2
0	1	1	REG 3
1	0	0	REG 4
1	0	1	REG 5
1	1	0	REG 6
1	1	1	REG 7

X = Register A or B.

REGISTER SHIFT OPTIONS FOR REGISTERS A OR B



X = Register A or B.

MULTIPLEX CONTROL

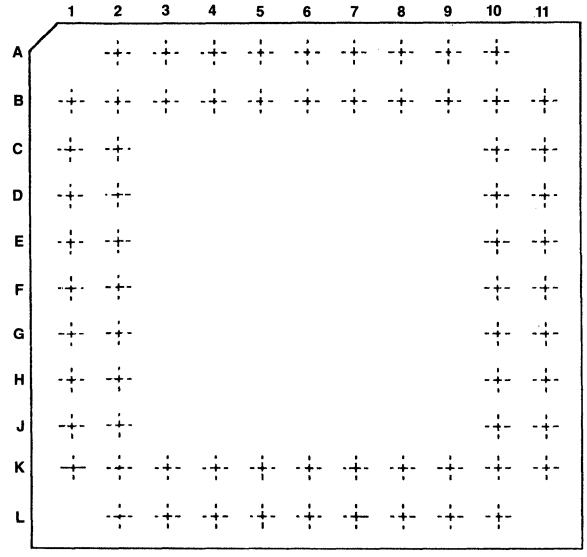
$\overline{OENA}$	$\overline{OENB}$	BYPASS	OPERATION
0	0	1	Pass Output of 8:1 Muxes to Outputs
0	0	0	Not Allowed (Input is Preferred)
0	1	0	Pass Input From DAYB (15:0) to Output DBYA (15:0)
0	1	1	Pass Output From 8:1 Mux to Outputs DBYA (15:0)
1	0	0	Pass Input From DBYA (15:0) to Output DAYB (15:0)
1	0	1	Pass Output From 8:1 Mux to Outputs DAYB (15:0)
1	1	X	Inhibit Outputs (High Impedance)

PIN DESCRIPTION

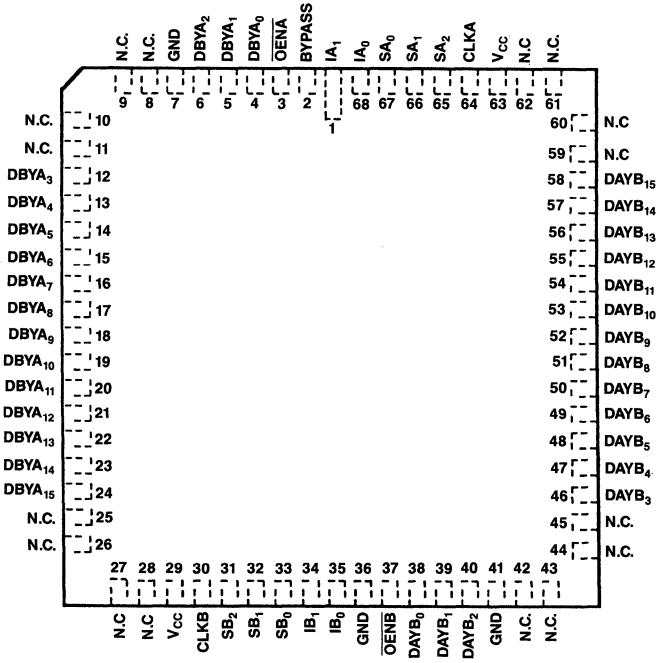
SIGNAL NAME	I/O	DESCRIPTION
IA_0, IA_1	I	Instruction Inputs for Register Bank A
IB_0, IB_1	I	Instruction Inputs for Register Bank B
SA_0-SA_2	I	Multiplex Select for Register Bank A
SB_0-SB_2	I	Multiplex Select for Register Bank B
$\overline{OENA}$	I	Output Enable for Output Port DBYA
$\overline{OENB}$	I	Output Enable for Output Port DAYB
CLKA	I	Clock Input for Register Bank A
CLKB	I	Clock Input for Register Bank B
DBYA 15:0	I/O	Register Bank B Input Port, Register Bank A Output Port
DAYB 15:0	I/O	Register Bank A Input Port, Register Bank B Output Port
BYPASS	I	BYPASS Control (Active Low). See Table on Output Control

PACKAGE ORIENTATION

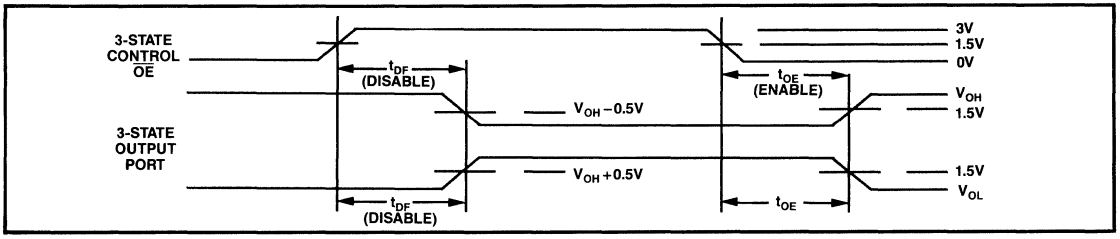
68 PIN CPGA
(Top Through Package View)



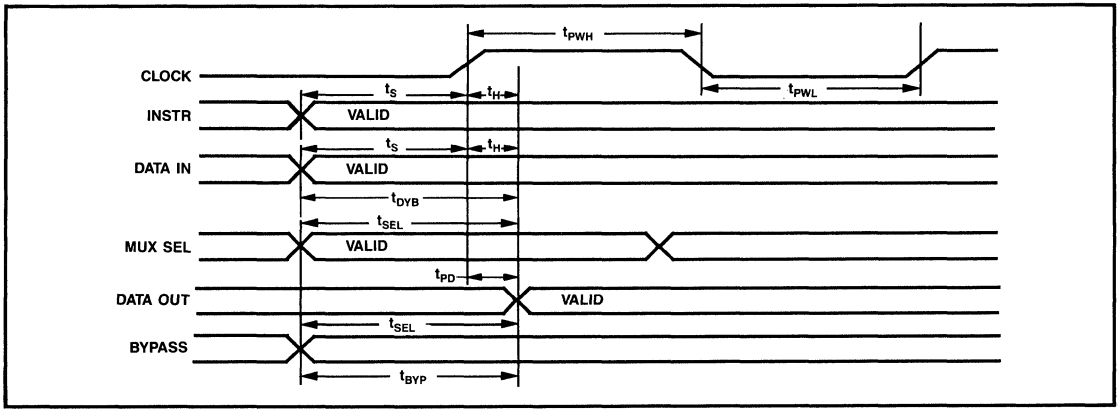
68 PIN PLDCC
(Top Through Package View)



WS59820 THREE STATE TIMING



WS59820 TIMING DIAGRAM



68 PIN CPGA PIN DESIGNATOR

PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME	PIN NAME	SIGNAL NAME
A_6	IA_1	B_6	BYPASS	A_5	$\overline{OENA}$	B_5	$DBYA_0$
A_4	$DBYA_1$	B_4	$DBYA_2$	A_3	GND	B_3	Not Used
A_2	Not Used	B_1	Not Used	B_2	Not Used	C_1	$DBYA_3$
C_2	$DBYA_4$	D_1	$DBYA_5$	D_2	$DBYA_6$	E_1	$DBYA_7$
E_2	$DBYA_8$	F_1	$DBYA_9$	F_2	$DBYA_{10}$	G_1	$DBYA_{11}$
G_2	$DBYA_{12}$	H_1	$DBYA_{13}$	H_2	$DBYA_{14}$	J_1	$DBYA_{15}$
J_2	Not Used	K_1	Not Used	L_2	Not Used	K_2	Not Used
L_3	V_{CC}	K_3	CLKB	L_4	SB_2	K_4	SB_1
L_5	SB_0	K_5	IB_1	L_6	IB_0	K_6	GND
L_7	$\overline{OENB}$	K_7	$DAYB_0$	L_8	$DAYB_1$	K_8	$DAYB_2$
L_9	GND	K_9	Not Used	L_{10}	Not Used	K_{11}	Not Used
K_{10}	Not Used	J_{11}	$DAYB_3$	J_{10}	$DAYB_4$	H_{11}	$DAYB_5$
H_{10}	$DAYB_6$	G_{11}	$DAYB_7$	G_{10}	$DAYB_8$	F_{11}	$DAYB_9$
F_{10}	$DAYB_{10}$	E_{11}	$DAYB_{11}$	E_{10}	$DAYB_{12}$	D_{11}	$DAYB_{13}$
D_{10}	$DAYB_{14}$	C_{11}	$DAYB_{15}$	C_{10}	Not Used	B_{11}	Not Used
A_{10}	Not Used	B_{10}	Not Used	A_9	V_{CC}	B_9	CLKA
A_8	SA_2	B_8	SA_1	A_7	SA_0	B_7	IA_0

ABSOLUTE MAXIMUM RATINGS*

Operating Temp. (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on any pin with
respect to GND . . . . . −0.6V to +7V
Latch Up Protection . . . . . > 200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS Over Operating Range (See Notes)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6.5 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA Comm'l I_{OL} = 16 mA Mil		0.5	V
V_{IH}	Input High Voltage	Guaranteed Input High Voltage		2.0		V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	V
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = GND or V_{CC}		−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = GND or V_{CC}		−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	0°C to +70°C (Comm'l)		12	mA
			−55°C to +125°C (Mil)		15	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.
3) C_L = 50 pF except for t_{DF} where C_L = 5 pF.

SWITCHING CHARACTERISTICS Over Operating Range (See Notes)

PARAMETER	DESCRIPTION	WS59820				UNITS
		COMMERCIAL		MILITARY		
		MIN	MAX	MIN	MAX	
t_{PD}	Clock to Data Out		23		25	ns
t_{SEL}	Mux Select to Data Out		20		22	ns
t_S	Input (Data/Instr.) Set Up	6		6		ns
t_H	Input (Data/Instr.) Hold	5		5		ns
t_{DF}	Output Disable	15			16	ns
t_{OE}	Output Enable	18			22	ns
t_{PWH}	Clock Pulse Width High	10		12		ns
t_{PWL}	Clock Pulse Width Low	11		12		ns
t_{BYP}	Bypass to Data Out		17		20	ns
t_{DYB}	Data Via BYPASS (Data In to Data Out When BYPASS is Active Low)		13		16	ns

NOTE: Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59820J	23	68 Pin PLDCC	J1	Comm'l	Standard
WS59820G	23	68 Pin Ceramic PGA	G1	Comm'l	Standard
WS59820GMB	25	68 Pin Ceramic PGA	G1	Military	MIL-STD-883C

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

Waferscale Integration, Inc. (WSI) is committed to supplying products that meet the demands of the Military/Hi-Reliability marketplace. WSI's very high performance CMOS EPROM (with its patented Split-Gate design) and Logic technology offers an intrinsic reliability that, when coupled with Military screening and testing, produces an extremely enhanced and reliable product. All WSI products can be procured fully compliant to Paragraph 1.2.1 of MIL-STD-883C.

The WSI Quality Assurance Program has been designed and implemented to perpetuate and maintain the high standards needed to repeatedly produce these products. The cohesiveness of the Program is accomplished through a comprehensive Document Control system that assures the repeatability of the process.

State-of-the-art equipment and techniques are being used extensively throughout Design, Wafer Fabrication, Assembly, Screening and Testing (Method 5004), and Quality Conformance Inspections (Method 5005) to produce the highest yields possible with their associated reliability enhancement.

The tables below describe the program in detail. Worthy of notation is the fact that WSI UV EPROMs are subjected to two 100% data retention tests: one in wafer form (48 hours at 200°C) and the other in finished package form (72 hours at 140°C). The wafer data retention test, with its high activation temperature, assures data retention problems are reduced and virtually eliminated.

TABLE I. 100% SCREENING TO METHOD 5004

All product is subjected to the following 100% screening flow. Screening test methods are in accordance with MIL-STD-883, Method 5004. (Latest issues in effect.)

SCREEN	TEST METHOD/CONDITION	QUALITY LEVEL
Data Retention (EPROMs Only)	48 Hours at 200°C	100%
Visual and Mechanical	**5004**	
Internal Visual	2010/Condition B	100%
High-Temperature Storage	1008/Condition C	100%
Temperature Cycle	1010/Condition C	100%
Constant Acceleration	2001/Condition D or E (Y_1 Axis)	100%
Hermeticity	1014	
Fine	Condition A or B	100%
Gross	Condition C	100%
External Visual	2009	100%
Data Retention (EPROMs Only)	72 Hours at 140°C	100%
Burn-In	**5004**	
Pre-Burn-In Electrical	Per Applicable WSI Device Specifications or Military Drawing. T_A = +25°C.	100%
Burn-In	1015/Condition D, T_A = +125°C Minimum	100%
Final Electrical Tests (See Note 1)	**5004**	
Static (DC)	a) T_A = +25°C, +125°C, and −55°C	100%
Functional	b) Power Supply Extremes	100%
Switching (AC)		
Percent Defective Allowable (PDA)	**5004** Paragraph 3.5.1	5%
Quality Conformance Inspection	**5005**	
Sample Selection	See Tables II Through V	Sample
External Visual	2009	**100%**

NOTE: 1. Per applicable WSI device specification or Military Drawing.

TABLE II. GROUP A QUALITY CONFORMANCE INSPECTION

Group A Inspection is performed on each inspection lot per MIL-STD-883, Method 5005, Table I.

TEST (SEE NOTE 1)	LTPD	MAXIMUM	
		SAMPLE SIZE	ACCEPT NUMBER
Subgroup 1 Static Tests at T_A = +25°C	2	266	2
Subgroup 2 Static Tests at Maximum Rated Operating Temperature	3	176	2
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	5	105	2
Subgroup 4 (See Note 2) Dynamic Tests at T_A = +25°C	2	266	2
Subgroup 5 (See Note 2) Dynamic Tests at Maximum Rated Operating Temperature	3	176	2
Subgroup 6 (See Note 2) Dynamic Tests at Minimum Rated Operating Temperature	5	105	2
Subgroup 7 Functional Tests at T_A = +25°C	2	266	2
Subgroup 8 Functional Tests at Maximum and Minimum Rated Operating Temperatures	5	105	2
Subgroup 9 Switching Tests at T_A = +25°C	2	266	2
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature	3	176	2
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature	5	105	2

NOTES: 1. Per applicable WSI device specification or Military Drawing. 2. Subgroups 4, 5, and 6 are not applicable to WSI products.

TABLE III. GROUP B QUALITY CONFORMANCE INSPECTION

Group B quality conformance tests are performed on each inspection lot in accordance with MIL-STD-883, Method 5005, Table IIb.

TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 1 Physical Dimensions	2016	Per WSI Outline Drawing and Appendix C of MIL-M-38510	2 Devices (No Failures)
Subgroup 2 Resistance to Solvents	2015	4 Chemical Solutions	4 Devices (No Failures)
Subgroup 3 Solderability	2003	Soldering Temperature of +245°C ± 5°C	LTPD 10/Accept = 2 38 Leads From 3 Devices Minimum
Subgroup 4 Internal Visual and Mechanical	2014	Failure Criteria Based on Design and Construction Requirements of WSI Specification	1 Device (No Failures)

(Table III Continued on Next Page.)

TABLE III. GROUP B QUALITY CONFORMANCE INSPECTION (Cont.)

Group B quality conformance tests are performed on each inspection lot in accordance with MIL-STD-883, Method 5005, Table IIb.

TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 5 Bond Strength Ultrasonic or Wedge	2011	Condition C or D	LTPD 15/Accept = 1 34 Bonds From 4 Devices Minimum
Subgroup 6 Internal Water Vapor Content	1018	This Test is Not Performed by WSI. WSI Packages Do Not Contain Dessicants.	3 Devices, 0 Failures or 5 Devices, 1 Failure
Subgroup 7 Seal Fine Gross	1014	 Condition A or B Condition C	LTPD 5/Accept = 2
Subgroup 8 Electrostatic Discharge Sensitivity Classification	3015	Unless Otherwise Specified, This Test Will be Performed for Initial Qualification of New Product or Redesign.	LTPD 15/Accept = 0

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TABLE IV. GROUP C QUALITY CONFORMANCE INSPECTION

Group C quality conformance tests are performed on inspection lots every 52 weeks in accordance with MIL-STD-883, Method 5005, Table III.

TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 1 Steady-State Life Test End-Point Electrical	1005	Condition D, 1000 Hours at T_A = 125°C or Equivalent Per WSI Specification or Military Drawing	LTPD 5/Accept = 2
Subgroup 2 Temperature Cycling Constant Acceleration Hermeticity Fine Gross Visual Examination End-Point Electrical Parameters	 1010 2001 1014 1010 or 1011 	 Condition C Condition D or E Condition A or B Condition C Per WSI Specification or Military Drawing	 LTPD 15/Accept = 2

TABLE V. GROUP D QUALITY CONFORMANCE INSPECTION

Group D quality conformance tests are performed on inspection lots every 52 weeks in accordance with MIL-STD-883, Method 5005, Table IV.

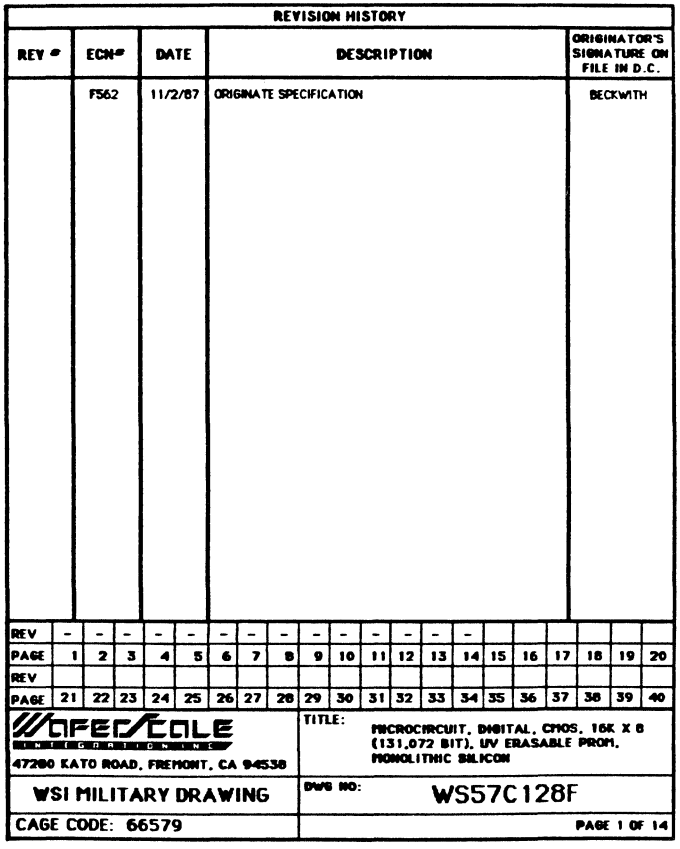
TEST	TEST METHOD	TEST CONDITIONS	QUALITY LEVEL/ MAXIMUM ACCEPT NUMBER
Subgroup 1			
Physical Dimensions	2016	Per WSI Outline Drawing and Appendix C of MIL-M-38510	LTPD 15/Accept = 2
Subgroup 2			
Lead Integrity	2004 or 2028	Test Condition B2 (Lead Fatigue) or D	LTPD 15/Accept = 2
Hermeticity, Fine and Gross	1014	Condition A or B and C	
Subgroup 3			
Thermal Shock	1011	Condition B Minimum	
Temperature Cycling	1010	Condition C Minimum	
Moisture Resistance	1004		LTPD 15/Accept = 2
Hermeticity, Fine and Gross	1014	Condition A or B and C	
Visual Examination	1004, 1010		
End-Point Electrical Parameters		Per WSI Specification or Military Drawing	
Subgroup 4			
Mechanical Shock	2002	Condition B Minimum	
Vibration, Variable Frequency	2007	Condition A Minimum	
Constant Acceleration	2001	Condition D or E	LTPD 15/Accept = 2
Hermeticity, Fine and Gross	1014	Condition A or B and C	
Visual Examination	2009		
End-Point Electrical Parameters		Per WSI Specification or Military Drawing	
Subgroup 5			
Salt Atmosphere	1009	Condition A Minimum	
Hermeticity, Fine and Gross	1014	Condition A or B and C	LTPD 15/Accept = 2
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor	1018	5,000 ppm Maximum Water Content at 100°C	3 Devices, 0 Failures or 5 Devices, 1 Failure
Subgroup 7			
Adhesion of Lead Finish	2025		LTPD 15/Accept = 2
Subgroup 8			
Lid Torque	2024	As Applicable to Glass-Frit Packages	LTPD 15/Accept = 0

WSI supports the Standardized Military Drawings (SMD) program sponsored by DESC (Defense Electronics Supply Center) and has submitted Certificates of Compliance for the following products:

MILITARY DRAWING NO.	WSI PART NO.	ESTIMATED DESC PUBLICATION DATE
85102	WS27C64F	Late Q1, 1988
5962-87661	WS27C128F	Available Now
5962-87063	WS27C256F	Late Q1, 1988
5962-87515	WS57C49 and WS57C49B	Late Q1, 1988
5962-87650	WS57C191 and WS57C291	Available Now

NOTE: Compliant MIL-STD-883C products are marked with the letter "C" preceding the date code.

When Military Drawings are not available for new, state-of-the-art products offered by WSI, WSI makes available its own version of a Military Drawing composed and formatted like a DESC SMD for ease of recognition. A sample of a WSI Military Drawing is depicted below. These can be obtained from a WSI sales office or authorized representative.



REVISION HISTORY

REV #	ECN#	DATE	DESCRIPTION	ORIGINATOR'S SIGNATURE ON FILE IN D.C.
	F562	11/2/87	ORIGINATE SPECIFICATION	BECKWITH

REV	-	-	-	-	-	-	-	-	-	-	-	-	-	-						
PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
REV																				
PAGE	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40

WAFERSCALE INTEGRATION INC.
47280 KATO ROAD, FREMONT, CA 94538

TITLE: MICROCIRCUIT, DIGITAL, CMOS, 16K X 8 (131,072 BIT), UV ERASABLE PROM, MONOLITHIC SILICON

WSI MILITARY DRAWING

DWG NO: WS57C128F

CAGE CODE: 66579

PAGE 1 OF 14

WSI's MIL-STD-883C COMPLIANT FAST EPROMs AND RPROMs

PART NUMBER	ARCHITECTURE	TYPE	0.300" CERDIP	0.600" CERDIP	28 PIN CERAMIC CLLCC	32 PIN CERAMIC CLLCC	24 PIN CERAMIC FLATPACK	FASTEST MILITARY SPEED
WS57C191	2K x 8	RPROM		24 Pin	X			50 ns
WS57C291	2K x 8	RPROM	24 Pin		X			50 ns
WS57C43	4K x 8	RPROM		24 Pin	X			70 ns
WS57C43B	4K x 8	RPROM	24 Pin	24 Pin	X		X	45 ns
WS27C64F	8K x 8	EPROM		28 Pin		X		90 ns
WS57C49	8K x 8	RPROM		24 Pin	X		X	70 ns
WS57C49B	8K x 8	RPROM	24 Pin	24 Pin	X		X	45 ns
WS57C64F	8K x 8	EPROM		28 Pin		X		70 ns
WS27C128F	16K x 8	EPROM		28 Pin		X		90 ns
WS57C51	16K x 8	RPROM		28 Pin		X		70 ns
WS57C51B	16K x 8	RPROM		28 Pin		X		45 ns
WS57C128F	16K x 8	EPROM		28 Pin		X		70 ns
WS27C256F	32K x 8	EPROM		28 Pin		X		90 ns
WS57C256F	32K x 8	EPROM		28 Pin		X		70 ns

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

THE SHORTEST PATH FROM SYSTEM CONCEPT TO MARKET

WSI supports the needs of high-performance system designers and provides them with the edge they need to survive and grow in today's competitive marketplace. WSI has positioned its organization and product portfolio to address the most important needs concerning today's system designer:

- Quick market entry
- Higher integration
- Lower power consumption
- Higher system performance

WSI offers very high performance integrated circuit products that combine nonvolatile memory with macro logic functions that result in "board-level" replacement circuits. Whether supplied as off-the-shelf product or customized for customer needs, WSI can deliver this capability quickly. This makes WSI unique among semiconductor companies.

High-Performance EPROM Core

At the core of this capability lies WSI's high-performance CMOS EPROM technology. This technology has proliferated into families of market leading EPROMs and bipolar PROM replacement products . . . memory products that feature bytewide and wordwide architectures, speeds as fast as 35 ns, and bit densities climbing to the 1 Mbit level. These fast nonvolatile memory products are described in this catalog.

User-Configurable Product Families

WSI continues to build on its EPROM core technology. Configured as EPROM macro cells in the WSI custom cell library, this high performance nonvolatile memory capability has been combined with other large functional CMOS macro cells, fast static RAM cells, fast multipliers, and random logic blocks to produce very fast programmable off-the-shelf circuits to address the above market needs. These families of high-performance user-configurable products are programmable by the user to suit particular system requirements. These products are supported by a complete system development environment that includes software and hardware development tools for use during evaluation, program development and debug.

The first user-configurable CMOS products offered by WSI are:

- The PAC™ family of Microprogrammable Controllers
- The MAP™ family of Mappable Memory Products (described in this databook)
- The SAM™ family of Stand Alone Microsequencers

Rapid System Design

These user-configurable programmable products provide system designers with the ability to quickly try new concepts or designs. With the development tools, system designers are free to fashion new products that combine new features and increased performance within the confines of their own development laboratory. When incorporated into a system, the new WSI user-configurable products deliver high levels of integration and exceptionally high system performance.

Custom Products for Custom Needs

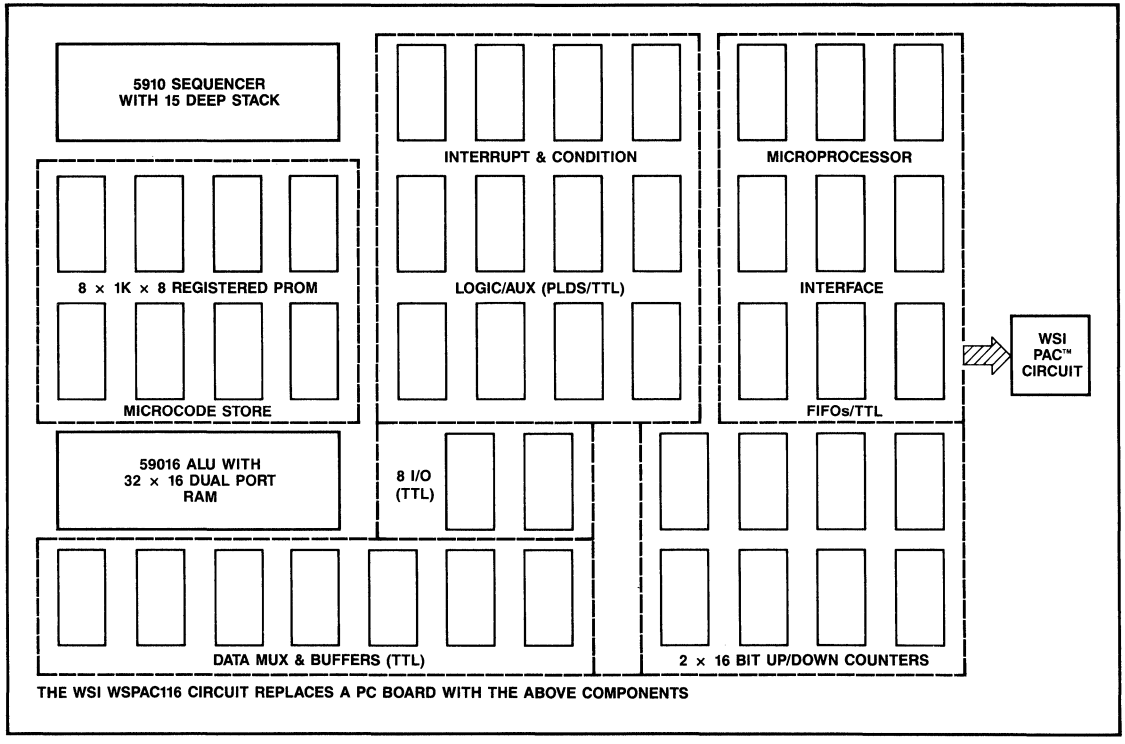
But this is not where WSI's capabilities end. For customers who have special needs, WSI will customize its standard products by modifying them to suit particular customer requirements. In addition, WSI will work with its customers to define and produce completely customized integrated circuits that take advantage of WSI's high performance memory and logic capabilities. WSI has a proprietary CAD/CAE design system and library of macrocells in place to guide its customers from the earliest system conceptual stages through prototyping and into production.

User-Configurable Product Applications

The new WSI user-configurable product families are expanding the range of choices for today's system designers who prefer to use low risk off-the-shelf products during the system prototyping and production stage. The Micro-programmable Controller PAC™ family provides high performance system solutions in a variety of applications ranging from the interface of a microprocessor to a high-speed system, fast stand-alone system controllers, high-speed graphics processors or replacement of bit-slice engines. The PAC™ family is ideal for applications such as address generation (both for instruction and data requirements), bus interface and control, fast arithmetic element controllers and DSP algorithm controllers.

THE WSPAC116 PROGRAMMABLE CONTROLLER

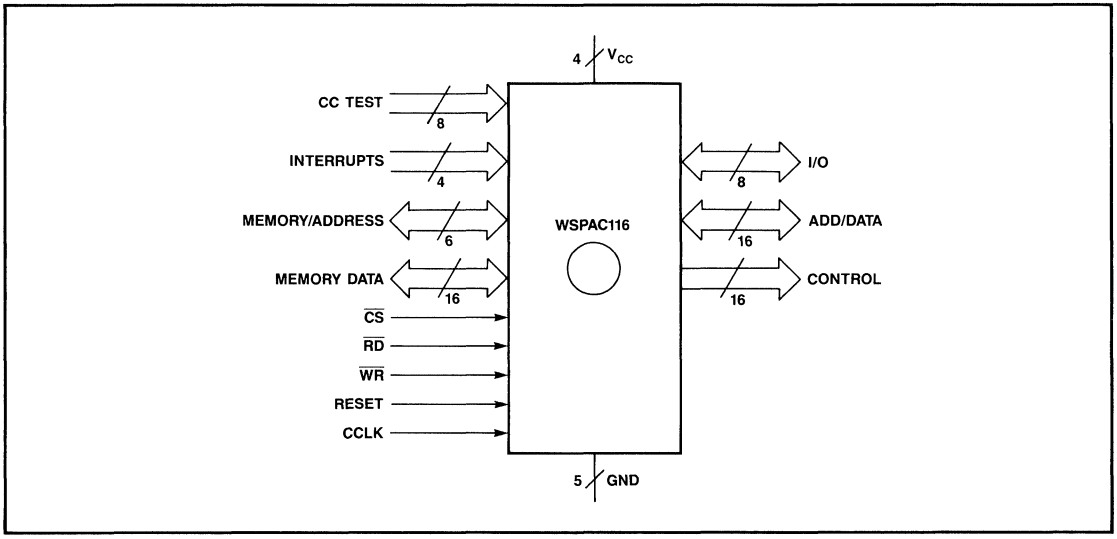
The first product in the PAC™ family is the WSPAC116, a single chip 20 MHz programmable controller that consists of a peripheral interface, 1K x 64 program store EPROM, a 16-bit instruction/data port, a 16-bit ALU, eight general purpose individually programmed I/Os, up to 4M words of addressing capability, eight high-speed program test conditions and four interrupts. The following provides information on the PAC™ controller architecture, features and capabilities. Please refer to the WSPAC116 product data sheet for detailed parameters or contact your WSI sales representative for additional information.



USER BENEFITS

- 100% faster than conventional microprocessor implementation
- 20 MHz clock operation (50 nsec cycle times)
- Military operation rated at 15 MHz (75 nsec cycle times)
- 50-to-1 PC parts count reduction
- 20x less power
- 5x lower cost

WSPAC116 CONFIGURATION

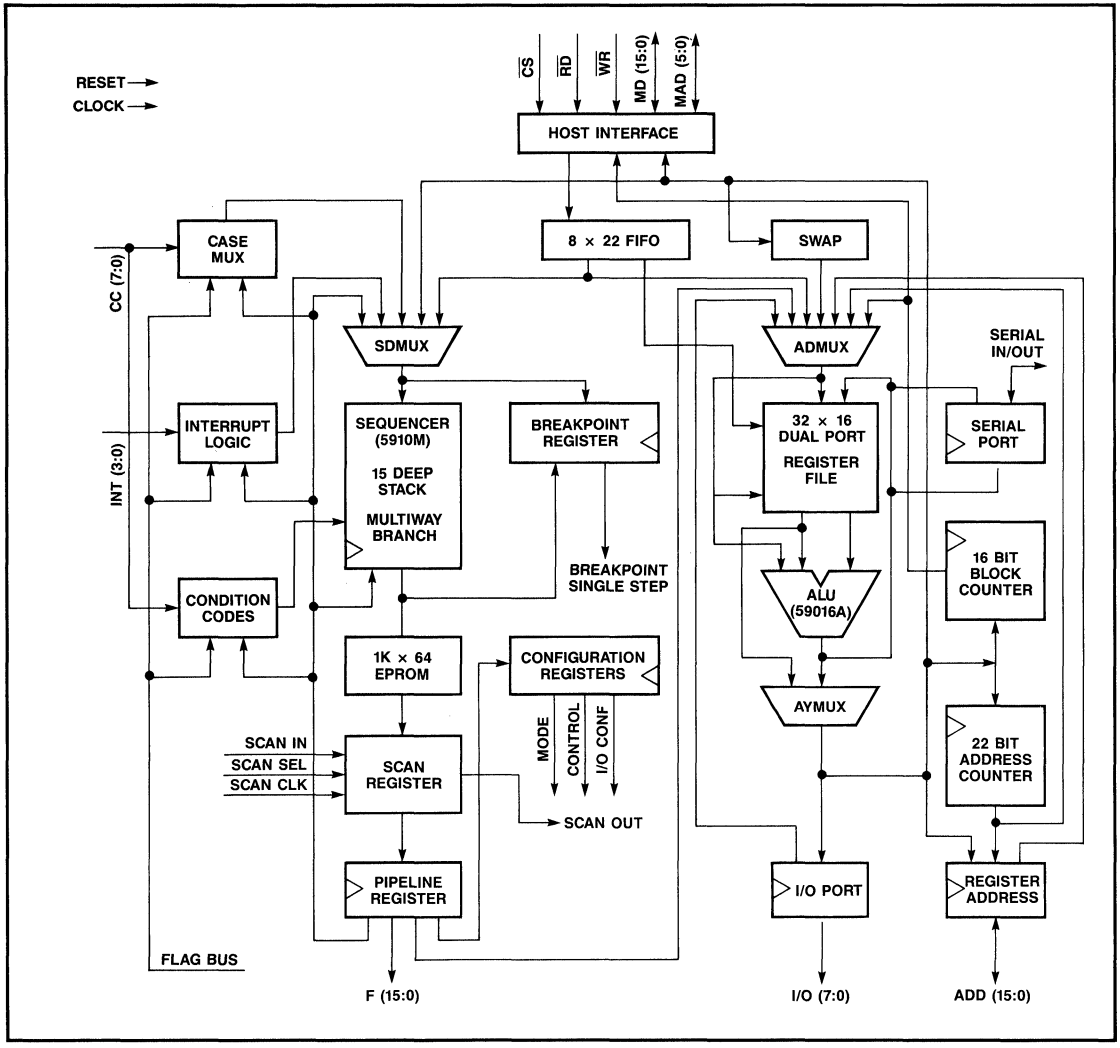


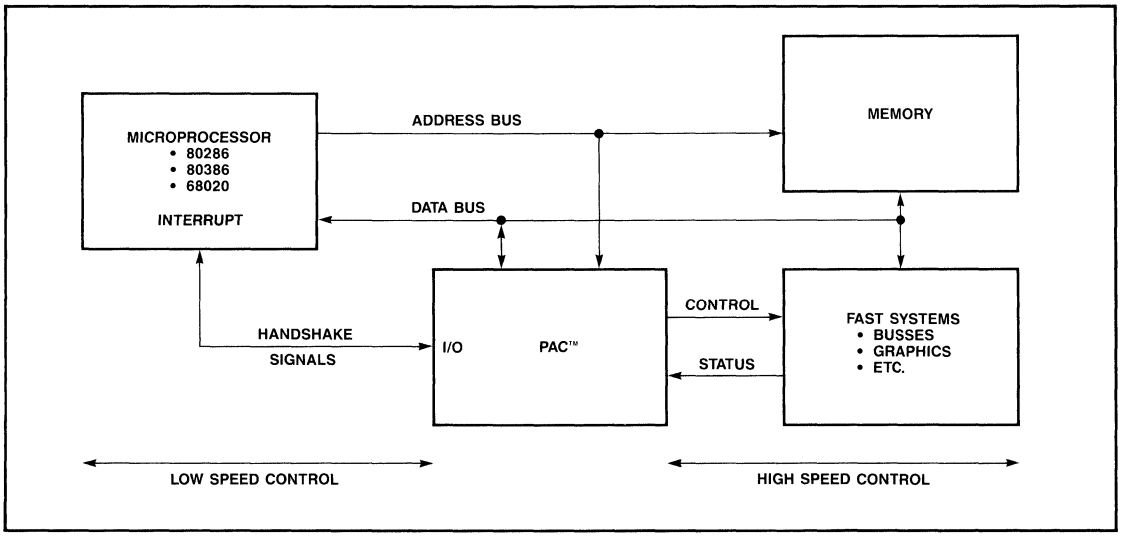
WSPAC116 FEATURES

- Dual mode of operation
  - — Stand-alone controller
  - — Microprocessor peripheral interface
    - — 16-bit microprocessor interface
    - — 8 word instruction/data queue
- Very high performance for real time control
  - — 20 MHz instruction execution rate (single instruction per cycle)
  - — 20 MHz output port and address bus
- Advanced 16-bit controller architecture
  - — 59016A 16-bit ALU
  - — 59010M 12-bit sequencer with 15 deep stack
  - — 32 x 16 register file
  - — 22-bit memory address bus
  - — Interrupt controller
- High performance reprogrammable memory
  - — 1K x 64 EPROM
- Dual I/O ports
  - — 16 real time control output lines
  - — 8 bidirectional I/O port
- High level program development tools
  - — Macro assembler with "C" like syntax
  - — Functional simulator
  - — Memory programmer
  - — Debug facilities

6

WSPAC116 FUNCTIONAL BLOCK DIAGRAM

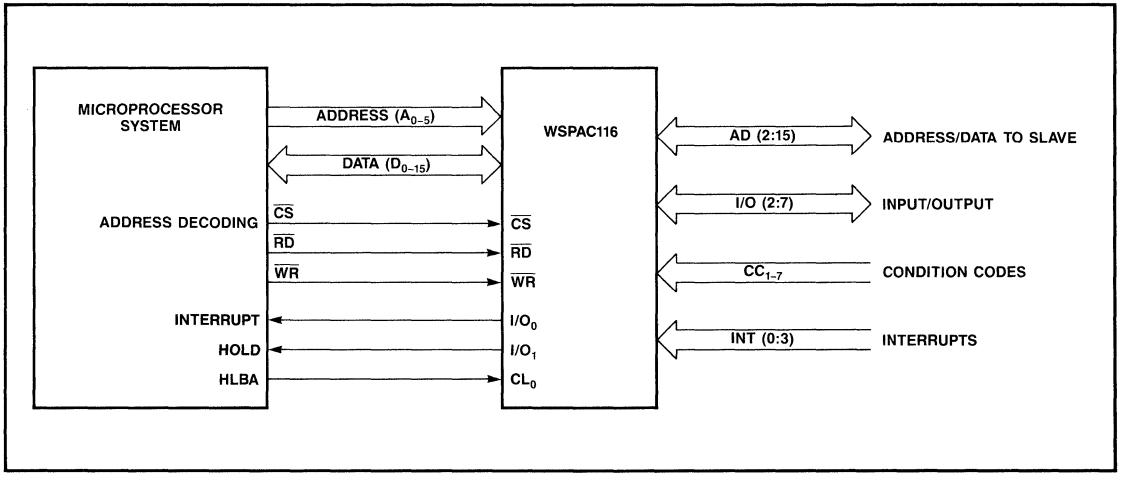




PAC™ PRODUCT DELIVERS REAL TIME, HIGH-SPEED CONTROL

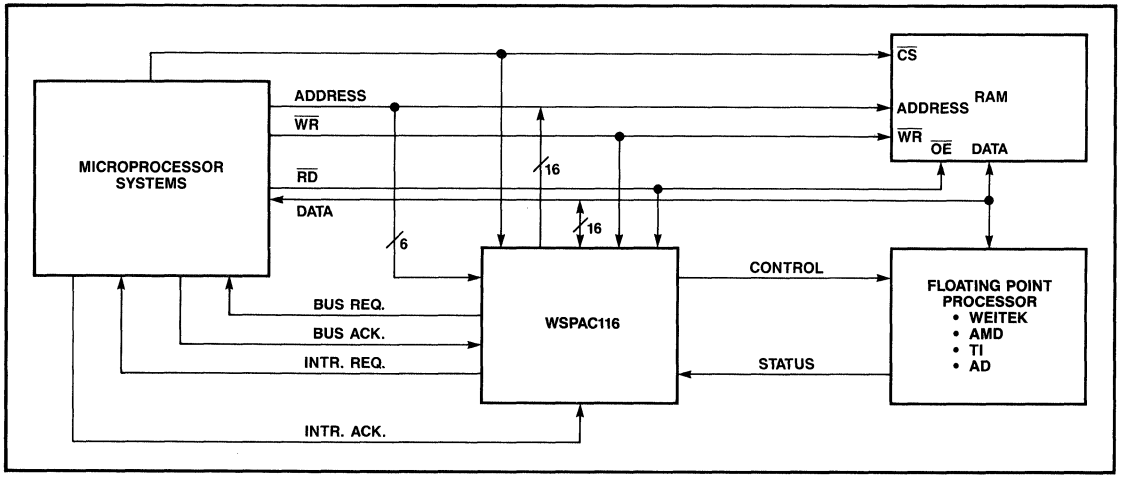
- Application program stored in the 1K x 64 on-board EPROM
- Standard peripheral interface link between host microprocessor and PAC™ product
- PAC™ product executes the application program, controls and monitors the fast system and generates addresses to memory in real time
- Handshake protocol between the host and the PAC™ circuit is done through the 8-bit I/O port

6



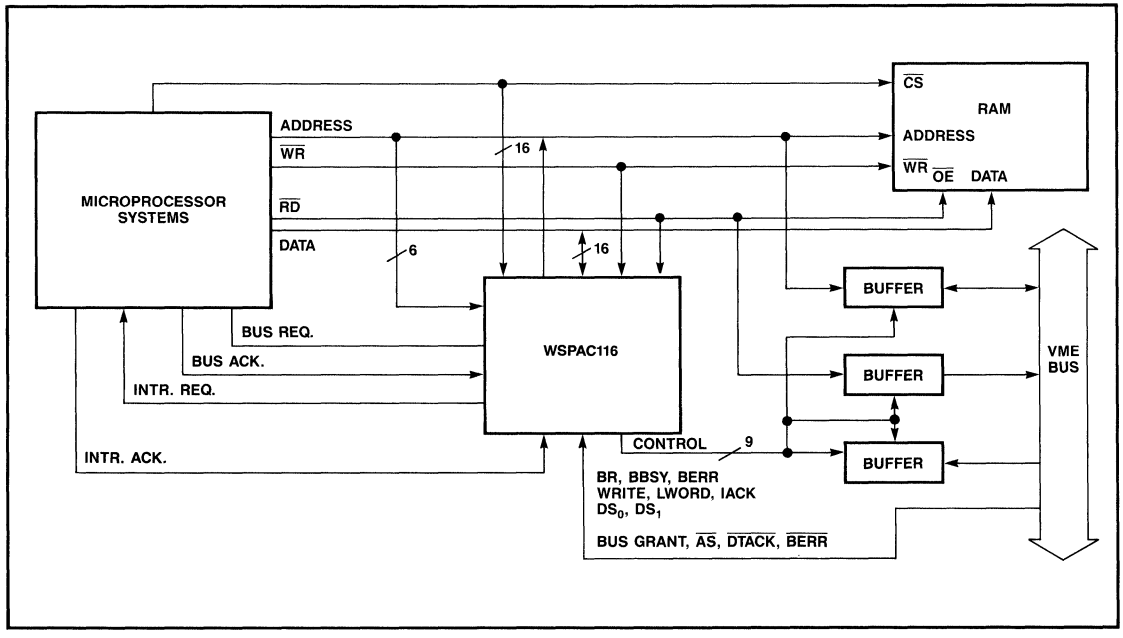
WSPAC116 PROVIDES A STRAIGHT-FORWARD BUS INTERFACE TO MICROPROCESSOR

- Simple host connections
- Interfaces like a peripheral
- 16-bit data bus for data and command transfer to WSPAC116
- 6-bit address bus for accessing internal WSPAC116 resources
- Standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ controls
- Handshake performed through I/O ports



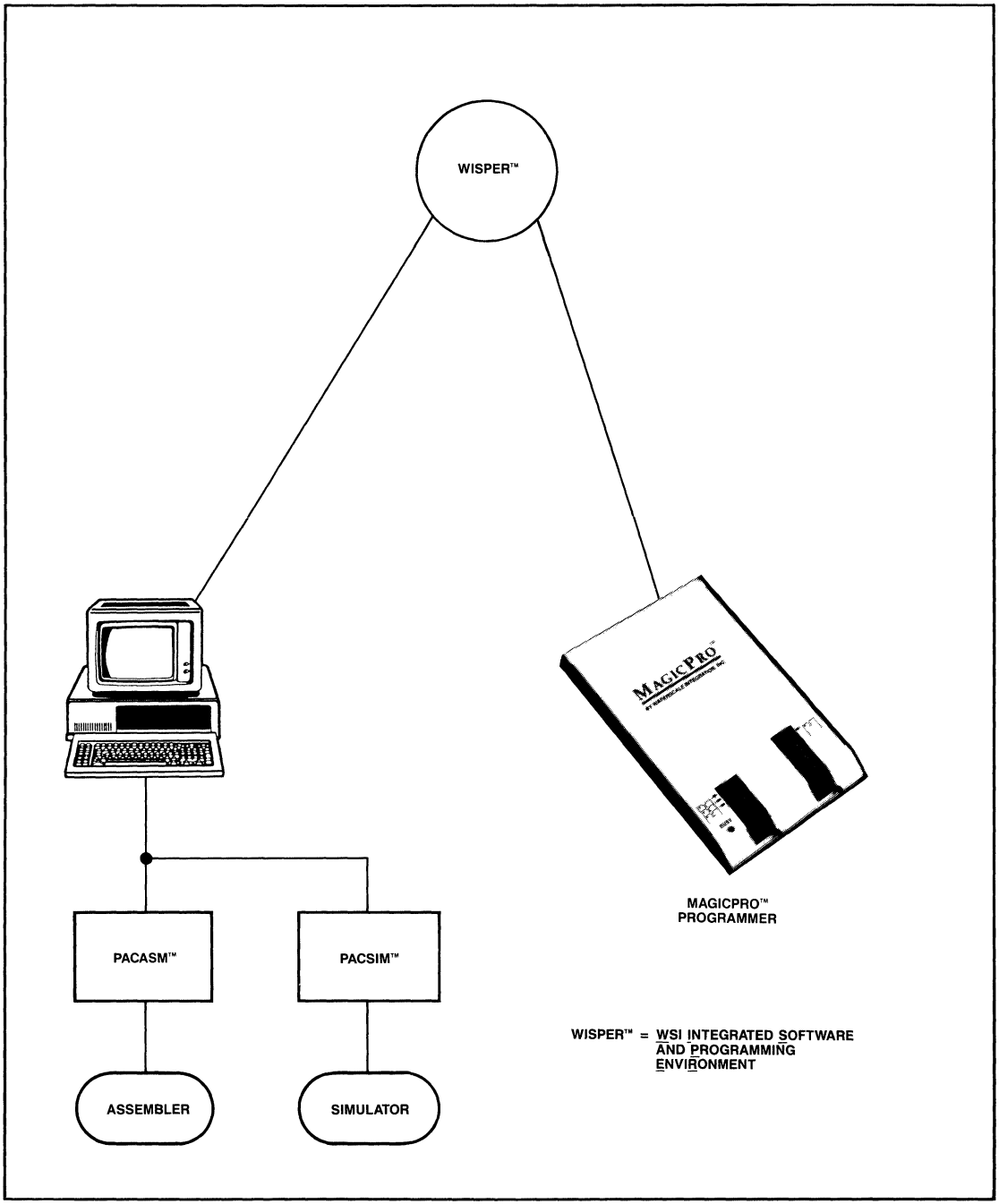
PAC™ CIRCUIT EXTENDS THE NUMBER CRUNCHING CAPABILITIES OF HIGH-SPEED FLOATING-POINT PROCESSOR SYSTEMS

- Direct floating-point unit interface from WSPAC116
- Peripheral interface to microprocessor
- Direct access to memory for data loading/storing from/to floating-point processor
- Matrix multiplication of 4 × 4 matrices with data access in 4 μsec



PAC™ INTERFACES A HOST MICROPROCESSOR TO A HIGH-SPEED BUS

- Performs bus protocol
- Data transfer to/from the microprocessor bus to/from a fast bus (like VME or Multibus)
- Transfer rate of up to 20 Mbyte/sec



PAC™ SYSTEM DEVELOPMENT TOOLS ARE USER FRIENDLY

- PACASM™ — High level program entry
- PACSIM™ — Logic simulator
- MagicPro™ — IBM PC© hardware compatible programmer

WS444/WS448 STAND-ALONE MICROSEQUENCERS (SAM™)

The third family of WSI's user-configurable products is known as STAND-ALONE MICROSEQUENCERS or SAM™s. These products are fully-integrated CMOS VLSI microsequencers designed to provide an efficient vehicle for the implementation of state machines and microcoded controllers. High performance on-chip EPROM memory (up to 448 words) is integrated with a microcode sequencer consisting of Branch Control logic, Stack and Loop Counter. Eight general-purpose inputs feed the Branch Control logic along with current state information. The Branch Control logic gives flexible multi-way microcode branch capability in a single clock, enhancing throughput beyond that of conventional controllers or sequencers. The generic microcoded architecture fits a wide range of applications spanning the spectrum from basic state machines to traditional bit-slice controller applications.

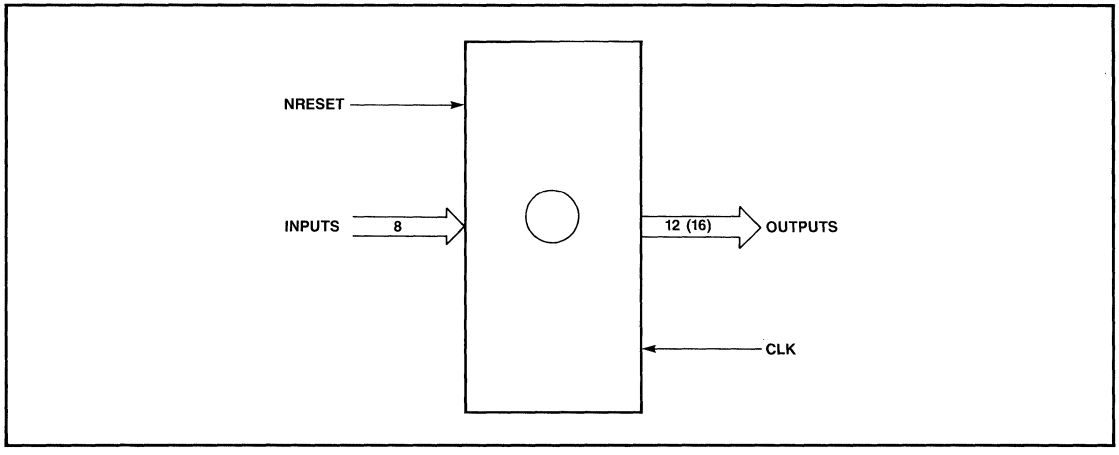
Two versions of the SAM™ architecture are initially available. The number of output pins and packaging are the key differences. The WS444 has 12 user-definable outputs, while the WS448 has 16. The SAM™ products are packaged in either DIP or JLCC/PLCC chip carrier packaging to maximize circuit board flexibility. One-Time-Programmable (OTP) plastic versions of the SAM™ products are available to minimize volume production costs.

WSI's world-class EPROM technology makes the microcode user-configurable and, in windowed packages, erasable. The products feature a combination of low CMOS power and greater than 20 MHz performance. Designing with the SAM™ products is eased through the use of WSI's MagicPro™ Programmer and SAM+PLUS™ Development Software. This software supports efficient microcode generation through high-level state machine entry and assembler microcode compilation.

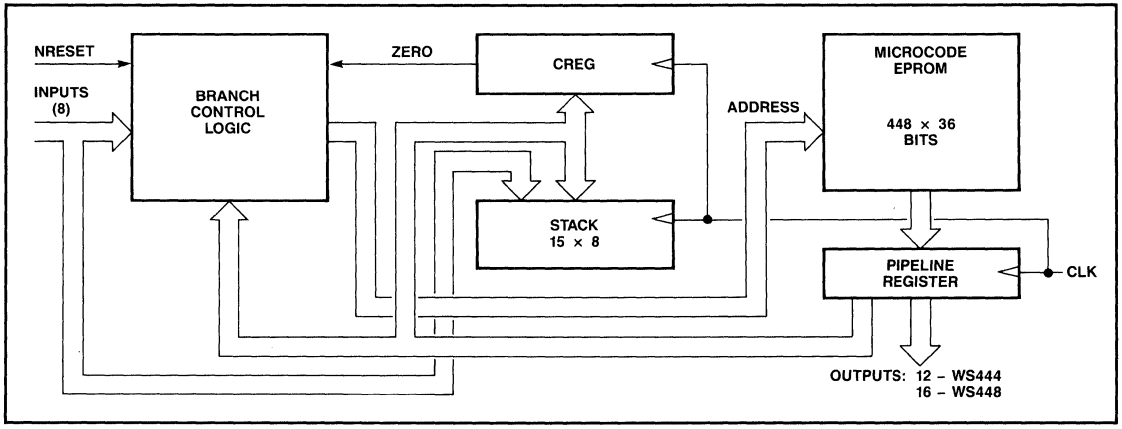
Ideal application areas for the SAM™ architecture include programmable sequencer generators, bus and memory controller functions, graphics and DSP algorithm controllers, and other complex, high performance machines.

For additional information, please refer to the WS444/WS448 product data brochures available from your WSI sales representative.

SAM™ DEVICE CONFIGURATION



WS44X SAM BLOCK DIAGRAM



SIMPLE ARCHITECTURE ENHANCES CAPABILITIES

- On-chip reprogrammable EPROM microcode memory up to 448 words deep
- 15 x 8 stack
- Loop counter
- Single clock, multi-way control branching
- 8 general-purpose branch control inputs
- 12 (WS444) or 16 (WS448) general-purpose control outputs

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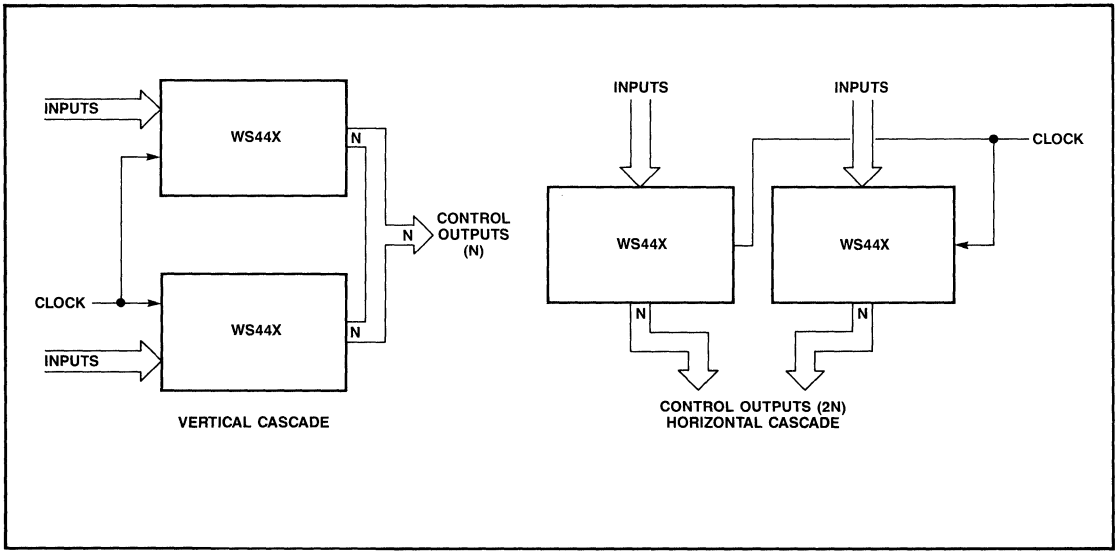
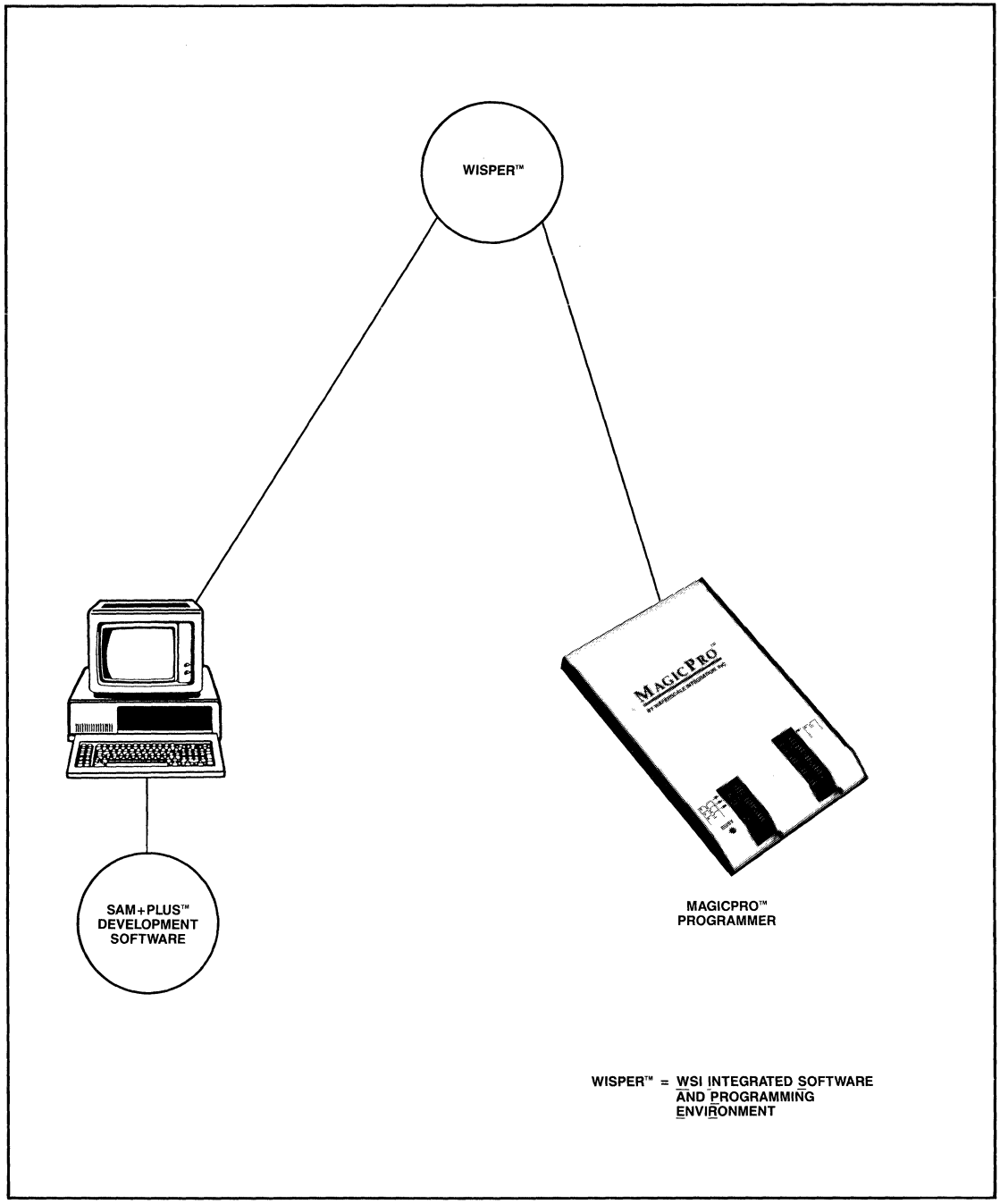
WS44X CASCADING



WSI SAM™ PRODUCT CASCADING BENEFITS

- Greater output fanout flexibility in horizontal cascaded mode
- Increased memory depth provided by vertical cascade implementation
- Cycle-by-cycle output enable control provides smooth device to device control transfer



WSI's DESIGN DEVELOPMENT SOFTWARE SIMPLIFIES DESIGN ENTRY

- Development tools supported by WSI's MagicPro™ development environment
- System supports If-Then-Else Constructs or Truth Table Entry
- Functional simulator provides simulation capabilities for the SAM™ products

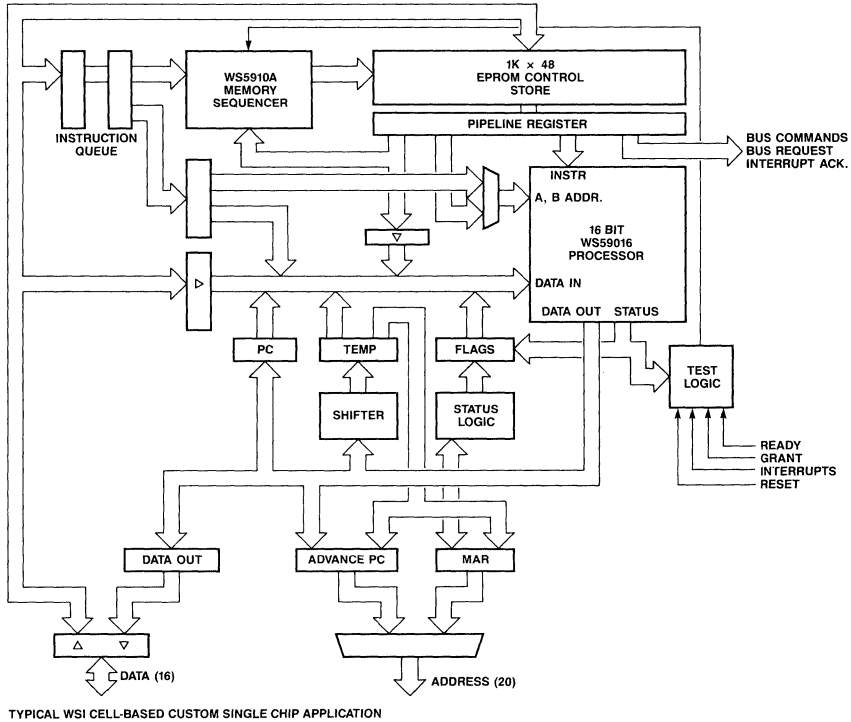
CELL-BASED CUSTOM DESIGN CAPABILITY

WSI's cell-based custom library offers the ability to modify or customize an existing standard or programmable product. Hence, when WSI's users are ready to move from the prototyping stage to full production, a path exists to accomplish the task.

The WSI cell-based custom library contains traditional SSI "glue" cells, soft macros (TTL-equivalent functions without fixed layout), and proprietary macro cells. The list of macro cells includes such functions as ALU's, sequencers, multipliers, register files, counters, FIFO's, barrel and funnel shifters, and memory arrays of ROMs, SRAMs and EPROMs.

Integration of WSI's CAD and macro cell library onto a flexible system development platform provides the user with a unique capability to quickly respond to market changes. For example, a custom cell-based design enables easy incorporation of known test patterns from other macro cell-based designs. The test patterns from the standard products can be incorporated into the larger test programs for the cell-based custom design. This provides obvious benefits:

1) Reduced test program development time
2) Expected timing values are known
3) Error-free test patterns



TYPICAL WSI CELL-BASED CUSTOM SINGLE CHIP APPLICATION

ON-CHIP EPROM DELIVERS FLEXIBILITY AND HIGH PERFORMANCE

- User-configurable functions
- Security protection bits available
- WSI on-chip EPROM insures high system performance
- On-board macro-elements enable system speeds as fast as 50 nsec per instruction
- Minimizes PC board space by replacing over 50 standard logic and memory devices
- Constructed using verified macro cell functions

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

QUALITY STATEMENT

WaferScale Integration, Inc. is committed to producing and delivering defect-free products and services that meet or exceed the specified requirements. We are dedicated to a system of defect prevention and an attitude of zero defects through management example.

The management of WaferScale Integration, Inc. pledges this to you . . . our CUSTOMER.

QUALITY & RELIABILITY PROGRAM

INTRODUCTION

The Quality & Reliability (Q & R) Program at WSI is intended to comply with the latest requirements of: MIL-I-45208, "Inspection System Requirements;" MIL-Q-9858, "Quality Program Requirements;" and Appendix A of MIL-M-38510, "Quality Assurance Program."

The task of the Q & R Program is to assure that all delivered products conform to the requirements of each order placed with the company and to drive the quality and reliability improvement process to optimize product performance and market acceptance.

In order to support the above, WSI has organized its Q & R Department into four main sections:

1.0 Quality Control (QC) — The main functions of QC are:

1.1 QC Engineering — To provide the Quality Control function and the manufacturing function with technical support.

1.2 Materials Quality Control — Assures that all raw materials used in the manufacture of the final product meet WSI specified requirements.

1.3 Process Quality Control — Assures that all WSI manufacturing processes are within their specified control limits and that in-process product maintains the highest quality level.

2.0 Quality Assurance (QA) — The main functions of QA are:

2.1 QA Engineering — To provide a factory interface for customers on all field returns and corrective action requests; to provide technical assistance to other QA functions and engineering functions in matters of product quality.

2.2 QA Inspection — To assure that the final product meets the internal product specifications, applicable customer specifications, and/or other contractual requirements.

2.3 Calibration — To provide a function that assures all equipment used to test or accept product is properly calibrated at set intervals to assure product quality.

3.0 Reliability — The main functions of Reliability are:

3.1 Reliability Engineering (RE) — To assure that all manufactured products reflect the highest reliability standards and to measure this with in-house programs to compare against these standards; to provide technical assistance to other engineering functions in matters of product reliability; to prepare and execute Qualification plans for new or revised designs, packages and processes.

3.2 Reliability Test Lab — To provide suitable step/stress facilities in-house, or at an appropriate vendor, for the purpose of conducting qualifications or quality conformance inspections.

3.3 Failure Analysis Lab — To provide and maintain a Failure Analysis function in-house, or at an appropriate vendor, for the purpose of investigating the cause(s) of failure(s) and for their systematic elimination from the product.

4.0 Configuration Control — The main functions are:

4.1 Document Control — To provide an organized, systematic function for originating, changing and distributing internal specifications and drawings; to provide for the prompt notification of changes to customers with Change Notification Requirements.

4.2 Audits — To provide a system for periodically checking WSI's and vendor's quality programs for compliance with stated policies, procedures and contractual requirements.

4.3 Specification Review and Writing — To provide a function for reviewing customer documentation and converting those requirements to in-house requirements.

5.0 For detailed coverage of WSI's total Q & R System, write or call for our "Quality & Reliability Policy Manual."

QUALITY

What Is Quality?

Quality is something we all strive for, but seem at a loss to define simply. At WSI we have chosen to adopt Phil Crosby's definition because it is the simplest and to-the-point.

Quality is: "Conformance to the requirements."

Quality is not relegated only to the state of the product. It encompasses all administrative areas also. At WSI we strive for *zero defects* and our programs are geared to attain this.

Product Flows

WSI offers four standard product flows which are shown below:

1.0	Flows	883 Class B	Mil-Temp	Standard	Standard
2.0	Packages	Hermetic	Hermetic	Hermetic	Plastic
3.0	Operating Temperature Range	Military −55°C to +125°C		Commercial 0°C to 70°C	

	SCREENS & INSPECTIONS	MIL-STD-883 METHOD/CONDITION OR WSI REQUIREMENT	883	MIL-TEMP	STANDARD	STANDARD
4.0	Preseal Inspection	M2010/Condition B	100%	N/A	N/A	N/A
		WSI Requirement	N/A	100%	100%	100%
5.0	Stabilization Bake	M1008/Condition C 24 Hours at +150°C	100%	N/A	N/A	N/A
6.0	Temperature Cycle	M1010/Condition C 10 Cycles, −65°C to +150°C	100%	N/A	N/A	N/A
7.0	Constant Acceleration	M2001/Condition D or E Y1:20K Gs or 30K Gs	100%	N/A	N/A	N/A
8.0	Hermeticity					
8.1	Fine Leak	M1014/Condition A or B	100%	100%	100%	N/A
8.2	Gross Leak	M1014/Condition C	100%	100%	100%	N/A
9.0	Data Retention (EPROMs only)	Packaged Parts — 72 Hours at 140°C	100%	N/A	N/A	N/A
		Wafers — 48 Hours at 200°C	100%	100%	100%	100%
10.0	Pre Burn-In Electricals	Per Applicable Data Sheet	100%	N/A	N/A	N/A
11.0	Burn-In	M1015/Condition A or D 160 Hours at +125°C or Equivalent	100%	N/A	N/A	N/A
12.0	Post Burn-In Electricals	Per Applicable Data Sheet	100%	N/A	N/A	N/A
13.0	% Defective Allowable	M5004, Paragraph 3.5.1	5%	N/A	N/A	N/A
14.0	Final Electricals	Per Applicable Data Sheet	100%	100%	100%	100%
15.0	Quality Conformance	QCI per M5005/Group A	Sample	Sample	Sample	Sample
16.0	External* Vision	M2009	100%	100%	N/A	N/A
		WSI Requirement	N/A	N/A	100%	100%
17.0	Quality Conformance	QCI per M5005/Group B, C and D	Sample	N/A	N/A	N/A
18.0	Shipping Inspection	Every Shipment	100%	100%	100%	100%

*WSI ships visual and mechanical criteria to a 1.0% AQL.

RELIABILITY

INTRODUCTION

WSI is committed to serving its customers with the most reliable products available. From the onset, products are designed, manufactured and tested to rigorous WSI standards which culminate in devices that are differentiatedly better in performance and reliability.

RELIABILITY GOALS

The failure rate for any integrated circuit has been classically described as having a "bathtub" curve (see Figure 1). The "bathtub" curve shows three main stages of a product's life: 1) A very high failure rate in the beginning, known as the infant mortality period, which normally represent the first 300 hours in a system. 2) A constant failure rate period, with relatively few failures, known as the intrinsic failure rate or useful life. This period represents the next 20 years or more of operation. 3) Eventually, the devices enter the wearout region where failures begin to occur very rapidly again. The mean time to failure for wearout is >20 years.

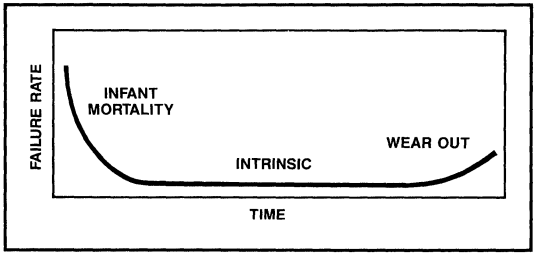


Figure 1 — Bathtub Curve

WSI has established the following Reliability Goals at T_A = 55°C:

• Infant Mortality	0–300 Hours	≤0.1%
• Intrinsic Failure Rate	300 Hours–20 Years	≤100 FITs
• Wear Out		MTTF >20 Years

In order to meet the infant mortality goal of 0.1%, an appropriate burn-in screen may be implemented. Data collected on 10,000 EPROMs, from various wafer fab runs, showed the failure rate to be 0.23% during the first six hours of burn-in which then dropped to 0.02% over the next 21 hours. This demonstrated that a proper burn-in (150°C, 6.5V) for six hours was sufficient to lower the failure rate to less than 0.1%. This screen is revisited on a periodic basis to determine whether or not it is continuing to meet the stated goal. Similar data is collected when a new process is released to production.

RELIABILITY PREDICTION

The life expectancy of an integrated circuit can be accelerated by both temperature and voltage. At WSI, both are used extensively in assessing product reliability.

Temperature

For many years, temperature had been known to be an accelerator of various types of failure mechanisms. By increasing the temperature, it was observed that the devices took less time to fail. By elevating the temperature, long term reliability data can be collected in a relatively short time. Failure rate calculations are based upon data collected from accelerated life testing.

The temperature dependence on accelerating failures has been shown to be exponential. The acceleration factor between two temperatures can be calculated by using the Arrhenius equation:

$$A = \text{Exp}\ \frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

T_1 = Application Junction Temperature
T_2 = Accelerated Stress Junction Temperature
k = 8.62×10^{-5} eV/°K
E_a = Thermal Activation Energy

Each failure mechanism is accelerated differently by temperature. The thermal activation energy is a constant which adjusts for the temperature dependence for the various failure mechanisms. The following activation energies are used for each failure mechanism:

Failure Mechanism	Activation Energy (E_a)
Oxide Defects	0.3 eV
Masking Defects	0.5 eV
Assembly Defects	0.5 eV
Bulk Silicon Defects	0.5 eV
Electromigration	0.5–0.9 eV
Charge Loss	0.6 eV
Contamination	1.0 eV

Voltage

Oxide defects are more highly accelerated by voltage than by temperature (note the low activation energy for oxide defects). To obtain a higher acceleration for oxide defects during a lifetest, the supply voltage is increased by 6.5 volts when possible. By increasing the supply voltage, an additional acceleration of 55× is obtained for oxide defects.

FAILURE RATE CALCULATIONS

Failure rate calculations are based on a summary of the life test results. Typically, the failure rate is calculated for a family of devices manufactured on a given process. To calculate a failure rate, the acceleration factor for each activation energy must be calculated between the accelerated stress temperature and the application temperature. Junction temperatures are used rather than ambient temperatures. The junction temperature is the temperature at the die surface due to the heat generated by the device itself. The junction temperature is the product of the power dissipation multiplied by the thermal resistance of the package and is then added to the ambient temperature.

$$T_J = T_A + (\theta_{JA})(P); \text{ where } P = (I_{CC})(V_{CC})$$

The next step is to calculate the number of accelerated device hours from the lifetest data. The number of device hours is the product of the sample size multiplied by the hours of the lifetest. The equivalent device hours for each activation energy is calculated by multiplying the device hours by the acceleration factor. The failure rate for each activation energy is computed by dividing the total number of failures with the same activation energy by the equivalent device hours. Typically a 60% confidence level is used for calculating failure rates. The total failure rate is the summation of all the failure rates for each activation energy. The failure rate is expressed in FITs which is the number of failures per 10^9 device hours:

$$\text{Failure Rate} = \sum \frac{F(E_a, 60\%\ UCL)}{A(E_a, T_1, T_2) \times D} \times 10^9 \text{ FITs}$$

$F(E_a, 60\%\ UCL) = 1.049$ (Failures with same E_a) + 1.0305
$A(E_a, T_1, T_2)$ = Acceleration Factor
D = Device Hours

RELIABILITY DATA SUMMARY

The Reliability Data Summary is a quarterly publication which presents all WSI reliability data and is available to WSI customers. The data is presented with the test results at each timepoint with accompanying failure analysis where applicable. In this manner, the customer can compute the failure rate for his own application. For convenience, the failure rates have been computed to 55°C using the previous method discussed.

Current life test results show a failure rate of 40 FITs at 55°C on EPROMs with a density of 64K and higher. This data was computed from approximately 5 million device hours. The failure rate for Bit Slice products was approximately 130 FITs after 1.4 million device hours.

PRODUCT RELIABILITY

ElectroStatic Discharge Sensitivity (ESDS)

WSI products are tested for ESDS in accordance with Method 3015 of MIL-STD-883. All devices exhibit an ESDS greater than 2,001 volts with typical inputs beginning to fail around 5,000 volts and outputs in the range of 3,000 to 4,000 volts. Testing is performed on new products or when changes occur that can influence the ESDS of a device (i.e., redesign, new process, etc.).

Latch-Up

Latch-up is a condition that occurs due to excessive current (spikes) in the circuit periphery and creates a large potential that triggers a parasitic SCR inherent to all CMOS processes. Latch-up can be destructive to the device. To reduce latch-up, WSI employs an epitaxial layer above a low resistivity substrate. This diverts the current to the substrate, away from the active circuitry, reducing the lateral potential which triggers the latch-up. WSI products are tested for latch-up between −1.0 and +7.0 volts with currents up to 200 mA forced on any one pin.

Qualifications

All new processes, major process changes, or new design rules must pass a reliability qualification. One to three lots are used depending on the reliability risk involved. Qualification requires a minimum 1000-hour life test at 125°C. EPROMs are stressed dynamically at 150°C with an overvoltage condition of 6.5 volts. (The overvoltage accelerates oxide defects an additional 55×.) Qualifications place heavy emphasis on the first 48 hours (infant mortality) of the life test. Larger sample sizes are used initially with the number decreasing as the qualification progresses. If other reliability stresses are to be used in the qualification, those units will receive a 48-hour burn-in prior to starting those stresses in order to eliminate any unrelated failures.

Bit Slice and EPROM products basically run on the same fab process with the Bit Slice products lacking the steps for the EPROM cell. Because of the common processing between the two product lines, more emphasis is placed on performing reliability studies on EPROMs. The peripheral circuitry of the EPROM, decoders, I/Os, etc., have the identical design rules as the Bit Slice products. Every reliability evaluation on an EPROM product also evaluates the Bit Slice product line. Testing and failure analysis is easier on an EPROM. Because of the large availability of EPROM burn-in boards, larger sample sizes can be used. Also, the straightforward operation of an EPROM allows 100% dynamic stressing during burn-in at a higher temperature and voltage.

EPROMs are subjected to special qualification requirements to study the data retention characteristics of the EPROM cell. These devices are programmed with a 100% zero pattern and then baked at 150°C, 200°C, and 250°C for 1000 hours. These tests are performed to insure that WSI reliability goals have been met.

Other tests include Temperature Cycle from −65°C to +150°C for 1000 cycles. In addition, plastic packaged products must pass 1000 hours of Temperature Humidity

Bias at 85°C and 85% relative humidity, and 168 hours of Pressure Pot at 15 PSIG.

EPROMs

Because of the floating gate storage cell, EPROMs have unique reliability considerations. Data retention is related to the ability to store a charge on the floating gate of the EPROM cell. Charge loss can shift the threshold of the EPROM cell from a programmed state to an unprogrammed state, i.e., from a logical 0 to a 1. Charge loss is the result of defects in the oxide surrounding the floating gate. These defects occur during wafer processing and generally affect a single bit in the array. It has been shown that defective bits of this type lose their charge very rapidly with high temperature. For this reason, they can be effectively screened out with a high temperature bake.

EPROM Screening

Data retention screening is performed on all EPROM products. Screening is at the wafer level so that higher temperatures can be used without the fear of affecting the solderability of a packaged unit. The screen consists of programming each device 100% and then baking the wafers for 48 hours at 200°C. After the bake, the 100% pattern is verified. This screen is equivalent to 4 years of continuous operation at 55°C. The High Temperature Storage Life (HTSL 200) data in Table 1 shows the effectiveness of the screen. The data shows that the failure rate is very low for the first 500 hours of a 200°C bake. This is equivalent to 38 years of operation at 55°C and thereby demonstrates the reliability of the EPROM cell.

Charge can also flow electrically to the floating gate. Charge gain is charge transfer from either the word line or the bit line to the floating gate such that an unprogrammed device becomes programmed. To date, charge gain has not been observed on any WSI EPROM.

EPROM Programming

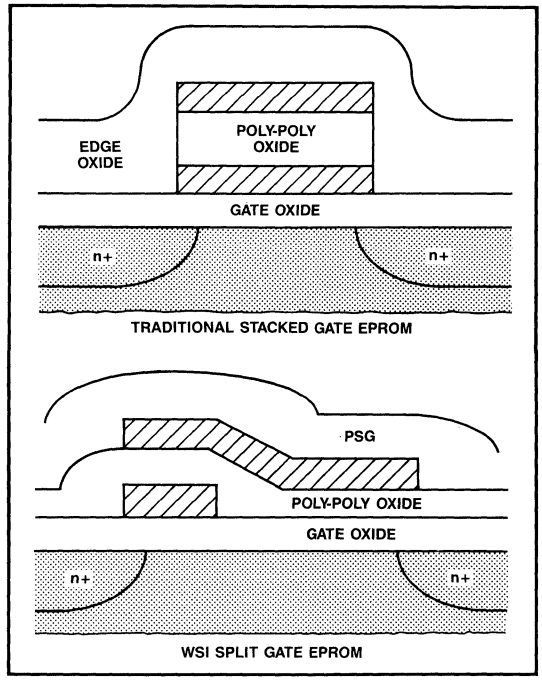
Electrical charge loss is the major cause for programming failure. Program Disturb is charge transfer from the floating gate to the bit line. This charge loss mechanism occurs during programming due to the high electrical fields present. Failure occurs when an already programmed cell loses charge as other cells, with the same bit line, are being programmed. This failure mechanism is the result of oxide defects at the edge of the floating gate.

DC Erase is electrical charge loss to the word line. DC Erase is the result of defects in the oxide between the floating gate and the word line above. Like Program Disturb, DC Erase occurs during programming when an already programmed cell losses charge as adjacent cells on the same word line are programmed.

The WSI split gate EPROM has matured to the point that programmability by the customer can be >99.9%. Product Assurance data collected on over 5000 units showed programmability to be 99.98%. The most recent Program/Erase cycling data had no fails out to 100 cycles. By focusing on eliminating Program Disturb and DC Erase, the threshold of a programmed EPROM cell is consistently well above 7.0 volts and typically above 8.0 volts. This provides additional operating margin and reliability.

Split Gate vs. Traditional EPROMs

The patented WSI split gate EPROM (Patent #4,639,893) has several inherent advantages over the traditional stacked gate EPROM. One major advantage is better control over the etching of the floating gate during wafer processing. With the traditional stacked gate EPROM, a self-aligning process is used to define the floating gate. That is, a layer of poly is first deposited for the floating gate, followed by an oxide layer, and finally another poly layer for the control gate. To define and etch the floating gate, the control gate poly and poly-poly oxide are first etched and are used as the mask to define the floating gate. This means that the etching of the control gate and the poly-poly oxide must be very well controlled in order to achieve good definition of the floating gate. For the WSI split gate EPROM, the floating gate is etched using conventional methods in the step following the poly deposition of the floating gate. This way the floating gate etch is very well controlled and is not dependent upon both a poly and an oxide etch.



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This leads to another advantage for the WSI split gate EPROM. Because of the critical etching involved with the traditional stacked gate EPROM, it is difficult to use a silicide on the control gate to reduce the poly resistance and speed up the device. The conventional processing steps used to make the WSI split gate EPROM does allow for the successful use of silicide and is used on many products.

Another advantage lies in the quality of the oxide surrounding the floating gate. Following the floating gate etch on the stacked gate EPROM, a third oxide is grown which contacts the edge of the floating gate as well as the poly-poly oxide. The floating gate is now surrounded by three separate oxides (gate oxide, poly-poly oxide and edge oxide), all of which contribute to defects. On the other hand, the WSI split gate EPROM has a homogeneous poly-poly oxide which contacts the floating gate at the top as well as the edges. Because the floating gate of the split gate EPROM is surrounded by only two oxides, neither of which are etched, better oxide integrity is obtained. Oxide integrity is the key in reducing reliability problems such as: Data Retention, Program Disturb and DC Erase.

PROCESS RELIABILITY

WSI utilizes a Class 10 wafer fab facility for all its wafer processing. Most processing is performed by robotics which reduces the human factors such as contamination and handling from contributing to reliability failures. Photolithography is performed using state-of-the-art steppers which eliminates marginal mask defects from becoming reliability hazards. Passivation cracks and metal shifting on double layer metal devices are minimized on even large die through a planarization process. When processing is completed, the back of the wafer is polished to remove oxides and other processing artifacts. This results in better eutectic die attach at assembly and reduces the chances of die cracking.

The CMOS Advantage

The low power characteristics of CMOS greatly enhance the reliability of any system. This can be demonstrated by comparing the thermal characteristics of WSI's RPROM vs a Bipolar PROM and applying it to reliability.

For instance, if we assume a 24-pin CERDIP package with a thermal resistance of 63°C in an ambient temperature of 55°C, the following junction temperatures are obtained:

WS57C49 CMOS RPROM (Standby)	WS57C49 CMOS RPROM (18 MHz)	64K Bipolar PROM
I_{CC} = 15 mA	I_{CC} = 50 mA	I_{CC} = 150 mA
P = 75 mW	P = 250 mW	P = 750 mW
T_R = 5°C	T_R = 16°C	T_R = 47°C
T_J = 60°C	T_J = 71°C	T_J = 102°C

Calculating the acceleration factor of the Bipolar PROM over the WSI EPROM, using an activation energy of 0.5 eV, we find that the acceleration is 7× in the standby mode and 4× at 18 MHz. This means that by running cooler, the WSI RPROM will have a life expectancy of 4 to 7 times greater than its Bipolar PROM equivalent.

The following tables show reliability results obtained on various WSI products.

EPROM RELIABILITY DATA

Dynamic High Temperature Life Test — Table 1

DHTL 150°C 6.5 Volts	48 Hours	168 Hours	500 Hours	1000 Hours	1500 Hours	2000 Hours
	4/6540	6/5079	2/4259	4/3970	0/486	0/486

Product Hours	Failures	Act. Eng.	Failure Rate 60% Conf at 55°C	Cause
4,808,388 Hours	3	0.3 eV × 55	1.6 FITs	Oxide Defects
	3	0.5 eV	18 FITs	Assembly Defects
	8	0.6 eV	19 FITs	Charge Loss
	2	1.0 eV	0.3 FITs	Contamination
		Combined Failure Rate:	38.9 FITs	

High Temperature Storage Life Test

HTSL 200°C No Bias	168 Hours 1/502	332 Hours 0/501	500 Hours 0/501	1000 Hours 5/501
HTSL 150°C No Bias	168 Hours 0/451	332 Hours 0/451	500 Hours 0/451	1000 Hours 0/451

Product Hours	Failures	Act. Eng.	Failure Rate 60% Conf at 55°C	Cause
(501,168 at 200°C / 451,000 at 150°C)	5	0.6 eV	16.5 FITs	Charge Loss
	1	1.0 eV	0.08 FITs	Contamination
		Combined Failure Rate:	16.6 FITs	

Product Types: WS27C64F, WS57C64F, WS57C49, WS27C128F, WS27C256F

OTP RELIABILITY DATA

Dynamic High Temperature Life Test

Table 2

DHTL 150°C 6.5 Volts	48 Hours	168 Hours	500 Hours	1000 Hours
	2/1522	0/314	0/246	1/246
	1 — Bond Short 1 — Output Leakage			1 — Charge Loss

Temperature/Humidity with Bias

THB 85°C/85% RH 5.0 Volts	168 Hours	500 Hours	1000 Hours
	0/287	0/287	0/287

Pressure Pot

PPOT 15 PSIG/121°C	96 Hours	168 Hours	240 Hours
	0/315	0/315	1/315
			1 — No Corrosion

Temperature Cycle

TC −55°C/+150°C	100 Cycles	500 Cycles	1000 Cycles
	0/234	0/234	2/234
			1 — Bond Lift 1 — Input Leakage

Products: WS57C64F

BIT SLICE RELIABILITY DATA

Dynamic High Temperature Life Test

Table 3

DHTL 125°C 5.5 Volts	48 Hours	168 Hours	500 Hours	1000 Hours
	1/1670	0/1606	1/1246	0/728
DHTL 150°C 5.5 Volts	**48 Hours**	**168 Hours**	**500 Hours**	**1000 Hours**
	1/1383	0/825	2/298	0/295

Product Hours	Failures	Act. Eng.	Failure Rate 60% Conf at 55°C	Cause
(1,023,672 at 125°C 411,826 at 150°C)	1 4	1.0 eV 0.5 eV	1.5 FITs 127 FITs	Ionic Contamination 1 — Bond Short 3 — Functional
		Combined Failure Rate:	128.5 FITs	

Temperature/Humidity with Bias

THB 85°C/85% RH 5.0 Volts	168 Hours	500 Hours	1000 Hours
	1/520	0/412	4/313
	1 — Static IDD		2 — Corrosion 1 — Functional 1 — Static IDD

Pressure Pot

PPOT 15 PSIG/121°C	96 Hours	168 Hours	240 Hours
	2/501	1/499	0/182
	2 — Short	1 — Functional	

Temperature Cycle

TC −55°C/+150°C	500 Cycles	1000 Cycles
	1/390	1/389
	1 — Wire to Wire Short	1 — Wire to Wire Short

Products: WS5901, WS59016, WS5910A, WS59520, ASIC1004

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WAFERSCALE INTEGRATION, INC.

WSI PRODUCT PACKAGES

(By Alphabetical Drawing Number)

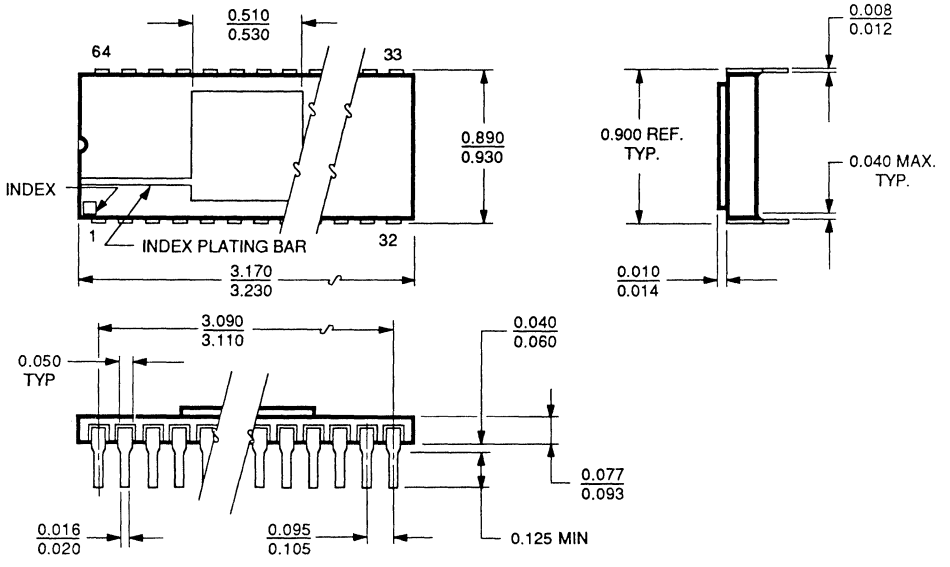
Drawing	Pins	Package	Window	Package Type	Page No.
B1	64	Sidebrazed Ceramic Dip, 0.9″	No	B	8-1
C1	(28)	Ceramic Leadless Chip Carrier	Yes	C	8-1
C2	(32)	Ceramic Leadless Chip Carrier	Yes	C	8-2
C3	(44)	Ceramic Leadless Chip Carrier	Yes	C	8-2
D1	24	CERDIP, 0.6″	Yes	D	8-3
D2	28	CERDIP, 0.6″	Yes	D	8-3
D3	40	CERDIP, 0.6″	Yes	D	8-4
D4	32	CERDIP, 0.6″	Yes	D	8-4
F1	24	Ceramic Flatpack	Yes	F	8-5
G1	68	Ceramic PGA	No	G	8-5
G2	101	Ceramic PGA	No	G	8-6
J1	68	Plastic Leaded Chip Carrier	No	J	8-6
J2	44	Plastic Leaded Chip Carrier	No	J	8-7
K1	24	CERDIP, 0.3″	No	K	8-7
L1	68	Ceramic Leaded Chip Carrier	No	L	8-8
M1	64	Plastic Dip, 0.9″	No	M	8-8
P1	40	Plastic Dip, 0.6″	No	P	8-9
P2	24	Plastic Dip, 0.6″	No	P	8-9
P3	28	Plastic Dip, 0.6″	No	P	8-10
S1	24	Plastic Dip, 0.3″	No	S	8-10
S2	28	Plastic Dip, 0.3″	No	S	8-11
T1	24	CERDIP, 0.3″	Yes	T	8-11
T2	28	CERDIP, 0.3″	Yes	T	8-12
X1	88	Ceramic PGA	Yes	X	8-12
X2	44	Ceramic PGA	Yes	X	8-13
Y1	40	CERDIP, 0.6″	No	Y	8-13
Z1	(68)	Ceramic Leadless Chip Carrier	No	Z	8-14

(In Order of Pin Count)

Pins	Package	Window	Package Type	Drawing	Page No.
24	CERDIP, 0.3″	No	K	K1	8-7
24	CERDIP, 0.3″	Yes	T	T1	8-11
24	Plastic Dip, 0.3″	No	S	S1	8-10
24	CERDIP, 0.6″	Yes	D	D1	8-3
24	Plastic Dip, 0.6″	No	P	P2	8-9
24	Ceramic Flatpack	Yes	F	F1	8-5
28	CERDIP, 0.3″	Yes	T	T2	8-12
28	Plastic Dip, 0.3″	No	S	S2	8-11
28	CERDIP, 0.6″	Yes	D	D2	8-3
28	Plastic Dip, 0.6″	No	P	P3	8-10
(28)	Ceramic Leadless Chip Carrier	Yes	C	C1	8-1
32	CERDIP, 0.6″	Yes	D	D4	8-4
(32)	Ceramic Leadless Chip Carrier	Yes	C	C2	8-2
40	CERDIP, 0.6″	No	Y	Y1	8-13
40	CERDIP, 0.6″	Yes	D	D3	8-4
40	Plastic Dip, 0.6″	No	P	P1	8-9
44	Plastic Leaded Chip Carrier	No	J	J2	8-7
(44)	Ceramic Leadless Chip Carrier	Yes	C	C3	8-2
44	Ceramic PGA	Yes	X	X2	8-13
64	Sidebrazed Ceramic Dip, 0.9″	No	B	B1	8-1
64	Plastic Dip, 0.9″	No	M	M1	8-8
68	Ceramic PGA	No	G	G1	8-5
(68)	Ceramic Leadless Chip Carrier	No	Z	Z1	8-14
68	Plastic Leaded Chip Carrier	No	J	J1	8-6
68	Ceramic Leaded Chip Carrier	No	L	L1	8-8
88	Ceramic PGA	Yes	X	X1	8-12
101	Ceramic PGA	No	G	G2	8-6

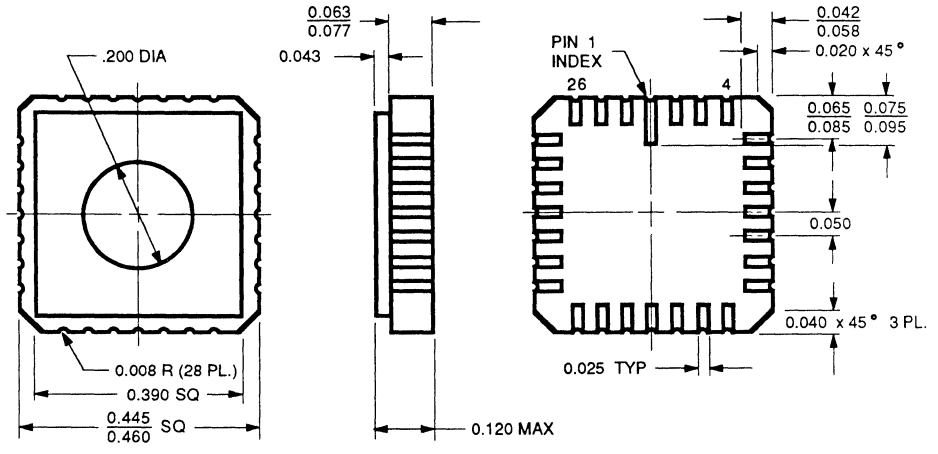
DRAWING B1

64 PIN Ceramic Side Braze (Package Type B)



DRAWING C1

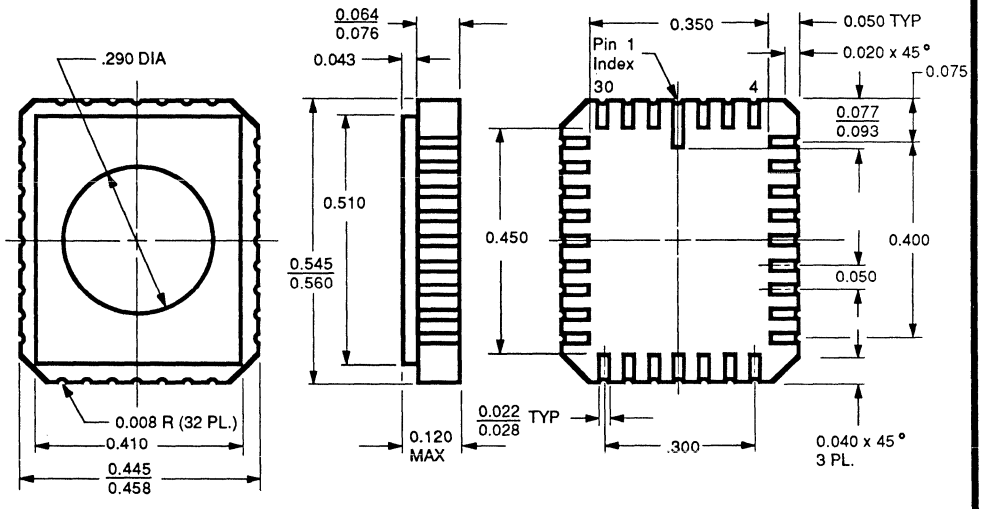
28 PAD Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



8

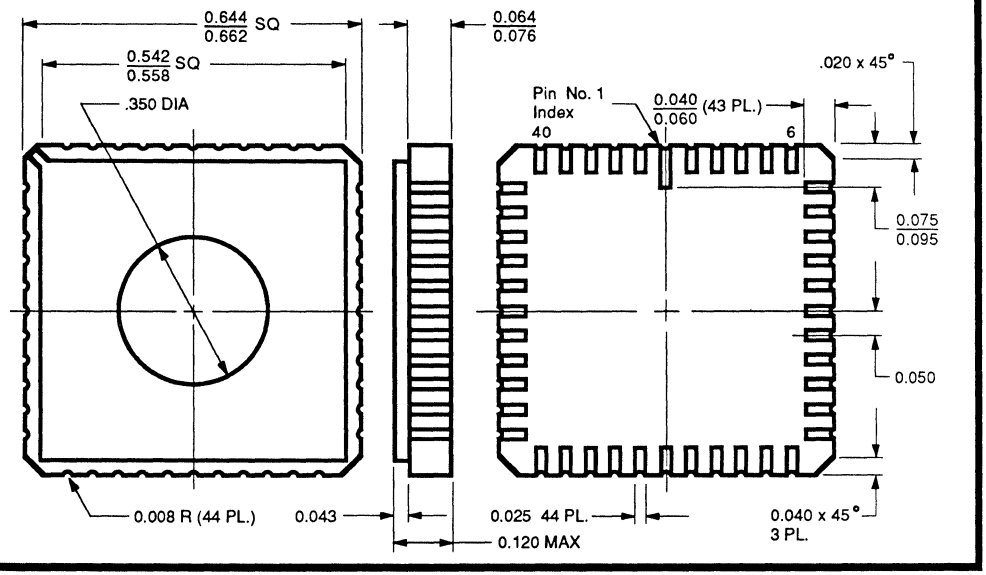
DRAWING C2

32 PAD Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



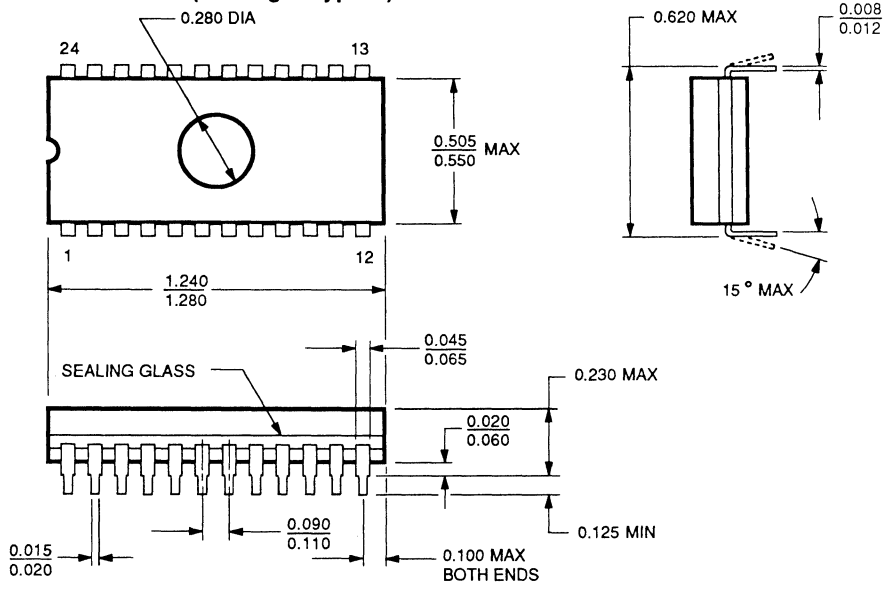
DRAWING C3

44 PAD Ceramic Leadless Chip Carrier (CLLCC) (Package Type C)



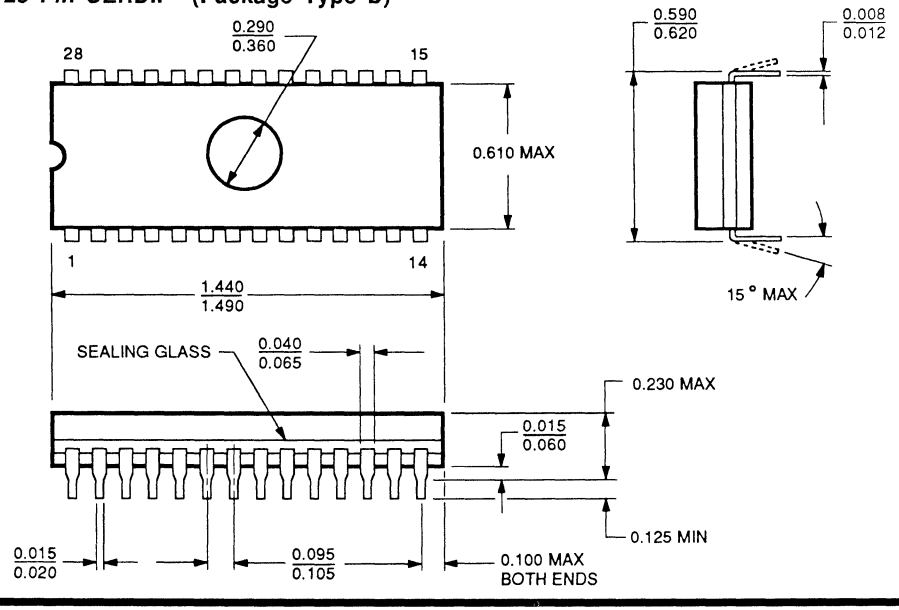
DRAWING D1

24 Pin CERDIP (Package Type D)



DRAWING D2

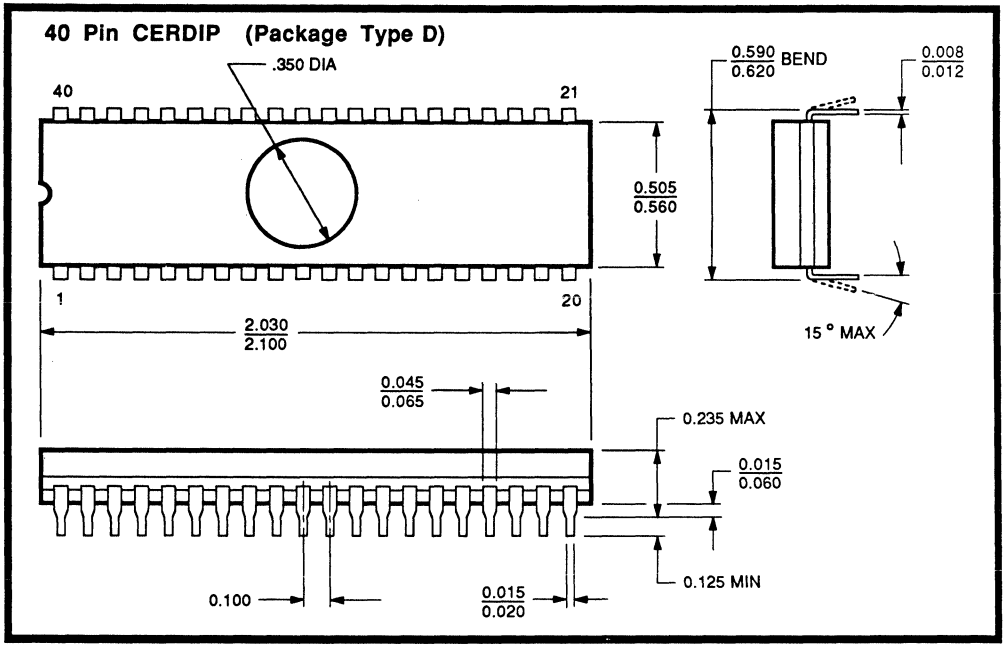
28 Pin CERDIP (Package Type D)



8

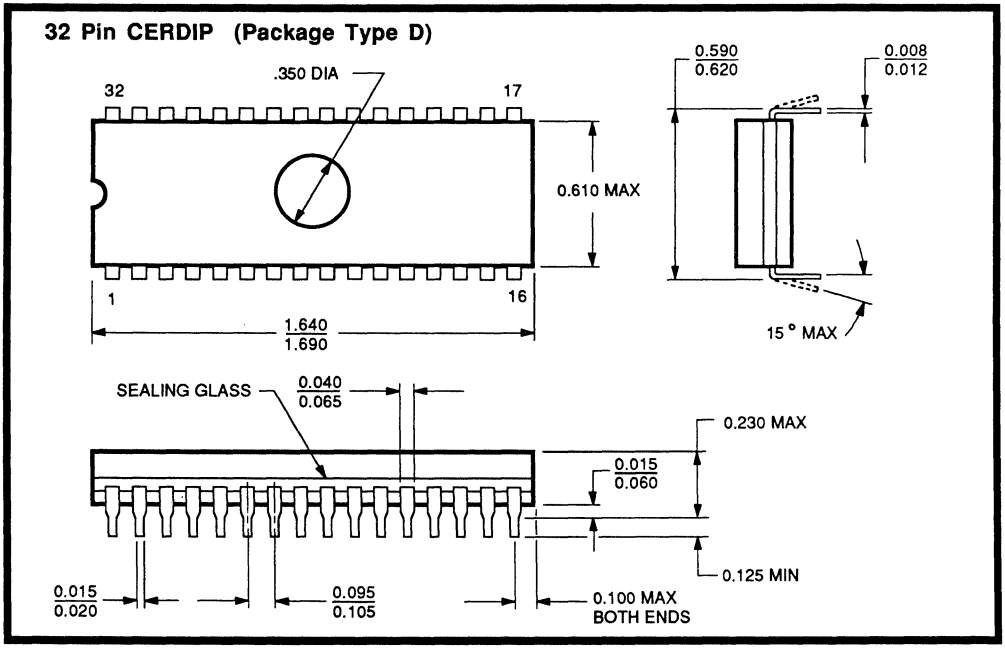
DRAWING D3

40 Pin CERDIP (Package Type D)



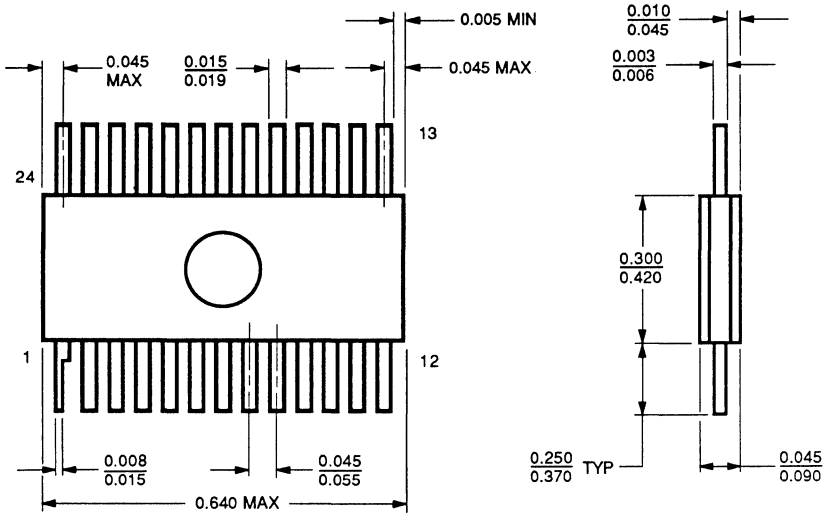
DRAWING D4

32 Pin CERDIP (Package Type D)



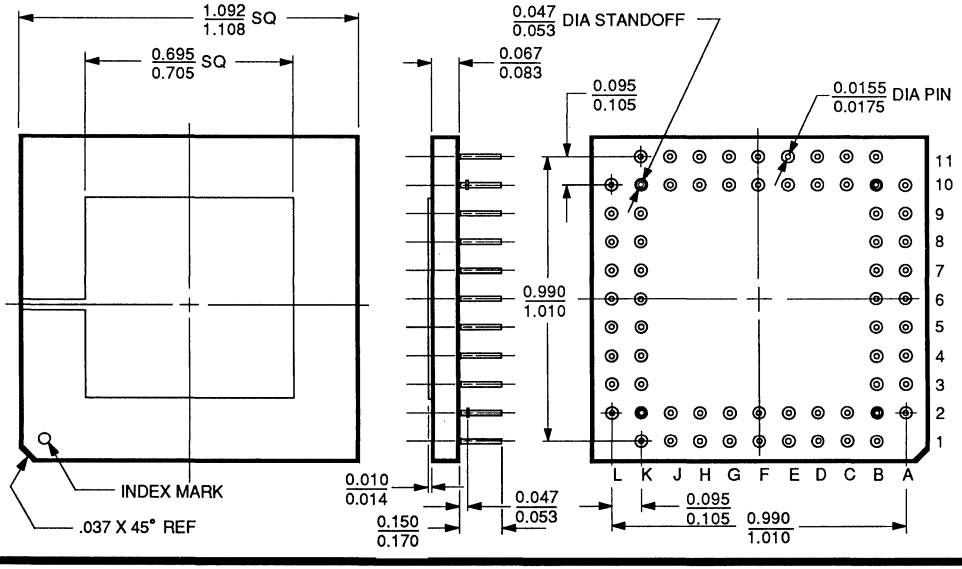
DRAWING F1

24 Pin Ceramic Flatpack (Package Type F)



DRAWING G1

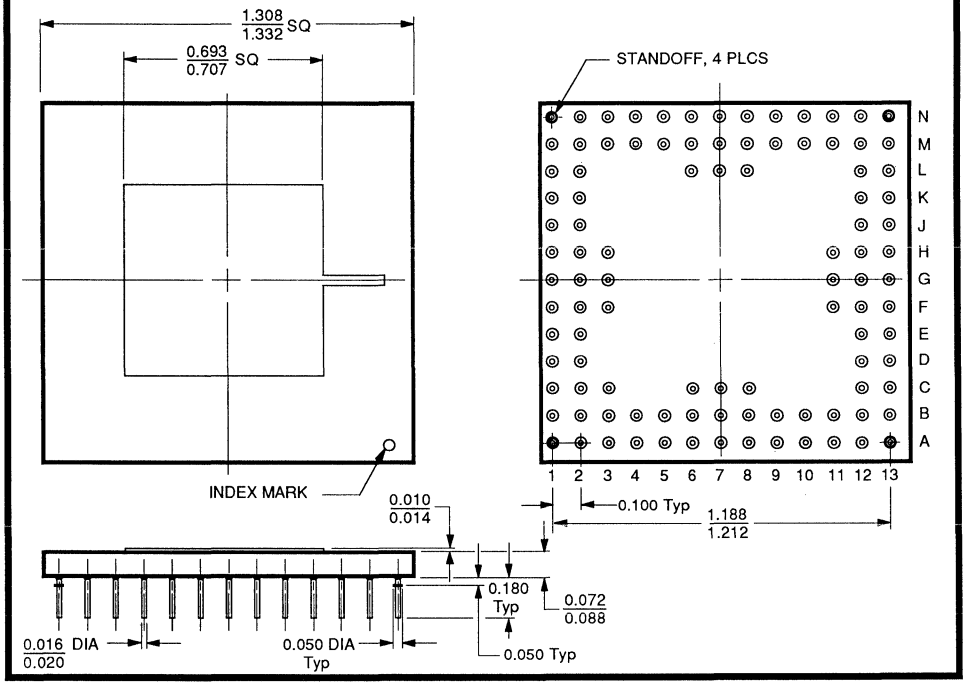
68 Pin CERAMIC PGA (Package Type G)



8

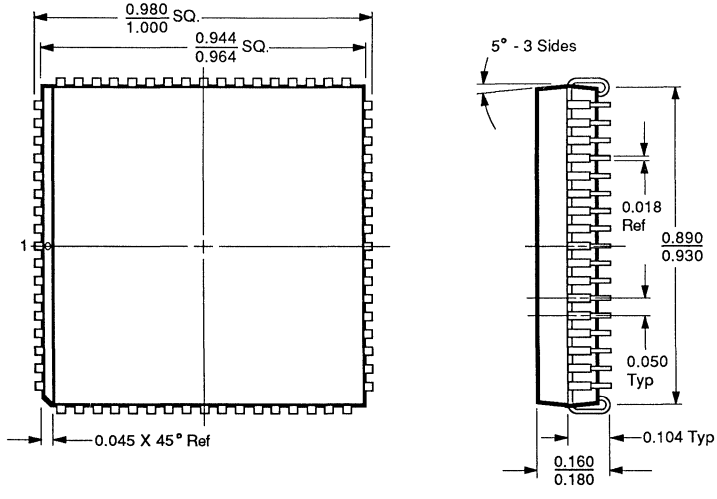
DRAWING G2

101 PIN Ceramic PGA (Package Type G)



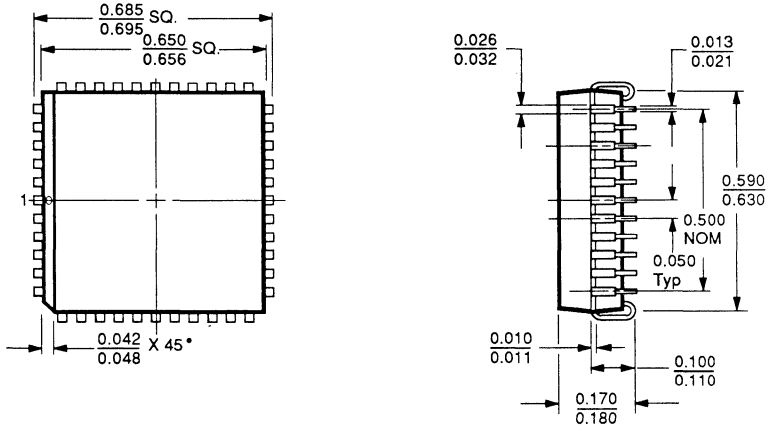
DRAWING J1

68 PIN Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



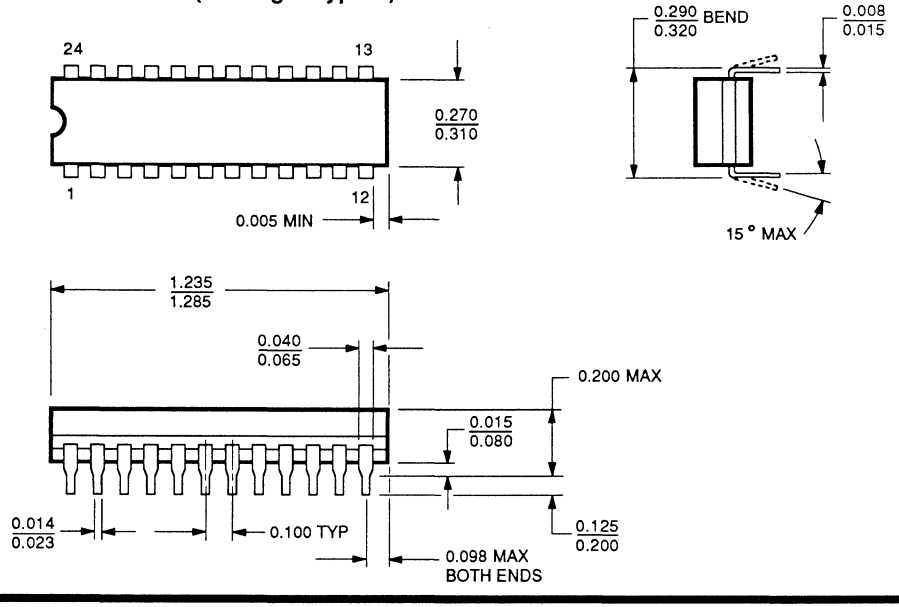
DRAWING J2

44 PIN Plastic Leaded Chip Carrier (PLDCC) (Package Type J)



DRAWING K1

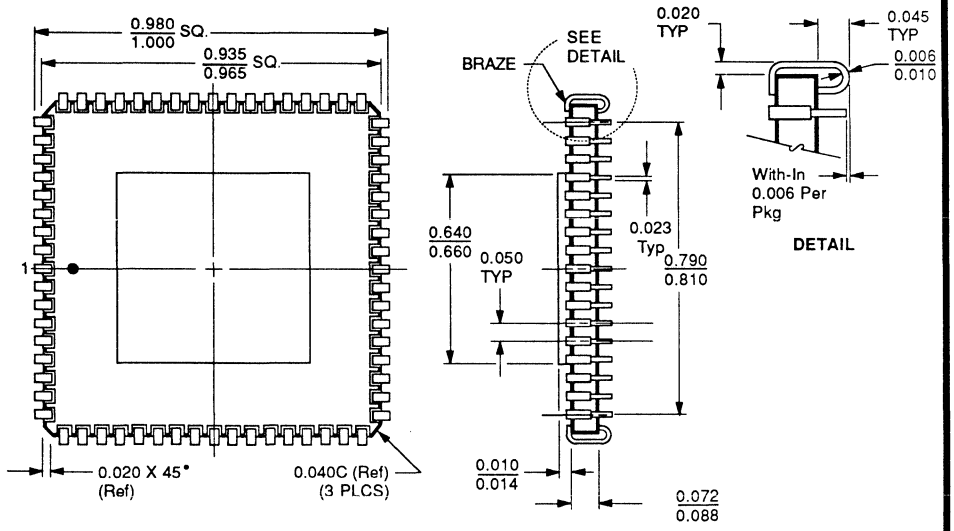
24 Pin CERDIP (Package Type K)



8

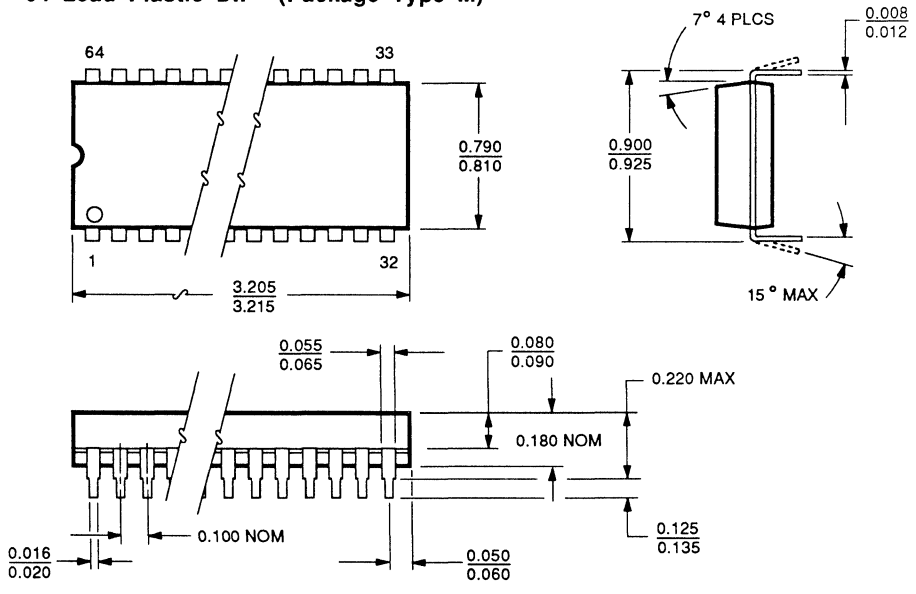
DRAWING L1

68 PIN Ceramic Leaded Chip Carrier (CLDCC) (Package Type L)



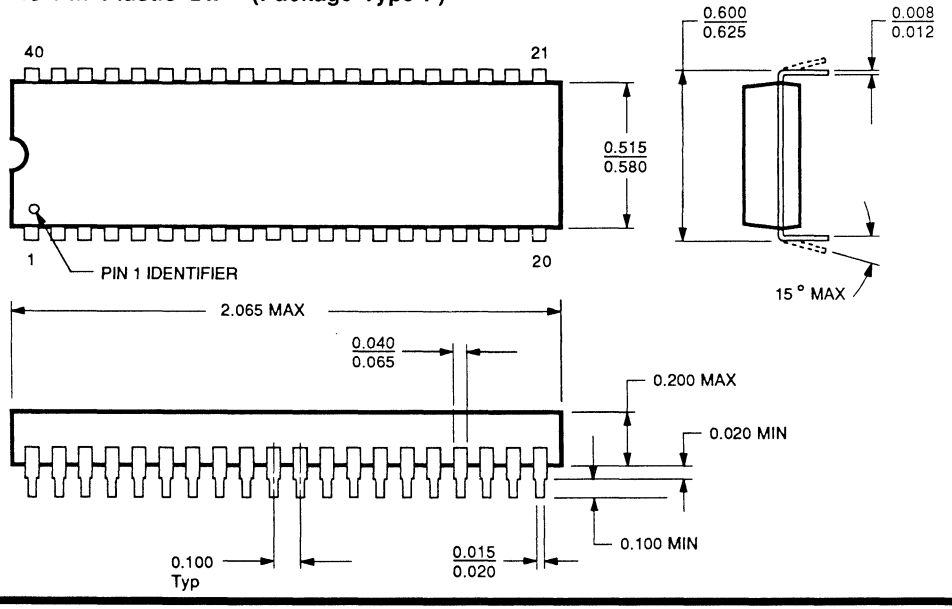
DRAWING M1

64 Lead Plastic DIP (Package Type M)



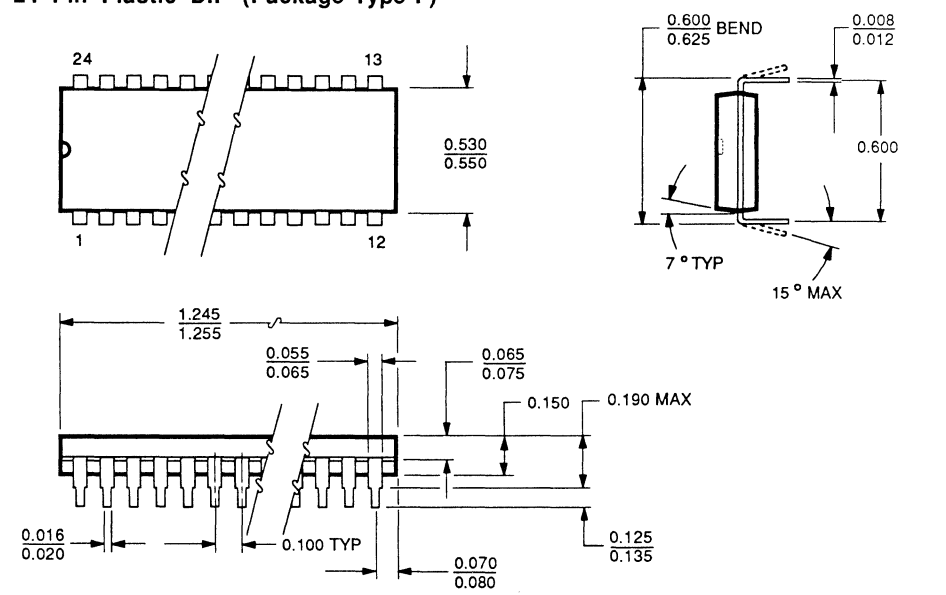
DRAWING P1

40 Pin Plastic DIP (Package Type P)



DRAWING P2

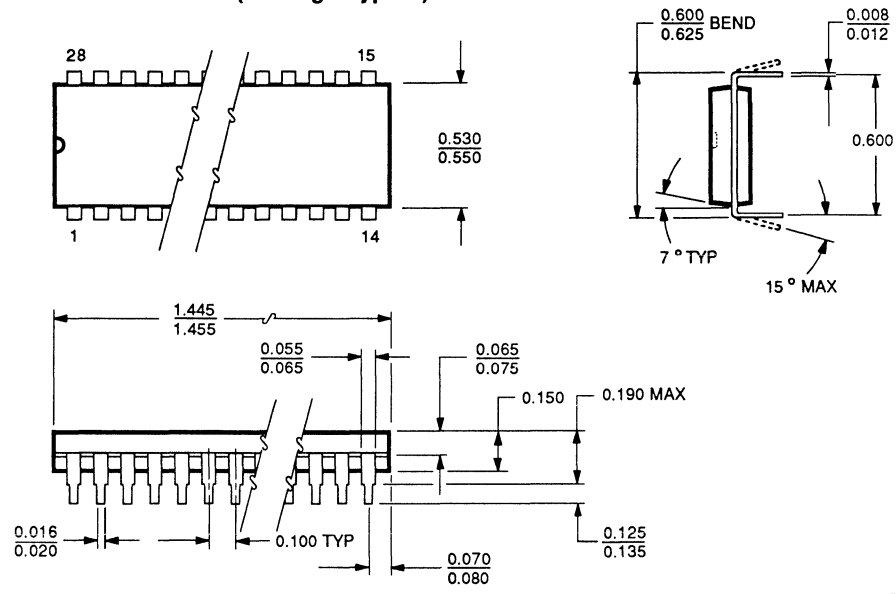
24 Pin Plastic DIP (Package Type P)



8

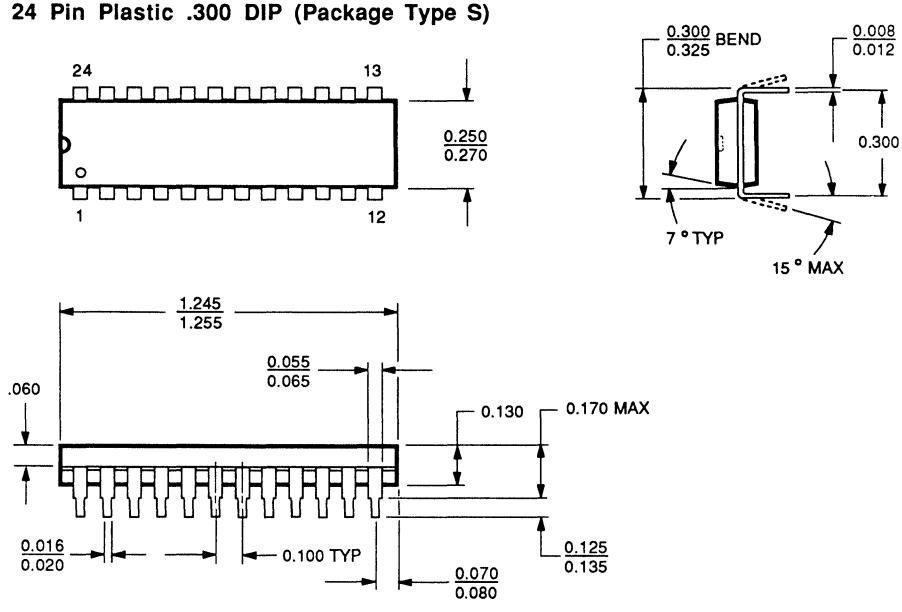
DRAWING P3

28 Pin Plastic DIP (Package Type P)



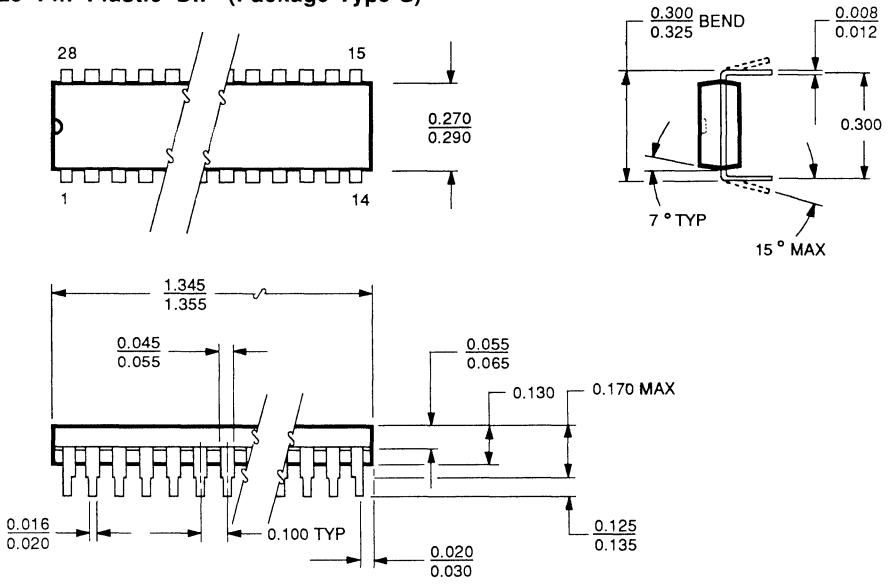
DRAWING S1

24 Pin Plastic .300 DIP (Package Type S)



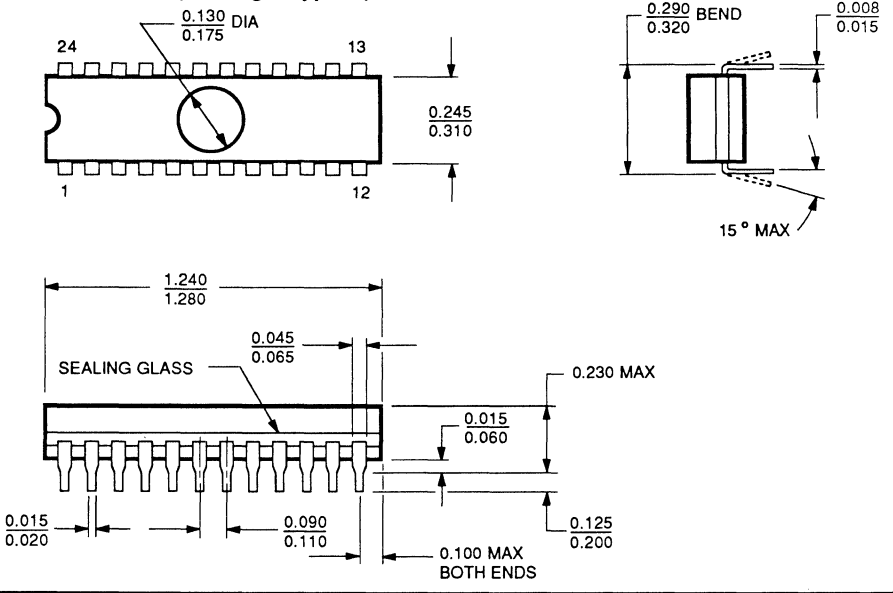
DRAWING S2

28 Pin Plastic DIP (Package Type S)



DRAWING T1

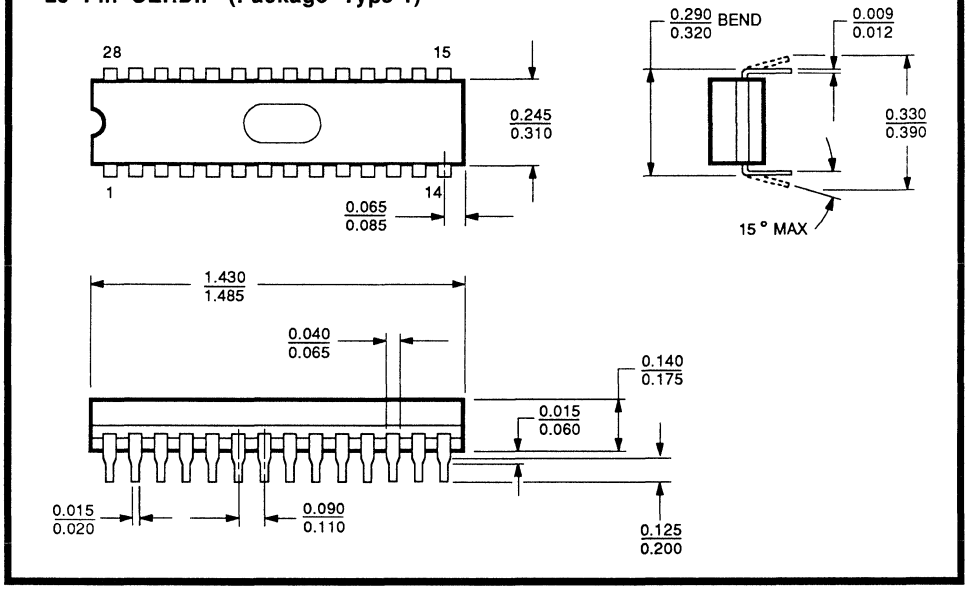
24 Pin CERDIP (Package Type T)



8

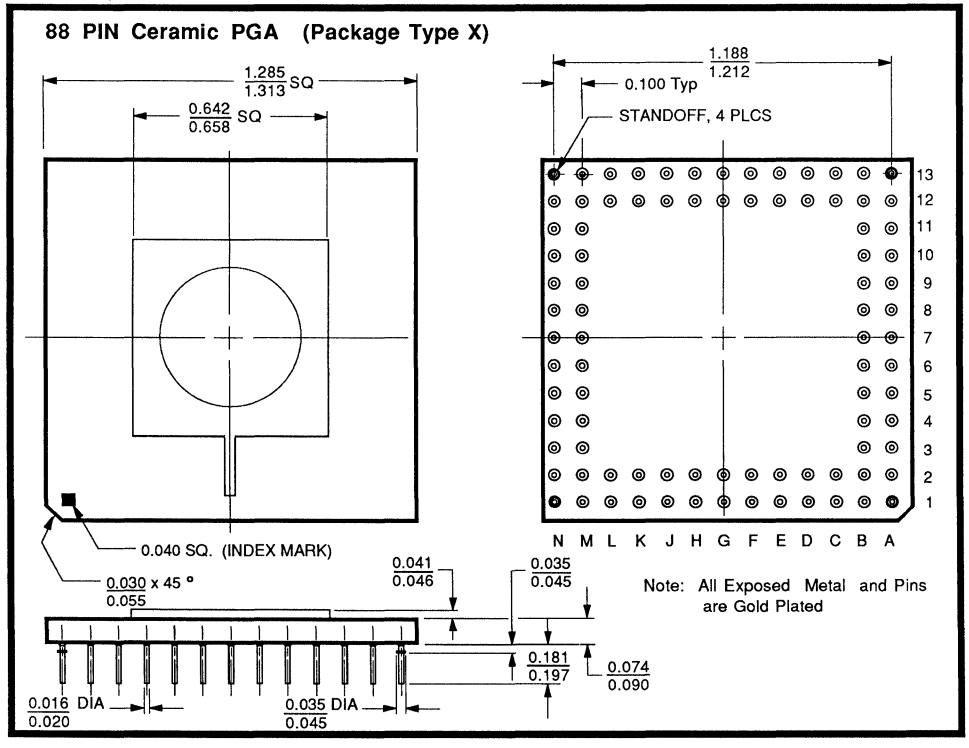
DRAWING T2

28 Pin CERDIP (Package Type T)



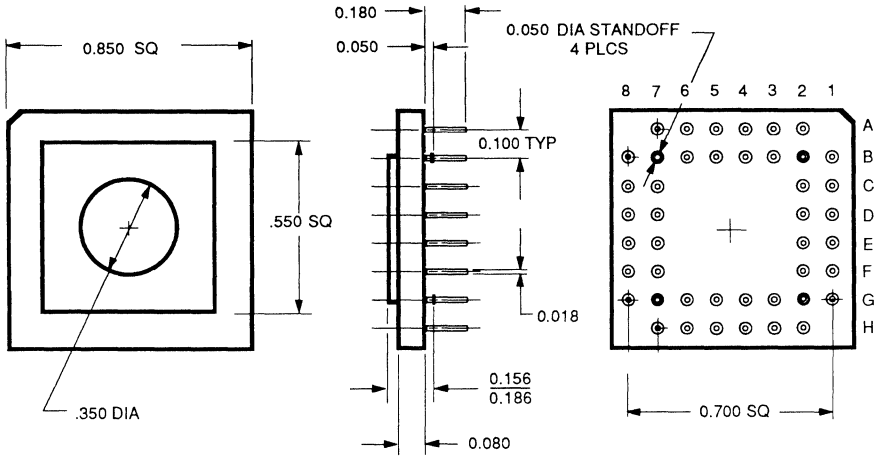
DRAWING X1

88 PIN Ceramic PGA (Package Type X)



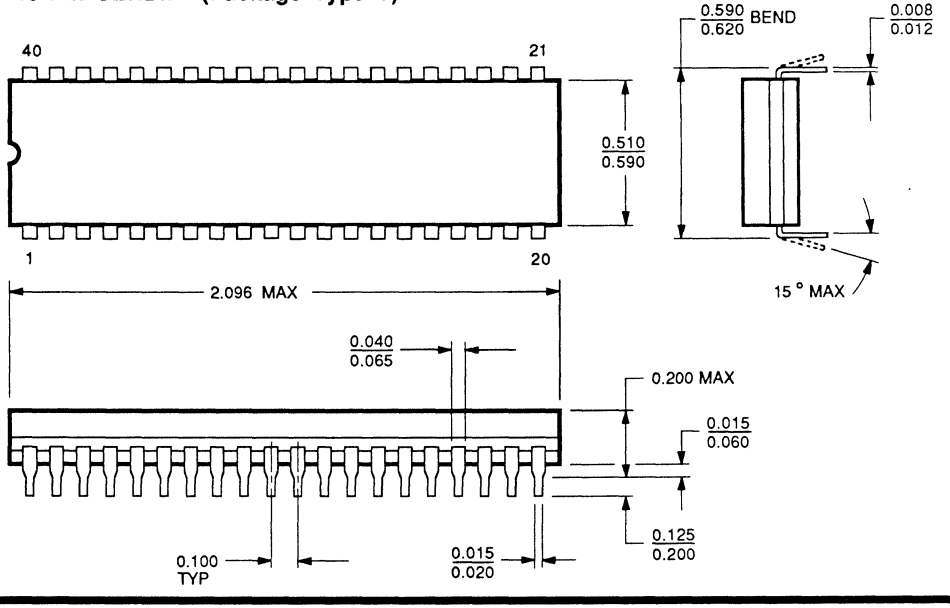
DRAWING X2

44 Pin Ceramic PGA (Package Designator X)



DRAWING Y1

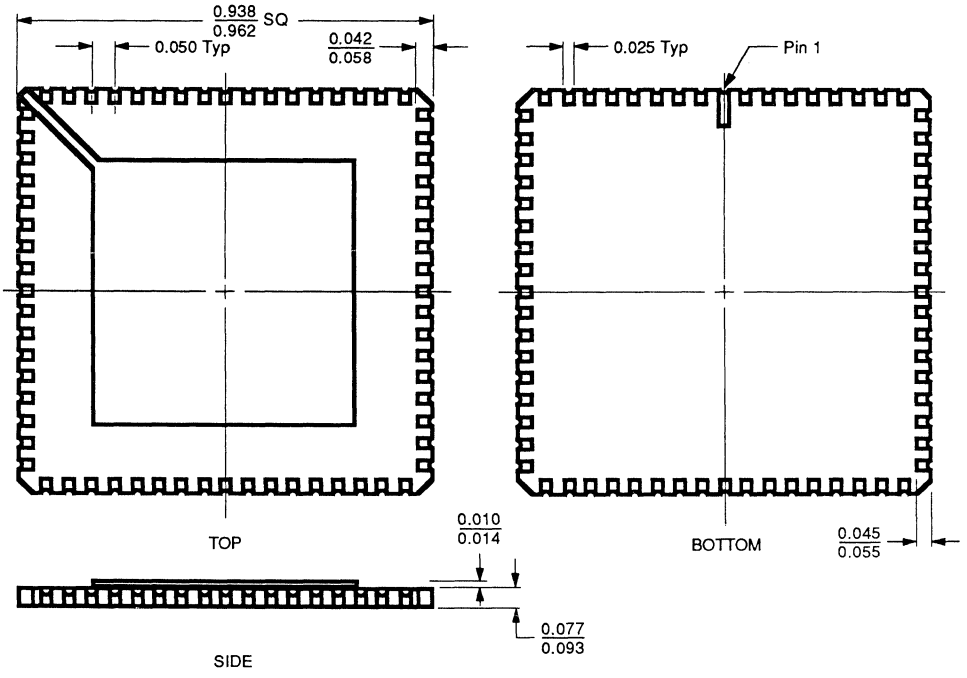
40 Pin CERDIP (Package Type Y)



8

DRAWING Z1

68 PAD Ceramic Leadless Chip Carrier (CLLCC) (Package Type Z)



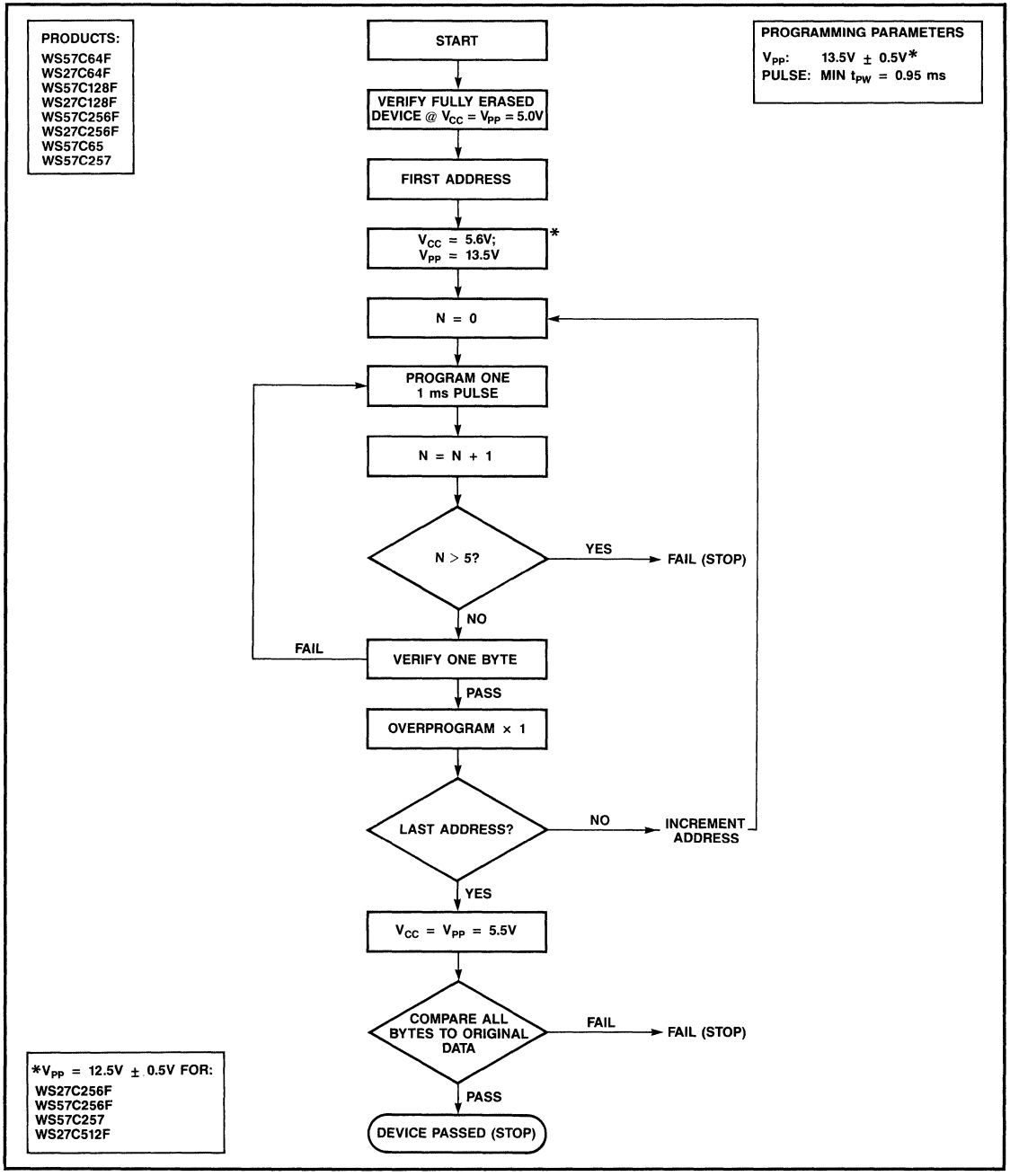
WAFERSCALE INTEGRATION, INC.

SECTION INDEX

PROGRAMMERS/PROGRAMMING

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

EPROM PROGRAMMING ALGORITHM A



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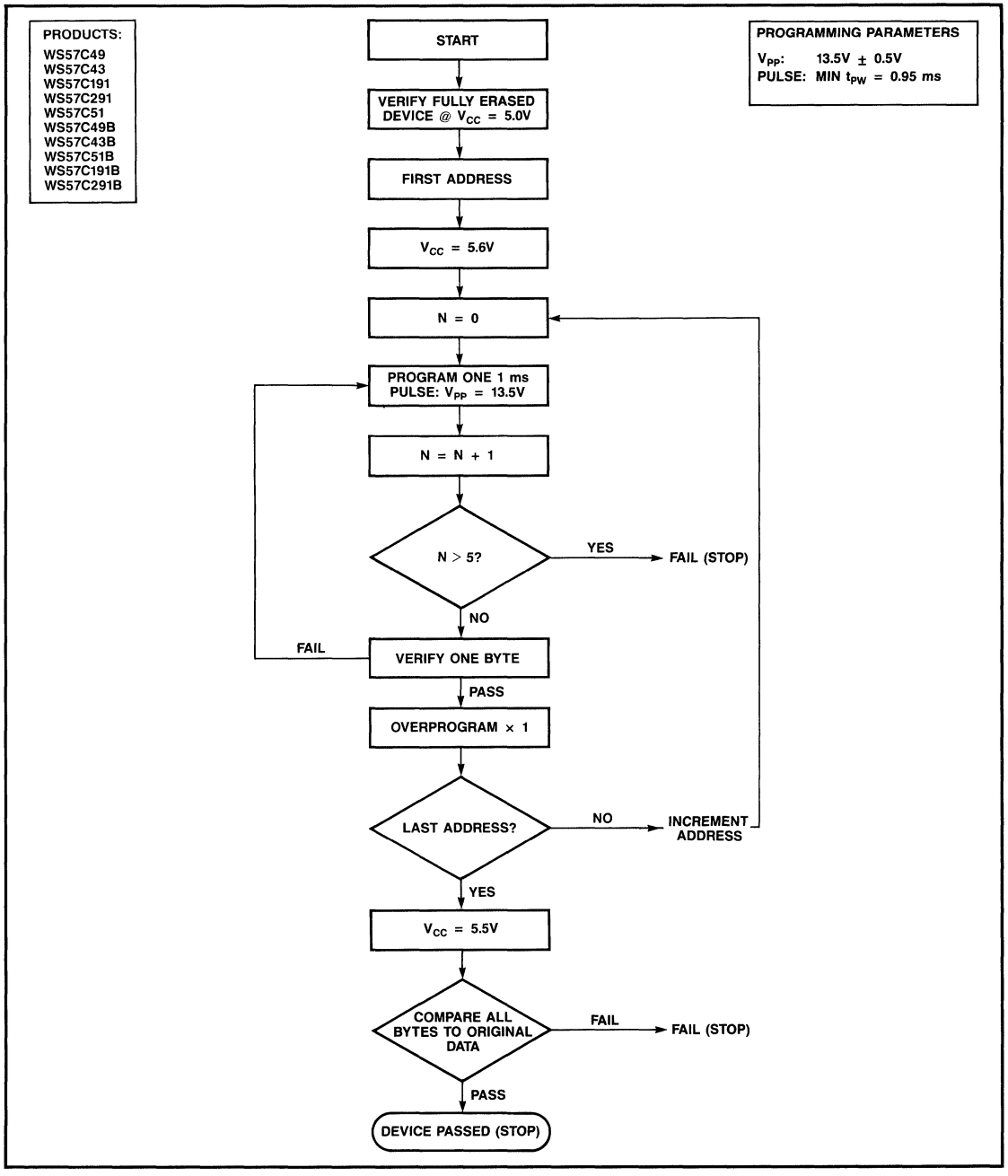
EPROM PROGRAMMING ALGORITHM B



WAFERSCALE INTEGRATION, INC.

MAGICPRO™ *MEMORY AND LOGIC PROGRAMMER*

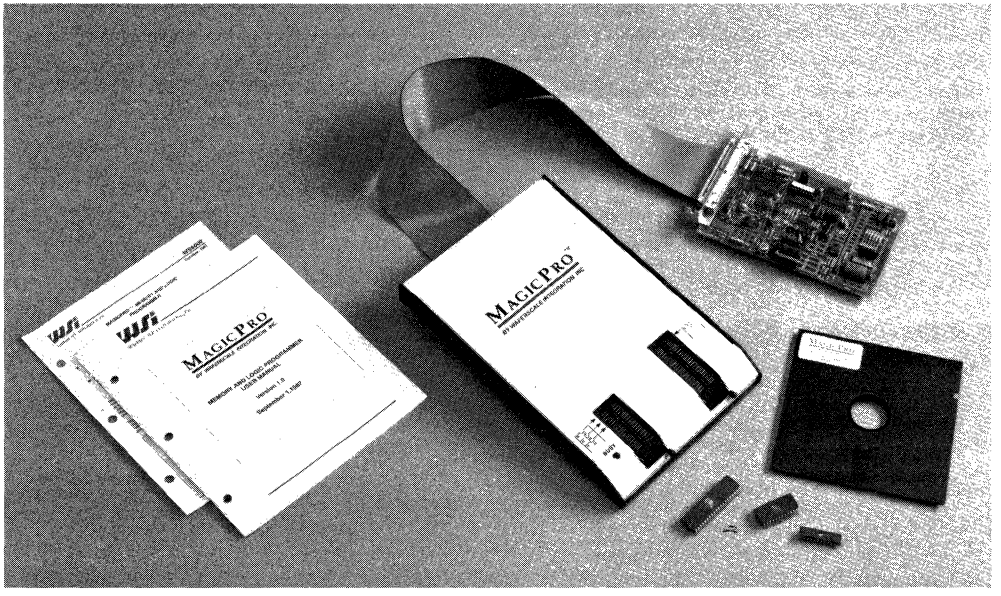
KEY FEATURES

- **Programs All WSI CMOS EPROMs and RPROMs™ (x8, x16, Mux I/O and All Future Programmable Products**
- **Programs 24, 28, 32 and 40 Pin Standard 600 Mil or Slim 300 Mil Dip Packages Without Adaptors**
- **Programs LCC and PGA Packaged Product by Using Adaptors**
- **Easy-to-Use Menu-Driven Software**
- **Compatible with IBM PC/XT/AT© Family of Computers (and True Plug-Compatible)**

GENERAL DESCRIPTION

MAGICPRO™ is an engineering development tool designed to program existing WSI EPROMs and RPROMs™ and future WSI programmable products. It is used within the IBM PC© and compatible environment. The MAGICPRO™ is meant to bridge the gap between the introduction of a new WSI programmable product and the availability of programming support from the EPROM programmer manufacturers (e.g., Data I/O, etc.). The MAGICPRO™ programmer and accompanying software enable quick programming of newly released WSI programmable products, thus accelerating the system design process.

The MAGICPRO™ plug-in board is integrated easily into the IBM PC©. It occupies a short expansion slot and its software requires only 256K bytes of computer memory. The two external ZIF-Dip sockets in the Remote Socket Adaptor (RSA) support WSI 24, 28, 32 and 40 pin standard 600 mil or slim 300 mil Dip packages without adaptors. LCC and PGA packages are supported using adaptors.



9

Many features of the MAGICPRO™ Programmer show its capabilities in supporting WSI's future products. Some of these are:

— 24 to 40 pin JEDEC Dip pinouts
— 1 Meg. address space (20 address lines)
— 16 data I/O lines

The MAGICPRO™ menu driven software system makes using different features of the MAGICPRO™ an easy task. Software updates are done via floppy disk which eliminates the need for adding a new memory device for system upgrading. Please call 800-TEAM-WSI for information regarding programming WSI products not listed herein. The MAGICPRO™ reads Intel Hex format for use with assemblers and compilers.

MAGICPRO™ COMMANDS

— Help
— Upload RAM from device
— Load RAM from disk
— Write RAM to disk
— Display RAM data
— Edit RAM
— Move/copy RAM
— Fill RAM
— Blank test device
— Verify device
— Program device
— Select device
— Configuration
— Quit MagicPro™

WSI PRODUCTS

WS57C191/291	2K × 8	RPROM™
WS57C43	4K × 8	RPROM™
WS57C43B	4K × 8	RPROM™
WS57C49	8K × 8	RPROM™
WS57C49B	8K × 8	RPROM™
WS57C51	16K × 8	RPROM™
WS57C51B	16K × 8	RPROM™
WS27C64F	8K × 8	EPROM
WS57C64F	8K × 8	EPROM
WS57C65	4K × 16	EPROM
WS57C66	4K × 16 (Mux I/O, 28 Pin DIP)	EPROM
WS27C128F	16K × 8	EPROM
WS57C128F	16K × 8	EPROM
WS27C256F	32K × 8	EPROM
WS57C256F	32K × 8	EPROM
WS57C257	16K × 16	EPROM
WS27C512F	64K × 8	EPROM

TECHNICAL INFORMATION

- Size: IBM PC© short length card
- Port Address Location: 100H to 1FFH—default 140H (If a conflict exists with this address space, the address location can be changed in software and with the switches on the plug-in board.)
- System Memory Requirements: 256K bytes of RAM
- Power: +5 Volts, 0.03 Amp.; +12 Volts, 0.04 Amp.
- Remote Socket Adaptor (RSA): The RSA contains two ZIF-Dip sockets that are used to program and read WSI programmable products. The 32 pin ZIF-Dip socket supports 24, 28 and 32 pin standard 600 mil or slim 300 mil Dip packaged product. The 40 pin ZIF-Dip socket supports all 40 pin Dip packages. Adaptor sockets are available for LCC and PGA packages.

ORDERING INFORMATION

The WS6000 MAGICPRO™ System contains:

MAGICPRO™ IBM PC© plug-in programmer board
MAGICPRO™ Remote Socket Adaptor and cable
MAGICPRO™ Operating System Floppy Disk and Operating Manual

MAGICPRO™ Adaptors include:

WS6001 28 CLLCC Adaptor
WS6002 32 CLLCC Adaptor
WS6003 44 CLLCC Adaptor
WS6005 28 Pin Dip WS57C66 Adaptor

All WSI memory products program easily on standard commercially available EPROM programmers. Manufacturers of these EPROM programmers offer a broad range of products which cover prototyping through high volume production requirements. The leading programmer manufacturer is Data I/O Corporation located in Redmond, Washington. The table below covers that portion of Data I/O's product line which supports WSI's programmable products. For more information regarding programming support for WSI products call toll-free 800-TEAM WSI (800-832-6974) or 415-656-5400 (CA).

Data I/O Programming Support

P/N	Family/Pinout	Unipak 2	Unipak 2B/Cartridge	Unisite/Module	GangPak
RPROMs: WS57C191	7B/21	V12	V12/—	1.5/Site 40	V07
WS57C291	7B/21	V12	V12/—	1.5/Site 40	—
WS57C43	7B/63	V12	V12/—	1.5/Site 40	V07
WS57C43B	7B/63	V12	V12/—	1.5/Site 40	V07
WS57C49	3C/67	V12	V12/—	—	V07
WS57C49	F3C/067	—	—	—	—
WS57C49	7B/67	—	—	1.5/Site 40	—
WS57C49B	3C/67	V12	V12/—	—	V07
WS57C49B	F3C/067	—	—	—	—
WS57C49B	7B/67	—	—	1.5/Site 40	—
WS57C51	7B/71	—	V13/351B101	1.5/Site 40	—
WS57C51B	7B/71	—	V13/351B101	1.5/Site 40	—
EPROMs: WS57C64F	3C/33	V12	V12/351B086	1.5/Site 40	V07
WS57C128F	3C/51	V12	V12/351B086	1.5/Site 40	V07
WS57C256F	3C/32	V12	V12/351B086	—	—
WS27C64F	3C/33	V12	V12/351B086	1.5/Site 40	V07
WS27C128F	3C/51	V12	V12/351B086	1.5/Site 40	V07
WS27C256F	3C/32	V12	V12/351B086	—	—
WS57C65	2C/E7	—	V12/351B095	1.5/Site 40	—
WS57C257	1F/E1	—	V13/351B095	—	—

WAFERSCALE INTEGRATION, INC.

SECTION INDEX

APPLICATION NOTES

For additional information,
call 800-TEAM-WSI (800-832-6974).
In California, call 415-656-5400.

EPROMs FOR MODERN TIMES

HIGH SPEED EPROMs:

Early generations of microprocessors (e.g., 6809, 8085, 8086, etc.) and microcontrollers (8048, 8051, 6805, etc.) operated at frequencies in the 1-5 MHz range. At these operating frequencies, memory access time requirements varied from 200-500 ns. The EPROM technology available at the time was well suited for such applications. This technology, based upon a single transistor "stacked gate" EPROM cell (see Figure 1), was optimized for programmability and density, not speed. Many manufacturers were quite successful with this technology and manufactured EPROMs from 16K bits up to 1 Mbit.

However, today's generation of high performance microprocessors (80286, 80386, 68000, 68020, etc.), microcontrollers (8096, etc.) and dedicated DSP processors (TMS320xx, MC56000, etc.) operate in the 12-40 MHz range and require memories with access times well below 100 ns (see Table 1).

Table 1
MEMORY ACCESS TIME REQUIREMENTS

PART #	FREQUENCY	MEMORY ACCESS
80386	16 MHz	70 ns
68020	20 MHz	70 ns
32020	20 MHz	75 ns
56000	20 MHz	55 ns
320C25	40 MHz	40 ns

As will be shown, the traditional single transistor "stacked gate" approach is not able to provide such high speeds. As a result, system designers are forced into alternatives such as down loading from slow EPROM into fast SRAM, which provides non-volatility and high speed. Unfortunately, these techniques result in higher system costs (board space, components, power, etc.).

Semiconductor manufacturers are attempting to solve this problem at the I.C. level with various approaches. This article explains the various techniques for achieving high speed EPROMs and allows the reader to determine which technique is best suited for their application and which technique provides the best path for the future.

HIGH SPEED NVM: A GENERAL DISCUSSION

Memory arrays are laid out in two-dimensional row and column formats. These are referred to as word lines and bit lines, respectively. Selecting a word line determines which row of cells in the array has been chosen to provide the programmed output. The bit line, or column, is used to determine which of the selected cells in the row is to be read from an output. Although this technique singles out a particular EPROM cell for reading, the output of the selected EPROM is still connected to the outputs of several non-selected EPROM cells which share the same column, or bit line. Each of these non-selected cells adds some capacitance to the bit line. This capacitance must be overcome by the selected cell before the proper state ("1" or "0") can be sent to the output. The selected cell must have enough drive to be able to discharge the combined bit line capacitance. Higher drive, or read current, results in a faster capacitive discharge and, therefore, faster reading. Lower bit line capacitance and/or increasing read current are the fundamental goals associated with developing high speed, dense EPROMs. Lowering bit line capacitance is easily achieved by reducing the number of memory cells. Although this results in a speed improvement, it severely limits density.

The main problem to solve, therefore, is how to manufacture an EPROM cell which can provide high read current (for speed), high density (for small size), high reliability and ease of programming.

The following paragraphs discuss four approaches for developing a fast, dense, reliable and programmable EPROM memory.

1. SINGLE TRANSISTOR ("STACKED GATE")

The industry standard single transistor stacked gate EPROM cell (Figure 1) is optimized for efficient programming and high density. It is not well suited for high speed because of its low read current. The typical read current for a single unprogrammed stacked gate EPROM cell is between 20-50 microamps and the total bit line capacitance for a typical EPROM can be as high as 3-5 pF. Consequently, at 40 microamps of worst-case read current, it would take a "stacked gate" EPROM cell 70 ns to discharge the bit line by enough voltage to detect an unprogrammed condition. Address decoding and output buffers add another 25-50 ns (depending upon technology). Clearly, this makes it very difficult to achieve a worst-case total access time which will allow an EPROM to run with today's generation of processors (see Table 1). Several semiconductor manufacturers are looking for alternatives to surmount the inherent limitations of the older single transistor "stacked gate" EPROM.

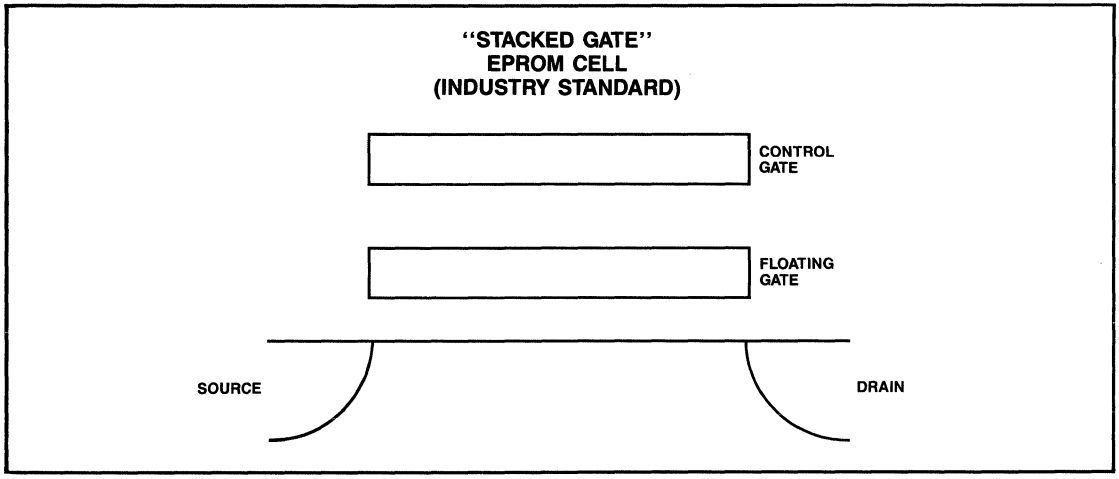


Figure 1

2. TWO TRANSISTOR FAST CELL ("STACKED GATE" EPROM)

In this approach each bit consists of *two stacked gate EPROM cells* in a differential pair. With this architecture, it is possible to employ a differential sensing technique which allows a programmed or unprogrammed state ("0" or "1") to be detected with a very small voltage swing. As a result, a memory cell can be read much faster than with a standard sensing technique. However, this incurs the penalty of twice the area of the single cell memory array as well as implications of lower yields, higher costs and lower reliability than a single cell approach.

3. FOUR TRANSISTOR FAST CELL ("STACKED GATE" EPROM)

In this approach, the differential sensing technique is also used. However, each half bit is constructed with two transistors, one of which is optimized for programming efficiency while the second transistor is optimized to give high read current (typically 150 microamps). This makes it possible to achieve very high speeds. However, a four transistor cell results in a very large memory array resulting in problems more severe than those of the two transistor approach (again, low yields, high costs and low reliability). Consequently, this technique is limited to low density devices.

STACKED GATE SUMMARY

MEMORY TYPE	RELATIVE SPEED	RELATIVE DIE SIZE
Single Transistor	Slow	Small
Two Transistor	Fast	Large
Four Transistor	Fastest	Larger

4. SINGLE TRANSISTOR FAST CELL ("SPLIT GATE" EPROM)

WaferScale Integration Inc. (WSI) has developed a proprietary technology which embodies all of the benefits of the single transistor "stacked gate" (ease of programming, reliability, and density) and conquers the fundamental problem of low read current. This patented technology is known as the "split gate" EPROM (see Figure 2).

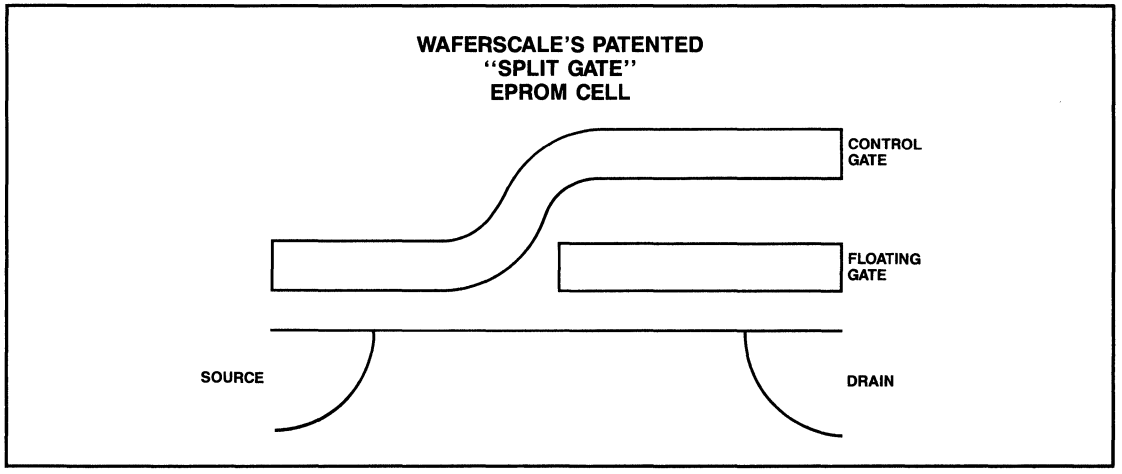


Figure 2

The "split gate" cell uses a single transistor per bit and, although it is nearly the same size as the "stacked gate," each cell provides a read current of at least 160 microamps under worst-case voltage and temperature conditions. This allows the design of very high density and *very fast* memory products. As an example of the capabilities of the "split gate," WaferScale has introduced a family of Fast EPROM products varying in density from 16K to 256K bits and in speed ranging from 35-55 ns, all manufactured with the same EPROM technology.

SPLIT GATE SUMMARY

MEMORY TYPE	RELATIVE SPEED	RELATIVE DIE SIZE
Single Transistor	Fastest	Small

As is seen from the table above, the WSI split gate EPROM technology provides the high density capability of the single transistor "stacked gate" and the fast speed of the four transistor solution.

REQUIRED FEATURES

Although speed and density are necessary EPROM attributes, they alone are not sufficient for today's memory requirements. Reliability and ease of programming play an equally important role in determining the usefulness of a memory product.

RELIABILITY

The fundamental criterion for evaluating the reliability of an EPROM cell is Data Retention. This is the ability of the cell to maintain its programmed state over time. Under extensive testing, the WaferScale patented "split gate" compares quite favorably to the industry standard "stacked gate." Figure 3 displays the results of testing which compares the charge loss of the two cell types over time.

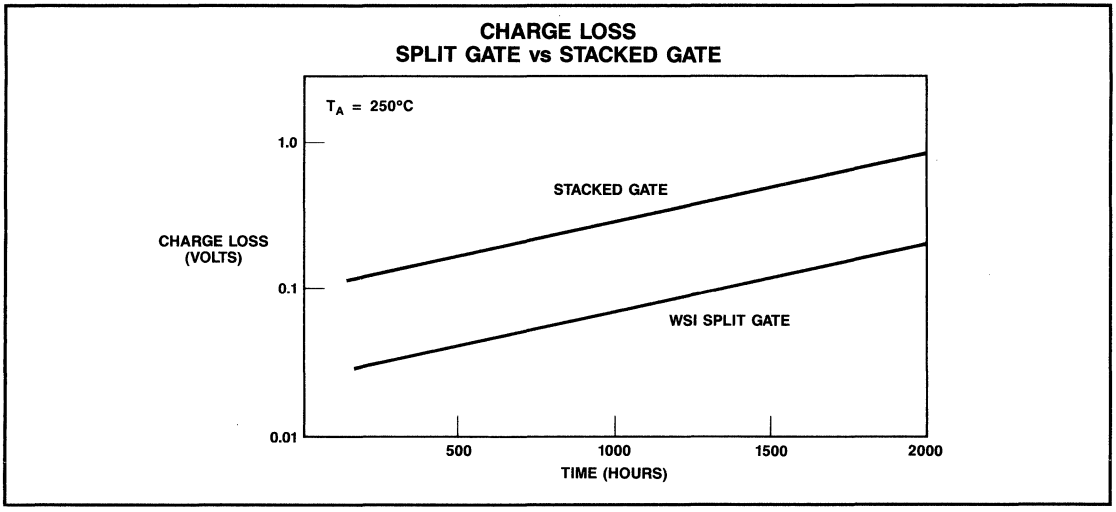


Figure 3

As can be seen from the above chart, the data retention of WaferScale's "split gate" is nearly an order of magnitude better than the older industry standard "stacked gate," which is considered a very reliable technology.

In addition, life test data has shown excellent results at higher than normal conditions (T_A = 150°C, V_{CC} = 6.5V). Fit levels of less than 100 are typical (1 Fit = 1 failure in 1 billion device hours).

This demonstrates that WaferScale has actually improved EPROM reliability in its pursuit of a high speed and high density EPROM technology. For the latest Reliability Data Summary, contact your local WaferScale sales representative.

PROGRAMMING

All WaferScale memory products are easily programmed using standard 3rd party EPROM/PROM programmers. The programming algorithms supplied to these manufacturers have been optimized for programming yield.

A further programming advantage is the fact that WaferScale devices program and verify with V_{CC} set at 5.5V. This feature is ideally suited for "on board" programming where other non-EPROM devices may be powered by the same V_{CC} power supply, because the common V_{CC} voltage used by all devices can also be used during EPROM programming. Most "stacked gate" algorithms require V_{CC} to be 6V or higher during the program mode and this requires either a separate V_{CC} supply or protection circuitry for the non-EPROM devices.

SUMMARY

Although the single transistor "stacked gate" EPROM technology is very well suited for its intended use (slow, dense NVM), it is not well suited for today's high performance memory requirements. Brute force techniques, such as using multiple transistor memory cells, can provide high performance; however, the penalty paid in die size and resultant higher costs limits these techniques to relatively low densities.

WaferScale's patented "split gate" technology combines all of the attributes of the single transistor "stacked gate" (reliability, ease of programming and density) with the speed of the multi-transistor memory cell. The result is a family of dense, high speed EPROM based products. Also, since WaferScale's technology is well suited for device scaling, the technology path for future products is already in place. This will result in products with higher density that utilize both standard and application specific architectures.

WAFERSCALE INTEGRATION, INC.

INTRODUCTION TO THE WSI MAP™ FAMILY OF MAPPABLE MEMORY PRODUCTS

The basic components in a typical microprocessor based system are an EPROM for program store, an SRAM for data store and a decoder for selecting the appropriate memory device based on the address (Figure 1). The decoder is typically implemented using descrete logic, 74XX138 type MSI building blocks or PAL® type of devices. Hardwired devices require jumpers on the P.C. board for memory configuration changes and expansion. PAL® based decoders are more flexible since they can be re-programmed for configuration changes.

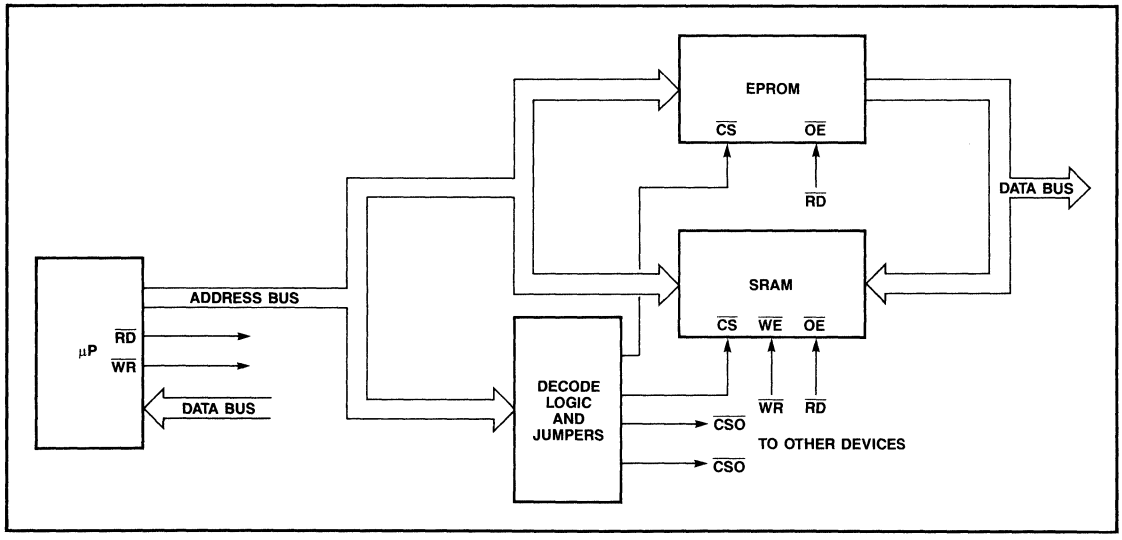


Figure 1. General Architecture — Discrete Solution

Regardless of the method chosen to implement the decoder, some compromises will be incorporated that affect system performance, board space and cost. Since the decoder is in the memory access path, the total memory access time is the sum of the decoder delay and the access time of the memory. For example, to achieve a 40 ns total access time, a 12 ns decoder can be used with a 25 ns memory allowing 3 ns for on-board interconnect delay (memory products in the 25 ns range are expansive and usually are available in by 1 or by 4 bits wide configuration).

The WSI MAP™ family of mappable memory products has been developed to significantly enhance system performance by integrating (on one chip) high density EPROM for program store, high density SRAM for data store and high performance logic in the form of a Programmable Mapping Decoder (PMD™) (Figure 2). The products are

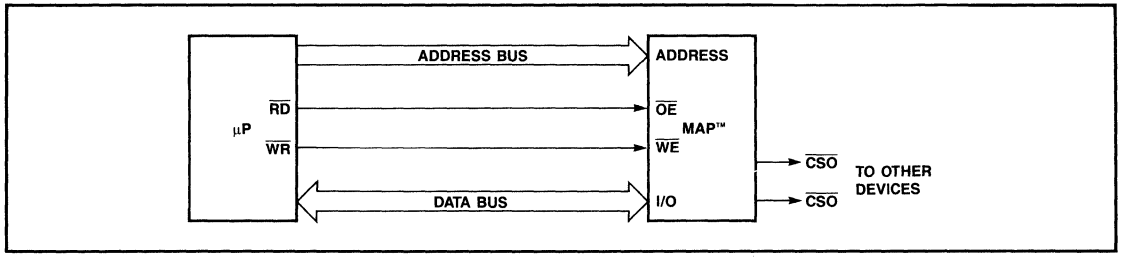


Figure 2. Single-Chip Solution Using Map™ Memory

ideally suited for DSP oriented applications (modems, analog data filtering or analysis, etc.), expansion memories for 8 or 16-bit microprocessors and microcontrollers and applications that are very board space sensitive (i.e., plug-in cards, avionics, portable systems, etc.).

The EPROM is based on WSI's patented split gate EPROM technology for high density and very high speed. The first generation of MAP™ products from WSI (WSMAP162/161, WSMAP168) contains a 128K bit UV erasable 40 ns EPROM. This EPROM can be organized in the bytewide configuration as 16K × 8 and in the wordwide configuration as 8K × 16.

The SRAM is based on the industry standard full CMOS 6-transistor cell. The advantages of this cell are high speed, very low stand-by power, high noise immunity and good data retention when disturbed by alpha particles. In the first MAP™ generation of products, the SRAM contains 32K bits which can be configured as 4K × 8 in the byte mode or 2K × 16 in the wordwide mode.

MAP™ MEMORY ARCHITECTURE

The memory is structured as a series of blocks to achieve a very flexible and highly configurable circuit for general purpose applications (Figure 3). The EPROM is subdivided into 8 blocks and the SRAM is subdivided into 2 blocks. These memory blocks can be considered as separate memories with dedicated internal chip selects. The on-board Programmable Mapping Decoder (PMD™) selects the appropriate block based on the incoming address. This architecture enables the product to be configured and compatible with virtually any system address map. Complicated address maps of microcontroller systems can be fully utilized by programming blocks of EPROM and SRAM to be addressed by the various portions of the system address map.

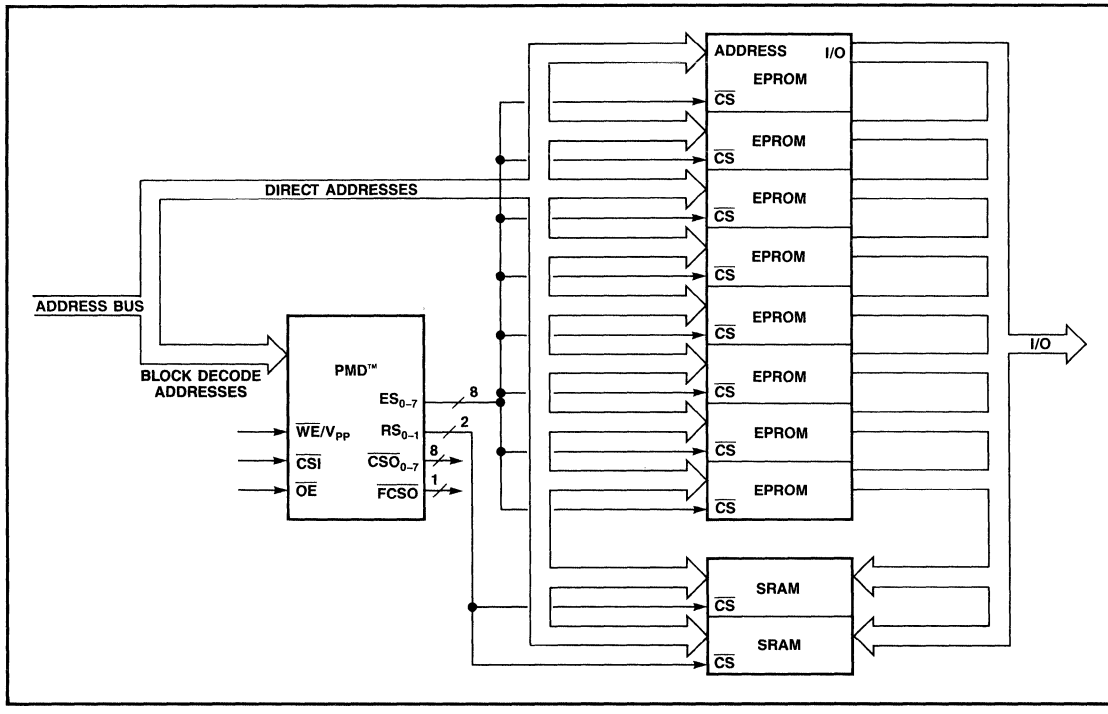


Figure 3. Map™ Memory Architecture

In addition to having fine control of memory allocation, it is now easier to make software updates which require changes in the address map boundaries. This can be accomplished by simply reprogramming the PMD™ when the EPROM code is altered. Now only one part is needed to be sent to the customer to accommodate field software changes, a user-transparent method that requires no change of PC board jumpers.

THE PROGRAMMABLE MAPPING DECODER (PMD™)

The PMD™ actually performs as an address comparator. When the address that was previously programmed into the PMD™ is detected, the PMD™ enables the internal "Chip Select" to the memory block that is selected by that address. If no block is selected by the address, both the EPROM and SRAM are powered down and the outputs are disabled (the SRAM retains its data). This enables other devices to drive the data bus. In addition to selecting internal blocks of memory, the PMD™ can also be programmed to select other devices using the Chip Select Outputs. The CSOs are programmable in the same block resolution as the internal memory. However, a CSO can be active for any number of blocks in the address space, i.e., it is possible to enable another external 128K byte memory by programming a single CSO to be active for that entire address range.

The PMD™ is implemented similar to a PAL® device. All the block decode addresses are connected to the AND plane. There is only one output per AND gate (there is no OR plane). Each AND gate output either selects a block of internal memory or, in the case of Chip Select Outputs ($\overline{CSO_{0-7}}$), can select a number of blocks of external memory. Addresses A_{11}–A_{20} are block decode addresses. EPROM select outputs ES_0–ES_7 (ES outputs) select 1 of 8 available EPROM blocks. SRAM select outputs RS_0–RS_1 (RS outputs) select one out of 2 available SRAM blocks. For a particular address, the selection of one memory block from ES_0–ES_7 or one from RS_0–RS_1 is allowed but not both. That is, only the EPROM or SRAM can be active at a particular time. The CSOs are independent of the ES and RS outputs. Any one address can be programmed to select one or more of the CSOs even if one of the ES or RS outputs is selected. This is particularly useful for I/O control or wait state generation address decode.

The PMD™ is implemented with UV erasable EPROM cell-based "fuses". After UV erase or with new parts, the EPROM cells are normally connected between the address inputs and the select outputs. The EPROM cells are disconnected by selective programming. For a select output to be enabled, all the "true" addresses must be disconnected. For example, for selection if the address contains $A_{11} = 0$, $\overline{A_{11}}$ must be disconnected and if the address contains $A_{12} = 1$, A_{12} must be disconnected (Figure 4). For ES and RS select outputs, it is possible to not select any combination by not disconnecting any of the addresses. The case when an address and its complement are not disconnected is termed "hard deselect".

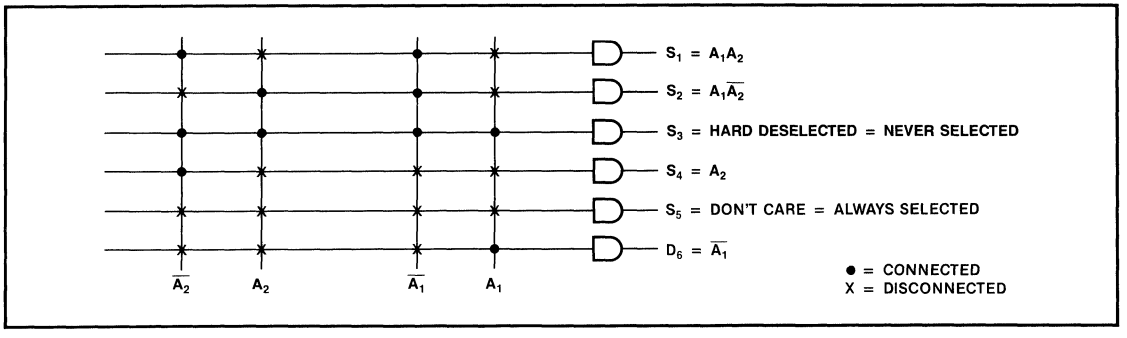


Figure 4. PMD™ Programming Examples

CHIP SELECT OUTPUTS (CSO)

For CSOs, it is possible to make an address line a "don't care" by deselecting both the true and the complement of that address (Figure 5). This enables the CSO to be active for more than one address combination. Thus, a group of blocks of external memory can be selected with only one CSO. A CSO can be programmed to function as a configuration bit which is always deselected (i.e., $\overline{CSO_0}$ = "1") or always selected (i.e., $\overline{CSO_0}$ = "0") by programming the addresses with "hard deselect" or with the "don't care" patterns respectively. This is similar in function to a PC board wire jumper. Unused CSOs should be programmed with all addresses "don't care" to eliminate switching and reduce power consumption.

Since the PMD™ is always powered up, $\overline{CSO}$s are always active (depending on the PMD™ configuration).

10

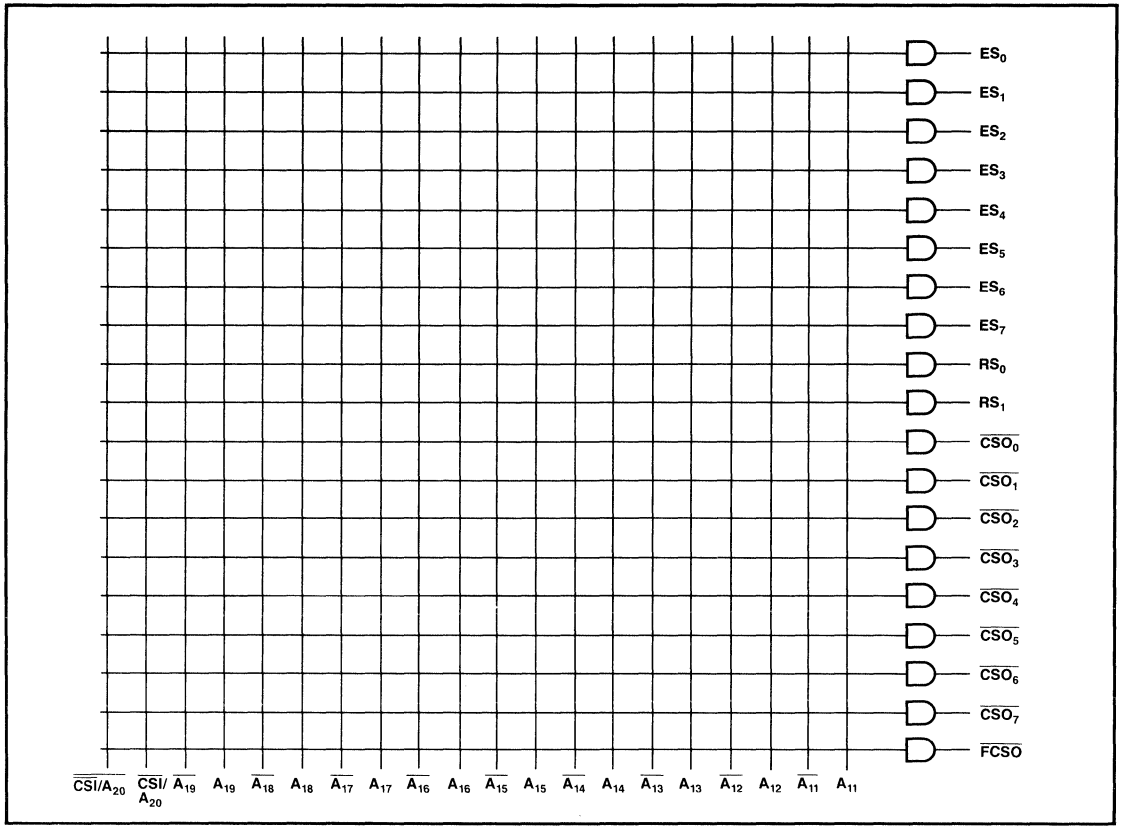


Figure 5. PMD Array Architecture

POWER DISSIPATION

Power dissipation on the chip is managed by selectively powering up either the EPROM or SRAM. If the EPROM is selected, it will draw power while the SRAM stays powered down and vice versa. When neither the EPROM or the SRAM is selected, both are powered down. Even though the SRAM is in a "powered down" mode, its data stays intact. A Chip Select Input ($\overline{CSI}$) is provided for a very low power quiescent mode. With $\overline{CSI}$ = "1", the EPROM and SRAM are powered down but the PMD™ is powered up (independent of the incoming address signals). The $\overline{CSI}$ input can be connected to a system power down signal if such signal exists. Otherwise, to save power in the stand-by mode, it is possible to address a location in memory that does not select either the EPROM or the SRAM. In this case, only the PMD™ is powered up and will draw only a small fraction of the active power.

The $\overline{CSI}/A_X$ input is a dual function pin. It is always an address (MSB) input. Optionally, it can be programmed to be a chip select input as well which enables the EPROM and SRAM memory when active low. In a system application, usually one or the other modes is employed but rarely both even though it is possible to employ both modes simultaneously.

SECURITY

The PMD™ is programmed through the circuit's address and I/O pins. When entering the PMD™ programming mode, the contents of the PMD™ can be addressed and accessed through the I/O pins. After programming is completed, it is possible to isolate the PMD's™ programmed configuration by programming the security (SEC) bit. The security bit, when programmed, disables external access to the PMD™ and ensures that the part can not be copied. To further aid in securing data in the MAP™ product, it is suggested that memory blocks that are addressed in a certain order be placed in a different order in the PMD™. The security bit will be erased during UV erase.

SYSTEM APPLICATIONS

The MAP™ family of products is designed to reduce memory access time and board area utilization in high performance digital signal processor and microcontroller and microprocessor systems. These systems typically have the following requirements:

- 16-bit data path (e.g., Motorola 68000/68020, Intel 8096/8086/80286 Processors or National HPC16000 microcontrollers and T.I. TMS32020/TMS320C25 DSP circuits).
- 64K–1 Meg address space
- Fast access time (100 ns to 40 ns)
- Need decoding for I/O and memory
- Printed circuit board area limitations
- Need a mix of memory
  - — Program store: 128K bits EPROM
  - — Data store: 32K bits SRAM

Figure 6 illustrates a typical system based upon a 40 MHz TMS320C25 digital signal processor. Such a system allows only 40 ns for memory access time. The access time can be broken down into decoding time and memory access time. The fastest decoders available today require approximately 10 ns to complete their decode function. Due to this decoding time, memory access time for both the EPROM and SRAM must be 30 ns or less. The MAP™ family of products performs decoding on-board the chip with no speed penalty. As a result, in the above example, a 40 ns MAP™ product would perform the function of a 10 ns decoder and a 30 ns EPROM and SRAM memory. In addition, the equivalent of two fast EPROMs, two fast SRAMs and at least one decoder are combined into one MAP™ product resulting in a 5 to 1 component count reduction.

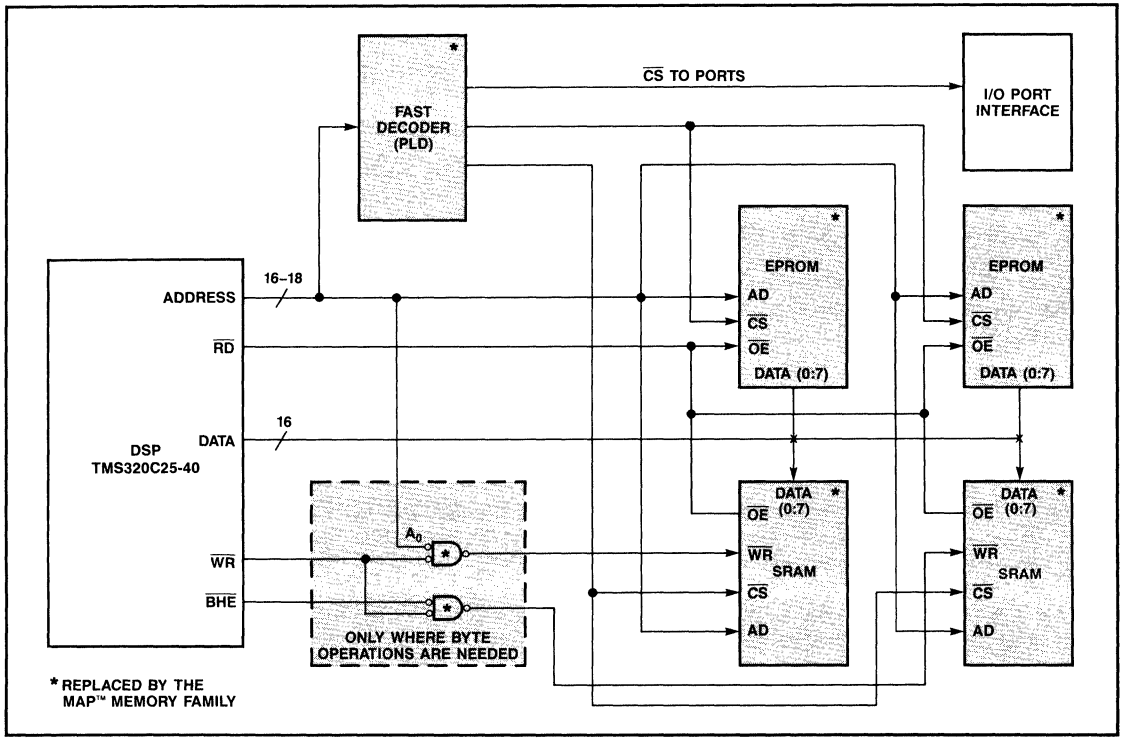
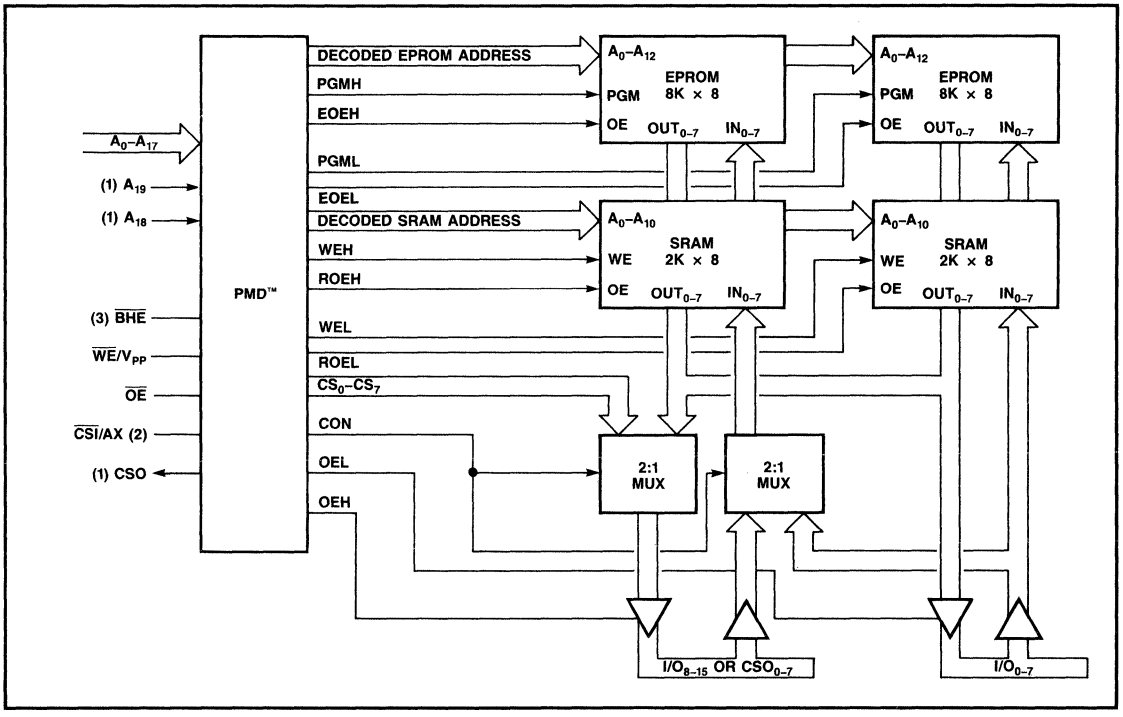


Figure 6. General Block Diagram of a DSP System

The general architecture of the first release of the MAP™ product line is shown in Figure 7. The family consists of three products. They are the WSMAP162, the WSMAP161 and the WSMAP168. The memory consists of 128K bits of EPROM and 32K bits of SRAM. A fast Programmable Memory Decoder (PMD™) is used on-board the circuit to map and access different EPROM and SRAM sections depending on the address inputs. The EPROM and SRAM can be partitioned into blocks of 1K 16-bit words or 2K 8-bit bytes depending on the user programmed configuration of the product.



Notes:
1. WSMAP168 Pins
2. WSMAP162 $A_X = A_{18}$
   WSMAP161 $A_X = A_{17}$
3. Only WSMAP168, WSMAP161

Figure 7. General Architecture of the MAP™ Products

Any of the three products can be programmed to operate in a bytewide or wordwide configuration. The internal memory is organized as 8K × 16 EPROM and 2K × 16 SRAM in the wordwide mode and 16K × 8 EPROM and 4K × 8 SRAM in the bytewide mode. When configured for byte operations, I/O_8 to I/O_{15} become outputs ($\overline{CSO_0}$ to $\overline{CSO_7}$) that can be programmed to select other devices in the system.

The Chip Select Input ($\overline{CSI}$) on each product can be programmed to select the chip or to be an additional (highest) address input. On the WSMAP162 it can be $\overline{CSI}$ or A_{18}; on the WSMAP161, $\overline{CSI}$ or A_{17}; and on the WSMAP168, $\overline{CSI}$ or A_{20}. Table 1 summarizes the programmable options.

Table 1. Programmable Features of the MAP™ Family

	WSMAP162	WSMAP161	WSMAP168
×8 or ×16	Yes	Yes	Yes
$\overline{CSI}$ or Address	$\overline{CSI}/A_{18}$	$\overline{CSI}/A_{17}$	$\overline{CSI}/A_{20}$
Programmable Decoder	Yes	Yes	Yes
Security Mode	Yes	Yes	Yes

SYSTEM INTERFACE TO WSMAP162

The WSMAP162 is especially suited for high-speed word-oriented (no byte operations) microprocessors. The TMS320C20/25 DSP family is an example of such a microprocessor. Figures 9 and 10 show two options of interfacing the WSMAP162 to a TMS320C25 operating at 40 MHz with no wait states. The TMS320C25 has two pins for selecting Program Memory ($\overline{PS}$) and Data Memory ($\overline{DS}$). These functions are connected to the higher order address of the WSMAP162. $\overline{PS}$ is connected to A_{18} and $\overline{DS}$ is connected to A_{17}. Usually $\overline{PS}$ will select the EPROM and $\overline{DS}$ will select the SRAM. See Figure 8.

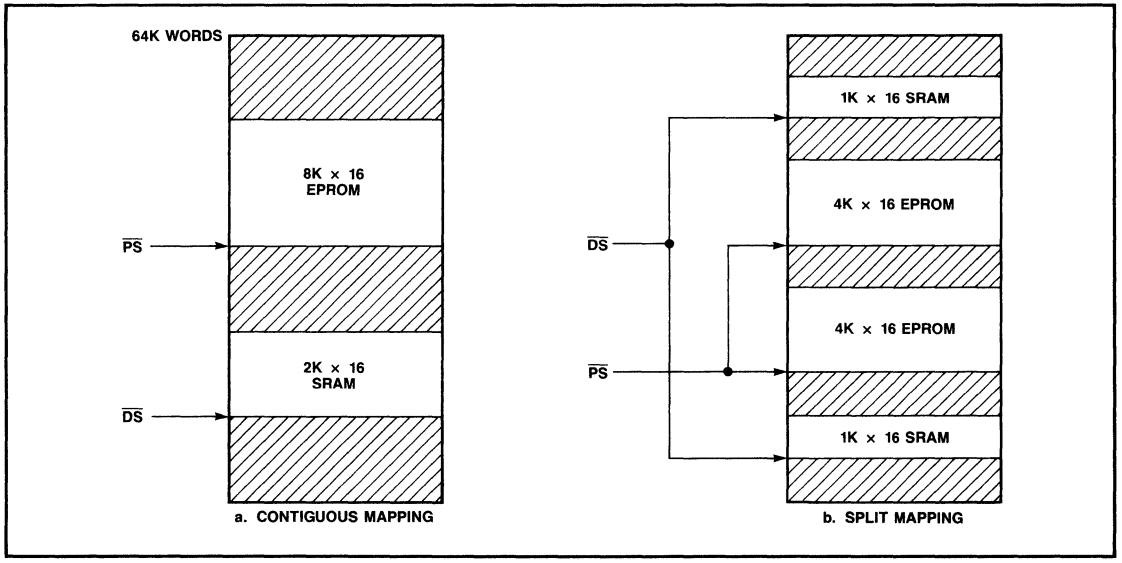


Figure 8. Examples of Mapping Memory Using the WSMAP162

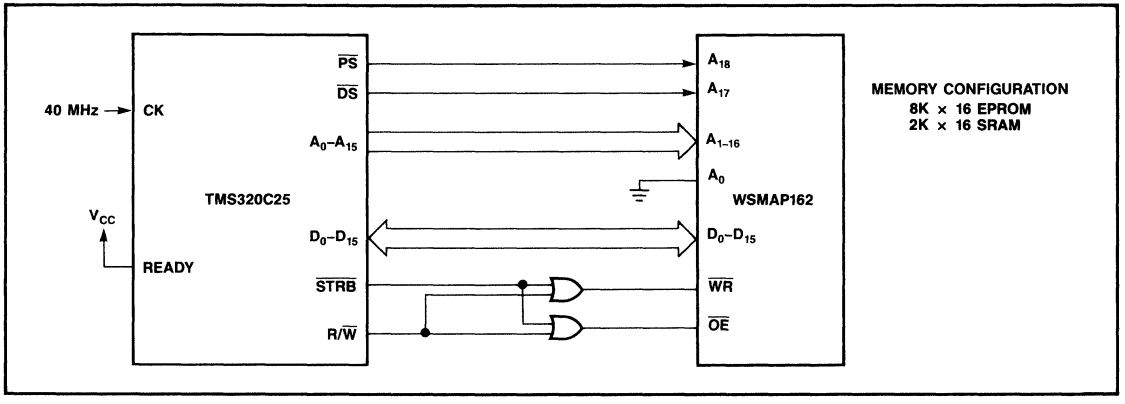


Figure 9. Interfacing the WSMAP162 to a TMS320C25 in a DSP Application (×16 Configuration)

When in a wordwide (×16) configuration, the total memory available on the WSMAP162 is 8K × 16 of EPROM and 2K × 16 of SRAM. See Figure 9. This implementation replaces a minimum of:

- one high-speed decoder (10 ns)
- two 8K × 8 EPROMs (30 ns)
- two 2K × 8 SRAMs (30 ns)

or a total of 5 circuits. If the system was previously implemented using a boot EPROM, the WSMAP162 replaces:

- one high-speed decoder (10 ns)
- two 8K × 8 EPROMs (30 ns)
- two 2K × 8 SRAMs (30 ns)
- two 8K × 8 slow EPROMs
- three ICs for Wait-State generation

or a total of 10 circuits.

In a byte wide (×8) configuration, two WSMAP162s can be interfaced directly with a TMS320C25. See Figure 10. Key features of this system are:

- 40 ns access time
- 16K × 16 EPROM
- 4K × 16 EPROM
- 16 general purpose programmable chip selects

The general purpose programmable chip selects can be mapped to any location in the address space via the PMD™. These chip selects can be used to access I/O ports, select additional memory or control other system functions.

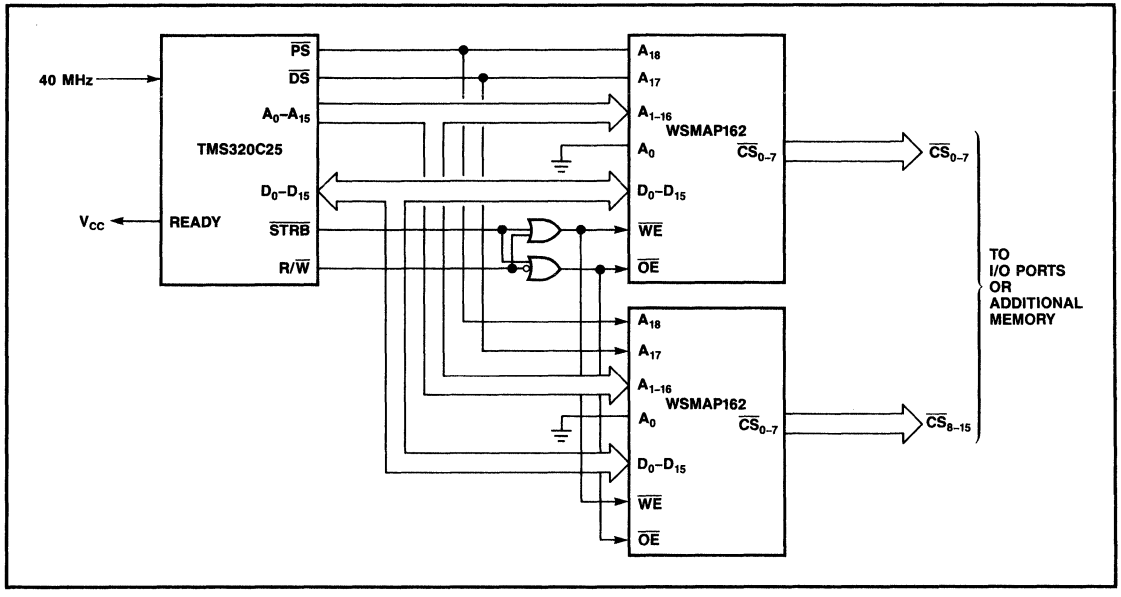


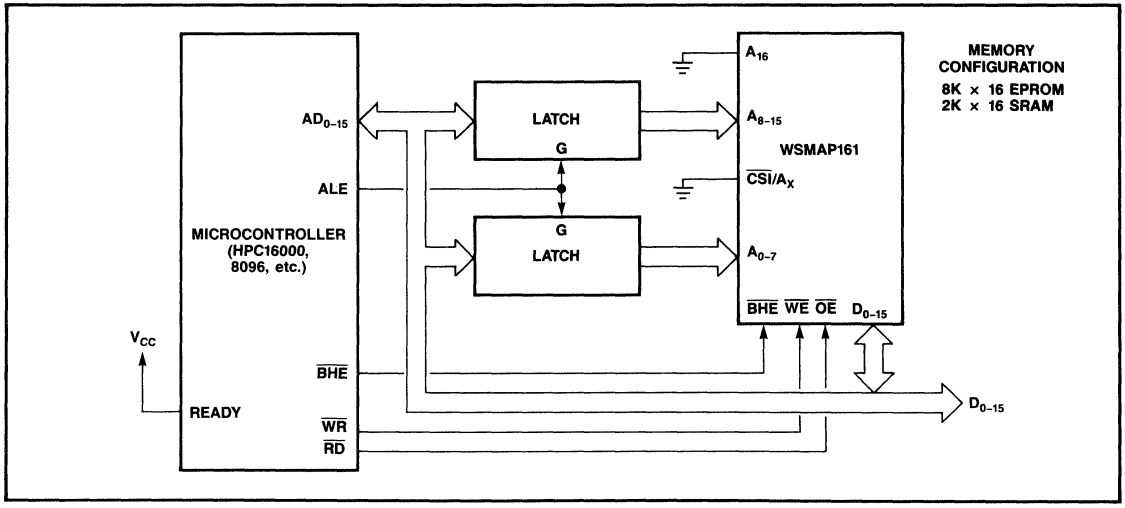
Figure 10. WSMAP162 in a ×8 Configuration

SYSTEM INTERFACE TO WSMAP161

The WSMAP161 has two basic configurations. They are a wordwide (×16) configuration with byte operation capability and a byte wide (×8) configuration with 8 chip select outputs (for byte wide only applications, it is suggested to use the WSMAP162 as the inclusion of A_{17} instead of $\overline{BHE}$ gives greater addressing range).

The 128K address space (during byte operations in the wordwide mode) makes the WSMAP161 especially suited for microcontroller applications. Figure 11 illustrates a simple interconnection of the WSMAP161 to a microcontroller. In the HPC16040 without wait states, the access time is 65 ns which makes the WSMAP161 (40 ns access time) a good fit with plenty of margin. See Figure 11.

The WSMAP161 can be configured in a bytewide (×8) mode. This is equivalent to the WSMAP162 and can also be used "doubled-up" as shown in Figure 10.



Note: In an HPC16040, the access time is 63 nsec.

Figure 11. Interfacing the WSMAP161 to a Microcontroller (×16 Configuration)

SYSTEM INTERFACE TO WSMAP168

The WSMAP168 has the following key features:

- 1 Meg address space decoding
- 40 ns access time
- Byte operations in wordwide mode ($\overline{BHE}$)
- One output chip select when in the wordwide mode ($\overline{FCSO}$)
- Nine output chip selects when in the bytewide mode
- Programmable Mapping Decoder (PMD™)

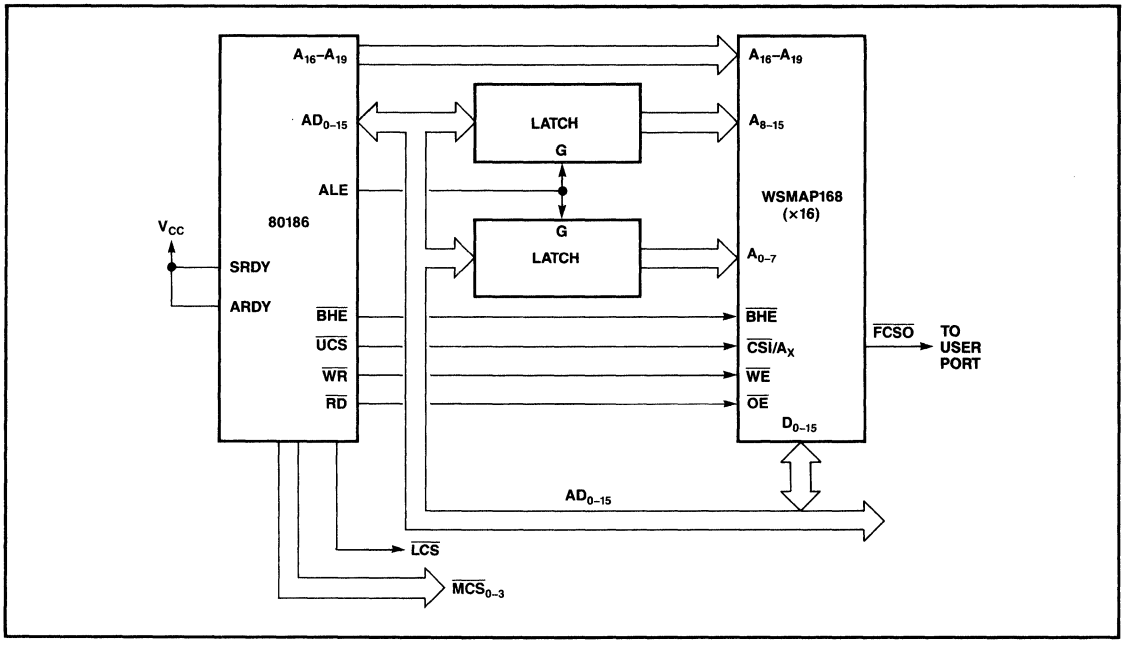


Figure 12. Interfacing the WSMAP168 to an 80186 in an Embedded Control Application (×16 Configuration)

10

Figure 12 illustrates the interface between an 80186 and the WSMAP168 (in the ×16 mode). The $\overline{UCS}$ (Upper Chip Select) is connected to $\overline{CSI}/A_X$ on the WSMAP168. The PMD™ is programmed to locate a 1K × 16 EPROM slot in the upper memory address space for a reset subroutine. The rest of the memory can be located as required by the user (Figure 13).

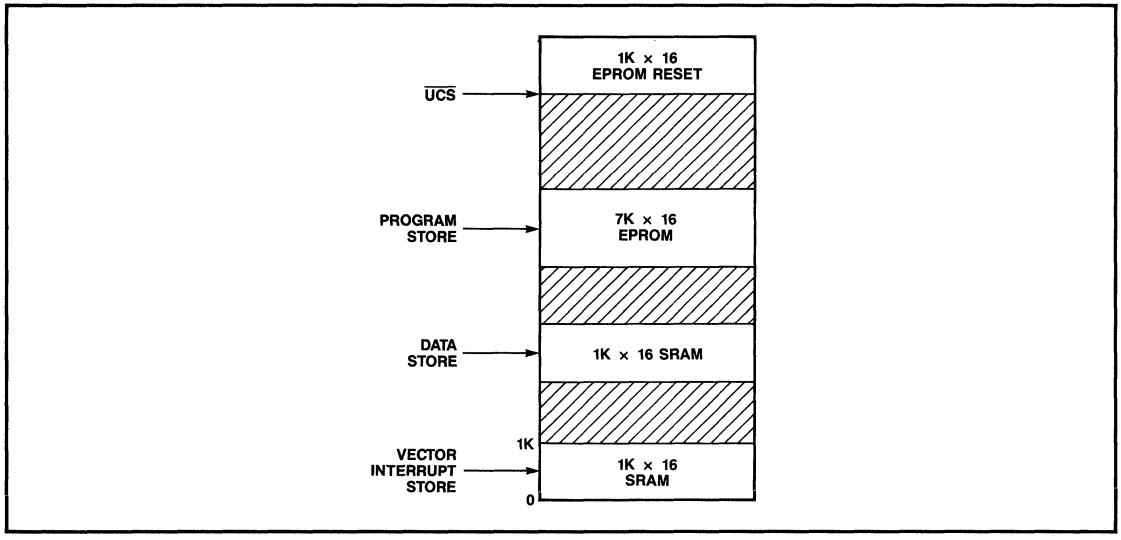


Figure 13. Optional Memory Mapping Using a WSMAP168 in an 80186 System

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WSI provides the programming environment needed to program the MAP™ family of products. The MagicPro™ and the MAP™ Utility provides the user with the ability to program the PMD™ and the EPROM. The menu-driven software and hardware use the IBM PC as a platform and are easily installed and used. For additional information, consult your nearest WSI sales representative.

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