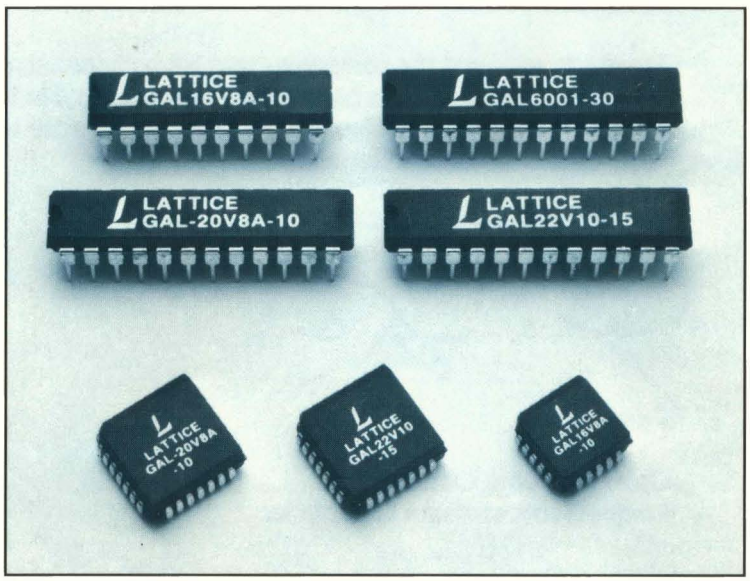
Lattice Semiconductor Corporation™

GAL® Data Book



High Performance E²CMOS™ PLDs

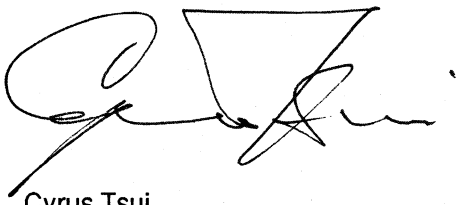
1989

In 1984, Lattice Semiconductor Corporation designed the world's first electrically erasable CMOS PLD, the GAL16V8. Five years later, Lattice is the largest volume supplier of CMOS Programmable Logic Devices.

Today, the GAL concept is being embraced by the largest PLD manufacturers in the world. These companies have recognized the benefits of GAL devices and are producing E²CMOS PLDs based on the GAL technology that Lattice pioneered. We welcome these companies into the high-speed CMOS marketplace. Their acceptance of Lattice's technology is a powerful endorsement of our efforts to develop what we believe is the best PLD.

In the future, Lattice will continue to supply our customers with the fastest, most innovative CMOS PLDs on the market. In 1989, we introduced the GAL16V8A-10 (10ns t_{PD}, 62.5 MHz) and the GAL22V10 (15ns t_{PD}, 50 MHz). These high-speed CMOS devices are in full production and provide the speed, power savings, and quality levels that our customers demand.

Thanks to you, and the companies that have chosen to second source GAL devices, Lattice's E²CMOS technology has become the new standard in the PLD marketplace. We look forward to helping you solve your system performance requirements and hope you find the 1989 GAL Data Book informative.

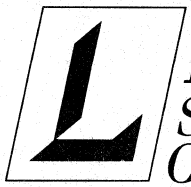


Cyrus Tsui

Chief Executive Officer
Lattice Semiconductor Corporation

GAL® Data Book

1989



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Lattice Semiconductor Corporation™

GAL PRODUCT INDEX

DEVICE	PINS	t_{PD} (ns)	I_{CC} (mA)	DESCRIPTION	PAGE
GAL16V8A	20	10, 12, 15, 25	55, 115	E²CMOS Generic PLD	9
GAL16V8	20	15, 20, 25	45, 90	E²CMOS Generic PLD	41
GAL20V8A	24	10, 12, 15, 25	55, 115	E²CMOS Generic PLD	9
GAL20V8	24	15, 20, 25	45, 90	E²CMOS Generic PLD	41
GAL22V10	24	15, 25	130	E²CMOS Generic PLD	59
GAL6001	24	30	150	E²CMOS FPLA	77
ispGAL16Z8	24	20, 25	90	E²CMOS In-System-Programmable PLD	91

Note: Specifications (t_{PD} and I_{CC}) listed above are for Commercial temperature range devices. See datasheets for Military and Industrial temperature range device specifications.

Introduction to Generic Array Logic

INTRODUCTION

Lattice Semiconductor, located in Hillsboro, Oregon, was founded in 1983 to design, develop and manufacture high-performance semiconductor components. It is a firm belief at Lattice that technological evolution can be accelerated through the continued development of higher-speed and architecturally superior products. This belief led to a decision to enter the programmable logic marketplace by developing the ideal product line: the GAL® (Generic Array Logic) family of devices.

GAL devices are ideal for four important reasons:

1. GAL devices are fabricated using very high-speed Electrically Erasable CMOS (E^2CMOS™), which offers the highest degree of testability and quality of any process technology, as well as instant erasability, making GAL devices ideal for prototyping and manufacturing.

2. GAL devices can directly replace PAL devices in nearly every application.

3. GAL devices have the low power consumption of CMOS, one-fourth to one-half that of bipolar devices.

4. GAL devices utilize Output Logic Macrocells (OLMCs), which allow the user to configure outputs as needed.

By melding all these features into a single product line, the GAL family is ideally targeted to replace TTL/74HC random logic, low-density gate arrays, and all other programmable logic. The GAL family offers the benefits of reduced system cost, product size and power requirements, as well as higher reliability and greatly simplified system design.

THE GAL CONCEPT

E^2CMOS — The Ideal Technology

Of the three major technology approaches available E^2CMOS, UVCMOS, and bipolar, the technology of choice is clearly E^2CMOS—for many reasons, including: testability, quality, high speed, low power, and instant erasure for prototyping and error recovery.

Testability

The biggest advantage of E^2CMOS over competing technologies is its inherent testability. Capitalizing on very fast (50ms) erase times, Lattice is able to pattern and erase all devices many times during manufacture, and to directly test all characteristics including AC, DC and functionality. The result is guaranteed 100% programming and functional yields to the customer—and no further board rework. Competing technologies suffer serious test constraints, as discussed below.

Low Power

Another advantage of this technology is the low power consumption of CMOS. This provides users the immediate benefit of decreased system power requirements allowing for higher-reliability, cooler-running systems, while maintaining high performance. The low power consumption of CMOS also permits circuit designs of much higher functional density, because of lower junction temperatures and power requirements on chip. The user will benefit because higher functional density means further reduction of chip count and smaller boards in the system.

High Speed

Also advantageous is the very high speed attainable with Lattice's state-of-the-art E^2CMOS process — speeds that are at least as fast as any device using any technology, with the exception of ECL circuits.

Prototyping and Error Recovery

Finally, E^2CMOS gives the user instant erasability, with no additional handling, or special packages necessary. This provides ideal products for prototyping because designs can be altered instantly, with no waste and no waiting. On the manufacturing floor, instant erasability can also be a big advantage for dealing with pattern changes or error recovery. If a GAL device is accidentally programmed to the wrong pattern, the recovery process is simple, again with no waiting or waste. Parts are simply put back into a device programmer and repatterned. No other technology can offer this.

A LOOK AT OTHER TECHNOLOGIES

Here, the technologies that compete with E²CMOS—bipolar and UVCMOS—are compared and contrasted with the E²CMOS approach.

Bipolar

Bipolar fuse-link technology was the first available for programmable logic devices. Although it offers high speed, it is saddled with high power dissipation. This not only significantly increases system power supply and cooling requirements it also limits the ability of high functional density.

Another weakness of this technology is the one-time-programmable fuses. Complete testing is impossible and manufacturers must rely on complex schemes using test rows and columns to simulate and correlate their device's performance, since the fuse array cannot be tested prior to programming. The result is programming failures at the customer location, due to incomplete testing. Also, because these devices can only be programmed once, no reuse in the event of mistakes during prototyping or errors on the production floor are possible and any misprogrammed devices must be discarded.

UVCMOS

UVCMOS addresses many of the weaknesses of the bipolar approach, but introduces many shortcomings of its own. This technology requires much lower power and, while it has the capability to erase, this comes at the expense of slower speeds.

Testability is increased over bipolar since the "fuse" array can be programmed and tested by the manufacturer. The problem here is the long (20 minutes) erase times of this technology, coupled with the requirement of exposing the devices to ultraviolet light for erasing. This becomes a very expensive step in the manufacturing process. Because of the time involved, patterning and erasing is performed only once—a compromised, rather than complete functional test.

Additionally, the devices must be housed in expensive windowed packages to allow users to erase them. Again, this erase is coupled with the time-consuming and cumbersome task of shining ultraviolet light on the parts to erase them. As a cost-cutting measure, UVCMOS PLD manufacturers offer their devices in windowless packages, which cannot be completely tested after packaging, since they cannot be erased. Of course, the user cannot erase them either. These factors significantly detract from the desirability of this technology.

THE GAL ADVANTAGE

GAL devices are ideal programmable logic devices because, as the name implies, they are architecturally generic. Lattice has employed the macrocell approach, which allows users to define the architecture and functionality of each output. The key benefit to the user is the freedom from being tied to any specific architecture. This is advantageous at the manufacturing level, as well as the design level.

Design Advantages

Early programmable logic devices gave the user the ability to specify a function, but limited them to specific, predetermined output architectures. Comparing the GAL device with fixed-architecture programmable logic devices is much like comparing these same fixed PLDs with SSI/MSI. The GAL family is the next generation in simplified system design. The user need not bother searching for the architecture that best suits a particular design. Instead, the GAL family's generic architecture lets him configure as he goes.

Manufacturing Advantages

The one-device-does-all approach greatly simplifies manufacturing flow. Inventorying one generic-architecture GAL device type versus having to monitor and maintain many different device types, each with its own architecture, will not only save money but will minimize the paperwork and headaches associated with the latter approach. Manufacturing flow is much smoother, too, because the handling process is greatly simplified. A generic-architecture GAL device also reduces the risk of running out of inventory and halting production, which can be a very expensive nightmare. Reduced chance of obsolete inventory and also easier QA tracking are additional benefits of the generic architecture.

THE IDEAL PACKAGE

Programmable logic devices are ideal for designing today's systems. Lattice Semiconductor believes that the ideal design approach should be supported with the ideal products. It was on this premise that GAL devices were invented. The ideal device—with a generic architecture—fabricated with the ideal process technology, E²CMOS.

Lattice will continue to develop and expand its line of E²CMOS programmable logic devices, bringing higher speeds, more flexibility, and exciting new capabilities such as in-system programmability with our ispGAL® family. This is the Lattice Commitment to programmable logic and to you, our customer.

Lattice Semiconductor Corporation™

DEFINITION OF DATASHEET LEVELS

Datasheet Identification	Product Status	Definition
Advanced	In Design	This datasheet contains advance information and specifications are subject to change without notice.
Preliminary	Sampling or Pre-Production	This datasheet contains preliminary data and supplementary data will be published at a later date. Lattice reserves the right to make changes at any time without notice.
No Identification	Full Production	This datasheet contains final specifications. Lattice reserves the right to make changes at any time without notice.

GAL®16V8A
GAL®20V8A

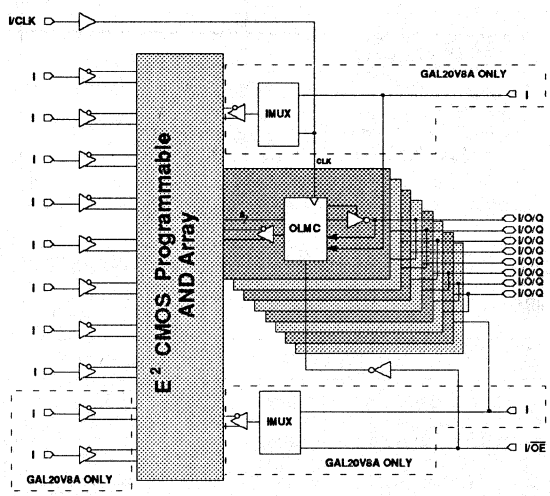
Generic Array Logic™

U.S. Patents 4,761,768 and 4,766,569

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— 10 ns Maximum Propagation Delay**
  - **— Fmax = 62.5 MHz**
  - **— 8 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 24 mA Outputs**
  - **— UltraMOS® III Advanced CMOS Technology**
- **50% REDUCTION IN POWER**
  - **— 75mA Typ I_{cc}**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<50ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— GAL16V8A Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
  - **— GAL20V8A Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

GAL16V8A / GAL20V8A BLOCK DIAGRAM



DESCRIPTION

The GAL16V8A and GAL20V8A, at 10 ns maximum propagation delay time, combine a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL16V8A and GAL20V8A to consume just 75mA typical I_{cc} which represents a 50% savings in power when compared to their bipolar counterparts. The E^2 technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8A and GAL20V8A are capable of emulating standard 20 and 24-pin PAL® devices. The GAL16V8A is capable of emulating standard 20-pin PAL architectures with full function/fuse map/parametric compatibility. The GAL20V8A is capable of emulating standard 24-pin PAL architectures with full function/fuse map/parametric compatibility. On the right is a table listing the PAL architectures that the GAL16V8A and GAL20V8A can replace.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

GAL16V8A / GAL20V8A ARCHITECTURE EMULATION

GAL20V8A PAL Architecture Emulation	GAL16V8A PAL Architecture Emulation
20L8	16L8
20H8	16H8
20R8	16R8
20R6	16R6
20R4	16R4
20P8	16P8
20RP8	16RP8
20RP6	16RP6
20RP4	16RP4
14L8	10L8
16L6	12L6
18L4	14L4
20L2	16L2
14H8	10H8
16H6	12H6
18H4	14H4
20H2	16H2
14P8	10P8
16P6	12P6
18P4	14P4
20P2	16P2

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May 1989

ABSOLUTE MAXIMUM RATINGS(1)

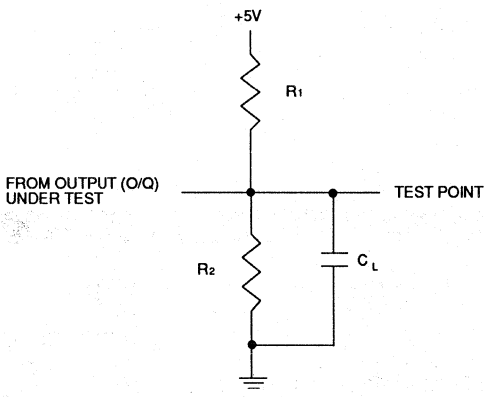
Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

COMMERCIAL DEVICES

Refer to AC Test Conditions:

R_2 = 390Ω

1) R_1 = 200Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 200Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 200Ω C_L = 5pF

MILITARY DEVICES

Refer to AC Test Conditions:

R_2 = 750Ω

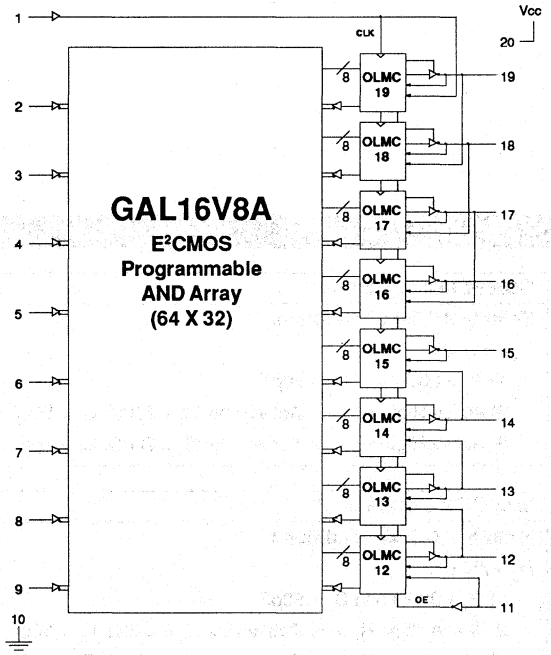
1) R_1 = 390Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 5pF

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

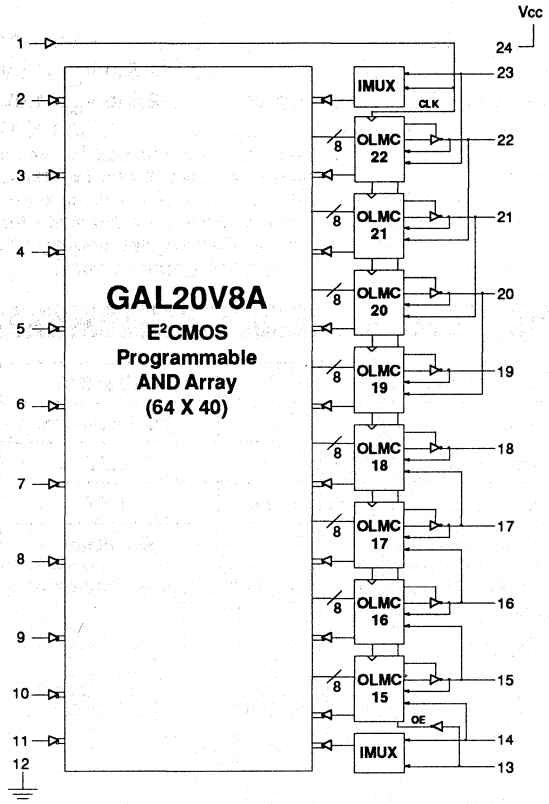
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL16V8A BLOCK DIAGRAM

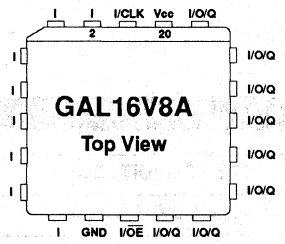


GAL20V8A BLOCK DIAGRAM

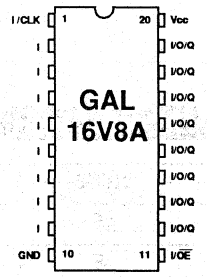


GAL16V8A PIN CONFIGURATION

Chip Carrier

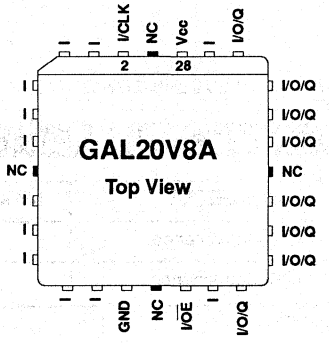


DIP



GAL20V8A PIN CONFIGURATION

Chip Carrier



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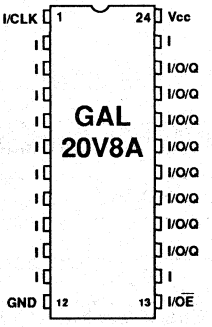

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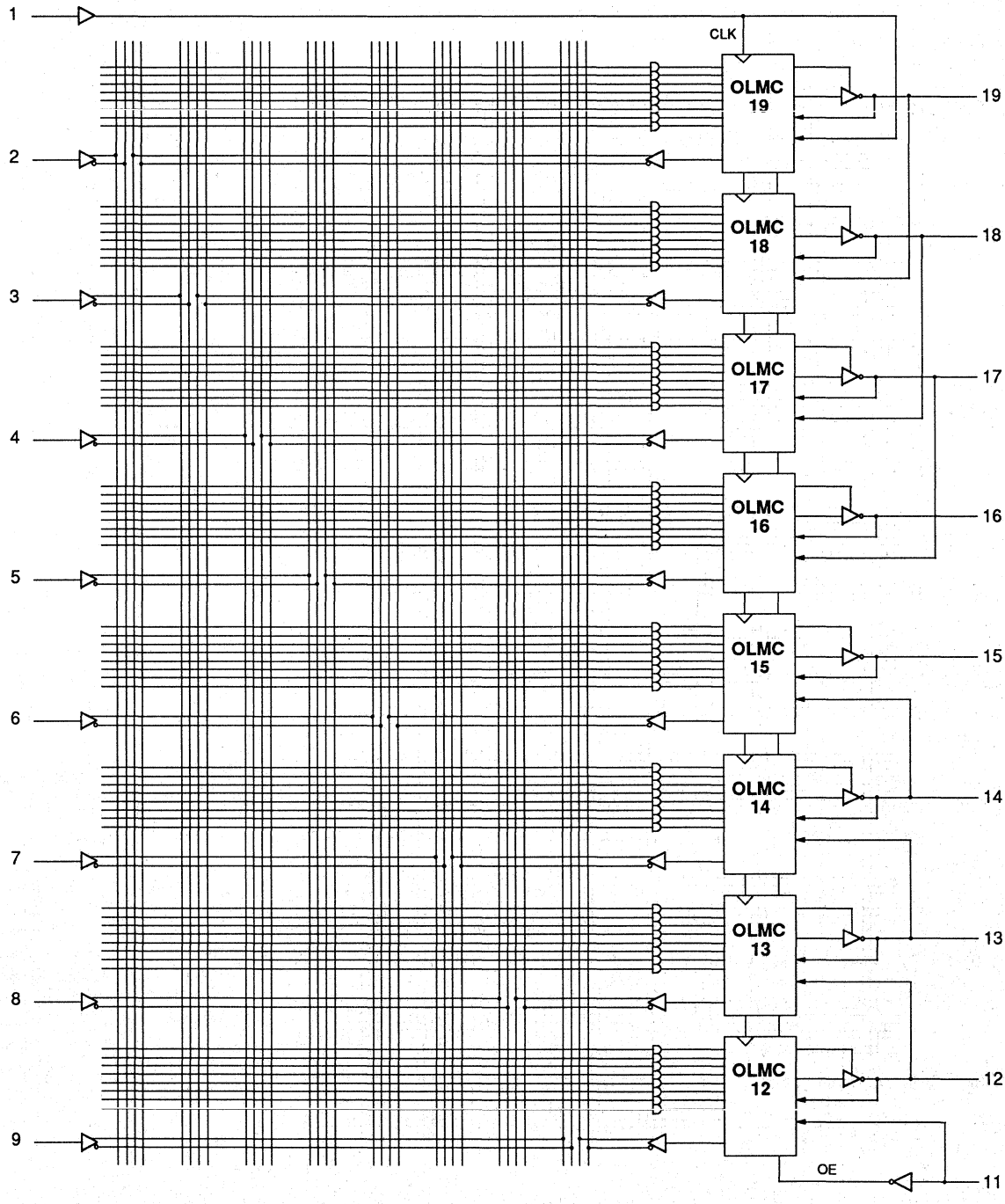
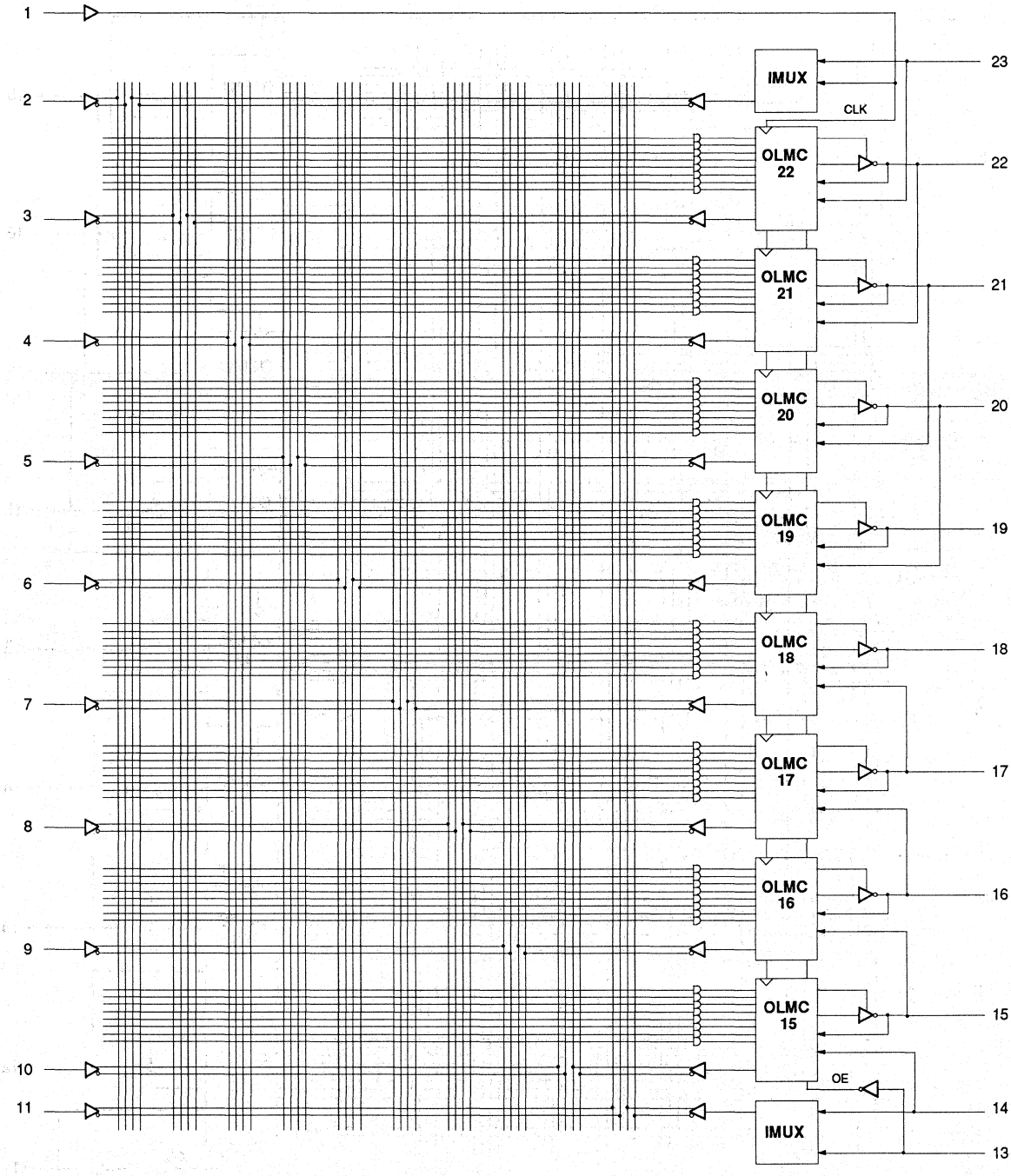
GAL16V8A LOGIC DIAGRAM



GAL20V8A LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-10L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-10L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-10L Commercial

Over Recommended Operating Conditions

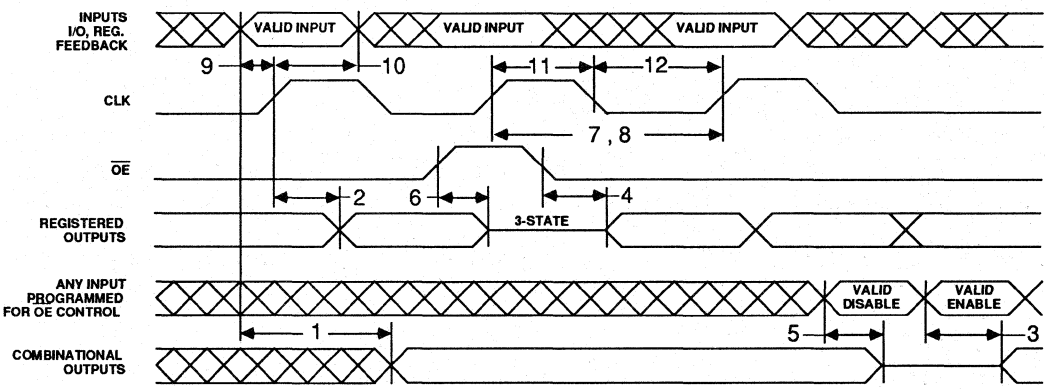
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	10	ns
	2	CLK	Q	Clock to Output Delay	1	2	8	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	10	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	10	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	10	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	10	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-10L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	62.5	MHz
	8	Clock Frequency with Feedback	1	0	55.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	10	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	8	—	ns
	12	Clock Pulse Duration, Low	—	8	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-12L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-12L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-12L Commercial

Over Recommended Operating Conditions

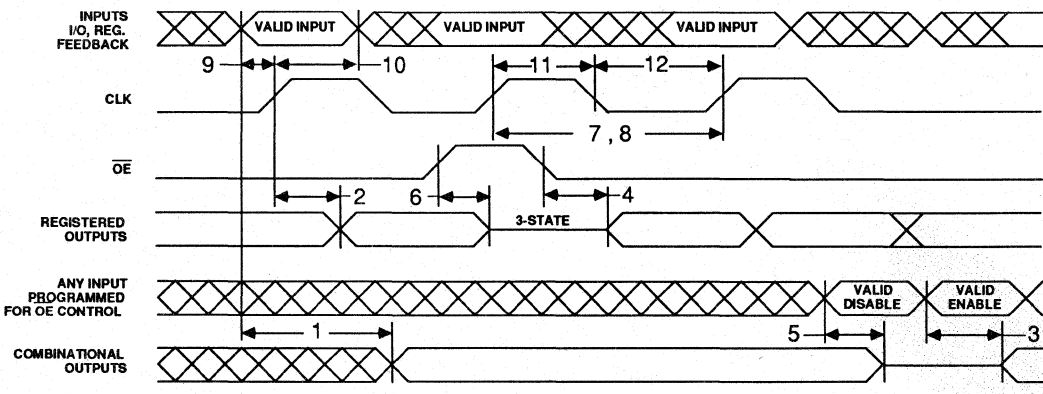
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	12	ns
	2	CLK	Q	Clock to Output Delay	1	2	10	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	12	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	10	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	12	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	10	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-12L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	62.5	MHz
	8	Clock Frequency with Feedback	1	0	50	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	10	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	8	—	ns
	12	Clock Pulse Duration, Low	—	8	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15L Commercial

Over Recommended Operating Conditions

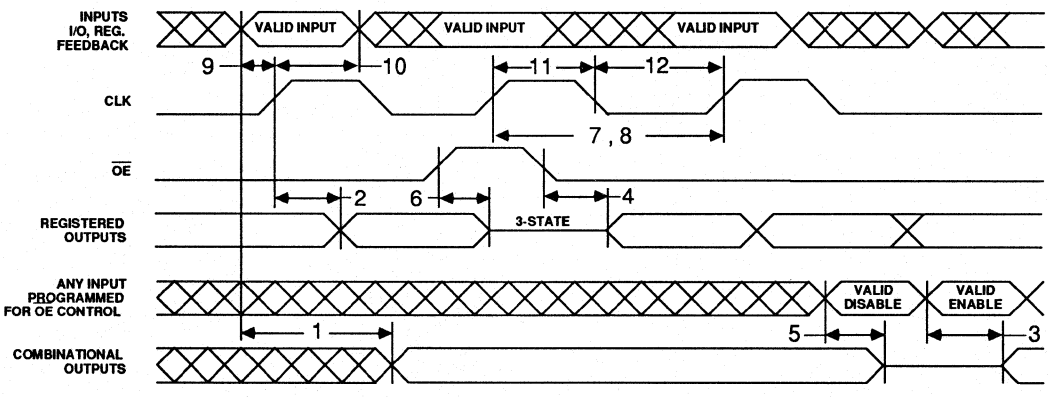
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	50	MHz
	8	Clock Frequency with Feedback	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	10	—	ns
	12	Clock Pulse Duration, Low	—	10	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15Q Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	45	55	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15Q Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15Q Commercial

Over Recommended Operating Conditions

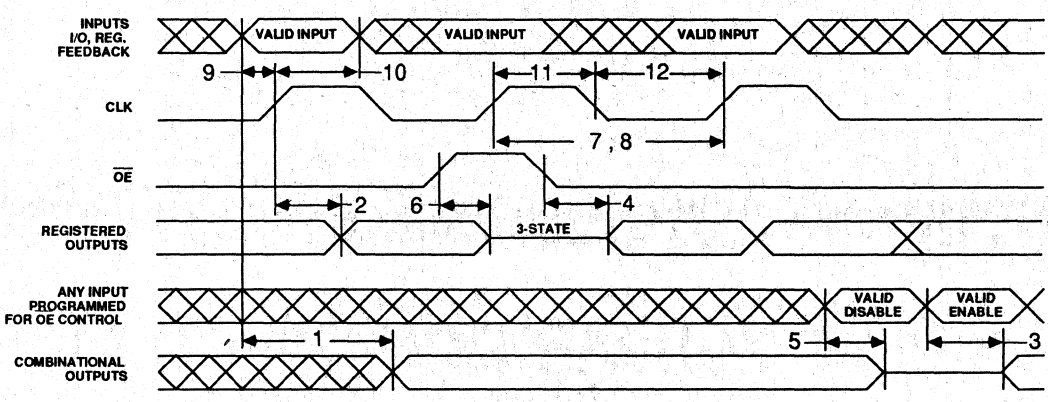
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15Q Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	50	MHz
	8	Clock Frequency with Feedback	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	10	—	ns
	12	Clock Pulse Duration, Low	—	10	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-25L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

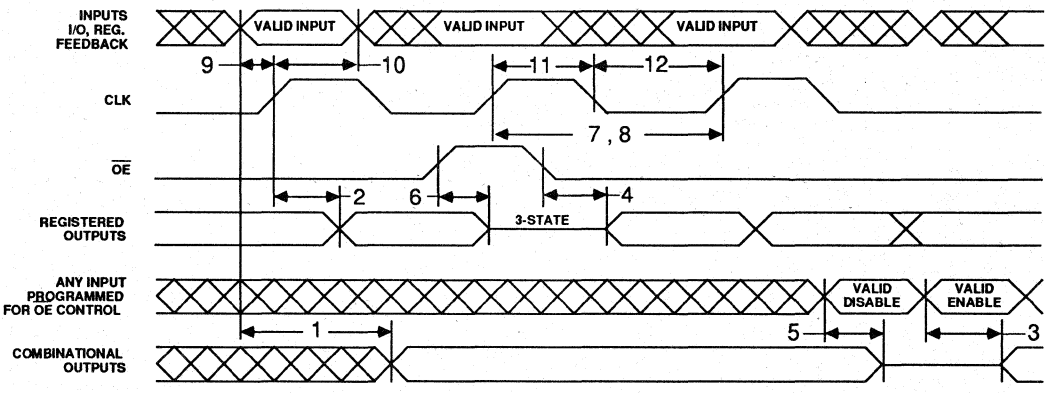
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

2

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15L Industrial

Over Recommended Operating Conditions

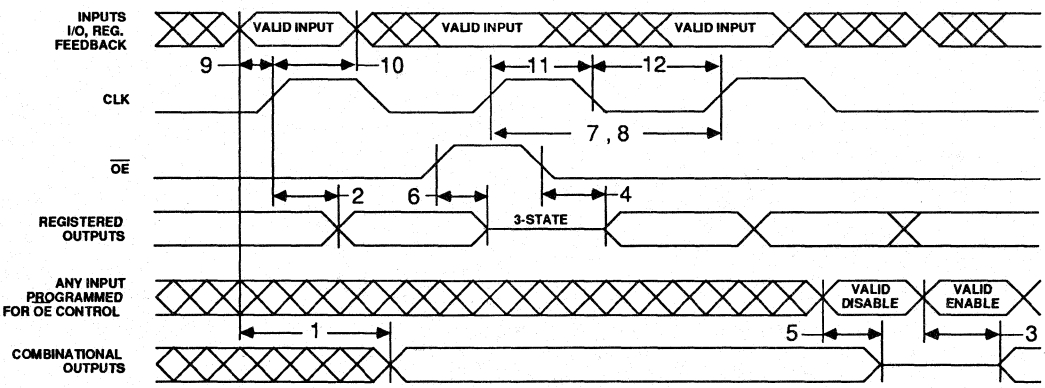
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	50	MHz
	8	Clock Frequency with Feedback	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	10	—	ns
	12	Clock Pulse Duration, Low	—	10	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-20L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

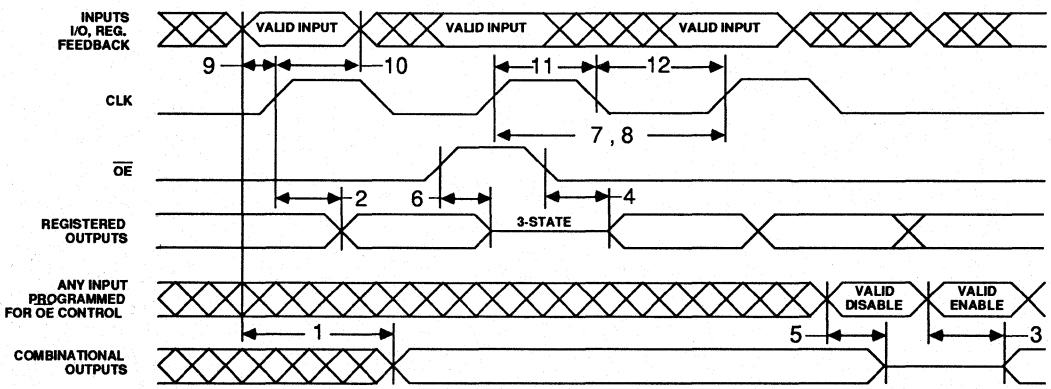
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	41.6	MHz
	8	Clock Frequency with Feedback	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	12	—	ns
	12	Clock Pulse Duration, Low	—	12	—	ns

2

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-25L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-25L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

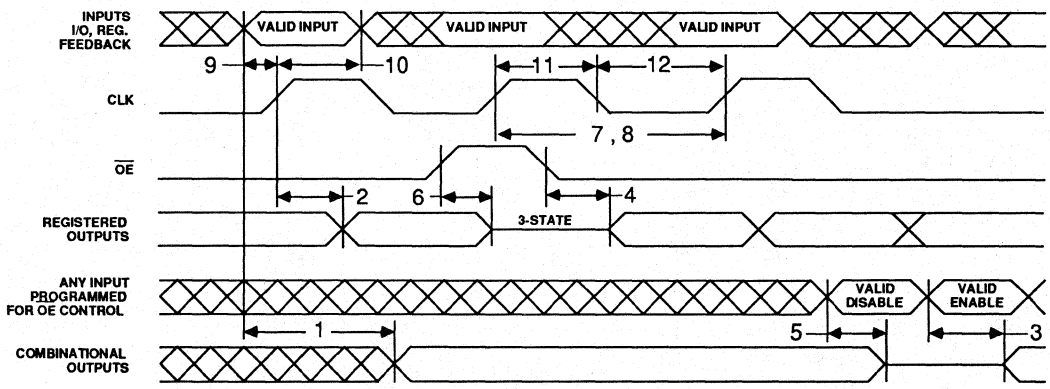
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-25L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

2

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-15L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-15L Military

Over Recommended Operating Conditions

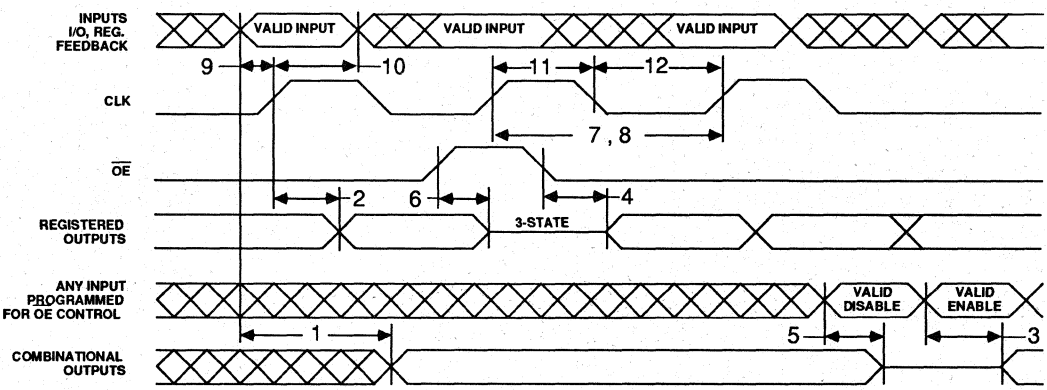
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-15L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	50	MHz
	8	Clock Frequency with Feedback	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	10	—	ns
	12	Clock Pulse Duration, Low	—	10	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-20L Military

Over Recommended Operating Conditions

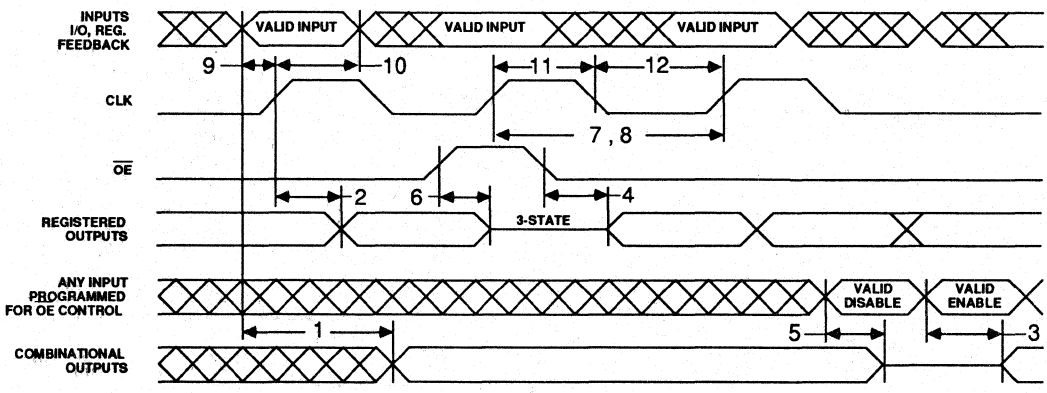
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	41.6	MHz
	8	Clock Frequency with Feedback	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	12	—	ns
	12	Clock Pulse Duration, Low	—	12	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16 / 20V8A-30L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-30L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	– 55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL16 / 20V8A-30L Military

Over Recommended Operating Conditions

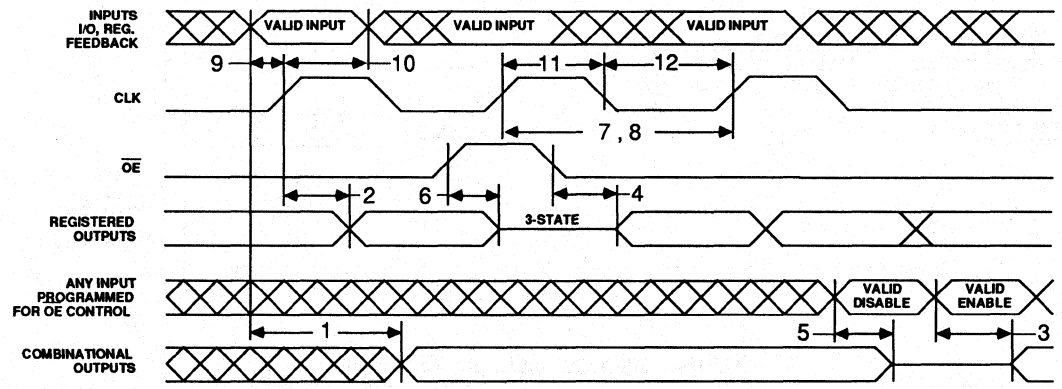
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	30	ns
	2	CLK	Q	Clock to Output Delay	1	2	20	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	30	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	25	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	30	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	25	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16 / 20V8A-30L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	22.2	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	25	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

SWITCHING WAVEFORMS



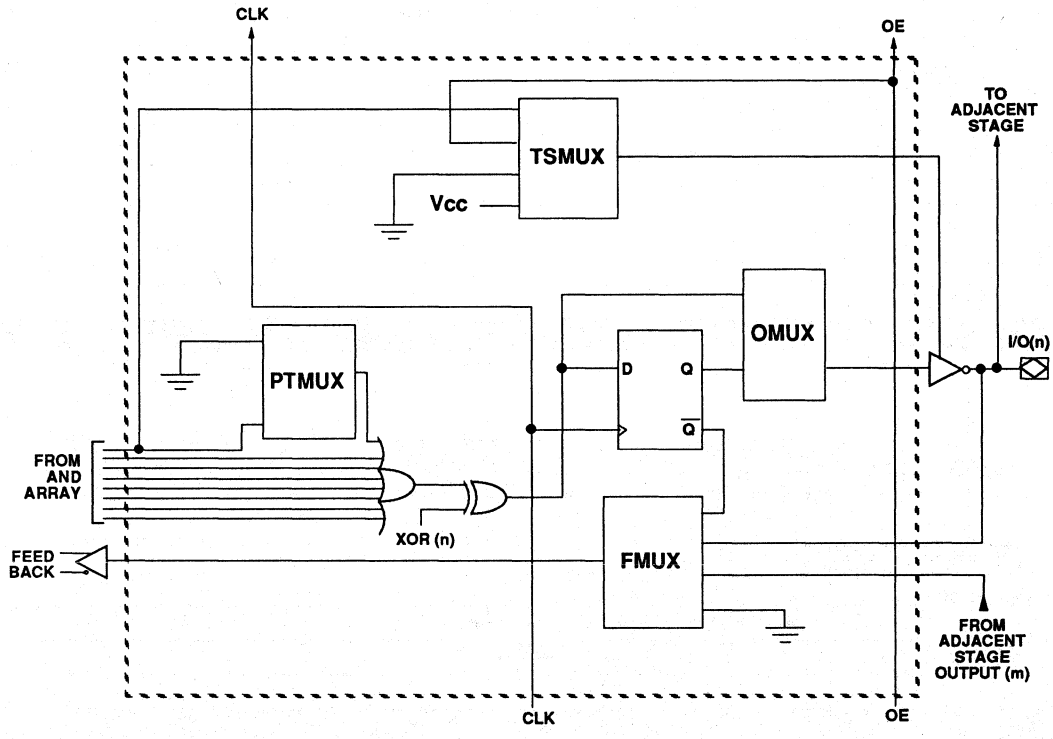
OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the small mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20 and 24-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.



GAL®16 / 20V8A Output Logic Macrocell(n)

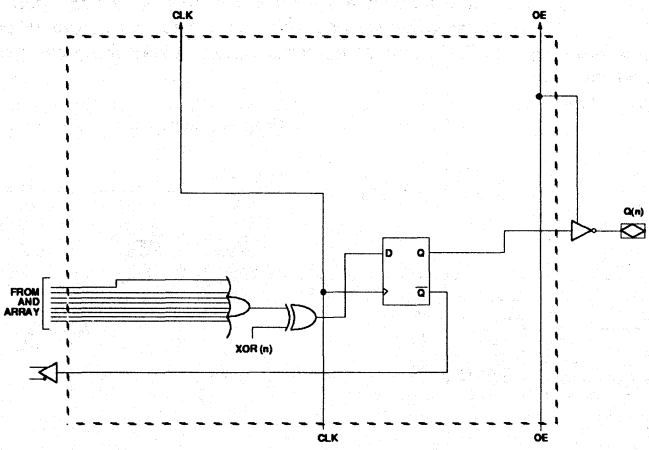
REGISTERED MODE

In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8, 20R6 and 16RP4 devices with various permutations of polarity, I/O and register placement.

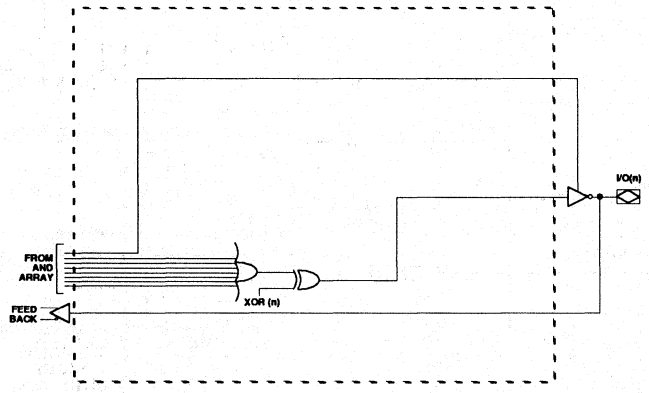
All registered macrocells share common clock and $\overline{OE}$ control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

Registered outputs have 8 data product terms per output. I/O's have 7 data product terms per output.



Registered Output with Programmable Polarity

NOTES:
- All macrocells can be individually configured to this function.
- Polarity of the register input is programmable on a macrocell by macrocell basis.
- Feedback into the AND array is from the $\overline{Q}$ signal of the register with active low and active high feedback paths provided.
- Registered macrocells have common clock (pin 1) and common $\overline{OE}$ (16V8 pin 11, 20V8 pin 13)



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- All macrocells can be individually configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- All macrocells have active high and active low feedback of the output buffer and/or device pin data into the AND array.
- When all 8 macrocells are configured into the I/O function the CLK and $\overline{OE}$ pins serve no valid logic function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

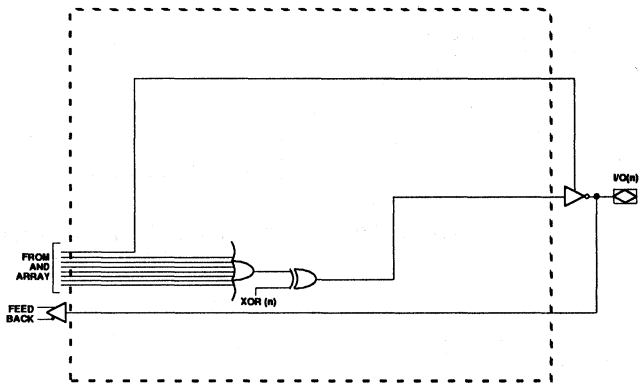
COMPLEX MODE

In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8, 20L8 and 16P8 devices with programmable polarity in each macrocell.

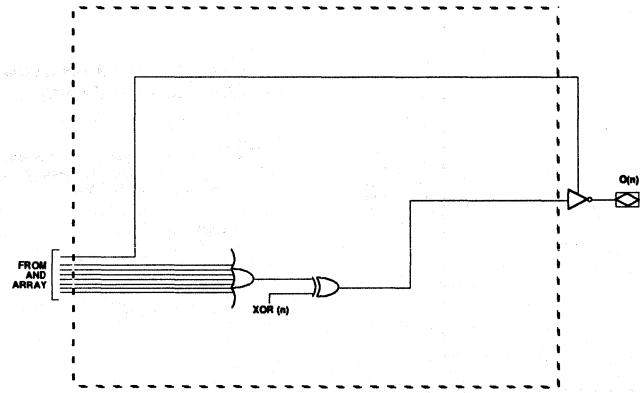
Up to 6 I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 11 on a GAL16V8, and pins 1 and 13 on a GAL20V8, are always available as data inputs into the AND array.



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- The outboard macrocells (16V8 pins 12 & 19, 20V8 pins 15 & 22) cannot perform this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- Each macrocell has active high and active low feedback of the output buffer and/or device pin data into the AND array.



Combinational Output with Programmable OE and Polarity

NOTES:
- The two outboard macrocells (16V8 pins 12 & 19, 20V8 pins 15 & 22) are permanently configured to this function when in the Complex mode.
- The other 6 macrocells can emulate this mode by not using the feedback data as a data input to the array.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

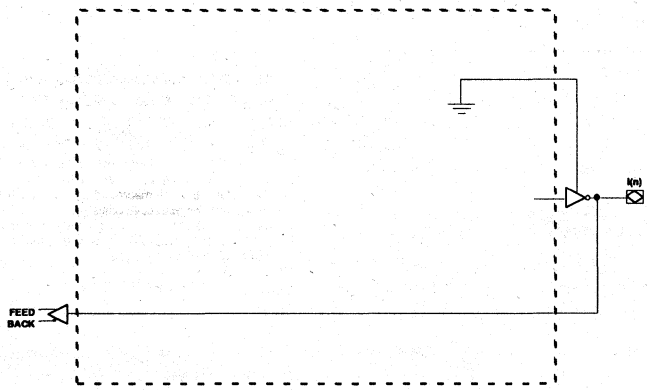
SIMPLE MODE

In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8, 18H4 and 16P6 devices with many permutations of generic polarity output or input choices.

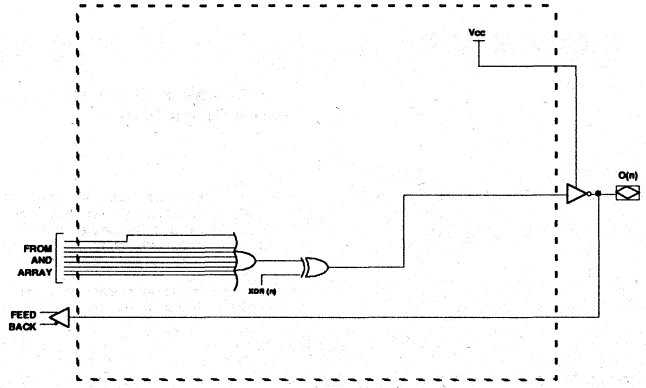
All ouputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 11 on a GAL16V8, and pins 1 and 13 on a GAL20V8, are always available as data inputs into the AND array. The "center" two macrocells (GAL16V8 pins 15 &16, GAL20V8 pins 18 & 19) cannot be used in the input configuration.



Dedicated Input Mode

NOTES:
- The "center" two macrocells (16V8 pins 15 & 16, 20V8 pins 18 & 19) cannot be configured to this function.



Dedicated Combinational Output with Programmable Polarity

NOTES:
- All Macrocells can be configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL16V8A and GAL20V8A device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL16V8A and GAL20V8A device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

INPUT BUFFERS

GAL16V8A and GAL20V8A devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL16V8A and GAL20V8A devices do not possess active pullups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL16V8A and GAL20V8A devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

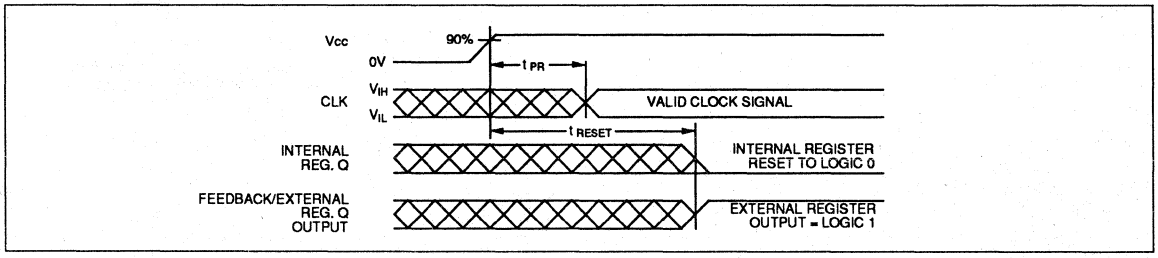
LATCH-UP PROTECTION

GAL16V8A and GAL20V8A devices are designed with an onboard charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

POWER-UP RESET



Circuitry within the GAL16V8A and GAL20V8A provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16V8A and GAL20V8A. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

GAL®16V8
GAL®20V8

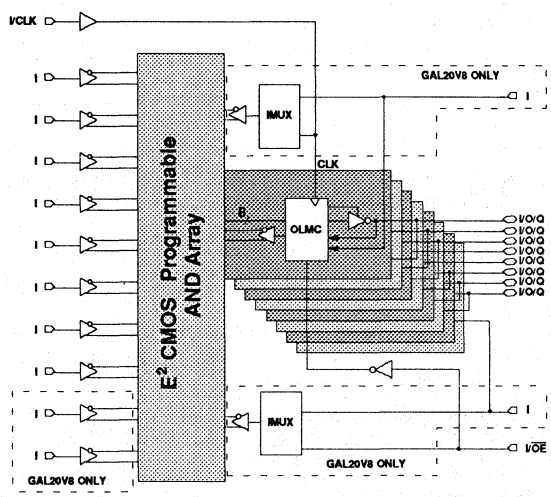
Generic Array Logic™

U.S. Patents 4,761,768 and 4,766,569

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **15 ns Maximum Propagation Delay**
  - **Fmax = 50 MHz**
  - **12 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 24 mA Outputs**
  - **UltraMOS® II Advanced CMOS Technology**
- **50% REDUCTION IN POWER OVER BIPOLAR**
  - **45mA Max I_{CC}**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<50ms)**
  - **20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **Maximum Flexibility for Complex Logic Designs**
  - **Programmable Output Polarity**
  - **GAL16V8 Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
  - **GAL20V8 Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

GAL16V8 / GAL20V8 BLOCK DIAGRAM



DESCRIPTION

The GAL16V8 and GAL20V8, at 15 ns maximum propagation delay time, combine a high performance CMOS process with Electrically Erasable (E^2) floating gate technology. CMOS circuitry allows the GAL16V8 and GAL20V8 to consume just 75mA typical I_{CC} (and just 40mA for Quarter Power versions) which represents a considerable savings in power when compared to their bipolar counterparts. The E^2 technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8 and GAL20V8 are capable of emulating standard 20 and 24-pin PAL® devices. The GAL16V8 is capable of emulating standard 20-pin PAL architectures with full function/fuse map/parametric compatibility. The GAL20V8 is capable of emulating standard 24-pin PAL architectures with full function/fuse map/parametric compatibility. On the right is a table listing the PAL architectures that the GAL16V8 and GAL20V8 can replace.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

GAL16V8 / GAL20V8 ARCHITECTURE EMULATION

GAL20V8 PAL Architecture Emulation	GAL16V8 PAL Architecture Emulation
20L8	16L8
20H8	16H8
20R8	16R8
20R6	16R6
20R4	16R4
20P8	16P8
20RP8	16RP8
20RP6	16RP6
20RP4	16RP4
14L8	10L8
16L6	12L6
18L4	14L4
20L2	16L2
14H8	10H8
16H6	12H6
18H4	14H4
20H2	16H2
14P8	10P8
16P6	12P6
18P4	14P4
20P2	16P2

LATTICE SEMICONDUCTOR CORP., PO BOX 2500, PORTLAND, OREGON 97208-2500, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

March 1989

ABSOLUTE MAXIMUM RATINGS(1)

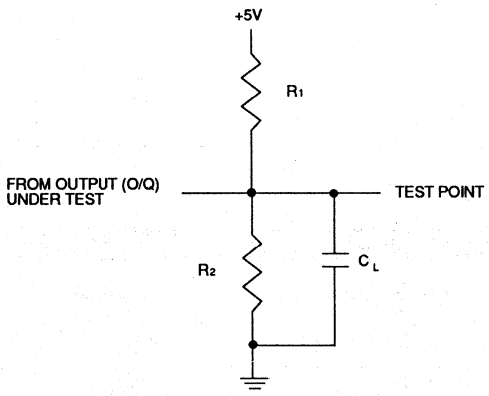
Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

COMMERCIAL DEVICES

Refer to AC Test Conditions:

R_2 = 390Ω

1) R_1 = 200Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 200Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 200Ω C_L = 5pF

MILITARY DEVICES

Refer to AC Test Conditions:

R_2 = 750Ω

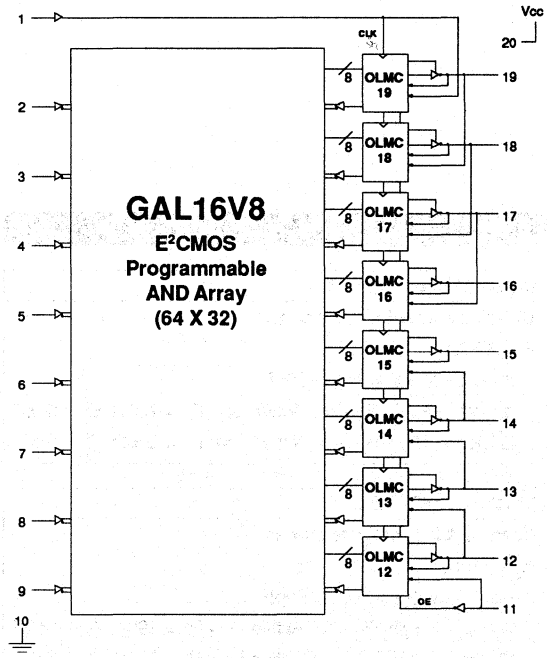
1) R_1 = 390Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 5pF

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

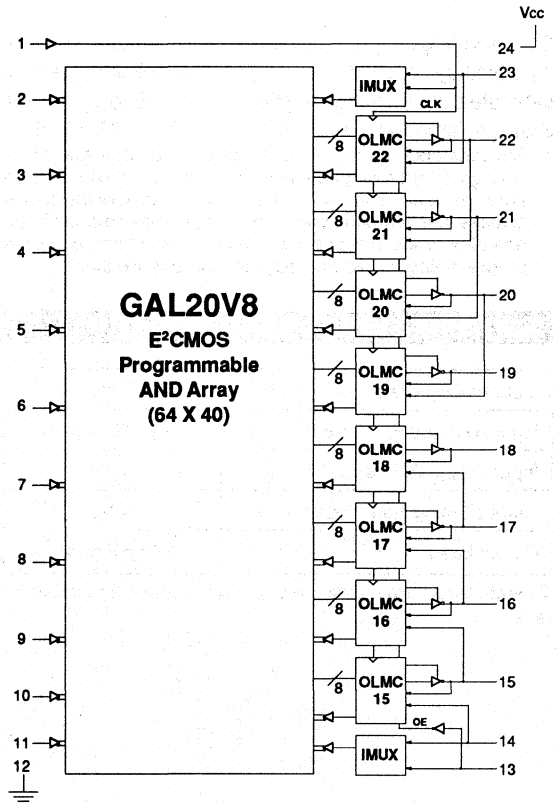
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL16V8 BLOCK DIAGRAM

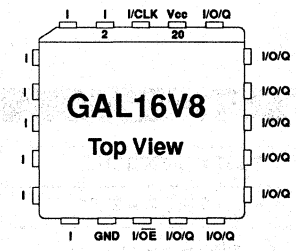


GAL20V8 BLOCK DIAGRAM

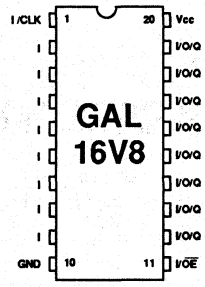


GAL16V8 PIN CONFIGURATION

Chip Carrier

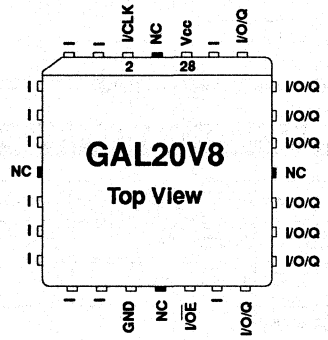


DIP

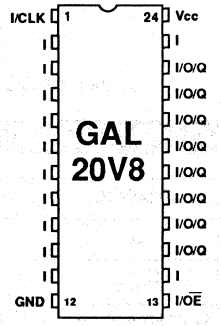


GAL20V8 PIN CONFIGURATION

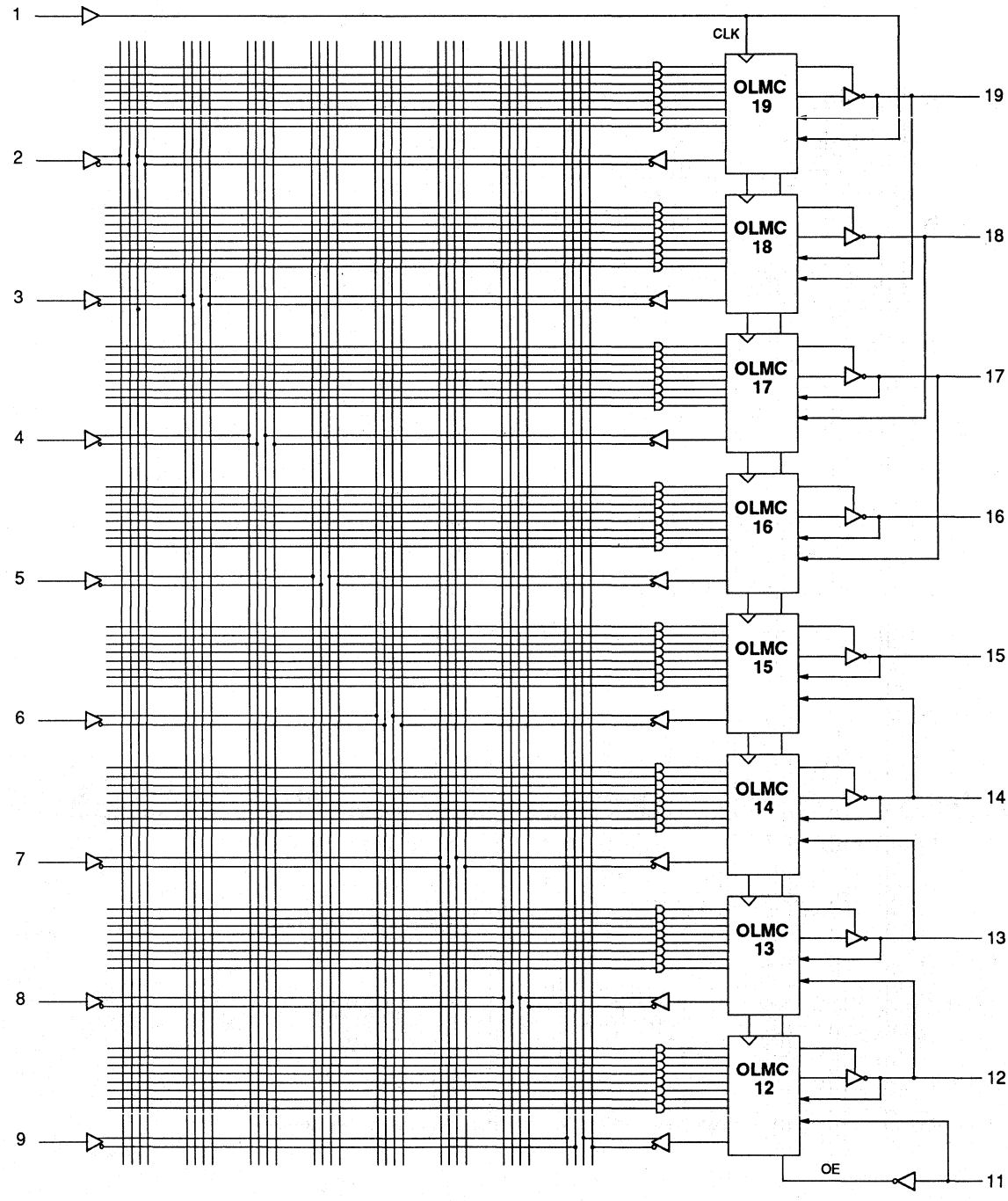
Chip Carrier



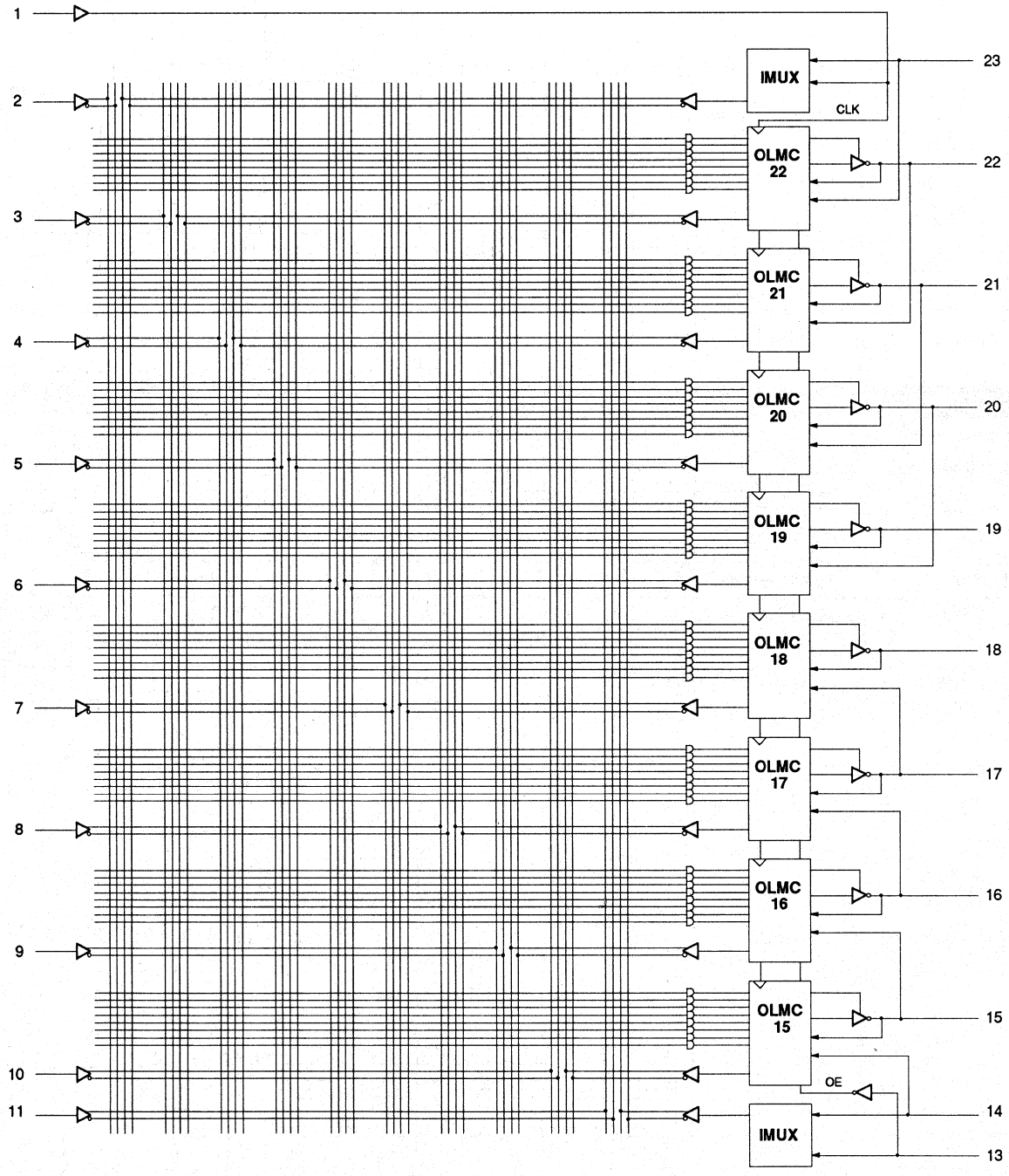
DIP



GAL16V8 LOGIC DIAGRAM



GAL20V8 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL16V8-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16V8-15L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16V8-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

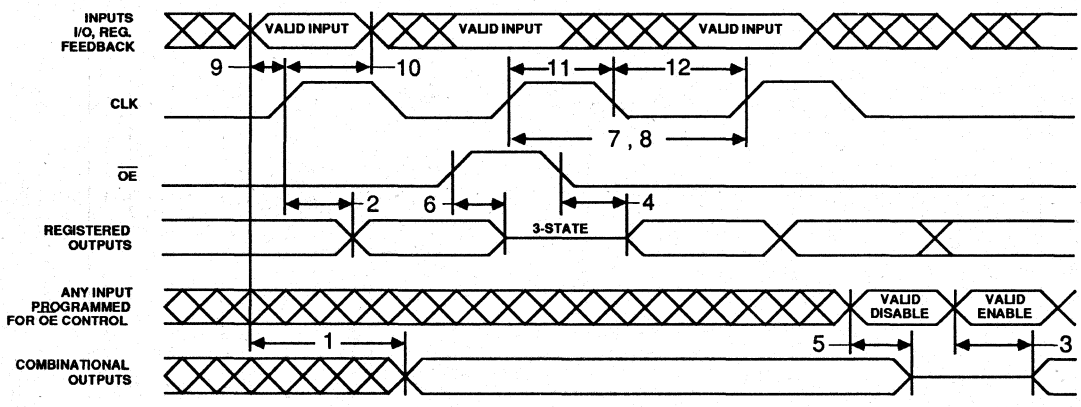
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16V8-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	50	MHz
	8	Clock Frequency with Feedback	1	0	41.6	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	10	—	ns
	12	Clock Pulse Duration, Low	—	10	—	ns

2

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16V8-20Q Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	40	45	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16V8-20Q Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16V8-20Q Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	—	20	ns
	2	CLK	Q	Clock to Output Delay	1	—	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

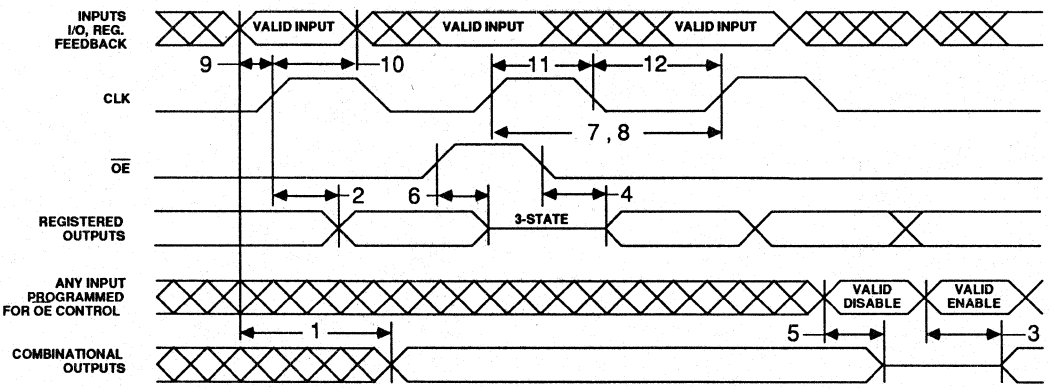
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16V8-20Q Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	41.6	MHz
	8	Clock Frequency with Feedback	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	12	—	ns
	12	Clock Pulse Duration, Low	—	12	—	ns

2

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16V8-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16V8-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16V8-25L Commercial

Over Recommended Operating Conditions

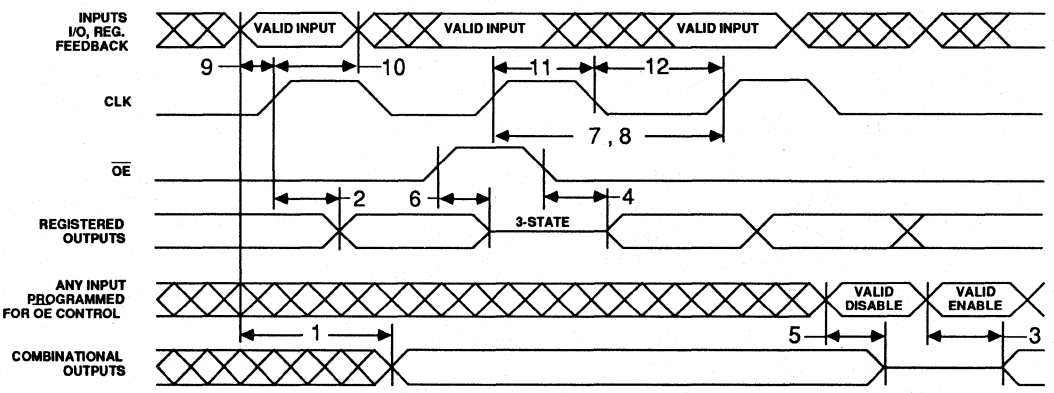
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	—	25	ns
	2	CLK	Q	Clock to Output Delay	1	—	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16V8-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL16V8-25Q Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	40	45	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL16V8-25Q Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL16V8-25Q Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	—	25	ns
	2	CLK	Q	Clock to Output Delay	1	—	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

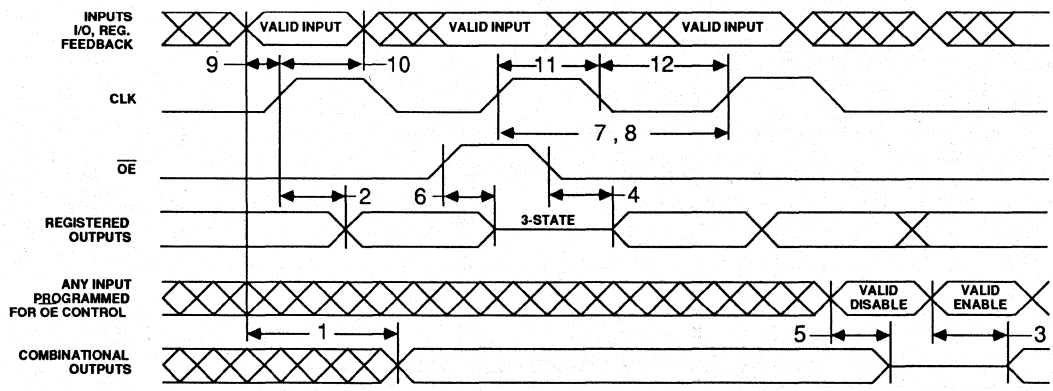
1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL16V8-25Q Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

2

SWITCHING WAVEFORMS



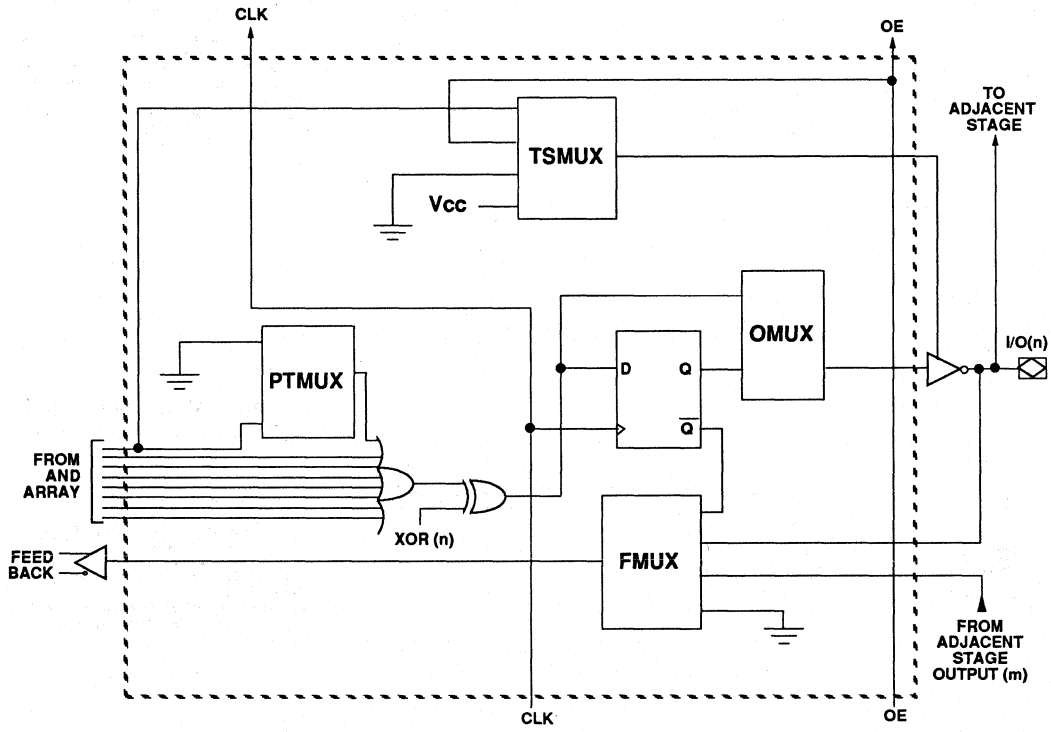
OUTPUT LOGIC MACROCELL (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the small mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20 and 24-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.



GAL®16/20V8 Output Logic Macrocell(n)

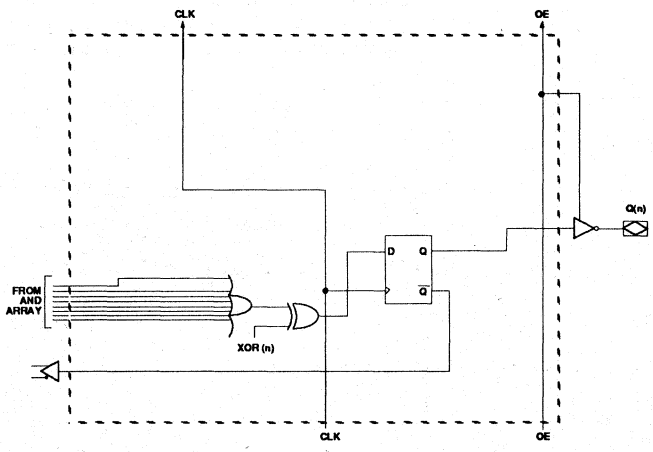
REGISTERED MODE

In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8, 20R6 and 16RP4 devices with various permutations of polarity, I/O and register placement.

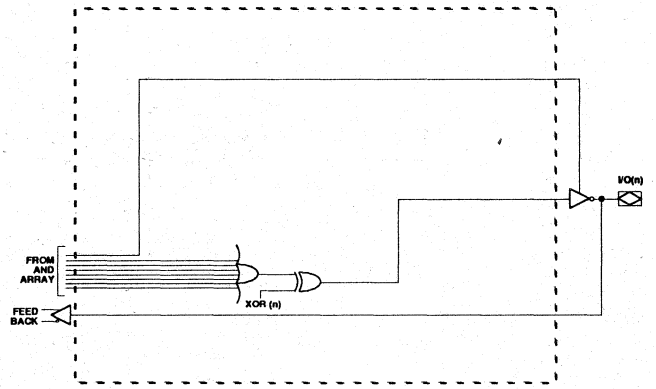
All registered macrocells share common clock and $\overline{OE}$ control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

Registered outputs have 8 data product terms per output. I/O's have 7 data product terms per output.



Registered Output with Programmable Polarity

NOTES:
- All macrocells can be individually configured to this function.
- Polarity of the register input is programmable on a macrocell by macrocell basis.
- Feedback into the AND array is from the $\overline{Q}$ signal of the register with active low and active high feedback paths provided.
- Registered macrocells have common clock (pin 1) and common $\overline{OE}$ (16V8 pin 11, 20V8 pin 13)



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- All macrocells can be individually configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- All macrocells have active high and active low feedback of the output buffer and/or device pin data into the AND array.
- When all 8 macrocells are configured into the I/O function the CLK and $\overline{OE}$ pins serve no valid logic function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

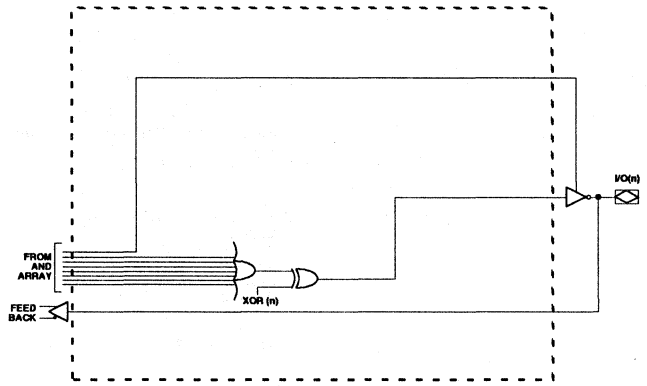
COMPLEX MODE

In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8, 20L8 and 16P8 devices with programmable polarity in each macrocell.

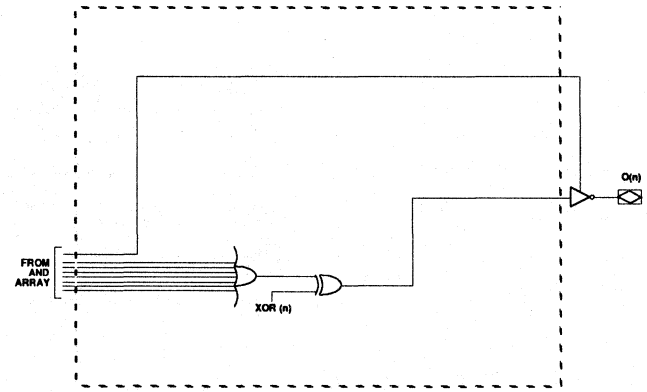
Up to 6 I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 11 on a GAL16V8, and pins 1 and 13 on a GAL20V8, are always available as data inputs into the AND array.



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- The outboard macrocells (16V8 pins 12 & 19, 20V8 pins 15 & 22) cannot perform this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- Each macrocell has active high and active low feedback of the output buffer and/or device pin data into the AND array.



Combinational Output with Programmable OE and Polarity

NOTES:
- The two outboard macrocells (16V8 pins 12 & 19, 20V8 pins 15 & 22) are permanently configured to this function when in the Complex mode.
- The other 6 macrocells can emulate this mode by not using the feedback data as a data input to the array.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

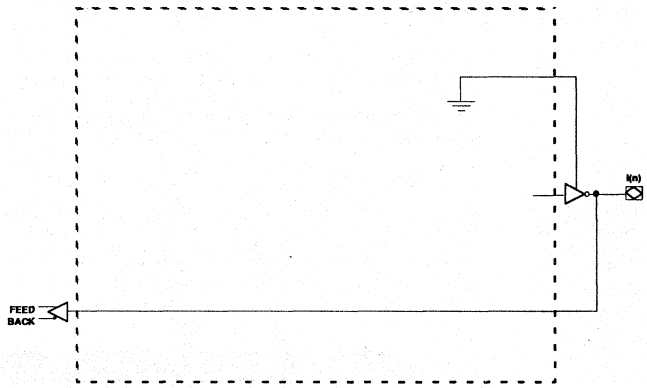
SIMPLE MODE

In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8, 18H4 and 16P6 devices with many permutations of generic polarity output or input choices.

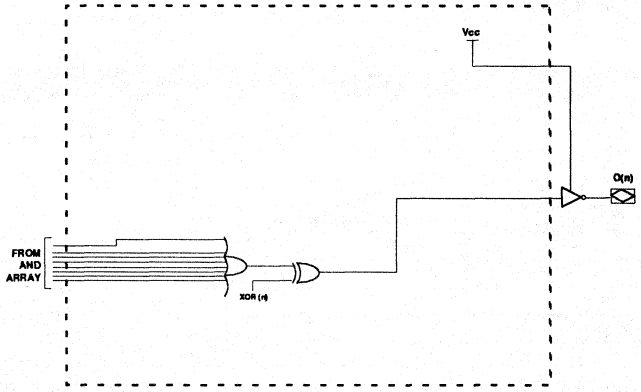
All ouputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 11 on a GAL16V8, and pins 1 and 13 on a GAL20V8, are always available as data inputs into the AND array. The "center" two macrocells (GAL16V8 pins 15 &16, GAL20V8 pins 18 & 19) cannot be used in the input configuration.



Dedicated Input Mode

NOTES:
- The "center" two macrocells (16V8 pins 15 & 16, 20V8 pins 18 & 19) cannot be configured to this function.



Dedicated Combinational Output with Programmable Polarity

NOTES:
- All Macrocells can be configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL16V8 and GAL20V8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL16V8 and GAL20V8 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

INPUT BUFFERS

GAL16V8 and GAL20V8 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL16V8 and GAL20V8 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL16V8 and GAL20V8 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

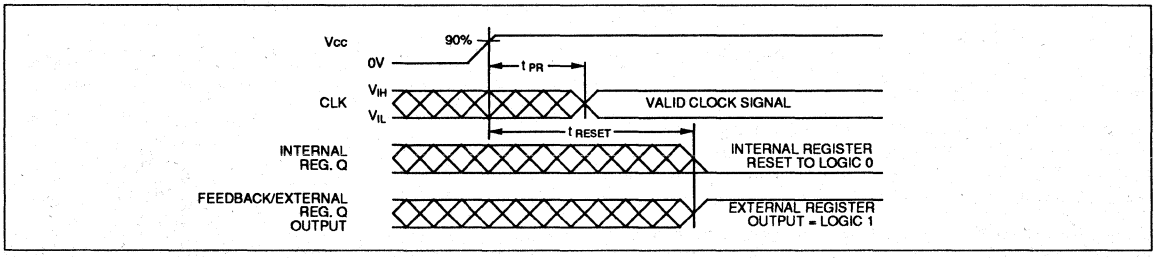
LATCH-UP PROTECTION

GAL16V8 and GAL20V8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

POWER-UP RESET



Circuitry within the GAL16V8 and GAL20V8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL16V8 and GAL20V8. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

Lattice Semiconductor Corporation™

GAL®22V10

Generic Array Logic™

U.S. Patents 4,761,768 and 4,766,569

FEATURES

- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 50 MHz**
  - **— 8 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Outputs**
  - **— UltraMOS® III Advanced CMOS Technology**
  - **— Internal Pull-Up Resistor on all Pins**
- **50% REDUCTION IN POWER**
  - **— 90mA Typ I_{cc}**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— High Speed Electrical Erasure (<50ms)**
  - **— 20 Year Data Retention**
- **TEN OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Full Function/Fuse Map/Parametric Compatibility with 22V10 Devices**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

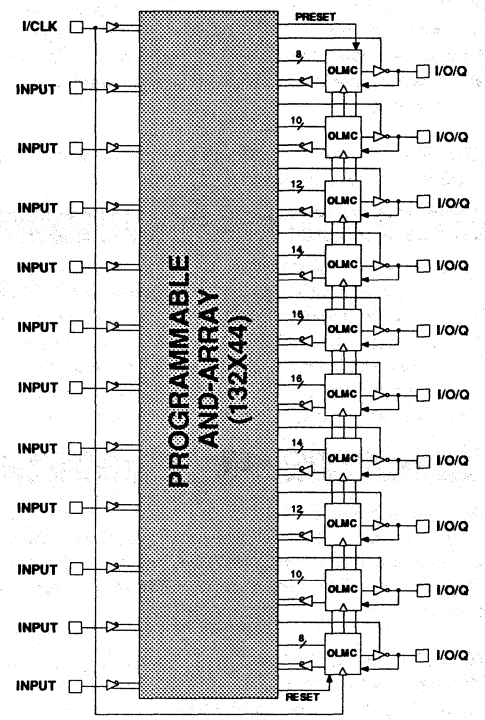
DESCRIPTION

The GAL®22V10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest performance available of any 22V10 device on the market. CMOS circuitry allows the GAL22V10 to consume just 90mA typical I_{cc} which represents a 50% savings in power when compared to its bipolar counterparts. The E^2 technology offers high speed (50ms) erase times providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL22V10 is fully function/fuse map/parametric compatible with bipolar and CMOS 22V10 devices.

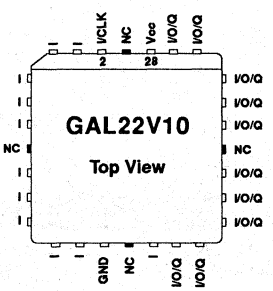
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

FUNCTIONAL BLOCK DIAGRAM

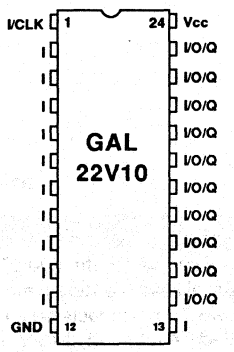


PACKAGE DIAGRAMS

Chip Carrier



DIP



LATTICE SEMICONDUCTOR CORP., PO BOX 2500, PORTLAND, OREGON 97208-2500 U.S.A.
Tel. (503) 681-0118 or 1-800-FASTGAL; FAX (503) 681-3037

April 1989

ABSOLUTE MAXIMUM RATINGS(1)

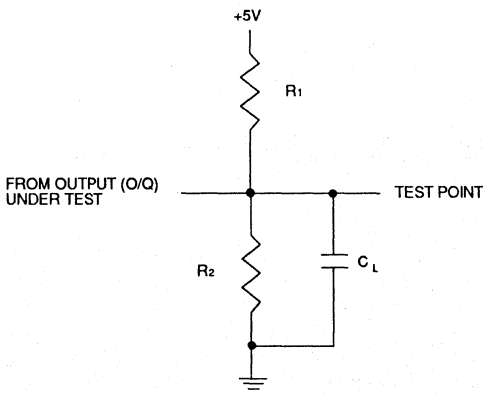
Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

COMMERCIAL DEVICES

Refer to AC Test Conditions:

R_2 = 390Ω

1) R_1 = 300Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 300Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 300Ω C_L = 5pF

MILITARY DEVICES

Refer to AC Test Conditions:

R_2 = 750Ω

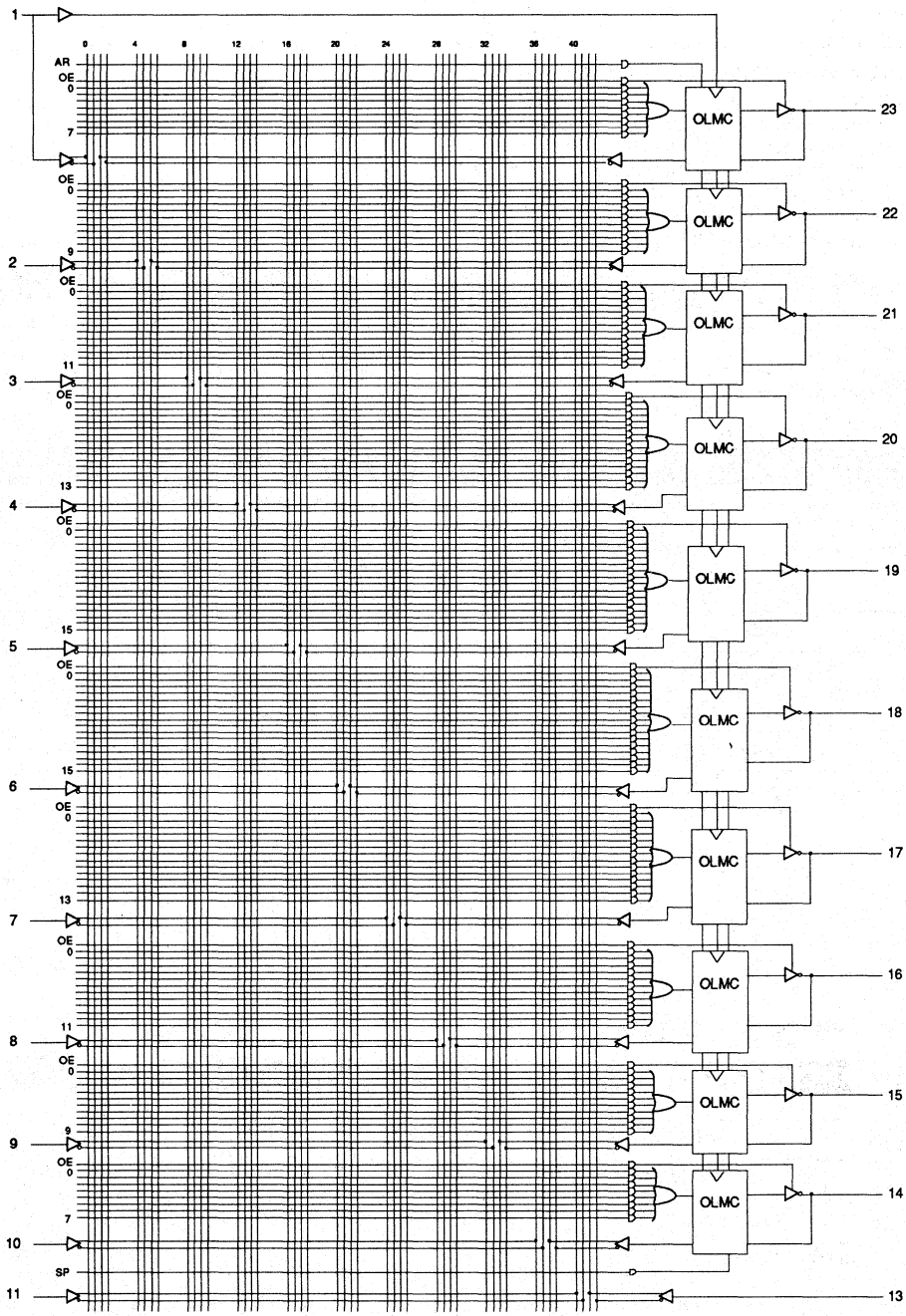
1) R_1 = 390Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 5pF

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL22V10 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL22V10-15L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}[1]	Input Leakage Current		10	—	–150	µA
$I_{I/O/Q}$[1]	Bidirectional Pin Leakage Current		10	—	–150	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-15L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL22V10-15L Commercial

Over Recommended Operating Conditions

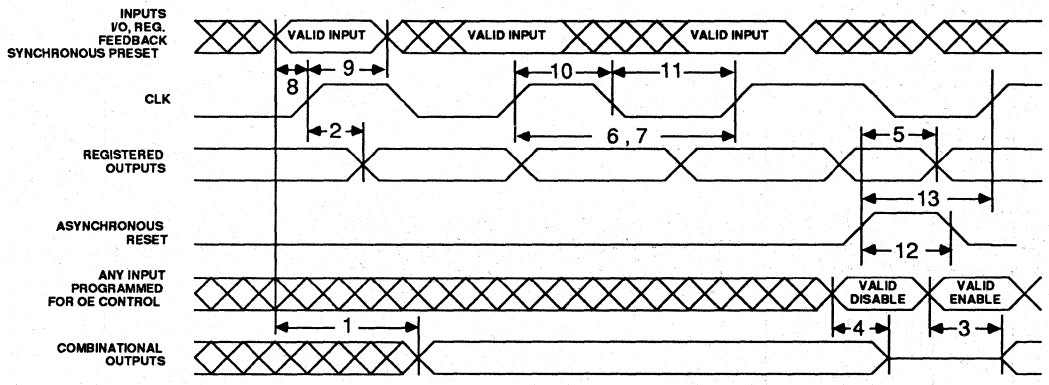
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	15	ns
	2	Clk ↑	Q	Clock to Register Output	1	—	8	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	15	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	15	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	20	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback	—	0	62.5	MHz
	7	Clock Frequency with Feedback	—	0	50	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	12	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High	—	8	—	ns
	11	Clock Pulse Duration, Low	—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	15	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	15	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL22V10-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}[1]	Input Leakage Current		10	—	–150	µA
$I_{I/O/Q}$[1]	Bidirectional Pin Leakage Current		10	—	–150	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL22V10-25L Commercial

Over Recommended Operating Conditions

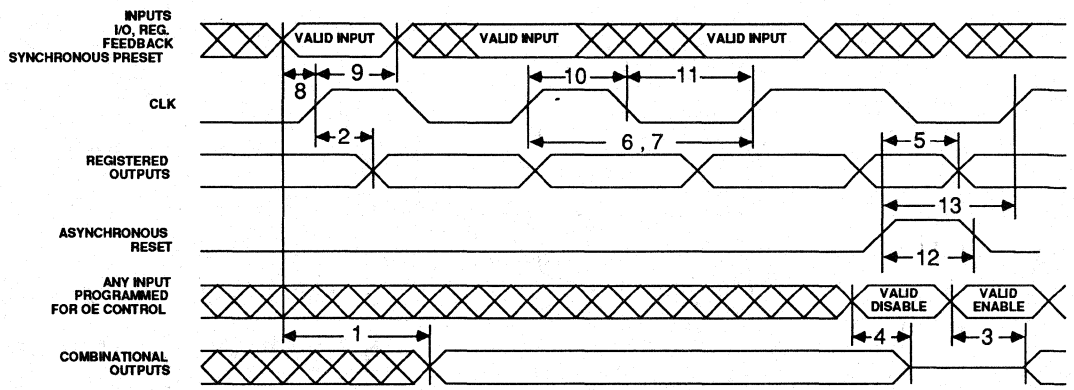
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	25	ns
	2	Clk ↑	Q	Clock to Register Output	1	—	15	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	25	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback	—	0	33.3	MHz
	7	Clock Frequency with Feedback	—	0	33.3	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	15	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High	—	15	—	ns
	11	Clock Pulse Duration, Low	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	25	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	25	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL22V10-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}[1]	Input Leakage Current		10	—	–150	µA
$I_{I/O/Q}$[1]	Bidirectional Pin Leakage Current		10	—	–150	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL22V10-20L Industrial

Over Recommended Operating Conditions

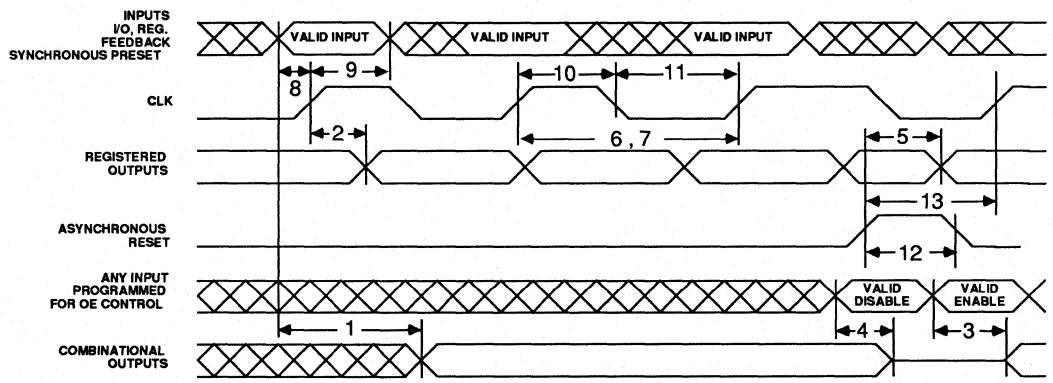
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
	2	Clk ↑	Q	Clock to Register Output	1	—	10	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	20	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	20	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	25	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-20L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback	—	0	50	MHz
	7	Clock Frequency with Feedback	—	0	40	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	15	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High	—	10	—	ns
	11	Clock Pulse Duration, Low	—	10	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	20	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL22V10-25L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}[1]	Input Leakage Current		10	—	–150	µA
$I_{I/O/Q}$[1]	Bidirectional Pin Leakage Current		10	—	–150	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-25L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — GAL22V10-25L Industrial

Over Recommended Operating Conditions

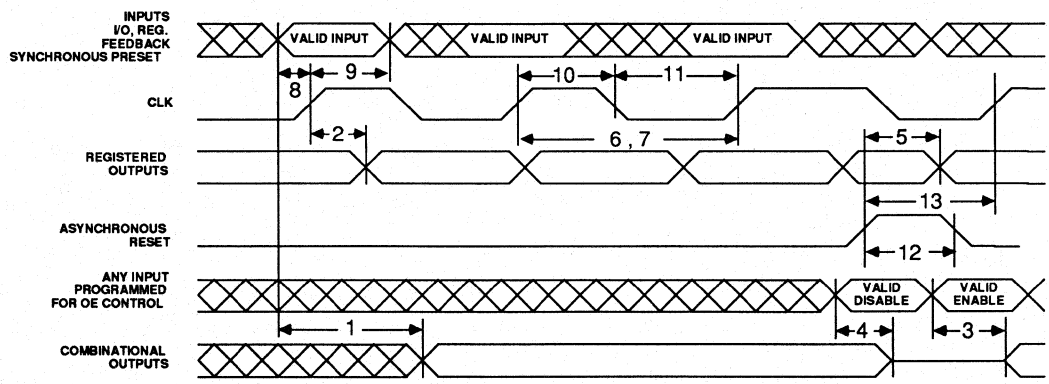
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	25	ns
	2	Clk ↑	Q	Clock to Register Output	1	—	15	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	25	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-25L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback	—	0	33.3	MHz
	7	Clock Frequency with Feedback	—	0	28.5	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	20	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High	—	15	—	ns
	11	Clock Pulse Duration, Low	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	25	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	25	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL22V10-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}[1]	Input Leakage Current		10	—	–150	µA
$I_{I/O/Q}$[1]	Bidirectional Pin Leakage Current		10	—	–150	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-20L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	–55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL22V10-20L Military

Over Recommended Operating Conditions

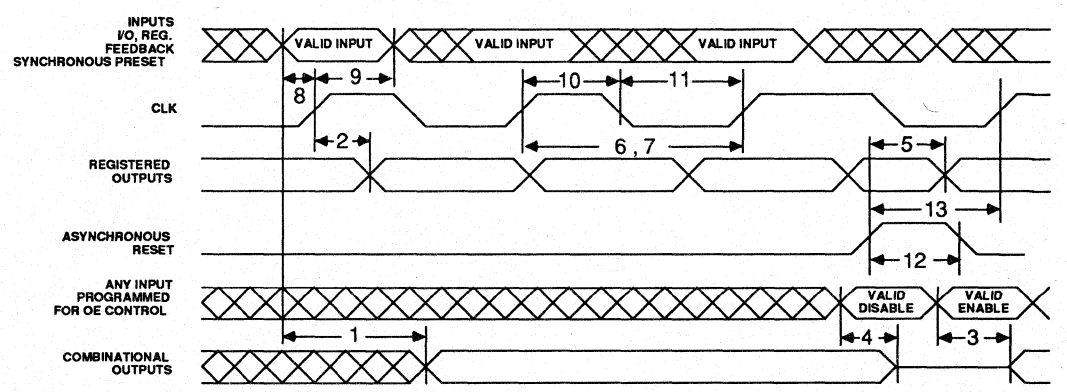
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
	2	Clk ↑	Q	Clock to Register Output	1	—	15	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z→ O, Q	2	—	20	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q→ Z	3	—	20	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	25	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback	—	0	33.3	MHz
	7	Clock Frequency with Feedback	—	0	31.2	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	17	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High	—	15	—	ns
	11	Clock Pulse Duration, Low	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	20	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — GAL22V10-30L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}[1]	Input Leakage Current		10	—	–150	µA
$I_{I/O/Q}$[1]	Bidirectional Pin Leakage Current		10	—	–150	µA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–50	—	–135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation.

DC RECOMMENDED OPERATING CONDITIONS — GAL22V10-30L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	-55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — GAL22V10-30L Military

Over Recommended Operating Conditions

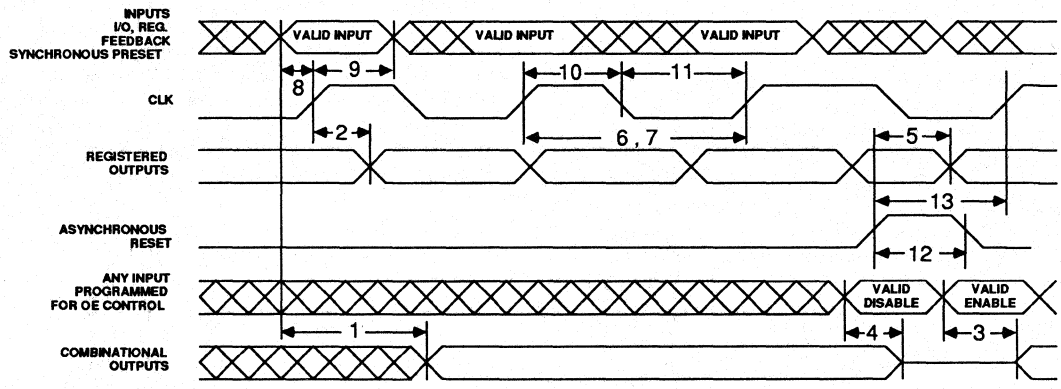
PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	30	ns
	2	Clk ↑	Q	Clock to Register Output	1	—	20	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	30	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL22V10-30L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback	—	0	25	MHz
	7	Clock Frequency with Feedback	—	0	22	MHz
t_{su}	8	Setup Time, Input or Feedback, before Clk ↑	—	25	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_w	10	Clock Pulse Duration, High	—	20	—	ns
	11	Clock Pulse Duration, Low	—	20	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	30	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	30	—	ns

SWITCHING WAVEFORMS



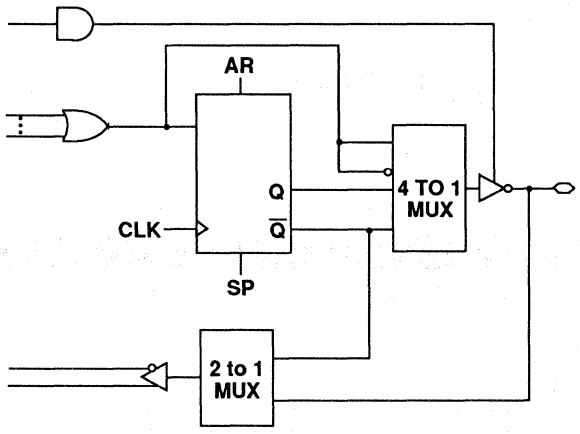
OUTPUT LOGIC MACROCELL ARCHITECTURE

The GAL22V10 has a variable number of product terms per OLMC. Of the ten available OLMCs, two OLMCs have access to eight product terms (pins 14 and 23), two have ten product terms (pins 15 and 22), two have twelve product terms (pins 16 and 21), two have fourteen product terms (pins 17 and 20), and two OLMCs have sixteen product terms (pins 18 and 19).

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinational or registered mode. This allows the user to reduce the overall number of product terms required in a design and to invert the output signal.

The GAL22V10 has a product term for AR (Asynchronous Reset) and a product term for SP (Synchronous Preset). These two product terms are common to all registered OLMCs.

NOTE: Output polarity selection does NOT affect the behavior of the OLMC's integral "D" flip-flop. The AR and SP product terms will force the flip-flop into the same state regardless of the polarity of the output.



GAL22V10 OUTPUT LOGIC MACROCELL (OLMC)

OUTPUT LOGIC MACROCELL CONFIGURATIONS

The GAL22V10 has two primary functional modes which may be selected at programming time (registered and combinational / input). Each of these two primary modes are described below.

REGISTERED

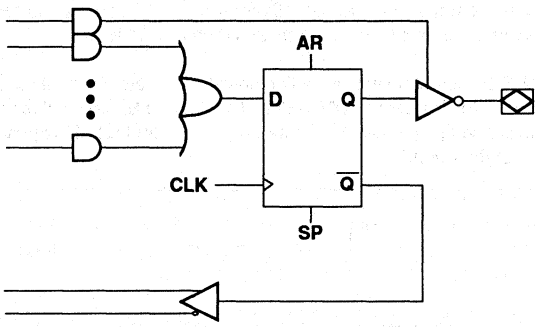
In registered mode the output pin associated with an individual OLMC is driven by the "Q" output of that OLMC's "D" flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or invert (active low). Output tri-state control is available and can be individually selected as either "on", "off", or "product-term driven." The "D" flip-flop's "/Q" output is fed back into the "AND" array via the "AND" array buffer. Both polarities (true and invert) of the OLMC are fed back into the "AND" array.

NOTE: In registered mode a tri-stated output pin may NOT be used as an input into the "AND" array.

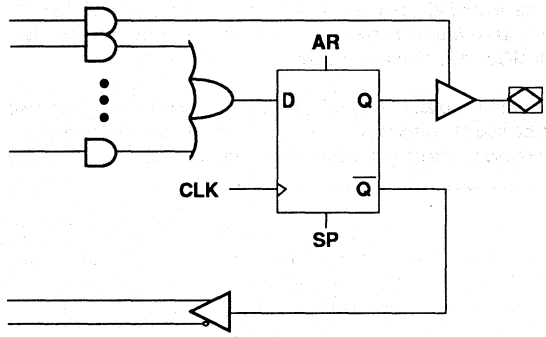
COMBINATIONAL / INPUT

In combinational mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or invert (active low). Output tri-state control is available and may be individually selected as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feed back into the "AND" array is from the pin, via the "AND" array buffer. Both polarities (true and invert) of the pin are fed back into the "AND" array.

REGISTERED MODE



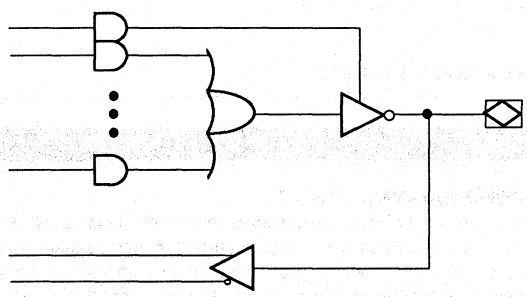
ACTIVE LOW



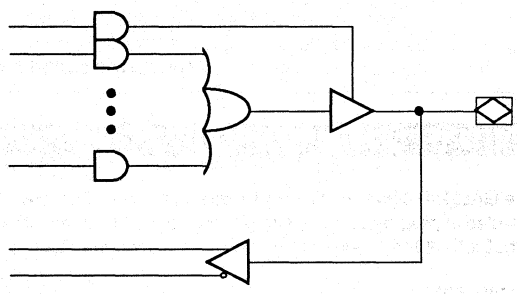
ACTIVE HIGH

2

COMBINATIONAL MODE



ACTIVE LOW



ACTIVE HIGH

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL®22V10 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided with every GAL®22V10 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

INPUT BUFFERS

GAL®22V10 devices are designed with TTL level compatible input buffers. These input buffers possess active pull-ups within their input structure. As a result, floating inputs are guaranteed to be a TTL "high" (logical "1").

OUTPUT REGISTER PRELOAD

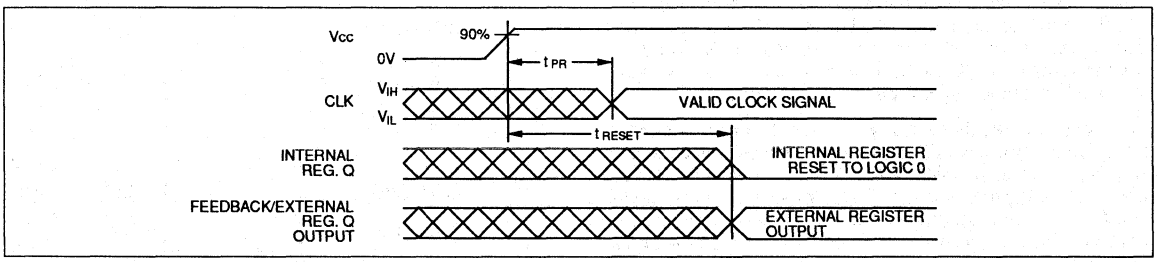
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL®22V10 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

LATCH-UP PROTECTION

GAL®22V10 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullup instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

POWER-UP RESET



Circuitry within the GAL®22V10 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL®22V10. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

GAL®6001

Generic Array Logic™

U.S. Patents 4,761,768 and 4,766,569

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - **— Instantly Reconfigurable Logic**
  - **— Instantly Reprogrammable Cells**
  - **— Guaranteed 100% Yields**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— Low Power: 90mA Typical**
  - **— High Speed: 12ns Max. Clock to Output Delay**
    25ns Max. Setup Time
    30ns Max. Propagation Delay
- **UNPRECENTED FUNCTIONAL DENSITY**
  - **— 78 x 64 x 36 FPLA Architecture**
  - **— 10 Output Logic Macrocells**
  - **— 8 Buried Logic Macrocells**
  - **— 20 Input and I/O Logic Macrocells**
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - **— Asynchronous or Synchronous Clocking**
  - **— Separate State Register and Input Clock Pins**
  - **— Functionally Supersets Existing 24-pin PAL® and IFL™ Devices**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **20-YEAR DATA RETENTION**

DESCRIPTION

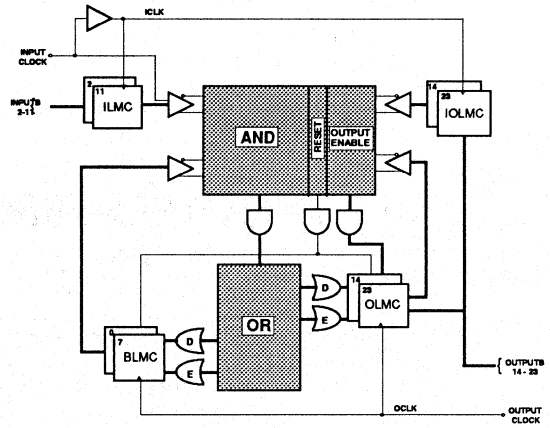
Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

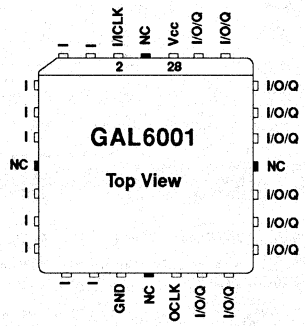
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

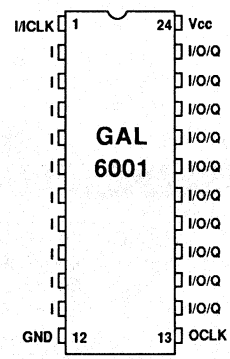
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN CONFIGURATION

Chip Carrier



DIP



LATTICE SEMICONDUCTOR CORP., PO BOX 2500, PORTLAND, OREGON 97208-2500 U.S.A.
Tel. (503) 681-0118 or 1-800-FAST GAL; FAX (503) 681-3037

March 1989

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

COMMERCIAL DEVICES

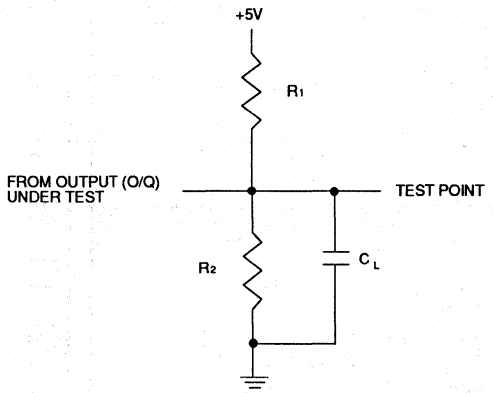
Refer to AC Test Conditions:

R_2 = 390Ω
1) R_1 = 300Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 300Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 300Ω C_L = 5pF

MILITARY DEVICES

Refer to AC Test Conditions:

R_2 = 750Ω
1) R_1 = 390Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 5pF



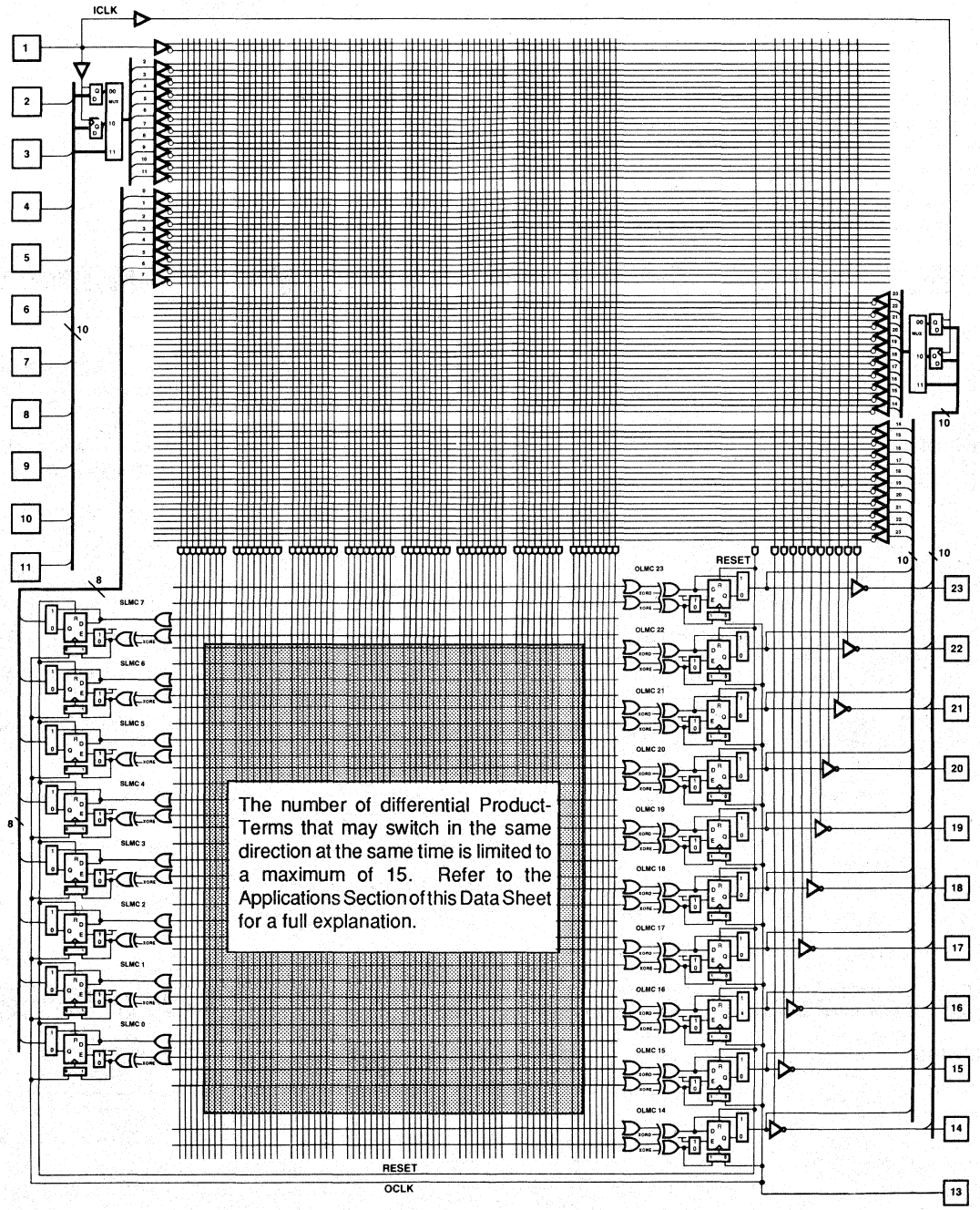
C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL6001 LOGIC DIAGRAM



The number of differential Product-Terms that may switch in the same direction at the same time is limited to a maximum of 15. Refer to the Applications Section of this Data Sheet for a full explanation.

2

ELECTRICAL CHARACTERISTICS — GAL6001-30 Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

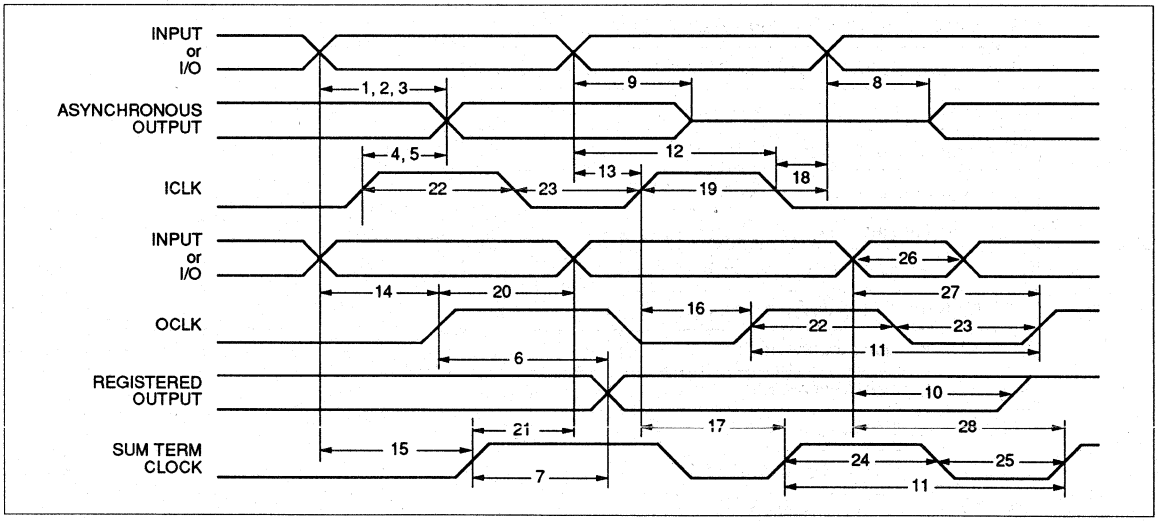
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-30 Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-30 Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	30	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	30	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	35	ns
	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	35	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	35	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	12	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	35	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-30 Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	27	MHz
t_{su}	12	Input Setup Time before ICLK ↓ , ILMC = Latch	—	2.5	—	ns
	13	Input Setup Time before ICLK ↑ , ILMC = Reg	—	2.5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑ , OLMC = D/E Reg	—	25	—	ns
	15	Setup Time, input or feedback, before STCLK ↑ , OLMC = DReg STCLK	—	7.5	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑ , OLMC = D/E Reg	—	30	—	ns
	17	Setup Time, ICLK ↑ , before STCLK ↑ , OLMC = DReg STCLK	—	15	—	ns
t_h	18	Hold Time after ICLK ↓ , ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑ , OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	10	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

ELECTRICAL CHARACTERISTICS — GAL6001-35 Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

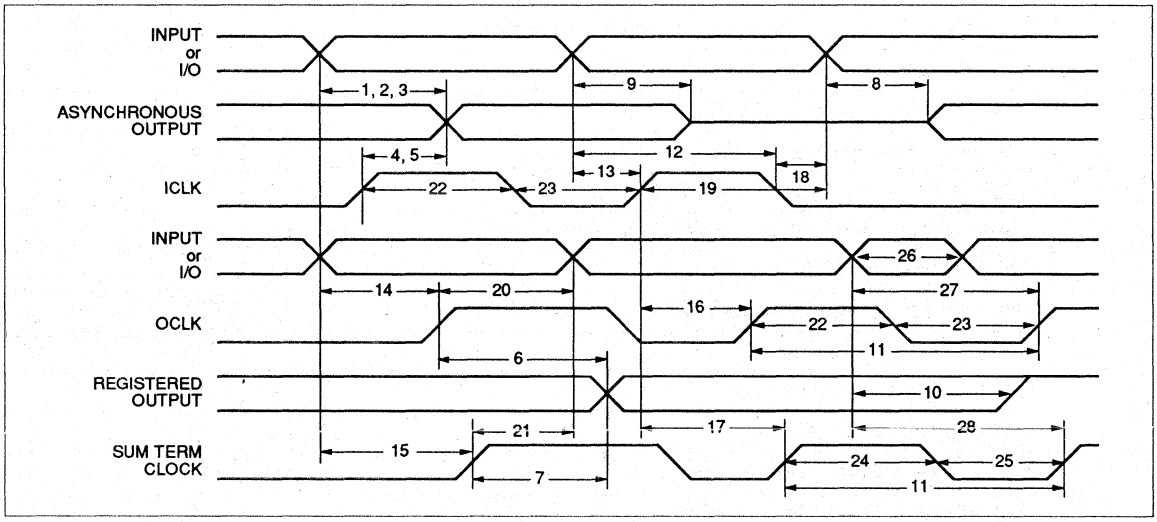
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	180	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-35 Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-35 Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	35	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	35	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	40	ns
	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	40	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	40	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	13.5	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	40	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	30	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	30	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

2

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-35 Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	22.9	MHz
t_{su}	12	Input Setup Time before ICLK ↓ , ILMC = Latch	—	3.5	—	ns
	13	Input Setup Time before ICLK ↑ , ILMC = Reg	—	3.5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑ , OLMC = D/E Reg	—	30	—	ns
	15	Setup Time, input or feedback, before STCLK ↑ , OLMC = DReg STCLK	—	10	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑ , OLMC = D/E Reg	—	35	—	ns
	17	Setup Time, ICLK ↑ , before STCLK ↑ , OLMC = DReg STCLK	—	17	—	ns
t_h	18	Hold Time after ICLK ↓ , ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑ , OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	12.5	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

ELECTRICAL CHARACTERISTICS — GAL6001-40 Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

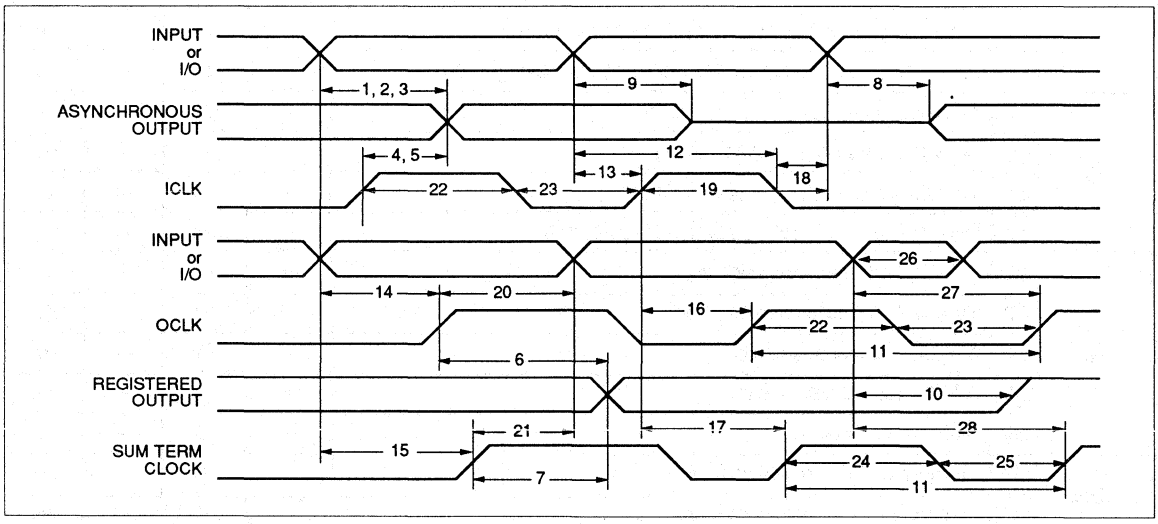
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	180	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-40 Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Case Temperature	– 55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	8	mA
I_{OH}	High Level Output Current	—	– 2.0	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-40 Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	40	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	40	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	45	ns
	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	45	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	45	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	15	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	45	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-40 Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	22.2	MHz
t_{su}	12	Input Setup Time before ICLK ↓ , ILMC = Latch	—	5	—	ns
	13	Input Setup Time before ICLK ↑ , ILMC = Reg	—	5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑ , OLMC = D/E Reg	—	30	—	ns
	15	Setup Time, input or feedback, before STCLK ↑ , OLMC = DReg STCLK	—	10	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑ , OLMC = D/E Reg	—	40	—	ns
	17	Setup Time, ICLK ↑ , before STCLK ↑ , OLMC = DReg STCLK	—	17	—	ns
t_h	18	Hold Time after ICLK ↓ , ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑ , OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	15	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

2

INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL®6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide systems designers with unparalled design flexibility. With the GAL®6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, "D-type register with sum term (asynchronous) clock", or "D/E-type register." Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the "D" XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selected through the "E" XOR.

When the macrocell is configured as a "D/E type registered", the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a "D type register with a sum term clock", the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

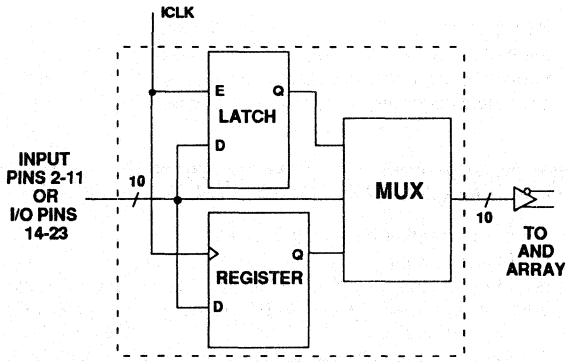
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an ouput pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

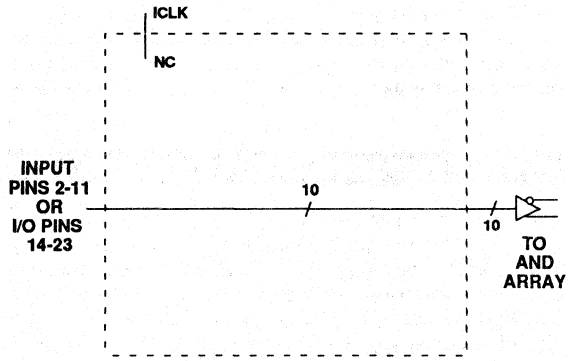
The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

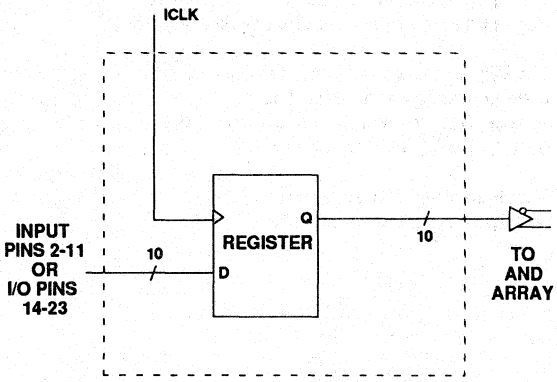
ILMC AND IOLMC CONFIGURATIONS



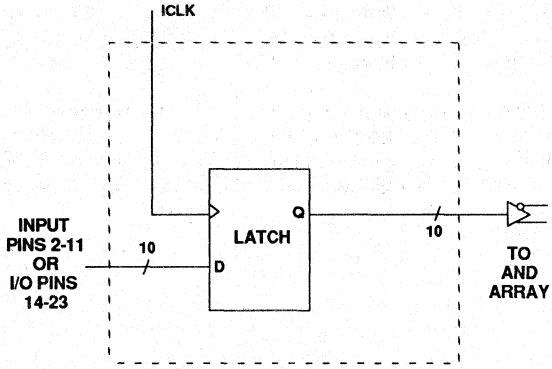
ILMC/IOLMC
Generic Block Diagram



Asynchronous Input



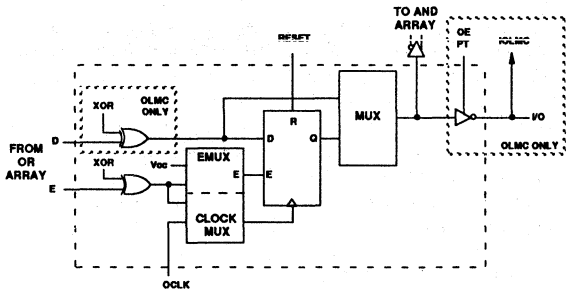
Registered Input



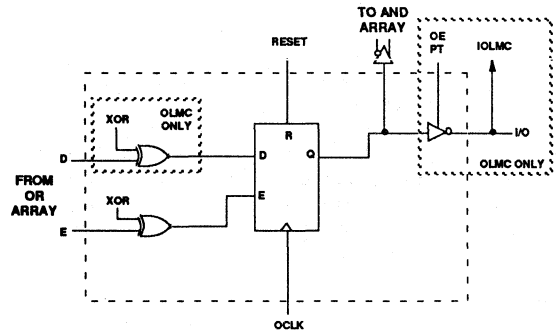
Latched Input

2

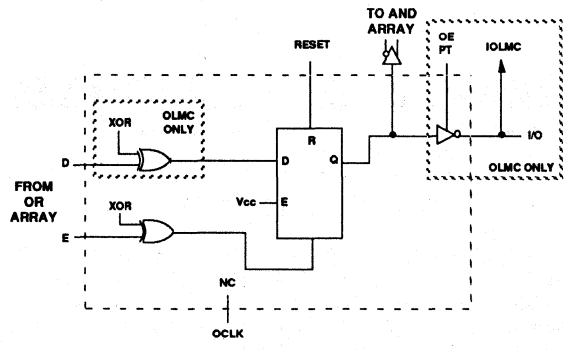
OLMC AND BLMC CONFIGURATIONS



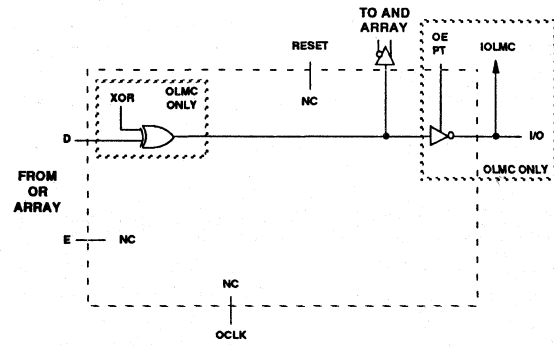
OLMC/BLMC
Generic Block Diagram



D/E Type Registered



D Type Register with Sum Term Asynchronous Clock



Combinational

ARRAY DESCRIPTION

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complemented forms). 64 product terms serve as inputs to the OR array. There is a RESET PT; it generates the RESET signal described in the earlier discussion of Output and Buried Logic Macrocells. There are 10 output enables, thus allowing device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

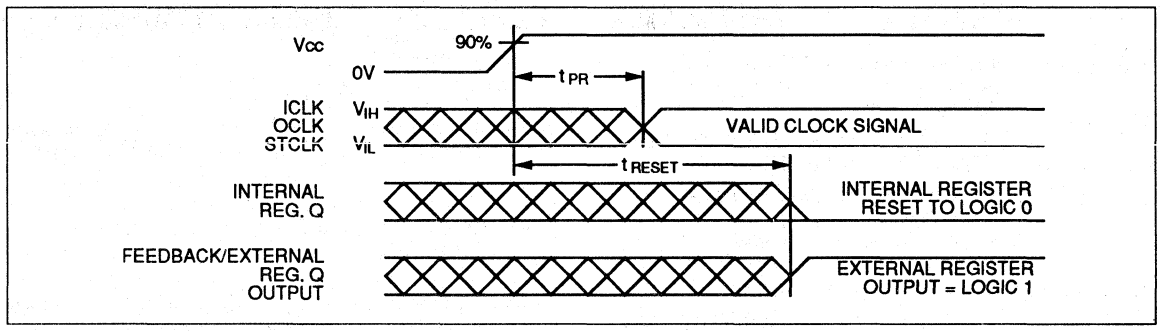
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL®6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL®6001. First, the Vcc rise must be monotonic. Second, the clock inputs must become a proper TTL level within the specified time (t_{PR}, 100µs). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (\text{P-Terms})_{LH} - (\text{P-Terms})_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL®6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).

ispGAL®16Z8

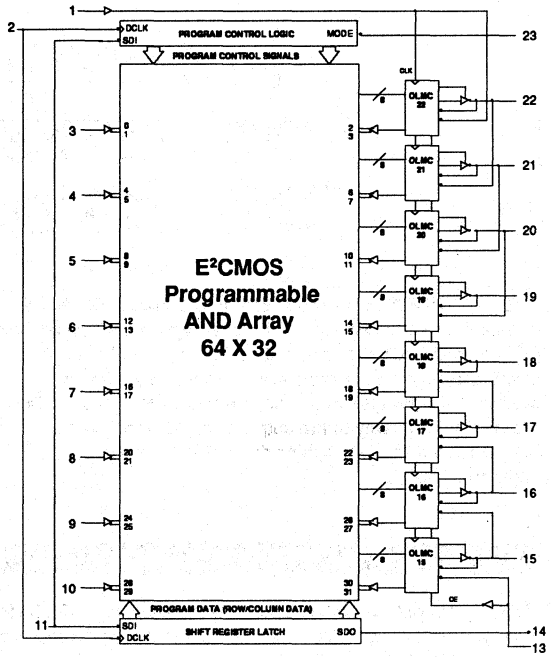
In-System Programmable Generic Array Logic™

U.S. Patents 4,761,768 and 4766,569

FEATURES

- **IN-SYSTEM-PROGRAMMABLE --- 5-VOLT ONLY**
  - **— Change Logic "On the Fly" (in less than 1 s)**
  - **— Nonvolatile E² Technology**
- **DIAGNOSTICS MODE FOR CONTROLLABILITY AND OBSERVABILITY OF SYSTEM LOGIC**
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - **— 20 ns Maximum Propagation Delay**
  - **— Fmax = 41.6 MHz**
  - **— 90mA MAX I_{CC}**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **24-PIN 300-MIL DIP, AND 28-LEAD PLCC PACKAGING**
- **MINIMUM 10,000 ERASE/WRITE CYCLES**
- **DATA RETENTION EXCEEDS 10 YEARS**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**
- **APPLICATIONS INCLUDE:**
  - **— Reconfigurable Interfaces and Decoders**
  - **— Copy Protection and Security Schemes**
  - **— "Soft" Hardware (Generic Systems)**
  - **— RFT™ (Reconfiguration For Test)**
  - **— Proprietary Hardware/Software Interlocks**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

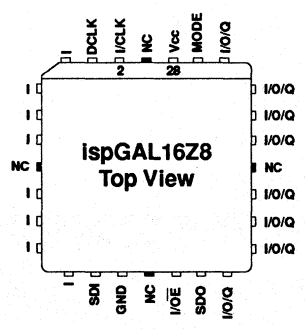
The Lattice ispGAL®16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmablitiy and real time, in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage internal programming control signals. Using Lattice's proprietary UltraMOS technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL16V8, but includes 4 extra pins to control in-system programming. These extra pins are: data clock (DCLK), serial data in (SDI), serial data out (SDO), and mode control (MODE). These pins are not associated with normal logic functions and are typically used for programming and for diagnostics. Additionally, this 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

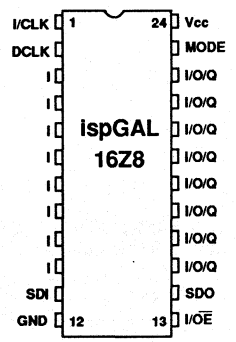
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of the GAL devices . A security circuit is built-in, providing proprietary designs with copy protection.

PIN DIAGRAMS

Chip Carrier



DIP



LATTICE SEMICONDUCTOR CORP., PO BOX 2500, PORTLAND, OREGON 97208-2500, U.S.A.
Tel. (503) 681-0118; 1-800-FASTGAL; FAX (503) 681-3037

April1989

ABSOLUTE MAXIMUM RATINGS(1)

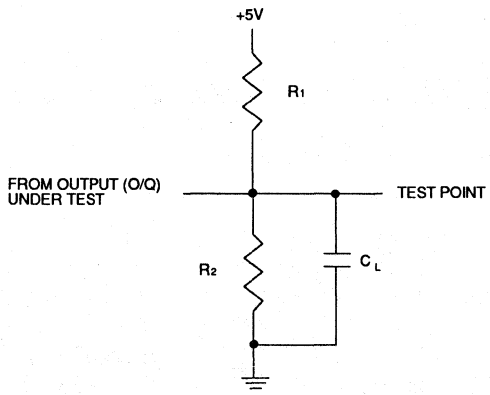
Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress-only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.



CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

COMMERCIAL DEVICES

Refer to AC Test Conditions:

R_2 = 390Ω

1) R_1 = 200Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 200Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 200Ω C_L = 5pF

MILITARY DEVICES

Refer to AC Test Conditions:

R_2 = 750Ω

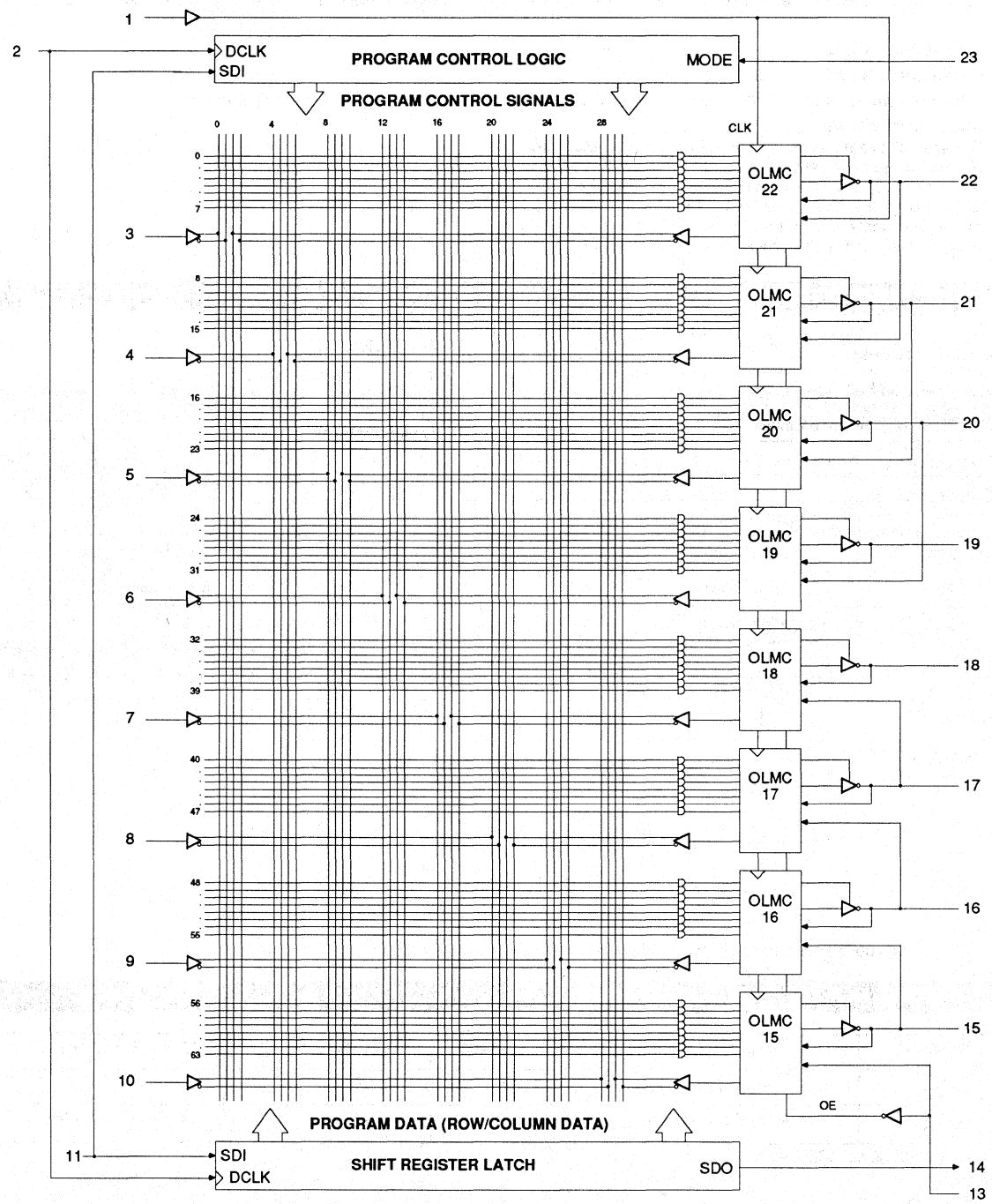
1) R_1 = 390Ω and C_L = 50pF
2) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 50pF
3) Active High R_1 = ∞; Active Low R_1 = 390Ω C_L = 5pF

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

ispGAL16Z8 LOGIC DIAGRAM



2

ELECTRICAL CHARACTERISTICS — ispGAL16Z8-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-20L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-20L Commercial

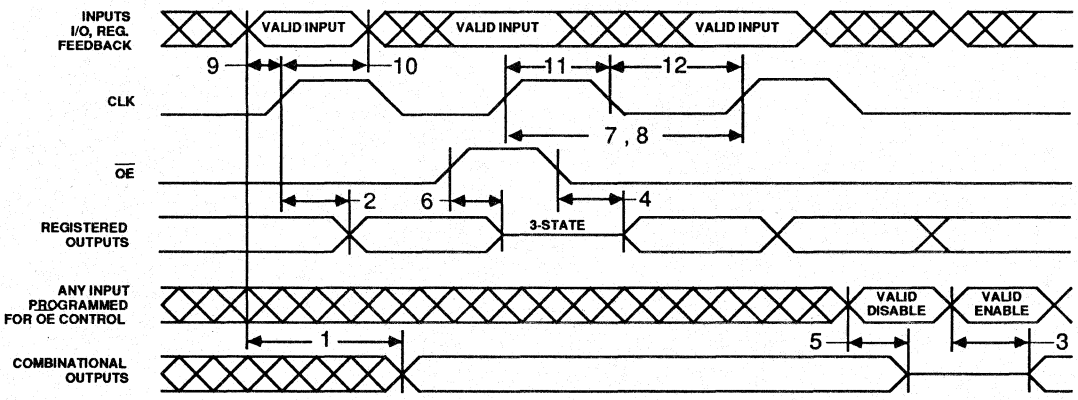
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-20L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	41.6	MHz
	8	Clock Frequency with Feedback	1	0	33.3	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	12	—	ns
	12	Clock Pulse Duration, Low	—	12	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — ispGAL16Z8-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	90	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-25L Commercial

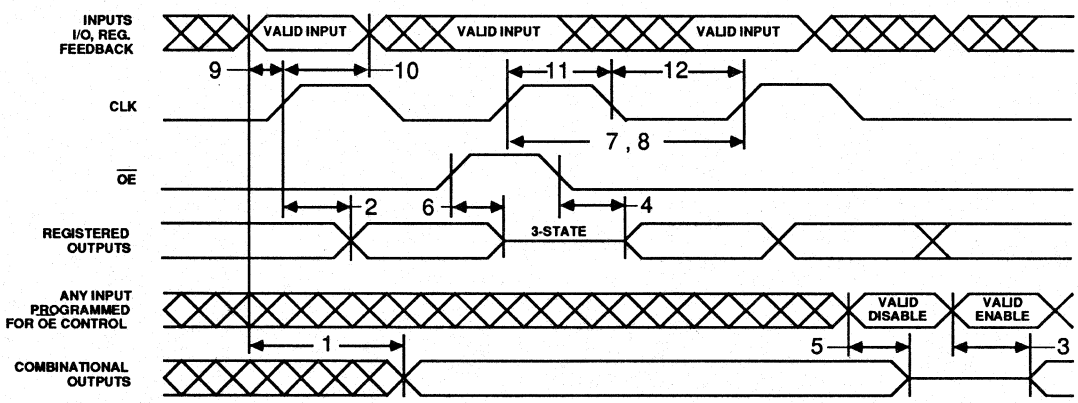
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — ispGAL16Z8-25L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage				0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	110	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	- 40	85	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	24	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-25L Industrial

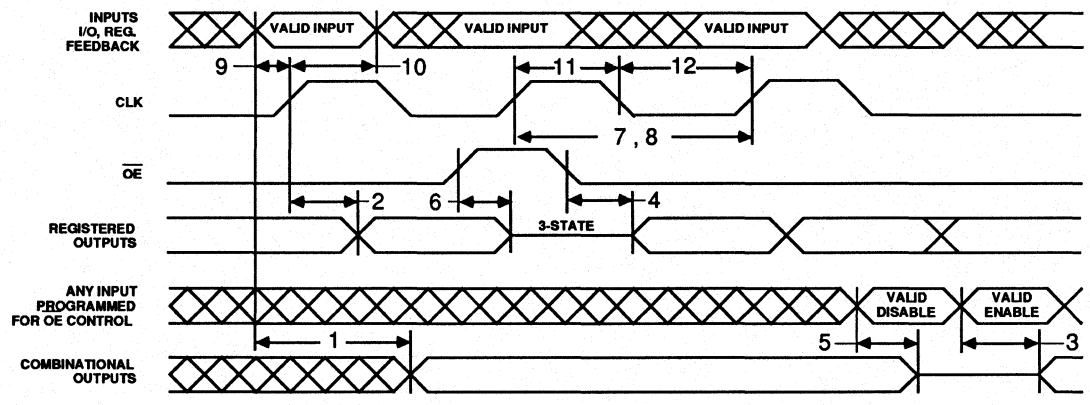
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
	2	CLK	Q	Clock to Output Delay	1	2	15	ns
t_{en}	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t_{dis}	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-25L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	28.5	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

SWITCHING WAVEFORMS



ELECTRICAL CHARACTERISTICS — ispGAL16Z8-30L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T = 25° C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	75	110	mA

1) One output at a time for a maximum duration of one second.

DC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-30L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_C	Ambient Temperature	- 55	125	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	12	mA
I_{OH}	High Level Output Current	—	–2.0	mA

SWITCHING CHARACTERISTICS — ispGAL16Z8-30L Military

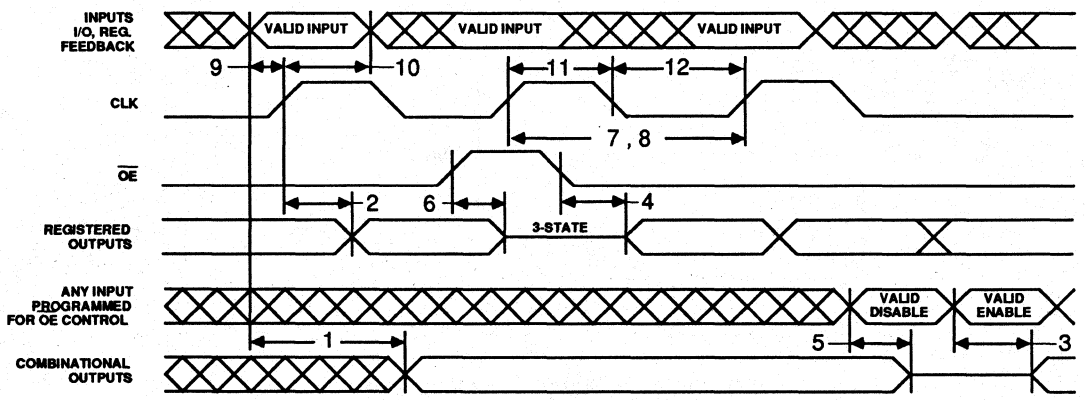
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Combinational Propagation Delay	1	3	30	ns
	2	CLK	Q	Clock to Output Delay	1	2	20	ns
t_{en}	3	I, I/O	O	Output Enable, Z→O	2	—	30	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z→Q	2	—	25	ns
t_{dis}	5	I, I/O	O	Output Disable, O→Z	3	—	30	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q→Z	3	—	25	ns

AC RECOMMENDED OPERATING CONDITIONS — ispGAL16Z8-30L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	7	Clock Frequency without Feedback	1	0	33.3	MHz
	8	Clock Frequency with Feedback	1	0	22.2	MHz
t_{su}	9	Setup Time, Input or Feedback, before CLK↑	—	25	—	ns
t_h	10	Hold Time, Input or Feedback, after CLK↑	—	0	—	ns
t_w	11	Clock Pulse Duration, High	—	15	—	ns
	12	Clock Pulse Duration, Low	—	15	—	ns

SWITCHING WAVEFORMS



OUTPUT LOGIC MACROCELL (OLMC)

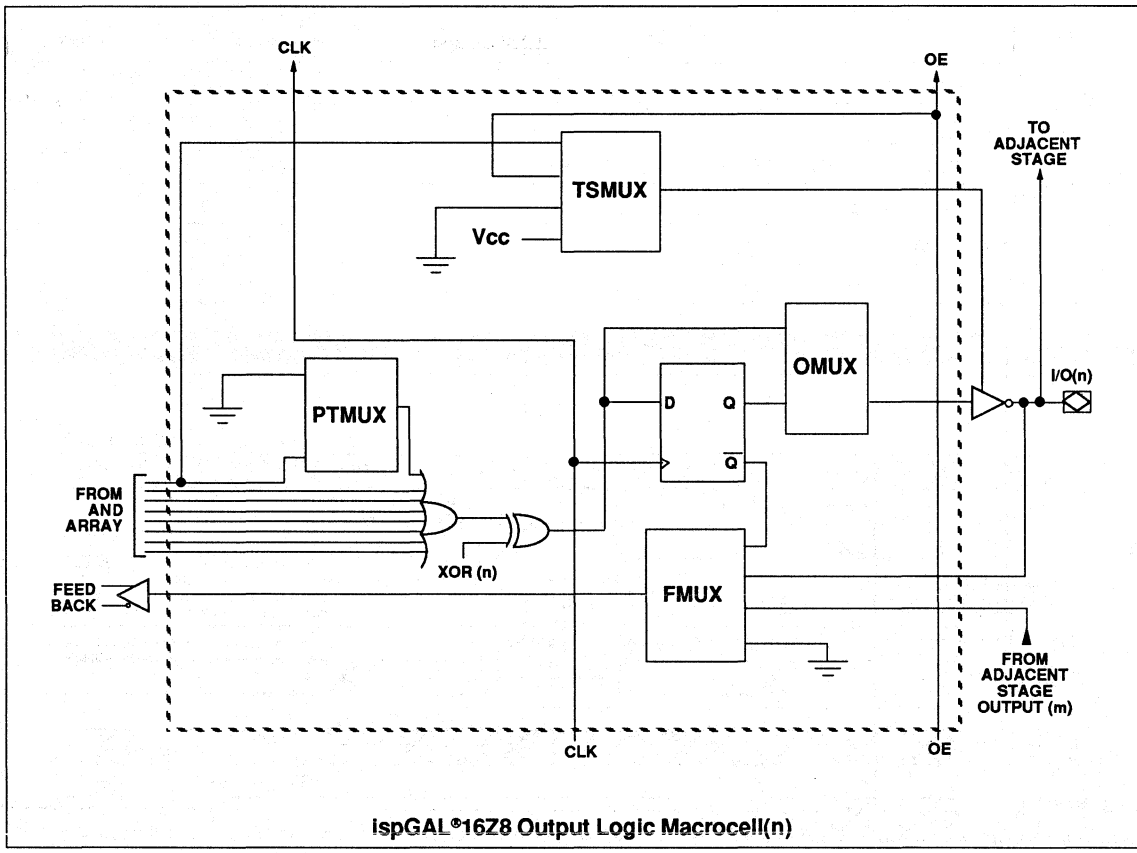
The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

NOTE: See ispGAL16Z8 Programmer's Guide for additional information on in-system OLMC reconfiguration.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous) configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the small mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.



ispGAL®16Z8 Output Logic Macrocell(n)

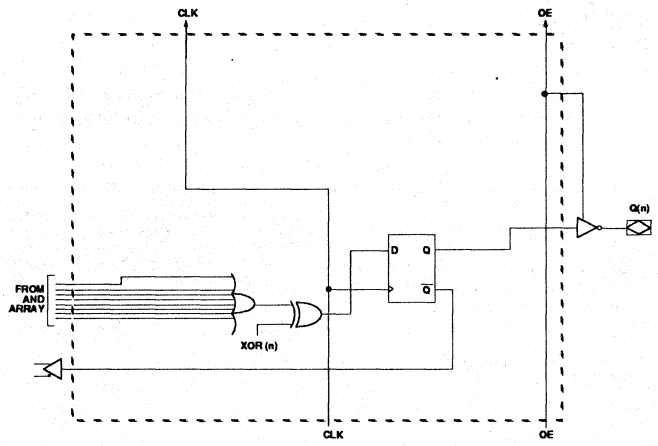
REGISTERED MODE

In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

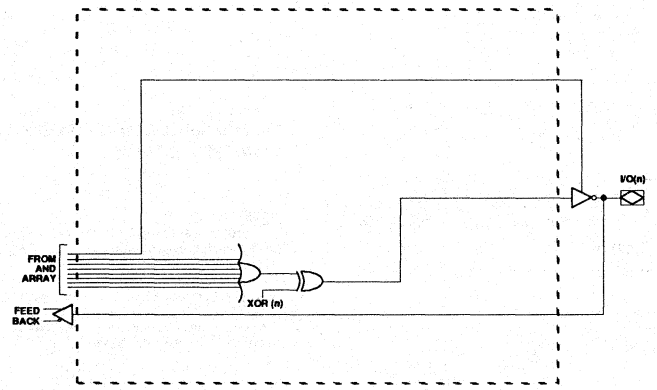
All registered macrocells share common clock and $\overline{OE}$ control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

Registered outputs have 8 data product terms per output. I/O's have 7 data product terms per output.



Registered Output with Programmable Polarity

NOTES:
- All macrocells can be individually configured to this function.
- Polarity of the register input is programmable on a macrocell by macrocell basis.
- Feedback into the AND array is from the $\overline{Q}$ signal of the register with active low and active high feedback paths provided.
- Registered macrocells have common clock (pin 1) and common $\overline{OE}$ (pin 13)



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- All macrocells can be individually configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- All macrocells have active high and active low feedback of the output buffer and/or device pin data into the AND array.
- When all 8 macrocells are configured into the I/O function the CLK and $\overline{OE}$ pins serve no valid logic function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

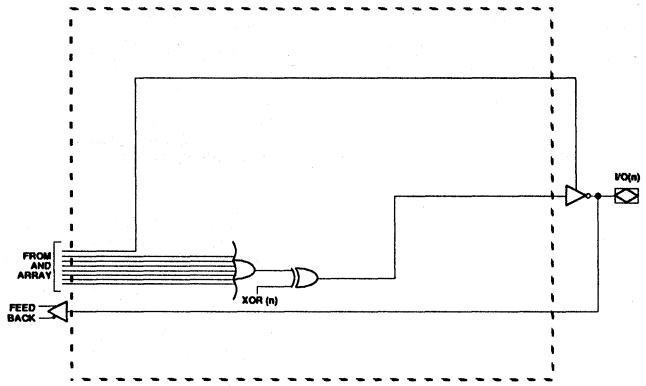
COMPLEX MODE

In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8 and 16P8 devices with programmable polarity in each macrocell.

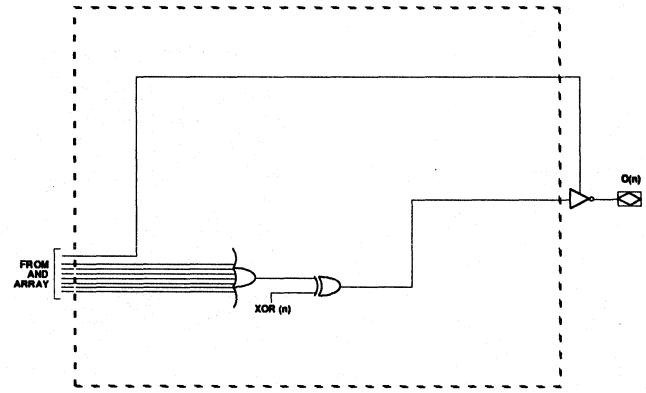
Up to 6 I/O's are possible in this mode. Dedicated inputs or outputs can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 13 are always available as data inputs into the AND array.



Combinational Input/Output with Programmable OE and Polarity

NOTES:
- The outboard macrocells (pins 15 & 22) cannot perform this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.
- Each macrocell has active high and active low feedback of the output buffer and/or device pin data into the AND array.



Combinational Output with Programmable OE and Polarity

NOTES:
- The two outboard macrocells (pins 15 & 22) are permanently configured to this function when in the Complex mode.
- The other 6 macrocells can emulate this mode by not using the feedback data as a data input to the array.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

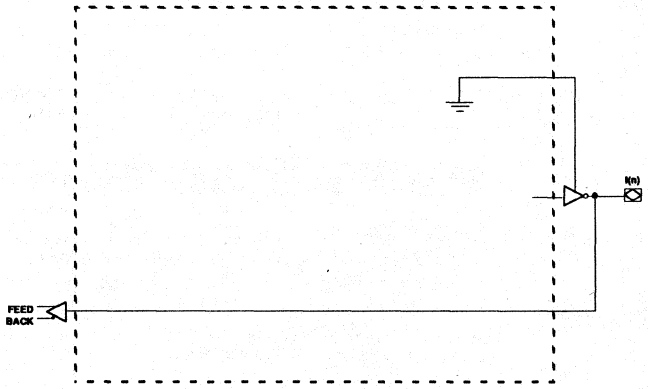
SIMPLE MODE

In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 16P6 devices with many permutations of generic polarity output or input choices.

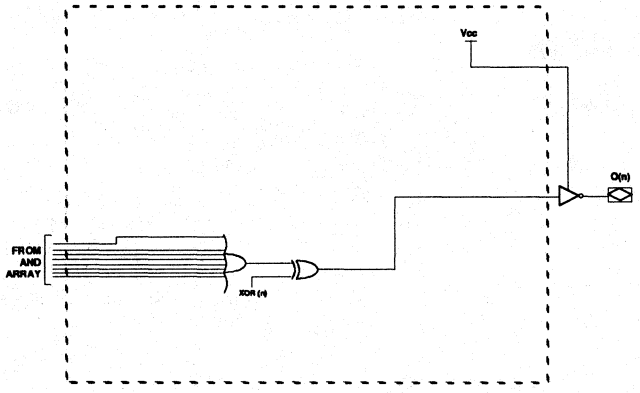
All ouputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 13 are always available as data inputs into the AND array. The "center" two macrocells (pins 15 &16) cannot be used in the input configuration.



Dedicated Input Mode

NOTES:
- The "center" two macrocells (18 & 19) cannot be configured to this function.



Dedicated Combinational Output with Programmable Polarity

NOTES:
- All Macrocells can be configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every ispGAL16Z8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

TC CELL

The ispGAL16Z8 is equipped with a TC (Tri-state Control) cell which allows output driver state control during in-system programming and/or diagnostic mode. In the default setting (logic 1), this cell causes the output state (logic 1, logic 0, or tri-state) to be latched upon entering the programming/diagnostic mode. In the tri-state setting (logic 0), this cell causes all outputs to tri-state upon entering the programming/diagnostic mode.

NOTE: See the ispGAL16Z8 Programmer's Guide for additional information on TC cell programming and functionality.

SECURITY CELL

A security cell is provided with every ispGAL®16Z8 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased.

NOTE: See the ispGAL16Z8 Programmer's Guide for additional information on Bulk Erase procedure.

OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break any feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next-state conditions.

The ispGAL®16Z8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any desired state condition can be forced for test sequencing.

NOTE: See ispGAL16Z8 Programmer's Guide for additional information on registered oriented diagnostic/preload.

LATCH-UP PROTECTION

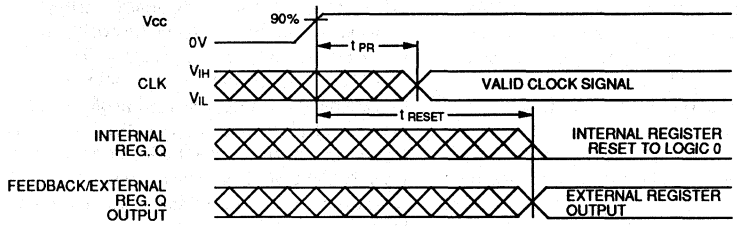
ispGAL®16Z8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullups instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

ispGAL®16Z8 devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, require much less drive current than traditional bipolar devices. This allows for a greater fan out from the driving logic.

ispGAL®16Z8 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the ispGAL®16Z8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs MAX). As a result, the state on the registered output pins (if they are enabled through $\overline{OE}$) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

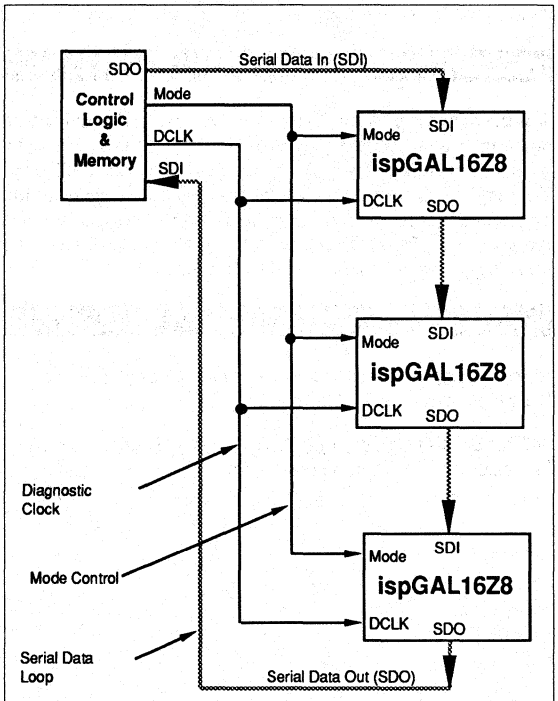
The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the ispGAL®16Z8. First, the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR}, 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

SERIAL PROGRAMMING: LOOP OPERATION

The following figure illustrates a simplified block diagram of a microprocessor system containing three (3) ispGAL16Z8 devices. These devices have been "daisy chained" together to form a serial programming/diagnostic loop. In this configuration, the data bit rate and the DCLK clock frequency are the same. A programming and/or diagnostic bit stream may be shifted through all three (3) devices at the maximum DCLK clock frequency. The ispGAL16Z8 data cells are not dynamic. In other words, there is no minimum DCLK clock frequency.

In this configuration, only four (4) wires are required to access and control an unlimited number of devices. All the functions associated with reprogrammable logic devices are available via this 4-wire interface. An important benefit offered by the ispGAL16Z8 is RFT (Reconfiguration For Test) capability. RFT is a concept pioneered and developed by Lattice Semiconductor. RFT, in brief, is the process of reprogramming Lattice ispGAL devices, in-circuit, to serve as on-board diagnostic test vector drivers and/or receivers. Any pin associated with an OLMC (Output Logic Macro-Cell) can be configured via the 4-wire serial interface to serve as an output or an input. Elementary test vector sequencing or driver/receiver control can be achieved by patterning portions of the ispGAL16Z8 to serve as a micro-control state-machine.

NOTE: See ispGAL16Z8 Programmer's Guide for additional information on RFT (Reconfiguration For Test) functionality.



Typical ispGAL16Z8 Daisy Chain

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Designing with High Speed Logic

INTRODUCTION

Because of the ever increasing speeds of logic devices, logic design engineers are finding themselves confronted with a new set of problems that did not exist with the slower types of logic devices.

With the advent of high speed logic families such as ACT, FACT and even AS devices, logic design engineers are now being faced with a new headache, transmission line effects. Transmission line effects are generated by a combination of factors: slew rate, the distributed inductance and the distributed capacitance of a printed circuit board trace (and its likely propagation delay).

Slew rate has never been of any particular concern to the logic design engineers until recently. TTL logic device manufactures have always specified speed as propagation delay, but have never said much about the device slew rate. For example on a standard bipolar 74LS device the slew rate is appropriately 0.75V/ns. Stated in terms of logic, it takes a bipolar device approximately 3 to 4ns to make a logic transition (0.5V to 2.4V). Where as with the FACT, ACT and AS type devices their edge rates are on the order of 2 to 3V/ns; or in terms of logic, it will take a fast slew rate device 1 to 2ns to complete a TTL logic transition.

NEXT GENERATION LOGIC DESIGNER

With the introduction of fast slew rate TTL compatible devices, printed circuit board design has become an important part of the system design process. The elimination of ringing, crosstalk, and ground bounce in a reliable high speed design can no longer be implemented by two independent contributors. The logic systems designer and the board layout designer must now work hand-in-hand to produce a functional and viable board/system.

The final responsibility for the functionality of the system falls on the design engineer. Therefore this design guide has been compiled for the systems design engineer rather than the board layout designer. It is not the intent of this article to fully explain high speed phenomenon such as transmission line effects but to make the reader aware of potential problems which may occur. Specifically, the necessary compromises and possible trade-offs that must be understood.

The following subjects will be discussed: ground and power planes, general board layout considerations, and transmission lines.

PLANES

GROUND PLANES

Ground planes are no longer "suggested" for reliable board performance, they are required. It is essential to assign at least one layer for a ground plane. The absolute necessity of a ground plane cannot be over stressed. The PCB ground plane should cover as large of an area as possible. A solid ground plane lowers the ground return path impedance as well as the device to device ground pin impedance. The ground plane for high current devices (relays, lamps, motors, and hard-drives) should be separate from the logic ground. This may be accomplished by partitioning the ground plane (see diagram 1). If the ground plane is fragmented, every effort should be made to keep the separations between the planes as narrow as possible. Locate any ground plane separations away from underlaying signal lines to minimize coupling. Fragmented planes can also cause discontinuities in the characteristic impedance of a transmission line (diagram- 1b is an example of a typical printed circuit card configuration). Also keep in mind that through-holes and vias take away from the effective area of the plane.

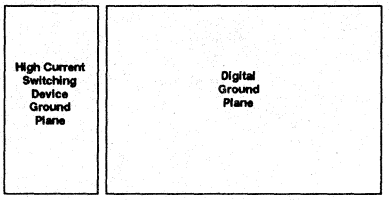


Diagram 1: Fragmented Ground Plane

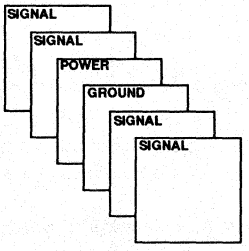


Diagram 1b: Typical Multilayer Printed Circuit Board

POWER PLANE.

Without going into great detail, a power plane is also standard design procedure.

Note: Even though the power plane is at a different potential the concepts are the same as with a ground plane.

SYSTEM GROUND

A good clean (low noise) system ground is also required for reliable system/board performance. It is recommended that at least 10% of the connections on the PC card be connected to the backplane ground to reduce card-to-backplane impedance. A separate ground conductor should be routed for the various sections of the system. For example, all relays, lamps, hard disk and other noise generating devices should have a separate ground path. The system's mechanical package (chassis, panels and cabinet doors) should also have a dedicated ground as well as the logic sections of the system. The three separate grounds then star to a central system ground point usually next to the power supply (see diagram 2).
The center point grounding technique can also be very effective in reducing EMI (Electromagnetic Interference) and RFI (Radio Frequency Interference).

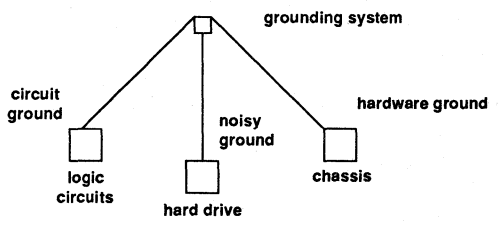


DIAGRAM 2: Common Point Near Power Supply

BOARD LAYOUT

Board layout design is now an important aspect of the design process. The actual logic design may be flawless, but improper implementation (i.e. board layout) can cause the board to be non-functional.
With the high slew rates of todays logic devices, board layout techniques must now be carefully analyzed before they are implemented on to the PCB.

CROSSTALK

High slew rate means high coupling of signals. Crosstalk is the undesirable coupling of a signal on one conductor to a nearby conductor. This signal coupling is made worse if the second trace has a high impedance or if the traces run parallel to one another for more than a few inches and are less than 150 mils apart.

Crosstalk can be catastrophic to a logic design. For example, if there are two traces that run parallel to each other for more than several inches (one of the traces being a clock line and the other being a data line) and if the data line cross couples or super imposes its signal onto the clock line the device the clock is driving may detect a illegal level transition.
The remedies to reduce crosstalk are straight forward, although not particularly elegant. Attenuating the coupling can be achieved by separating the adjacent traces as much as possible. This can become a very difficult task if the design engineer is constrained by the board real estate. Ground stripping or shielding is an effective means of reducing crosstalk. With ground stripping a ground trace is run between the two parallel traces to act as a shield. If ground stripping is used, through holes to the ground plane should be placed at least every 1.0" to 1.5" along the ground strip to eliminate the chance of creating a stub or high frequency antenna. Another method of reducing crosstalk is to effectively lower the impedance of the second trace.

DECOUPLING CAPACITORS

Even with the use of power and ground planes on the PC board decoupling capacitors must be used on every high speed device. The nearly instantaneous change in current requirements caused when a device switches states can cause noise on the V_{CC} plane (especially if a large load is being driven). The high speed logic device requires a nearby current source to prevent any possible lags or noise on the V_{CC} plane. The power plane is unable to supply such a demand therefore a high quality decoupling capacitor is required. A 0.1µF MLC capacitor or RF quality capacitor (low inductance) should be placed on every fast slew rate device and as close to the V_{CC} pin as possible. Dip sockets with built-in decoupling capacitors also work very well in this application.

CIRCUIT LOADING CONSIDERATIONS

When designing with high speed logic, input and output AC loading becomes an important factor of the design. DC loading, previously referred to as Fan-out and Fan-in, is rarely considered with today's state-of-the-art logic devices.
The input capacitive loading of a device is an important parameter that needs to be looked at very closely before choosing a particular device for a design. The input capacitance can greatly effect the overall performance of the logic circuit. To assure proper data sheet performance the total load capacitance that a device drives should not exceed the devices specified capacitive load; most high speed devices maximum loading is 50pF ($C_{load} = C_{out} + C_{in1} + C_{in2} + \ldots + C_{inn}$) (see diagram 3). This does not take into account the distributed capacitance of the line, which is usually negligible for most

designs. As rule of thumb 4 to 6 devices should be the maximum loads per device output for the best speed/load performance. Note that there are devices on the market that have higher output drive capabilities.

BOARD LAYOUT

The single largest offender of improper board layout is the autorouter. Autorouters do a very good job of what they were designed for: trace placement and efficient management of the PC board real estate. However most autorouters do not have the capability to determine which devices are considered high speed and which devices are not. This is where the logic designer must step in and hand layout the devices or islands of high speed logic that must conform to the high speed design techniques that have been discussed to this point.

TRANSMISSION LINE THEORY

To be successful in designing with high speed logic, a basic understanding of transmission lines and proper termination techniques is required. Any connection between two devices within a high speed design should be considered as a transmission line. Because of the high ratio of rise time to propagation delay time of the line, signal lines for slow speed logic circuits may be several feet long without signal distortion. However, as edge rates increase with faster forms of logic devices, the line lengths (propagation delays) must be shorter, or proper termination must be incorporated in order to retain signal purity (free of under-shoot and over-shoot).

For diagram 4 the rise time, (t_r), is less than the line propagation delay (T_D). In other words, a complete TTL level transition will occur before the pulse is received at the receiving end of the line; therefore reflections (ringing) will occur. The voltage change at point A on the line can be expressed by equation 1 below.

equation 1

$$\Delta V_A = \Delta V_{int} \cdot (Z_o / (R_o + Z_o))$$

Where: V_{int} = internal voltage on the output of the driver.
R_o = output impedance of the driving gate.
R_L = load impedance.
Z_0 = the characteristic line impedance.
V_A = the source voltage at the sending end of the line

Note that the equation result is expressed as ΔV_A. It is the dV/dt that introduces the transmission line effects on to the line. Since R_o is so small when compared to the line impedance (Z_0) the change in voltage at point A (ΔV_A) will be approximately equal to the change in internal voltage (ΔV_{int}). This voltage transition (ΔV_A) propagates down the line and is seen at point B after the line propagation delay, T_D. If the rise time, t_r, is less then the line delay, T_D, the line will become reflective. At a closer look, ΔV_A arrives at point B, at T_D later; but unless $R_L = Z_O$, a portion of the wave will be reflected back towards point A. This voltage reflection is dependent on two variables, R_L and Z_o.

equation 2

$$\rho_L = (R_L - Z_o) / (R_L + Z_o)$$

Where the voltage reflection coefficient, ρ (rho), is defined by equation 3

equation 3

$$\rho = V_{REFLECTED} / V_{INCIDENT}$$

It should be evident after examining equation 2, that $-1 \leq \rho \leq 1$.

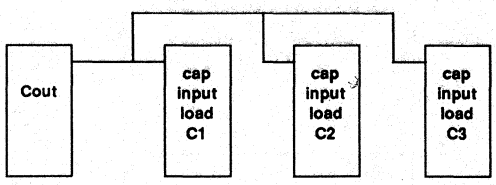


DIAGRAM 3: Capacitive Loading

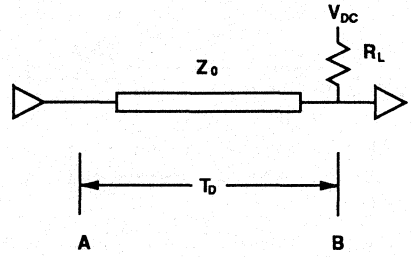


DIAGRAM 4: Transmission Line Model

Therefore equation 3 demonstrates that the reflected voltage can be as large as the incident voltage and of either positive or negative polarity. The above explanation will also hold true for the sending end of the line as shown in equation 4.

equation 4

$$\rho_S = (R_o - Z_o)/(R_o + Z_o)$$

The instances where ringing will not occur is when the printed circuit board trace is impedance matched (properly terminated line, $Z_o = R_L$). The second case is where the line is sufficientlly short enough that the level tansistion can not be completed within the time that is required for the pulse to reach the recieving end on the line. It should also be noted that both the sending end and the receiving end of the transmission line may reflect.

UNTERMINATED LINES

Diagram 5 shows a transmission line referred to as an "open line," a "stub" or "unterminated line". The unterminated line has no load impedance (R_L) and is therefore a impedance mismatched line. The behavior of this line (if connected to a fast slew rate device) is as follows. At time zero an initial TTL voltage transition occurs at point A (2.5Vdc to 0.5Vdc). Time T_D later, the signal reaches point B and is reflected by ρ_L. The input impedance is very high with respect to Z_o therefore R_L is approximately equal to infinity ($R_L \approx \infty$),

$$\rho_L \approx (\infty - Z_o) / (\infty + Z_o)$$

equation 5

$$\rho_L = 1$$

Solving for the reflected voltage from equation 3, it is discovered that the reflected voltage is equal to the incident voltage.

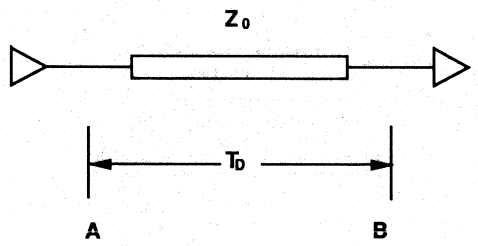


DIAGRAM 5: Unterminated Transmission Line

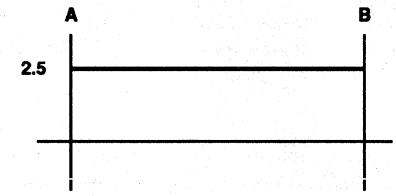


DIAGRAM 6: t = 0 -

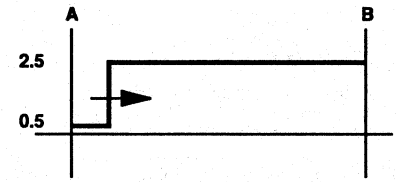


DIAGRAM 7: t = 0+

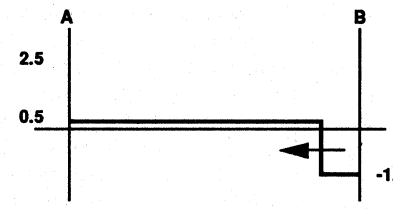


DIAGRAM 8: t = T_D+

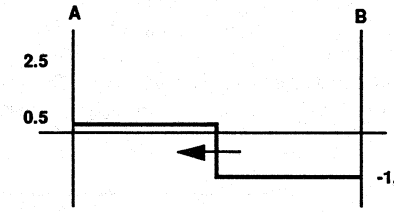


DIAGRAM 9: t = 1.5 T_D

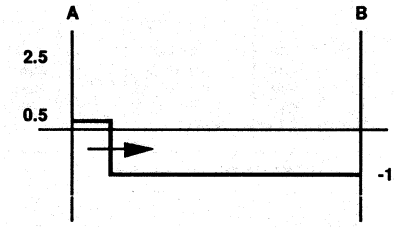


DIAGRAM 10: t = 2 T_D+

Repeating the above calculations for the sending end of the line (point A), where $R_o \approx 0$ then

$$p_s \approx (0 - Z_o)/(0 + Z_o)$$
$$p_s \approx -1$$

At point A there is also a reflection but it is negative in magnitude (reflected voltage ($V_{REFLECTED}$) = -1 • incident voltage ($V_{INCIDENT}$). The voltage transistion scenario can be discribed as (refer to diagram 6):

1) At t = 0 the gate at point A makes a level transition from a logic 1 to a logic 0 (refer to diagram 7), then

ΔV_A = Voltage low - Voltage high
0.5Vdc - 2.5Vdc = -2.0Vdc.

2) The -2V voltage step or pulse travels down the line until it reaches point B in time (T_D). At time T_D a reflected pulse of -2V now travels back towards point A creating a -2.0V reflection toward the sending end (refer to diagram 8 and 9).

$$\Delta V_A = V_{INCIDENT} + V_{REFLECTED}$$
$$\Delta V_A = -2V + -2V = -4V.$$

3) At t = $2T_D$ the pulse hits the sending end of the line and reflects back according to the reflection coefficient p_s. Note the incident voltage $V_{INCIDENT}$ = -2V, the reflected voltage $V_{REFLECTED}$ can be found by manipulating equation 3 to produce equation 7, don't forget that the 0.5V is a DC offset (refer to diagram 10).

equation 6

$$V_{REFLECTED} = p_s \cdot V_{INCIDENT}$$

$$-1V \cdot -2V = 2V$$

equation 7

$$\Delta V_A = V_{INCIDENT} + V_{REFLECTED}$$
$$-2V + 2 = 0V$$

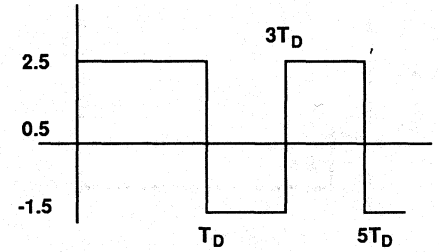


DIAGRAM 11: Load Voltage Waveform

4) At $3T_D$ another reflection occurs at point B with the $V_{INCIDENT}$ equal to 2V. The $V_{REFLECTED}$ is equal to 2V, therefore, ΔV_A is equal to 4V.

If point B was observed instead of the entire line the waveform would appear as in diagram 11. Diagram12 is a lattice diagram for the reflection that would be observed.

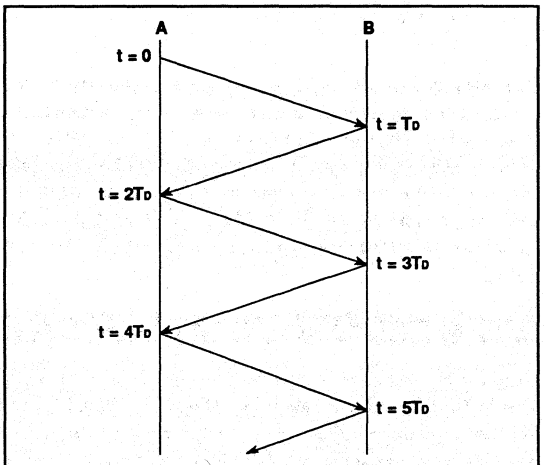


DIAGRAM 12: Typical Reflection Example

The assumptions throughout this discussion have been ideal conditions and first approximations. If output impedance, finite input impedance, and various other conditions relating to the transmission line were considered then p_L will in reality have a value less than that of 1.Similarly, p_s will be greater than -1 under these conditions. Thus the reflections will become successively smaller, causing the condition that is known as ringing (refer to diagram 13). If the ringing effect is large enough in amplitude it can cause the receiving device to see an illegal level transition, which could have catastrophic effects on the logic design. Or in some cases if the amplitude of the ringing is large enough that it actually damages the input of the recieving device.

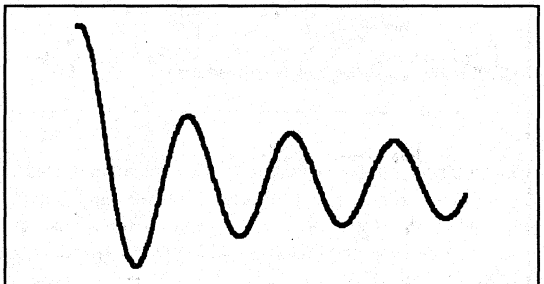


DIAGRAM 13: Ringing Diagram

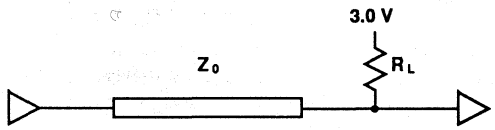


DIAGRAM 14: Parallel Termination

PARALLEL TERMINATION

Parallel termination refers to a line which is terminated at the receiving end of the transmission line with a resistor that is chosen to match the characteristic line impedance, Z_o.

In the configuration in diagram 14, $R_L = Z_o$ and R_L is pulled up to 3V DC (in theory R_L could be tied to ground but TTL compatable devices could not supply the necessary drive). The drawback to diagram 14 is that a 3V supply is required. Solving for p_L from equation 2 it can be found that $p_L = 0$. This indicates that there are no reflections or distortions on the line. When a voltage transition is propagated from point A to point B, it stops at the receiving device side. Other than the time delay T_D, the line will act as if it were a DC circuit. It is important to note that even though devices or gates may be placed at any location on the line, the terminating resistor should be placed at the virtual end of the line.

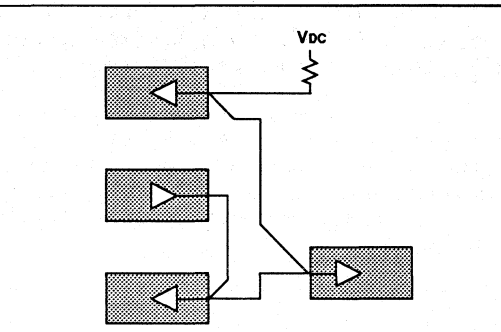


DIAGRAM 15: Correct Terminating

The 3.0V power source of diagram 14 is a major draw back but R_L can be theveninized. Diagram 16 shows the electrically equivalent circuit that is easily implemented into the board design. However, the circuit in diagram 16 will dissipate additional power.

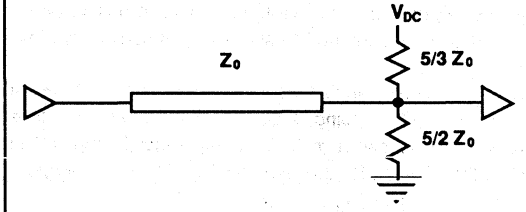


DIAGRAM 16: Thevenin Termination

There exists a third type of parallel termination as shown in diagram 17. A capacitor is placed between the DC power source and the terminating resistor. The recommend value is a 0.1μF MLC type. In this configuration the circuit will dissipate only AC power as opposed to the pull-up pull-down circuit which burns DC power. Several manufactures produce both the capacitor/resistor and pull-up/pull-down termination packs. The pull-up/pull-down packs usually come in a SIP (Single Inline Package) with 0.1 centers, while the capacitor/resistor combination come in a DIP (Dual Inline Package) 16-pin package. The most common SIP pull-up-pulldown resistor values are 220Ω/330Ω, 330Ω/470Ω combinations. Dale Electronics and Murata, to name a few, are vendors that supply the above packages.

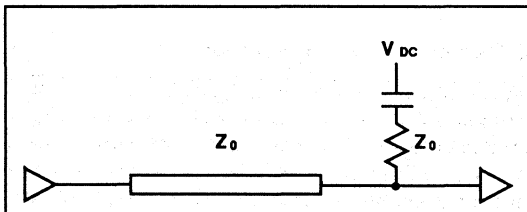


DIAGRAM 17: AC Equivalent

SERIES TERMINATION

A less widely used method of terminating a line in logic design is to serially terminate the line at the sending end of the line.

The idea in serially terminating a transmission line is to make $p_S = 0$ and $p_L = 1$. In doing so sets the $R_L = \infty$. With this type of termination no load termination is required only source load termination. Adding R_S then causes $R_S + R_O = Z_o$. Therefore adding R_S changes ΔV_A.

$$\Delta V_A = \Delta V_{INCIDENT} (Z_o / (R_o + R_S + Z_o))$$

$$\Delta V_A \approx \Delta V_{INCIDENT} \cdot 1/2$$

Notice in diagram 18 that ΔV_A is now half of ΔV_{int}.

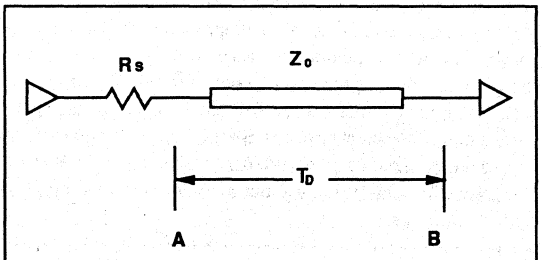


DIAGRAM 18: Series Termination

Because of the voltage divider of R_S and Z_o, ΔV_A is one half a transition. This pulse travels down the line, and at time T_D, is reflected by $p_L = 1$. Since the receiving end is unterminated, $\Delta V_A = 2 \Delta V_B$. This means that half a pulse was sent down the line and half a pulse is sent back. At the receiving end the only thing seen is a full size pulse because of the instant doubling effect of $p_L = 1$.

This may seem a little unusual, but the reflected voltage is expected to double the voltage on the transmission line (see diagram 19).

The major disadvantage of series termination is that the receiving gate or gates must be at the end of the line i.e. no distributed loading. The obvious advantage that series termination has over parallel termination is there is no need for an additional supply (the +3v) and the savings in power.

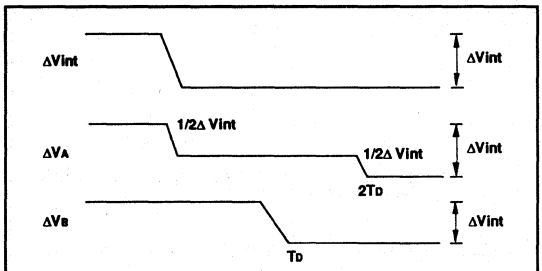


DIAGRAM 19: Transmission Line Voltage

PROPAGATION DELAY

Rise time of a gate is t_r, and T_D is the propagation delay from point A to point B. For most of the state of the art, high speed logic devices a typical t_r may be 2ns for a good clean TTL voltage transition. For a printed circuit board with a continuous ground plane and a signal trace on the adjacent layer, the propagation delay is dependent on only one variable, the dielectric constant of the board material.

equation 8

$$tpd = 1.017 \sqrt{0.475\, e_r + 0.67} \text{ ns/ft}$$

Where tpd is the propagation delay of the transmission line in ns/ft. For a typical board constructed of FR4 material, e_r (dielectric constant) is 4.7 to 4.9 If an average e_r of 4.8 is used in equation 8, then the tpd = 1.75 ns/ft. If a signal run is 12 inches long, it will take 1.75 ns for a voltage transition to travel from point A to point B, therefore, T_D = 1.75 ns. As a rule of thumb, any line that is over 7" long should be suspected of being a transmission line and delt with accordingly.

TEN RULES TO FOLLOW

1) When using high speed logic, signal interconnections should be kept as short as possible.

2) A multilayer printed circuit board is required.

3) Ground and power planes are required.

4) A separate ground for the high current switching devices should be provided.

5) Decoupling capacitors are required on every high speed logic device (0.1µF MLC type) located as close to the V_{CC} pin as possible.

6) Provide maximum possible spacing among all high speed parallel signal leads.

7) Terminate high speed signal lines where tr < T_D.

8) Beware of AC loading conditions within the design. Exceeding the manufacturers recommended operating conditions, particularly capacitance, can cause problems. Also, create islands of high speed devices on the PC board. This simplifies board layout and "ropes off" the high speed areas.

9) When using parallel termination serpentine all high speed signal runs that go to more than one load. Use a termination load at the absolute end of the line (refer to diagram 21).

10) Sharp bends in the transmission line and discontinuities in the ground plane should be avoided because reflections can occur from abrupt changes in the characteristic impedance.

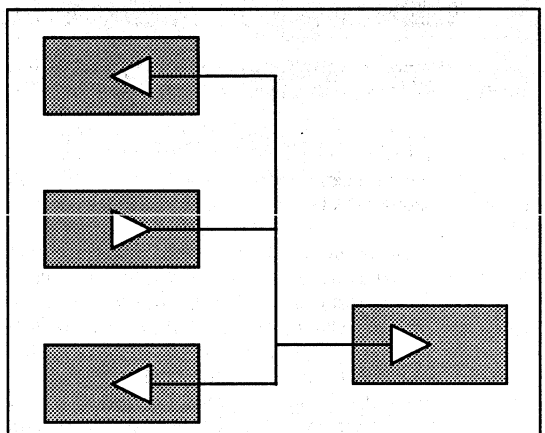


DIAGRAM 20: Not Recommended Terminating

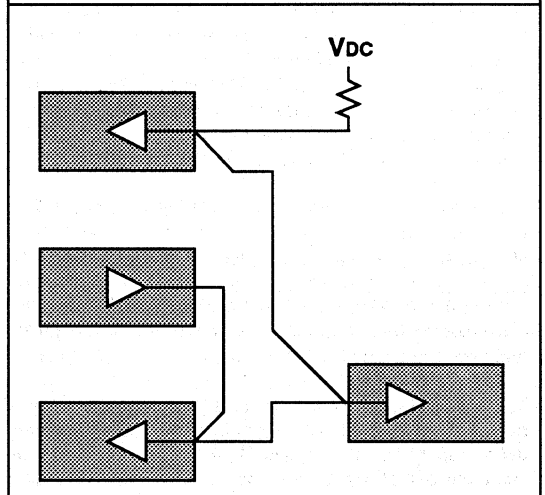


DIAGRAM 21: Correct Terminating

END

GAL METASTABILITY REPORT

INTRODUCTION

The dictionary definition of metastability is "a situation that is characterized by a slight margin of stability." When applied to bi-stable (digital) logic, the term refers to an undesirable marginally stable output state between VIL max and VIH min.

Metastability can occur in bi-stable storage elements (registers, latches, memories, etc.) when setup and/or hold times are violated. Since setup and hold times vary with temperature and operating voltage, among other factors, the times referred to here are not the min/max numbers printed in data sheets, but rather the actual times for the given set of operating conditions. Typical applications where such times are likely to be violated include bus & memory arbiters, interfaces, synchronizers, and other state machines employing asynchronous inputs or asynchronous clocks.

Metastability manifests itself in a number of different ways. Common responses are (shown as they might be captured on a digital oscilloscope in Figure 1): runt pulse (1a), decreased output slew rate (1b), output oscillation (1c), and increased clock-to-output time (1d). By definition, the phenomenon of metastability is statistical in nature. Not only is entry into the state uncertain, but the time spent there is also variable.

Because PLDs are commonplace in today's designs, a thorough understanding of their metastable behavior is crucial. In some applications, output anomalies shorter than one clock cycle may be acceptable, but in applications where the register output is used as a control signal (clock, bus grant, chip select, etc.) for other circuitry, faults such as runt pulses and oscillation cannot be tolerated.

This report will not study the causes or characteristics of metastability in great detail; excellent material has already been prepared on this subject [1-5]. Rather, this report will introduce a mathematical model for the metastable phenomenon, discuss potential test methodologies, present and compare test results from various bipolar and CMOS PLDs, and discuss how to interpret the data. This report will close with suggestions on how to design metastable tolerant systems.

DERIVATION OF CONSTANTS

The basic premise of all metastability models is that a device's output is more likely to have settled to a valid state in time(t) than in time(t-n). In fact, the failure probability distribution follows an exponential curve. Figure 2 shows a typical failure frequency plot.

It is accepted [1] that metastable failures can be accurately modeled by the equation:

$$\log \text{Failure} = \log \text{MAX} - b(\Delta - \Delta o) \qquad (1)$$

In this equation, MAX represents the maximum failure rate for a particular environment, Δ is the time delayed before sampling the DUT (Device Under Test) output, and Δo is the time at which the number of failures starts to decrease. On a failure frequency plot (such as the one in Figure 2), Δo represents the knee of the curve. The constant b is rate at which the frequency of failures decreases after the knee is reached.

Recall that:

$$\log X = a \ln (X), \text{ where } a = \log (e)$$

Substituting this into (1):

$$a \cdot \ln \text{Failure} = a \cdot \ln \text{MAX} - b(\Delta - \Delta o) \qquad (2)$$

MAX is related to the clock frequency (fCLOCK) and data frequency (fDATA). That is,

$$\text{MAX} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) \qquad (3)$$

Substituting (3) into (2) and applying some algebra:

$$a \cdot \ln \text{Failure} = a \cdot \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) - b(\Delta - \Delta o)$$

$$\ln \text{Failure} - \ln (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) = -b/a(\Delta - \Delta o)$$

Setting k2 = b/a and rearranging the equation yields:

$$\text{Failure} = (k1 \cdot \text{fCLOCK} \cdot \text{fDATA}) e^{-k2} (\Delta - \Delta o) \qquad (4)$$

When used with equation (4), the constants k1, k2, and Δo, completely describe a particular device's metastable characteristics; they indicate how quickly a device can resolve the metastable condition. Devices which transition out of the metastable region quickly are characterized by a small Δo and a large k2.

The constant k1 is peculiar to the test apparatus (it can be thought of as a "scaling factor"). The maximum metastable failure rate (MAX) is limited by fCLOCK; a failure cannot occur if the device isn't clocked. Likewise, it is true that a metastable failure cannot occur unless data has changed. So, if fDATA < fCLOCK, then MAX = fDATA. This was the case in the test fixture Lattice used (fCLOCK=10MHZ, fDATA=2.5MHz). Substituting MAX = fDATA back into equation (3) yields: k1 = 1/fCLOCK, so k1 = 100ns for our tests.

TEST FIXTURE

The goal of testing a particular device's metastable characteristics is to generate real numbers for the constants k2 and Δo. To do this, the device must first be forced into the metastable state. This is done by intentionally violating setup and/or hold times. Once metastable, the output can be observed on an oscilloscope or used to increment an event counter.

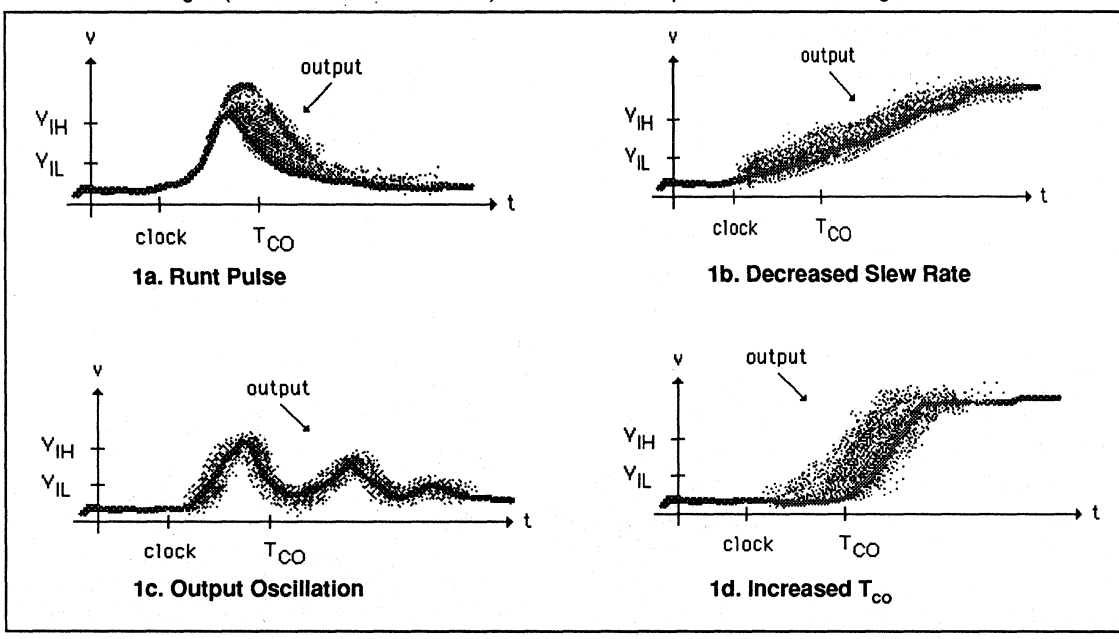
Traditional Approach

One approach to characterizing a device's metastable behavior employs a test fixture similar to that shown in Figure 3a. In such a fixture, data to the device includes a "jitter band" so that the device sees changing data as it is clocked. The DUT output is fed to a window comparator to determine when it is in the metastable region (between VIL max and VIH min). The comparator output can be sampled periodically and used to increment an event counter.

This method of testing, though it directly yields MTBF numbers, has some drawbacks. The first is that it does not distinguish between the different types of metastable behavior (runt pulse, oscillation, slow rise/fall time, delayed transition), and it may have difficulty detecting every type. Also, the registers used in the detector circuit itself may become metastable, which would adversely affect the results.

A New Approach

The test method used to gather data for this report used the circuit shown in Figure 3b. The tester employed an "infinite precision" variable delay circuit to control clock placement with respect to data. This arrangement allowed exact worst



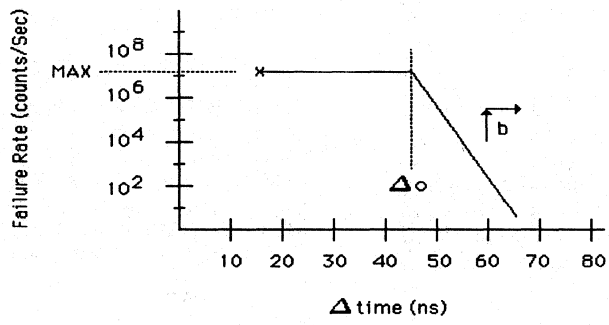


Figure 2. Typical Failure Frequency Plot

case placement of the clock, so as to induce metastability with nearly every clock pulse.

Using a digital oscilloscope (Tektronix 11402) in point accumulate mode, metastable failures were recorded over a lengthy period of time. A hardcopy was then made and the constants empirically obtained (details below).

The oscilloscope approach, being visual in nature, enables the designer to make educated decisions regarding maximum clock and data rates, as well as the suitability of using the output to drive other circuitry. The five minute sample period used in our tests contained approximately 750 million failures. Much longer sample periods were evaluated, but they provided no perceptible gain in usable information.

A slight disadvantage of this approach is that extracting k2 and Δo values from the hardcopies is not straightforward. Because each point on the hardcopy can represent any number of actual samples (between one and 1.5 million), one cannot simply count the points at time(t) for the MTBF at that time (although, in the case of the scattered points, the probability is low that a single isolated point represents more than one sample).

To generate values for k2 and Δo, it was necessary to refer to previous metastability studies [1]. By studying the output plots of devices with known constants, certain relationships were established. For example, it was determined that Δo represents the time from the leading edge of the output until the "dot density" starts to decrease measurably. It should be noted that Δo in previous studies included device propagation delays, whereas in our test it does not.

The time from Δo until the dot density equals zero was defined to be the "time to metastable release" or simply time(r). The relationship between k2 and time(r) is given below in (5), and shown graphically in Figure 4. Recall that MAX=2.5x10^6 and a=log(e).

$$k2 = \log(MAX) / (time(r) \cdot a) = 14.73/time(r) \qquad (5)$$

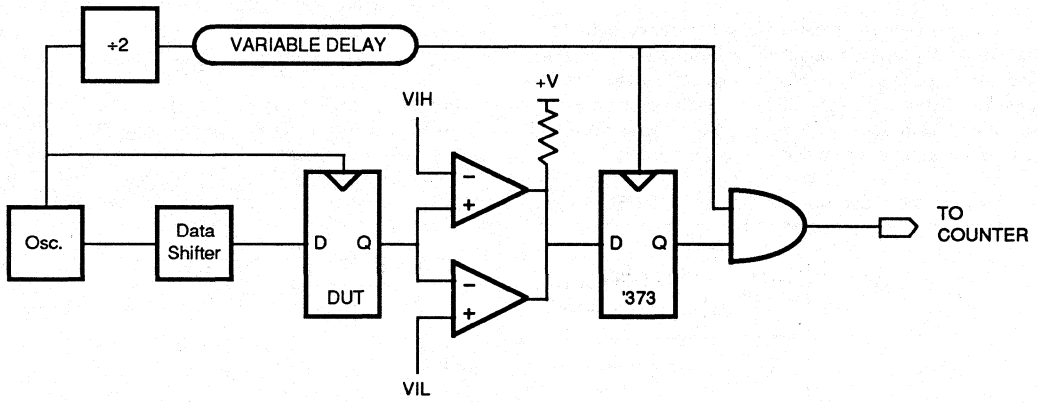


Figure 3a. Traditional Metastability Test Circuit

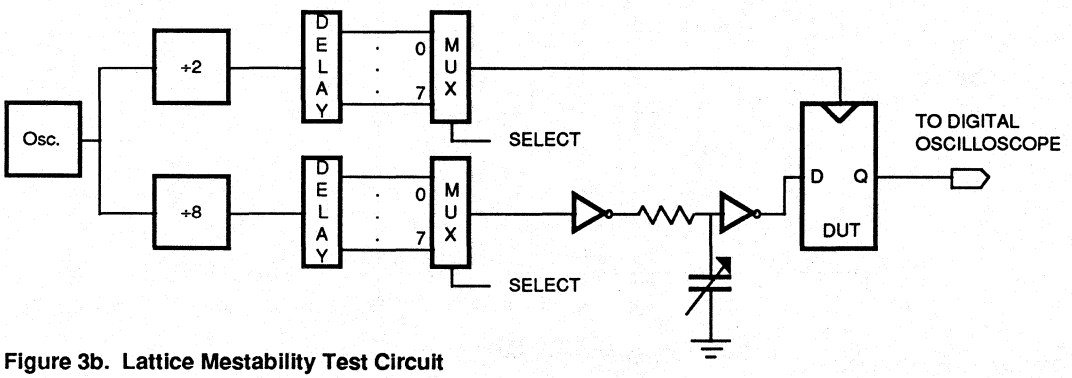


Figure 3b. Lattice Mestability Test Circuit

INTERPRETING THE RESULTS

In addition to examining E²CMOS GAL devices, this study also tested several bipolar PAL devices as well as other CMOS PLDs. To insure that the results of this study would be relevant, all necessary precautions were observed: the devices were of recent vintage and were acquired blindly through distributors; multiple samples of each device were tested and the results combined; all devices had either fixed 16R8 architectures or were configured to emulate the 16R8 architecture; the devices were programmed from the same JEDEC fuse map file (the source equations and the JEDEC fuse map file are presented in Listing 1).

Plots 1 through 4 on the following pages are some of the oscilloscope plots generated for this study. The top waveform in each plot is the clock signal and the middle trace is the data input. The horizontal scale is 10ns per division, so the exact data setup time that caused the metastable condition can be read directly. The vertical scale is 2V per division for the top two traces, and 1V per division for the bottom trace. Only the bottom trace is aligned with the voltage scale on the left margin of the plot.

The bottom waveform in each plot is the device output (the only signal captured in point accumulate mode). In every case, the output signal plot shows two stable levels after the transition. This is a direct result of the "indecision" caused by metastability; on some cycles the output settled to a high level, while on others it settled to a low level.

Plot 1 shows the response of a bipolar PAL16R8B (15ns). Notice the very well defined runt pulse (this correlates with previous data gathered on similar devices by the manufacturer [1]). The absence of a secondary trace along ground indicates that the output always starts to transition to a high level, even when it finally settles to a low level. This characteristic makes the device unsuitable for use in control path applications (when metastability is possible). All of the bipolar parts examined showed similar results.

Plot 2 is from a UV-EPLD. This CMOS device, as did all CMOS PLDs Lattice tested, exhibited characteristics far superior to bipolar parts. This can be attributed, in part, to the higher switching speed of CMOS logic. GAL devices, for example, have output slew rates approaching 5V/ns, compared to about 1V/ns for bipolar devices.

Plot 3 is from a GAL16V8-15 and Plot 4 is from a GAL6001. Aside from the fact that setup time violations may cause tCO to increase by a small (but random) amount, the outputs are very clean and well behaved. The fact that there are no runt pulses or other anomalies is extremely significant, as the GAL6001 not only allows asynchronous clocking, but encourages that activity. Compare Plots 3 & 4 with Plot 2. Just as the characteristics of CMOS PLDs (in general) are superior to those of bipolar PLDs, the metastable response of GAL devices is noticeably better than that of UV-CMOS EPLDs.

For reference purposes, Plots 5 through 7 are included. Plot 6 shows a normal (ie. non-metastable) GAL16V8-15 transition, and Plot 7 a normal PAL16R8B transition. Plot 5 is from a TTL flip-flop (TI 7474). For consistency, only rising edges have been shown. Our tests also covered falling edges which,

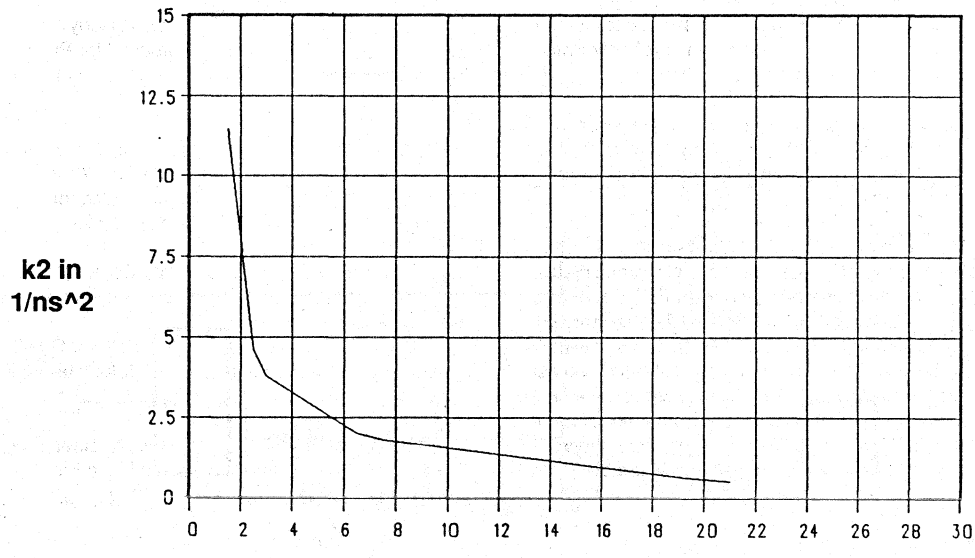


Figure 4. K2 Contstant

in general, were interesting but did not provide any additional information.

For a more quantitative look at the phenomenon of metastability, refer to the table beneath each plot. These tables list the measured values of the constants Δo and k2 for the device whose plot is shown, and for similar devices. Recall that large k2 and small Δo values are desirable. The numbers in the tables correlate closely with the results of earlier tests [1,5], confirming the validity of our test method.

Since all current GAL devices possess very similar register and output buffer circuitry, and all are fabricated using the same basic process, the data shown in Table 1 for the GAL16V8 is considered applicable to all devices and speed grades in the GAL family.

USING THE RESULTS

If a register enters the metastable state in a system, then data was obviously unstable as the register was being clocked. The argument over which data should have been captured (old or new) is academic as the register will randomly pick one or the other. Signals in most asynchronous systems are active for more than one clock cycle, so if they are missed initially, they could be captured on a subsequent clock cycle.

It is the task of the state machine designer to take adequate precautions against metastability causing illegal states to be entered. One way to do this is by using "gray codes" when ordering states. Gray code state equations allow only one state bit to change during a state transition. Thus, the worst metastability could do would be to delay a state transition by one clock cycle. If more than one bit were allowed to change, the outcome would be purely random, and probably illegal. Figure 5 shows examples of both cases.

Other solutions are to externally (or internally) synchronize the asynchronous signals, or to increase cycle times to allow time for metastable outputs to settle. An example of the latter solution is given below.

It is worth noting at this point that state machines (synchronous or asynchronous) can fail for reasons other than metastability. A not insignificant component of a PLD's specified setup time is directly attributable to internal data skewing [2]. Data skewing is the inevitable result of differing signal path lengths, loading conditions, and gate delays. Stated another way, each input to output path has its own set of actual AC specifications. If insufficient setup time has passed, different "versions" of the same data may be present at the inputs of different registers as they are clocked. A good example of this is:

```
Output_Pin19 := Input_Pin2;
Output_Pin15 := !Input_Pin2;
```

If clocked at precisely the right moment after an input transition, one register will capture old data while the other captures new data, resulting in a system failure. This condition, though also the result of a setup time violation, should not be confused with metastability (the "incorrect" data that is captured has normal output characteristics); it is, pure and simply, the result of a violation of specifications. Incidentally, there is less than 1.5ns of skew between the various paths through a 15ns GAL device.

Example

To determine the maximum clock rate (given an acceptable error rate) that a particular device will allow in an asynchronous environment, equation (4) is used. For example, the system shown in Figure 6 utilizes a 9600 baud (bits/sec) asynchronous data stream. The system clock period is tCO+tPD+tSU+Δ. For one failure per year:

$$3.2\text{x}10\text{-}8 = [(1\text{x}10\text{-}7)(1/(\Delta+49))(9600)]e^{-[8(\Delta-2)]}$$

Solving for Δ yields Δ=2.796ns, or about 3ns, for a cycle time of 52ns. Referring back to Plot 2, the additional delay of 3ns intuitively makes sense. Remember, in terms of setup and hold time violations, the oscilloscope plots were made under worst case failure conditions; the scattered dots could represent MTBFs of days, years, or even millenniums in a typical asynchronous environment.

Due to the extremely quick metastable settling times of GAL devices, a relatively small increase in the cycle time will produce a dramatic improvement in reliability.

BIBLIOGRAPHY

1. D.M.Tavana (MMI), "Metastability - A study of the Anomalous Behavior of Synchronizer Circuits," in: Programmable Array Logic Handbook, Monolithic Memories Inc., 1986, pp 11-13 - 11-16.

2. K.Rubin (Force Computers), "Metastability Testing in PALs," Wescon/87 Conference Record (San Francisco, November 17-19, 1987). Los Angeles: Electronics Conventions Management, Inc, 1987, pp 16/1 1-10.

3. K.Nootbaar (Applied Microcircuits Corp.), "Design, Testing, and Application of a Metastable Hardened Flip-Flop," ibid., pp 16/2 1-9.

4. J.Birkner (MMI), "Understanding Metastability," ibid., pp 16/3 1-3.

5. R.K.Breuninger, K.Frank, "Metastable Characteristics of Texas Instruments Advanced Bipolar Logic Families," application note SDAA004, Texas Instruments, 1985.

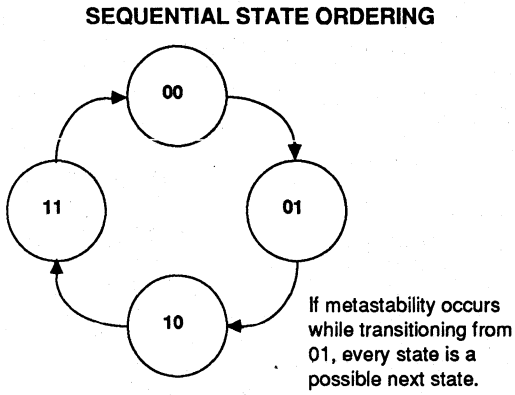


Figure 5.

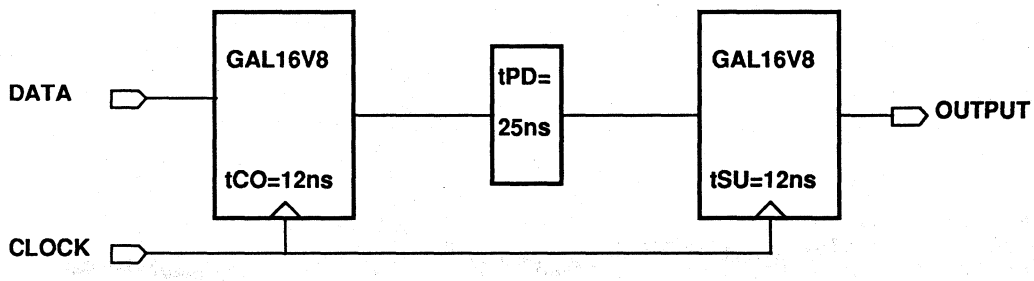


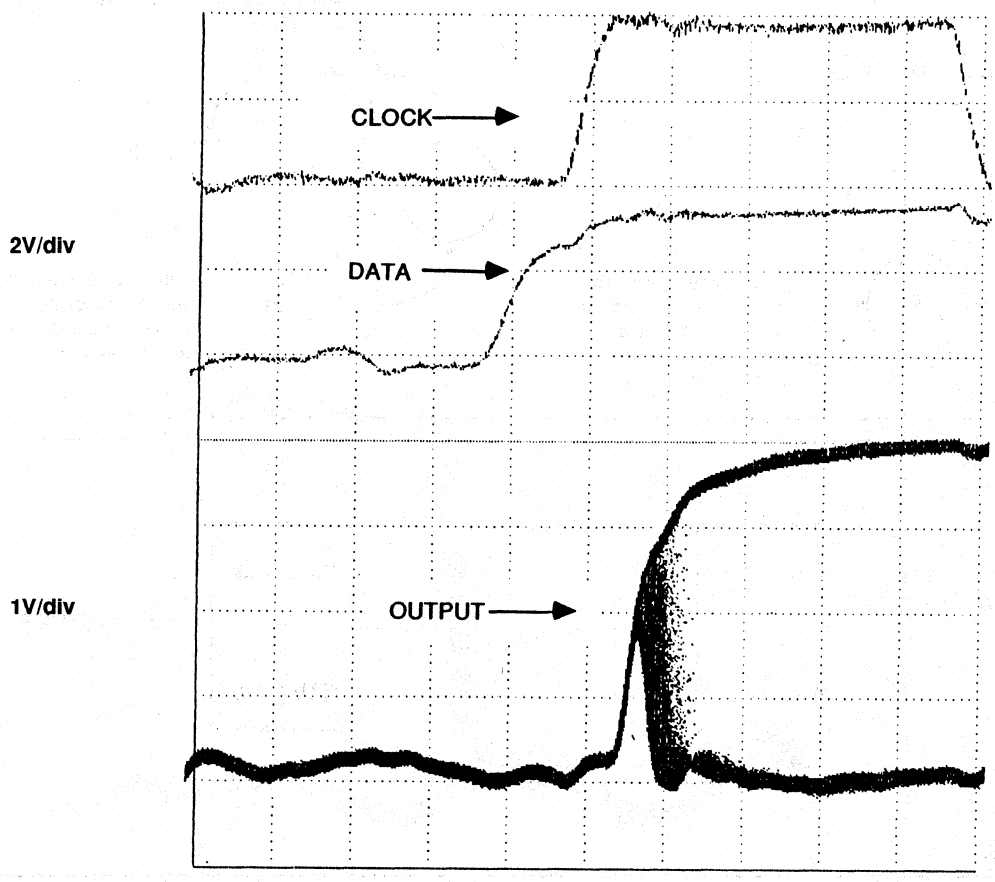
Figure 6.

```
MODULE metastable

TITLE 'Metastable Test
Pattern'

u00 Device 'P16R8';

d       PIN  2;
q1,q2   PIN  12,19;
        EQUATIONS
q1 := d;
q2 := d;
        End metastable
```

Listing 1a. Source equations

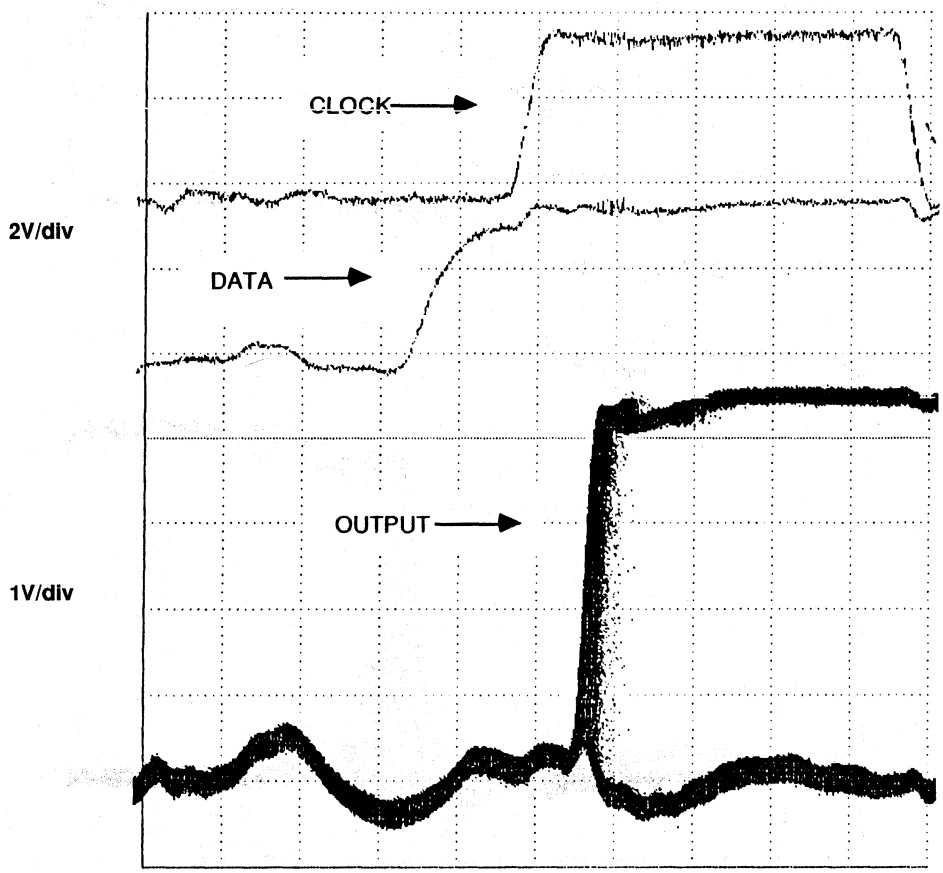
```
JEDEC file for: P16R8
Metastability Test Pattern*
QP20* QF2048* F0*
L0000 10111111111111111111111111111111*
L1792 10111111111111111111111111111111*
C07F4*
```

Listing 1b. JEDEC file



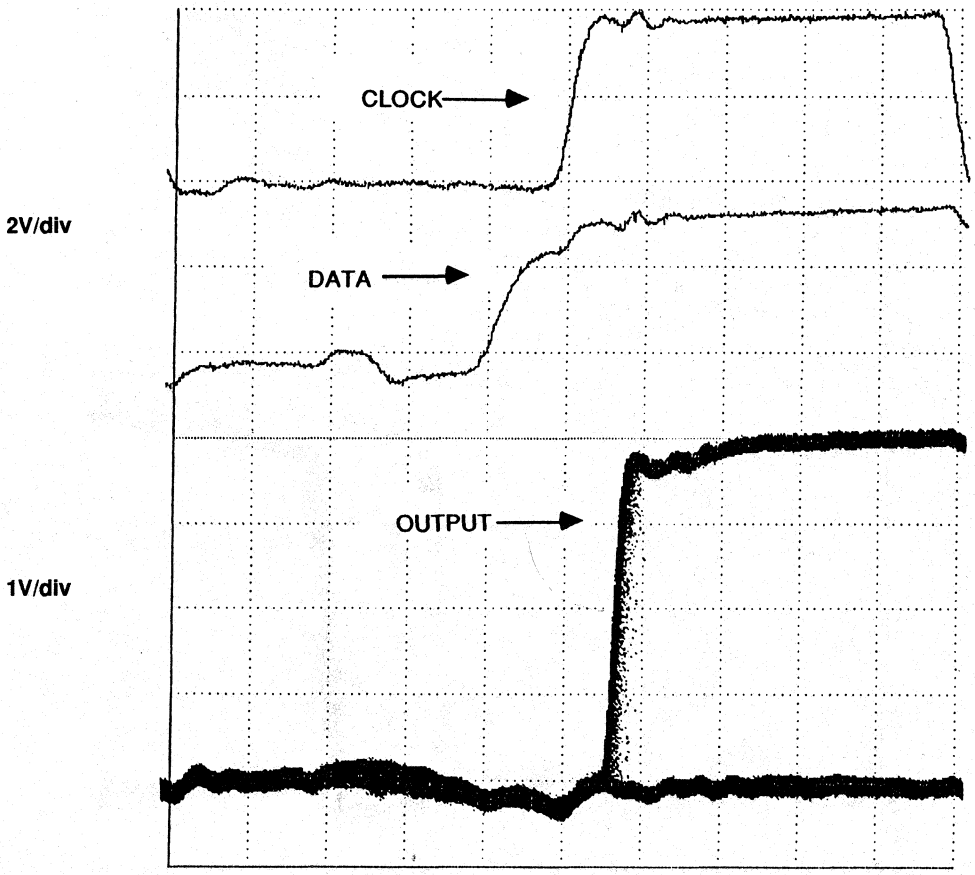
Plot 1. PAL16R8B

Part #	Date Code	∆o (ns)	k2/ns^{-2}
PAL16R8A	8721	11	2.0
PAL16R8B	8722	6	3.0
AmPAL16R8A	8631	8	1.9
TIBPAL16R8-15	8723	5	1.25



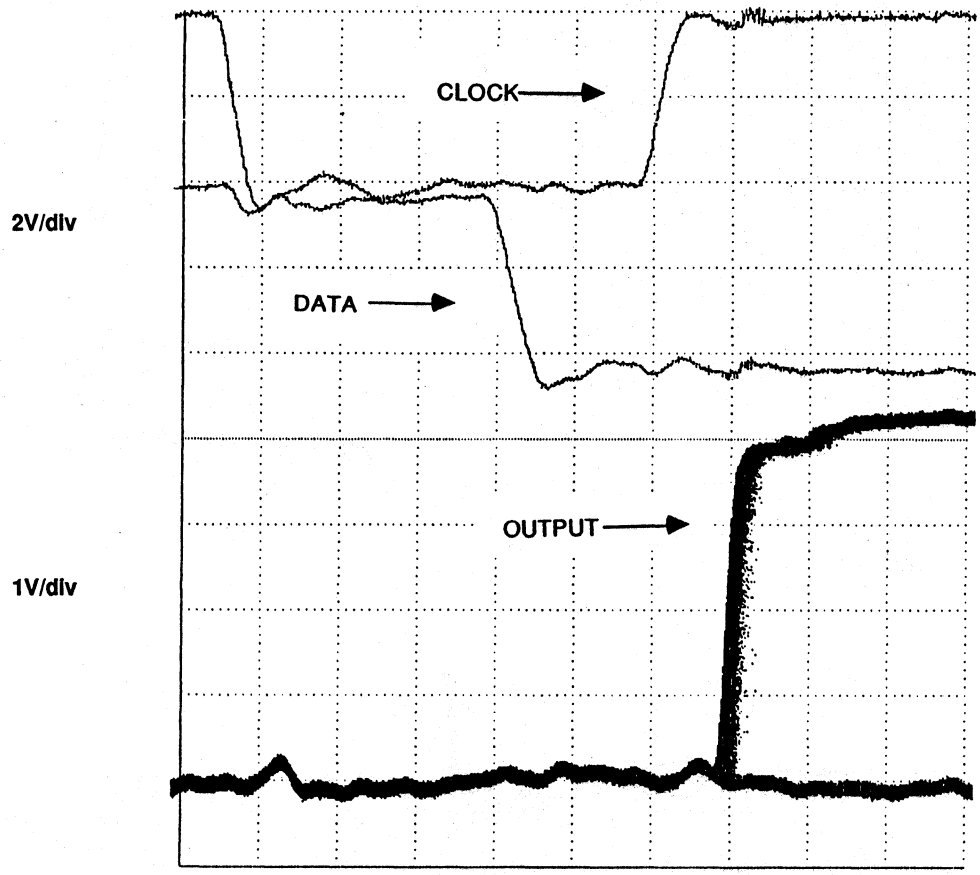
Plot 2. CYPALC16R8-25

Part #	Date Code	Δo (ns)	k2/ns^{-2}
CYPALC16R8-25	8622	3	3.75



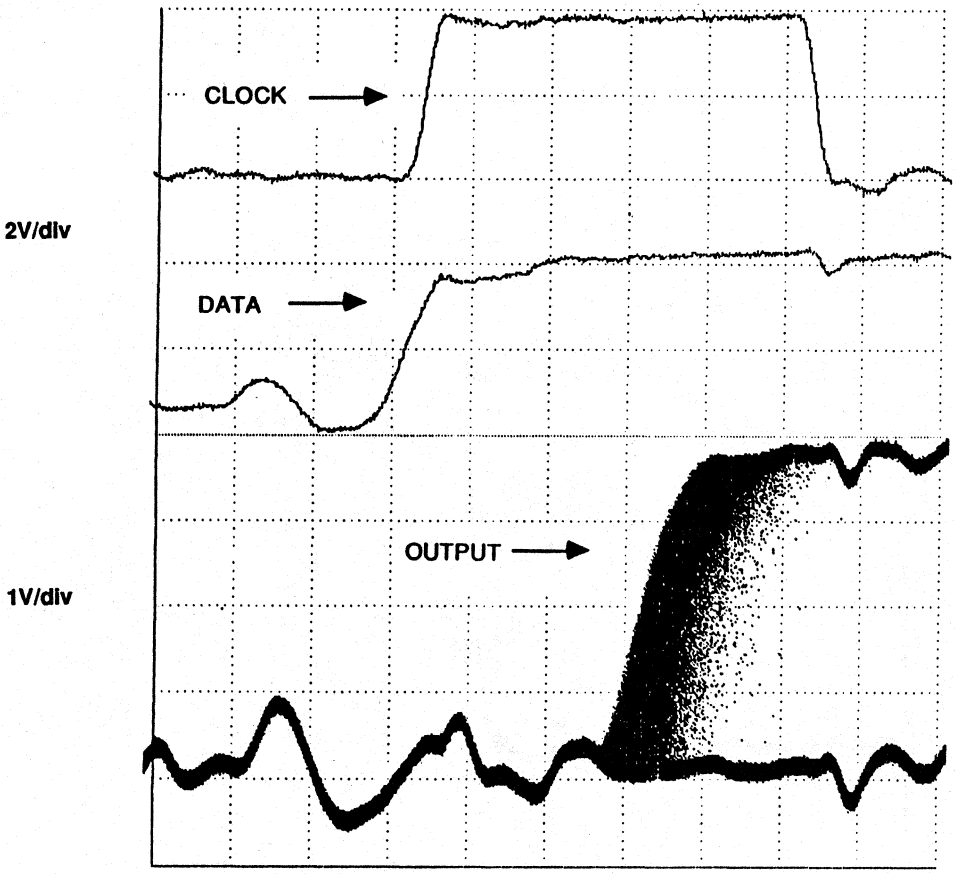
Plot 3. Lattice GAL16V8-15L

Part #	Date Code	△o (ns)	$k2/ns^{-2}$
GAL16V8-15	8731	2	8
GAL16V8-25	8730	2	8



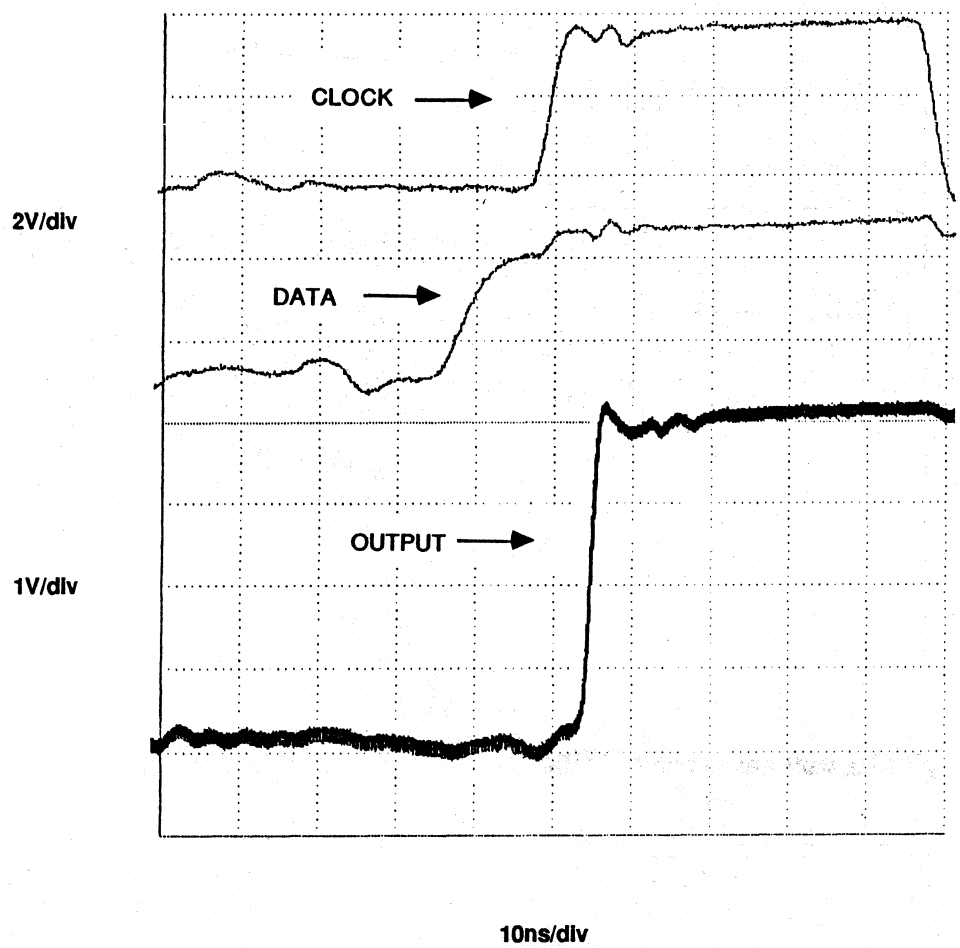
Plot 4. Lattice GAL6001ES

Part #	Date Code	Δo (ns)	k2/ns^{-2}
GAL6001ES	8652	1	6.25

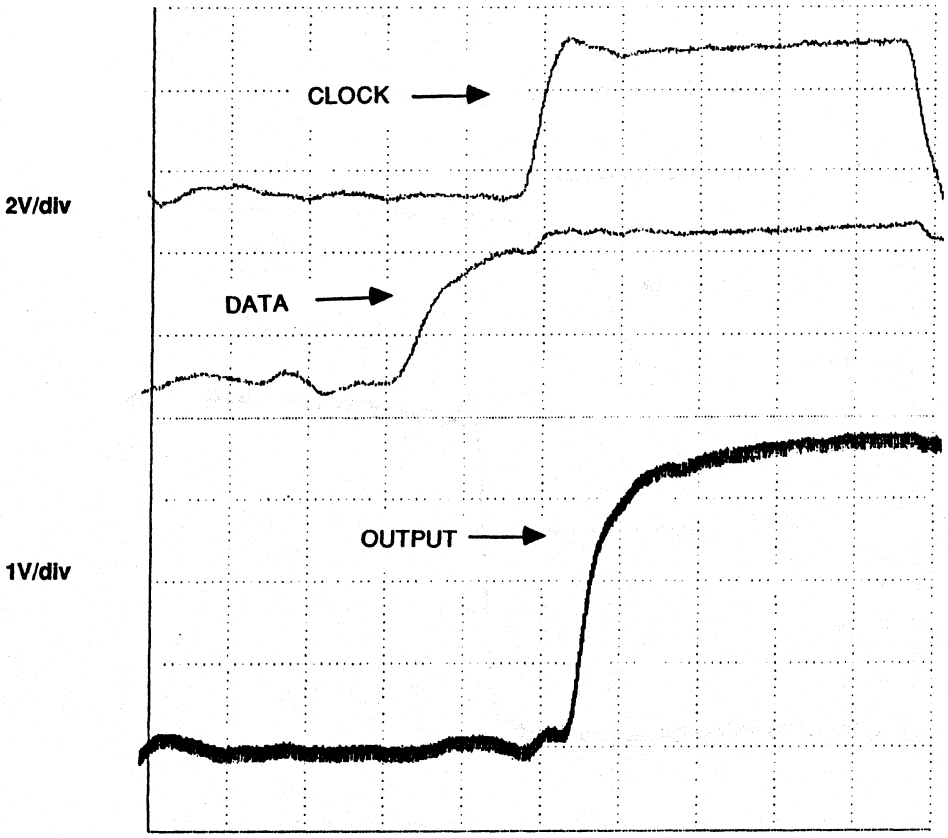


Plot 5. 7474

Part #	Date Code	Δo (ns)	k2/ns^{-2}
SN7474N	7615	6	1.3
9N74/7474	7341	7	1.25



Plot 6. Normal Lattice GAL16V8-15L Transition



Plot 7. Normal PAL16R8B Transition

END

COPYING PAL PATTERNS INTO GAL DEVICES

INTRODUCTION

The generic architecture of the GAL family offers the user many different device configurations. For example, the GAL16V8/16V8A has the ability to emulate 21 of the most popular 20-pin PAL devices. To put it simply, the GAL16V8/16V8A is functionally, parametrically, and fuse map compatible with all common 20-pin PAL devices. Table 1 lists the PAL devices that the GAL16V8/16V8A can replace. Table 2 shows the 21 different 24-pin PAL devices that the GAL20V8/20V8A can fully replace. This technical brief addresses the procedure of copying a PAL pattern - either a PAL master or a PAL JEDEC file - into a GAL device.

The technique of copying a PAL into a GAL device is straightforward, since existing JEDEC files or PAL masters can be used without modification. Other devices that only emulate PAL architectures may require access to source equations and/or design modifications. The Lattice approach has been to allow customers the ability to "cross program" a PAL pattern without having to change the programming procedure, master device, or JEDEC file.

Lattice GAL devices configured as PAL architectures are referred to as RAL devices. There is a one-to-one correspondence between PAL architectures and RAL architectures (see figure 1 and 2).

COPYING A PAL MASTER INTO A GAL DEVICE

If a programmed PAL is available, and is one of the devices listed in Table 1 or Table 2, all that is needed to copy a PAL pattern into a GAL device is a qualified GAL programmer .

1) Place the PAL device into the programmer and read the PAL using the normal procedure.

2) Select the appropriate RAL family/pinout code for the PAL being emulated. Note: the RAL code is required for PAL device copying in order to con figure the architecture properly. Do not use the GAL device code for copying PAL devices.

GAL16V8/16V8A PAL Architecture Emulation
16L8
16H8
16R8
16R6
16R4
16P8
16RP8
16RP6
16RP4
10L8
12L6
14L4
16L2
10H8
12H6
14H4
16H2
10P8
12P6
14P4
16P2

TABLE 1: PAL Architectures Emulated by the GAL16V8/16V8A

GAL20V8/20V8A PAL Architecture Emulation
20L8
20H8
20R8
20R6
20R4
20P8
20RP8
20RP6
20RP4
14L8
16L6
18L4
20L2
14H8
16H6
18H4
20H2
14P8
16P6
18P4

TABLE 2: PAL Architectures Emulated by the GAL20V8/20V8A

3) Place the GAL device into the programmer and program the GAL device using the appropri ate RAL family/pinout code. The copy procedure is complete and the resulting GAL device is 100% compatible with the PAL device it copied.

COPYING A PAL JEDEC FILE INTO A GAL DEVICE

If a JEDEC file for one of the PAL devices listed in Table 1 or Table 2 is available, again all that is needed is a qualified GAL programmer.

1) Select the appropriate RAL family/pinout code for the PAL JEDEC file that is to be downloaded to the programmer. Note: the RAL code is required for the programmer to configure the architecture properly. Do not use the GAL device code when downloading a PAL JEDEC file.

2) Download the PAL JEDEC file from a computer to the programmer using the normal procedure.

3) Place the GAL device into the programmer and program the GAL device without changing the family/ pinout code. The programming procedure is complete and the resulting GAL device is 100% compatible with the PAL device being emulated.

NOTES

•Some programmers use different names for "family/ pinout code." "Select codes," "algorithm" or menu selections are interchangeable.

•Programming PAL patterns into GAL devices is not unlike copying a PAL pattern from PAL vendor A to PAL vendor B. The difference is that you must have a generic GAL device in the socket with a specific RAL architecture code selected.

•JEDEC files compiled with GAL16V8 or GAL20V8 target devices should be programmed with GAL device codes selected.

•The GAL22V10 code emulates PAL22V10 devices directly (no RAL code is required).

•After programming, the GAL device still retains its full erasability feature. The device can be reused with different array patterns and architecture configurations, as selected by the designer.

GAL DEVELOPMENT TOOLS

Introduction
The Tools Engineering Group at Lattice Semiconductor works closely with hardware and software vendors to insure programming support for GAL devices is available in a timely manner.

Lattice works with a variety of programming vendors to satisfy your needs, whether you need a low-cost programmer, an engineering programmer, or a production programmer.

For a current list of Lattice qualified GAL programmers, please contact Lattice's Applications Engineering Department (Tel: 503-681-0118, or FAX: 503-681-3037).

Benefits of Using Lattice Approved Programmers
Lattice provides one of the most extensive review and qualification procedures in the industry. When Lattice approves a programmer, you are insured that it conforms to all programming procedures and specifications. In addition, programmers qualified by Lattice adhere to the latest JEDEC communication standards.

The use of unapproved equipment will void all warranties, including quality, reliability and data retention.

Below are lists of programmer manufacturers and software developers that provide Lattice qualified GAL development tools.

PROGRAMMER MANUFACTURERS

BP-Microsystems
10681 Haddington
Suite 190
Houston, TX 77043
Phone: (713) 461-9430

Data I/O Corp.
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
Phone: (206) 881-6444
FAX: (206) 882-1043

Inlab, Inc.
2150-I W. 6th Ave.
Broomfield, CO 80020
Phone: (303) 460-0103

Japan Macnics Corp.
516 Imaiminami-Cho,
Nakahara-ku
Kawasaki-City, 211 Japan
Phone: 044-711-0022

Kontron
630 Clyde Ave.
Mountain View, CA 94039
Phone: (415) 361-1012
FAX: (415) 965-3505

Logical Devices
1321 N.W. 65th Place.
Fort Lauderdale, FL 33309
Phone: (305) 974-0967
FAX: (305) 974-8531

Microprocss
Parc d'Activite des Pres
5 rue Denis-Papin
59650 Villeneuvue d'Ascq
France

One-D/Advin systems
1050 East Duane Ave.
Suite L
Sunnyvale, CA 94086
Phone: (415) 969-9900

Programmable Logic Tech.
P.O. Box 1567
Longmont, CO 80501
Phone: (303) 772-9059
FAX: (303) 772-5617

Qwerty Inc.
5346 Bragg Street
San Diego, CA 92122
Phone: (619) 455-0500
FAX: (619) 453-4648

SMS Micro Systems
1M Morgenthal
D-8994 Hergatz
Scwarzenberg
W. Germany

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
Phone: (408) 988-1118
FAX: (408) 988-1232

System General
3Fl., No. 6, Lane 4
Tun Hwa N. Rd.
P.O. Box: 53-591
Taipei, Taiwan R.O.C.
Phone: 886-2-7212613
FAX: 886-2-7212615

SOFTWARE DEVELOPERS

Capilano Computing
P.O. Box 86971
North Vancouver, BC
V7L 4P6 Canada
Phone: (604) 669-6343

Data I/O / FutureNet
10515 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073
Phone: (206) 881-6444
FAX: (206) 882-1043

ISDATA GmbH
Hansastraße 29A
D-7500 Karlsruhe 21
West Germany
Phone: 0721-57-9509

Logical Devices
1321 N.W. 65th Place.
Fort Lauderdale, FL 33309
Phone: (305) 974-0967
FAX: (305) 974-8531

Minc Incorporated
1575 York Rd.
Colorado Springs, CO 80918
Phone: (719) 590-1155
FAX: (719) 594-4708

Pistohl Electronics
22560 Alcalde Rd.
Cupertino. CA 95014
Phone: (408) 255-2422

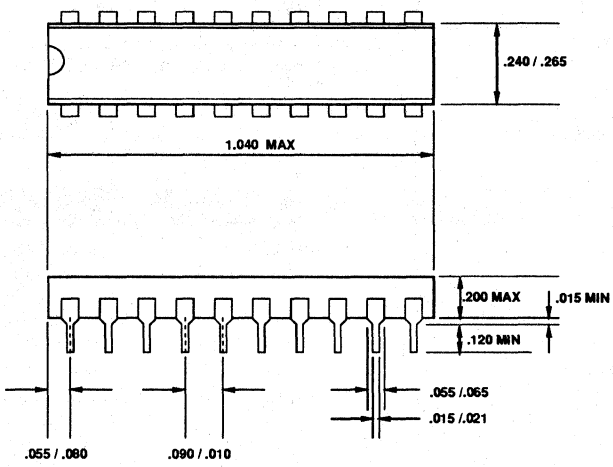
Programmable Logic Tech.
P.O. Box 1567
Longmont, CO 80501
Phone: (303) 772-9059
FAX: (303) 772-5617

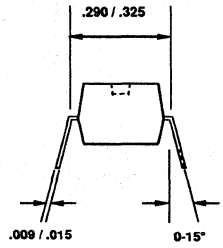
Qwerty Inc.
5346 Bragg Street
San Diego, CA 92122
Phone: (619) 455-0500
FAX: (619) 453-4648

PACKAGE DIAGRAMS

20-Pin Plastic DIP

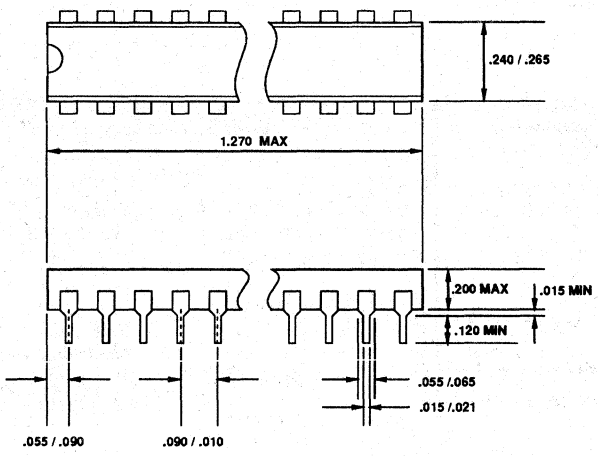
Dimensions in Inches MIN. / MAX.

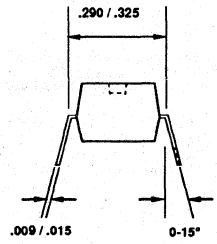




24-Pin Plastic DIP

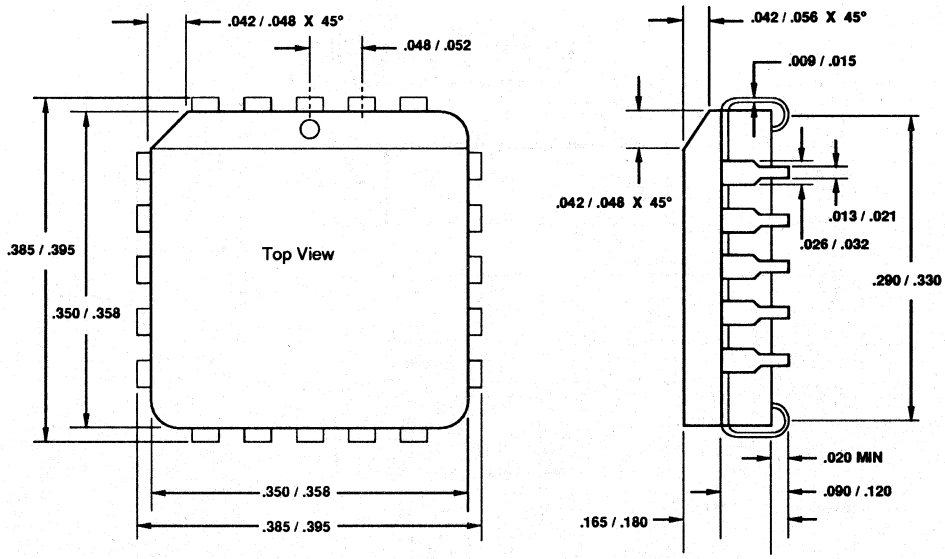
Dimensions in Inches MIN. / MAX.





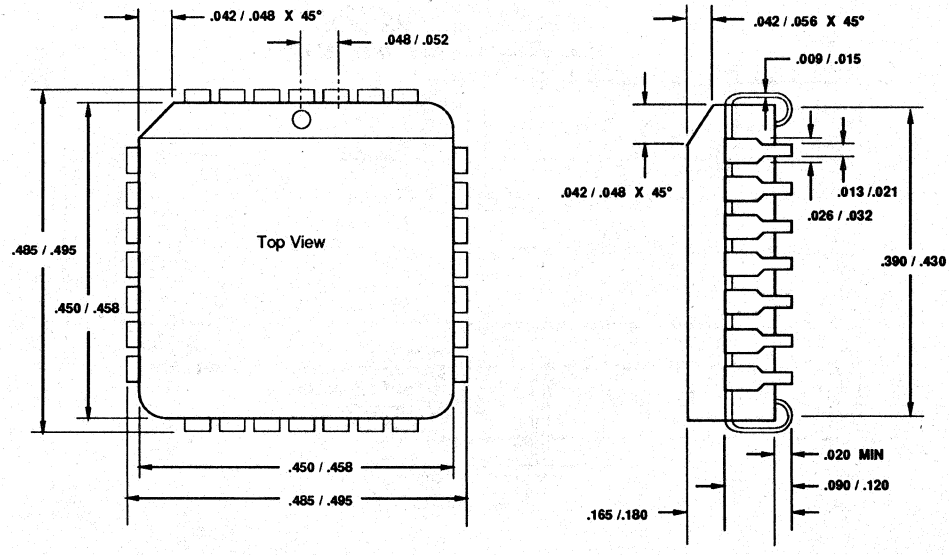
20-Pin PLCC Package

Dimensions in Inches MIN. / MAX.



28-Pin PLCC Package

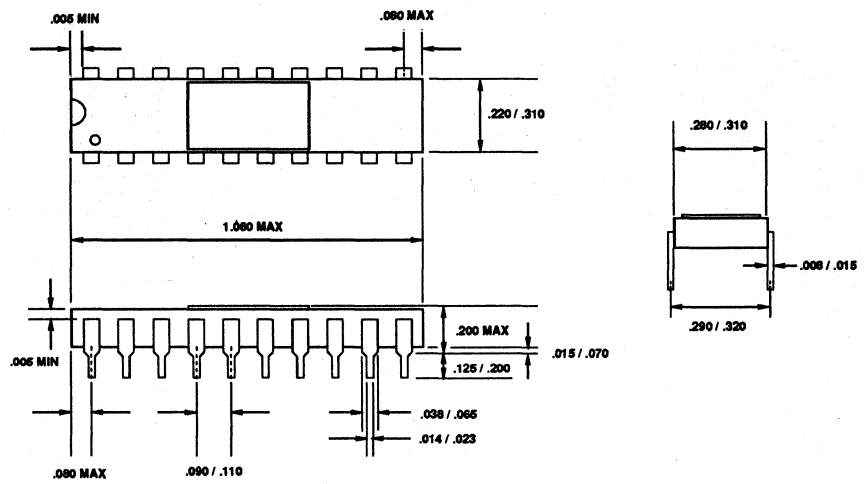
Dimensions in Inches MIN. / MAX.



4

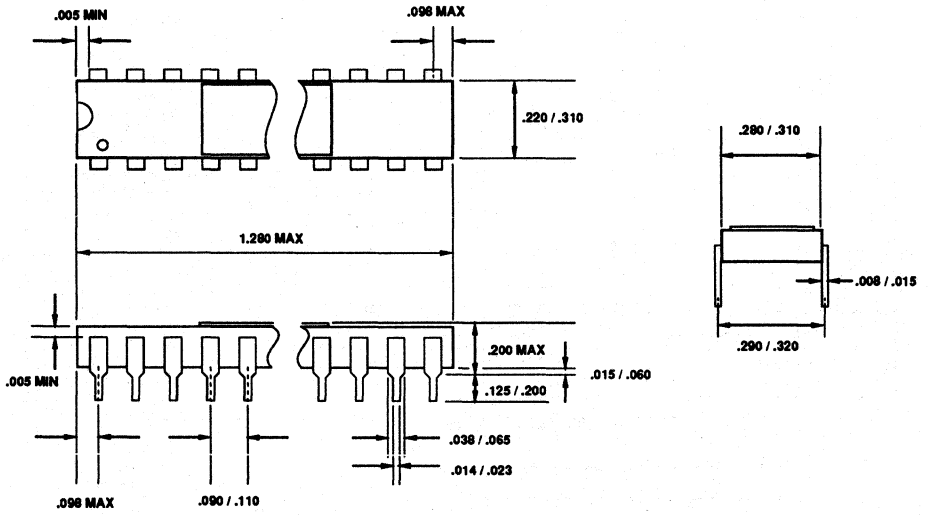
20-Pin (300 MIL) Sidebrazed DIP

Dimensions in Inches MIN. / MAX.



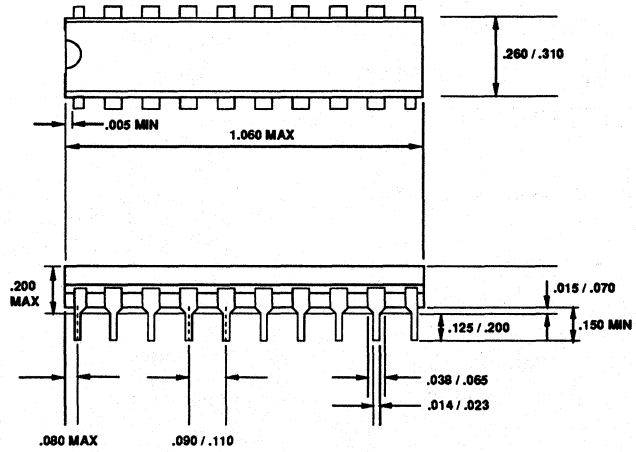
24-Pin (300 MIL) Sidebrazed DIP

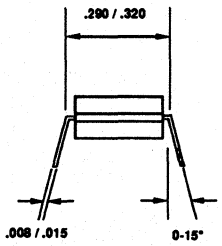
Dimensions in Inches MIN. / MAX.



20-Pin (300 MIL) CERDIP

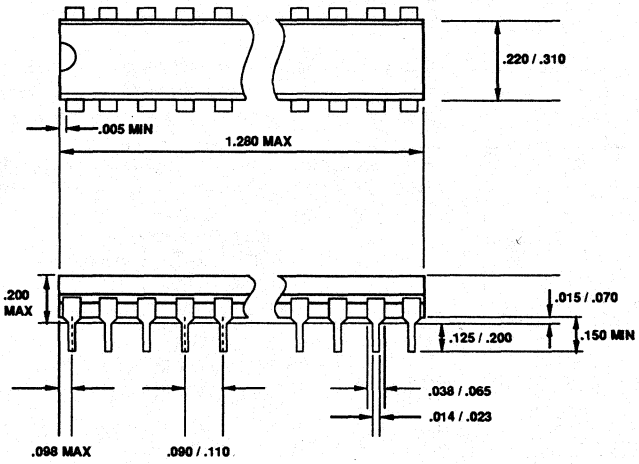
Dimensions in Inches MIN. / MAX.

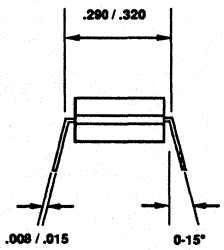




24-Pin (300 MIL) CERDIP

Dimensions in Inches MIN. / MAX.

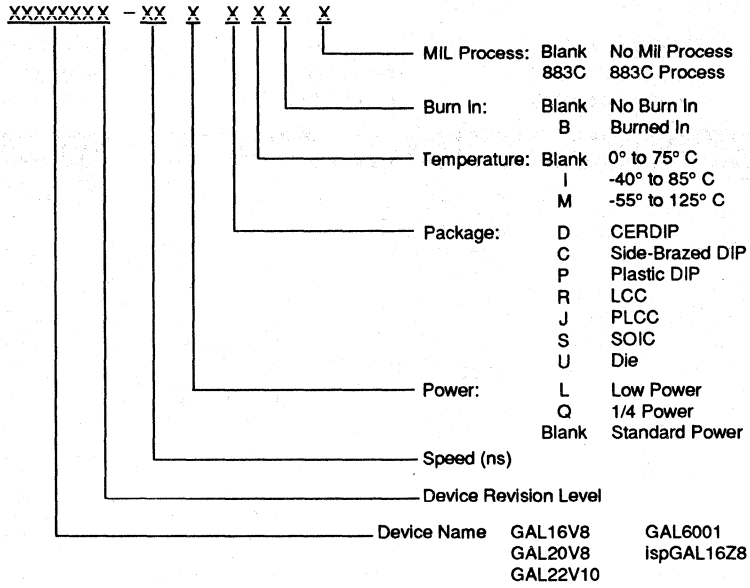




4

ORDERING INFORMATION

PART NUMBER DESCRIPTION



GAL16V8 / 20V8 CROSS REFERENCE

SPEED	POWER	GAL DEVICE	BIPOLAR PAL DEVICE
10ns	115mA	A-10L	--
10ns	180mA	use A-10L	D or -10C
12ns	115mA	A-12L	--
12ns	200mA	use A-12L	-12C
15ns	45mA	A-15Q	--
15ns	115mA	A-15L	--
15ns	180mA	use A-15L	B or -15C
15ns*	130mA	A-15LM	--
15ns*	220mA	use A-15LM	-15M
20ns	55mA	-20Q	--
20ns	115mA	A-20L	--
20ns*	130mA	A-20LM	--
20ns*	210mA	use A-20LM	B MIL
25ns	45mA	-25Q	--
25ns	90mA	A-25L	B-2
25ns	180mA	use A-25L	A
30ns*	55mA	-30QM	--
30ns*	125mA	-30LM	--
35ns	45mA	use -35Q	B-4
35ns	90mA	use A-25L	A-2
35ns	180mA	use A-25L	STD

* Military Temperature Range

FACTORY PATTERNING

The additional service of having GAL devices custom programmed and permanently ink marked with customer specific indentification codes is available from Lattice.

Due to Lattice's stringent test philosophy and 100% AC/DC testing, the quality of pre-patterned GAL devices will be higher than pre-patterned bipolar or UVCMOS devices.

For more information on pre-patterned and custom marked GAL devices please contact:

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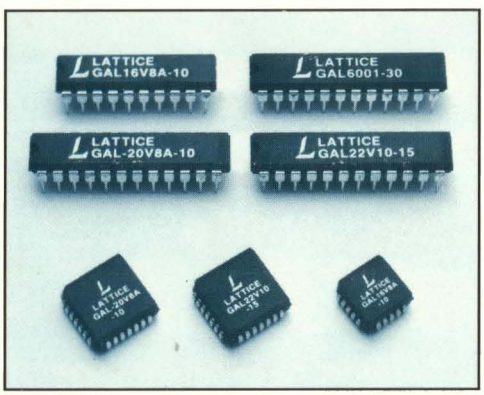

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