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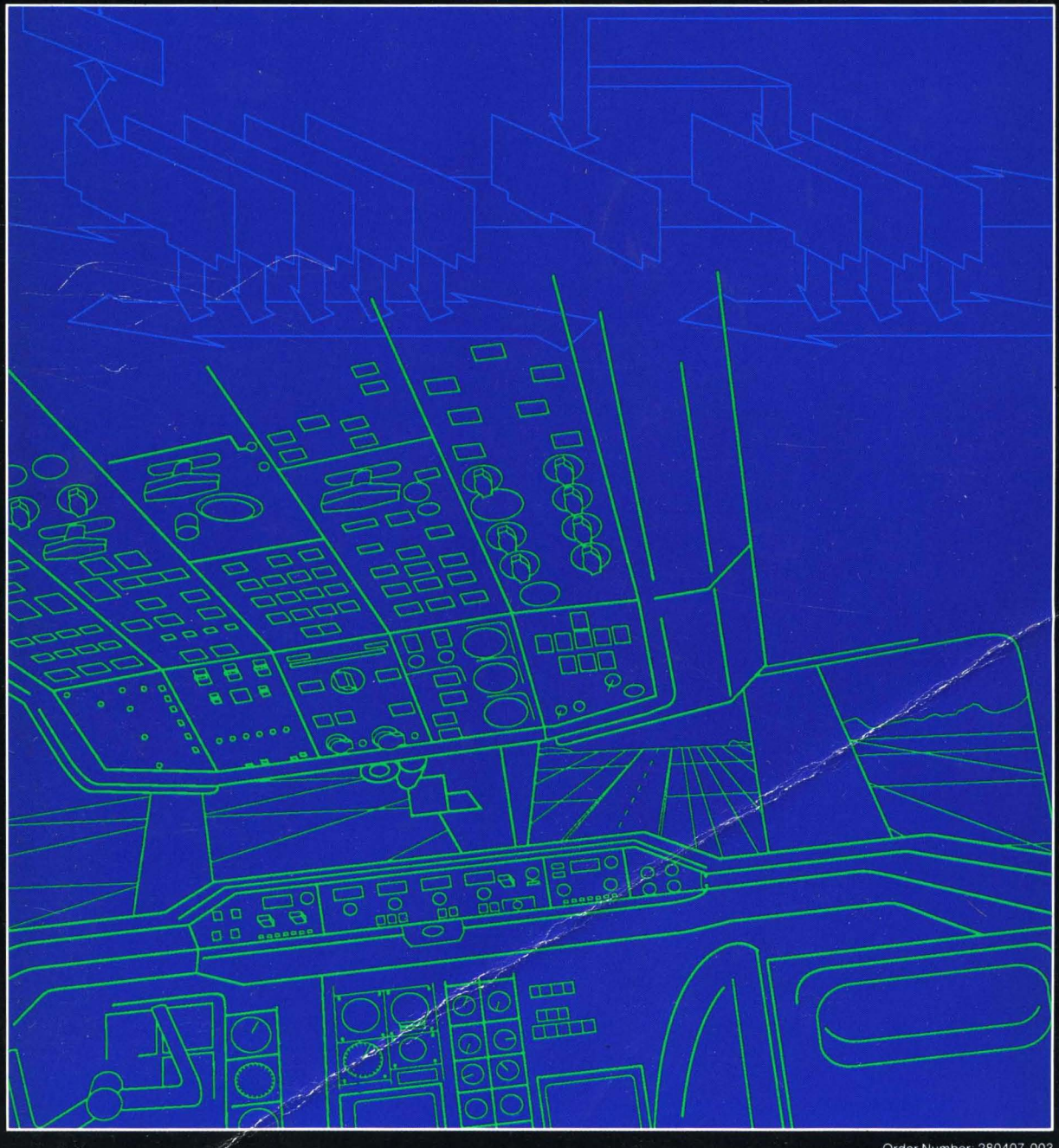
OEM Boards and Systems Handbook



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OEM BOARDS AND SYSTEMS HANDBOOK

1989

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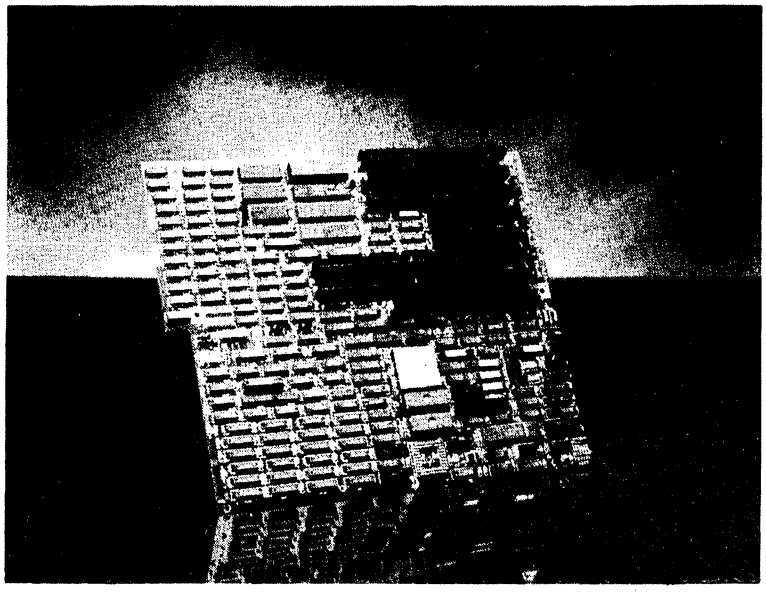
iSBC®386AT PRODUCT PROFILE



POWERFUL 32-BIT PERFORMANCE WITH PC AT FLEXIBILITY

The iSBC386AT is the board level core for an advanced 32-bit computing system. The board is form, fit and function compatible with the PC AT, but with the 80386 as the CPU, provides 2-3 times the performance of the PC AT. Additional features include on-board serial and parallel ports, two 32-bit memory expansion slots, and a socket which supports the 80387 math coprocessor.

A system designed using the iSBC386AT emulates the PC AT but replaces the 16-bit data paths of the AT with 32-bit data handling for both memory and math interfaces. It also provides access to the full capabilities of 80386 protected mode architecture. With the ability to address up to 16 MB of memory, it is an excellent platform for UNIX* applications. The complete iSBC386AT board set includes the system baseboard, and 32-bit memory expansion boards available in densities of 2 and 8 MB. It provides the capability to bring a high quality 32-bit DOS compatible system to market quickly with a minimum of technical risk.

FEATURES

iSBC386AT—BASEBOARD

- Intel 80386 CPU running at 16 MHz
- Socket for 16 MHz 80387 numeric coprocessor
- Phoenix Technologies ROM BIOS
- 512 KB of 32-bit RAM on the baseboard and two connectors for high speed 32-bit RAM expansion
- Expansion bus interface: two PC-compatible 8-bit bus slots and four PC AT compatible 16-bit bus slots
- Keyboard interface and Clock/calendar with battery-backed CMOS memory
- Sixteen interrupts and Seven DMA (direct memory access) channels
- One IBM-compatible serial RS-232 communication port and one Centronics-compatible parallel printer port

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August, 1988
Order Number: 280736-003

FEATURES

iSBC386MEM020 AND iSBC386MEM080—MEMORY BOARDS

- Available in densities of 2 MB (020) and 8 MB (080)
- Plugs into baseboard connectors for high speed 32-bit RAM expansion

INTEL QUALITY—YOUR GUARANTEE

Intel brings the same high standards to the design and manufacture of the SBC386AT family that it is known for in component, board, and system products.

Intel quality is designed in and then verified by rigorous testing in our state-of-the-art Environmental Test Laboratory.

SERVICE & SUPPORT

90 day return to factory warranty.

Enhanced warranty and service contracts for fast part repair are available on a worldwide basis.

Factory services include part exchange and spare parts.

SPECIFICATIONS

ENVIRONMENT

Ambient Temperature	
Operating	0 to +55°C
Non-operating	−40 to +70°C
Relative Humidity	
Operating	0 to 85% noncondensing at 55°C
Altitude	
Operating	0-10,000 feet
Shock	30 G for 11 msec, ½ sine wave
Vibration	Random variation 0-1,000 Hz

PHYSICAL CHARACTERISTICS

Length	12.0 in. (304.8 mm)
Width	13.8 in. (350.5 mm)
Approximate Weight	18 oz. (510 gm)

POWER REQUIREMENTS

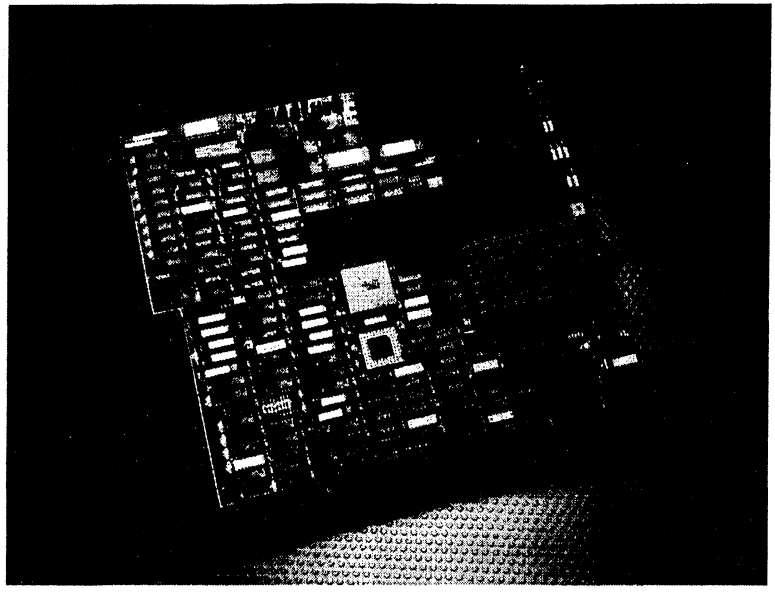
Voltage and Tolerance	Nominal Current	Watts
+5 V ± 5%	5.2 A	26.00
+12V ± 10%	0.06 A	0.72
−12 V ± 10%	0.08 A	0.96
TOTAL		27.68

Note: Does NOT include power for expansion boards.

REFERENCE MANUAL

iSBC386AT User's Guide Order #149568-002

iSBC® 386ATZ BASEBOARD



HIGH PERFORMANCE 16 MHz 386™ BASEBOARD

The iSBC 386ATZ is an advanced 16 MHz 80386, PC AT compatible, baseboard. Two megabytes of on-board memory running at zero wait states, and the ability to download Phoenix BIOS into RAM, allow for excellent performance. Highly flexible, the board offers 32-bit memory expandable to 16 MB, and eight I/O expansion slots.

The unique design of the iSBC 386ATZ captures the full 32-bit capabilities of the powerful 80386 CPU, without sacrificing compatibility with the industry standard 8 MHz PC AT bus. Exhaustive testing of numerous add-in boards and applications assures this compatibility. The iSBC 386 ATZ delivers the OEM unsurpassed quality, flexibility, and performance in an off-the-shelf PC AT compatible product.

iSBC® 386ATZ BASEBOARD STANDARD FEATURES:

- Intel 80386 running at 16 MHz
- 2 MB of zero wait state on-board SIMM memory
- Socket for a 16 MHz 80387 math coprocessor
- Phoenix Technologies ROM BIOS
- 8 flexible I/O expansion slots:
  - –Two 32-bit slots or 8-bit PC slots
  - –Four 16-bit standard PC AT slots or 8-bit PC slots
  - –Two dedicated 8-bit PC slots
- One serial and one parallel port

OPTIONS:

- 2 MB (iSBC 386 MEM020) 32-bit, one wait state, add-in memory board
- 8 MB (iSBC 386 MEM080) 32-bit, one wait state, add-in memory board
- Ability to download Phoenix BIOS into RAM

August, 1988
Order Number: 280835-002

SPECIFICATIONS

BASEBOARD

Central Processor	Intel 80386, 16 MHz
Floating-Point Processor	Intel 80387, 16 MHz
Main Memory	
RAM	2 MB on-board
Maximum RAM	16 MB
Cycle Time	125 ns
Data Bus Width	32-Bits
Error Detection	Bit Parity
I/O	One serial port (asynch. RS232C, 9-pin connector, AT compatible) One parallel port (Centronics compatible, 25-pin connector, AT compatible) 8 expansion slots 2 32-bit or 8-bit slots 2 8-bit slots 4 16-bit or 8-bit slots

PHYSICAL CHARACTERISTICS

Length	12.0 in. (304.8 mm)
Width	13.8 in. (350.5 mm)
Approximate Weight	36.8 oz. (1043 gm)

POWER REQUIREMENTS

Voltage and Tolerance	Nominal Current	Watts
+5 V ± 5%	7.3 A	36.50
+12V ± 10%	0.06 A	0.72
−12V ± 10%	0.08 A	0.96
TOTAL		38.18

Note: Does NOT include power for expansion boards.

ENVIRONMENT

Ambient Temperature	
Operating	0 to +55°C
Non-operating	−40 to +70°C
Relative Humidity	
Operating	0 to 85% noncondensing at 55°C
Altitude	
Operating	0-10,000 feet
Shock	50 G for 11 msec, ½ sine wave
Vibration	Random variation 0-1,000 Hz

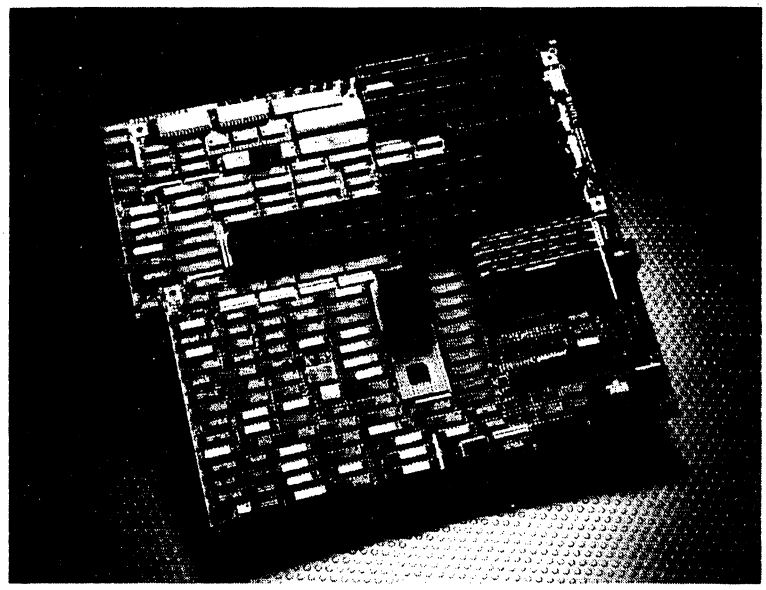
SERVICE & SUPPORT

90 day return to factory warranty.

Enhanced warranty and service contracts for fast part repair are available on a worldwide basis.

Factory services include part exchange and spare parts.

iSBC® 386AT-25 BASEBOARD



INTEL 25 MHz 80386 PERFORMANCE—PC AT COMPATIBLE

The iSBC 386AT-25, based on Intel's 25 MHz 80386, offers OEMs the board level core to develop a superior 32-bit computing system. Highly flexible and extremely powerful, the board offers eight I/O expansion slots and up to 24 MB of zero wait state memory in several configurations. Additional features include a 25 MHz 80387 math coprocessor socket, two serial ports, one parallel port, and a real-time clock.

A system design using the iSBC 386AT-25 takes advantage of the full power of the 80386 at 25 MHz, yet remains completely compatible with the industry standard 8 MHz PC AT bus. The iSBC 386AT-25 allows an OEM the opportunity to bring a high quality, superior performance system to market quickly with a minimum of risk.

iSBC® 386AT-25 BASEBOARD FEATURES

- Intel 80386 running at 25 MHz
- Zero wait state performance provided by a 64K byte cache
- 1, 2, 4, or 8 megabytes on-board SIMM main memory
- Phoenix Technologies ROM BIOS (optional download into RAM)
- 8 flexible I/O expansion slots:
  - –Two 32-bit high performance or 16-bit PC AT or 8-bit PC slots
  - –One dedicated 8-bit PC slot
  - –Five 16-bit PC AT or 8-bit PC slots
- Optional 32-bit 8 MB (iSBC ATMEM8) and 4 MB (iSBC ATMEM4) add-in cards allow memory expansion to 24 MB
- Two IBM-compatible serial RS 232 communication ports
- One Centronics-compatible parallel printer port
- Real-time clock with battery-backed CMOS memory
- IBM AT compatible keyboard interface

June, 1988
Order Number: 280840-001

SPECIFICATIONS

BASE BOARD

Central Processor	Intel 80386, 25 MHz
Floating-Point Processor	Intel 80387, 25 MHz
Main Memory	
On-board RAM	1 MB, 2 MB, 4 MB, or 8 MB
Maximum RAM	24 MB
Cycle Time	80 ns
Data Bus Width	32-Bits
Error Detection	Bit Parity
Cache	64K bytes, direct map with write through
I/O	2 serial ports (asynch, RS232C, 9-pin connector, AT compatible) 1 parallel port (Centronics compatible, 25-pin connector, AT compatible) 8 expansion slots 2 32-bit, 16-bit, or 8-bit slots 1 8-bit slot 5 16-bit or 8-bit slots

REGULATIONS

Compliant with the following specifications:

Safety	
U.S.	UL 478 5th Edition
Canada	CSA C22.2 No. 220
Europe/Asia	IEC 950, VDE 0806/IEC 380
EMI/RFI	
U.S. and Canada	FCC CFR 47 Part 15 Subpart J, Class B
Europe	VDE 0871 Level B

COMPATIBILITY

An extensive list of applications and add-in cards has been verified as compatible.

PHYSICAL CHARACTERISTICS

Length	12.0 in. (304.8 mm)
Width	13.8 in. (350.5 mm)
Approximate Weight	43 oz. (1219 gm)

POWER REQUIREMENTS

Voltage and Tolerance	Nominal Current	Watts
+5 V ± 5%	12.0 A	60.00
+12V ± 10%	0.06 A	0.72
−12V ± 10%	0.08 A	0.96
TOTAL		61.68

Note: Does NOT include power for expansion boards.

ENVIRONMENT

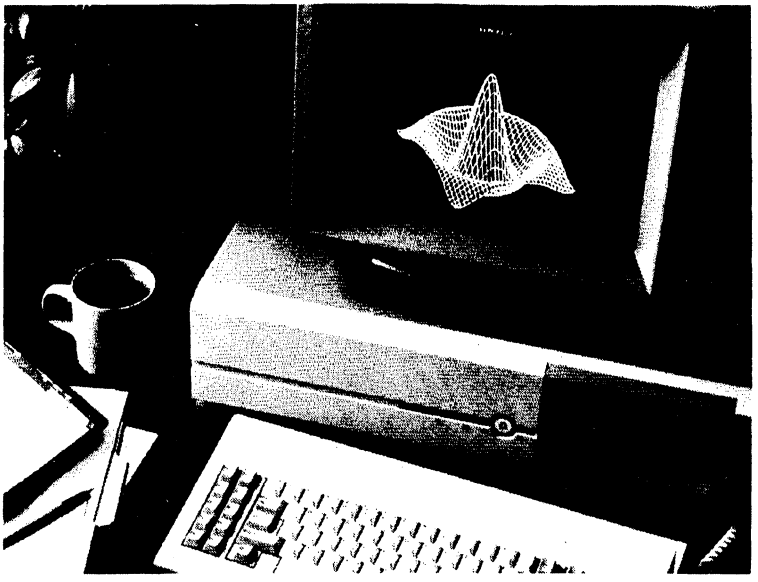
Ambient Temperature	
Operating	0 to +55°C
Non-operating	−40 to +70°C
Relative Humidity	
Operating	0 to 85% noncondensing at 55°C
Altitude	
Operating	0-10,000 feet
Shock	50 G for 11 msec, ½ sine wave
Vibration	Random variation 0-1,000 Hz

SERVICE & SUPPORT

90 day return to factory warranty.

Enhanced warranty and service contracts for fast part repair are available on a worldwide basis.

Factory services include part exchange and spare parts.



32-BIT SYSTEM PERFORMANCE WITH PC AT CAPABILITY

The MicroSystem/AT 301Z offers the power of the Intel 80386 microprocessor with the flexibility of the PC AT based architecture. This combination produces an OEM system well suited to high performance applications such as computer aided design (CAD), computer aided engineering (CAE), and advanced financial analysis which require greater processing and memory capability as well as PC compatibility. With eight PC card slots, the system can be customized easily by OEMs using off-the-shelf boards, operating systems and application software.

STANDARD FEATURES:

- Intel 80386 processor running at 16 MHz, 0 wait state
- 2 MB main memory
- Phoenix Technologies ROM BIOS
- 8 I/O expansion slots
  - 2 8-Bit PC XT
  - 2 8-Bit PC XT or 32-Bit memory expansion
  - 4 16-Bit PC AT
- 220 watt power supply and chassis
- Serial port
- Centronics parallel port
- Expansion capability for up to five half-height, 5.25" peripheral devices.

OPTIONS:

- Intel 80387 Floating-Point coprocessor
- 2 MB and 8 MB 32-Bit memory expansion boards (2 slots maximum)
- Zero memory option
- 40 MB Winchester disk drive
- 1.2 MB floppy disk drive
- Disk Controller with floppy or Winchester

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August, 1988
Order Number: 280827-003

SPECIFICATIONS

BASE SYSTEM

Central Processor	Intel 80386, 16 MHz
Floating-Point Processor	Intel 80387, 16 MHz
Main Memory	
RAM	2M Bytes on CPU board
Expansion RAM	2M Bytes board, 8M Bytes board
Maximum RAM	16M Bytes
Cycle Time	125 ns
Data Bus Width	32-Bits
Error Detection	Byte Parity
I/O	1 serial port (asynchronous, RS232C, 9-pin connector) 1 parallel port (centronics compatible, 25 pin connector) 8 expansion slots
Floppy Disk Option	5.25" footprint High Density Floppy Disk Drive Unformatted Capacity 1.6 MB
Step Rate	6 milliseconds
Head Settling Time	15 milliseconds
Winchester Disk	5.25" footprint
Unformatted Capacity	40.8 MB formatted
Average Access Time	28ms typ

REGULATIONS

Meets or exceeds the following requirements:

Safety	
US	UL 478 5th Edition
Canada	CSA C22.2 No. 154
Europe	IEC 435 and VDE 0806
EMI/RFI	
US and Canada	FCC47 CFR Part 15 Subpart J Class A
Europe	VDE 0871 Level A

ENVIRONMENT

Ambient Temperature	
System On:	15.6 to 32.2°C (60 to 90°F)
System Off:	– 34 to 60°C
Relative Humidity	
System On:	5 to 85%, noncondensing
System Off:	5 to 95%, noncondensing
Altitude	
Operating:	2133.6 meters (7000 ft.) maximum
Static Discharge:	7.5 Kv maximum

ELECTRICAL

AC Voltage/Frequency	Switching power supply, 115 V/60Hz or 230V/50 Hz; convenience outlet
DC Power	220 Watts
+ 5v	23.0 A maximum continuous
+ 12v	8.0 A maximum continuous; 11.0 A maximum total for 15 seconds
– 12v	0.5 A maximum continuous
– 5v	0.5 A maximum continuous

DIMENSIONS

Length	17.3 inches (441 millimeters)
Width	21.3 inches (541 millimeters)
Height	6.5 inches (163 millimeters)

WEIGHT

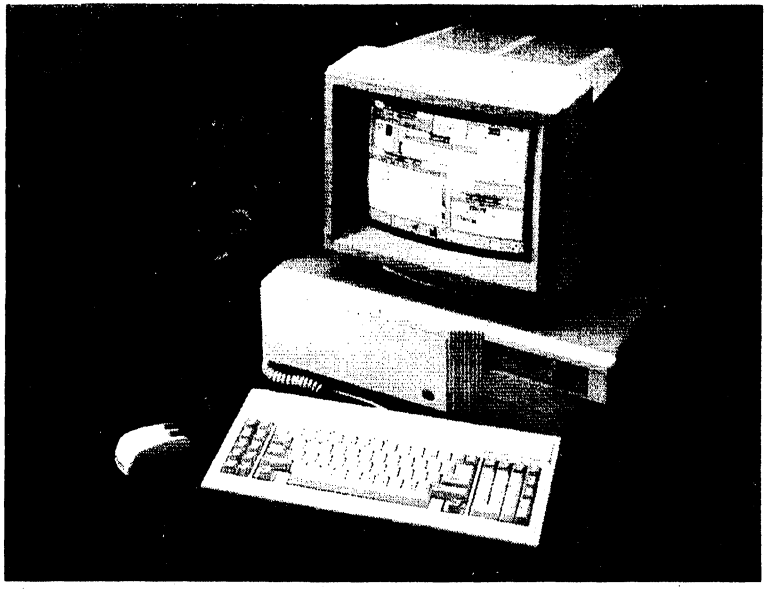
Base system:	44 pounds (20 kilograms)

SERVICE & SUPPORT

90 day return to factory warranty.

Extended warranty and post warranty on-site service contracts are available on a worldwide basis. The above options can include third party devices attached to the system.

Factory services include part exchange and spare parts.



INTEL 25 MHZ 80386 PERFORMANCE IN A PC AT COMPATIBLE

Running at 25 MHz, the Intel 80386 based MicroSystem/AT 302 offers OEM's state-of-the-art performance in a PC AT compatible design. A 64K Byte cache provides effective 0 wait state execution, without the high cost of fast access main memory. Memory capacity is extensive, beginning with 4M Bytes on-board, expandable to 24M Bytes via two 32-bit expansion slots. Additionally, the 302 is designed to pass FCC B and VDE B levels of EMI/RFI regulations, a significant test at 25 MHz.

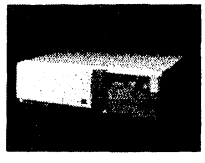
Based upon the PC AT architecture, the MicroSystem/AT 302 is compatible with such software products as MS-DOS, OS/2, and UNIX*. Furthermore, PC AT hardware products from a multitude of vendors plug into 8 I/O expansion slots. If your application runs on a PC today, it will run on the 302.

STANDARD FEATURES:

- Intel 80386 running at 25 MHz
- 64K Byte cache (0 w.s. performance)
- 4M Byte Main Memory (Customer expandable to 8M Byte)
- Phoenix Technologies ROM BIOS
- High Reliability Chassis
- 8 I/O expansion slots
- 220 watt power supply
- 2 32-Bit I/O Expansion Slots
- 2 Serial Ports
- 1 Centronics Parallel Port
- 5 Half-Height, 5¼" Peripheral Bays
- FCC Class B/VDE Level B
- UL/CSA/TUV

OPTIONS:

- Intel 80387 Running at 25 MHz
- 2M Byte Main Memory Option
- Zero Main Memory Option
- 1.2M Byte Floppy Drive
- 8-16M Byte Extended Memory
- 40M Byte Winchester Drive



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*Unix is a trademark of AT&T

August, 1988
Order Number: 280826-003

SPECIFICATIONS

BASE SYSTEM

Central Processor	Intel 80386, 25 MHz
Floating-Point Processor	Intel 80387, 25 MHz
Main Memory	
RAM	2 MB or 4 MB on-board
Extended Memory	8 to 16 MB
Maximum RAM	24 MB
Cycle Time	80 ns
Data Bus Width	32-Bits
Error Detection	Bit Parity
Cache	64K Bytes, Direct map with write through
I/O	2 serial ports (asynch, RS232C, 9-pin connector) AT Compatible) 1 parallel port (Centronics compatible, 25-pin connector, AT Compatible) 8 expansion slots (7 16-bit 2 32-bit)
Floppy Disk Option	5.25" footprint 1.2 MB high density
Step Rate	3 milliseconds
Head Settling Time	15 ms max
Winchester Disk Option	5.25" half height 40.8 MB formatted
Access Time	28 ms typ

REGULATIONS

Meets or exceeds the following requirements:

Safety	
US	UL 478 5th Edition
Canada	CSA C22.2 No. 154
Europe	IEC 435 & VDE 0806
EMI/RFI	
US and Canada	FCC 47 CFR Part 15 Subpart J, Class B
Europe	VDE 0871 Level B

ENVIRONMENT

Ambient Temperature	
System On:	15.6 to 32.2°C (60 to 90°F)
System Off:	– 34 to 60°C
Relative Humidity	
System On:	5% to 85% noncondensing
System Off:	5% to 95% noncondensing
Altitude	
Operating:	2133.6 meters (7000 ft) max
Static Discharge:	7.5 Kv max

ELECTRICAL

AC Voltage/Frequency	Switching power supply, 115 V/60Hz or 230 V/50 Hz
DC Power	220 W
+ 5v	23.0 A maximum continuous
+ 12v	8.0 A maximum continuous; 12.0 A maximum surge 15 seconds
– 12v	0.5 A maximum continuous
– 5v	0.5 A maximum continuous

DIMENSIONS

Length	18.7 inches (47.5 cm)
Width	21.3 inches (54.1 cm)
Height	6.4 inches (16.3 cm)

WEIGHT

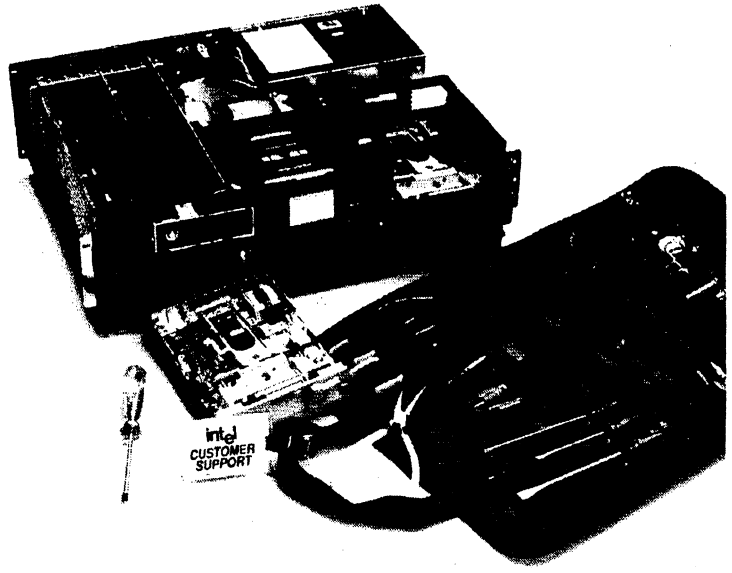
Base system: 35 pounds (15.9 kg)

SERVICE AND SUPPORT

90 day return to factory warranty.

Extended warranty and post warranty on-site service contracts are available on a worldwide basis. The above options can include third party devices attached to the system.

Factory services include part exchange and spare parts.



INTEL MAINTENANCE SUPPORT OPTIONS

Intel has packaged enhanced warranty and service offerings to complement OEM field service. Intel can provide on-site support, carry-in or factory repair options on a worldwide basis. Enhanced warranty options minimize the investment in spares and repair capabilities by providing direct priority access to Intel's field service personnel, logistics and repair centers around the world. Intel's Worldwide Service organization has 100 service locations, four repair centers and 850 people and has been providing microcomputer field service since 1973. Dispatch centers are located in the US (toll free), Europe and Japan.

Standard Offerings:

- On-site maintenance
- Installation
- Per call repair
- Carry-in repair
- Spare parts
- Third party maintenance
- Network design
- Priority part delivery
- Service training
- Factory repair

Enhanced on-site warranty

Low cost, on-site support can be provided through Intel's enhanced warranty program. Two options are available for on-site pass through maintenance. The first option provides on-site, maintenance for one full year. The second option provides the first 90 days on-site with the remainder of the year covered by mail-in repair. Warranty options may be tailored to include hardware support for third party devices installed by OEM's or end users. On-site post warranty options are available that cover Intel and third party devices.

intel

May, 1988
Order Number: 280832-001

		On-site coverage[1]					
		Labor	Parts	Response	Coverage	Contract Period Monthly	Contract Period Annual
Enhanced Warranty	System 30X Plan A Plan B	1 year 90 days	1 year 1 year	Next Day Next Day	7:00 am-6:00 pm Mon.-Fri.		✓ YES ✓ YES
	Third party devices	✓ YES[2]	✓ YES[2]	✓ YES[2]			✓ YES
Post Warranty	System 30X	✓ YES	✓ YES	Next Day	7:00 am-6:00 pm Mon.-Fri.	✓ YES	✓ YES
	Installation	✓ YES[2]					
	[1] 50 miles radius of service location. Zone mark ups apply. [2] Negotiated						

FACTORY SERVICES

Intel has designed factory services to provide the OEM's field service organization full access to Intel's part delivery and repair services. Standard Offerings are:

- Enhanced warranties
- Spare parts
- Custom consulting
- Part repair
- Service training
- Service diagnostics

Enhanced OEM Warranties

Two enhanced OEM warranty options provide low cost, rapid part delivery and quick turn around time on part repairs. The first option provides next day part delivery for the Intel field replaceable units. The second option will ship a replacement part 48 hours after receipt of the defective part. Both warranty plans cover part replacement for one year.

Spares and Service Training

Spare parts for field replaceable units are available for current Intel products and some obsolete parts.

Service training for field service personnel is available in a classroom setting or self paced video tape modules. Training modules may be customized to include unique third party devices.

Custom Services

Intel's experienced field consulting staff can provide specific expertise to your engineering staff in areas of UNIX* driver development, customized diagnostics and system design support.

	Factory Services Repair/Replacement[3]			
	Response	Next Day	48 hour	4 week
Enhanced Warranty	System 30X Plan A	✓ YES		
	Plan B		✓ YES	
	30X modules	✓ YES	✓ YES	
	Per Incident			✓ YES
	[3] Module level repair			

Real-Time Systems and Software

2

LOW-COST REAL-TIME 80386 SYSTEM FROM INTEL

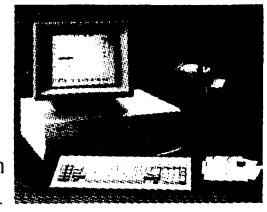
The Intel System 120 delivers real-time capability to users demanding a low-cost system for running time-critical applications. The System 120 combines the rich functionality of the world's most popular Real-Time Operating System with the power and speed of the 386™ 32-bit microprocessor.

For the first time, the System 120 makes available the ability to host, on a standard computing platform, real-time applications that have previously been impractical with other AT-Bus systems.

Applications developed for the System 120 can be moved easily to Intel's complete line of MULTIBUS® I and MULTIBUS II products, giving the user a broad spectrum of price, performance, and functions from which to choose.

FEATURES:

- iRMX® II.3: a complete real-time operating system; more than a kernel
- Intel 386™ low-cost AT-Bus system
- Development platform for iRMX applications
- Easy migration of applications to and from MULTIBUS systems
- I/O expansion for PC-AT* and PC boards
- iRMX II.3 to DOS file exchange capability
- OpenNET™ networking support.
- Intel 80387 numeric co-processor support



The System 120 as an iRMX® development platform with the addition of a monitor, video adapter, and keyboard.

June, 1988
Order Number: 280649-001

iRMX® II.3: A COMPLETE REAL-TIME OPERATING SYSTEM

iRMX system software is used in more real-time designs than any other operating system. There are over 500,000 CPUs worldwide running the iRMX Operating System, making it the most widely accepted standard real-time operating system for microprocessor-based designs.

The iRMX II.3 Operating System provides a rich set of real-time programming facilities not found in general-purpose operating systems such as DOS, OS/2** or UNIX**. These include:

- Pre-emptive, dynamic priority-based scheduling of application tasks
- Bounded interrupt latency
- Multitasking support for real-time applications
- Inter-task communications through priority-based mailboxes, semaphores, and regions
- Interrupt management with exception handling
- Cross or on-target development

The iRMX II.3 Operating System also offers high performance and code integrity. iRMX typically responds 100 times faster than general-purpose operating systems, enabling real-time applications to keep up with the rapid data and control flow of machine and communication interfaces. Code integrity is ensured through sophisticated memory protection schemes.

Finally, the iRMX II.3 Operating System is highly configurable. Its modular design allows you to select only those functions and device drivers that are required. This keeps memory requirements to a minimum. Guided by the many examples in the System 120 Development Toolkit documentation, you can add custom device drivers and applications to the iRMX Operating System.

LOW COST PC-AT BASED CONFIGURATIONS

The System 120 is available with a number of memory and mass storage options to fit a range of applications. These include a basic system with 8 open slots, and a 40M-byte hard disk system with an 80387 and floppy disk (see Table 1).

Intel offers PC-AT add-in boards for the System 120 that include: 2M-byte and 8M-byte 32-bit memory boards, the OpenNET PCLINK2 networking board and the iPCX 344A BITBUS™ board. A standard keyboard is also available.

Table 1: System 120 Configurations

PRODUCT CODE	CPU		RAM	FLOPPY DISK	HARD DISK
	386	387	M-bytes	360 K-bytes	40 M-bytes
SYP12016Z0*	✓		2		
SYP12016Z40*	✓	✓	2	✓	✓

*Available Q4 1988.

EASY APPLICATION DEVELOPMENT

Development Toolkits are available for development and testing of applications. These toolkits contain the System 120 (in 40M-byte or 80M-byte configurations), iRMX II.3 and languages, an editor and a debugger (see Table 2). The iRMX II.3 Operating System includes a pre-configured operating system, object modules and device drivers, interface libraries, and a powerful tool for system generation.

System 120 Development Toolkits

You can develop applications directly on the system using the System 120 Development Toolkit. In addition to the special version of the iRMX II.3 Operating System for the System 120, the toolkit contains: PL/M 286 Compiler, ASM assembler, AEDIT and a source level debugger, Soft-Scope* II. Intel also offers a number of compilers (C, Fortran, Pascal), performance and debug tools for iRMX II.3.

MULTIBUS Development Toolkits

Toolkits are also available for the development of MULTIBUS and component-level applications. These are packaged with a preconfigured operating system and allow development of MULTIBUS I and MULTIBUS II applications on a low-cost System 120 platform.

Table 2: System 120 and MULTIBUS® Development Toolkits

PRODUCT CODE	SOFTWARE			CPU	RAM	DISKS			
	iRMX® II.3 FOR SYSTEM 120	iRMX® II.3 FOR MULTIBUS®	PL/M 286 ASM AEDIT SOFTSCOPE	386 & 387	Mb	FLOPPY		HARD	
						360Kb	1.2Mb	40Mb	80Mb
SYS120KITB40	✓		✓	✓	2.5	✓		✓	
SYS120KITB80	✓		✓	✓	4.5	✓	✓		✓
SYS120KITZ40*	✓		✓	✓	2	✓		✓	
SYS120KITZ80*	✓		✓	✓	4	✓	✓		✓
SYS120MBZ40*		✓	✓	✓	2	✓		✓	
SYS120MBZ80*		✓	✓	✓	4	✓	✓		✓

*Available Q4 1988

BITBUS is a registered trademark of Intel Corporation.

**OS/2 is a trademark of Microsoft.
UNIX is a trademark of AT&T.
Soft-Scope is a trademark of Concurrent Sciences, Inc.

FEATURES

APPLICATION MIGRATION TO HIGHER PERFORMANCE SYSTEMS

Applications written for the System 120 can be easily moved to the higher performance and functionality of MULTIBUS I and MULTIBUS II designs. That's because the System 120 iRMX II.3 Operating System is binary compatible with the MULTIBUS implementation of iRMX II.3.

The iRMX II.3 Operating System spans the entire Intel systems product line, from the low-cost System 120 through the MULTIBUS I System 320, to the high-end, multi-processing MULTIBUS II products. Applications can easily be re-hosted on different bus architectures, allowing you to create a group of products satisfying a wide range of customer performance requirements.

DOS APPLICATION COMPATIBILITY

The System 120 supports the DOS 3.X operating system as well as iRMX II.3, enabling you to use popular DOS applications to process data collected in real time. The System 120 hard disk can be divided into iRMX and DOS partitions, allowing users to boot from either partition. A System 120 utility allows transfer of iRMX files into a DOS environment. DOS execution requires a customer-supplied version of DOS, a video adapter, a monitor, and a keyboard.

WORLDWIDE SERVICE AND SUPPORT

The System 120 is fully supported by Intel's worldwide staff of trained hardware and software support engineers. Intel also provides field application assistance, extensive iRMX Operating System classes, maintenance services, and a help hotline.

The System 120 Development Toolkits come with a 90-day software warranty and a one-year hardware warranty. In volume, the System 120 comes with a 90-day hardware warranty. Other support packages are optionally available; for more information please contact your local Intel Sales Office.

INTEL QUALITY AND RELIABILITY

The System 120 is designed to meet the high standards of quality and reliability that users have come to expect from Intel products. The iRMX Operating System software has undergone thousands of hours of testing and evaluation and is one of the most stable operating systems in the industry today.

SPECIFICATIONS

SYSTEM 120 BASE SYSTEM

Central Processor	Intel 80386, 16 MHz
Floating-Point Processor	Intel 80387, 16 MHz**
Main Memory	2M Bytes on CPU Board* 0.5M Bytes on CPU Board
Maximum RAM	16M Bytes
Cycle Time	120 ns
Data Bus Width	32-Bits
Error Detection	Byte Parity
I/O	1 serial port (asynchronous, RS232C, 9-pin connector) 1 parallel port (centronics compatible, 25 pin connector)
8 expansion slots:	2 32-or 8-bit slots 4 16-bit slots 2 8-bit slots

REGULATIONS

Meets or exceeds the following requirements:

Safety	
US	UL 478 5th Edition
Canada	CSA C22.2 No. 154-M1983
Europe	IEC 435 and VDE 0806
EMI/RFI	
US and Canada	FCC47 CFR Part 15 Subpart J Class A
Europe	VDE 0871 Level A

*Available Q4, 1988
**Not included in SYP12016Z0

ENVIRONMENT

Ambient Temperature	
System On:	15.6 to 32.2°C
System Off:	−34 to 60°C
Relative Humidity	
System On:	5 to 85%, noncondensing
System Off:	5 to 95%, noncondensing
Altitude	
Operating:	2133.6 meters (7000 ft.) maximum
Static Discharge:	7.5 Kv maximum

ELECTRICAL

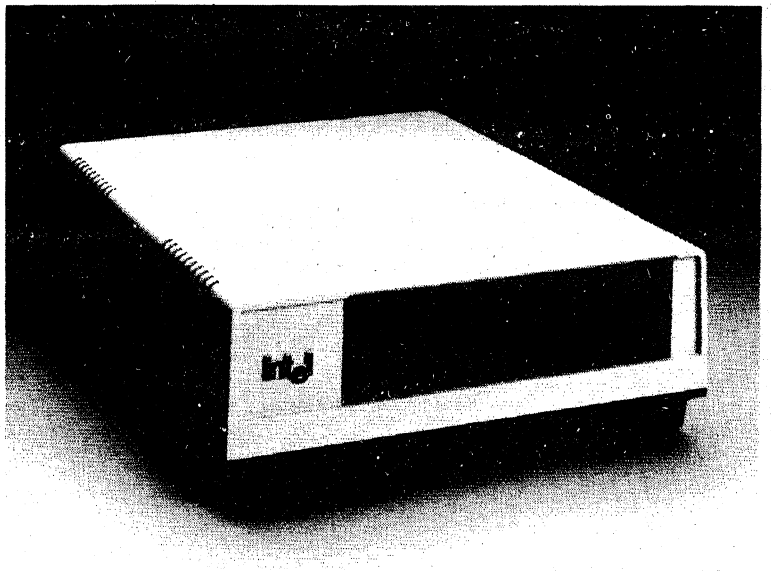
AC Voltage/Frequency	Switching power supply, 115 V/60Hz or 230V/50 Hz; convenience outlet
DC Power	220 Watts
+5 V	23.0 A maximum continuous
+12 V	8.0 A maximum continuous; 11.0 A maximum total for 15 seconds
−12 V	0.5 A maximum continuous
−5 V	0.5 A maximum continuous

DIMENSIONS

Length	441 millimeters (17.3 inches)
Width	541 millimeters (21.3 inches)
Height	163 millimeters (6.5 inches)

WEIGHT

Base System:	20 kilograms (44 lbs)



SYSTEM 310 AP

The System 310 AP is faster than many minicomputers. Powerful dedicated processors for communications and mass storage input/output control allow the 8 MHz 80286 CPU to concentrate on application software. The System 310 AP is open, which means you can upgrade performance and/or functionality in the future without purchasing a new system. The open system design protects your investment from becoming obsolete. Open systems design also means easy system customization with Intel and third-party add-in MULTIBUS® boards.

FEATURES

- 80286 Based System
- Open System MULTIBUS architecture for upgradeability and growth
- iRMX® Operating System
- OpenNET™ Local Area Networking
- Total hardware and software support from Intel's worldwide customer support organization

June, 1988
Order Number: 270129-005

FEATURES

SYSTEM 310 AP—AN OPEN SYSTEM

The Intel System 310 AP is based on the MULTIBUS architecture, (IEEE 796) industry standard system bus supported by over 200 vendors providing over 2000 compatible products.

The System 310 AP is an 80286 based open system designed with expansion in mind. The system can be expanded to accommodate up to 9MB of parity-checked RAM, all accessible with no wait states across MULTIBUS's Local Bus Extension (LBX™). For terminal communications, the systems can be expanded to a total of 18 RS232 serial ports.

The System 310 AP supports 40MB-140MB of Winchester disk storage. The 310 AP also supports a 320KB 5¼" floppy drive and a 60MB streaming tape cartridge drive.

iRMX® OPERATING SYSTEM

The iRMX operating system delivers real-time performance. Designed to manage and extend the resources of the System 310 AP, this multitasking operating system provides configurable resources ranging from interrupt management and standard device drivers to data file maintenance commands for human interface and program development.

A wide range of popular industry standard high-level languages are supported for application development. The iRMX facilities also include powerful utilities for easy, interactive configuration and debugging.

OpenNET™—NETWORKING CAPABILITY

Intel's OpenNET product family provides a complete set of networking software and hardware that follows the International Standards Organization (ISO) Open Systems Interconnect (OSI) model.

OpenNET Network File Access Protocol adheres to the IBM/Microsoft/Intel Core File Sharing Protocol specification, providing transparent local/remote file access and file transfer capability between Intel's complete line of systems products, as well as with MSNET* and VAX/VMS** based systems.

The System 310 AP distributes the transport protocol processing to intelligent Ethernet controllers that host Intel's OSI-compliant iNA 960 Class 4 Transport software, thereby unburdening the system CPU for greater performance.

INTEL SERVICE AND SUPPORT

The System 310 AP is backed by Intel's worldwide service and support organization. Total hardware and software support is available, including a hotline number for when you need help fast.

SPECIFICATIONS

SYSTEM/MODELS	310 AP-40B	310 AP-41B	310 AP-42	310 AP-82B	310 AP-142
Microprocessor	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz	80286 8 MHz
Numeric Coprocessor	80287	80287	80287	80287	80287
RAM Memory	1MB	1MB	1MB	2MB	2MB
Floppy	360KB	360KB	360KB	360KB	360KB
Mass Storage	40MB	40MB	40MB	85MB	140MB
Tape Backup	NA	NA	60MB	60MB	60MB
Serial I/O Ports	2	10	10	14	10
Parallel Ports	1	1	1	1	1
OpenNET					

ENVIRONMENT

Operating Temperature	10°C to 35°C
Wet Bulb Temperature	26°C maximum
Relative Humidity	20% to 70% noncondensing
Altitude	Sea level to 8,000 feet

REGULATIONS

Meets or exceeds the following requirements:

Safety	
US	UL114
Canada	CSA C22.2
Europe	TUV ICE 435
EMI/RFI	
US and Canada	FCC Docket 20780—Class A
Europe	VDE 0871 Class A

ELECTRICAL

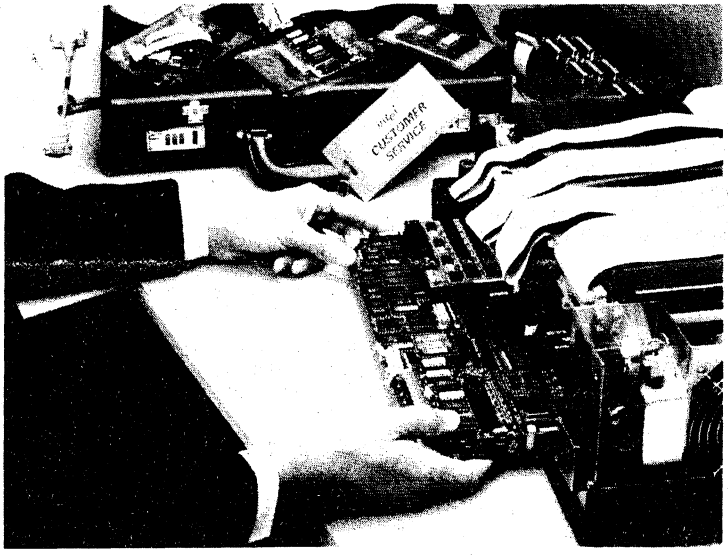
DC Power Output	360 watt maximum
AC Power Input	88-132 VAC or 180-264 VAC, 47-63 Hz (user selectable)

DIMENSIONS

Height	6½"
Width	17"
Depth	22"
Weight	Approx. 55 lbs

* MSNET is a trademark of Microsoft
** VAX/VMS is a trademark of Digital Equipment Corporation

SYSTEM 310 386 UPGRADE



Intel's System 310 386 Upgrade offers the user an upgrade path to the performance of the 386™ microprocessor without sacrificing existing software and hardware investments. This Customer Service Installed upgrade is designed for the System 310 and System 310AP series of microcomputer systems using iRMX II operating system.

STANDARD FEATURES

- 16 MHz 386™ Microprocessor
- 16 Bit 80287 Numeric Data Processor
- Memory Options:
  1, 2, 4 and 8 MB
  0 wait state RAM
- Systems Confidence Test (SCT) and boot firmware
- Installed by Intel Customer Service at your location

intel

October, 1987
Order Number 280705-001

SPECIFICATIONS

The iSXM™ 386 Kit is designed to meet certain UL, FCC, CSA, IEC and VDE requirements when it is installed into an INTEL System 310 and System 310AP. It is the responsibility of the customer to reconfirm that the specific systems they have created from MULTIBUS elements continue to meet the required safety and environmental specifications in the customer environment. Intel is not responsible for any changes made after the product is accepted by Intel's customer.

SAFETY REQUIREMENT/EMI LIMITS

The iSXM 386 Kit is designed to meet:

Safety:
- UL 478 5th edition
- CSA C22.2 no. 154
- TUV IEC435 and VDE 0806

RMI/EMI:
- FCC 47 CFR Part 15 Subpart J Class A
- VDE 0871 Level A

Actual compliance will depend on the modules, peripherals and cable connectors which you install in the system.

ELECTRICAL

Voltage and Maximum Current:

iSXM 386 KIT-1, 1 MB Memory

±5 VDC	±5%	12.5 amps
+12 VDC	±5%	0.025 amps
−12 VDC	±5%	0.025 amps

2 MB Memory add .3 amps @5 VDC
4 MB Memory add .0 amps @5 VDC
8 MB Memory add .3 amps @5 VDC

BASE REQUIREMENTS

You must have a current copy of iRMX II Release 2.0 or later installed on your system before the system can be upgraded. The −4 and −8 kits are recommended for use on 80 MB or 140 MB Winchester based systems only.

ORDERING INFORMATION

Your memory requirements will determine the product order code:

Memory Requirement	Order Code
1 MB RAM	iSXM386KIT-1
2 MB RAM	iSXM386KIT-2
4 MB RAM	iSXM386KIT-4
8 MB RAM	iSXM386KIT-8

SYSTEM SOFTWARE

iRMX II Languages:
FORTRAN 286, C286
Assembler 286, PL/M 286

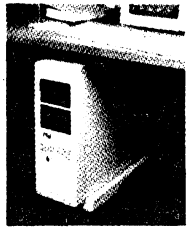
Intel believes that the information in this document is accurate as of its publication date. Such information is subject to change without notice. Intel is not responsible for any inadvertent errors.

iRMX® SYSTEM 320

Intel combines the power of its high performance 386™ microprocessor-based System 320, the widely used iRMX II real-time software, complete network service software and comprehensive customer support capabilities to deliver, install and maintain a complete system. The result is the iRMX System 320 gives you the performance and capabilities of a minicomputer at less than half the cost. The system is especially suited for applications requiring real-time response and resource control typically found in financial transaction, industrial automation, medical and communications markets. The iRMX System 320 is also appropriate as the development environment for module-based design.

iRMX® SYSTEM 320 FEATURES

- 80386 Based System
- iRMX Real-time Multitasking Operating System
- Open System Architecture
- OpenNET Local Area Networking
- Complete Installation, Service and Support
- Worldwide User Group Support
- Range of Configurations



intel

September, 1988
Order Number: 280502-002

FEATURES

iRMX® II—REAL-TIME SOFTWARE

The iRMX II operating system delivers real-time performance. Designed to manage and extend the resources of the System 320, this multitasking operating system provides configurable resources ranging from interrupt management and standard device drivers to data file maintenance commands for human interface and program development. The iRMX II facilities also include powerful utilities for easy, interactive configuration and debugging.

SYSTEM 320—AN OPEN SYSTEM

The iRMX System 320 is based on MULTIBUS architecture, (IEEE 796) industry standard system bus supported by over 200 vendors providing over 2000 compatible products, and on the iRMX II operating system composed of modular layers, highly configurable for tailoring to target applications. A wide range of popular industry standard high-level languages are supported for application development. Special configurations can be tailored by the user, by Intel's Custom System Integration group or by Intel's authorized Value Added Distribution Centers.

OpenNET™ NETWORKING CAPABILITY

Intel's OpenNET product family provides a complete set of networking software and hardware that follows the International Standards Organization (ISO) Open Systems Interconnect (OSI) model.

OpenNET Network File Access Protocol adheres to the IBM/Microsoft/Intel Core File Sharing Protocol specification, providing transparent local/remote file access and file transfer capability between Intel's complete line of systems products, as well as with MSNET* and VAX/VMS** based systems.

The System 320 distributes the transport protocol processing to intelligent Ethernet controllers that host Intel's OSI-compliant iNA 960 Class 4 Transport software, thereby unburdening the system CPU for greater performance.

INSTALLATION SERVICE & SUPPORT

The Intel iRMX System 320 is backed by Intel's worldwide service and support organization. Installation is available to quickly get the system up and running. Total hardware and software support is available, including a hotline number for when the user needs help fast. Intel also provides hands-on training workshops to give the user a thorough understanding of the iRMX System 320. These workshops are conducted at Intel training centers or customer sites worldwide.

WORLDWIDE USER GROUP SUPPORT

iRUG (iRMX User Group), provides members a user's library of iRMX software tools and utilities, access to the group bulletin board, receipt of regularly published newsletters and invitations to User Group Conferences. iRUG numbers over 42 local chapters in 20 countries worldwide.

RANGE OF CONFIGURATIONS

Intel offers a wide range of configurations for the iRMX System 320. Contact your local Intel representative for further information.

* MSNET is a trademark of Microsoft
** VAX/VMS is a trademark of Digital Equipment Corporation

SPECIFICATIONS

ENVIRONMENT

Operating Temperature	10°C to 40°C
Wet Bulb Temperature	26°C maximum
Relative Humidity	85% at 40°C
Altitude	Sea level to 10,000 feet

REGULATIONS

Meets or exceeds the following requirements:

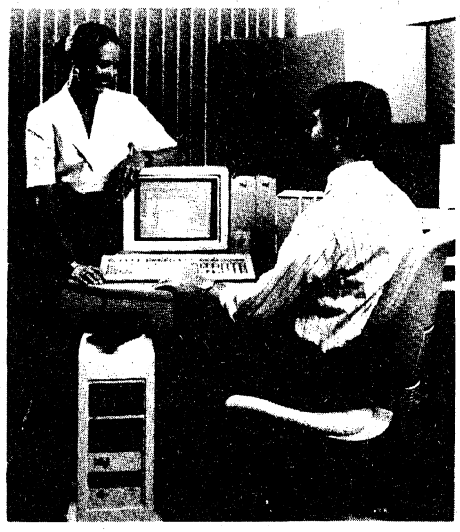
Safety	
US	UL 478
Canada	CSA C22.2
Europe	IEC 435
EMI/RFI	
US and Canada	FCC Class B Computing Device
Europe	VDE Limit Class B

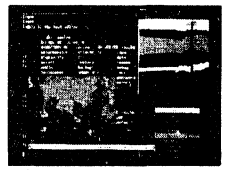
ELECTRICAL

DC Power Output	435 watt maximum
AC Power Input	88-132 VAC or 176-264 VAC, 47-63 Hz, single phase

DIMENSIONS

Height	8"
Width	17.5"
Depth	22.25"
Weight	Approx. 55 lbs





UNLOCKS THE POWER OF REAL-TIME MULTIPROCESSING IN AN INTEL® 386™ MULTIBUS® II OEM SYSTEM

The Intel iRMX II System 520 and MULTIBUS II System Architecture (MSA) make it easy to unlock the power of real-time multiprocessing. The System 520 is the first in a family of high performance, real-time OEM systems to combine Intel's open MSA architecture, the powerful 386 microprocessor, and the industry-leading iRMX II Real-Time Multitasking Operating System. Together, they provide the first easily scalable, recomposable multiprocessor open bus system.

As an open OEM system, the System 520 allows users to add to the basic system, or purchase the system's contents separately and repackage them into another enclosure. Intel's MSA provides this capability via a structured set of open, standard interfaces and protocols that build on and are fully compatible with the MULTIBUS II (IEEE 1296) bus standard. As a result, the iRMX II System 520 provides new standards of ease of integration, ease of use, and board compatibility for the OEM.

FEATURES

- 386-based high performance MULTIBUS II multiprocessor OEM system
- iRMX II Real-Time Multitasking Operating System
- 386 Application Processor Expansion (1 to 4)
- High performance 386-based SCSI I/O subsystem
- Easy system expansion via Intel's MULTIBUS II System Architecture (MSA) & iSBC® family
- OpenNET™ transparent remote file sharing & virtual terminal between iSBC 386 processors and IEEE 802.3 networked systems
- Hardware windowed graphics/virtual terminal support
- iRMX II development systems available

intel

Order Number: 280672-001

THE MULTIBUS II SYSTEM ARCHITECTURE (MSA)

The System 520 is built around Intel's MULTIBUS II System Architecture (MSA) to ease the development and integration work of MULTIBUS II OEM system designers. Intel's MSA delivers open system interface and protocol standards that build-on and extend the basic MULTIBUS II (IEEE/ANSI 1296) bus standard. The MSA specifications define diagnostics control/built-in self test, system initialization and boot loading, board configuration, and message passing. The user benefits from MSA because the level of vendor/board compatibility has been raised above basic electrical bus specifications to a set of powerful programmatic interfaces that "hide" the bus specifics with software. This provides OEMs quicker time to market with faster system integration and shorter design cycles.

EASY USER EXPANSION AND "RECOMPOSABLE" SYSTEMS

The MULTIBUS II System Architecture is used as the foundation for integrating Intel's full line of Single Board Computer (iSBC®) modules and iRMX II system software into the System 520. The "recomposability" of the System 520 means that OEMs have the option to buy the contents of the system (i.e. the boards, the firmware, the software, etc.) separately, and "recompose" all or part of the system's pieces into a different configuration or enclosure.

The System is available initially in two basic hardware configurations (See Table 1). As hardware only platforms, they may be purchased without the iRMX II Operating System by OEMs requiring a MULTIBUS II System 520 to host their own operating system software.

Easy user expansion and recomposability of the System 520 is supported by a line of "System Integration Toolkits" (SIT kits) that contain all the firmware necessary to allow standard, off-the-shelf MULTIBUS II boards to integrate cleanly into the System 520. With these toolkit products, the OEM can purchase the pieces needed and profit from greater ease of use, ease of integration, and leveraging higher levels of open standards.

A NETWORK IN THE SYSTEM

Using the MULTIBUS II backplane as an ultra-fast network (40MBytes/sec), multiple peer-to-peer 386™-based iRMX application processors operate as independent "networked" iRMX systems over the MULTIBUS II Parallel System Bus (PSB). Each iRMX application processor running Intel's OpenNET™ network software will provide transparent distributed file sharing, file transfer, and virtual terminal capability among all application processors on the backplane, and IEEE 802.3-based (1.25MBytes/sec) OpenNET networked system nodes (See Figure 1). Using the PSB as a network makes the System 520 a high performance "minicomputer" cluster condensed into one multiprocessor system.

The major advantage to the OEM is total network extensibility inside and outside the system, using the same OpenNET software. The key benefits are: reduced cost through the "replacement" of multiple uni-processor networked systems and servers, drastically reduced physical space requirements, increased overall network throughput and performance, and preserved software investment.

WINDOWED GRAPHICS AND VIRTUAL TERMINAL SUBSYSTEM

The iRMX II System 520 hosts a new iRMX Graphics Interface driven by Intel's 82786-based graphics subsystem, the iSBX 279. The graphics subsystem and its companion software use the unique hardware windowing feature of the 82786 display processor to provide a windowed virtual terminal console with graphics capabilities. With its on-board processing power and its large graphics memory buffer, the iSBX 279 off-loads the application processors of the display processing tasks. The user interfaces to the System 520's subsystem via an RGB color monitor (640 × 480), a mouse, and an AT-style keyboard (purchased separately).

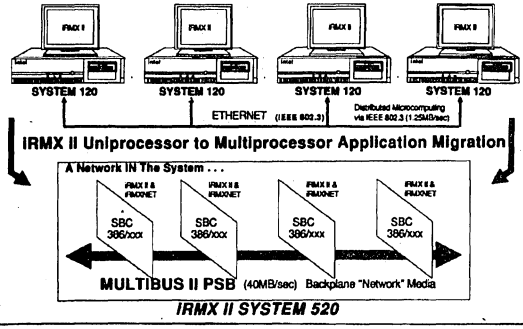


Figure 1: A Network IN the System with an iSBC 386 board cluster; also shows iRMX II application migration from networked System 120s to an iRMX II System 520 running OpenNET IN the System

HIGH PERFORMANCE 386-BASED I/O SUBSYSTEM

The System 520 uses the Intel iSBC 386/258 SCSI Peripheral Controller to provide minicomputer level I/O performance to SCSI (Small Computer System Interface) mass storage devices. I/O critical applications are accelerated by the combination of a 16 MHz 386 processor, a large (1-4MBytes) data buffer for cacheing, and a 4 MByte per second SCSI synchronous transfer rate. This flexible I/O subsystem can be used as an intelligent disk controller, or a hybrid iRMX II application processor/file server, through soft-loaded "serverware."

APPLICATION MIGRATION ACROSS INTEL386™ SYSTEM LINES

With the addition of the System 520, OEMs can easily migrate their real-time applications across a complete line of Intel system products, each offering a unique level of price, performance, and function. The iRMX II Operating System supports application compatibility across the three leading open system bus standards: AT-bus, MULTIBUS I, and MULTIBUS II. The link that binds the systems together is OpenNET networking software for Ethernet (IEEE 802.3) and MULTIBUS II message passing. The System 520 provides the developer a migration path from a group of uni-processor networked systems to a high-speed cluster of MULTIBUS II boards running the same operating systems and network software (See Figure 1). The customer can choose the combination of packaging, CPU/system performance, and communications bandwidth suited for the application.

iRMX II: A FULL FEATURED REAL-TIME OPERATING SYSTEM FOR MULTIBUS II

Intel's iRMX II Real-Time Multitasking Operating System is a full featured, stand alone operating environment, designed to address the complete range of real-time applications, from embedded control designs to reprogrammable MULTIBUS II multiprocessor systems. It provides complete MULTIBUS II facilities supporting MULTIBUS II Transport message passing and Interconnect space access. Using iRMX II software, engineers can assemble a powerful, "cluster" of application processors into a single, integrated multiprocessor system. The iRMX II system software manages all message transmission and reception, making the construction of real-time multiprocessor systems easier.

The iRMX II Operating System provides a rich set of real-time programming facilities not found in general-purpose operating systems. Some of its key features include pre-emptive, dynamic priority-based scheduling of application tasks; bounded interrupt latency; multitasking support; inter-task communications & synchronization through priority-based mailboxes, semaphores, and regions; and interrupt management with exception handling. By combining these features with a modular design; quick response; and sophisticated memory protection schemes, the OEM receives a highly configurable, customizable operating system with the high performance and code integrity that real-time applications require.

COMPLETE MULTIBUS II DEVELOPMENT ENVIRONMENT

The iRMX II System 520 is also available as a bundled, complete, networked iRMX II Development System for MULTIBUS II modules development, software development and testing of real-time applications. The System 520 is unique as a MULTIBUS II development system, because its multiprocessor cluster capability can support both on-target or cross-hosted system/software development in one chassis.

OpenNET NETWORKING CAPABILITY

Intel's OpenNET product family provides a complete set of networking software and hardware that follows the International Standards Organization (ISO) Open Systems Interconnect (OSI) seven layer model. The System distributes the ISO/OSI transport protocol processing to intelligent Ethernet controllers hosting Intel's OSI compliant iNA 960 Class 4 Transport software. Intel's OpenNET Network File Access (NFA) protocol provides the upper layer functionality of transparent local/remote file access and file transfer between Intel's complete line of system products, as well as MSNET*-based personal computers. The OpenNET NFA protocol adheres to the standard IBM*/Microsoft*/Intel Core File Sharing protocol specification.

WORLDWIDE SERVICE AND SUPPORT

The iRMX II System 520 is fully supported by Intel's worldwide staff of trained hardware and software support engineers. Intel also provides field application assistance, extensive iRMX Operating System classes, maintenance services, and a help hotline.

The System 520 OEM System products come with a standard 90-day hardware warranty. The iRMX II System 520 MULTIBUS II Development System product comes bundled with a one (1) year service warranty. This one year warranty includes: hardware installation and one year of on-site maintenance, software installation of the iRMX II Operating System and 48 hours of TIPS phone support.

INTEL QUALITY AND RELIABILITY

The System 520 is designed to meet the high standards and reliability that users have come to expect from Intel products. The iRMX Operating System software has undergone thousands of hours of testing and evaluation, and is one of the most stable operating systems in the industry today.

*IBM is a registered trademark of International Business Machines Corp.
*Microsoft and MSNET are trademarks of Microsoft Corporation.

SYSTEM 520 CONFIGURATION/OPTIONS—TABLE 1

Product	SBC CSM Cent. Serv.	SBC 386/120 w/4 MB	SBC 386/258 w/4 MB	SBX 279 Graphics	SBC 186/410 Term. Ctlr.	SBC 186/530 Enet Ctlr.	1X0MB Hard Disk (SCSI)	380 MB Hard Disk (SCSI)	125/150 MB ¼" Tape (SCSI)	1.2 MB Flopp. w/Adapt (SCSI)	RMX II Dev. System S/W Pack	Floor Stand Chassis Sta	Table Top Chassis (optum)
System 520 OEM Base Plus I/O	✔	✔	✔	✔	✔	✔	Add-[1] In.	✔	✔	✔		✔	T[1]
System 520 OEM Base[1]	✔		✔				Add-[1] In.			✔		✔	T[1]
System 520 Development System	✔	✔	✔	✔	✔	✔	Add-[1] In.	✔	✔	✔	✔	✔	

[1]Contact Intel for configuration availability information.

iRMX II System 520 Development System Software Contents:

iRMX II Operating System
iRMXNet Networking Software
iNA 960 Networking Transport Software
SYRII Language Kit: (PLM & ASM 286, builder/binder)
C 286 compiler
iRMX Toolbox
Softscope* II Source Level Debugger
AEDIT Editor
RUN/UDI for 86-based UDI Development Tools
iPPS PROM programmer support
iSBX 279 Graphics Interface Software
OpenNET Virtual Terminal (VT)

*Softscope is a registered trademark of Concurrent Sciences Inc.

REGULATIONS

Meets or exceeds the following requirements:

Safety

US	UL 478 5th Editon
Canada	CSA C22.2 No. 220
Europe	IEC 380 and VDE 0806

EMI/RFI

US & Canada	FCC47 CFR Part 15 Subpart J Class B
Europe	VDE 0871 Level B

ELECTRICAL

DC Power Output	535 watt maximum
AC Power Input	88-132 VAC or 180-264 VAC; 47-63 Hz, single phase

OPERATING ENVIRONMENT

Operating Temperature	10°C to 40°C
Relative Humidity	85% non-condensing (operating) 95% condensing (non-operating)
Altitude	Sea level to 10,000 feet

DIMENSIONS

	Floorstand	Table Top
Height	22.25"	8"
Width	8"/12" at base	17.5"
Depth	23"	22.25"
Weight	Approx. 70 lbs.	Approx. 60 lbs.

ORDERING INFORMATION

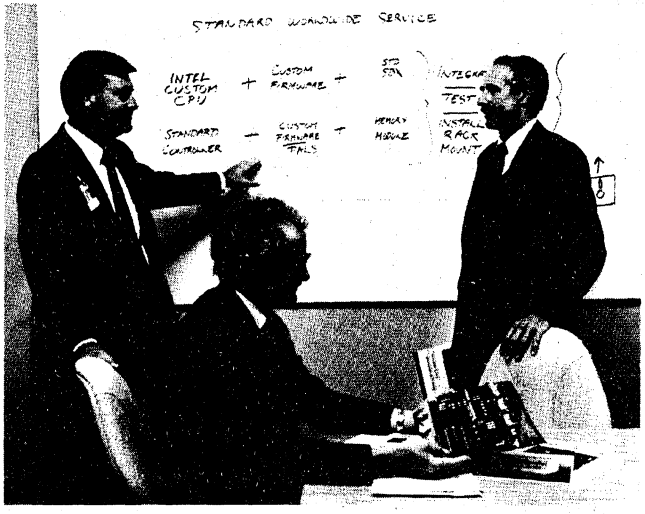
SYP520R1BP	System 520 MULTIBUS II Base Plus I/O OEM System (SYP520R1BPT for Table Top option)
SYP520R1B	System 520 MULTIBUS II Base OEM System (SYP520R1BT for Table Top option)
SYS520R1DKIT2	iRMX II System 520 MULTIBUS II Development System

LICENSING

Before iRMX II software will be shipped, a customer must sign (or have already signed) Intel's Software License Agreement (SLA). Once the SLA is signed, the customer is licensed for development. Customers who want to "incorporate" portions of the iRMX II Object Code in an application will have to sign an Incorporation License which clearly spells out the terms and conditions under which incorporations can be made.

Contact your local Intel office for more information on the System 520 and for iRMX licensing.

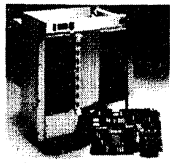
For more information or the number of your nearest Intel sales office, call 800-548-4725 (good in the U.S. and Canada).

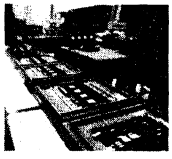


DESIGN, MANUFACTURING AND INTEGRATION TO YOUR SPECIFICATIONS

The Intel Custom Board and Systems Group offers a broad array of custom services for OEMs seeking unique solutions for their markets. We have the expertise to design, manufacture and test products to your specifications. We also modify, integrate and test Intel and other vendors' products to your requirements.

Our custom services help you hit your market window. You are able to use our custom OEM product expertise and concentrate on your value-added expertise. Though we deliver *custom* products, you can count on Intel's high *standards* of quality, reliability, worldwide service, and support.





SERVICES:

- Modifying MULTIBUS® and AT®-bus boards to specific functional requirements.
- Integrating boards and system components to fit application needs.
- Redesigning standard Intel products to meet your unique price/performance requirements.
- modifying standard modules and systems to enhance product reliability and environmental characteristics
- Developing custom software and firmware.
- Advanced manufacturing technology and processes

intel

September, 1988
Order Number: 280676-001

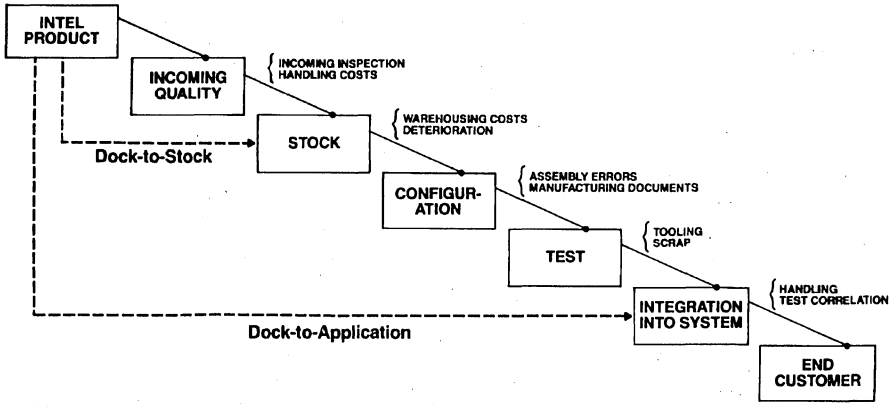


Figure 1: Dock to Application Avoids Costly Steps

CUSTOM PROJECTS MILESTONES MODEL

	Quote	*EPS*	*Prototype (<5 units)*	*Preproduction* (optional)*	*Production**
RECONFIGURE A BOARD	10 work days	2 weeks	1–2 mo	4–5 mo	5–6 mo
INTEGRATE BOARDS	10 days	2 weeks	1–2 mo	4–5 mo	5–6 mo
INTEGRATE SYSTEM	10 days	4 weeks	2–3 mo	5–6 mo	6–7 mo
MINOR BOARD DESIGN	10 days	4 weeks	3 mo	6 mo	9 mo
MAJOR BOARD DESIGN	10 days	8 weeks	6 mo	9 mo	12 mo
		After Receipt of Order			

*Requires External Product Specification (EPS) approval

Figure 2: Typical Schedule for Custom Products

MODIFYING BOARDS TO FUNCTIONAL REQUIREMENTS

Starting with existing products we will develop manufacturing and test programs to provide the functionality you specify. This includes jumper modification, custom firmware and PAL programming, higher reliability parts replacement and other similar services.

INTEGRATING BOARDS AND SYSTEMS

Intel quality allows you to implement "dock-to-stock" programs while Intel custom capabilities allow you to implement "dock-to-application" programs. We can integrate your requirements at both board and system levels. The resulting custom tailored board or system moves from your dock to your application environment with no additional steps or inspections required. (See figure 1.)

IMPROVING PRICE/PERFORMANCE

Sometimes your specific needs will present a cost/performance demand that can't be met by our broad array of standard products. In today's stringent business climate you need to match your products to the needs of the market or you risk the loss of market share and your competitive edge. Intel will take standard products and add or delete functionality to your price/performance requirements. And because you are leveraging proven designs you can enter your market at the lowest risk and in a timely fashion.

ENHANCING PRODUCT RELIABILITY

Intel standard system products are designed and manufactured to work in commercial environments. If your needs fall outside normal temperature, reliability or other environmental ranges (extended reliability, wider temperature range, shock and vibration . . .) we can recommend and apply various methods for enhancing these characteristics, at the board and system level.

DESIGNING TO YOUR REQUIREMENTS

Intel has experienced senior engineering resources on staff to design and build products to your specifications. These engineers are skilled at working to understand your needs and to propose the best solution for your requirements. We will provide you with a detailed proposal of key milestones and deliverables based on a commonly agreed set of specifications. Once we implement your program you will benefit from dealing with an organization that has the skill to take your product from design to manufacture and test.

CUSTOM SOFTWARE AND FIRMWARE

Your custom application may also include custom software. Our team will work closely with you on defining these software needs and implementing them. This allows Intel to be your total custom service vendor, ensuring a strong link of support from hardware to software.

CUSTOM SERVICES FOCUSED ON YOUR NEEDS

Your local sales office will work with you and our group to characterize your technical and business requirements. Our engineers will work with your engineers to review your functional or technical specifications and then propose a solution that best meets your needs. Our quotes specify all costs involved in a project, including non-recurring engineering, per unit price, key milestones and delivery of prototypes and products (refer to figure 2).

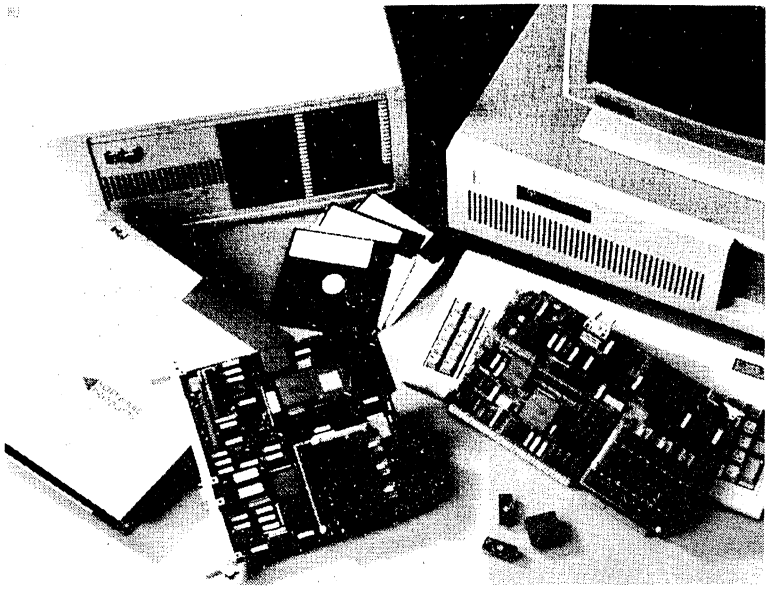
Dedicated engineering groups are assigned to your project and are responsible for all its aspects. The External Product Specification that we provide details all the form, fit and function characteristics of your product, including any compliance you may require: UL, FCC, VDE, CSA and TÜV. Regular engineering contact and program reviews ensure that your product is delivered to your specifications and on time.

ADVANCED MANUFACTURING TECHNOLOGY AND PROCESSES

Throughout Intel's existence we have placed great emphasis on high quality and control in our manufacturing processes. We use the latest in manufacturing and process technologies (surface mount, wave solder, automated lines and factories, statistical process control . . .) to ensure that all system products, custom and standard, are manufactured to the highest standards of workmanship and reliability.

WORLDWIDE SERVICE AND SUPPORT AN INTEL STANDARD

The Intel worldwide service organization is involved in all steps of the design process of custom products. Because the same design, manufacture and test procedures are used on your custom product, it is serviced and supported by Intel personnel worldwide.

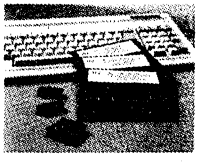


A 32-BIT REAL-TIME KERNEL

The iRMK™ Version 1.2 Real-time Kernel is the 32-bit real-time executive developed, sold, and supported by Intel, the Intel386™ architecture experts. It reduces the cost and risk of designing and maintaining software for numerous real-time applications such as embedded control systems and dedicated real-time subsystems in multiprocessor systems.

FEATURES

- 32-bit real-time multitasking kernel
- Rich set of real-time services
- Designed and optimized for the Intel386™ and Intel376™ families
- Extremely fast execution with predictable response times for time critical applications
- Compact design, as small as 8K bytes
- Multiprocessor support
- Requires only the 80386 or 80376; Provides optional support for 80387 and 80387SX Numeric Coprocessors and other peripheral devices
- Works with any bus including the MULTIBUS® I and MULTIBUS II architectures
- Optional MULTIBUS II message passing support provided
- Designed for easy customization and enhancement
- Easily programmed into PROMs or EPROMs
- Comprehensive development tool support
- Supported by Intel



intel

May, 1988

Order Number: 280613-002

REAL-TIME SOFTWARE FROM THE INDUSTRY LEADER

Intel has been the industry leader in microprocessor-based real-time computing since it invented the microprocessor. No other company supplies the range of real-time solutions that we do. Since 1977, thousands of customers have used our iRMX® real-time operating systems.

Now Intel has put its real-time expertise into a 32-bit kernel that supports the 80386 microprocessor and the 80376 embedded controller. The iRMK Version 1.2 Kernel saves you the cost of designing, debugging, and maintaining your own executive for real-time systems. You can concentrate on writing your application rather than on writing a kernel.

THE QUICKEST PATH FOR A WIDE RANGE OF REAL-TIME APPLICATIONS

The iRMK Kernel's high performance and rich set of real-time services make it ideal for a wide range of real-time applications, including:

Data acquisition and analysis
Continuous process control
Discrete process control
Simulation
Medical instruments
Test instrumentation
Image processing
Automated test
Avionics and navigation
Field command control
Energy and environmental control
Radio control
Satellite communications
Terminals
Graphics work stations
Robotics
Signal processing
Laser printers
Front-end concentrators
Host communications

A RICH SET OF REAL-TIME SERVICES

The iRMK Version 1.2 Kernel provides a rich set of services for real-time applications, including:

- Task management with system calls to create, manage, and schedule tasks in a multitasking environment. The Kernel offers pre-emptive priority scheduling combined with optional time-slice (round robin) scheduling.

  The scheduling algorithm used by the iRMK Kernel allows tasks to be rescheduled in a fixed amount of time regardless of the number of tasks. Applications may contain any number of tasks.

  An application can provide optional task handlers to customize task management. These handlers can execute on task creation, task switch, task deletion, and task priority change. Task handlers can be used for a wide range of functions including saving and restoring the state of coprocessor registers on task switch, masking interrupts based on task priority, or implementing statistical and diagnostic monitors.

- Interrupt management by immediately switching control to user-written interrupt handlers when an interrupt occurs. Response to interrupts is both fast and predictable. Most of the Kernel's system calls can be executed directly from interrupt handlers.

- Time management providing single-shot alarms, repetitive alarms, and a real-time clock. Alarms can be reset.

  These time management facilities can solve a wide range of real-time programming problems. Single-shot alarms, for example, can be used to handle timeouts. If the timeout occurs, the alarm invokes a user-written handler; if the event occurs before the timeout, the application simply deletes the alarm. Other uses for the Kernel's time management facilities include polling devices with repetitive alarms, putting tasks to sleep for specified periods of time, or implementing a time-of-day clock.

- Semaphores, regions, and mailboxes for intertask synchronization and communication. Semaphores are used for intertask signalling and synchronization. Regions are special binary semaphores used to ensure mutual exclusion and prevent deadlock when tasks contend for control of system resources. A task holding a region's unit runs at the priority of the highest priority task waiting for the region's unit.

  Mailboxes are queues that can hold any number of messages and are used to exchange data between tasks. Either data or pointers can be sent using mailboxes. The Kernel allows mailbox messages to be of any length. High priority messages can be placed (jammed) at the front of the message queue to ensure that they are received before other messages queued at the mailbox.

  To ensure that high priority tasks are not blocked by lower priority tasks, the Kernel allows tasks to queue at semaphores and mailboxes in priority order. The Kernel also supports first-in, first-out task queuing.

- Memory pool manager that provides fixed and variable block allocation. Memory can be divided into any number of pools. Multiple memory pools might be created for different speed memories or for allocating different size blocks. Access to a memory pool for fixed-sized allocation is always deterministic.

  The Kernel-supplied memory manager works with flat, segmented, and paged addressing. Users can write their own memory manager to provide different memory management policies or to support virtual memory.

SUPPORT FOR MULTIPROCESSING VIA MULTIBUS® II ARCHITECTURE

The MULTIBUS II architecture is designed to optimize multiprocessor designs. This bus:

- Implements a loosely coupled architecture in which interprocessor interrupts and data are exchanged via messages transmitted as packets over the bus;
- Provides fast bus access;
- Allows interprocessor signalling at interrupt speeds from as many as 255 sources;
- Provides data transfer rates of up to 32 megabytes per second;
- Allows multiple communication sessions to occur simultaneously between processors;
- Supports up to 21 CPU boards per chassis with each board providing the processor, memory, and I/O needed for its portion of the application; and
- Provides registers—called Interconnect Space—on each board that can be used for dynamic system configuration.

Two optional modules allow iRMK Kernel applications to make full use of the MULTIBUS II architecture. The first module implements message passing allowing the application to have direct access to the message passing hardware or to use Intel's MULTIBUS II transport protocol. The second module implements interconnect space access to support dynamic system configuration.

These modules can be used to implement high performance multiprocessor designs that:

- Break a highly complex real-time application into multiple lower complexity applications distributed across multiple processors
- Distribute an application that's too CPU intensive for a single processor between several processors
- Provide redundancy
- Dedicate processors to specific tasks
- Provide interoperation with any operating system or controller board that uses Intel's MULTIBUS II transport protocol, including the iRMX™ II.3, iRMK I.2, and Intel System V/386 operating systems.

HARDWARE REQUIREMENTS AND SUPPORT

The iRMK Kernel requires only an 80386 microprocessor or an 80376 embedded controller and sufficient memory for itself and its application. Its design, however, recognizes that many systems use additional programmable peripheral devices and coprocessors. The Kernel provides optional device managers for:

- The 80387 and 80387SX Numeric Coprocessors
- The 82380 and 82370 Integrated System Peripherals
- The 8254 Programmable Interval Timer
- The 8259A Programmable Interrupt Controller

An application can supply managers for other devices and coprocessors in addition to or in replacement of the devices listed above.

The iRMK Kernel was designed to be programmed into PROM or EPROM, making it easy to use in embedded designs.

The iRMK Kernel can be used with any system bus including the MULTIBUS I and MULTIBUS II busses. The optional MULTIBUS II message passing and Interconnect Space access modules use the Message Passing Coprocessor (MPC). The Kernel provides managers to use the 82380/82370 Integrated System Peripherals or the 82258 Advanced DMA controller with the MPC for message passing.

SUPPORT FOR THE INTEL386™ AND INTEL376™ ARCHITECTURES

The iRMK Kernel provides 32-bit, protected mode 80386 and 80376 operation. By default, the Kernel and its application execute in a flat memory space of up to 4 gigabytes and in a single privilege level. Applications can add support for any mixture of additional protected mode features including:

- Any model of segmentation
- Memory paging
- Virtual memory
- Multiple privilege levels
- Call and trap gates

These protected mode features can be used to increase the reliability of the application by using the processor's hardware to:

- Protect against attempts to write beyond segment bounds (to catch, for example, situations like stack overflow or underflow)
- Allow only privileged or trusted code to access key routines and data
- Isolate bugs to single modules so that the rest of the application and the Kernel are not corrupted
- Assign access rights to code and data
- Isolate address spaces

To use these features, the application manipulates the processor's descriptor tables. Since the Kernel was designed specifically to support 80386 and 80376 applications, it provides an optional Descriptor Table manager that simplifies protected mode programming. This manager provides system calls to read and write descriptor table entries, to convert addresses from linear to physical and vice versa, and to get a segment's selector.

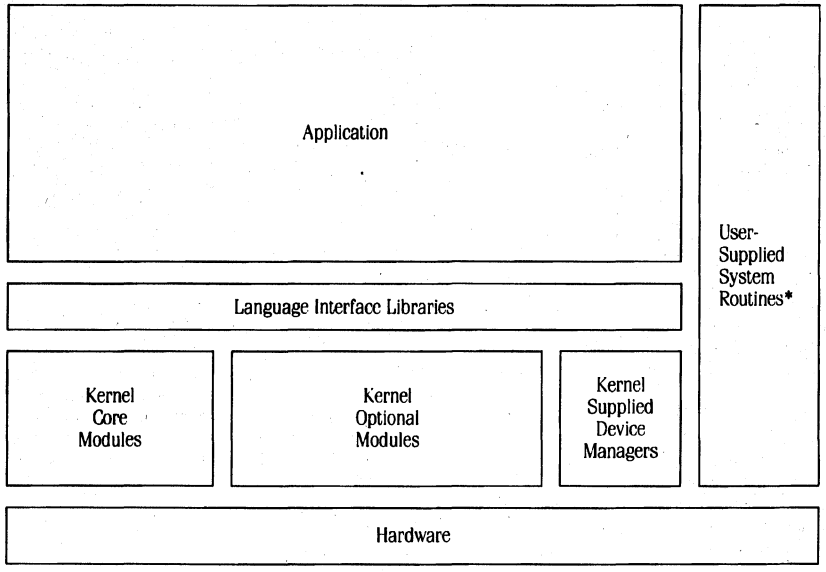


Figure 1: iRMK™ Version 1.2. Real-Time Kernel Architecture

*User-supplied system routines would include interrupt handlers, user-written device managers, and similar routines.

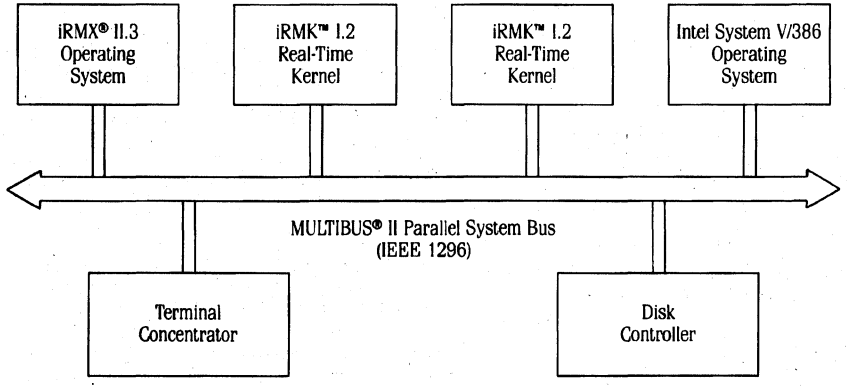


Figure 2: The optional MULTIBUS® II message passing modules give the iRMK™ 1.2 Version Kernel full multiprocessing capabilities for distributing applications among processors and interoperating with other operating systems.

A MODULAR ARCHITECTURE FOR EASY CUSTOMIZATION

The iRMK Kernel was designed for maximum flexibility so it can be customized for each application. Each major function—mailboxes, for example—was implemented as a separate module. The Kernel's modules have not been linked together and are supplied individually. You link the modules you need for your application. Any module not used does not need to be linked in, and does not increase the size of the Kernel in your application. You can also replace any optional Kernel module with one that implements specific features required by your application. For example, you might want to replace the Kernel's memory manager with one that supports virtual memory.

Table 1 lists the Kernel's modules.

Table 1: iRMK™ Version 1.2 Kernel Modules

Core Functions	Optional Modules	Optional Device Managers
• Task manager • Time manager • Interrupt manager	• Mailbox manager • Semaphore manager • Memory Pool manager • Descriptor Table manager • MULTIBUS II Message Passing • MULTIBUS II Interconnect Space Access	• 80387 & 80387SX • 82380 & 82370 • 8254 • 8259A

DEVELOPING WITH THE iRMK™ REAL-TIME KERNEL

iRMK Kernel applications can be written using any language or compiler that produces code that executes in the 80386's protected mode or on the 80376. This independence is achieved by using interface libraries. These libraries work with the idiosyncrasies of each language—for example, the ordering of parameters. The interface libraries translate the call provided by the language into a standard format expected by the Kernel. Intel provides interface libraries for our iC 386 and PL/M 386 languages. The source code for these libraries is provided so you can modify them to support other compilers.

Intel's 80386 Utilities are used to link the Kernel's modules and to locate the Kernel in memory. Applications written with a compiler that produces OMF386 object module format can be linked directly to the Kernel for the highest possible performance. Alternately, applications written in OMF386 or another object module format can access the Kernel through a call gate mechanism included with the Kernel.

Because the Kernel is supplied as unlinked object modules, applications can be developed on any system that hosts the development tools that you will use.

COMPREHENSIVE DEVELOPMENT TOOL SUPPORT

Intel provides a complete line of 80386 and 80376 development tools for writing and debugging iRMK Kernel applications. These tools include:

Software:	PL/M 386 Compiler
	iC 386 Compiler
	ASM 386 Assembler
	RLL 386 Utilities
Debuggers:	ICE™ 386 and ICE 376
	P-MON 386
	D-MON 386

These tools run on IBM* PC AT systems and compatibles running PC- or MS-DOS* 3.X. The languages and utilities also run on VAX/VMS and MicroVAX/VMS* systems. The iRMK Version 1.2 Kernel software is available on IBM PC format 5¼ inch, 360K byte diskettes.

INTEL SUPPORT, CONSULTING, AND TRAINING

With the iRMK Kernel you get the Intel386 architecture and real-time expertise of Intel's customer support engineers. We provide phone support, on- or off-site consulting, troubleshooting guides, and updates. The Kernel includes 90 days of Intel's Technical Information Phone Service (TIPS). Extended support and consulting are also available.

CONTENTS OF THE iRMK™ KERNEL DEVELOPMENT PACKAGE

The iRMK Kernel comes in a comprehensive package that includes:

- Kernel object modules
- Source for the Kernel-supplied 82380 and 82370 Integrated System Peripherals; 8259A PIC; 8254 PIT; and 80387 and 80387SX Numeric Coprocessor device managers
- Source for PL/M 386 and iC 386 interface libraries
- Source for the call gate interface
- Source for sample applications showing:
  - —Structure of Kernel applications
  - —Use of the Kernel with application written in both PL/M 386 and iC 386
  - —Compile, bind, and build sequences
  - —Sample initialization code for the 80386 microprocessor
  - —MULTIBUS II message passing
  - —Applications written to execute in a flat memory space and in a segmented memory space
- User Reference Guide
- 90 days of Customer Support

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*MS-DOS is a trademark of Microsoft Corporation.
*VAX is a registered trademark of Digital Equipment Corporation. VMS is a trademark of Digital Equipment Corporation.

iRMK™ VERSION 1.2 KERNEL SYSTEM CALLS[1]

KERNEL INITIALIZATION

KN_initialize	Initialize Kernel

OBJECT MANAGEMENT

KN_token_to_ptr	Returns a pointer to area holding object
KN_current_task	Returns a token for the current task

TASK MANAGEMENT

KN_create_task	Create a task
KN_delete_task	Delete a task
KN_suspend_task	Suspend a task
KN_resume_task	Resume a task
KN_set_priority	Change priority of a task
KN_get_priority	Return priority of a task

INTERRUPT MANAGEMENT

KN_set_interrupt	Specify interrupt handler
KN_stop_scheduling	Suspend task switching
KN_start_scheduling	Resume task switching

TIME MANAGEMENT

KN_sleep	Put calling task to sleep
KN_create_alarm	Create and start virtual alarm clock
KN_reset_alarm	Reset an existing alarm
KN_delete_alarm	Delete alarm
KN_get_time	Get time
KN_set_time	Set time
KN_tick	Notify kernel that clock tick has occurred

INTERTASK COMMUNICATION AND SYNCHRONIZATION

KN_create_semaphore	Create a semaphore
KN_delete_semaphore	Delete a semaphore
KN_send_unit	Add a unit to a semaphore
KN_receive_unit	Receive a unit from a semaphore
KN_create_mailbox	Create a mailbox
KN_delete_mailbox	Delete a mailbox
KN_send_data	Send data to a mailbox
KN_send_priority_data	Place (jam) priority message at head of message queue
KN_receive_data	Request a message from a mailbox

MEMORY MANAGEMENT

KN_create_pool	Create a memory pool
KN_delete_pool	Delete a memory pool
KN_create_area	Create a memory area from a pool
KN_delete_area	Return a memory area to a memory pool
KN_get_pool_attributes	Get a memory pool's attributes

DESCRIPTOR TABLE MANAGEMENT

KN_get_descriptor_attributes	Get a descriptor's attributes
KN_set_descriptor_attributes	Set a descriptor's attributes
KN_initialize_LDT	Initialize local descriptor table (LDT)
KN_null_descriptor	Overwrite a descriptor with the null descriptor
KN_initialize_subsystem	Allows application to be divided into multiple subsystems when application interfaces to Kernel through a call gate
KN_linear_to_ptr	Convert a linear address to a pointer
KN_ptr_to_linear	Convert a pointer to a linear address
KN_get_data_selector	Get the selector for the data segment
KN_get_code_selector	Get the selector for the code segment
KN_translate_ptr	Converts a pointer that will be based on a user-specified selector

82380, 82370, AND 8259A PIC MANAGEMENT

KN_initialize_PICs	Initialize the PICs
KN_mask_slot	Mask out interrupts on a specified slot
KN_unmask_slot	Unmask interrupts on a specified slot
KN_send_EOI	Signal the PIC that the interrupt on a specified slot has been serviced
KN_new_masks	Change interrupt masks
KN_get_slot	Return the most important active interrupt slot

82380, 82370, AND 8254 PIT MANAGEMENT

KN_initialize_PIT	Initialize a PIT
KN_start_PIT	Start PIT counting
KN_get_PIT_interval	Return PIT interval

80387 AND 80387SX NUMERIC COPROCESSOR MANAGEMENT

KN_initialize_NDP	Initialize an 80387 or 80387SX Numeric Coprocessor

MULTIBUS® II MESSAGE PASSING MANAGEMENT

KN_initialize_message_passing	Initialize the message passing module
KN_mp_working_storage_size	Compute size of work space needed for message passing
KN_send_tp	Send a transport message
KN_attach_receive_mailbox	Attach a receive mailbox
KN_cancel_tp	Cancel a solicited message or request-response transaction
KN_send_dl	Send a data link message
KN_attach_protocol_handler	Attach a protocol handler
KN_cancel_dl	Cancel a data link buffer request

MULTIBUS® II INTERCONNECT SPACE MANAGEMENT

KN_initialize_interconnect	Initialize the interconnect module
KN_get_interconnect	Get the value of an interconnect register
KN_set_interconnect	Set the value of an interconnect register
KN_local_host_ID	Get the host ID of the local host

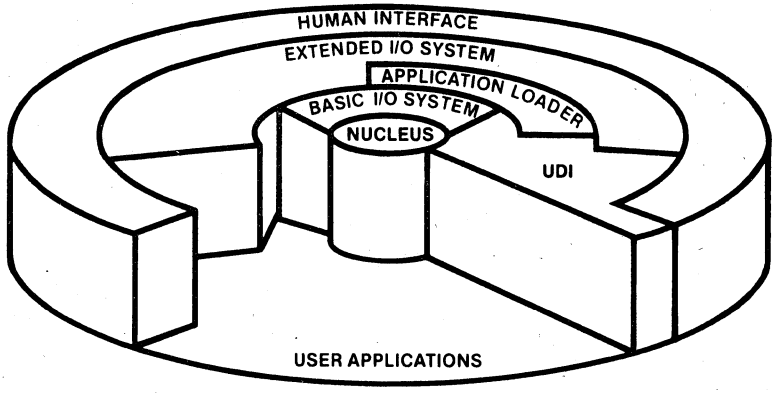
ORDERING INFORMATION

Order Code	*Product*	*Contents*
RMK	iRMK Version I.2 Development Software	iRMK Version I.2 Kernel
RMKDEVP RMKDEVC	iRMK Version I.2 Developer's Kit	iRMK Version I.2 Kernel PL/M 386 or iC 386 Compilers ASM 386 Assembler RLL 386 Utilities
SSC-430	Technical Information Phone Support	Phone support *;Comments* Magazine, Troubleshooting Guides
CONSULT/DAILY CONSULT/LT	On- or off-site consulting on iRMK I.2 Kernel or other Intel products by Intel systems engineer. Available on a daily or long term basis.	
	iRMK Real-time Kernel	Customer Training Workshop
	80386 Programming Using ASM 386	Customer Training Workshop
	80386 System Software	Customer Training Workshop
	80386 System Hardware Design	Customer Training Workshop

iRMX® I OPERATING SYSTEM

- **Real-Time Processor Management for Time-Critical 8086, 8088, 80186, 80188, and 80286/386™ (Real Address Mode) Applications**
- **On-Target System Development with Universal Development Interface (UDI)**
- **Configurable System Size and Function for Diverse Application Requirements**
- **All iRMX® I Code Can Be (P)ROM'ed to Support Totally Solid State Designs**
- **Configured Systems for the 8086, 80286, and 386 Processors in the Intel System 300 Series Microcomputers**
- **Multi-Terminal Support with Multi-User Human Interface**
- **Broad Range of Device Drivers Included for Industry Standard MULTIBUS® Peripheral Controllers**
- **Support of 8087, 80287, and 80387 Processor Extension**
- **Powerful Utilities for Interactive Configuration and Real-Time Debugging**

The iRMX I Operating System is an easy-to-use, real-time, multi-tasking and multi-programming software system designed to manage and extend the resources of iSBC® 86, iSBC 186, iSBC 188, iSBC 286, and iSBC 386 Single Board Computers, as well as other 8086, 8088, 80186, 80188, and 80286/386™ (Real Address Mode) based microcomputers. The Operating System provides a number of standard interfaces that allow iRMX I applications to take advantage of industry standard device controllers, hardware components, and a number of software packages developed by Independent Software Vendors (ISVs). Many high-performance features extend the utility of iRMX I Systems into applications such as data collection, transaction processing, and process control where immediate access to advances in VLSI technology is paramount. These systems may deliver real-time performance and explicit control over resources; yet also support applications with multiple users needing to simultaneously access terminals. The configurable layers of the System provide services ranging from interrupt management and standard device drivers for many sophisticated controllers, to data file maintenance commands provided by a comprehensive multi-user human interface. By providing access to the standard Universal Development Interface (UDI) for each user terminal, Original Equipment Manufacturers (OEMs) can pass program development and target application customization capabilities to their users.



210885-1

iRMX® VLSI Operating System

November 1988
Order Number: 210885-004

The iRMX I Operating System is a complete set of system software modules that provide the resource management functions needed by computer systems. These management functions allow Original Equipment Manufacturers (OEMs) to best use resources available in microcomputer systems while getting their products to market quickly, saving time and money. Engineers are relieved of writing complex system software and can concentrate instead on their application software.

This data sheet describes the major features of the iRMX I Operating System. The benefits provided to engineers who write application software and to users who want to take advantage of improving microcomputer price and performance are explained. The first section outlines the system resource management functions of the Operating System and describes several system calls. The second section gives a detailed overview of iRMX I features aimed at serving both the iRMX I system designer and programmer, as well as the end users of the product into which the Operating System is incorporated.

FUNCTIONAL DESCRIPTION

To take best advantage of 8086, 8088, 80186, 80188, and 80286/386 (Real Address Mode) microprocessors in applications where the computer is required to perform many functions simultaneously, the iRMX I Operating System provides a multiprogramming environment in which many independent, multi-tasking application programs may run. The flexibility of independent environments allows application programmers to separately manage each application's resources during both the development and test phases.

The resource management functions of the iRMX I System are supported by a number of configurable software layers. While many of the functions supplied by the innermost layer, the Nucleus, are required by all systems, all other functions are optional. The I/O systems, for example, may be omitted in systems having no secondary storage requirement. Each layer provides functions that encourage application programmers to use modular design techniques for quick development of easily maintainable programs.

The components of the iRMX I Operating System provide both implicit and explicit management of system resources. These resources include processor scheduling, up to one megabyte of system memory, up to 57 independent interrupt sources, all input and output devices, as well as directory and data files contained on mass storage devices and accessed by a number of independent users. Management of these system resources and methods for sharing resources between multiple processors and users is discussed in the following sections.

Process Management

To implement multi-tasking application systems, programmers require a method of managing the different processes of their application, and for allowing the processes to communicate with each other. The Nucleus layer of the iRMX I System provides a number of facilities to efficiently manage these processes, and to effectively communicate between them. These facilities are provided by system calls that manipulate data structures called tasks, jobs, regions, semaphores and mailboxes. The iRMX I System refers to these structures as 'objects".

Tasks are the basic elements of all applications built on the iRMX I Operating System. Each task is an entity capable of executing CPU instructions and issuing system calls in order to perform a function. Tasks are characterized by their register values (including those of an optional 8087, 80287, or 80387 Numeric Processor Extension), a priority between 0 and 255, and the resources associated with them.

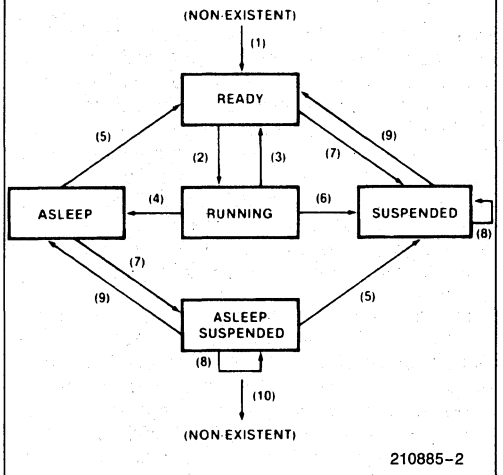
Each iRMX I task in the system is scheduled for operation by the iRMX I Nucleus. Figure 1 shows the five states in which each task may be placed, and some examples of how a task may move from one state to another. The iRMX I Nucleus ensures that each task is placed in the correct state, defined by the events in its external environment and by the task issuing system calls. Each task has a priority to indicate its relative importance and need to respond to its environment. The Nucleus guarantees that the highest priority ready-to-run task is the task that runs. The nucleus can also be configured to allow multiple tasks of the same priority to run in a round-robin, time-slice fashion.

Jobs are used to define the operating environment of a group of tasks. Jobs effectively limit the scope of an application by collecting all of its tasks and other objects into one group. Because the environment for execution of an application is defined by an iRMX I job, separate applications can be efficiently developed by separate development teams.

The iRMX I Operating System provides two primary techniques for real-time event synchronization in multi-task applications: regions and semaphores.

Regions are used to restrict access to critical sections of code and data. Once the iRMX I Operating System gives a task access to resources guarded by a region, no other tasks may make use of the resources, and the task is given protection against deletion and suspension. Regions are typically used to protect data structures from being simultaneously updated by multiple tasks.

Semaphores are used to provide mutual exclusion between tasks. They contain abstract "units" that are sent between the tasks, and can be used to implement the cooperative sharing of resources.



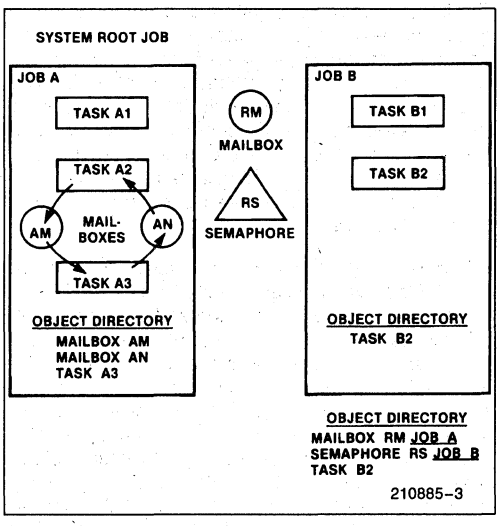
NOTES:
1. Task is created.
2. Task becomes highest priority ready task.
3. Task gets pre-empted by one with higher priority.
4. Task calls SLEEP or task waits at an exchange.
5. Task sleep period has ended, message was sent to waiting task or wait has ended.
6. Task calls SUSPEND on self.
7. Task suspended by other than self.
8. Task suspended by other than self or a resume that did not bring suspension depth to zero.
9. Task was resumed by other task.
10. Task is deleted.

Figure 1. Task State Diagram

Multi-tasking applications must communicate information and share system resources among cooperating tasks. The iRMX I Operating System assigns a unique 16-bit number, called a token, to each object created in the System. Any task in possession of this token is able to access the object. The iRMX I Nucleus allows tasks to gain access to objects, and hence system resources, at run-time with two additional mechanisms: mailboxes and object directories.

Mailboxes are used by tasks wishing to share objects with other tasks. A task may share an object by sending the object token via a mailbox. The receiving task can check to see if a token is there, or can wait at the mailbox until a token is present.

Object Directories are also used to make an object available to other tasks. An object is made public by cataloging its token and name in a directory. In this manner, any task can gain access to the object by knowing its name, and job environment that contains the directory.



Two example jobs are shown in Figure 2 to demonstrate how two tasks can share an object that was not known to the programmer at the time the tasks were developed. Both Job 'A' and Job 'B' exist within the environment of the 'Root Job' that forms the foundation of all iRMX I systems. Each job posseses a directory in which tasks may catalog the name of an object. Semaphore 'RS', for example, is accessible by all tasks in the system, because its name is cataloged in the directory of the Root Job. Mailbox "AN" can be used to transfer objects between Tasks 'A2' and 'A3' because its token is accessible in the object directory for Job 'A'.

Table 1 lists the major functions of the iRMX I Nucleus that manages system processes.

Memory Management

Each job in an iRMX I System defines the amount of the one megabyte of addressable memory to be used by its tasks. The iRMX I Operating System manages system memory and allows jobs to share this critical resource by providing another object type: segments.

Segments are contiguous pieces of memory between 16 Bytes and 64 Kbytes in length, that exist within the environment of the job in which they were created. Segments form the fundamental piece of system memory used for task stacks, data storage, system buffers, loading programs from secondary storage, passing information between tasks, etc.

The example in Figure 2 also demonstrates when information is shared between Tasks 'A2' and 'A3'; 'A2' only needs to create a segment, put the information in the memory allocated, and send it via the Mailbox 'AM' using the RQ$SEND$MESSAGE sys-

Table 1. Process Management System Calls

System Call	Function Performed
RQ$CREATE$JOB	Creates an environment for a number of tasks and other objects, as well as creating an initial task and its stack.
RQ$DELETE$JOB	Deletes a job and all the objects currently defined within its bounds. All memory used is returned to the job from which the deleted job was created.
RQ$OFFSPRING	Provides a list of all the current jobs created by the specified job.
RQ$CATALOG$OBJECT	Enters a name and token for an object into the object directory of a job.
RQ$UNCATALOG$OBJECT	Removes an object's token and its name from a job's object directory.
RQ$LOOKUP$OBJECT	Returns a token for the object with the specified name found in the object directory of the specified job.
RQGETTYPE	Returns a code for the type of object referred to by the specified token.
RQ$CREATE$MAILBOX	Creates a mailbox with queues for waiting tasks and objects with FIFO or PRIORITY discipline.
RQ$DELETE$MAILBOX	Deletes a mailbox.
RQ$SEND$MESSAGE	Sends an object to a specified mailbox. If a task is waiting, the object is passed to the appropriate task according to the queuing discipline. If no task is waiting, the object is queued at the mailbox.
RQ$RECEIVE$MESSAGE	Attempts to receive an object token from a specified mailbox. The calling task may choose to wait for a specified number of system time units if no token is available.
RQ$DISABLE$DELETION	Prevents the deletion of a specified object by increasing its disable count by one.
RQ$ENABLE$DELETION	Reduces the disable count of an object by one, and if zero, enables deletion of that object.
RQ$FORCE$DELETE	Forces the deletion of a specified object if the disable count is either 0 or 1.
RQ$CREATE$TASK	Creates a task with the specified priority and stack area.
RQ$DELETE$TASK	Deletes a task from the system, and removes it from any queues in which it may be waiting.
RQ$SUSPENDS$TASK	Suspends the operation of a task. If the task is already suspended, its suspension depth is increased by one.
RQ$RESUME$TASK	Resumes a task. If the task had been suspended multiple times, the suspension depth is reduced by one, and it remains suspended.
RQ$SLEEP	Causes a task to enter the ASLEEP state for a specified number of system time units.
RQGETTASK$TOKENS	Gets the token for the calling task or associated objects within its environment.
RQSETPRIORITY	Dynamically alters the priority of the specified task.
RQGETPRIORITY	Obtains the current priority of a specified task.
RQ$CREATE$REGION	Creates a region, with an associated queue of FIFO or PRIORITY ordering discipline.
RQ$DELETE$REGION	Deletes the specified region if it is not currently in use.
RQ$ACCEPT$CONTROL	Gains control of a region only if the region is immediately available.
RQ$RECEIVE$CONTROL	Gains control of a region. The calling task may specify the number of system time units it wishes to wait if the region is not immediately available.
RQ$SEND$CONTROL	Relinquishes control of a region.
RQ$CREATE$SEMAPHORE	Creates a semaphore.
RQ$DELETE$SEMAPHORE	Deletes a semaphore.
RQ$SEND$UNITS	Increases a semaphore counter by the specified number of units.
RQ$RECEIVE$UNITS	Attempts to gain a specified number of units from a semaphore. If the units are not immediately available, the calling task may choose to wait.

tem call (see Table 1). Task 'A3' would get the message by using the RQ$RECEIVE$MESSAGE system call. The Figure also shows how the receiving task could signal the sending task by sending an acknowledgement via the second Mailbox 'AN'.

Each job is created with both maximum and minimum limits set for its memory pool. Memory required by all objects and resources created in the job is taken from this pool. If more memory is required, a job may be allowed to borrow memory from the pool of its containing job (the job from which it was created). In this manner, initial jobs may efficiently allocate memory to jobs they subsequently create, without knowing their exact requirements.

The iRMX I Operating System supplies other memory management functions to search specific address ranges for available memory. The System performs this search at system initialization, and can be configured to ignore non-existent memory and addresses reserved for I/O devices and other application requirements.

Table 2 lists the major system calls used to manage the system memory.

Interrupt Management

Real-time systems, by their nature, must respond to asynchronous and unpredictable events quickly. The iRMX I Operating System uses interrupts and the event-driven Nucleus described earlier to give real-time response to events. Use of a pre-emptive scheduling technique ensures that the servicing of high priority events always takes precedence over other system activites.

The iRMX I Operating system gives applications the flexibility to optimize either interrupt response time or interrupt response capability by providing two tiers of Interrupt Management. These two distinct tiers are managed by Interrupt Handlers and Interrupt Tasks.

Interrupt Handlers are the first tier of interrupt service. For small simple functions, interrupt handlers are often the most efficient means of responding to an event. They provide faster response than interrupt tasks, but must be kept simple since interrupts (except the 8086, 8088, 80186, 80188, 80286, and 386™ processors non-maskable interrupts) are masked during their execution. When extended service is required, interrupt handlers "signal" a waiting interrupt task that, in turn, performs more complicated functions.

Interrupt Tasks are distinct tasks whose priority is associated with a hardware interrupt level. They are permitted to make an iRMX I system call. While an interrupt task is servicing an interrupt, interrupts of lower priority are not allowed to pre-empt the system.

Table 3 shows the iRMX I System Calls provided to manage interrupts.

Table 2. Memory Management System Calls

System Call	Function Performed
RQ$CREATE$SEGMENT	Dynamically allocates a memory segment of the specified size.
RQ$DELETE$SEGMENT	Deletes the specified segment by deallocating the memory.
RQGETPOOL$ATTRIBUTES	Returns attributes such as the minimum and maximum, as well as current size of the memory in the environment of the calling task's job.
RQGETSIZE	Returns the size (in bytes) of a segment.
RQSETPOOL$MIN	Dynamically changes the minimum memory requirements of the job environment containing the calling task.

Table. 3. Interrupt Management System Calls

System Call	Function Performed
RQSETINTERRUPT	Assigns an interrupt handler and, if desired, an interrupt task to the specified interrupt level. Usually the calling task becomes the interrupt task.
RQ$RESET$INTERRUPT	Disables an interrupt level, and cancels the assignment of the interrupt handler for that level. If an interrupt task was assigned, it is deleted.
RQGETLEVEL	Returns the number of the highest priority interrupt level currently being processed.
RQ$SIGNAL$INTERRUPT	Used by an interrupt handler to signal the associated interrupt task that an interrupt has occurred.
RQ$WAIT$INTERRUPT	Used by an interrupt task to SLEEP until the associated interrupt handler signals the occurrence of an interrupt.
RQ$EXIT$INTERRUPT	Used by an interrupt handler to relinquish control of the System.
RQ$ENABLE	Enables the hardware to accept interrupts from a specified level.
RQ$DISABLE	Disables the hardware from accepting interrupts at or below a specified level.

INTERRUPT MANAGEMENT EXAMPLE

Figure 3 illustrates how the iRMX I Interrupt System may be used to output strings of characters to a printer. In the example, a mailbox named 'PRINT' is used by all tasks in the system to queue messages to be printed. Application tasks put the characters in segments that are transmitted to the printer interrupt task via the PRINT Mailbox. Once printing is complete, the same interrupt task passes the messages on to another application via the FINISHED Mailbox so that an operator message can be displayed.

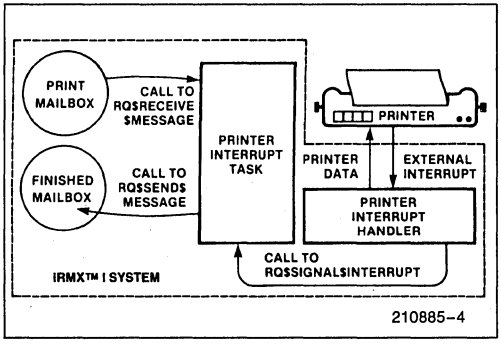


Figure 3. Interrupt Management Example

Basic I/O System

The Basic I/O System (BIOS) provides the direct access to I/O devices needed by real-time applications. The BIOS allows I/O functions to overlap other system functions. In this manner, application tasks make asynchronous calls to the iRMX I BIOS, and proceed to perform other activities. When the I/O request must be completed before an application can continue, the task waits at a mailbox for the result of the operation. Some system calls provided by the BIOS are listed in Table 4.

The Basic I/O System communicates with peripheral devices through device drivers. These device drivers provide the System with four basic functions needed to control and communicate with devices: Initialize I/O, Finish I/O, Queue I/O, and Cancel I/O. Using the device driver interface, users of non-standard devices may write custom drivers compatible with the I/O System.

The iRMX I Operating System includes a number of device drivers to allow applications to use standard USART serial communications devices, multiple CRTs and keyboards, bubble memories, diskettes, disks, a Centronics-type parallel printer, and many of Intel's iSBC and iSBX™ device controllers (see Table 8). If an application requires use of a non-standard device, users need only write a device driver to be included with the BIOS, and access it as if it were part of the standard system. For most common random-access devices, this job is further simplified by using standard routines provided with the System. Use of this technique ensures that applications can remain device independent.

Table 4. Key BIOS I/O Management System Calls

System Calls	Function Performed
RQAATTACH$FILE	Creates a Connection to an existing file.
RQACHANGE$ACCESS	Changes the types of accesses permitted to the specified user(s) for a specific file.
RQACLOSE	Closes the Connection to the specified file so that it may be used again, or so that the type of access may be changed.
RQACREATE$DIRECTORY	Creates a Named File used to store the names and locations of other Named Files.
RQACREATE$FILE	Creates a data file with the specified access rights.
RQADELETE$CONNECTION	Deletes the Connection to the specified file.
RQAGET$FILE$STATUS	Returns the current status of a specified file.
RQAOPEN	Opens a file for either read, write, or update access.
RQAREAD	Reads a number of bytes from the current position in a specified file.
RQASEEK	Moves the current data pointer of a Named or Physical file.
RQAWRITE	Writes a number of bytes at the current position in a file.
RQ$WAIT$IO	Synchronizes a task with the I/O System by causing it to wait for I/O operation results.

Multi-Terminal Support

The iRMX I Terminal Support provides line editing and terminal control capabilities. The Terminal Support communicates with devices through simple drivers that do only character I/O functions. Dynamic terminal reconfiguration is provided so that attributes such as terminal type and line speed may be changed without modifying the application or the Operating System. Dynamic configuration may be typed in, generated programmatically or stored in a file and copied to a terminal I/O connection.

The iRMX I Terminal Support provides automatic translation of control characters to specific control sequences for each terminal. This translation enables applications using standard control characters to function with non-standard terminals. The translation requirements for each terminal can be stored in terminal description files and copied to a connection, as described above.

Peripheral Device Drivers

Each device driver can be used to interface to a number of separate and, in some cases, different devices. The iSBC 215G Device Driver, supplied with the system, is capable of supporting the iSBC 215G Winchester Disk Controller, the iSBC 220 SMD Disk Controller, and the iSBX 218A Flexible Disk Controller (when mounted on an iSBC 215G board). Each device controller may, in turn, control a number of separate device units. In addition, each driver may control a number of like device controllers. This capability allows the use of large storage systems with a minimum of I/O system code to write or maintain.

Extended I/O System

The iRMX I Extended I/O System (EIOS) adds a number of I/O management capabilities to simplify access to files. Whereas the BIOS provides users with the basic system calls needed for direct management of I/O resources, many users prefer to have the system perform all the buffering and synchronization of I/O requests automatically. The EIOS allows users to access I/O devices without having to write procedures for buffering data, or to specify particular devices with constant device names.

By performing device buffering automatically, the iRMX I EIOS optimizes accesses to disks and other devices. Often, when an application task asks the System to READ a portion of a file, the System is able to respond immediately with the data it has read in advance of the request. Similarly, the EIOS will not delay a task for writing data to a device unless it is specifically told to, or if its output buffers are filled.

Logical file and device names are provided by the EIOS to give applications complete file and device independence. Applications may send data to the 'line printer' (:LP:) without needing to know which specific device will be used as the printer. This logical name may, in fact, not be a printer at all, but it could be a disk file that is later scheduled for printing.

The EIOS uses the functions provided by the BIOS to synchronize individual I/O requests with results returned by device drivers. Most EIOS system calls are similar to the BIOS calls, except that they appear to suspend the operation of the calling task until the I/O requests are completed.

File Management

The iRMX I Operating System provides three distinct types of files to ensure efficient management of both program and data files: Named Files, Physical Files, and Stream Files. Each file type provides access to I/O devices through the standard device drivers mentioned earlier. The same device driver is used to access physical and named files for a given device.

NAMED FILES

Named files allow users to access information on secondary storage by referring to a file with its ASCII name. The names of files stored on a device are stored in special files called directories in a hierarchical file structure.

The iRMX I BIOS uses an efficient format for writing the directory and data information into secondary storage. This structure enables the system to directly access any byte in a file, often without having to do additional I/O to access space allocation information. The maximum size of an individual file is 4.3 billion bytes.

EASE OF ACCESS

The hierarchical file structure is provided to isolate and organize collections of named files. To give operators fast and simple access to any level within the file tree, an ATTACHFILE command is provided. This command allows operators to create a logical name to a point in the tree so that a long sequence of characters need not be typed each time a file is referred to.

ACCESS PROTECTION

Access to each Named File is protected by the rights assigned to each user by the owner of the file. Rights to read, append, update, and delete may be

selectively granted to other users of the system. In general, users of Named Files are classified into one of two categories: User and World. Users are used when different programmers and programs need to share information stored in a file. The World classification is used when rights are to be granted to all who can use the system.

PHYSICAL FILES

Physical Files allow more direct device access than Named Files. Each Physical File occupies an entire device, treated as a single stream of individually accessible bytes. No access control is provided for Physical Files as they are typically used for such applications as driving a printing device, translating from one device format to another, driving a paper tape device, real-time data acquisition, and controlling analog mechanisms.

STREAM FILES

Stream Files provide applications with a method of using iRMX I file management methods for data that does not need to go into secondary storage. Stream Files act as direct channels, through system memory, from one task to another. These channels are very useful to programs, for example, wishing to preserve file and device independence allowing data sent to a printer one time, to a disk file another time, and to another program on a different occasion.

BOOTSTRAP AND APPLICATION LOADERS

Two utilities are supplied with the System to load programs and data into system memory from secondary storage devices:

The iRMX I Bootstrap is typically used to load the initial system from the system disk into memory, and begin its execution. Error reporting and debug switch features have been added to the Bootstrap Loader. When the Bootstrap Loader detects errors such as: "File Does Not Exist" or "Device Not Ready", an error message is reported back to the user. The debug switch will cause the Bootstrap Loader to load the system but not begin its execution. Instead the Bootstrap Loader will pass control to the monitor at the first instruction to be executed by the system.

The Application Loader is typically used by application programs already running in the system to load additional programs and data from any secondary storage device. The Human Interface layer, for example, uses the Application Loader to load the nonresident Human Interface Commands. The Application Loader is capable of loading both relocatable and absolute code as well as program overlays.

Human Interface

The flexibility of the interface between computer controlled machines and their users often determines the usability and ultimate success of the machines. Table 11 lists iRMX I Human Interface functions giving users and applications simple access to the file and system management capabilities described earlier. The process, interrupt, and memory management functions described earlier, are performed automatically for Human Interface users.

MULTI-USER ACCESS

Using the multi-terminal support provided by the BIOS, the iRMX I Human Interface can support several simultaneous users. The real-time nature of the system is maintained by providing a priority for each user, and using the event-driven iRMX I Nucleus to schedule tasks. High-performance interrupt response is guaranteed even while users interact with various application packages. For example, multi-terminal support allows one person to be using the iRMX I Editor, while another compiles a FORTRAN 86 or PASCAL 86 program, while several others load and access applications.

Each terminal attached to the iRMX I multi-user Human Interface is automatically associated with a user, a memory pool, and an initial program to run when the terminal is connected. This association is made using a file that may be changed at any time. Changes are effective the next time the system is initialized.

The initial program specified for each terminal can be a special application program, a custom Human Interface, or the standard iRMX I Command Line Interpreter (CLI).

Specifying an application program as a terminal's initial program makes the interface between operators and the computer system much simpler. Each operator need only be aware of the function of a particular application.

Specifying the standard iRMX I Human Interface CLI as the initial program enables users of the terminals to access all iRMX I functions. This CLI makes it easy to manage iRMX I files, load and execute Intel-supplied and custom programs, and submit command files for execution.

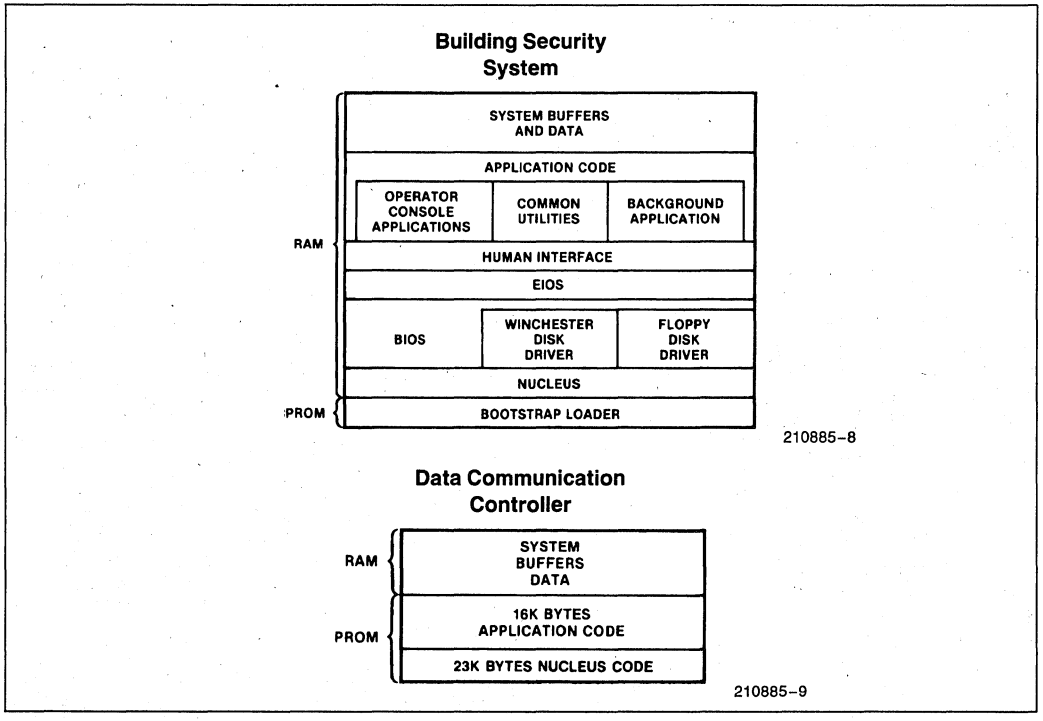


Figure 4. Typical iRMX® I Configurations

FEATURE OVERVIEW

The iRMX I Operating System is well suited to serve the demanding needs of real-time applications executing on complex microprocessor systems. The iRMX I System also provides many tools and featues needed by real-time system developers and programmers. The following sections describe features useful in both the development and execution environments. The description of each feature outlines the advantages given to hardware and software engineers concerned with overall system cost, expandability with custom and industry standard options, and long-term maintenance of iRMX I-based systems. The development environment features also describe the ease with which the iRMX I Operating System can be incorporated into overall system designs.

Execution Environment Features

REAL-TIME PERFORMANCE

The iRMX I Operating System is designed to offer the high performance, multi-tasking functions required by real-time systems. Designers can make use of VLSI devices such as the 8087, 80287 or 80387 Numeric Processor Extension.

Many real-time systems require high performance operation. To meet this requirement, all of iRMX I can be put into high-speed P(ROM). This approach eliminates the possibility of disk access times slowing down performance, while allowing system designers to take advantage of high performance memory devices.

CONFIGURABILITY

The iRMX I Operating system is configurable by system layer, and by system call within each layer. In addition all the I/O port addresses used by the System are configurable by the user. This flexibility gives designers the freedom to choose configurations of hardware and software that best suit their size and functional requirements. Two example configurations are shown in Figure 4.

Most configuration options are selected during system design stages. Others may be selected during system operation. For example, the amount of memory devoted to queues within a Mailbox can be specified at the time the Mailbox is created. Devoting more memory to the Mailbox allows more messages to be transmitted to other tasks without having to degrade system performance to allocate additional memory dynamically.

The chart shown in Table 6 indicates the actual memory size required to support these different configurations of the iRMX I System. Systems requiring only Nucleus level functions may require no more than 13 Kbytes for the Operating System. Other applications, needing I/O managment functions, may select portions of additional layers that fit their needs and size constraints.

This configurability also applies to the Terminal Handler, Dynamic Debugger, and System Debugger. The Terminal Handler provides a serial terminal interface in a system that otherwise doesn't need an I/O system. Either one of the debuggers need to be included only as debugging tools (usually only during system development).

MULTI-USER ACCESS

Many real-time systems must provide a variety of users access to system control functions and collected data. The iRMX I System provides easy-to-use support for applications to access multiple terminals. It also enables multiple and different users to access different applications concurrently.

Figure 5 illustrates a typical iRMX I application simultaneously supporting multi-terminal data collection and real-time environments. Shown is a group of terminals used by machinists on a shop floor to communicate with a job management program, a building security system that constantly monitors energy usage requirements, a system operator console capable of accessing all system functions, and a group of terminals in the Production Engineering department used to monitor job costs while developing new device control specifications instructions. The iSBC 544A Intelligent Terminal Interface supports multiple user terminals without degrading system performance to handle character I/O.

EXTENDABILITY

The iRMX I Operating System provides three means of extensions. This extendability is essential for support of OEM and volume end user value added features. This ability is provided by user-defined op-

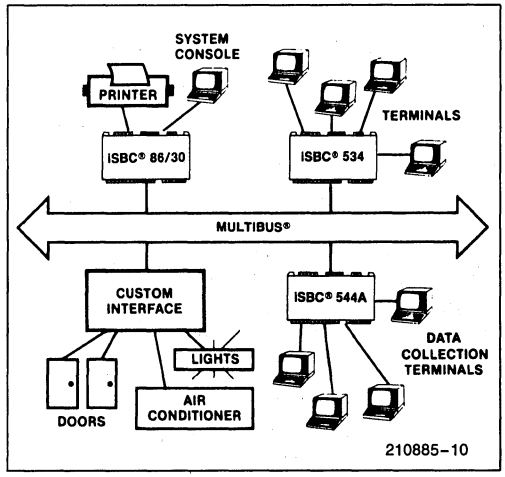


Figure 5. Multi-Terminal and Multi-User Real-Time System

Table 6. iRMX™ 86 Configuration Size Chart

System Layer	Min. ROMable Size	Max. Size	Data Size
Bootstrap Loader	1K	1.5K	6K*
Nucleus	10.5K	24K	2K
BIOS	26K	78K	1K
Application Loader	4K	10K	2K
EIOS	10.5K	12.5K	1K
Human Interface	22K	22K	15K
UDI	8K	8K	0
Terminal Handler	3K	3K	0.3K
System Debugger	20K	20K	1K
Dynamic Debugger	28.5K	28.5K	1K
Human Interface Commands			116K
Interactive Configuration Utility			308K

*Usable by System after bootloading.

Table 7. User Extension System Calls

System Call	Function Performed
RQ$CREATE$COMPOSITE	Creates a custom object built of previously defined objects.
RQ$DELETE$COMPOSITE	Deletes the custom object, but not the various objects from which it was built.
RQ$INSPECT$COMPOSITE	Returns a list of Token Identifiers for the component objects from which the specified composite object is built.
RQ$ALTER$COMPOSITE	Replaces a component object of a composite object.
RQ$CREATE$EXTENSION	Creates a new type of object and assigns a mailbox used for collecting these objects when they are deleted.
RQ$DELETE$EXTENSION	Deletes an extension definition.

erating system calls, user-defined objects (similar to Jobs, Tasks, etc.), and the ability to add functions later in the product life cycle. The modular, layered structure of the System easily facilitates later additions to iRMX I applications. User-defined objects are supported by the functions listed in Table 7.

Using standard iRMX I system calls, users may define custom objects, enabling applications to easily manipulate commonly used structures as if they were part of the original operating system.

EXCEPTION HANDLING

The System includes predefined exception handlers for typical I/O and parameter error conditions. The errors handling mechanism is both configurable and extendable.

SUPPORT OF STANDARDS

The iRMX I Operating System supports the many hardware and software standards needed by most application systems to ensure that commonly available hardware and software packages may be interfaced with a minimum of cost and effort. The iRMX I System supports the iSBC family of products built on the Intel MULTIBUS I (IEEE Standard 796), and a number of standard software interfaces such as the UDI and the common device driver interface (See Figure 6). The procedural interfaces of the UDI are listed in Table 9.

The Operating System includes support for the 8087 Numeric Data Processor and equivalent instructions and registers in the 80287 and 80387 Numeric Data

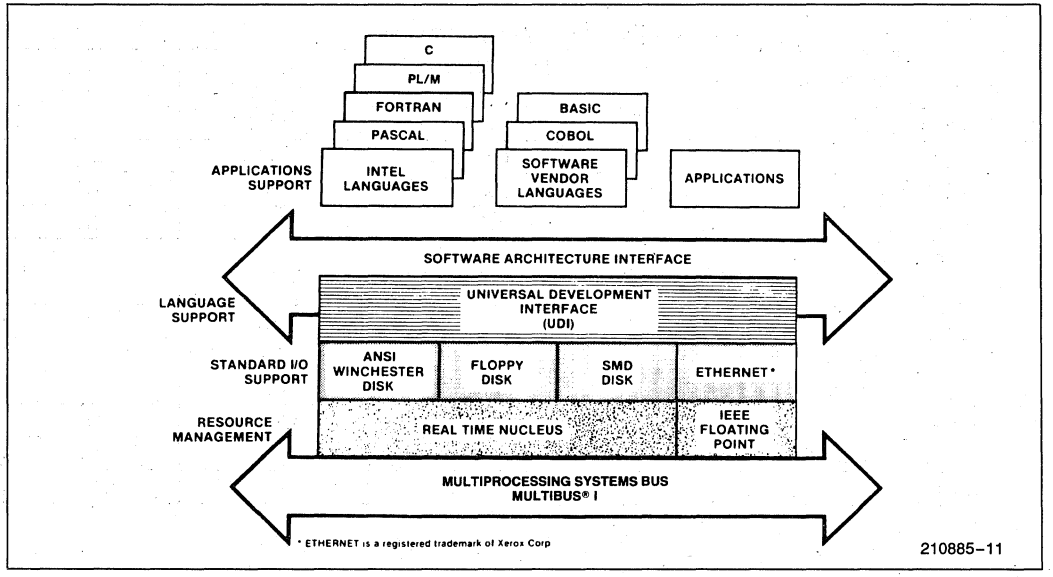


Figure 6. iRMX® I Standard Interfaces

Processors. Standards such as an Ethernet communication interface are supported by optional software packages available to run on the iRMX I System.

SPECTRUM OF CPU PERFORMANCE

The iRMX I Operating System supports a broad range of Intel processors. In addition to support for 8086, 8088, 80186 and 80188-based systems, the iRMX I system has been enhanced to support 80286/386, (16-bit, Real Address Mode)-based Systems. This new support enables the user to take advantage of the faster speed and higher performance of Intel's 80286 and 386 based microprocessors such as the iSBC 286/12 and iSBC 386/21 single board computers. By choosing the appropriate CPU, designers can choose from a wide range of performance options, without having to change application software.

COMPONENT LEVEL SUPPORT

The iRMX I System may be tailored to support specific hardware configurations. In addition to system memory, only an 8086, 8088, 80186, 80188, 80286, or 386 microprocessor, an 8259A Programmable Interrupt Controller (PIC), and either an 8253, 8254, or 82530 Programmable Interval Timer (PIT) are required as follows:

- 8086 and 8088 systems need either:
  — 8253/4 PIT and 8259A PIC (master) or
  — 80130 firmware (PIC is master)
- 80186 and 80188 systems where 186 PIC is slave, needs either:
  — 8253/4 PIT and 8259A PIC (master) or
  — 80130 firmware (PIC is master)

  where 186 PIC is master:

  — Use 186 PIT for the system clock; no external PIT is needed
  — Can use either
  186 PIC (master) only or
  8259A/80130 PIC (slave)
- 80286 systems need
  — 8253/4 PIT and 8259A PIC

For systems requiring extended mathematics capability, an 8087, 80287, or 80387 Numeric Data Processor may be added to perform these functions up to 100 times faster than equivalent software. For applications servicing more than 8 interrupt sources, additional 8259A's may be configured as slave controllers.

BOARD LEVEL SUPPORT

The iRMX I Operating System includes device drivers to support a broad range of MULTIBUS I device controllers. The particular boards and types of devices supported are listed in Table 8. The device controllers all adhere to industry standard electrical and functional interfaces.

In addition to the on-CPU board terminal drivers, the iRMX I BIOS includes two iSBC board-level device drivers to support multiple terminal interfaces:

The iSBC 544A Intelligent Four-Channel Terminal Interface Device Driver provides support for multiple controllers each supporting up to four standard RS232 terminals. The iSBC 544A driver takes advantage of an on-board processor to greatly reduce the system processor time required for terminal I/O by locally managing input and output buffers. The iSBC 544A firmware provided with the operating system can offload the system CPU by as much as 75% when doing character outputting.

The iSBC 534 Four-Channel USART Controller Device Driver also provides support for multiple controller boards each supporting up to four standard RS232 terminals.

The RAM disk feature in iRMX I makes a portion of the memory address space look like a disk drive to the I/O system.

Table 8. Supported Devices

Function	Module/Device
Single Board Computer (Note 1)	iSBC® 86/C38, 86/05A, 86/12A, 86/30, 86/35, 186/03A, 186/51, 188/56, 286/10A, 286/12, 386/21, 386/31
Peripheral Controller	iSBC 186/03A SCSI, 208, 214, 215G, 220, 221, iSBX™ 217C, 218A
Terminal Controller/ Host Comm.	iSBC 188/56,534, 544A, 548, iSBX 351, 354
Network Controller	iSBC 552A, 186/51
Graphics	iSBX 279
Microprocessor (Note 1)	8086, 8088, 80186, 80188, 80286, 386
Math Coprocessor (Note 1)	8087, 80287, 80387
Serial Port	8251A, 8274, 82530
Interrupt Controller	8259A, 80130, 80186
Timer	8253, 8254, 80186
Parallel Port/ Line Printer	8255, iSBX 350
RAM Disk	SRAM, DRAM

NOTE:
1. Supports 16-bit, real address mode, 8086/8087 instruction set, functions and registers.

Development Environment Features

The iRMX I Operating System supports the efficient utilization of programming time by providing important tools for program development. Some of the tools necessary to develop and debug real-time systems are included with the Operating System. Others, such as language compilers, are available from Intel and from leading Independent Software Vendors.

LANGUAGES

The iRMX I Operating System supports 31 standard system calls known as the Universal Development Interface (UDI). Figure 6 shows the iRMX I standard interfaces to many compilers and language translators, including Intel's 8086 Macro Assembler and the Pascal 86, PL/M 86, FORTRAN 86 and C86 compilers.

Table 9. UDI System Calls

System Call	Function Performed
MEMORY MANAGEMENT	
DQ$ALLOCATE	Creates a Segment of a specified size.
DQ$FREE	Returns the specified segment to the System.
DQGETSIZE*	Returns the size of the specified Segment.
DQ$RESERVE$IO$MEMORY*	Reserves memory to OPEN and ATTACH files.
FILE MANAGEMENT	
DQ$ATTACH	Creates a Connection to a specified file.
DQ$CHANGE$ACCESS*	Changes the user access rights associated with a file or directory.
DQ$CHANGE$EXTENSION	Changes the extension of a file name in memory.
DQ$CLOSE	Closes the specified file Connection.
DQ$CREATE	Creates a Named File.
DQ$DELETE	Deletes a Named File.
DQ$DETACH	Closes a Named File and deletes its Connection.
DQ$OPEN	Opens a file for a particular type of access.
DQGETCONNECTION$STATUS*	Returns the current status of the specified file Connection.
DQ$FILES$INFO*	Returns data about a file Connection.
DQ$READ	Reads the next sequence of bytes from a file.
DQ$RENAME*	Renames the specified Name File.
DQ$SEEK	Moves the position pointer of a file.
DQ$TRUNCATE	Truncates a file.
DQ$WRITE	Writes a sequence of bytes to a file.
PROCESS MANAGEMENT	
DQ$EXIT	Exits from the current application job.
DQ$OVERLAY*	Causes the specified overlay to be loaded.
DQ$SPECIAL	Performs special I/O related functions on terminals with special control features.
DQ$TRAP$CC	Capture control when CNTRL/C is type.
EXCEPTION HANDLING	
DQGETEXCEPTION$HANDLER	Returns a pointer to the program currently being used to process errors.
DQ$DECODE$EXCEPTION	Returns a short description of the specified error code.
DQ$TRAP$EXCEPTION	Identifies a custom exception processing program for a particular type of error.
APPLICATION ASSISTANCE	
DQ$DECODE$TIME	Returns system time and date in binary and ASCII character format.
DQGETARGUMENT*	Returns the next argument from the character string used to invoke the application program.
DQGETSYSTEM$ID*	Returns the name of the underlying operating system supporting the UDI.
DQGETTIME*	Returns the current time of day as kept by the underlying operating system.
DQ$SWITCH$BUFFER	Selects a new buffer from which to process commands.

*Calls available only through the UDI.

Also included are other Intel development tools, language translators and utilities available from other vendors. The full set of UDI calls (which includes the URI system calls) is required to run a compiler.

These standard software interfaces (the UDI) ensure that users of the iRMX I Operating System may transport their applications to future releases of the iRMX I Operating System and other Intel and independent vendor software products. The calls available in the UDI are shown in Table 9.

The high performance of the iRMX I Operating System enhances the throughput of compilers and other development utilities.

TOOLS

Certain tools are necessary for the development of microcomputer applications. The iRMX I Human Interface includes many of these tools an non-resident commands. They can be included on the system disk of a application system, and brought into memory when needed to perform functions as listed in Table 10.

Table 10. Major Human Interface Utilities

Command	Function
BACKUP	Copy directories and files from one device to another.
COPY	Copy one or more files to one or more destination files.
CREATEDIR	Create a directory file to store the names of other files.
DIR	List the names, sizes, owners, etc. of the files contained in a directory.
ATTACHFILE	Give a logical name to a specified location in a file directory tree.
PERMIT	Grant or rescind user access to a file.
RENAME	Change the name of a file.
SUBMIT	Start the processing of a series of commands stored in a file.
SUPER	Change operator's ID to that of the System Manager with global access rights and privileges.
TIME	Set the system time-of-day clock.
VERIFY	Verify the structure of an iRMX I Named File volume, and check for possible disk data errors.

INTERACTIVE CONFIGURATION UTILITY

The iRMX I Operating System is designed to provide OEMs the ability to configure for specific system hardware and software requirements. The Interactive Configuration Utility (ICU) builds iRMX I configurations by asking appropriate questions and making reasonable assumptions. It runs on either an Intellec® Series IV development system or iRMX I development system that includes a hard disk and the UDI. Table 11 lists the hardware and support software requirements of different iRMX I development system environments.

Table 11. iRMX® Development Environment

Intellec Series IV: ASM 86 Assembler and Utilities PL/M 86 Compiler One hard disk and one diskette drive
iRMX I Development System: ASM 86 Assembler and Utilities PL/M 86 Compiler iSDM System Debug Monitor 640K Bytes of RAM 5M Byte On-Line Storage and one double-density diskette drive
SYSTEM 86/300, 286/300, or 386/300 Series: Microcomputer System Basic configuration

Figure 7 shows one of the many screen displayed during the process of defining a configuration. It shows the abbreviations for each choice on the left, a more complete description with the range of possible answers in the center, and the current (sometimes default) choice on the right. The bottom of the screen shows three changes made by the operator (lower case lettering), and a request for help on the Exception Mode question. In response to a request for help, the ICU displays an additional screen outlining possible choices and some overall system effects.

The ICU requests only information required as a result of previous choices. For example, if no Extended I/O System functions are required, the ICU will not ask any further questions about the EIOS. Once a configuration session is complete, the operator may save all the information in a file. Later when small changes are necessary, this file can be modified. A completely new session is not required.

REAL-TIME DEBUGGING TOOLS

The iRMX I Operating System supports two distinct debugging environments: Static and Dynamic. While the iRMX I Operating System does support a multi-user Human Interface, these real-time debugging aids are usually most useful in a single-user environment where modifications made to the system cannot affect other users.

System Debugger

The static debugging aid is the iRMX I System Debugger. This debugger is an extension of the iSDM System Debug Monitor. The System Debugger provides static debugging facilities when the system hangs or crashes, when the Nucleus is inadvertently overwritten or destroyed, or when synchronization requirements prevent the debugging of certain tasks. The System Debugger stops the system and allows you to examine the state of the system at that instant, and allows you to:

— Identify and interpret iRMX I system calls.

— Display information about iRMX I objects.

— Examine a task's stack to determine system call history.

iRMX® I Dynamic Debugger

The iRMX I Dynamic Debugger runs as part of an iRMX I application. It may be used at any time during program development, or may be integrated into an OEM system to aid in the discovery of latent errors. The Dynamic Debugger can be used to search for errors in any task, even while the other tasks in the system are running. The iRMX I Dynamic Debugger communicates with the developer via a terminal handler that supports full line editing.

PARAMETER VALIDATION

Some iRMX I System Calls require parameters that may change during the course of developing iRMX I applications. The iRMX I Operating System includes an optional set of routines to validate these parameters to ensure that correct numeric values are used and that correct object types are used where the System expects to manipulate an object. For systems based only on the iRMX I Nucleus, these routines may be removed to improve the performance and code size of the System once the development phase is completed.

START-UP SYSTEMS

Three ready-to-run start-up systems are included in the iRMX I Operating System package for 8086, 80286, and 386-based MULTIBUS I systems. These iRMX I start-up systems are fully configured, iRMX I Operating Systems ready to be loaded into memory by the Bootstrap Loader. The start-up systems are configured to include all of the system calls for each layer and most of the features provided by iRMX I software. iRMX I start-up systems include UDI support so that users may run languages such as PL/M-86, Pascal, FORTRAN, and software packages from independent vendors.

The start-up system for the 8086 processor is configured for Intel SYSTEM 86/300 Series microcomputers with a minimum of 384K bytes of RAM. The following devices are supported.

- iSBC 215G/iSBX 218 or iSBC 215G/iSBX 218A or iSBC 214
- Line Printer
- 8251A Terminal Driver
- iSBC 544A, Terminal Driver

```
Nucleus
(ASC)    All Sys Calls [Yes/No]                          Yes
(PV)     Parameter Validation [Yes/No]                   Yes
(ROD)    Root Object Directory Size [0-0FF0h]            0014H
(MTS)    Minimum Transfer Size [0-0FFFFH]                0040H
(DEH)    Default Exception Handler [Yes/No/Deb/Use]      Yes
(NEH)    Name of Ex Handler Object Module [1-32 chs]
(EM)     Exception Mode [Never/Program/Environ/All]      Never
(NR)     Nucleus in ROM [Yes/No]                         No

Enter Changes [Abbreviations ?/ = new-value]:  ASC = N
:pv = no
:rod = 48
:em?
```

Figure 7. ICU Screen for iRMX® I Nucleus

The start-up system for the 80286 processor is configured for Intel SYSTEM 286/300 Series microcomputers with a minimum of 512 Kbytes and a maximum of 896 Kbytes of RAM. The following devices are supported.

- iSBC 208
- iSBC 215G/iSBX 218 or iSBC 215G/iSBX 218A
- Line Printer for iSBC 286/1X
- 8274 Terminal Driver
- iSBC 544A Terminal Driver

A start-up system is also provided for 386-based designs.

The systems will run without hardware or software configuration changes and can be reconfigured on a standard system with at least 512 Kbytes of RAM. Definition files are also included for iSBC 186/03A, 186/51 and 188/56 configurations.

This start-up system may be used to run the ICU (if a Winchester disk is attached to the system) to develop custom configurations such as those pictured in Figure 5. As shipped, the Human Interface supports a single user terminal. However, the Start-up System terminal configuration file may be altered easily to support from two to five users.

SPECIFICATIONS

Supported Software Products

R86ASM86	8086 Assembler and Utilities
R86C86	C 86 Compiler
R86PAS86	PASCAL 86 Compiler
R86FOR86	FORTRAN 86 Compiler
R86PLM86	PL/M 86 Compiler
iRMX 864	AEDIT Screen-oriented Editor

Supported Hardware Products

COMPONENTS

8086 and 8088 Microprocessors

80186 and 80188 Microprocessors

80286/386 Microprocessors (16-bit, Real Address Mode Only)

8087 Numeric Data Processor Extension

80287/387 Numeric Data Processor Extension (8087 Functions and Registers)

8253 and 8254 Programmable Interval Timers

8259A Programmable Interrupt Controller

8251A USART Terminal Controller

8255 Programmable Parallel Interface

8274 Terminal Controller

82530 Serial Communications Controller

iSBC® MULTIBUS BOARD AND SYSTEM PRODUCTS

iSBC 86/C38, 86/12A, 80/05A, 86/30, 86/35, and 88/40A Single Board Computers

iSBC 186/03A Single Board Computer

iSBC 186/51 Ethernet Controller

iSBC 188/56 Communications Controller

iSBC 286/10A and 286/12 Single Board Computers (Real Address Mode only)

iSBC 386/21 and 386/31 (16-bit, Real Address Mode only)

iSBC 208 Diskette Controller

iSBC 214 and 215(G) Winchester Disk Controllers

iSBX 218A Flexible Diskette Multi-Module Controller

iSBC 220 SMD Disk Hard Controller

iSBC 221 Disk Controller

iSBC 534 4-Channel Terminal Interface

iSBC 544A Intelligent 4-Channel Terminal Interface and Controller

iSBC 548 Intelligent 8-Channel Terminal Controller

iSBC 552A Ethernet Controller

iSBX 350 Parallel Port (Centronics-type Printer Interface)

iSBX 351 and 354 Serial Communications Port

iSBX 279 Graphics Subsystem

SYSTEM 86/300 Family

SYSTEM 286/300 Family

SYSTEM 386/300 Family

USER MANUALS

The iRMX I Operating System is provided with one five volume set of reference manuals:

Volume I	iRMX I INSTALLATION AND PROGRAMMER'S GUIDES
Volume II	iRMX I OPERATING SYSTEM USER GUIDES
Volume III	iRMX I SYSTEM CALLS
Volume IV	iRMX I OPERATING SYSTEM UTILITIES
Volume V	iRMX I INTERACTIVE CONFIGURATION UTILITY REFERENCE GUIDE

Additional sets of manuals may be ordered.

Training Courses

Training courses are available on the iRMX I Operating System, Intel languages, and Intel microprocessor architectures.

ORDERING INFORMATION

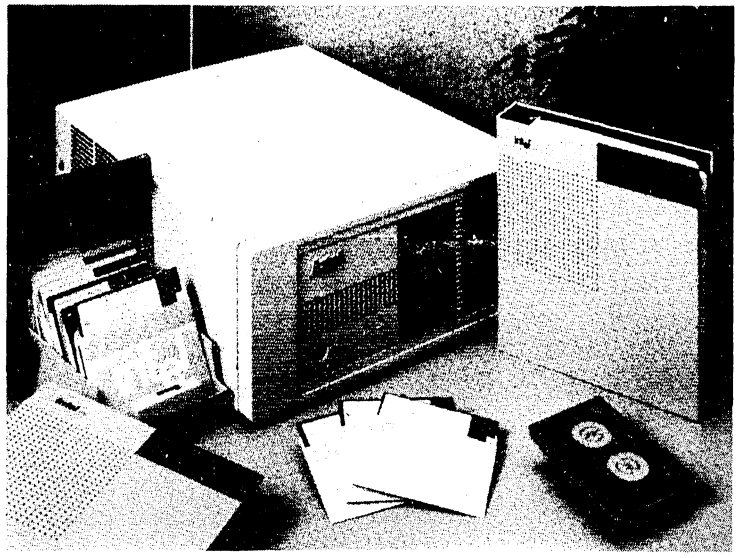
iRMX I Operating System development software is available on both 5¼" and 8" iRMX-format diskettes. The software includes one set of user manuals and 90 days of initial support. This support includes: "TIPS" Technical Information Phone Service; software updates that occur during the support period; monthly ";Comments" magazine and quarterly Troubleshooting Guide; Software Problem Report Service; and membership in the Insite User's Program Library.

Please contact your local Intel Sales Office or authorized distributer for product order codes.

LICENSING

Before iRMX I software will be shipped, a customer must sign (or have already signed) Intel's Software License Agreement (SLA). Once the SLA is signed, the customer is licensed to use the iRMX software for application development. Customers who want to "incorporate" portions of the iRMX I Object Code in an application, will have to sign an Incorporation License which clearly spells out the terms and conditions under which incorporations can be made. Contact your local Intel office for more information and for appropriate licensing.

iRMX® II OPERATING SYSTEMS



The iRMX II family of operating systems provides designers the world's most advanced real-time software for 16-bit designs based on the 80286 and 386™ processors. The product of ten years of real-time expertise by Intel, iRMX II software provides high performance response to external events, excellent support of special purpose hardware, and sophisticated real time programming facilities.

ADVANCED FEATURES AVAILABLE TODAY

- 80286 and 386™ microprocessor support
- 80287 and 80387 math coprocessor support
- 16 megabyte memory addressability
- Multiple tasks and multiple jobs
- Multiprocessing support
- Priority based and/or round robin scheduling
- User extendable object oriented architecture
- Multiple users

A COMPLETE REAL-TIME OPERATING SYSTEM, NOT JUST A KERNEL

- Major functions of iRMX II software include:
  - —Nucleus
  - —Named, Remote, Physical and Stream File System
  - —Basic I/O and Extended I/O systems including device drivers for many Intel MULTIBUS® I/O boards
  - —Bootstrap and Application Loaders
  - —Human Interface supporting on target development and end user reprogramming
  - —Interactive Configuration Utility
  - —System Debugger
  - —Optional networking to systems running the MS-DOS*, VAX/VMS*, XENIX*, iNDX, iRMX I and iRMX II Operating Systems

SOFTWARE WITH A FUTURE

- The leading real time microprocessor software with over 6000 licenses sold
- An active iRMX Users Group (iRUG*) with over 40 chapters worldwide, a regular newsletter, and an annual technical convention.
- Future 80286/80386 family processors will be supported by iRMX operating systems
- Highly compatible with the iRMX I Operating Systems

intel

September, 1988
Order Number: 280618-003

FEATURES

SUPPORT FOR THE FULL RANGE OF REAL TIME APPLICATIONS

The iRMX II Operating Systems support the full range of real time applications, from embedded control designs, to reprogrammable systems which require dynamic creation, deletion, and prioritization of tasks. This flexibility makes it possible to save substantial staff retraining and software maintenance costs by using a single operating system for many different real time systems and subsystems. The iRMX II Operating Systems are ideal for such applications as:

avionics
communications
communication concentrators
data acquisition and analysis
energy management
factory automation
financial trader workstations
image processing
machine control
manufacturing test
medical instruments
military
process control
railroad control
rockets
satellite communications
simulation
SCADA systems
transaction processing

REAL TIME SOFTWARE FOR REAL TIME APPLICATIONS

Real Time Applications are easier to develop with special software. Operating Systems designed for general business use typically lack essential real time features, so real time application development is often expensive, difficult, or even impossible. In contrast, iRMX II software is real time software designed to make the development of real time applications easy and successful.

- **High performance.**
  For real time applications, iRMX II software is typically 100 times faster than general purpose operating systems. This high performance enables applications based on iRMX II software to keep up with the rapid data and control flow of machine and communication interfaces.

- **More reliable code**
  Using iRMX II software ensures more reliable code. When the iRMX II software allocates memory to a task, it assigns read, write, and/or execute-only status to the allocated code and data segments. If the code attempts to execute outside of its range (e.g. stack overflow) or write to a data segment marked read-only, the operating system will issue a "protection" error. This flag can be used to notify an operator of the exact location in the code where the problem occurred. Bounds and access rights checking, which is enforced by the hardware, can catch up to 90% of common coding errors.

- **A rich set of real time programming facilities.**
  The iRMX II software includes a rich set of real time programming facilities that are usually missing in whole or in part from non-real time operating systems. These facilities include:
  —interrupt management with custom exception handlers
  —support for multiple tasks
  —preemptive, priority based scheduling with round robin (time slice) scheduling within a priority level
  —intertask communication through mailboxes and semaphores

- **Easily programmed into PROM.**
  Real time applications built with iRMX II software are easily programmed into PROM's or EPROM's for highly reliable embedded systems which do not require disks. A complete set of languages which support reentrant code are available for use with iRMX II software.

- **Excellent Support for special purpose hardware.**
  Most real time applications involve some special purpose hardware, and general purpose operating systems are often relatively monolithic and difficult to interface to this hardware. In contrast, iRMX II software is a highly configurable, modular software system which easily supports custom hardware. Support for special purpose hardware includes:
  —the ability to configure the operating system by layer
  —hooks for user written handlers at key points
  —the ability to add operating system extensions.
  —standard device driver interfaces

- **Support for designs based on Intel systems, single board computers, and components.**

Central Processing Unit Support

Systems— Bootable preconfigured software supports:
Intel System 310 AP family
Intel System 320 family
Intel System 520 family

Single Board Computers—Preconfigured software is included for:
MULTIBUS I: iSBC® 286/10A, iSBC 286/12/14/16, iSBC 386/12, iSBC 386/2X/3X
MULTIBUS II: iSBC 386/116/120, iSBC 386/258

Component Designs—Minimum required hardware to run iRMX II software:
80286 or 386™ microprocessor
8259A Programmable Interrupt Controller
8254 or 8253 Programmable Interval Timer
Necessary memory

MULTIBUS® II HARDWARE AND iRMX® SOFTWARE BUILD HIGH-PERFORMANCE MULTIPROCESSOR SYSTEMS

MULTIBUS II systems, which pass data over the bus using high-speed messages, enable engineers to easily assemble high-performance, multiprocessor systems. Bus arbitration problems are virtually eliminated and slower speed I/O boards cannot slow down data transfer across the bus since all data is passed at the full bus bandwidth of 40 MBytes/second.

With iRMX II software and other software from Intel's family of real-time software products, engineers can design complex, high-capability systems with a minimum of custom code. An example is the system shown in figure 1. This system has a single iSBC 386/258 peripheral controller board that functions as both a bootserver and fileserver to multiple iSBC 386/120 CPU boards in the system. File transfers are handled via the iSBC 186/530 Network Interface Adapter, which also provides an Ethernet network connection. The iSBC 186/410 terminal controller board uses communication software that is downloaded from the system disk. The iSBX™ 279 Display Subsystem, together with iRMX Virtual Terminal software, provides access to any processor in the system via a single console with multiple windows.

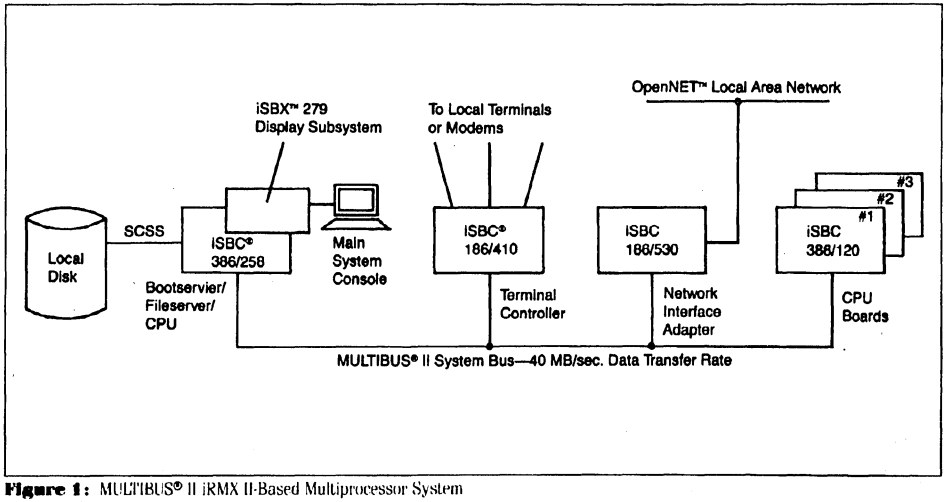


Figure 1: MULTIBUS® II iRMX II-Based Multiprocessor System

A COMPLETE REAL TIME OPERATING SYSTEM, NOT JUST A KERNEL

With comparable performance, iRMX II operating systems provide many features that are extra cost items, or simply unavailable, in real time kernels. These features make the development of real time applications much easier and faster, but do not add unneccessary overhead. In fact, all functional layers except the nucleus are optional in iRMX II software. This flexibility allows you to include only those features that your application requires. The following is a brief description of the major functional groups within iRMX II software.

Nucleus

The Nucleus is the heart of the operating system and controls all resources available to the system. The nucleus provides key real time features including:

- support of multiple tasks
- priority based and/or time slice scheduling
- dynamic priority adjustment
- memory management with 16 megabyte addressability
- intertask communication and synchronization using mailboxes and semaphores
- interrupt management with custom exception handlers
- descriptor table management
- time management
- object management
- the addition of custom operating system extensions

Nucleus Communications Service

The Nucleus Communications Service provides the software interface between application code and the MULTIBUS II message-passing coprocessor. This software simplifies the job of sending messages between tasks on different boards and provides a standard software interface to any other MULTIBUS II board in the system.

Basic I/O System (BIOS)

The Basic I/O System (BIOS) provides primitives to read from and write to peripherals, as well as the ability to buffer I/O. The BIOS also sets up the file structures used by the system and provides access to all required peripherals through a standard device driver interface. Many device drivers are provided with iRMX II Operating Systems, and custom device drivers and file drivers may be added by the user.

iRMX® II Device Drivers

iSBX™ 350	Parallel Port (printer interface)
iSBX 217C	Tape Drive Controller
iSBX 218A	Flexible Disk Controller
iSBX 279	Display Subsystem
iSBX 354	2 Channel Serial Port
8251A, 8274, 82530	Serial Communications Controllers
Memory	RAM Disk Driver
MULTIBUS I:	
iSBC 188/56	Terminal Controller
iSBC 548	Terminal Controller
iSBC 208	Flexible Disk Controller
iSBC 220	SMD Disk Controller
iSBC 214	Multi-Peripheral Controller
iSBC 215G	Winchester Disk Controller
iSBC 221	Peripheral Controller
iSBC 534	4 Channel Terminal Interface
iSBC 544A	Intelligent 4 Ch. Terminal Controller
MULTIBUS II:	
iSBC 186/410	Terminal Controller
iSBC 186/224A	Peripheral Controller
iSBC 286/100A	SCSI Driver
iSBC 386/258	Peripheral Controller/CPU

Extended I/O System (EIOS)

The Extended I/O System (EIOS) provides similar services to the BIOS, with simplified calls that give less explicit control of device behavior and performance. The EIOS also provides a logical-to-physical device connection, and allows a program to specify a logical address for output.

FEATURES

Universal Development Interface (UDI)
The Universal Development Interface provides an easy to use interface with a standard set of system calls to allow programs and languages to be easily transported to or from iRMX II Operating Systems to other operating systems that support the UDI standard.

Application Loader
The Application Loader is used to load programs from mass storage into memory. Programs may be loaded under program or operator control.

Bootstrap Loader
The Bootstrap Loader is used at initialization to load the operating system or an application system from mass storage into memory, and then to begin the system's execution.

System Debugger
The System Debugger is used to debug applications and give a view into the system itself.

Human Interface
The Human Interface allows multiple users to effectively develop applications, maintain files, run programs, and communicate with the operating system. It consists of a set of system calls, a set of commands, and a Command Line Interpreter. Commands are available for file management, device management, and system status. The Command Line Interpreter is a sophisticated tool for program development and system design. Its features include dynamic logon, full line editing, user extensions, and support for background jobs. In addition, the Command Line Interpreter may be replaced for special applications. For example, a Computer Aided Tomography (CAT) scanner controlled by iRMX II software can use a custom Command Line Interpreter to allow the operator to direct the movement of the scanner.

iRMX networking allows your real time application to communicate effectively with general purpose computer systems as well as other real time systems.

iRMX® II Configuration Size*

System Layer	Code Size	Data Size
Nucleus	34KB	2KB
Nucleus Comm. Service	17KB	3KB
BIOS	97KB	108 bytes
EIOS	19KB	16 bytes
UDI	9KB	32 bytes
Application Loader	10KB	100 bytes
System Debugger	35KB	1KB
Human Interface	84KB	224 bytes

*All layers are optional except the nucleus.

iRMX® II and iRMX-NET™ Software Make Networking Easy
Systems using iRMX II software are easily networked to other iRMX, DOS, VAX/VMS, or XENIX systems using iRMX-NET networking software, a member of Intel's family of OpenNET™ network software products. Using this software, a local system can access files on other systems connected to the network, including the ability to Backup and Restore files to a remote system or disk. This network file access is transparent to the local system, even if the remote systems use an operating system other than iRMX II software.

MULTIBUS I systems have the added capability of booting over the network and executing as a diskless workstation. This capability can greatly reduce the overall cost of networked systems.

ON TARGET DEVELOPMENT—A BETTER WAY TO DEVELOP REAL TIME APPLICATIONS

Designers familiar with both cross development and on target development agree that on target development is the easier, more reliable method for developing applications. Testing is greatly simplified, and you need become comfortable with only one operating system. Furthermore, a whole set of bugs is avoided by eliminating the transition from one operating system to another.

iRMX II Operating Systems provide solid on target development capability—a capability entirely missing from other real time software for microprocessors.

INTERACTIVE CONFIGURATION UTILITY SPEEDS SYSTEM SOFTWARE DESIGN

iRMX II software includes the Interactive Configuration Utility (ICU), a Computer Aided Software Engineering tool that can be used to generate a custom version of the operating system to match exact system requirements. The ICU automates the time consuming and error prone traditional hand configuration of the system by prompting the user for system parameters and requirements, then creates a command file to compile, assemble, build, and bind necessary files.

Development facilities included with iRMX II software:

- a Human Interface supporting multiple users
- 51 Human Interface commands for system status, device management, and file management
- a sophisticated Command Line Interpreter supporting background jobs and full line editing
- Interactive Configuration Utility (ICU)
- Hardware traps to catch up to 90% of typical programming errors
- System Debugger (requires the iSDM Monitor)
- Bootstrap loader with debug option
- Parameter and Data validation
- Universal Development Interface
- Numerous device drivers for Intel MULTIBUS boards

Development facilities available separately for use with iRMX II software:

- Reentrant languages—PL/M 286, FORTRAN 286, C 286, and Pascal 286
- AEDIT—a menu-driven, screen-oriented text editor
- iSDM R3.2 System Debug Monitor—Allows downloading from an iRMX II host to an iRMX II or iRMX I target system
- Soft-Scope* II debugger—an interactive, source level, symbolic debug tool
- ASM286—an 80286 Development Utilities Package including the 80286 Macro Assembler, Builder, Binder, Librarian and Mapper
- ASM86—an 8086 Development Utilities Package including the 8086 Macro Assembler, Linker, Locator, Librarian, and line editor

*Soft-Scope is a registered trademark of Concurrent Sciences, Inc.

FEATURES

INTERACTIVE CONFIGURATION (CONTINUED)

- iRMX-NET™ Networking Software—allows your development effort to be shared over several systems. Includes support for both the iSBC® 186/51, iSBC 186/530, and the iSBC 552A Network Interface Adapters
- VDI™ 720—Graphics software for the iSBC™ 186/78A graphics controller
- iPAT—a Performance Analysis Tool, hosted on an IBM* PC-AT* or equivalent, to aid in the performance optimization of an iRMX application.
- In Circuit Emulators—hosted on an IBM PC-AT or equivalent, to aid in hardware debugging and software tracing
- iUP-200A/iUP-201A Universal Prom Programmer
- a variety of user supplied utilities and special software are available from the iRMX Users Group (iRUG)

SOFTWARE WITH A FUTURE

With over 6000 OEM and development licenses outstanding, the iRMX operating systems are far and away the leading real time software for microprocessors. The iRMX community has grown so that today there is an active iRMX Users Group with over 40 chapters worldwide, an annual technical convention, and a regular newsletter. In addition major universities such as Queens College and the University of California at Berkeley use iRMX software and/or teach real time programming courses featuring the iRMX operating systems.

Over the last decade, Intel has steadily improved the performance and functionality of the iRMX operating systems. You can count on continued improvements in the future.

The iRMX II software runs compatibly on 80286 and 386™ microprocessors, and iRMX operating systems will run on future advanced microprocessors from Intel. **Over the last four years the performance of Intel's 8086 family microprocessors has increased 400%.** When you're using the iRMX operating systems, you benefit from these tremendous performance improvements with a high degree of real time application portability.

OUTSTANDING TECHNICAL SUPPORT

With iRMX II software you're not alone when you're developing a real time application. Intel has the best technical sales support in the real time business. If you run into a snag; training, consulting, and design advice are available close at hand.

*PC-AT and IBM are trademarks of International Business Machine, Inc.

SYSTEM CALLS

iRMX® II SYSTEM CALLS

NUCLEUS

Job Management

RQ$CREATE$JOB	Creates an environment (job) within which related tasks run (memory pool limited to 1 MB)
RQE$CREATE$JOB	Creates an environment (job) within which related tasks run (memory pool up to 16 MB)
RQ$DELETE$JOB	Deletes a job
RQ$OFFSPRING	Provides tokens of the child jobs of the specified jobs
RQE$OFFSPRING	Provides a list of tokens for the child jobs of the specified job in a user supplied data structure

Task Management

RQ$CREATE$TASK	Creates a task
RQ$DELETE$TASK	Deletes a task that is not an interrupt task
RQGETPRIORITY	Returns the static priority of a task
RQSETPRIORITY	Changes a task's priority
RQGETTASK$TOKENS	Returns to the caller a token for the specified task
RQ$SUSPEND$TASK	Increases a task's suspension depth by one; suspends the task if it is not already suspended
RQ$RESUME$TASK	Decreases a task's suspension depth by one; resumes the task if the suspension depth becomes zero
RQ$SLEEP	Places the calling task in the asleep state for a specified amount of time

Exception Handler Management

RQGETEXCEPTION$HANDLER	Returns the current values of the caller's exception handler
RQSETEXCEPTION$HANDLER	Sets exception handler and exception mode attributes

Mailbox Management

RQ$CREATE$MAILBOX	Creates a mailbox which can hold up to 160 messages
RQ$DELETE$MAILBOX	Deletes a mailbox
RQ$SEND$DATA	Sends a message to a mailbox
RQE$RECEIVE$DATA	Allows the calling task to receive a message from a mailbox; the task can optionally wait
RQ$SEND$MESSAGE	Sends an object to a mailbox
RQ$RECEIVE$MESSAGE	Allows the calling task to receive an object; the task can optionally wait if no objects are present

Interrupt Management

RQ$ENABLE	Enables an interrupt level
RQ$DISABLE	Disables an interrupt level
RQSETINTERRUPT	Assigns an interrupt handler and an interrupt task to an interrupt level
RQ$RESET$INTERRUPT	Deletes the interrupt task for an interrupt level
RQGETLEVEL	Returns the interrupt level of highest priority which an interrupt handler has started but not completed
RQENDINIT$TASK	Informs root task that a synchronous initialization process has completed
RQ$ENTER$INTERRUPT	Sets up a data segment base address for an interrupt handler

iRMX® II SYSTEM CALLS

NUCLEUS

Interrupt Management (continued)

RQ$SIGNAL$INTERRUPT	Used by interrupt handlers to invoke interrupt tasks
RQ$EXIT$INTERRUPT	Used by interrupt handlers to send an end-of-interrupt signal to hardware
RQE$TIMED$INTERRUPT	Puts the calling interrupt task to sleep until it is awakened by an interrupt handler, or a specified time period elapses
RQ$WAIT$INTERRUPT	Puts the calling interrupt task to sleep until it is awakened by an interrupt handler

Semaphore Management

RQ$CREATE$SEMAPHORE	Creates a counting semaphore
RQ$DELETE$SEMAPHORE	Deletes a semaphore
RQ$SEND$UNITS	Adds a specific number of units to a semaphore
RQ$RECEIVE$UNITS	Asks for a specific number of units from a semaphore

Region Management

RQ$CREATE$REGION	Creates a region
RQ$DELETE$REGION	Deletes a region
RQ$SEND$CONTROL	Relinquishes control to the next task waiting at the region
RQ$ACCEPT$CONTROL	Causes the calling task to accept control from a region if control is immediately available
RQ$RECEIVE$CONTROL	Causes the calling task to wait at the region until the task receives control

Memory Segment and Memory Pool Management

RQ$CREATE$SEGMENT	Creates a memory segment
RQ$DELETE$SEGMENT	Returns a segment to the memory pool from which it was allocated
RQGETSIZE	Returns the size of a segment
RQSETPOOL$MIN	Changes the minimum size of the memory pool of the caller's job
RQGETPOOL$ATTRIB	Returns memory pool attributes of the caller's job
RQEGETPOOL$ATTRIB	Returns information about a job with more than 1 megabyte of memory
RQE$CREATE$DESCRIPTOR	Creates a descriptor in the Global Descriptor Table describing a memory segment
RQE$DELETE$DESCRIPTOR	Removes a descriptor entry from the Global Descriptor Table
RQE$CHANGE$DESCRIPTOR	Changes the physical address or size of a memory segment by modifying its descriptor in the Global Descriptor Table
RQ$CREATE$BUFFER$POOL	Establishes a buffer pool and returns a token for it
RQ$DELETE$BUFFER$POOL	Deletes a buffer pool
RQ$ATTACH$BUFFER$POOL	Associates a buffer pool with one or more ports
RQ$DETACH$BUFFER$POOL	Ends the association between a buffer pool and a port
RQ$REQUEST$BUFFER	Gets a buffer from an existing buffer pool
RQ$RELEASE$BUFFER	Returns a buffer to the specified buffer pool

MULTIPROCESSING SUPPORT—NUCLEUS COMMUNICATIONS SERVICE

Board and Port ID Assignment

RQ$CREATE$PORT	Creates a port (task ID) for sending/receiving messages between boards
RQ$ATTACH$PORT	Forwards all messages received at a port to another port
RQ$DETACH$PORT	Ends message forwarding
RQGETHOST$ID	Returns the host ID of the board on which the task is running
RQGETPORT$ATTRIBUTES	Returns information about how the port is set up

Interconnect Space

RQGETINTERCONNECT	Retrieves the contents of the specified interconnect register
RQSETINTERCONNECT	Alters the contents of an interconnect register

Message Passing Support

RQ$SEND	Sends a data message to a remote port
RQ$RECEIVE	Accepts a message at a port
RQ$SEND$RSVP	Sends a message and requests a reply
RQ$CANCEL	Cancels an RSVP message transmission
RQ$BROADCAST	Broadcasts a control message to all boards
RRQ$RECEIVE$FRAGMENT	Accepts a part (fragment) of a request (RSVP) data message
RQ$SEND$REPLY	Sent in response to the RQ$SEND$RSVP system call
RQ$RECEIVE$REPLY	Accepts a message that is a reply to an earlier request
RQ$SEND$SIGNAL	Sends a signal (dataless message) to a remote port
RQ$RECEIVE$SIGNAL	Receives a signal from a remote port
RQ$CONNECT	Creates/deletes a connection between the sending task and a remote port

OBJECT ORIENTED PROGRAMMING SUPPORT

Object Management

RQ$CATALOG$OBJECT	Places an object in an object directory
RQ$UNCATALOG$OBJECT	Removes an object from an object directory
RQ$LOOKUP$OBJECT	Returns a token for the catalogued name of an object
RQEGETOBJECT$ACCESS	Returns the access type of an object
RQE$CHANGE$OBJECT$TYPE	Changes the access type of an object
RQEGETADDRESS	Returns the physical address of an object
RQGETTYPE	Returns the type code of an object

Extension Object Management

RQ$CREATE$EXTENSION	Creates a new type of object
RQ$DELETE$EXTENSION	Deletes the new type of object and all instances of that type

Composite Object Management

RQ$CREATE$COMPOSITE	Creates a new object of a type defined by RQ$CREATE$EXTENSION
RQ$DELETE$COMPOSITE	Deletes a new object of a type defined by RQ$CREATE$EXTENSION
RQ$ALTER$COMPOSITE	Replaces components of composite objects
RQ$INSPECT$COMPOSITE	Returns a list of the component tokens contained in a composite object

Operating System Extension Management

RQESETOS$EXTENSION	Attaches a user written system call to the operating system
RQ$SIGNAL$EXCEPTION	Signals the occurrence of an exception to a user written system call to the operating system

Deletion Control Management

RQ$DISABLE$DELETION	Makes an object immune to ordinary deletion
RQ$ENABLE$DELETION	Makes an object susceptible to ordinary deletion
RQ$FORCE$DELETE	Deletes objects whose disabling depths are zero or one

BASIC I/O SYSTEM

Job Level

RQSETDEFAULT$PREFIX	Set default prefix for job
RQGETDEFAULT$PREFIX	Inspect default prefix
RQSETDEFAULT$USER	Set default user for job
RQGETDEFAULT$USER	Inspect default user
RQ$ENCRYPT	Encodes user password

Device Level

RQAPHYSICAL$ATTACH$DEVICE	Asynchronous attach device
RQAPHYSICAL$DETACH$DEVICE	Asynchronous detach device
RQASPECIAL	Asynchronous perform device-level function

File Level

RQACREATE$FILE	Asynchronous data file creation
RQACREATE$DIRECTORY	Asynchronous create a directory
RQADELETE$FILE	Asynchronous delete a data file or a directory
RQAATTACH$FILE	Asynchronous attach file
RQADELETE$CONNECTION	Asynchronous delete file connection
RQACHANGE$ACCESS	Asynchronous change access rights to a file
RQARENAME$FILE	Asynchronous rename file
RQATRUNCATE	Asynchronous truncate file
RQAOPEN	Asynchronous open file
RQACLOSE	Asynchronous close file
RQAREAD	Asynchronous read file
RQAWRITE	Asynchronous write file
RQASEEK	Asynchronous move file pointer
RQAUPDATE	Asynchronous finish writing to output device
RQ$WAIT$IO	Synchronous wait for status after Input/Output

Status/Attribute

RQAGET$CONNECTION$STATUS	Asynchronous get connection status
RQAGET$DIRECTORY$ENTRY	Asynchronous inspect directory entry
RQAGET$FILE$STATUS	Asynchronous get file status
RQAGET$PATH$COMPONENT	Asynchronous obtain path name from connection token

User Objects

RQ$CREATE$USER	Create a user object
RQ$DELETE$USER	Delete a user object
RQ$INSPECT$USER	Get IDs in a user object

Extension Data

RQASET$EXTENSION$DATA	Asynchronous store a file's extension data
RQAGET$EXTENSION$DATA	Asynchronous receive a file's extension data

Time/Date

RQSETTIME	Set date/time value in internally-stored format
RQGETTIME	Get date/time value in internally-stored format
RQSETGLOBAL$TIME	Sets the battery backed-up hardware clock to a specified time
RQGETGLOBAL$TIME	Obtains the time of day from the battery backed-up hardware clock

Logical to Physical Address Conversion

RQ$BIOS$GET$ADDRESS	Returns the physical address of a selector

BASIC I/O SYSTEM (continued)

MULTIBUS II Bootstrap Loader Calls

BS$SEND	Send a message to a remote port
BS$RECEIVE	Receives a data message
BS$SEND$RSVP	Sends a message to a remote port and requests a reply
BS$BROADCAST	Broadcasts a control message to all boards
BSSETINTERCONNECT	Writes to the specified interconnect register
BSGETINTERCONNECT	Reads the specified interconnect register

The bootstrap loader also includes 41 macro procedures for initializing both MULTIBUS I and MULTIBUS II systems.

EXTENDED I/O SYSTEM

Input/Output Jobs

RQ$CREATE$IO$JOB	Creates an I/O job with a memory pool of up to 1M bytes
RQE$CREATE$IO$JOB	Creates an I/O job with a memory pool of up to 16M bytes
RQ$START$IO$JOB	Starts (makes ready) the initial task in an I/O job
RQ$EXIT$IO$JOB	Sends a message to a mailbox and deletes the calling task

Logical Names

RQ$LOGICAL$ATTACH$DEVICE	Creates and catalogs a logical name for a device
RQ$HYBRID$DETACH$DEVICE	Temporarily removes the correspondence between a logical name and a physical device established via LOGICAL$ATTACH$DEVICE
RQ$LOGICAL$DETACH$DEVICE	Deletes a logical name created with LOGICAL$ ATTACH$DEVICE
RQSCATALOG$CONNECTION	Creates a logical name for a connection
RQSLOOKUPCONNECTION	Searches through an I/O job's object directories to find the connection associated with a logical name
RQSUNCATALOG$CONNECTION	Deletes a logical name from the object directory of a job

Status

RQGETLOGICAL$DEVICE$STATUS	Provides status information about logical devices
RQSGET$CONNECTION$STATUS	Provides status information about file and device connections
RQSGET$FILE$STATUS	Allows a task to obtain information about a file

Users

RQGETUSER$IDS	Returns the user ID as defined in the User Definition File
RQ$VERIFY$USER	Verifies a user's name and password

Files

RQSCREATE$DIRECTORY	Creates a new directory
RQSCREATE$FILE	Creates a new physical, stream, or named data file
RQSDELETE$FILE	Deletes a stream, physical, or named file
RQSATTACH$FILE	Creates a connection to an existing file
RQSDELETE$CONNECTION	Deletes a file connection.
RQSOPEN	Opens a connection to a file
RQSCLOSE	Closes an open connection to a file
RQSREAD$MOVE	Reads a number of bytes from a file to a buffer
RQSWRITE$MOVE	Writes a collection of bytes from a buffer to a file
RQSSEEK	Moves the file pointer
RQSTRUNCATE$FILE	Removes information from the end of a named data file
RQSCHANGE$ACCESS	Changes the access list for a named file
RQSRENAME$FILE	Changes the path of a named file

Special Devices

RQSSPECIAL	Allows a task to perform functions that are peculiar to a specific device

APPLICATION LOADER

RQALOAD	Loads object code or data into memory
RQALOADIOJOB	Creates an I/O job asynchronously with a memory pool of up to 1M bytes, loads the job's code, and causes the job's task to run
RQEALOADIOJOB	Creates an I/O job asynchronously with a memory pool of up to 16M bytes, and loads the job's code, and causes the job's task to run
RQSLOADIOJOB	Creates an I/O job synchronously with a memory pool of up to 1M bytes, loads the job's code, and causes the job's task to run
RQESLOADIOJOB	Creates an I/O job synchronously with a memory pool of up to 16M bytes, loads the job's code, and causes the job's task to run
RQSOVERLAY	Loads an overlay into memory

UNIVERSAL DEVELOPMENT INTERFACE

Program Control

DQ$EXIT	Exits from the current application job
DQ$OVERLAY	Causes the specified overlay to be loaded
DQ$TRAP$CC	Captures control when CONTROL-C is typed

Files

DQ$ATTACH	Creates a connection to a specified file
DQ$CHANGE$ACCESS	Changes access rights associated with a file or directory
DQ$CHANGE$EXTENSION	Changes the extension of a file name in memory
DQ$CLOSE	Closes the specified file connection
DQ$CREATE	Creates a file for use by the application
DQ$DELETE	Deletes a file
DQ$DETACH	Closes a file and deletes its connection
DQ$FILE$INFO	Returns data about a file connection
DQGETCONNECTION$STATUS	Returns status of a file connection
DQ$OPEN	Opens a file for a particular type of access
DQ$READ	Reads the next sequence of bytes from a file
DQ$RENAME	Renames the specified file
DQ$SEEK	Moves the current position pointer of a file
DQ$SPECIAL	Sets terminal line-edit/ transparent mode
DQ$TRUNCATE	Truncates a file to the specified length
DQ$WRITE	Writes a sequence of bytes to a file

Memory Management

DQ$ALLOCATE	Requests a memory segment of a specified size
DQ$FREE	Returns a memory segment to the system
DQGETMSIZE	Returns the size of the specified memory block
DQGETSIZE	Returns the size of the specified segment
DQ$MALLOCATE	Requests a logically contiguous memory segment of a specified size
DQ$MFREE	Returns memory allocated by DQ$MALLOCATE to the Free Space Pool
DQ$RESERVE$IO$MEMORY	Requests memory to be set aside for overhead to be incurred by I/O operations

Exception Handling

DQ$DECODE$EXCEPTION	Converts an exception numeric code into its equivalent mnemonic
DQGETEXCEPTION$HANDLER	Returns a pointer to the address of the program currently being used to process errors
DQ$TRAP$EXCEPTION	Identifies a custom exception processing program for a particular type of error

Utility and Command Parsing

DQ$DECODE$TIME	Returns system time and date in both binary and ASCII-character format
DQGETARGUMENT	Returns an argument from a STRING
DQGETSYSTEM$ID	Returns the identity of the environment for the UDI
DQGETTIME	Obsolete: included for compatibility
DQ$SWITCHSBUFFER	Selects a new buffer from which to process commands

System Debugger Commands

VC Display system call information
VD Display a job's object directory
VH Display help information
VJ Display job hierarchy
VK Display ready and sleeping tasks
VO Display objects in a job
VR Display I/O Request/Result Segment
VS Display stack and system call information
VT Display any iRMX II object
VU Display system calls in a task's stack

Human Interface

I/O Processing

RQCGET$INPUT$ CONNECTION	Return an EIOS connection for the specified input file
RQCGET$OUTPUT$ CONNECTION	Return an EIOS connection for the specified output file

Command Parsing

RQCBACKUP$CHAR	Move the parsing buffer pointer back one byte
RQCGET$CHAR	Get a character from the command line
RQCGET$INPUT$ PATHNAME	Parse the command line and return an input pathname
RQCGET$OUTPUT$ PATHNAME	Parse the command line and return an output pathname
RQCGET$PARAMETER	Parse the command line for the next parameter and return it as a keyword name and a value
RQCSET$PARSE$BUFFER	Parse a buffer other than the current command line
RQCGET$COMMAND$ NAME	Return the command name by which the current command was invoked

Message Processing

RQCFORMAT$EXCEPTION	Create a default message for an exception code
RQCSENDCORESPONSE	Send a message to the command output (CO) and read a response from the command input (CI)
RQCSENDEORESPONSE	Send a message to the operator's terminal and return a response from that terminal

Command Processing

RQCCREATE$COMMAND$ CONNECTION	Create a command connection
RQCDELETE$COMMAND$ CONNECTION	Delete a command connection
RQCSEND$COMMAND	Concatenate command lines into the data structure created by CREATE$COMMAND$-CONNECTION and then invoke the command

Program Control

RQCSET$CONTROL$C	Changes a calling task's CONTROL-C exchange to the semaphore specified by the call

Command Line Interpreter Commands

!	Recalls a specified command line
Alias	Assigns an abbreviation to a command
Background	Causes a command to be executed in background mode
Changeid	Changes the current user ID to any value between 0 and 65535
Deallas	Cancels the abbreviation assigned by Alias
Exit	Leaves the Super mode
History	Recalls the last 40 lines entered at the terminal
Jobs	Displays a list of background jobs by their job identification number
Kill	Cancels a background job
Logoff	Ends a user session at a dynamic logon terminal
Set	Alters the Command Line Interpreter environment by allowing on-line changes to the terminal name, minimum and maximum background memory pool size, the memory for alias tables, or the prompt string
Submit	Reads, loads, and executes a string of commands from a secondary storage file instead of from the keyboard
Super	Changes the operator to the system manager by changing the user ID

Commonly Used System Programs— File Management Commands

Attachfile	Associates a logical name with an existing file
Copy	Copies files specified in an input list to files specified in an output list
Copydir	Copy a tree of files
Createdir	Creates one or more new directories
Delete	Deletes data files and empty directories from a secondary storage device
Deletedir	Delete a tree of files
Detachfile	Removes the association of a logical name with a file
Deviceinfo	Displays the size and space information for a volume
Dir	Lists a directory's filenames and file attributes
Downcopy	Copies files from an iRMX II volume to an Intellec Development System via the iSDM monitor
Dump	Convert a file into hexadecimal bytes or words
Find	Find a given file name in the file system
Grep	Search a file for a pattern
Help	Provide information on using some Human Interface commands
Modinfo	Display/change static and dynamic segment sizes
Paginate	Break a file into pages with headers
Permit	Grants or rescinds user access to a file
Rename	Changes the names of files or directories
Skim	Examine a text file a screenful at a time
Term	Display or modify the connection or terminal attribute
Translate	Convert to upper or lower case
Tree	Display directory hierarchy and disk usage
Uniq	Reports repeated lines in a file
Upcopy	Copies files, via the iSDM monitor, from an Intellec Development System to an iRMX II volume

SYSTEM CALLS

HUMAN INTERFACE (Continued)

Volume Management Commands

Addloc	Combines the output of LOCDATA and an iRMX II bootloadable file. The output of ADDLOC is another iRMX II bootloadable file
Attachdevice	Attaches a new physical device to the system and catalogs its logical name in the root job's object directory
Backup	Copies named files to a backup volume
Detachdevice	Removes a physical device from system use and deletes its logical name from the root job's object directory
Diskverify	Verifies the data structures of named and physical volumes
Format	Writes format information on an iRMX II volume
Locdata	Reads the specified data and creates a "located" file that can be processed by the ADDLOC command
Restore	Copies files from a backup volume to a named volume
Retension	Retensions a tape before Backup or Restore

System Management Commands

Accounting	Tracks activities of dynamic logon users
Initstatus	Displays the initialization status of Human Interface terminals
Jobdelete	Deletes a running interactive job
Lock	Prevents the Human Interface from automatically creating an interactive job
Logoff	Ends a user session for users with a customized Command Line Interpreter
Password	Changes passwords for dynamic logon users and creates new users when invoked by the system manager
Super	Changes the operator's user ID into that of the system manager (user ID 0) for users who are using a custom Command Line Interpreter
Unlock	Permits the Human Interface to create an interactive job, after the terminal has been locked by the LOCK command

General Utility Commands

Date	Reads or sets the local/global clock date
Debug	Transfers control to the iSDM monitor to debug an iRMX II application program
Logicalnames	Lists all the logical names available to the user
Memory	Displays the memory available to the user
Pause	Prompts the user with a message and waits for a carriage return
Path	Shows the pathname fo a file
Shutdown	Provides an orderly shutdown of the system
Submit	Reads, loads, and executes a string of commands from secondary storage instead of from the keyboard for users with a custom Command Line Interpreter
Time	Reads or sets the local/global clock time
Version	Displays the version numbers of commands
Whoami	Displays the current ID associated with the user
Zscan	Lists the ZAPs (updates) applied to an object module, library, or bootloadable file

ORDERING INFORMATION

iRMX II OPERATING SYSTEMS

Versions of iRMX II Operating Systems are available to support component, Multibus I and Multibus II-based designs, the System 300 Series microcomputers, and the System 520.

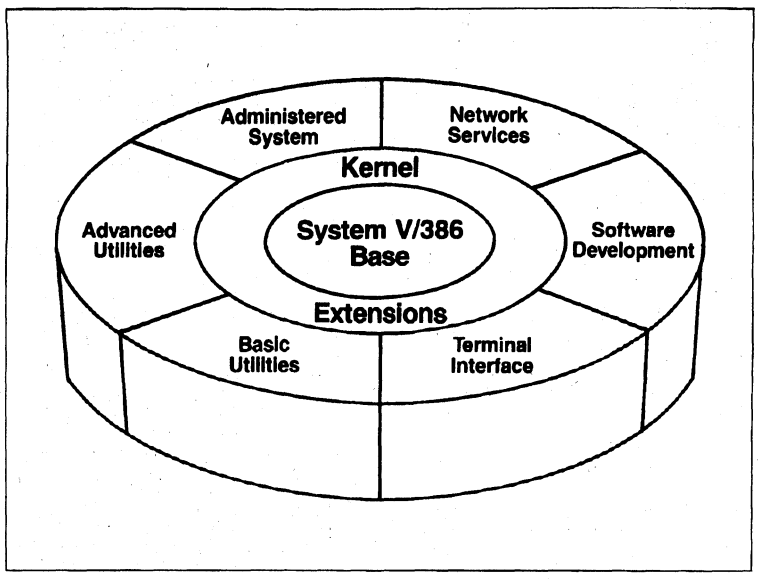
iRMX II software is also available with application development languages, software debuggers, and the iPAT™ Performance Analysis Tool.

Please contact your local Intel Sales Office or authorized distributor for ordering information.

All information is subject to change without notice.

LICENSING

Before iRMX II software will be shipped, a customer must sign (or have already signed) Intel's Software License Agreement (SLA). Once the SLA is signed, the customer is licensed for development. Customers who want to "incorporate" portions of the iRMX II Object Code in an application, will have to sign an Incorporation License which clearly spells out the terms and conditions under which incorporations can be made. Contact your local Intel office for more information and for appropriate licensing.



THE COMPLETE SYSTEM V/386 ENVIRONMENT FOR MULTIBUS SYSTEMS

System V/386 from Intel is a MULTIBUS® I and II version of AT&T's UNIX* System V Release 3.1. It is a complete, UNIX application and system software development environment for MULTIBUS I, MULTIBUS II and the 386™ and is conformant to the System V Interface Definition, Issue 2 (SVID2, Volumes 1, 2 and 3), as well as the defacto System V/386 Applications Binary Interface.

FEATURES

- Full, 32-bit 80386 UNIX System V implementation
- 80386 Hardware demand paging, virtual memory and memory management support
- 80287 and 80387 numeric corprocessor support
- STREAMS OpenNET™ support
- MULTIBUS II system support
- Complete, enhanced UNIX development environment
- SVID2-certified
- Service and support from Intel

FEATURES

STANDARD UNIX* ENVIRONMENT

Developed over the past twenty years, first at AT&T Bell Laboratories, then in Universities and more recently in commercial organizations, UNIX is the most popular multi-user, multitasking operating system available for multiple computer architectures, from micros to mainframes. UNIX System V/386 is the standard interactive, multi-user operating system for the 386.

The UNIX system offers one of the richest development environments available and is the most widely used in technical settings, where its logical, hierarchical structure, uniform file and device I/O, ease of reconfiguration and wealth of applications and tools make it the system software environment of choice for multi-user, multi-tasking applications.

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STANDARD FEATURES

- MULTIBUS II support including an application level interface to MULTIBUS II transport, driver and kernel-level support for message passing and interconnect space access.
- Complete, enhanced UNIX development environment, including Version 4.1 of the C Programming Language Utilities, System Generation Utilities, the Advanced Programming Utilities and Productivity tools. Intel enhancements include an improved kernel debugger, COFF-to-Intel OMF conversion tools and Virtual 86 UDI tools support.
- System V Enhancements, including executable shared libraries, demand paging/virtual memory, reliable signals, the 2KB file system, file and record locking, media independent UUCP, extensive terminal support utilities, the terminfo database and tools, and multiple installation and system administration tools and enhancements from previous releases.
- STREAMS and TLI support, including support for a STREAMS-based version of OpenNET providing interoperation with RMXNET, XNXNET, MSNET, and VMSNET and support for the ISO/OSI Transport Layer Interface.
- International environments support including full support for 8-bit code sets, alternate date and time formats, and alternate character and conversion sets.

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Intel's world-wide support organization provides phone support, troubleshooting guides and updates. On-site or off-site consulting engineers are available, as are training courses in device driver writing and system internals. Ninety days of support and service are included with the product. Extended hardware service, software support and consulting contracts are also available.

ORDERING INFORMATION

ORDER CODES

MBIIMDP1	Single processor MULTIBUS II Modules Development Platform
MBIIMDP2	Dual processor MULTIBUS II Modules Development Platform
SYSTEM 520	MULTIBUS II OEM Platforms. See Product Catalog for details
SYSTEMV386II	MULTIBUS II UNIX binary tape and documentation

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APPLICATION NOTE

AP-405

May 1987

Software Migration From iRMX® 86 to iRMX® 286

MAYNE MIHACSI
OSD Technical Marketing

Order Number 280608-001

INTRODUCTION

The iRMX® 286 operating system represents the evolution of the iRMX® 86 operating system to the protected-mode 80286 and 80386 microprocessors. Therefore, the iRMX 286 operating system has most of the same features of its 8086 counterpart.

Many Intel customers are going to migrate their software from iRMX 86 to iRMX 286. Most customers should be pleasantly surprised at the ease of migration between the two operating systems. This compatibility between the two operating systems was a key objective of the iRMX 286 project. Thus in the majority of cases, an iRMX user should encounter no changes or only trivial changes when porting their software to iRMX 286. In the other cases, iRMX users with a little patience, work, and the help of this paper, should quickly have their application running on iRMX 286.

Before reading this migration note, it is strongly suggested that readers acquaint themselves with the fundamentals of the 80286 architecture.

iRMX® 286 SYSTEM ARCHITECTURE

There are inherent differences between iRMX 86 and iRMX 286 due to the differences in microprocessor architectures. To take advantage of some unique 80286 features additional system calls have been added in the iRMX 286 operating system. These new calls can be identified by an RQE$ in their preface, with the E denoting "extended", to take advantage of the 80286's 16MB addressability.

Figure 1 lists the differences for each layer of iRMX 286.

iRMX® Layer	iRMX® 286 Changes
Nucleus	– 16MB address space – New hardware traps – Descriptor management – Privilege management – Round robin scheduling – Interrupt management – New calls
BIOS	– Memory buffer protection
EIOS	– New calls – Memory buffer protection
Application Loader	– Only loads 80286 OMF records – Only loads STL modules – New calls
Human Interface	– Enhanced CLI – New commands
UDI	– New calls
Bootstrap Loader	– New third stage interface
ICU	– Single stage ICU

Figure 1. iRMX® 286 Architectural Differences

iRMX® 286 NUCLEUS

16 Megabyte Address Space

Today's applications have pushed beyond the 1MB memory limitation of the 8086 architectures. Many Intel customers have chosen iRMX 286 simply because of its ability to address 16MB of memory. While the 80286 architecture allows for accessing 24 physical address lines, to yield 16MB physical and 16MB virtual addressability, the operating system is not automatically allowed the same abilities. As further generations of CPUs become available and memory becomes cheaper, operating systems will strive toward hardware independence. One method used is accessing memory logically, not physically. In the iRMX 286 operating system all memory addresses are logical addresses available via a descriptor table. A logical address may be thought of as a pointer consisting of a selector and an offset. The selector will point to an entry in a descriptor table containing the 24-bit physical address. Therefore, tokens are affected by containing selectors that reference an entry in the descriptor table. No longer do tokens contain the physical address of an object.

New Hardware Traps

Because the 80286 processor detects several types of exceptions and interrupts from exceptions, iRMX 286 also alerts programs generating these exception conditions. These hardware traps will be generated from the following conditions:

INTERRUPT VECTOR	FUNCTION
8	Double exception
9	Processor extension segment overrun
10	Invalid task state segment *
11	Segment not present *
12	Stack segment overrun or not present
13	General protection

*Seldom seen

Users porting iRMX 86 code to iRMX 286 should be aware that the working code in iRMX 86 might still contain errors that will be "trapped" in iRMX 286.

Descriptor Management

While the 80286 CPU is in Protected Virtual Address Mode (PVAM), all application programs deal exclusively with logical addresses. That is, the programs do not directly access actual physical addresses generated by the processor. Instead, a memory-resident table, called a descriptor table, records the mapping between the segment address and the physical locations allocated to each segment. Whenever the 80286 decodes a logical address, translating a full 32-bit pointer into a corresponding 24-bit physical address, it implicitly references one of several descriptor tables. One table is called the Global Descriptor Table (GDT) and provides a complete description of the global address space. Another table is provided, the Local Descriptor Table (LDT), to describe the local address space for one or more tasks. To the application programmer, much of the internal operation and management of the descriptor tables are transparent. However, the systems programmer will need to manage the descriptors to:

A. Gain access to undefined or allocated memory areas, and

B. Add device drivers to the system.

Several new calls were added to help manage descriptor tables:

1. RQE$CREATE$DESCRIPTOR
2. RQE$CHANGE$DESCRIPTOR
3. RQE$DELETE$DESCRIPTOR

For the applications programmer several features are available in iRMX 286.

1. Of the maximum 8K objects available, all are indexed in the GDT with the operating system using the LDT.
2. While using an iRMX 86-style task switch, iRMX 286 runs as one 80286 hardware task.

Privilege Management

Some means of protection is required to prevent programs from improperly using code or data that belongs to the operating system. The four privilege levels of the 80286 are numbered from 0 to 3, where 0 is the most trusted level. The privilege level is an attribute assigned to all segments in a hierarchical fashion. Operating system code and data segments are placed at the most privileged level (0) which is where iRMX 286 operates. (See Figure 2.)

The privilege levels apply to tasks and three types of descriptors:

1. Main memory segments
2. Gates
3. Task state segments (not used in iRMX 286)

Of particular interest to discussions concerning iRMX 286 is the gate descriptor and its usage in application programs.

Of the four types of gates in the 80286 processor, iRMX 286 uses call gates. Once invoked, control is transferred using only the selector portion. This address becomes fixed, allowing any program to invoke another. This prohibits tasks that have not used these entry points from jumping into the middle of the operating system. The use of gates is fundamental to the 80286 architecture and is reflected in other areas of iRMX 286.

All iRMX 286 system calls go through a call gate in order to invoke a given service procedure. In the iRMX 86 operating system, all calls were through software interrupts, invoking an operating system extension handler, then finally the service procedure. For iRMX code that was written for the iRMX 86 operating system, this will have little impact until it comes time to build the system, unless a conflict exists between the old and new nucleus calls. (See next section.) Analogous to the iRMX 86 operating system having a software interrupt at each level, iRMX 286 possesses call gates for each system call at each layer of the operating system, eliminating the need for an operating system extension handler. Call gates can be specified through system calls and the Interactive Configuration Utility (ICU). (See the example for RQESETOS$ EXTENSION.)

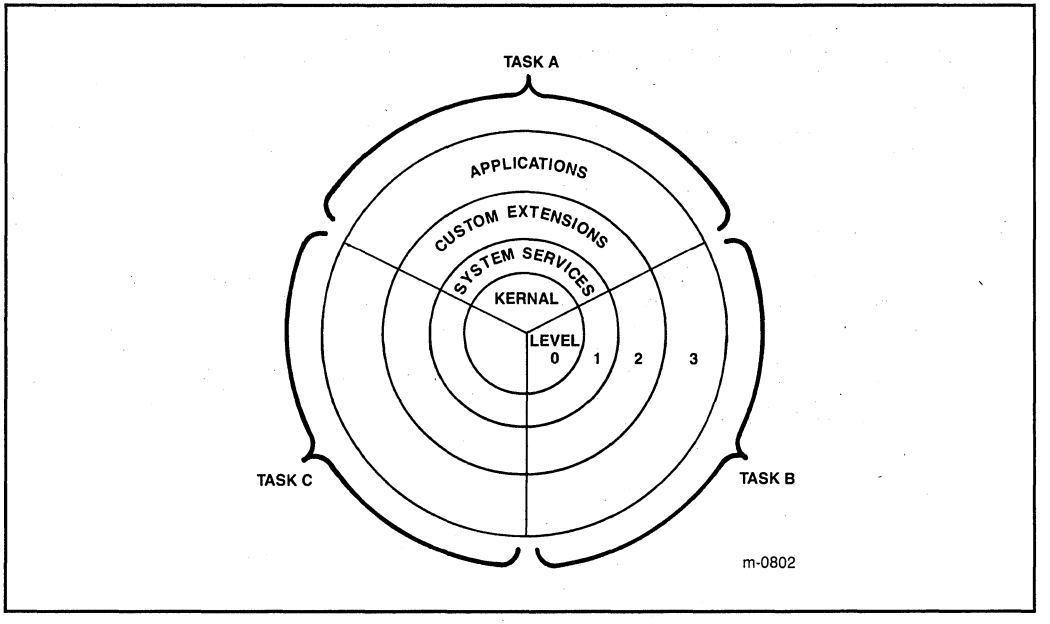
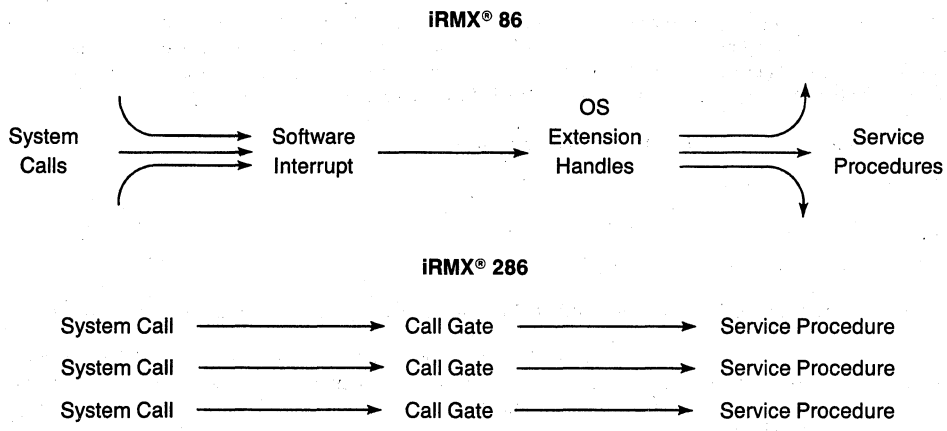


Figure 2. Example Privilege Level Assignments



Call Gates vs. Software Interrupts

Round Robin Scheduling

The iRMX 286 operating system schedules tasks based upon tasks competing for CPU resources. To prevent the occurrence of one or more tasks waiting indefinitely, round robin scheduling is available on the iRMX 286 operating system. One area that could benefit from this scheduling scheme is multi-user environments.

Round robin scheduling will permit equal priority tasks a finite time they may have control of the processor. Once the time expires, the task with the same priority and ready will gain CPU control. Hardware interrupts and higher-priority tasks can still bump any of the lower-priority tasks from running. This scheme allows all equal priority tasks an opportunity to execute.

This scheduling is determined in the "nucleus" screen of the Interactive Configuration Utility (ICU). (See the iRMX 286 Interactive Configuration Utility Reference Manual for details.)

Interrupt Management

In the iRMX 286 operating system interrupt management has changed. In the iRMX 86 operating system an interrupt vector table contains the address of an interrupt handler. In the iRMX 286 operating system this table has been called the Interrupt Descriptor Table (IDT) and is very similar to the GDT and LDT, except that it is referred to only when an interrupt occurs. Interrupt addresses can be entered into the IDT when using the iRMX 286 SET$INTERRUPT nucleus system call. Entering interrupts is still identical for both operating systems, however, with PL/M 286 not having a SET$INTERRUPT built in, interrupts have become easier to use. (See the section on PL/M 286.) The following is a description of the allocated interrupt entries. (Also see the section on BUILD 286 for another way to set interrupts.)

Entry Number	iRMX® 286 Interrupt Allocation Description
0	Divide by zero
1	Single step (used by iSDM™ 286)
2	Power failure (non-maskable interrupt, used by iSDM™ 286)
3	One-byte interrupt instruction (used by iSDM 286)
4	Interrupt on overflow
5	Run-time array bounds error
6	Undefined opcode
7	NPX not present/NPX task switch
8	Double fault
9	NPX segment overrun
10	Invalid TSS
11	Segment not present
12	Stack exception
13	General protection
14-15	<Reserved>
16	NPX error
17-55	<Reserved>
56-63	8259A PIC master
64-127	8259A PIC slaves
128-255	* Available to users *

New Calls

GENERAL RULES

IMPORTANT

Here are some general rules to apply.

1. All iRMX 286 system calls beginning with RQ$... are 100% compatible with iRMX 86.
2. All iRMX 286 system calls beginning with RQE$... are new to iRMX and exist only in iRMX 286.
   a. All iRMX 86 system calls beginning with RQ$... for which there is a like iRMX 286 system call beginning with a RQE$... use the function procedure of the RQE$... call.
3. All iRMX 286 system calls and user extensions use call gates.
4. All iRMX 86 BIOS, EIOS, and loader calls are 100% compatible with iRMX 286 calls.
5. All objects are identified by 16-bit tokens which represent an entry in the Global Descriptor Table (GDT).
6. The iRMX 286 system call RQESETOS$EXTENSION must be used in place of RQSETOS$EXTENSION. This call dynamically attaches an operating system extension to a call gate.

A few specific system calls merit further discussion.

RQESETOS$EXTENSION

This system call as mentioned in Rule 6 above will find the following usage.

```
DECLARE
                . Typical PL/M 286 statements
                .
MY$OS$EXT: PROCEDURE EXTERNAL;

                .
                . Typical PL/M 286 statements
                .
END MY$OS$EXT;

CALL RQE$SET$EXTENSION (0141H, @MY$OS$EXT, @STATUS);
```

Where: 0141H represents the entry number of the call gate from the GDT. This parameter is named GATE$NUMBER.

: @MYOSEXT represents the pointer to first instruction of MYOSEXT. This parameter is named START$ADDR.

: @STATUS represents a pointer to a word containing the condition code for this call. This parameter is named EXCEPT$PTR.

A user-written operating system extension can also be attached to a call by the Interactive Configuration Utility (ICU).

Example of an ICU screen:

```
OS Extension
(GSN) GDT slot number                    [0140H-01FFEH] 0141H
(OCN) entry point name                   [1-45 characters] MY$OS$EXT

Enter changes [Abbreviation ?/= NEW_VALUE]:
Do you need any more O.S. extensions?
```

This causes the GDT slot 141H to be configured as a call gate whose entry point is MYOSEXT.

RQE$CREATE$JOB

This call is an example of Rule 2a where two calls perform nearly the same function. In this case the extended versions of POOL$MIN and POOL$MAX parameters are DWORDS instead of WORDS. This is to allow a memory pool of up to 16MB for tasks and objects. While RQ$CREATE$JOB will create a memory pool of up to 1MB, it will use the same function procedure as RQE$CREATE$JOB. This is possible because the RQ$CREATE$JOB interface procedure changes the word pool parameters to DWORDS by padding them with zeros, then calling the RQE$CREATE$JOB function procedure.

RQ$CREATE$SEGMENT

This call's first parameters, SIZE, yields a different value than in iRMX 86.

In iRMX 86: Segment = RQ$CREATE$SEGMENT (SIZE, EXCEPT$PTR);

Where: SIZE is a word containing the size, in bytes, of the requested segment in MULTIPLES OF 16 BYTES.

In iRMX 286: SEGMENT = RQ$CREATE$SEGMENT (SIZE, EXCEPT$PTR);

Where: SIZE is a word containing the actual memory size in bytes.

RQGETPOOL$ATTRIB

In this case more parameters have been added.

In iRMX 86: RQGETPOOL$ATTRIB (ATTRIB$PTR, EXCEPT$PTR);

Where: ATTRIB$PTR is a pointer to the following structure.

```
Structure  (POOLMAX WORD,
            POOLMIN WORD,
            INITIAL$SIZE WORD,
            ALLOCATED WORD,
            AVAILABLE WORD);
```

In iRMX 286: RQEGETPOOL$ATTRIB has a different structure though everything else is the same

```
Structure  (TARGET$JOB TOKEN,
            PARENT$JOB TOKEN,
            POOLMAX DWORD,
            POOLMIN DWORD,
            INITIAL$SIZE DWORD,
            ALLOCATED DWORD,
            AVAILABLE DWORD,
            BORROWED DWORD);
```

RQSETINTERRUPT

Users should also be aware of the following when using this call in iRMX 286. When specifying interrupts in iRMX 286, a special descriptor table called the Interrupt Descriptor Table (IDT) is located at a user-specified address in memory. This table is accessible through an entry in the Global Descriptor Table (GDT). This makes an interrupt procedure entry point to be directly accessed via a jump to the specific SELECTOR:OFFSET pointer in the IDT. All interrupts will have a SELECTOR:OFFSET address just as in the iRMX 86 operating system. Therefore, the system calls syntax will remain the same, except the parameter called INTERRUPT$HANDLER as shown below:

Example: iRMX 286

```
CALL RQ$SET$INTERRUPT (LEVEL, INTERRUPT$FLAGS, INTERRUPT$HANDLER,
                       INT$HANDLER$DS, EXCEPT$PTR);
```

Where INTERRUPT$HANDLER, the entry point to the interrupt handler, should be coded directly, i.e., @MY$HANDLER.

By referencing a handler directly, all other intermediate steps are unnecessary. (See the example in the PL/M 286 section.)

BASIC INPUT/OUTPUT SYSTEM (BIOS)

The BIOS of the iRMX 86 operating system is nearly identical to the iRMX 86 operating system BIOS. The same system calls are available with no changes or additions. The significant differences between the two BIOS's are the 16MB addressability and memory protection available in the iRMX 286 operating system.

Protection

The memory protection offered by the iRMX 286 operating system BIOS protects the code and data by preventing any task from reading or writing a segment of memory unless explicit access has been granted. It also prevents memory reads or writes from crossing segment boundaries. Therefore any task using the A$READ or A$WRITE BIOS system calls must have read or write access privileges.

Device Drivers

Not all iRMX 86 operating system device drivers have been included in the iRMX 286 operating system. Consult the following list or the iRMX 286 Interactive Configuration Utility for the specific Intel-supplied drivers.

Intel Device Drivers Supplied With iRMX® 286 R. 2.0

- iSBC® 215G
- iSBC 214
- iSBX™ 218A
- iSBX 217C
- iSBC 220
- iSBC 208
- iSBX 251
- iSBC 264
- iSBX 350 Line Printer
- Line Printer for 286/10
- iSBC 534
- iSBC 544
- Terminal Comm Cntlr
  - to include:
    - iSBC 188/48
    - iSBC 188/56
    - iSBC 546
    - iSBC 547
- iSBC 548
- 8274
- 8251A
- 82530
- RAM disk
- iSBC 286/10
- iSBC 286/10A
- iSBC 286/1X
- iSBC 386/2X

Not included are the following device drivers:

- iSBC 204
- iSBC 206
- SCSI
- iSBC 226

EXTENDED INPUT/OUTPUT SYSTEM (EIOS)

The EIOS of the iRMX 286 operating system is nearly identical to the iRMX 86 operating system EIOS. The same system calls are available with few changes and additions. The significant differences between the two EIOS's are the 16MB addressability and memory protection available in the iRMX 286 operating system.

Protection

The memory protection offered by the iRMX 286 operating system EIOS protects the code and data by preventing any task from reading or writing a segment of memory unless explicit access has been granted. It also prevents memory reads and writes from crossing segment boundaries. The system calls S$READ$MOVE and S$WRITE$MOVE are two calls that will send an exception code called EBADBUFF whenever this occurs.

Extended Memory Pool

Since the iRMX 286 operating system supports the 16MB addressability of the 80286 processor, the memory pools created by I/O jobs can also be as large as 16MB. The new system call providing this feature is called RQE$CREATE$IO$JOB.

New Calls

Several new system calls have been added to the iRMX 286 operating system EIOS layer. They are:

1. RQE$CREATE$IO$JOB
   POOLMIN and POOLMAX parameters changed to DWORDS for 16MB addressability.
2. RQSGETDIRECTORY$ENTRY
   Retrieve name of any file in a directory.
3. RQSGETPATH$COMPONENT
   Retrieve name of any file as it is known in its parent directory.

iRMX® 286 APPLICATION LOADER

80286 OMF

Two utilities are supplied with the iRMX 286 operating system to load programs and data into system memory from secondary storage devices. They are the bootstrap loader and the application loader. Typically the bootstrap loader is used to load the initial system and begin its execution. The application loader will typically be called, by programs running in the system, to load additional programs. The application loader can load I/O jobs up to 16MB. These programs must be in the 80286 Object Module Format (OMF). This differs from the iRMX 86 operating system, which loads only 8086 OMF records. Further, the 80286 records must be in STL format. (See a later section called BND 286 for a discussion of STL format.)

New Calls

RQEALOADIOJOB

This calls memory pools changed to DWORD values from word. (See RQE$CREATE$JOB call in the Nucleus section.)

RQESLOADIOJOB

Same as above.

HUMAN INTERFACE

Enhanced Command Line Interpreter (CLI)

The new CLI provides line-editing features, as well as its own set of commands. With CLI commands, aliases can be created, background programs ran, output redirected or redefined for a terminal in the configuration file. The commands are:

!	ALIAS	BACKGROUND	CHANGEID	DEALIAS	EXIT	
HISTORY	JOBS	KILL	LOGOFF	SET	SUBMIT	SUPER

To include or customize features in the CLI, user extensions have been added to the Human Interface.

New Calls

ADDLOC	LOGOFF	SHUTDOWN	LOCK	UNLOCK	ZSCAN

Old Calls

The following Human Interface commands have been revised:

BACKUP	DISKVERIFY	FORMAT	LOCDATA	RESTORE

UDI

New System Calls

The iRMX 286 UDI contains three system calls not contained in the iRMX 86 UDI. They are:

DQ$MALLOCATE

DQ$MFREE

DQGETMSIZE

All of the calls have their counterparts in the iRMX 86 UDI, however, the new system calls use full pointers instead of selectors and DWORD instead of WORD for memory block start address and size specifications, respectively.

These three calls are only supported in programs compiled in the compact or large segmentation models. Also, earlier versions of these calls cannot be mixed. For example:

After using DQ$MALLOCATE to allocate memory, do not use DQ$FREE to free it.

Use DQ$MFREE instead.

BOOTSTRAP LOADER

Two Stage Loader

To facilitate loading an application so that it may execute has been known as "pulling it up by its bootstraps" or simply "booting" the application. iRMX bootstrap loaders have been divided into stages, each possessing a unique purpose and role.

In the iRMX 86 operating system, the bootstrap loader exists as only two stages. The first stage resides in PROM located on the CPU's board. If supplied by Intel, it will occupy less than 8Kb of memory within the PROM. Once running, it will identify the applications name and location, then load part of the second stage, passing control to it. The second stage finishes loading itself, loads the application into memory, then passes control to the application. While the first stage is user-configurable, the second stage is not. The second stage is only supplied by Intel and is present on all iRMX formatted, named volumes.

New Third Stage

In the iRMX 286 operating system, the bootstrap loader exists as three stages. The extra stage was added to be able to load 80286 OMF files. This will also permit loading 8086 OMF files with just the first and second stages. This means either system can be booted without compromising the other. To allow for this, some files have to be renamed and some new conventions adopted. (See below and Figure 3.)

1. All 80286 OMF bootloader application systems must have the extension ".286".
2. The third stage bootstrap loader must have the same name as the application, less the extension.
3. The third stage bootstrap loader must reside in the same directory as the bootloadable system.

File Name Conventions

Third Stage	System to be Loaded
/SYSTEM/RMX86	/SYSTEM/RMX86.286
/SYSTEM/RMX	/SYSTEM/RMX.286
/BOOT/RMX286	/BOOT/RMX286.286

This chart indicates to those wanting to boot the iRMX 86 operating system that their file /SYSTEM/RMX86 had better be renamed to avoid confusion.

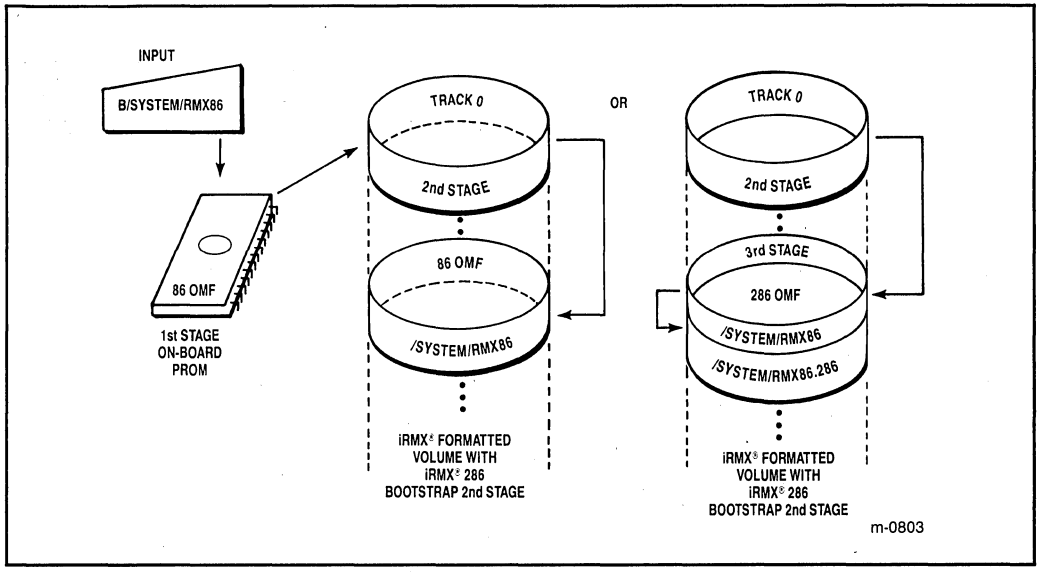


Figure 3.

When installing the iRMX 286 operating system on a system containing the iRMX 86 operating system, the "BS" option of the format command will install ONLY the new second stage bootstrap loader on track 0 of the hard disk. The installation process will also add new directories as required by the iRMX 286 operating system.

Memory Locations of the Three Stages

Bootstrap Loader Locations

Description	Default	Approx. Size	Config. File
1st STAGE CODE	Application dependent	12KB	BS1.CSD
2nd STAGE CODE 1st/2nd DATA and STACK	0B8000H	8KB	BS1.CSD
3rd STAGE (specific) CODE DATA and STACK	0BC000H	16KB	BS3.CSD
3rd STAGE (generic) CODE	0BC000H	8KB	BG3.CSD
3rd STAGE (generic) DATA and STACK	0B8000H	—	BG3.csd

CONFIGURATION SIZE CHART

Operating System Layer	iRMX® 286 Memory Requirements	iRMX® 86* Code Size	iRMX® 286* Code Size	iRMX® 86* Data Size	iRMX® 286* Data Size
Nucleus	34K	24K	27K	2K	3.5K
BIOS	95K	78K	67K	1K	19.5K
EIOS	19K	12.5K	16K	1K	16.75K
Application Loader	12K	10K	11K	2K	2K
HI	36K	22K	26K	15K	1K
UDI	11K	8K	9.4K	0K	0.1K
Bootstrap Loader	—	1.5K	32K	6K	6K
ICU	—	—	—	308K	384K

*These numbers reflect actual memory size required to support the different configurations of the operating systems.

FILE STRUCTURE

The file system of the iRMX 286 operating system provides for the same types of files as are on the iRMX 86 operating system. In fact, both file systems can exist on the same volume using the same hierarchical file structure. This is made possible through the installation of the iRMX 286 bootstrap loader's second stage onto the iRMX 86 operating system's volume. This second stage will allow either operating system to be booted from the same volume. One fact should be remembered: iRMX 286 uses the 80286 OMF, while iRMX 86 uses the 8086 OMF. This stops either operating system from loading and executing the other's files or programs. Copying, deleting or other maintenance operations can still be accomplished across the volume. iRMX 286 operating system will also read iRMX 86 back-up format files from another volume. The following Figure 4 shows a file system with both operating systems installed, including the changes to its structure. Remember, iRMX 286 can reside by itself or with iRMX 86 on the same volume.

Conventions

New file conventions have been adopted to differentiate between several types of files. They are:

*.P28 — PL/M 286 source files
*.P86 — PL/M 86 source files
*.A28 — ASM 286 source files
*.A86 — ASM 86 source files
*.GAT — Gate definition files
*.BLD — Build, file for BLD 286
*.286 — Bootable iRMX 286 system file
*.86 — Bootable iRMX 86 system file

After booting iRMX 286, the following assignments are assumed:

: SYSTEM : = /SYS286
: UTIL : = /UTIL286
: LANG : = /LANG286

After booting iRMX 86, the following still apply:

: SYSTEM : = /SYSTEM
: UTIL : = /UTILS
: LANG : = /LANG

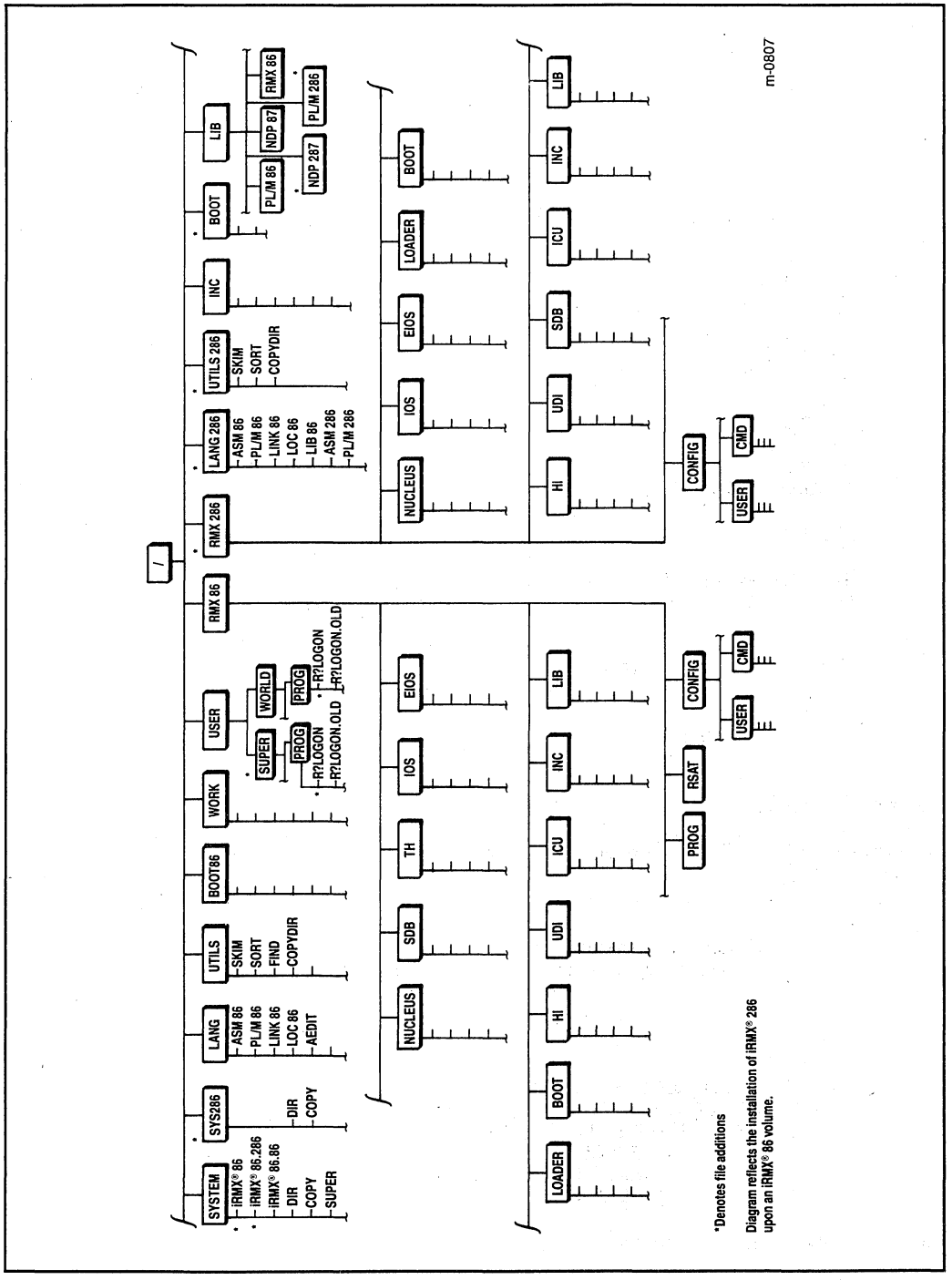

/
SYSTEM
iRMX® 86
iRMX® 86.286
iRMX® 86.86
DIR
COPY
SUPER
SYS286
DIR
COPY
LANG
ASM 86
PL/M 86
LINK 86
LOC 86
AEDIT
UTILS
SKIM
SORT
FIND
COPYDIR
BOOT86
WORK
SUPER
PROG
R?LOGON
R?LOGON.OLD
USER
WORLD
PROG
R?LOGON
R?LOGON.OLD
RMX 86
RMX 286
LANG 286
ASM 86
PL/M 86
LINK 86
LOC 86
LIB 86
ASM 286
PL/M 286
UTILS 286
SKIM
SORT
COPYDIR
INC
BOOT
PL/M 86
NDP 87
RMX 86
NDP 287
PL/M 286
LIB
NUCLEUS
IOS
EIOS
LOADER
BOOT
HI
UDI
SDB
ICU
INC
LIB
CONFIG
USER
CMD
NUCLEUS
SDB
TH
IOS
EIOS
HI
UDI
ICU
INC
LIB
PROG
RSAT
CONFIG
USER
CMD
LOADER
BOOT
m-0807
*Denotes file additions
Diagram reflects the installation of iRMX® 286
upon an iRMX® 86 volume.

Figure 4.

LANGUAGES: ASM 286

Because ASM 286 supports the 80286 in protected mode, ASM 286 has more changes than other languages. Often users converting their programs to ASM 286 from ASM 86 will assemble the programs in ASM 286 and store the error messages generated and change the code accordingly. A few notable changes are listed below.

Group Directive

ASM 286 does not possess a group directive as in ASM 86. By giving the segments the same name, they will be grouped together into one segment at link time.

Example: ASM 86

```
DATAGRP GROUP DATA1, DATA2
DATA1 SEGMENT
ABYTE DB 0
DATA1 ENDS

DATA2 SEGMENT
AWORD DW 0
DATA2 ENDS
ASSUME DS:DATAGRP

: ASM 286

DATA1 SEGMENT RW PUBLIC
ABYTE DB 0                    } In one module
DATA1 ENDS

DATA1 SEGMENT RW PUBLIC
AWORD DW 0                    } In another module
DATA1 ENDS
ASSUME DS:DATA1
```

Segment Directive

The fields of the SEGMENT directive are also different. ASM 286 does not use anything but para-aligned and access-type.

Example: ASM 86

```
NAME SEGMENT [ALIGN-TYPE] [COMBINE-TYPE]
  WHERE [ALIGN-TYPE] = PARA, BYTE, WORD, PAGE, INPAGE,
                       OR NONE

ASM 286

NAME SEGMENT [ACCESS-TYPE] [COMBINE-TYPE]
  WHERE SEGMENT IS ALWAYS PARA-ALIGNED AND
    [ACCESS-TYPE] = READ-ONLY (RO),
                    EXECUTE-ONLY (EO),
                    EXECUTE-READ (ER), or
                    READ-WRITE (RW)
```

Class name is also not present in ASM 286

Stack Segment

In ASM 286, stack segments are defined using the STACKSEG directive.

Example: ASM 286

```
PROG_STACK STACKSEG 10;                    /* MEANS 10 BYTES ON STACK */
```

The operator STACKSTART is used to define a label at the beginning of the stack to initialize the Stack Pointer (SP).

Example: ASM 286

```
MOV SP, STACKSTART PROG_STACK
```

Selector Access

In ASM 286 the selectors used for the DS, SS, and ES in the ASSUME directive must have certain access types.

Example: ASM 286

```
ASSUME DS:EDATA
EDATA SEGMENT RW PUBLIC
        WHERE DB 0
EDATA ENDS
```

Further, the ASSUME directive will not accept an assume for the code segment. The current code segment being assembled is automatically assumed into the CS. For more information regarding other changes in ASM 286 consult: *ASM 286 Reference Manual* (Appendix G), order #122671

LANGUAGES: PL/M 286

Users migrating their code to PL/M 286 should be aware of the following:

Pointer and Selector Variables

Pointer and selector variables cannot be assigned absolute values. All values must be assigned by reference to another variable or through based-variables.

Example: PL/M 86

```
Declare
   A$POINTER     POINTER;

Start: DO;
       A$POINTER = 0;
```

Example: PL/M 286

```
Declare
   A$POINTER     POINTER;

Start: DO;
       A$POINTER = NIL;
```

Similarly selectors can be assigned values as follows:

Example: PL/M 86

```
Declare token literally 'WORD',
        A$TOKEN     TOKEN;

Start: DO;
       A$TOKEN = 0;
```

Example: PL/M 286

```
Declare token literally 'SELECTOR',
        A$TOKEN     TOKEN;

Start: DO;
       A$TOKEN = SELECTOR$OF(NIL);
```

The only relational operations allowed in PL/M 286 for pointers and selectors are "equals" and "not equals".

Models of Compilation

In PL/M 86 the default is SMALL

In PL/M 286 the default is LARGE

Interrupt Vectors

In PL/M 286 all interrupt numbers on all interrupt procedures must be deleted. The required interrupt vectors will be assigned by the 80286 system builder if not already defined by the iRMX 286 operating system call RQSET INTERRUPT.

Consequently the PL/M 86 built-ins SET$INTERRUPT and INTERRUPT$PTR are unavailable in PL/M 286 and should be removed. Also, all calls to interrupt procedures are not allowed. As the conversion process takes shape, all of these changes turn out better than initially expected as the following example shows.

Example: PL/M 86

```
 1. DECLARE      ZERO        LITERALLY       '00001000b',
 2.              INTERRUPT_HANDLER POINTER;
                          .
                          . TYPICAL PL/M 86 STATEMENTS
                          .
 6. INTERRUPT_HANDLER : PROCEDURE INTERRUPT 56 PUBLIC REENTRANT;
                          .
                          . TYPICAL PL/M 86 STATEMENTS
                          .
10.                       CALL RQ$SIGNAL$INTERRUPT (ZERO, @STATUS);
11. END INTERRUPT_HANDLER;

12. INTERRUPT_TASK    : PROCEDURE PUBLIC REENTRANT;
                          .
                          . TYPICAL PL/M 86 STATEMENTS
                          .
16.          INTERRUPT_HANDLER = INTERRUPT$PTR (INTERRUPT_HANDLER);
17.                       CALL RQ$SET$INTERRUPT (ZERO, 1, INTERRUPT_HANDLER,
                                    DATA$SEG$ADDRESS.BASE, @STATUS);
                          .
                          . TYPICAL PL/M 86 STATEMENTS
                          .
21.                       CALL RQ$WAIT$INTERRUPT (ZERO, @STATUS);
22.    END INTERRUPT_TASK;
```

Comments

Line Number	Description
2.	INTERRUPT_HANDLER was defined as a pointer
6.	Interrupt entry 56 was "hard-coded"
16.	INTERRUPT_HANDLER was assigned the location (address) of the first instruction of the handler via the PL/M 86 built-in "INTERRUPT$PTR"
17.	This call could have looked like: RQSETINTERRUPT (ZERO, 1, INTERRUPT_PTR(INTERRUPT_HANDLER), etc eliminating lines 2 and 16.

Example: PL/M 286

```
 1. DECLARE     ZERO      LITERALLY        '00001000b';
                          .
                          . TYPICAL PL/M 286 STATEMENTS
                          .
 5. INTERRUPT_HANDLER  : PROCEDURE INTERRUPT PUBLIC REENTRANT;
                          .
                          . TYPICAL PL/M 286 STATEMENTS
                          .
 9.                       CALL RQ$SIGNAL$INTERRUPT (ZERO, @STATUS);
10.    END INTERRUPTHANDLER;

11. INTERRUPT_TASK     : PROCEDURE PUBLIC REENTRANT;
                          .
                          . TYPICAL PL/M 286 STATEMENTS
                          .
15.                       CALL RQ$SET$INTERRUPT (ZERO, 1, @INTERRUPT_HANDLER,
                                                 DATA$SEG$ADDRESS.BASE, @STATUS);
                          .
                          . TYPICAL PL/M 286 STATEMENTS
                          .
19.                       CALL RQ$WAIT$INTERRUPT (ZERO, @STATUS);
20.      END INTERRUPT_TASK;
```

Comments

Line Number	Description
5.	Notice PL/M 286 does not need to identify the interrupt in this statement
15.	The third parameter becomes simply a pointer to the first instruction of the handler.

DEVELOPMENT TOOLS — BND 286

All iRMX 86 programs linked using LINK 86 will instead have to be bound using BND 286. BND 286 is used to create all single-task application programs that will be dynamically loaded. (See Figure 5.) The following are tasks of the binder.

1. Creates a linkable or loadable module by combining input modules with other bindable modules.
2. Checks the type of variables and procedures.
3. Selects modules from libraries to resolve all symbolic references.
4. Combines logical segments by name, attribute, and privilege levels into physical segments that the processor can manipulate efficiently.
5. Can create a module the application loader can load.

Linkable Modules

In a process called incremental linking, BND 286 combines linkable object modules, including library modules, output by translators. The result is a file containing a linkable module.

Loadable Modules

A dynamically loadable module created by BND 286 is an executable module created by the combination of one or more linkable modules. Loadable modules can be of two types:

1. Single-task loadable (STL)
2. Variable-task loadable (VTL)

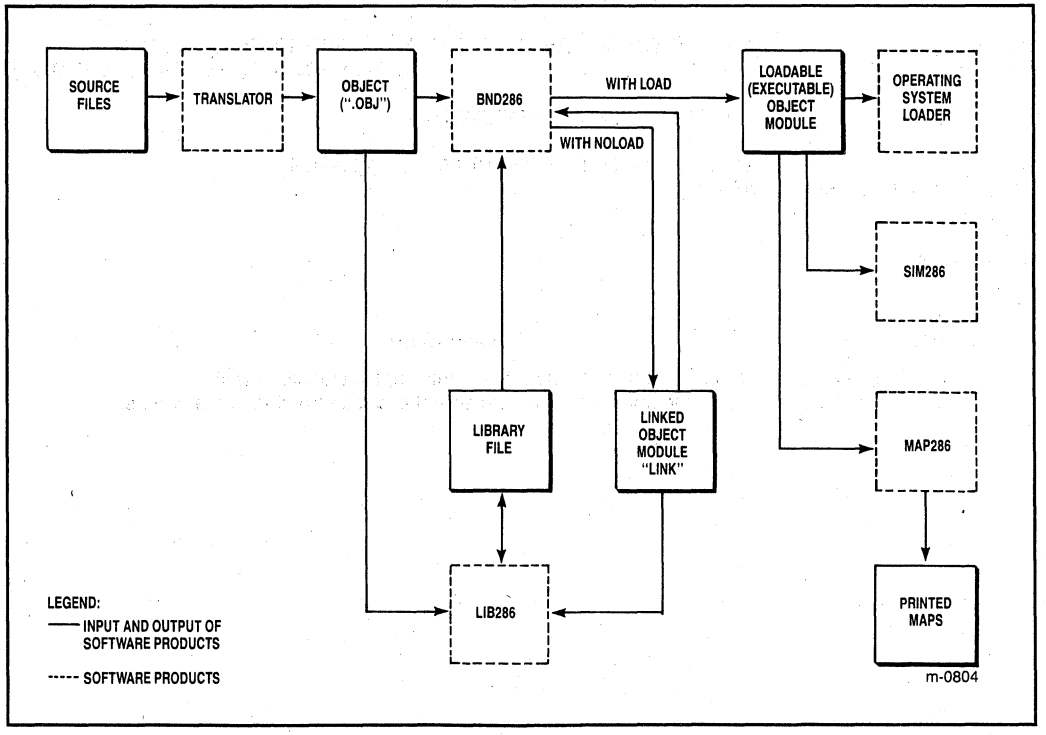


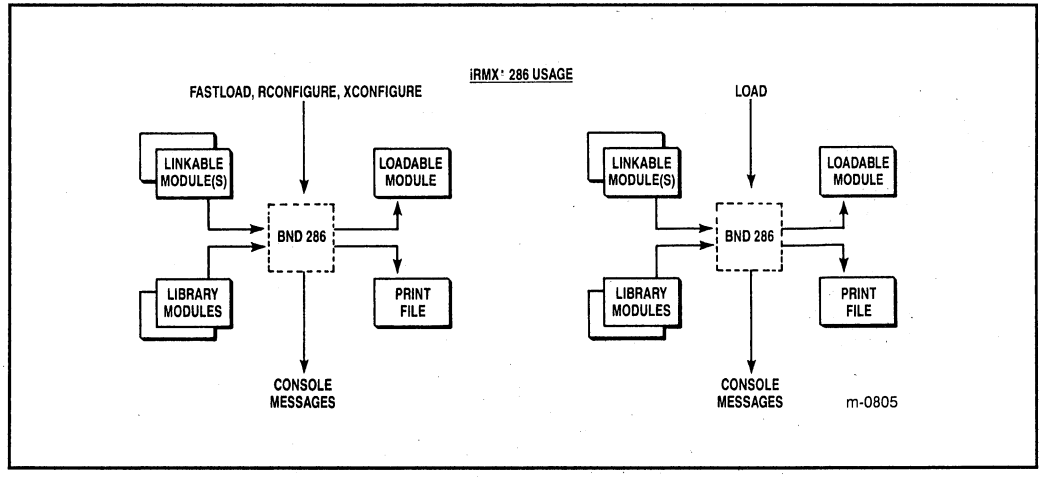
Figure 5. BND 286 Application Program Development

STL Modules

These modules are functionally similar to LTL-format records in the 8086 OMF. STL modules are designed to optimize loader execution time because each contains only one executable task. iRMX 286 and XENIX 286 operating systems will execute only files containing STL modules. BND 286 outputs STL modules when the FASTLOAD, RCONFIGURE, and XCONFIGURE controls are specified. In iRMX 286 only, the RCONFIGURE control is used.

VTL Modules

VTL modules are designed, when provided by BND 286, to also contain a single executable task, but in a format structured for multiple tasks. BND 286 outputs VTL modules when the LOAD control is specified.



BND 286 TO LINK 86 COMPARISON

BND 286 CONTROLS	LINK 86 CONTROLS
CONTROLFILE (pathname)	—
DEBUG/NODEBUG	SYMBOLS/NOSYMBOLS
ERRORPRINT (pathname)/ NOERRORPRINT	—
FASTLOAD/NOFASTLOAD	FASTLOAD/NOFASTLOAD
*LDTSIZE ([+] number)	—
LOAD/NOLOAD	—
NAME (modulename)	NAME (modulename)
OBJECT (pathname)/ NOOBJECT	—
PACK/NOPACK	—
PRINT (pathname)/ NOPRINT	PRINT (pathname)/ NOPRINT
PUBLICS/NOPUBLICS	PUBLICS/NOPUBLICS/PUBLICSONLY
RCONFIGURE (dm,m)	BIND and MEMPOOL
RENAMESEG (old to new)	—
RESERVE (number)	—
SEGSIZE (name(size))	SEGSIZE (name(size))
*TASKPRIVILEGE ( )	—
TYPE/NOTYPE	TYPE/NOTYPE
*XCONFIGURE	—

*Not used in iRMX 286

The following is an example of BND 286 for a simple human interface Commonly Used System Program (CUSP) used on an iRMX 286 Release 1.0 system.

```
BND 286          EXAMPLE.OBJ,                          &
                 EXAMPLE.LIB,                          &
iRMX 286 Libraries—  /RMX286/LIB/UPIFC.LIB,            &
                 /RMX286/LIB/UDI.GAT,                  &
                 /RMX286/LIB/HPIFC.LIB,                &
                 /RMX286/LIB/HI.GAT,                   &
                 /RMX286/LIB/LPIFC.LIB,                &
                 /RMX286/LIB/LOA.GAT,                  &
                 /RMX286/LIB/EPIFC.LIB,                &
                 /RMX286/LIB/EIO.GAT,                  &
                 /RMX286/LIB/IPIFC.LIB,                &
                 /RMX286/LIB/IOS.GAT,                  &
                 /RMX286/LIB/NUCIFC.LIB,               &
                 /RMX286/LIB/NUC.GAT                   &
                 RCONFIGURE (DM(10000H, 10000H))
(Analogous to BIND&MEMPOOL)
                 SEGSIZE (STACK(1024))
(Analogous to segsize)
                 OBJECT (EXAMPLE)
(A new control)
```

iRMX 286 Library Privilege Gates

The following is an example of BND 286 for a simple human interface Commonly Used System Program (CUSP) on an iRMX 286 Release 2.0 system. Notice all of the .GAT files and many of the .LIB files are gone. All of these "missing" files are now contained in the files RMXIFC.LIB and UDIIFC.LIB for convenience.

```
BND 286          EXAMPLE.OBJ,                          &
                 EXAMPLE.LIB,                          &
                 /RMX286/LIB/UDIIFC.LIB,               &
                 /RMX286/LIB/RMXIFC.LIB,               &
                 RCONFIGURE (DM(10000H,10000H))
(Analogous to BIND & MEMPOOL)
                 SEGSIZE (STACK(1024))
(Analogous to SEGSIZE)
                 OBJECT (EXAMPLE)
(A new control)
```

iRMX(R) XXX.BLD File

```
system_bld;
segment
        nucdat.code(dpl = 0),
        nucdat.data(dpl = 0),
memory
        (reserve = (0..0001FFFH,
         003A000H..0FFFFFFh));
        .
        .
gate
        Gate_CreateJob (entry =
            RqCreateJob, dpl = 0, wc = 0),
        .
        .
table
        ldt1 (limit = 00600h,dpl = 0,
        reserve = (2..2, 4..4AH,
        4CH..4EH, 51H..59h,
        122H..005FFh),
        entry = ( 0:nucdat.escape_ss,
                  3:nucdat.stack,
                 75:nucdat.jobdat,
                 79:nucdat.escape_ss,
                 80:nucdat.entry_code) );
task
        rmxtask (dpl = 0,object = nucdat,
                 ldt = ldt1, no ie);

table
        gdt (limit = 00600H, dpl = 0,
        reserve = (3..3BH, 3DH..4EH,
        51H..53H, 55H..59H, 0C1H..0C7H,
        0E3H..0E5H,0EAH..0EFH,
        101H..103H, 00137h..00140h),
        entry = (60:nucdat.data,
                 79:rmxtask,
                 80:nucdat.code,
                 84:ldt1,
                 90:Gate_AcceptControl,
                 91:Gate_AlterComposite,
                .
                .
                308:sdbcnf.code,
                309:sdbcnf.data,
                310:sdbcnf.newstack,
                291:bios_code,
                292:bios_data,
                .
                .
table
        idt(limit = 00080h, dpl = 0);
end
```

DEVELOPMENT TOOLS — BLD 286

BLD 286 exceeds LOC 86 in capability and versatility. In many cases the use of BLD 286 is transparent to iRMX 286 users, due to the ICU 286 automatically generating the BUILD file. All iRMX 286 users, however, should possess an understanding of the following key functions:

A. Assigns physical addresses to entities, sets segment limits and access rights. (See XXX.BLD file)

B. Allows memory ranges to be reserved or allocated for specific entities. (See XXX.BLD file)

C. Creates one Global Descriptor Table (GDT), one Interrupt Descriptor Table (IDT), and one Local Descriptor Table (LDT). (See XXX.BLD file)

D. Creates gates. (See XXX.BLD file)

E. Creates task state segments and (task gates). (See XXX.BLD file)

F. Creates a bootloadable module. (See XXX.BLD file)

G. Creates object files containing exported system entries. (See XXX.BLD file)

H. Selects required modules from specified libraries automatically, as needed to resolve symbolic references.

I. Performs reference-resolution and typechecking.

J. Detects and reports errors and warnings found during processing (in the XXX.MP2 file)

See Figure 6 for an example of BLD 286 program development.

Usage

BLD 286 is primarily used for building an application program that deals extensively with system interfaces to a hardware environment. This could include configuring gates and/or segments that provide this interface, then place these interfaces in a separate file for later exportation.

The types of executable output produced by BLD 286 are bootloadable, loadable, or incremental-built. Bootloadable modules are absolutely-located object modules that are booted via a simple loader. Loadable modules consist of single- or multiple-task modules used for dynamic loading. Incrementally-built modules are non-executable modules used interactively to build large systems.

Many users will only use BLD 286 when they produce a new configuration using the ICU. ICU 286 generates a file called ICUBLD.CSD which invokes the builder using the file XXX.BLD as the builder definition file.

The following is a typical example of the contents of ICUBLD.CSD:

```
BLD 286,                                &
        NUCLUS.LNK,                     &
        SDB.LNK,                        &
        IOS.LNK,                        &
        EIOS.LNK,                       &
        LOADER.LNK,                     &
(Produced by BND 286)
        HI.LNK,                         &
        UDI.LNK                         &
        OBJECT (/BOOT/***.286)          &   ( Where to put the
                                              bootloadable file)
        NODEBUG NOTYPE                  &
        BUILDFILE (***.BLD)                 ( Where to obtain the
                                              build information)
```

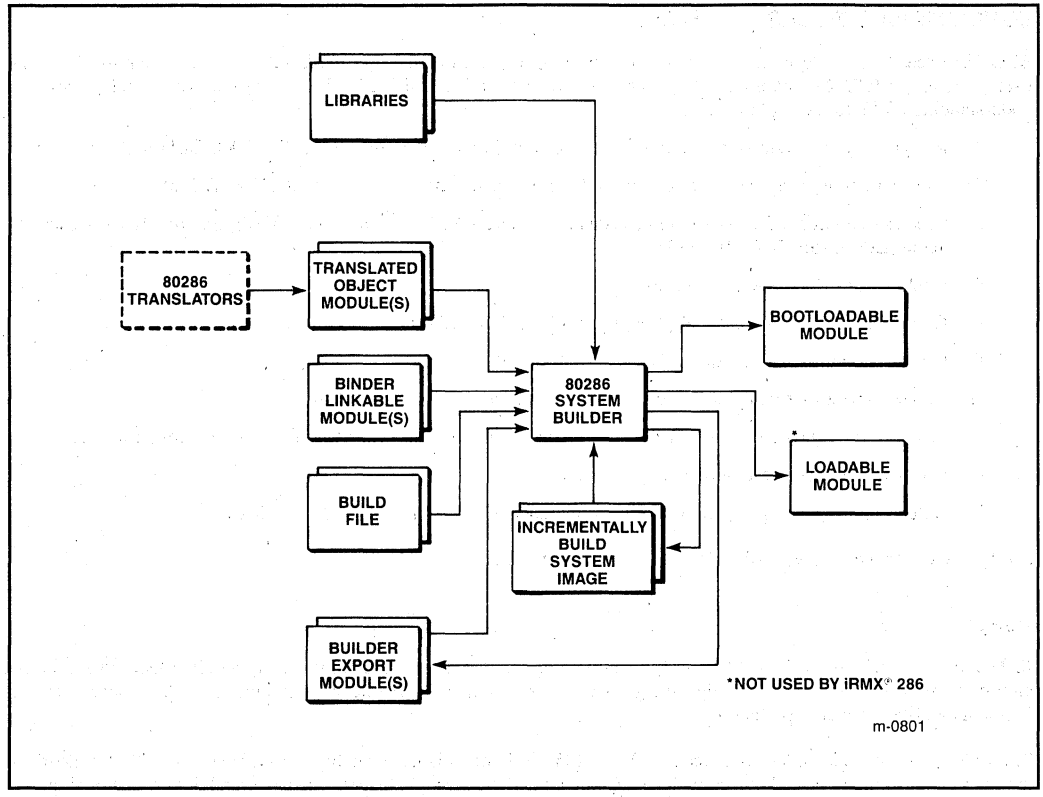


Figure 6. BLD 286 Application Program Development

The build file contains a specific language used by BLD 286 to produce the system or system program. BLD 286 takes all linked input modules and assigns all of the access and protection attributes for each subsystem. A build file is created to specify the characteristics of the relationships among the subsystems. Segment attributes, gates, descriptor tables, aliases, and memory allocation are also described in the build file and read by BLD 286.

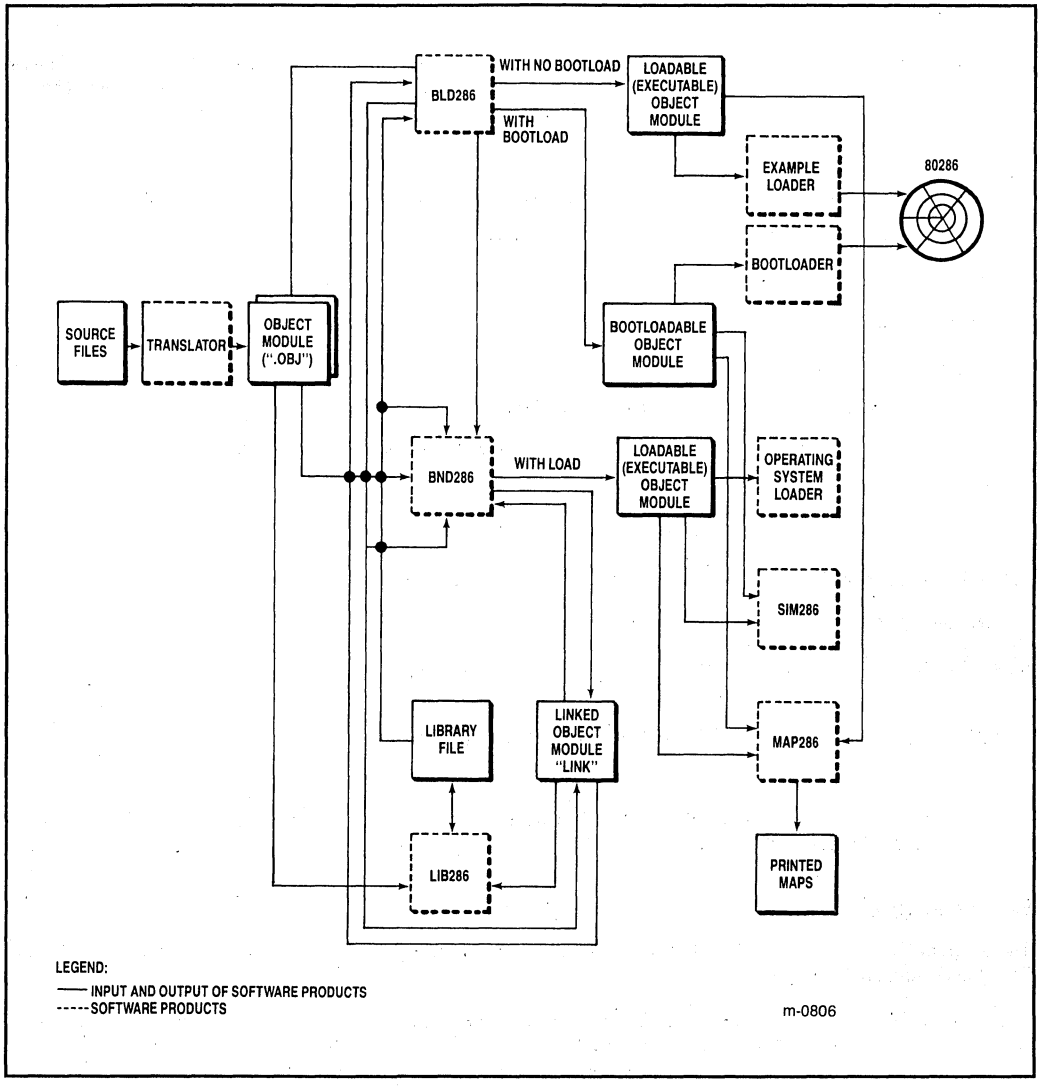

BLD286
WITH NO BOOTLOAD
WITH BOOTLOAD
LOADABLE (EXECUTABLE) OBJECT MODULE
EXAMPLE LOADER
80286
BOOTLOADER
SOURCE FILES
TRANSLATOR
OBJECT MODULE (".OBJ")
BOOTLOADABLE OBJECT MODULE
BND286
WITH LOAD
LOADABLE (EXECUTABLE) OBJECT MODULE
OPERATING SYSTEM LOADER
SIM286
LIBRARY FILE
LINKED OBJECT MODULE "LINK"
MAP286
LIB286
PRINTED MAPS
LEGEND:
—— INPUT AND OUTPUT OF SOFTWARE PRODUCTS
----- SOFTWARE PRODUCTS
m-0806

Figure 7.

MAP 286

The 80286 mapper is a noninteractive utility that generates object module information that BND 286 and BLD 286 do not produce. The utility is offered separately instead of having the builder and linder performing identical functions. The user should note that if debug information is contained in the invocation file, all of the maps will be produced.

MAP 286 will accept the following input:

A. Executable files containing a single executable module, and only one per invocation of MAP 286.

B. Executable files containing a single bootloadable module.

C. One or more linkable or library files.

MAP 286 produces the following output maps:

For executable input files:

A. An output object file with or without debug information.

B. Table MAP, segment MAP, gate MAP, public MAP, symbol MAP, task MAP, and crossreference MAP.

For linkable input files:

A. Only a cross reference map including a module list.

In iRMX 286 the following is a typical invocation of the mapper on an executable file called

```
MAP    286    MYPROG    <CR>
```

If debug information is in "MYPROG" all of the maps will be produced.

iRMX® 86 OPERATING SYSTEM PROGRAM MIGRATION

Compiling in PL/M 286

The following is an example of converting an iRMX 86 Commonly Used System Program (CUSP) called NOTE. To assist readers, all of the conversion steps will be described.

Source Program

The program NOTE is written in PL/M 86 for use on iRMX 86 operating system. When invoked, the utility will echo a line of keyboard input to the console.

The source code file name for NOTE is NOTE.P86. To adhere to PL/M 286 and iRMX 286 operating system file naming conventions, the file should be renamed to NOTE.P28. Next, the file has to be changed to reflect changes in PL/M 286 and iRMX 286 library files. Finally the file is compiled and bound with BND 286. See the following examples for further explanation.

STEP 1

Copy NOTE.P86 to NOTE.P28 <CR>

STEP 2

The NOTE.P28 file has to be edited to change

A. All '0' pointers to 'NIL'

B. All '0' selectors to 'SELECTORS$OF(NIL)'

Also notice all of the include files assume an iRMX 86 operating system and have to be changed to iRMX 286 libraries.

STEP 3

The new NOTE.P28 program is compiled and any errors are corrected.

```
$title('iRMX 86 HI NOTE command')
$subtitle('module header')
/*************************************************************************
 TITLE: note
 ABSTRACT:
  This module contains the main routine for the HI note command.

    NOTE  message

  Message will be printed on EO.
*************************************************************************/
hnote: DO;

$include(:sd:inc/hstand.lit)
$include(:sd:rmx86/inc/hgtchr.ext)
$include(:sd:rmx86/inc/hsneor.ext)
$include(:sd:inc/hutil.ext)

DECLARE
 version(*) BYTE  DATA( 'program_version_number=F001',
       'program_name=Note',0);

1  main: DO;
    /* local variables */
2 DECLARE
3  excep   WORD,
4  char   BYTE,
5  count   WORD,

6  msg  STRUCTURE(
7       length    BYTE,
8       char(STRING$MAX) BYTE);

9     count = 0;
10    char = rq$C$get$char( @excep);
11    DO WHILE( (char := rq$C$get$char( @excep)) <> 0);
12   IF  count < LAST(msg.char)  THEN
13    DO;
14     msg.char(count) = char;
15     count = count + 1;
16    END;
17     END;
18     msg.char(count) = cr;
19     count = count + 1;
20     msg.char(count) = lf;
21     count = count + 1;
22     msg.length = count;
23    CALL rq$C$send$EO$response( 0, 0, @msg, @excep);

    /* exit from command */

24    CALL cusp$error( excep, @(0), @(0), ABORT);
25   END main;

END hnote;
```

THIS POINTER NEEDS CHANGING.

PLM 86 Example

```
$title('iRMX 286 HI NOTE command')
$subtitle('module header')
/*************************************************************************
 TITLE: note
 ABSTRACT:
  This module contains the main routine for the HI note command.

    NOTE  message

  Message will be printed on EO.
*************************************************************************/
hnote: DO;

$include(:sd:inc/hstand.lit)
$include(:sd:rmx86/inc/hgtchr.ext)
$include(:sd:rmx86/inc/hsneor.ext)
$include(:sd:inc/hutil.ext)

DECLARE
 version(*) BYTE  DATA( 'program_version_number=F001',
       'program_name=Note',0);

1  main: DO;
    /* local variables */
2  DECLARE
3   excep   WORD,
4   char    BYTE,
5   count   WORD,

6   msg  STRUCTURE(
7       length    BYTE,
8       char(STRING$MAX) BYTE);

9    count = 0;
10    char = rq$C$get$char( @excep);
11    DO WHILE( (char := rq$C$get$char( @excep)) <> 0);
12   IF  count < LAST(msg.char)  THEN
13    DO;
14     msg.char(count) = char;
15     count = count + 1;
16    END;
17    END;
18     msg.char(count) = cr;
19     count = count + 1;
20     msg.char(count) = lf;
21     count = count + 1;
22    msg.length = count;
23    CALL rq$C$send$EO$response( NIL, 0, @msg, @excep);

    /* exit from command */

24     CALL cusp$error( excep, @(0), @(0), ABORT);
25   END main;

END hnote;
```

THIS IS OK NOW.

PLM 286 Version Example

Binding an iRMX® 286 Application

STEP 1

If a program was previously linked in iRMX 86, we then examine the original LINK file used and notice the following:

```
PLM86 %0.P86 COMPACT ROM OPTIMIZE(3) NOTYPE PW(132)
;
LINK86      %0.obj,                          &
   /rmx86/hi/hutil.lib,          &
   /lib/plm86/plm86.lib,         &
   /rmx86/lib/hpifc.lib,         &
   /rmx86/lib/epifc.lib,  &
   /rmx86/lib/ipifc.lib,  &
   /rmx86/lib/rpifc.lib  &
   to %.86
   bind  mempool(10000,0B0000H)
   nosb noty
```

1. The library names will change
2. The pathnames to access the libraries will change
3. BIND and MEMPOOL will change.

STEP 2

The following is the iRMX 286 Release 1.0 version of the file in Step 4. Remember the libraries have changed names between iRMX 286 Release 1.0 and 2.0.

```
PLM286 %0.p28 COMPACT ROM OPTIMIZE(3) NOTYPE PW( 132)
;
bnd286   %0.obj,                                          &
         /rmx286/lib/hutil.lib,                           &
         /rmx286/lib/plm286.lib,                          &
         /rmx286/lib/hpifc.lib, /rmx286/lib/hi.gat,       &
         /rmx286/lib/epifc.lib, /rmx286/lib/eio.gat,      &
         /rmx286/lib/ipifc.lib, /rmx286/lib/ios.gat,      &
         /rmx286/lib/nucifc.lib, /rmx286/lib/nuc.gat      &
         renameseg(hi_code to code, hi_data to data) segsize (stack(1000H)) &
         object(%0) rc(dm(12000,1000000))
         nodebug noty
```

STEP 3

This is an example of the Step 4 file modified to run on iRMX 286 Release 2.0. Notice the reduction of library statements.

```
PLM286 %0.p28 COMPACT ROM OPTIMIZE(3) NOTYPE PW( 132)
;
bnd286   %0.obj,                              &
         /RMX286/hi/hutil.lib,                &
         /RMX286/lib/plm286/plm286.lib,       &
         /RMX286/lib/rmxifc.lib               &
         renameseg(hi_code to code, hi_data to data) segsize (stack(1000H)) &
         object(%0)  rc(dm(12000,1000000))
         nodebug noty
```

Though these few migration examples reflect trivial modifications, larger and more complex applications might require a little more attention.

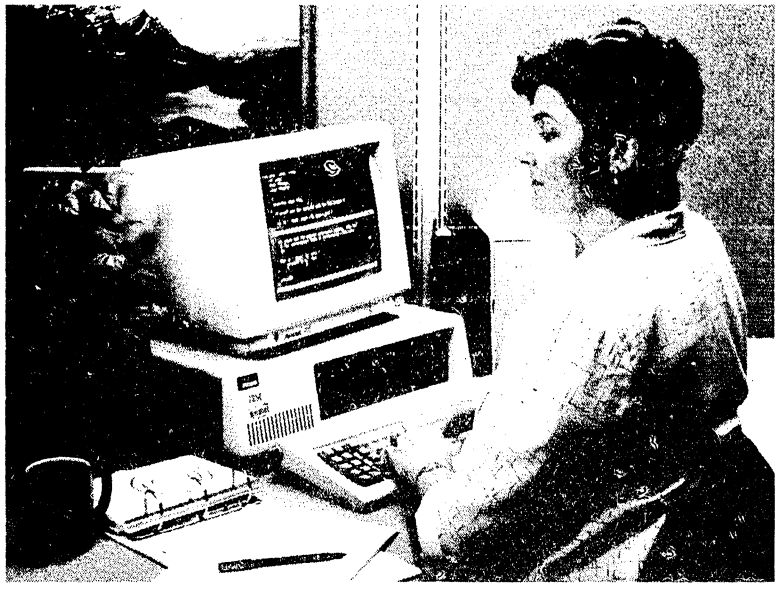
SUMMARY

The purpose of this application note is to provide insight and direction to those individuals contemplating using the iRMX 286 operating system. For those already familiar with the iRMX 86 operating system, this paper's focus is to provide the pathway to a superior product.

The iRMX 286 operating system is a vast improvement over its previous counterpart. Some notable changes are round robin scheduling, hardware-enforced protection, hardware-assisted debugging, and access to the 80386 processor. With this operating system the capabilities of the 80286 processor can be fully utilized for multiple environments.

Since the iRMX product line was introduced, many applications, programs, and lines of code have been written to support a tangible demand for real-time processing; in manufacturing, in medicine, and in finance, to name a few. As a result more time is being spent on designing, writing, and testing software than ever before. The iRMX 286 operating system is the preferred product for generating error-free programs while utilizing the highest CPU technology available in the OEM modules market.

AEDIT SOURCE CODE AND TEXT EDITOR



PROGRAMMER SUPPORT

AEDIT is a full-screen text editing system designed specifically for software engineers and technical writers. With the facilities for automatic program block indentation, HEX display and input, and full macro support, AEDIT is an essential tool for any programming environment. And with AEDIT, the output file is the pure ASCII text (or HEX code) you input—no special characters or proprietary formats.

Dual file editing means you can create source code and its supporting documents at the same time. Keep your program listing with its errors in the background for easy reference while correcting the source in the foreground. Using the split-screen windowing capability, it is easy to compare two files, or copy text from one to the other. The DOS system-escape command eliminates the need to leave the editor to compile a program, get a directory listing, or execute any other program executable at the DOS system level.

There are no limits placed on the size of the file or the length of the lines processed with AEDIT. It even has a batch mode for those times when you need to make automatic string substitutions or insertions in a number of separate text files.

AEDIT FEATURES

- Complete range of editing support—from document processing to HEX code entry and modification
- Supports system escape for quick execution of PC-DOS System level commands
- Full macro support for complex or repetitive editing tasks
- Hosted on PC-DOS and RMX operating systems
- Dual file support with optional split-screen windowing
- No limit to file size or line length
- Quick response with an easy to use menu driven interface
- Configurable and extensible for complete control of the editing process

September, 1988
Order Number: 280804 002

FEATURES

POWERFUL TEXT EDITOR

As a text editor, AEDIT is versatile and complete. In addition to simple character insertion and cursor positioning commands, AEDIT supports a number of text block processing commands. Using these commands you can easily move, copy, or delete both small and large blocks of text. AEDIT also provides facilities for forward or reverse string searches, string replacement and query replace.

AEDIT removes the restriction of only inserting characters when adding or modifying text. When adding text with AEDIT you may choose to either insert characters at the current cursor location, or over-write the existing text as you type. This flexibility simplifies the creation and editing of tables and charts.

USER INTERFACE

The menu-driven interface AEDIT provides makes it unnecessary to memorize long lists of commands and their syntax. Instead, a complete list of the commands or options available at any point is always displayed at the bottom of the screen. This makes AEDIT both easy to learn and easy to use.

FULL FLEXIBILITY

In addition to the standard PC terminal support provided with AEDIT, you are able to configure AEDIT to work with almost any terminal. This along with user-definable macros and full adjustable tabs, margins, and case sensitivity combine to make AEDIT one of the most flexible editors available today.

MACRO SUPPORT

AEDIT will create macros by simply keeping track of the command and text that you type, "learning" the function the macro is to perform. The editor remembers your actions for later execution, or you may store them in a file to use in a later editing session.

Alternatively, you can design a macro using AEDIT's powerful macro language. Included with the editor is an extensive library of useful macros which you may use or modify to meet your individual editing needs.

TEXT PROCESSING

For your documentation needs, paragraph filling or justification simplifies the chore of document formatting. Automatic carriage return insertion means you can focus on the content of what you are typing instead of how close you are to the edge of the screen.

SERVICE, SUPPORT, AND TRAINING

Intel augments its development tools with a full array of seminars, classes, and workshops; on-site consulting services; field application engineering expertise; telephone hot-line support; and software and hardware maintenance contracts. This full line of services will ensure your design success.

SPECIFICATIONS

HOST SYSTEM

AEDIT for PC-DOS has been designed to run on the IBM* PC XT, IBM PC AT, and compatibles. It has been tested and evaluated for the PC-DOS 3.0 or greater operating system.

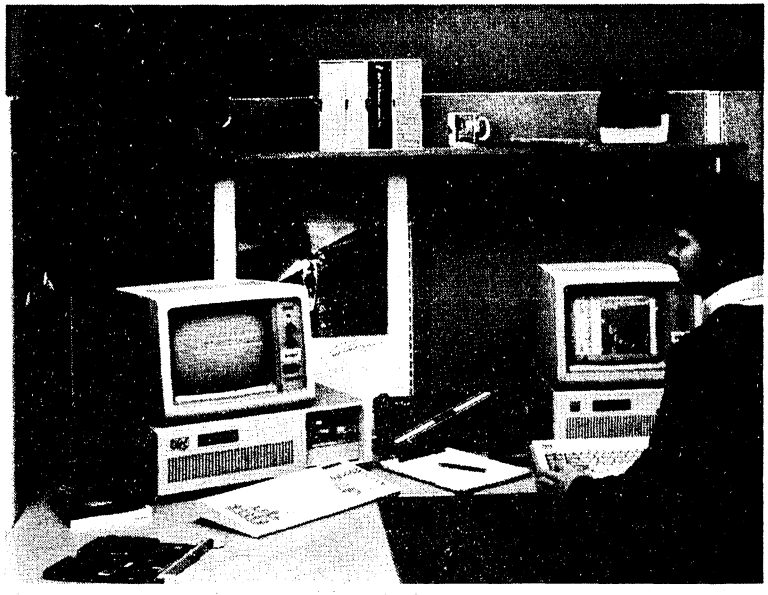
Versions of AEDIT are available for the iRMX™-86 and RMX II Operating System.

ORDERING INFORMATION

D86EDINL	AEDIT Source Code Editor Release 2.2 for PC-DOS with supporting documentation
122716	AEDIT-DOS Users Guide
122721	AEDIT-DOS Pocket Reference
RMX864WSU	AEDIT for iRMX-86 Operating System
R286EDI286EU	AEDIT for iRMX II Operating System

For direct information on Intel's Development Tools, or for the number of your nearest sales office or distributor, call 800-874-6835 (U.S.). For information or literature on additional Intel products, call 800-548-4725 (U.S. and Canada).

iPAT™ PERFORMANCE ANALYSIS TOOL



REAL-TIME SOFTWARE ANALYSIS FOR THE 8086/88, 80186/188, 80286, AND 80386

Intel's iPAT™ Performance Analysis Tool enables OEMs developing applications based on the 8086/88, 80186/188, 80286, or 80386 microprocessors to analyze real-time software execution in their prototype systems at speeds up to 20 MHz. Through such analysis, it is possible to speed-tune applications with real-time data, optimize use of operating systems (such as Intel's iRMX® II Real-Time Multitasking Executive for the 80286 and 80386, and iRMK™ Real-Time Multitasking Kernel for the 80386), characterize response characteristics, and determine code execution coverage by real-time test suites. Analysis is performed symbolically, non-intrusively, and in real-time with 100% sampling in the microprocessor prototype environment. iPAT supports analysis of OEM-developed software built using 8086, 80286, and 80386 assemblers and compilers supplied by Intel and other vendors.

All iPAT Performance Analysis Tool products are serially linked to DOS computer systems (such as IBM* PC AT, PC XT, and PS/2* Model 80) to host iPAT control and graphic display software. Several means of access to the user's prototype microprocessor system are supported. For the 80286 (real and protected mode), a 12.5 MHz iPAT-286 probe can be used with the iPATCORE system. For the 8086/88 (MAX MODE designs only), a 10 MHz iPAT-88 probe can be used with the iPATCORE system. iPATCORE systems also can be connected to sockets provided on the ICE™-286 and ICE-186 in-circuit emulators, or interfaced to I²ICE™ in-circuit emulators with probes supporting the 8086/88, 80186/188, or 80286. The 20 MHz iPAT™-386™ probe, also supported by the common iPATCORE system, can be operated either in "piggyback" fashion connected to an Intel ICE in-circuit emulator for the Intel386™, or directly connected to a prototype system independent of an ICE. iPAT-386 supports all models of 80386 applications anywhere in the lowest 16 Megabytes of the 80386 linear address space.

iPAT FEATURES

- Up to 20 MHz real-time analysis
- Histograms and analysis tables
- Performance profiles of up to 125 partitions
- Code execution coverage over up to 252K
- Hardware or software interrupt analysis
- Simple use with function keys and graphics
- Use with or without Intel ICEs

intel

June, 1988
Order Number: 280786-002

FEATURES

MOST COMPLETE REAL-TIME ANALYSIS AVAILABLE TODAY

iPAT Performance Analysis Tools use in-circuit probes containing proprietary chip technology to achieve full sampling in real-time non-intrusively.

MEETS THE REAL-TIME DESIGNER'S NEEDS

The iPAT products include support for interactions between real-time software and hardware interrupts, real-time operating systems, "idle" time, and full analysis of real-time process control systems.

SPEED-TUNING YOUR SOFTWARE

By examining iPAT histogram and tabular information about procedure usage (including or not including their interaction with other procedures, hardware, operating systems, or interrupt service routines) for critical functions, the software engineer can quickly pinpoint trouble spots. Armed with this information, bottlenecks can be eliminated by means such as changes to algorithms, recoding in assembler, or adjusting system interrupt priorities. Finally, iPAT can be used to prove the acceptability of the developer's results.

EFFICIENCY AND EFFECTIVENESS IN TESTING

With iPAT code execution coverage information, product evaluation with test suites can be performed more effectively and in less time. The evaluation team can quickly pinpoint areas of code that are executed or not executed under real-time conditions. By this means, the evaluation team can substantially remove the "black box" aspect of testing and assure 100% hits on the software under test. Coverage information can be used to document testing at the module, procedure, and line level. iPAT utilities also support generation of instruction-level code coverage information.

ANALYSIS WITH OR WITHOUT SYMBOLICS

If your application is developed with "debug" symbolics generated by Intel 8086, 80286, or 80386 assemblers and compilers, iPAT can use them—automatically. Symbolic names also can be defined within the iPAT environment, or conversion tools supplied with the iPAT products can be used to create symbolic information from virtually any vendor's map files for 8086, 80286, and 80386 software tools.

REAL OR PROTECTED MODE

iPAT supports 80286 and 80386 protected mode symbolic information generated by Intel 80286 and 80386 software tools. It can work with absolute addresses, as well as base:offset or selector:offset references to partitions in the prototype system's execution address space.

FROM ROM-LOADED TO OPERATING SYSTEM LOADED APPLICATIONS

The software analysis provided by iPAT watches absolute execution addresses in-circuit in real time, but also supports use of various iPAT utilities to determine the load locations for load-time located software, such as applications running under iRMXII, DOS, Microsoft Windows*, or MS*-OS/2.

USE STANDALONE OR WITH ICE

The iPAT-386, iPAT-286, and iPAT-86/88 probes, together with an iPATCORE system, provide standalone software analysis independent of an ICE (in-circuit emulator) system. The iPATCORE system and DOS-hosted software also can be used together with ICE-386, ICE-286, ICE-186, and I²ICE-86/88, 186/188, or 286 in-circuit emulators and DOS-hosted software. Under the latter scenario, the user can examine prototype software characteristics in real-time on one DOS host while another DOS host is used to supply input or test conditions to the prototype through an ICE. It also is possible to use an iPATCORE and I²ICE system with integrated host software on a single Intel Series III or Series IV development system, or on a DOS computer.

UTILITIES FOR YOUR NEEDS

Various utilities supplied with iPAT products support generation of symbolic information from map files associated with 3rd-party software tools, extended analysis of iPAT code execution coverage analysis data, and convenience in the working environment. For example, symbolics can be generated for maps produced by most software tools, instruction-level code execution information can be produced, and iRMXII-format disks can be read/written in DOS floppy drives to facilitate file transfer.

WORLDWIDE SERVICE AND SUPPORT

All iPAT Performance Analysis Tool products are supported by Intel's worldwide service and support. Total hardware and software support is available, including a hotline number when the need is there.

*Microsoft Windows and MS are trademarks of Microsoft Corporation. IBM and PS/2 are trademarks of International Business Machines. iPAT, ICE, iRMK, I2ICE, iRMX II, Intel386 are trademarks of Intel Corporation.

CONFIGURATION GUIDE

For all of the following application requirements, the iPAT system is supported with iPAT 2.0 (or greater) or iPAT/I²ICE 1.2 (or greater) host software, as footnoted.

Application Software	Option	iPAT Order Codes	Host System
80386 Embedded	#1	iPAT386DOS[1], iPATCORE	DOS
iRMK on 80386	#1	iPAT386DOS, iPATCORE	DOS
iRMXII OS-Loaded or Embedded on 386	#1	iPAT386DOS, iPATCORE	DOS
OS/2-Loaded on 386	#1	iPAT386DOS, iPATCORE	DOS
iRMXII OS-Loaded or Embedded	#1	iPAT286DOS, iPATCORE	DOS
80286 Embedded	#1	iPAT286DOS, iPATCORE	DOS
	#2	ICEPATKIT[2]	DOS
	#3	I²ICEPATKIT[3]	DOS
	#4	IIIPATD, iPATCORE[3]	DOS[4]
	#5	IIIPATB, iPATCORE[3]	Series III[4]
	#6	IIIPATC, iPATCORE[3]	Series IV[4]
DOS OS-Loaded 80286	#1	iPAT286DOS, iPATCORE	DOS
OS/2 OS-Loaded 80286	#1	iPAT286DOS, iPATCORE	DOS
80186/188 Embedded	#1	ICEPATKIT[2]	DOS
	#2	I²ICEPATKIT[3]	DOS
	#3	IIIPATD, iPATCORE[3]	DOS[4]
	#4	IIIPATB, iPATCORE[3]	Series III[4]
	#5	IIIPATC, iPATCORE[3]	Series IV[4]
DOS OS-Loaded 8086/88	#1	iPAT88DOS, iPATCORE	DOS
8086/88 Embedded	#1	iPAT88DOS, iPATCORE	DOS
	#2	I²ICEPATKIT[3]	DOS
	#3	IIIPATD, iPATCORE[3]	DOS[4]
	#4	IIIPATB, iPATCORE[3]	Series III[4]
	#5	IIIPATC, iPATCORE[3]	Series IV[4]

Notes:

1. Operable standalone or with ICE-386 (separate product; separate host). iPAT-386 probe connects directly to prototype system socket, or to optional 4" probe-to-socket hinge cable (order code TA386A), or to ICE-386 probe socket.
2. Requires ICE-186 or ICE-286 in-circuit emulator system.
3. Requires I²ICE in-circuit emulator system.
4. Includes iPAT/I²ICE integrated software (iPAT/I²ICE 1.2 or greater), which only supports sequential iPAT and ICE operation on one host, rather than in parallel on two hosts (iPAT 2.0 or greater).

SPECIFICATIONS

HOST COMPUTER REQUIREMENTS

All iPAT Performance Analysis Tool products are hosted on IBM PC AT, PC XT, or PS/2 Model 80 personal computers, or 100% compatibles, and use a serial link for host-to-iPAT communications. At least a PC AT class system is recommended. The DOS host system must meet the following minimum requirements:

- 640K Bytes of Memory
- 360K Byte or 1.2M Byte floppy disk drive
- Fixed disk drive
- A serial port (COM1 or COM2) supporting 9600 baud data transfer
- DOS 3.0 or later
- IBM or 100% compatible BIOS

PHYSICAL DESCRIPTIONS

	Width		Height		Length	
Unit	Inches	Cm.	Inches	Cm.	Inches	Cm.
iPATCORE	8.25	21.0	1.75	4.5	13.75	35.0
Power Supply	7.75	20.0	4.25	11.0	11.0	28.0
iPAT-386 probe	3.0	7.6	0.50	1.3	4.0	10.1
iPAT-286 probe	4.0	10.2	1.12	2.8	6.0	15.3
iPAT-86 probe	4.0	10.2	1.12	2.8	6.0	15.3
iPATCABLE (to ICE-186/286)	4.0	10.2	.25	.6	36.0	91.4
IIIPATB.C.D (I²ICE board)	12.0	30.5	12.0	30.5	.5	1.3
Serial cables PC AT/XT PS/2					144.0	370.0

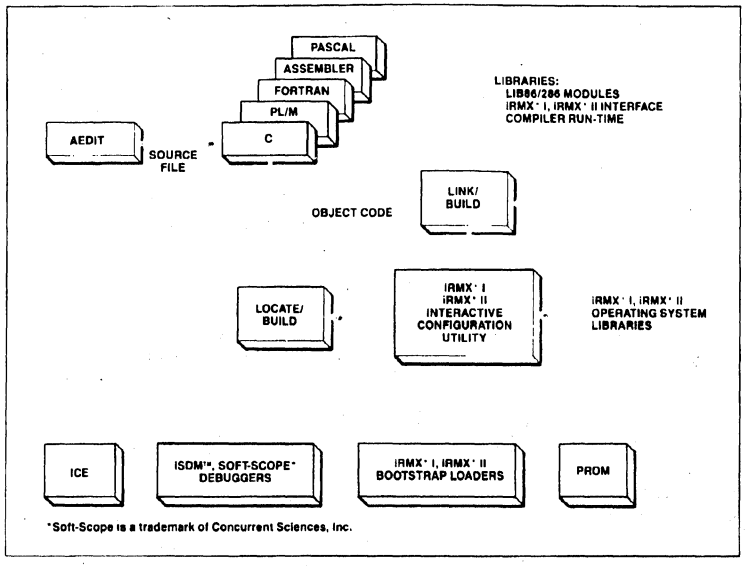
ELECTRICAL CONSIDERATIONS

The iPATCORE system power supply uses an AC power source at 100V, 120V, 220V, or 240V over 47Hz to 63Hz. 2 amps (AC) at 100V or 120V; 1 amp at 220V or 240V.

iPAT-386, iPAT-286 and iPAT-86/88 probes are externally powered, impose no power demands on the user's prototype, and can thus be used to analyze software activity through power down and power up of a prototype system. For ICE-386, ICE-286, ICE-186, and I²ICE microprocessor probes, see the appropriate in-circuit emulator factsheets.

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature:	10°C to 40°C (50°F to 104°F) ambient
Operating Humidity:	Maximum of 85% relative humidity, non-condensing



FULL LANGUAGE SUPPORT FOR iRMX®-BASED SYSTEMS

Intel's iRMX® I and iRMX II-based systems are completely supported by a wide variety of popular languages, utilities, and other tools that build fast, real-time, multi-tasking and multi-processing applications.

iRMX languages and tools run on Intel's iRMX-based 300 series microcomputers and the 386™ processor-based System 120. These languages support development for 8086/88, 80186/188, 80286 and 386-based applications.

FEATURES:

- Industry standard languages—C, PL/M, FORTRAN, Pascal, Assembler
- AEDIT Text Editor
- Complete set of utilities to create and manage object modules
- Supports 8086/186, 8088/188, 80286, and 386 processors
- Supports 8087, 80287, and 80387 math coprocessors
- Optional tools speed software development
  —iPAT™ Performance Analysis Tool
  —Soft-Scope* II source code debugger
  —iRMX Source Control System
  —iRMX Toolbox

FEATURES

FULL LANGUAGE SUPPORT FOR iRMX®-BASED SYSTEMS

Intel has all the software languages and tools you will need to develop a wide range of high-performance applications using the 8086/186, 8088/188, 80286, and 386 processors. iRMX language compilers run on an Intel 300 series microcomputer or System 120, and can be used for MULTIBUS® I or II target systems or embedded applications. Software tools are also available for 8051-family applications.

iRMX languages include C, PL/M, FORTRAN, Pascal, and Assembler. Application code can be easily transported across processor architectures to yield increased performance. For example, 8086 object code will run on the 80286 and 386 processors, and 80286 code will run on the 386 processor. Faster execution results from increased processor pipelining and higher clock rates.

In addition to the wealth of languages available, iRMX-based systems are complemented by utilities with which to create and manage object modules. For the iRMX II system, utilities are provided that allow system programmers to initialize and manage the memory protection features of the 80286/386 transparently to the applications programmer. This latitude in configurability allows programmers to team their efforts in order to achieve a shorter development time than would otherwise be possible.

Because the high-level languages are actually resident on the iRMX-based system, OEMs can pass application software directly on to end users. End users may then tailor the OEM's system to better meet application needs by writing programs using the same languages.

LANGUAGE-INDEPENDENT APPLICATION DEVELOPMENT

Intel's Universal Development Interface (UDI) and Object Module Format (OMF) enable several users to write different modules of an application, in different languages, then link them together.

The OMF provides users with the ability to mix languages on a single application system, affording the luxury of choosing exactly the right language tools for specific pieces of the application, rather than compromising specialized tasks for the sake of one, project-wide language.

FAST, LEAN PROGRAMS FOR RAPID PROCESSING

The iRMX language products enable programmers to write the smallest, fastest programs available in high-level languages, due to the compiler's superior ability to optimize code.

iRMX operating system calls are made directly from C, FORTRAN, Pascal and PL/M. This means that application developers can take full advantage of the iRMX multi-tasking capability, whereby multiple applications execute concurrently on the operating system. Multi-tasking, a requirement of most real-time systems, is as necessary in application software development as in an operating system environment.

STANDARDIZED MATH SUPPORT

All the iRMX languages support floating point operations. This ensures universal consistency in numeric computation results and enables the user to take advantage of the Intel 8087, 80287, and 80387 Numeric Data Processors.

COMPLETE SET OF PROGRAM LINKAGE AND SYSTEM BUILDING UTILITIES

Utilities for iRMX I operating systems include Intel's LINK 86, LOCATE 86 and LIBRARIAN. For iRMX II systems, BND 286 and BLD 286 replace LINK and LOCATE.

Using the LINK 86 or BND 286 programs, users may combine individually compiled object modules to form a single, relocatable object module. This provides the ability to merge work from several programmers into one cohesive application system.

The LOCATE 86 utility maps relocatable object code into the processor memory segments, allowing user definition of module/memory type allocation. For example, often-used portions of an application may be mapped to (P)ROM.

The BLD 286 utility provides the major capabilities of LOCATE 86 plus allows the system programmer to specify the memory protection scheme for the 80286 system.

The LIBRARIAN object code library manager affords easy creation, collection and maintenance of related object code to reduce the overhead of separately maintained modules.

Finally, the MACRO Assemblers for the 8086, 80186, 8088, 80188, 80286, and 386 processors generate extremely efficient code and invoke 8086/8087 or 80286/386 machine instructions.

iRMX® C COMPILER

The popular programming language C is fully supported on iRMX-based systems. iRMX C offers both small and large segmentation models, enabling applications to be written efficiently. The iRMX C compilers combine assembly language efficiency with high-level language convenience; it can manipulate on a machine-address level while maintaining the power and speed of a structured language.

The iRMX C compilers afford easy portability of existing C programs to iRMX-based systems.

iRMX® PL/M

PL/M offers full access to micro-computer architecture while simultaneously offering all the benefits of a high-level language. Invented by Intel in 1976, PL/M 80 was the first microcomputer-specific, block-structured, high-level language available. Since then, thousands of users have generated code for millions of microcomputer-based systems using PL/M 80, PL/M 86, and PL/M 286.

PL/M 86 software written for 8086 processors are easily ported to PL/M 286 for more powerful applications on the 80286 and 386 processors.

iRMX® FORTRAN

The iRMX FORTRAN compiler provides total compatibility with FORTRAN 66 language standards, plus most features provided by the FORTRAN 77 language standard including complex numbers. iRMX FORTRAN includes extensions specifically for microcomputer application development. Programming is simplified by relocatable object libraries, which provide run-time support for execution time activities.

iRMX FORTRAN 86 supports the 8087 math coprocessor and iRMX FORTRAN 286 supports the 80287 for the most powerful microcomputer solutions available in number-intensive applications.

iRMX® PASCAL

iRMX Pascal meets the ISO language standard and implements several microcomputer extensions. A compile-time option checks conformance to the standard, making it easy to write uniform code. Industry-standard specifications contribute to portability of application programs and provide greater reliability.

Pascal supports extensions, such as an interrupt-handler and direct port I/O extension, that allow programs to be written specifically for microcomputers. Separate module compilation allows linkage of Pascal modules with modules written in other high-level languages.

8051 LANGUAGES

For target applications using an 8051 family microcontroller, Intel offers the PL/M 51 compiler and the ASM 51 Macro Assembler and Utilities. Both languages are for use on iRMX I-based development system.

iRMX® AEDIT TEXT EDITOR

The iRMX AEDIT Text Editor is screen-oriented, menu-driven and easy to learn. Guided by the menu of commands at the bottom of the screen, the user can edit text and programs easily and efficiently.

iRMX AEDIT Text Editor allows the simultaneous edit of two files. This allows easy transferral of text between files and use of existing material in the creation of new files. Creating macros, strings of frequently-used commands, is also very simple. The editor "remembers" the selected commands and allows the user to re-use them repeatedly. The iRMX II version also supports operating system level command execution.

iRMX® II SOFT-SCOPE II HIGH LEVEL LANGUAGE DEBUGGER

The Soft-Scope II debugger allows users to debug programs running on the iRMX II Operating System. Programs written in PL/M 286, FORTRAN 286, Pascal 286, and C 286 can be debugged using source code listings.

REAL-TIME SOFTWARE ANALYSIS FOR THE 8086/88, 80186/188, & 80286

Intel's iPAT Performance Analysis Tool enables OEMs developing applications based on the 8086/88, 80186/188, or 80286 microprocessors to analyze real-time software execution in their prototype systems at speeds up to 12.5 MHz. Through such analysis, it is possible to speed-tune applications, optimize use of operating systems (such as Intel's iRMX® II Real-Time Multitasking Executive), characterize response, and determine code execution coverage by test suites. Analysis is performed symbolically, non-intrusively, and in real-time with 100% sampling in the microprocessor prototype environment.

iRMX® SOURCE CONTROL SYSTEM

The iRMX Source Control System (SCS) provides an integrated version control and generation management system for users in an iRMX software development cycle. This facility is useful for large and small software projects to assist in bringing more control, order and methodology to the software development process. SCS can be effectively used on a single iRMX II-based system or across the OpenNET™ network.

iRMX TOOLBOX

The iRMX Toolbox is a set of utilities that provide text formatting, spelling verification, file comparison, and files/record/data sorting for program development. The Toolbox also includes a floating point "desk" calculator. The iRMX Toolbox supports 80286 language application development on an iRMX II host system.

WORLDWIDE SUPPORT

With iRMX Languages, you're not alone when developing a real time application. Intel has the best technical sales support in the real time business. If you run into a problem, training, consulting, and design advice is available through Intel's Worldwide customer support organization. To ensure a successful product life, Support Contracts are available on an annual basis that include:

- Technical Information Phone Service
- Software Updates
- Troubleshooting Guides
- Monthly *:Comments* Magazine
- Response to Software Problem Reports
- Membership to Insite Users' Program Library

FEATURES

INTEL HAS TOTAL SOLUTIONS FOR REAL-TIME SYSTEMS

iRMX I and iRMX II are the fastest, most powerful operating systems available for multi-tasking, multi-user, real-time applications. Complemented by a wide range of industry-standard languages and utilities, the iRMX-based systems are highly flexible and configurable.

Application development for iRMX-based systems is possible at the board or the system level. OEMs can integrate functionality at the most profitable level of product design, using one system for both development and target use. Intel's choice of industry standard high-level languages enables the end user to extend OEM-provided functionality even further, if desired.

Who is better qualified to write and supply software for Intel VLSI than Intel? Today you have the ability to tap into hundreds of available application software packages, languages and utilities, peripherals and controllers and MULTIBUS® boards.

Intel also has a broad range of hardware products, including MULTIBUS I and II boards and systems, and the System 120, a low-cost system for both software development and real-time target applications.

Tomorrow, and ten years down the road, you will be able to tap into the latest high-performance VLSI—without losing today's software investment.

SPECIFICATIONS

REQUIRED HARDWARE

- Any 8086/286/386-based or iSBC 86/286/386-based system including Intel's System 300 series microcomputer family or the System 120.

  Note: 8086 object code will run on 80286 and 386 processors and 80286 object code will also run on the 386 processor. In both cases, the compilers only support 8086/80286 instruction sets, registers and functions.
- 700KB of memory
- Two iRMX compatible floppy disks or one hard disk
- One 5.25" double-density floppy disk drive for distribution software
- System console device

REQUIRED SOFTWARE

The iRMX I (iRMX 86) Operating System Release 7 or later, including the Nucleus, Basic I/O System, Extended I/O System and Human Interface layers.

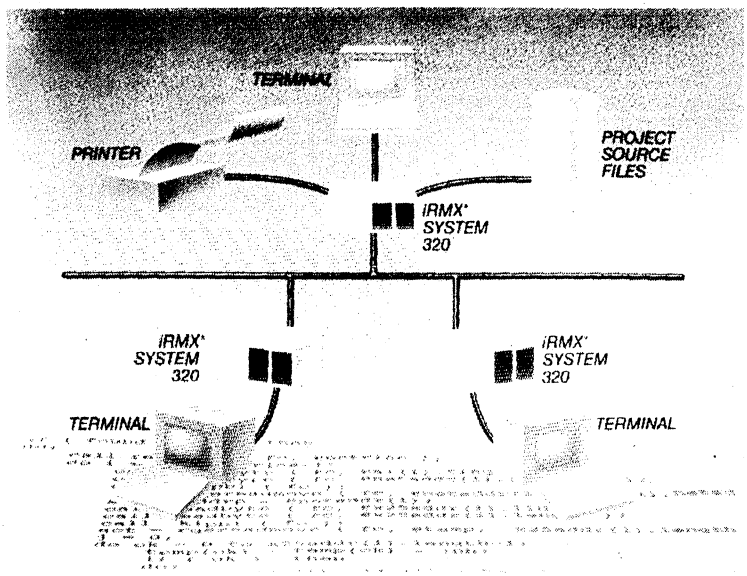
— or —

The iRMX II (iRMX 286) Operating System Release 2 or later, including the Nucleus, Basic I/O System, Extended I/O System and Human Interface.

Purchase of any iRMX-resident language requires signing of Intel's Software License Agreement (SLA).

DATA SHEETS

- 8086 Compilers:
  8086/88/186/188 Software Packages
  (Intel order number 210689)
- 80286 Compilers:
  80286 Software Development Tools
  (Intel order number 231665)
- 8051 Software:
  8051 Software Packages
  (Intel order number 162771-004)



iRMX® SOURCE CONTROL SYSTEM

The iRMX Source Control System (SCS) provides an integrated version control and generation management system for users in an iRMX software development cycle. This facility is useful for large and small software projects to assist in bringing more control, order and methodology to the software development process. SCS can be effectively used on a single iRMX System or across the OpenNET™ network.

FEATURES

- Controls access to source files
- Tracks changes to source files
- Approachable and efficient
- Generates any version of project
- Supports range of iRMX languages

FEATURES

CONTROLS ACCESS TO SOURCE FILES

With iRMX Source Control System the system manager (project leader) has certain privileged commands. These commands can be useful to designate those team members who can access the source files only for object generation and those who can access the source files for updating or changing. Other such privileged commands include the ability to archive a specific version of source and combine several versions of a source file.

TRACKS CHANGES TO SOURCE FILES

The iRMX Source Control System keeps track of changes made to any source files. These changes are stored as backward deltas for disk economy and fast access to the latest version. The project team can now better interact and synchronize using the latest updated version for integration and testing, especially as projects grow increasingly complex. The specific versions of tools used to produce the source code is also tracked.

APPROACHABLE AND EFFICIENT

The iRMX Source Control System has several facilities that help make it very approachable by the user. The tutorial leads the first time SCS user through the structure and capabilities of the iRMX Source Control System. The menu interface helps even the experienced SCS user learn and take advantage of the powerful capabilities of SCS. An on-line help facility assists in quick reminders for using the referenced commands.

The iRMX Source Control System makes efficient use of the system storage area and the development engineer's time.

The iRMX Source Control System can be used on a single iRMX System or can be utilized by a networked/distributed development team.

GENERATES ANY VERSION OF PROJECT

The iRMX Source Control System can be of particular use to both new active development projects as well as the evolving enhancement and maintenance of previous product releases. SCS provides for generation of any version of a project so that users can support (or test) different releases of a project from one source data base. Versions can be tagged for retrieval with symbolic names, state attributes or programmer name. Parallel development paths can be more easily and automatically merged using SCS.

SUPPORTS RANGE OF iRMX LANGUAGES

The iRMX Source Control System can be utilized by developers using any of the popular iRMX languages—PL/M, Assembler, FORTRAN, 'C,' PASCAL. The user can also configure support other special language requirements.

SPECIFICATIONS

PREREQUISITE HARDWARE

iRMX System 320 with at least 2MB, random access memory, 140MB winchester disk, and tape drive.

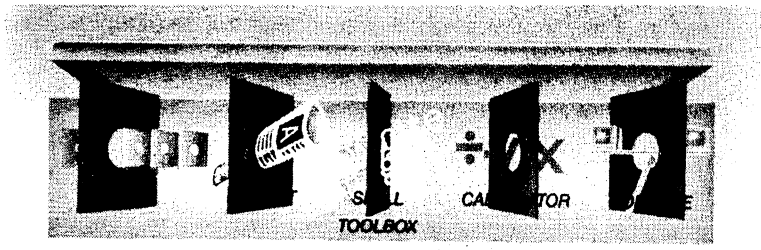
PREREQUISITE SOFTWARE

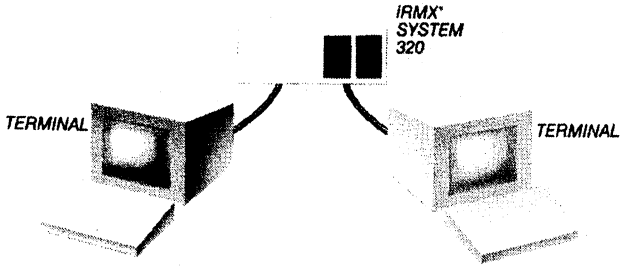
iRMX 286 R2.0 and AEDIT for single node system access. The above software prerequisite and iRMXNET R2.0 are required for networked utilization.

ORDER CODE

RMNSCSSU

iRMX® TOOLBOX





The iRMX toolbox is a set of utilities to provide assistance to the software developer in the housekeeping aspects of program development. These utilities offer facilities for text processing and document preparation.

Sort facilities and a desk calculator are also included.

FEATURES:

- Text formatting
- Spelling verification
- File comparisons
- Sort
- Floating point desk calculator
- Pocket reference guide

FEATURES

TEXT FORMATTING (SCRIPT)

The SCRIPT utility is a text formatting program that streamlines document formatting and preparation. Commands include facilities to do paging, centering, left and right margins, justification, subscripts, superscripts, page headers and footers, underlines, boldface type, upper and lower case, etc.

Input text which has been prepared using the AEDIT utility can be formatted using the SCRIPT utility and the output directed to a printer or stored on disk for future manipulation. A short tutorial example is provided to help the first time user of this formatter.

SPELLING VERIFICATION (SPELL, WSORT)

The SPELL utility finds misspelled words in a text file. The included dictionary can be expanded by the user for any additions as well as specialized vocabularies. This utility can be used interactively or in a batch mode. Another utility (WSORT) then can be used to sort and compress the user created dictionary.

FILE COMPARISONS (COMP)

The COMP utility performs line oriented text file comparisons showing changes between text or source files. This utility can also compare object files.

SORT (ESORT, HSORT)

Files can be sorted on multiple keys (or fields) in ascending or descending order and the resultant sorted files stored.

Another utility can be invoked to sort records or data in ASCII lexical order.

FLOATING POINT DESK CALCULATOR (DC)

The DC utility accepts lines of text as input. Each line containing an expression is parsed, evaluated and the result displayed on the console. Expressions can contain embedded assignment statements and single letter variables.

POCKET REFERENCE GUIDE

In addition to the User's Guide provided with iRMX Toolbox, a reference guide in small pocket format provides a handy reference to commands and functions.

SPECIFICATIONS

OPERATING ENVIRONMENT

iRMX 286 Operating System Release 2.0 or later running on an Intel Series 300 System or equivalent hardware with Numeric Data Processor (NDP) support and at least 1MB of memory. The AEDIT utility is required for use of the SCRIPT text formatting program.

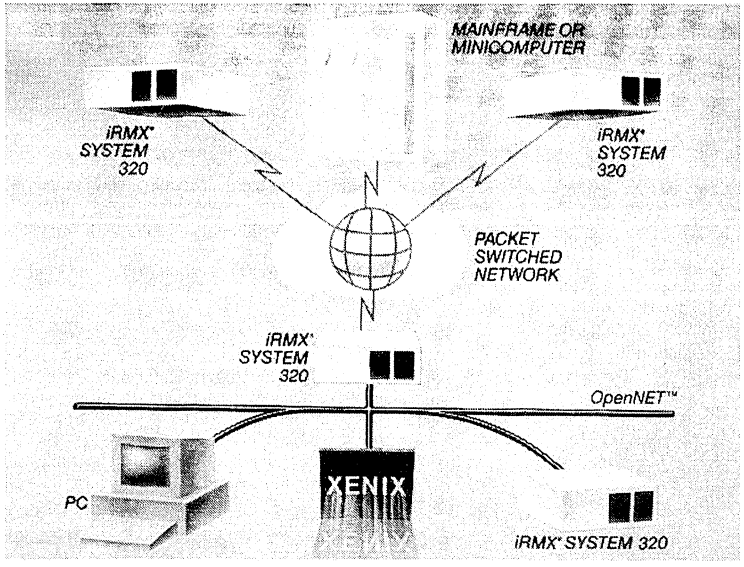
DOCUMENTATION

An iRMX 286 Toolbox User's Guide and Pocket Reference Guide are shipped with the product.

ORDERING INFORMATION

Product Code: RMX286TLB

The product is shipped on a 5¼" iRMX formatted floppy diskette.



iRMX® X.25 COMMUNICATIONS SOFTWARE

The iRMX X.25 Communications Software provides routines to connect an iRMX System 320 to a Packet Switch Network (PSN). The iRMX X.25 software allows connections of similar as well as dissimilar computer types that support the CCITT X.25 1980/1984 recommendation.

The iRMX X.25 software has been designed to allow the programmer the greatest flexibility in accessing packet-switch networks. In order to achieve this functionality, the programmer has access to a full-function programmatic interface. The design of iRMX X.25 allows not only host computer access as a Data Terminal Equipment (DTE) device, but in addition as a Data Circuit-terminating Equipment (DCE) device. The DCE configuration makes possible the programming of a complete packet-switch network service.

SOFTWARE FEATURES

- Application interface library
- Interactive utility package
- Conforms to CCITT X.25 1980
- User Selectable X.25 variants
- User Configurable
  - —Four physical links supported
  - —Software configurable Baud Rates
  - —Configurable as DTE/DCE
  - —255 Configurable Virtual Circuits (Permanent or Switched)

FEATURES

APPLICATION INTERFACE LIBRARY

Intel's software provides a three-level application interface library. Library routines are grouped into packet transfer services, network services, and management services. The user can choose the level of application interface which matches his X.25 experience. Those new to X.25 may prefer to start with network services routines, while proficient users will work directly with the packet transfer routines.

INTERACTIVE UTILITY PACKAGE

Several utility packages are included with the iRMX X.25 Communication Software that make it very approachable by the user. One of these tools is the User Confidence Test (UCT). The UCT has two modes of operation: a tutorial mode that demonstrates the use of the interface routines to help users quickly learn the calls to X.25; and, an interpreter mode that provides facilities to confirm the correct operation of iRMX X.25.

The UCT has been designed to assist users in testing X.25 applications. In addition to the UCT is CXTEST and CXPerform. Both of these utilities allow the user to gain more familiarity with X.25.

The product includes user documentation with detailed interface procedures, application examples with source code, and performance tools.

USER CONFIGURABLE

A configuration utility is provided to assist users in selecting the appropriate certification interface (see list under specification) for their X.25 network.

Once the user has selected their required network interface and specific parameters, the appropriate X.25 software routines are downloaded into the memory of the system's intelligent communication subsystem. This download capability allows the user application to run independently of the communications subsystem.

Under program control user may change the network configuration parameters. Some of these parameters are line baud rates (300 baud to 64K baud), packet size (maximum 1024 bytes supported) and retransmission limits.

The X.25 Communication Software can also be configured to support point-to-point interfaces via a serial link and a pair of modems.

SPECIFICATIONS

NETWORK CERTIFICATIONS

The products and services incorporating versions of X.25 have undergone extensive network certifications around the world.

A list of the countries where the software is known to have been successfully connected to the national network is given below:

Finland	Datapak	Yes
France	Transpac	N/A
Germany	Datex-P	*
Italy	Itapac	N/A
Netherlands	Datanet-1	*
South Africa	Saponet	Yes
Spain	Iberpac	N/A
Switzerland	Telepac	N/A
UK	PSS	Yes
USA	DDN	Yes
USA	GTE Telenet	Yes
USA	ATT Accunet	*

N/A—these PTTs have no formal approval procedure
*—is being certified

Many Packet switching networks are derivatives of early national implementations of the X.25 (1980) recommendation. The X.25 product is believed to be suitable for use on the following networks, based on these derivations:

Australia	Austpac
Belgium	DCS
Canada	Datapac
Denmark	Datapak
Ireland	Eirepac
Israel	Isranet
Luxembourg	Luxpac
Norway	Datapac
Portugal	Telepac
Singapore	Telepac

HARDWARE REQUIREMENTS:

System 320 with H4 Communications Option supports up to four (4) links (2 links full DMA, 2 links with transmit only DMA)

SOFTWARE PREREQUISITE:

iRMX 286 Release 2.0 or later

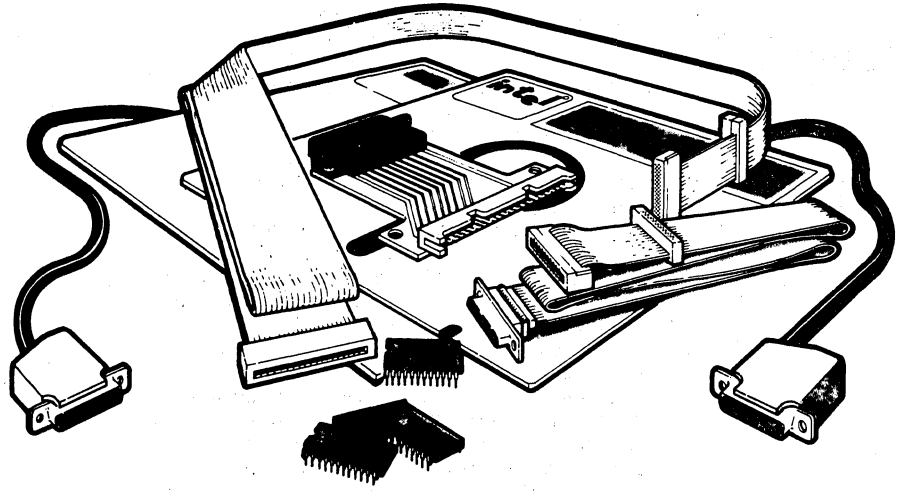
ORDER CODE:

System 320 Option HRX25SU (software)

iSDM™
SYSTEM DEBUG MONITOR

- **Supports Target System Debugging for iSBC® 8086, 8088, 80186, 80188, 80286 and 386™ CPU-Based Applications**
- **Provides Interactive Debugging Commands Including Single-Step Code Execution and Symbolic Displays of Results**
- **Supports 8087, 80287, and 80387 Numeric Processor Extensions (NPX) for High-Speed Math Applications**
- **Allows Building of Custom Commands Through the Command Extension Interface (CEI)**
- **Supports Application Access to ISIS-II Files**
- **Provides Program Load Capability from iSBC 8086, 80286 and 386 CPU-Based iRMX® I and II Development Systems and from an Intellec® Development System**
- **Contains Configuration Facilities which Allow an Applications Bootstrap from iRMX® File Compatible Peripherals**
- **Modular to Allow Use from an Intellec® Development System, from a Stand-Alone Terminal or from iRMX I or iRMX II Based Systems**

The Intel iSDM™ System Debug Monitor package contains the necessary hardware, software, cables, EPROMs and documentation required to interface, through a serial or parallel connection, an iSBC 86/05A, 86/12A, 86/14, 86/30, 86/35, 88/25, 88/40A, 88/45, 186/03A, 186/51, 188/48, 188/56, 286/10A, 286/12/14/16, 386/2X, 386/3X, 386/1XX or 8086, 8088, 80186 or 80188, 80286 and 386 CPU-based target system to a Series III, or Series IV Intellec® Microcomputer Development System or iRMX I or II Based System for execution and interactive debugging of applications software on the target system. The Monitor can: load programs into the target system; execute the programs instruction by instruction or at full speed; set breakpoints; and examine/modify CPU registers, memory content, and other crucial environmental details. Additional custom commands can be built using the Command Extension Interface (CEI). The Monitor supports the OEM's choice of the iRMX I Operating System, the iRMX II Operating System, or a custom system for the target application system. OEM's may utilize any iRMX supported target system peripheral for a bootstrap of the application system or have full access to the ISIS-II files of the Intellec System or the iRMX file system.



230882-1

October 1988
Order Number: 230882-005

FUNCTIONAL DESCRIPTION

Overview

The iSDM Monitor extends the software development capabilities of an iRMX or Intellec system so the user can effectively develop applications to ensure timely product availability.

The iSDM package consists of four parts:

- The loader program
- The iSDM Monitor
- The Command Extension Interface (CEI)
- The UDI Library Interface

The user can use the iSDM package to load programs into the target system from the development system, execute programs in an instruction-by-instruction manner, and add custom commands through the command extension interface. The user also has the option of using just the iSDM Monitor and the CEI in a stand-alone application, without the use of a development system.

Powerful Debugging Commands

The iSDM Monitor contains a powerful set of commands to support the debugging process. Some of the features included are: bootstrap of application software; selective execution of program modules based on breakpoints or single stepping requests; examination, modification and movement of memory contents; examination and modification of CPU registers, including NPX registers. All results are displayed in clearly understandable formats. Refer to Table 1 for a more detailed list of the iSDM monitor commands.

Numeric Data Processor Support

Arithmetic applications utilizing the 8087, 80287 or 80387 Numeric Processor Extension (NPX) are fully supported by the iSDM Monitor. In addition to executing applications with the full NPX performance, users may examine and modify the NPX's registers using decimal and real number format.

This feature allows the user to feel confident that correct and meaningful numbers are entered for the application without having to encode and decode complex real, integer, and BCD hexadecimal formats.

Command Extension Interface (CEI)

The Command Extension Interface (CEI) allows the addition of custom commands to the iSDM Monitor commands. The CEI consists of various procedures that can be used to generate custom commands. Up to three custom commands (or sets of commands) can be added to the monitor without programming new EPROMs or changing the monitor's source code.

Table 1. Monitor Commands

Command	Function
B	**Bootstrap** application program from target system peripheral device
C	**Compare** two memory blocks
D	**Display** contents of memory block
E*	**Exit** from loader program to iRMX or ISIS-II Interface
F	**Find** specified constant in a memory block
G	**Execute** application program
I	**Input** and display data obtained from input port
K	**Echo** console display to a file
L*	**Load** absolute object file into target system memory
M	**Move** contents of memory block to another location
N	**Display and execute** single instruction
O	**Output** data to output port
P	**Print** values of literals
R*	**Load and execute** absolute object file in target system memory
S	**Display and (optionally) modify** contents of memory
U, V, W	**User** defined custom commands extensions
X	**Examine and (optionally) modify** CPU and NPX registers
Y	**Display/Define** 80286 compiler symbol information

*Commands require an attached development system.

Universal Development Interface

The Universal Development interface (UDI) consists of libraries that contain interfaces to iRMX and ISIS II I/O calls. A program running on an 8086, 8088, 80186, 80188, 80286, or 386 CPU-based system can use UDI and access iRMX and ISIS II I/O calls. The interface allows the inclusion of these calls into the program; however, most of the calls require an iRMX or Intellec host system. Table 2 contains a summary of the major I/O calls.

Program Load Capability

The iSDM loader allows the loading of 8086, 8088, 80186, 80188, 80286 or 386 CPU-based programs into the target system. It executes on a development system and communicates with the target system through a serial or a parallel load interface.

Configuration Facility

The monitor contains a full set of configuration facilities which allows it to be carefully tailored to the requirements of the target system. Pre-configured EPROM-resident monitors are supplied by Intel for the iSBC 86/05A, 86/12A, 86/14, 86/30, 86/35, 88/25, 88/10A, 88/45, 186/03A, 186/51, 188/48, 188/56, 286/10A, 286/12/14/16, 386/2X/3X, and 386/1XX boards. The monitor must be configured by the user for other 8086, 8088, 80186, or 80188 applications. iRMX I and iRMX II system users may use the configuration facilities to include the Bootstrap Loader (V5.0 or newer) in the monitor.

Variety of Connections Available

The physical interface between the development system and the target system can be established in one of three ways. The systems can be connected via a serial link, a parallel link or a fast parallel link. The cabling arrangement is different depending upon the development system being used.

The iSDM Monitor does not require the use of a development system. The monitor can be used by simply attaching a stand-alone terminal to the target system.

Table 2. Routines for Services Available to Target System Applications

Routine	Target System Function
DQ$ATTACH	Creates a connection to a specified file.
DQ$CLOSE	Closes the specified file connection.
DQ$CREATE	Creates a file for use by the application.
DQ$DELETE	Deletes a file.
DQ$DETACH	Closes a file and deletes its connection.
DQGETCON-NECTION$STATUS	Returns status of a file connection.
DQ$OPEN	Opens a file for a particular type of access.
DQ$READ	Reads the next sequence of bytes from a file.
DQ$RENAME	Renames the specified file.
DQ$SEEK	Moves the current position pointer of a file.
DQ$SPECIAL	Defines options and actions for the program execution environment.
DQ$TRUNCATE	Truncates a file to the specified length.
DQ$WRITE	Writes a sequence of bytes to a file.

SPECIFICATIONS

Hardware

- Supported iSBC Microcomputers:
  - iSBC 86/05A Single Board Computer
  - iSBC 86/12A Single Board Computer
  - iSBC 86/14 Single Board Computer
  - iSBC 86/30 Single Board Computer
  - iSBC 86/35 Single Board Computer
  - iSBC 88/25 Single Board Computer
  - iSBC 88/40A Single Board Computer
  - iSBC 88/45 Single Board Computer
  - iSBC 186/03A Single Board Computer
  - iSBC 186/51 Single Board Computer
  - iSBC 188/48 Single Board Computer
  - iSBC 186/56 Single Board Computer
  - iSBC 286/10A Single Board Computer
  - iSBC 286/12/14/16 Single Board Computer
  - iSBC 386/2X/3X Single Board Computer
  - iSBC 386/1XX Single Board Computer
- Supported iSBX™ MULTIMODULE Boards:
  - iSBX 351 Serial I/O MULTIMODULE Board
  - iSBX 354 Serial I/O MULTIMODULE Board
- Supported Microcomputer Systems 8086/8088/80186/80188/80286/386/CPU 8087/80287/80387 NPX with Serial Controller: 8274 Serial Controller and 8253/8254 timer, or 8251A Serial Controller and 8253/8254 timer, or 82530 Serial Controller 4 KB RAM, and 32 KB EPROM

iSDM™ Package Contents

Cables:
- 4—RS232 Cable Assemblies (for iRMX/Intellec host system and standard terminals)
- Hardware package for the cable assemblies

Interface and Execution Software Diskettes:
- 2—DS/DD, iRMX-Format 5¼"
- 2—SS/DD, iRMX—Format 8"
- 2—SS/DD, ISIS II-Format 8"

System Monitor EPROMs:

Intel Board	EPROM Description
iSBC 86/05A iSBC 86/14 iSBC 86/30 iSBC 86/35	Two 27128 EPROMs
iSBC 86/12A	SUBMIT Files on the Release Diskette

System Monitor EPROMs: (Continued)

Intel Board	EPROM Description
iSBC 88/25	Two 27128 EPROMs
iSBC 88/40A	Two 27128 EPROMs
iSBC 88/45	Two 27128 EPROMs
iSBC 186/03A	Two 27128 EPROMs
iSBC 186/51	Two 27128 EPROMs
iSBC 188/48 iSBC 188/56	Two 27128 EPROMs
iSBC 286/10A iSBC 286/12/14/16	Two 27128 EPROMs
iSBC 386/2X/3X	Two 27256 EPROMs
iSBC 386/1XX	Two 27256 EPROMs

Reference Manual (Supplied):

iSDM System Debug Monitor Installation and Configuration

iSDM System Debug Monitor User's Guide

ORDERING INFORMATION

Part Number	Description
SDMSC	Object Software iRMX and Intellec host to target system interface and target system monitor, suitable for use on iSBC 86, 88, 186, 188, 286, 386 computers, or other 8086, 8088, 80186, 80188, 80286, 386 microcomputers. Package includes cables, EPROMs, software and reference manual. The OEM license option listed here allows use on a single host/target system and incorporation into their applications. Each incorporation requires payment of an Incorporation Fee. The iSDM package also includes 90 days of support services that include Software Program Report Services. As with all Intel Software, purchase of any of these options requires execution of a standard Intel Software License Agreement.
SDMRFX	Incorporation fee. Permits incorporation of a configured iSDM monitor into a target system.

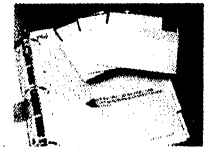
SOFT-SCOPE*II SOURCE-LEVEL DEBUGGER

SOURCE-LEVEL ON-TARGET DEBUGGER FOR iRMX® II APPLICATIONS

The Soft-Scope II Debugger is an interactive debugging tool specifically designed for software developed to execute with the iRMX II Operating Systems on Intel's broad set of system and board-level products. It reduces the time required to debug real-time software and allows the developer to debug at the most effective level, in the original source code itself.

FEATURES:

- Complete High-Level Debugging Functionality
- Source Code Interface and On-line Listings
- Automatic Expansion of Data Types
- Symbolic Display of iRMX II Objects
- Second Terminal Option for "Remote" Debugging
- Multitasking Support
- Handling of 80286/386™ Protection Traps and Software Exceptions



intel

September, 1988
Order Number: 280837-002

COMPLETE HIGH-LEVEL DEBUGGING

For real-time applications running with iRMX II Operating Systems on Intel 80286/386 CPU boards, software professionals want to focus on original source code for most debugging operations. Soft-Scope II does just that. It integrates the original source code into the debugging process directly. All breakpoint prompts and high-level stepping operations prompt with original source code rather than reporting what line number the program has reached or what assembly instruction is next.

SOURCE CODE INTERFACE AND ON-LINE LISTINGS

The source code interface frees the programmer from having to divide attention between the console and program listings, eliminates the need to get a fresh program listing each time a small change is made, and reduces the time needed to make software modifications.

AUTOMATIC EXPANSION OF DATA TYPES

Symbols declared in the program are accessible by name for display and modification of contents. These symbols include arrays, structures, static variables, based variables, and stack-based variables (including local variables, re-entrant variables, and passed parameters). Memory can also be displayed with absolute references or with register-relative references.

SYMBOLIC DISPLAY OF ALL IRMX II SYSTEM OBJECTS

The VIEW command allows viewing the status of any iRMX II object including tasks, jobs, mailboxes, semaphores, regions, and segments. With VIEW, the stack of a task can be examined to determine which iRMX II call the task has made most recently. Any job's object directory and the list of ready and sleeping tasks can be examined.

SECOND TERMINAL OPTION

Because so many applications today are screen-intensive, the Soft-Scope Debugger allows the option of using a second terminal for all debugger I/O, freeing the main console for exclusive use by the application for application output.

MULTI-TASKING SUPPORT

The Soft-Scope II Debugger supports simultaneous debugging of concurrent tasks when they are all linked together as a Human Interface command and each concurrent task is coded in a separate module. Soft-Scope loads and then allows the user to suspend and resume execution of the tasks from the command line with the SUSPEND and RESUME commands. In this way the developer can observe the effect of dynamic changes on the software under test.

HANDLING OF 80286/386 PROTECTION TRAPS AND SOFTWARE EXCEPTIONS

Exception Handling: The exact source line which causes an exception can easily be reached and displayed. All environmental and programmer exceptions are trapped and reported, without causing a Soft-Scope debugger exit.

Most of the 80286/386 hardware traps are handled by the Soft-Scope II Debugger, including Bounds Check (INT 5), Invalid Opcode (INT 6), Double Fault (INT 8), Stack Fault (INT 12), and General Protection (INT 13). Upon encountering one of these interrupts, the Soft-Scope II Debugger breaks execution with a message similar to the following:

```
< General Protection fault (INT 13) >?
[ Break near line #145 in TESTPROC (:TESTMODULE) ]
145: ARRAYX(INDEX) = XYZ;
```

In the above example, the General Protection trap could have been caused by the variable INDEX being too large for the segment which contained ARRAYX, or by ARRAYX being based on an undefined pointer. Because the debugger handles these traps directly, other users in a multi-user system won't even be aware in most cases that there was a hardware fault.

INTEL QUALITY—YOUR GUARANTEE

The Soft-Scope Debugger is built to the same exacting standards as Intel's component and board products. This product's reliability is been proven in many real-time product settings over the past several years.

WORLDWIDE SUPPORT AND SERVICE—AN INTEL STANDARD

Standard support products for the Soft-Scope Debugger are available through Intel's support organization.

SOFT-SCOPE II COMMANDS

Function	Commands
Invoking the Debugger	SSCOPE
Viewing the Source Code	LIST, LINE, FIND
Opening a Module	LINE, OPEN, MODULES, ASSIGN, DETACH
Controlling Execution	GO, STEP, ASTEP
Setting Breakpoints	GO, STEP, BREAKPOINT, RANGE
Examine Data/Descriptor	.variable, TYPE, EVAL, DUMP, STACK, ADDR
Examining Code	LINE, ASM
Port I/O	IN, OUT

Function	Commands
Debugger I/O	CONSOLE, ECHO
Examining Registers	REG, NPXREG
Requesting Help	HELP
Setting Options	OPTIONS
View iRMX II Objects	VIEW
Start/Stop Tasks	SUSPEND, RESUME
Execute a Submit File	SUBMIT
Run an RMX Program	RUN
Stack Trace	NEST
Initialize Stack	STACKINIT

SPECIFICATIONS

The Soft-Scope II Debugger supports the following languages:

Intel PL/M 286
Intel C 286
Intel Pascal 286
Intel ASM 286
Intel FORTRAN 286

The Soft-Scope Debugger requires a full configuration of the iRMX II Operating System, including the Human Interface and UDI. Either the iSDM System Debug Monitor or the D-MON monitor must be included in the firmware of the CPU board to use the VIEW command. The debugger utilizes approximately 130k bytes of memory beyond the load size of the program being debugged.

ORDERING INFORMATION

Product Code	Product Contents
RMXIISFTSCP	Soft-Scope II Debugger for iRMX II Operating Systems on 5¼" iRMX media diskettes

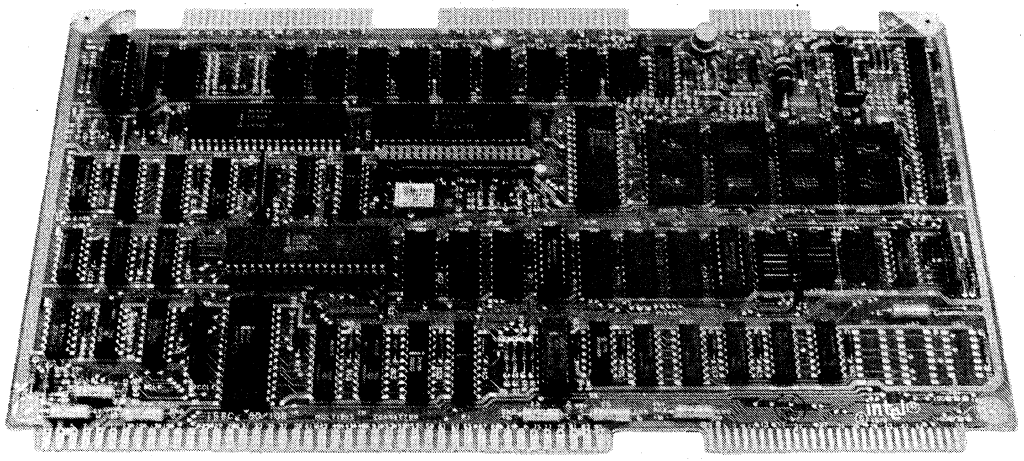
MULTIBUS® I
Single Board Computers

3

iSBC® 80/10B
SINGLE BOARD COMPUTER

- **8080A CPU Used as Central Processing Unit**
- **One iSBX™ Bus Connector for iSBX™ MULTIMODULE™ Board Expansion**
- **1K Byte of Read/Write Memory with Sockets for Expansion up to 4K Bytes**
- **Sockets for up to 16K Bytes of Read Only Memory**
- **48 Programmable Parallel I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **Programmable Synchronous/ Asynchronous Communications Interface with Selectable RS232C or Teletypewriter Compatiblity**
- **Single Level Interrupt with 11 Interrupt Sources**
- **Auxiliary Power Bus and Power-Fail Interrupt Control Logic for RAM Battery Backup**
- **1.04 Millisecond Interval Timer**
- **Limited Master MULTIBUS® Interface**

The Intel iSBC 80/10B board is a member of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/10B board is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, iSBX bus interface, read/write memory, read only memory sockets, I/O ports and drivers, serial communications interface, bus control logic, and drivers all reside on the board.



280217-1

September 1987
Order Number: 280217-002

FUNCTIONAL DESCRIPTION

Intel's powerful 8-bit n-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/10B board. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. A block diagram of iSBC 80/10B board functional components is shown in Figure 1.

iSBX™ Bus MULTIMODULE™ Board Expansion

The new iSBX bus interface brings an entirely new dimension to system design offering incremental on-board expansion with small iSBX boards. One iSBX bus connector interface is provided to accomplish plug-in expansion with any iSBX MULTIMODULE board. iSBX boards are available to provide expansion equivalent to the I/O available on the iSBC 80/10B board or the user may configure entirely new functionality such as math directly on-board. The iSBX 350 programmable I/O MULTIMODULE board provides 24 I/O lines using an 8255A programmable peripheral interface. Therefore, the iSBX 350 module together with the iSBC 80/10B board may offer 72 lines of programmable I/O. Alternately, a serial port may be added using the iSBX 351 serial I/O multimodule board or math may be configured on-board with the iSBX 332 floating point math MULTIMODULE board.

The iSBX board is a logical extension of the on-board programmable I/O and is accessed by the iSBC 80/10B single board computer as common I/O port locations. The iSBX board is coupled directly to the 8080A CPU and therefore becomes an integral element of the iSBC 80/10B single board computer providing optimum performance.

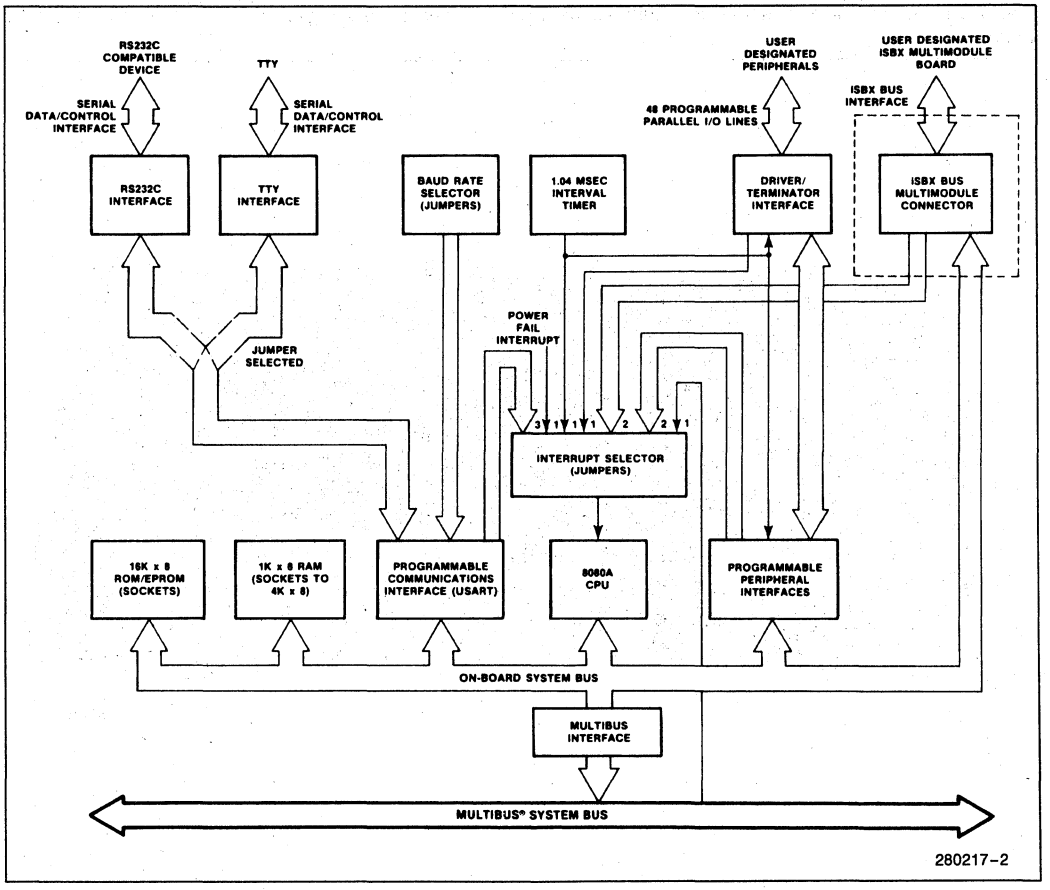


Figure 1. iSBC® 80/10B Single Board Computer Block Diagram

Memory Addressing

The 8080A has a 16-bit program counter which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Memory Capacity

The iSBC 80/10B board contains 1K bytes of read/write static memory. In addition, sockets for up to 4K bytes of RAM memory are provided on board. Read/write memory may be added in 1K byte increments using two 1K x 4 Intel 2114A-5 static RAMs. All on-board RAM read and write operations are performed at maximum processor speed. Sockets for up to 16K bytes of nonvolatile read-only-memory are provided on the board. Read-only-memory may be added in 1K byte increments up to 4K bytes (using Intel 2708 or 2758); in 2K byte increments up to 8K bytes (using Intel 2716); or in 4K byte increments up to 16K bytes (using Intel 2732). All on-board ROM or EPROM read operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/10B board contains 48 programmable parallel I/O lines implemented using two Intel 8255A programmable peripheral interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output, and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable or round cable.

Serial I/O Interface

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A jumper selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed

Table 1. Input/Output Port Modes of Operation

Port	Lines (Qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	8	X		X			X(1)
4	8	X		X			
5	8	X		X			
6	4	X		X			
	4	X		X			

NOTE:
1. Port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

by the system software to select the desired synchronous or asynchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format and parity are all under program control. The 8251A provides full duplex, double-buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of jumper selectable TTY or RS232C compatible interfaces on the board, in conjunction with the USART, provides a direct interface to teletypes, CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems. The RS232C or TTY command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable.

Interrupt Capability

Interrupt requests may originate from 11 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Three jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), a character is ready to be transmitted (i.e., the USART is ready to accept a character from the CPU), or when the transmitter is empty (i.e., the USART has no character to transmit). These five interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly to user designated peripheral devices; one via the MULTIBUS system bus and the other via the I/O edge connector. One jumper selectable interrupt request may be interfaced to the power-fail interrupt control logic. One jumper selectable interrupt request may originate from the interval timer. Two general purpose interrupt requests are jumper selectable from the iSBX interface. These two signals permit a user installed MULTIMODULE board to interrupt to 8080A CPU. The eleven interrupt request lines share a single CPU interrupt level. When an interrupt request is recognized, a restart instruction (RESTART 7) is generated. The processor responds by suspending program execution and executing a user defined interrupt service routine originating at location 38_{16}.

Power-Fail Control

A power-fail interrupt may be detected through the AC-low signal generated by the power supply. This signal may be configured to interrupt the 8080A CPU to initiate an orderly power down instruction sequence.

Interval Timer

A 1.04 millisecond timer is available for interval interrupts or as a clock output to the parallel I/O connector. The timer output is jumper selectable to the programmable parallel interface, the parallel I/O connector (J1), or directly to the 8080A CPU.

MULTIBUS® System Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS™ system compatible expansion boards. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. In addition, the iSBC 80/10B board performs as a limited bus master in that it must occupy the lowest priority when used with other MULTIBUS masters. The bus master may take control of the MULTIBUS system bus by halting the iSBC 80/10B board program execution. Mass storage capability may be achieved by adding single density diskette, double density diskette, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

SPECIFICATIONS

Word Size

Instruction: 8, 16, or 24 bits
Data: 8 bits

Cycle Time

Basic Instruction Cycle: 1.95 μs

NOTE:
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM
0–0FFF using 2708, 2758
0–1FFF using 2716
0–3FFF using 2732

On-Board RAM
3C00–3FFF with no RAM expansion
3000–3FFF with 2114A-5 expansion

NOTE:
All RAM configurations are automatically moved up to a base address of 4XXX when configuring EPROM for 2732.

Memory Capacity

On-Board ROM/EPROM
16K bytes (sockets only)

On-Board RAM
1K byte with user expansion in 1K increments to 4K byte using Intel 2114A-5 RAMs.

Off-Board Expansion
Up to 64K bytes using user specified combinations of RAM, ROM, and EPROM.

I/O Addressing

On-Board Programmable I/O

Device	I/O Address
8255 No. 1	
Port A	E4
Port B	E5
Port C	E6
Control	E7
8255 No. 2	
Port A	E8
Port B	E9
Port C	EA
Control	EB
8251A	
Data	EC
Control	ED
iSBX Multimodule	
MCS0	F0–F7
MCS1	F8–FF

Serial Baud Rates

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷16	÷64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
6.98	6980	—	110
4.8	4800	300	75

Connectors

Interface	Double-Sided Pins (Qty)	Centers (in.)	Mating Connectors
MULTIBUS System	86	0.156	Viking 2KH43/9AMK12 Wire-wrap
iSBX Bus	36	0.1	iSBX 960-5
Parallel I/O (2)	50	0.1	3M 3415-000 Flat
Serial I/O	26	0.1	AMP 87194-6 Flat

I/O Capacity

Parallel: 48 programmable lines

Serial: 1 transmit, 1 receive

MULTIMODULE: 1 iSBX Bus MULTIMODULE Board

Serial Communications Characteristics

Synchronous: 5–8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous: 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Interrupts

Single-level with on-board logic that automatically vectors the processor to location 38H using a restart instruction (RESTART 7). Interrupt requests may originate from user specified I/O (2); the programmable peripheral interface (2); the iSBX MULTIMODULE board (2); the programmable communications interface (3); the power fail interrupt (1); or the interval timer (1).

Interfaces

MULTIBUS: All signals TTL compatible

iSBX Bus: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Serial I/O: RS232C or a 20 mil current loop TTY interface (jumper selectable)

Interrupt Requests: All TTL compatible (active-low)

Clocks

System Clock: 2.048 MHz ±0.1%

Interval Timer: 1.042 ms ±0.1% (959.5 Hz)

Physical Characteristics

Width: 12.00 in (30.48 cm)

Height: 6.75 in. (17.15 cm)

Depth: 0.05 in. (1.27 cm)

Weight: 14 oz. (397.3 gm)

Electrical Characteristics

DC Power Requirements

Voltage	Without EPROM(1)	With 2708 EPROM(2)	With 2758, 2716, or 2732 EPROM(3)	Power Down Requirements (RAM and Support Circuit)
V_{CC} = +5V ±5%	I_{CC} = 2.0A(4)	3.1A	3.46A	84 mA + 140 mA/K (2114A-5)
V_{DD} = +12V ±5%	I_{DD} = 150 mA	400 mA	150 mA	Not Required
V_{BB} = −5V ±5%	I_{BB} = 2 mA	200 mA	2 mA	Not Required
V_{AA} = −12V ±5%	I_{AA} = 175 mA	175 mA	175 mA	Not Required

NOTES:

1. Does not include power required for optional ROM/EPROM, I/O drivers, or I/O terminators.
2. With four Intel 2708 EPROMS and 220Ω/330Ω for terminators, installed for 48 input lines. All terminator inputs low.
3. Same as #2 except with four 2758s, 2716s, or 2732s installed.
4. I_{CC} shown without RAM supply current. For 2114-5 add 140 mA per K byte to a maximum of 560 mA.

Line Drivers and Terminators

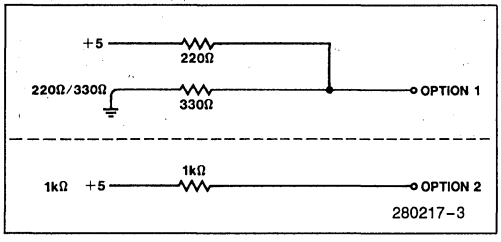
I/O Drivers: The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 80/10B Board:

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I—inverting, NI—non-inverting, OC—open collector.

Port 1 has 25 nA totem pole drivers and 1 kΩ terminators.

I/O Terminators: 220Ω/330Ω divider or 1 kΩ pull up.



MULTIBUS® Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	25
Address	Tri-State	25
Commands	Tri-State	25

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Equipment Supplied

iSBC 80/10B Single Board Computer
iSBC 80/10B Schematics

Reference Manual

9803119-01— iSBC 80/10B Single Board Computer Hardware Reference Manual (NOT SUPPLIED).

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

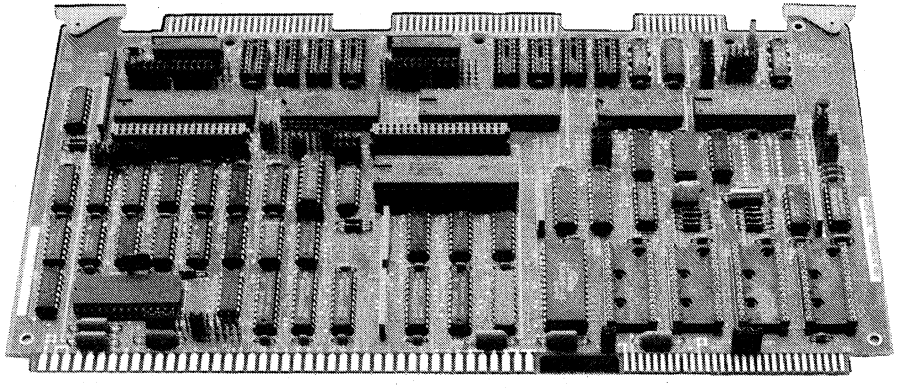
ORDERING INFORMATION

Part Number	Description
iSBC80/10B	Single Board Computer

iSBC® 80/24A
SINGLE BOARD COMPUTER

- **Upward Compatible Replacement for iSBC 80/20-4 Single Board Computer**
- **8085A-2 CPU Operating at 4.8 or 2.4 MHz**
- **Two iSBX™ Bus Connectors for iSBX MULTIMODULE™ Board Expansion**
- **8K Bytes of Static Read/Write Memory**
- **Sockets for Up to 32K Bytes of Read Only Memory**
- **48 Programmable Parallel I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rates**
- **Full MULTIBUS® Control Logic for Multimaster Configurations and System Expansion**
- **Two Programmable 16-Bit BCD or Binary Timers/Event Counters**
- **12 Levels of Programmable Interrupt Control**
- **Auxiliary Power Bus, Memory Protect, and Power-Fail Interrupt Control Logic Provided for Battery Backup RAM Requirements**

The Intel 80/24A Single Board Computer is a member of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's LSI technology to provide economical, self-contained computer-based solutions for OEM applications. The iSBC 80/24A board is a complete computer system on a single 6.7 × 12.00-inch printed circuit card. The CPU, system clock, iSBX bus interface, read/write memory, read only memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic, and programmable timers all reside on the board. Full MULTIBUS interface logic is included to offer compatibility with the Intel OEM Microcomputer Systems family of Single Board Computers, expansion memory options, digital and analog I/O expansion boards, and peripheral and communications controllers.



142927-1

September 1988
Order Number: 142927-004

FUNCTIONAL DESCRIPTION

Central Processing Unit

Intel's powerful 8-bit N-channel 8085A-2 CPU fabricated on a single LSI chip, is the central processor for the iSBC 80/24A board operating at either 4.8 or 2.4 MHz (jumper selectable). The 8085A-2 CPU is directly software compatible with the Intel 8080A CPU. The 8085A-2 contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing single and double precision operators. Minimum instruction execution time is 826 nanoseconds. A block diagram of the iSBC 80/24A functional components is shown in Figure 1.

MULTIMODULE™ Board Expansion

The iSBX bus interface brings designers incremental on-board expansion at minimal cost. Two iSBX bus MULTIMODULE connectors are provided for plug-in expansion of any iSBX MULTIMODULE board. The iSBX MULTIMODULE concept provides the ability to adapt quickly to new technology, the economy of buying only what is needed, and the ready availability of a spectrum of functions for greater application potential. iSBX boards are available to provide expansion equivalent to the I/O available on the iSBC 80/24A board or the user may configure entirely new functionality, such as math, directly on board.

The iSBX 350 Parallel I/O MULTIMODULE board provides 24 I/O lines using an 8255A Programmable Peripheral Interface. Therefore two iSBX 350 modules together with the iSBC 80/24A board may offer 96 lines of programmable I/O. Alternately, a serial port may be added using the iSBX 351 Serial I/O MULTIMODULE board.

Memory Addressing

The 8085A-2 has a 16-bit program counter which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

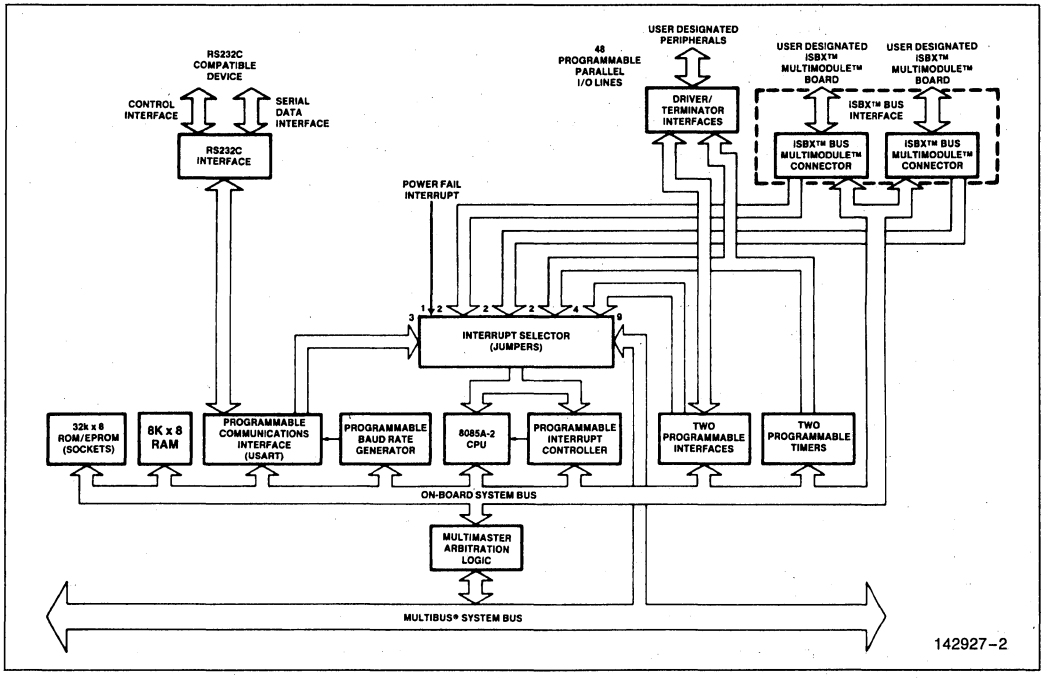


Figure 1. iSBC® 80/24A Single Board Computer Block Diagram

Memory Capacity

The iSBC 80/24A board contains 8K bytes of static read/write memory using an 8K × 8 SRAMs. All RAM read and write operations are performed at maximum processor speed. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements.

Four sockets are provided for up to 32K bytes of nonvolatile read only memory on the iSBC 80/24A board. EPROM may be added as shown with whiteout and 2732A.

Parallel I/O Interface

The iSBC 80/24A board contains 48 programmable parallel I/O lines implemented using two Intel 8255A Programmable Peripheral Interfaces. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports as indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, woven, or round cables.

Serial I/O Interface

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 80/24A board. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e. synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable.

Multimaster Capability

The iSBC 80/24A board is a full computer on a single board with resources capable of supporting a large variety of OEM system requirements. For

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

those applications requiring additional processing capacity and the benefits of multiprocessing (i.e. several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 80/24A board provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/24A boards or other bus masters to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the MULTIBUS system bus with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/24A board or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus since transfers via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design provides slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct memory access (DMA) operations, and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/24A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller, to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, or may be routed as inputs to the 8255A chip. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8254 provides the programmable baud rate generator for the RS232C USART serial port. In utilizing the iSBC 80/24A board, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occuring after the counting "window' has been enabled or an interrupt may be generated after N events occur in the system.

Interrupt Capability

The iSBC 80/24A board provides vectoring for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A-2 CPU and represent the four highest priority interrupts of the iSBC 80/24A board. Requests are routed to the 8085A-2 interrupt inputs—TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority), each of which generates a call instruction to

a unique address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5: 2CH). An 8085A-2 JMP instruction at each of these addresses then provides linkage to interrupt service routines located independently anywhere in memory. All interrupt inputs with the exception of the trap interrupt may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A-2 CPU. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, iSBX bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32 or 64-byte block may be located to begin at any 32 or 64-byte boundary in the 65,536-byte memory space. A single 8085A-2 JMP instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Autorotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Interrupt Request Generation

Interrupt requests may originiate from 23 sources. Two jumper selectable interrupt requests can be generated by each iSBX MULTIMODULE board. Two jumper selectable interrupt requests can be automatically generated by each programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Three jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receiver channel buffer is full), a character is ready to be transmitted (i.e., the USART is ready to accept a character from the CPU), or when the transmitter is empty (i.e., the USART has no character to transmit). A jumper selectable request can be generated by each of the programmable timers. Nine interrupt request lines are available to the user for direct interface to user designated peripheral devices via the MULTIBUS system bus. A power-fail signal can also be selected as an interrupt source.

Power-Fail Control

A power-fail interrupt may be detected through the AC-low signal generated by the power supply. This signal may be configured to interrupt the 8085A-2 CPU to initiate an orderly power down instruction sequence.

MULTIBUS® System Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS system compatible expansion boards. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette or hard disk controllers as subsystems. Expanded communication needs can be handled by communication controllers. Modular expandable backplanes and card cages are available to support multiboard systems.

SPECIFICATIONS

Word Size

Instruction— 8, 16 or 24 bits
Data — 8 bits

Cycle Time

BASIC INSTRUCTION CYCLE

826 ns (4.84 MHz operating frequency)
1.65 μs (2.42 MHz operating frequency)

NOTE:
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

ON-BOARD EPROM

0-0FFF using 2708, 2758 (1 wait state)
0-1FFF using 2716 (1 wait state)
0-3FFF using 2732 (1 wait state)
using 2732A (no wait states)
0-7FFF using 2764A (no wait states)

ON-BOARD RAM

E000-FFFF

NOTE:
Default configuration—may be reconfigured to top end of any 16K boundary.

Memory Capacity

ON-BOARD EPROM

32K bytes (sockets only)

May be added in 1K (using 2708 or 2758), 2K (using 2716), 4K (using Intel 2732A), or 8K (using Intel 2764A) byte increments.

ON-BOARD RAM

8K bytes

OFF-BOARD EXPANSION

Up to 64K bytes using user specified combinations of RAM, ROM, and EPROM.

Up to 128K bytes using bank select control via I/O port and 2 jumper options.

May be disabled using PROM ENABLE via I/O port and jumper option, resulting in off-board RAM overlay capability.

I/O Addressing

ON-BOARD PROGRAMMABLE I/O

Device	I/O Address
8255A No. 1	
Port A	E4
Port B	E5
Port C	E6
Control	E7
8255A No. 2	
Port A	E8
Port B	E9
Port C	EA
Control	EB
8251A	
Data	EC, EE
Control	ED, EF
iSBX MULTIMODULE J5	
MCS0	C0–C7
MCS1	C8–CF
iSBX MULTIMODULE J6	
MCS0	F0–F7
MCS1	F8–FF

I/O Capacity

Parallel — 48 programmable lines
Serial — 1 transmit, 1 receive, 1 SID, 1 SOD
iSBX MULTIMODULE— 2 iSBX MULTIMODULE Boards

Serial Communications Characteristics

Synchronous — 5–8 bit characters; internal or external character synchronization; automatic sync insertion

Asynchronous— 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detectors

Baud Rates

Output Frequency in kHz	Baud Rate (Hz)	
	Synchronous	Asynchronous
		÷16 ÷64
153.6	—	9600 2400
76.8	—	4800 1200
38.4	38400	2400 600
19.2	19200	1200 300
9.6	9600	600 150
4.8	4800	300 75
2.4	2400	150 —
1.76	1760	110 —

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Register Address (hex notation, I/O address space)

DE Baud rate register

NOTE:
Baud rate factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

Interrupts

Addresses for 8259A Registers (hex notation, I/O address space)

DA or D8 Interrupt request register
DA or D8 In-service register
DB or D9 Mask register
DA or D8 Command register
DB or D9 Block address register
DA or D8 Status (polling register)

NOTE:
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt levels routed to 8085A-2 CPU automatically vector the processor to unique memory locations:

Interrupt Input	Memory Address	Priority	Type
TRAP	24	Highest	Non-maskable
RST 7.5	3C	↓	Maskable
RST 6.5	34	↓	Maskable
RST 5.5	2c	Lowest	Maskable

Timers

Register Addresses (hex notation, I/O address space)

DF Control register
DC Timer 0
DD Timer 1
DE Timer 2

NOTE:
Timer counts loaded as two sequential output operations to same address as given.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.86 μs	60.948 ms	3.72 μs	1.109 hrs
Programmable One-Shot	1.86 μs	60.948 ms	3.72 μs	1.109 hrs
Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-Wave Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Software Triggered Strobe	1.86 μs	60.948 ms	3.72 μs	1.109 hrs
Hardware Triggered Strobe	1.86 μs	60.948 ms	3.72 μs	1.109 hrs

NOTE:
Input frequency to timers is 1.0752 MHz (default configuration).

Input Frequencies

Reference: 1.0752 MHz ±0.1% (0.930 μs period, nominal)

Event Rate: 1.1 MHz max

Interfaces

MULTIBUS — All signals TTL compatible
iSBX Bus — All signals TTL compatible
Parallel I/O — All signals TTL compatible
Serial I/O — RS232C compatible, configurable as a data set or data terminal
Timer — All signals TTL compatible
Interrupt Requests— All TTL compatible

System Clock (8085A-2 CPU)

4.84 or 2.42 MHz ±0.1% (jumper selectable)

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

I/O Driver— The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBC 80/24A Board:

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I = inverting; NI = non-inverting; OC = open collector.

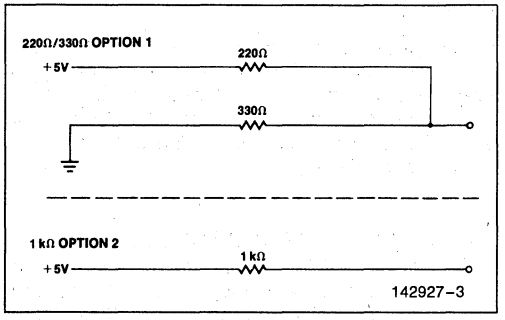
Ports E4 and E8 have 32 mA totem-pole drivers and 1K terminators.

I/O Terminators— 220Ω/330Ω divider of 1 kΩ pull-up.

Connectors

Interface	Double-Sided Pins (qty)	Centers (In.)	Mating Connectors*
MULTIBUS System Bus	86	0.156	ELFAB BS1562043PBB Viking 2KH43/9AMK12 Soldered PCB Mount EDAC 337086540201 ELFAB BW1562D43PBB EDAC 337086540202 ELFAB BW1562A43PBB Wire Wrap
Auxiliary Bus	60	0.100	EDAC 345060524802 ELFAB BS1020A30PBB EDAC 345060540201 ELFAB BW1020D30PBB Wire Wrap
Parallel I/O (2)	50	0.100	3M 3415-001 Flat Crimp GTE Sylvania 6AD01251A1DD Soldered
Serial I/O	26	0.100	AMP 15837151 EDAC 345026520202 PCB Soldered 3M 3462-0001 AMP 88373-5 Flat Crimp

***NOTE:**
Connectors compatible with those listed may also be used.



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Address	Tri-State	32
Commands	Tri-State	32

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 12.64 oz. (354 gm)

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements			
	$V_{CC} = +5V$ ±5% (max)	$V_{DD} = +12V$ ±5% (max)	$V_{BB} = -5V$ ±5% (max)	$V_{AA} = -12V$ ±5% (max)
Without EPROM(1)	2.66A	40 mA	—	20 mA
RAM Only(2)	0.01A	—	—	—
With iSBC 530(3)	2.66A	140 mA	—	120 mA
With 4K EPROM(4) (using 2708)	3.28A	300 mA	180 mA	20 mA
With 4K EPROM(4) (using 2758)	3.44A	40 mA	—	20 mA
With 8K EPROM(4) (using 2716)	3.44A	40 mA	—	20 mA
With 16K EPROM(4) (using 2732A)	3.46A	40 mA	—	20 mA
With 32K EPROM(4) (using 2764A)	3.42A	40 mA	—	20 mA

NOTES:
1. Does not include power for optional EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus.
3. Does not include power for optional EPROM, I/O drivers, I/O terminators. Power for iSBC 530 Adapter is supplied via serial port connector.
4. Includes power required for four EPROM chips, and I/O terminators installed for 16 I/O lines; all terminators inputs low.

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Reference Manual

148437-001— iSBC 80/24A Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

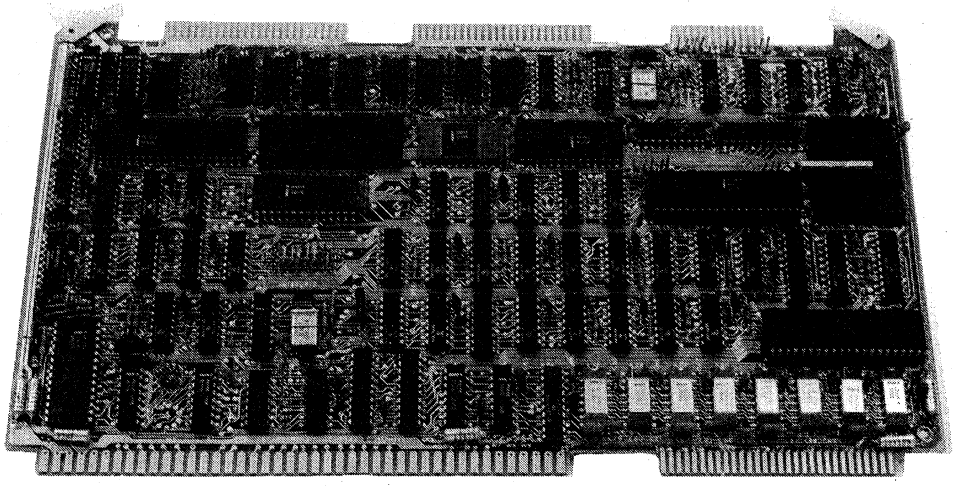
ORDERING INFORMATION

Part Number	Description
SBC 80/24A	Single Board Computer

iSBC® 80/30
SINGLE BOARD COMPUTER

- 8085A CPU Used as Central Processing Unit
- 16K Bytes of Dual Port Dynamic Read/Write Memory with On-Board Refresh
- Sockets for up to 8K Bytes of Read Only Memory
- Sockets for 8041A/8741A Universal Peripheral Interface and Interchangeable Line Drivers and Line Terminators
- 24 Programmable Parallel I/O Lines with Sockets for Interchangeable Line Drivers and Terminators
- Full MULTIBUS® Control Logic Allowing up to 16 Masters to Share the System
- Programmable Synchronous/Asynchronous RS232C Compatible Serial Interface with Fully Software Selectable Baud Rate Generation
- 12 Levels of Programmable Interrupt Control
- Two Programmable 16-Bit BCD or Binary Counters
- Auxiliary Power Bus, Memory Protect, and Power-Fail Interrupt Control Logic for RAM Battery Backup
- Compatible with Optional iSBC® 80 CPU, Memory, and I/O Expansion Boards

The iSBC 80/30 Single Board Computer is a member of Intel's complete line of OEM computer systems which take full advantage of Intel's LSI technology to provide economical self-contained computer-based solutions for OEM applications. The iSBC 80/30 is a complete computer system on a single 6.75 x 12.00-inch printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, universal peripheral interface capability, I/O ports and drivers, serial communications interface, priority interrupt logic, programmable timers, MULTIBUS control logic, and bus expansion drivers all reside on the board.



280219-1

September 1988
Order Number: 280219-002

FUNCTIONAL DESCRIPTION

Central Processing Unit

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/30. The 8085A CPU is directly software compatible with the Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. The minimum instruction execution time is 1.45 microseconds. The 8085A CPU has a 16-bit program counter. An external stack, located within any portion of iSBC 80/30 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this eternal stack. This stack provides subroutine nesting bounded only by memory size.

Bus Structure

The iSBC 80/30 has an internal bus for all on-board memory and I/O operations and a system bus (i.e., the MULTIBUS) for all external memory and I/O operations. Hence, local (on-board) operations do not tie up the system bus, and allow true parallel processing when several bus masters (i.e., DMA devices, other single board computers) are used in a multimaster scheme. A block diagram of the iSBC 80/30 functional components is shown in Figure 1.

RAM Capacity

The iSBC 80/30 contains 16K bytes of dynamic read/write memory using Intel 2117 RAMs. All RAM read and write operations are performed at maximum processor speed. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 80/30 contains a dual port controller, which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the iSBC 80/30 or from any other bus master interfaced via the MULTIBUS. Since on-board RAM accesses do not require the MULTIBUS, the bus is available for any other concurrent operations (e.g., DMA data transfers) requiring the use of the MULTIBUS. Dynamic RAM refresh is accomplished automatically by the iSBC 80/30 for accesses originating from either the CPU or via the MULTIBUS. Memory space assignment can be selected independently for on-board and MULTIBUS RAM accesses. The on-board RAM, as seen by the 8085A CPU, may be placed anywhere within the 0- to 64K-address space. The iSBC 80/30 provides extended addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the MULTIBUS. In addition, jumper options are provided which allow the user to reserve 8K- and 16K-byte segments of on-board RAM for use by the 8085A CPU only. This reserved RAM space is not accessible via the MULTIBUS and does not occupy any system address space.

EPROM/ROM Capacity

Sockets for up to 8K bytes of nonvolatile read only memory and provided on the iSBC 80/30 board. Read only memory may be added in 1 K-byte increments up to a maximum of 2 K-bytes using Intel 2708 or 2758 erasable and electrically reprogrammable ROMs (EPROMs); in 2 K-byte increments up to a maximum of 4 K-bytes using Intel 2716 EPROMs; or in 4 K-byte increments up to 8K-bytes maximum using Intel 2732 EPROMs. All on-board EPROM/ROM operations are performed at maximum processor speed.

Parallel I/O Interface

The iSBC 80/30 contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripharal Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable.

Universal Peripheral Interface (UPI)

The iSBC 80/30 provides sockets for a user supplied Intel 8041A/8741A Universal Peripheral Interface (UPI) chip and the associated line drivers and terminators for the UPI's I/O ports. The 8041A/8741A is a single chip microcomputer containing a CPU, 1K bytes of ROM (8041A) or EPROM (8741A), 64 bytes of RAM, 18 programmable I/O lines, and an 8-bit timer. Special interface registers included in the chip allow the 8041A to function as a

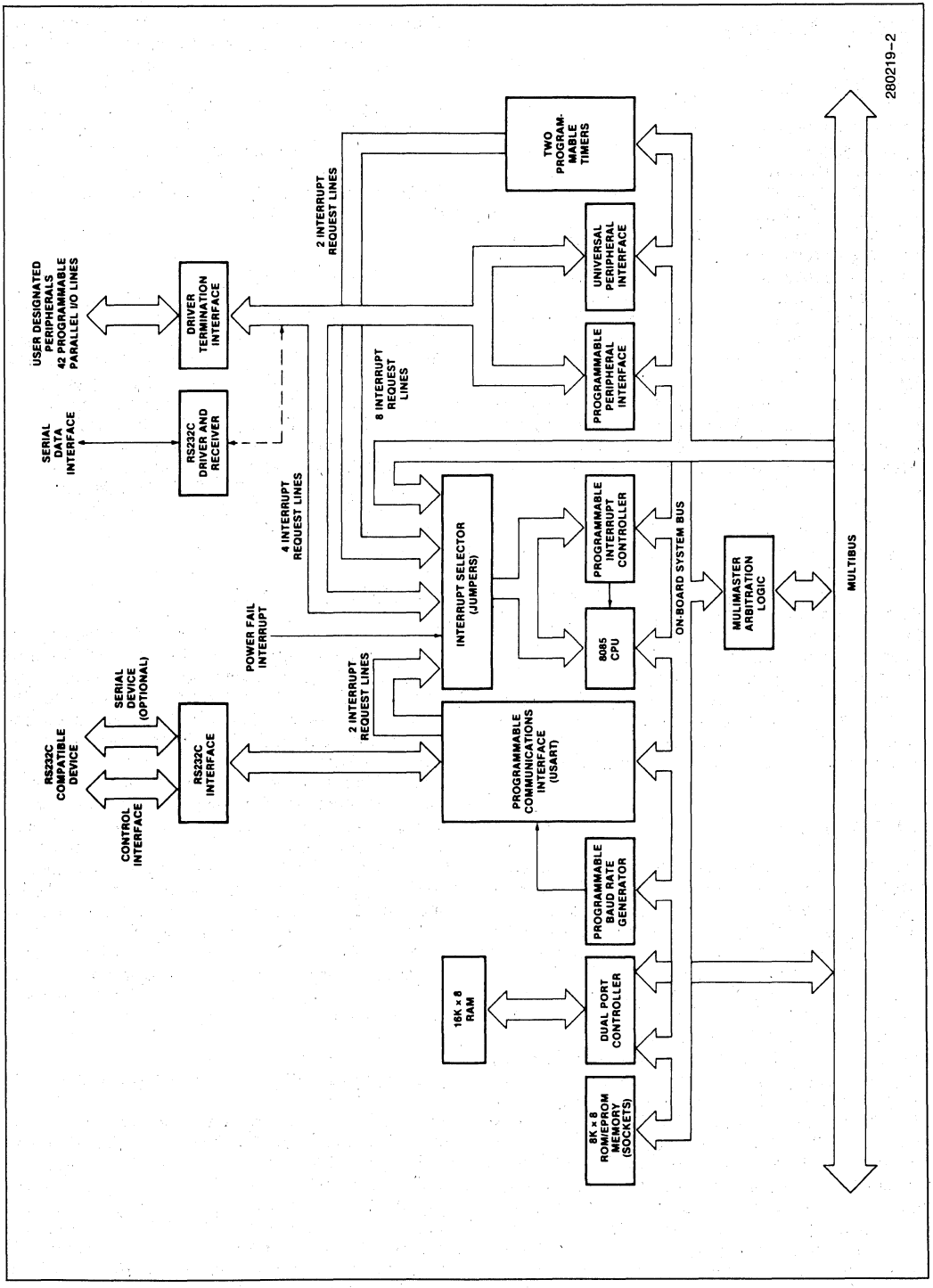


Figure 1. iSBC® 80/30 Single Board Computer Block Diagram

slave processor to the iSBC 80/30's 8085A CPU. The UPI allows the user to specifiy algorithms for controlling user peripherals directly in the chip, thereby relieving the 8085A for other system functions. The iSBC 80/30 provides an RS232C driver and an RS232C receiver for optional connection to the 8041A/8741A in applications where the UPI is programmed to handle simple serial interfaces. For additional information, including 8041A/8741A instructions, refer to the UPI-41A User's Manual and application note AP-41.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 80/30. A software selectable baud rate generator provides the USART with all common communication frequencies. The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM By-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground line are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cable.

Multimaster Capability

The iSBC 80/30 is a full computer on a single board with resources capable of supporting a great variety of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication over the system bus), the iSBC 80/30 provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 80/30's or other bus masters to share the system bus in serial (daisy chain) priority fashion, and up to 16 masters to share the MULTIBUS with the addition of an external priority network. The MULTIBUS arbitration logic operates synchronously with a MULTIBUS clock (provided by the iSBC 80/30 or optionally connected directly to the MULTIBUS clock) while data is transferred via a handshake between the master and slave modules. This allows different speed controllers to share resources on the same bus, and transfer via the bus proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. The most obvious applications for the master-slave capabilities of the bus are multiprocessor configurations, high speed direct memory access (DMA) operations, and high speed peripheral control, but are by no means limited to these three.

Programmable Timers

The iSBC 80/30 provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capabile of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Program-

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

mable Interrupt Controller, to the I/O line drivers associated with the 8255A Programmable Peripheral Interface, and to the 8041A/8741A Universal Programmable Interface, or may be routed as inputs to the 8255A and 8041A/8741A chips. The gate/trigger inputs may be routed to I/O terminators associated with the 8255A or as output connections from the 8255A. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 80/30 RS232C USART serial port. In utilizing the iSBC 80/30, the systems designer simply configures, via software, each timer independently to meet system requirements.

Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be read "on the fly".

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

Interrupt Capability

The iSBC 80/30 provides vectoring for 12 interrupt levels. Four of these levels are handled directly by the interrupt processing capability of the 8085A CPU and represent the four highest priority interrupts of the iSBC 80/30. Requests are routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5, and RST 5.5 (in decreasing order of priority) and each input generates a unique memory address (TRAP: 24H; RST 7.5: 3CH; RST 6.5: 34H; and RST 5.5: 2CH). An 8085A jump instruction at each of these addresses then provides linkage to interrupt service routines located independently anywhere in memory. All interrupt inputs with the exception of the trap interrupt may be masked via software. The trap interrupt should be used for conditions such as power-down sequences which require immediate attention by the 8085A CPU. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer for use in designing request processing configurations to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8085A jump instruction at each of these addresses then provides linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation—Interrupt requests may originate from 18 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when

a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive channel buffer is full), or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers and by the universal peripheral interface, eight additional interrupt request lines are available to the user for direct interface to user designated peripheral devices via the system bus, and two interrupt request lines may be jumper routed directly from peripherals via the parallel I/O driver/terminator section.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 Power Supply or equivalent.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added by using Intel MULTIBUS compatible expansion boards. High speed integer and floating point arithmetic capabilities may be added. Memory may be expanded to 65,536 bytes by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers as sub-systems. Modular expandable backplanes and cardcages are available to support multi-board systems.

SPECIFICATIONS

Word Size

Instruction: 8, 16, or 24 bits
Data: 8 bits

Cycle Time

Basic Instruction Cycle: 1.45 μs

NOTE:
Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM: 0-07FF (using 2708 or 2758 EPROMs); 0-0FFF (using 2716 EPROMs); 0-1FFF (using 2716 EPROMs; 0-1FFF (using 2732 EPROMs).

On-Board RAM: 16K bytes of dual port RAM starting on a 16K boundary. One or two 8 K-byte segments may be reserved for CPU use only.

Memory Capacity

On-Board Read Only Memory: 8K bytes (sockets only)
On-Board RAM: 16K bytes
Off-Board Expansion: Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM

NOTE:
Read only memory may be added in 1K, 2K, or 4K byte increments.

I/O Addressing

On-Board Programmable: I/O (see Table 1)

Port	8255A				8041A/8741A		USART	
	1	2	3	Control	Data	Control	Data	Control
Address	E8	E9	EA	EB	E4 or E6	E5 or E7	EC	ED

I/O Capacity

Parallel: 42 programmable lines using one 8255A (24 I/O lines) and an optional 8041A/8741A (18 I/O lines)

Serial: 2 programmable lines using one 8251A and an optional 8041A/8741A programmed for serial operation

NOTE:
For additional information on the 8041A/8741A refer to the UPI-41 User's Manual (Publication 9800504).

Serial Communications Characteristics

Synchronous: 5–8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous: 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2) .

Interrupts

Addresses for 8259A Registers (Hex notation, I/O address space)

DA Interrupt request register

DA In-service register

DB Mask register

DA Command register

DB Block address register

DA Status (polling register)

NOTE:
Several registers have the same physical address; sequence of access and one data bit of control word determine which register will respond.

Interrupt Levels routed to 8085A CPU automatically vector the processor to unique memory locations:

Interrupt Input	Memory Address	Priority	Type
TRAP	24	Highest	Non-maskable
RST 7.5	3C	↑	Maskable
RST 6.5	34	↓	Maskable
RST 5.5	2C	Lowest	Maskable

Timers

Register Addresses (Hex notation, I/O address space)

DF Control register

DC Timer 0

DD Timer 1

DE Timer 2

NOTE:
Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference: 2.46 MHz ±0.1% (0.041 μs period, nominal); 1.23 MHz ±0.1% (0.81 μs period, nominal); or 153.60 kHz ±0.1% (6.51 μs period nominal).

NOTE:
Above frequencies are user selectable

Event Rate: 2.46 MHz max

NOTE:
Maximum rate for external events in event counter function.

Interfaces

MULTIBUS: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Interrupt Requests: All TTL compatible

Timer: All signals TTL compatible

Serial I/O: RS232C compatible, data set configuration

System Clock (8085A CPU)

2.76 MHz ±0.1%

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 2KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000
Serial I/O	26	0.1	3M 3462-000

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

Line Drivers and Terminators

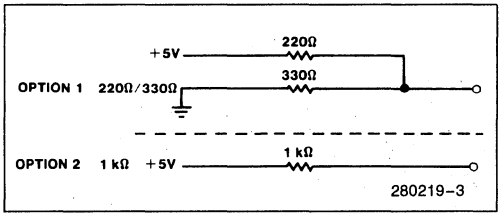
I/O Drivers: The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/30.

Driver	Characteristics	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I = inverting; NI = non-inverting; OC = open collector

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 kΩ terminators.

I/O Terminators: 220Ω/330Ω divider or 1 kΩ pullup



Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 18 oz. (509.6 gm)

Output Frequencies/Timing Intervals

Function	Single Timer/ Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63 μs	427.1 ms	3.26 μs	466.50 min
Programmable One-Shot	1.63 μs	427.1 ms	3.26 μs	466.50 min
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-Wave Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software Triggered Strobe	1.63 μs	427.1 ms	3.26 μs	466.50 min
Hardware Triggered Strobe	1.63 μs	427.1 ms	3.26 μs	466.50 min

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements			
	V_{CC} = +5V ±5% (max)	V_{DD} = +12V ±5% (max)	V_{BB} = −5V ±5% (max)	V_{AA} = −12V ±5% (max)
Without EPROM(1)	I_{CC} = 3.5A	I_{DD} = 220 mA	I_{BB} = −	I_{AA} = 50 mA
With 8041/8741(2)	3.6A	220 mA	—	50 mA
RAM only(3)	350 mA	20 mA	2.5 mA	—
With iSBC 530(4)	3.5A	320 mA	—	150 mA
With 2K EPROM(5) (using 8708)	4.4A	350 mA	95 mA	40 mA
With 2K EPROM(5) (using 2758)	4.6A	220 mA	—	50 mA
With 4K EPROM(5) (using 2716)	4.6A	220 mA	—	50 mA
With 8K EPROM(5) (using 2332)	4.6A	220 mA	—	50 mA

NOTES:
1. Does not include power required for optional EPROM/ROM, 8041A/8741A I/O drivers, and I/O terminators.
2. Does not include power required for optional EPROM/ROM. I/O drivers and I/O terminators.
3. RAM chips powered via auxiliary power bus.
4. Does not include power required for optional EPROM/ROM, 8041A/8741A I/O drivers, and I/O terminators. Power for iSBC 530 is supplied through the serial port connector.
5. Includes power reqiured for two EPROM/ROM chips, 8041A/8741A and 220Ω/330Ω input terminators installed for 34 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Reference Manual

9800611B— iSBC 80/30 Single Board Computer Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED. Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

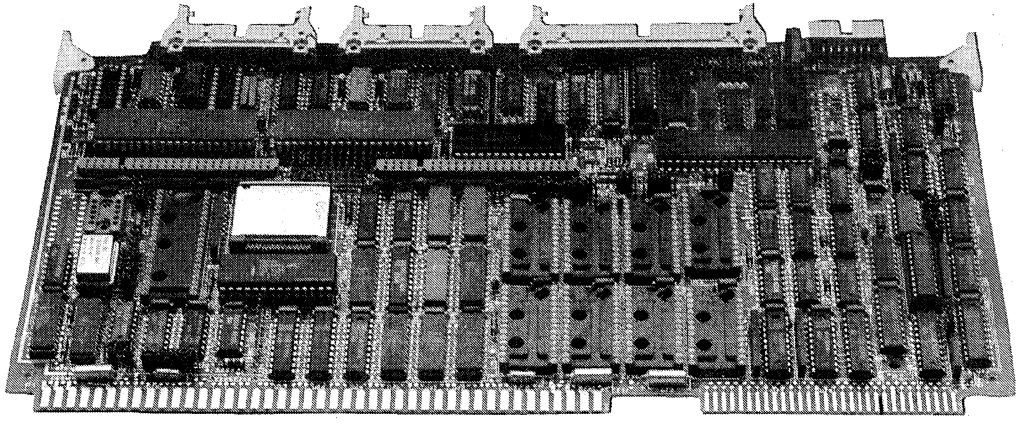
Part Number	Description
SBC 80/30	Single Board Computer with 16K bytes RAM

iSBC® 186/03A SINGLE BOARD COMPUTER

- **8.0 MHz 80186 Microprocessor with Optional 8087 Numeric Data Processor**
- **Eight (Expandable to 12) JEDEC 28-Pin Sites**
- **Six Programmable Timers and 27 Levels of Vectored Interrupt Control**
- **MULTIBUS® Interface for System Expansion and Multimaster Configuration**
- **24 Programmable I/O Lines Configurable as a SCSI Interface, Centronics Interface or General Purpose I/O**
- **Two iSBX™ Bus Interface Connectors for Low Cost I/O Expansion**
- **iLBX™ (Local Bus Extension) Interface for High-Speed Memory Expansion**
- **Two Programmable Serial Interfaces; One RS 232C, the Other RS 232C or RS 422 Compatible**

The iSBC 186/03A Single Board Computer is a member of Intel's complete line of microcomputer modules and systems that take advantage of Intel's VLSI technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete microcomputer system on a 7.05 x 12.0 inch printed circuit card. The CPU, system clock, memory, sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board.

The iSBC 186/03A board incorporates the 80186 CPU and SCSI interface on one board. The extensive use of high integration VLSI has produced a high-performance single-board system. For large memory applications, the iLBX local bus expansion maintains this high performance.



230988-1

September 1987
Order Number: 230988-005

OVERVIEW

Operating Environment

The iSBC 186/03A single board computer features have been designed to meet the needs of numerous microcomputer applications. Typical applications include:

- Multiprocessing single board computer
- BITBUS master controller
- Stand-alone singel board system

MULTIPROCESSING SINGLE BOARD COMPUTER

High-performance systems often need to divide system functions among multiple processors. A multiprocessing single board computer distributes an applications processing load over multiple processors that communicate over a system bus. Since these applications use the system bus for inter-processor communication, it is required that each processor has local execution memory.

The iSBC 186/03A board supports loosely coupled multiprocessing (where each processor performs a specific function) through its MULTIBUS compatible architecture. The IEEE 796 system bus facilitates processor to processor communication, while the iLBX bus makes high-speed data and execution memory available to each CPU as shown in Figure 1. This architecture allows multiple processors to run in parallel enabling very high-performance applications.

BITBUS™ MASTER CONTROLLER

The BITBUS interconnect environment is a high performance low-cost microcontroller interconnect technology for distributed control of intelligent industrial machines such as robots and process controllers. The BITBUS interconnect is a special purpose serial bus which is ideally suited for the fast transmission of short messages between the microcontroller nodes in a modularly distributed system.

The iSBC 186/03A board can be implemented as the MULTIBUS-based master controller CPU which monitors, processes and updates the control status of the distributed system. The iSBX 344 board is used to interface the iSBC 186/03A board to the BITBUS interconnect. Actual message transfer over the iSBX bus can be accomplished by either software polling by the CPU or by using the on-chip 80186 DMA hardware instead of the CPU. Using DMA, the CPU is only required to start the DMA process and then poll for the completion of the message transfer, thus dramatically improving the data transmission rate and master control processor efficiency. The maximum transfer rates over the iSBX bus for the iSBC 186/03A board are about 900 messages/second in polled mode and 2500 messages/second in DMA mode. An 8 MHz iSBC 186/03A board in DMA mode is 3 times as fast as a typical 5 MHz iSBC 86/30 board running in polled mode. The iSBC 186/03A board in DMA mode provides the highest performance/price solution for BITBUS message transmission out of all of Intel's complete line of 16-bit CPU modules.

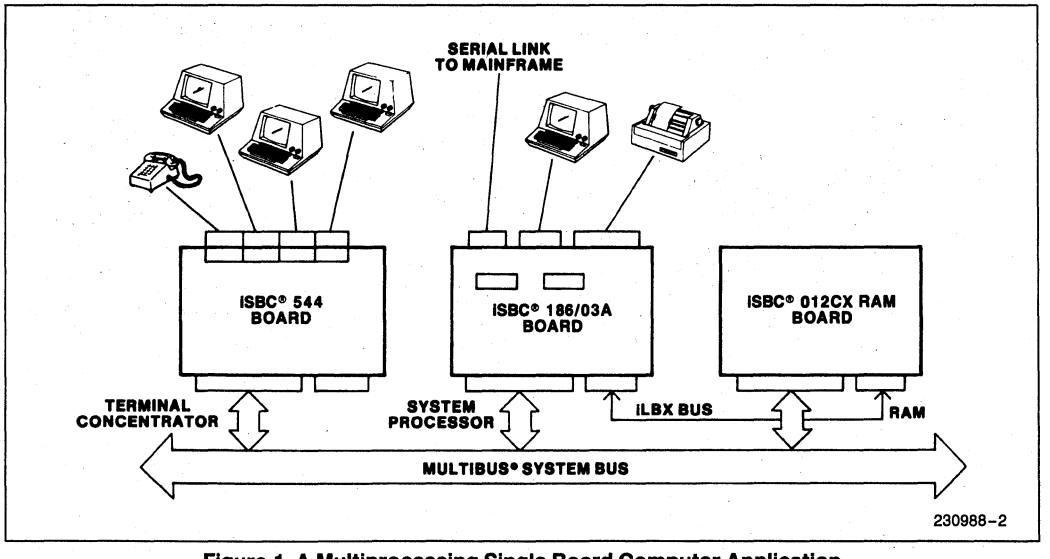


Figure 1. A Multiprocessing Single Board Computer Application

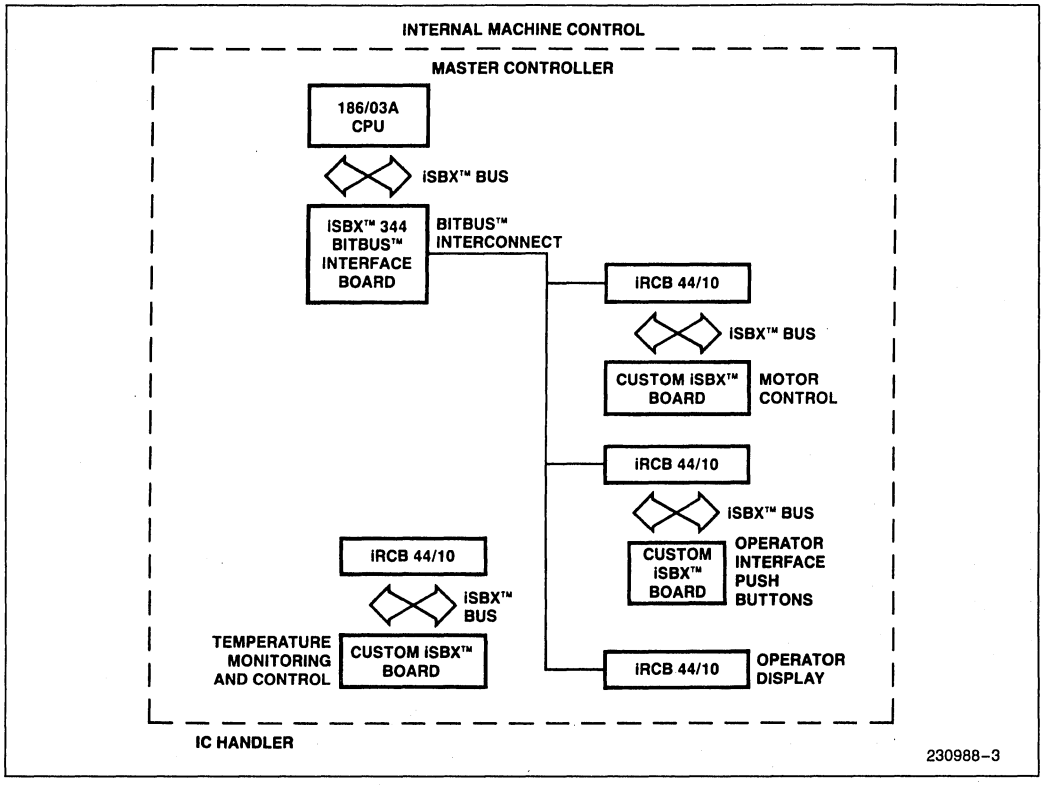


Figure 2. Sample iSBC® 186/03A BITBUS™ Master Application

STAND-ALONE SINGLE BOARD SYSTEM

A stand-alone single board system is a complete computer system on one board. By reducing the system's board count, the single board system saves space, power, and ultimately, costs. The on-board resources need to be capable of performing all of the basic system functions. These applications typically require terminal support, peripheral control, local RAM and program execution. In previous generations of single board computers, these functions could only be obtained with multiple board solutions.

The iSBC 186/03A board integrates all the functions of a general purpose system (CPU, memory, I/O and peripheral control) onto one board. The iSBC 186/03A board can also be customized as a single board system by the selection of memory and iSBX I/O options. The board's 8 JEDEC 28-pin sockets can accommodate a wide variety of byte-wide memory devices. For example, four 27256 EPROMS and four 2186 IRAMs can be installed for a total of 128 KB of EPROM program storage and 32 KB of RAM data storage. In addition, Intel's JEDEC site compatible 27916 KEPROM™ (Keyed Access EPROM) memory device may be configured for use on the iSBC 186/03A board. The KEPROM memory device employs a data protection mechanism which makes the memory array unreadable until unlocked by an authorized 64-bit "key". KEPROMs protect system software from unauthorized use. If more memory is needed, an optional iSBC 341 memory site expansion board can be added to provide an additional four JEDEC sites. Two iSBX MULTIMODULE™ boards can be added to the iSBC 186/03A board to customize the board's I/O capabilities. As shown in Figure 3, the iSBX connectors can support a single-board system with the analog input and output modules needed by machine or process control systems.

FUNCTIONAL DESCRIPTION

Architecture

The iSBC 186/03A board is functionally partitioned into six major sections: central processor, memory, SCSI compatible parallel interface, serial I/O, interrupt control and MULTIBUS bus expansion. These areas are illustrated in Figure 4.

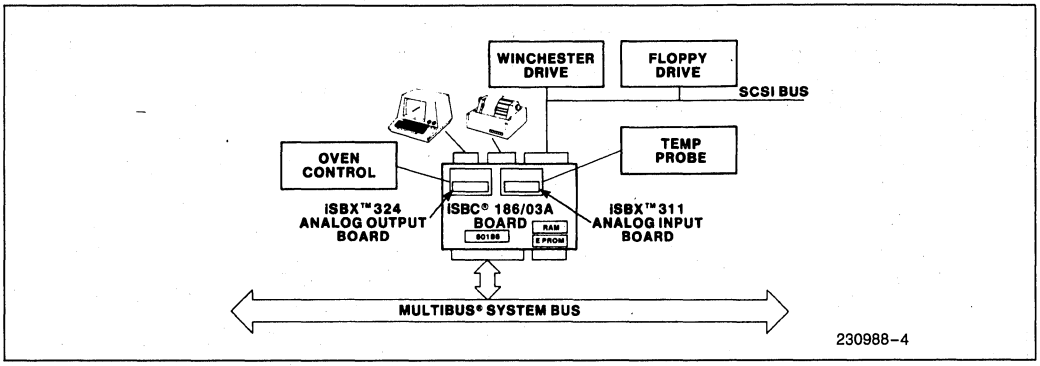


Figure 3. A Stand-Alone Single Board System Application

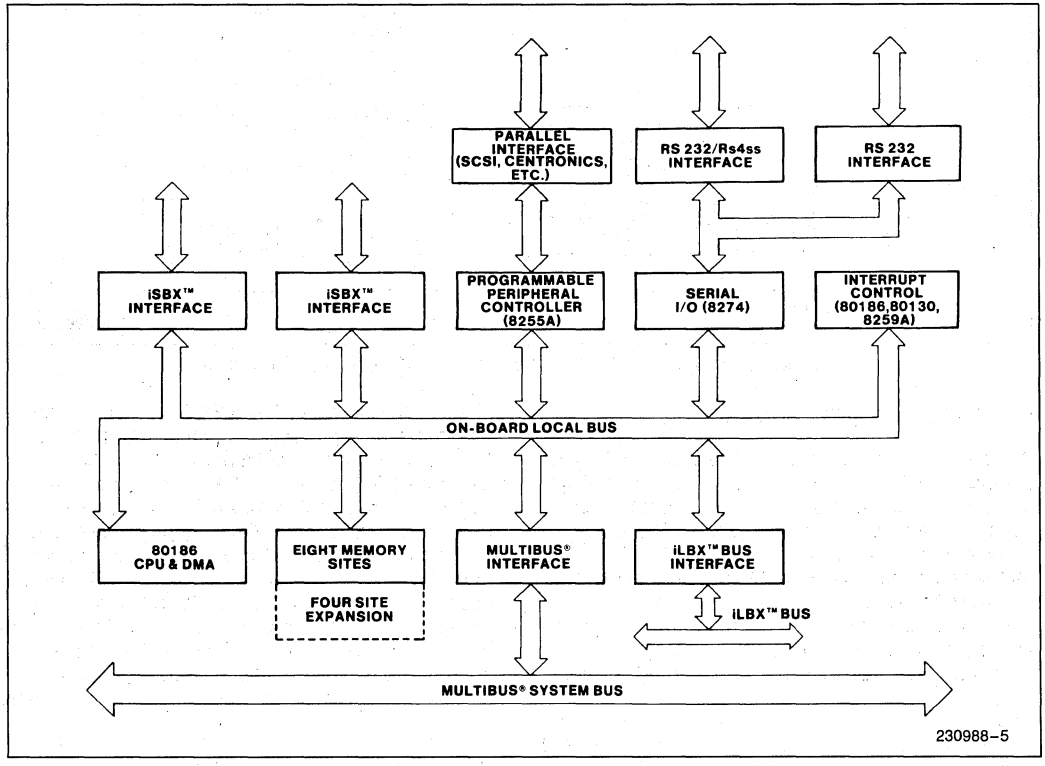


Figure 4. iSBC® 186/03A Board Block Diagram

CENTRAL PROCESSOR

The 80186 component is a high-integration 16-bit microprocessor. It combines several of the most common system components onto a single chip (i.e. Direct Memory Access, Interval Timers, Clock Generator and Programmable Interrupt Controller). The 80186 instruction set is a superset of the 8086. It maintains object code compatability while adding ten new instructions. Added instructions include: Block I/O, Enter and Leave subroutines, Push Immediate, Multiply Quick, Array Bounds Checking, Shift and Rotate by Immediate, and Pop and Push All.

Use of the 80130 component is limited to the 3 timers and 8 levels of interrupts available. Direct processor execution of the 16K bytes of iRMX 86 Operating System nucleus primitives is not supported.

An optional 8087 Numeric Data Processor may be installed by the user to dramatically improve the 186/03A board's numerical processing power. The interface between the 8087 and 80186 is provided by the factory-installed 82188 Integrated Bus Controller which completes the 80186 numeric data processing system. The 8087 Numeric Data Processor option adds 68 floating-point instructions and eight 80-bit floating point registers to the basic iSBC 186/03A board's programming capabilities. Depending on the application, the 8087 will increase the performance of floating point calculations by 50 to 100 times.

TIMERS

The 80186 provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (two per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. As shipped on the iSBC 186/03A board, these two timers are connected to the serial interface, and provide baud rate generation. The third timer is not connected to any external pins, and is useful for real-time coding and time-delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source. The 80130 provides three more programmable timers. One is a factory default baud rate generator and outputs an 8254 compatible square wave that can be used as an alternate baud rate source to either serial channel. The 80130's second timer is used as a system timer. The third timer is reserved for use by the iRMX Operating System. The system software configures each timer independently to select the desired function. Available functions include: interrupt on terminal count, programmable one-shot, rate generator, square-wave generator, software triggered strobe, hardware triggered strobe and event counter. The contents of each counter may be read at any time during system operation.

MEMORY

There are eight JEDEC 28-pin memory sites on the iSBC 186/03A board providing flexible memory expansion. Four of these sites (EPROM sites) may be used for EPROM or E^2PROM program storage, while the other four (RAM sites) may be used for static RAM or iRAM data storage or used as additional program storage. The eight sites can be extended to twelve by the addition of an iSBC 341 MULTIMODULE board. These additional sites will provide up to 64K bytes of RAM using 8K x 8 SRAM or iRAM devices. The EPROM sites (Bank B) are compatible with 8K x 8 (2764), 16K x 8 (27128A), 32K x 8 (27256), 64K x 8 (27512) as well as 2K x 8 (2817A) and 8K x 8 (2864) E^2PROMs. The RAM sites (Bank A) are compatible with all bytewide SRAM, iRAM or NVRAM devices. NVRAM usage requires additional circuitry in order to guarantee data retention. (Refer to AP-173 for further information.) Bank A can be reassigned to upper memory just below the assigned memory space for Bank B to support additional EPROM or E^2PROMs.

Memory addressing for the JEDEC sites depends on the device type selected. The four EPROM sites are top justified in the 1 MB address space and must contain the power-on instructions. The device size determines the starting address of these devices. The four RAM sites are, by default, located starting at address 0. The addressing of these sites may be relocated to upper memory (immediately below the EPROM site addresses) in applications where these sites will contain additional program storage. The optional iSBC 341 MULTIMODULE sites are addressable immediately above the RAM site addresses.

Power-fail control and auxiliary power are provided for protection of the RAM sites when used with static RAM devices. A memory protect signal is provided through an auxiliary connector (J4) which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

SCSI PERIPHERAL INTERFACE

The iSBC 186/03A board includes a parallel peripheral interface that consists of three 8-bit parallel ports. As shipped, these ports are configured for general purpose I/O. The parallel interface may be reconfigured to be compatible with the SCSI disk interface by adding two user-supplied and programmed Programmable Array Logic (PAL) devices, moving jumpers and installing a user-supplied 74LS640-1 device. Alternatively, the parallel interface may be reconfigured as a DMA controlled Centronics compatible line printer interface by adding one PAL and changing jumpers. Refer to the iSBC 186/03A Hardware Reference Manual for PAL equations and a detailed implementation procedure.

The SCSI (Small Computer Systems Interface) interface allows up to 8 mass storage peripherals such as Winchester disk drives, floppy disk drives and tape drives to be connected directly to the iSBC 186/03A board. Intel's iSBC 186/03A board utilizes a single initiator, single target implementation of the SCSI bus specification. Bus arbitration and deselect/reselect SCSI features are not supported. Single host, multiple target configurations can be used. However, the iSBC 186/03A board will stay connected to one target until the transaction is completed before switching to the second target. The iSBC 186/03A board's SCSI interface implements a 5 megabit/second transfer rate. A sample SCSI application is shown in Figure 5. Intel tested iSBC 186/03A board compatible SCSI controllers include Adaptek 4500, DTC 1410, Iomega Alpha 10, Shugart 1601 and 1610, Vermont Research 8103 and Xebec 1410.

The Centronics interface requires very little software overhead since a PAL device is used to provide necessary handshake timing. Interrupts are generated for printer fault conditions and a DMA request is issued for every character. The interface supports Centronics type printers compatible with models 702 and 737.

SERIAL I/O

The iSBC 186/03A Single Board Computer contains two programmable communications interfaces using the Intel 8274 Multi-Protocol Serial Controller (MPSC).

Two 80186 timer outputs are used as software selectable baud rate generators capable of supplying the serial channels with common communications frequencies. An 80130 baud rate timer may be jumpered to either serial port to provide higher frequency baud rates. The mode of operation (i.e., asynchronous, byte synchronous or bisynchronous protocols), data format, control character format, parity, and baud rate are all under program control. The 8274 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the MPSC. The iSBC 186/03A board supports operation in the polled, interrupt and DMA driven interfaces through jumper options. The default configuration is with channel A as RS422A/RS449, channel B as RS232C. Channel A can optionally be configured to support RS232C. Both channels are default configured as data set (DCE). Channel A can be reconfigured as data terminal (DTE) for connection to a modem-type device.

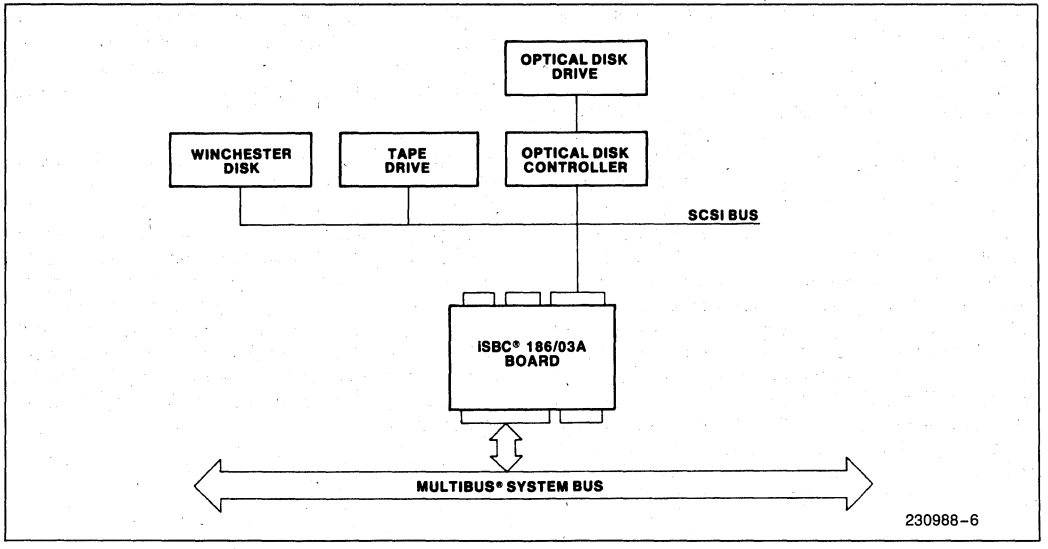


Figure 5. Sample SCSI Application

INTERRUPT CONTROL

The iSBC 186/03A board provides 27 on-board vectored interrupt levels to service interrupts generated from 33 possible sources.

The interrupts are serviced by four programmable interrupt controllers (PICs): one in the 80186 component, one in the 80130 component, one in the 8259A component and one in the 8274 component. The 80186, 8259A and 8274 PICs act as slaves to the 80130 master PIC. The highest priority interrupt is the Non-Maskable Interrupt (NMI) line which is tied directly to the 80186 CPU. This interrupt is typically used to signal catastrophic events (e.g. power failure). The PICs provide prioritization and vectoring for the other 26 interrupt requests from on-board I/O resources and from the MULTIBUS system bus. The PICs then resolve the requests according to the programmable priority resolution mode, and if appropriate, issue an interrupt to the CPU.

Table 1 contains a list of devices and functions capable of generating interrupts. These interrupt sources are jumper configurable to the desired interrupt request level.

Expansion

OVERVIEW

The iSBC 186/03A board architecture includes three bus structures: the MULTIBUS system bus, the iLBX local bus expansion and the iSBX MULTIMODULE expansion bus as shown in Figure 6. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The iLBX bus allows large amounts of high performance memory to be accessed by the iSBC 186/03A board over a private bus. The iSBX MULTIMODULE expansion board bus is a means of adding inexpensive I/O functions to the iSBC 186/03A board. Each of these bus structures are implemented on the iSBC 186/03A board providing a flexible system architecture solution.

MULTIBUS® SYSTEM BUS—IEEE 796

The MULTIBUS system bus is an industry standard (IEEE 796) microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 20 or 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations with multiple processors and intelligent slave, I/O and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board-level products, LSI interface components, detailed published specifications and application notes.

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Bus Interface INT0–INT7	Requests from MULTIBUS Bus Resident Peripherals or Other CPU	8
8274 Serial Controller	Transmit Buffer Empty, Receive Buffer Full and Channel Errors	8
Internal 80186 Timer and DMA	Timer 0, 1, 2, Outputs (Function Determined by Timer Mode) and 2 DMA Channel Interrupts	5
80130 Timer Output	iRMX System Timer (SYSTICK)	1
iSBX Bus Connectors	Function Determined by iSBX MULTIMODULE Board	6 (3 per iSBX Connector)
Bus Fail-Safe Timer	Indicates Addressed MULTIBUS Bus Resident Device Has Not Responded to Command within 10 ms	1
8255A Parallel I/O Controller	Parallel Port Control	2
J4 Connector	External/Power-Fail Interrupts	2

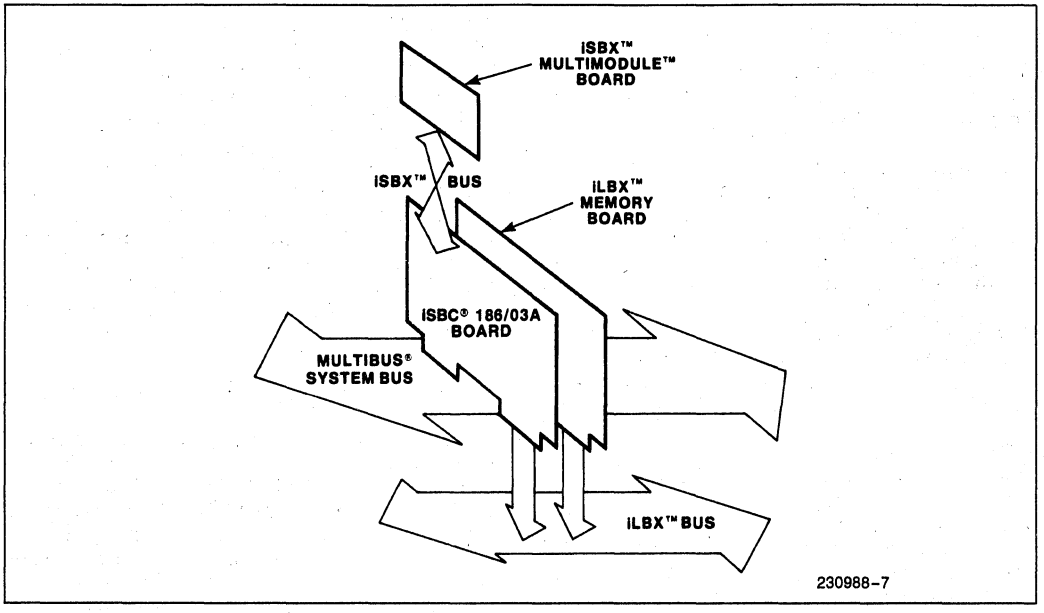


Figure 6. iSBC® 186/03A Board System Architecture

iLBX™ BUS—LOCAL BUS EXTENSION

The iSBC 186/03A board provides a local bus extension (iLBX) interface. This standard extension allows on-board memory performance with physically off-board memory. The combination of a CPU board and iLBX memory boards is architecturally equivalent to a single board computer and thus can be called a "virtual single board computer". The iLBX bus is implemented over the P2 connector and requires independent cabling or backplane connection.

iSBX™ BUS MULTIMODULE™ ON-BOARD EXPANSION

Two iSBX MULTIMODULE board connectors are provided on the iSBC 186/03A microcomputer board. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, and graphics control. The iSBX bus connectors on the iSBC 186/03A board provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 186/03A board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX bus modules may also be designed. An iSBX bus interface specification is available from Intel.

OPERATING SYSTEM SUPPORT

Intel's iRMX 86 Operating System is a highly functional operation system with a very rich set of features and options based on an object-oriented architecture. In addition to being modular and configurable, functions include a sophisticated file management and I/O system, and a powerful human interface. The iRMX 86 Release 6 Operating System can be used with the iSBC 186/03A board to generate application code for iRMX 86 based systems.

NOTE:
Intel does not support the direct processor execution of the 16K bytes of the iRMX 86 Operating System nucleus primitives from the 80130 component.

DEVELOPMENT ENVIRONMENT

Intel offers numerous tools to aid in the development of iSBC 186/03A board applications. These include on-target development, full development systems, in-circuit emulators and programming languages. Some of the features of each are described below.

Using the iRMX 86 Operating System, software development can be performed directly on the iSBC 186/03A board. This on-target development is the most economical way to develop iSBC 186/03A board based projects.

The development cycle of iSBC 186/03A board products can be significantly reduced and simplified by using either the System 86/3XX (iRMX 86-based) or the Intellec® Series Microcomputer Development Systems.

The Integrated Instrumentation In-Circuit Emulator (I^2ICE^{TM}) provides the necessary link between an Intellec development system and the "target" iSBC 186/03A execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 186/03A boards, the I^2ICE 186 emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

Intel has two systems implementation languages, PL/M 86 and C 86. Both are available for use on the iRMX 86 Operating System, on the System 86/3XX and on the Intellec Microcomputer Development System. PL/M 86 provides the capability to program in algorithmic language and eliminates the need to manage register usage or allocate memory while still allowing explicit control of the system's resources when needed. C 86 is especially appropriate in applications requiring portability and code density. FORTRAN 86, PASCAL 86, and BASIC 86 are also available on the iRMX 86 operating system, on the System 86/3XX and on the Intellec development system.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24 or 32 bits
Data—8 or 16 bits

System Clock

8.0 MHz

Numeric Data Processor (Optional)

8087-1

Basic Instruction Cycle Time

750 ns
250 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles plus instruction fetch). Zero wait-state memory is assumed.

MEMORY RESPONSE TIMES

Device Type	Max Access Time (from Chip Enable)	Min Cycle Time
EPROM Memory Sites		
0 Wait States	245 ns	318 ns
1 Wait State	370 ns	443 ns
RAM Memory Sites with SRAMs or EPROMs		
0 Wait States	197 ns	318 ns
1 Wait States	322 ns	443 ns
with 2186 IRAMs		
1 Wait State	261 ns	443 ns
2 Wait States	386 ns	568 ns

NOTE:
The number of wait states inserted is jumper selected depending on memory device specifications.

MEMORY CAPACITY/ADDRESSING

Four EPROM Sites		
Device	**Capacity**	**Address Range**
2764 EPROM	32 KB	$F8000_H$–$FFFFF_H$
27128 EPROM	64 KB	$F0000_H$–$FFFFF_H$
27256 EPROM	128 KB	$E0000_H$–$FFFFF_H$
27512 EPROM	256 KB	$C0000_H$–$FFFFF_H$
Four RAM Sites		
Device	**Capacity**	**Address Range**
2K SRAM	8 KB	0–$01FFF_H$
8K SRAM	32 KB	0–$07FFF_H$
32K SRAM	128 KB	0–$1FFFF_H$
2186 RAM	32 KB	0–$07FFF_H$
2817A E²PROM	8 KB	$F0000_H$–$F7FFF_H$*
2764 EPROM	32 KB	$F0000_H$–$F7FFF_H$ (below EPROM Sites)
27128 EPROM	64 KB	$E0000_H$–$EFFFF_H$ (below EPROM Sites)
27256 EPROM	128 KB	$C0000_H$–$DFFFF_H$ (below EPROM Sites)
Four iSBC® 341 Expansion Sites		
Device	**Capacity**	**Address Range**
2K SRAM	8 KB	02000_H–$03FFF_H$
8K SRAM	32 KB	08000_H–$0FFFF_H$
32K SRAM	128 KB	10000_H–$1FFFF_H$
2186 RAM	32 KB	08000_H–$0FFFF_H$
2817A E²PROM	8 KB	02000_H–$03FFF_H$**

NOTE:
All on board memory is local to the CPU (i.e. not dual-ported).

*Must use 8k x 8 decode option, there are four copies of the E²PROM in the 8K x 8 address area.

**(May be mixed with 2K x 8 SRAM)

Serial Communications Characteristics

Synchronous— 5–8 bit characters, internal or external character synchronization; automatic sync insertion; break character generation

Asynchronous— 5–8 bit characters; 1, ½, or 2 stop bit; false start bit detection.

Common Baud Rates

Using 80186 Timers:	Using 80130 Timer:
500K	750K
125K	500K
64K	125K
48K	64K
19.2K	48K
9600	19.2K
4800	9600
2400	4800
1200	2400
600	1200
300	600
150	300
110*	150
75*	110*
	75*

*Asynchronous use only

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register of 80186 or 80130 timers.

Timer Input Frequency

80186 Reference: 2.0 MHz ±0.1%
80130 Reference: 8.0 MHz ±0.1%

Interface Compliance

MULTIBUS— IEEE 796 compliance: Master D16 M24 116 VO EL

iSBX Bus— Two 8/16 bit iSBX bus connectors allow use of up to 2 single-wide modules or 1 single-wide and 1 double-wide module. Intel iSBX bus compliance: D16/16 DMA

iLBX— Intel iLBX bus compliance: PM D16

Serial— Channel A: Configurable as RS 422A or RS 232C compatible, configurable as a data set or data terminal

Channel B: RS 232C compatible, configured as data set

Parallel I/O— SCSI (ANSI—X3T9, 2/82-s) compatible or Centronics 702 or 737 compatible (requires user supplied PALs and 74LS640-1)

CONNECTORS

Interface	Double-sided Pins	Mating Connectors
MULTIBUS System	86 (P1)	Viking 3KH43/9AMK12 Wire Wrap
	60 (P2)	Viking 3KH30/9JNK
iSBX Bus 8-Bit Data	36	Viking 000292-0001
16-Bit Data	44	Viking 000293-0001
Serial I/O	26	3M 3452-0001 Flat AMP88106-1 Flat
iLBX Bus	60	Kelam RF30-2853-542
Parallel Interface	50	3M 3425-6000 3M 3425-6050 w/strain Ansley 609-5001M

ORDERING INFORMATION

Part Number	Description
SBC 186/03A	186-based single board computer

REFERENCE MANUAL

iSBC® 186/03A Single Board Computer Hardware Reference Manual—Order Number 148060

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Length: 7.05 in (17.90 cm)
Height: 0.50 in. (1.78 cm)
Weight: 13 ounces

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 60°C at 6 CFM airflow over the board.

Relative Humidity: to 90% (without condensation)

ELECTRICAL CHARACTERISTICS

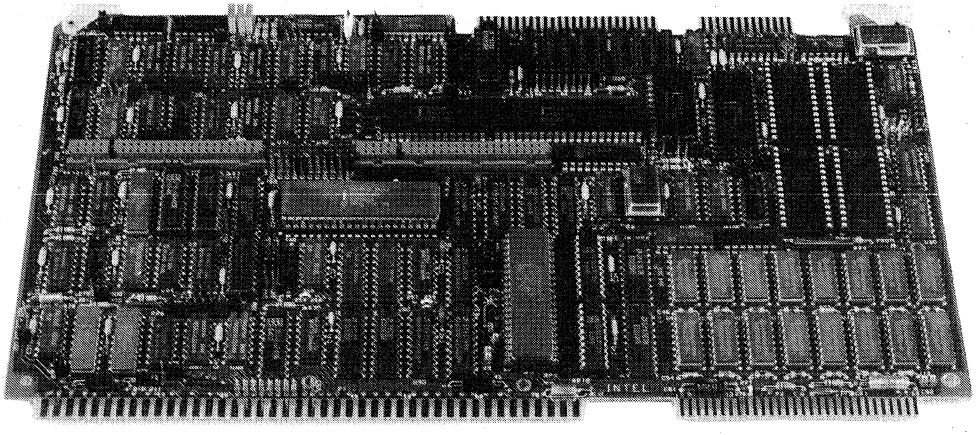
The maximum power required per voltage is shown below. These numbers do not include the power required by the optional memory devices, SCSI PALs, battery back-up or expansion modules.

Voltage (volts)	Max. Current (amps)	Max Power (watts)
+5	5.4	27
+12	0.04	0.48
−12	0.04	0.48

iSBC® 86/35
SINGLE BOARD COMPUTER

- **8086 (8086-2) Microprocessor with 5 or 8 MHz CPU Clock**
- **Optional 8086 Numeric Data Processor with iSBC® 337A MULTIMODULE™ Processor**
- **Upward Compatible with iSBC 86/30 Single Board Computer**
- **512K Bytes of Dual-Port Read/Write Memory Expandable On-Board to 640K or 1M Bytes**
- **Sockets for up to 128K Bytes of JEDEC 24/28-Pin Standard Memory Devices**
- **Two iSBX™ Bus Connectors**
- **24 Programmable Parallel I/O Lines**
- **Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rates**
- **Three Programmable 16-Bit BCD or Binary Timers/Event Counters**
- **9 Levels of Vectored Interrupt Control, Expandable Off Board to 65 Levels**
- **MULTIBUS® Interface for Multimaster Configurations and System Expansion**
- **Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral Controllers, Packaging and Software**

The iSBC 86/35 Single Board Computer is a member of Intel's complete line of OEM microcomputer systems that take full advantage of Intel's technology to provide economical, self-contained, computer-based solutions for OEM applications. The board is a complete computer system containing the CPU, system clock, dual port read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all on a single 6.75 x 12.00 in. printed circuit card. The iSBC 86/35 board is distinguished by its large RAM content of 512K bytes which is expandable on-board to 1 megabyte; the direct addressing capability of the 8086-2 CPU. The large, on-board memory resource combined with the 8086 microprocessor provides high-level system performance ideal for applications, such as robotics, process control, medical instrumentation, office systems, and business data processing.



210219-1

September 1987
Order Number: 210219-004

FUNCTIONAL DESCRIPTION

Overview

The iSBC 86/35 board combines the power of the industry standard 8086 CPU with up to a megabyte page of board resident, dual ported system memory to improve the system's overall performance. By placing the direct memory addressing capability of the iAPX 86/10 CPU on board, MULTIBUS® access to system memory can be eliminated, significantly improving system throughput. Intel's incorporation of 256K bit DRAM technology, parallel and serial I/O, iSBX™ connectors, and interrupt control capabilities make this high performance single board computer system a reality.

Central Processing Unit

The central processor for the iSBC 86/35 board is Intel's iAPX 86/10 (8086-2) CPU. A clock rate of 8 MHz is supported with a jumper selectable option for 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit index registers, all accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages as well as assembly language.

Instruction Set

The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced 5 or 8 MHz numerics processing capability, the iSBC 337A MULTIMODULE Numeric Data Processor extends the iAPX 86/10 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

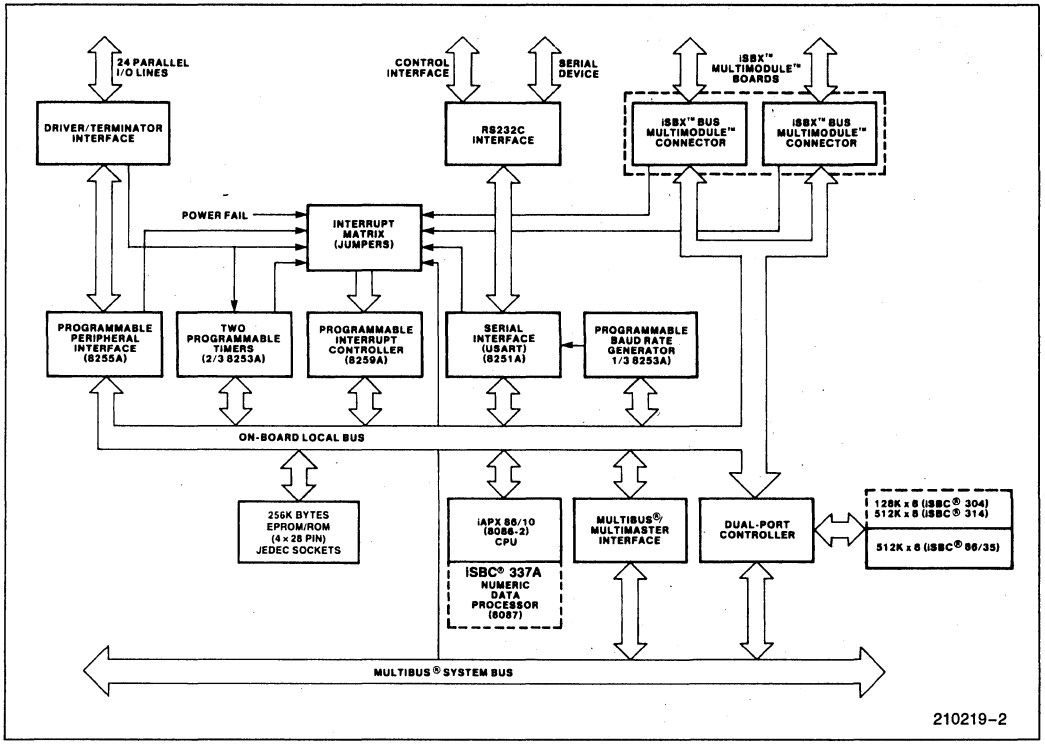


Figure 1. iSBC® 86/35 Block Diagram

Architectural Features

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 750 ns minimum instruction cycle to 250 ns for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, inter-modular communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

RAM Capabilities

The iSBC 86/35 microcomputer contains 512K bytes of dual-port dynamic RAM which may be expanded on-board by adding a RAM Multimodule board as an option. The on-board RAM may be expanded to 640K bytes with the iSBC 304 MULTIMODULE board mounted onto the iSBC 85/35 board. Likewise, the iSBC 86/35 microcomputer may be expanded to 1 Megabyte with the iSBC 314 MULTIMODULE board option.

The dual-port controller allows access to the on-board RAM (including RAM MULTIMODULE board options) from the iSBC 86/35 board and from any other MULTIBUS master via the system bus. Segments of on-board RAM may be configured as a private resource, protected from MULTIBUS system access.

EPROM Capabilities

Four 28-pin JEDEC sockets are provided for the use of Intel 2764, 27128, 27256, 27512, EPROMs and their respective ROMs. When using 27512, the on-board EPROM capacity is 256K bytes. Other JEDEC standard pinout devices are also supported, including byte-wide static RAMs.

Parallel I/O Interface

The iSBC 86/35 Single Board Computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 86/35 board. A software selectable baud rate generator provides the USART with all common communication frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector.

Programmable Timers

The iSBC 86/35 board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate timer intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 86/35 board's RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 86/35 microcomputer. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks),

and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 86/35 board provides all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 86/35 microcomputer. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 86/35 board. An iSBX bus interface specification and iSBX connectors are available from Intel.

MULTIBUS® SYSTEM BUS CAPABILITIES

Overview

The MULTIBUS system bus is Intel's industry standard (IEEE 796) microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes. Please refer to the MULTIBUS Handbook (order number 210883) for more detailed information.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e. several CPUs and/or controllers logically sharing system tasks through communication on the system bus), the iSBC 86/35 board provides full MULTIBUS arbitration control logic. This control logic allows both serial (daisy chain) and parallel priority schemes. The serial scheme allows up to three iSBC 86/35 boards/bus masters to share the MULTIBUS system bus; while up to 16 masters may be connected using the parallel scheme and external decode logic.

Interrupt Capability

The iSBC 86/35 board provides 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8086-2 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Intel 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Table 3. Programmable Interrupt Masks

Mode	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Interrupt Request Generation

Interrupt requests to be serviced by the iSBC 86/35 board may originate from 28 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is included to accept a power-fail interrupt in conjunction with the AC-low signal from the Power Supply to initiate an orderly shut down of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS® interface	Requests from MULTIBUS® resident peripherals or other CPU boards	8; may be expanded to 64 with slave 8259A PICs on MULTIBUS® boards
8255A Programmable Peripheral Interface	Signals input buffer full or output buffer empty; also BUS INTR OUT general purpose interrupt from driver/terminator sockets	3
8251A USART	Transmit buffer empty and receive buffer full	2
8253 Timers	Timer 0, 1 outputs; function determined by timer mode	2
iSBX™ connectors	Function determined by iSBX™ MULTIMODULE™ board	4 (2 per iSBX™ connector)
Bus fail safe timer	Indicates addressed MULTIBUS® resident device has not responded to command within 6 ms	1
Power fail interrupt	Indicates AC power is not within tolerance	1
Power line clock	Source of 120 Hz signal from power supply	1
External interrupt	General purpose interrupt from auxiliary (P2) connector on backplane	1
iSBC 337A MULTIMODULE Numeric Data Processor	Indicates error or exception condition	1
Edge-level conversion	Converts edge triggered interrupt request to level interrupt	1
OR-gate matrix	Outputs of OR-gates on-board for multiple interrupts	2

down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

System Development Capabilities

The development cycle of iSBC 86/35 products can be significantly reduced and simplified by using either the System 86/330 or the Intellec® Series IV Microcomputer Development System.

IN-CIRCUIT EMULATOR

The I²ICE In-Circuit Emulator provides the necessary link between the software development environment and the "target" iSBC 86/35 execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 86/35 board, the I²ICE In-Circuit Emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

Software Support

Real time support for the iSBC 86/35 board is provided by the iRMX 86 operating system. The iRMX 86 Operating System is a highly functional operating system with a rich set of features and options based on an object-oriented architecture. In addition to being modular and configurable, functions beyond the nucleus include a sophisticated file management and I/O system, and powerful human interface. Both packages are easily customized and extended by the user to match unique requirements.

Interactive multi-user support is provided by the Xenix* operating system. Xenix is a compatible derivative of UNIX**, System III.

Language support for the iSBC 86/35 board includes Intel's ASM 86, PL/M 86, and PASCAL, and FORTRAN, as well as many third party 8086 languages. The iSDM monitor provides on-target, interactive system debug capability including breakpoint and memory examination features. The monitor supports iSBC/iAPX 86, 88, 186, and 188 based applications.

*Xenix is a trademark of Microsoft Corp.
**UNIX is a trademark of Bell Labs.

SPECIFICATIONS

Word Size

INSTRUCTION — 8, 16, 24, or 32 bits

DATA — 8, 16 bits

System Clock

5 MHz or 8 MHz ±0.1% (jumper selectable)

Cycle Time

BASIC INSTRUCTION CYCLE

8 MHz — 250 ns (assumes instruction in the queue)

5 MHz — 400 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles). Jumper selectable for 1 wait-state on-board memory access.

Memory Capacity/Addressing

ON-BOARD EPROM

Device	Total Capacity	Address Range
2764	32K bytes	$F8000-FFFFF_H$
27128	64K bytes	$F0000-FFFFF_H$
27256	128K bytes	$E0000-FFFFF_H$
27512	256K bytes	$D0000-FFFFF_H$

ON-BOARD RAM

Board	Total Capacity	Address Range
iSBC 86/35	512K bytes	$0-7FFFF_H$

WITH MULTIMODULE™ RAM

Board	Total Capacity	Address Range
iSBC 304	640K bytes	$8-9\ FFFF_H$
iSBC 314	1M bytes	$8-FFFFF_H$

I/O Capacity

PARALLEL—24 programmable lines using one 8255A.

SERIAL—1 programmable line using one 8251A.

iSBX™ MULTIMODULE™—2 iSBX boards

Serial Communications Characteristics

SYNCHRONOUS—5–8 bit characters; internal or external character synchronization; automatic sync insertion

ASYNCHRONOUS—5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection

BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Timers

INPUT FREQUENCIES

Reference: 2.46 MHz ±0.1% (0.041 μs period, nominal); or 153.60 kHz ±0.1% (6.51 μs period, nominal)

NOTE:
Above frequencies are user selectable.

Event Rate: 2.46 MHz max

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (Cascaded)	
	Min	Max	Min	Max
Real-time Interrupt	**1.63** μs	427.1 ms	3.26s	466.50 min
Programmable one-shot	1.63 μs	427.1 ms	3.26s	466.50 min
Rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-wave rate generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software triggered strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Hardware triggered strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Event counter	—	2.46 MHz	—	—

Interfaces

MULTIBUS®—All signals TTL compatible

iSBX™ BUS—All signals TTL compatible

PARALLEL I/O—All signals TTL compatible

SERIAL I/O—RS232C compatible, configurable as a data set or data terminal

TIMER—All signals TTL compatible

INTERRUPT REQUESTS—All TTL compatible

Connectors

Interface	Double-Sided Pins	(in.)	Connectors
MULTIBUS® System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
iSBX™ Bus			Viking
8-Bit Data	36	0.1	000292-0001
16-Bit Data	44	0.1	000293-0001
Parallel I/O (2)	50	0.1	3M 3415-000 Flat or TI H312125 Pins
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

Line Drivers and Terminators

I/O DRIVERS—The following line drivers are all compatible with the I/O driver sockets on the iSBC 86/05 board

Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

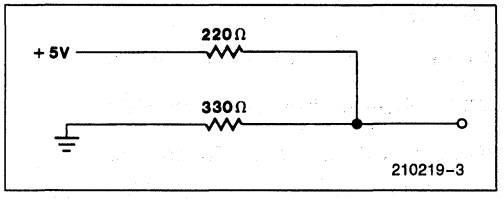
NOTE:
I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bi-directional drives and 1 kΩ temrinators

I/O TERMINATORS—220Ω/330Ω divider or 1 kΩ pullup

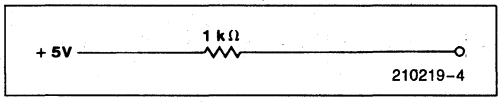
(OPTION 1)

220Ω/330Ω



(OPTION 2)

1 kΩ



MULTIBUS® Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Address	Tri-State	32
Commands	Tri-State	32
Bus Control	Open Collector	20

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.70 in. (1.78 cm)
Weight: 14 oz. (388 gm)

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM(1)	5.1A	25 mA	23 mA
RAM only(2)	660 mA	—	—
With 32K EPROM(3) (using 2764)	5.6A	25 mA	23 mA
With 64K EPROM (using 27128)	5.7A	25 mA	23 mA
With 128K EPROM (using 27256)	5.8A	25 mA	23 mA

NOTES:
1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Environmental Characteristics

OPERATING TEMPERATURE — 0°C to 55°C @ 200 linear feet per minute (LFM) air velocity

RELATIVE HUMIDITY — to 90% (without condensation)

Reference Manual

146245-002 — iSBC 86/35 Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

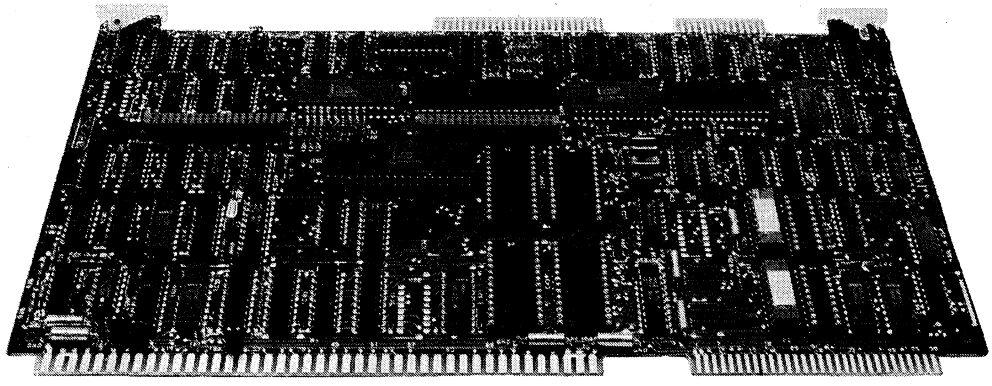
ORDERING INFORMATION

Part Number	Description
SBC 86/35	Single Board Computer

iSBC® 88/25
SINGLE BOARD COMPUTER

- 8-Bit 8088 Microprocessor Operating at 5 MHz
- One Megabyte Addressing Range
- Two iSBX™ Bus Connectors
- Optional Numeric Data Processor with iSBC® 337A MULTIMODULE™ Processor
- 4K Bytes of Static RAM; Expandable On-Board to 16K Bytes
- Sockets for up to 64K Bytes of JEDEC 24/28-Pin Standard Memory Devices; Expandable On-Board to 128K Bytes
- Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rates
- 24 Programmable Parallel I/O Lines
- Two Programmable 16-Bit BCD or Binary Timers/Event Counters
- 9 Levels of Vectored Interrupt Control, Expandable to 65 Levels
- MULTIBUS® Interface for Multimaster Configurations and System Expansion
- Development Support with Intel's iPDS, Low Cost Personal Development System, and EMV-88 Emulator

The iSBC 88/25 Single Board Computer is a member of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's technology to provide economical, self-contained, computer-based solutions for OEM applications. The iSBC 88/25 board is complete computer system on a single 6.75 × 12.00-in. printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The large control storage capacity makes the iSBC 88/25 board ideally suited for control-oriented applications such as process control, instrumentation, industrial automation and many others.



143847-1

October 1988
Order Number: 143847-003

FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processor for the iSBC 88/25 board is Intel's 8088 CPU operating at 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers, all accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages, as well as assembly language.

Instruction Set

The 8088 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the iSBC 337A MULTIMODULE Numeric Data Processor extends the architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16, 32, and 64-bit integer, and 32 and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

Architectural Features

A 4-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 750 ns minimum instruction cycle to 250 ns for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, inter-module communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities

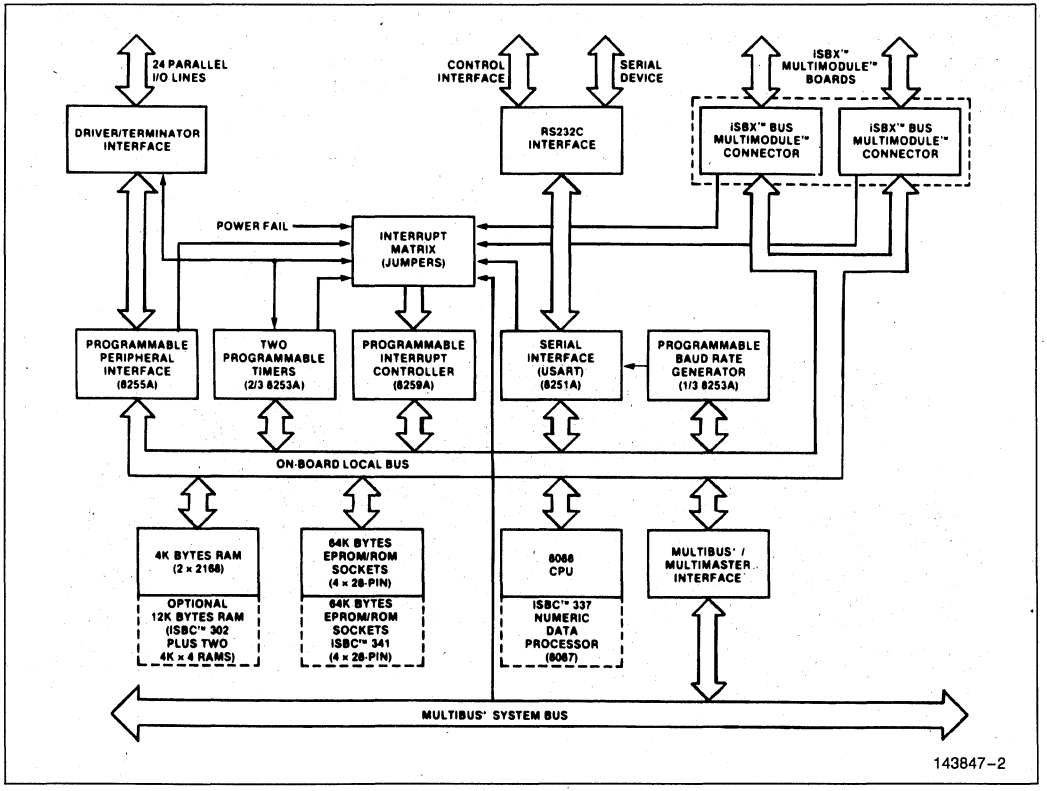


Figure 1. iSBC® 88/25 Block Diagram

offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64 Kbytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions. All Intel languages support the extended memory capability, relieving the programmer of managing the megabyte memory space, yet allowing explicit control when necessary.

Memory Configuration

The iSBC 88/25 microcomputer contains 4 Kbytes of high-speed static RAM on-board. In addition, the on-board RAM may be expanded to 12 Kbytes via the iSBC 302 8 Kbyte RAM module which mounts on the iSBC 88/25 board and then to 16 Kbytes by adding two 4K × 4 RAM devices in sockets on the iSBC 302 module. All on-board RAM is accessed by the 8088 CPU with no wait states, yielding a memory cycle time of 800 ns.

In addition to the on-board RAM, the iSBC 88/25 board has four 28-pin sockets, configured to accept JEDEC 24/28-pin standard memory devices. Up to 64 Kbytes of EPROM are supported in 16 Kbyte increments with Intel 27128 EPROMs. The iSBC 88/25 board is also compatible with the 2716, 2732 and 2764 EPROMs allowing a capacity of 8K, 16K and 32 Kbytes, respectively. Other JEDEC standard pinout devices are also supported, including byte-wide static and integrated RAMs.

With the addition of the iSBC 341 MULTIMODULE EPROM option, the on-board capacity for these devices is doubled, providing up to 128 Kbytes of EPROM capacity on-board.

Parallel I/O Interface

The iSBC 88/25 Single Board Computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics.

The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 88/25 board. A software selectable baud rate generator provides the USART with all common communication frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun and framing error detection are all incorporated in the USART. The RS232C compatible interface on each board, in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes and asynchronous and synchronous modems. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector.

Table1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X(1)
	4	X		X			X(1)

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Programmable Timers

The iSBC 88/25 board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 88/25 board RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8-bit iSBX MULTIMODULE connectors are provided on the iSBC 88/25 microcomputer. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULES optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 88/25 provide all signals necessary to interface to the local on-board bus. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 88/25 board. An iSBX bus interface specification and iSBX connectors are available from Intel.

MULTIBUS® SYSTEM BUS AND MULTIMASTER CAPABILITIES

Overview

The MULTIBUS system bus is Intel's industry standard microcomputer bus structure. Both 8 and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processor and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 88/25 board provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 88/25 boards or other bus masters, including iSBC 80 and iSBC 86 family MULTIBUS compatible single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Interrupt Capability

The iSBC 88/25 board provides 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8088 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Intel 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Table 3. Programmable Interrupt Mode

Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-Rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

Interrupt Request Generation

Interrupt requests to be serviced by the iSBC 88/25 board may originate from 24 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 and iSBC 640 Power Supply or equivalent, to initiate an orderly shut down of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out of the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

System Development Capabilities

The development cycle of iSBC 88/25 products can be significantly reduced and simplified by using the Intellec Series IV Microcomputer Development System.

PL/M-86

Intel's system's implementation language, PL/M-86, is available as an Intellec Microcomputer Development System option. PL/M-86 provides the capability to program in algorithmic language and eliminates the need to manage register usage or allocate memory while still allowing explicit control of the system's resources when needed.

Run-Time Support

Intel also offers two run-time support packages; iRMX 88 Realtime Multitasking Executive and the iRMX 86 Operating System. iRMX 88 is a simple, highly configurable and efficient foundation for small, high performance applications. Its multitasking structure establishes a solid foundation for modular system design and provides task scheduling and management, intertask communication and synchronization, and interrupt servicing for a variety of peripheral devices. Other configurable options include terminal handlers, disk file system, debuggers and other utilities. iRMX 86 is a high functional operating system with a very rich set of features and options based on an object-oriented architecture. In addition to being modular and configurable, functions beyond the nucleus include a sophisticated file management and I/O system, and powerful human interface. Both packages are easily customized and extended by the user to match unique requirements.

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS resident peripherals or other CPU boards	8; may be expanded to 64 with slave 8259A PIC's on MULTIBUS boards
8255A Programmable Peripheral Interface	Signals into buffer full or output buffer empty; also BUS INTR OUT general purpose interrupt from driver/ terminator sockets	3
8251A USART	Transmit buffer empty and receive buffer full	2
8253 Timers	Timer 0, 1 outputs; function determined by timer mode	2
iSBX Connectors	Function determined by iSBX MULTIMODULE board	4 (2 per iSBX connector)
Bus Fail Safe Timer	Indicates addressed MULTIBUS resident device has not responded to command within 6 ms	1
Power Fail Interrupt	Indicates AC power is not within tolerance	1
Power Line Clock	Source of 120 Hz signal from power supply	1
External Interrupt	General purpose interrupt from parallel port J1 connector	1
iSBC 337 MULTIMODULE Numeric Data Processor	Indicates error or exception condition	1

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, or 32 bits
Data—8 bits

System Clock

5.00 MHz or 4.17 MHz ±0.1% (jumper selectable)

NOTE:
4.17 MHz required with the optional iSBC 337 module.

Cycle Time

BASIC INSTRUCTION CYCLE

At 5 MHz—1.2 μs
—400 ns (assumes instruction in the queue)

NOTES:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Memory Cycle Time

RAM—800 ns (no wait states)
EPROM—Jumper selectable from 800 ns to 1400 ns

Memory Capacity/Addressing

ON-BOARD EPROM

Device	Total Capacity	Address Range
2716	8 Kbytes	FE000-FFFFF$_H$
2732	16 Kbytes	FC000-FFFFF$_H$
2764	32 Kbytes	F8000-FFFFF$_H$
27128	64 Kbytes	F0000-FFFFF$_H$

WITH iSBC 341 MULTIMODULE EPROM

Device	Total Capacity	Address Range
2716	16 Kbytes	FC000-FFFFF$_H$
2732	32 Kbytes	F8000-FFFFF$_H$
2764	64 Kbytes	F0000-FFFFF$_H$
27128	128 Kbytes	E0000-FFFFF$_H$

NOTES:
iSBC 88/25 EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMs (2 sockets); iSBC 341 sockets also support E^{2}PROMs.

ON-BOARD RAM

4 Kbytes—0-0FFF$_H$

WITH iSBC 302 MULTIMODULE RAM

12 Kbytes—0-2FFF$_H$

WITH iSBC 302 MULTIMODULE BOARD AND TWO 4K x 4 RAM CHIPS

16 Kbytes—0-3FFF$_H$

I/O Capacity

Parallel—24 programmable lines using one 8255A
Serial—1 programmable line using one 8251A
iSBX Multimodule—2 iSBX MULTIMODULE boards

Serial Communications Characteristics

Synchronous—5 8-bit characters; internal or external character synchronization; automatic sync insertion
Asynchronous—5 8-bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection

Baud Rates

Frequency (KHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTES:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Timers

INPUT FREQUENCIES

Reference: 2.458 MHz ±0.1% (406.9 ns period, nominal); or 1.229 MHz ±0.1% (813.8 ns period, nominal); or 153.6 KHz ± 0.1% (6.510 μs period, nominal)

NOTE:
Above frequencies are user selectable.

Event Rate: 2.46 MHz max

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63 μs	427.1 ms	3.26s	466.50 min
Programmable One-Shot	1.63 μs	427.1 ms	3.26s	466.50 min
Rate Generator	2.342 Hz	613.5 KHz	0.000036 Hz	306.8 KHz
Square-Wave Rate Generator	2.342 Hz	613.5 KHz	0.000036 Hz	306.8 KHz
Software Triggered Strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Hardware Triggered Strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Event Counter	—	2.46 MHz	—	—

Interfaces

Multibus: All signals TTL compatible

iSBX Bus: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Serial I/O: RS232C compatible, configurable as a data set or data terminal

Timer: All signals TTL compatible

Interrupt Requests: All TTL compatible

CONNECTORS

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
MULTIBUS System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
iSBX Bus 8-Bit Data	36	0.1	iSBX 960-5
Parallel I/O (2)	50	0.1	3M 3415-000 Flat or TI H312125 Pins
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

Line Drivers and Terminators

I/O Drivers: The following line drivers are all compatible with the I/O driver sockets on the iSBC 88/25 board.

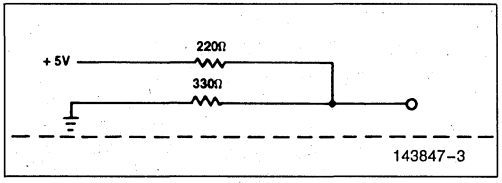
Driver	Characteristics	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

NOTES:
I = inverting; NI = non-inverting; OC = open collector.

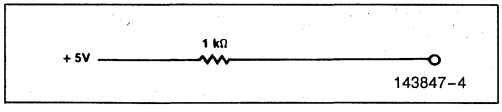
Port 1 of the 8255A has 32 mA totem-pole bidirectional drivers and 10Ω terminators.

I/O Terminators: 220Ω/330Ω divider or 1 KΩ pullup.

220Ω/330Ω Option 1



1 KΩ Option 2



MULTIBUS Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Address	Tri-State	24
Commands	Tri-State	32
Bus Control	Open Collector	20

Physical Characteristics

Width: 12.00 in. (30.48 cm)

Height: 6.75 in. (17.15 cm)

Depth: 0.70 in. (1.78 cm)

Weight: 14 oz. (388 gm)

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM(1)	3.8A	25 mA	23 mA
RAM only(2)	104 mA		
With 8K EPROM(3) (using 2716)	4.3A	25 mA	23 mA
With 16K EPROM(3) (using 2732)	4.4A	25 mA	23 mA
With 32K EPROM(3) (using 2764)	4.4A	25 mA	23 mA

NOTES:
1. Does not include power for optional ROM/EPROM, I/O drivers and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode. Does not include power for optional RAM.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Relative Humidity: to 90% (without condensation)

Reference Manual

143825-001—iSBC 88/25 Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

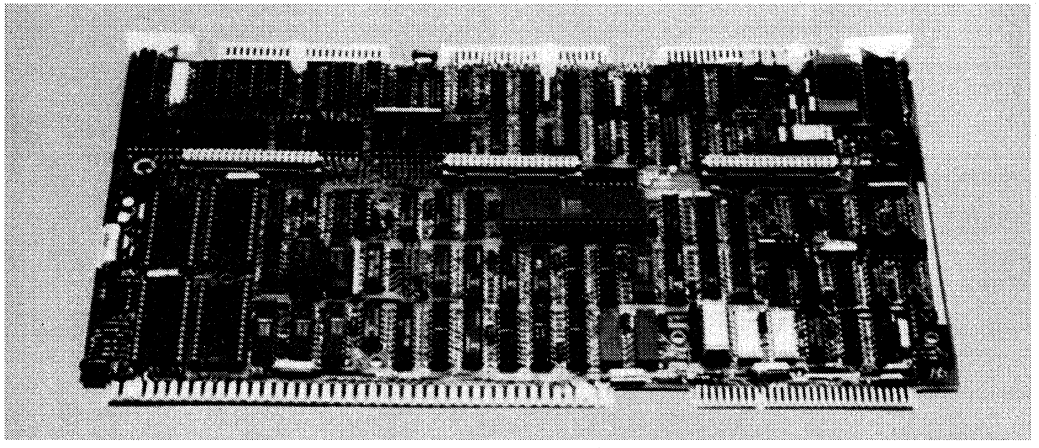
ORDERING INFORMATION

Part Number	Description
SBC 88/25	8-bit Single Board Computer with 4 Kbytes RAM

iSBC® 88/40A
MEASUREMENT AND CONTROL COMPUTER

- **High Performance 4.8/6.67 MHz 8088 8-Bit HMOS Processor**
- **12-Bit KHz Analog-to-Digital Converter with Programmable Gain Control**
- **16-Bit Differential/32 Single-Ended Analog Input Channels**
- **Three iSBX™ MULTIMODULE™ Connectors for Analog, Digital, and other I/O Expansion**
- **4K Bytes Static RAM, Expandable via iSBC® 301 MULTIMODULE™ RAM to 8K Bytes (1K Byte Dual-Ported)**
- **Four EPROM/E²PROM Sockets for up to 64K Bytes, Expandable to 128K Bytes with iSBC® 341 Expansion MULTIMODULE™**
- **MULTIBUS® Intelligent Slave or Multimaster**

The Intel iSBC 88/40A Measurement and Control Computer is a member of Intel's large family of Single Board Computers that takes full advantage of Intel's VLSI technology to provide an economical self-contained computer based solution for applications in the areas of process control and data acquisition. The on-board 8088 processor with its powerful instruction set allows users of the iSBC 88/40A board to update process loops as much as 5–10 times faster than previously possible with other 8-bit microprocessors. For example, the high performance iSBC 88/40A can concurrently process and update 16 control loops in less than 200 milliseconds using a traditional PID (Proportional-Integral-Derivative) control algorithm. The iSBC 88/40A board consists of a 16 differential/32 single ended channel analog multiplexer with input protected circuits, A/D converter, programmable central processing unit, dual port and private RAM, read only memory sockets, interrupt logic, 24 channels of parallel I/O, three programmable timers and MULTIBUS control logic on a single 6.75 by 12.00-inch printed circuit card. The iSBC 88/40A board is capable of functioning by itself in a stand-alone system or as a multimaster or intelligent slave in a large MULTIBUS system.



280220-1

October 1986
Order Number: 280220-001

FUNCTIONAL DESCRIPTION

Three Modes of Operation

The iSBC 88/40A Measurement and Control Computer (MACC) is capable of operating in one of three modes: stand-alone controller, bus multimaster or intelligent slave. A block diagram of the iSBC 88/40A Measurement and Control Computer is shown in Figure 1.

Stand-Alone Controller

The iSBC 88/40A Measurement and Control Computer may function as a stand-alone single board controller with CPU, memory and I/O elements on a single board. The on-board 4K bytes of RAM and up to 64K bytes of read only memory, as well as the analog-to-digital converter and programmable parallel I/O lines allow significant control and monitoring capabilities from a single board.

Bus Multimaster

In this mode of operation the iSBC 88/40A board may interface and control a wide variety of iSBC memory and I/O boards or even with additional iSBC 88/40 boards or other single board computer masters or intelligent slaves.

Intelligent Slave

The iSBC 88/40A board can perform as an intelligent slave to any Intel 8- or 16-bit MULTIBUS master CPU by not only offloading the master of the analog data collection, but it can also do a significant amount of pre-processing and decision-making on its own. The distribution of processing tasks to intelligent slaves frees the system master to do other system functions. The Dual port RAM with flag bytes for signaling allows the iSBC 88/40A board to process and store data without MULTIBUS memory or bus contention.

Central Processing Unit

The central processor unit for the iSBC 88/40A board is a powerful 8-bit HMOS 8088 microprocessor. By moving on-board jumpers, the user can select either a 4.8 or 6.67 MHz CPU clock rate. The iSBC 88/40A board can also run at 8 MHz by changing the CPU clock oscillator to a 24 MHz unit. For 8 MHz operation, the iSBC 88/40A board should either be the only MULTIBUS master in the system or be an intelligent slave that never directly accesses the MULTIBUS interface.

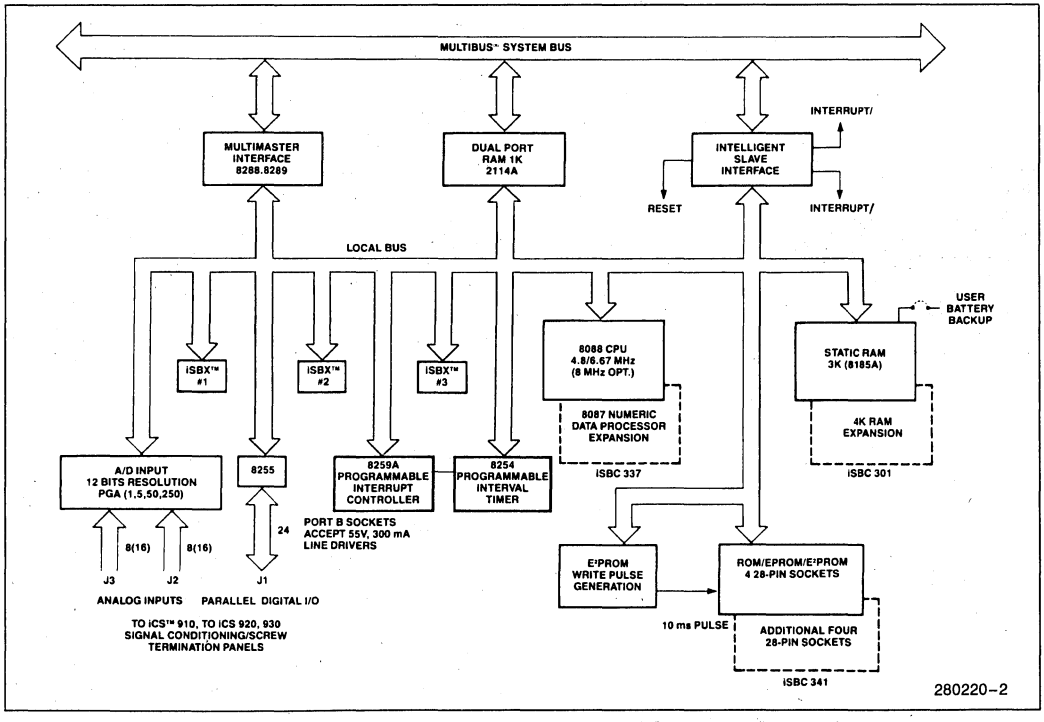


Figure 1. iSBC® 88/40A Measurement and Control Computer Block Diagram

INSTRUCTION SET—The 8088 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. The instruction set of the 8088 is a superset of the 8080A/8085A family and with available software tools, programs written for the 8080A/8085A can be easily converted and run on the 8088 processor. Programs can also be run that are implemented on the 8088 with little or no modification.

ARCHITECTURAL FEATURES—A 4-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 1.04 ms minimum instruction cycle to 417 ns (at 4.8 MHz clock rate) for queued instructions. The stack oriented architecture facilitates nested subroutines and co-routines, reentrant code and powerful interrupt handling. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

Bus Structure

The iSBC 88/40A single board computer has three buses: 1) an internal bus for communicating with on-board memory, analog-to-digital converter, ISBX MULTIMODULES and I/O options; 2) the MULTIBUS system bus for referencing additional memory and I/O options, and 3) the dual-port bus which allows access to RAM from the on-board CPU and the MULTIBUS system bus. Local (on-board) accesses do not require MULTIBUS communication, making the system bus available for use by other MULTIBUS masters (i.e., DMA devices and other single board computers transferring to additional system memory). This feature allows true parallel processing in a multiprocessor environment. In addition, the MULTIBUS interface can be used for system expansion through the use of other 8- and 16-bit iSBC computers, memory and I/O expansion boards.

RAM Capabilities

DUAL-PORT RAM—The dual-port RAM of the iSBC 88/40A board consists of 1K bytes of static RAM, implemented with Intel 2114A chips. The on-board base address of this RAM is 00C00 (3K) normally; it is relocated to 01C00 (7K) when the iSBC 301 MULTIMODULE RAM is added to the protected RAM. The MULTIBUS port base address of the dual-port RAM can be jumpered to any 1K byte boundary in the 1M byte address space. The dual-port RAM can be accessed in a byte-wide fashion from the MULTIBUS system bus. When accessed from the MULTIBUS system bus, the dual-port RAM decode logic will generate INH1/ (Inhibit RAM) to allow dual-port RAM to overlay other system RAM. The dual-port control logic is designed to favor an on-board RAM access. If the dual-port is not currently performing a memory cycle for the MULTIBUS system port, only one wait state will be required. The on-board port any require more than one wait state if the dual-port RAM was busy when the on-board cycle was requested. The LOCK prefix facility of the iAPX 88/10 assembly language will disallow system bus accesses to the dual-port RAM. In addition, the on-board port to the dual-port RAM can be locked by other compatible MULTIBUS masters, which allows true symmetric semaphore operation. When the board is functioning in the master mode, the LOCK prefix will additionally disable other masters from obtaining the system bus.

PRIVATE RAM—In addition to the 1K byte dual-port RAM, there is a 3K byte section of private static RAM not accessible from the system bus. This RAM has a base address of 00000, and consists of three Intel 8185 RAM chips which are interfaced to the multiplexed address/data bus of the 8088 microprocessor. Expansion of this private RAM from 3K to 7K byte scan be accomplished by the addition of an iSBC 301 MULTIMODULE RAM (4K bytes). When the 301 is added, protected RAM extends from 0 to 7K, and the base address of the dual-port RAM is relocated from 3K (00C00) to 7K (01C00). All protected RAM accesses require one wait state. The private RAM resides on the local on-board bus, which eliminates contention problems between on-board accesses to private RAM and system bus accesses to dual-port AM. The private RAM can be battery backed (up to 16K bytes).

Additional RAM can be added by utilizing JEDEC-compatible static RAMs in the available EPROM sockets.

Parallel I/O Interface

The iSBC 88/40A single board computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. There the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O

configurations, sockets are provided for interchangeable I/O line drivers and terminators. Port 2 can also accept TTL compatible peripheral drives, such as 75461/462, 75471/472, etc. These are open collector, high voltage drivers (up to 55 volts) which can sink 300 mA. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector that mates with flat, woven, or round cable. This edge connector is also compatible with the Intel ICS™ 920 Digital I/O and iCS 930 AC Signal Conditioning/Termination Panels, for field wiring, optical isolation and high power (up to 3 amp) power drive.

EPROM Capabilities

Four 28-pin sockets are provided for the use of Intel 2716s, 2732s, 2764s, 27128s, future JEDEC-compatible 128K and 256K bit EPROMs and their respective ROMs. When using 27128s the on-board EPROM capacity is 64K bytes. Read only memory expansion is available through the use of the iSBC 341 EPROM/ROM memory expansion MULTIMODULE. When the iSBC 341 is used an additional four EPROM sockets are made available, for a total iSBC 88/40A board capacity of 128K bytes EPROM with Intel 27128s.

E²PROM Capabilities

The four 28-pin sockets can also accommodate Intel 2817A or 2816A E²PROMs, for dynamic storage of control loop setpoints, conversion parameters, or other data (or programs) that change periodically but must be kept in nonvolatile storage.

Timing Logic

The iSBC 88/40A board provides an 8254-2 Programmable Interval Timer, which contains three independent, programmable 16-bit timers/event counters. All three of these counters are available to generate time intervals or event counts under software control. The outputs of the three counters may be independently routed to the interrupt matrix. The inputs and outputs of timers 0 and 1 can be connected to parallel I/O lines on the J1 connector, where they replace 8255A port C lines. The third counter is also used for timing E²PROM write operations.

Interrupt Capability

The iSBC 88/40A board provides 9 vectored interrupt levels. The highest level is NMI (Nonmaskable Interrupt) line which is directly tied to the 8088 CPU. This interrupt cannot be inhibited by software and is typically used for signalling catastrophic events (i.e., power failure). On servicing this interrupt, program control will be implicitly transferred through location 00008_H. The Intel 8259A Programmable Interrupt Controller (PIC) provides vectoring for the next eight interrupt levels. As shown in Table 2, a selection of four priority processing modes is available to the designer to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PCI accepts interrupt requests from the programmable parallel and/or iSBX interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority than the level currently being serviced, and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt make register of the PIC. The PIC generates a

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X(1)
	4	X		X			X(1)

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

unique memory address for each interrupt level. These addresses are equally spaced at 4-byte intervals. This 32-byte lock may begin at any 32-byte boundary in the lowest 1K bytes of memory, and contains unique instruction pointers and code segment offset values (for expanded memory operation) for each interrupt level. After acknowledging an interrupt and obtaining advice identifier byte from the 8259A PIC, the CPU will store its status flags on the stack and execute an indirect CALL instruction through the vector location (derived from the device identifier) to the interrupt service routine.

NOTE:
The first 32 vector locations are reserved by Intel for dedicated vectors. Users who wish to maintain compatibility with present and future Intel products should not use these locations for user-defined vector addresses.

Table 2. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

INTERRUPT REQUEST GENERATION—Interrupt requests may originate from 26 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). A jumper selectable request can be generated by each of the programmable timers. An additional interrupt request line may be jumpered directly from the parallel I/O driver terminator section. Eight prioritized interrupt request lines allow the iSBC 88/40A board to recognize and service interrupts originating from peripheral boards interfaced via the MULTIBUS system bus. The fail safe timer can be selected as an interrupt source. Also, interrupts are provided from the iSBX connectors (6), end-of-conversion, PFIN and from the power line clock.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635, iSBC 640, and iCS 645 Power Supply or equivalent.

iSBX™ MULTIMODULE™ Expansion Capabilities

Three iSBX MULTIMODULE connectors are provided on the iSBC 88/40A board. Up to three single wide MULTIMODULE or one double wide and one single wide iSBX MULTIMODULE can be added to the iSBC 88/40A board. A wide variety of peripheral controllers, analog and digital expansion options are available. For more information on specific iSBX MULTIMODULES consult the Intel OEM Microcomputer System Configuration Guide.

Processing Expansion Capabilities

The addition of a iSBC 337 Multimodule Numeric Data Processor offers high performance integer and floating point math functions to users of the iSBC 88/40A board. The iSBC 337 incorporates the Intel 8087 and because of the MULTIMODULE implementation, it allows on-board expansion directly on the iSBC 88/40A board, eliminating the need for additional boards or floating point requirements.

MULTIBUS® Expansion

Memory and I/O capacity may be expanded further and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combination of RAM boards, EPROM boards, or memory combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O MULTIBUS expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers either through the use of expansion boards and iSBX MULTIMODULES. Modular expandable backplanes and cardcages are available to support multiboard systems.

NOTE:
Certain system restrictions may be incurred by the inclusion of some of the iSBC 80 family options in an iSBC 88/40 system. Consult the Intel OEM Microcomputer System Configuration Guide for specific data.

Analog Input Section

The analog section of the iSBC 88/40A board receives all control signals through the local bus to

initiate channel selection, gain selection, sample and hold operation, and analog-to-digital conversion. See Figure 2.

INPUT CAPACITY—32 separate analog signals may be randomly or sequentially sampled in single-ended mode with the 32 input multiplexers and a common ground. For noisier environments, differential input mode can be configured to achieve 16 separate differential signal inputs, or 32 pseudo differential inputs.

RESOLUTION—The analog section provides 12-bit resolution with a successive approximation analog-to-digital converter. For bipolar operation (−5 to +5 or −10 to +10 volts) it provides 11 bits plus sign.

SPEED—The A-to-D converter conversion speed is 50 μs (20 kHz samples per second). Combined with the programming interface, maximum throughput via the local bus and into memory will be 55 microseconds per sample, or 18 kHz samples per second, for a single channel, a random channel, or a sequential channel scan at a gain of 1, 5 ms at a gain of 5,250 ms at a gain of 50, and 20 ms at a gain of 250. A-to-D conversion is initiated via a programmed command from the 8088 central processor. Interrupt on end-of-conversion is a standard feature to ease programming and timing constraints.

ACCURACY—High quality components are used to achieve 12 bits resolution and accuracy of 0.035% full scale range ±½ LSB at gain = 1. Offset is adjustable under program control to obtain a nominal ±0.024% FSR ±½ LSB accuracy at any fixed temperature between 0°C and 60°C (gain = 1). See specifications for other gain accuracies.

GAIN—To allow sampling of millivolt level signals such as strain gauges and thermocouples, gain is made configurable via user program commands up to 250 × (20 millivolts full scale input range). User can select gain ranges of 1 (5V), 5 (1V), 50 (100 mV), 250 (20 mV) to match his application.

OPERATIONAL DESCRIPTION—The iSBC 88/40A single board computer addresses the analog-to-digital converter by executing IN or OUT instructions to the port address. Analog-to-digital conversions can be programmed in either of two modes: 1) start conversion and poll for end-of-conversion (EOC), or 2) start conversion and wait for interrupt at end of conversion. When the conversion is complete as signaled by one of the above techniques, INput instructions read two bytes (low and high bytes) containing the 12-bit data word.

Output Command—Select input channel and start conversion.

	GAIN		CONNECTOR		CHANNEL SELECT			
BIT POSITION	7	6	5	4	3	2	1	0
INPUT CHANNEL	G1	G2		J	C3	C2	C1	C0

Input Data—Read converted data (low byte) or Read converted data (high byte).

	DATA							
BIT POSITION	7	6	5	4	3	2	1	0
LOW/STATUS BYTE	D3	D2	D1	D0				EOC

	DATA							
HIGH BYTE	D11	D10	D9	D8	D7	D6	D5	D4

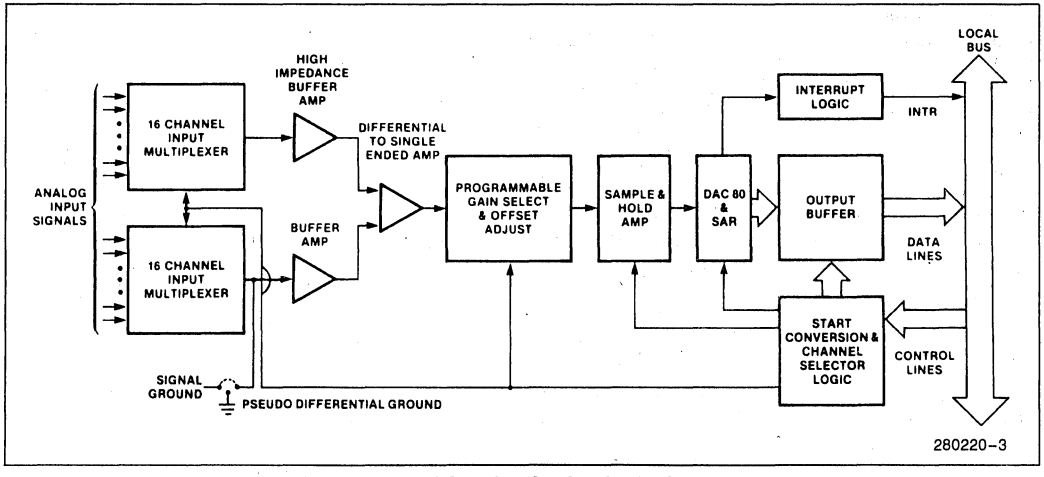


Figure 2. iSBC® 88/40 Analog Input Section

Offset Correction—At higher gains (×50, ×250) the voltage offset tempco in the A/D circuitry can sometimes cause unacceptable inaccuracies. To correct for this offset, one channel can be dedicated to be used as a reference standard. This channel can be read from the program to determine the amount of offset. The reading from this channel will then be subtracted from all other channel readings, in effect eliminating the offset tempco.

SYSTEM SOFTWARE DEVELOPMENT

The development cycle of the iSBC 88/40 board may be significantly reduced using an Intel Intellec Microcomputer Development System and Intel's FORTRAN, PASCAL, or PL/M 86/88 Software packages.

SPECIFICATIONS

Word Size

Instruction—8, 16, or 32 bits
Data—8 bits

Instruction Cycle Time (minimum)

Instruction	8088 Clock Rate			Number of Clock Cycles
	4.8 MHz	6.67 MHz	8.0 MHz	
In Queue	417 ns	300 ns	250 ns	2
Not in Queue	1.04 ns	750 ns	625 ns	5

MEMORY CAPACITY

On-Board ROM/EPROM/E²PROM

Up to 64K bytes; user installed in 2K, 4K, 8K or 16K byte increments or up to 128K if iSBC 341 MULTIMODULE EPROM option installed. Up to 8K bytes of E²PROM using Intel 2816As or 2817As may be user-installed in increments of 2, 4, or 8 bytes.

On-Board RAM

4K bytes or 8K bytes if the iSBC 301 MULTIMODULE RAM is installed. Integrity maintained during power failure with user-furnished batteries. 1K bytes are dual-ported.

Off-Board Expansion

Up to 1 megabyte of user-specified combination of RAM, ROM, and EPROM.

MEMORY ADDRESSING

On-Board ROM/EPROM

FE000-FFFFF (using 2716 EPROMs)
FC000-FFFFF (using 2732 EPROMs)
F8000-FFFFF (using 2764 EPROMs)
F0000-FFFFF (using 27128 EPROMs)

On-Board ROM/EPROM (With iSBC 341 MULTIMODULE EPROM option installed)

FC000-FFFFF (using 2716 EPROMs)
F8000-FFFFF (using 2732 EPROMs)
F0000-FFFFF (using 2764 EPROMs)
E0000-FFFFF (using 27128 EPROMs)

On-Board RAM (CPU Access)

00000-00FFF
00000-01FFF (if iSBC 301 MULTIMODULE RAM option installed)

On-Board RAM

Jumpers allow 1K bytes of RAM to act as slave RAM for access by another bus master. Addressing may be set within any 1K boundary in the 1-megabyte system address space.

Slave RAM Access

Average: 350 ns

INTERVAL TIMER

Output Frequencies

Function	Single Timer		Dual Timers (Two Timers Cascaded)
	Min	Max	
Real-Time Interrupt Interval	0.977 μs	64 ms	69.9 minutes maximum
Rate Generator (Frequency	15.625 Hz	1024 KHz	0.00024 Hz minimum

CPU CLOCK

4.8 MHz ±0.1% or 6.67 MHz ±0.1%. (User selectable via jumpers);

8.0 MHz (with user installed 24 MHz oscillator)

I/O Addressing

All communications to parallel I/O ports, iSBX bus, A/D port, timers, and interrupt controller are via read and write commands from the on-board 8088 CPU.

Interface Compatability

Parallel I/O—24 programmable lines (8 lines per port); one port includes a bidirectional bus driver. IC sockets are included for user installation of line drivers and/or I/O terminators and/or peripheral drivers as required for interface ports.

Interrupts

8088 CPU includes a non-maskable interrupt (NMI). NMI interrupt is provided for catastrophic events such as power failure. The on-board 8259A PIC provides 8-bit identifier of interrupting device to CPU. CPU multiplies identifier by four to derive vector address. Jumpers select interrupts from 26 sources without necessity of external hardware. PIC may be programmed to accommodate edge-sensitive or level-sensitive inputs.

Analog Input

16 differential (bipolar operation) or 32 single-ended (unipolar operation).

Full Scale Voltage Range—−5 to +5 volts (bipolar), 0 to +5 volts (unipolar).

NOTE:
Ranges of 0 to 10V and ±10V achievable with externally supplied ±15V power.

Gain—Program selectable for gain of 1, 5, 50, or 250.

Resolution—12 bits (11 bits plus sign for ±5, ±10 volts).

Accuracy—Including noise and dynamic errors.

Gain	25°C
1	±0.035% FSR*
5	±0.06% FSR*
50	±0.07% FSR*
250	±0.12% FSR*

NOTE:
FSR = Full Scale Range ±½ LSB. Figures are in percent of full scale reading. At any fixed temperature between 0°C and 60°C, the accuracy is adjustable to ±0.05% of full scale.

Gain TC (at gain = 1)—30 PPM (typical), 56 PPM (max) per degree centigrade, 40 PPM at other gains.

Offset TC— (in % of FSR/°C)	Gain	Offset TC (typical)
	1	0.0018%
	5	0.0036%
	50	0.024%
	250	0.12%

Sample and Hold-Sample Time: 15 μs
Aperature-Hold Aperature Time: 120 ns
Input Overvoltage Protection: 30 volts
Input Impedance: 20 megohms (min.)
Conversion Speed: 50 μs (max.) at gain = 1
Common Mode Rejection Ratio: 60 dB (min.)

Physical Characteristics

Width: 30.48 cm (12.00 in.)
Length: 17.15 cm (6.75 in.)
Height: 1.78 cm (0.7 in.)
2.82 cm (1.13 in.) with iSBC Memory Expansion, MULTIMODULES, iSBX Numeric Data Processor or iSBX MULTIMODULES.

Electrical Requirements

Power Requirements

Voltage	Current	
	Maximum	Typical
+5V	5.5A	4A
+5V Aux	150 mA	100 mA
+12V	120 mA	80 mA
−12V	40 mA	30 mA

NOTES:
1. The current requirement includes one worst case (active-standby) EPROM current.
2. If +5V Aux is supplied by the iSBC 88/40A board, the total +5V current is the sum of the +5V and the +5V Aux.

Environmental Requirements

Operating Temperature: 0° to +60°C with 6 CFM min. air flow across board
Relative Humidity: to 90% without condensation

Equipment Supplied

iSBC 88/40A Measurement and Control Computer Schematic diagram

REFERENCE MANUALS

147049-001— SBC 88/40A Measurement and Control Computer Hardware Reference Manual (Order Separately).

Manuals may be ordered from an Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

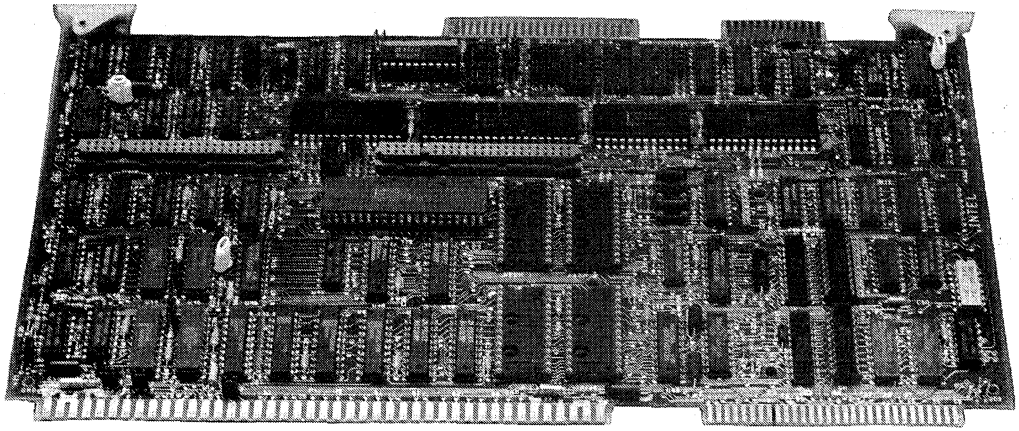
ORDERING INFORMATION

Part Number	Description
SBC 88/40A	Measurement and Control Computer

iSBC® 86/05A
SINGLE BOARD COMPUTER

- 8086/10 (8086-2) Microprocessor with 5 or 8 MHz CPU Clock
- Software Compatible with 8086, 8088, 80186, 80286 Based 16-bit Single Board Computers
- Optional 8086/20 Numeric Data Processor with iSBC® 337 A MULTIMODULE™ Processor
- 8K bytes of Static RAM; Expandable On-Board to 16K Bytes
- Sockets for up to 256K Bytes of JEDEC 24/28-Pin Standard Memory Devices; Expandable On-Board to 512K Bytes
- Two iSBX™ Bus Connectors
- Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rate
- 24 Programmable Parallel I/O Lines
- Two Programmable 16-Bit BCD or Binary Timers/Event Counters
- 9 Levels of Vectored Interrupt Control, Expandable to 65 Levels
- MULTIBUS® Bus Interface for Multimaster Configurations and System Expansion
- Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral Controllers, Packaging and Software

The iSBC 86/05A Single Board Computer is a member of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's technology to provide economical, self-contained, computer-based solutions for OEM applications. The iSBC 86/05A board is a complete computer system on a single 6.75 x 12.00 in. printed circuit card. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The large control storage capacity makes the iSBC 86/05A board ideally suited for control-oriented applications such as process control, instrumentation, industrial automation, and many others.



143325-1

September 1987
Order Number: 143325-003

FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processor for the iSBC 86/05A board is Intel's iAPX 86/10 (8086-2) CPU. a clock rate of 8 MHz is supported with a jumper selectable option of 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers. All are accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages as well as assembly language.

Instruction Set

The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8- and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the iSBC 337A MULTIMODULE Numeric Data Processor extends the iAPX 86/10 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

Architectural Features

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 740 ns minimum instruction cycle to 250 ns for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, inter-module communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time with activation of a specific register controlled explicity by program control and selected implicity by specific functions and instructions. All Intel languages support the extended memory capability, relieving the programmer of managing the megabyte memory space yet allowing explicit control when necessary.

Memory Configuration

The iSBC 86/05A microcomputer contains 8K bytes of high-speed 8K x 4 bit static RAM on-board. In addition, the above on-board RAM may be expanded to 16K bytes with the iSBC 302 MULTIMODULE RAM option which mounts on the iSBC 86/05A board. All on-board RAM is accessed by the 8086-2 CPU with no wait states, yielding a memory cycle time of 500 ns.

The iSBC 86/05A board also has four 28-pin, 8-bit wide (byte-wide) sockets, configured to accept JEDEC 24/28-pin standard memory devices. Up to 256K bytes of EPROM are supported in 64K byte increments with Intel 27512 EPROMs. The iSBC 86/05A board also supports 2K x 8, 4K x 8, 8K x 8, 16K x 8 and 32K x 8 EPROM memory devices. These sites also support 2K x 8 and 8K x 8 byte-wide static RAM (SRAM) devices and iRAM devices, yielding up to 32K bytes of SRAM in 8K byte increments on the baseboard.

When the addition of the iSBC 341 MULTIMODULE EPROM option, the on-board capacity for these devices is doubled, providing up to 512K bytes of EPROM and 64K bytes of byte-wide SRAM capacity on-board.

Parallel I/O Interface

The iSBC 86/05A Single Board Computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 86/05A board. A software selectable baud rate generator provides the USART with all common communication frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all

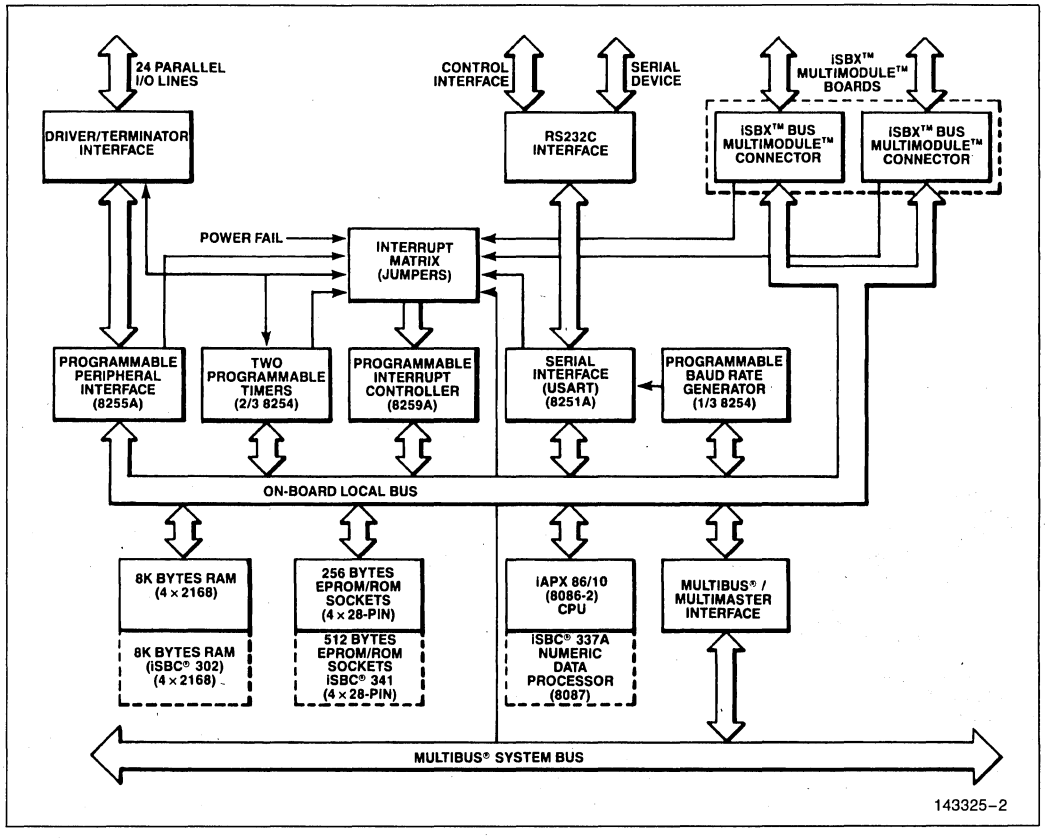


Figure 1. iSBC® 86/05A Block Diagram

incorporated in the USART. The RS232C compatible interface in conjunction with the USART, provides a direct interface to RS232C compatible terminals, cassettes, and asynchronous/synchronous modems. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector.

Programmable Timers

The iSBC 86/05A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8254 provides the programmable baud rate generator for the iSBC 86/05A board RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 86/05A microcomputer. Through these connectors, additional on-board I/O and memory functions may be added. iSBX MULTIMODULE boards support functions such as additional parallel and serial I/O, analog I/O, mass storage device controllers (e.g., cassettes and floppy disks), BITBUS™ controllers, bubble memory, and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less inter-

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Latched	Latched & Strobed	Latched	Latcched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When Terminal Count is Reached, an Interrupt Request is Generated. This Function is Extremely Useful for Generation of Real-Time Clocks.
Programmable One-Shot	Output Goes Low upon Receipt of an External Trigger Edge or Software Command and Returns High when Terminal Count is Reached. This Function is Retriggerable.
Rate Generator	Divide by N Counter. The Output will go Low for One Input Clock Cycle, and the Period from One Low Going Pulse to the Next is N Times the Input Clock Period.
Square-Wave Rate Generator	Output will Remain High Until One-Half the Count has been Completed, and go Low for the Other Half of the Count.
Software Triggered Strobe	Output Remains High Until Software Loads Count (N). N Counts After Count is Loaded, Output goes Low for One Input Clock Period.
Hardware Triggered Strobe	Output Goes Low for One Clock Period N Counts After Rising Edge Counter Trigger Input. The Counter is Retriggerable.
Event Counter	On a Jumper Selectable Basis, the Clock Input Becomes an Input from the External System. CPU may Read the Number of Events Occurring After the Counter "Window" has been Enabled or an Interrupt may be Generated After N Events Occur in the System.

face logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 86/05A board provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 86/05A microcomputer. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 86/05A board. An iSBX bus interface specification is available from Intel.

MULTIBUS SYSTEM BUS AND MULTIMASTER CAPABILITIES

Overview

The MULTIBUS system bus (IEEE 796) is Intel's industry standard microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 86/05A board provides full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 86/05A boards or other bus masters to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Interrupt Capability

The iSBC 86/05A board provides 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Intel 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Interrupt Request Generation

Interrupt requests to be serviced by the iSBC 86/05A board may originate from 24 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is also included, to accept a power-fail interrupt in conjunction with a power-supply having AC-low signal generation capabilities, to initiate an orderly shut down of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt Request Line Priorities Fixed at 0 as Highest, 7 as Lowest.
Auto-Rotating	Equal Priority. Each Level, After Receiving Service, Becomes the Lowest Priority Level until next Interrupt Occurs.
Specific Priority	System Software Assigns Lowest Priority Level. Priority of all Other Levels Based in Sequence Numerically on this Assignment.
Polled	System Software Examines Priority-Encoded System Interrupt Status via Interrupt Status Register.

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Bus Interface	Requests from MULTIBUS Resident Peripherals or Other CPU Boards	8; may be Expanded to 64 with Slave 8259A PICs on MULTIBUS Boards
8255A Programmable Peripheral Interface	Signals Input Buffer Full or Output Buffer Empty; also BUS INTR OUT General Purpose Interrupt from Driver/Terminator Sockets	3
8251A USART	Transmit Buffer Empty and Receive Buffer Full	2
8254 Timers	Timer 0, 1 Outputs; Function Determined by Timer Mode	2
iSBX Connectors	Function Determined by iSBX MULTIMODULE Board	4 (2 per iSBX Connector)
Bus Fail Safe Timer	Indicates Addressed MULTIBUS Resident Device has not Responded to Command within 6–10 ms	1
Power Fail Interrupt	Indicates AC Power is not within Tolerance	1
Power Line Clock	Source of 120 Hz Signal from Power Supply	1
External Interrupt	General Purpose Interrupt from Auxiliary (P2) Connector on Backplane	1
iSBC 337A MULTIMODULE Numeric Data Processor	Indicates Error or Exception Condition	1

System Development Environment

Development support for the iSBC 86/05A Board is offered on the System 310 and Series IV Microcomputer Development System from Intel as well as the IBM Personal Computer.

In the Series IV, System 310 and IBM PC development environments, languages offered are Assembler, PLM-86, C, Fortran and Pascal. A powerful software debugger, PSCOPE, is also offered on all development systems. PSCOPE provides Software Trace Execution, defineable breakpoints and user defined/executable debugging procedures.

In-Circuit Emulator

The I²ICE™ In-Circuit Emulator provides the necessary link between the software development environment and the "target" iSBC 86/05A board, the I²ICE In-Circuit Emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

iSDM™ System Debug Monitor

The Intel iSDM System Debug Monitor package contains the necessary hardware, software, cables, EPROMs and documentation required to interface, through a serial or parallel connection, an iSBC 86/05A target system to System 310 or Series IV Intellec® Microcomputer Development System for execution and interactive debugging of applications software on the target system. The Monitor can: load programs into the target system; execute the programs instruction by instruction or at full speed; set breakpoints; and examine/modify CPU registers, memory content, and other crucial environmental details. Additional custom commands can be built using the Command Extension Interface (CEI).

Software Support

The iRMX 86 operating system is offered for development with a System 310 and provides users with a powerful set of system building blocks for developing many different real-time applications. Key iRMX 86 operating system features include multitasking, multiprogramming, interrupt management, device independence, file protection and control, interactive debugging, plus interfaces to many Intel and non-Intel developed hardware and software products.

The iRMX 86 operating system is highly modular and configurable, and includes a sophisticated file management, I/O system, and powerful human interface. The iRMX 86 operating system is also easily customized and extended by the user to match unique requirements.

SPECIFICATIONS

Word Size

Instruction: 8, 16, 24, or 32 bits
Data: 8, 16 bits

System Clock

5.00 MHz or 8.00 MHz ± 0.1% (jumper selectable)

Basic Instruction Cycle

At 8 MHz: 750 ns
250 ns (assumes instruction in the queue)
At 5 MHz: 1.2 sec.
400 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Memory Cycle Time

500 ns cycle time (no wait states requires a memory component access time of 250 ns or less)
RAM: 500 ns
EPROM: Jumper selectable from 500 ns to 875 ns

Memory Capacity/Addressing

JEDEC 24/28 Pin Sites		
Device	**Total Capacity**	**Address Range**
2K × 8	8K bytes	FE000-FFFFF$_H$
4K × 8	16K bytes	FC000-FFFFF$_H$
8K × 8	32K bytes	F8000-FFFFF$_H$
16K × 8	64K bytes	F0000-FFFFF$_H$
32K × 8	128K bytes	E0000-FFFFF$_H$
64K × 8	256K bytes	C0000-FFFFF$_H$
With iSBC® 341 MULTIMODULE™ EPROM/SRAM		
Device	**Total Capacity**	**Address Range**
2K × 8	16K bytes	FC000-FFFFF$_H$
4K × 8	32K bytes	F8000-FFFFF$_H$
8K × 8	64K bytes	F0000-FFFFF$_H$
16K × 8	128K bytes	E0000-FFFFF$_H$
32K × 8	256K bytes	C0000-FFFFF$_H$
64K × 8	512K bytes	80000-FFFFF$_H$

NOTE:
iSBC 86/05A EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMS.

ON-BOARD STATIC RAM

8K bytes — 0-1FFF$_H$

16K bytes— 0-3FFF$_H$ (with iSBC 302 MULTIMODULE Board)

I/O CAPACITY

PARALLEL — 24 programmable lines using one 8255A.

SERIAL — 1 programmable line using one 8251A.

iSBX MULTIMODULE— 2 iSBX single wide MULTIMODULE board or 1 iSBX double-width MULTIMODULE board.

SERIAL COMMUNICATIONS CHARACTERISTICS

SYNCHRONOUS — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

ASYNCHRONOUS— 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit direction.

Baud Rates

Frequency (KHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		+16	+64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
1. Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8254 Timer 2).

TIMERS

Input Frequencies

Reference: 2.46 MHz ±0.1% (0.041 sec. period, nominal); or 153.60 KHz ±0.1% (6.51 sec. period, nominal)

NOTE:
Above frequencies are user selectable

Event Rate: 2.46 MHz max

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63 μs	427.1 ms	3.26s	466.50 min
Programmable One-Shot	1.63 μs	427.1 ms	3.26s	466.50 min
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-Wave Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software Triggered Strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Hardware Triggered Strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Event Counter	—	2.46 MHz	—	—

INTERFACES

MULTIBUS Bus:	All signals TTL compatible
iSBX BUS Bus:	All signals TTL compatible
PARALLEL I/O:	All signals TTL compatible
SERIAL I/O:	RS232C compatible, configurable as a data set or data terminal
TIMER:	All signals TTL compatible
INTERRUPT REQUESTS:	All TTL compatible

Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
MULTIBUS System	86	0.156	Viking Wire Wrap
iSBX Bus			
8-Bit Data	36	0.1	iSBX 960-5
16-Bit Data	44	0.1	iSBX 961-5
Parallel I/O (2)	50	0.1	3M Flat or T1 PINS
Serial I/O	26	0.1	3M Flat or AMP Flat

LINE DRIVERS AND TERMINATORS

I/O Drivers

The following line drivers are all compatible with the I/O driver sockets on the iSBC 86/05A board.

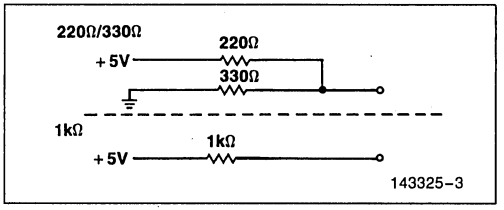
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

NOTES:
I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1K terminators

I/O Terminators

220/330 divider or 1K pullup



MULTIBUS® DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	50
Address	Tri-State	50
Commands	Tri-State	32
Bus Control	Open Collector	20

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.70 in. (1.78 cm)
Weight: 14 oz (388 gm)

ELECTRICAL CHARACTERISTICS

DC Power Requirements

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM(1) RAM only(2)	4.7A 120 mA	25 mA	23 mA
With 8K EPROM(3) (using 2716)	5.0A	25 mA	23 mA
With 16K EPROM(3) (using 2732)	4.9A	25 mA	23 mA
With 32K EPROM(3) (using 2764)	4.9A	25 mA	23 mA

NOTES:
1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 55°C

Relative Humidity: to 90% (without condensation)

REFERENCE MANUAL

Order no. 147162-002—*iSBC 86/05A Hardware Reference Manual* (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

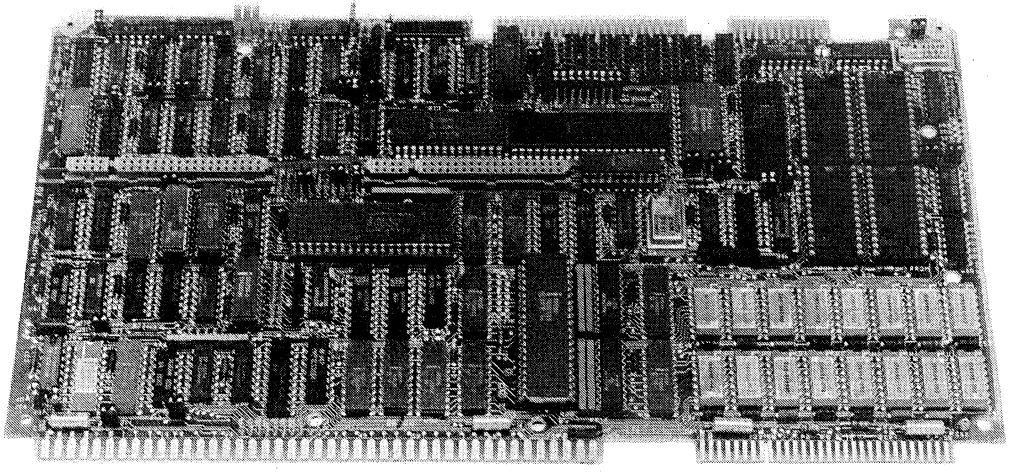
ORDER INFORMATION

Part Number	Description
SBC 86/05A	16-bit Single Board Computer with 8K bytes RAM

iSBC® 86/14 AND iSBC® 86/30 SINGLE BOARD COMPUTERS

- 8086 Microprocessor with 5 or 8 MHz CPU Clock
- Fully Software Compatible with iSBC® 86/12A Single Board Computer
- Optional 8086 Numeric Data Processor with iSBC® 337A MULTIMODULE™ Processor
- 32K/128K bytes of Dual-Port Read/ Write Memory Expandable On-Board to 256K bytes with On-Board Refresh
- Sockets for up to 64K bytes of JEDEC 24/28-pin Standard Memory Devices
- Two iSBX™ Bus Connectors
- 24 Programmable Parallel I/O Lines
- Programmable Synchronous/ Asynchronous RS232C Compatible Serial Interface with Software Selectable Baud Rates
- Two Programmable 16-Bit BCD or Binary Timers/Event Counters
- 9 Levels of Vectored Interrupt Control, Expandable to 65 Levels
- MULTIBUS® Interface for Multimaster Configurations and System Expansion
- Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral Controllers, Packaging and Software

The iSBC 86/14 and iSBC 86/30 Single Board Computers are members of Intel's complete line of OEM microcomputer systems which take full advantage of Intel's technology to provide economical, self-contained, computer-based solutions for OEM applications. Each board is a complete computer system on a single 6.75 x 12.00-in. printed circuit card distinguished by RAM memory content with 32K bytes and 128K bytes provided on the iSBC 86/14 and iSBC 86/30 board, respectively. The CPU, system clock, read/write memory, nonvolatile read only memory, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the boards.



280007-1

September 1987
Order Number: 280007-004

FUNCTIONAL DESCRIPTION

Central Processing Unit

The central processor for the iSBC 86/XX* boards is Intel's iAPX 86/10 (8086-2) CPU. A clock rate of 8 MHz is supported with a jumper selectable option of 5 MHz. The CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers, all accessed by a total of 24 operand addressing modes for comprehensive memory addressing and for support of the data structures required for today's structured, high level languages as well as assembly language.

NOTE:
iSBC 86/XX designates both the iSBC 86/14 and iSBC 86/30 CPU boards.

Instruction Set

The 8086 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the iSBC 337A MULTIMODULE Numeric Data Processor extends the 8086/10 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32, and 64-bit integer, and 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary.

Architectural Features

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 750 nsec minimum instruction cycle to 250 nsec for queued instructions. The stack-oriented architecture readily supports modular programming by facilitating fast, simple, inter-module communication, and other programming constructs needed for asynchronous real-time systems. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

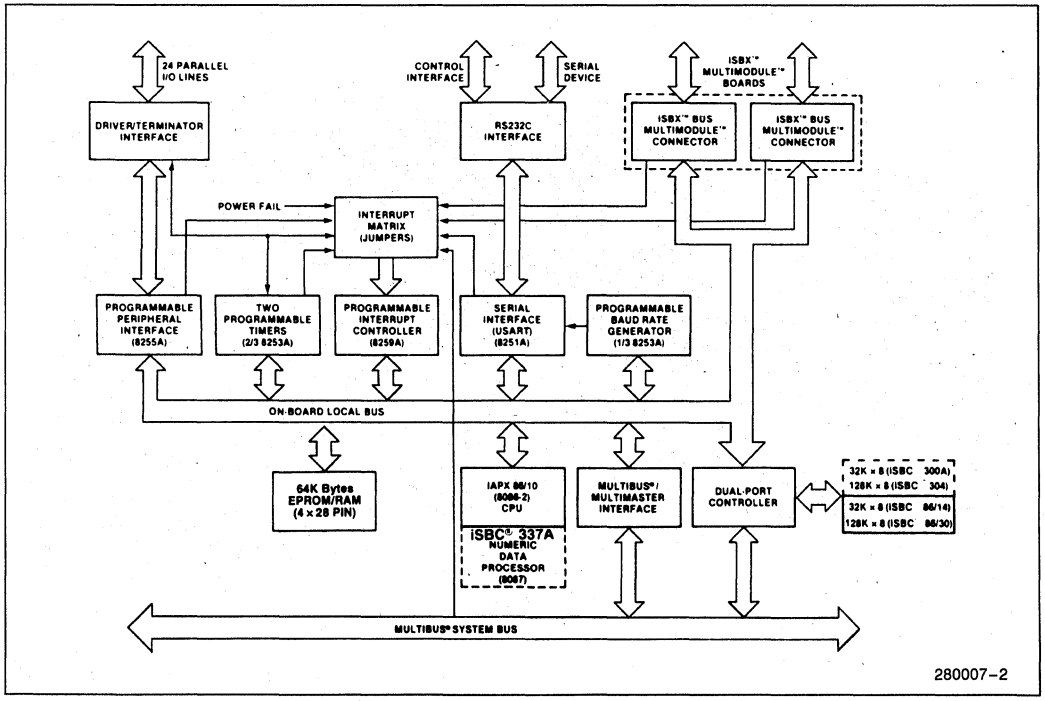


Figure 1. iSBC® 86/XX Block Diagram

RAM Capabilities

The iSBC 86/14 and iSBC 86/30 microcomputers contain 32K bytes and 128K bytes of dual-port dynamic RAM, respectively. In addition, on-board RAM may be doubled on each microcomputer by optionally adding RAM MULTIMODULE boards. The on-board RAM may be expanded to 256K bytes with the iSBC 304 MULTIMODULE Board mounted onto the iSBC 86/30 board. Likewise, the iSBC 86/14 microcomputer may be expanded to 64K bytes with the iSBC 300A MULTIMODULE option. The dual-port controller allows access to the on-board RAM (including RAM MULTIMODULE options) from the iSBC 86/XX boards and from any other MULTIBUS master via the system bus. Segments of on-board RAM may be configured as a private resource, protected from MULTIBUS system access. The amount of memory allocated as a private resource may be configured in increments of 25% of the total on-board memory ranging from 0% to 100% (optional RAM MULTIMODULE boards double the increment size). These features allow the multiprocessor systems to establish local memory for each processor and shared system memory configurations where the total system memory size (including local on-board memory) can exceed one megabyte without addressing conflicts.

EPROM Capabilities

Four 28-pin sockets are provided for the use of Intel 2716s, 2732As, 2764s, 27128s, and their respective ROMs. When using 27128s, the on-board EPROM capacity is 64K bytes. Other JEDEC standard pinout devices are also supported, including byte-wide static RAMs.

Parallel I/O Interface

The iSBC 86/XX Single Board Computers contain 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. In order to take advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators, allowing the selection of the appropriate combination of optional line drivers and terminators with the required drive/termination characteristics. The 24 programmable I/O lines and signal ground lines are brought out to a 50-pin edge connector.

Serial I/O

A programmable communications interface using the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the iSBC 86/XX boards. A software selectable baud rate generator provides the USART with all common communication frequencies. The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The RS232C command lines, serial data lines and signal ground line are brought out to a 26-pin edge connector.

Programmable Timers

The iSBC 86/XX boards provide three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8253 Programmable In-

Table 1. Input/Output Port Modes of Operation

Port	Lines (Qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Latched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X(1)
	4	X		X			X(1)

NOTE:
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.

terval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of two of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller and to the I/O terminators associated with the 8255A to allow external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8253 provides the programmable baud rate generator for the iSBC 86/XX boards' RS232C USART serial port. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation or real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an internal trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

iSBX™ MULTIMODULE™ On-Board Expansion

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 86/XX microcomputers. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 86/XX boards provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 86/XX microcomputers. A broad range of iSBX MULTIMODULE options are available in this family from Intel. Custom iSBX modules may also be designed for use on the iSBC 86/XX boards. An iSBX bus interface specification and iSBX connectors are available from Intel.

MULTIBUS® SYSTEM BUS AND MULTIMASTER CAPABILITIES

Overview

The MULTIBUS system bus is Intel's industry standard microcomputer bus structure. Both 8 and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In its simplest application, the MULTIBUS system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the MULTIBUS structure also allows very powerful distributed processing configurations with multiple processors and intelligent slave I/O, and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. On-

board EPROM capacity may be expanded to 128K by user reprogramming of a PAL device to support 27256 EPROM devices. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 86/XX boards provide full MULTIBUS arbitration control logic. This control logic allows up to three iSBC 86/XX boards or other bus masters, including iSBC 80 family MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Interrupt Capability

The iSBC 86/XX boards provide 9 vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 8086 CPU. This interrupt is typically used for signaling catastrophic events (e.g., power failure). The Intel 8259A Programmable Interrupt Controller (PIC) provides control and vectoring for the next eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available for use in designing

Table 3. Programmable Interrupt Modes

Mode	Operation
Fully Nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-Rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific Priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority-encoded system interrupt status via interrupt status register.

request processing configurations to match system requirements for efficient interrupt servicing with minimal latencies. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from all on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves requests according to the selected mode and, if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked via software, by storing a single byte in the interrupt mask register of the PIC. In systems requiring additional interrupt levels, slave 8259A PICs may be interfaced via the MULTIBUS system bus, to generate additional vector addresses, yielding a total of 65 unique interrupt levels.

Interrupt Request Generation

Interrupt requests to be serviced by the iSBC 86/XX boards may originate from 28 sources. Table 4 includes a list of devices and functions supported by interrupts. All interrupt signals are brought to the interrupt jumper matrix where any combination of interrupt sources may be strapped to the desired interrupt request level on the 8259A PIC or the NMI input to the CPU directly.

Power-Fail Control and Auxiliary Power

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 and iSBC 640 Power Supply or equivalent, to initiate an orderly shut down of the system in the event of a power failure. Additionally, an active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences. An auxiliary power bus is also provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

System Development Capabilities

The development cycle of iSBC 86/XX products can be significantly reduced and simplified by using either the System 86/310 or the Intellec Series IV Microcomputer Development System or the IBM PC.

IN-CIRCUIT EMULATOR

The I²ICE In-Circuit Emulator provides the necessary link between the software development environment and the "target" iSBC 86/XX execution system. In addition to providing the mechanism for loading executable code and data into the iSBC 86/XX boards, the I²ICE In-Circuit Emulator provides a sophisticated command set to assist in debugging software and final integration of the user hardware and software.

PL/M-86

Intel's system's implementation language, PL/M-86, is standard in the System 86/310 and is also available for the Series IV and the IBM PC. PL/M-86 provides the capability to program in algorithmic language and eliminates the need to manage register usage or allocate memory while still allowing explicit control of the system's resources when needed. FORTRAN 86, PASCAL 86 and C86 are also available the Intellec Series IV, 86/310 systems and the IBM PC.

SPECIFICATIONS

Word Size

Instruction: 8, 16, 24, or 32 bits

Data: 8, 16 bits

System Clock

5.00 MHz or 8.00 MHz ±0.1% (jumper selectable)

Cycle Time

BASIC INSTRUCTION CYCLE

8 MHz: 750 ns
250 ns (assumes instruction in the queue)

5 MHz: 1.2 μs
400 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Table 4. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS resident peripherals or other CPU boards.	8; may be Expanded to 64 with Slave 8259A PICs on MULTIBUS Boards
8255A Programmable Peripheral Interface	Signals input buffer full or output buffer empty; also BUS INTR OUT general purpose interrupt from driver/terminator sockets.	3
8251A USART	Transmit buffer empty and receive buffer full.	2
8253 Timers	Timer 0, 1 outputs; function determined by timer mode.	2
iSBX Connectors	Function determined by iSBX MULTIMODULE board.	4 (2 per iSBX Connector)
Bus Fail Safe Timer	Indicates addressed MULTIBUS resident device has not responded to command within 6 ms.	1
Power Fail Interrupt	Indicates AC power is not within tolerance.	1
Power Line Clock	Source of 120 Hz signal from power supply.	1
External Interrupt	General purpose interrupt from auxiliary (P2) connector on backplane.	1
iSBC 337A MULTIMODULE Numeric Data Processor	Indicates error or exception condition.	1
Parity Error	Indicates on-board RAM parity error from iSBC 303 parity MULTIMODULE board (iSBC 86/14 option).	1
Edge-Level Conversion	Converts edge triggered interrupt request to level interrupt.	1
OR-Gate Matrix	Outputs of OR-gates on-board for multiple interrupts.	2

Memory Cycle Time

RAM: 750 ns

EPROM: Jumper selectable from 500 ns to 875 ns

Memory Capacity/Addressing

ON-BOARD EPROM

Device	Total Capacity	Address Range
2716	8K bytes	FE000–FFFFF$_H$
2732A	16K bytes	FC000–FFFFF$_H$
2764	32K bytes	F8000–FFFFF$_H$
27128	64K bytes	F0000–FFFFF$_H$

NOTE:
iSBC 86/XX EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMs. Total EPROM capacity may be increased to 128 bytes by the user reprogramming an on-board PAL.

ON-BOARD RAM

Board	Total Capacity	Address Range
iSBC 86/14	32K bytes	0–07FFF$_H$
iSBC 86/30	128K bytes	0–1FFFF$_H$

WITH MULTIMODULE™ RAM

Board	Total Capacity	Address Range
iSBC 300A (with iSBC 86/14)	64K bytes	0–0FFFF$_H$
iSBC 304 (with iSBC 86/30)	256K bytes	0–3FFFF$_H$

I/O Capacity

Parallel: 24 programmable lines using one 8255A

Serial: 1 programmable line using one 8251A

iSBX MULTIMODULE: 2 iSBX boards

Serial Communications Characteristics

Synchronous: 5–8 bits characters; internal or external character synchronization; automatic sync insertion

Asynchronous: 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit direction

BAUD RATES

Frequency (kHz) (Software Selectable	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTE:
Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register (8253 Timer 2).

Timers

INPUT FREQUENCIES

Reference: 2.46 MHz ±0.1% (0.041 μsec period, nominal); or 153.60 kHz ±0.1% (6.51 μsec period, nominal)

NOTE:
Above frequencies are user selectable.

Event Rate: 2.46 MHz max

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/counter (Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	1.63μs	427.1 ms	3.26s	466.50 min
Programmable One-Shot	1.63 μs	427.1 ms	3.26s	466.50 min
Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Square-Wave Rate Generator	2.342 Hz	613.5 kHz	0.000036 Hz	306.8 kHz
Software Triggered Strobe	1.63μs	427.1 ms	3.26s	466.50 min
Hardware Triggered Strobe	1.63 μs	427.1 ms	3.26s	466.50 min
Event Counter	—	2.46 MHz	—	—

Interfaces

MULTIBUS: All signals TTL compatible

iSBX Bus: All signals TTL compatible

Parallel I/O: All signals TTL compatible

Serial I/O: RS232C compatible, configurable as a data set or data terminal

Timer: All signals TTL compatible

Interrupt Requests: All TTL compatible

Connectors

Interface	Double-Sided Pins	Centers (in.)	Mating Connectors
MUILTIBUS System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
iSBX Bus 8-Bit Data	36	0.1	iSBX 960-5
Parallel I/O (2)	50	0.1	3M 3415-000 Flat or TI H312125 Pins
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

Line Drivers and Terminators

I/O DRIVERS

The following line drivers are all compatible with the I/O driver sockets on the iSBC 86/05 board.

Driver	Characteristics	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

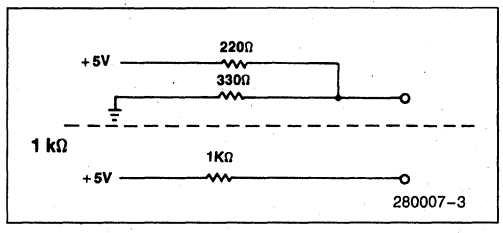
NOTE:
I = inverting; NI = non-inverting; OC = open collector.

Port 1 of the 8255A has 20 mA totem-pole bidirectional drivers and 1 KΩ terminators

I/O TERMINATORS

220Ω/330Ω divider or 1 kΩ pullup

220Ω/330Ω



MULTIBUS® Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-State	32
Address	Tri-State	32
Commands	Tri-State	32
Bus Control	Open Collector	20

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.70 in. (1.78 cm)
Weight: 14 oz (388 gm)

Environmental Characteristics

Operating Temperature: 0°C to 55°C
Relative Humidity: to 90% (without condensation)

Electrical Characteristics

DC POWER REQUIREMENTS

Configuration	Current Requirements (All Voltages ±5%)		
	+5V	+12V	−12V
Without EPROM[1]	5.1A	25 mA	23 mA
RAM only[2]	600 mA	—	—
With 8K EPROM[3] (using 2716)	5.4A	25 mA	23 mA
With 16K EPROM[3] (using 2732A)	5.5A	25 mA	23 mA
With 32K EPROM[3] (using 2764)	5.6A	25 mA	23 mA

NOTES:
1. Does not include power for optional ROM/EPROM, I/O drivers, and I/O terminators.
2. RAM chips powered via auxiliary power bus in power-down mode.
3. Includes power required for 4 ROM/EPROM chips, and I/O terminators installed for 16 I/O lines; all terminator inputs low.

Environmental Characteristics

Operating Temperature: 0°C to 55°C
Relative Humidity: to 90% (without condensation)

Reference Manual

144044-002: iSBC 86/14 and iSBC 86/30 Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

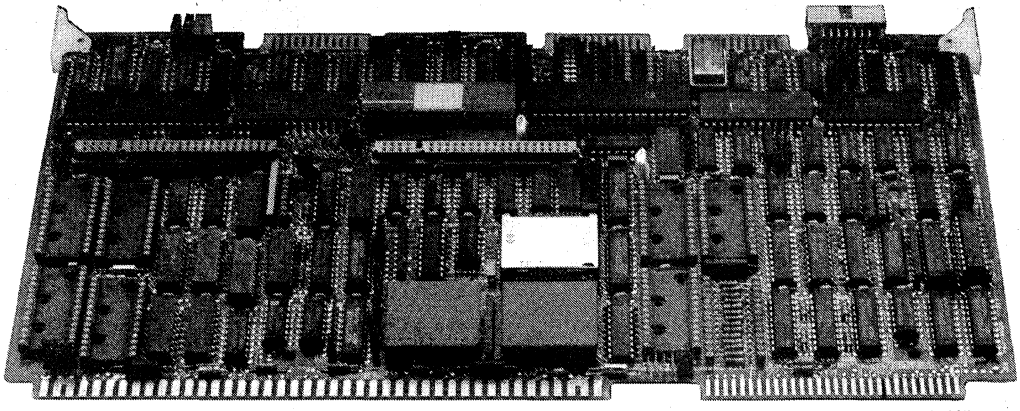
ORDERING INFORMATION

Part Number	Description
SBC 86/14	Single Board Computer
SBC 86/30	Single Board Computer

iSBC® 286/10A SINGLE BOARD COMPUTER

- 8 MHz 80286 Microprocessor
- Supports User Installed 80287 Numeric Data Processor
- iLBX™ Interface for iLBX Memory Board Expansion
- 0 Wait-State Synchronous Interface to EX Memory Expansion Boards
- Eight JEDEC 28-Pin Sites for Optional SRAM/iRAM/EPROM/E²PROM Components
- Optional Expansion to Sixteen JEDEC 28-Pin Sites with Two iSBE® 341 Boards
- Maximum On-Board Memory Capacity 384 KB
- Two iSBX™ Bus Interface Connectors for I/O Expansion
- 16 Levels of Vectored Interrupt Control
- Centronics-Compatible Parallel I/O Printer Interface
- Two Programmable Multiprotocol Synchronous/Asynchronous Serial Interfaces; One RS232C, the Other RS232C or RS422/449 Compatible

The iSBC® 286/10A Single Board Computer is a member of Intel's complete line of microcomputer modules and systems which take advantage of Intel's VLSI technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete microcomputer system on a 6.75 x 12.0 inch printed circuit card. The CPU, system clock, memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers all reside on the board. The iSBC 286/10A board offers both a standard iLBX interface for high-speed memory access to Intel's series of iLBX memory boards and a new, 0 wait-state, synchronous interface for use with Intels EX series of memory boards. The iSBC 286/10A Single Board Computer is fully compatible with its predecessor, the iSBC 286/10A board, and can be used in applications originally designed for the earlier model.



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* XENIX™ is a trademark of MICROSOFT Inc.
* UNIX® is a registered trademark of BELL Labs.

September 1987
Order Number: 280079-005

FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/10A board utilizes the powerful 80286 CPU within the MULTIBUS® system architecture, enhanced by the industry standard iLBX bus and a new, 0 wait-state, synchronous memory interface, to provide a high performance 16-bit solution. This board also includes on-board interrupt, memory and I/O features facilitating a complete signal board computer system. The iSBC 286/10A board is designed to be fully compatible with the iSBC 286/10 board, and only minor changes to software timing loops may be required.

Central Processing Unit

The central processor for the iSBC 286/10A board is the 80286 CPU operating at a 8.0 MHz clock rate. The 80286 CPU is upwardly compatible with Intel's 8088 and iAPX 86 CPUs. The 80286 CPU runs 8088 and 86 code at substantially higher speeds due to it's parallel chip architecture. In some cases, software timing loops may have to be adjusted to accommodate the faster CPU clock. In addition, the 80286 CPU provides on chip memory management and protection and virtual memory addressing of up to 1 gigabyte per task. Numeric processing power may be enhanced with the user installed 80287 numerics processor. The clock rates for the 80286 and the 80287 are independent with the 80287 rate jumper selectable at either 5.3 or 8.0 MHz.

Instruction Set

The 80286 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the 80287 Numeric Data Processor extends the 80286 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The 80287 meets the proposed IEEE P754 standard for numeric data processing and maintains compatibility with 8087-based systems.

Architectural Features

The 8086, 8088, 80186 and the 80286 microprocessor family contains the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088, and 80186 CPUs.

The 80286 operates in two modes: 8086 real address mode, and protected virtual address mode. In 8086 real address mode, programs use real address with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same base instruction set, registers, and addressing modes.

VECTORED INTERRUPT CONTROL

Incoming interrupts are handled by two on-board 8259A programmable interrupt controllers and by the 80286's NMI line. Interrupts originating from up to 16 sources are prioritized and then sent to the CPU as a vector address. Further interrupt capability is available through bus vectored interrupts where slave 8259 interrupt controllers are resident on separate iSBC boards and are then cascaded into the on-board interrupt control.

INTERRUPT SOURCES

Twenty-three potential interrupt sources are routed to the interrupt jumper matrix where the user can connect the desired interrupt sources to specific interrupt levels. Table 1 includes a list of devices and functions supported by interrupts.

MEMORY CAPABILITIES

There are a total of eight 28-pin JEDEC sites on board. Four sites are for local memory and can contain up to 256K bytes of EPROM devices. The four other sites are known as the dual-port memory and may be addressed by the MULTIBUS interface and the on-board CPU bus. Up to 128K bytes of either iRAM, SRAM, EPROM, or E^2PROM can reside in these sites. Both the local and dual-port memory can be expanded to eight sites each by using two iSBC 341 JEDEC expansion modules. In this way, smaller size memory devices can be used up to the 256KB (local) and 128KB (dual-port) memory capacities.

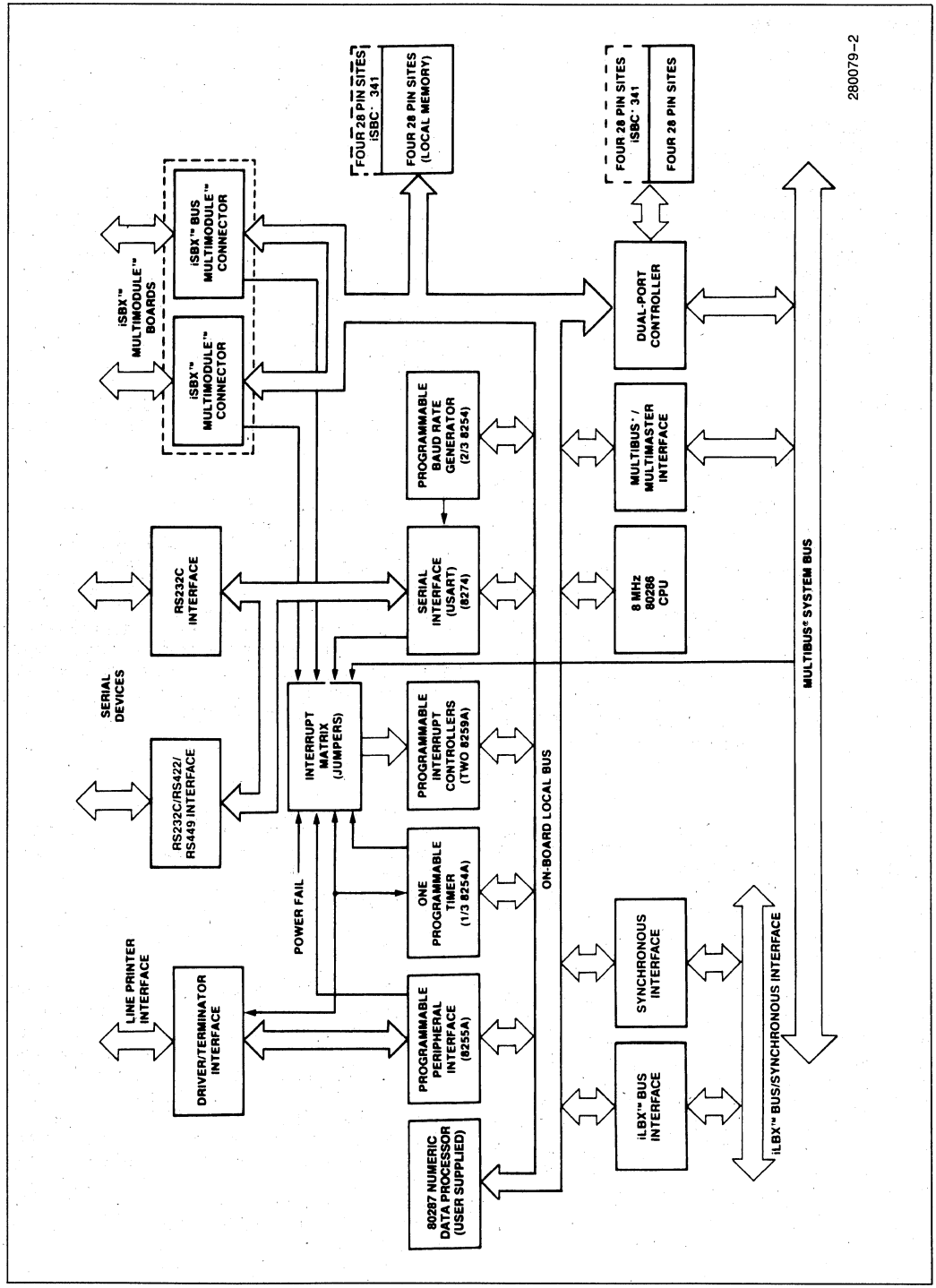


Figure 1. iSBC® 286/10A Block Diagram

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS Resident Peripherals or Other CPU Boards	8*
8259A Programmable Interrupt Conroller	8 Level Vectored Interrupt Request Cascaded to Master 8259A	1
8274 Serial Controller	8 Level Vectored Interrupt Request Cascaded to Master 8259A	1
8255A Line Printer Interface	Signals Output Buffer Empty	1
8254 Timers	Timer 0, 1 Outputs; Function Determined by Timer Mode	2
iSBX Connectors	Function Determined by iSBX MULTIMODULE Board	4 (2 per iSBX™ Connector)
Bus Fail Safe Timer	Indicates Addressed MULTIBUS Resident Device Has not Responded to Command within 6 ms	1
Power Fail Interrupt	Indicates AC Power Is not within Tolerance	1
External Interrupt	General Purpose Interrupt from Auxiliary Connector, Commonly Used as Front Panel Interrupt	1
On-Board Logic	Conditioned Interrupt Source from Edge Sense Latch, Inverter, or OR Gate	3

* May be expanded to 56 with slave 8259A PICs on MULTIBUS* boards

SERIAL I/O

A two channel serial communications interface using Intel's 8274 Multi-Protocol Serial Controller (MPSC) is contained on the iSBC 286/10 board. Two independent software selectable baud rate generators provide the MPSC with all common communication frequencies. The protocol (i.e., asynchronous, IBM* bisync, or SDLC/HDLC), data format, control character format, parity and baud rate are all under program control. Software interfacing to the MPSC can be via either a polled or interrupt driven routine. One channel may be configured for an RS232C or RS422/RS449 interface with the other channel RS232C only. The data, command and signal ground lines for each channel are brought out to two 26-pin edge connectors.

PROGRAMMABLE TIMERS

The iSBC 286/10A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller or to the 8274 MPSC to count external events or provide baud rate generation. The third interval timer in the 8254 is dedicated to providing a clock for the programmable baud rate generator in the iSBC 286/10A board's MPSC serial controller. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

LINE PRINTER INTERFACE

An 8255A Programmable Peripheral Interface (PPI) provides a line printer interface, several on-board functions, and four non-dedicated input bits. Drivers are provided for a complete Centronics compatible line printer interface. The on-board functions implemented with the PPI are power fail sense, override, NMI mask, non-volatile RAM enable, clear timeout interrupt, LED 0 and 1, clear edge sense flop, MULTIBUS interrupt, and serial channel A loopback. The PPI's I/O lines are divided into three eight bit ports: A, B, and C. Four non-dedicated input bits allow the state of four user-configured jumper connections to be input. The PPI must be programmed for mode 0 with ports A and C used as outputs and port B as input. A 16-bit write to Port B is used to set the iSBC 286/10A board into 24-bit address mode. The parallel port assignment is shown in Table 3.

Table 2. Programmable Time Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Even Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

Table 3. Parallel Port Bit Assignment

Port A—Output	
Bit	**Function**
0	Line Printer Data Bit 0
1	Line Printer Data Bit 1
2	Line Printer Data Bit 2
3	Line Printer Data Bit 3
4	Line Printer Data Bit 4
5	Line Printer Data Bit 5
6	Line Printer Data Bit 6
7	Line Printer Data Bit 7
Port B—Input	
Bit	**Function**
0	General Purpose Input 0
1	General Purpose Input 1
2	General Purpose Input 2
3	General Purpose Input 3
4	Line Printer ACK/ (Active Low)
5	Power Fail Sense/ (Active Low)
6	Line Printer Error (Active Hi)
7	Line Printer Busy (Active Hi)
Port C—Output	
Bit	**Function**
0	Line Printer Data Strobe (Active Hi)
1	Override/ (Active Low)
2	NMI Mask (0 = NMI Enabled)
3	Non-Volatile RAM Enable; Clear Timeout Interrupt/
4	LED 0 (1 = On); Clear Edge Sense Flop/
5	MULTIBUS Interrupt (1 = Active)
6	Serial CHA Loopback (0 = Online, 1 = Loopback)
7	LED 1 (1 = 0n); Clear Line Printer Ack Flop/

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the MULTIMODULE expansion bus as shown in Figure 2. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The local bus extension allows large amounts of high performance memory to be accessed from a CPU board over a private bus. The MULTIMODULE extension bus is a means of adding inexpensive I/O functions to a base CPU board. Each of these three bus structures are implemented on the iSBC 286/10A board providing a total system architecture solution.

SYSTEM BUS—IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a board array of board level products. VLSI interface components, detailed published specifications and application notes.

SYSTEM BUS—EXPANSION CAPABILITIES

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, bubble memory boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

SYSTEM BUS—MULTIMASTER CAPABILITIES

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 286/10A board provides full system bus arbitration control logic. This control logic allows up to three iSBC 286/10A board or other bus masters, including the iSBC 80 board family of MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to multiprocessing configuration made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

HIGH SPEED OFF-BOARD MEMORY

The iSBC 286/10A board can access off-board memory either over the MULTIBUS (P1) interface, or over the P2 interface as shown in Figure 3. Memory transfers over the P2 interface are faster because the CPU board doesn't have to arbitrate for access to the MULTIBUS interface.

Using the P2 interface, the iSBC 286/10A Board can be configured to operate with either a standard iLBX interface or with a high-performance, synchronous interface.

The iSBC 286/10A Board as supplied is configured to operate with a synchronous, P2 interface. This high-performance interface is designed to connect to Intel's new EX series of memory expansion boards to yield a CPU to memory read/write time of 0 wait-states. The EX memory expansion boards are available in sizes ranging from 512K bytes up to 4M

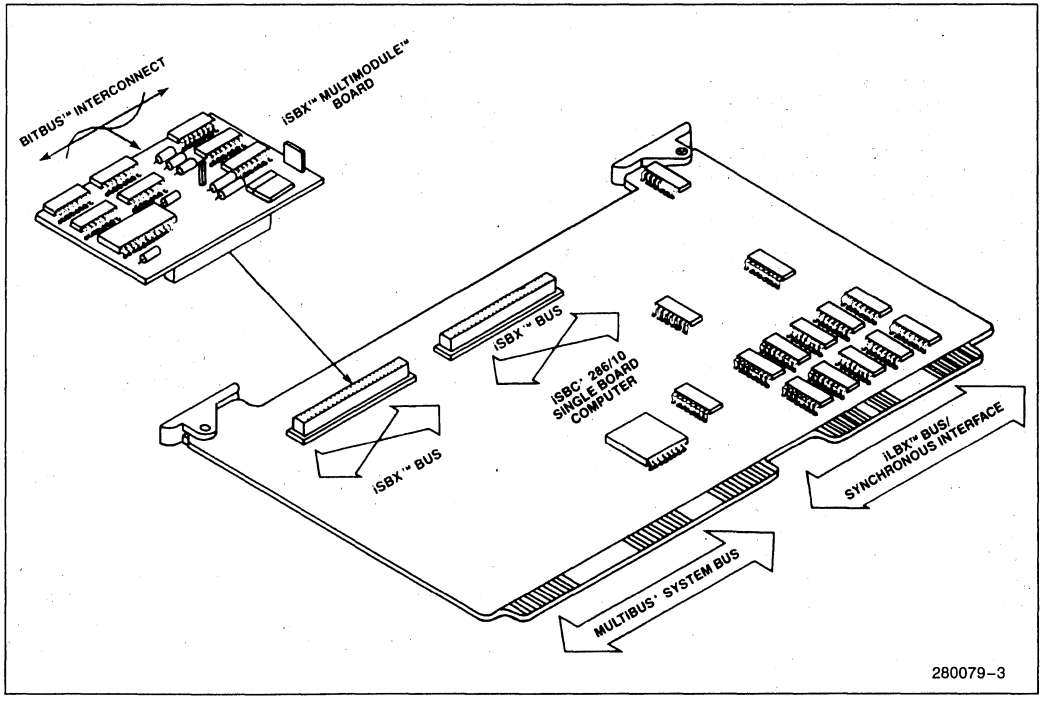


Figure 2. MULTIBUS® System Architecture

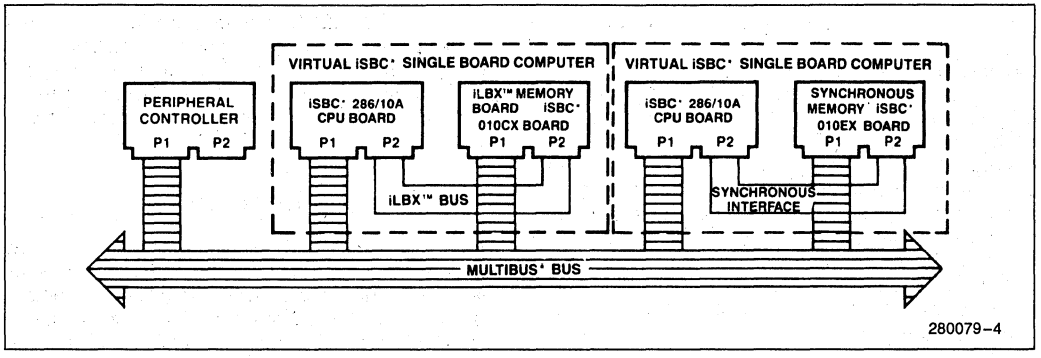


Figure 3. MULTIBUS®/iLBX™/Synchronous Interface Configurations

bytes and available in sizes ranging from 512K bytes up to 2M bytes. Memory expansion boards from other manufacturers that meet the iLBX standard may also be used. CPU to memory access time is usually 1 or more wait-states depending on the speed of the memory used.

A total of four memory boards can be placed on the iLBX or synchronous interface bus. With 4M byte memory boards, this results in a total of 16M bytes on the memory expansion bus.

iSBX™ BUS MULTIMODULE™ ON-BOARD EXPANSION

Two 8/16-bit iSBX MULTIMODULE connectors are provided on the iSBC 286/10A microcomputer board. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULEs optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., bubble cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS Board form factor compatible boards. The iSBX interface connectors on the iSBC 286/10A provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 286/10A microcomputer board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification and iSBX connectors are available from Intel.

Software Support

Software support from Intel includes the iRMX 86, iRMX 286, and XENIX* operating systems, assembly and high level languages, development systems, in-circuit emulators, and various other hardware and software tools.

For those applications needing a real-time, multitasking operating system, Intel offers the iRMX 86 and iRMX 286 operating systems. The iRMX operating systems are particularly well suited for industrial or commercial applications where the processor is simultaneously controlling multiple, real-time, interrupt intensive processes. Typical applications include machine and process control, data aquisition, signal processing, front-end processing, and digital PABX control. The iRMX operating systems employ a highly configurable, modular structure that allows easy system configuration and expansion.

The iRMX 86 operating system enables the iSBC 286/10A board to address up to 1MB of memory in real address mode. Using the iRMX 286 operating system, this address range is extended to 16 MB in native mode. The iRMX 286 operating system also allows the user to take advantage of the hardware traps built into the 80286 processor that provide expanded debug capabilities and increased code reliability.

Application code written for the iRMX 86 operating system can be compiled using 286 compilers to run under the iRMX 286 operating system. Application code will require only minor changes.

Assembly and many high level languages are supported by the iRMX operating systems and Intellec® Series IV development systems. Language support for the iSBC 286/10A board in real address board

includes Intel's ASM 86, PL/M 86, PASCAL 86, FORTRAN 86, and C86, as well as many third party 8086 languages. Language support for native address mode include ASM 286, PL/M 286, PASCAL 286 and FORTRAN 286. Programs developed in these languages can be downloaded from an Intel System 310 or Series IV Development System to the iSBC 286/10A board via the iSDM System Debug Monitor. The iSDM monitor also provides on-target program debugging support including breakpoint and memory examination features.

Intel also offers the XENIX operating system which is designed for those applications needing an interactive, multiple user system. Typical applications include small business systems, software development/engineering workstations, distributed data processing, communications, and graphics.

Intel's XENIX operating system is a fully licensed derivative of UNIX*, enhanced by Intel to provide device driver support for Intel board and component products plus other features that yield greater flexibility, increased reliability, and easier configurability. Intel's XENIX operating system has been optimized for use with the 80286 microprocessor and supports such features as on-chip memory management and protection which provide ease of portability and higher performance.

Applications software can be written in either Intel's FORTRAN, COBOL, or BASIC languages using a XENIX-based, Intel 286/310 or 286/380 system, or by using an Intel iDIS™ Database Information System. The user can also select from a wide variety of existing third party languages and applications software.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, 32 or 40 bits
Data—8 or 16 bits

System Clock

CPU—8.0 MHz
Numeric Processor—5.3 or 8.0 MHz (Jumper Selectable)

Cycle Time

Basic Instruction—8.0 MHz—375 ns; 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles)

Local Memory

Number of sockets—Four 28-pin JEDEC sites, expandable to 8 sites using iSBC 341 JEDEC Expansion Module

Maximum Size—256 KB

Compatible Devices—EPROM, up to 64K x 8 (Intel 27512)

Dual-Port Memory

Number of sockets—Four 28-pin JEDEC sites, expandable to 8 sites using iSBC 341 JEDEC Expansion Module

Maximum Size—128 KB

Compatible Devices—EPROM, up to 32K x 8 (Intel 27256)

SRAM
iRAM, up to 8K x 8 (Intel 2186)
E^2PROM, up to 2K x 8 (Intel 2817A)

Off-Board Physical Memory

Operating System	Address Mode	Size
iRMX 86 Rlse. 6	Real	1MB
iRMX 286 Rlse. 1	Native	16 MB
XENIX Rlse. 3	Native	16 MB

I/O Capability

Parallel—Line printer interface, on-board functions, and four non-dedicated input bits

Serial—Two programmable channels using one 8274 device

Timers—Three programmable timers using one 8254 device

Expansion—Two 8/16-bit iSBX MULTIMODULE connectors

BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)				
	Synchronous	Asynchronous			
Reference: 1.23 MHz	÷1	÷1	÷16	÷32	÷64
615.	615,000	615,000	38,400	19,200	9,600
307.	307,000	307,000	19,200	9,600	4,800
154.	154,000	154,000	9.600	4,800	2,400
76.8	76,800	76,800	4,800	2,400	1,200
56.0	56,000	—	—	—	—
38.4	38,400	38,400	2,400	1,200	600
19.2	19,200	19,200	1,200	600	300
9.6	9,600	9.600	600	300	150
4.6	4,800	4,800	300	150	75
2.4	2,400	2,400	150	75	—
1.2	1,200	1,200	75	—	—
0.6	600	600	—	—	—

Serial Communications Characteristics

Synchronous—5–8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity

Asynchronous—5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity

Interrupt Capacity

Potential Interrupt Sources—25, 5 fixed, 20 jumper selectable

Interrupt Levels—16 vectored requests using two 8259As and the 80286's NMI line.

Timers

Input Frequencies—1.23 MHz ±0.1% or 3.00 MHz ±0.1% (Jumper Selectable)

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	667 ns	53.3 ms	1.33 μs	58.2 min
Programmable One-Shot	667 ns	53.3 ms	1.33 μs	58.2 min
Rate Generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Square-Wave Rate Generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Software Triggered Strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Hardware Triggered Strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Event Counter	—	8.0 MHz	—	—

MATING CONNECTORS (OR EQUIVALENT PART)

Function	# of Pins	Centers (in)	Connector Type	Vendor	Vendor Part No.
iSBX Bus Connector 16-Bit (J5, J6)	44	0.1	Soldered	Viking	000293-001
I/O Connectors (J1–J3)	26	0.1	Flat Crimp	3M	3462-0001
Front Panel Connector (J4)	14	0.5	Flat Crimp	3M	3385-6014
iLBX/Synch. Interface Edge Connector (P2)	60	0.1	Flat Crimp	KEL-AM T & B Ansley	RF30-2803-5 A3020

INTERFACES

MULTIBUS Bus—All signals TTL compatible

iSBX Bus—All signals TTL compatible

iLBX Bus—All signals TTL compatible

Synchronous Interface—All signals TTL compatible

Serial I/O—Channel A: RS232C/RS422/RS449 compatible, DCE or DTE; Channel B; RS232C compatible, DCE only

NOTE:
User supplied 34487 line driver and SIP termination resistor need to be installed for RS422/RS499 operation.

Timer—All signals TTL compatible

Interrupt Requests—All TTL compatible

MULTIBUS® DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	16
Address	Tri-State	16
Commands	Tri-State	32
Bus Control	Open Collector	20

iLBX™ DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	9
Address	Tri-State	20
Commands	Tri-State	8
Bus Control	TTL	8

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.4 in. (1.0 cm)
Minimum Slot Spacing: 0.6 in. (1.5 cm)
Weight: 14 oz. (397 gm)

Electrical Characteristics

DC Power Requirements: +5V, 7.0A; ±12V, 50 mA (serial I/O)

NOTE:
Does not include power for optional EPROM, E^2PROM, or RAM memory devices, or installed MULTIMODULE boards

Environmental Characteristics

Operating Temperature: 0°C to 60°C with 7 CFM airflow across board

Relative Humidity: to 90% (without condensation)

Reference Manual

147532-001—iSBC® 286/10A Hardware Reference Manual (order separately)

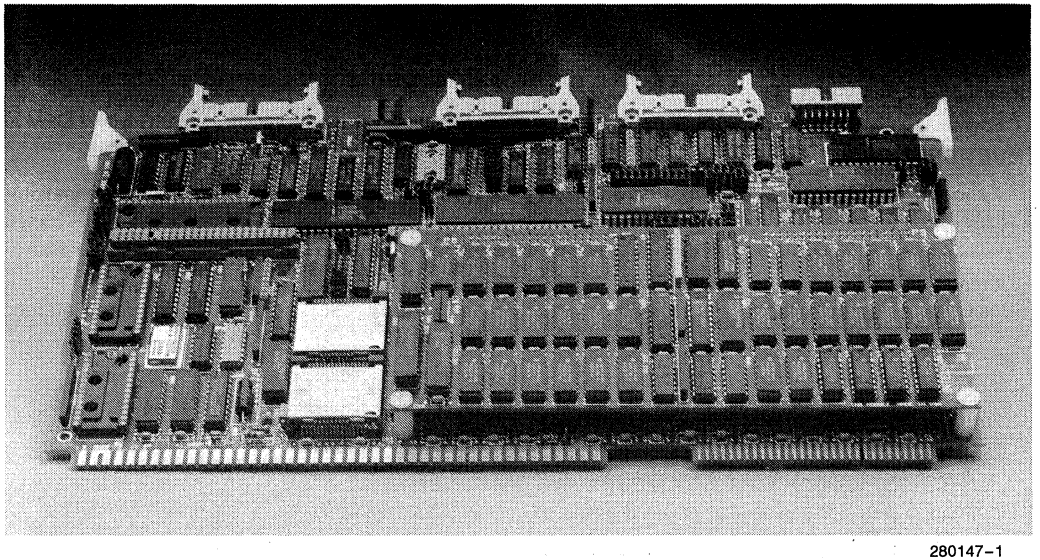
ORDERING INFORMATION

Part Number	Description
SBC 286/10A	Single Board Computer

iSBC® 286/12, 286/14, 286/16 SINGLE BOARD COMPUTERS

- 8 MHz 80286 Microprocessor
- Two JEDEC 28-Pin Sites for up to 128K Bytes of Local EPROM Memory, Expandable to 256K Bytes Using an iSBC® 341 Expansion Module
- 1, 2, or 4 Megabyte, 0 Wait-State, Dual-Port, Parity Memory
- Supports User Installed 80287 Numeric Data Processor and 82258 Advanced DMA Controller Devices
- Two iSBX™ Bus Interface Connectors for I/O Expansion
- Synchronous High-Speed Interface for 0 Wait-State Read/Write to EX Memory Expansion Boards
- iLBX™ Interface for iLBX Memory Board Expansion
- 16 Levels of Vectored Interrupt Control
- Centronics-Compatible Parallel I/O Printer Interface
- Two Programmable Multiprotocol Synchronous/Asynchronous Serial Interfaces; One RS232C, the Other RS232C or RS422/449 Compatible

The iSBC 286/12, iSBC 286/14, and iSBC 286/16 Single Board Computers are members of Intel's high performance family of 16-bit microcomputers. The boards feature an 80286 microprocessor running at 8 MHz together with 1, 2, or 4 megabytes of dual-ported, 0 wait-state, parity memory. These features make the iSBC 286/12/14/16 boards the ideal single board solution for applications requiring high performance and up to 1, 2, or 4 megabytes of memory. For those applications needing more memory, up to four memory expansion boards may be connected to the iSBC 286/12/14/16 boards over its P2 interface. The P2 interface supports both standard iLBX memory boards and Intel's EX series of synchronous, 0 wait-state, memory boards that provide up to 16 megabytes of system memory. The iSBC 286/12/14/16 boards also feature two sockets for user installed 80287 Numeric Data Processor and 82258 Advanced Direct Memory Access Controller devices. These components further increase board performance by off-loading time intensive tasks from the 80286 microprocessor. The iSBC 286/12/14/16 CPU boards are true single-board solutions that also include two serial I/O channels, one parallel line printer channel, local memory, interrupt controllers and programmable timers all on one board.



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*XENIX is a registered trademark of Microsoft Corp.

**UNIX is a trademark of Bell Laboratories.

September 1986
Order Number: 280147-002

FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/12/14/16 boards utilizes the powerful 80286 CPU within the MULTIBUS® system architecture, enhanced by the industry standard iLBX bus and a new, 0 wait-state, synchronous memory interface, to provide a high-performance 16-bit solution. This board features 1, 2, or 4 megabytes of dual-port, 0 wait-state, parity memory, plus interrupt, memory and I/O features facilitating a complete single-board computer system. The iSBC 286/12/14/16 boards can be used in many applications originally designed for Intel's other 16-bit microcomputers. Only minor changes to the system hardware or applications software may be required to match the application to the iSBC 286/12/14/16 boards. These changes may include adjusting software timing loops, changing the (jumper) default configuration of the board, and using pin and socket I/O connectors in place of edge connectors.

Central Processing Unit

The central processor for the iSBC 286/12/14/16 board is the 80286 CPU operating at an 8.0 MHz clock rate. The 80286 CPU is upwardly compatible with Intel's 8088 and 8086 CPUs. The 80286 CPU runs 8088 and 8086 code at substantially higher speeds due to its parallel architecture. In addition, the 80286 CPU provides on-chip memory management and protection and virtual memory addressing of up to 1 gigabyte per task. Processing speed and efficiency may be further enhanced by installing an 80287 numerics coprocessor and an 82258 ADMA controller. The clock rates for the 80286 and the 80287 are independent with the 80287 rate jumper selectable at either 5.3 MHz or 8.0 MHz.

Instruction Set

The 80286 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

Numeric Data Processor

For enhanced numerics processing capability, the 80287 Numeric Data Processor extends the 80286 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental,

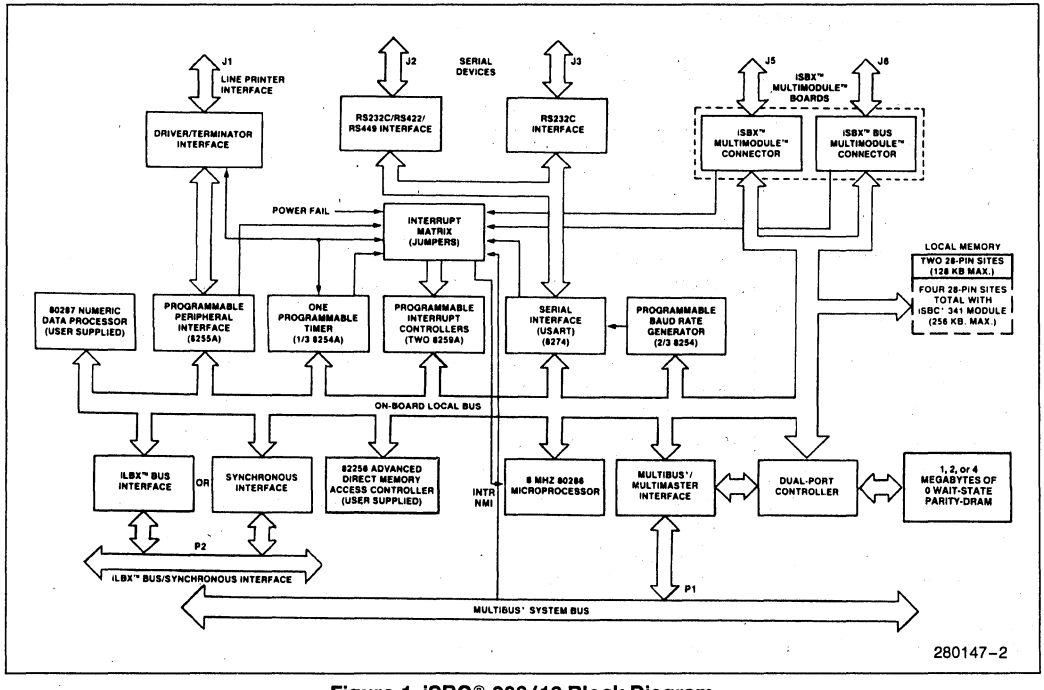


Figure 1. iSBC® 286/12 Block Diagram

logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The 80287 meets the IEEE P754 standard for numeric data processing and maintains compatibility with 8087-based systems.

Advanced DMA Controller

For those applications that require frequent moving of large blocks of data, the user may install an Intel 82258, 4 channel, advanced DMA (ADMA) controller to further increase system performance. The ADMA Controller supports DMA requests from the 8274 USART (2 channels) and the iSBX interfaces on the board (1 per interface). The ADMA can also perform data transfers over the on-board CPU bus, the MULTIBUS (P1) interface, and the iLBX/synchronous (P2) interface. With this arrangement, the device can rapidly move blocks of data between the iSBC 286/12/14/16 boards and iSBX MULTIMODULE™ Boards installed on the baseboard, between the iSBC 286/12/14/16 boards and other boards installed in the system, or between any other memory/controller/I/O boards installed in the system.

ARCHITECTURAL FEATURES

The 8086, 8088, 80186 and 80286 microprocessor family contains the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088, and 80186 CPUs.

The 80286 operates in two modes: 8086 real address mode, and protected virtual address mode. In 8086 real address mode, programs use real address with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same base instruction set and registers.

Vectored Interrupt Control

Incoming interrupts are handled by two on-board 8259A programmable interrupt controllers (PIC) and by the 80286's NMI line. Interrupts originating from up to 15 sources are prioritized and then sent to the CPU. The 8259 devices support both polled and vectored mode of operation. Further interrupt capability is available through bus vectored interrupts where slave 8259 interrupt controllers resident on separate iSBC Boards supply an interrupt vector to the on-board CPU.

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS resident peripherals or other CPU boards	8*
8259A Programmable Interrupt Controller	8 level vectored interrupt request from slave 8259A	1
8274 Serial Controller	6 internal interrupt requests directed to master 8259A	1
8255A Line Printer Interface	Signals output buffer empty. Directed to slave PIC	1
8254 Timers	Timer 0, 1 outputs; function determined by timer mode	2
iSBX connectors	Function determined by iSBX MULTIMODULE board Directed to slave PIC	2 per iSBX Connector
Bus Fail Safe Timer	Indicates addressed MULTIBUS resident device has not responded to command within 10 ms	1
Power Fail Interrupt	Indicates AC power is not within tolerance (from power supply)	1
ADMA Interrupt	Common interrupt for 4 DMA channels	1
Parity Interrupt	Parity error indicator from memory module	1
On-Board Logic	Conditioned interrupt source from edge sense latch, inverter, or OR gate	3
Bus Request Error	Indicates CPU was unable to access the MULTIBUS interface	1
External Interrupt	Supports system front panel reset switch	1

NOTE:
*May be expanded to 56 with slave 8259A PICs on MULTIBUS boards.

Interrupt Sources

Twenty-six potential interrupt sources are routed to the slave PIC device and to the interrupt jumper matrix where the user can connect the desired interrupt sources to specific interrupt levels. Table 1 includes a list of devices and functions supported by interrupts.

Memory Capabilities

DUAL-PORT MEMORY

The iSBC 286/12/14/16 boards feature 1, 2, or 4 megabytes of 0 wait-state, parity memory installed on the board. This memory, which is implemented using 256 Kb or 1 Mb DRAMs installed on a daughter board, is dual-ported to the on-board CPU bus and the MULTIBUS (P1) interface. For those applications requiring more memory, the iSBC 286/12/14/16 boards also feature an iLBX and synchronous memory interface to increase physical memory capacity to 16 megabytes.

LOCAL MEMORY

Two, 28-pin sites are provided for installing up to 128 KB of EPROM firmware.

By installing an iSBC 341 EPROM expansion module, local memory can be increased to four sites to support up to 256 KB of EPROM. Local memory access time is selectable at one, two, or three wait-states and is a function of the speed of the devices used.

Serial I/O

A two-channel serial communications interface using Intel's 8274 Multi-Protocol Serial Controller (MPSC) is contained on the iSBC 286/12/14/16 boards. Two independent software selectable baud rate generators (⅔ of the 8254 timer) provide the MPSC with all common communication frequencies. The protocol (i.e. asynchronous, bisync, or SDLC/HDLC), data format, control character format, parity and baud rate are all under program control. Software interfacing to the MPSC can be via either a polled or interrupt driven routine. Channel A may be configured for an RS232C or RS422/RS449 interface; channel B is set for RS232C operation only. DMA operation for channel A is available if the optional 82258 (ADMA) is installed. The data, clock, control, and signal ground lines for each channel are brought out to two 26-pin, pin and socket connectors.

Programmable Timers

The iSBC 286/12/14/16 boards provide three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller or to the 8274 MPSC to count external events or provide baud rate generation. The third interval timer in the 8254 is dedicated to providing a clock for the programmable baud rate generator in the iSBC 286/12/14/16 boards' MPSC serial controller. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When a terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Outputs goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

Line Printer Interface/Board ID

An 8255A Programmable Peripheral Interface (PPI) provides a Centronics compatible line printer interface, several on-board functions, and four non-dedicated input bits. Drivers are provided for a complete Centronics compatible line printer interface. The on-board functions implemented with the PPI are Power Fail Sense, Lock Override, NMI Mask, Clear Timeout Interrupt, LED 1 and 4, Clear Edge Sense flop, and MULTIBUS interface directed interrupts (2). The PPI's I/O lines are divided into three eight bit ports; A, B, and C. The PPI must be programmed for mode 0 with ports A and C used as outputs and port B as input. A 16-bit write to Port B is used to set the iSBC 286/12/14/16 boards into 24 bit address mode.

Table 3. Parallel Port Bit Assignment

Port A—Output	
Bit	**Function**
0	Line Printer Data Bit 0
1	Line Printer Data Bit 1
2	Line Printer Data Bit 2
3	Line Printer Data Bit 3
4	Line Printer Data Bit 4
5	Line Printer Data Bit 5
6	Line Printer Data Bit 6
7	Line Printer Data Bit 7
Port B—Input	
Bit	**Function**
0	Board ID Bit 0
1	Board ID Bit 1
2	Board ID Bit 2
3	LPT Interrupt (Active High)
4	Line Printer ACK/(Active Low)
5	Power Fail Sense/(Active Low)
6	Line Printer Error (Active High)
7	Line Printer Busy (Active High)
Port C—Output	
Bit	**Function**
0	Line Printer Data Strobe (Active High)
1	Override/(0 = lock asserted)
2	NMI Mask (0 = NMI Enabled)
3	Clear Timeout Interrupt (Active High)
4	LED 0 (1 = On); Clear Edge Sense Flop/
5	MULTIBUS Interrupt 1 (Active High)
6	MULTIBUS Interrupt 2 (Active High)
7	LED 1 (1 = On); Clear Line Printer ACK Flop/(Active High)

Three jumpers on the iSBC 286/12/14/16 boards let the software determine, by examining bits 0, 1, and 2 of port B, the board type (iSBC 286/10A board or iSBC 286/12/14/16 board), and the presence of hardware options (82258 ADMA and 80287 Numeric Data Processor devices) installed on the board. The parallel port assignment is shown in Table 3.

Software Reset

The software reset feature allows the 80286 microprocessor to return to Real Address mode operation from PVAM under software control. The system reset line (INIT*) and the dual-port memory are not affected, and all I/O context is preserved. The software reset is activated by a byte write to I/O location 00E0H. To distinguish the software reset from a true system initialization reset, a flag is provided. Another flag is provided that indicates whether the iSBC 286/12/14/16 board hardware (not the 80286 device) is currently configured for PVAM or Real Address Mode.

Front Panel Connector—J4

A 14-pin connector is mounted on the top edge of the board and is designed to connect to the front panel and power supply of the system enclosure. Leads supported include Reset and Interrupt input lines from (conditioned) front panel switches, a Run signal to drive a front panel LED, a Power Fail Interrupt line that connects to the power supply, and extra power and ground leads to support miscellaneous front panel circuitry.

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the iSBX MULTIMODULE expansion bus as shown in Figure 2. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The local bus extension allows large amounts of high performance memory to be accessed from a CPU board over a private bus. The MULTIMODULE extension bus is a means of adding inexpensive I/O functions to a base CPU board. Each of these three bus structures are implemented on the iSBC 286/12/14/16 boards providing a total system architecture solution.

System Bus—IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a broad array of board level products, VLSI interface components, detailed published specifications and application notes.

System Bus—Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MUTLIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, bubble memory boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

System Bus—Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 286/12/14/16 boards provide full system bus arbitration control logic. This control logic allows up to three iSBC 286/12/14/16 boards or other bus masters, including the iSBC 80 Board family of MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy

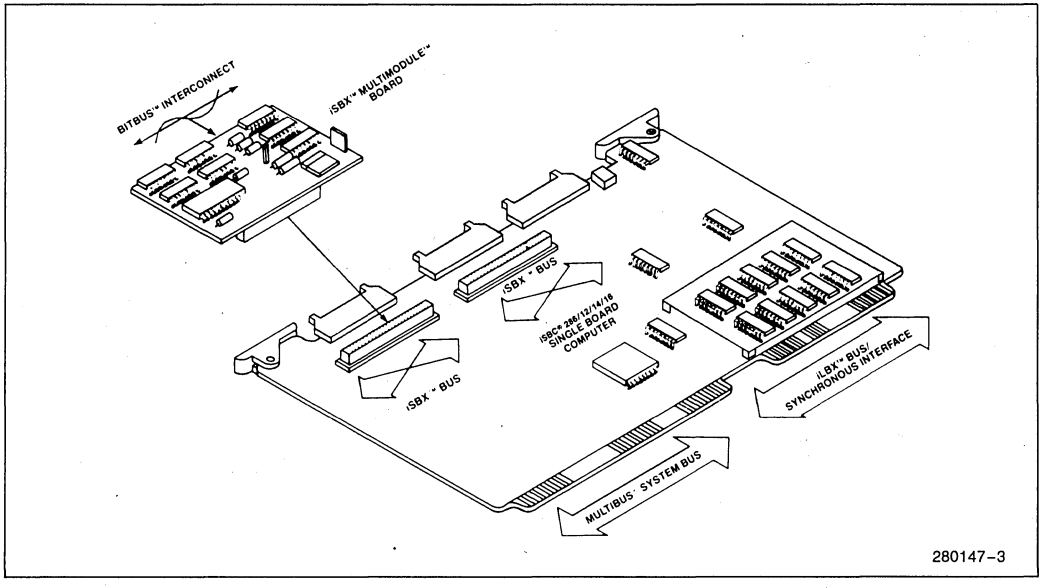


Figure 2. MULTIBUS® System Architecture

chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to multiprocessing configuration made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Memory Map

The memory map of the iSBC 286/12/14/16 board is shown in Figure 3. The memory maps for the iSBC 286/14 and iSBC 286/16 boards are similar, except the total amount of on-board DRAM memory is 2 or 4 MB, and the dual-port memory space is larger. The memory map, which shows the default configuration of the board, may be easily changed by the user to meet the needs of almost any system design. As a result, the iSBC 286/12/14/16 boards are particularly suited for complex multiple processor and/or multiple intelligent I/O board-based systems.

The memory map can be changed by moving on-board jumpers or by installing user-programmed PALs (programmable array logic devices).

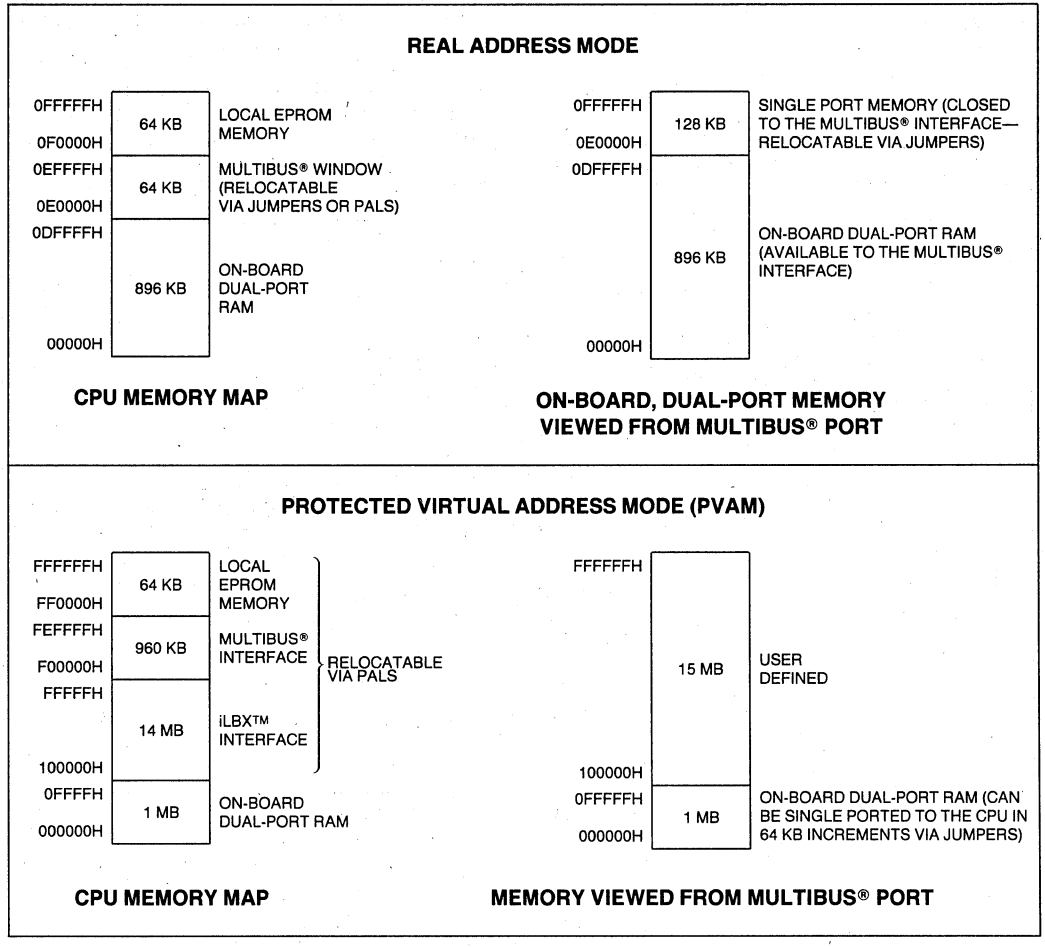


Figure 3. Memory Map for iSBC® 286/12 Board (Default Configuration)

Using only the jumpers on the iSBC 286/12/14/16 board, the MULTIBUS window size can be set at 0 (no window), 64 KB, 128 KB, 256 KB, or 1 MB in real address mode. The MULTIBUS window is normally not available in PVAM, however, a PAL may be programmed to provide this feature. Jumpers are also used to set aside a portion of the dual-port memory so that it may only be accessed by the CPU (single-ported memory). Block sizes of 64 KB, 128 KB, 256 KB, 512 KB or 1 MB may be selected. Finally, jumpers are used to select any of 6 EPROM memory sizes ranging from 4 KB (using 2716 devices) up to 256 KB (using 27512 devices and an iSBC 341 module).

If the user needs to alter the memory map further, five PALs on the baseboard are socketed and may be replaced by custom designed devices. Using programmed PALs, the designer can:

— Set the base DRAM memory starting address (as viewed by the 80286 microprocessor) at 0 (default configuration) or to any ½ megabyte boundary up through 16 MB (0 or 512 KB in real address mode).

— Set the base DRAM memory starting address (as viewed by other boards over the MULTIBUS interface) at 0 (default configuration) or to any megabyte boundary up through 16 MB (fixed at 0 in real address mode).

— Set single or multiple MULTIBUS windows as small as 64 KB or as large as 1 MB within the first megabyte of address space. MULTIBUS windowing can be enabled both in real address mode and PVAM. The window size can also be set at 0 (no window) so that the CPU can only access its own DRAM memory.

The jumper and PAL changes may be used in combination with each other. For example, jumpers can be installed to set EPROM address space and to exclusively allocate (single-port) a portion of the dual-port memory to the CPU. Then, PALs can be installed to establish two MULTIBUS windows of different sizes and to set the DRAM base starting addresses.

High Speed Off-Board Memory

The iSBC 286/12/14/16 boards can access off-board memory either over the MULTIBUS (P1) interface, or over the P2 interface as shown in Figure 4. Memory transfers over the P2 interface are faster because the CPU board doesn't have to arbitrate for access to the MULTIBUS interface.

Using the P2 interface, the iSBC 286/12/14/16 boards can be configured to operate with either a standard iLBX interface or with a high-performance, synchronous interface.

The iSBC 286/12/14/16 boards as supplied are configured to operate with a synchronous, P2 inter-

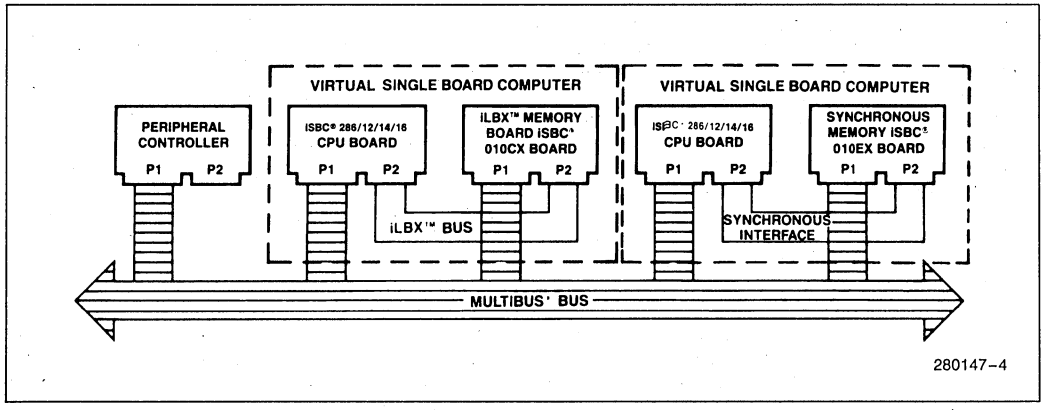


Figure 4. MULTIBUS®/iLBX™/Synchronous Interface Configurations

face. This high-performance interface is designed to connect to Intel's EX series of memory expansion boards to yield a CPU to memory read/write time of 0 wait-states. The EX memory expansion boards are available in sizes ranging from 512K bytes up to 4M bytes.

By moving several jumpers on the board, the iSBC 286/12/14/16 Single Board Computers may be reconfigured for an iLBX interface, and are compatible with Intel's CX series of memory expansion boards, which are available in sizes ranging from 512K bytes up to 2M bytes. Memory expansion boards from other manufacturers that meet the iLBX standard may also be used. CPU to memory access time is usually 1 or more wait-states depending on the speed of the memory used.

A total of four memory boards can be placed on the iLBX or synchronous interface bus. With 4M byte memory boards, this results in a total of 16M bytes on the memory expansion bus.

iSBX™ Bus MULTIMODULE™ On-Board Expansion

Two 8-, 16-bit iSBX MULTIMODULE connectors are provided on the iSBC 286/12/14/16 boards. Through these connectors, additional on-board I/O functions may be added. The iSBX MULTIMODULE Boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS Board form factor compatible boards. The iSBX interface connectors on the iSBC 286/12/14/16 boards provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. The iSBX MULTIMODULE Boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 286/12/14/16 microcomputer boards. A broad range of iSBX MULTIMODULE Board options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification is available from Intel.

SOFTWARE SUPPORT

Software support from Intel includes the iRMX 86, iRMX 286, and XENIX* Operating Systems, assembly and high level languages, development systems, in-circuit emulators, and various other hardware and software tools.

For those applications needing a real time, multitasking operating system, Intel offers the iRMX 86 Release 6 and iRMX 286 Release 1 Operating Systems. The iRMX operating systems are particularly well suited for industrial or commercial applications where the processor is simultaneously controlling multiple, real time, interrupt-intensive processes. Typical applications include machine and process control, data acquisition, signal processing, front-end processing, and digital PABX control. The iRMX operating systems employ a highly configurable, modular structure that allows easy system configuration and expansion.

The iRMX 86 Release 6 Operating System enables the iSBC 286/12/14/16 boards to address up to 1 MB of memory in real address mode. Using the iRMX 286 Operating System, this address range is extended to 16 MB in protected mode. The iRMX 286 Operating System also allows the user to take advantage of the hardware traps built into the iAPX 286 processor that provide expanded debug capabilities and increased code reliability.

Applications software written for earlier releases of the iRMX 86 Operating System is upwardly compatible through Release 6. Furthermore, application code written for the iRMX 86 Operating System can be compiled using 286 compilers to run under the iRMX 286 Operating System. Application code will require only minor changes.

Assembly and many high level languages are supported by the iRMX Operating Systems and Intellec® Series III and Series IV development systems. Language support for the iSBC 286/12/14/16 boards in real address mode includes Intel's ASM 86, PL/M 86, PASCAL 86, FORTRAN 86, and C86, as well as many third party 8086 languages. Language support for protected address mode include ASM 286, PL/M 286, PASCAL 286, and FORTRAN 286. Programs developed in these languages can be downloaded from an Intel Series III or IV Development System to the iSBC 286/12/14/16 boards via the iSDM™ 286 System Debug Monitor. The iSDM 286 monitor also provides on-target program debugging support including breakpoint and memory examination features.

Intel also offers the XENIX operating system which is designed for those applications needing an interactive, multiple user system. Typical applications include small business systems, software develop-

ment/engineering workstations, distributed data processing, communications, and graphics.

Intel's XENIX operating system is a fully licensed derivative of UNIX**, enhanced by Intel to provide device driver support for Intel board and component products plus other features that yield greater flexibility, increased reliability, and easier configurability. Intel's XENIX operating system has been optimized for use with the 80286 microprocessor and supports such features as on-chip memory management and protection which provide ease of portability and higher performance.

Applications software can be written in either Intel's FORTRAN, COBOL, or BASIC languages using a XENIX based, Intel 286/310 or 286/380 system, or by using an Intel iDIS™ Database Information System. The user can also select from a wide variety of existing third party languages and applications software.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, 32 or 40 bits

Data—8 or 16 bits

System Clock

CPU—8.0 MHz

Numeric Processor—5.3 MHz or 8.0 MHz (Jumper Selectable)

Cycle Time

Basic Instruction—8.0 MHz - 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles)

Dual-Port Memory

1, 2, or 4 megabyte, 0 wait-state, parity DRAM dual-ported to the on-board CPU bus and the MULTIBUS interface.

Local Memory

Number of sockets—two 28-pin JEDEC sites, expandable to 4 sites using iSBC 341 JEDEC Expansion Module

Maximum Size—128 KB expandable to 256 KB by installing an iSBC 341 EPROM Expansion Module. Memory size is set by jumpers on the iSBC 286/12/14/16 board.

Compatible Devices—EPROM, up to 64K x 8 (Intel 27512)

Off-Board Physical Memory

Operating System	Address Mode	Size
iRMX 86 Release 6 O.S.	Real	1 MB
iRMX 286 Release 1 O.S.	Protected	16 MB
XENIX Release 3 O.S.	Protected	16 MB

Socket provided for Intel 82258, 4 channel, advanced DMA controller. Data transfer rate = 4 MB per second (two cycle transfer mode, memory to memory); 2.67 MB per second (16-bit iSBX I/O to dual-port memory).

Interrupt Capacity

26 interrupt sources (total); 5 hard-wired to the 8259A PIC; 21 jumper selectable

Interrupt Levels—16 vectored requests using two 8259A devices and the 80286 microprocessor's NMI line

I/O Capability

Parallel — Line printer interface, on-board functions, and 3-bit board installed options code

Serial — Two programmable channels using one 8274 device

Timers — Three programmable timers using one 8254 device

Expansion— Two 8/16-bit iSBX MULTIMODULE connectors

Timers

Input Frequencies—1.23 MHz ±0.1% or 4.00 MHz ±0.1% (Jumper Selectable)

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	500 ns	53.3 ms	1.0 μs	58.2 min
Programmable One-Shot	500 ns	53.3 ms	1.0 μs	58.2 min
Rate Generator	18.8 Hz	2.0 MHz	0.000286 Hz	1 MHz
Square-Wave Rate Generator	18.8 Hz	2.0 MHz	0.000286 Hz	1 MHz
Software Triggered Strobe	500 ns	53.3 ms	1.0 μs	58.2 min
Hardware Triggered Strobe	500 ns	53.3 ms	1.0 μs	58.2 min
Event Counter	—	8.0 MHz	—	—

Interfaces

MULTIBUS Bus—All signals TTL compatible

iSBX Bus—All signals TTL compatible

iLBX Bus—All signals TTL compatible

Synchronous Interface—All signals TTL compatible

Serial I/O— Channel A: RS232C/RS422/RS449 compatible, DCE or DTE

Channel B: RS232C compatible, DCE

NOTE:
For RS422/RS449 operation, user supplied line drivers and resistor terminators must be installed.

Timer—All signals TTL compatible

Interrupt Requests—All TTL compatible

MULTIBUS® DRIVERS

Function	Type	Sink Current (mA)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	32
Bus Control	Open Collector	16/32

iLBX™ DRIVERS

Function	Type	Sink Current (mA)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	24
Bus Control	TTL	24

Serial Communications Characteristics

Synchronous—5-8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity

Asynchronous—5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity

BAUD RATES

Synchronous—600, 1.2 KB, 2.4 KB, 4.8 KB, 9.6 KB, 19.2 KB, 38.4 KB, 56 KB, 76.8 KB, 154 KB, 307 KB, 615 KB.

Asynchronous—75, 150, 300, 600, 1.2 KB, 2.4 KB, 4.8 KB, 9.6 KB, 19.2 KB.

NOTE:
Baud rates are software selectable.

Physical Characteristics

Width: 12.00 in. (30.48 cm)

Height: 7.05 in. (18.00 cm)

Depth: 0.88 in. (2.24 cm)
1.16 in. (2.95 cm) with iSBX MULTIMODULE board installed

Recommended Slot spacing (without iSBX MULTIMODULE): 1.2 in. (3.0 cm)

Weight: 26 oz. (731 gm)

Mating Connectors (or Equivalent Part)

Function	# of Pins	Centers (in)	Connector Type	Vendor	Vendor Part No.
iSBX Bus Connector 16-Bit (J5, J6)	44	0.1	Soldered	Viking	000293-0001
I/O Connectors (J1–J3)	26	0.1	Flat Crimp	3M	3399-6026
Front Panel Connector (J4)	14	0.5	Flat Crimp	3M	3385-6014
iLBX/Synch. Interface Edge Connector (P2)	60	0.1	Flat Crimp	KEL-AM T & B Ansley	RF30-2803-5 A3020

Electrical Characteristics

DC Power Requirements:

Maximum: +5V, 8.7A; ±12V, 35 mA (for serial I/O)

Typical: +5V, 5.7A; ±12V, 20 mA

NOTE:
Power requirements are for the default configuration. Does not include power for optional EPROM, 80287 or 82258 devices, or installed iSBX MULTIMODULE boards.

Environmental Characteristics

Operating Temperature: 0°C to 60°C with 8 CFM airflow across board (default configuration)

Relative Humidity: to 90% (without condensation)

Reference Manual

147533— iSBC 286/12/14/16 Hardware Reference Manual (order separately)

ORDERING INFORMATION

Part Number Description

SBC 286/12 Single Board Computer with 1 MB of Memory

SBC 286/14 Single Board Computer with 2 MB of Memory

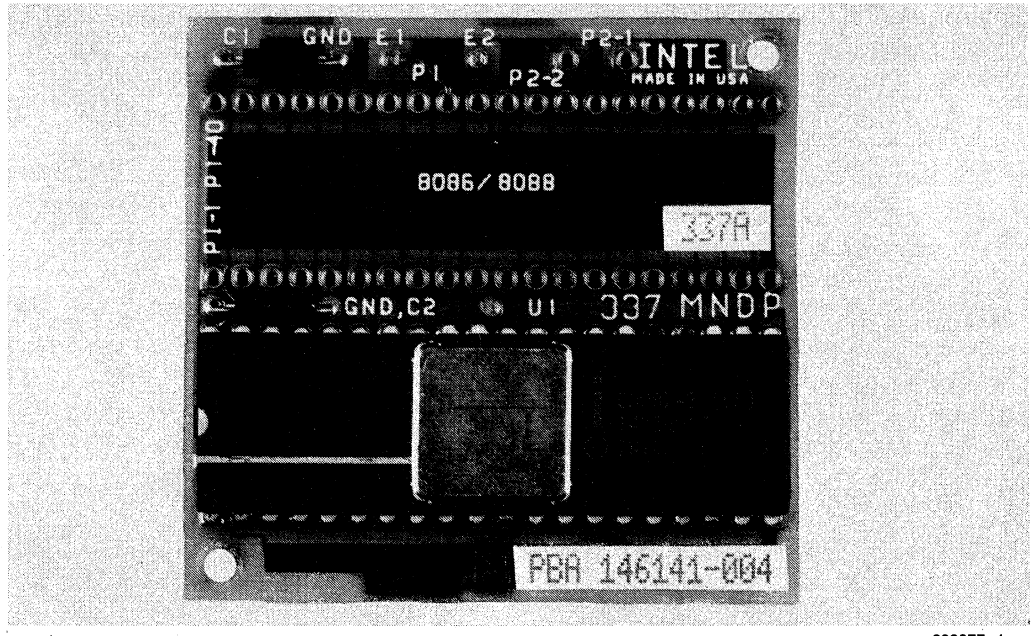
SBC 286/16 Single Board Computer with 4 MB of Memory

C80287-3 Numeric Processor Ext., 5 MHz
D80287-8 Numeric Processor Ext., 8 MHz
R82258-8 ADMA Coprocessor, 8 MHz

iSBC® 337A MULTIMODULE™ NUMERIC DATA PROCESSOR

- **High Speed Fixed and Floating Point Functions for 8 MHz or 5 MHz iSBC® 86, 88 and iAPX 86, 88 Systems**
- **Extends Host CPU Instruction Set with Arithmetic, Logarithmic, Transcendental and Trigonometric Instructions**
- **MULTIMODULE™ Option Containing 8087 Numeric Data Processor**
- **Up to 80X Performance Improvement in Whetstone Benchmarks over 8 MHz iAPX-86/10 Performance**
- **Supports Seven Data Types Including Single and Double Precision Integer and Floating Point**
- **Software Support through ASM 86/88 Assembly Language and High Level Languages**
- **Fully Supported in the Multi-Tasking Environment of the iRMX™ 86 Operating System**

The Intel iSBC® 337A MULTIMODULE™ Numeric Data Processor offers high performance numerics support for iSBC 86 and iSBC 88 Single Board Computer users, for applications including simulation, instrument automation, graphics, signal processing and business systems. The coprocessor interface between the 8087 and the host CPU provides a simple means of extending the instruction set with over 60 additional numeric instructions supporting seven additional data types. The MULTIMODULE implementation allows the iSBC 337A module to be used on all iAPX 86/88 board designs, all iSBC 86/88 single board computers and can be added as an option to custom iAPX board designs.



280077-1

October 1988
Order Number: 280077-001

OVERVIEW

The iSBC 337A MULTIMODULE Numeric Data Processor (also called NDP) provides arithmetic and logical instruction extensions to the 86/88 of the iAPX 86/88 families. The instruction set consists of arithmetic, transcendental, logical, trigonometric and exponential instructions which can all operate on seven different data types. The data types are 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18 digit packed BCD and 80-bit temporary.

Coprocessor Interface

The coprocessor interface between the host CPU and the iSBC 337A MULTIMODULE provides easy to use and high performance math processing. Installation of the iSBC 337A is simply a matter of removing the host CPU from its socket, installing the iSBC 337A MULTIMODULE into the host's CPU socket, and reinstalling the host CPU chip into the socket provided for it on the iSBC 337A MULTIMODULE (see Figure 1).

All synchronization and timing signals are provided via the coprocessor interface with the host CPU. The two processors also share a common address/data bus. (See Figure 2.) The NDP component is capable of recognizing and executing NDP numeric instructions as they are fetched by the host CPU. This interface allows concurrent processing by the host CPU and the NDP. It also allows NDP and host CPU instructions to be intermixed in any fashion to provide the maximum overlapped operation and the highest aggregate performance.

High Performance and Accuracy

The 80-bit wide internal registers and data paths contribute significantly to high performance and minimize the execution time difference between single and double precision floating point formats. This 80-bit architecture provides very high resolution and accuracy.

This precision is complemented by extensive exception detection and handling. Six different types of exceptions can be reported and handled by the NDP. The user also has control over internal precision, infinity control and rounding control.

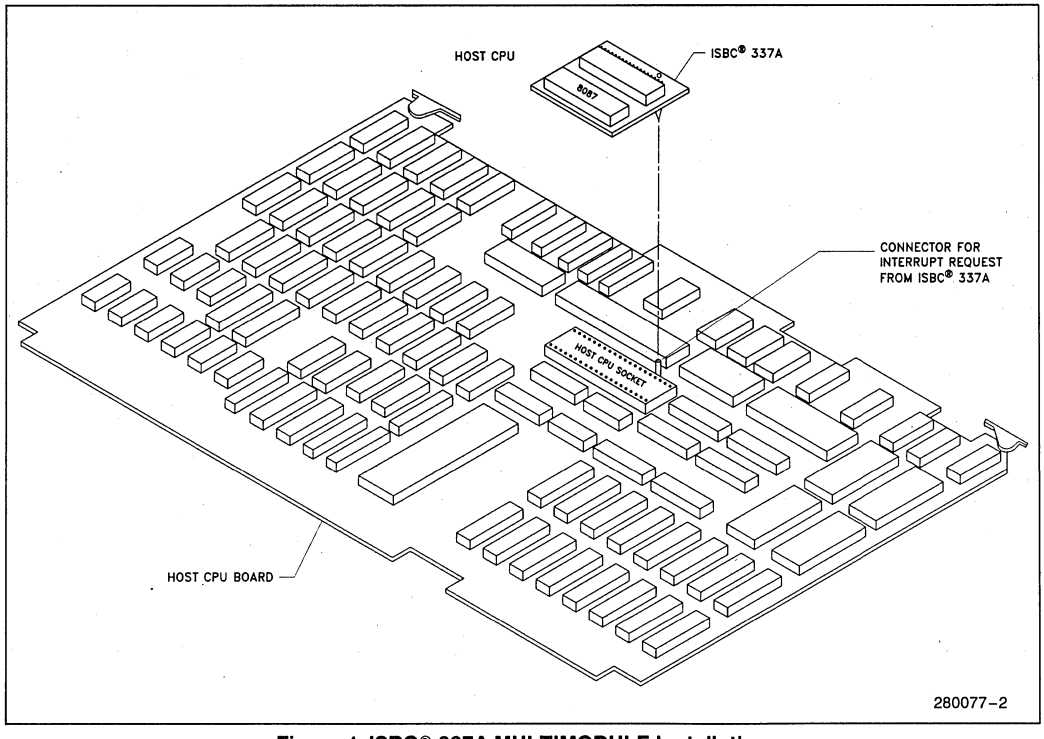


Figure 1. iSBC® 337A MULTIMODULE Installation

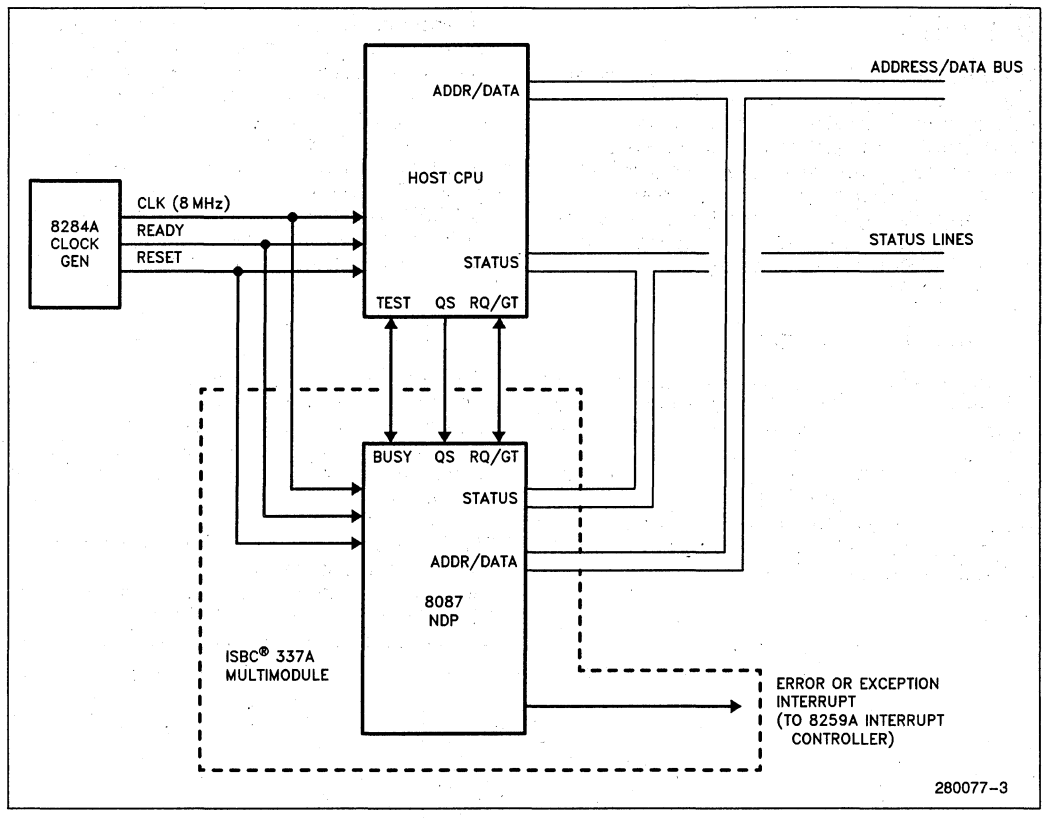


Figure 2. iSBC® 337A System Configuration

SYSTEM CONFIGURATION

As a coprocessor to the Host CPU, the NDP is wired in parallel with the CPU as shown in Figure 2. The CPU's status and queue status lines enable the NDP to monitor and decode instructions in synchronization with the CPU and without any CPU overhead. Once started, the NDP can process in parallel with and independent of the host CPU. For resynchronization, the NDP's BUSY signal informs the CPU that the NDP is executing an instruction and the CPU WAIT instruction tests this signal to insure that the NDP is ready to execute subsequent instructions.

The NDP can interrupt the CPU when it detects an error or exception. The interrupt request line is routed to the CPU through an 8259A Programmable Interrupt Controller. This interrupt request signal is brought down from the iSBC 337A MULTIMODULE to the single board computer through a single pin connector (see Figure 1). The signal is then routed to the interrupt matrix for jumper connection to the 8259A Interrupt Controller. Other iAPX designs may use a similar arrangement, or by masking off the CPU "READ" pin from the iSBC 337A socket, provisions are made to allow the now vacated pin of the host's CPU socket to be used to bring down the interrupt request signal for connection to the base board and then to the 8259A. Another alternative is to use a wire to establish this connection.

PROGRAMMABLE INTERFACE

Table 1 lists the seven data types the NDP supports and presents the format for each type. Internally, the NDP holds all numbers in the temporary real format. Load and store instructions automatically convert operands represented in memory as 16-, 32- or 64-bit integers, 32- or 64-bit floating point numbers or 18-digit packed BCD numbers into temporary real format and vice versa.

Computations in the NDP use the processor's register stack. These eight 80-bit registers provide the equivalent capacity of 40 16-bit registers. The NDP register set can be accessed as a stack, with instructions operating on the top stack element, or as a fixed register set with instructions operating on explicitly designated registers.

Table 2 lists the NDP instructions by class. Assembly language programs are written in ASM 86/88, the iAPX family assembly language.

Table 3 gives the execution times of some typical numeric instructions and their equivalent time on an 8 MHz 8086-2.

FUNCTIONAL DESCRIPTION

The NDP is internally divided into two processing elements, the control unit (CU) and the numeric execution unit (NEU), providing concurrent operation of the two units. The NEU executes all numeric instructions, while the CU receives and decodes instructions, reads and writes memory operands and executes processor control instructions.

Control Unit

The CU keeps the NDP operating in synchronization with its host CPU. NDP instructions are intermixed with CPU instructions in a single instruction stream. The CPU fetches all instructions from memory; by monitoring the status signals emitted by the CPU, the NDP control unit determines when a 8086-2 instruction is being fetched. The CU taps the bus in parallel with the CPU and obtains that portion of the data stream.

After decoding the instruction, the host executes all opcodes but ESCAPE (ESC), while the NDP executes only the ESCAPE class instructions. (The first five bits of all ESCAPE instructions are identical). The CPU does provide addressing for ESC instructions however.

Table 1. 8087 Datatypes

Data Formats	Range	Precision	Most Significant Byte
			7 0 7 0 7 0 7 0 7 0 7 0 7 0 7 0
Word Integer	10^4	16 Bits	I_{15} ... I_0 Two's Complement
Short Integer	10^9	32 Bits	I_{31} ... I_0 Two's Complement
Long Integer	10^{19}	64 Bits	I_{63} ... I_0 Two's Complement
Packed BCD	10^{18}	18 Digits	S — D_{17} D_{16} ... D_1 D_0
Short Real	$10^{\pm 38}$	24 Bits	S E_7 E_0 F_1 ... F_{23} F_0 Implicit
Long Real	$10^{\pm 308}$	53 Bits	S E_{10} E_0 F_1 ... F_{52} F_0 Implicit
Temporary Real	$10^{\pm 4932}$	64 Bits	S E_{14} E_0 F_0 ... F_{63}

Note:
Integer: I **Sign: S**
Fraction: F **BCD Digit (4 Bits): D**
Exponent: E

Packed BCD: $(-1)^S(D_{17} \ldots D_0)$

Real: $(-1)^S(2^{E\text{-}BIAS})(F_0F_1 \ldots)$

Bias = 127 for Short Real
1023 for Long Real
16i383 for Temp Real

Table 2. 8087 Instruction Set

Data Transfer Instructions

Real Transfers	
FLD	Load Real
FST	Store Real
FSTP	Store Real and Pop
FXCH	Exchange Registers
Integer Transfers	
FILD	Integer Load
FIST	Integer Store
FISTP	Integer Store and Pop
Packed Decimal Transfers	
FBLD	Packed Decimal (BCD) Load
FBSTP	Packed Decimal (BCD) Store and Pop

Comparison Instructions

FCOM	Compare Real
FCOMP	Compare Real and Pop
FCOMPP	Compare Real and Pop Twice
FICOM	Integer Compare
FICOMP	Integer Compare and Pop
FTST	Test
FXAM	Examine

Transcendental Instructions

FPTAN	Partial Tangent
FPATAN	Partial Arctangent
F2XM1	$2^X - 1$
FYL2X	$Y \bullet \log_2 X$
FYL2XP1	$Y \bullet \log_2 (X+1)$

Arithmetic Instructions

FADD	Add Real
FADDP	Add Real and Pop
FIADD	Integer Add
Subtraction	
FSUB	Subtract Real
FSUBP	Subtract Real and Pop
FISUB	Integer Subtract
FSUBR	Subtract Real Reversed
FSUBRP	Subtract Real Reversed and Pop
FISUBR	Integer Subtract Reversed
Multiplication	
FMUL	Multiply Real
FMULP	Multiply Real and Pop
FIMUL	Integer Multiply
Division	
FDIV	Divide Real
FDIVP	Divide Real and Pop
FIDIV	Integer Divide
FDIVR	Divide Real Reversed
FDIVRP	Divide Real Reversed and Pop
DIDIVR	Integer Divide Reversed
Other Operations	
FSQRT	Square Root
FSCALE	Scale
FPREM	Partial Reminder
FRNDINT	Round to Integer
FXTRACT	Extract Exponent and Significand
FABS	Absolute Value
FCHS	Change Sign

Processor Control Instructions

FINIT/FNINIT	Initialize Processor
FDISI/FNDISI	Disable Interrupts
FENI/FNENI	Enable Interrupts
FLDCW	Load Control Word
FSTCW/FNSTCW	Store Control Word
FSTSW/FNSTSW	Store Status Word
FCLEX/FNCLEX	Clear Exceptions
FSTENV/FNSTENV	Store Environment
FLDENV	Load Environment
FSAVE/FNSAVE	Save State
FRSTOR	Restore State
FINCSTP	Increment Stack Pointer
FDECSTP	Decrement Stack Pointer
FFREE	Free Register
FNOP	No Operation
FWAIT	CPU Wait

Table 3. Execution Time for Selected 8087 Actual and Emulated Instructions

Floating Point Instruction	Approximate Execution Time (Microseconds)		
	8087 (5 MHz Clock)	8086 Emulation	8087 (8 MHz Clock)
Add/Subtract Magnitude	14/18	1,600	9/11
Multiple (Single Precision)	19	1,600	12
Multiply (Extended Precision)	27	2,100	17
Divide	39	3,200	24
Compare	9	1,300	6
Load (Double Precision)	10	1,700	6
Store (Double Precision)	21	1,200	13
Square Root	36	19,600	23
Tangent	90	13,000	56
Exponentiation	100	17,100	63

An NDP instruction either will not reference memory, will require loading one or more operands from memory into the NDP, or will require storing one or more operands from the NDP into memory. In the first case, a non-memory reference escape is used to start NDP operation. In the last two cases, the CU makes use of a "dummy read" cycle initiated by the CPU, in which the CPU calculates the operand address and initiates a bus cycle, but does not capture the data. Instead, the CPU captures and saves the address which the CPU places on the bus. If the instruction is a load, the CU additionally captures the data word when it becomes available on the local data bus. If data required is longer than one word, the CU immediately obtains the bus from the CPU using the request/grant protocol and reads the rest of the information in consecutive bus cycles. In a store operation, the CU captures and saves the store address as in a load, and ignores the data word that follows in the "dummy read" cycle. When the NDP is ready to perform the store, the CU obtains the bus from the CPU and writes the operand starting at the specified address.

Numeric Execution Unit

The NEU executes all instructions that involve the register stack. These include arithmetic, logical, transcendental, constant and data transfer instructions. The data path in the NEU is 80 bits wide (64 fraction bits, 15 exponent bits and a sign bit) which allows internal operand transfers to be performed at very high speeds.

When the NEU begins executing an instruction, it activates the NDP BUSY signal. This signal is used in conjunction with the CPU WAIT instruction to resynchronize both processors when the NEU has completed its current instruction.

Register Set

The NDP register set is shown in Figure 3. Each of the eight data registers in the NDP's register stack is 80 bits wide and is divided into "fields" corresponding to the NDP's temporary real data type. The register set may be addressed as a push down stack, through a top of stack pointer or any register may be addressed explicitly relative to the top of stack.

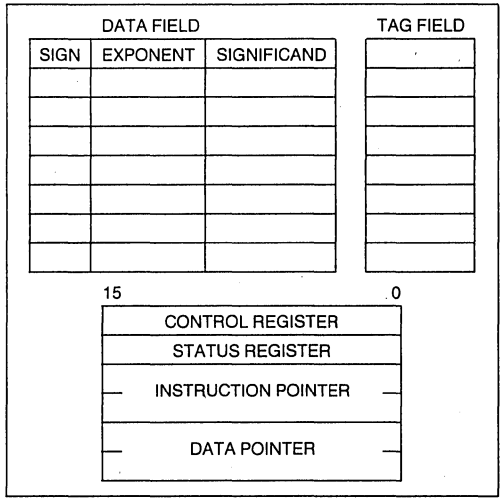


Figure 3. 8087 Register Set

Status Word

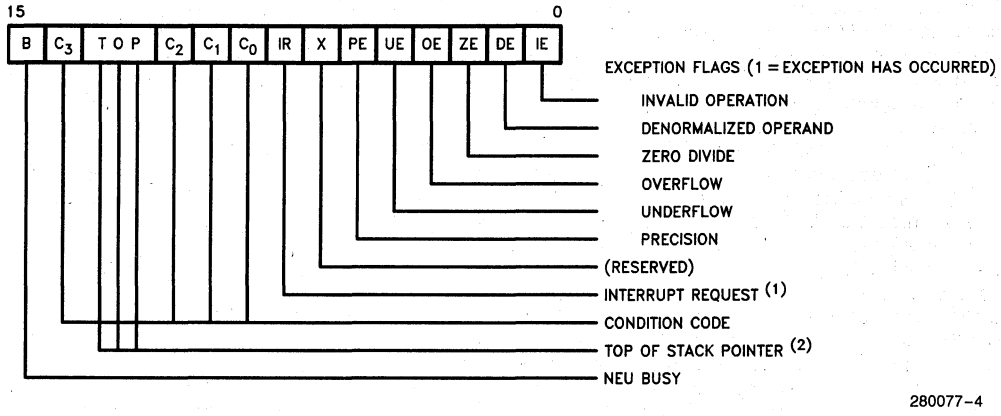
The status word shown in Figure 4 reflects the overall state of the NDP; it may be stored in memory and then inspected by CPU code. The status word is a 16-bit register divided into fields as shown in Figure 4. The busy bit (bit 15) indicates whether the NEU is executing an instruction (B = 1) or is idle (B = 0). Several instructions which store and manipulate the status word are executed exclusively by the CU, and these do not set the busy bit themselves.

The four numeric condition code bits (C_0–C_3) are similar to the flags in a CPU: various instructions update these bits to reflect the outcome of NDP operations.

Bits 13–11 of the status word point to the NDP register that is the current top-of-stack (TOP).

Bit 7 is the interrupt request bit. This bit is set if any unmasked exception bit is set and cleared otherwise.

Bits 5–0 are set to indicate that the NEU has detected an exception while executing an instruction.



NOTES:
1. IR is set if any unmasked exception bit is set, cleared otherwise.
2. Top Values:
   000 = Register 0 is Top of Stack.
   001 = Register 1 is Top of Stack.
   •
   •
   •
   111 = Register 7 is Top of Stack.

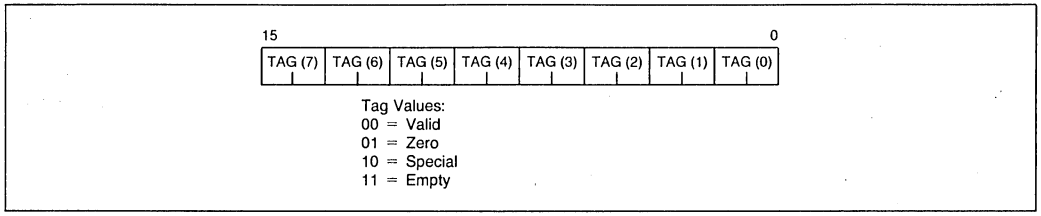


Figure 5. 8087 Tag Word

Tag Word

The tag word marks the content of each register as shown in Figure 5. The principal function of the tag word is to optimize the NDP's performance. The tag word can be used, however, to interpret the contents of NDP registers.

Instruction and Data Pointers

The instruction and data pointers (see Figure 6) are provided for user-written error handlers. Whenever the NDP executes an NEU instruction, the CU saves the instruction address, the operand address (if present) and the instruction opcode. The NDP can then store this data in memory.

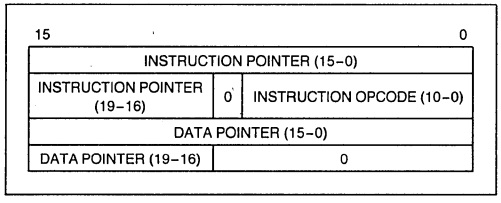


Figure 6. 8087 Instruction and Data Pointers

Control Word

The NDP provides several processing options which are selected by loading a word from memory into the control word. Figure 7 shows the format and encoding of the fields in the control word.

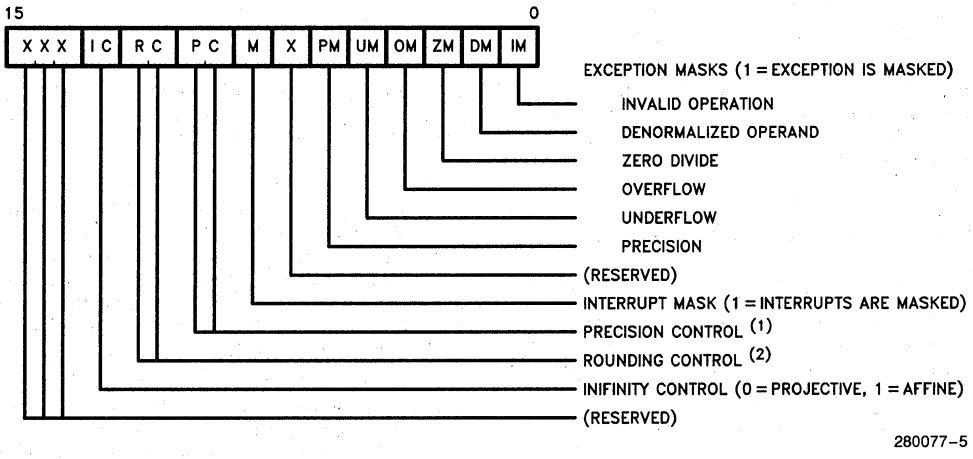
Exception Handling

The NDP detects six different exception conditions that can occur during instruction execution. Any or all exceptions will cause an interrupt if unmasked and interrupts are enabled.

If interrupts are disabled, the NDP will simply suspend execution until the host clears the exception. If a specific exception class is masked and that exception occurs however, the NDP will post the exception in the status register and perform an on-chip default exception handling procedure, thereby allowing processing to continue. The exceptions that the NDP detects are the following:

1. **INVALID OPERATION:** Stack overflow, stack underflow, indeterminate form (0/0, $-$, etc.) or the use of a Non-Number (NAN) as an operand. An exponent value is reserved and any bit pattern with this value in the exponent field is termed a Non-Number and causes this exception. If this exception is masked, the NDP default response is to generate a specific NAN called INDEFINITE, or to propagate already existing NANs as the calculation result.
2. **OVERFLOW:** The result is too large in magnitude to fit the specified format. The NDP will generate the code for infinity if this exception is masked.
3. **ZERO DIVISOR:** The divisor is zero while the dividend is a non-infinite, non-zero number. Again, the NDP will generate the code for infinity if this exception is masked.

4. **UNDERFLOW:** The result is non-zero but too small in magnitude to fit in the specified format. If this exception is masked the NDP will denormalize (shift right) the fraction until the exponent is in range. This process is called gradual underflow.
5. **DENORMALIZED OPERAND:** At least one of the operands or the result is denormalized; it has the smallest exponent but a non-zero significand. Normal processing continues if this exception is masked off.
6. **INEXACT RESULT:** If the true result is not exactly representable in the specified format, the result is rounded according to the rounding mode, and this flag is set. If this exception is masked, processing will simply continue.



NOTES:
1. Precision Control
   00 = 24 Bits
   01 = Reserved
   10 = 53 Bits
   11 = 64 Bits
2. Rounding Control
   00 = Round to Nearest or Even
   01 = Round Down (toward −)
   10 = Round Up (toward +)
   11 = Chop (Truncate Toward Zero)

Figure 7. 8087 Control Word

SOFTWARE SUPPORT

The iSBC 337A MULTIMODULE is supported by the following Intel software products: iRMX™ 86 Operating System, iRMX 88 Real-time Multi-tasking Executive, ASM 86/88 Assembly language, PL/M 86/88 Systems Implementation Languages, Pascal 86/88, Fortran 86/88 along with iRMX Development Utilities Package. In addition to the instructions provided in the languages to support the additional math functions, a software emulator is also available to allow the execution of iAPX instructions without the need for the iSBC 337A MULTIMODULE. This allows for the development of software in an environment without the iAPX processor and then transporting to its final run time environment with no changes in software code or mathematical results.

SPECIFICATIONS

Physical Characteristics

Width— 5.33 cm (2.100″)
Length— 5.08 cm (2.000″)
Height— 1.82 cm (0.718″)
iSBC 337A board + host board
Weight— 17.33 grams (0.576 oz.)

Electrical Characteristics

DC Power Requirements

V_{CC} = 5V ±5%
I_{CC} = 475 mA max.
I_{CC} = 350 mA typ.

Environmental Characteristics

Operating Temperature—0°C to 55°C with 200 linear feet/minute airflow

Relative Humidity—Up to 90% R.H. without condensation.

Reference Manual

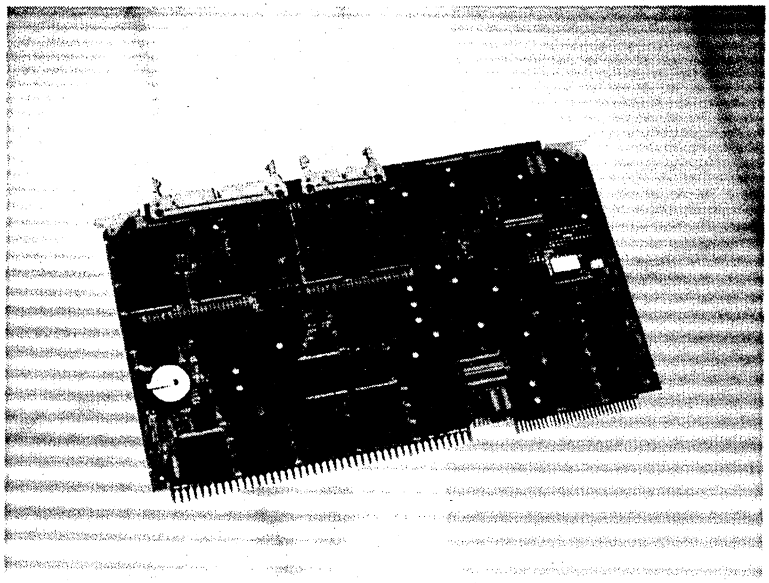
147163-001—iSBC 337A MULTIMODULE Numeric Data Processor Hardware Reference Manual (NOT SUPPLIED WITH MULTIMODULE BOARD).

Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California, 95051.

ORDERING INFORMATION

Part Number	Description
SBC 337A	MULTIMODLE Numeric Data Processor

iSBC® 86C/38 PRODUCT PROFILE



CMOS 80C86-BASED MULTIBUS® I SINGLE-BOARD COMPUTER

The iSBC® 86C/38 Single-Board Computer is a high-performance, low-power MULTIBUS® I CPU board based on advanced CMOS (complementary metal oxide semiconductor) technology. The board features Intel's 8 MHz 80C86 microprocessor—which provides the highest performance possible with static CMOS devices—a full megabyte of zero wait state DRAM memory, and power consumption of typically less than 8 watts when operating at full speed. The board's high performance, low power consumption, low heat generation and high reliability make it ideal for embedded real-time applications in harsh industrial environments.

STANDARD FEATURES

- Advanced CMOS 8 MHz 80C86 microprocessor
- 1 Mbyte of dual-port, zero wait state DRAM with parity
- Sockets for up to 512 Kbytes of standard 32-pin JEDEC EPROM devices
- Real-time clock/calendar with on-board battery backup
- Temperature-sensing device socket
- Optional 8087 numeric data processor with iSBC 337A MULTIMODULE™
- Upward-compatible with iSBC 86/35
- iRMX® Real-Time Operating System support

September, 1987
Order Number: 280630-001

FEATURES

CMOS TECHNOLOGY FOR LOW POWER, LOW HEAT

The Intel iSBC 86C/38 has been implemented entirely in CMOS, from the 80C86 CPU and EPLDs to the discrete logic and peripheral components. CMOS means low power consumption and low heat generation.

When running at full speed (8MHz), the iSBC 86C/38 typically requires less than 8 watts of power. However, a power-saving Slow Mode further reduces power consumption to about 4 watts when operating speed is reduced to 1 MHz.

Slow Mode operation is especially useful during temporary or emergency conditions when battery power is called into use. In a power-fail situation, for instance, Slow Mode operation allows the uninterrupted processing of an application on battery power.

The iSBC 86C/38 generates so little heat that it can operate without any air flow. This allows elimination of fans and other expensive cooling equipment and operation of the iSBC 86C/38 in a sealed enclosure, protected from harsh environments.

HIGH RELIABILITY

The iSBC 86C/38 features improved reliability on several levels. First, CMOS technology is inherently more reliable than NMOS technology: because devices run at lower junction temperatures, they last longer.

Parity error checking in the DRAM circuitry improves system integrity by detecting memory errors.

Finally, improved pin and socket I/O connectors with locking tabs assure secure connection of cables to the board.

MORE MEMORY

The amount of on-board memory has been doubled in the iSBC 86C/38 from earlier iSBC 86/35 board models. The iSBC 86C/38 comes with a full megabyte of zero wait state dynamic RAM, supporting the full 8086 address space. A full megabyte of on-board memory also eliminates the need to add DRAM modules, preserving the economy of a single-slot solution.

UPWARD-COMPATIBILITY WITH iSBC 86/35 DESIGNS

The iSBC 86C/38 provides complete hardware and software compatiblity with Intel iSBC 86/35 designs. All features supported on the iSBC 86/35 board run on the iSBC 86C/38 board with no changes. This includes full access to the MULTIBUS I 16 Mbyte memory address range and support for MULTIBUS I multimaster, 8087 math coprocessor, iSBC 86/35 I/O devices, iSBX connectors and interrupt capability.

PERFECT FOR REAL-TIME EMBEDDED APPLICATIONS

Real-time process control and industrial automation applications frequently require the CPU and control system to be physically located on the factory floor or in the field. These environments are typically harsh, full of dust, dirt, electrical noise and widely fluctuating temperatures.

Because the iSBC 86C/38 generates so little heat and can operate without cooling, it can be placed in a sealed enclosure, protected from harsh factory environments. It also offers excellent noise immunity and tolerance to extreme temperatures.

WORLDWIDE SERVICE AND SUPPORT

Assistance in developing real-time applications is available through Intel's worldwide network of field application engineers. We're real-time hardware and software experts and want to make your iSBC 86C/38 design a success.

SPECIFICATIONS

BASE SYSTEM

Central Processor

80C86 CPU	8 MHz
Numberic Processor iSBC 337A MULTIMODULE	8 MHz

Cycle Time

Basic Instruction	8 MHz, 500 ns (assumes instruction in queue)

Note: Basic instruction cycle is defined as the fastest instruction time (i.e. four clock cycles).

DRAM Memory

On-board parity memory	1 M byte, 0 Wait States at 8 MHz

Note: Power fail battery backup capability via P2 connector.

BASE SYSTEM (CONTINUED)

EPROM Memory

Number of sockets	Four 32-pin JEDEC Sites (compatible with 28-pin and 32-pin devices)
Device access speeds	265ns (minimum) to 640ns (maximum)
Maximum memory	512 Kb with 27010 (1 M bit) EPROMS

Note: EPROM, E²PROM (read only), and Static RAM devices are supported.

I/O CAPABILITY

Parallel Channel

Quantity	Three 8-bit parallel ports (50 pin socket connectors) using an 82C55A

Serial Channel

Quantity	One RS-232-C channel using an 82C51 device with speeds from 110 to 19.2 Kb
Expansion	Two 8/16-bit iSBX interface connectors for single or double wide iSBX MULTIMODULE boards

Real Time Clock/Calendar

An OKI MSM6242 provides real time clock/calendar capability with clock operation in either 12 or 24 hour format. The clock/calendar is sustained up to 10,000 hours by an on-board BR2325 lithium battery.

Temperature Sensing

Temperature sensing is an optional capability, allowing system designers to choose the appropriate level of temperature sensing for their application. A socket is on-board which supports four-pin temperature sensor devices.

Interrupt Capacity

Potential Interrupt Sources	37 jumper selectable
Interrupt Levels	9 using the 82C59A device and the 80C86 NMI line

Note: Bus Vectored Interrupt capability is supported.

Timers

Quantity	Three programmable timer/counters using one 82C54 device
Input Frequency	1.23 MHz ± 0.1%

Output Frequencies/Timing Intervals

Function	Single Counter	
	Min	Max
Real-time interrupt	1.63 μsec	53.3 ms
Rate Generator	18.8 Hz	615 kHz
Square-wave rate generator	18.8 Hz	615 kHz
Software triggererd strobe	1.63 μsec	53.3 ms

Interfaces

MULTIBUS Bus	All signals TTL compatible
iSBX Bus	All signals TTL compatible
Parallel I/O	All signals TTL compatible
Serial I/O	RS-232-C

POWER REQUIREMENTS/ CONSUMPTION

	8 MHz	1 MHz
Maximum:		
+ 5V	1.56 A, 7.8 Watts	.8 A, 4.0 Watts
+ 12V	.06 A, .72 Watts	.06 A, .72 Watts
− 12V	.08 A, .96 Watts	.08 A, .96 Watts
Typical:		
+ 5V	.82 A, 4.1 Watts	.7 A, 3.5 Watts
+ 12V	.04 A, .48 Watts	.04 A, .48 Watts
− 12V	.06 A, .72 Watts	.06 A, .72 Watts

Note: Does not include power for iSBC modules, iSBX modules or EPROM memory.

ENVIRONMENTAL REQUIREMENTS

Operating Temperature	0° to + 60°C at zero LFM air flow
Relative Humidity	0 to 95% noncondensing
Storage Temperature	− 40° to + 70°C

PHYSICAL CHARACTERISTICS

Dimensions

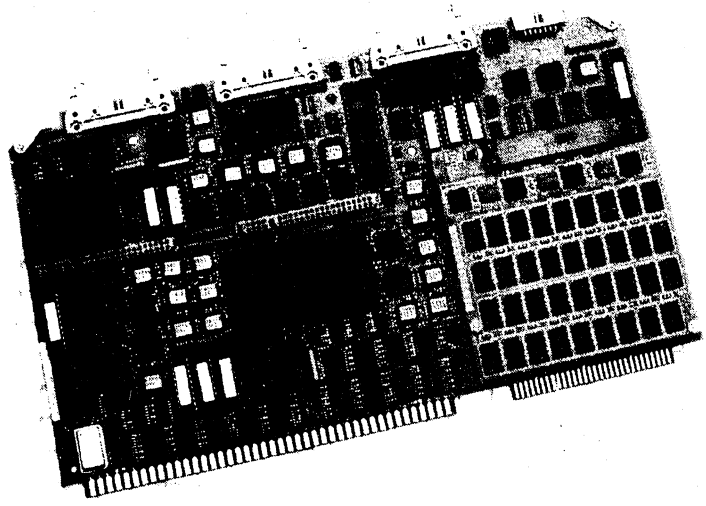
Width:	12.00 in. (30.48 cm)
Depth:	7.05 in. (17.91 cm)
Height:	.375 in. (.96 cm)

Recommended Minimum Cardcage Slot Spacing
.6 in (1.5 cm) without iSBC 337A or iSBX MULTIMODULE
1.2 in (3.0 cm) with iSBC 337A or iSBX MULTIMODULE

Approximate Weight 21.5 oz. (609.5 gm)

REFERENCE MANUAL

454554—iSBC 86C/38 Single Board Computer User's Guide



iSBC 386/12 SERIES SECOND-GENERATION, 386™ CHIP SINGLE BOARD COMPUTERS WITH IMPROVED I/O AND COMPUTING FOR MULTIBUS®I

The iSBC 386/12 series is Intel's second generation 386™ microprocessor-based MULTIBUS®I family of boards. The iSBC® 386/12 series provides increased I/O performance and functionality, and full compatibility with past 80286-based MULTIBUS I single board computers for easy design migration. Extensive use of surface mount technology combined with new memory and I/O controller designs enables both speed and functionality to be improved over previous generation boards. A variety of models is available, differing in speeds, amount of on-board DRAM memory, and installation of a math coprocessor.

FEATURES

- 16 or 20 MHz 80386 microprocessor and optional 80387 numeric coprocessor
- ADMA Advanced DMA Controller
- Dual-bus architecture with separate high-bandwidth execution bus
- 1–16MB of 32-bit, dual-port, on-board, parity DRAM
- Sockets for up to 1MB EPROM memory
- Two serial and one parallel I/O ports
- iLBX™ bus and two iSBX™ Bus Interface Connectors
- Multiprocessor support, including memory aliasing
- Upward-compatible from iSBC 286/12 single board computers

September, 1988
Order Number: 280671-001

FEATURES

386 MICROPROCESSOR PERFORMANCE

Using advanced design techniques from Intel's first generation, 386 chip-based CPU boards, the iSBC 386/12 series offers an immediate 2X performance increase over 8086 and 80286-based MULTIBUS CPU boards. Computing performance is optimized by an on-board, high speed, 32-bit execution bus connecting the 386 CPU, 80387 coprocessor, and 1 to 16MB of dual-ported DRAM memory. Performance starts with the iSBC 386/12 series 16 or 20 MHz 386 processor.

80387 NUMERIC COPROCESSOR

Numeric processing speed may be enhanced with a 32-bit 80387 floating point math coprocessor. The 80387 provides 80-bit precision, accelerating floating point calculations through hardware execution. Matched to the speed of the 386 CPU, the iSBC 386/12 series supports the 16 or 20 MHz versions of the 80387 coprocessor.

DUAL-BUS ARCHITECTURE

The iSBC 386/12 series uses multiple busses, a design technique that increases system performance. The board includes both a high-speed 32-bit execution bus matching the needs of the CPU, and a separate on-board bus for I/O, iLBX, and local EPROM transfers. The architecture also provides separate access to on-board DRAM over MULTIBUS I and a variety of parallel bus operations, increasing system performance. For example, other CPU boards can access the iSBC 386/12's dual-ported DRAM over MULTIBUS I while the iSBC 386/12 is handling I/O, EPROM, or iLBX operations. This increases total system responsiveness over all bus and I/O transactions.

HIGH-SPEED MEMORY CONTROLLER

On-board DRAM memory is provided on modules attached to the baseboard, providing from 1 to 16 MB of parity on-board DRAM. On-board access is optimized by a high-speed memory controller and the latest DRAM technology. DRAM memory is dual-ported and fully addressable from the 32-bit on-board bus or from MULTIBUS I. The iSBC 386/12 boards also include two 32-pin JEDEC sockets for up to 512 KB of local EPROM using 27020, 2 megabit EPROM devices.

Memory addressing flexibility surpasses the iSBC 286/12. For example, on-board DRAM memory may be addressed above the 16MB address space, allowing use of the first 16MB address space for EPROM, iLBX, and MULTIBUS I.

HIGH PERFORMANCE I/O AND BUS CONTROLLERS

The iSBC 386/12 series I/O and bus controllers have been designed using the latest high speed custom logic to speed up on-board I/O and to maximize throughput over the MULTIBUS I, dual-port, and iLBX bus interface. As a result, most applications can expect measurable increases in system and I/O performance over other MULTIBUS I single board computers.

In addition, on-board I/O recovery time is handled by the iSBC 386/12 series in hardware, eliminating the need to add or adjust software delay loops, and optimizing performance.

COMPLETE I/O FEATURE SET

Through extensive use of surface mount technology, the iSBC 386/12 series has substantially increased the on-board functionality over previous CPU boards. Each board provides two serial ports based on Intel's 8274 Multi-Protocol Serial Controller and one parallel port based on the 8255A Programmable Peripheral Interface. It also provides interrupt support based on two 8259A programmable interrupt controllers and the 386 chip's own Non Maskable Interrupt line and programmable timer/counter functions based on the 8254 Programmable Interval Timer.

Direct memory access transfers are provided by the 82258 advanced DMA (ADMA) controller. The ADMA controller has been further enhanced to increase flexibility and support synchronous transfers over both of the boards' serial ports and iSBX Bus Interface Connectors for use in high speed data communications.

I/O EXPANSION USING iSBX BUS

Two iSBX Bus Interface Connectors allow you to add a variety of capabilities, such as additional serial or parallel ports, SCSI, BITBUS, or network controllers, on-board graphics support, or your own custom-built SBX modules.

MULTIBUS I AND iLBX COMPLIANCE

The iSBC 386/12 boards support the full MULTIBUS I specification, including the MULTIBUS I system bus (with full Multimaster and bus-vectored interrupt support), the iLBX local bus extension, and the iSBX MULTIMODULE™ expansion bus with two iSBX connectors.

MULTI-PROCESSING SUPPORT

Multiprocessor support is enhanced through high performance dual-port arbitration control logic, and features like "aliasing" memory over MULTIBUS I, bus-vectored interrupts, and the real mode page register (compatible with the iSBC 86/35). In addition, the addressing approach used in iSBC 386/2X/3X boards is also supported.

iSBC 286/12 COMPATIBILITY

The iSBC 386/12 series is fully compatible with 80286-based CPU boards, so applications can be upgraded with a simple board swap. To increase performance, only changes to software timing loops are needed. Some of the features that provide this level of compatibility are independent jumber-configurable memory maps for real and protected modes, dual port memory granularity of 64K segments, support for bus vectored interrupts, support for memory aliasing, and support for the iLBX bus extension. To make upgrades even easier, the *iSBC 386/12 Series Software Upgrade Guide* provides all the information for an upgrade in one concise document.

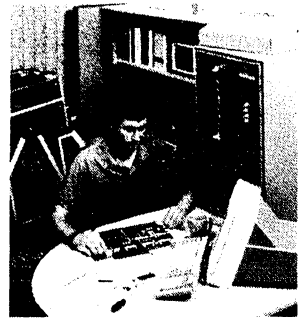
DEVELOPMENT SUPPORT

To help complete designs, Intel offers a choice of operating systems, languages, in-circuit emulators, and other debug tools. Real-time operating systems include the iRMX®-I Operating System in real mode and the iRMX-II Operating System in protected mode applications. For 32-bit embedded applications Intel offers the iRMK™ real-time kernel.

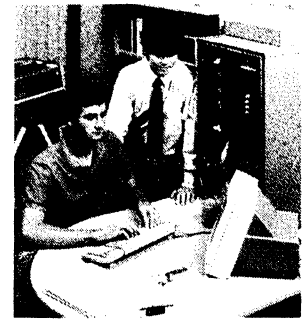
FEATURES

UPGRADING TO THE iSBC 386/12 IS AS EASY AS 1 . . . 2 . . . 3.

1. Remove your MULTIBUS I, iSBC 80286 based CPU board.



2. Jumper your new iSBC 386/12.



3. Run your application

WORLDWIDE SUPPORT AND SERVICE

Assistance in developing and supporting applications is available through Intel's worldwide network of field application engineers, system engineers, customer training centers and service centers. We're experts in developing a variety of real-time and system applications and can help make your iSBC 386/12 series design a success.

INTEL QUALITY—YOUR GUARANTEE

The iSBC 386/12 series is designed and manufactured in accordance with Intel's high quality standards. Quality is verified by rigorous testing in Intel's state-of-the-art Environmental Test Laboratory.

SPECIFICATIONS

WORD SIZE

Instruction—8, 16, 24, 32, or 40 bits
Data—8, 16, or 32 bits

SYSTEM CLOCK

386 CPU: 16 or 20 MHZ
80387 Numeric Coprocessor: matches CPU speed

DUAL-PORT DRAM MEMORY

On-board, parity memory
Available with 1, 2, 4, or 8 MB installed

Memory expansion available by plugging in one additional iSBC MMOxFP module.

Maximum Addressable Physical Memory:
16 Megabytes in protected virtual address mode, 1 Megabyte in real address mode. On-board DRAM memory may be addressed above the 16 MB address space to allow use of the first 16 MB address space for EPROM, iLBX, and MULTIBUS.

Memory Map Granularity:
CPU real mode addressing granularity—64KB
CPU protected mode addressing granularity—64KB/1MB
Dual-port addressing granularity—64KB

EPROM MEMORY

Two 32-pin JEDEC sockets (compatible with 28 and 32 pin devices). Maximum Size: 512K bytes using 27020 (2 MB) EPROMs when available. Memory Addressing granularity: 16K blocks using 2764 EPROMs.

INTERRUPT CAPACITY

Interrupt sources: 26 total, 5 hard-wired to the 8259A PIC, 21 jumper selectable
Interrupt levels: 16 vectored requests using two 8259A devices and the 80386 CPU's NMI line.
Supports both on-board and bus-vectored interrupts.

I/O CAPABILITY

Expansion: Two 8/16-bit iSBX MULTIMODULE connectors, supporting up to two single-wide, or one single and one double-wide iSBX MULTIMODULE boards.
Parallel: Line printer interface, on-board functions, and 3-bit board installed options code.
Serial: Two programmable channels using one 8274 device
Timers: Three programmable timers using one 8254 device
DMA: Intel 8 or 10 MHz, 82258, advanced DMA (ADMA) controller, depending on CPU speed. Supports DMA block transfers between on-board memory over the MULTIBUS I interface, iLBX interface, both iSBX interfaces, and both serial channels.

SERIAL COMMUNICATIONS CHARACTERISTICS

Synchronous: 5-8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity; baud rates from 600 baud to 615 KB.

Asynchronous: 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity; baud rates from 75 baud to 19.2 KB.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS

Width: 12.00 in. (30.48 cm)
Width: 7.05 in. (18.00 cm)
Depth: 0.86 in. (2.18 cm), 1.62 in. (4.11 cm) with added memory module

Recommended slot spacing: 1.2 in. (3.0 cm), 1.8 in. (4.6 cm) with added memory module.

INTERFACES

MULTIBUS I Bus: All signals TTL compatible
iSBX Bus: All signals TTL compatible
iLBX Bus: All signals TTL compatible
Serial I/O: Channel A: RS232C/RS422/RS449 compatible. DCE or DTE
Channel B: RS232C compatible, DCE

NOTE: For RS422/RS449 operation, line drivers and resistor terminators must be supplied.

Timer: All signals TTL compatible
Interrupt Requests: All TTL compatible

ELECTRICAL CHARACTERISTICS

DC Power Requirements:

Maximum: +5V, 14A ±12V, 35 ma
Typical: +5V, 9A ±12V, 20 ma

NOTE: Power requirements are for versions without an 80387 device. Does not include power for EPROM, iSBX MULTIMODULE boards, or iSBC MMOX-FP memory modules.

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to 60°C at 8 CFM airflow across board (default configuration)
Relative Humidity: 0% to 90% (without condensation)
Storage Temperature: −40°C to +70°C

REFERENCE MANUALS

455528-001 iSBC 386/12 Series Hardware Reference Manual (order separately). Provides complete information on hardware features, installation, jumpering, memory maps, addressing, and schematics.

462435-001 iSBC 386/12 Series Software Upgrade Guide (order separately). Provides complete information on upgrading existing applications (hardware and software), from an iSBC 286/10A/12/14/16, iSBC 86/30/35, or iSBC 386/2X/3X to an iSBC 386/12 board.

ORDERING INFORMATION

Part Number	Description
iSBC 386/12-16F01	16 MHz iSBC with 1 MB DRAM memory
iSBC 386/12-16F02	16 MHz iSBC with 2 MB DRAM memory
iSBC 386/12-16F04	16 MHz iSBC with 4 MB DRAM memory
iSBC 386/12-16F08	16 MHz iSBC with 8 MB DRAM memory

Part Number	Description
iSBC 386/12-20F01	20 MHz iSBC with 1 MB DRAM memory
iSBC 386/12-20F02	20 MHz iSBC with 2 MB DRAM memory
iSBC 386/12-20F04	20 MHz iSBC with 4 MB DRAM memory
iSBC 386/12-20F08	20 MHz iSBC with 8 MB DRAM memory

Models with an installed 80387 coprocessor may be ordered by adding an M suffix to the above order codes. For example, an iSBC 386/12-20F08M is the order code for a 20 MHz iSBC with 8 MB DRAM memory and installed 80387 math coprocessor.

To order additional memory, use the following codes:

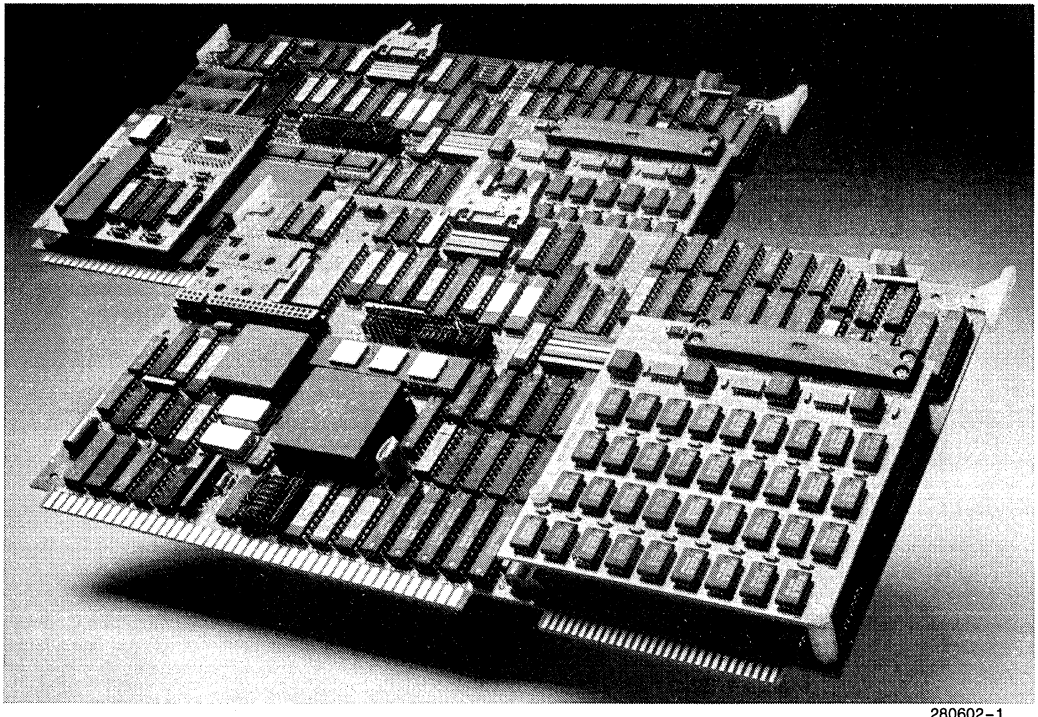
iSBC MM01-FP	1 MB, 85ns parity DRAM memory expansion module
iSBC MM02-FP	2 MB, 85ns parity DRAM memory expansion module
iSBC MM04-FP	4 MB, 85ns parity DRAM memory expansion module
iSBC MM08-FP	8 MB, 85ns parity DRAM memory expansion module

For more information or the number of your nearest Intel sales office, call 800-548-4725 (good in the U.S. and Canada).

iSBC® 386/21/22/24/28 AND 386/31/32/34/38 SINGLE BOARD COMPUTERS

- **Choice of 16 MHz or 20 MHz 386™ Microprocessor**
- **Available with 1, 2, 4, or 8 Megabytes of On-Board 32-Bit Memory, expandable to 16 Megabytes**
- **High Speed 80387 Floating Point Math Coprocessor**
- **Uses iRMX® or iRMK Kernel Operating Systems**
- **Complete Starter Kits to Speed Development**
- **Two 32-Bit JEDEC Sites for up to 512 Kilobytes of EPROM Memory**
- **RS232C Interface for Local/Remote Control and Diagnostics**
- **iSBX® Interface for Low Cost I/O Expansion**
- **16 Levels of Direct Vectored Interrupt Control**
- **64 Kilobyte 0 Wait-State Cache Memory**

The iSBC® 386/2x and 3x series boards (iSBC 386/21/22/24/28 and iSBC 386/31/32/34/38) are Intel's highest performance MULTIBUS® I CPU boards. These boards feature either a 16 MHz or 20 MHz 386 CPU, an 80387 math coprocessor, a 64k byte, 0 wait-state cache memory to support the CPU, and a 32-bit interface to 1, 2, 4, or 8 megabytes of dual-port parity DRAM memory. An additional 1, 2, 4, or 8 MB iSBC MM0x series memory module may be installed to provide up to 16 MB of on-board DRAM memory. The iSBC 386/2x and 3x boards also feature an 8/16-bit iSBX MULTIMODULE interface for low-cost I/O expansion, an asynchronous RS232C interface to support a local terminal or modem, two 16-bit programmable timer/counters, a 16-level direct-vectored interrupt controller, two 32-pin JEDEC sites for up to 512 kb of EPROM memory, and multimaster MULTIBUS arbitration logic. The iSBC 386/2x and 3x boards are ideal for applications needing 32-bit performance together with full MULTIBUS I compatibility.



280602-1

*XENIX is a registered trademark of Microsoft Corp.
*UNIX is a trademark of AT&T.

October 1988
Order Number: 280602-001

OVERVIEW—iSBC 386/2x AND 3x SERIES CPU BOARDS

The iSBC 386/21/22/24/28 and iSBC 386/31/32/34/38 boards (iSBC 386/2x and 3x series) are Intel's first 32-bit MULTIBUS I single board computers using the 386 microprocessor. The boards employ a dual-bus structure, a 32-bit CPU bus for data transfers between the CPU and memory, and a 16-bit bus for data transfers over the MULTIBUS interface, iSBX interface, EPROM local memory, and I/O interfaces. In this manner, the boards take advantage of the 386 CPU's 32-bit performance while maintaining full compatibility with the MULTIBUS I interface and iSBX MULTIMODULE boards.

The DRAM memory, which is on a module that is secured to the baseboard, may be expanded by installing a second 1, 2, 4, or 8M byte memory module. A block diagram of the board is shown in Figure 1.

The iSBC 386/2x and 3x series boards can be used in many applications originally designed for Intel's other 8- and 16-bit microcomputer based, single board computers.

16 MHz or 20 MHz Central Processor Unit

The heart of the iSBC 386/2x and 3x CPU board is the 386 microprocessor. The complete series includes two lines, with a choice of CPU speed. The iSBC 386/21/22/24/28 boards use the 16 MHz 386 microprocessor and the iSBC 386/31/32/34/38 boards use the 20 MHz 386 microprocessor. The 386 CPU utilizes address pipelining, a high speed execution unit, and on-chip memory management/protection to provide the highest level of system performance. The 386 microprocessor also features an Address Translation Unit that supports up to 64 terabytes of virtual memory.

The 386 CPU is upward compatible from Intel's 8088, 8086, 80186, and 80286 CPUs. Application software written for these other 8- and 16-bit microprocessor families can be recompiled to run on the 80386 microprocessor. Some changes to the software such as adjustment of software timing loops and changing I/O address references may be required. The 386 microprocessor resides on the 32-bit wide CPU bus which interconnects the CPU with the math coprocessor and dual-port memory.

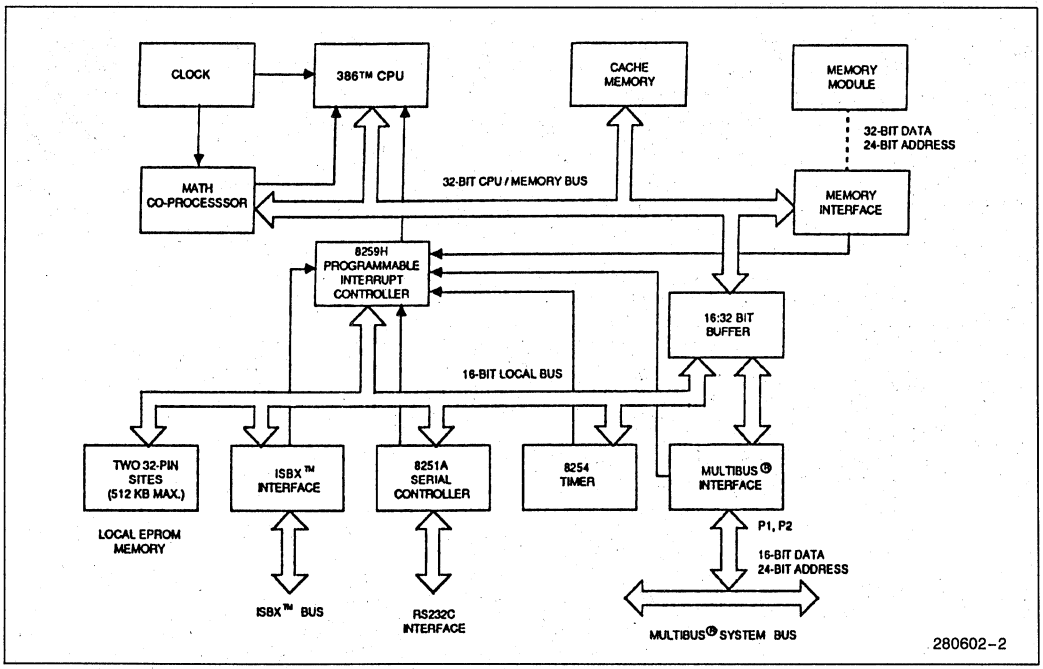


Figure 1. iSBC® 386/2x and 3x CPU Board Block Diagram

Instruction Set

The 386 CPU instruction set includes: variable length instruction format (including double operand instructions; 8-, 16-, and 32-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data; and iterative word and byte string manipulation functions. All existing instructions have been extended to support 32-bit addresses and operands. New bit manipulation and other instructions have been added for extra flexibility in designing complex software.

Numeric Data Processor

For enhanced numerics processing compatibility, the iSBC 386/2x and 3x boards include an 80387 numeric coprocessor. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The numeric data processor meets the IEEE P754 (Draft 7) standard for numeric data processing and maintains compatibility with 8087-based systems. Data transfers to and from the CPU are 32-bits wide.

Architectural Features

The 8086, 8088, 80188, 80286, and 386 microprocessor family contain the same basic sets of registers, instructions, and addressing modes. The 80386 processor is upward compatible with the 8086, 8088, 80186, 80188, and 80286 CPU's.

Architectural Features

The 386 CPU operates in two modes: protected virtual address mode; and 8086 real address mode. In protected virtual address mode (also called protected mode), programs use virtual addresses. In this mode, the 386 CPU automatically translates logical addresses to physical addresses. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. In 8086 real address mode, programs use real addresses with up to one megabyte of address space. Both modes provide the same base instruction set and registers.

Interrupt Control

Incoming interrupts are handled by two cascaded on-board 8259A programmable interrupt controllers and by the 386's NMI line. Twenty interrupt sources are routed to the programmable controllers and the interrupt jumper matrix. Using this jumper matrix, the user can connect the desired interrupt sources to specific interrupt levels. The interrupt controllers prioritize interrupts originating from up to 15 sources and send them to the CPU. The user can connect a sixteenth interrupt to the 386 NMI line. Table 1 includes a list of devices and functions suported by interrupts. Bus vectored interrupts are not supported.

Table 1. Interrupt Request Sources

Source	Function	Number of Interrupts
MULTIBUS® Interface	Requests from MULTIBUS® resident peripherals or other CPU baords	8
8251A Serial Controller	Indicates status of transmit and receive buffers and RI lead of the RS232C interface	3
8254 Timers	Timer 0, 1 outputs; function determined by timer mode (hardwired to interrupt controller)	2
iSBX™ Connector	Function determined by iSBX™ MULTIMODULE™ board	4
Bus Timeout	Indicates addressed MULTIBUS® or iSBX™ resident device has not responded to a command within 10 ms	1
Power Fail Interrupt	Indicates AC power is not within tolerance (signal generated by system power supply)	1
Parity Interrupt	Indicates on-board parity error	1
Programmable Register	Generate interrupt under program control	1

Memory Capabilities

The iSBC 386/2x and 3x boards support both EPROM local memory and dynamic RAM (DRAM), which is located on-board. The DRAM is supported by a high speed on-board cache memory.

DRAM Memory

The iSBC 386/2x and 3x series CPU boards come with 1, 2, 4, or 8M bytes of DRAM memory. This memory is on a low profile module that is installed on the baseboard. The module measures approximately 4″ x 4″ and uses surface mount DRAM devices. The DRAM memory supports byte-parity error detection and has a 32-bit wide data path to the 80386 CPU and 16-bit wide data path to the MULTIBUS interface.

The memory may be expanded by installing an additional iSBC MM0x series memory module, which is available in 1, 2, 4, or 8M byte sizes. All mounting hardware is included. Maximum DRAM memory is 16M bytes using an iSBC 386/28 or 386/38 CPU board and an 8M byte iSBC MM08 memory module. This combination requires only 1.8 inches of card-cage space.

Cache Memory

A 64K byte cache memory on the iSBC 386/2x and 3x boards supports the 386 CPU and provides 0 wait-state reads for data and program code resident in the cache memory. The cache memory is updated whenever data is written into the dual-port memory or when the CPU executes a read cycle and the data or program code is not present in cache memory. This process is controlled by the cache replacement algorithm. Cache "misses" require additional wait-states to retrieve data from the DRAM memory. If the processor is in pipelined mode, 2 wait-states (4 clock cycles) are required to retrieve data. If the processor is in non-pipelined mode, 3 wait-states are required. All writes to DRAM memory require 2 (pipelined) or 3 (non-pipelined) wait-states.

The cache memory supports 16K entries, with each entry comprised of a 32-bit data field and an 8-bit tag field. The tag field is used to determine which actual memory word currently resides in a cache entry. The cache memory size and effective replacement algorithm are designed to optimize both the probability of cache "hits" and local bus utilization.

EPROM Memory

The EPROM memory consists of two 32-pin JEDEC sites that are intended for boot-up and system diagnostic/monitor routines, application code, and ROM-able operating system software. Maximum local memory capacity is 512K bytes using Intel 27020 (256k x 8) 2 megabit EPROM devices. The EPROM memory resides at the upper end of the 386 device's memory space for both real address mode and PVAM operation.

Memory Map

In real address mode, the maximum amount of addressable physical memory is 1 Mbyte. In protected virtual address mode (PVAM), the maximum amount of addressable physical memory is 16 Mbytes. The system designer can easily change the CPU memory map to adapt the CPU board to the required overall system memory map. Reconfiguration is usually necessary for multiple processor-based systems with more than two CPU boards and/or intelligent I/O boards. By changing PAL devices and/or by moving jumpers, the designer can set:

- EPROM memory space
- Starting address of DRAM memory
- Amount of DRAM memory that is dual-ported to the CPU and MULTIBUS interface or single-ported to the CPU
- Access to off-board MULTIBUS address space

EPROM Memory

The EPROM memory space is set using four jumpers to accommodate 27256 (256 kb), 27512 (512 kb), 27010 (1 Mb), or 27020 (2 Mb) byte-wide devices. Smaller EPROM devices may be used, however the EPROM will appear more than once within the EPROM address space. Using a pair of 27020 EPROMs will provide 512k bytes of memory. The iSBC 386/2x and 3x series boards are designed to accommodate EPROM devices with access times ranging from 130 ns–320 ns. In real address mode, the ending address of EPROM memory is always 1M byte (FFFFFH). In PVAM, the ending address of EPROM memory is always 4G bytes (FFFF FFFFH), which is the top of the 386 CPU address space.

DRAM Memory Size/Location

The iSBC 386/2x and 3x boards allow the user to control the location and size of the DRAM memory (on the iSBC 386/2x and 3x boards) available for use by the CPU and other boards in the system. In PVAM, the starting address of DRAM can be set to start on any 1M byte boundary up through 15M bytes by setting jumpers and by installing a custom-programmed PAL device. In real address mode, the DRAM memory always starts at 0H (hex).

The ending address can be set on 64k byte boundaries using jumpers in both PVAM and real address mode. Setting the ending address at lower than the actual amount of installed memory effectively deselects a portion of DRAM and creates additional MULTIBUS address space.

MULTIBUS Address Space

Any address space not set aside as EPROM or DRAM memory automatically becomes address space the CPU can use to access other boards in the system. For example, Figure 2A shows a real address mode CPU memory map for a 1M byte iSBC 386/21 board. With the DRAM ending address set at 512k bytes and 128k bytes of installed EPROM, 384k bytes of MULTIBUS address space is accessable by the CPU. Figure 2B shows a typical PVAM configuration where the 4 Mbytes of DRAM has been set to start at 1M byte and end at 4.5M bytes. The address space from 0 to 1M byte and 4.5 to 16M bytes is the MULTIBUS address space accessable by the CPU.

Figure 2C illustrates another way the board can establish additional MULTIBUS address space. If the DRAM memory starts at 0, a jumper on the board can be used to create additional MULTIBUS address space between 512k bytes and 1M byte. This feature is available both in real address mode and PVAM.

Dual-Port/Local Memory

A portion or all of the DRAM memory can be selected to be dual-port (shared) memory. Both the starting and ending addresses are set on 256k byte boundaries using jumpers on the board. Any DRAM memory that is not configured as dual-port memory is local (single-port) memory available only to the CPU.

Programmable Timer

Three 16-bit, programmable interval timer/counters are provided using an 8254 device, with one timer dedicated to the serial port for use as a baud rate generator. The other two timers can be used to generate accurate time intervals under software control. The timers are not cascadable. Four timer/counter modes are available as listed in Table 2. Each counter is capable of operating in either BCD or binary modes. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.

Serial I/O

The iSBC 386/2x and 3x boards include one RS232C serial channel, which is configured as an

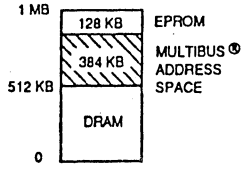


Figure 2A. Real Address Mode iSBC® 386/21 Board Memory Map

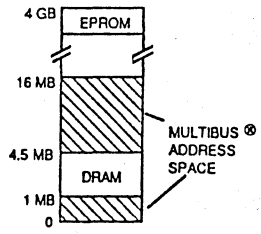
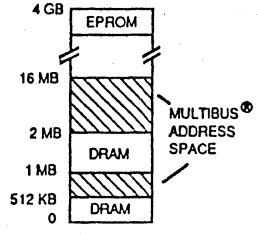


Figure 2B. PVAM iSBC® 386/24 Board Memory Map



280602-3

Figure 2C. PVAM iSBC® 386/22 Board Memory Map

asynchronous, DTE interface. Data rates up to 19.2k baud may be selected. The serial channel can connect either to a host system for software development or to a stand alone terminal for field diagnostic support. For stand alone use, unhosted monitor software needs to be programmed by the user into the local EPROM memory. The serial channel may also be connected to a modem to provide remote diagnostic support or to download program codes. The physical interface is a 10-pin ribbon-style connector located on the front edge of the board.

iSBX™ Interface

For iSBX MULTIMODULE support, the iSBC 386/2x and 3x CPU boards provide an 8/16-bit iSBX connector that may be configured for use with either 8- or 16-bit, single or double-wide iSBX MULTIMODULE boards. Using the iSBX interface, a wide variety of specialized I/O functions can be added easily and inexpensively to the iSBC 386/2x and 3x boards.

Reset Functions

The iSBC 386/2x and 3x boards are designed to accept an Auxilliary Reset signal via the boards' P2 interface. In this way, system designs that require front panel reset switches are supported. The iSBC 386/2x and 3x boards use the AUX reset signal to reset all on-board logic (excluding DRAM refresh circuitry) and other boards in the MULTIBUS system. The iSBC 386/2x and 3x boards will also respond to an INIT reset signal generated by another board in the system.

LED Status Indicators

Mounted on the front edge of the iSBC 386/2x and 3x boards are four LED indicators that indicate the operating status of the board and system. One LED is used to show that an on-board parity error or a MULTIBUS bus parity error has occurred. A second LED indicates that a MULTIBUS or iSBX bus access timeout has occurred. The third LED is triggered by the start of an 386 bus cycle and will turn off if the 386 CPU stops executing bus cycles. The fourth LED will light under software control if the program writes to a specific I/O location.

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the MULTIBUS system bus, the iLBX local bus extension and the iSBX MULTIMODULE expansion bus. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The iLBX bus, which is usually used for memory expansion, is not supported by the iSBC 386/2x and 3x boards since all DRAM memory is located on-board. The iSBX bus povides a low cost way to add I/O to the board.

System Bus—IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a broad array of board level products, VLSI interface components, detailed published specifications and application notes.

System Bus—Expansion Capabilities

The user can easily expand or add features to his system by adding various MULTIBUS boards to his system. Products available from Intel and others include: video controllers; D/A and A/D converter boards; peripheral controller cards for floppy disk, hard disk, and optical disk drives; communications/networking boards; voice synthesis and recognition boards; and EPROM/bubble memory expansion boards.

System Bus—Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers sharing system tasks through communication over the system bus), the iSBC 386/2x and 3x boards provide full system bus arbitration control logic. This control logic allows up to four bus masters to share the system bus using a serial (daisy chain) priority scheme. By using an external parallel priority decoder, this may be extended to 16 bus masters. In addition to multiprocessing, the multimaster capability also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

iSBX™ Bus MULTIMODULE™ On-Board Expansion

One 8-/16-bit iSBX MULTIMODULE interface is provided on the iSBC 386/2x and 3x microcomputer boards. Through this interface, additional on-board I/O functions may be added, such as parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., floppy disks), BITBUS Control, and other custom interfaces to meet specific needs. Compared to other alternatives such as MULTIBUS I boards, iSBX modules need less interface logic and power, and offer simpler packaging and lower cost. The iSBX interface connector on the iSBC 386/2x and 3x boards provides all the signals necessary to interface to the local on-board bus, and is compatible with both 8-bit and 16-bit MULTIMODULES. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed using Intel's "MULTIBUS I Architecture Reference Book" (order no. 210883) as a guide.

SOFTWARE SUPPORT

Operating Systems

The iSBC 386/2x and 3x boards are supported by a variety of operating systems, including the iRMX I Release 8, iRMX II Release 2, and XENIX Release 3.4.2 operating systems from Intel, and System V/386 operating systems from third party vendors.

The iRMX II Release 2 operating system is a real-time multi-tasking and multi-programming software system capable of executing all the configurable layers of the iRMX II operating system on the 386 microprocessor and the iSBC 386/2x and 3x single board computers. Up to 16 MB of physical system memory is supported. The iRMX II Operating System also allows the user to take advantage of the hardware traps built into the 386 processor that provide expanded debug capabilities and increased code reliability.

The iRMX II Release 2 operating system is designed to support time-critical applications requiring real time performance in the industrial automation, financial; medical, communications, and data acquisition and control (including simulation) marketplaces.

Application code written under the iRMX I operating system can also run on the iSBC 386/2x and 3x boards. The code may either be run directly on the iRMX I operating system, or may be recompiled using Intel's 286 compilers and then run under iRMX II release 2 software. Application code will require only minor changes and may then take advantage of the added memory addressability, code reliability, and debug capability of the iRMX 286 operating system.

Applications software written for Release 1 of the iRMX II Operating Systems is upward compatible with iRMX II Release 2 software.

The XENIX operating system is a very high performance, UNIX operating system. This industry standard multi-user, multitasking operating system, provides a broad range of programming languages, system software, and application software for the system and application designer.

For customers preferring the UNIX operating system, third party software vendors offer UNIX System V.3.

Languages and Tools

A wide variety of languages is available for the iRMX, XENIX and System V/386 operating systems. For the iRMX II Release 2 operating system, Intel offers ASM 286, PASCAL 286, PL/M 286, C 286, and FORTRAN 286. For the XENIX operating system Intel offers ASM 386, PL/M 386, C 386, and PASCAL 386. For the System V/386 Operating System several different software vendors provide selections of languages, including ASM, C, PASCAL, FORTRAN, COBOL, RPG, PL1, BASIC, and Artificial Intelligence programming languages LISP and Arity/Prolog. Software development tools include PSCOPE Monitor 386 (PMON 386 and DMON 386), Softscope 286 (for iRMX II Release 2), and an ICE 386 in-circuit-emulator.

Starter Kits

The iSBC 386/2x and 3x Starter Kits are a set of hardware, software and support products designed to allow the user to easily evaluate the iSBC 386/2x and 3x boards and 386 microprocessor, and to begin system design and software development for their iSBC 386/2x and 3x applications. The kits include an iSBC 386/2x or 3x board (with memory module), choice of iRMX II release 2 software or of the DMON 386/020 Debug Monitor, free admission to one Customer Training Workshop, valuable discounts on development tools, and complete documentation. Each kit includes all items at one low price. The kits come in two major types, either the iRMX Starter Kits or the DMON-based Starter Kits. Each of these types are described below.

iRMX® II Release 2-Based iSBC® 386/2x Starter Kits

The iRMX Starter Kits are designed to provide a complete development solution for new iRMX-based applications and enable an existing iRMX II Release 1 application to run on the iSBC 386/2x and 3x boards. The starter kits include the complete iRMX II Release 2 operating system with single user license and include a 16-bit debug monitor that supports 16-bit application software development either in an on-target development environment using an Intel 286/310 system or in a host-target development environment using a Series III/IV system. These two development environments are shown in Figure 3.

The starter kit contains diskettes, two 27256 EPROMs, 10 foot serial cables for connection to the host Series III/IV development system or separate console terminal, and installation/operating instructions.

The diskettes provide the iRMX II Release 2 Operating System, ported to run on the iSBC 386/2x and 3x boards, and 16-bit monitor software. Both 8" ISIS format and 5¼" iRMX format diskette media are provided. The EPROMs, which the user installs on the iSBC 386/2x and 3x boards, contain the boot-loader, device initialization code, and the debug monitor. The iRMX 286/310 system or Intellec® Series III/IV development system are user provided.

The monitor allows the designer to debug both real mode and protected mode applications that run on the iSBC 386/2x and 3x boards.

The monitor provides commands that perform the following functions:

- Bootstrap load the program of your choice
- Examine and modify the contents of the 386 CPU registers and board memory
- Display the contents of memory and descriptor tables
- Load and execute relocatable and absolute object files
- Move blocks of memory from one location to another
- Perform I/O to a specified port
- Disassemble and execute instructions
- Single-step execution of instructions
- Define and examine symbols in a program

Using the starter kit, designers can generate and debug 16-bit application software either on the host Intellec system or on the iSBC 386/2x and 3x based system.

The iRMX II Operating System together with the monitor support the use of iRMX II 16-bit lan-

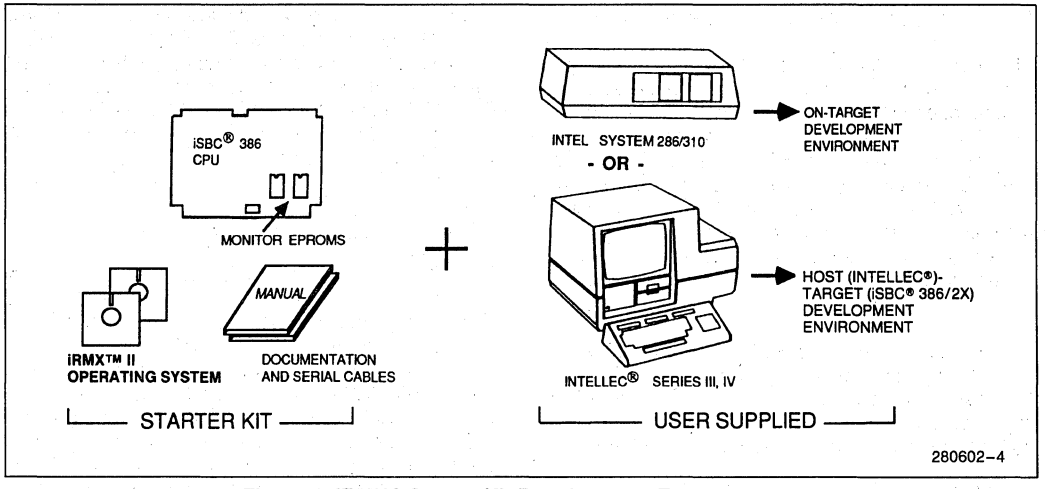


Figure 3. iRMX® Starter Kit Development Environments

guages and tools including ASM 86, ASM 286, PL/M 286, BIND 286, BUILD 286, and AEDIT text editor. Thirty-two-bit languages are not supported.

The starter kit also allows designers to download all or part of an existing iRMX II-based application to the iSBC 386/2x and 3x boards for execution. In some cases, software timing loops may need to be readjusted to compensate for the increased clock rate of the 386 microprocessor. Furthermore, I/O address references may also need changing to match the I/O map of the iSBC 386/2x and 3x boards.

iRMX I-based 8086 applications will also run on the iSBC 386/2x and 3x boards under the iRMX I operating system or under the iRMX II operating system included in the starter kit. To run them under the iRMX II operating system, the code is first recompiled using 286 compilers. The code is then downloaded to the iSBC 386/2x and 3x boards using the monitor software. As with other code, the iRMX I application code may have to be modified to adjust software timing loops and I/O address references.

Configuring the On-Target Development Environment

If the designer chooses to configure an on-target development environment using an Intel 286/310 system, either a standard SYS 310-40(A), -41(A), or -17(A) system may be used.

In addition to the iSBC 386/2x and 3x boards and memory, other boards that the iRMX II software supports may be installed in the system. These boards include the iSBC 214/215G/217/218A series of disk controller boards, the iSBC 188/48 and iSBC 544A 8- and 4-channel communications boards, the iSBC 350 line printer board, the iSBX 351 2-channel communications MULTIMODULE™ and a RAM (disk) driver, and many more.

On-Target Debug with the DMON 386020-Based iSBC 386/2x and 3x Starter Kits

The DMON 386-Based starter kits use the unhosted DMON 386020 Debug Monitor, which is intended for debugging embedded, 32-bit code. Once the user has either downloaded their code (using their own bootstrap loader) to the iSBC 386/2x and 3x board's DRAM memory, or programmed their code in EPROMs and plugged them in the iSBC 386/2x's and 3x's sockets, DMON may be used to fully debug the code, including any code using the 386's 32-bit OMF (object module format).

The DMON 386020 portion of the DMON-based starter kits provides DMON in two 27512 EPROMs, ready for use immediately in an iSBC 386/2x and 3x board, and in a 5¼" diskette, for integration with other, user-supplied code. Complete documentation is also included.

The DMON 386020 monitor provides the following debug capabilities:

- Examine/modify memory, I/O ports, processor registers, descriptor tables, and the task state segment
- Evaluate expression
- Control execution both in real and protected mode
- Set software breakpoints on execution addresses
- Set hardware breakpoints on execution and data addresses
- Disassemble instructions

The DMON 386020 based starter kit does not provide operating system (O.S.) support. If the application software uses an O.S. interface, the O.S. must be ported to run with the 386 microprocessor, the 8251A Serial Controller, and the 80387 math coprocessor (if used).

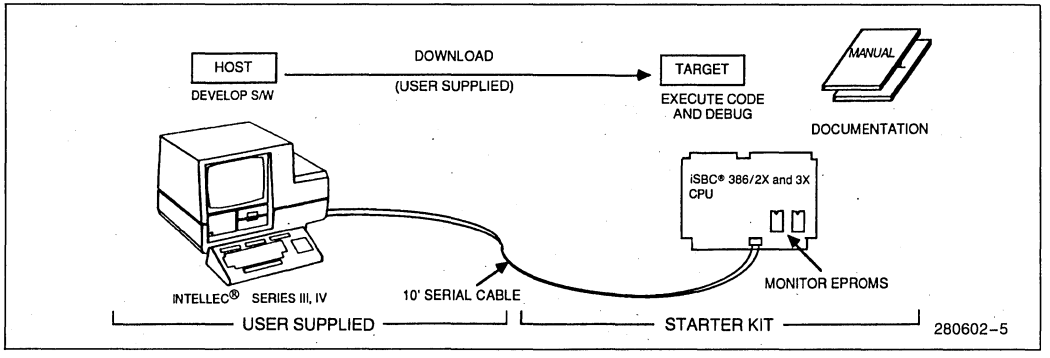


Figure 4. D-MON386ES Target Development Environment

System Compatibility

The iSBC 386/2x and 3x Single Board Computers are complemented by a wide range of MULTIBUS hardware and software products from over 200 manufacturers worldwide. This product support enables the designer to easily and quickly incorporate the iSBC 386/2x boards into his system design to satisfy a wide range of high performance applications.

Applications that use other 8- and 16-bit MULTIBUS single board computers (such as Intel's iSBC 286/10A and iSBC 286/12 8 MHz, 80286 based single board computers) can be upgraded to use the iSBC 386/2x and 3x boards. Changes to hardware and systems software (for speed and I/O configuration dependent code) may be required.

BOARD SPECIFICATIONS

Word Size

Instruction—8, 16, 24, 32 or 40 bits
Data—8, 16, 32 bits

System Clock

386 CPU—16 MHz or 20 MHz
Numeric Processor—80387 module—16 MHz or 20 MHz

Cycle Time

Basic Instruction: iSBC 386/21/22/24/28, 16 MHz—125 ns
iSBC 386/31/32/34/38, 20 MHz—100 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles)

DRAM Memory

On-board parity memory
- iSBC 386/21/31 board—1M byte
- iSBC 386/22/32 board—2M bytes
- iSBC 386/24/34 board—4M bytes
- iSBC 386/28/38 board—8M bytes

Memory expansion—One additonal plug-in module:
- iSBC MM01—1M byte
- iSBC MM02—2M bytes
- iSBC MM04—4M bytes
- iSBC MM08—8M bytes

Maximum Addressable Physical Memory—16 Megabytes (protected virtual address mode) 1 Megabyte (real address mode)

EPROM Memory

Number of sockets—Two 32-pin JEDEC Sites (compatible with 28-pin and 32-pin devices)

Sizes accommodated—64 kb (8k x 8), 128 kb (16k x 8), 256 kb (32k x 8), 512 kb (64k x 8), 1 Mb (128k x 8), 2 Mb (256k x 8)

Device access speeds—130 ns to 320 ns
Maximum memory—512k bytes with 27020 (2M bit) EPROMs

I/O Capability

Serial Channel

Type—One RS232C DTE asynchronous channel using an 8251A device

Data Characteristics—5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; automatic break detect and handling; even/odd parity error generation and detection

Speed—110, 150, 300, 600, 1.2 kb, 2.4 kb, 4.8 kb, 9.6 kb, 19.2 kb

Leads supported—TD, RD, RTS, CTS DSR, RI, CD, SG

Connector Type—10 pin ribbon

Expansion—One 8/16-bit iSBX interface connector for single or double wide iSBX MULTIMODULE board.

Interrupt Capacity

Potential Interrupt Sources—21 (2 fixed, 19 jumper selectable)

Interrupt Levels—16 using two 8259A devices and the 80386 NMI line

Timers

Quality—Two programmable timers using one 8274 device

Input Frequency—1.23 MHz ± 0.1%

Output Frequencies/Timing Intervals

Function	Single Counter	
	Min	Max
Real-time interrupt	1.63 μs	53.3 ms
Rate Generator	18.8 Hz	615 kHz
Square-wave rate generator	18.8 Hz	615 kHz
Software triggered strobe	1.63 μs	53.3 ms

Interfaces

MULTIBUS Bus—All signals TTL compatible
iSBX Bus—All signals TTL compatible
Serial I/O—RS 232C, DTE

MULTIBUS® DRIVERS

Function	Type	Sink Current (mA)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	32
Bus Control	Open Collector	16/32

Power Requirements

iSBC 386/2x and 3x boards
Maximum: +5V, 12.5A
±12V, 35 mA
Typical: +5V, 9A
±12V, 20 mA

NOTE:
Does not include power for iSBX module, EPROM memory, or added iSBCMM0x memory modules.

Add the following power when adding iSBC MM0X memory modules:

iSBC MM01 +5V, 0.71A
MM02 +5V, 0.96A
MM04 +5V, 0.71A
MM08 +5V, 0.96A

Environmental Requirements

Operating Temperature—0°C to 60°C at 300 LFM
Relative Humidity—0% to 85% noncondensing
Storage Temperature—−40°C to +70°C

Physical Characteristics

Dimensions
Width—12.00 in. (30.48 cm)
Height—7.05 in. (17.91 cm)
Depth—0.86 in. (2.18 cm), 1.62 in. (4.11 cm) with added memory module

Recommended Minimum Cardcage Slot Spacing
1.2 in. (3.0 cm), with or without iSBX MULTIMODULE
1.8 in. (4.6 cm), with addded iSBC MM0x memory module

Approximate Weight
26 oz. (738 gm)
29 oz. (823 gm), with added iSBC MM0x memory module

Reference Manual

149094—iSBC 386/21/22/24/28 Hardware Reference Manual (order separately)

453652—iSBC 386/31/32/34/38 Single Board Computer Hardware Reference Manual

Ordering Information

Part Number	Description
CPU Boards	
SBC38621	16 MHz 386 MULTIBUS I CPU Board with 1 MB DRAM Memory
SBC38622	16 MHz 386 MULTIBUS I CPU Board with 2 MB DRAM Memory
SBC38624	16 MHz 386 MULTIBUS I CPU Board with 4 MB DRAM Memory
SBC38628	16 MHz 386 MULTIBUS I CPU Board with 8 MB DRAM Memory
SBC38631	20 MHz 386 MULTIBUS I CPU Board with 1 MB DRAM Memory
SBC38632	20 MHz 386 MULTIBUS I CPU Board with 2 MB DRAM Memory
SBC38634	20 MHz 386 MULTIBUS I CPU Board with 4 MB DRAM Memory
SBC38638	20 MHz 386 MULTIBUS I CPU Board with 8 MB DRAM Memory
Memory Modules	
SBCMM01	1 MB Parity DRAM Memory Expansion Module
SBCMM02	2 MB Parity DRAM Memory Expansion Module
SBCMM04	4 MB Parity DRAM Memory Expansion Module
SBCMM08	8 MB Parity DRAM Memory Expansion Module

Starter Kits

SBC38621SPKG	SBC38621 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38621SPKGR2	SBC38621 plus iRMX II R.2. O.S., Monitor, Training, Documentation, and Discount on tools.
SBC38622SPKG	SBC38622 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38622SPKGR2	SBC38622 plus iRMX II R.2. O.S., Monitor, Training, Documentation, and Discount on tools.
SBC38624SPKG	SBC38624 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38624SPKGR2	SBC38624 plus iRMX II R.2. O.S., Monitor, Training, Documentation, and Discount on tools.
SBC38628SPKG	SBC38628 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
DMON386020	Debug Monitor provided in two media, both in EPROMs for immediate use in the iSBC 386/2x board, and in a 5¼" diskette. Also includes documentation.
SBC38628SPKR2	SBC38628 plus iRMX II R.2. O.S. Monitor, Training, Documentation and Discount on tools.

Starter Kits

SBC38631SPKG	SBC38631 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38631SPKGR2	SBC38631 plus iRMX II R.2. O.S., Monitor, Training, Documentation, and Discount on tools.
SBC38632SPKG	SBC38632 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38632SPKGR2	SBC38632 plus iRMX II R.2. O.S., Monitor, Training, Documentation, and Discount on tools.
SBC38634SPKG	SBC38634 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38634SPKGR2	SBC38634 plus iRMX II R.2. O.S., Monitor, Training, Documentation, and Discount on tools.
SBC38638SPKG	SBC38638 plus DMON386020 Debug Monitor, Training, Documentation, and Discount on tools.
SBC38638SPKR2	SBC38638 plus iRMX II R.2. O.S. Monitor, Training, Documentation and Discount on tools.

Mating Connectors

Function	No. of Pins	Centers (in)	Connector Type	Vendor	Vendor Part Number
iSBX Bus Connector	44	0.1	Soldered	Viking	000293-0001
Serial RS232C Connector	10	0.1	Flat Crimp	3M	3399-6010
P2 Interface Edge Connector	60	0.1	Flat Crimp	Kel-AM T&B Ansley	RF30-2803-5 A3020

MULTIBUS® I
Memory Expansion Boards

4

iSBC® MM01, MM02, MM04, MM08 HIGH PERFORMANCE MEMORY MODULES

- **Provides High Speed Parity Memory Expansion for Intel's iSBC 386/2X, iSBC 386/3X and iSBC 386/1XX CPU Boards**
- **Available in 1M, 2M, 4M, and 8M Byte Sizes**
- **32 Bits Wide with Byte Parity**
- **Stackable to Provide up to 16M Bytes of High Speed Memory for MULTIBUS I and MULTIBUS II CPU Boards**
- **Supports 32-Bit, 16-Bit and 8-Bit Data Paths**
- **Supports Independent Read/Writes**
- **Easily Installed**

The iSBC MM01, iSBC MM02, iSBC MM04, and iSBC MM08 DRAM memory modules are members of Intel's complete line of iSBC memory and I/O expansion boards. The MM-Series of memory modules use a dedicated interface to maximize CPU/memory performance. The iSBC MM series of memory modules have been designed to provide both the on-board and expansion memory for the iSBC 386/2X, the iSBC 386/3X and the iSBC 386/1XX CPU Boards.

The modules contain (respectively) 1M byte, 2M, 4M, and 8M bytes of read/write memory using surface mounted DRAM components (see Figure 1).

Due to the high speed interface of the memory modules, they are ideally suited in applications where memory performance is critical.

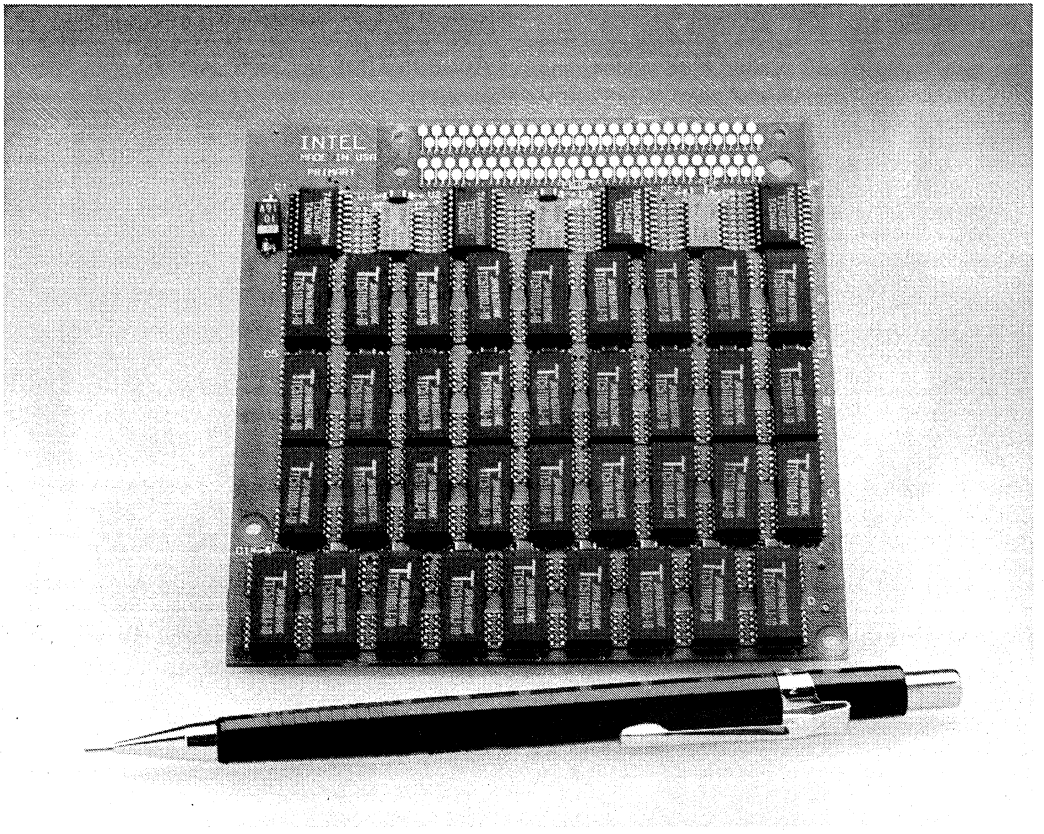


Figure 1. iSBC® MM08 Memory Module

280346-1

September 1988
Order Number: 280346-002

FUNCTIONAL DESCRIPTION

The iSBC MMxx memory modules provide high performance, 32-bit parity DRAM memory for the MULTIBUS I and MULTIBUS II CPU boards. These CPU boards come standard with one MMxx module installed, with memory expansion available through the addition of a second stackable iSBC MMxx module.

Memory Access Capabilities

The dynamic RAM memory of the memory modules is accessed through the dedicated memory module interface.

The MM memory module is designed for direct transfer of data between the CPU and the memory module without accessing the MULTIBUS interface.

MM01/MM02/MM04/MM08 Memory Size

The iSBC MM01, iSBC MM02, iSBC MM04, and iSBC MM08 modules can be stacked on the CPU baseboard in any combination.

Data Bus Structure

The MMxx-series memory modules use a 32-bit wide data path with storage for byte parity that can accommodate 8-bit byte, 16-bit or 32-bit word data transfers. In addition, the data path is capable of independent byte operations. This means that one byte can be written while the other three bytes (or any other combination) can be read.

Parity

One parity bit is provided for each of the four, 8-bit bytes in the 32-bit wide data path. For special applications, the parity bits can serve as data bits making possible 9-, 18-, or 36-bit data transfers.

Memory Function

The module protocol supports standard dynamic RAM READ, WRITE, RAS* only REFRESH cycles, and CAS* before RAS* REFRESH.

Installation

The iSBC MMxx memory modules are easily installed by the user. Each module includes all necessary connectors, screws, and other hardware for installation, either as a second stacked module or as a replacement for a module with less memory.

SPECIFICATIONS

Word Size Supported

8-, 16-, or 32-bits

Memory Size

iSBC MM01	1,048,576 bytes
iSBC MM02	2,097,152 bytes
iSBC MM04	4,194,304 bytes
iSBC MM08	8,388,608 bytes

Access Time (All Densities)

Read/Write — 107 ns (max)

The MMxx-series memory modules run with the iSBC 386/2X and iSBC 386/116 Boards at 16 MHz, and with the iSBC 386/3X and iSBC 386/120 Boards at 20 MHz. Wait state performance information with each of these CPU baseboards is contained in the Hardware Reference Manual for the specific CPU baseboard.

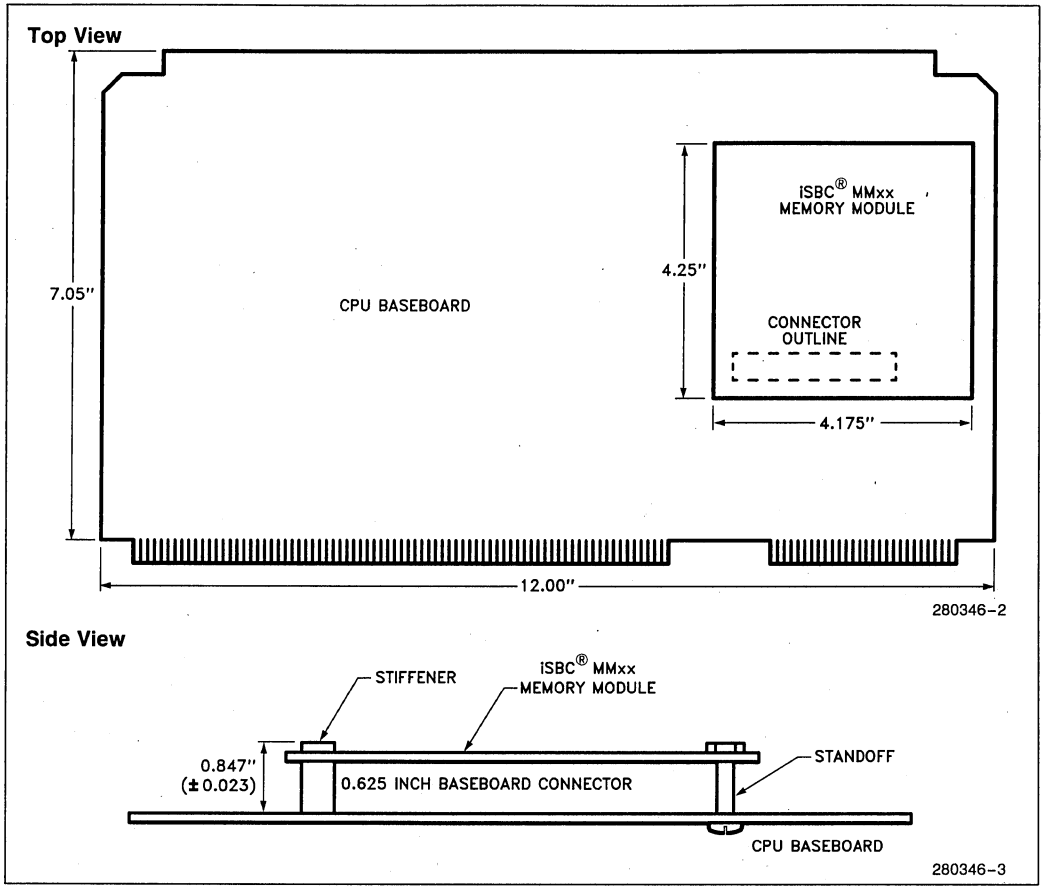
Cycle Time (All Densities)

Read/Write — 200 ns (min)

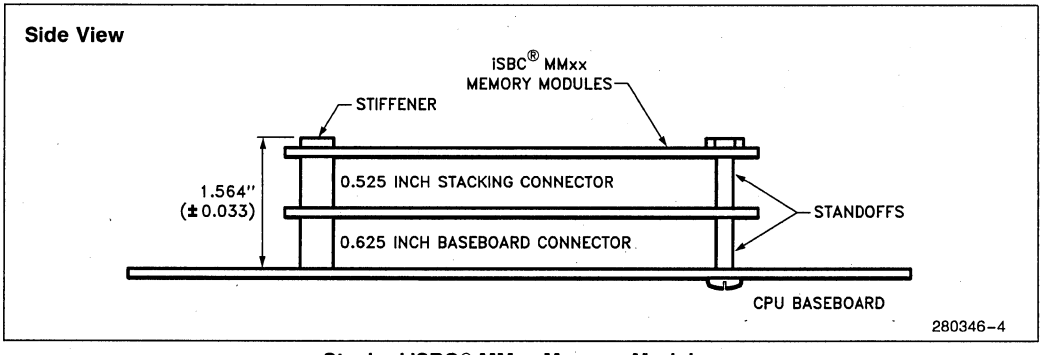
Power Requirements

Voltage −5 VDC ±5%

Memory addressing for the iSBC MMxx memory modules is controlled by the host CPU board over the memory module interface. The maximum system RAM size is 16M Bytes.



Single iSBC® MMxx Memory Module



Stacked iSBC® MMxx Memory Modules

Environmental Requirements

Operating Temperature — 0°C to 60°C

Storage Temperature — 40°C to +75°C

Cooling Requirement — 3 cubic feet per minute of airflow at an ambient temperature of 0°C to 60°C

Operating Humidity — To 95% relative humidity without condensation

Physical Dimensions

Module Alone:

Width — 4.250 inches (10,795 cm)

Length — 4.175 inches (10,604 cm)

Height — 0.500 inches (1,270 cm)

Weight — iSBC MM01/MM04: 2.5 ounces (70.0 gm)
iSBC MM02/MM08: 3.5 ounces (110.0 gm)

ORDERING INFORMATION

Part Number	Description
iSBC MM01	1M Byte RAM Memory Module
iSBC MM02	2M Byte RAM Memory Module
iSBC MM04	4M Byte RAM Memory Module
iSBC MM08	8M Byte RAM Memory Module

The Memory Modules ship with the required hardware (connectors, mounting screws, stand-offs, etc.) to stack a second module on the module already mounted on the base CPU board.

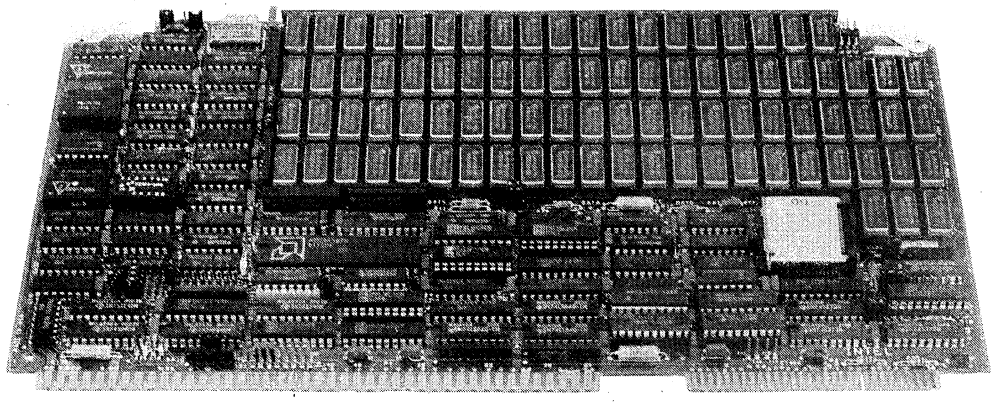
iSBC® 012CX, 010CX, AND 020CX iLBX™ RAM BOARDS

- **Dual Port Capability via MULTIBUS® and iLBX Interfaces**
- **Single Bit Error Correction and Double Bit Error Detection Utilizing Intel 8206 ECC Device**
- **512K Byte, 1024K Byte, and 2048K Byte Versions Available**
- **Control Status Register Supports Multiple ECC Operating Modes**
- **Error Status Register Provides Error Logging by Host CPU Board**
- **16 Megabyte Addressing Capability**
- **Supports 8- or 16-bit Data Transfer and 24-bit Addressing**
- **Auxiliary Power Bus and Memory Protect Logic for Battery Back-Up RAM Requirements**

The iSBC 012CX, iSBC 010CX and iSBC 020CX RAM memory boards are members of Intel's complete line of iSBC memory and I/O expansion boards. Each board interfaces directly to any iSBC 80, iSBC 86, iSBC 186, and iSBC 286 Single Board Computers. The dual port feature of the CX series of RAM-boards allow access to the memory of both the MULTIBUS and iLBX bus interfaces.

In addition to the dual port features the "CX" series of RAM-boards provide Error Checking and Corrections Circuitry (ECC) which can detect and correct single bit errors and detect, but not correct, double and most multiple bit errors.

The iSBC 012CX board contains 512K bytes of read/write memory using 64K dynamic RAM components. The iSBC 010 CX and iSBC 020 CX boards contain 1024K and 2048K bytes of read/write memory using 256K dynamic RAM components.



231023-1

September 1988
Order Number: 231023-002

FUNCTIONAL DESCRIPTION

General

The iSBC 012CX, 010CX, and 020CX RAM boards are physically and electrically compatible with the MULTIBUS interface standard, IEEE-796, as outlined in the Intel MULTIBUS specification. In addition the CX series of RAM-boards are physically and electrically compatible with the iLBX bus (Local Bus Extension) interface as outlined in the Intel iLBX Specification (see Figure 1).

Dual Port Capabilities

The "CX" series of RAM-boards can be accessed by either the MULTIBUS interface or the iLBX interface (see Figure 2). Intel's iLBX interface is an unarbitrated bus architecture which allows direct transfer of data between the CPU and the memory boards

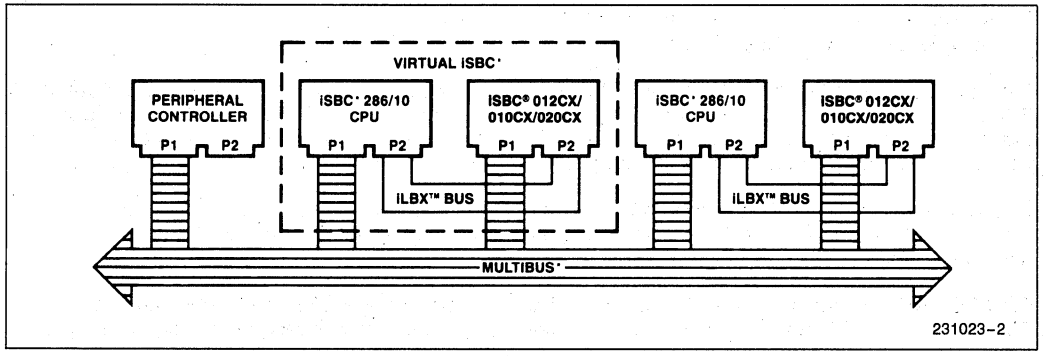


Figure 1. Typical iLBX™ System Configuration

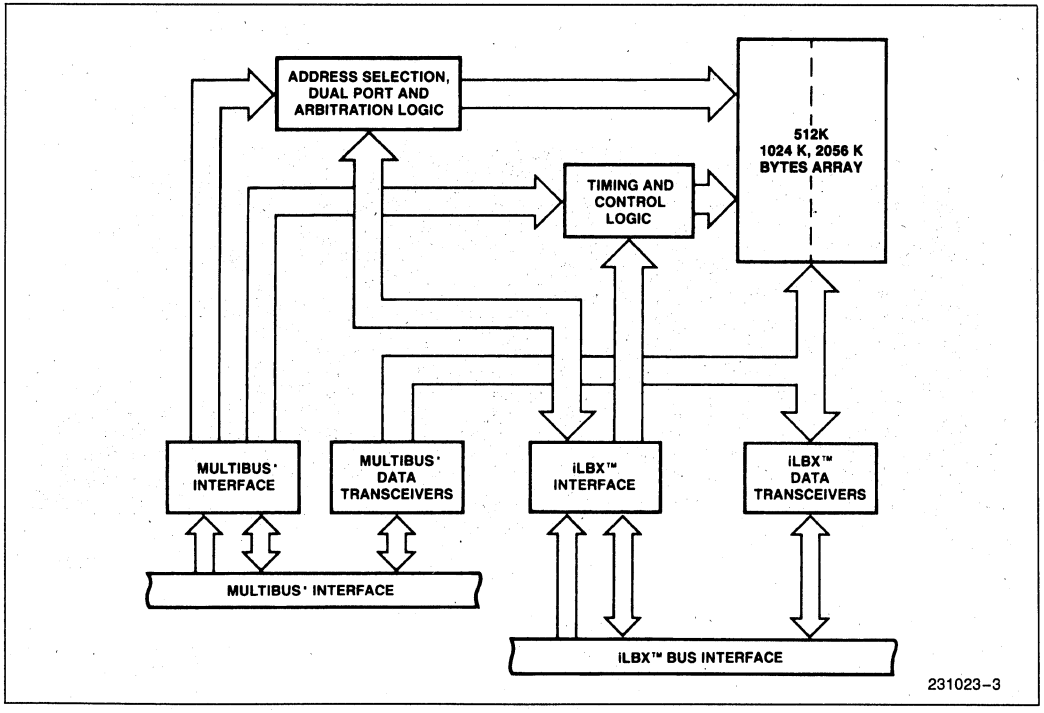


Figure 2. iSBC® 012CX/010CX/020CX Block Diagram

without accessing the MULTIBUS bus. Due to the unarbitrated nature of the iLBX interface significant improvements in memory access times result, typically a 2-6 Wait State improvement over MULTIBUS memory access.

System Memory Size

Maximum system memory size with this series of boards is 16 megabytes. Memory partitioning is independent for the MULTIBUS interface and the iLBX interface.

For MULTIBUS operations, on-board jumpers assign the board to one of four 4-megabyte pages. Each page is partitioned into 256 blocks of 16K bytes each. The smallest partition on any board in this series is 8K bytes. Jumpers assign the base address (lowest 16K block) within the selected 4-megabyte page.

The iLBX bus memory partitioning differs from the MULTIBUS bus partitioning in that the iLBX bus address space consists of 256 contiguous blocks of 64K bytes totaling 16 megabytes. As with the MULTIBUS bus partitioning, the base addresses are set with on-board jumpers.

Error Checking and Correcting (ECC)

Error checking and correction is accomplished with the Intel 8206 Error Checking and Correcting device. This ECC component, in conjunction with the ECC check bit RAM array, provides error detection and correction of single bit errors and detection only of double bit and most multiple bit errors. The ECC circuitry can be programmed via the Control Status Register (CSR) to various modes while error logging is supported by the Error Status Register (ESR). Both CSR and ESR communicate with the master CPU board through a single I/O port.

ECC I/O Address Selection

The processor board communicates with the ECC circuitry via a single I/O port. This port is used for the Control Status Register (CSR) and the Error Status Register (ESR). The CSR is programmed by the user to determine the mode of operation while the ESR provides information about memory errors.

The iSBC 012CX, iSBC 010CX, and iSBC 020CX RAM boards are shipped with a Programmed Array Logic (PAL) device which allows selecting one of 9 possible addresses for the I/O port. The actual selection is done by jumper configuration. Additional unprogrammed locations are left in the PAL to allow application specific I/O addresses to be defined.

CONTROL STATUS REGISTER

There are six ECC modes of operation in the "CX" family of RAM boards. Each mode is obtained by software programming of the CSR from the master iSBC board. The six modes are:

a. Interrupt on any error mode
b. Interrupt on non-correctable error only mode
c. Correcting mode
d. Non-correcting mode
e. Diagnostic mode
f. Examine syndrome word mode

Modes (a) and (b) can be used in conjunction with (c) and (d). The six modes are described below.

Interrupt on Any Error Mode—In this mode the RAM board will interrupt the iSBC processor board when any error (single bit or multiple bit) is detected by the ECC circuitry.

Interrupt on Non-Correctable Error Mode—In this mode the RAM board will interrupt the iSBC processor board only when a non-correctable (multiple bit) error is detected by the ECC circuitry. A multiple bit error is not correctable by the ECC circuitry.

Correcting Mode—In this mode the RAM board corrects any correctable error (single bit error). Errors which are not correctable are not modified. Interrupts are generated depending on the interrupt mode selected.

Non-Correcting Mode—In this mode the RAM board does not correct any error. The ECC circuitry continues to check for errors, but no corrective action is taken. Interrupts continue as described previously.

Diagnostic Mode—This mode is used for testing the on-board ECC circuitry. In this mode the write enable strobe to the ECC RAM array is continuously disabled. The diagnostic mode can be used to simulate errors and in conjunction with the "Examine Syndrome Word Mode" examine the check bits generated by the ECC circuitry.

Examine Syndrome Word Mode—This mode, in conjunction with the diagnostic mode, is used for testing the ECC memory. In this mode, the syndrome bits/check bits are clocked into the ESR on every memory read/write cycle, respectively. The ESR translation PROM switches to a transparent mode in the examine syndrome word mode. This allows the actual syndrome word generated by the 8206 ECC device to be examined.

Table 1. Error Status Register Format

Bit 6	Bit 5	Meaning	
0	0	Error in row	0
0	1		1
1	0		2
1	1		3

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Meaning	
0	0	0	0	0	Error in data bit	0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0		8
0	1	0	0	1		9
0	1	0	1	0	Error in data bit	10
0	1	0	1	1		11
0	1	1	0	0		12
0	1	1	0	1		13
0	1	1	1	0		14
0	1	1	1	1		15
1	0	0	0	0	Error in check bit	0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1		5
1	1	1	1	0	No Error	
1	1	1	1	1	Non-correctable (multiple-bit error)	

ERROR STATUS REGISTER

The 8-bit register contains information about memory errors. The ESR reflects the latest error occurrence. Table 1 shows the status register format. Bits 5 and 6 show the failing row while bits 0 through 4 indicate which bit (of the 16-bit data word or the 6-bit ECC syndrome) is in error. Bit 7 is always high.

Battery Back-Up/Memory Protect

An auxiliary power bus is provided to allow separate power to the RAM array for systems requiring back-up of read/write memory. An active low TTL compatible memory protect signal is brought out on the auxiliary bus connector which, when asserted, disables read/write access to the RAM board. This input is provided for the protection of RAM contents during system power-down sequences.

SPECIFICATIONS

Word Size Supported

8- or 16-bits

Memory Size

524,288 bytes (iSBC 012CX board)
1,048,576 bytes (iSBC 010CX board)
2,097,152 bytes (iSBC 020CX board)

Access Times (All densities)

MULTIBUS® System Bus

Read/Full Write— 380 ns (max)
Write Byte — 530 ns (max)

iLBX™ Local Bus

Read/Full Write— 340 ns (max)
Write Byte — 440 ns (max)

Cycle Times (All densities)

MULTIBUS® System Bus

Read/Full Write— 490 ns (max)
Write Byte — 885 ns (max)

iLBX™ Local Bus

Read/Full Write— 375 ns
Write Byte — 740 ns

NOTE:
If an error is detected, read access time and cycle times are extended to 255 ns (max)

Memory Partitioning

Maximum System memory size is 16M Bytes for both MULTIBUS and iLBX BUS. MULTIBUS partitioning is by Page, Block and Base, while the iLBX BUS is by Block and Base only.

Page Address

MULTIBUS®— 0–4 megabytes; 4–8 megabytes, 8–12 megabytes; 12–16 megabytes

iLBX™ BUS — N/A

Base Address

MULTIBUS® System Bus— Any 16K byte boundary within the 4M-byte page.

iLBX™ Local Bus — Any 64K byte boundary selectable on board boundaries to 8M-bytes and some 64K-byte boundaries in the first megabyte. Others available if PAL programming is changed.

Power Requirements

Voltage—5 VDC ±5%

Product	Current	Standby (Battery Back-Up)
iSBC® 012CX Board	4.4A (typ.) 6.8A (max.)	2.2A (typ.) 2.4A (max.)
iSBC® 010CX Board	4.8A (typ.) 7.0A (max.)	2.1A (typ.) 2.3A (max.)
iSBC® 020CX Board	5.3A (typ.) 7.5A (max.)	2.2A (typ.) 2.4A (max.)

Environmental Requirements

Operating Temperature: 0°C to 55°C airflow of 200 linear feet per minute

Operating Humidity: To 90% without condensation

Physical Dimensions

Width: 30.48 cm (12 inches)

Height: 17.15 cm (6.75 inches)

Thickness: 1.27 cm (0.50 inches)

Weight: iSBC 012CX board: 6589 gm (23.5 ounces); iSBC 010CX board: 5329 gm (19.0 ounces); iSBC 020CX board: 6589 gm (23.5 ounces)

Reference Manuals

145158-003—iSBC® 028CX/iSBC® 056CX/iSBC® 012CX Hardware Reference Manual

144456-001—Intel iLBX™ 010CX, 020CX Specification

9800683-03—Intel MULTIBUS® Specification

Manuals may be ordered from any Intel Sales Representative, Distributor Office or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA. 95051

ORDERING INFORMATION

Part Number	Description
iSBC 012CX	512K byte RAM board with ECC and iLBX Connectors
iSBC 010CX	1M byte RAM board with ECC and iLBX Connectors
iSBC 020CX	2M byte RAM board with ECC and iLBX Connectors

iSBC® 012EX, 010EX, 020EX, and 040EX HIGH PERFORMANCE RAM BOARDS

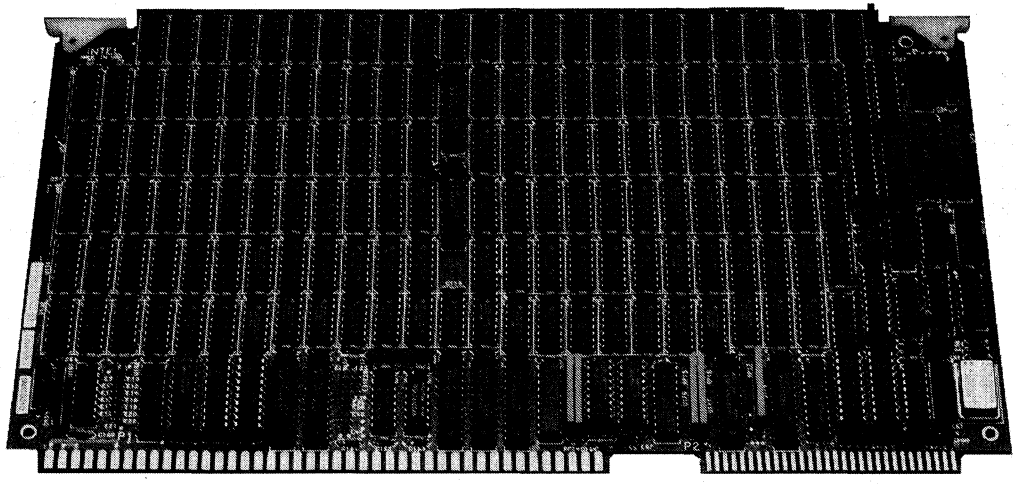
- **0 Wait States at 8 MHz Performance with the iSBC® 286/10A, iSBC 286/12 Board**
- **Dual Port Capability Via MULTIBUS® and High Speed Synchronous Interface**
- **Configurable to Function Over iLBX™ Bus**
- **On-Board Parity Generator/Checker**
- **Independently Selectable Starting and Ending Addresses**
- **16 Megabyte Addressing Capability**
- **512K Byte, 1024K Byte, 2048K Byte, and 4096K Byte Densities Available**

The iSBC 012EX, iSBC 010EX, iSBC 020EX, and iSBC 040EX RAM memory boards are members of Intel's complete line of iSBC memory and I/O expansion boards. The EX boards are dual ported between the MULTIBUS interface and one of two types of dedicated memory buses. The dedicated buses are the iLBX bus and a high speed interface. The EX series of RAM-boards can be configured to be accessed over the iLBX bus, as well as MULTIBUS bus, to provide memory support for the iSBC 286/10 board, performing at 6 MHz and the iSBC 186/03A board, performing at 8 MHz. The EX boards are default configured to run over the MULTIBUS interface and the high speed interface. This provides 0 wait state 8 MHz memory support for the iSBC 286/10A and iSBC 286/12 boards.

The EX RAM-boards generate byte oriented parity during all write operations and perform parity checking during all read operations. An on-board LED provides a visual indication that a parity error has occurred.

The iSBC 012EX, iSBC 010EX, iSBC 020EX, and iSBC 040EX boards contain 512K bytes, 1M byte, 2M bytes, and 4M bytes of read/write memory using 256K dynamic RAM components.

Due to the high speed synchronous interface capability of the boards, they are ideally suited in applications where memory performance is critical.



280142-1

September 1988
Order Number: 280142-001

FUNCTIONAL DESCRIPTION

General

The iSBC 012EX, 010EX, 020EX, and 040EX RAM boards are physically and electrically compatible with the MULTIBUS interface standard, IEEE-796, as outlined in the Intel MULTIBUS architecture specification.

Dual Port Capabilities

The "EX" series of RAM-Boards can be accessed by the MULTIBUS interface, and either the iLBX Bus, or the high speed synchronous interface (see Figures 1 and 2). The EX series require jumper and PAL configuration to be accessed over iLBX Bus.

Intel's iLBX interface is an unarbitrated bus architecture which allows direct transfer of data between the CPU and the memory boards without accessing the MULTIBUS bus. Due to the unarbitrated nature of the iLBX interface, significant improvements in memory access times compared to the MULTIBUS bus accesses result. The EX Boards provide 1 wait state performance at 6 MHz and 2 wait states at 8 MHz over the iLBX board. The EX Memory Board Hardware Reference Manual should be consulted for details.

The high speed synchronous interface, like the iLBX Bus, is a bus architecture which allows direct transfer of data between the CPU and the memory boards without accessing the MULTIBUS bus. This high speed interface runs synchronously with the iSBC 286/10A and iSBC 286/12 to provide 0 wait state performance at 8 MHz.

System Memory Size

Maximum system memory size with this series of boards is 16 megabytes. Memory partitioning is independent for the MULTIBUS interface and the iLBX interface.

Address Selection/Memory

SELECTABLE STARTING ADDRESS

A 256K boundary select is implemented on the iSBC 012EX board. A 512K boundary select is implemented on the iSBC 010EX board. A 1M boundary is implemented on the iSBC 020EX and iSBC 040EX boards.

SELECTABLE ENDING ADDRESS

The ending address is selectable as memory size minus select options of 0, 128K, 256K, or 512K on all of the EX boards.

PARITY INTERRUPT CLEAR

The I/O address of the Parity Interrupt Clear circuitry is jumperable to any one of 256 addresses.

SPECIFICATIONS

Word Size Supported

8- or 16-bits.

Memory Size

524,288 bytes (iSBC 012EX board)
1,048,576 bytes (iSBC 010EX board)
2,097,152 bytes (iSBC 020EX board)
4,194,304 bytes (iSBC 040EX board)

Access Times (All densities)

MULTIBUS® SYSTEM BUS

Read/Full Write— 375 ns (max)
Write Byte— 375 ns (max)

HIGH SPEED SYNCHRONOUS INTERFACE

Read/Full Write— 167 ns (max)
Write Byte— 132 ns (max)

iLBX™ BUS

Read/Full Write— 295 ns (max)
Write Byte— 116 ns (max)

Cycle Times (All densities)

MULTIBUS® SYSTEM BUS

Read/Full Write— 625 ns (max)
Write Byte— 625 ns (max)

HIGH SPEED SYNCHRONOUS INTERFACE

Read/Full Write— 250 ns (max)
Write Byte — 250 ns (max)

iLBX™ BUS

Read/Full Write— 437.5 ns (max)
Write Byte — 437.5 ns (max)

Memory Partitioning

Maximum System memory size is 16M Bytes for the MULTIBUS, iLBX bus and the high speed interface.

BASE ADDRESS

Board	Base Address
iSBC 012EX Board	any 256K boundary in first 4 megabytes
iSBC 010EX Board	any 512K boundary in first 8 megabytes
iSBC 020EX Board	any 1M boundary
iSBC 040EX Board	any 1M boundary

Power Requirements

Voltage—5 VDC ±5%

Product	Current
iSBC 012EX Board	3.2A (typ) 4.9A (max)
iSBC 010EX Board	3.4A (typ) 5.0A (max)
iSBC 020EX Board	3.7A (typ) 5.2A (max)
iSBC 040EX Board	3.9A (typ) 5.5A (max)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0°C to 60°C airflow of 5 cubic feet per minute

Storage Temperature: −40°C to +75°C

Operating Humidity: To 90% without condensation

PHYSICAL DIMENSIONS

Width: 12 inches (30.48 cm)
Height: 6.75 inches (17.15 cm)
Thickness: 0.50 inches (1.27 cm)
Weight: iSBC 012EX board: 6.8 ounces (1910 gm)
iSBC 010EX board: 9.0 ounces (2550 gm)
iSBC 020EX board: 13.5 ounces (3830 gm)
iSBC 040EX board: 18.0 ounces (5100 gm)

REFERENCE MANUALS

147783-001— iSBC 012EX/iSBC 010EX/iSBC 020EX/iSBC 040EX Hardware Reference Manual
9800683-03— Intel MULTIBUS Specification
144456-001— Intel iLBX Specification

Manuals may be ordered from any Intel Sales Representative, Distributor Office or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 012EX	512K byte RAM board with parity, iLBX connectors, and high speed interface
iSBC 010EX	1M byte RAM board with parity, iLBX connectors, and high speed interface
iSBC 020EX	2M byte RAM board with parity, iLBX connectors, and high speed interface
iSBC 040EX	4M byte RAM board with parity, iLBX connectors, and high speed interface

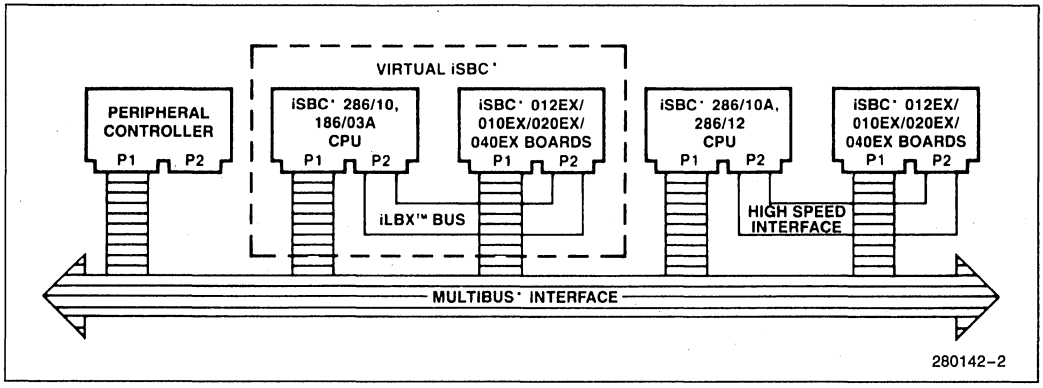


Figure 1. Typical iLBX™ System Configuration

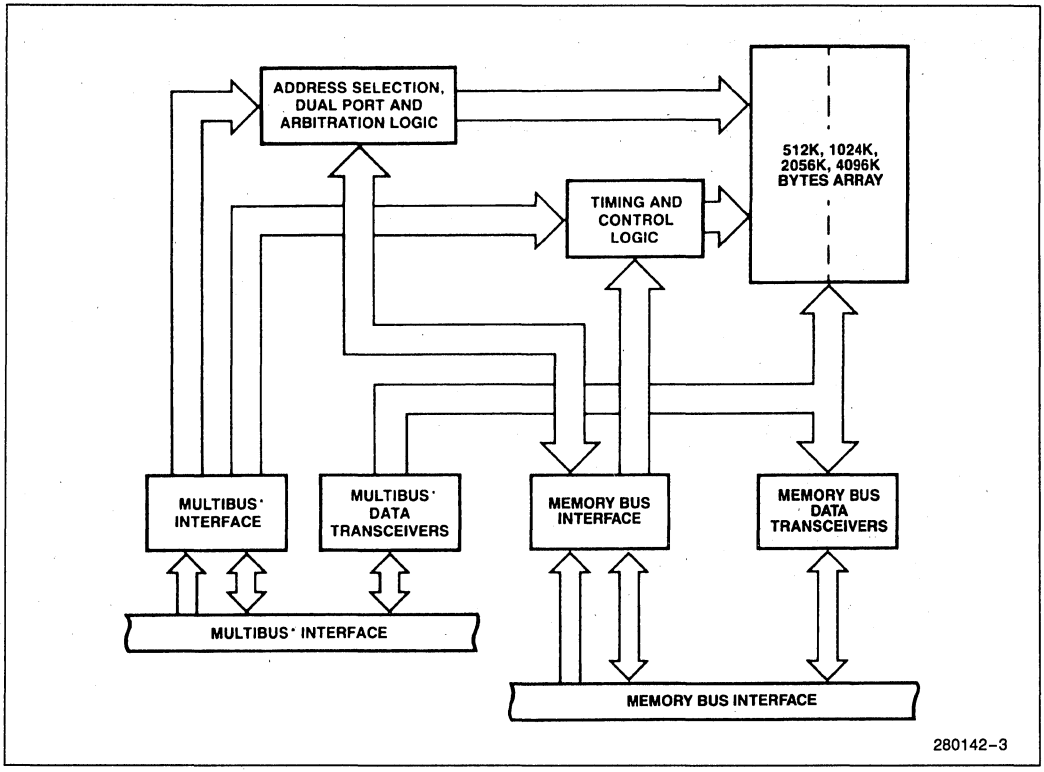
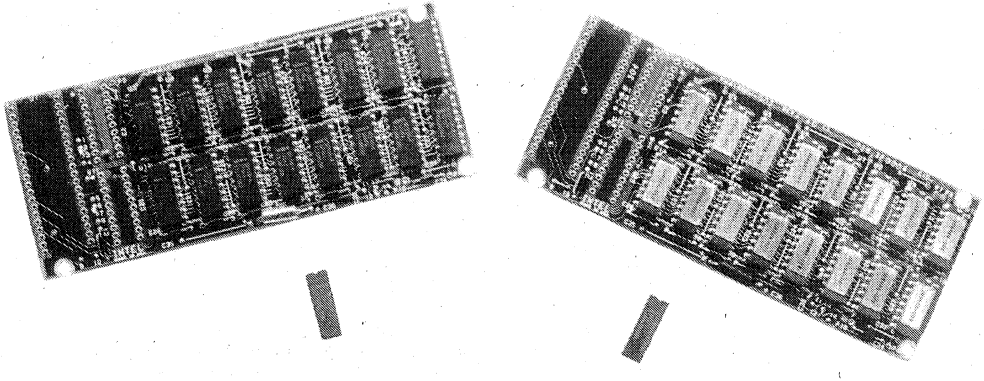


Figure 2. iSBC® EX Memory Board Block Diagram

iSBC® 304 128K BYTE RAM MULTIMODULE™ BOARD
iSBC® 300A 32K BYTE RAM MULTIMODULE™ BOARD

- **iSBC® 304 Module Provides 128K Bytes of Dual Port RAM Expansion for the iSBC 86/30 or iSBC 86/35 Board**
- **iSBC 300A Module Provides 32K Bytes of Dual Port RAM Expansion for the iSBC 86/14 Board**
- **Simple, Reliable, Mechanical and Electrical Interconnection**
- **On-Board Memory Expansion for the iSBC 86/30, iSBC 86/14 and iSBC 86/35 Single Board Computers**
- **On-board Memory Expansion Eliminates MULTIBUS® System Bus Latency and Increases System Throughput**
- **Low Power Requirements**

The iSBC 304 and iSBC 300A RAM modules provide simple, low cost expansion of the memory compliment available on the iSBC 86/30 and iSBC 86/14 Single Board Computers, respectively. Each module doubles the on-board RAM memory capacity of the host board. Additionally, the iSBC 304 provides 128K bytes RAM expansion to the iSBC 86/35 giving a total capacity of 640K bytes RAM memory. The RAM MULTIMODULE options for the host boards offer system designers a new level of flexibility in defining and implementing Intel single board computer systems. Because they expand the memory configuration on-board, they can be accessed as quickly as the existing host board memory by eliminating the need for accessing the additional memory via the MULTIBUS system bus.



210329-1

September 1987
Order Number: 210329-002

FUNCTIONAL DESCRIPTION

Each MULTIMODULE contains dynamic RAM devices and sockets for the Intel 8203 dynamic RAM controller and memory interface latching. To install the module, the latches and controller from the host CPU board are removed and inserted into sockets on the RAM MULTIMODULE. The module is then mounted onto the host board. Pins extending from the controller and latch sockets mate with device sockets underneath (see Figure 1). Additional pins mate to supply other signals to complete the electrical interface.

The module is then secured at three additional points with nylon hardware to ensure the mechanical security of the assembly.

To complete the installation, one socketed PROM is replaced on the host CPU board with the one supplied with the MULTIMODULE kit. This is the MULTIBUS address decode PROM which allows the host board logic to recognize its expanded on-board memory compliment.

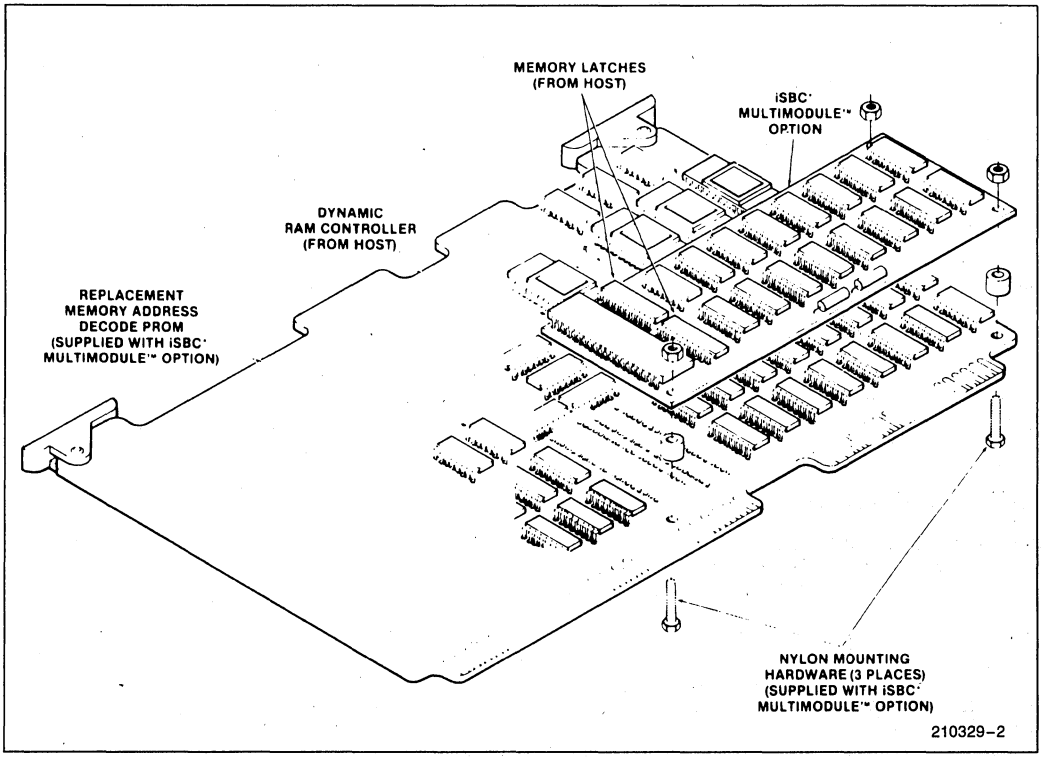


Figure 1. Installation of the MULTIMODULE™ RAM on the Host Single Board Computer

SPECIFICATIONS

Word Size

8 or 16 bits (16-bit data paths)

Memory Size

iSBC 304 Module—128K bytes RAM

iSBC 300A Module—32K bytes RAM

Cycle Time

iSBC 304—700 ns (read); 700 ns (write)

iSBC 300A—700 ns (read); 700 ns (write)

Memory Addressing

CPU ACCESS

iSBC 304 (with iSBC 86/35)—640K bytes (total capacity); 0–9FFFFH (address range)

iSBC 304 (with iSBC 86/30)—256K bytes (total capacity); 0–3FFFFH (address range)

iSBC 300A (with iSBC 86/14)—64K bytes (total capacity); 0–0FFFFH (address range)

MULTIBUS® Access

Jumper selectable for any 32K (8K) byte boundary, but not crossing a 256K (128K) byte boundary on the iSBC 86/30 (iSBC 86/14) host board.

Interface

The interfaces for the iSBC 304 and iSBC 300A module options are designed only for the iSBC 86/30 and iSBC 86/14 host boards, respectively.

Private Memory Allocation

Segments of the combined host/MULTIMODULE RAM memory may be configured as a private resource, protected from MULTIBUS system access. The amount of memory allocated as a private resource may be configured in increments of 25% of the total on-board memory ranging from 0% to 100%. The iSBC 304 module mounted on the iSBC 86/30 board, therefore, supports private allocation of 64K, 128K, 192K, or 256K bytes of RAM memory.

The iSBC 300A module mounted on the iSBC 86/14 board supports private allocation of 16K, 32K, 48K, or 64K bytes of RAM memory.

Auxiliary Power

The low power memory protection option included on the CPU host boards supports the RAM modules.

Physical Characteristics

Width: 2.4 in. (6.10 cm)

Height: 5.75 in. (14.61 cm)

Depth*: 0.72 in. (1.83 cm)

Weight: 0.13 oz. (59 g)

***NOTE:**
Combined depth including host board.

Electrical Characteristics

DC POWER REQUIREMENTS

iSBC 304: 640 mA at +15V incremental power

iSBC 300A: 256 mA at +5V incremental power

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Relative Humidity: to 90% (without condensation)

Reference Manual

All necessary documentation for the iSBC 304 and iSBC 300A MULTIMODULE boards is included in the iSBC 86/14 and iSBC 86/30 Hardware Reference Manual, Order No. 144044-002 (NOT SUPPLIED).

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

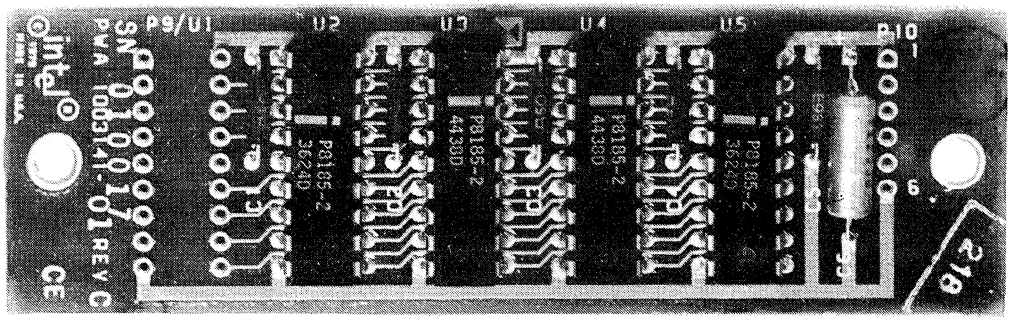
Part Number Description

SBC 304	128K MULTIMODULE option for iSBC 86/30 or iSBC 86/35 CPU boards
SBC 300A	32K MULTIMODULE option for iSBC 86/14 board

iSBC® 301
4K-BYTE RAM
MULTIMODULE™ BOARD

- **On-Board Memory Expansion to 8K Bytes for iSBC® 88/40A Single Board Computers**
- **Provides 4K Bytes of Static RAM Directly On-Board**
- **Uses 5 MHz (8185-2) RAMs**
- **Single +5V Supply**
- **0.5 Watts Incremental Power Dissipation**
- **On-Board Memory Expansion Eliminates MULTIBUS® System Bus Latency and Increases System Throughput**
- **Reliable Mechanical and Electrical Interconnection**

The Intel iSBC 301 4K-byte RAM MULTIMODULE Board provides simple, low cost expansion to double the RAM capacity on the iSBC 88/40A Single Board Computer to 8K bytes. This offers system designers a new level of flexibility in defining and implementing system memory requirements. Because memory is configured on-board, it can be accessed as quickly as the existing iSBC 88/40A memory, eliminating the need for accessing the additional memory via the MULTIBUS system bus. As a result, the iSBC 301 board provides a high speed, cost effective solution for systems requiring incremental RAM expansion. Incremental power required by the iSBC 301 module is minimal, dissipating only 0.5 watts.



280224-1

September 1988
Order Number: 280224-001

FUNCTIONAL DESCRIPTION

The iSBC 301 Board measures 3.95″ by 1.20″ and mounts above the RAM area on the iSBC 88/40A single board computer. It expands the on-board RAM capacity from 4K bytes to 8K bytes. The iSBC 301 MULTIMODULE board contains four 1K byte static RAM devices and a socket for one of the RAM devices on the iSBC 88/40A board. To install the iSBC 301 MULTIMODULE board, one of the RAMs is removed from the host board and inserted into the socket on the iSBC 301 board. The add-on board is then mounted into the vacated RAM socket on the host board. Pins extending from the RAM socket mate with the device's socket underneath (see Figure 1). Additional pins mate to the power supply and chip select lines to complete the electrical interface. The MULTIMODULE board is then secured at two additional points with nylon hardware to insure mechanical security of the assembly. With the iSBC 88/40A board mounted in the top slot of an iSBC 604 or iSBC 614 cardcage, sufficient clearance exists for mounting the iSBC 301 option. If the iSBC 88/40A board is inserted into some other slot, the combination of boards will physically (but not electrically) occupy two cardcage slots.

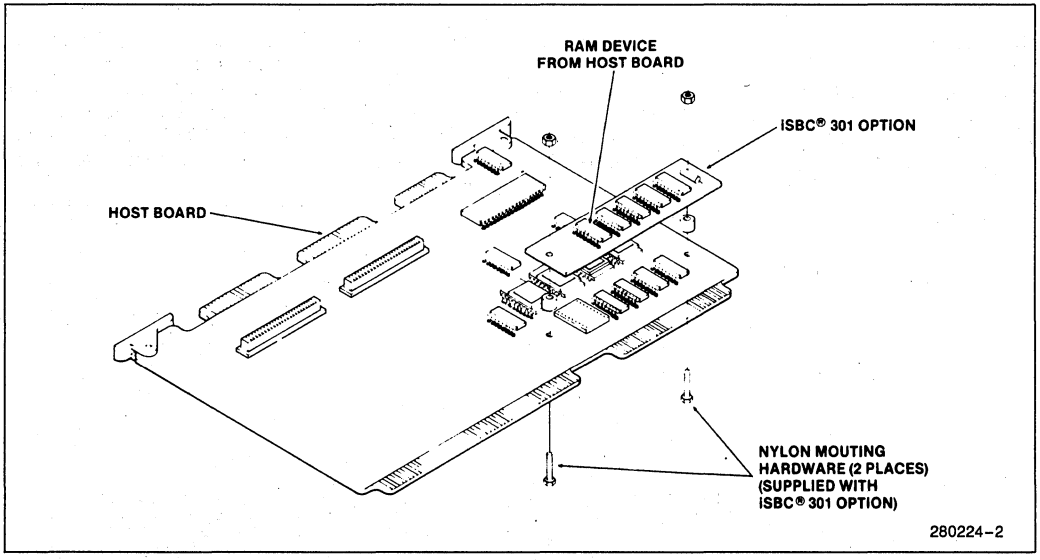


Figure 1. Installation of iSBC® 301 4K Byte RAM MULTIMODULE™ Board

SPECIFICATIONS

Word Size

8 bits

Memory Size

4096 bytes of RAM

Access Time

Read: 140 ns (from READ command)
200 ns (from ALE)
Write: 150 ns (from READ command)
190 ns (from ALE)

Memory Addressing

Memory addressing for the iSBC 301 4K-Byte-RAM MULTIMODULE Board is controlled by the host board via the address and chip select signal lines and is contiguous with the host board RAM.

iSBC 88/40A and iSBC 301 board: 00000-01FFF

Physical Characteristics

Width: 1.20 in. (3.05 cm)
Length: 3.95 in. (10.03 cm)
Height: 0.44 in. (1.12 cm) iSBC 301 Board
0.56 in. (1.42 cm)
iSBC 301 Board + host board
Weight: 0.69 oz. (19 gm)

Electrical Characteristics DC Power Requirements:

10 mA at +5 Volts incremental power

Environmental Characteristics

Operating Temperature: 0°C to +55°C
Relative Humidity: to 90% (without condensation)

Reference Manuals

All necessary documentation for the iSBC 301 MULTIMODULE board is included in the CPU board Hardware Reference Manual (NOT SUPPLIED)

iSBC 88/40A—Order No. 147049-001

Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

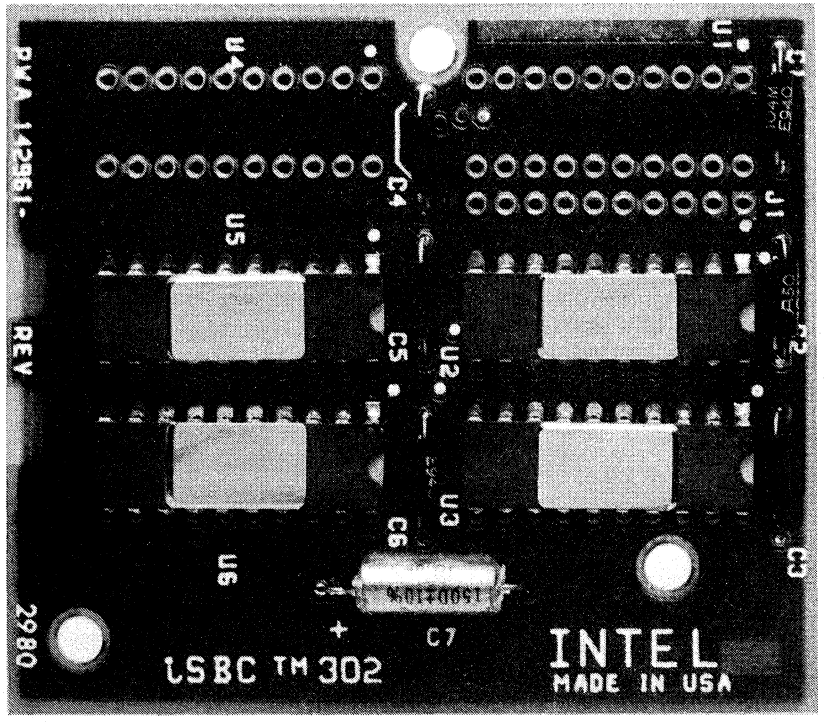
SPECIFICATIONS

Part Number	Description
SBC 301	4K Byte RAM MULTIMODULE Board

iSBC® 302
8K BYTE RAM MULTIMODULE™

- **Expands On-Board Memory of the iSBC 86/05A and iSBC 88/25 Signal Board Computers**
- **Uses Four Intel 2168 Static RAMs**
- **Single +5V Supply**
- **On-Board Memory Expansion Eliminates System Bus Latency and Increases System Throughput**
- **Reliable Mechanical and Electrical Interconnection**

The Intel iSBC 302 8K byte MULTIMODULE RAM provides simple, low cost expansion to double the RAM capacity on the iSBC 86/05A Single Board Computer to 16K bytes or increase RAM capacity on the iSBC 88/25 Single Board Computer to 12K bytes. This offers system designers a new level of flexibility in implementing system memory. Because the MULTIMODULE memory is configured on-board, it can be accessed as quickly as the standard on-board iSBC 86/05A or iSBC 88/25 memory, eliminating the need for accessing the additional memory via the MULTIBUS system bus. As a result, the iSBC 302 board provides a high-speed, cost effective solution for systems requiring incremental RAM expansion.



280225-1

September 1988
Order Number: 280225-001

FUNCTIONAL DESCRIPTION

The iSBC 302 MULTIMODULE measures 2.60″ by 2.30″ and mounts above the RAM area on the iSBC 86/05A or iSBC 88/25 Single Board Computer. The iSBC 302 MULTIMODULE board contains four 4K x 4 static RAM devices and sockets for two of the RAM devices on the iSBC 80/05A board. With the iSBC 302 MULTIMODULE mounted on the iSBC 88/25 board, the two sockets on the iSBC 302 MULTIMODULE may be filled with 4K x 4 static RAMs. The two sockets on the iSBC 302 module have extended pins which mate with two sockets on the base board. Additional pins mate to the power supply and chip select lines to complete the electrical interface. The mechanical integrity of the assembly is assured with nylon hardware securing the module in two places. With the iSBC 86/05A or iSBC 88/25 board mounted in the top slot of an iSBC 604/614 cardcage, sufficient clearance exists for the mounted iSBC 302 option. If the iSBC 86/05A or iSBC 88/25 board is inserted into some other slot, the combination of the boards will physically (but not electrically) occupy two cardcage slots.

SPECIFICATIONS

Word Size

8/16 bits

Memory Size

16,384 bytes of RAM

Cycle Time

Provides "no wait state"memory operations on the iSBC 86/05A board at 5 MHz or 8 MHz or the iSBC 88/25 at 5 MHz.

5 MHz cycle time — 800 ns
8 MHz cycle time — 500 ns

Memory Addressing

Memory addressing for the iSBC 302 MULTIMODULE board is controlled by the host board via the address and chip select signal lines.

With the iSBC 86/05A board:

The 8K bytes of RAM on the iSBC 302 board occupy the 8K byte address space immediately after that of the iSBC 86/05A board's 8K RAM (i.e., default configuration —

iSBC 86/05A board's RAM — $00000-01FFF_H$

iSBC 302 board's RAM — $02000-03FFF_H$).

With the iSBC 88/25 board:

The 8K bytes of RAM on the iSBC 302 board occupy the 8K byte address space immediately after that of the iSBC 88/25 board's 4K RAM (i.e., default configuration —

iSBC 88/25 board's RAM — $0-0FFF_H$

iSBC 302 board's RAM — $01000_H-02FFF_H$).

Physical Characteristics

Width: 2.6 in. (6.60 cm)

Length: 2.3 in. (5.84 cm)

Height: 0.56 in. (1.42 cm) iSBC 302 board + iSBC 86/05A or iSC 88/25 board

Weight: 1.25 oz. (35 gm)

Electrical Characteristics

DC Power Requirements: 720 mA at +5V incremental power

Environmental Characteristics

Operating Temperature: 0°C to +55°C

Relative Humidity: to 90% (without condensation)

Reference Manuals

All necessary documentation for the iSBC 302 MULTIMODULE board is included in the CPU board Hardware Reference Manuals (NOT SUPPLIED).

iSBC 86/05A —Order No. 147162-002

iSBC 88/25 —Order No. 143825-002

Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

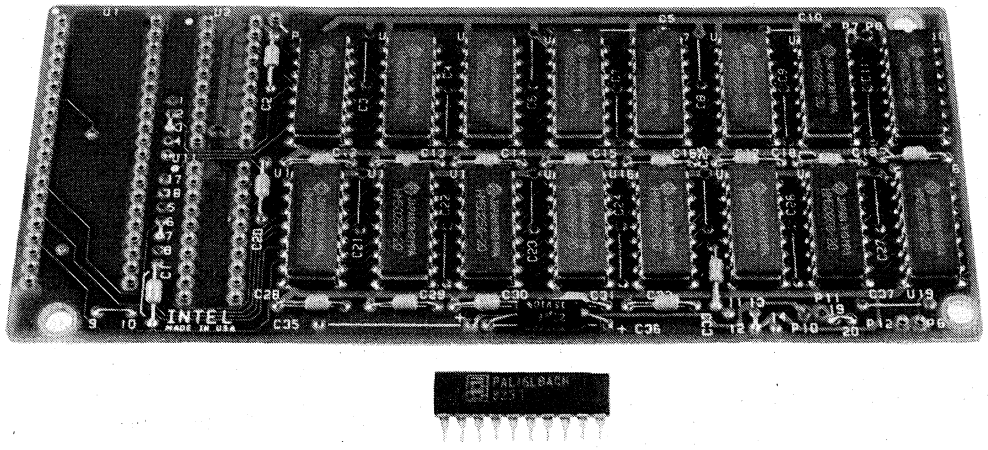
ORDERING INFORMATION

Part Number	Description
SBC 302	8K byte RAM MULTIMODULE

iSBC® 314
512K BYTE RAM MULTIMODULE™ BOARD

- **On-Board Memory Expansion for the iSBC 86/35 Single Board Computer**
- **iSBC 314 Module Provides 512K Bytes of Dual Port RAM Expansion for the iSBC 86/35 Board**
- **Reliable Mechanical and Electrical Interconnection**
- **Completes iSBC 86/35 Memory Array Providing a Full Megabyte Page of System Memory**
- **Increases System Throughput by Reducing Accesses to MULTIBUS® Global Memory**
- **Low Power Requirements**
- **Battery Backup Capability**

The iSBC 314 512K byte RAM MULTIMODULE board provides simple, low cost expansion to double the on-board RAM capacity of the iSBC 86/35 Single Board Computer host to one megabyte. This RAM MULTIMODULE option offers system designers a simple, practical solution to expanding and improving the memory capability and performance of the iSBC 86/35 board. The iSBC 314 memory is configured on-board and can be accessed as quickly as the standard iSBC 86/35 memory, eliminating the need for accessing additional memory via the MULTIBUS system bus.



280000-1

October 1986
Order Number: 280000-002

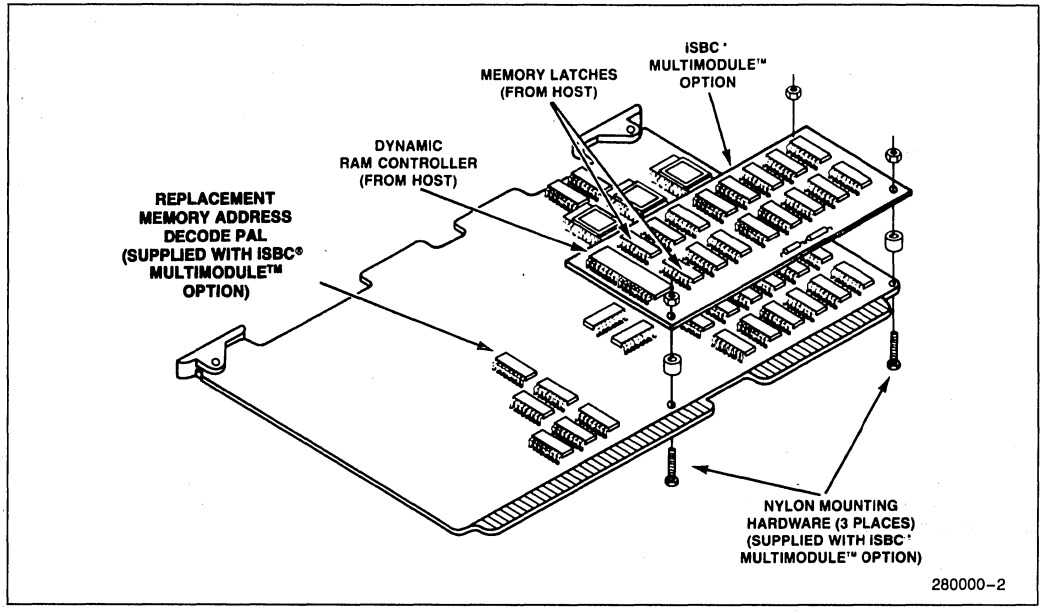


Figure 1. Installation of the MULTIMODULE™ RAM Module on the Host Single Board Computer

FUNCTIONAL DESCRIPTION

The iSBC 314 MULTIMODULE board measures 2.40″ by 5.75″ and mounts above the RAM array on the iSBC 86/35 Single Board Computer. The iSBC 314 board contains sixteen 256 Kbit x 1 dynamic RAM devices and three sockets; two for the memory latches and one for the Intel 8203 dynamic RAM controller. The addition of the iSBC 314 memory MULTIMODULE board to the iSBC 86/35 board makes possible a one megabyte single board solution; the full direct addressing capability of the iAPX 86 CPU.

To install the module, the latches and controller from the host iSBC 86/35 board, are removed and inserted into sockets on the iSBC 314 board. The module is then mounted onto the host board. Pins extending from the controller and latch sockets mate with device sockets underneath (see Figure 1). Additional pins mate to supply other signals to complete the electrical interface. The module is then secured at three additional points with nylon hardware to ensure the mechanical security of the assembly.

To complete the installation, one socketed PAL is replaced on the iSBC 86/35 board with the one supplied with the MULTIMODULE kit. This is the PAL which allows the host board logic to recognize its expanded on-board memory compliment.

SPECIFICATIONS

Word Size

8 or 16 bits (16-bit data paths)

Memory Size

512K bytes RAM

System Cycle Time (8 MHz, 2 Wait States)

750 ns (read); 750 ns (write)

NOTE:
1 wait state achieved with jumper change on iSBC 86/35 board.

Memory Addressing

iSBC 314 module with iSBC 86/35 board — 1M byte (total capacity); 0–FFFFFH. (See Figure 2, Memory Allocation)

Interface

The interface for the iSBC 314 MULTIMODULE board option is designed only for the iSBC 86/35 host board.

Wait-State Performance

A significant performance advantage of 2 wait-states is achieved when accessing memory on-board the iSBC 86/35 versus the performance of 6 wait-states when accessing memory off-board over the MULTIBUS. The iSBC 314 puts an additional 512K bytes of system memory on-board the iSBC 86/35 reducing the execution time by as much as 70%.

Memory Allocation

Segments of the combined host/MULTIMODULE RAM may be configured to be accessed either from off-board or on-board resources. The amount of memory allocated as either public or private resource may be configured in a variety of sizes. The address range boundaries for the 1 megabyte of RAM array of the iSBC 314 and iSBC 86/35 board combination are shown in Figure 2 for accesses from both on-board and off-board resources.

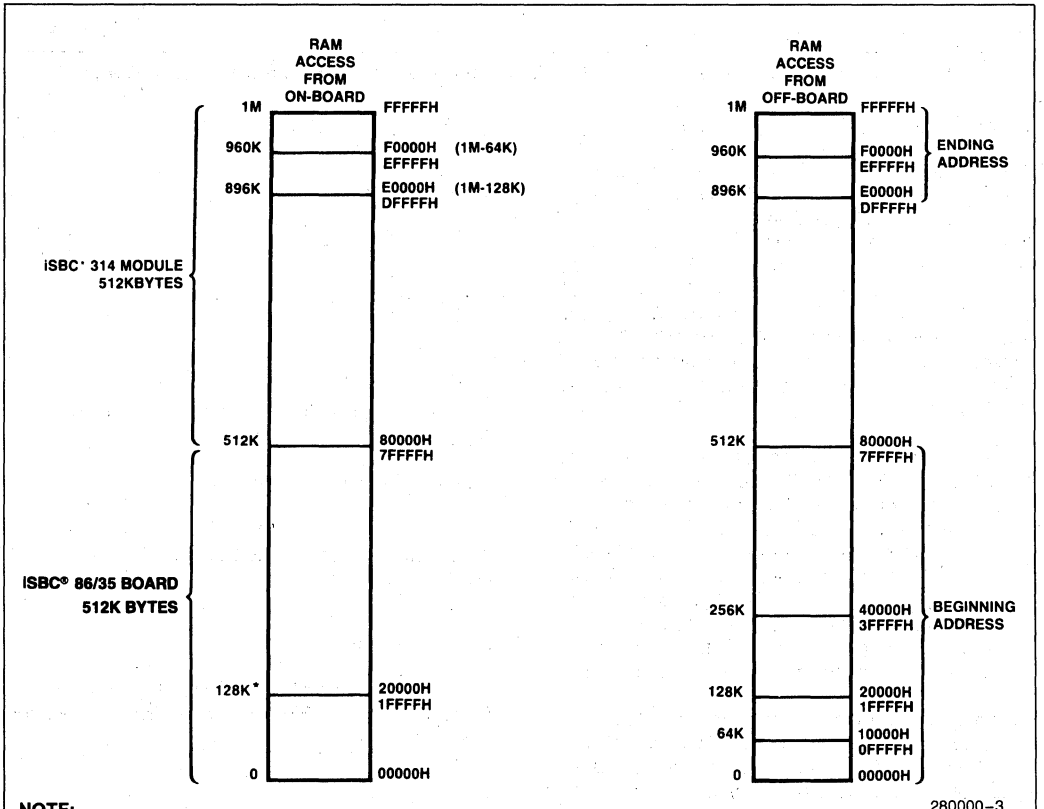
Auxiliary Power

The low power memory protection option included on the iSBC 86/35 board supports the iSBC 314 module.

Physical Characteristics

Width: 2.4 in. (6.10 cm)
Length: 5.75 in. (14.61 cm)
Depth*: 0.72 in. (1.83 cm)
Weight: 0.13 oz. (59g)

NOTE:
*Combined depth including host board.



NOTE:
All memory above this boundary may be disabled under software control to allow access to MULTIBUS® system bus.

Figure 2. Address Range Selection

Electrical Characteristics

DC Power Requirements*

*Additional power required by the iSBC 314 MULTIMODULE is:

Typical: 60 mA @ +5V

Maximum: 140 mA @ +5V

Environmental Characteristics

Operating Temperature: 0°C to +55°C

Relative Humidity: to 90% (without condensation)

Reference Manual

All necessary documentation for the iSBC 314 MULTIMODULE board is included in the iSBC 86/35 Hardware Reference Manual (NOT SUPPLIED); Order Number: 146245-002.

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

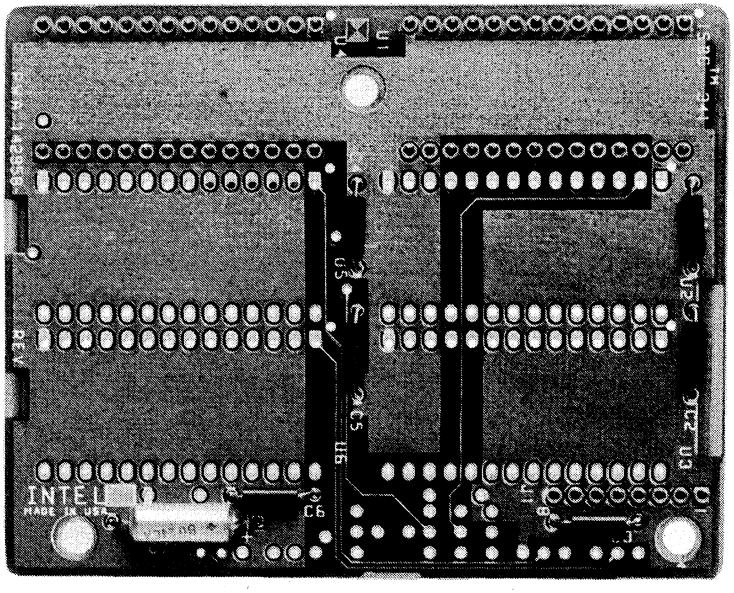
Part Number	Description
iSBC® 314	512K byte Memory MULTIMODULE option for iSBC 86/35 board

iSBC® 341
28-PIN MULTIMODULE™ EPROM

- **On-board Memory Expansion for iSBC® 86/05A, iSBC 88/25, iSBC 186/03A, iSBC 286/10A, iSBC 286/12 Series, and iSBC 88/40A Microcomputers**
- **Supports JEDEC 24/28-Pin Standard Memory Devices, Including EPROMs, Byte-Wide RAMs, and E²PROMs**
- **Sockets for Up to 256K Bytes of Expansion with Intel 27512 EPROMs**
- **On-Board Expansion Provides "No Wait State" Memory Access with Selected Devices**
- **Simple, Reliable Mechanical and Electrical Interface**

The iSBC 341 28-pin MULTIMODULE EPROM board provides simple, low-cost expansion of the on-board EPROM capacity of the iSBC 86/05A, the iSBC 88/25, iSBC 186/03A, iSBC 286/10A, iSBC 286/12 Series Single Board Computers and the iSBC 88/40A Measurement and Control Computer. Four additional 28-pin sockets support JEDEC 24/28-pin standard devices, including EPROMs, byte-wide static and psuedo-static RAMs.

The MULTIMODULE expansion concept provides the optimum mechanism for incremental memory expansion. Mounting directly on the microcomputer, the benefits include low cost, no additional power requirements beyond the memory devices, and higher performance than MULTIBUS-based memory expansion.



280214-1

October 1988
Order Number: 280214-001

FUNCTIONAL DESCRIPTION

The iSBC 341 28-pin MULTIMODULE EPROM option effectively doubles the number of sockets available for EPROM on the base microcomputer board on which it is mounted. The iSBC 341 board contains six 28-pin sockets. Two of the sockets have extended pins which mate with two of the sockets on the base board. Two of the EPROMs which would have been inserted in the base board are then reinserted in the iSBC 341 sockets. Additional interface pins also connect chip select lines and power. The mechanical integrity of the assembly is assured with nylon hardware securing the unit in two places.

Through its unique interface, the iSBC 341 board can support 8- or 16-bit data paths. The data path width is determined by the base board—being 8 bits for the iSBC 88/40A and iSBC 88/25 microcomputers, and 8/16 bits for the iSBC 86/05A, iSBC 186/03A, iSBC 286/10A, and iSBC 286/12 Series Single Board Computers.

SPECIFICATIONS

Word Size

8 or 8/16 bits (determined by data path width of base board).

Memory Size

256K bytes with available technology (JEDEC standard defines device pin-out to 512-bit devices).

Device Size (Bytes)	EPROM Type	Max iSBC® 341 Capacity (Bytes)
2K x 8	2716	8K
4K x 8	2732A	16K
8K x 8	2764	32K
16K x 8	27128	64K
32K x 8	27256	128K
64K x 8	27512	256K

Access Time

Varies according to base board and memory device access time. Consult data sheet of base board for details.

Memory Addressing

Consult data sheet of base board for addressing data.

POWER REQUIREMENTS

Devices(1)	Max Current @ 5V ±5%
2716	420 mA
2732A	600 mA
2764	600 mA

NOTE:
1. Incremental power drawn from host board for four additional devices.

Auxiliary Power

There are no provisions for auxiliary power (battery backup) on the iSBC 341 option.

Physical Characteristics

Width: 3.4 in. (8.64 cm)

Length: 2.7 in. (6.86 cm)

Height: 0.78 in. (1.98 cm)*

Weight: 5 oz. (141.5 gm)

*Includes height of mounted memory devices and base board.

All necessary mounting hardware (nylon screws, spacers, nuts) is supplied with each kit.

Environmental Characteristics

Operating Temperature: 0°C to +55°C

Relative Humidity: to 90% (without condensation)

Reference Manuals

All necessary documentation for the iSBC 341 module is included in the CPU board Hardware Reference Manuals (NOT SUPPLIED)

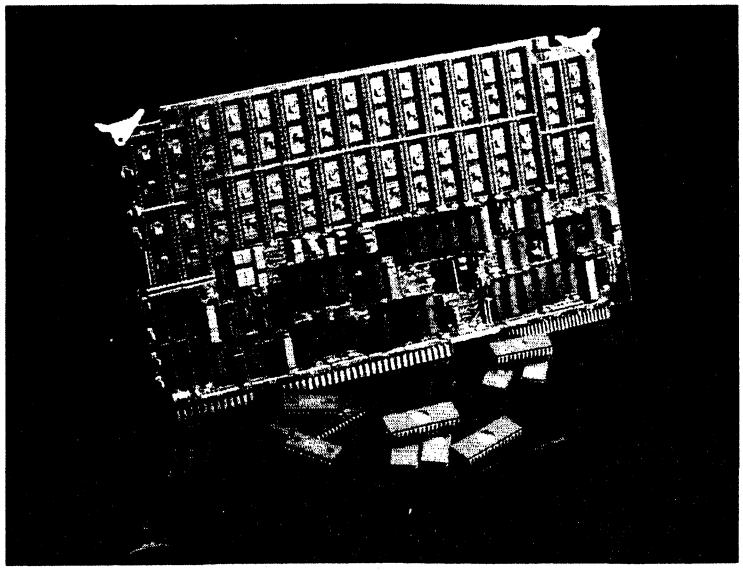
iSBC 186/03A — Order No. 148060-001
iSBC 86/05A — Order No. 147162-002
iSBC 88/25 — Order No. 143825-002
iSBC 88/40A — Order No. 147049-001
iSBC 286/10A — Order No. 147532-001
iSBC 286/12 — Order No. 147533-001

Manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 341	28-Pin MULTIMODULE EPROM

iSBC® 429 UNIVERSAL SITE MEMORY EXPANSION BOARD



CMOS MULTIBUS®I MEMORY EXPANSION BOARD SUPPORTS LATEST MEMORY TECHNOLOGY

The iSBC 429 board provides a wide range of memory expansion capabilities for MULTIBUS designs. Up to 4 MBytes of memory can be installed using EPROM, Flash memory, SRAM, E²PROM or Static NVRAM.

The CMOS implementation of the iSBC 429 makes it ideal for low power applications.

All of Intel's Single Board Computers can communicate with the iSBC 429 using the MULTIBUS System bus. Alternatively, the iSBC 429 may be optionally configured to use the iLBX™ bus for faster access to the iSBC 186/03A, 286/10A, 286/12 series or 386/12 series of Single Board Computers.

FEATURES:

- Supports EPROM, Page Mode EPROM, E²PROM, Flash Memory, SRAM and Static NVRAM
- Thirty-two standard 32-pin JEDEC sites (supports both 28-pin and 32-pin devices) up to 4MByte capacity
- iLBX Bus or MULTIBUS Configurability
- Low power CMOS design
- Battery Backup/Memory Protect support
- Assignable anywhere within a 16 Megabyte address space on 4K byte boundaries

September, 1988
Order Number: 280668-001

FEATURES

iLBX Bus

The iSBC 429 board can be configured via jumpers to communicate with either the MULTIBUS interface or the iLBX Bus interface. Significant memory access time improvements can be realized using the iLBX Bus interface versus the MULTIBUS interface, due to its dedicated, unarbitrated architecture. Additional information on the iLBX Bus is available in the iLBX Specification, order number 145695-Rev. A.

CMOS DESIGN

For embedded control applications which are sensitive to power consumption, the iSBC 429 was designed with CMOS components and it will support many CMOS memory devices. Unpopulated, the iSBC 429 requires 5.25 watts at 5 volts.

FLASH MEMORY SUPPORT

The iSBC 429 board supports Intel's new CMOS Flash Memory devices. These new memory devices offer the most cost-effective and reliable alternative for updatable non-volatile memory. Memory contents can be erased and reprogrammed on-board during subassembly test, in-system during final test, and in-system after sale.

MEMORY BANKS

The thirty-two sites on the iSBC 429 board are partitioned into two banks of 16 sites each. Both banks are independently configurable to any of the device types supported on the board. Each bank can support up to 2 Megabytes using 27010 devices.

MEMORY ADDRESSING

The address space of each bank can be independently configured for starting address and size. The starting address can be on any 4 KByte boundary within the 16 MByte MULTIBUS address space. The size of each bank is a multiple of 64 KBytes.

MODE OF OPERATION

The iSBC 429 board can operate in one of two modes: the 8 bit only mode or the 8/16 bit mode. The 8 bit mode provides the most efficient memory configuration for systems handling 8 bit data only. The 8/16 bit mode allows the iSBC 429 board to be compatible with systems employing 8 bit and 16 bit masters. The mode of operation is selected by on-board jumpers and is available for both MULTIBUS and iLBX Bus configurations.

MEMORY ACCESS

The iSBC 429 board has jumper-selectable access times for each bank which allows the board to be tailored to the performance of the particular devices which are installed in the iSBC 429 board. The iSBC 429 accepts devices with an access time ranging from 150 ns with a minimum granularity of 99 ns and results in a board access time from 182 ns to 1667 ns. Each bank can be configured for access time.

INHIBITS

Inhibit signals are provided on the iSBC 429 board to allow ROM to overlay RAM for bootstrapping or diagnostic operations. Each bank of the iSBC 429 board can be overlayed with the system RAM by jumpers provided on the board. (i.e. If banks are overlapped, inhibits can be used to select the appropriate bank.)

BATTERY BACKUP

The iSBC 429 board supports battery backup operation via a connector on the board. An auxiliary power bus is provided to allow separate power to the memory array for systems requiring battery backup. Selection of this auxiliary power bus is made via jumpers on the board.

An active-low TTL compatible Memory Protect signal is brought out on the auxiliary connector which, when asserted, disables access to the memory array. This input is provided for the protection of Memory contents during system power-down sequences.

INTEL QUALITY—YOUR GUARANTEE

The iSBC 429 is designed and manufactured in accordance with Intel's high quality standards. We then verify quality through rigorous testing in our state-of-the-art Environmental Test Laboratory.

WORLDWIDE SERVICE AND SUPPORT

The iSBC 429 is fully supported by Intel's worldwide network of field application engineers. We're experts in developing a variety of real-time and system applications and want to make your design succeed.

SPECIFICATIONS

MEMORY DEVICES SUPPORTED BY THE iSBC 429

Size / Type	8K x 8	16K x 8	32K x 8	64K x 8	128K x 8	256K x 8	4 x 16K x 8	8 x 16K x 8
EPROM	2764	27128	27256	27512	27010	27020	—	—
ROM	✓[1]	✓	✓	✓	✓	✓	—	—
Page Mode EPROM	—	—	—	—	—	—	27513	27011
E²PROM[2]	2864A	—	—	—	—	—	—	—
Flash Memory[3]	27F64	—	27F256 28F256	—	—	—	—	—
Static NVRAM[4]	✓	—	✓	—	—	—	—	—
SRAM	✓	—	✓	—	—	—	—	—

[1] "✓" denotes that the iSBC 429 board will support the device indicated, but that it is not currently available from Intel.
[2] Five Volt only, Enhanced
[3] 12 Volt V_{pp} only
[4] Static NVRAM devices exceed the height specification for MULTIBUS. The iSBC 429 will occupy more than one slot with these devices installed.

WORD SIZE

8 or 8/16 bits

MEMORY SIZE

Sockets are provided for up to thirty-two 32-pin or 28-pin devices which can provide up to 4 Megabytes of EPROM/ ROM/SRAM/Flash Memory.

ACCESS TIME

Access time is jumperable from 182 ns to 1667 ns with a granularity of 99 ns to optimize performance for the devices which are installed and is equivalent for MULTIBUS and iLBX Bus.

POWER REQUIREMENTS

V_{cc} = 5 volts ± 5%
V_{pp} = 12 volts ± 5%
I_{cc} = 1.2 amps, maximum, without any memory devices in the board.

PHYSICAL CHARACTERISTICS

Width - 12.00 inches (30.48 cm)
Depth - 7.05 inches (17.91 cm)
Height - .5 inches (1.27 cm)

ENVIRONMENT

Operating Temperature - 0°C to + 60°C (Convection cooling)
Relative Humidity - 90% non-condensing

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
SBC 429	Universal Site Memory Expansion Board

REFERENCE MANUAL

457317-001 - iSBC 429 Hardware Reference Manual (NOT SUPPLIED)

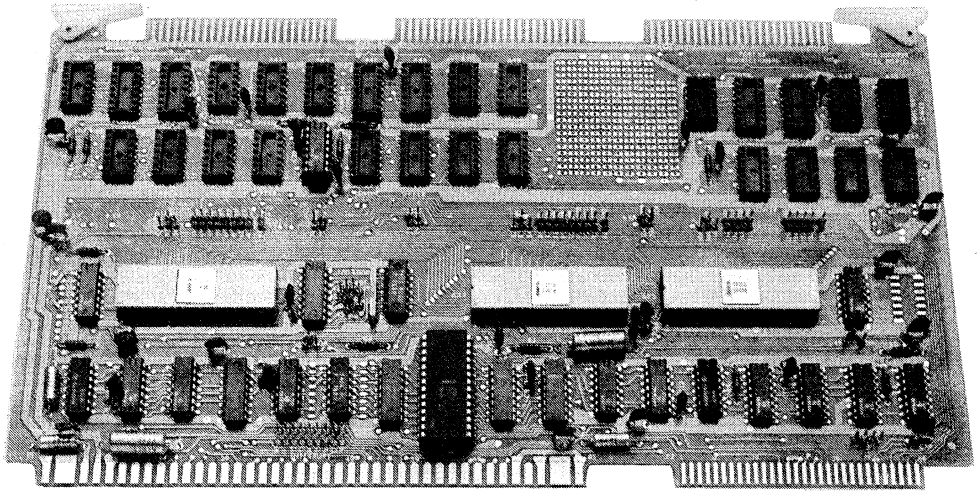
ADDITIONAL LITERATURE

980683-004 - Intel MULTIBUS Specification Manual
145695-001 - iLBX Bus Specification

iSBC® 519/iSBC® 519A PROGRAMMABLE I/O EXPANSION BOARD

- **iSBC® I/O Expansion via Direct MULTIBUS® Interface**
- **72 Programmable I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **iSBC® 519A Provides Full 16-Bit I/O Addressability**
- **iSBC® 519A Provides 3 iSBX Multimodule Connectors**
- **iSBC® 519A Provides 16 Maskable Interrupt Request Lines**
- **Jumper Selectable 0.5, 1.0, 2.0, or 4.0 ms Interval Timer**
- **The iSBC® 519 Provides Eight Maskable Interrupt Request Lines with Priority Encoded and Programmable Interrupt Algorithms**

The iSBC 519/iSBC 519A Programmable I/O Expansion Board is a member of Intel's complete line of iSBC memory and I/O expansion boards. The iSBC 519/iSBC 519A interfaces directly to any iSBC single board computer via the system bus to expand input and output port capacity. The iSBC 519/iSBC 519A provides 72 programmable I/O lines. The system software is used to configure the I/O lines to meet a wide variety of peripheral requirements. The flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. Address selection is accomplished by using wire-wrap jumpers. The board operates with a single +5V power supply.



280230-1

September 1988
Order Number: 280230-001

FUNCTIONAL DESCRIPTION

The 72 programmable I/O lines on the iSBC 519/ iSBC 519A are implemented utilizing three Intel 8255A programmable peripheral interfaces. The system software is used to configure the I/O lines in combinations of undirectional input/output and bidirectional ports. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. The 72 programmable I/O lines and signal ground lines are brought out to three 50-pin edge connectors that mate with flat, round, or woven cable.

Interval Timer

Typical I/O read access time is 350 nanoseconds.

Typical I/O read/write cycle time is 450 nanoseconds. The interval timer provided on the iSBC 519/ iSBC 519A may be used to generate real time clocking in systems requiring the periodic monitoring of I/O functions. The time interval is derived from the constant clock (BUS CCLK) and the timing interval is jumper selectable. Intervals of 0.5, 1.0, 2.0, and 4.0 milliseconds may be selected when an iSBC single board computer is used to generate the clock. Other timing intervals may be generated if the user provides a separate constant clock reference in the system.

Eight-Level Vectored Interrupt

Intel 8259A programmable interrupt controller(s) (PIC) provides vectoring for interrupt levels. As shown in Table 1, a selection of three priority processing algorithms is available to the system designer so that the manner in which requests are serviced may be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation.

Table 1. Interrupt Priority Options

Algorithm	Operation
Fully nested	Interrupt request line priorities fixed.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels are based in sequence numerically on this assignment.

iSBX™ MULTIMODULE™ Expansion Capabilities

Three iSBX MULTIMODULE connectors are provided on the iSBC 519A board. Up to three single wide MULTIMODULE or one double wide and one single wide iSBX MULTIMODULE can be added to the iSBC 519A board. A wide variety of expansion options are available.

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm),
1.16 in. (2.95 cm) with iSBX modules
Weight: 14 oz. (397.3 gm)

Electrical Characteristics

Average DC Current

Voltage	Without Termination(1)	With Termination(2)
V_{CC} = +5V ±5%	I_{CC} = 1.5A max	3.5A max

NOTES:
1. Does not include power required for operational I/O drivers and I/O terminators.
2. With 18 220Ω/330Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature: 0°C to +55°C

Reference Manual

9800385B—iSBC 519/iSBC 519A Hardware Reference manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 519	Programmable I/O Expansion Board
SBC 519A	Programmable I/O Expansion Board

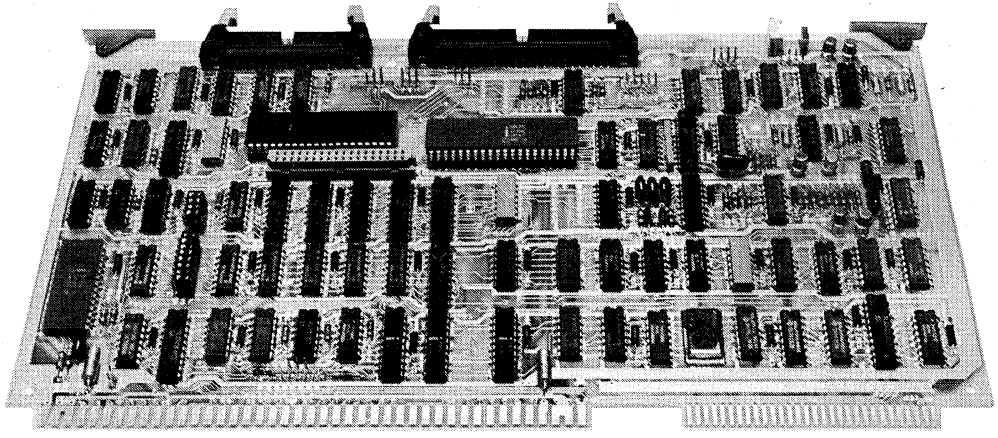
MULTIBUS® I Peripheral Controllers

5

iSBC® 208
FLEXIBLE DISKETTE CONTROLLER

- **Compatible with All iSBC® 80, iSBC 86, and iSBC 88 Single Board Computers**
- **Controls Most Single and Double Density Diskette Drives**
- **On-Board iSBX™ Bus for Additional Functions**
- **User-Programmable Drive Parameters allow Wide Choice of Drives**
- **Phase Lock Loop Data Separator Assures Maximum Data Integrity**
- **Read and Write on Single or Multiple Sectors**
- **Single +5V Supply**
- **Capable of Addressing 16M Bytes of System Memory**

The Intel iSBC 208 Flexible Disk Controller is a diskette controller capable of supporting virtually any soft-sectored, double density or single density diskette drive. The standard controller can control up to four drives with up to eight surfaces. In addition to the standard IBM 3740 formats and IBM System 34 formats, the controller supports sector lengths of up to 8192 bytes. The iSBC 208 board's wide range of drive compatiblity is achieved without compromising performance. The operating characteristics are specified under user program control. The controller can read, write, verify, and search either single or multiple sectors. Additional capability such as parallel or serial I/O or special math functions can be placed on the iSBC 208 board by utilizing the iSBX bus connection.



280228-1

September 1986
Order Number: 280228-001

FUNCTIONAL DESCRIPTION

Intel's 8272 Floppy Disk Controller (FDC) circuit is the heart of the iSBC 208 Controllller. On-board data separation logic performs standard MFM (double density) and FM (single density) encoding and decoding, eliminating the need for external separation circuitry at the drive. Data transfers between the controller and memory are managed by a DMA device which completely controls transfers over the MULTIBUS® system bus. A block diagram of the iSBC 208 Controller is shown in Figure 1.

Universal Drives and the iSBC® 208 Controller

Because the iSBC 208 Controller has universal drive compatibility, it can be used to control virtually any standard- or mini-sized diskette drive. Moreover, the iSBC 208 Controller fully supports the iSBX bus and can be used with any iSBX module compatible with this bus. Because the iSBC 208 Controller is programmable, its performance is not compromised by its universal drive compatibility. The track-to-track access, head-load, and head-unload characteristics of the selected drive model are program specified. Data may be organized in sectors up to 8192 bytes in length.

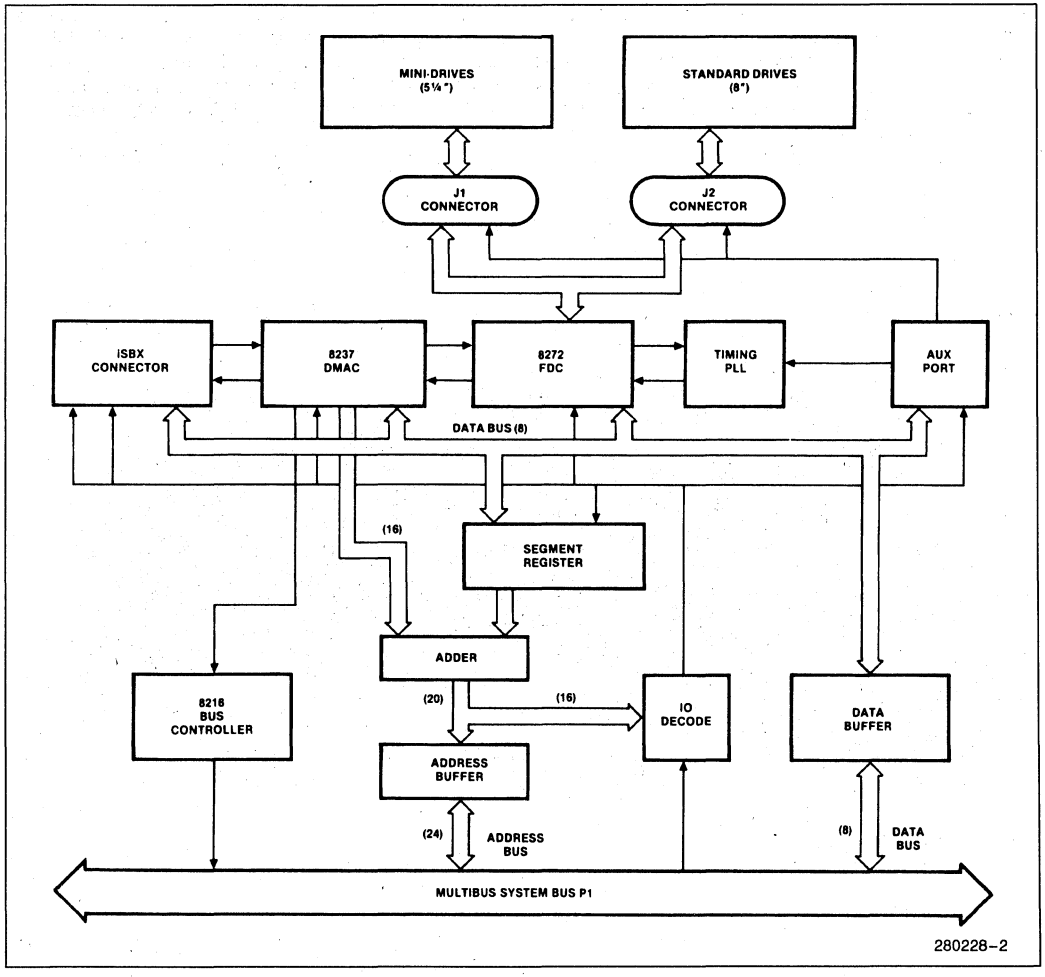


Figure 1. iSBC® 208 Flexible Disk Controller Block Diagram

Interface Characteristics

The standard iSBC 208 Controller includes an Intel 8272 Floppy Disk Controller chip which supports up to four drives, single or double sided.

SIMPLIFIED INTERFACE—The cables between the iSBC 208 Controller and the drive(s) may be low cost, flat ribbon cable with mass termination connectors. The mechanical interface to the board is a right-angle header with locking tabs for security of connection.

PROGRAMMING—The powerful 8272 FDC circuit is capable of executing high-level commands that simplify system software development. The device can read and write both single and multiple sectors. CRC characters are generated and checked automatically. Recording density is selected at each Read and Write to support the industry standard technique of recording basic media information on Track 0 of Side 0 in single density, and then switching to double density (if, necessary) for operations on other tracks.

Program Initiation—All diskette operations are initiated by standard input/output (I/O) port operations through an iSBC single board computer.

System software first initializes the controller with the operating characteristics of the selected drive. The diskette is then formatted under program control. For subsequent transfers, the starting memory address and transfer mode are specified for the DMA controller. Data transfers occur in response to commands output by the CPU.

Data Transfer—Once a diskette transfer operation has been initiated, the controller acts as a bus master and transfers data over the MULTIBUS at high speed. No CPU intervention is required until the transfer is complete as indicated either by the generation of an interrupt on the bus or by examination of a "done" bit by the CPU.

iSBX BUS SUPPORT—One connector is available on the iSBC 208 board which supports the iSBX system bus. This connector supports single-byte transfer as well as higher-speed transfers supervised by the DMA controller. Transfers may take place in polled or interrupt modes, user-selected. The presence of the iSBX bus allows many different functions to be added to the board. Serial I/O, parallel I/O and various special-purpose math functions are only a few of the capabilities available on iSBX MULTIMODULE boards.

SPECIFICATIONS

Compatibility

CPU — Any iSBC MULTIBUS computer or system main frame

Devices— Double or single density standard (8") and mini (5¼") flexible disk drives. The drives may be single or double sided. Drives known to be compatible are:

Standard (8")		Mini (5¼")	
Caldisk	143M	Shugart	450 SA 400
Remex	RFD 4000	Micropolis	1015-IV
Memorex	550	Pertec	250
MFE	700	Siemens	200-5
Siemens	FDD 200-8	Tandon	TM-100
Shugart	SA 850/800	CDC	9409
Pertec	FD 650	MPI	51/52/91/92
CDC	9406-3		

Diskette— Unformatted IBM Diskette 1 (or equivalent single-sided media); unformatted IBM Diskette 2D (or equivalent double-sided)

Equipment Supplied

iSBC 208 Controller
Reference Schematic
Controller-to-drive cabling and connectors are not supplied with the controller. Cables can be fabricated with flat cable and commercially-available connectors as described in the iSBC 208 Hardware Reference Manual

Physical Characteristics

Width: 6.75 inches (17.15 cm)
Height: 0.5 inches (1.27 cm)
Length: 12.0 inches (30.48 cm)
Shipping Weight: 1.75 pounds (0.80 Kg)
Mounting: Occupies one slot of iSBC system chassis or iSBC 604/614 Cardcage/Backplane. With an iSBX MULTIMODULE board mounted, vertical height increases to 1.13 inches (2.87 cm).

Electrical Characteristics

Power Requirements: +5 VDC @ 3.0A

Data Organization and Capacity

Standard Size Drives

	Double Density						Single Density					
	IBM System 34			Non-IBM			IBM System 3740			Non-IBM		
Bytes per Sector	256	512	1024	2048	4096	8192	128	256	512	1024	2048	4096
Sectors per Track	26	15	8	4	2	1	26	15	8	4	2	1
Tracks per Diskette	77			256			77			256		
Bytes per Diskette (Formatted, per diskette surface)	512,512 (256 bytes/sector) 591,360 (512 bytes/sector) 630,784 (1024 bytes/sector)			630,784			256,256 (128 byte/sector) 295,680 (256 bytes/sector) 315,392 (512 bytes/sector)			315,392		

Drive Characteristics

	Standard Size	Mini Size
	Double/Single Density	Double/Single Density
Transfer Rate (K bytes/s)	62.5/31.25	31.25/15.63
Disk Speed (RPM)	360	300
Step Rate Time (Programmable)	1 to 16 ms/track in 1 ms increments	2 to 32 ms/track in 2 ms increments
Head Load Time (Programmable)	2 to 254 ms in 2 ms increments	4 to 508 ms in 4 ms increments
Head Unload Time (Programmable)	16 to 240 ms in 16 ms increments	32 to 480 ms in 32 ms increments

Environmental Characteristics

Temperature: 0°C to 55°C (operating); −55°C to +85°C (non-operating)

Humidity: Up to 90% Relative Humidity without condensation (operating); all conditions without condensation or frost (non-operating)

Reference Manual

143078-001— iSBC 208 Flexible Disk Controller Hardware Reference Manual (NOT SUPPLIED).

Reference manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa, Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
SBC 208	Flexible Disk Controller

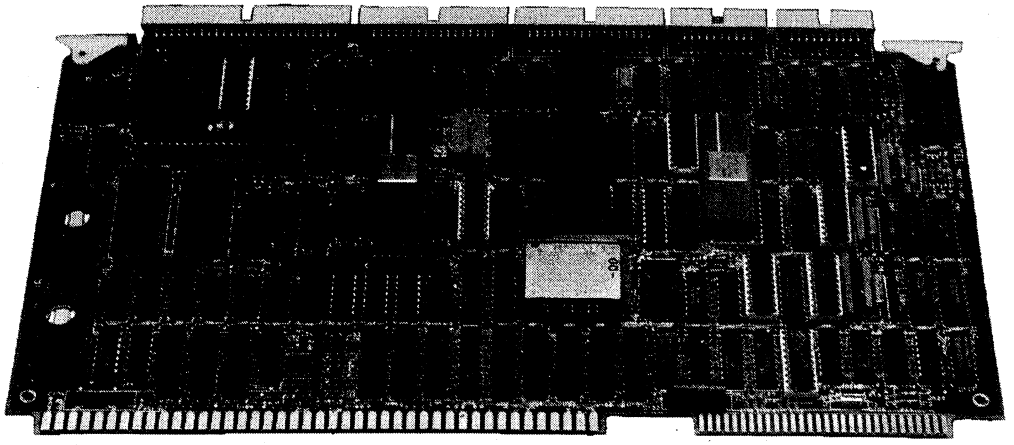
iSBC® 214
PERIPHERAL CONTROLLER SUBSYSTEM

- **Based on the 80186 Microprocessor**
- **Controls up to Two ST506/412 5¼" Winchester Disk Drives**
- **Controls up to Four Single/Double Sided and Single/Double Density 5¼" Flexible Disk Drives**
- **Controls up to Four QIC-02 Streaming Tape Drives**
- **Supports 20 or 24-Bit Addressing**
- **On-Board Diagnostics and Winchester ECC**
- **Incorporates Track Caching to Reduce Winchester Disk Access Times**
- **iRMX™ and XENIX* Operating System Support**

The iSBC 214 Subsystem is a single-board, multiple device controller that interfaces standard MULTIBUS® systems of three types of magnetic storage media. The iSBC 214 Peripheral Controller Subsystem supports the following interface standards: ST506/412 (Winchester Disk), SA 450/460 (Flexible Disk), and QIC-02 (¼" Streaming Tape).

The board combines the functionality of the iSBC 215 Generic Winchester Controller and the iSBC 213 Data Separator, the iSBX™ 218A Flexible Disk Controller, and the iSBX 217C ¼" Tape Drive Interface Module. The iSBC 214 Subsystem emulates the iSBC 215G command set, allowing users to avoid rewriting their software.

The iSBC 214 Peripheral Controller Subsystem offers a single slot solution to the interface of multiple storage devices, thereby reducing overall power requirements, increasing system reliability, and freeing up backplane slots for addtional functionality. In addition, the new iSBC 214 Subsystem can be placed in a 16 Megabyte memory space.



280089-1

*XENIX is a trademark of MICROSOFT Corp.

September 1986
Order Number: 280089-001

The iSBC 214 represents a new Peripheral Controller Subsystem architecture which is designed around a dual bus structure and supported by real-time, multitasking firmware. The 80186 controls the local bus and manages the interface between the MULTIBUS and the controller. It is responsible for high speed data transfers of up to 1.6 megabytes per second between the iSBC 214 Subsystem and host memory. The 80186 and the multitasking firmware decode the command request, allocate RAM buffer space, and dispatch the tasks.

A second bus, the I/O Transfer Bus, supports data transfers between the controller and the various peripheral devices. It is this dual bus system that allows the iSBC 214 Subsystem to provide simultaneous data transfers between the controller and the storage devices, and between the controller and the MULTIBUS. (See Figure 1).

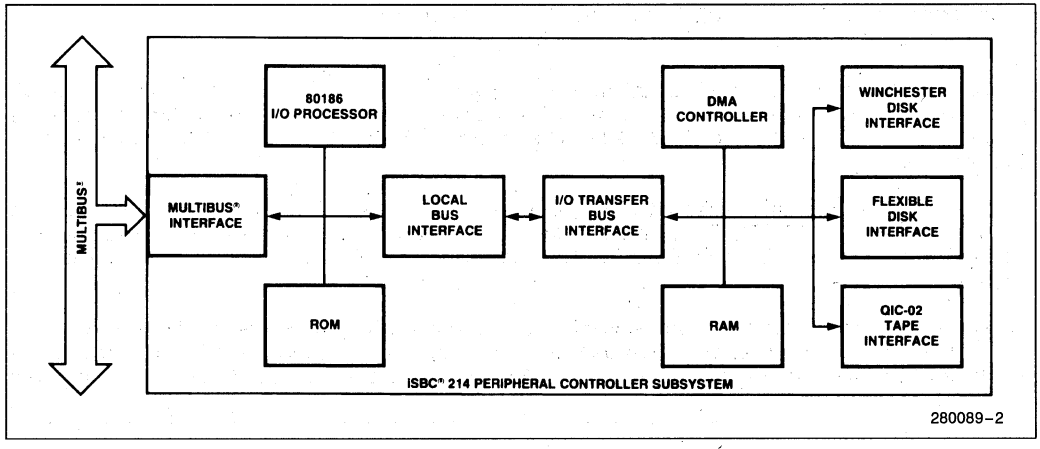


Figure 1. Block Diagram iSBC® 214 Peripheral Controller Subsystem

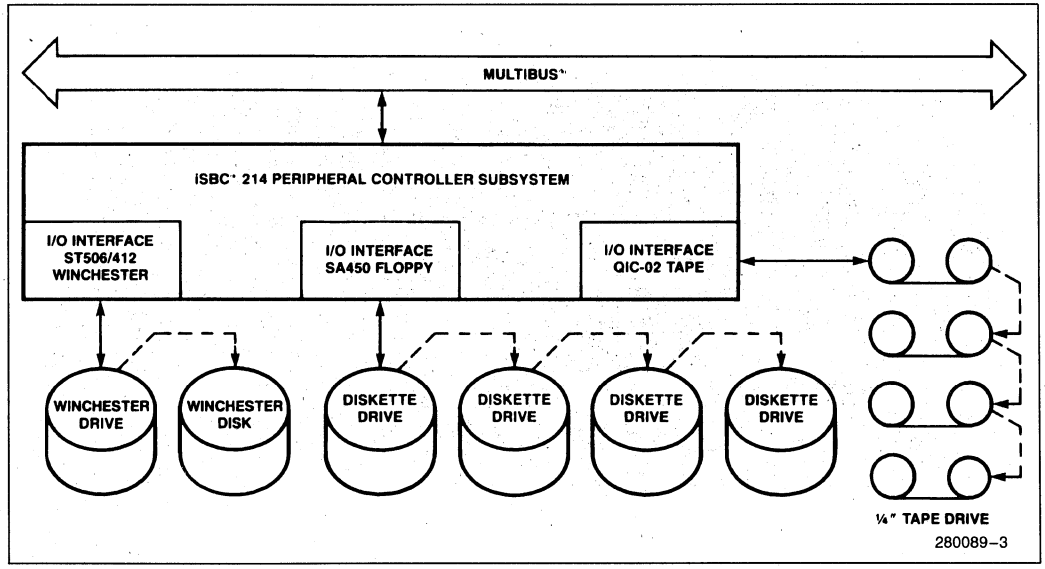


Figure 2. Fully Configured Peripheral Subsystem

The iSBC 214 Subsystem implements an intelligent track caching scheme through dynamic allocation of buffer space. This provides reduced access times to the Winchester disk and improved system performance. Operating systems with file management designed to handle sequential data can be supplied directly from the cache without incremental access to the disk.

FUNCTIONAL DESCRIPTION

Winchester Disk Interface

The iSBC 214 Subsystem provides control of one or two ST506/412 compatible Winchester devices and supports up to 16 Read/Write heads per drive. The Intel 82062 acts as the main controller taking care of FM/MFM encoding and decoding, bit stream serialization and deserialization, address mark detection and generation, sector identification comparisons, CRC error checking and format generation. The board uses a standard daisy-chained control cable and a separate data transfer cable for each device supported.

ECC

High data integrity is provided by on-board Error Checking Code logic. For burst error correction, a 32-bit code is appended to the sector data fields by the controller. During a read operation, the same logic regenerates the ECC polynomial and compares this second code to the appended ECC. The ECC logic can detect an erroneous data burst up to 32 bits in length with correction up to 11 bits.

If an ECC error is detected the controller automatically initiates a retry operation on the data transfer. If the maximum retry count is exceeded, the location of the bad data within the transfer buffer is identified and the 80186 then performs error correction on the data bytes.

Flexible Disk Interface

The Flexible Disk Controller performs all data separation, FM (single density) and MFM (double density) encoding, and CRC support. The 34-pin connector is designed to support the SA450/460 interface directly and up to four flexible disk devices may be connected to the controller.

Tape Controller Interface

The tape controller section of the iSBC 214 Subsystem is based on the 8742 Universal Peripheral Interface (UPI). It is capable of supporting up to four QIC-02 compatible streaming tape drives over a standard 50-pin daisy-chained cable.

All standard QIC-02 commands are supported. All drives must be capable of streaming at 30 or 90 inches per second.

MULTIBUS® Host Interface

The MULTIBUS connection consists of two standard printed circuit board edges that plug into MULTIBUS edge connectors on a backplane in the system bus. An active P1 connector is required and serves as the Host systems's communciation channel to the controller. An active P2 connector is optional and only required for supporting full 24-bit addressing and power fail signals.

SPECIFICATIONS

Compatibility

CPU—any iSBC MULTIBUS computer or system mainframe.

Winchester disk—Any ST506/412 compatible, 5.25″ disk drive.

Flexible disk—Any SA450/460 compatible, 5.25″ disk drive.

Tape drive—Any QIC-02 compatible, .25″ streaming tape drive.

Controller-to-drive cabling and connectors are not supplied with the controller. Cables can be fabricated with flat cable and commercially-available connectors as described in the iSBC 214 Hardware Reference Manual.

Physical Characteristics

Width: 6.75 in. (17.15 cm)
Height: 0.5 in. (1.27 cm)
Length: 12.0 in. (30.48 cm)
Shipping Weight: 19 oz. (540 g)

Ordering Information

iSBC 214 Peripheral Controller Subsystem.

Mounting: Occupies one slot or SBC system chassis or cardcage/backplane.

Electrical Characteristics

Power Requirements: +5 VDC @ 4.5A max.

Environmental Characteristics

Temperature: 10°C to 55°C with airflow of 200 linear feet per minute (operating); −55°C to +85°C (non-operating).

Humidity: Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating).

Reference Manual

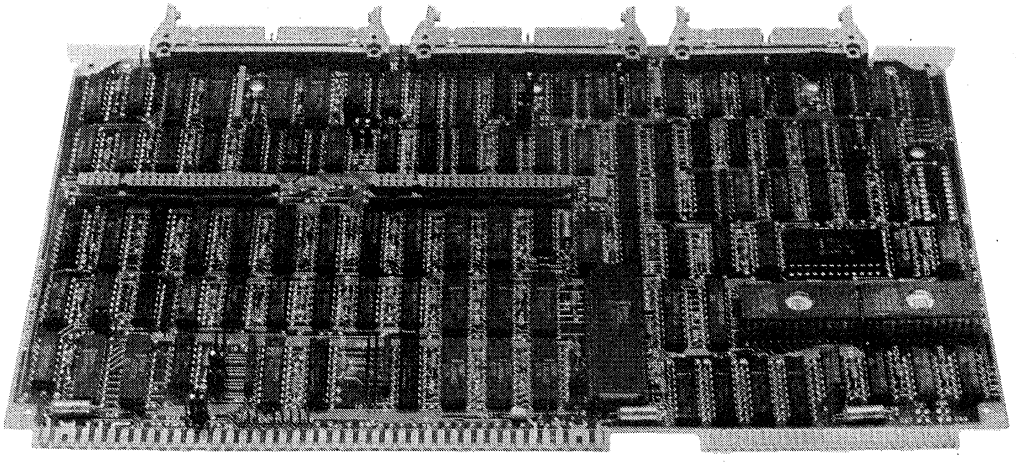
134910-001: iSBC 214 Peripheral Controller Subsystem Hardware Reference Manual (not supplied). Reference Manual may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

iSBC® 215
GENERIC WINCHESTER CONTROLLER

- **Controls up to Four 5¼", 8" or 14" Winchester Disk Drives from Over Ten Different Vendors**
- **Compatible with Industry Standard MULTIBUS® (IEEE 796) Interface**
- **Supports ANSI X3T9/1226 Standard Interface**
- **Software Drivers Available for iRMX™ 86, iRMX 88 and Xenix* Operating Systems**
- **Intel 8089 I/O Processor Provides Intelligent DMA Capability**
- **On-Board Diagnostics and ECC**
- **Full Sector Buffering On-Board**
- **Capable of Directly Addressing 16 MB of System Memory**
- **Removable Back-up Storage Available Through the iSBX™ 218A Flexible Disk Controller and the iSBX 217C ¼" Tape Interface Module**

Using VLSI technology, the iSBC 215 Generic Winchester Controller (GWC) combines three popular Winchester controllers onto one MULTIBUS board: the iSBC 215A open loop controller, the iSBC 215B closed loop controller, and an ANSI X3T9/1226 standard interface controller. The combined functionality of the iSBC 215 Generic Controller supports up to four 5¼", 8" or 14" Winchester drives from over 10 different drive vendors. Integrated back-up is available via two iSBX MULTIMODULE boards; the iSBX 218A module for floppy disk drives and the iSBX 217C module for ¼" tape units.

From the MULTIBUS side, the iSBC 215 GWC appears as one standard software interface, regardless of the drive type used. In short, the iSBC 215 GWC allows its user to change drive types without rewriting software. The iSBC 215 Generic Controller is totally downward compatible with its predecessors, the iSBC 215A and 215B controller; allowing existing iSBC 215A and 215B users to move quickly to the more powerful iSBC 215 Generic Winchester Controller. In addition, the iSBC 215 GWC directly addresses up to 16 megabytes of system memory.



210618-1

Xenix is a trademark of Microsoft Corp.

October 1986
Order Number: 210618-002

FUNCTIONAL DESCRIPTION

Disk Interface

The iSBC 215 Generic Winchester Controller can interface to over 10 different disk drives. To change drive types the user need only reconfigure a minimal number of board jumpers and, if required, insert the proper formatting information into the command parameter blocks.

The ANSI X3T9/1226 standard interface is a simple one-for-one flat cable connection from drive to controller.

Full On-Board Buffer

The iSBC 215 Generic controller contains enough on-board RAM for buffering one full data sector. The controller is designed to make use of this buffer in all transfers. The on-board sector buffer prevents data overrun errors and allows the iSBC 215 Generic Winchester Controller to occupy any priority slot on the MULTIBUS.

ECC

High data integrity is provided by on-board Error Checking Code (ECC) logic. When writing sector ID or data fields, a 32-bit ECC, for burst error correction, is appended to the field by the controller. During a read operation, the same logic regenerates the ECC polynomial to the appended ECC. The ECC logic can detect an erroneous data burst up to 32 bits in length and using an 8089 algorithm can correct an erroneous burst up to 11 bits in length.

iSBX™ Interface

Two iSBX bus connectors provide I/O expansion capability for the iSBC 215 GWC. With the optional addition of the iSBX 218A Flexible Disk Controller MULTIMODULE™ and or the iSBC 217C ¼" Tape Interface Module, the iSBC 215 GWC can be configured into one of four types of peripheral subsystems, see Table 1.

Table 1. Peripheral Subsystem Configurations

	iSBC® 215	iSBX™ 218A	iSBX™ 217C
Winchester Only	✓		
Winchester + Floppy	✓	✓	
Winchester + ¼" Tape	✓		✓
Winchester + Floppy + ¼" Tape	✓	✓	✓

Expanded I/O Capability

The iSBC 215 GWC controller allows the execution of user-written 8089 programs located in on-board or MULTIBUS system RAM. Thus the full capability of the 8089 I/O processor can be utilized for custom I/O requirements.

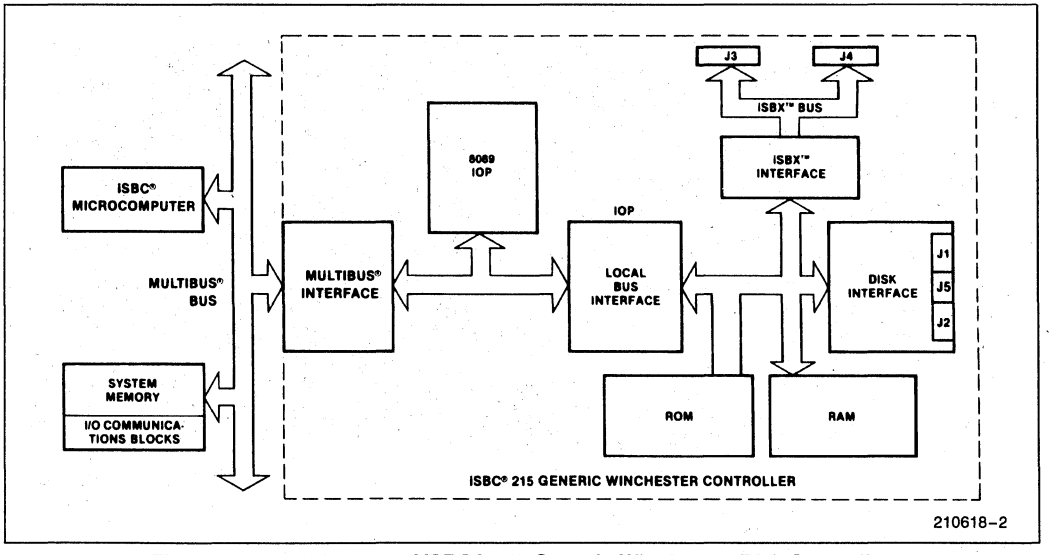
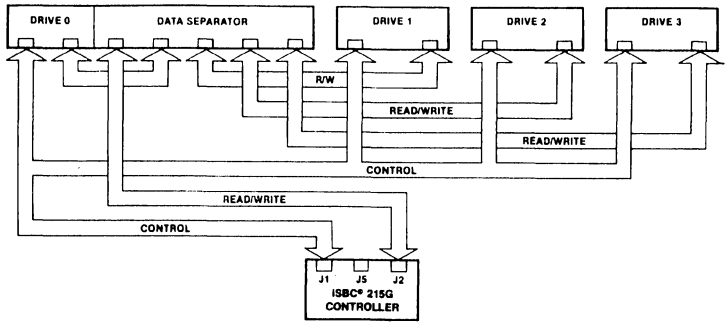


Figure 1. Block Diagram of iSBC® 215 Generic Winchester Disk Controller

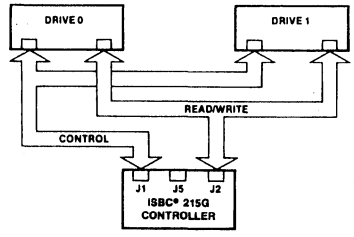
Interface with Shugart/Quantum/RMS Drives



210618-3

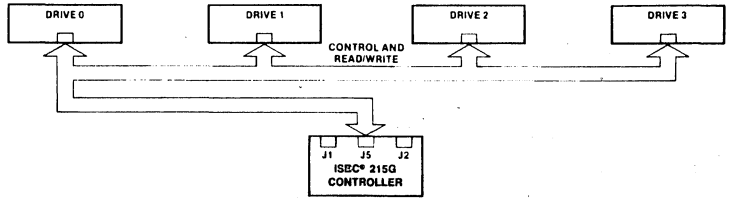
NOTE:
1. Shugart SA1000 or RMS Data Express.* *Data Express is a trademark of Rotating Memory Systems.

Interface with Memorex/Shugart Drives



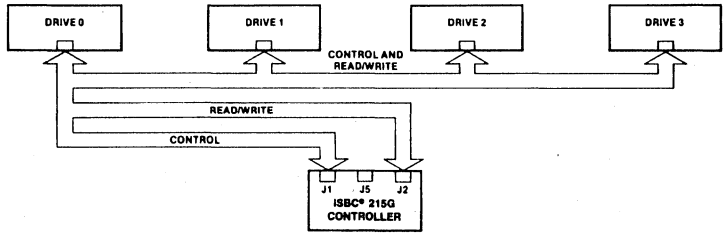
210618-4

Interface with ANSI Drive



210618-5

Interface with PRIAM Drives



210618-6

Figure 2. Controller to Drive Interfacing

MULTIBUS® Interface

The iSBC 215 Generic Controller interfaces to the system CPU(s) through MULTIBUS memory. The iSBC 215 Generic controller directly addresses 16 megabytes of system memory. Commands are passed to and from the iSBC 215 GWC via memory based parameter blocks. These parameter blocks are executed directly by the iSBC 215 GWC thus off-loading the system CPU(s). Data transfers to and from the iSBC 215 GWC are done via the high speed DMA capability of the Intel 8089 I/O processor.

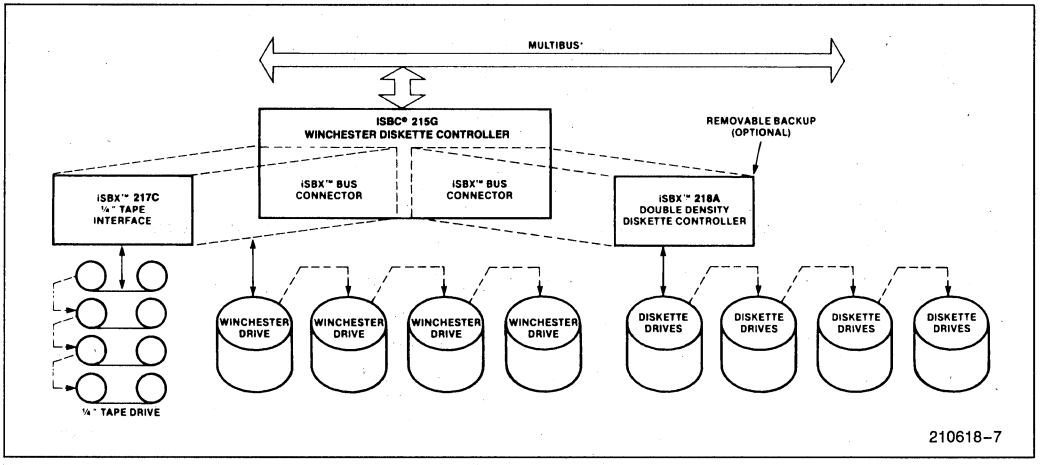


Figure 3. Subsystem Configuration (with Optional Diskette Backup)

SPECIFICATIONS

Compatibility

CPU—Any iSBC MULTIBUS computer or system mainframe.

Disk Drives—Winchester Disk Drives; both open-loop and closed-loop head positioner types. The following drives are known to be compatible:

Open-Loop
Shugart SA 1000 Series
Shugart SA 4000 Series
Memorex 100 Series
Quantum Q2000 Series
Fujitsu 2301, 2302
CDC 9410
RMS 5¼" Series
Rodine 5¼" Series
Ampex 5¼" Series
CMI 5¼" Series
Closed-Loop
Priam 8" and 14" Drive Series
ANSI
3M 8430 Series
Kennedy 6170 Series
Micropolis 8" Series
Pertec Trackstar Series
Priam 8" Series
Megavault (SLI) 8" Series
iSBX™ MULTIMODULE™ Boards
iSBX™ 218A Flexible Disk Controller
iSBX™ 217C ¼" Tape Interface

Equipment Supplied

iSBC 215 Generic Winchester Controller
Reference Schematic

Controller-to-drive cabling and connectors are not supplied with the controller. Cables can be fabricated with flat cable and commercially-available connectors as described in the iSBC 215G Hardware Reference Manual.

Physical Characteristics

Width:	6.75 in. (17.15 cm)
Height:	0.5 in. (1.27 cm)
Length:	12.0 in. (30.48 cm)
Shipping Weight:	19 oz. (0.54 kg)
Mounting:	Occupies one slot of iSBC system chassis or cardcage/backplane

With an iSBX MULTIMODULE board mounted, vertical height increases to 1.13 in. (2.87 cm).

Electrical Characteristics

Power Requirements

+5 VDC@4.52A max
−5 VDC@0.015A max[1]
+12 VDC@0.15A max[2]
−12 VDC@0.055A max[1,2]

NOTES:
1. On-board regulator and jumper allows −12 VDC usage from MULTIBUS.
2. Required for some iSBX MULTIMODULE boards.

Data Organization

Bytes/Sector	Sectors/Track(1) 128	256	512	1024
Priam 8″	72	42	23	12
Priam 14″	107	63	35	18
RMS/Shugart 8″ /Quantum/Ampes/Rodine/CM1	54	31	17	9
Fujitsu/Memorex	64	38	21	11
Shugart 14″	96	57	31	16
CDC Finch	64	41	23	12
3M (ANSI)	82	51	29	16
Megavault (ANSI)	73	43	21	12
Kennedy (ANSI)	74	43	23	12
Micropolis (ANSI)	71	44	25	13
Pertec (ANSI)	85	52	29	15

NOTE:
1. Maximum allowable for corresponding selection of bytes per sector.

Drives per Controller

5¼″ Winchester Disk Drives—Up to four RMS, CMI, Rodine or Ampex drives.

8″ Winchester Disk Drives—Up to four ANSI, Shugart, Quantum or Priam drives; up to two Memorex, CDC, or Fujitsu drives.

14″ Winchester Disk Drives—Up to four Priam drivers; up to two Shugart drives.

Flexible Disk Drives—Up to four drives through the optional iSBX 218A Flexible Disk Controller connected to the iSBC 215 GWC board's iSBX connector.

¼″ Tape Drives—Up to four drives through the optional iSBX 217C ¼″ Tape Interface Module connected to the iSBC 215 GWC board's iSBX connector.

Environmental Characteristics

Temperature—0° to 55°C (operating); −55°C to +85°C (non-operating)

Humidity—Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating).

Reference Manual

144780—iSBC 215 Generic Winchester Controller Hardware Reference Manual (NOT SUPPLIED)

Reference manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

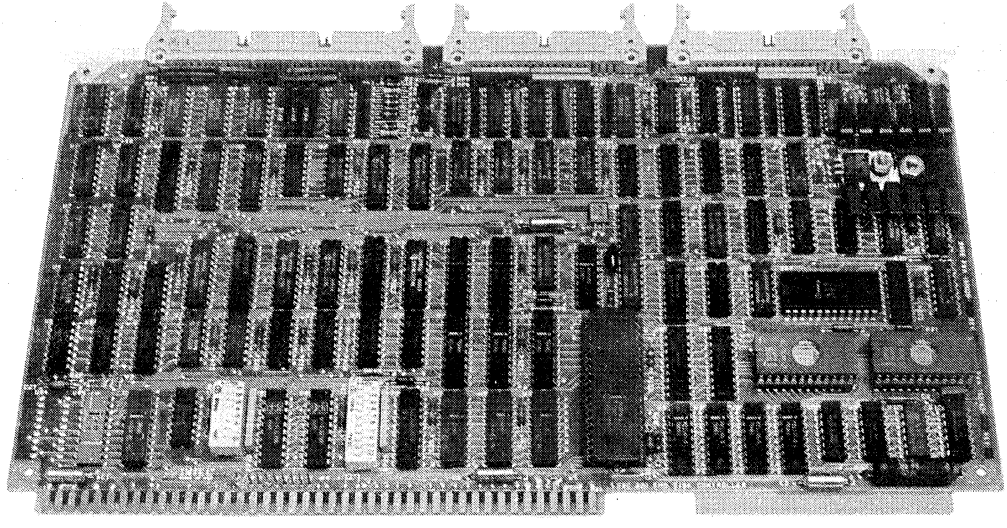
Part Number	Description
SBC 215G	Generic Winchester Controller

iSBC® 220
SMD DISK CONTROLLER

- **Controls up to Four Soft Sectored SMD Interface Compatible Disk Drives**
- **12 MB to 2.4 GB per Controller**
- **Compatible with all iSBC® 80, iSBC® 88, and iSBC® 86 Single Board Computers**
- **Intel 8089 I/O Processor Provides Two High Speed DMA Channels as well as Controller Intelligence**
- **Software Drivers Available for iRMX™ 286 and XENIX* Operating Systems**
- **On-Board Diagnostic and ECC**
- **Full Sector Buffering On-Board**
- **Capable of Addressing 1 MB of System Memory**
- **SMD Interface Available on Winchester, CMD, SMD and Large Fixed-Media Drives**

The iSBC 220 SMD Disk Controller brings very large mass storage capabilities to any iSBC 80, iSBC 88, or iSBC 86 MULTIBUS® system. The controller will interface to any soft sectored disk drive conforming to the industry standard SMD interface. Using simplified cable connections, up to four drives may be connected to the iSBC 220 Controller Board to give a total maximum capacity of 2.4 gigabytes. The Intel 8089 I/O Processor simplifies programming through the use of memory-based parameter blocks. A linked list technique allows the user to perform multiple disk operations.

*XENIX is a registered trademark of Microsoft.



143283-1

November 1986
Order Number: 143283-002

FUNCTIONAL DESCRIPTION

Full On-Board Buffer

The iSBC 220 SMD Controller contains enough on-board RAM for one full sector buffering. The controller is designed to make use of this buffer in all transfers. The on-board sector buffer prevents data overrun errors and allows the iSBC 220 SMD Controller to occupy any priority slot on the MULTIBUS.

ECC

High data integrity is provided by on-board Error Checking Code (ECC) logic. When writing sector ID or data fields, a 32-bit Fire code, for burst error correction, is appended to the field by the controller. During a Read operation, the same logic regenerates the ECC polynomial and compares this second polynomial to the appended ECC. The ECC logic can detect an erroneous data burst up to 32 bits in length and using an 8089 alrogithm can correct an erroneous burst up to 11 bits in length.

SMD Interface

High speed, reliable data transfers are a major benefit of suing the SMD interface. A data transfer rate of 1.2 MB is accomplished by using separate (radial) differential data line cabling for each drive. Control signals are daisy-chained from drive to drive.

Defective Track Handling

When a track is deemed defective, the host processor reformats the track, giving it a defective track code and enters the address of the next available alternate track. When the controller accesses a track previously marked defective, the controller automatically seeks to the assigned alternate track. The alternate track seek is totally automatic and invisible to the user.

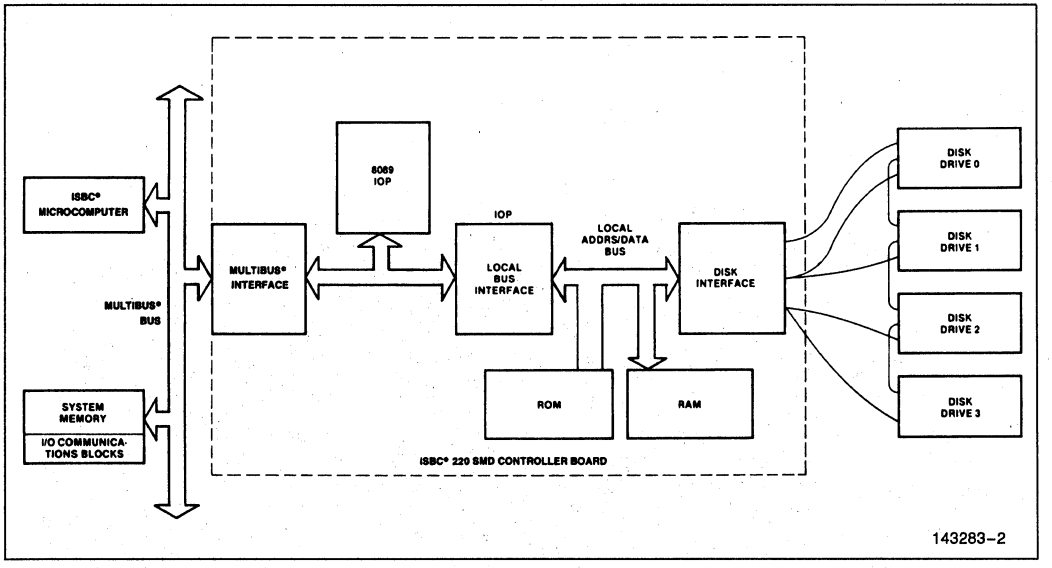


Figure 1. Simplified Block Diagram of iSBC® 220 SMD Disk Controller

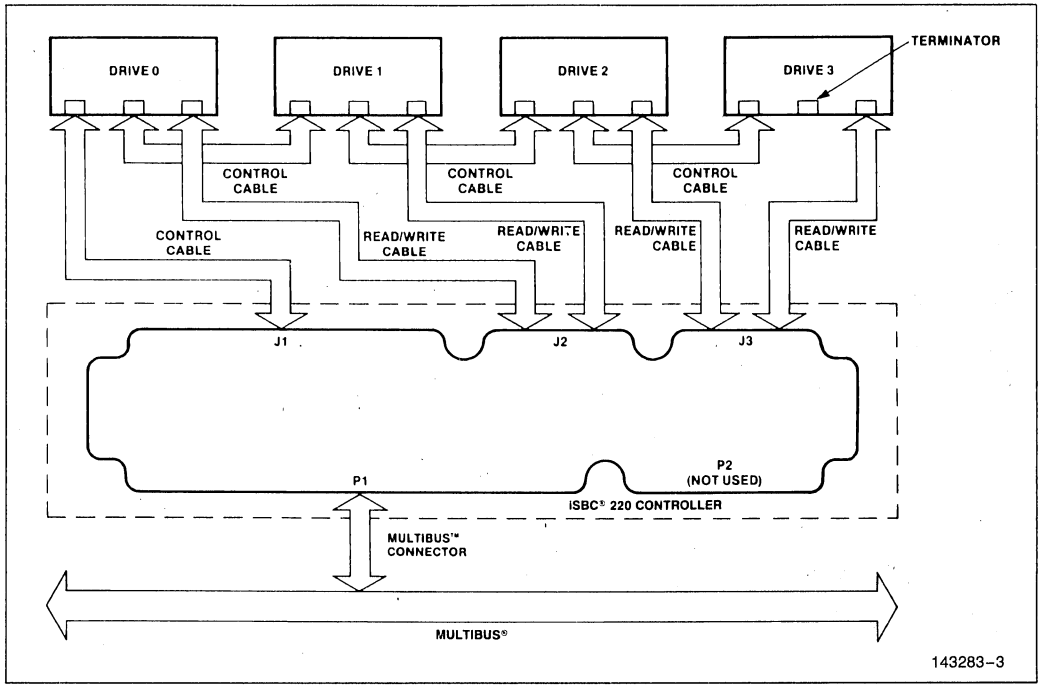


Figure 2. Typical Multiple Drive System

SPECIFICATIONS

Compatibility

CPU: Any iSBC MULTIBUS computer on system mainframe

Disk Drive: Any soft sectored SMD interface-compatible disk drive

Equipment Supplied

iSBC 220 SMD Disk Controller
Reference schematic

Controller-to-drive cabling and connectors are not supplied with the controller. Cables can be fabricated with flat cable and commercially-available connectors as described in the iSBC 220 SMD Disk Controller Hardware Reference Manual.

Physical Characteristics

Width: 6.75 in (17.15 cm)
Height: 0.5 in (1.27 cm)
Length: 12.0 in. (30.48 cm)
Shipping Weight: 19 oz. (0.54 kg)
Mounting: Occupies one slot of iSBC system chassis or cardcage/backplane

Electrical Characteristics

Power Requirements:
+5 VCD @ 3.25A max
−5 VDC @ 0.75A max(1)

NOTE:
1. On-board voltage regulator allows optional −12 VDC usage from MULTIBUS.

Data Organization and Capacity

Bytes per Sector(2): 128 256 521 1024
Sector per Track(2): 108 64 35 18

NOTE:
2. Software selectable.

Table 1. Drive Characteristics (Typical)

Disk (spindle) Speed	3600 rpm	
Tracks per Surface	823	
Head Positioning	Closed loop servo type, track following	
Access Time	Track to Track	6 ms
	Average	30 ms
	Maximum	55 ms
Data Transfer Rate	1.2 megabytes/second	
Storage Capacity	12 to 2.4 gigabytes	

Environmental Characteristics

Temperature: 0°C to 55°C (operating); −55°C to +85°C (non-operating)

Humidity: Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating)

Reference Manual

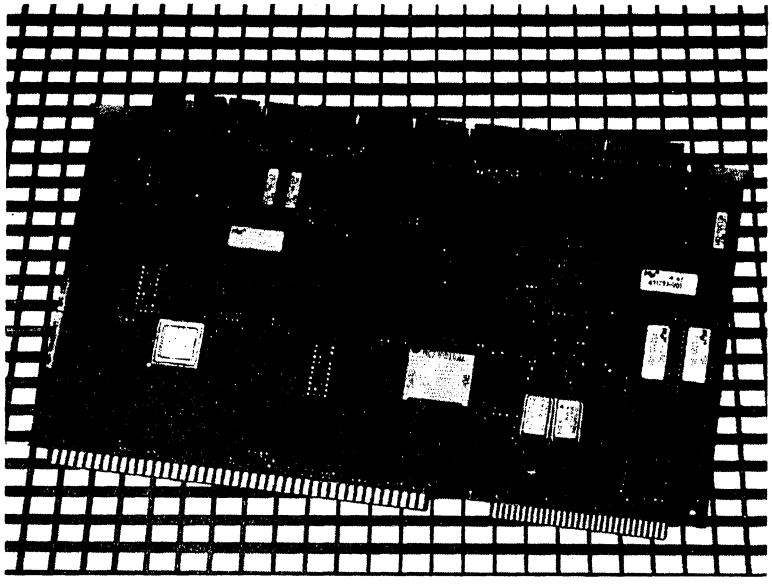
121597-001—iSBC 220 SMD Disk Controller Hardware Reference Manual (NOT SUPPLIED)

Reference manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
SBC 220	SMD Disk Controller

iSBC™ 221 PERIPHERAL CONTROLLER



MULTIBUS® I CONTROLLER FOR HIGH-PERFORMANCE, HIGH CAPACITY PERIPHERALS

The iSBC 221 is a multifunction peripheral controller that provides access to high-performance, high-capacity disk drives (hard, flexible, and streaming tape). I/O bound applications and/or those requiring high disk capacity will especially benefit from this fast, reliable controller. The iSBC 221 can replace the Intel iSBC 214 without changing the operating system device driver, or the disk drives.

FEATURES:

- Support for ESDI and ST506/412 hard disk drives, SA 45X/46X/475 flexible disk drives, and QIC-02 streaming tape drives
- Multiple track caching via 128K on-board data buffer
- Dual bus structure
- 10 MHz 80186 Microprocessor
- Mirror backup/restore between tape and hard drive
- On-board self-test diagnostics
- Error-checking and correcting code logic
- Support for 4,096 cylinders and 16 heads

February, 1988
Order Number: 280410-002

FEATURES

INTERFACE SUPPORT

	Interface	Transfer Rate
Hard Disk (up to 2)	EDSI	up to 10 Mbit/sec
	ST506/412	5 Mbit/sec
Flexible Disk (up to 4)	SA 475	250/500 Kbit/sec
	SA 460/465	125/250 Kbit/sec
	SA 450/455	125/250 Kbit/sec
Streaming Tape (up to 4)	QIC-02	90/112.5 Kbit/sec (typical)

HIGH PERFORMANCE

I/O-bound applications are accelerated by the combination of the ESDI standard, a 128K data buffer, a 10 MHz 80186 microprocessor, and a dual bus structure. The dual bus structure allows the iSBC 221 to concurrently transfer data between the controller and the peripheral devices, and between the controller and the host.

WORLDWIDE SERVICE AND SUPPORT

Intel provides support for board repair or on-site service. Development support options include phone support, subscription service, on-site consulting, and customer training.

QUALITY AND RELIABILITY TESTING

The iSBC 221 is designed and manufactured in accordance with Intel's high quality standards. We then verify quality through rigorous testing in our state-of-the-art Environmental Test Laboratory.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS

Length: 12.0 in. (304.8 mm)
Width: 6.75 in. (171.5 mm)
Approximate Weight: 24 oz (680 g)

POWER REQUIREMENTS

+5 VDC @ 4.5A maximum
±12V @ 0.5A

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0 to 55°C @ 200 LFM
Non-operating: −55 to 85°C
Humidity: 0 to 90% non-condensing

REFERENCE MANUAL

iSBC 221 Peripheral Controller User's Guide
Order #451210

DEVICE DRIVERS

Check the latest release of the following operating systems for details:

iRMX 86 XENIX*
iRMX II UNIX*

*XENIX is a trademark of Microsoft, Inc.
UNIX is a trademark of American Telephone and Telegraph, Inc.

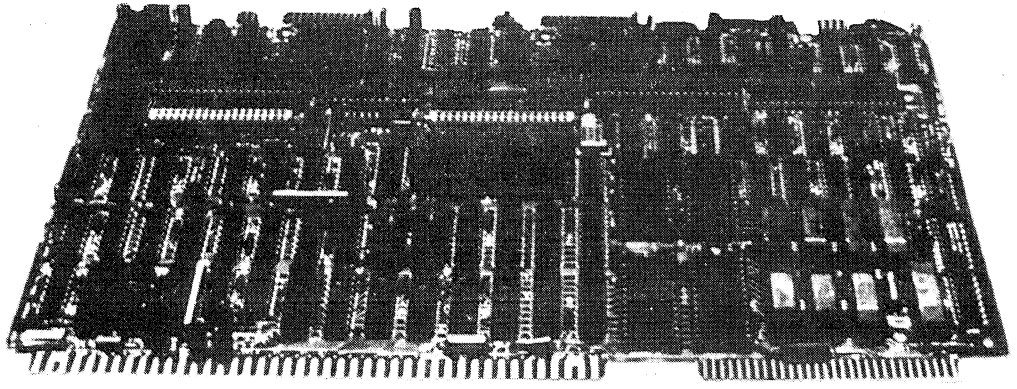
MULTIBUS® I
Serial Communication Boards

6

iSBC® 88/45
ADVANCED DATA COMMUNICATIONS PROCESSOR BOARD

- **Three HDLC/SDLC Half/Full-Duplex Communication Channels—Optional ASYNC/SYNC on Two Channels**
- **Supports RS232C (Including Modem Support), CCITT V.24, or RS422A/449 Interfaces**
- **On-Board DMA Supports 800K Baud Operation**
- **Self-Clocking NRZI SDLC Loop Data Link Interface**
  - **— Point-to-Point**
  - **— Multidrop**
- **Software Programmable Baud Rate Generation**
- **8088 (8088-2) Microprocessor Operates at 8 MHz**
- **iSBC® 337 Numeric Data Processor Option Supported**
- **16K Bytes Static RAM (12K Bytes Dual-Ported)**
- **Four 28-Pin JEDEC Sites for EPROM/RAM Expansion; Four Additional 28-Pin JEDEC Sites Added with iSBC® 341 Board**
- **Two iSBX™ Bus Connectors**
- **MULTIBUS® Interface Supports Multimaster Configuration**

The iSBC 88/45 Advanced Data Communications Processor (ADCP) Board adds 8 MHz, 8088 (8088-2) 8-bit microprocessor-based communications flexibility to the Intel line of OEM microcomputer systems. The iSBC 88/45 ADCP board offers asynchronous, synchronous, SDLC, and HDLC serial interfaces for gateway networking or general purpose solutions. The iSBC 88/45 ADCP board provides the CPU, system clock, EPROM/RAM, serial I/O ports, priority interrupt logic, and programmable timers to facilitate higher-level application solutions.



210372-1

September 1987
Order Number: 210372-002

FUNCTIONAL DESCRIPTION

Three Communication Channels

Three programmable HDLC/SDLC serial interfaces are provided on the iSBC 88/45 ADCP board. The SDLC interface is familiar to IBM system and terminal equipment users. The HDLC interface is known by users of CCITT's X.25 packet switching interface.

One channel utilizes an Intel 8273 controller to manage the serial data transfers. Accepting the 8-bit data bytes from the local bus, the 8273 controller translates the data into the HDLC/SDLC format. The channel operates in half/full-duplex mode.

In addition to the synchronous mode, the 8273 controller operates asynchronously with NRZI encoded data which is found in systems such as the IBM 3650 Retail Store System. An SDLC loop configuration using iSBX 352 and iSBC 88/45 products is shown in Figure 1.

The two additional channels utilize the Intel 8274 Multi-Protocol Serial Controller (MPSC). The MPSC provides two independent half/full-duplex serial channels which provide asynchronous, synchronous, HDLC or SDLC protocol operations. The sync and async protocol operations are commonly used to communicate with inexpensive terminals and systems.

The three serial channels of the iSBC 88/45 ADCP board offer communications capability to manage a gateway application. The gateway application, as shown in Figure 1, manages diverse protocol requirements for data movement between channels. Typical protocol management software layers implemented by the user include SNA terminal interfaces to IBM systems.

On-Board DMA

For high-speed communications, one MPSC channel has a DMA capacity to support an 800K baud rate. The second channel attached to the MPSC is capable of simultaneous 800K baud operation when configured with DMA capability, but is connected to an RS232C interface which is defined as 20K baud maximum. Figure 2 shows an RS422A/449 multidrop application which supports high-speed operation.

Interfaces Supported

The iSBC 88/45 ADCP board provides an excellent foundation to support these electrical and diverse software drivers protocol interfaces. The control lines, serial data lines, and signal ground lines are brought out to the three double-edge connectors. Figure 3 shows the cable to connector construction. Two connectors are pre-configured for RS422A/449. All three channels are configurable for RS232C/CCITT V.24 interfaces as shown in Table 1.

Table 1. iSBC® 88/45 Supported Configurations

Connection	Synchronous		Asynchronous	
	Modem	Direct	Modem*	Direct
Point-to-Point	X**	X	X	X
Multidrop	X	X	X	X
Loop	N.A.	N.A.	C (Only)	C (Only)

*Modem should not respond to break.
**Channels A, B, and C denoted by X.

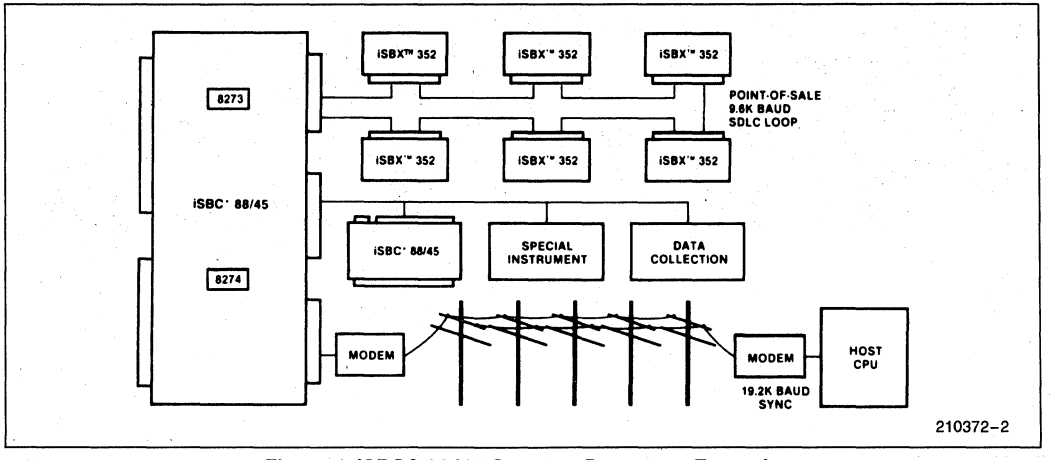
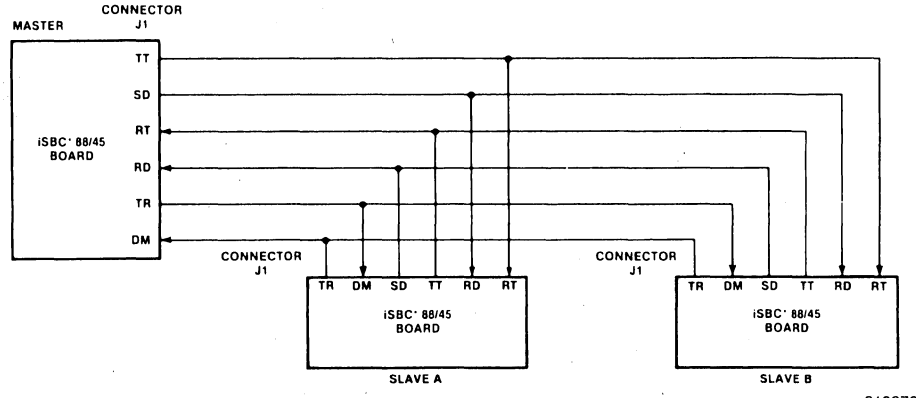


Figure 1. iSBC® 88/45 Gateway Processor Example



NOTE:
The last slave device in the system must contain termination resistors on all signal lines received by the slave board. The master device contains bias resistors on all signal lines.

Figure 2. Synchronous Multidrop Network Configuration Example—RS422A

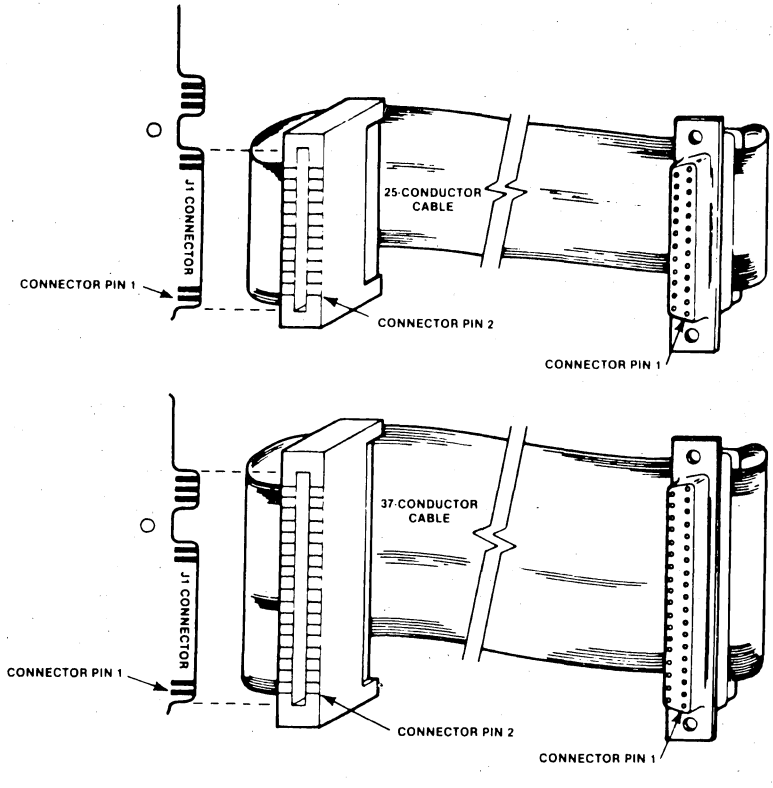


Figure 3. Cable Construction and Installation for RS232C and RS422A/449 Interface

Self Clocking Point-to-Point Interface

The iSBC 88/45 ADCP board is used in an asynchronous mode interface when configured as shown in Figure 4. The point-to-point RS232C example uses the self-clocking mode interface for NRZI encoding/decoding of data. The digital phase-lock loop allows operation of the interface in either half-duplex or full/duplex implementation with or without modems.

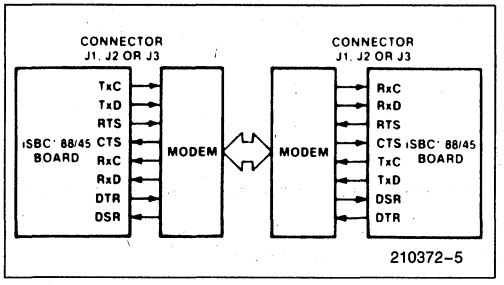


Figure 4. Self-Clocking or Asynchronous Point-to-Point Modem Interface Configuration Example—RS232C

Synchronous Point-to-Point Interface

Figure 5 shows a synchronous point-to-point mode of operation for the iSBC 88/45 ADCP board. This RS232C example uses a modem to generate the receive clock for coordination of the data transfer. The iSBC 88/45 ADCP board generates the transmit synchronizing clock for synchronous transmission.

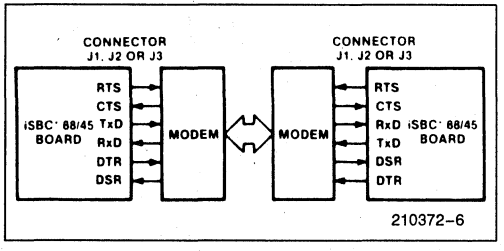


Figure 5. Synchronous Point-to-Point Modem Interface Configuration Example—RS232C

Central Processing Unit

The central processor for the iSBC 88/45 Advanced Data Communications Processor board is Intel's iAPX 8088 microprocessor operating at 8 MHz. The microprocessor interface to other functions is illustrated in Figure 6. The microprocessor architecture is designed to effectively execute the application and networking software written in higher-level languages.

This architectural support includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers and two 16-bit index registers. These registers are addressable through 24 different operand addressing modes for comprehensive memory addressing and for high-level language data structure manipulation.

The stack-oriented architecture readily supports Intel's iRMX executives and iMMX multiprocessing software. Both software packages are designed for modular application programming. Facilitating the fast inter-module communications, the 4-byte instruction queue supports program constructs needed for real-time systems.

Since programs are segmented between pure procedure and data, four segment registers (code, stack, data, extra) are available for addressing 1 megabyte of memory space. These registers contain the offset values used to address a 64K byte segment. The registers are controlled explicitly through program control or implicitly by high-level language functions and instructions.

The real-time system software can also utilize the programmable timers as shown in Table 2 and various interrupt control modes available on the ADCP board to have responsive and effective application solutions.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	An interrupt is generated on terminal count being reached. This function is useful for generation of real-time clocks.
Rate Generator	Divide by N counter. Based on the input clock period, the output pulse remains low until the count is expired.
Square Wave Generator	Output remains high for one-half the count, goes low for the remainder of the count.
Software Triggered Strobe	Output remains high until count expires, then goes low for one clock period.

Numeric Data Processor Extension

The 8088 instruction set includes 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD, and unpacked ASCII data. For enhanced numerics processing capability, the iSBC 337 MULTIMODULE Numeric Data Processor extends the 8088 architecture and data set.

The extended numerics capability includes over 60 numeric instructions offering arithmetic, trigonometric, transcendental, logarithmic, and exponential instructions. Many math-oriented applications utilize the 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD, and 80-bit temporary data types.

16K Bytes Static Ram

The iSBC 88/45 ADCP board contains 16K bytes of high-speed static RAM, with 12K bytes dual-ported which is addressable from other MULTIBUS devices. When coupled with the high-speed DMA capability of the iSBC 88/45 ADCP board, the dual-ported memory provides effective data communication buffers. The dual-ported memory is useful for interprocessor message transfers.

Interrupt Capability

The iSBC 88/45 ADCP board provides nine vectored interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line. The additional eight interrupt levels are vectored via the Intel 8259A Programmable Interrupt Controller (PIC). As shown in Table 3, four priority processing modes are available to match interrupt servicing requirements. These modes and priority assignments are dynamically configurable by the system software.

Table 3. Programmable Interrupt Modes

Mode	Operation
Nested	Interrupt request line priorities fixed; interrupt 0 is the highest and 7 is the lowest.
Auto-Rotating	The interrupt priority rotates; once an interrupt is serviced it becomes the lowest priority.
Specific Priority	System software assigns lowest level priority. The other levels are sequenced based on the level assigned.
Polled	System software examines priority interrupt via interrupt status register.

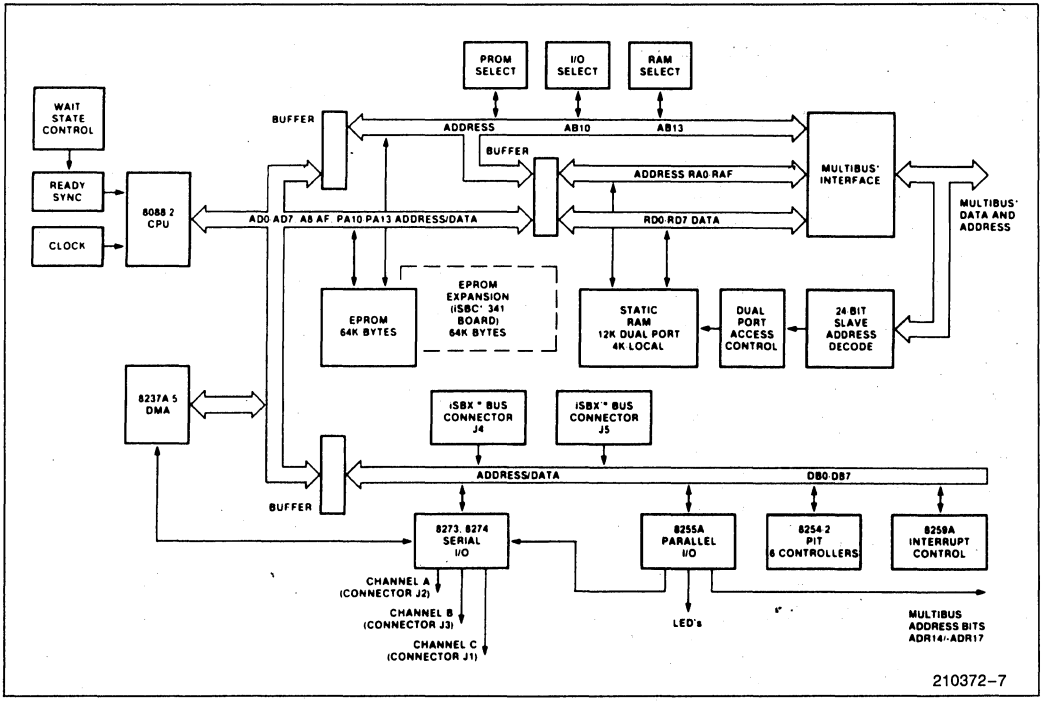


Figure 6. Block Diagram of the iSBC® 88/45 ADCP Board

Interrupt Request Generation

Listed in Table 4 are the devices and functions supported by interrupts on the iSBC 88/45 ADCP board. All interrupt signals are brought to the interrupt jumper matrix. Any of the 23 interrupt sources are strapped to the appropriate 8259A PIC request level. The PIC resolves requests according to the software selected mode and, if the interrupt is unmasked, issues an interrupt to the CPU.

EPROM/RAM Expansion

In addition to the on-board RAM, the iSBC 88/45 ADCP board provides four 28-pin JEDEC sockets for EPROM expansion. By using 2764 EPROMs, the board has 32K bytes of program storage. Three of the JEDEC standard sockets also support byte-wide static RAMs or iRAMs; using 8K x 8 static RAMs provides an additional 24K bytes of RAM.

Inserting the optional iSBC 341 MULTIMODULE EPROM expansion board onto the iSBC 88/45 ADCP board provides four additional 28-pin JEDEC sites. This expansion doubles the available program storage or extends the RAM capability by 32K bytes.

iSBX™ MULTIMODULE™ Expansion

Two 8-bit iSBX MULTIMODULE connectors are provided on the iSBC 88/45 microcomputer. Through these connectors, additional iSBX functions extend the I/O capability of the microcomputer. The iSBX connectors provide the necessary signals to interface to the local bus.

In addition to specialized or custom designed iSBX boards, the customer has a broad range of Intel iSBC MULTIMODULEs available, including parallel I/O, analog I/O, iEEE 488 GPIB, floppy disk, magnetic bubbles, video, and serial I/O boards.

The serial I/O MULTIMODULE boards include the iSBX 351 (one ASYNC/SYNC serial channel) the iSBX 352 (one HDLC/SDLC serial channel) and the iSBX 354 (two SYNC/ASYNC, HDLC/SDLC serial channels) boards. Adding two iSBX 352 MULTIMODULE boards to the iSBC 88/45 ADCP provides a total of five HDLC/SDLC channels.

MULTIBUS® Multimaster Capabilities

OVERVIEW

The MULTIBUS system is Intel's industry standard microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the MULTIBUS structure with 24 address and 16 data lines. In addition to expanding functions contained on a single board computer (e.g., memory and digital I/O), the MULTIBUS structure allows very powerful distributed processing configurations with multiple processors, intelligent slaves, and peripheral boards.

Multimaster Capability

The iSBC 88/45 ADCP board provides full MULTIBUS arbitration control logic. This control

Table 4. Interrupt Request Sources

Device	Function	No. of Interrupts
MULTIBUS Interface	Select 1 interrupt from MULTIBUS resident peripherals or other CPU boards.	8
8273 HDLC/SDLC Controller	Transmit buffer empty and receive buffer full	2
8274 HDLC/SDLC SYNC/ASYNC Controller	Software examines register for status of communication operation	1
8254-Timer	Counter 2 of both PIT devices	2
iSBX Connectors	Function determined by iSBX MULTIMODULE Board (2 interrupts per socket)	4
Bus Fail Safe Timer	Indicates MULTIBUS addressed device has not responded to command within 4 msec	1
Power Line Clock	Source of 60 MHz signal from power supply	1
Bus Flag Interrupt	Flag interrupt in byte location 1000H signals board reset or data handling request	2
iSBC 337A Board	Numeric Data Processor generated status information	1
8237A-5	Signals end of 8237 DMA operation	1

logic allows up to three iSBC 88/45 ADCP boards or other bus masters, including iSBC 286, iSBC 86 and iSBC 86 family boards to share the system bus using a serial (daisy chain) priority scheme. By using an external parallel priority decoder, the MULTIBUS system bus could be shared among sixteen masters.

The Intel standard MULTIBUS Interprocessor Protocol (MIP) software, implemented as the Intel iMMX 800 package for iRMX 86 and iRMX 88 Real-Time Executives, fully supports multiple 8- and 16-bit distributed processor functions. The software manages the message passing protocol between microprocessors.

System Development Capabilities

The application development cycle for an iSBC 88/45 ADCP board is reduced and simplified through the usage of several Intel tools. The tools include the Intellec Series Microcomputer Development System, the ICE-88 In-Circuit Emulator, the iSDM 86 debug monitor software, and the iRMX 86 and iRMX 88 run-time support packages.

The Intellec Series Microcomputer Development System offers a complete development environment for the iSBC 88/45 software. In addition to the operating system, assembler, utilities and application debugger features provided with the system, the user optionally can utilize higher-level languages like PL/M, PASCAL, and FORTRAN.

The ICE-88 In-Circuit Emulator provides a link between the Intellec system and the target iSBC 88/45-based system for code loading and execution. The ICE-88 package assists the developer with the debugging and system integrating processes.

Run-Time Building Blocks

Intel offers run-time foundation software to support applications which range from general purpose to high-performance solutions. The iRMX 88 Real-time Multitasking Executive provides a multitasking structure which includes task scheduling, task management, intertask communications, and interrupt servicing for high-performance applications. The highly configurable modules make the system tailoring job easier whether one uses the compact executive or the complete executive with its variety of peripheral devices supported.

The iRMX 86 Operating System provides a very rich set of features and options to support sophisticated applications solutions. In addition to supporting real-time requirements, the iRMX 86 Operating System has a powerful, but easy-to-use human interface. When added to the sophisticated I/O system, the iRMX 86 Operating System is readily extended to support assembler, PL/M, PASCAL, and FORTRAN software development environments. The modular building block software lends itself well to customized application solutions.

SPECIFICATIONS

Word Size

Instruction: 8, 16, 24, or 32 bits
Data: 8 or 16 bits

System Clock

8 MHz: ±0.1%

NOTE:
Jumper selectable for 4 MHz operation with iSBC 337 Numeric Data Processor module or ICE-88 product.

Cycle Time

Basic Instruction Cycle at 8.00 MHz: 1.25 μs, 250 ns (assumes instruction in the queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles).

Memory Cycle Time

RAM: 500 ns (no wait states)
EPROM: jumper selectable from 500 ns to 625 ns.

On-Board RAM*

K Bytes	Hex Address Range
16 (total)	0000–3FFF
12 (dual-ported)	1000–3FFF

*Four iSBC 88/45 EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMs (3 sockets); iSBC 341 (4 sockets)

Environmental Characteristics

Temperature: 0°C to +55°C, free moving air across the base board and MULTIMODULE board

Humidity: 90%, non-condensing

Physical Characteristics

Width: 30.48 cm (12.00 in)
Length: 17.15 cm (6.75 in)
Height: 1.50 cm (0.59 in)
Weight: 6.20 gm (22 oz)

Memory Capacity/Addressing

On-Board EPROM*

Device	Total K Bytes	Hex Address Range
2716	8	FE000–FFFFF
2732A	16	FC000–FFFFF
2764	32	F8000–FFFFF
27128	64	F0000–FFFFF

With optional iSBC® 341 MULTIMODULE™ EPROM

Device	Total K Bytes	Hex Address Range
2716	16	FC000–FFFFF
2732A	32	F8000–FFFFF
2764	64	F0000–FFFFF
27128	128	E0000–FFFFF

*Four iSBC 88/45 EPROM sockets support JEDEC 24/28-pin standard EPROMs and RAMs (static and iRAM, 3 sockets); iSBC 341 sockets also support EPROMs and RAMs.

Timer Input Frequency—8.00 MHz ±0.1%

Interfaces

iSBX™ Bus—All signals TTL compatible

Serial RS232C Signals—

CTS	CLEAR TO SEND
DSR	DATA SET READY
DTE TXC	TRANSMIT CLOCK
DTR	DATA TERMINAL READY
FG	FRAME GROUND
RTS	REQUEST TO SEND
RXC	RECEIVE CLOCK
RXD	RECEIVE DATA
SG	SIGNAL GROUND
TXD	TRANSMIT DATA

Serial RS422A/449 Signals—

CS	CLEAR TO SEND
DM	DATA MODE
RC	RECEIVE COMMON
RD	RECEIVE DATA
RS	REQUEST TO SEND
RT	RECEIVE TIMING
SC	SEND COMMON
SD	SEND DATA
SG	SIGNAL GROUND
TR	TERMINAL READY
TT	TERMINAL TIMING

Electrical Characteristics

DC Power Dissipation—28.3 Watts

DC Power Requirements

Configuration	Current Requirements (All Voltages ±5%) +5V	+12V	−12V
Without EPROM(1)	5.1A	20 mA	20 mA
With 8K EPROM (Using 2716)	+0.14A	—	—
With 16K EPROM (Using 2732A)	+0.20A	—	—
With 32K EPROM (Using 2764)	+0.24A	—	—
With 64K EPROM (Using 27128)	+0.24A	—	—

NOTE:
1. AS SHIPPED—no EPROMs in sockets, no iSBC 341 module. Configuration includes terminators for two RS422A/449 and one RS232C channels.

Serial Communication Characteristics

Channel	Device	Supported Interface	Max. Baud Rate
A	8274(1)	RS442A/449 RS232C CCITT V.24	800K SDLC/HDLC 125K Synchronous 50K Asynchronous
B	8274	RS232C CCITT V.24	125K Synchronous(2) 50K Asynchronous
C	8273(3)	RS442A/449 RS232C CCITT V.24	64K SDLC/HDLC(3) 9.6K SELF CLOCKING

NOTES:
1. 8274 supports HDLC/SDLC/SYNC/ASYNC multiprotocol
2. Exceed RS232C/CCITT V.24 rating of 20K baud
3. 8273 supports HDLC/SDLC

BAUD RATE EXAMPLES (Hz)

8254 Timer Divide Count N	Synchronous K Baud	Asynchronous ÷16 K Baud	÷32 K Baud	÷64 K Baud
10	800	50.0	25.0	12.5
26	300	19.2	9.6	4.8
31	256	16.1	8.06	4.03
52	154	9.6	4.8	2.4
104	76.8	4.8	2.4	1.2
125	64	4.0	2.0	1.0
143	56	3.5	1.7	0.87
167	48	3.0	1.5	0.75
417	19.2	—	—	—
833	9.6	—	—	—
EQUATION	$\frac{8{,}000{,}000}{N}$	$\frac{500K}{N}$	$\frac{250K}{N}$	$\frac{125K}{N}$

SERIAL INTERFACE CONNECTORS

Interface	Mode(1)	MULTIMODULE™ Edge Connector	Cable	Connector
RS232C	DTE	26-pin(4), 3M-3462-0001	3M(2)-3349/25	25-pin(6), 3M-3482-1000
RS232C	DCE	26-pin(4), 3M-3462-0001	3M(2)-3349/25	25-pin(6), 3M-3483-1000
RS449	DTE	40-pin(5), 3M-3464-0001	3M(3)-3349/37	37-pin(7), 3M-3502-1000
RS449	DCE	40-pin(5), 3M-3464-0001	3M(3)-3349/37	37-pin(7), 3M-3503-1000

NOTES:
1. DTE—Data Terminal Equipment Mode (male connector); DCE—Data Circuit Equipment mode (female connector) requires line swaps.
2. Cable is tapered at one end to fit the 3M-3462 connector.
3. Cable is tapered to fit 3M-3464 connector.
4. Pin 26 of the edge connector is not connected to the flat cable.
5. Pins 38, 39, and 40 of the edge connector are not connected to the flat cable.
6. May be used with the cable housing 3M-3485-1000.
7. Cable housing 3M-3485-4000 may be used wih the connector.

Line Drivers (Supplied)

Device	Characteristic	Qty	Installed
1488	RS232C	3	1
1489	RS232C	3	1
3486	RS422A	2	2
3487	RS422A	2	2

Reference Manual

143824—iSBC 88/45 Advanced Data Communications Processor Board Hardware Reference Manual (not supplied).

Reference manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

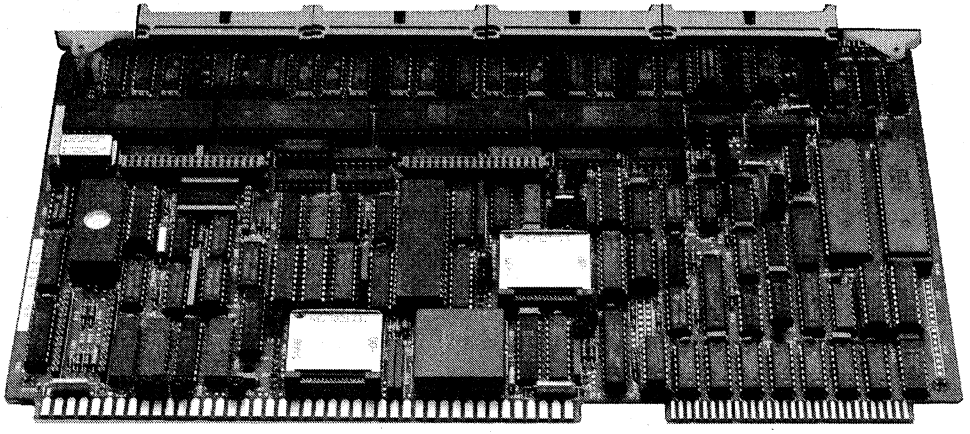
ORDERING INFORMATION

Part Number	Description
SBC 88/45	8-bit 8088-based Single Board Computer with 3 HDLC/SDLC serial channels

iSBC® 188/56
ADVANCED COMMUNICATING COMPUTER

- **iSBC® Single Board Computer or Intelligent Slave Communication Board**
- **8 Serial Communications Channels, Expandable to 12 Channels on a Single MULTIBUS® Board**
- **8 MHz 80188 Microprocessor**
- **Supports RS232C Interface on 6 Channels, RS422A/449 or RS232C Interface Configurable on 2 Channels**
- **Supports Async, Bisync HDLC/SDLC, On-Chip Baud Rate Generation, Half/Full-Duplex, NRZ, NRZI or FM Encoding/Decoding**
- **7 On-Board DMA Channels for Serial I/O, 2 80188 DMA Channels for the iSBX™ MULTIMODULE™ Board**
- **MULTIBUS Interface for System Expansion and Multimaster Configuration**
- **Two iSBX Connectors for Low Cost I/O Expansion**
- **256K Bytes Dual-Ported RAM On-Board**
- **Two 28-pin JEDEC PROM Sites Expandable to 6 Sites with the iSBC 341 MULTIMODULE Board for a Maximum of 192K Bytes EPROM**
- **Resident Firmware to Handle up to 12 RS232C Async Lines**

The iSBC 188/56 Advanced Communicating Computer (COMMputer™) is an intelligent 8-channel single board computer. This iSBC board adds the 8 MHz 80188 microprocessor-based communications flexibility to the Intel line of OEM microcomputer systems. Acting as a stand-alone CPU or intelligent slave for communication expansion, this board provides a high performance, low-cost solution for multi-user systems. The features of the iSBC 188/56 board are uniquely suited to manage higher-layer protocol requirements needed in today's data communications applications. This single board computer takes full advantage of Intel's VLSI technology to provide state-of-the-art, economic, computer based solutions for OEM communications-oriented applications.



280715-1

*IBM is a registered trademark of International Business Machines
*UNIX is a trademark of Bell Laboratories
*XENIX is a trademark of Microsoft Corporation

November 1986
Order Number: 280715-002

OPERATING ENVIRONMENT

The iSBC 188/56 COMMputer™ features have been designed to meet the needs of numerous communications applications. Typical applications include:

1. Terminal/cluster controller
2. Front-end processor
3. Stand-alone communicating computer

Terminal/Cluster Controller

A terminal/cluster controller concentrates communications in a central area of a system. Efficient handling of messages coming in or going out of the system requires sufficient buffer space to store messages and high speed I/O channels to transmit messages. More sophisticated applications, such as cluster controllers, also require character and format conversion capabilities to allow different types of terminals to be attached.

The iSBC 188/56 Advanced Communicating Computer is well suited for multi-terminal systems (see Figure 1). Up to 12 serial channels can be serviced in multi-user or cluster applications by adding two iSBX 354 MULTIMODULE boards. The dual-port RAM provides a large on-board buffer to handle incoming and outgoing messages at data rates up to 19.2K baud. Two channels are supported for continuous data rates greater than 19.2K baud. Each serial channel can be individually programmed for different baud rates to allow system configurations with differing terminal types. The firmware supplied on the iSBC 188/56 board supports up to 12 asynchronous RS232C serial channels, provides modem control and performs power-up diagnostics. The high performance of the on-board CPU provides intelligence to handle protocols and character handling typically assigned to the system CPU. The distribution of intelligence results in optimizing system performance by releasing the system CPU of routine tasks.

Front-End Processor

A front-end processor off-loads a system's central processor of tasks such as data manipulation and text editing of characters collected from the attached terminals. A variety of terminals require flexible terminal interfaces. Program code is often dynamically downloaded to the front-end processor from the system CPU. Downloading code requires sufficient memory space for protocol handling and program code. Flow control and efficient handling of interrupts require an efficient operating system to manage the hardware and software resources.

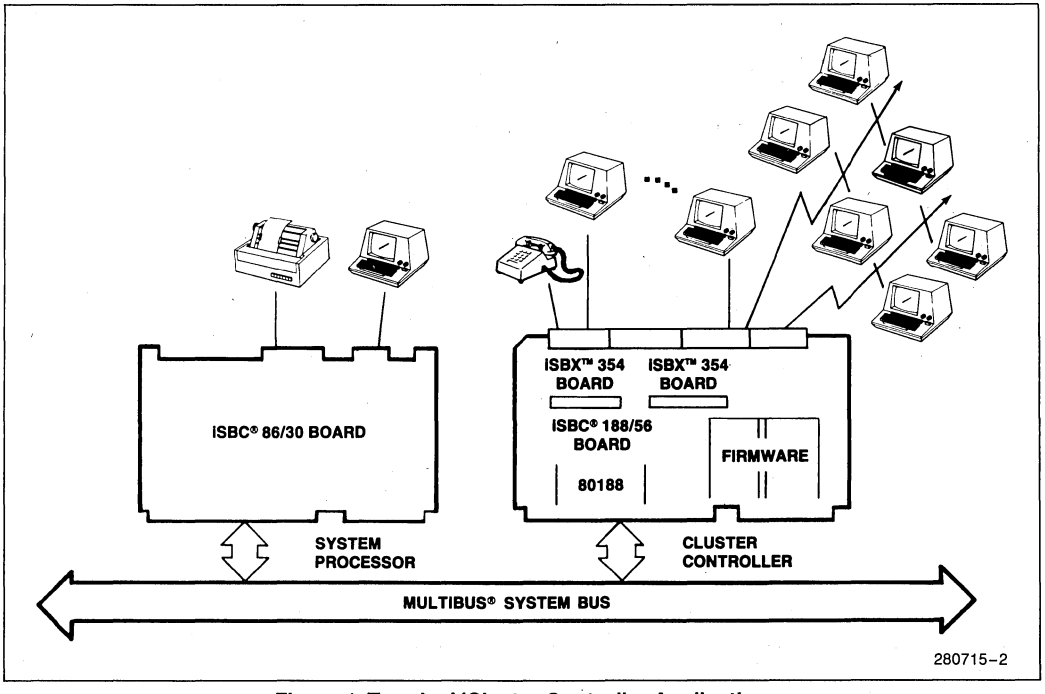


Figure 1. Terminal/Cluster Controller Application

The iSBC 188/56 board features are designed to provide a high performance solution for front-end processor applications (see Figure 2). A large amount of random access memory is provided for dynamic storage of program code. In addition, local memory sites are available for storing routine programs such as X.25, SNA or bisync protocol software. The serial channels can be configured for links to mainframe systems, point-to-point terminals, modems or multidrop configurations.

Stand-Alone COMMputer™ Application

A stand-alone communication computer is a complete computer system. The CPU is capable of managing the resources required to meet the needs of multi-terminal, multi-protocol applications. These applications typically require multi-terminal support, floppy disk control, local memory allocation, and program execution and storage.

To support stand-alone applications, the iSBC 188/56 COMMputer board uses the computational capabilities of an on-board CPU to provide a high-speed system solution controlling 8 to 12 channels of serial I/O (see Figure 3). The local memory available is large enough to handle special purpose code, execution code and routine protocol software.

The MULTIBUS interface can be used to access additional system functions. Floppy disk control and graphics capability can be added to the iSBC standalone computer through the iSBX connectors.

ARCHITECTURE

The four major functional areas are Serial I/O, CPU, Memory and DMA. These areas are illustrated in Figure 4.

Serial I/O

Eight HDLC/SDLC serial interfaces are provided on the iSBC 188/56 board. The serial interface can be expanded to 12 channels by adding 2 iSBX 354 MULTIMODULE boards. The HDLC/SDLC interface is compatible with IBM* system and terminal equipment and with CCITT's X.25 packet switching interface.

Four 82530 Serial Communications Controllers (SCC) provide eight channels of half/full duplex serial I/O. Six channels support RS232C interfaces. Two channels are RS232C/422/449 configurable and can be tri-stated to allow multidrop networks. The 82530 component is designed to satisfy several serial communications requirements; asynchronous,

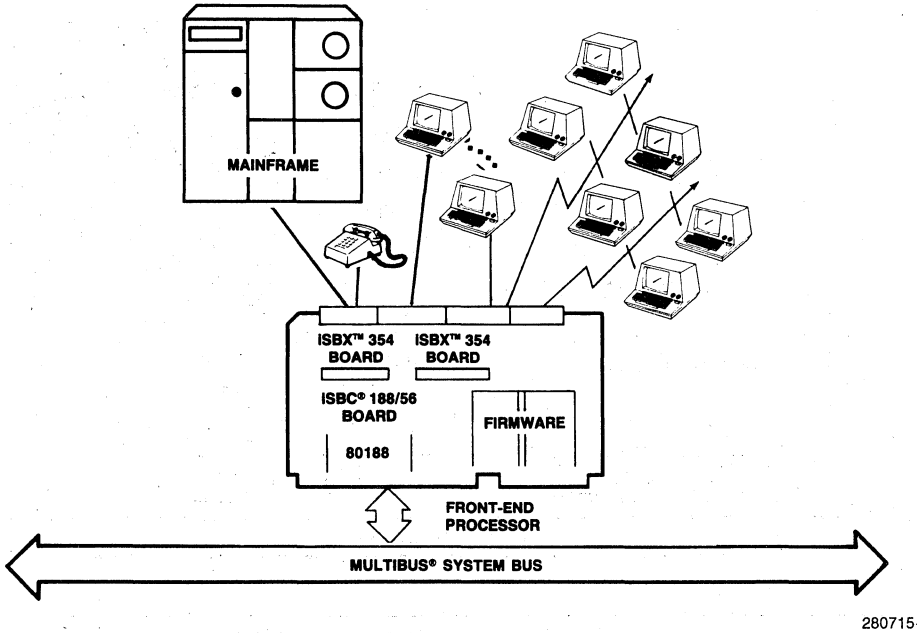


Figure 2. Front-End Processor Application

byte-oriented synchronous (HDLC/SDLC) modes. The increased capability at the serial controller point results in off-loading the CPU of tasks formerly assigned to the CPU or its associated hardware. Configurability of the 82530 allows the user to configure it to handle all asynchronous data formats regardless of data size, number of start or stop bits, or parity requirements. An on-chip baud rate generator allows independent baud rates on each channel.

The clock can be generated either internally with the SCC chip, with an external clock or via the NRZ1 clock encoding mechanism.

All eight channels can be configured as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). Table 1 lists the interfaces supported.

Table 1. iSBC® 188/56 Interface Support

Connection	Synchronous	Asynchronous
	Modem to Direct	Modem to Direct
Point-to-Point	X**	X
	Channels	Channels
Multidrop	0 and 1	0 and 1
Loop	X	N/A

**All 8 channels are denoted by X.

Central CPU

The 80188 central processor component provides high performance, flexibility and powerful processing. The 80188 component is a highly integrated microprocessor with an 8-bit data bus interface and a 16-bit internal architecture to give high performance. The 80188 is upward compatible with 86 and 186 software.

The 80188/82530 combination with on-board PROM/EPROM sites, and dual-port RAM provide the intelligence and speed to manage multi-user, multi-protocol communication operations.

Memory

There are two areas of memory on-board: dual-port RAM and universal site memory. The iSBC 188/56 board contains 256K bytes of dual-port RAM that is addressable by the 80188 on-board. The dual-port memory is configurable anywhere in a 16M byte address space on 64K byte boundaries as addressed from the MULTIBUS port. Not all of the 256K bytes are visible from the MULTIBUS bus side. The amount of dual-port memory visible to the

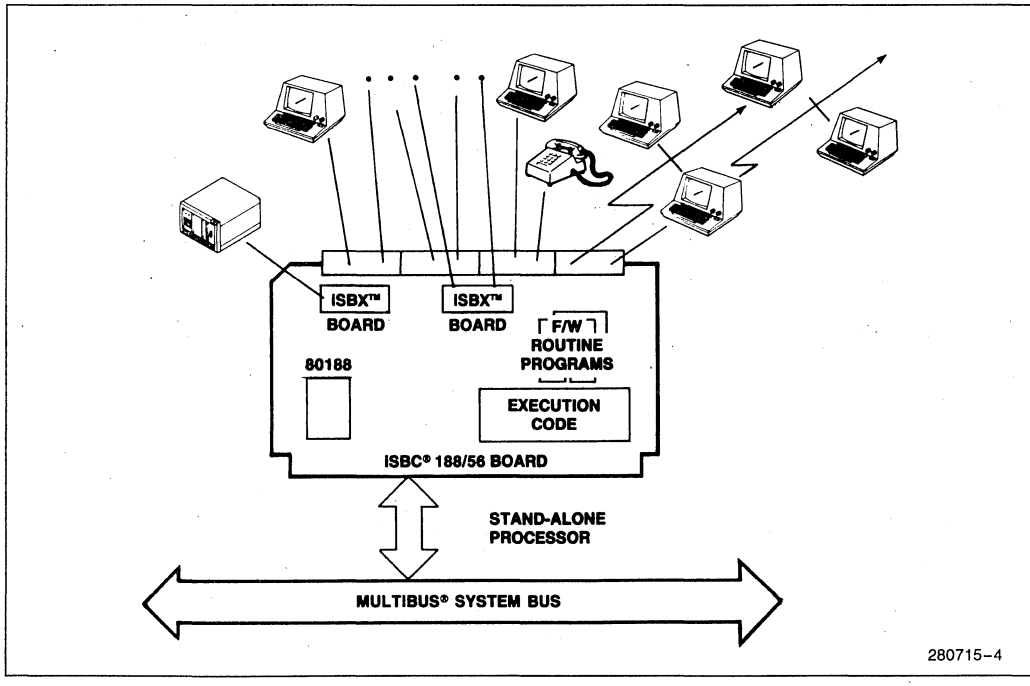


Figure 3. Stand-Alone COMMputer™ Application

MULTIBUS side can be set (with jumpers) to none, 16K bytes, or 48K bytes. In a multiprocessor system these features provide local memory for each processor and shared system memory configurations where the total system memory size can exceed one megabyte without addressing conflicts.

The second area of memory is universal site memory providing flexible memory expansion. Two 28-pin JEDEC sockets are provided. One of these sockets is used for the resident firmware as described in the FIRMWARE section.

The default configuration of the boards supports 16K byte EPROM devices such as the Intel 27128 component. However, these sockets can contain ROM, EPROM, Static RAM, or EEPROM. Both sockets must contain the same type of component (i.e. as the first socket contains an EPROM for the resident firmware, the second must also contain an EPROM with the same pinout). Up to 32K bytes can be addressed per socket giving a maximum universal site memory size of 64K bytes. By using the iSBC 341 MULTIMODULE board, a maximum of 192K bytes of universal site memory is available. This provides sufficient memory space for on-board network or resource management software.

On-Board DMA

Seven channels of Direct Memory Access (DMA) are provided between serial I/O and on-board dual port RAM by two 8237-5 components. Each of channels 0, 1, 2, 3, 5, 6, and 7 is supported by their own DMA line. Serial channels 0 and 1 are configurable for full duplex DMA. Configuring the full duplex DMA option for Channels 0 and 1 would require Channels 2 and 3 to be interrupt driven or polled. Channel 4 is interrupt driven or polled only.

Two DMA channels are integrated in the 80188 processor. These additional channels can be connected to the iSBX interfaces to provide DMA capability to iSBX MULTIMODULE boards such as the iSBX 218A Floppy Disk Controller MULTIMODULE board.

OPERATING SYSTEM SUPPORT

Intel offers run-time foundation software to support applications that range from general purpose to high-performance solutions.

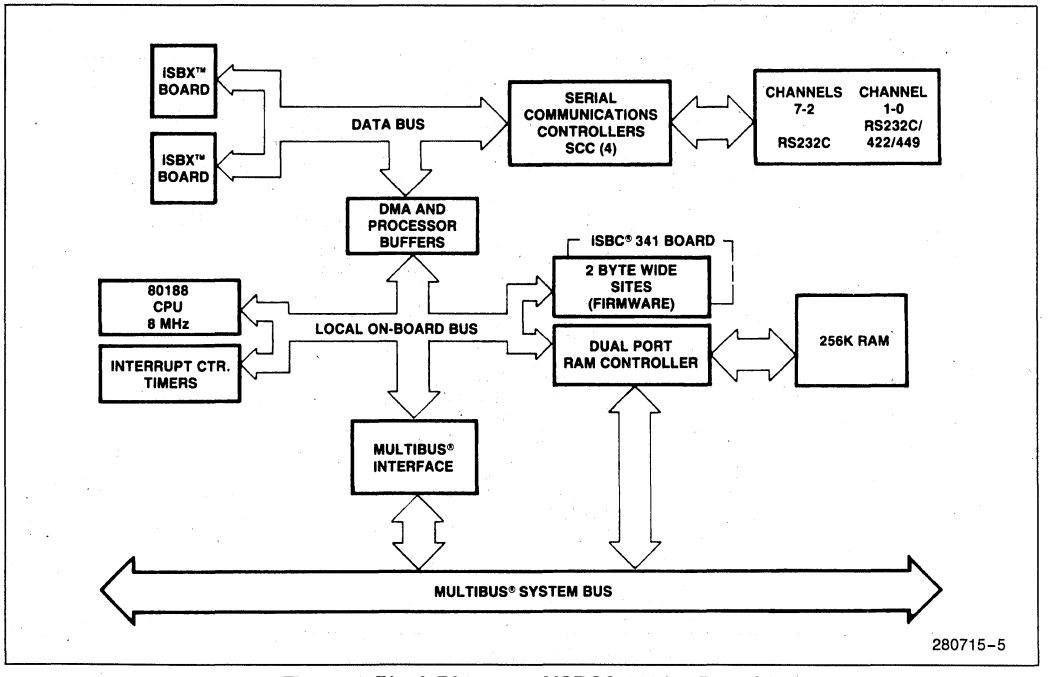


Figure 4. Block Diagram of iSBC® 188/56 Board

Release 6 of the iRMX 86 Operating System provides a rich set of features and options to support sophisticated stand-alone communications applications on the iSBC 188/56 Advanced Communicating Computer. In addition to supporting real-time requirements, the iRMX 86 Operating System Release 6 has a powerful, yet easy to use human interface. Services provided by the iRMX 86 Operating System include facilities for executing programs concurrently, sharing resources and information, servicing asynchronous events and interactively controlling system resources and utilities. The iRMX 86 Operating System is readily extended to support assembler, PL/M, PASCAL, and FORTRAN software development environments. The modular building block software lends itself well to customized application solutions. If the iSBC 188/56 board is acting as an intelligent slave in a system environment, an iRMX 86 driver resident in the host CPU can be written by following the examples in the manual "Guide to Writing Device Driven for iRMX 86 and iRMX 88 I/O Systems".

The iSDM™ 86 System Debug Monitor supports target system debugging for the iSBC 188/56 Advanced Communicating COMMputer board. The monitor contains the necessary hardware, software and documentation required to interface the iSBC 188/56 target system to an Intel microcomputer development system for debugging application software.

The XENIX* 286 Operating System, Release 3, is a fully licensed adaptation of the Bell Laboratories System III UNIX* Operating System. The XENIX system is an interactive, protected, multi-user, multitasking operating system with a powerful, flexible human interface. Release 3 of XENIX 286 includes a software driver for the iSBC 188/56 board (and up to two iSBX 354 MULTIMODULE Boards) acting as an intelligent slave for multi-user applications requiring multiple persons running independent, terminal-oriented jobs. Example applications include distributed data processing, business data processing, software development and engineering or scientific data analysis. XENIX 286 Release 3 Operating System services include device independent I/O, tree-structured file directory and task hierarchies, re-entrant/shared code and system accounting and security access protection.

Table 2. Features of the iSBC® 188/56 Firmware

Feature	Description
Asynchronous Serial Channel Support	Supports the serial channels in asynchronous ASCII mode. Parameters such as baud rate, parity generation, parity checking and character length can be programmed independently for each channel.
Block Data Transfer (On Output)	Relieves the host CPU of character-at-a-time interrupt processing. The iSBC 188/56 board accepts blocks of data for transmission and interrupts the processor only when the entire block is transmitted.
Limited Modem Control	Provides software control of the Data Terminal Ready (DTR) line on all channels. Transitions on the Carrier Detect (CD) line are sensed and reported to the host CPU.
Tandem Modem Support	Transmits an XOFF character when the number of characters in its receive buffer exceeds a threshold value and transmits an XON character when the buffer drains below some other threshold.
Download and Execute Capability	Provides a capability for the host CPU to load code anywhere in the address space of the iSBC 188/56 board and to start executing at any address in its address space.
Power Up Confidence Tests	On board reset, the firmware executes a series of simple tests to establish that crucial components on the board are functional.

FIRMWARE

The iSBC 188/56 Communicating COMMputer board is supplied with resident firmware that supports up to 12 RS232C asynchronous serial channels. In addition, the firmware provides a facility for a host CPU to download and execute code on the iSBC 188/56 board. Simple power-up confidence tests are also included to provide a quick diagnostic service. The firmware converts the iSBC 188/56 COMMputer board to a slave communications controller. As a slave communications controller, it requires a separate MULTIBUS host CPU board and requires the use of MULTIBUS interrupt line to signal the host processor. Table 2 summarizes the features of the firmware.

INTERRUPT CAPABILITY

The iSBC 188/56 board has two programmable interrupt controllers (PICs). One is integrated into the 80188 processor and the other in the 80130 component. The two controllers are configured with the 80130 controller as the master and the 80188 controller as the slave. Two of the 80130 interrupt inputs are connected to the 82530 serial controller components to provide vector interrupt capabilities by the serial controllers. The iSBC 188/56 board provides 22 interrupt levels. The highest level is the NMI (Non-Maskable Interrupt) line which is directly tied to the 80188 CPU. This interrupt is typically used for signaling catastrophic events (e.g. power failure). There are 5 levels of interrupts internal to the 80188 processor. Another 8 levels of interrupts are available from the 80130 component. Of these 8, one is tied to the programmable interrupt controller (PIC) of the 80188 CPU. An additional 8 levels of interrupts are available at the MULTIBUS interface. The iSBC 188/56 board does not support bus vectored interrupts. Table 3 lists the possible interrupt sources.

Table 3. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface INT0–INT7	Requests from MULTIBUS resident peripherals or other CPU boards.	8
82530 Serial Controllers	Transmit buffer empty, receive buffer full and channel errors 1 and external status.	8 per 82530 Total = 32
Internal 80188 Timer and DMA	Timer 0, 1, 2 outputs and 2 DMA channel interrupts.	5
80130 Timer Outputs	Timer 0, 1, 2 outputs of 80130.	3
Interrupt from Flag Byte Logic	Flag byte interrupt set by MULTIBUS master (through MULTIBUS® I/O Write).	1
Bus Flag Interrupt	Interrupt to MULTIBUS® (Selectable for INT0 to INT7) generated from on-board 80188 I/O Write.	1
iSBX Connectors iSBX DMA	Function determined by iSBX MULTIMODULE board. DMA interrupt from iSBX (TDMA).	4 (Two per Connector) 2
Bus Fail-Safe Timeout Interrupt.	Indicates iSBC 188/48 board timed out either waiting for MULTIBUS access or timed out from no acknowledge while on MULTIBUS System Bus.	1
Latched Interrupt	Converts pulsed event to a level interrupt. Example: 8237A-5 EOP.	1
OR-Gate Matrix	Concentrates up to 4 interrupts to 1 interrupt (selectable by stake pins).	1
Ring Indicator Interrupt	Latches a ring indicator event from serial channels 4, 5, 6, or 7.	1
NOR-Gate Matrix	Inverts up to 2 interrupts into 1 (selectable by stake pins).	1

SUPPORT FOR THE 80130 COMPONENT

Intel does not support the direct processor execution of the iRMX nucleus primitives from the 80130 component. The 80130 component provides timers and interrupt controllers.

EXPANSION

EPROM Expansion

Memory may be expanded by adding Intel compatible memory expansion boards. The universal site memory can be expanded to six sockets by adding the iSBC 341 MULTIMODULE board for a maximum total of 192K bytes of universal site memory.

iSBX™ MULTIMODULE™ Expansion Module

Two 8-bit iSBX MULTIMODULE connectors are provided on the iSBC 188/56 board. Using iSBX modules additional functions can be added to extend the I/O capability of the board. In addition to specialized or custom designed iSBX boards, there is a broad range of iSBX MULTIMODULE boards from the Intel including parallel I/O, analog I/O, IEEE 488 GPIB, floppy disk, magnetic bubbles, video and serial I/O boards.

The serial I/O MULTIMODULE boards available include the iSBX 354 Dual Channel Expansion MULTIMODULE board. Each iSBX 354 MULTIMODULE board adds two channels of serial I/O to the iSBC 188/56 board for a maximum of twelve serial channels. The 82530 serial communications controller on the MULTIMODULE board handles a large variety of serial communications protocols. This is the same serial controller as is used on the iSBC 188/56 board to offer directly compatible expansion capability for the iSBC 188/56 COMMputer board.

MULTIBUS® INTERFACE

The iSBC 188/56 Advanced COMMputer board can be a MULTIBUS master or intelligent slave in a multimaster system. The iSBC 188/56 board incorporates a flag byte signalling mechanism for use in multiprocessor environments where the iSBC 188/56 board is acting as an intelligent slave. The mechanism provides an interrupt handshake from the MULTIBUS System Bus to the on-board-processor and vice-versa.

The Multimaster capabilities of the iSBC 188/56 board offers easy expansion of processing capacity and the benefits of multiprocessing. Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24 or 32 bits
Data Path—8 bits

Processor Clock	82530 Clock	DMA Clock
8 MHz	4.9152 MHz	4 MHz

Dual Port RAM

iSBC 188/56 Board—256 bytes

As viewed from the 80188—64K bytes

As viewed from the MULTIBUS System Bus—Choice: 0, 16K or 48K

EPROM

iSBC® 188/56 Board Using:	Size	On Board Capacity	Address Range
2732	4K	8K bytes	FE000–FFFFF$_H$
2764	8K	16K bytes	FC000–FFFFF$_H$
27128	16K	32K bytes	F8000–FFFFF$_H$
27256	32K	64K bytes	F0000–FFFFF$_H$
27512	64K	128K bytes	E0000–FFFFF$_H$

Memory Expansion

EPROM with iSBC® 341 Board Using:	Capacity	Address Range
2732	24K bytes	F8000–FFFFF$_H$
2764	48K bytes	F0000–FFFFF$_H$
27128	96K bytes	E0000–FFFFF$_H$
27256	192K bytes	C0000–FFFFF$_H$

I/O Capacity

Serial—8 programmable lines using four 82530 components

iSBX MULTIMODULE—2 iSBX single-wide boards

Serial Communications Characteristics

Synchronous—Internal or external character synchronization on one or two synchronous characters

Asynchronous—5–8 bits and 1, 1½, or 2 stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.

Baud Rates

Synchronous X1 Clock	
Baud Rate	**82530 Count Value (Decimal)**
64000	36
48000	49
19200	126
9600	254
4800	510
2400	1022
1800	1363
1200	2046
300	8190
Asynchronous X16 Clock	
Baud Rate	**82530 Count Value (Decimal)**
19200	6
9600	14
4800	30
2400	62
1800	83
1200	126
300	510
110	1394

Interfaces

iSBX™ BUS

The iSBC 188/56 board meets iSBX compliance level D8/8 DMA

MULTIBUS® SYSTEM BUS

The iSBC 188/56 board meets MULTIBUS compliance level Master/Slave D8 M24 I16 VO EL.

SERIAL RS232C SIGNALS

CD	Carrier
CTS	Clear to Send
DSR	Data Set Ready
DTE TXC	Transmit Clock
DTR	Data Terminal Ready
RTS	Request to Send
RXC	Receive Clock
RXD	Receive Data
SG	Signal Ground
TXD	Transmit Data
RI	Ring Indicator

RS422A/449 SIGNALS

RC	Receive Common
RD	Receive Data
RT	Receive Timing
SD	Send Data
TT	Terminal Timing

Environmental Characteristics

Temperature: 0 to 55°C at 200 Linear Feet/Min. (LFM) Air Velocity

Humidity: to 90%, non-condensing (25°C to 70°C)

Physical Characteristics

Width: 30.48 cm (12.00 in)
Length: 17.15 cm (6.75 in)
Height: 1.04 cm (0.41 in)
Weight: 595 gm (21 oz)

Electrical Characteristics

The power required per voltage for the iSBC 188/56 board is shown below. These numbers do not include the current required by universal memory sites or expansion modules.

Voltage (Volts)	Current (Amps) typ.	Power (Watts) typ.
+5	4.56A	22.8W
+12	0.12A	1.5W
−12	0.11A	1.3W

Reference Manual

iSBC 188/56 Advanced Data Communications Computer Reference Manual Order Number 148209-001.

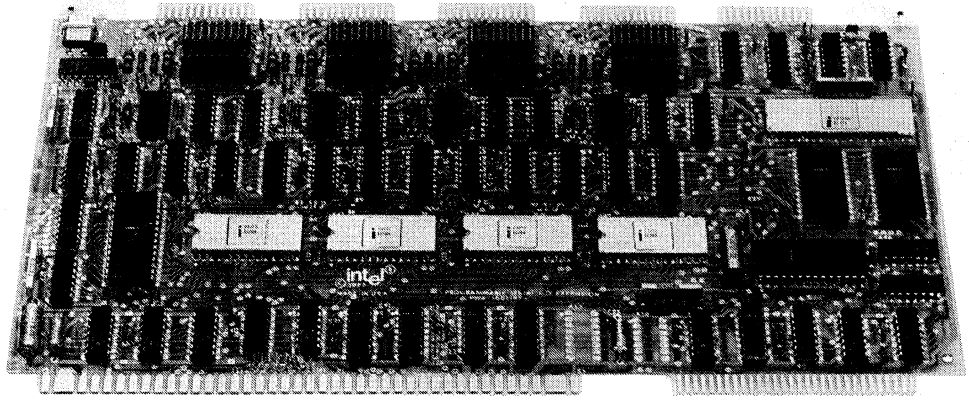
ORDERING INFORMATION

Part Number	Description
iSBC 188/56	8-Serial Channel Advanced Communicating Computer

iSBC® 534
FOUR CHANNEL COMMUNICATION EXPANSION BOARD

- **Serial I/O Expansion Through Four Programmable Synchronous and Asynchronous Communications Channels**
- **Individual Software Programmable Baud Rate Generation for Each Serial I/O Channel**
- **Two Independent Progammable 16-Bit Interval Timers**
- **Sixteen Maskable Interrupt Request Lines with Priority Encoded and Programmable Interrupt Algorithms**
- **Jumper Selectable Interface Register Addresses**
- **16-Bit Parallel I/O Interface Compatible with Bell 801 Automatic Calling Unit**
- **RS232C/CCITT V.24 Interfaces Plus 20 mA Optically Isolated Current Loop Interfaces (Sockets)**
- **Programmable Digital Loopback for Diagnostics**
- **Interface Control for Auto Answer and Auto Originate Modems**

The iSBC 534 Four Channel Communication Expansion Board is a member of Intel's complete line of memory and I/O expansion boards. The iSBC 534 interfaces directly to any single board computer via the MULTIBUS to provide expansion of system serial communications capability. Four fully programmable synchronous and asynchronous serial channels with RS232C buffering and provision for 20 mA optically isolated current loop buffering are provided. Baud rates, data formats, and interrupt priorities for each channel are individually software selectable. In addition to the extensive complement of EIA Standard RS232C signals provided, the iSBC 534 provides 16 lines of RS232C buffered programmable parallel I/O. This interface is configured to be directly compatible with the Bell Model 801 automatic calling unit. These capabilities provide a flexible and easy means for interfacing Intel iSBC based systems to RS232C and optically isolated current loop compatible terminals, cassettes, asynchronous and synchronous modems, and distributed processing networks.



280238-1

November 1986
Order Number: 280238-001

FUNCTIONAL DESCRIPTION

Communications Interface

Four programmable communications interfaces using Intel's 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) are contained on the board.* Each USART can be programmed by the system software to individually select the desired asynchronous or synchronous serial data transmission technique (including IBM Bisync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. Each 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in each USART. Each set of RS232C command lines, serial data lines, and signal ground lines are brought out to 26-pin edge connectors that mate with RS232C flat or round cables.

16-Bit Interval Timers

The iSBC 534 provides six fully programmable and independent BCD and binary 16-bit interval timers utilizing two Intel 8253 programmable interval timers.* Four timers are available to the systems designer to generate baud rates for the USARTs under software control. Routing for the outputs from the other two counters is jumper selectable. Each may be independently routed to the programmable interrupt controller to provide real time clocking or to the USARTs (for applications requiring different transmit and receive baud rates). In utilizing the iSBC 534, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given baud rate or time delay is needed, software commands to the programmable timers select the desired function. Three functions of these timers are supported on the iSBC 534, as shown in Table 1. The contents of each counter may be read at any time during system operation.

Table 1. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached an interrupt request is generated. This function is used for the generation of real-time clocks.
Rate generator	Divide by N counter. The output will go low for one input clock cycle and high for N−1 input clock periods.
Square wave rate generator	Output will remain high for one-half the count and low for the other half of the count.

Interrupt Request Lines

Two independent Intel 8259A programmable interrupt controllers (PIC's) provide vectoring for 16 interrupt levels.* As shown in Table 2, a selection of three priority processing algorithms is available to the system designer. The manner in which requests are serviced may thus be configured to match system requirements. Priority assignments may be reconfigured dynamically via software at any time during system operation. Any combination of interrupt levels may be masked through storage, via software, of a single byte to the interrupt mask register of each PIC. Each PIC's interrupt request output line may be jumper selected to drive any of the nine interrupt lines on the MULTIBUS.

Table 2. Interrupt Priority Options

Algorithm	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.

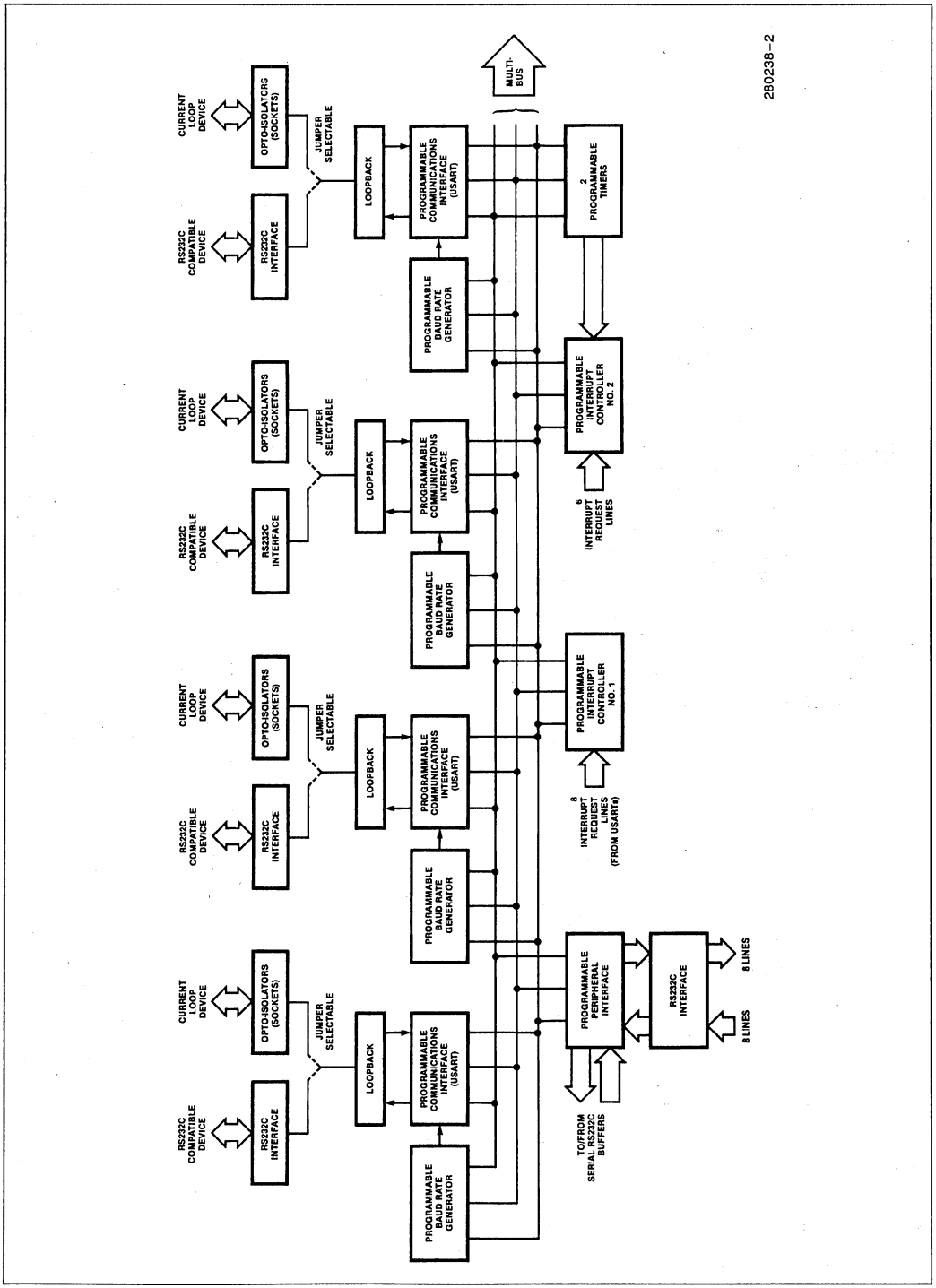


Figure 1. iSBC® 534 Four Channel Communications Expansion Board Block Diagram

Interrupt Request Generation—As shown in Table 3, interrupt requests may originate from 16 sources. Two jumper selectable interrupt requests (8 total) can be automatically generated by each USART when a character is ready to be transferred to the MULTIBUS system bus (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). Jumper selectable requests can be generated by two of the programmable timers (PITs), and six lines are routed directly from peripherals to accept carrier detect (4 lines), ring indicator, and the Bell 801 present next digit request lines.

Systems Compatibility

The iSBC 534 provides 16 RS232C buffered parallel I/O lines implemented utilizing an Intel 8255A programmable peripheral interface (PPI) configured to operate in mode 0.* These lines are configured to be directly compatible with the Bell 801 automatic calling unit (ACU). This capability allows the iSBC 534 to interface to Bell 801 type ACUs and up to four modems or other serial communications devices. For systems not requiring interface to an ACU, the parallel I/O lines may also be used as general purpose RS232C compatible control lines in system implementation.

***NOTE:**
Complete operational details on the Intel 8251A USART, the Intel 8253 Programmable Interval Timer, the Intel 8255A Programmable Peripheral Interface, and the Intel 8259A Programmable Interrupt Controller are contained in the Intel Component Data Catalog.

Table 3. Interrupt Assignments

Interrupt Request Line	PIC 0	PIC 1
0	PORT 0 R_X RDY	PIT 1 counter 1
1	PORT 0 T_X RDY	PIT 2 counter 2
2	PORT 1 R_X RDY	Ring Indicator (all ports)
3	PORT 1 T_X RDY	Present next digit
4	PORT 2 R_X RDY	Carrier detect port 0
5	PORT 2 T_X RDY	Carrier detect port 1
6	PORT 3 R_X RDY	Carrier detect port 2
7	PORT 3 T_X RDY	Carrier detect port 3

SPECIFICATIONS

Serial Communications Characteristics

Synchronous— 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous— 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Sample Baud Rates(1)

Frequency(2) (kHz, Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous	
		÷ 16	÷ 64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

NOTES:
1. Baud rates shown here are only a sample subset of possible software programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit programmable interval timer (used here as frequency divider).
2. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.

Interval Timer and Baud Rate Generator Frequencies

Input Frequency (On-Board Crystal Oscillator)—1.2288 MHz ± 0.1% (0.813 μs period, nominal)

Function	Single Timer		Dual/Timer Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt Interval	1.63 μs	53.3 ms	3.26 μs	58.25 minutes
Rate Generator (Frequency)	18.75 Hz	614.4 kHz	0.0029 Hz	307.2 kHz

Interfaces—RS232C Interfaces

EIA Standard RS232C Signals provided and supported:

Carrier detect	Receive data
Clear to send	Ring indicator
Data set ready	Secondary receive data
Data terminal ready	Secondary transmit data
Request to send	Transmit clock
Receive clock	Transmit data

Parallel I/O—8 input lines, 8 output lines, all signals RS232C compatible

Bus—All signals MULTIBUS system bus compatible

I/O Addressing

The USART, interval timer, interrupt controller, and parallel interface registers of the iSBC 534 are configured as a block of 16 I/O address locations. The location of this block is jumper selectable to begin at any 16-byte I/O address boundary (i.e., 00H, 10H, 20H, etc.).

I/O Access Time

400 ns	USART registers
400 ns	Parallel I/O registers
400 ns	Interval timer registers
400 ns	Interrupt controller registers

Compatible Connectors

Interface	Pins (qty.)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 2KH43/9 AMK12
Serial and parallel I/O	26	0.1	3m 3462-0001 or TI H312113

Compatible Opto-Isolators

Function	Supplier	Part Number
Driver	Fairchild General Electric Monsanto	4N33
Receiver	Fairchild General Electric Monsanto	4N37

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (398 gm)

Electrical Characteristics

Average DC Current

Voltage	Without Opto-Isolators	With Opto-Isolators(1)
V_{CC} = +5V	1.9 A, max	1.9 A, max
V_{DD} = +12V	275 mA, max	420 mA, max
V_{AA} = −12V	250 mA, max	400 mA, max

NOTE:
1. With four 4N33 and four 4N37 opto-isolator packages installed in sockets provided to implement four 20 mA current loop interfaces.

Environmental Characteristics

Operating Temperature: 0°C to +55°C

Reference Manual

502140-002—iSBC 534 Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

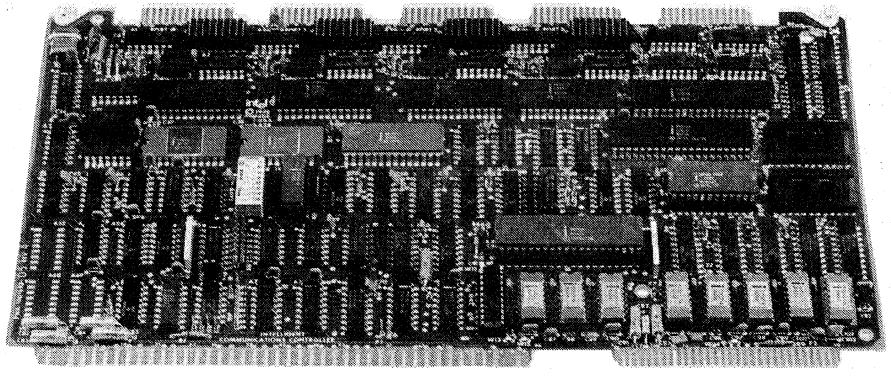
ORDERING INFORMATION

Part Number	Description
SBC 534	Four Channel Communication Expansion Board

iSBC® 544
INTELLIGENT COMMUNICATIONS CONTROLLER

- **iSBC® Communications Controller Acting as a Single Board Communications Computer or an Intelligent Slave for Communications Expansion**
- **On-Board Dedicated 8085A Microprocessor Providing Communications Control and Buffer Management for Four Programmable Synchronous/Asynchronous Channels**
- **Sockets for Up To 8K Bytes of EPROM**
- **16K Bytes of Dual Port Dynamic Read/Write Memory with On-Board Refresh**
- **Extended MULTIBUS® Addressing Permits iSBC 544 Board Partitioning into 16K-Byte Segments in a 1-Megabyte Address Space**
- **Ten Programmable Parallel I/O Lines Compatible with Bell 801 Automatic Calling Unit**
- **Twelve Levels of Programmable Interrupt Control**
- **Individual Software Programmable Baud Rate Generation for Each Serial I/O Channel**
- **Three Independent Programmable Interval Timer/Counters**
- **Interface Control for Auto Answer and Auto Originate Modem**

The iSBC 544 Intelligent Communications Controller is a member of Intel's family of single-board computers, memory, I/O, and peripheral controller boards. The iSBC 544 board is a complete communications controller on a single 6.75 x 12.00 inch printed circuit card. The on-board 8085A CPU may perform local communications processing by directly interfacing with on-board read/write memory, nonvolatile read only memory, four synchronous/asynchronous serial I/O ports, RS232/RS366 compatible parallel I/O, programmable timers, and programmable interrupts.



280239-1

November 1986
Order Number: 280239-001

FUNCTIONAL DESCRIPTION

Intelligent Communications Controller

Two Mode Operation — The iSBC 544 board is capable of operating in one of two modes: 1) as a single board communications computer with all computer and communications interface hardware on a single board; 2) as an "intelligent bus slave" that can perform communications related tasks as a peripheral processor to one or more bus masters. The iSBC 544 may be configured to operate as a standalone single board communications computer with all MPU, memory and I/O elements on a single board. In this mode of operation, the iSBC 544 may also interface with expansion memory and I/O boards (but no additional bus masters). The iSBC 544 performs as an intelligent slave to the bus master by performing all communications related tasks. Complete synchronous and asynchronous I/O and data management are controlled by the on-board 8085A CPU to coordinate up to four serial channels. Using the iSBC 544 as an intelligent slave, multichannel serial transfers can be managed entirely onboard, freeing the bus master to perform other system functions.

Architecture — The iSBC 544 board is functionally partitioned into three major sections: I/O, central computer, and shared dual port RAM memory (Figure 1). The I/O hardware is centered around the four Intel 8251A USART devices providing fully programmable serial interfacing. Included here as well is a 10-bit parallel interface compatible with the Bell 801 automatic calling unit, or equivalent. The I/O is under full control of the on-board CPU and is protected from access by system bus masters. The second major segment of the intelligent communications controller is a central computer, with an 8085A CPU providing powerful processing capability. The 8085A together with on-board EPROM/ROM, static RAM, programmable timers/counters, and programmable

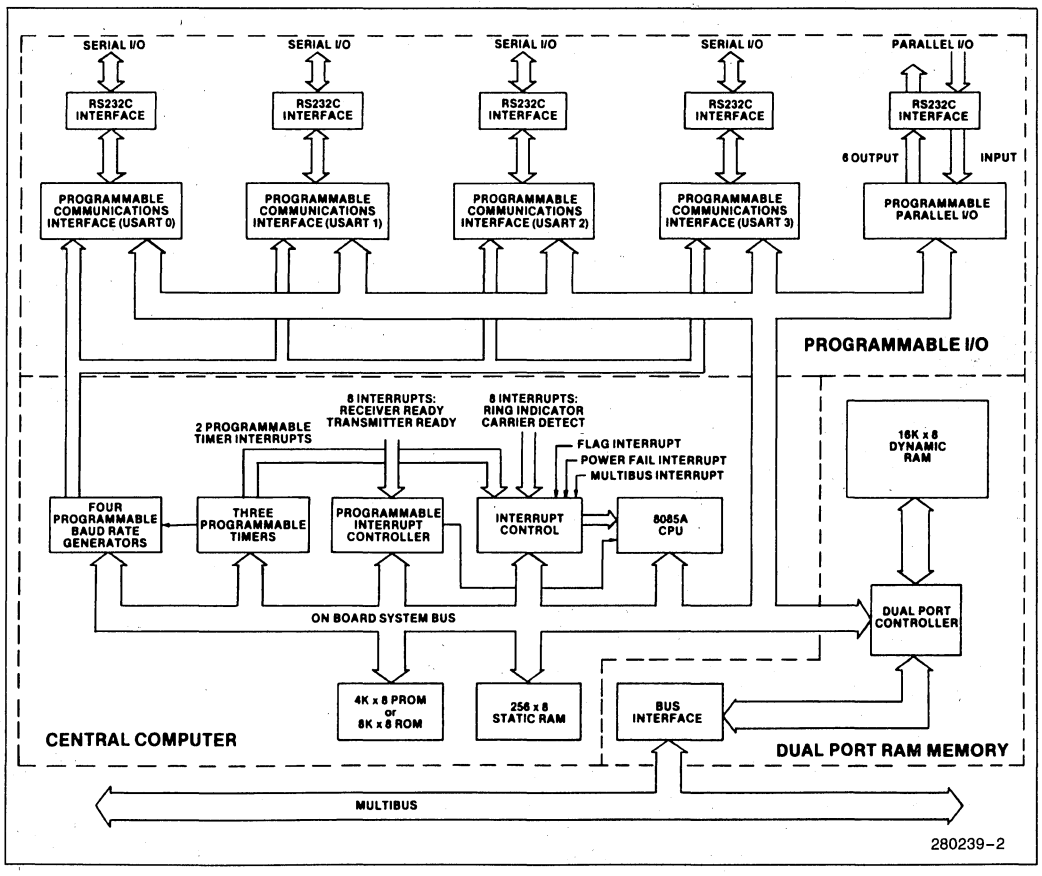


Figure 1. iSBC® 544 Intelligent Communications Controller Block Diagram

interrupt control provide the intelligence to manage sophisticated communications operations on-board the iSBC 544 board. The timer/counters and interrupt control are also common to the I/O area providing programmable baud rates to the USARTs and prioritizing interrupts generated from the USARTs. The central computer functions are protected for access only by the on-board 8085A. Likewise, the on-board 8085A may not gain access to the system bus when being used as an intelligent slave. When the iSBC 544 is used as a bus master, the on-board 8085A CPU controls complete system operation accessing on-board functions as well as memory and I/O expansion. The third major segment, dual port RAM memory, is the key link between the iSBC 544 intelligent slave and bus masters managing the system functions. The dual port concept allows a common block of dynamic memory to be accessed by the on-board 8085A CPU and off-board bus masters. The system program can, therefore, utilize the shared dual port RAM to pass command and status information between the bus masters and on-board CPU. In addition, the dual port concept permits blocks of data transmitted or received to accumulate in the on-board shared RAM, minimizing the need for a dedicated memory board.

Serial I/O

Four programmable communications interfaces using Intel's 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) are contained on the board and controlled by the on-board CPU in combination with the on-board interval timer/counter to provide all common communication frequencies. Each USART can be programmed by the system software to individually select the desired asynchronous or synchronous serial data transmission technique (including IBM Bisync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. Each 8251A provides full duplex, double-buffered, transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in each USART. Each channel is fully buffered to provide a direct interface to RS232C compatible terminals, peripherals, or synchronous/asynchronous modems. Each channel of RS232C command lines, serial data lines, and signal ground lines are brought out to 26-pin edge connectors that mate with RS232C flat or round cable.

Parallel I/O Port

The iSBC 544 provides a 10-bit parallel I/O interface controlled by an Intel 8155 Programmable Interface (PPI) chip. The parallel I/O port is directly compatible with an Automatic Calling Unit (ACU) such as the Bell Model 801, or equivalent, and can also be used for auxiliary functions. All signals are RS232C compatible, and the interface cable signed assignments meet RS366 specifications. For systems not requiring an ACU interface, the parallel I/O port can be used for any general purpose interface requiring RS232C compatibility.

Central Processing Unit

Intel's powerful 8-bit n-channel 8085A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 544. The 8085A CPU is directly software compatible with the Intel 8080A CPU. The 8085A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operators. The minimum instruction execution time is 1.45 microseconds. The 8085A CPU has a 16-bit program counter. An external stack, located within any portion of iSBC 544 read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

EPROM/ROM Capacity

Sockets for up to 8K bytes of nonvolatile read only memory are provided on the iSBC 544 board. Read only memory may be added in 2K byte increments up to a maximum of 4K bytes using Intel 2716 EPROMs or masked ROMs; or in 4K byte increments up to 8K bytes maximum using Intel 2732 EPROMs. All on-board EPROM/ROM operations are performed at maximum processor speed.

RAM Capacity

The iSBC 544 contains 16K bytes of dynamic read/write memory using Intel 2117 RAMs. Power for the on-board RAM may be provided on an auxiliary power bus, and memory protect logic is included for RAM battery backup requirements. The iSBC 544 contains a dual port controller, which provides dual port capability for the on-board RAM memory. RAM accesses may occur from either the on-board 8085A CPU or from another bus master, when used as an intelligent slave. Since on-board RAM accesses do not require the MULTIBUS, the bus is available for concurrent bus master use. Dynamic RAM refresh is accomplished automatically by the iSBC 544 for accesses originating from either the CPU or from the MULTIBUS.

Addressing — On board RAM, as seen by the on-board 8085A CPU, resides at address 8000_H–$BFFF_H$. On-board RAM, as seen by an off-board CPU, may be placed on any 4K byte address boundary. The iSBC 544 provides extended addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the MULTIBUS. In addition, jumper options are provided which allow the user to protect 8K or 12K bytes on-board RAM for use by the on-board 8085 CPU only. This reserved RAM space is not accessible via the MULTIBUS and does not occupy any system address space.

Static RAM — The iSBC 544 board also has 256 bytes of static RAM located on the Intel 8155 PPI. This memory is only accessible to the on-board 8085A CPU and is located at address $7F00_H$–$7FFF_H$.

Programmable Timers

The iSBC 544 board provides seven fully programmable and independent interval timer/counters utilizing two Intel 8253 Programmable Interval Timers (PIT), and the Intel 8155. The two Intel 8253 PITs provide six independent BCD or binary 16-bit interval timer/counters and the 8155 provides one 14-bit binary timer/counter. Four of the PIT timers (BDG0–3) are dedicated to the USARTs providing fully independent programmable baud rates.

Three General Use Timers — The fifth timer (BDG4) may be used as an auxiliary baud rate to any of the four USARTs or may alternatively be cascaded with timer six to provide extended interrupt intervals. The sixth PIT timer/counter (TINT1) can be used to generate interrupt intervals to the on-board 8085A. In addition to the timer/counters on the 8253 PITs, the iSBC 544 has a 14-bit timer available on the 8155 PPI providing a third general use timer/counter (TINT0). This timer output is jumper selectable to the interrupt structure of the on-board 8085A CPU to provide additional timer/counter capability.

Timer Functions — In utilizing the iSBC 544 board, the systems designer simply configures, via software, each timer independently to meet systems requirements. Whenever a given baud rate or interrupt interval is needed, software commands to the programmable timers select the desired function. The on-board PITs together with the 8155 provide a total of seven timer/counters and six operating modes. Mode 3 of the 8253 is the primary operating mode of the four dedicated USART baud rate generators. The timer/counters and useful modes of operation for the general use timer/counters are shown in Table 1.

Interrupt Capability

The iSBC 544 board provides interrupt service for up to 21 interrupt sources. Any of the 21 sources may interrupt the intelligent controller, and all are brought through the interrupt logic to 12 interrupt levels. Four interrupt levels are handled directly by the interrupt processing capability of the 8085A CPU and eight levels are serviced from an Intel 8259A Programmable Interrupt Controller (PIC) routing an interrupt request output to the INTR input of the 8085A (see Table 2).

Table 1. Programmable Timer Functions

Function	Operation	Counter
Interrupt on Terminal Count (Mode 0)	When terminal count is reached, an interrupt request is generated. This function is useful for generation of real-time clocks.	**8253** TINT1
Rate Generator (Mode 2)	Divide by N counter. The output will go low for one input clock cycle and high for N − 1 input clock periods.	**8253** BDG4*
Square-Wave Rate Generator (Mode 3)	Output will remain high until one-half the TC has been completed, and go low for the other half of the count. This is the primary operating mode used for generating a Baud rate clocked to the USARTs.	**8253** BDG0–4 TINT1
Software Triggered Strobe (Mode 4)	When the TC is loaded, the counter will begin. On TC the output will go low for one input clock period.	**8253** BDG4* TINT1
Single Pulse	Single pulse when TC reached.	**8155** TINT0
Repetitive Single Pulse	Repetitive single pulse each time TC is reached until a new command is loaded.	**8155** TINT0

* BDG4 is jumper selectable as an auxiliary baud rate generator to the USARTs or as a cascaded output to TINT1. BDG4 may be used in modes 2 and 4 only when configured as a cascaded output.

Table 2. Interrupt Vector Memory Locations

Interrupt Source		Vector Location	Interrupt Level
Power Fail	TRAP	24_H	1
8253 TINT1	RST 7.5	$3C_H$	2
8155 TINT0			
Ring Indicator(1)	RST 6.5	34_H	3
Carrier Detect			
Flag Interrupt	RST 5.5	$2C_H$	4
INT0/–INT7/ (1 of 8)			
RXRDY0	INTR	Programmable	5–12
TXRDY0			
RXRDY1			
TXRDY1			
RXRDY2			
TXRDY2			
RXRDY3			
TXRDY3			

NOTE:
1. Four ring indicator interrupts and four carrier detect interrupts are summed to the RST 6.5 input. The 8155 may be interrogated to inspect any one of the eight signals.

Interrupt Sources — The 22 interrupt sources originate from both on-board communications functions and the MULTIBUS. Two interrupts are routed from each of the four USARTs (8 interrupts total) to indicate that the transmitter and receiver are ready to move a data byte to or from the on-board CPU. The PIC is dedicated to accepting these 8 interrupts to optimize USART service request. One of eight interrupt request lines are jumper selectable for direct interface from a bus master via the system bus. Two auxiliary timers (TINT0 from 8155 and TINT1 from 8253) are jumper selectable to provide general purpose counter/timer interrupts. A jumper selectable Flag Interrupt is generated to allow any bus master to interrupt the iSBC 544 by writing into the base address of the shared dual port memory accessable to the system. The Flag Interrupt is then cleared by the iSBC 544 when the on-board processor reads the base address. This interrupt provides an interrupt link between a bus master and intelligent slave (see System Programming). Eight inputs from the serial ports are monitored to detect a ring indicator and carrier detect from each of the four channels. These eight interrupt sources are summed to a single interrupt level of the 8085A CPU. If one of these eight interrupts occur, the 8155 PPI can then be interrogated to determine which port caused the interrupt. Finally, a jumper selectable Power Fail Interrupt is available from the MULTIBUS to detect a power down condition.

8085 Interrupt — Thirteen of the twenty-two interrupt sources are available directly to four interrupt inputs of the on-board 8085A CPU. Requests routed to the 8085A interrupt inputs, TRAP, RST 7.5, RST 6.5 and RST 5.5 have a unique vector memory address. An 8085A jump instruction at each of these addresses then provides software linkage to interrupt service routines located independently anywhere in the Memory. All interrupt inputs with the exception of the TRAP may be masked via software.

8259A Interrupts — Eight interrupt sources signaling transmitter and receiver ready from the four USARTs are channeled directly to the Intel 8259A PIC. The PIC then provides vectoring for the next eight interrupt levels. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts transmitter and receiver interrupts from the four USARTs. It then determines which of the incoming requests is of highest priority, determines whether this request is of higher priority than the level currently being serviced, and , if appropriate, issues an interrupt to the CPU. The output of the PIC is applied directly to the INTR input of the 8085A. Any combination of interrupt levels may be masked, via software, by storing a single byte in the interrupt mask register of the PIC. When the 8085A responds to a PIC interrupt, the PIC will generate a CALL instruction for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. Interrupt response to the PIC is software programmable to a 32- or 64-byte block of memory. Interrupt sequences may be expanded from this block with a single 8085A jump instruction at each of these addresses.

Interrupt Output — In addition, the iSBC 544 board may be jumper selected to generate an interrupt from the on-board serial output data (SOD) of the 8085A. The SOD signal may be jumpered to any one of the 8 MULTIBUS interrupt lines (INT0/–INT7/) to provide an interrupt signal directly to a bus master.

Power-Fail Control

Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635 Power Supply or equivalent.

Expansion Capabilities

When the iSBC 544 board is used as a single board communications controller, memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS™ compatible expansion boards. In this mode, no other bus masters may be configured in the system. Memory may be expanded to a 65K byte capacity by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O expan-

sion boards. Furthermore, multiple iSBC 544 boards may be included in an expanded system using one iSBC 544 board as a single board communications computer and additional controllers as intelligent slaves.

System Programming

In the system programming environment, the iSBC 544 board appears as an additional RAM memory module when used as an intelligent slave. The master CPU communicates with the iSBC 544 board as if it were just an extension of system memory. Because the iSBC 544 board is treated as memory by the system, the user is able to program into it a command structure which will allow the iSBC 544 board to control its own I/O and memory operation. To enhance the programming of the iSBC 544 board, the user has been given some specific tools. The tools are: 1) the flag interrupt, 2) an on-board RAM memory area that is accessible to both an off-board CPU and the on-board 8085A through which a communications path can exist, and 3) access to the bus interrupt line.

Flag Interrupt — The Flag Interrupt is generated anytime a write command is performed by an off-board CPU to the base address of the iSBC 544 board's RAM. This interrupt provides a means for the master CPU to notify the iSBC 544 board that it wishes to establish a communications sequence. In systems with more than one intelligent slave, the flag interrupt provides a unique interrupt to each slave outside the normal eight MULTIBUS interrupt lines (INT0/–INT7/).

On-Board RAM — The on-board 16K byte RAM area that is accessible to both an off-board CPU and the on-board 8085A can be located on any 4K boundary in the system. The selected base address of the iSBC 544 RAM will cause an interrupt when written into by an off-board CPU.

Bus Access — The third tool to improve system operation as an intelligent slave is access to the MULTIBUS interrupt lines. The iSBC 544 board can both respond to interrupt signals from an off-board CPU, and generate an interrupt to the off-board CPU via the MULTIBUS.

System Development Capability

The development cycle of iSBC 544 board based products may be significantly reduced using the Intellec series microcomputer development systems. The Intellec resident macroassembler, text editor, and system monitor greatly simplify the design, development and debug of iSBC 544 system software. An optional ISIS-II diskette operating system provides a linker, object code locater, and library manager. A unique in-circuit emulator (ICE-85) option provides the capability of developing and debugging software directly on the iSBC 544 board.

SPECIFICATIONS

Serial Communications Characteristics

Synchronous — 5–8 bit characters; automatic sync insertion; parity.

Asynchronous — 5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; break character detection.

Baud Rates

Frequency (KHz)(1) (Software Selectable)	Baud Rate (Hz)(2)		
	Synchronous	Asynchronous	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

NOTES:
1. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.
2. Baud rates shown here are only a sample subset of possible software programmable rates available. Any frequency from 18.75 Hz to 614.4 KHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as a frequency divider).

8085A CPU

Word Size — 8, 16 or 24 bits/instruction; 8 bits of data

Cycle Time — 1.45/μs ±0.01% for fastest executable instruction; i.e., four clock cycles.

Clock Rate — 2.76 MHz ± 0.1%

System Access Time

Dual port memory — 740 ns

NOTE:
Assumes no refresh contention.

Memory Capacity

On-Board ROM/PROM — 4K, or 8K bytes of user installed ROM or EPROM

On-Board Static RAM — 256 bytes on 8155

On-Board Dynamic RAM (on-board access) — 16K bytes. Integrity maintained during power failure with user-furnished batteries (optional)

On-Board Dynamic RAM (MULTIBUS access) — 4K, 8K, or 16K bytes available to bus by swtich selection

Memory Addressing

On-Board ROM/PROM — 0-0FFF (using 2716 EPROMs or masked ROMs); 0-1FFF (using 2732A EPROMs)

On-Board Static RAM — 256 bytes: 7F00-7FFF

On-Board Dynamic RAM (on-board access) — 16K bytes: 8000-BFFF.

On-Board Dynamic RAM (MULTIBUS® access) — any 4K increment 00000-FF000 which is switch and jumper selectable. 4K, 8K or 16K bytes can be made available to the bus by switch selection.

I/O Capacity

Serial — 4 programmable channels using four 8251A USARTs

Parallel — 10 programmable lines available for Bell 801 ACU, or equivalent use. Two auxiliary jumper selectable signals

I/O Addressing

On-Board Programmable I/O

Port	Data	Control
USART 0	D0	D1
USART 1	D2	D3
USART 2	D4	D5
USART 3	D6	D7
8155 PPI	E9 (Port A)	E8
	EA (Port B)	
	EB (Port C)	

Interrupts

Address for 8259A Registers (Hex notation, I/O address space)

E6 Interrupt request register
E6 In-service register
E7 Mask register
E6 Command register
E7 Block address register
E6 Status (polling register)

NOTE:
Several registers have the same physical address: Sequence of access and one data bit of the control word determines which register will respond.

Interrupt levels routed to the 8085 CPU automatically vector the processor to unique memory locations:

24 TRAP
3C RST 7.5
34 RST 6.5
2C RST 5.5

Timers

Addresses for 8253 Registers (Hex notation, I/O address space)

Programmable Interrupt Timer One

D8	Timer 0	BDG0
D9	Timer 1	BDG1
DA	Timer 2	BDG2
DB	Control register	

Programmable Interrupt Timer Two

DC	Timer 0	BDG3
DD	Timer 1	BDG4
DE	Timer 2	TINT1
DF	Control register	

Address for 8155 Programmable Timer

E8	Control	
	Timer (LSB)	TINT0
ED	Timer (MSB)	TINT0

Input Frequencies — Jumper selectable reference 1.2288 MHz ± 0.1% (0.814 μs period nominal) or 1.843 MHz ±0.1% crystal (0.542 μs period, nominal)

Output Frequencies (at 1.2288 MHz)

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt Interval	1.63 μs	53.3 μs	3.26 μs	58.25 min
Rate Generator (frequency)	18.75 Hz	614.4 KHz	0.00029 Hz	307.2 KHz

Interfaces

Serial I/O — EIA Standard RS232C signals provided and supported:

Carrier Detect	Receiver Data
Clear to Send	Ring Indicator
Data Set Ready	Secondary Receive Data*
Data Terminal Ready	Secondary Transmit Data *
Request to Send	Transmit Clock
Receive Clock	Transmit Data
	DTE Transmit clock

* Optional if parallel I/O port is not used as Automatic Calling Unit.

Parallel I/O — Four inputs and eight outputs (includes two jumper selectable auxiliary outputs). All signals compatible with EIA Standard RS232C. Directly compatible with Bell Model 801 Automatic Calling Unit, or equivalent.

MULTIBUS — Compatible with iSBC MULTIBUS.

On-Board Addressing

All communications to the parallel and serial I/O ports, to the timers, and to the interrupt controller, are via read and write commands from the on-board 8085A CPU.

Auxiliary Power

An auxiliary power bus is provided to allow separate power to RAM for systems requiring battery backup of read/write memory. Selection of this auxiliary RAM power bus is made via jumpers on the board.

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 2KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or AMP 88083-1
Serial I/O	26	0.1	3M 3462-000 or AMP 88373-5

Memory Protect

An active-low TTL compatible memory protect signal is brought out on the auxiliary connector which, when asserted, disables read/write access to RAM memory on the board. This input is provided for the protection of RAM contents during the system power-down sequences.

Bus Drivers

Function	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	15
Commands	Tri-state	32

NOTE:
Used as a master in the single board communications computer mode.

Physical Characteristics

Width:	30.48 cm (12.00 inches)
Depth:	17.15 cm (6.75 inches)
Thickness:	1.27 cm (0.50 inch)
Weight:	3.97 gm (14 ounces)

Electrical Characteristics

DC Power Requirements

Configuration	Current Requirements			
	$V_{CC} = +5V \pm 5\%$ (max)	$V_{DD} = \pm 12V \pm 5\%$ (max)	$V_{BB} = -5V^{(3)} \pm 5\%$ (max)	$V_{AA} = -12V \pm 5\%$ (max)
With 4K EPROM (using 2716)	I_{CC} = 3.4A max	I_{DD} = 350 mA max	I_{BB} = 5 mA max	I_{AA} = 200 mA max
Without EPROM	3.3A max	350 mA max	5 mA max	200 mA max
RAM only(1)	390 mA max	176 mA max	5 mA max	—
RAM(2) refresh only	390 mA max	20 mA max	5 mA max	

NOTES:
1. For operational RAM only, for AUX power supply rating.
2. For RAM refresh only. Used for battery backup requirements. No RAM accessed.
3. V_{BB} is normally derived on-board from V_{AA}, eliminating the need for a V_{BB} supply. If it is desired to supply V_{BB} from the bus, the current requirement is as shown.

Environmental Characteristics

Operating Temperature: 0°C to 55°C (32°F to 131°F)

Relative Humidity: To 90% without condensation

Reference Manual

502160 — iSBC 544 Intelligent Communications Controller Board Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

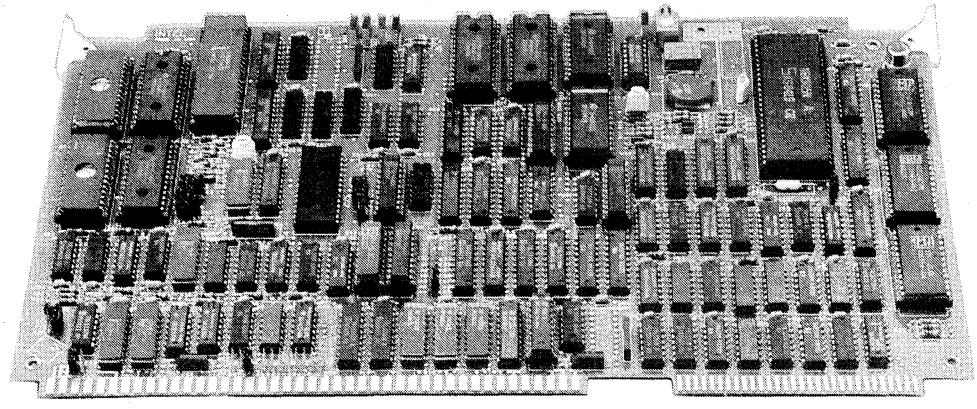
Part Number	Description
iSBC 544	Intelligent Communications Controller

iSBC® 561
SOEMI (Serial OEM Interface)
CONTROLLER BOARD

- **Dedicated I/O Controller Provides a Direct Connection of MULTIBUS®-Based Systems to an IBM 9370 or 4361 Mainframe Host or to any IBM System/370 via an IBM 3174 Subsystem Control Unit via IBM's SOEMI (Serial OEM Interface) Protocol**
- **Physical Interface is via IBM 3270 Coax with a Maximum Distance of 1.5 km**
- **Maximum Transmission Rate of 2.36 Megabits/Second**
- **Dual I/O Processors Manage Both SOEMI and MULTIBUS® Interfaces**
- **Includes a SMC-to-BNC Cable Assembly to Attach into the IBM 3270 Information Display System**
- **On-Board Diagnostic Capability Provides Operational Status of Board Function and Link with the Host**
- **Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral and Graphics Controllers' Packaging and Software**

The Intel iSBC 561 SOEMI (Serial OEM Interface) Controller Board is a member of Intel's family of single board computers, memory, I/O, peripheral and graphics controller boards. It is a dedicated intelligent I/O controller on a MULTIBUS form-factor printed circuit card. The board allows OEMs of MULTIBUS-based systems a direct, standard link to an IBM 9370 Information System, to an IBM System 4361, or to any IBM System/370 attached to an IBM 3174 Subsystem Control Unit via the SOEMI (Serial OEM Interface). The iSBC 561 Controller also provides IBM System/370 users access to the broad range of applications supported by hundreds of MULTIBUS vendors.

The SOEMI interface is comprised of an IBM System/370 programming interface and an IBM 3270 coax interface. It is a flexible, high speed, point-to-point serial interface offered as a feature on the IBM 9370 and 4361 processor families and on the 3174 Subsystem Control Unit. The iSBC 561 SOEMI Controller Board contains two processors and provides the necessary intelligence for conversion, control functions, and buffer management between the IBM mainframe and the MULTIBUS system. This board allows an IBM user to distribute control and information to MULTIBUS compatible systems for a variety of applications including factory automation, data acquisition, measurement, control, robotics, process control, communications, local area networking, medical instrumentation, and laboratory automation.



290114-1

*IBM is a trademark of International Business Machines Corp.

November 1988
Order Number: 280114-002

SOEMI INTERFACE OVERVIEW

The Serial OEM Interface (SOEMI) is a new means of connecting Original Equipment Manufacturer (OEM) MULTIBUS-based systems and subsystems to an IBM System/370 mainframe. Previously, the only low-cost way to attach non-IBM equipment into the IBM mainframe environment was to use 3270 emulation software and hardware adaptors. This type of interface is low-speed (approx. 19.6K bits/sec.) and not very flexible as to the type and format of data that can be transferred. The 3270 emulators must mimic the device formats of the displays and printers that are typically attached on this interface; stripping out command characters, carriage return andl line feed characters, etc. The SOEMI interface is available on; the IBM 9370, the IBM 4361, and the 3174 Subsystem Control Unit model 1L. The SOEMI Protocol is much faster and more flexible, in that any type of raw data or formatted data may be sent across the connecting coax cable.

The SOEMI attachment into the MULTIBUS system architecture, via the iSBC 561 SOEMI Controller Board, extends the attachment capabilities of the IBM 9370, 4361 and 3174 to a variety of systems, boards, and I/O devices provided by other manufacturers. Figure 1 is an example of the variety achievable on Intel's MULTIBUS (IEEE 796) system architecture.

The SOEMI interface utilizes the System/370 Programming Interface on the IBM 9370, 4361 and 3174 to create the protocols and formats required by a given application for connection to and communication with virtually any type of OEM device.

The System/370 Programming Interface provides the standard System/370 I/O instructions for exchanging data between the host and the MULTIBUS-based system. System/370 applications see MULTIBUS system memory as one or more entities called "spaces." The System/370 host system program writes to and reads from these spaces. The user can define the number of spaces or the layout of fields in the SOEMI interface at his discretion and as required by the application and the MULTIBUS system configuration.

The 3270 coax interface provides the physical connection between the OEM MULTIBUS system and the IBM host. The coax cable (type RG62AU) can operate over a distance of 1.5 kilometers at a maximum transfer rate of 2.3587 Mbits/second. The distance of 1.5 kilometers can be increased to a maximum of 3 kilometers by installing an IBM 3299 Terminal Multiplexer (repeater) between the IBM 9370, 4361 or 3174 and the MULTIBUS system. The protocol at the coax interface includes a polling mechanism, a set of Write and Read commands, and requires a buffer with an address register at the OEM controller end.

The connection to the IBM 4361 is made via the IBM 3270 Information Display System's Display/Printer Adapter (DPA) and/or Work Station Adapter (WSA) coax ports. The DPA can drive up to sixteen 3270/SOEMI coax ports, and is the standard configuration. The WSA is an optional add-on to the IBM 4361 that increases the total number coax ports supported to 40. The connection to the IBM 9370 is made via the Workstation Subsystem Controller feature, and a workstation adapter which can connect up to

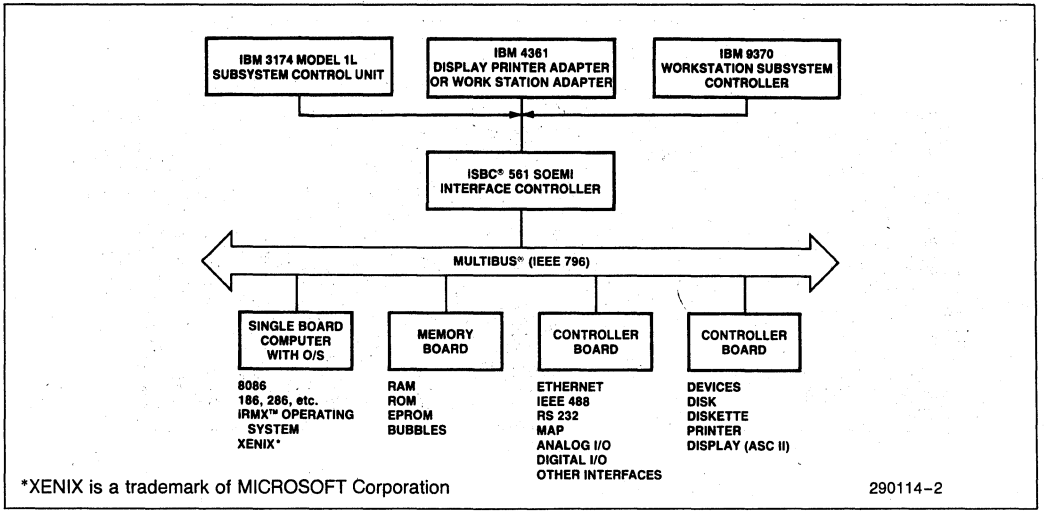


Figure 1. IBM 4361-to-MULTIBUS® Attachment Capability Block Diagram

6 SOEMI ports. This can be increased to 32 ports using optional terminal multiplexers. The connection to the IBM 3174 model 1L is made via IBM dual-purpose connectors (DPC) which can connect up to 4 SOEMI ports. This can be increased to 32 ports using terminal multiplexer adapters. A typical configuration can support an aggregate data rate of approximately 45K Bytes/second (approx. 360K bits/second).

OPERATING ENVIRONMENT

The iSBC board functions as a slave to the host mainframe, reacting and executing under System/370 program control as as mainframe resource. In addition, it has a full multimaster MULTIBUS interface that allows the board to arbitrate for bus ownership, generate bus clocks, respond to and generate interrupts, etc. With the iSBC 561 controller connected to the mainframe, all MULTIBUS system resources are available to the IBM host program/controller. From the IBM side, the mainframe is capable of accessing the entire 16 MBytes of MULTIBUS system memory, 64K Bytes of I/O space, and all on-board resources of the iSBC 561 board. Other intelligent MULTIBUS boards access iSBC 561 controller services through normal interrupt mechanisms.

Using the SOEMI interface in a relatively low-level application may simply require the user to write System/370 application control programs that reside in the IBM mainframe. A more elaborate implementation would also involve application programs that reside in the MULTIBUS system under its "native" op-

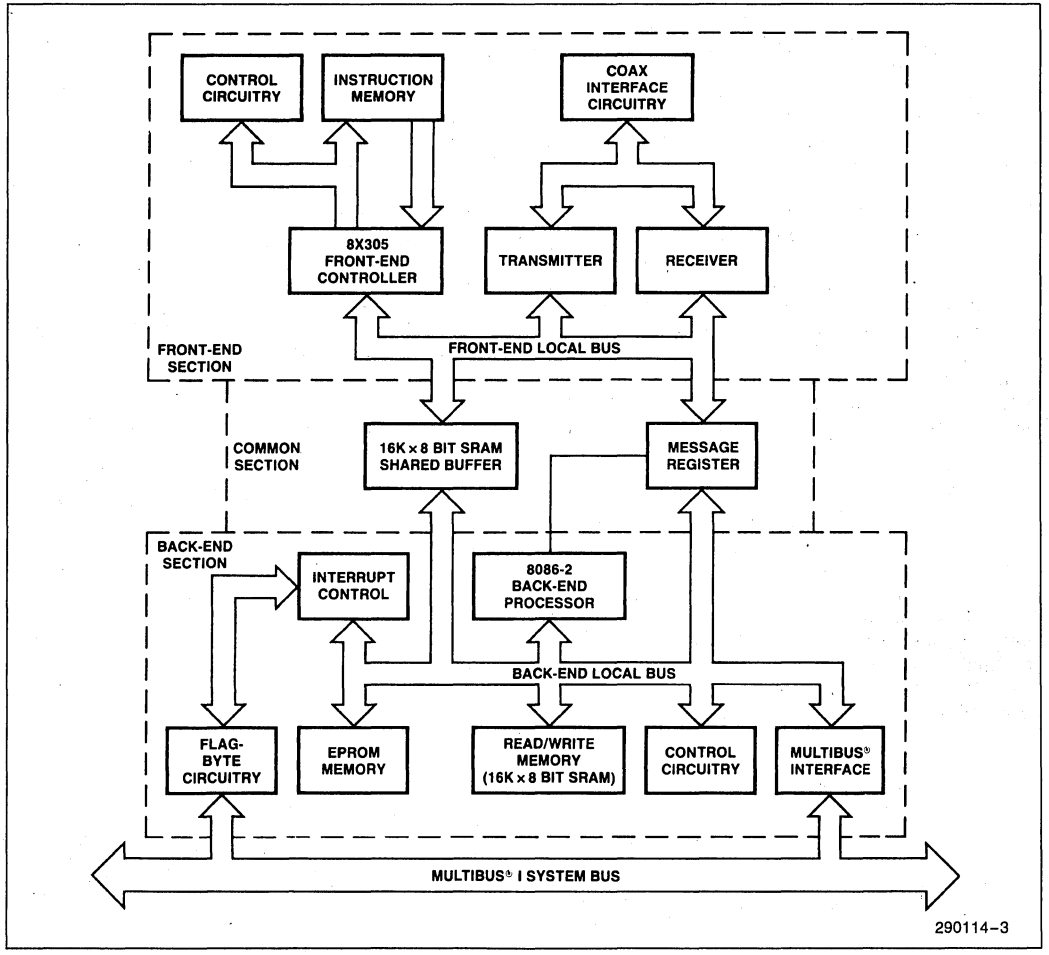


Figure 2. iSBC® 561 SOEMI (Serial OEM Interface) Controller Board Functional Block Diagram

erating environment (i.e., iRMX or XENIX operating systems) and an end-to-end protocol that ties both sets of application programs together.

ARCHITECTURE

The iSBC 561 board is functionally partitioned into three major sections: the front-end section, the common section, and the back-end section (see Figure 2).

Front-End Processor Section: IBM Host Interface

The front-end section of the iSBC 561 Controller board interfaces with the IBM mainframe via the IBM 3270 Information Display System, and consists of an 8X305 Signetics microcontroller, the 8X305 instruction memory, and the coaxial interface. The 8X305 executes the coax commands and places the structured field's instructions in shared memory buffers for subsequent execution by the back-end processor. The front-end instruction memory consists of three 2K x 8-bit PROMs which provide the instruction code for the 8X305 processor and the information needed to generate the various control signals required by the 8X305 to elicit system functions. The information contained in each PROM is not modifiable by the user. The coaxial interface is based on a DP8340 transmitter component that converts 8-bit parallel data received from the front-end processor to a 12-bit serial stream, and a DP8341 receiver component, that converts a 12-bit serial stream of data from the mainframe to parallel data with separated command and parity bits.

Common Section: Shared Memory Buffer

The common section of the iSBC 561 board consists of two 8-bit, bi-directional message registers and a 16K x 8-bit static RAM shared buffer. This shared memory buffer between the front-end processor and the back-end processor is the resource for transferring information and control messages between the IBM host and the MULTIBUS system.

Back-End Processor Section: MULTIBUS® Interface

The back-end section of the board provides an intelligent interface to the MULTIBUS system bus, and consists of the 8086-2 microprocessor, local memory, bus interface circuitry, and memory-mapped logic. The 8086 processor is capable of either retrieving information the 8X305 placed in the shared buffer, or placing information in the shared buffer, depending on the direction of the transfer and type of operation or task to be performed. The information is stored in the shared buffer as a set(s) of structured fields. The back-end processor transfers this information by performing 8- or 16-bit data transfers to or from the MULTIBUS system bus, the shared buffer, and the local memory.

The control program for this high-speed, back-end processor is resident in two local ROM sites. The processor also has access to 16K bytes of static RAM for local data storage.

The back-end section interfaces to other MULTIBUS boards through two bus controllers, a bus arbiter, and the address, data, and command buffers for access over the 24 address lines and 16 data lines of the MULTIBUS system bus.

OPERATION FLOW

The commands and information passed along the coax by the IBM host to the iSBC 561 controller represent what is known as a "structured field." The iSBC 561 front-end processor strips out the 12-bit protocol header deposits the remaining structured field(s) in the shared memory buffer, and notifies the back-end processor. The back-end processor then processes these structured fields in order to access the proper MULTIBUS memory space and I/O ports. It then deposits the information or task in the space and notifies the MULTIBUS subsystem master that a transfer has occurred and is awaiting service.

When requiring service, the MULTIBUS system application sends an interrupt to the iSBC 561 board. The board then issues an attention to the mainframe. At this point, the mainframe is under no obligation or time constraint to service the interrupt, and its response is application dependent.

The mainframe issues commands to service the interrupt. The information concerned with the interrupt is then passed through the shared memory and serialized by the iSBC 561 board before being sent to the mainframe. The exact communications protocol used for this end-to-end transfer is defined by the user application programs running in both operating environments.

Interface Connector/Cable Assembly

The cable assembly used to connect the iSBC 561 SOEMI Controller Board to the IBM mainframe or 3174 control unit cable assembly consists of RG180 type cable having an SMC connector on one end (which mates to the iSBC 561 board right angle SMC connector) and a BNC connector on the other end (which mates to the IBM cable assembly connector).

SPECIFICATIONS

Operational Characteristics

Back-end processor— Intel 8086-2/5 MHz
— 20-bit address path; 8/16 bit data path

Front-end processor— Signetics 8X305/8 MHz
— 16-bit instruction path; 8-bit data path

Serial Transfer Rate— 2.3587 Mbits/second (max. bit rate)
— 360K bits/second (approx. aggregate throughput)

Serial Transfer Rate— Binary dipulse (with 12-bit serial stream)

Memory Capacity — All iSBC 561 controller board memory is available to on-board firmware only.

Common memory — 16K Bytes of Shared Buffer memory (SRAM @ 0 wait state access)

8086-2 memory — 16K Bytes of EPROM;
— 16K Bytes of SRAM

8X305 memory — 4K Bytes of Instruction memory (EPROM)
— 2K Bytes of Control memory (EPROM)

Physical Characteristics

Width: 30.48 cm (12.00 in)
Height: 17.15 cm (6.75 in)
Depth: 1.78 cm (0.70 in)
Weight: 510 gm (18 oz)

Electrical Characteristics

DC Power Requirements:
Voltage—+5V
Current (Max)—6.28A
Current (Typ)—5.46A
Power Dissipation (Max)—35.5VA

ORDERING INFORMATION

Part Number	Description
iSBC 561	SOEMI (Serial OEM Interface) Controller board

Cable Characteristics

Impedance: coax connector—50 ohms (nominal)
external cable (user furnished)—95 ohms (nominal)

Capacitance: 35 pF/ft

Propagation: 1.6 ns/ft

Environmental Characteristics

Operating Temperature: 0° to 55°C at 200 LFM air velocity

Operating Humidity: 10 to 85% non-condensing (0° to 55°C)

Non-Operating Temperature: −40°C to 75°C

Shock: 30G for a duration of 11 ms with ½ sinewave shape.

Vibration: 0 to 55 Hz with 0.0 to 0.010 inches peak to peak excursion.

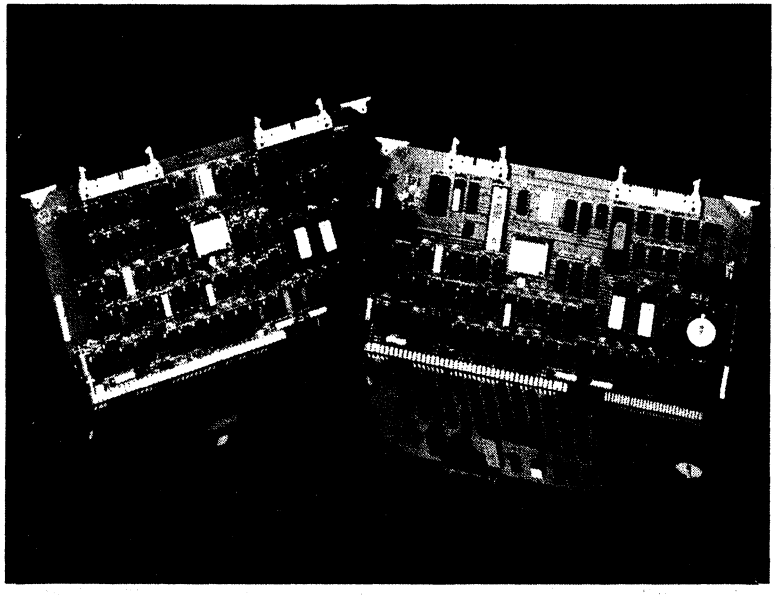
Reference Manuals

147048-001— iSBC 561 SOEMI (Serial OEM Interface) Controller Board Hardware Reference Manual (NOT SUPPLIED)

Reference manual may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

GA33-1585-0 (File No. S370-03—IBM Serial OEM Interface (SOEMI) Reference Manual (NOT SUPPLIED)

Reference manual may be ordered from IBM Advanced Technical Systems; Dept. 3291, 7030-16; Schoenaicherstr. 220; 7030 Boeblingen. Federal Republic of Germany.



HIGH PERFORMANCE TERMINAL CONTROLLER BOARDS FOR MULTIBUS®I

The iSBC 548 and iSBC 549 are intelligent terminal controllers for MULTIBUS I applications. The iSBC 548 provides basic multiuser support with 8 channels of RS 232 Asynchronous interface. The iSBC 549 combines 4 serial channels with a real-time clock and a line printer interface. Acting as intelligent slaves for communication expansion, these boards provide high performance, low cost solutions for multi-user systems.

FEATURES

iSBC 548 FEATURES

- Supports eight channels asynchronous RS232 interface

iSBC 549 FEATURES

- Supports four channels asynchronous RS232 interface
- Line printer interface
- Real-time clock/calendar with battery backup

STANDARD iSBC 548/549 FEATURES

- 8 MHz 80186 Microprocessor
- Supports transfer rates up to 19.2K Baud
- 128K Bytes Zero Wait State DRAM (32K Dual Port)
- Supports Full Duplex Asynchronous Transmissions
- Jumper selectable memory mapping, I/O mapping and MULTIBUS Interrupts

intel

September, 1988
Order Number: 280674-001

FEATURES

ASYNCHRONOUS RS232 INTERFACE SUPPORT

The iSBC 548/549 Asynchronous RS232 Internal support is presented in DTE Configuration. 82530 Serial Communications Controllers (SCCs) provide channels of half/full duplex serial I/O. Configurability of the 82530 allows handling all asynchronous data formats regardless of data size, number of start or stop bits, or parity requirements. The synchronous transmission features of the 82530 are not supported. An on-chip baud rate generator allows independent baud rates on each channel. The serial lines can be brought to the back-panel via 40-pin connectors and ribbon cable.

LINE PRINTER INTERFACE

The iSBC 549 incorporates a standard line printer interface compatible with IBM* or Centronics* line printers. Intelligent buffering on the iSBC 549 allows the CPU to offload printing tasks and return to higher priority jobs.

REAL-TIME CLOCK/CALENDAR

Multibus systems will benefit from the real-time clock present on the iSBC 549 in applications requiring time stamp operations, unattended boots and other calendar requirements. The clock/calendar circuit is backed up by a non-rechargeable battery which keeps the clock/calendar operating for six months with all other power off.

8 MHZ 80186 MICROPROCESSOR

The 80186 central processor component provides high-performance, flexibility, and powerful processing. The 80186/82530 combination with on-board PROM/EPROM sites, and dual-port RAM provides the intelligence and speed to manage multi-user communications.

TRANSFER RATES UP TO 19.2K BAUD

Collectively, each board has dual-port RAM providing an on-board buffer to handle incoming and outgoing messages at data rates up to 19.2K baud. The resident firmware supports asynchronous RS232 serial channels, provides modem control and performs power-up diagnostics. Each serial channel can be individually programmed to different baud rates to allow system configurations with differing terminal types.

*IBM is a trademark of International Business Machines.
*Centronics is a registered trademark of Centronics, Inc.

MEMORY

The iSBC 548/549 have three areas of memory on-board: dual-port RAM, private RAM, and EPROM. Each board contains 128K bytes of on-board RAM, 32K bytes of dual-port RAM can be addressed by other MULTIBUS boards. The dual port memory is configurable in a 16M byte address space on 32K byte boundaries as addressed from the MULTIBUS port. The starting address is jumper selectable.

The second area of memory is 96K bytes of private RAM which is addressable by the 80186 on-board.

The third area of memory is EPROM memory expansion. Two 28-pin JEDEC sockets are provided. These sockets come populated with two EPROMs which contain the controller firmware. The boards can support 2764, 27128 and 27256 EPROMs, giving a total capacity of 64K bytes. The EPROM runs with zero wait states if EPROMs of access times 250 ns or less are used. No jumper changes are needed to access different size EPROMs.

WORLDWIDE SERVICE AND SUPPORT

Intel provides support for board repair or on-site service. Development options include phone support, subscription service, on-site consulting, and customer training.

QUALITY AND RELIABILITY

The iSBC 548 and iSBC 549 are designed and manufactured in accordance with Intel's high quality standards. We then verify quality through rigorous testing in our state-of-the-art Environmental Test Laboratory.

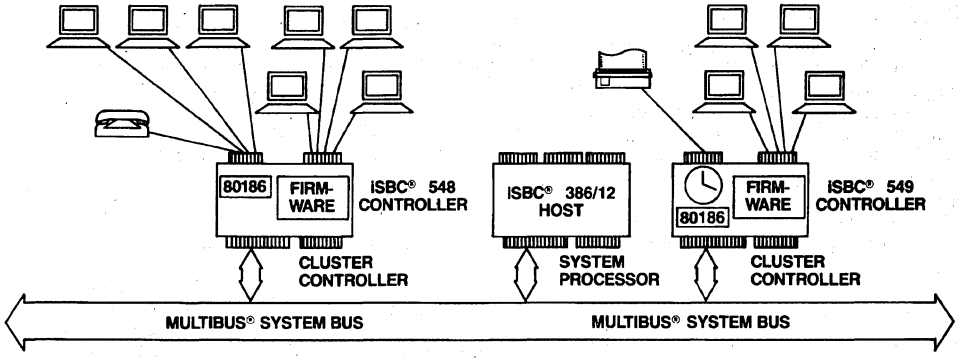


Figure 1: Terminal/Cluster Controller Application

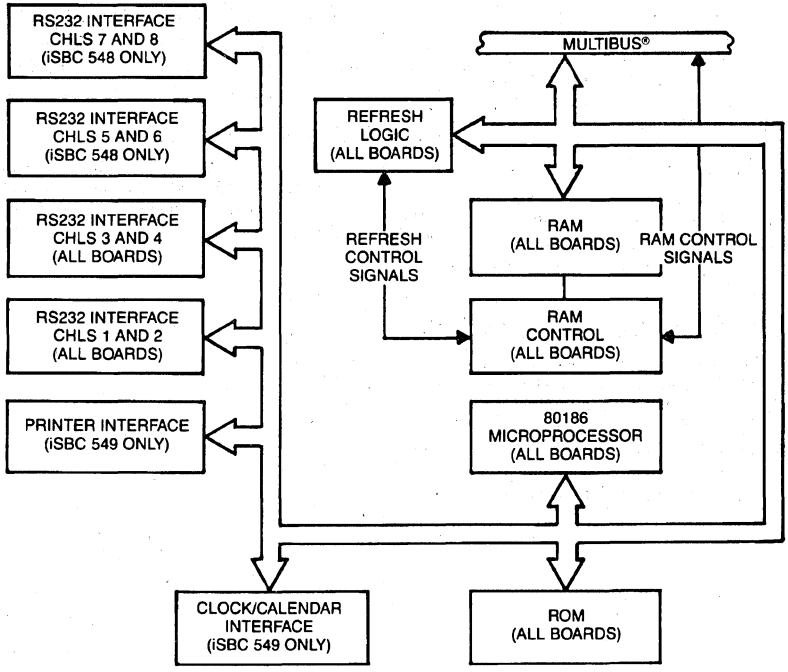


Figure 2: iSBC 548/549 Boards Block Diagram

SPECIFICATIONS

SERIAL COMMUNICATIONS CHARACTERISTICS

Asynchronous only
- 6-8 bit character length
- 1, 1½, or 2 stop bits per character
- Parity
- Programmable clock
- Break Generation
- Framing error detection

Baud Rates

The on-board firmware can automatically detect and set baud rates of 150, 300, 600, 1200, 4800, 9600 and 19200. Other baud rates can be set by the host.

Serial RS232C Signals Supported
- CD Carrier Detect
- RXD Receive Data
- TXD Transmit Data
- DTR Data Terminal Ready
- SG Signal Ground
- DSR Data Set Ready
- RTS Ready to Send
- CTS Clear to Send
- RI Ringer Indicator

These signals are supported by the iSBC 548/549 Controller and on-board firmware. All signals may not be supported by the host operating system.

MEMORY

On-Board RAM - 128K bytes total
Private RAM - 96K bytes
Dual Port RAM - 32K bytes, can be addressed from MULTIBUS interface at any 32K boundary between 80000H and F8000H or between F80000H and FF8000H.

EPROM Options -

Component	On-Board Capacity	Start Address
2764	16K	FC000H
27128	32K	F8000H
27256	64K	F000H

MULTIBUS SYSTEM BUS INTERFACE

The iSBC 548/549 boards meet MULTIBUS (IEEE 796) bus specification D16 M24 I16 V0 E.

DEVICE DRIVERS

Check the latest release of the following operating systems for details:

iRMX 86 iRMX II

ENVIRONMENTAL CHARACTERISTICS

Temperature - 0 to 55°C at 200 Linear Feet/Minute (LFM) Air Velocity
Humidity - 5% to 90% non-condensing (25 to 70°C)

PHYSICAL CHARACTERISTICS

	iSBC 548	iSBC 549
Width	30.34cm (12.00 in)	30.34cm (12.00 in)
Length	16.87cm (6.75 in)	16.87cm (6.75 in)
Height	1.27 cm (.5 in)	1.27 cm (.5 in)
Weight	400 gm (14 oz)	358 gm (12.5 oz)

POWER REQUIREMENTS

Maximum Power Required per Voltage

Voltage (Volts)	Current (Amps)	Power (Watts)
iSBC 548		
+ 5	3.49	17.5
+ 12	.14	1.7
− 12	.11	1.3
iSBC 549		
+ 5	3.26	16.3
+ 12	.07	.8
− 12	.06	.7

ORDERING INFORMATION

Part Number	Description
iSBC 548	8 Channel High Performance Terminal Controller
iSBC 549	4 Channel High Performance Terminal Controller with Line Printer/Clock

REFERENCE MANUALS

iSBC 546/547/548/549 High Performance Terminal Controller Hardware Reference Manual - Order Number 122704-002

For more information or the number of your nearest Intel sales office, call 800-548-4725 (good in the U.S. and Canada).

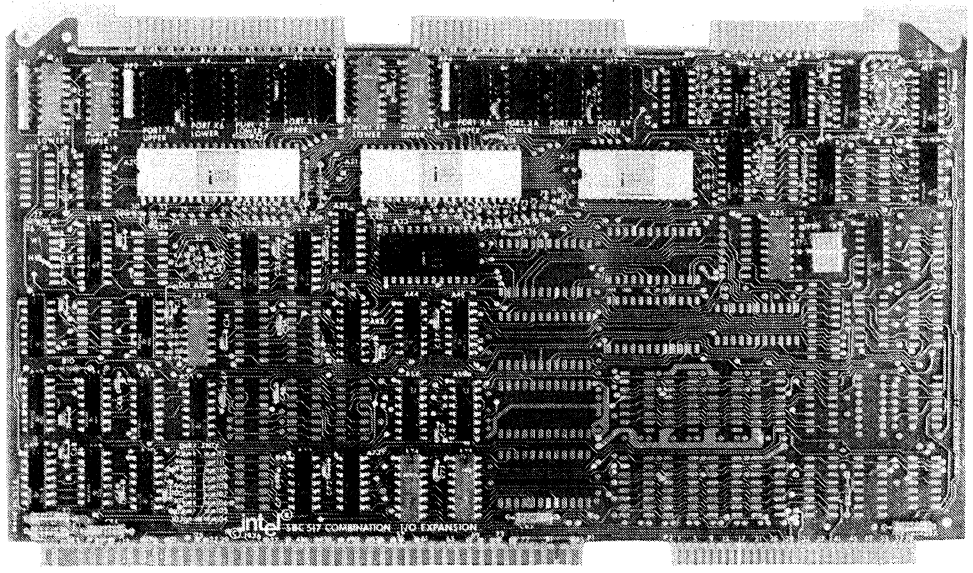
MULTIBUS® I Digital and Analog I/O Boards

7

iSBC® 517
COMBINATION I/O EXPANSION BOARD

- **48 Programmable I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **Synchronous/Asynchronous Communications Interface with RS232C Drivers and Receivers**
- **Eight Maskable Interrupt Request Lines with a Pending Interrupt Register**
- **1 ms Interval Timer**

The iSBC 517 Combination I/O Expansion Board is a member of Intel's complete line of iSBC memory and I/O expansion boards. The board interfaces directly with any iSBC single board computer via the system bus to expand serial and parallel I/O capacity. The combination I/O board contains 48 programmable parallel I/O lines. The system software is used to configure the I/O lines to meet a wide variety of system peripheral requirements. The flexibility of the I/O interface is significantly enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. A programmable RS232C communications interface is provided on the iSBC 517. This interface may be programmed by the system software to provide virtually any asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). A comprehensive RS232C interface to CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems is thus on the board. An on-board register contains the status of eight interrupt request lines which may be interrogated from the system bus, and each interrupt request line is maskable under program control. The iSBC 517 also contains a jumper selectable 1 ms interval timer and interface logic for eight interrupt request lines.



280229-1

October 1986
Order Number: 280229-001

FUNCTIONAL DESCRIPTION

Programming Flexibility

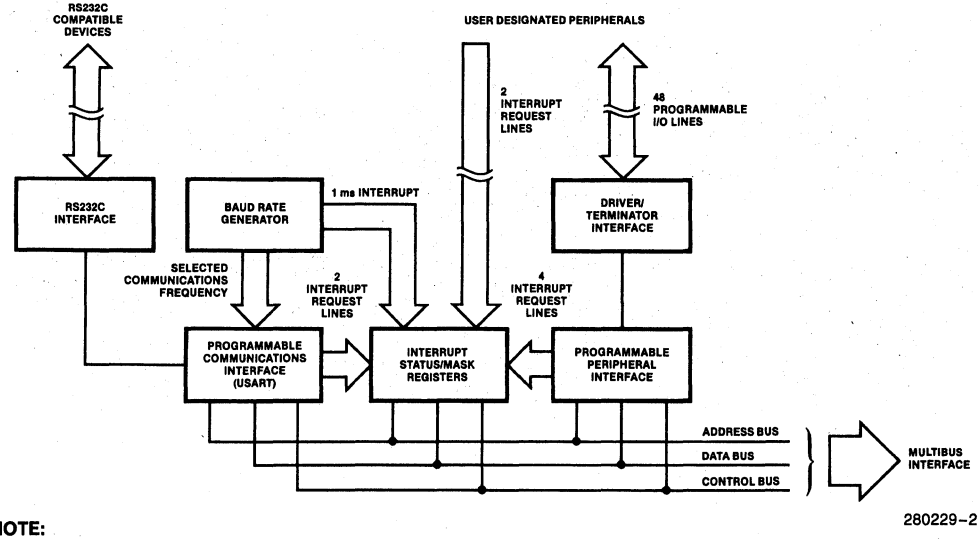
The 48 programmable I/O lines on the iSBC 517 are implemented utilizing two Intel 8255 programmable peripheral interfaces. The system software is used to configure these programmable I/O lines in any of the combinations of unidirectional input/output, and bidirectional ports indicated in Table 1. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat, round, or woven cable. Typical I/O read access time is 280 nanoseconds. Typical I/O read cycle time is 600 nanoseconds.

Communications Interface

The programmable communications interface on the iSBC 517 is provided by an Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART can be programmed by the system software to select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and asynchronous serial transmission rate are all under program control. The 8251 provides full duplex, double-buffered transmit and receive capability, and parity, overrun, and framing error detection are all incorporated in the USART. The comprehensive RS232C interface on the board provides a direct interface to RS232C compatible equipment. The RS232C serial data lines and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat or round cables.

Interrupt Request Lines

Interrupt requests may originate from eight sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a character has been transmitted (i.e., output data buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the CPU (i.e., receive buffer is full) or a character has been transmitted (transmit buffer is empty). These six interrupt request lines are all maskable under program control. Two interrupt request lines may be interfaced directly from user designated peripheral devices via the I/O edge connector. An onboard register contains the status of all eight interrupt request lines, and may be interrogated by the CPU. Each interrupt request line is maskable under program control. Routing for the eight interrupt request lines is jumper selectable. They may be ORed



NOTE:
Interrupts originating from the programmable communications interface and programmable peripheral interface are jumper selectable.

Figure 1. iSBC® 517 Combination I/O Expansion Board Block Diagram

Table 1. Input/Output Port Modes of Operation

Ports	Lines (qty)	Mode of Operation					
		Unidirectional				Bidirectional	Control
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X(1)
	4	X		X			X(1)
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X(2)
	4	X		X			X(2)

NOTES:
1. Part of port 3 must be used as control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

to provide a single interrupt request line for the iSBC 80/10B, or they may be individually provided to the system bus for use by other iSBC single board computers.

Interval Timer

Each board contains a jumper selectable 1 ms interval timer. The timer is enabled by jumpering one of the interrupt request lines from the I/O edge connector to a 1 ms interval interrupt request signal originating from the baud rate generator.

SPECIFICATIONS

I/O Addressing

Port	1	2	3	4	5	6	8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
Address	X4	X5	X6	X8	X9	XA	X7	XB	XC	XD

NOTE:
X is any hex digit assigned by jumper selection.

I/O Transfer Rate

Parallel—Read or write cycle time 760 ns max
Serial—(USART)

Frequency (kHz) (Jumper Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷16	÷64
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	—	110

Serial Communications Characteristics

Synchronous—5–8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous—5–8 bit characters; peak characters generation; 1, 1½, or 2 stop bits; false start bit detectors.

Interrupts

Eight interrupt request lines may originate from the programmable peripheral interface (4 lines), the USART (2 lines), or user specified devices via the I/O edge connector (2 lines) or interval timer.

Interrupt Register Address

X1 Interrupt mask register
X0 Interrupt status register

NOTE:
X is any hex digit assigned by jumper selection.

Timer Interval

1.003 ms ±0.1% when 110 baud rate is selected
1.042 ms ±0.1% for all other baud rates

Interfaces

Bus—All signals TTL compatible
Parallel I/O—All signals TTL compatible
Serial I/O—RS232C
Interrupt Requests—All TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	CDC VPB01E43A00A1
Parallel I/O	50	0.1	3M 3415-000 or TI H312125
Serial I/O	26	0.1	3M 3462-000 or TI H312113
Auxiliary(1)	60	0.1	AMP PE5-14559 or TI H311130

NOTE:
1. Connector heights and wire-wrap pin lengths are not guaranteed to conform to Intel OEM or system packaging. Auxiliary connector is used for test purposes only.

Line Drivers and Terminators

I/O Drivers—The following line drivers and terminators are compatible with all the I/O driver sockets on the iSBC 517:

Driver	Characteristics	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

NOTE:
I = Inverting; NI = non-inverting; OC = open-collector.

Ports 1 and 4 have 25 mA totem-pole drivers and 1 kΩ terminators.

I/O Terminators—220Ω/330Ω divider or 1 kΩ pullup

Bus Drivers

Function	Characteristics	Sink Current (mA)
Data	Tri-state	50
Commands	Tri-state	25

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 14 oz. (397.3 gm)

Electrical Characteristics

Average DC Current
V_{CC} = +5V ±5%
V_{DD} = +12V ±5%
V_{AA} = −12 ±5%
I_{CC} = 2.4 mA max
I_{DD} = 40 mA max
I_{AA} = 60 mA max

NOTE:
Does not include power required for optional I/O drivers and I/O terminators. With eight 220Ω/330Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature—0°C to +55°C

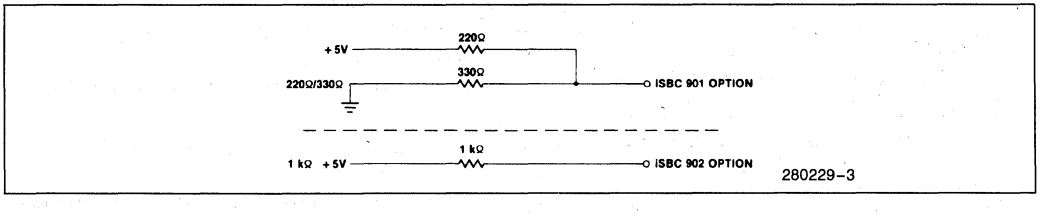
Reference Manual

9800388B—iSBC 517 Hardware Reference manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

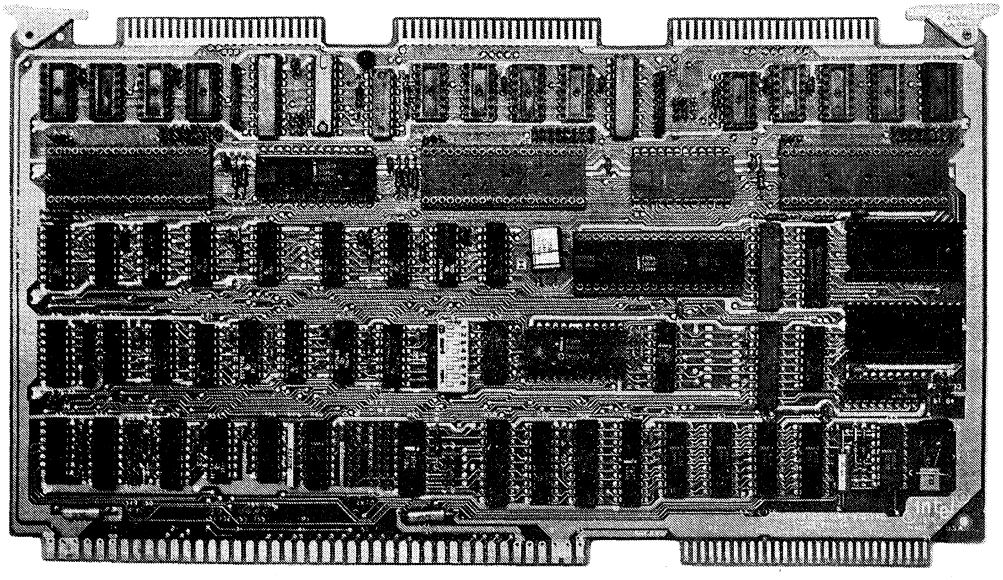
Part Number	Description
SBC 517	Combination I/O Expansion Board



iSBC® 569
INTELLIGENT DIGITAL CONTROLLER

- **Single Board Digital I/O Controller with up to Four Microprocessors to Share the Digital Input/Output Signal Processing**
- **3 MHz 8085A Central Control Processor**
- **Three Sockets for 8041/8741A Universal Peripheral Interface (UPI-41A) for Distributed Digital I/O Processing**
- **Three Operational Modes**
  - **— Stand-Alone Digital Controller**
  - **— MULTIBUS® Master**
  - **— Intelligent Slave (Slave to MULTIBUS Master)**
- **2K Bytes of Dual Port Static Read/Write Memory**
- **Sockets for up to 8K Bytes of Intel 2758, 2716, 2732 Erasable Programmable Read Only Memory**
- **48 Programmable Parallel I/O Lines with Sockets for Interchangeable Line Drivers or Terminators**
- **Three Programmable Counters**
- **12 Levels of Programmable Interrupt Control**
- **Single +5V Supply**
- **MULTIBUS Standard Control Logic Compatible with Optional iSBC 80 and iSBC® 86 CPU, Memory, and I/O Expansion Boards**

The Intel iSBC® 569 Intelligent Digital Controller is a single board computer (8085A based) with sockets for three 8041A/8741A Universal Peripherals Interface chips (UPI-41A). These devices, which are programmed by the user, may be used to offload the 8085A processor from time consuming tasks such as pulse counting, event sensing and parallel or serial digital I/O data formatting with error checking and handshaking. The iSBC 569 board is a complete digital controller with up to four processors on a single 6.75 inches x 12.00 inches (17.15 cm x 30.48 cm) printed circuit board. The 8085A CPU, system clock, read/write memory, non-volatile memory, priority interrupt logic, programmed timers, MULTIBUS control and interface logic, optional UPI processors and optional line driver and terminators all reside on one board.



280232-1

October 1986
Order Number: 280232-001

FUNCTIONAL DESCRIPTION

Intelligent Digital Controller

Three Modes of Operation—The iSBC 569 Intelligent Digital Controller is capable of operating in one of three modes; stand alone controller, bus master, or intelligent slave.

Stand Alone Controller—The iSBC 569 board may function as a stand alone, single board controller with CPU, memory, and I/O elements on a single board. Five volt (+5VDC) only operation allows configuration of low cost controllers with only a single power supply voltage. The on-board 2K bytes RAM and up to 16K bytes ROM/EPROM, as well as the assistance of three UPI-41A processors, allow significant digital I/O control from a single board.

Bus Master—In this mode of operation, the iSBC 569 controller may interface with and control iSBC expansion memory and I/O boards, or even other iSBC 569 Intelligent Digital Controllers configured as intelligent slaves (but no additional bus masters).

Intelligent Slave—The iSBC 569 controller can perform as an intelligent slave to any 8- or 16-bit MULTIBUS master CPU by offloading the master of digital control related tasks. Preprocessing of data for the master is controlled by the on-board 8085A CPU which coordinates up to three UPI-41A processors.

Using the iSBC 569 board as an intelligent slave, multi-channel digital control can be managed entirely on-board, freeing a system master to perform other system functions. The dual port RAM memory allows the iSBC 569 controller to process and store data without MULTIBUS memory contention.

Simplified Programming

By using Intel UPI-41A processors for common tasks such as counting, sensing change of state, printer control and keyboard scanning/debouncing, the user frees up time to work on the more important application programming of machine or process optimization. Controlling the Intel UPI-41A processors becomes a simple task of reading or writing command and data bytes to or from the data bus buffer register on the UPI device.

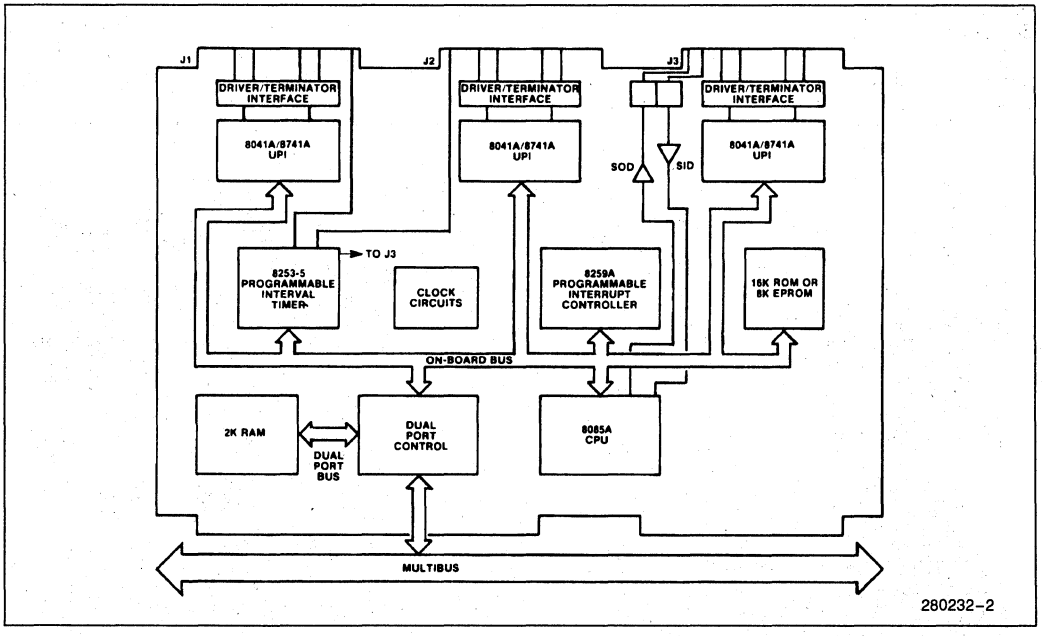


Figure 1. iSBC® 569 Intelligent Digital Controller Block Diagram

Central Processing Unit

A powerful Intel 8085A 8-bit CPU, fabricated on a single LSI chip, is the central processor for the iSBC 569 controller. The six general purpose 8-bit registers may be addressed individually or in pairs, providing both single and double precision operations. The program counter can address up to 64K bytes of memory using iSBC expansion boards. The 16-bit stack pointer controls the addressing of an external stack. This stack provides sub-routine nesting bounded only by memory size. The minimum instruction execution time is 1.30 microseconds. The 8085A CPU is software compatible with the Intel 8080A CPU.

Bus Structure

The iSBC 569 Intelligent Digital Controller utilizes a triple bus architecture concept. An internal bus is used for on-board memory and I/O operations. A MULTIBUS interface is available to provide access for all external memory and I/O operations. A dual port bus with controller enables access via the third bus to 2K bytes of static RAM from either the on-board CPU or a system master. Hence, common data may be stored in on-board memory and may be accessed either by the on-board CPU or by system masters. A block diagram of the iSBC 569 functional components is shown in Figure 1.

RAM Capacity

The iSBC 569 board contains 2K bytes of read/write memory using Intel 2114 static RAMs. RAM accesses may occur from either the iSBC 569 controller or from any other bus master interfaced via the MULTIBUS system bus. The iSBC 569 board provides addressing jumpers to allow the on-board RAM to reside within a one megabyte address space when accessed via the system bus. In addition, a switch is provided which allows the user to reserve a 1K byte segment of on-board RAM for use by the 8085A CPU. This reserved RAM space is not accessible via the system bus and does not occupy any system address space.

EPROM/ROM Capacity

Two sockets for up to 16K bytes of nonvolatile read only memory are provided on the iSBC 569 board. Nonvolatile memory may be added in 1K byte increments up to a maximum of 2K bytes using Intel 2758 erasable and electrically reprogrammable ROMs (EPROMs); in 2K byte increments up to a maximum of 4K bytes using Intel 2316 ROMs or 2716 EPROMs; in 4K byte increments up to 8K bytes maximum using Intel 2732 EPROMs; or in 8K byte increments up to 16K bytes maximum using Intel 2364 ROMs (both sockets must contain same type ROM/EPROM). All on-board ROM/EPROM operations are performed at maximum processor speed.

Universal Peripheral Interfaces (UPI-41A)

The iSBC 569 Intelligent Digital Controller board provides three sockets for user supplied Intel 8041A/8741A Universal Peripheral Interface (UPI-41A) chips. Sockets are also provided for the associated line drivers and terminators for the UPI I/O ports. The UPI-41A processor is a single chip microcomputer containing a CPU, 1K byte of ROM (8041A) or EPROM (8741A), 64K bytes of RAM, 16 programmable I/O lines, and an 8-bit timer/event counter. Special interface registers included in the chip allow the UPI-41A processor to function as a slave processor to the iSBC 569 controller board's 8085A CPU. The UPI processor allows the user to specify algorithms for controlling peripherals directly thereby freeing the 8085A for other system functions. For additional information, including UPI-41A instructions, refer to the UPI-41 User's Manual (Manual No. 9800504).

Programmable Timers

The iSBC 569 Intelligent Digital Controller board provides three independently programmable interval timer/counters utilizing one Intel 8253 Programmable Interval Timer (PIT). The Intel 8253 PIT provides three 16-bit BCD or binary interval timer/counters. Each timer may be used to provide a time reference for each UPI™ processor or for a group of UPI processors. The output of each timer also connects to the 8259A Programmable Interrupt Controller (PIC) providing the capability of timed interrupts. All gate inputs, clock inputs, and timer outputs of the 8253 PIT are available at the I/O ports for external access.

Timer Functions—In utilizing the iSBC 569 controller, the systems designer simply configures, via software, each timer to meet systems requirements. The 8253 PIT modes are listed in Table 1. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications. The contents of each counter can be read "on-the-fly" for time stamping events or time clock referenced program initiations.

Table 1. 8253 Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N counts occur in the system.

Interrupt Capability

The iSBC 569 Intelligent Digital Controller provides interrupt service for up to 12 interrupt sources. Any of the 12 sources may interrupt the on-board processor. Four interrupt levels are handled directly by the 8085A CPU and eight levels are serviced from an Intel 8259A Programmable Interrupt Controller (PIC) routing an interrupt request output to the INTR input of the 8085A.

8085A Interrupt—Each of four direct 8085A interrupt inputs has a unique vector memory address. An 8085A jump instruction at each of these addresses then provides software linkage to interrupt service routines located independently anywhere in the memory.

8259A Interrupts—The eight interrupt sources originate from both on-board controller functions and the system bus:

UPI-41A Processors—One interrupt from each of three UPI processor sockets.

8253 PIT—One interrupt from each of three outputs.

MULTIBUS System Bus—one of eight MULTIBUS interrupt lines may be jumpered to either of two 8259A PIC interrupt inputs.

Programmable Reset—The iSBC 569 Intelligent Digital Controller board has a programmable output latch used to control on-board functions. Three of the outputs are connected to separate UPI-41A RESET inputs. Thus, the user can reset any or all of the UPI-41A processors under software control. A fourth latch output may be used to generate an interrupt request onto the MULTIBUS interrupt lines. A fifth latch output is connected to a light-emitting diode which may be used for diagnostic purposes.

Expansion Capabilities

When the iSBC 569 controller is used as a single board digital controller, memory and I/O capacity may be expanded using Intel MULTIBUS compatible expansion boards. In this mode, no other bus masters may be in the system. Memory may be expanded to a 64K byte capacity by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be increased by adding I/O expansion boards. Multiple iSBC 569 boards may be included in an expanded system using one iSBC 569 Intelligent Digital Controller as the system master and additional controllers as intelligent slaves.

Intelligent Slave Programming

When used as an intelligent slave, the iSBC controller appears as an additional RAM memory module. System bus masters communicate with the iSBC 569 boards as if it were just an extension of system memory. To simplify this communication, the user has been given some specific tools:

Flag Interrupt—The Flag Interrupt is generated any time a write command is performed by an off-board CPU to the first location of iSBC 569 RAM. This interrupt provides a means for the master CPU to notify the iSBC 569 controller that it wished to establish a communications sequence. The flag interrupt is cleared when the on-board processor reads the first location of its RAM. In systems with more than one intelligent slave, the flag interrupt provides a unique

interrupt to each slave outside the normal MULTIBUS interrupt lines (INT0/-INT7/).

RAM—The on-board 2K byte RAM area that is accessible to both an off-board CPU and the on-board 8085A may be configured for system access on any 2K boundary.

MULTIBUS® Interrupts—The third tool to improve system operation as an intelligent slave is access to the MULTIBUS interrupt lines. The iSBC 569 controller can both respond to interrupt signals from an off-board CPU, and generate an interrupt to the off-board CPU via the system bus.

System Development Capability

Software development for the iSBC 569 Intelligent Digital Controller board is supported by the Intellec® Microcomputer Development System including a resident macroassembler, text editor, system monitor, a linker, object code locator, and Library Manager. In addition, both PL/M AND FORTRAN language programs can be compiled to run on the iSBC 569 board. A unique incircuit emulator (ICE-85™) option provides the capability of developing and debugging software directly on the iSBC 569 board. This greatly simplifies the design, development, and debug of iSBC 569 system software.

SPECIFICATIONS

8085A CPU

Word Size: 8, 16 or 24 bits

Cycle Time: 1.30 μs ±0.1% for fastest executable instruction; i.e., four clock cycles.

Clock Rate: 3.07 MHz ±0.1%

System Access Time

Dual port memory—725 ns

Memory Capacity

On-board ROM/EPROM—2K, 4K, 8K, or 16K bytes of user installed ROM or EPROM.

On-board RAM—2K bytes of static RAM. Fully accessible from on-board 8085A. Separately addressable from system bus.

Off-board expansion—up to 64K bytes of EPROM/ROM or RAM capacity.

I/O Capacity

Parallel-Timers—Three timers, with independent gate input, clock input, and timer output user-accessible. Clock inputs can be strapped to an external source or to an on-board 1.3824 MHz reference. Each timer is connected to a 8259A Programmable Interrupt Controller and may also be optionally connected to UPI processors.

UPI-I/O—Three UPI-41A interfaces, each with two 8-bit I/O ports plus the two UPI Test Inputs. The 8-bit ports are user-configurable (as inputs or outputs) in groups of four.

Serial—1 TTL compatible serial channel utilizing SID and SOD lines of on-board 8085A CPU.

On-Board Addressing

All communications to the UPI-41A processors, to the programmable reset latch, to the timers, and to the interrupt controller are via read and write commands from the on-board 8085A CPU.

Memory Addressing

On-board ROM/EPROM—0-07FF (using 2758 EPROMs); 0-OFFF (using 2716 EPROMs or 2316 ROMs); 0-1FFF (using 2732 EPROMs); 0-3FFF (using the 2364 ROMs)

On-board RAM—8000-87FF System access—any 2K increment 00000-FF800 (switch selection); 1K bytes may be disabled from bus access by switch selection.

I/O Addressing

Source	Addresses
8253	0E0H-0E3H
UPI0	0E4H-0E5H
UPI1	0E6H-0E7H
UPI2	0E8H-0E9H
PROGRAMMABLE RESET	0EAH-0EBH
8259A	0ECH-0EDH

Timer Specifications

Input Frequencies—jumper selectable reference

Internal: 1.3824 MHz ±0.1% (0.723 μs, nominal)
External: User supplied (2 MHz maximum)

Output Frequencies (at 1.3824 MHz)

Function	Min[1]	Max[1]
Real-time interrupt interval	1.45 μsec	47.4 msec
Rate Generator (frequency)	21.09 Hz	691.2 KHz
1. Single 16-bit binary count		

Interfaces

MULTIBUS™ Interface—All signals compatible with iSBC and MULTIBUS architecture

Parallel I/O—All signals TTL compatible

Interrupt Requests—All TTL compatible

Timer—All signals TTL compatible

Serial I/O—All signals TTL compatible

Connectors

Interface	Pins (qty)	Centers (in.)	Mating Connectors
Bus	86	0.156	Viking 3KH43/9AMK12
Parallel I/O	50	0.1	3M 3415-000 or TI H312125

Physical Characteristics

Width: 30.48 cm (12.00 inches)

Depth: 17.15 cm (6.75 inches)

Thickness: 1.27 cm (0.50 inch)

Weight: 3.97 gm (14 ounces)

Electrical Characteristics

DC Power Requirements—+5V @ 2.58A with no optional devices installed. For each 8741A add 135 mA. For each 220/330 resistor network, add 60 mA. Add the following for each EPROM/ROM installed.

Type	+5.0V Current Requirement	
	1ROM	2ROM
2758	100 mA	125 mA
2716	100 mA	125 mA
2316E	120 mA	240 mA
2732	40 mA	55 mA
2364	40 mA	55 mA

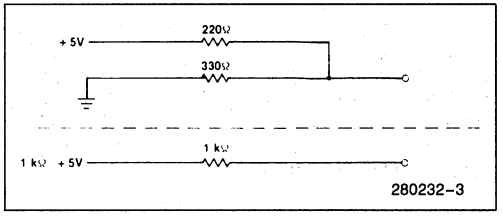
Line Drivers and Terminators

I/O /Drivers—The following line drivers are all compatible with the I/O driver sockets on the iSBC 569 Intelligent Digital Controller.

Driver	Characteristics	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

NOTE:
I = inverting; NI = non-inverting; OC = open collector.

I/O Terminators—220Ω/330Ω divider or 1 kΩ pull-up (DIP) - user supplied



Environmental Characteristics

Operating Temperature: 0° C to 55° C (32° F to 131 °F)

Relative Humidity: To 90% without condensation

Reference Manual

502180—iSBC 569 Intelligent Digital Controller Board Hardware Reference Manual (NOT SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 569	Intelligent Digital Controller

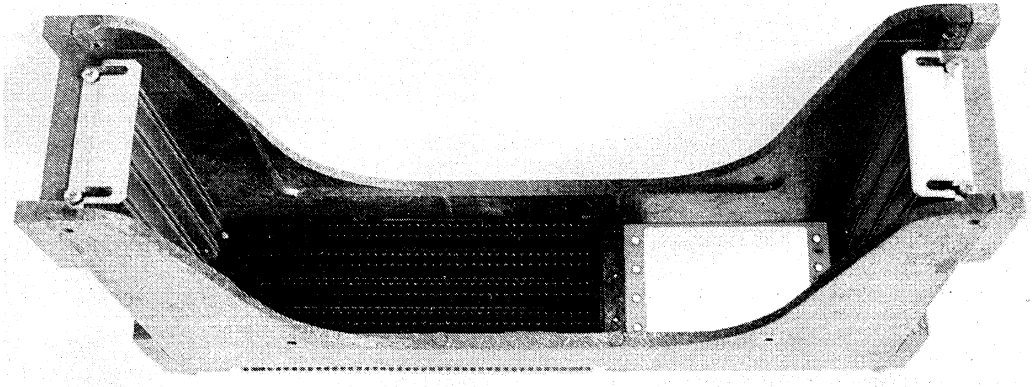
MULTIBUS® I System Packaging and Power Supplies

8

iSBC® 604/614
MODULAR CARDCAGE ASSEMBLIES

- **Interconnects and Houses up to Four MULTIBUS® Boards per Cardcage**
- **Connectors Allow Interconnection of up to Four Cardcage Assemblies for 16 Board Systems**
- **Strong Cardcage Structure Helps Protect Installed Boards from Warping and Physical Damage**
- **Cardcage Mounting Holes Facilitate Interconnection of Units**
- **Compatible with 3.5-Inch RETMA Rack Mount Increments**
- **Interleaved Grounds on Backplane Minimize Noise and Crosstalk**
- **Up to 3 CPU Boards per System for Multiprocessing Applications**

The iSBC 604 and iSBC 614 Modular Cardcage Assemblies units provide low-cost, off-the-shelf housing for OEM products using two or more MULTIBUS boards. Each unit inerconnects and houses up to four boards. The base unit, the iSBC 604 Cardcage Assembly, contains a male backplane PC edge connector and bus signal termination circuits, plus power supply connectors. It is suitable for applications requiring a single unit, or may be interconnected with up to three iSBC 614 cardcage assemblies for a four cardcage (16 board) system. The iSBC 614 contains both male and female backplane connectors, and may be interconnected with iSBC 604/614 units. Both units are identical, with the exception of the bus signal terminator feature. A single unit may be packaged in a 3.5 inch RETMA rack enclosure, and two interconnected units may be packaged in a 7 inch enclosure. The units are mountable in any of three planes.



280205-1

September 1986
Order Number: 280205-001

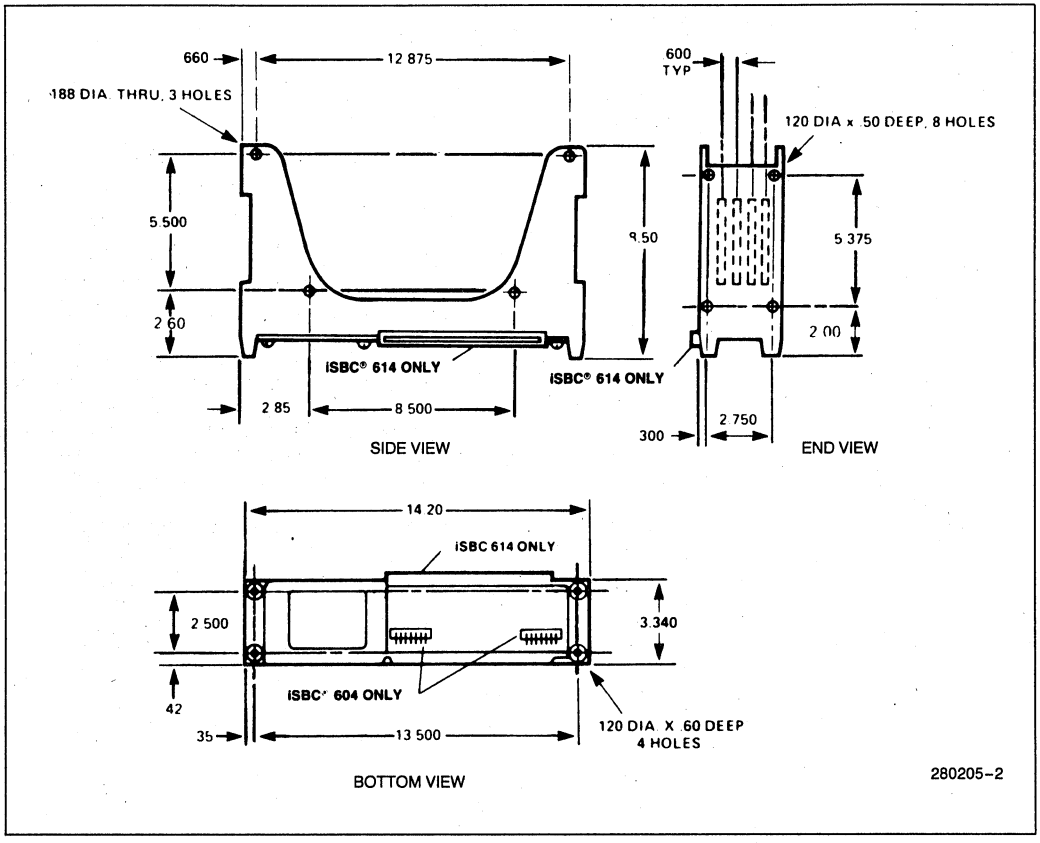


Figure 1. iSBC® 604/614 Cardcage Assembly Dimensions

SPECIFICATIONS

Backplane

Bus Lines—All MULTIBUS system bus address, data, and command bus lines are bussed to all four connectors on the printed circuit backplane

Power Connectors—G for ground, +5, −5, +12V, −12V, and −10V power supply lines

iSBC 604—Bus signal terminators, backplane male PC edge connector only, and power supply headers

iSBC 614—Backplane male and female connectors and power supply headers

Mating Power Connectors

AMP	Connector	87159-7
	Pin	87023-1
	Polarizing Key	87116-2
Molex	Connector	09-50-7071
	Pin	08-50-0106
	Polarizing Key	15-04-0219

NOTE:
1. Pins from a given vendor may only be used with connectors from the same vendor.

ORDERING INFORMATION

Part Number	Description
SBC 604	Modular Cardcage Assembly (Base Unit)

Bus Arbitration: Serial; up to 3 CPU masters

Equipment Supplied: iSBC 604 or iSBC 614 Cardcage Schematic

Physical Dimensions

Height: 8.5 in. (21.59 cm)

Width: 14.2 in. (36.07 cm)

Depth: 3.34 in. (8.48 cm)

Weight: 35 oz. (992.23 gm)

Card Slot Spacing: 0.6 in.

Environmental Characteristics

Operating Temperature: 0°C to 55°C

Reference Manual

9800708—iSBC 604/614 Cardcage Hardware Reference Manual (ORDER SEPARATELY)

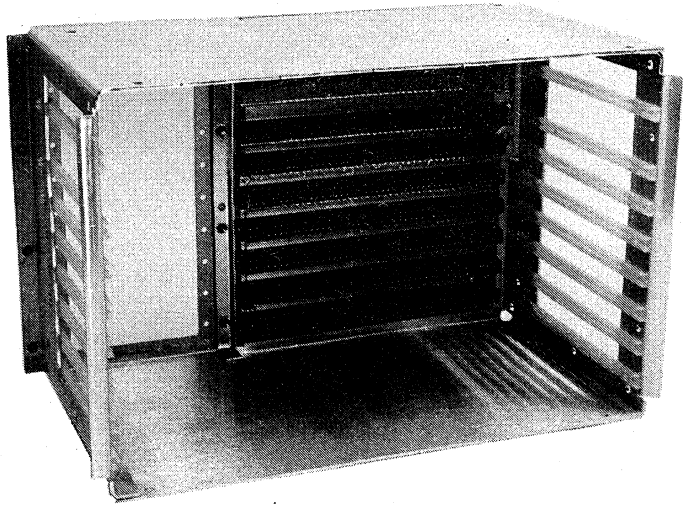
Part Number	Description
SBC 614	Modular Cardcage Assembly (Expansion Unit)

iSBC® 608/618 CARDCAGES

- **Houses Eight MULTIBUS® iSBC® Boards in an Aluminum Package**
- **Board-to-Board Clearance for iSBC® MULTIMODULE™ Boards on All Slots**
- **Board-to-Board Clearance for iSBX™ MULTIMODULE™ Boards on Two Slots**
- **Parallel Priority Circuitry for up to Eight Multimaster iSBC® Boards**
- **Enhanced Bus Noise Immunity for High Speed Systems**
- **Plug on iSBC 618 Unit for up to Sixteen Board Systems**
- **NEMA-Type Backwall or 19-Inch Rack Mount Hardware Included**
- **Signal Line Termination Circuitry on iSBC® 608 Cardcage**

Intel's iSBC 608/618 Cardcages are matched to the latest generation of iSBC/iSBX boards which mount in the MULTIBUS system bus. These products provide several features which make them the industry's leading price/performance cardcage product. MULTIMODULE board clearance, parallel priority circuitry, enhanced backplane noise immunity, and precision fit card guides are a few of the distinctions which make this the industry's better product.

The iSBC 608 Cardcage is the base unit, housing up to eight iSBC boards and their MULTIMODULE boards. Additionally, this base unit includes mounting hardware and fan mounting bracketry. The iSBC 618 is the expansion unit, providing eight additional iSBC board slots to the iSBC 608 Cardcage for a total of sixteen board slots which can be NEMA-type backwall or 19-inch rack mounted. This is accomplished with the mounting hardware of the iSBC 608 Cardcage. The iSBC 618 expansion unit also includes fan mounting bracketry.



210373-1

November 1986
Order Number: 210373-001

FUNCTIONAL DESCRIPTION

Mechanical Aspects

The iSBC 608/618 Cardcages provide housing and a MULTIBUS system bus for up to sixteen single board computers and their MULTIMODULE boards. The iSBC 608 unit and iSBC 618 unit offer board-to-board clearance (0.8 inches or greater) on all eight slots for iSBC MULTIMODULE boards. Two slots provide clearance (1.2 inches or greater) for iSBX MULTIMODULE boards as shown in Figure 1. Each cardcage includes precision fitted nylon cardguides for secure board fit and accurate MULTIBUS board pin alignment. Fan mounting bracketry is also included with each cardcage. This bracketry allows the mounting of several industry standard fans. The iSBC 608 Cardcage base unit includes aluminum mounting hardware for NEMA-type backwall mounting, or anchoring a sixteen slot iSBC 608/618 combination in a standard 19-inch rack.

Electrical Aspects

The iSBC 608/618 Cardcages implement a parallel priority resolution scheme by using plug-in jumper connections. There are six different priority schemes allowed, each requiring a different jumper configuration. In systems where an iSBC 618 Cardcage is attached to the base unit, the base unit will have lower priority overall. That is, master boards in the iSBC 608 base unit bay gain control of the MULTIBUS lines only when no boards in the iSBC 618 expansion unit are asserting the bus request (BREQ/) signal.

Noise-minimizing ground traces are strategically interleaved between signal and address lines on these backplanes. This provides the enhanced noise immunity and minimized signal-to-signal coupling which is important in high speed, high board count microcomputer systems.

The iSBC 608/618 Cardcages provide power connector lug bolts for +5 VDC and ground. The lug bolts, compared to other power connection methods, help transfer higher amounts of current. Other voltages (±12 VDC, −5 VDC) are connected via a mating power connector plug as shown in Figure 2.

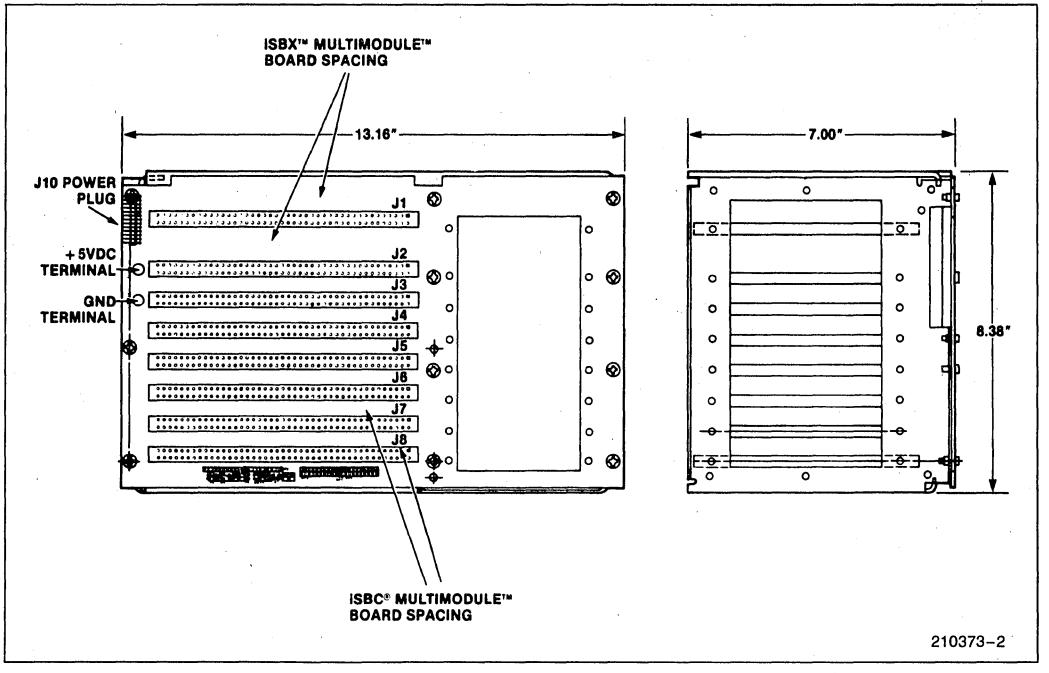


Figure 1. iSBC® 608/618 Cardcages Dimensions

SPECIFICATIONS

Bus Lines

All MULTIBUS (IEEE 796) system bus address and command lines are bussed to each of the eight MULTIBUS connectors on the backplane. Ground traces are interleaved among these signal lines and bussed to the backplane edge connector for interconnection of the iSBC 608 and iSBC 618 backplane.

Power Connectors

Ground (0V), +5V, −5V, +12V, −12V power supply header stakes and power lug bolts are provided on the iSBC 608/618 Cardcages as shown in Figure 2.

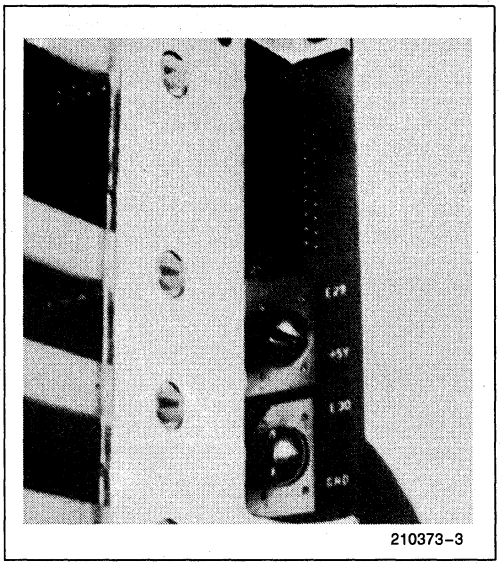


Figure 2. Power Header Stakes and Lugs

Environmental Characteristics

Operating Temperature:	0°C to 55°C
Storage Temperature:	−40°C to +85°C
Humidity:	50% to 95% non-condensing at 25°C to 40°C.
Vibration and Shock:	2G max. through 50 Hz

Physical Characteristics

SLOT-TO-SLOT DIMENSIONS (See Figure 1)

Top-J1:	1.200 in. (to center)
J1-J2:	1.300 in. (center to center)
J8-Bottom:	0.700 in. (to center)
All Others:	0.800 (center to center)

Physical Dimensions

Height:	8.38 in. (21.29 cm)
Length:	13.16 in. (33.43 cm)
Width:	7.50 in. (19.05 cm)
Weight:	3.50 lbs (1.59 kg)
Shipping Weight:	5.75 lbs (2.61 kg)

Equipment Supplied

iSBC® 608 BASE UNIT

Eight Slots:	Two at greater than 1.2 inches; six at 0.8 inches
Male Backplane Connector:	For expansion with iSBC 618 cardcage
Parallel Priority Circuitry:	Eight slots are configurable via the use of jumper stakes. Six priority schemes allowed
Construction Materials:	Aluminum card housing
	Nylon card guides
	Power connector header stakes and lug bolts

Accessories

iSBC® 618 EXPANSION UNIT

Eight-Slots:	Two at greater than 1.2 inches; six at 0.8 inches
Female Backplane Connector:	For expansion to iSBC 608 base unit
Parallel Priority Circuitry:	Eight slots are configurable via the use of jumper stakes. Six priority schemes allowed.
Construction Materials:	Aluminum card housing
	Nylon card guides
	Power connector header stakes and lug bolts
	Fan Mounting Hardware
	Schematic

User-Supplied Equipment

MATING POWER CONNECTORS

Vendor	Part Number
3M	3399-6026
Ansley	609-2600M
Berg	65485-009

MOUNTABLE FANS

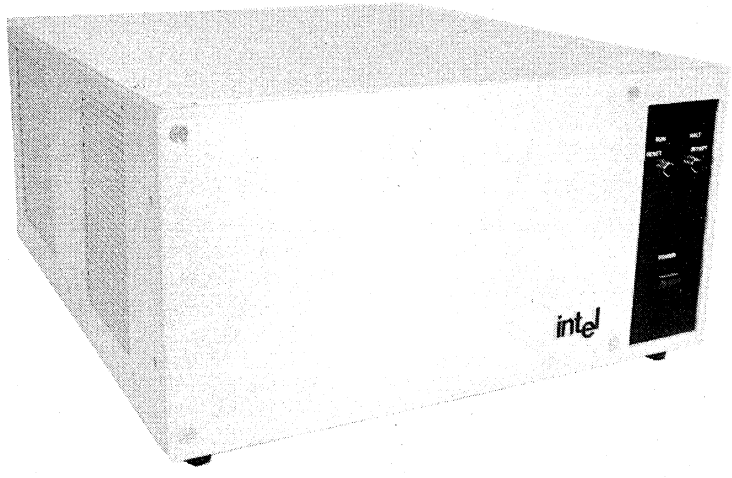
Vendor	Part Number
Rotron	SU2A1-028267
Torin	TA300-A30473-10
Pamotor	8506D

iSBC® 661
SYSTEM CHASSIS

- **Eight-Slot MULTIBUS® Chassis with Parallel Priority Circuitry**
- **UL, FCC and CSA Approved for Data Processing Equipment**
- **230 Watt Power Supply with Power Fail Warning**
- **Designed for Slide Rack Mounting or Table-Top Use**
- **Extra-Wide Cardcage Slot Spacing for iSBX™ MULTIMODULE™ Board Clearance**
- **Configurable for Front or Rear Access to MULTIBUS® Circuit Boards**
- **Five Connector Ports for I/O Cabling**
- **Operational from 47 Hz to 63 Hz, 100/120/220/240 VAC ±10%**

The iSBC 661 System Chassis is an advanced MULTIBUS (IEEE) 796 chassis which incorporates unique usability and service features not found on competitive products. This chassis is designed or rack-mount or table-top applications and reliably operates up to an ambient temperature of 50°C. Additionally, this sytem chassis is certified by UL, CSA and FCC for data processing equipment.

An application requiring multiprocessing will find this eight-slot MULTIBUS chassis particularly well suited to its needs. Parallel priority bus arbitration circuiry has been integrated into the backplane. This permits a bus master to reside in each slot. Extra-wide inter-slot spacing on the cardcage allows the use of plug-on MULTIMODULE boards without blocking adjacent slots. For this reason, the iSBC 661 System Chassis provides the slot-functionality of most 16-slot chassis. Standard logic recognizes a system AC power failure and generates a TTL signal for use in powerdown control. Additionally, current limiting and over-voltage protection are provided at all outputs.



210866-1

October 1986
Order Number: 210866-002

FUNCTIONAL DESCRIPTION

Mechanical Features

The iSBC 661 System Chassis houses, cools, powers, and interconnects up to eight iSBC single board computers and their MULTIMODULE boards for the MULTIBUS System Bus. Based on Intel's iSBC 608 Cardcage, the chassis provides 0.8 inches of board center-to-center clearance on six slots, and 1.2 inches or more of center-to-center clearance on two slots. This permits the users of standard MULTIMODULE boards and custom wire-wrap boards to plug into the MULTIBUS System Bus without blocking adjacent slots. All slots provide enough clearance for iSBC MULTIMODULE boards, and two slots can accommodate iSBX MULTIMODULE boards.

High-technology MULTIBUS applications requiring rack-mount, or laboratory table-top use will find the iSBC 661 System Chassis ideal. Standard 19″ slide-rack mounting is possible with user-provided slides attached to the side panels. Slide mounting holes are provided in the chassis for the slide-rails listed under User Supplied Options. Rubber feet are included on the chassis for convenient table-top use.

The chassis is constructed of burnished aluminum which has been coated with corrosion-resistant chromate. It contains a system control module which presents the front panel control switches to the user, and holds the I/O cabling bulkhead to the rear. The chassis has the unique feature of being configurable for either front or rear access to MULTIBUS circuit boards.

This is accomplished by a simple procedure involving removal of the system control module, reversing it end-for-end, and re-securing it to the chassis. The system chassis is shipped in a configuration such that the MULTIBUS boards are installed from the front.

Electrical Features

The iSBC 661 System Chassis is powered by the iSBC 640 power supply. This is a standard Intel power supply which has been adopted by several MULTIBUS vendors throughout the industry. It sup-

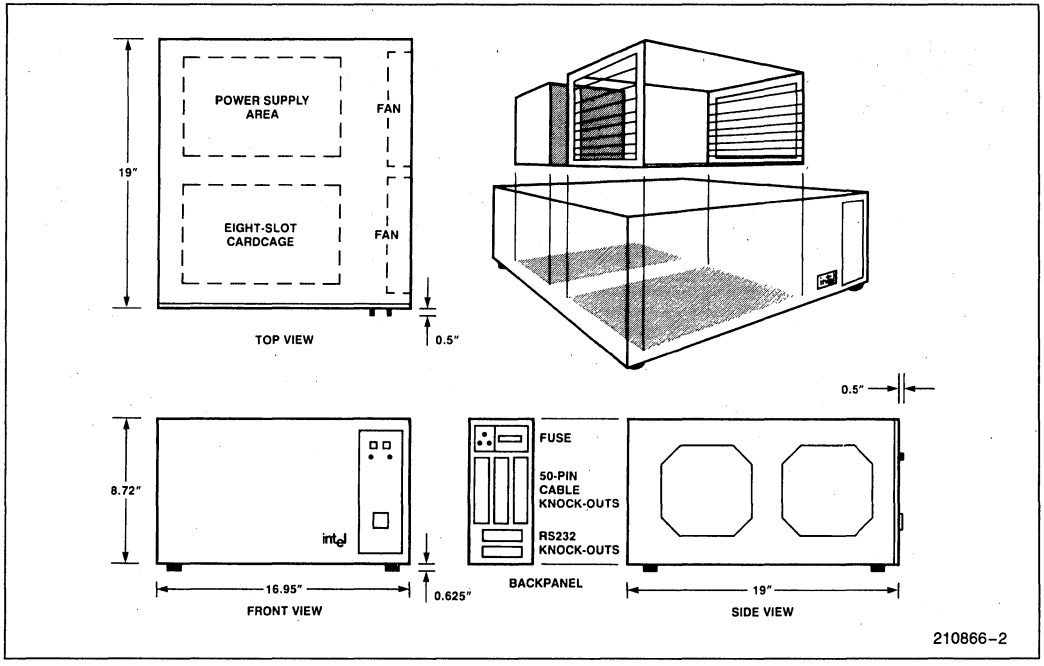


Figure 1. iSBC® 661 System Chassis Dimensions

plies 230 watts of power, power fail warning, and remote sensing of +5 volts. Its electrical and operational parameters are listed under Specifications.

The cardcage of the iSBC 661 System Chassis implements a user-changeable parallel priority bus arbitration scheme by using plug-in jumper connections. Six different priority schemes are allowed, each scheme fixing the priority to the eight MULTIBUS board slots. Bus contention among eight busmasters in a multiprocessing environment can be managed using this approach.

Noise minimizing ground traces are strategically interleaved between signal and address lines on the system bus. This provides the enhanced noise immunity and minimized signal-to-signal coupling which is particularly important in high speed, high board count microcomputer systems.

SPECIFICATIONS

Electrical Parameters

OUTPUT POWER

Table 1. Output Power Levels iSBC® 661-1

Voltage	Output Current (max.)	Current Limits (amps)	Over-Voltage Protection
+12V	4.5A	4.7–6.8	15V ±1V
+5V	30.0A	31.5–45.0	6.2V ±0.4V
−5V	1.75A	1.8–3.2	−6.2V ±0.4V
−12V	1.75A	1.8–3.2	−15V ±1V

Operational Parameters

Input AC Voltage—100/120/220/240 VAC ±10% (User selects via external switch), 47–63 Hz

Power-Fail Indication and Hold-Up Time (triggered at 90% of VAC in)—TTL O.C. High 3 msec. (min.)

Output Ripple and Noise—1% Peak-to-Peak output nominal (DC to 0.5 MHz)

Operational Temperature—0°C to 50°C

Storage Temperature—−40°C to 70°C

Operational Humidity—10% to 85% relative, noncondensing

Remote Sensing—Provided for +5 VCD

Output Transient Response—50 μs or less for ±50% load change

Physical Characteristics

Width: 16.95 inches (43.05 cm)

Height: 8.72 inches (22.2 cm)

Depth: 19.00 inches (48.3 cm)

Weight: 41 pounds (21 kg)

Shipping Weight (approx.): 50 pounds (25 Kg)

Equipment Supplied

iSBC® 661-1—Eight-slot MULTIBUS system chassis with parallel priority arbitration circuitry and 230 watt linear power supply

Reference Manual

(Not included: order separately)

145340-001—iSBC 661 System Chassis Hardware Reference Manual

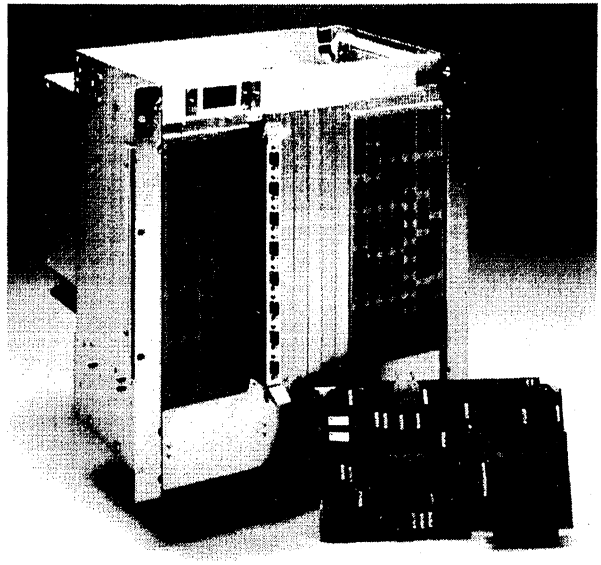
User Supplied Options

Compatible Rack-Mount Slides—Chassis Trak, Inc., P. O. Box 39100, Indianapolis, IN 46239; Part No. C300 S 122

ORDERING INFORMATION

Part Number	Description
SBC 6611	Eight-slot MULTIBUS system chassis with parallel priority arbitration circuitry and 230 watt Linear Power Supply

SYP341 CARD CAGE MODULE

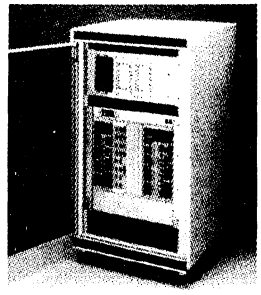


A 16-SLOT MULTIBUS®I CARD CAGE MODULE FOR FLEXIBLE, EXPANDABLE SYSTEMS CONFIGURATIONS

Intel's SYP341 Card Cage is a standard module designed to provide, along with the companion SYP342 Peripheral Module, a basic platform for the integration of large capacity systems. Intel's modular packaging scheme allows for integration into standard 19 inch rack-mount cabinets or NEMA-type enclosures.

FEATURES

- 16-slot MULTIBUS I backplane with integrated priority and interrupt circuitry.
- Accepts standard 7 × 12 inch MULTIBUS I boards and up to seven 10 × 12 inch boards.
- Meets EIA, 19 inch rack standard.
- 4-layer backplane construction. Interleaved bus signal traces. Dedicated power and ground layers.
- 24-bit addressing supported on all slots.
- Extended gold pins for all P2 signals. Supports iLBX bus cables.
- Backplane generated bus clock.
- MULTIBUS reset and interrupt switches with power-on and status indicators.
- 750 watt multiple output switching power supply. Switch selectable 110/220 VAC.
- Forced air cooling. Provides 300 lfm across boards.



SYP341 and SYP342 mounted in typical 19-inch rack-mount cabinet.

intel

September, 1988
Order Number: 280641-002

SPECIFICATIONS

ENVIRONMENTALS

Ambient Temperature	
Operating	0 to 55°C
Non-Operating	– 40 to 80°C
Relative Humidity	
Operating	80% at 40°C
Non-operating	95% at 55°C
Altitude	
Operating	Sea Level to 10,000 feet
Non-Operating	Sea Level to 40,000 feet

ELECTRICAL

DC Power Output	750 watt maximum
+ 5v	100.0 A maximum
+ 12v	10.0 A maximum
– 12v	10.0 A maximum
AC Power Input	90-132 VAC or 180-264 VAC 47-63 Hz

REGULATIONS

Meets the following safety requirements:

US	UL478 5th Edition recognized
Canada	CSA C22.2 No. 220 certified
Europe	IEC 380 and IEC 950

Power Supply meets the following EMI/RFI requirements:

US	FCC Class B Conducted emissions
Europe	VDE Limit Class B Conducted emissions

PHYSICAL CHARACTERISTICS

Dimensions

Standard Rear Mount Power Supply

Height	488.1 mm (19.22 in)
Width	482.7 mm (19.00 in)
Depth	501.6 mm (19.75 in)
Weight	23.9 kilograms (53 lbs)

Optional Mounting:
Side Mounted Power Supply

Width	597.0 mm (23.50 in)
Depth	355.7 mm (14.00 in)

Backplane Slot Spacing

Slots 5, 13 — 1.8"
Slot 1 — 1.4"
Slots 2-4, 6-12, 14-16 — 0.8"
Slots 6-12 accommodate 10 × 12 inch boards

ORDER CODES

SYP341V1—Configured 110 VAC
SYP341V2—Configured 220 VAC

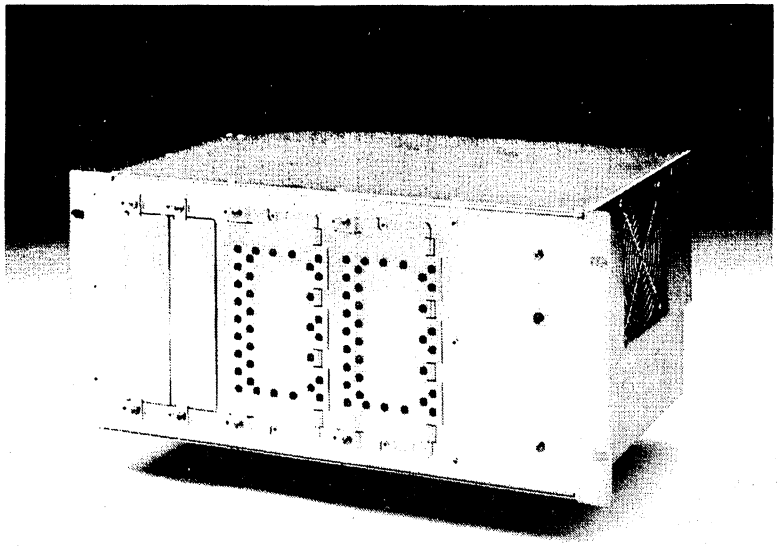
WORLDWIDE SERVICE AND SUPPORT

Intel provides support for Intel and non-Intel boards and peripherals as well as on-site service. Development support options include phone support, subscription service, on-site consulting, and customer training.

QUALITY AND RELIABILITY

The SYP341 is designed, tested and manufactured in accordance with Intel's industry leading quality and reliability standards.

SYP342 PERIPHERAL MODULE

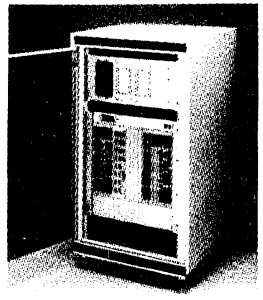


A PERIPHERAL MODULE FOR FLEXIBLE, EXPANDABLE SYSTEM CONFIGURATIONS

Intel's SYP342 Peripheral Module is a standard module designed to provide, along with the companion SYP341 Card Cage Module, a basic platform for the integration of large capacity systems. Intel's modular packaging scheme allows for integration into standard 19-inch rack-mount cabinets or NEMA-type enclosures.

FEATURES

- Houses up to 3 full-height or 6 half-height 5¼ inch peripherals
- Meets EIA, 19-inch rack standard
- 175 Watt multiple output switching power supply
- Auto selectable 110/220 VAC
- Forced air cooling
- Selectable exposed or recessed peripheral mounting positions
- Peripheral carriers, filler panels and ESD panels provided



SYP341 and SYP342 mounted in typical 19-inch rack-mount cabinet.

intel

September, 1988
Order Number: 280642-002

ENVIRONMENTALS

Ambient Temperature	
Operating	0° to 50°C
Non-Operating	– 40° to 80°C
Relative Humidity	
Operating	80% at 40°C
Non-Operating	95% at 55°C
Altitude	
Operating	Sea Level to 10,000 feet
Non-Operating	Sea Level to 40,000 feet

ELECTRICAL

DC Power Output	175 watt maximum continuous (220 watt maximum peak)
+ 5v	15 A maximum continuous
+ 12v	12A maximum continuous (18 A maximum peak)
AC Power Input	90-130 VAC or 180-260 VAC 47-63 Hz

REGULATIONS

Meets the following safety requirements:

US	UL478 5th Edition recognized
Canada	CSA C22.2 No. 220 certified
Europe	IEC 380 and IEC 950

Power Supply meets the following EMI/RFI requirements:

US	FCC Class B Conducted emissions
Europe	VDE Limit Class B Conducted emissions

PHYSICAL CHARACTERISTICS

Height	220.9 mm (8.7 in)
Width	482.7 mm (19.0 in)
Depth	292.1 mm (11.5 in)
Weight	12.7 kilograms (28 lbs)

ORDER CODE

SYP342E

WORLDWIDE SERVICE AND SUPPORT

Intel provides support for Intel and non-Intel boards and peripherals as well as on-site service. Development support options include phone support, subscription service, on-site consulting, and customer training.

QUALITY AND RELIABILITY

The SYP342 is designed, tested and manufactured in accordance with Intel's industry leading quality and reliability standards.

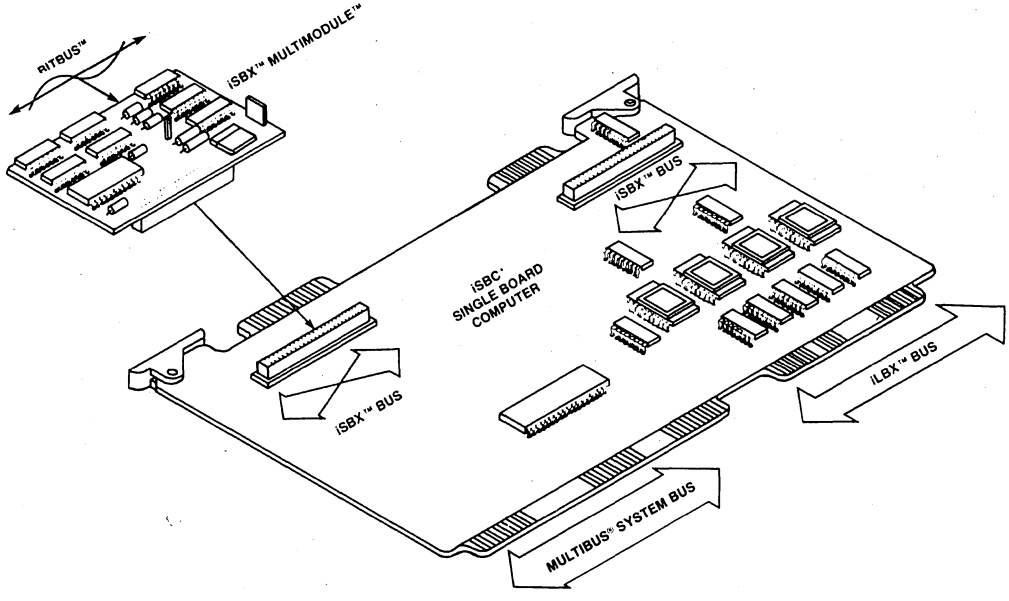
MULTIBUS® I Architecture

9

MULTIBUS® SYSTEM BUS

- **IEEE 79688 Industry Standard System Bus**
- **Supports Multiple Processor Systems with Multi-Master Bus Structure**
- **8-Bit, 16-Bit, and 32-Bit Devices Share the Same MULTIBUS® System Resources**
- **Foundation of Intel's Total System Architecture: MULTIBUS®, iLBX™, BITBUS™ and iSBX™ Buses**
- **16 Mbyte Addressing Capability**
- **Bus Bandwidth of Up to 10 Megabytes Per Second**
- **Supported by a Complete Family of Single Board Computers, Memory, Digital and Analog I/O, Peripheral Controllers, Graphics and Speech Recognition, Packaging and Software**
- **Supported by Over 200 Vendors Providing Over 2000 Compatible Products**

The MULTIBUS® System bus is one of a family of standard bus structures resident within Intel's total system architecture. The MULTIBUS interface is a general purpose system bus structure containing all the necessary signal lines to allow various system components to interact with one another. This device interaction is built upon the master-slave concept. The "handshaking" between master and slave devices allows modules of different speeds to use the MULTIBUS interface and allows data rates of up to 5 million transfers per second. The MULTIBUS system bus can support multiple master devices (16) on a 18 inch backplane and can directly address up to 16 megabytes of memory. As a non-proprietary, standard system bus, the MULTIBUS interface has become the most prominent 8/16-bit microcomputer system bus in the industry with over 200 vendors supplying over 2000 MULTIBUS compatible products. Its success as the industry standard has been reinforced by adoption of the MULTIBUS specification by the Institute of Electrical and Electronic Engineers—(IEEE 79688 System Backplane Bus). MULTIBUS-based systems have been designed into applications, such as, industrial automation and control, office systems and word processing, graphics systems and CAD/CAM, telecommunications systems and distributed processing.



280294-1

September 1988
Order Number: 280294-001

FUNCTIONAL DESCRIPTION

Architectural Overview

The MULTIBUS® system bus is the physical framework and the conceptual foundation of Intel's total system architecture. It is a general purpose system bus used in conjunction with the single board computer concept to provide a flexible mechanism for inter-module processing, control and communication. The MULTIBUS interface supports modular CPU, memory and I/O expansion in flexible, cost effective microcomputer system configurations. These configurations implement single board computers and expansion modules in a multiple processor approach to enhance system performance. This enhanced performance is achieved through partitioning of overall system functions into tasks that each of several processors can handle individually. When new system functions are added (peripherals) more processing power can be applied to handle them without impacting existing processor tasks.

Structural Features

The MULTIBUS interface is an asynchronous, multiprocessing system bus designed to perform 8-bit and 16-bit transfers between single board computers, memory and I/O expansion boards. Its interface structure consists of 24 address lines, 16 data lines, 12 control lines, 9 interrupt lines, and 6 bus exchange lines. These signal lines are implemented on single board computers and a mating backplane in the form of two edge connectors resident on 6.75″ × 12.00″ form factor PC boards. The primary 86-pin P1 connector contains all MULTIBUS signal lines except the four address extension lines. The auxiliary 60-pin P2 connector contains the four MULTIBUS address extension lines, and reserves the remaining 56 pins for implementing the iLBX Execution Bus into the MULTIBUS system architecture.

Bus Elements

The MULTIBUS system bus supports three device categories: 1) Master, 2) Slave, 3) Intelligent Slave.

A bus master device is any module which has the ability to control the bus. This ability is not limited to only one master device. The MULTIBUS interface is capable of supporting multiple masters on the same system through bus exchange logic. Once access has been acquired by a master device, it has a period of exclusive control to affect data transfers through a generation of command signals, address signals and memory or I/O addresses.

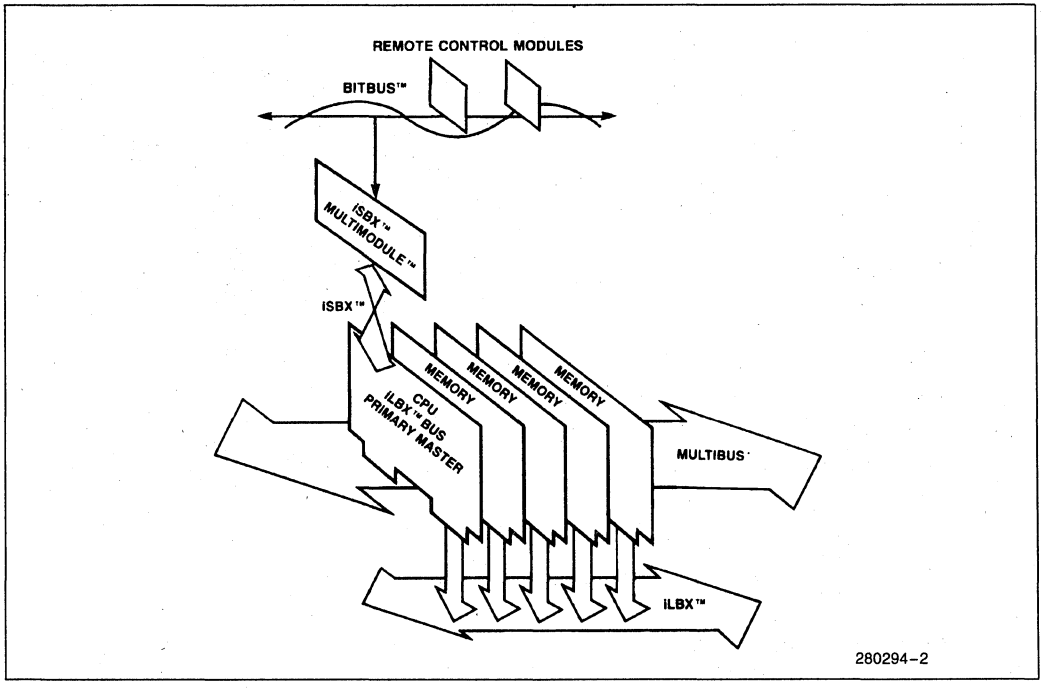


Figure 1. MULTIBUS® System Architecture

A bus slave device is a module that decodes the address lines on the MULTIBUS and acts upon the command signals from the bus masters. Slave devices are not capable of controlling the MULTIBUS interface.

The intelligent slave has the same bus interface attributes as the slave device but also incorporates an on-board microprocessor to control on-board memory and I/O tasks. This combination of on-board processor, memory and I/O allow the intelligent slave to complete on-board operations without MULTIBUS access.

Bus Interface/Signal Line Descriptions

The MULTIBUS system bus signal lines are grouped into five classes based on the functions they perform: 1) control lines, 2) address and inhibit lines, 3) data lines, 4) interrupt lines, 5) bus exchange lines. Figure 2 shows the implementation of these signal lines.

The MULTIBUS control lines are broken down into five sub-groups: clock signals (2), commands (4), acknowledge (1), initialize (1), and lock (1). The two clock signals provide for the generation of a master

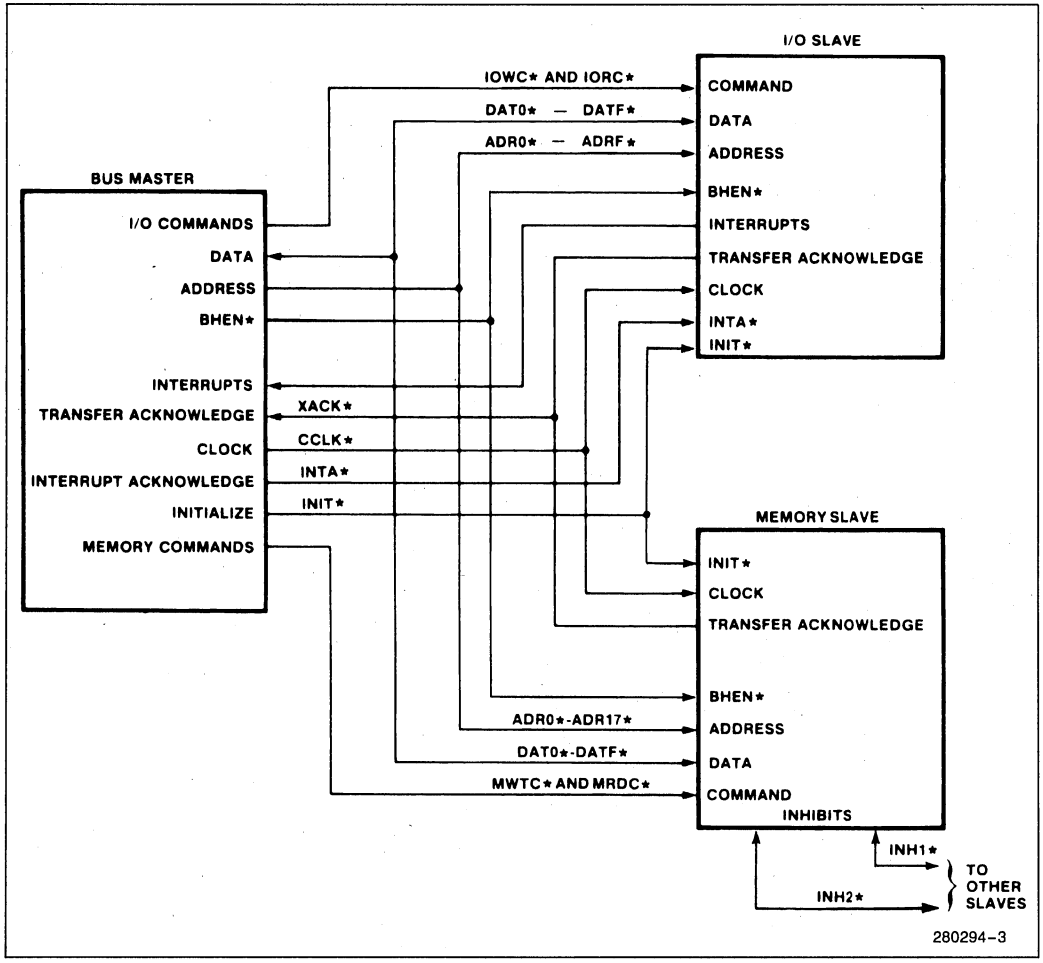


Figure 2. MULTIBUS® Interface Signal Lines

clock for the system and the synchronization of bus arbitration logic. The four command lines are the communication links between the bus masters and bus slaves, specifying types of operations to be performed such as reads or writes from memory or I/O. The transfer acknowledge line is the slave's acknowledgement that a requested action of the master is complete. The initialize signal is generated to reset the entire system to a known state. The lock signal is used by an active bus master to lock dual-ported for mutual exclusion.

The address and inhibit lines are made up of 24 address lines, two inhibit lines, and one byte control line. The 24 address lines are signal lines used to carry the address of the memory location or the I/O device that is being referenced. These 24 lines allow a maximum of 16 million bytes of memory to be accessed. When addressing an I/O device, sixteen address lines are used to address a maximum of 64 thousand devices. The two inhibit lines are used to allow different types of memory (RAM, ROM, etc.) having the same memory address to be accessed in a preferred priority arrangement. The byte control line is used to select the upper byte of a 16-bit word in systems incorporating 16-bit memory and I/O modules.

The MULTIBUS interface supports sixteen bi-directional data lines to transmit or receive information to or from a memory location or an I/O port.

The MULTIBUS interrupt lines consist of eight interrupt request lines and one interrupt acknowledge line. Interrupts are requested by activating one of the eight interrupt request lines. The interrupt acknowledge signal is generated by the bus master when an interrupt request is received. It effectively freezes interrupt status and requests the placement of the interrupt vector address onto the data lines. There are six bus exchange lines that support two bus arbitration schemes on the MULTIBUS system bus. A bus master gains control of the bus through the manipulation of these signals. The bus request, bus priority, bus busy, and bus clock signals provide for a slot dependent priority scheme to resolve bus master contention on the MULTIBUS interface. Use of the common bus request signal line can save arbitration time by providing for a higher priority path to gain control of the system bus.

Bus Operation Protocol

DATA TRANSFER OPERATION

The data transfer operation of the MULTIBUS system bus is a straight-forward implementation of an asynchronous master-slave handshaking protocol. Figures 3 and 4 show the basic timing for a read and write data transfer operation. A MULTIBUS data transfer begins by having the bus master place the memory or I/O port address on the address bus. If the operation is a write, the data is also placed on the data lines at this time. The bus master then generates a command (I/O read or write, or memory read or write) which activates the appropriate bus slave. The slave accepts the data if it is a write operation, or places data on the data bus if it is a read. A transfer acknowledge is then sent to the bus master by the bus slave, allowing the bus master to complete its cycle, removing the command from the command line, and then removing the address and data from the MULTIBUS interface.

INTERRUPT OPERATIONS

The MULTIBUS interface supports two types of interrupt implementation schemes, Non-Bus Vectored and Bus Vectored. Non-Bus vectored interrupts are interrupts handled on the bus master which do not require the MULTIBUS interface for transfer of the interrupt vector address. The interrupt vector address is generated by the interrupt controller on the master and transferred to the processor over the local bus when an interrupt request line is activated by a slave module over the MULTIBUS interface. Bus vectored interrupts are interrupts which transfer the interrupt vector address along the MULTIBUS data lines from the slave to the bus master using the interrupt acknowledge command signal for synchronization. When an interrupt request occurs, the interrupt control logic on the bus master interrupts the processor, generating an interrupt acknowledge command that freezes the interrupt logic on the bus for priority resolution and locks the MULTIBUS system bus. After the bus master selects the highest priority active interrupt request lines, a set of interrupt sequences allow the bus slave to put its interrupt vector address on the data lines. This address is used as a pointer to interrupt the service routine.

BUS EXCHANGE TECHNIQUES

The MULTIBUS system bus can accommodate several bus masters on the same system, each one taking control of the bus as it needs to affect data transfers. The bus masters request bus control through a bus exchange sequence.

The MULTIBUS interface provides for two bus exchange priority techniques: a serial technique and a parallel technique. In a serially arbitrated MULTIBUS system, requests for system bus access are ordered by priority on the basis of bus slot location. Each master on the bus notifies the next lower priority master when it needs to use the bus, and it monitors the bus request status of the next higher priori-

ty-master. Thus, the masters pass bus requests along from one to the next in a daisy chain fashion. The parallel bus arbitration technique resolves system bus master priorities using external hardware in the form of a priority resolution circuit. This parallel arbitration logic is included in many commercially available cardcages.

Mechanical Implementation

BUS PIN ASSIGNMENTS

Printed circuit boards (6.75" x 12.00") designed to interface to the MULTIBUS system bus have two connectors which plug into the bus backplane. These connectors, the 86-pin P1 (Primary) and the 60-pin P2 (Auxiliary), have specific pin/signal assignments. Because of this, the designer must insure that the MULTIBUS backplane being designed is compatible (pin-for-pin) with these two connectors. Tables 1 and 2 show the pin/signal assignments for the P1 and P2 edge connectors. The MULTIBUS interface connection is accomplished via a rigid backplane that has connectors that mate to the P1 (43/86-pin) board edge connector and allows for connectors that mate to the P2(30/60-pin) board edge connector. Figure 5 shows a typical MULTIBUS backplane. Figure 6 displays the connector and pin numbering convention. Figure 7 shows the standard MULTIBUS form-factor printed wiring board outline.

Please refer to Intel's MULTIBUS specification and iLBX bus specification for more detailed information.

Table 1. MULTIBUS® Pin/Signal Assignment—(P1)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5V	+5Vdc	4	+5V	+5 Vdc
	5	+5V	+5Vdc	6	+5V	+5 Vdc
	7	+12V	+12Vdc	8	+12V	+12 Vdc
	9		Reserved, bussed	10		Reserved, bussed
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK*	Bus Clock	14	INIT*	Initialize
	15	BPRN*	Bus Pri. In	16	BPRO*	Bus Pri. Out
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Cmd	20	MWTC*	Mem Write Cmd
	21	IORC*	I/O Read Cmd	22	IOWC*	I/O Write Cmd
	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (disable RAM)
Bus Controls and Address	25	LOCK*	Lock	26	INH2*	Inhibit 2 (disable PROM
	27	BHEN*	Byte High Enable	28	AD10*	or ROM)
	29	CBRQ*	Common Bus Request	30	AD11*	Address
	31	CCLK*	Constant Clk	32	AD12*	Bus
	33	INTA*	Intr Acknowledge	34	AD13*	
Interrupts	35	INT6*	Parallel	36	INT7*	Parallel
	37	INT4*	Interrupt	38	INT5*	Interrupt
	39	INT2*	Requests	40	INT3*	Requests
	41	INT0*		42	INT1*	
Address	43	ADRE*		44	ADRF*	
	45	ADRC*		46	ADRD*	
	47	ADRA*	Address	48	ADRB*	Address
	49	ADR8*	Bus	50	ADR9*	Bus
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADR0*		58	ADR1*	

Table 1. MULTIBUS® Pin/Signal Assignment—(P1) (Continued)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
Data	59	DATE*		60	DATF*	
	61	DATC*		62	DATD*	
	63	DATA*	Data	64	DATB*	Data
	65	DAT8*	Bus	66	DAT9*	Bus
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DAT0*		74	DAT1*	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77		Reserved, bussed	78		Reserved, bussed
	79	−12V	−12 Vdc	80	−12V	−12 Vdc
	81	+5V	+5 Vdc	82	+5V	+5 Vdc
	83	+5V	+5 Vdc	84	+5V	+5 Vdc
	85	GND	Signal GND	86	GND	Signal GND

NOTES:
All Reserved pins are reserved for future use and should not be used if upwards compatibility is desired.
*The Reserved MULTIBUS P2 connector pin/signal assignments are contained in Intel's iLBX Bus Specification.

Table 2. MULTIBUS® Pin/Signal Assignment—(P2)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
	1		Reserved	2		Reserved
	3		Reserved	4		Reserved
	5		Reserved	6		Reserved
	7		Reserved	8		Reserved
	9		Reserved	10		Reserved
	11		Reserved	12		Reserved
	13		Reserved	14		Reserved
	15		Reserved	16		Reserved
	17		Reserved	18		Reserved
	19		Reserved	20		Reserved
	21		Reserved	22		Reserved
	23		Reserved	24		Reserved
	25		Reserved	26		Reserved
	27		Reserved	28		Reserved
	29		Reserved	30		Reserved
	31		Reserved	32		Reserved
	33		Reserved	34		Reserved
	35		Reserved	36		Reserved
	37		Reserved	38		Reserved
	39		Reserved	40		Reserved

Table 2. MULTIBUS® Pin/Signal Assignment—(P2) (Continued)

	Pin	(Component Side)		Pin	(Circuit Side)	
		Mnemonic	Description		Mnemonic	Description
	41		Reserved	42		Reserved
	43		Reserved	44		Reserved
	45		Reserved	46		Reserved
	47		Reserved	48		Reserved
	49		Reserved	50		Reserved
	51		Reserved	52		Reserved
	53		Reserved	54		Reserved
Address	55	ADR16*	Address Bus	56	ADR17*	Address Bus
	57	ADR14*		58	ADR15*	
	59		Reserved, Bussed	60		Reserved, Bussed

NOTES:
All Reserved Pins are reserved for future use and should not be used if upwards compatibility is desired.
*The Reserved MULTIBUS P2 connector pin/signal assignments are contained in Intel's iLBX Bus Specification.

SPECIFICATION

Word Size

Data: 8- and 16-bit

Memory Addressing

24-bits: 16 megabyte-direct access

I/O Addressing

16-bit: 64 Kbytes

Maximum Bus Backplane Length

18 inches

Electrical Characteristics

BUS POWER SUPPLY SPECIFICATIONS

Table 3

Standard(1)				
Parameter	Ground	+5	+12	−12
Mnemonic	GND	+5V	+12V	−12V
Bus Pins	P1-1,2,11,12, 75,76,85,86	P1-3,4,5,6, 81,82,83, 84	P1-7,8,	P1-79,80
Tolerance	Ref.	±1%	±1%	±1%
Combined Line & Load Reg	Ref.	0.1%	0.1%	0.1%
Ripple (Peak to Peak)	Ref.	50 mV	50 mV	50 mV
Transient Response (50% Load Change)		100 μs	100 μs	100 μs

NOTE:
1. Point of measurement is at connection point between motherboard and power supply. At any card edge connector a degradation of 2% maximum (e.g. voltage tolerance ±2%) is allowed.

Bus Devices Supported

16 total devices—(Master, Slave, Intelligent Slave)

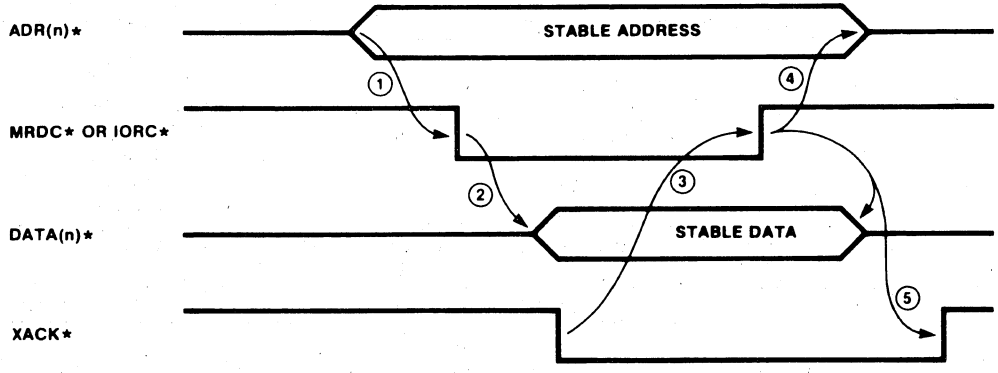
Bus Bandwidth

10 megabytes/sec: 16-bit
5 megabytes/sec: 8-bit

Bus Exchange Cycle

200 ns—Best Case; 300 ns—Worst Case (assuming no bus master is currently active on the bus.)

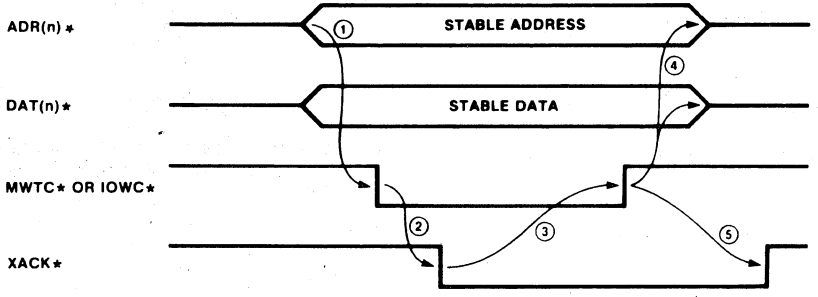
BUS TIMING



280294-4

NOTES:
1. Address Setup Time: 50 Nanoseconds Minimum.
2. Time Required for Slave to Get Data Onto Bus in Accordance with Setup Time Requirement. XACK* can be Asserted as soon as Data is on Bus.
3. Time Required for Master to Remove Command.
4. Address and Data Hold Time; 50 Nanoseconds Minimum.
5. XACK* and Data Must be Removed from the Bus a Maximum of 65 Nanoseconds after the Command is Removed.

Figure 3. Memory or I/O Read Timing



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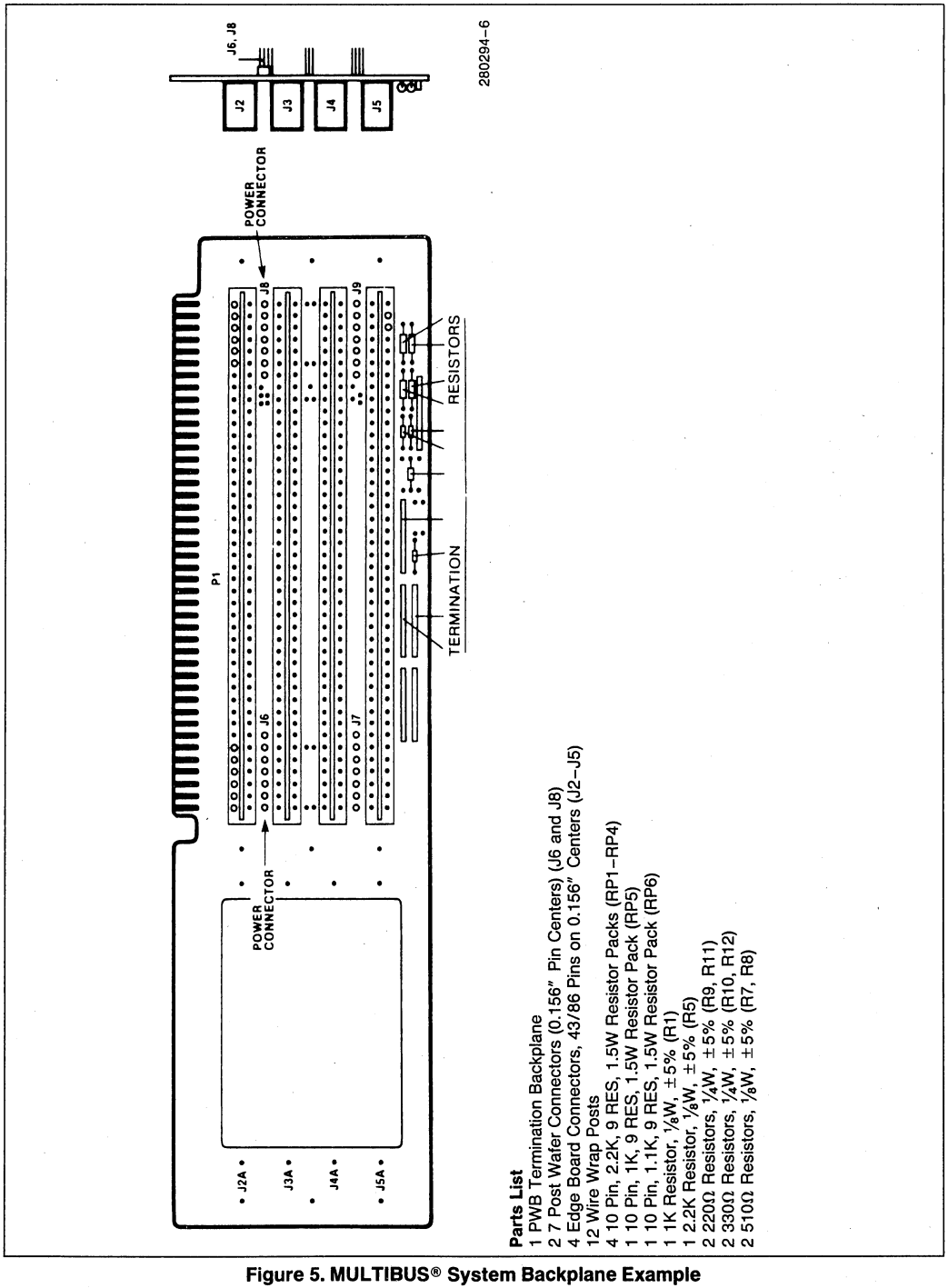
NOTES:
1. Address and Data Setup; 50 Nanoseconds Minimum.
2. Time Required for Slave to Accept Data.
3. Time Required for Master to Remove Command from Bus.
4. Address and Data Hold Time; 50 Nanoseconds Minimum.
5. XACK* Must be off the Bus 65 Nanoseconds after Command.

Figure 4. Memory or I/O Write Timing

PHYSICAL CHARACTERISTICS



Parts List
1 PWB Termination Backplane
2 7 Post Wafer Connectors (0.156" Pin Centers) (J6 and J8)
4 Edge Board Connectors, 43/86 Pins on 0.156" Centers (J2–J5)
12 Wire Wrap Posts
4 10 Pin, 2.2K, 9 RES, 1.5W Resistor Packs (RP1–RP4)
1 10 Pin, 1K, 9 RES, 1.5W Resistor Pack (RP5)
1 10 Pin, 1.1K, 9 RES, 1.5W Resistor Pack (RP6)
1 1K Resistor, 1/8W, ±5% (R1)
1 2.2K Resistor, 1/8W, ±5% (R5)
2 220Ω Resistors, 1/4W, ±5% (R9, R11)
2 330Ω Resistors, 1/4W, ±5% (R10, R12)
2 510Ω Resistors, 1/8W, ±5% (R7, R8)

Figure 5. MULTIBUS® System Backplane Example

Physical Characteristics (Continued)

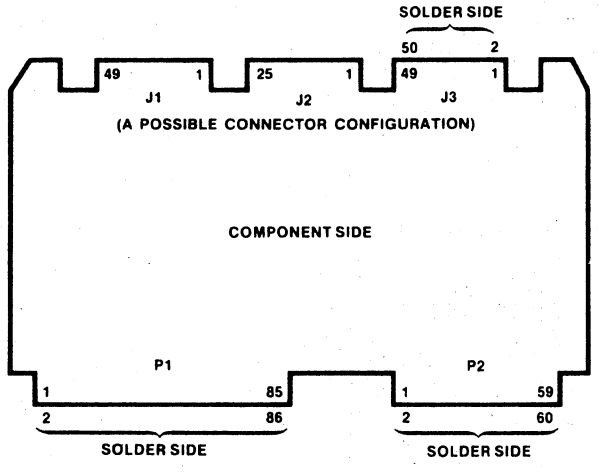


Figure 6. Connector and Pin Numbering

PHYSICAL CHARACTERISTICS (Continued)

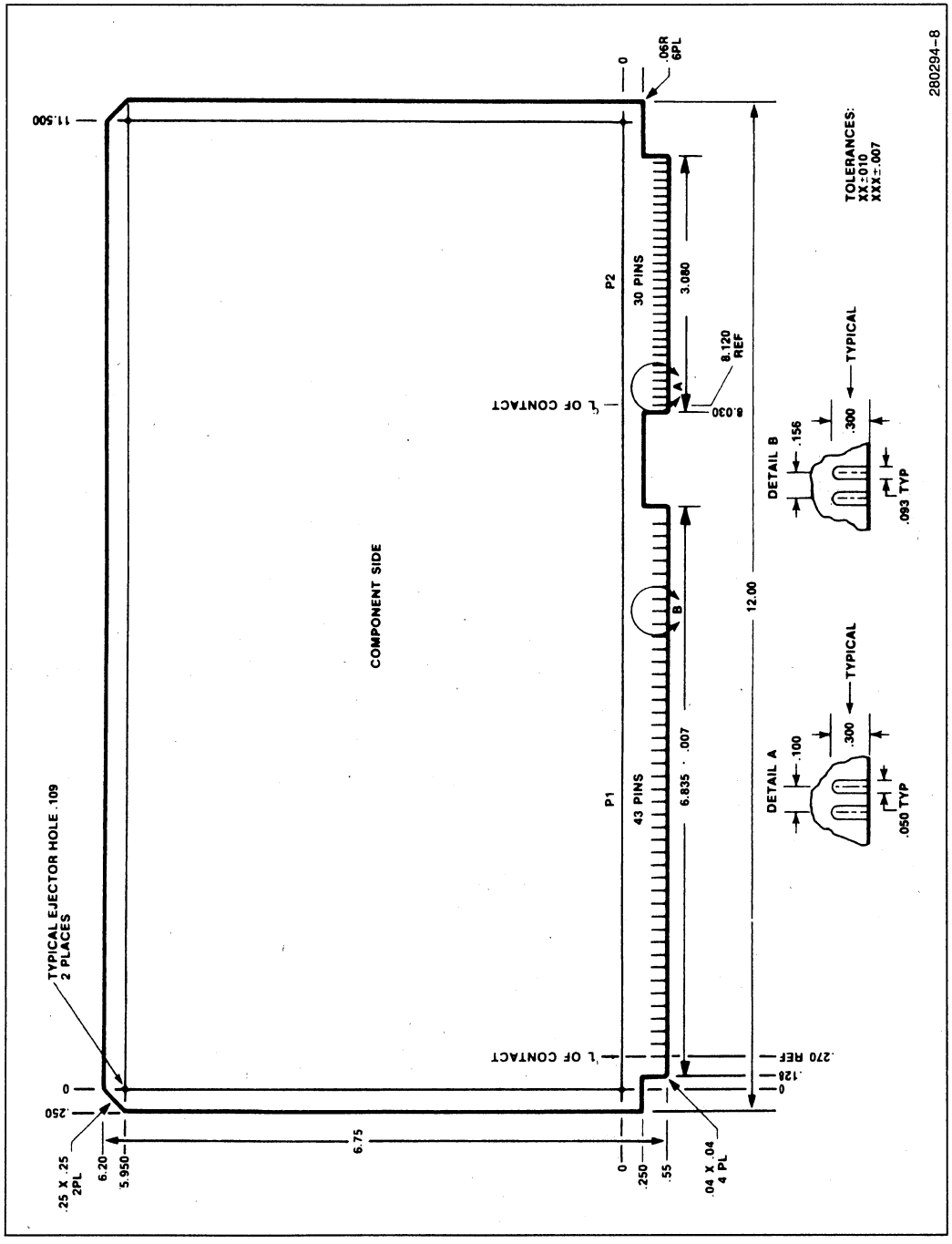


Figure 7. Standard Printed Wiring Board Outline

Backplane Connectors

Table 4. Connector Vendors

Function	# Of Pins	Centers Inches	Connector Type	Vendor	Vendor #	Intel #
Multibus Connector (P1)	43/86	0.156	Soldered(1)	VIKING ELFAB	2KH43/9AMK12 BS1562D43PBB	102247-001
Multibus Connector (P1)	43/86	0.156	Wire wrap(1, 2)	ELFAB ELDAC	BW1562D43PBB 3370860540201	102248-001
				ELFAB EDAC	BW1562A43PBB 337086540202	102273-001(3)
Auxiliary Connector (P2)	30/60	0.1	Soldered(1)	ELFAB EDAC	BS1020A30PBB 345060524802	102238-001
Auxiliary Connector (P2)	30/60	0.1	Wire wrap(1, 2)	TI VIKING	H421121-30 3KH30/9JNK	N/A(3)
				EDAC ELFAB	345060540201 BW1020D30PBB	102241-001

NOTES:
1. Connector heights are not guaranteed to conform to Intel packaging equipment.
2. Wirewrap pin lengths are not guaranteed to conform to Intel packaging equipment.
3. With mounting ears with 0.128 mounting holes.

Environmental Characteristics

Operating Temperature: 0°C to 60°C; free moving air across modules and bus

Humidity: 90% maximum (no condensation)

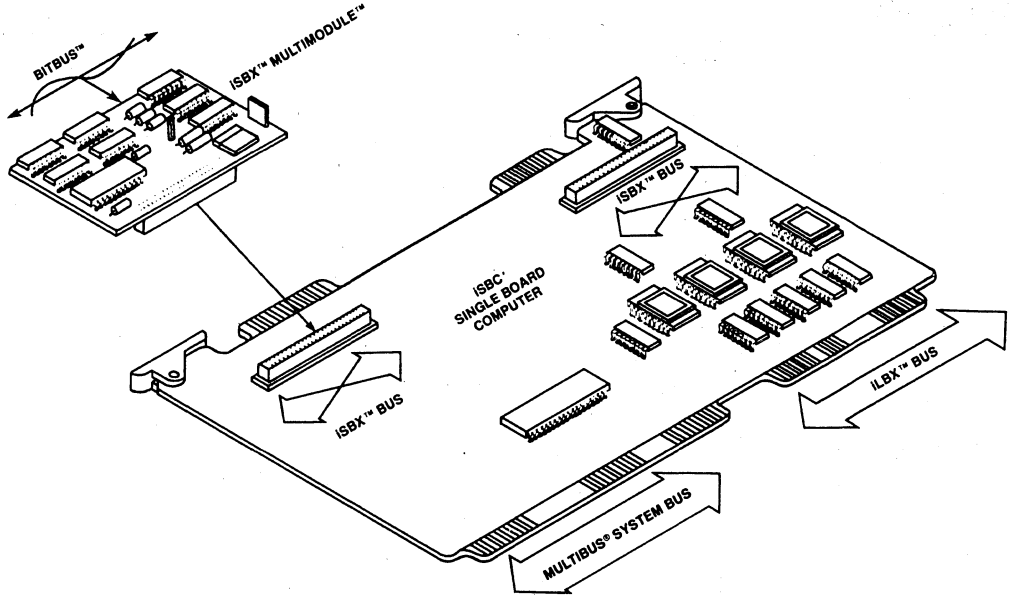
Reference Manuals

210883-002— MULTIBUS Architecture Reference Book

iLBX™ EXECUTION BUS

- **High Bus Bandwidth**
  - **— 9.5 Mbytes/sec. for 8-Bit Transfers**
  - **— 19 Mbytes/sec. for 16-Bit Transfers**
- **16 Mbyte Addressing Range**
- **8 and 16-Bit Data Transfers**
- **Supports up to 5 iLBX™ Compatible Devices Per Bus**
- **Primary and Secondary Master Bus Exchange Capabilities**
- **Standard 60-Pin MULTIBUS® P2 Connector**

The iLBX™ Execution Bus is one of a family of standard bus structures resident within Intel's total system architecture. The Local Bus Extension (iLBX) Bus is a dedicated execution bus capable of significantly increasing system performance by extending the processor board's on-board local bus to off-board resources. This extension provides for arbitration-free, direct access to high-performance memory. Acting as a "virtual" iSBC®, up to 16 megabytes of processor addressable memory can be accessed over the iLBX bus and appear as though it were resident on the processor board. The iLBX Bus preserves advantages in performance and architecture of on-board memory, while allowing memory configurations larger than possible on a single board computer. High throughput and independence from MULTIBUS® activities make the iLBX bus an ideal solution for "working store" type program memory and data processing applications requiring large amounts of high performance memory. Such applications include graphics systems, robotics, process control, office systems, and CAD/CAM.



280215-1

September 1988
Order Number: 280215-001

FUNCTIONAL DESCRIPTION

Architectural Overview

The iLBX bus is an architectural solution for supporting large amounts of high performance memory. It is the first structure that allows the CPU board selection to be decoupled from the on-board memory requirement, and still maximizes the processor's performance potential. It eliminates the processor's need to access its off-board memory resources solely over the MULTIBUS system bus. Architectural consistency with the single board computer approach including iLBX memory can be maintained by dual port access of memory resources between the iLBX bus and the MULTIBUS system bus. This allows for global access by other processors and I/O devices while still providing high speed local CPU operations. This sub-system created by the iLBX bus of a single board computer and a maximum of 4 memory cards can be perceived architecturally as a "virtual single board computer". The implementation of iLBX bus "virtual modules" makes it possible to create functional modules with a new level of flexibility and performance in implementing a wide range of memory capabilities. With future needs in mind, the iLBX bus has the capability of accessing a full 16 megabytes of memory.

Structural Features

The iLBX bus uses a non-multiplexed 16-bit configuration capable of 8 and 16-bit transfers. Used in conjunction with the MULTIBUS interface, the iLBX bus resides on the MULTIBUS form factor P2 connector and supercedes the MULTIBUS interface definitions for the P2 signals. The iLBX bus uses the standard 60-pin MULTIBUS P2 connector and occupies 56 of the P2 connector pins with 16 data lines, 24 address lines plus control, command access, and parity signals. The four MULTIBUS address extension lines on the MULTIBUS/iLBX P2 connector retain the standard MULTIBUS interface definition.

Bus Elements

The iLBX bus supports three distinct device categories: 1) Primary Master, 2) Secondary Master, 3) Slave. These three device types may be combined to create several iLBX local busses ranging (in size) from a minimum of two to a maximum of five devices per iLBX bus. There is only one Primary Master in any given implementation of iLBX bus, and its presence is required along with the attachment of at least one Slave device. To provide alternate access over an iLBX bus, one optional Secondary Master

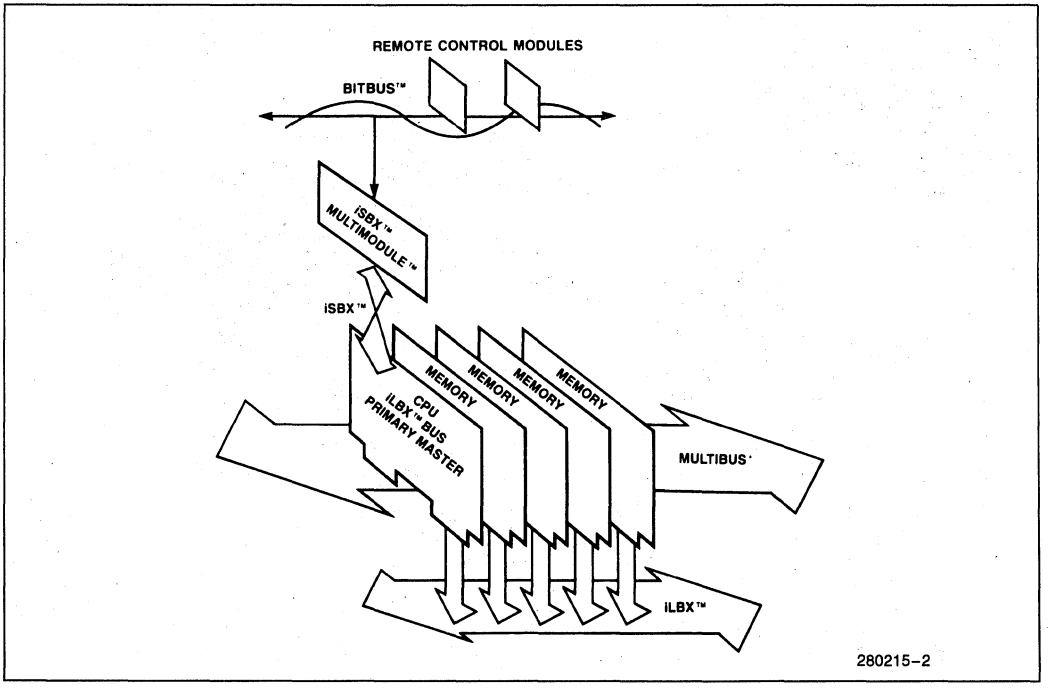


Figure 1. MULTIBUS® System Architecture

may be incorporated to create a "two-master" local bus subsystem. By limiting the iLBX bus to two masters (a Primary and a Secondary), bus arbitration is reduced to a simple request and acknowledge process, with privileged use of the bus maintained by the Primary Master, and limited access granted to the Secondary Master when needed.

The Primary Master executes the role of iLBX bus "supervisor" by controlling the general operation of the bus and managing Secondary Master accesses to the Slave memory resources.

The Secondary Master Device is an option providing alternate access to the Slave resources on the iLBX bus. Secondary master devices are typically DMA driven. This feature is provided for implementation flexibility when occasional DMA transfers in and out of iLBX memory resources can optimize the overall system performance. The Secondary Master essentially duplicates the Primary Master's data transfer capability, but must rely on the Primary Master to grant access. Once access is granted, the Secondary Master controls the bus, and drives all signal lines until the operation is complete and control is passed back to the Primary Master.

The Slave devices contain the memory resources used by the Primary Master and the optional Secondary Master. Each iLBX implementation can contain a maximum of four Slave devices. Using 64K RAM technology on four slave devices with ECC can provide for over 2 megabytes of "on-board" high performance memory. With 256K RAM chips, each iLBX bus could contain slave devices with memory totalling 8 megabytes. As memory technology increases, the iLBX bus is designed to incorporate it in rapid fashion because it is capable of directly accessing a full 16 megabytes of memory on its high-performance Slave devices.

Bus Interface/Signal Line Descriptions

The iLBX bus interface is divided into four functional classes of signal lines: address and data lines, control lines, command lines, and bus access lines. The 40 address and data lines defined by the iLBX Bus Specification consist of 16 data lines and 24 address lines.

There are 16 bi-directional data lines exclusively used to handle 8-bit and 16-bit data transfers between the active bus master and the selected slave device. The iLBX bus uses these data lines for all data transfers, and are driven by tri-state drivers.

The 24 address lines on the iLBX bus provide the ability to directly address 16 megabytes of memory. These single-direction address lines are exclusively driven by the active bus master. The iLBX bus master uses them to select a specific slave device. Three control lines specify the type of data transfer between master and slave devices, while the three command lines initiate, control, and terminate the transfer. There are also three bus access lines used to transfer bus control between master devices.

Bus Pin Assignments

The iLBX bus uses the standard 60-pin MULTIBUS P2 connector. The physical location of each pin assignment and its corresponding function is listed in Table 1. The four MULTIBUS address extension lines (pins 55–58 on the P2 connector) retain the standard MULTIBUS interface functions.

Bus Operation Protocol

The operation protocol for the iLBX bus is a straightforward set of procedures consisting of three basic operations: bus control access, write data to memory, read data from memory. These operations use asynchronous protocol with positive acknowledgment.

Bus Access

The iLBX bus is shared by at most two masters; one Primary Master and one optional Secondary Master, each providing an alternate access path to iLBX bus memory resources. The mechanism for obtaining bus access is a simple request and acknowledge process communicated between masters. Each master is a bus controller of similar capabilities, responsible for data transfer operations between devices, but the Primary Master has the added responsibility of controlling iLBX bus accesses.

The Primary Master has default control of the iLBX bus. If the Secondary Master needs access to the bus, it must initiate a request and wait for acknowledgment from the Primary Master. The choice of when to surrender control of the bus rests with the Primary Master, but if no data transfer is in progress, the Primary Master normally relinquishes control immediately to the Secondary Master.

Data Transfer Operation

The iLBX bus supports two types of data transfer operations: write data to memory and read data from memory. These data transfer operations facilitate the passing of information between the active bus master and the selected slave device. The operation of these two transfer types is very similar; the only differences being the direction of the data transfer and the device driving the data lines.

For either type of data transfer, the active bus master first initiates the transfer operation by placing the memory address on the address lines (AB23–AB0) and a control configuration on the control lines to select the slave device. Once the slave device is selected, the type of data transfer becomes the key factor. With the write operation, the active master maintains control of the data lines and provides valid data within the specified time. Upon accepting a data element, the slave sends a receipt acknowledgment signal to the master which completes the data transfer operation.

With the read operation, the slave device drives the data lines and places valid data on the data lines before sampling by the active master. The slave acknowledges the master to signal the end of the data transfer, and the master completes the operation.

The iLBX Bus Specification includes provisions for both optimized and non-optimized data transfers. Optimized operation uses pipelining and signal overlapping techniques to manage the data transfer timing relationships between the active bus master and the selected slave. The use of signal overlapping requires that every device attached to the iLBX bus provide a means of varying the timing of the slave request and acknowledge signals. The non-optimized operation uses fixed signal sequences, instead of signal overlapping, to assure a valid data transfer, and a device does not need a variable request or acknowledge to read data-valid timing on the iLBX bus. Please refer to the iLBX Bus Specification for detailed descriptions of these transfer operations.

Table 1. iLBX™ Bus Pin Assignments, P2 Edge Connector

Component Side			Solder Side		
16-Bit Pin	**Mnemonic**	**Signal Name**	**16-Bit Pin**	**Mnemonic**	**Signal Name**
1	DB0	Data Line 0	2	DB1	Data Line 1
3	DB2	Data Line 2	4	DB3	Data Line 3
5	DB4	Data Line 4	6	DB5	Data Line 5
7	DB6	Data Line 6	8	DB7	Data Line 7
9	GND	Ground	10	DB8	Data Line 8
11	DB9	Data Line 9	12	DB10	Data Line 10
13	DB11	Data Line 11	14	DB12	Data Line 12
15	DB13	Data Line 13	16	DB14	Data Line 14
17	DB15	Data Line 15	18	GND	Ground
19	AB0	Address Line 0	20	AB1	Address Line 1
21	AB2	Address Line 2	22	AB3	Address Line 3
23	AB4	Address Line 4	24	AB5	Address Line 5
25	AB6	Address Line 6	26	AB7	Address Line 7
27	GND	Ground	28	AB8	Address Line 8
29	AB9	Address Line 9	30	AB10	Address Line 10
31	AB11	Address Line 11	32	AB12	Address Line 12
33	AB13	Address Line 13	34	AB14	Address Line 14
35	AB15	Address Line 15	36	GND	Ground
37	AB16	Address Line 16	38	AB17	Address Line 17
39	AB18	Address Line 18	40	AB19	Address Line 19
41	AB20	Address Line 20	42	AB21	Address Line 21
43	AB22	Address Line 22	44	AB23	Address Line 23
45	GND	Ground	46	ACK*	Slave Acknowledge
47	BHEN	Byte High Enable	48	R/$\overline{W}$	Read Not Write
49	ASTB*	Address Strobe	50	DSTB*	Data Strobe
51	SMRQ*	Secondary Master Request	52	SMACK*	Secondary Master Acknowledge
53	LOCK*	Access Lock	54	GND	Ground
55	ADR22*	MULTIBUS® Address Extension Line 22	56	ADR23*	MULTIBUS® Address Extension Line 23
57	ADR20*	MULTIBUS® Address Extension Line 20	58	ADR21*	MULTIBUS® Address Extension Line 21
59	RES	Reserved	60	TPAR*	Transfer Parity

Mechanical Implementation

Because the iLBX bus uses the P2 connector of the MULTIBUS form factor, the iLBX bus "shares" a MULTIBUS chassis with the MULTIBUS backplane system bus in the system design. The iLBX mechanical specifications are synonymous with the MULTIBUS specifications for board-to-board spacing, board thickness, component lead length, and component height above the board. The iLBX bus interconnection can use either flexible ribbon cable or a rigid backplane. The iLBX bus interconnect maximum length is limited to 10 cm (approximately 4 inches); that is sufficient to span 5 card slots across two connected chassis. Figure 2 shows an iLBX bus cable assembly.

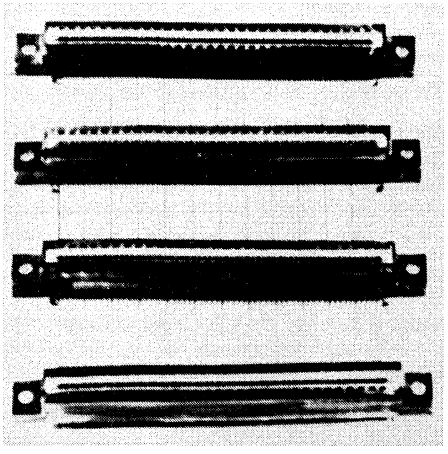


Figure 2. Typical iLBX™ Bus Interface Cable Assembly

Electrical Characteristics

DC SPECIFICATIONS

Table 2

Signal Name	Driver Type	Termination (to +5 Vdc At Master	Min Driver Requirements			Max Receiver Requirements		
			High	Low	Load Cap.	High	Low	Load Cap.
DB15–0	TRI-STATE	10 KΩ	0.6 mA	9 mA	75 pF	0.15 mA	2 mA	18 pF
TPAR*	TRI-STATE	10 KΩ	0.6 mA	9 mA	75 pF	0.15 mA	2 mA	18 pF
AB23–0	TRI-STATE	None	0.4 mA	20 mA	120 pF	0.10 mA	5 mA	30 pF
R/$\overline{W}$	TRI-STATE	None	0.2 mA	8 mA	75 pF	0.05 mA	2 mA	18 pF
BHEN	TRI-STATE	None	0.2 mA	8 mA	75 pF	0.05 mA	2 mA	18 pF
LOCK*	TRI-STATE	None	0.2 mA	8 mA	75 pF	0.05 mA	2 mA	18 pF
SMRQ*	TTL	10 KΩ	0.05 mA	2 mA	20 pF	0.05 mA	2 mA	18 pF
SMACK*	TTL	None	0.05 mA	2 mA	20 pF	0.05 mA	2 mA	18 pF
†ASTB*	TRI-STATE	10 KΩ	0.2 mA	9 mA	75 pF	0.05 mA	2 mA	18 pF
†DSTB*	TRI-STATE	10 KΩ	0.2 mA	9 mA	75 pF	0.05 mA	2 mA	18 pF
ACK*	Open Coll.	330 Ω	N.A.	20 mA	45 pF	0.05 mA	2 mA	18 pF

†At slave, additional series RC termination to GND (100 Ω, 10 pF).

SPECIFICATIONS

Word Size

Data: 8 and 16-bit

Memory Addressing

24-bits—16 megabyte—direct access

Bus Bandwidth

9.5 megabytes/sec: 8-bit
19 megabytes/sec: 16-bit

BUS TIMING

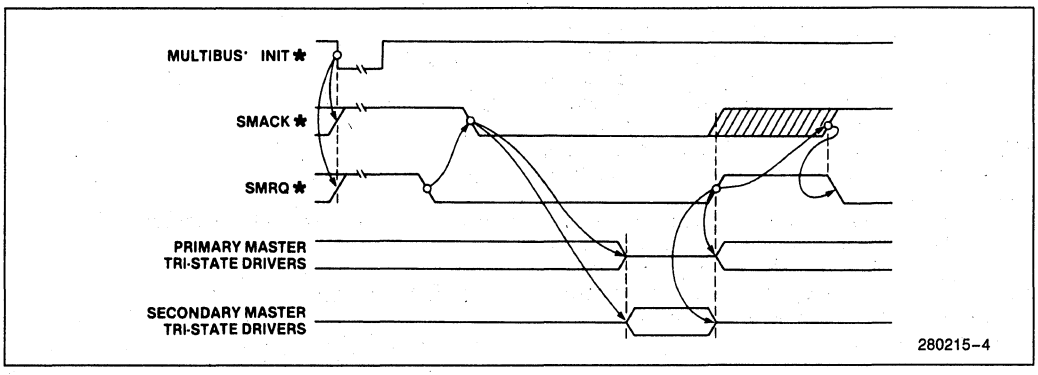


Figure 3. iLBX™ Bus Granting Timing Chart

16-Bit Transfer Timing

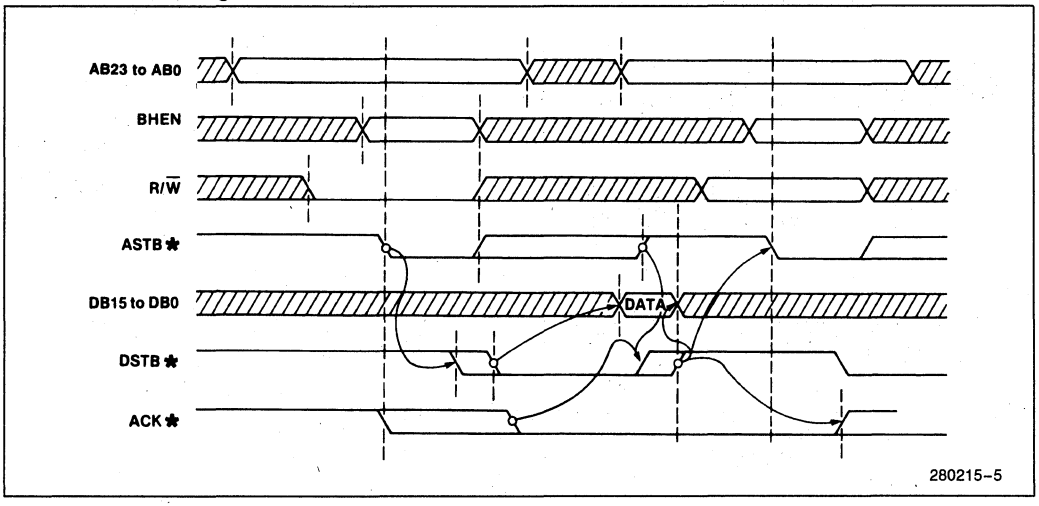


Figure 4. Write Data-to-Memory

BUS TIMING (Continued)

16-Bit Transfer Timing (Continued)

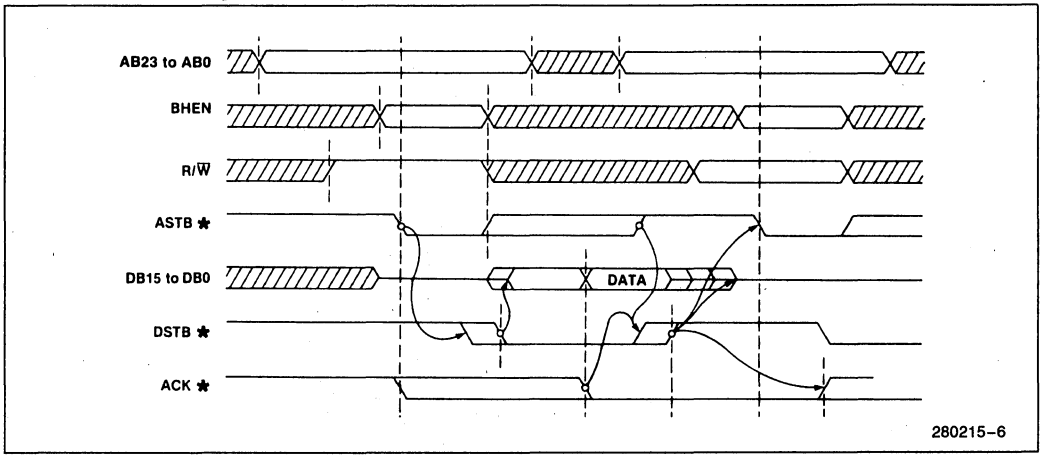


Figure 5. Read Data-From-Memory

Physical Characteristics

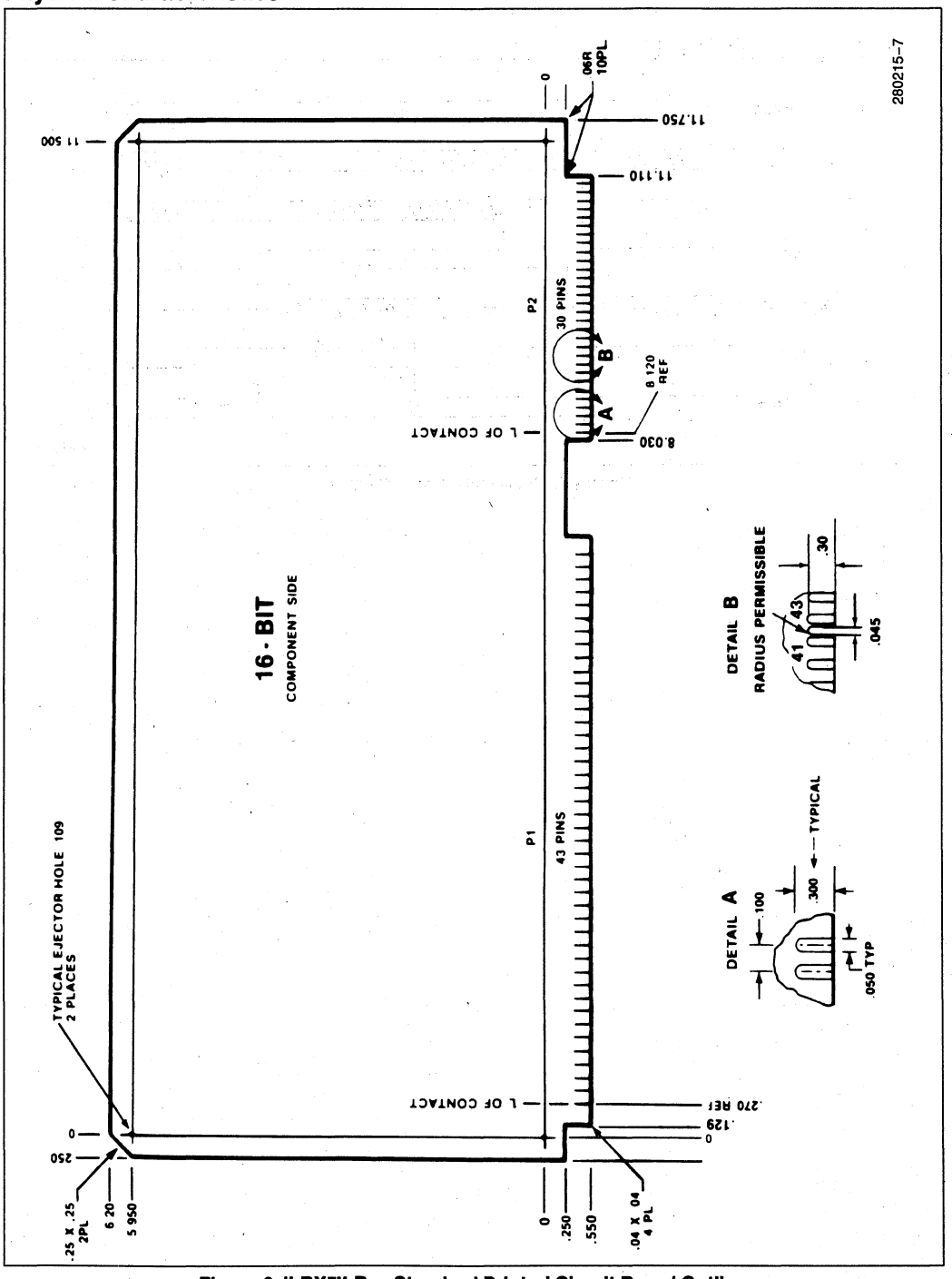


Figure 6. iLBX™ Bus Standard Printed Circuit Board Outline

Cables and Connectors

Table 3. Cable and Receptacle Vendors

iLBX™ Bus Compatible Cable		
Vendor	**Vendor Part No.**	**Conductors**
T & B Ansley	171-60	60
T & B Ansley	173-60	60
3M	3365/60	60
3M	3306/60	60
Berg	76164-060	60
Belden	9L28060	60
Spectrastrip	455-240-60	60
iLBX™ Bus Compatible Receptacles		
Vendor	**Vendor Part No.**	**Pins**
Kelam	RF30-2803-5	60
T & B Ansley	A3020 (609-6025 Modified)	60

Environmental Characteristics

OPERATING

Temperature: 0°C to 60°C

Relative Humidity: 0% to 85%; non-condensing

Reference Manuals

210883-002—MULTIBUS Architecture Reference Book

MULTIBUS® II
Single Board Computers

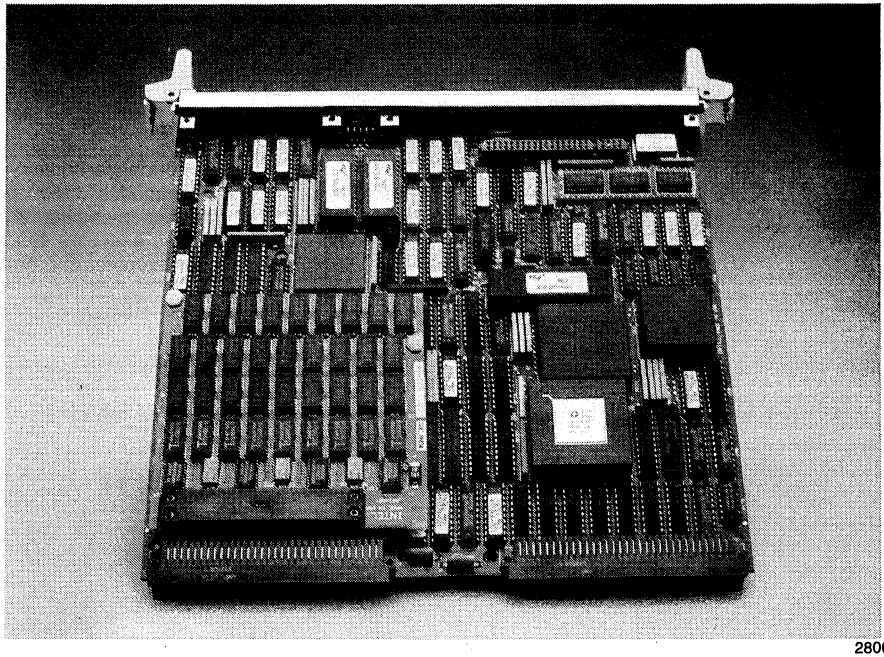
10

iSBC® 386/116 AND 386/120 MULTIBUS® II SINGLE BOARD COMPUTERS

- **High Performance 32-bit 386™ Processor Operating at 16 MHz or 20 MHz**
- **80387 Numerics Co-Processor Providing IEEE 754 Floating Point Instruction Set, Operating at 16 MHz or 20 MHz**
- **64K byte Static RAM Cache Providing Zero Wait State Reads**
- **1, 2, 4 or 8M Bytes of On-Board Dual-Ported Dynamic RAM Memory with Parity Error Detection, Expandable to 16M Bytes**
- **One RS 232C Serial I/O Port**
- **82258 DMA Controller Providing 4 High Performance DMA Channels**
- **32-Bit MULTIBUS®II Parallel System Bus (IEEE 1296) Interface with Full Message Passing Capability**
- **8-, 16-Bit iSBX™ Bus (IEEE P959) Interface with DMA for I/O Expansion**
- **Resident Firmware to Support Built-In-Self-Test (BIST) Power-Up Diagnostics**
- **MULTIBUS II Interconnect Space for Software Configurability and Diagnostics**

The iSBC 386/116 and 120 MULTIBUS II Single Board Computers are based on Intel's 386 high performance 32-bit microprocessor. The 386 CPU maintains software compatibility with the entire 8086 microprocessor family and delivers new performance standards for microcomputer-based systems. Four versions of the iSBC 386/116 and 120 boards are offered: the M01, which contains 1M byte of DRAM; the M02, which contains 2M bytes of DRAM; the M04, which includes 4M bytes of DRAM; and the M08 which contains 8M bytes of DRAM. An optional memory expansion module can be added to expand the iSBC 386/116 or 120 board's resident memory to a maximum of 16M bytes.

The 64K byte static RAM cache enables the 386 CPU to execute at its full potential performance, while the MULTIBUS II bus provides an interface for reliable, high performance multiprocessing.



280631-1

October 1988
Order Number: 280631-001

FUNCTIONAL DESCRIPTION

Overview

The iSBC 386/116 and 120 boards utilize Intel's 386 32-bit microprocessor. The advanced capabilities of the MULTIBUS II architecture coupled with the high performance and compatibility features of the 386 CPU, provide the designer with a superior 32-bit solution for multiprocessing applications. By using the MULTIBUS II architecture, multiprocessing systems are enhanced through advanced bus features including: 21-board distributed arbitration, virtual interrupts, hardware-assisted message passing, bus parity for high reliability, and software configurability using interconnect address space. The MULTIBUS II parallel system bus (iPSB) interface on the iSBC 386/116 and 120 boards support full message passing and dual-port architectures and is fully compatible with other SBCs based on the MULTIBUS II (IEEE 1296) bus specification.

The iSBC 386/116 and 120 boards are offered in four versions: M01, M02, M04 and M08 which contain 1, 2, 4 and 8M bytes of resident DRAM memory respectively. This memory is physically located on an expansion board, and can be accessed directly from the iSBC 386/116 or 120 board's local bus or by another CPU over the iPSB bus. This dual-port memory can be expanded to a maximum of 16M bytes though the addition of a second Intel iSBC MM01, MM02, MM04 or MM08 (1, 2, 4 or 8M byte) memory expansion module. Parity error detection is included on all resident DRAM memory.

Architecture

The iSBC 386/116 and 120 logic consists of eight resource modules and three interfaces connected together over an on-board local bus. The resources include the 386 CPU, the 80387 numeric co-processor, the 82258 DMA controller, the dual-port DRAM memory, the SRAM cache memory, the EPROM memory with BIST software, the programmable timers and the interrupt controllers. Interfaces included are the iPSB parallel system bus, the iSBX I/O bus and the RS 232C serial I/O interface. A block diagram of the iSBC 386/116, 120 board is shown in Figure 1. The following text describes each of the resources and interfaces.

386™ PROCESSOR

Intel's 386 CPU is the central processor for the iSBC 386/116 and 120 boards. This is the first 32-bit member of Intel's 8086 family of microprocessors. At 16 MHz and 20 MHz, the 386 is capable of executing at sustained rates of 4 and 5 million 32-bit instructions per second, respectively. This performance is made possible through a state-of-the-art design combining advanced VLSI semiconductor technology, a pipelined architecture, address translation caches and a high performance local bus interface.

The 386 processor provides a rich, generalized register and instruction set for manipulating 32-bit data and addresses. Features such as scaled indexing and a 64-bit barrel shifter ensure the efficient addressing and fast instruction processing. Special emphasis has been placed on providing optimized instructions for high-level languages and operating system functions. Advanced functions, such as hardware-supported multitasking and virtual memory support, provide the foundation necessary to build the most sophisticated multitasking and multiuser systems. Many operating system functions have been placed in hardware to enhance execution speed. The integrated memory management and protection mechanism translates virtual addresses to physical addresses and enforces the protection rules necessary for maintaining task integrity in a multiprocessing environment.

The 386 CPU provides access to the large base of software developed for the 8086 family of microprocessors. Binary code compatibility allows execution of existing 16-bit applications without recompilation or reassembly, directly in a virtual 8086 environment. Programs and even entire operating systems written for 8086 family processors can be run as tasks under 32-bit operating systems written for the 386 CPU.

80287 NUMERIC CO-PROCESSOR

The 80387 is a high-performance floating-point co-processor that takes numerics functions which would normally be performed in software by the 386 microprocessor and instead executes them in hardware. The instruction set executed by the 80387 is compatible with the IEEE 754 floating point standard, with high-precision 80-bit architectures and full support for single, double and extended precision operations. The 80387 executes floating point operations at a rate of 1.5M Whetstones per second at 16 MHz, and 1.86M Whetstones per second at 20 MHz.

82258 ADVANCED DMA CO-PROCESSOR

The 82258 is a high performance 4 channel DMA co-processor. Unlike other DMA devices, the 82258 has processing capabilities. Its command chaining feature and data manipulation capabilities (compare, verify, translate), allow the 82258 to execute simple

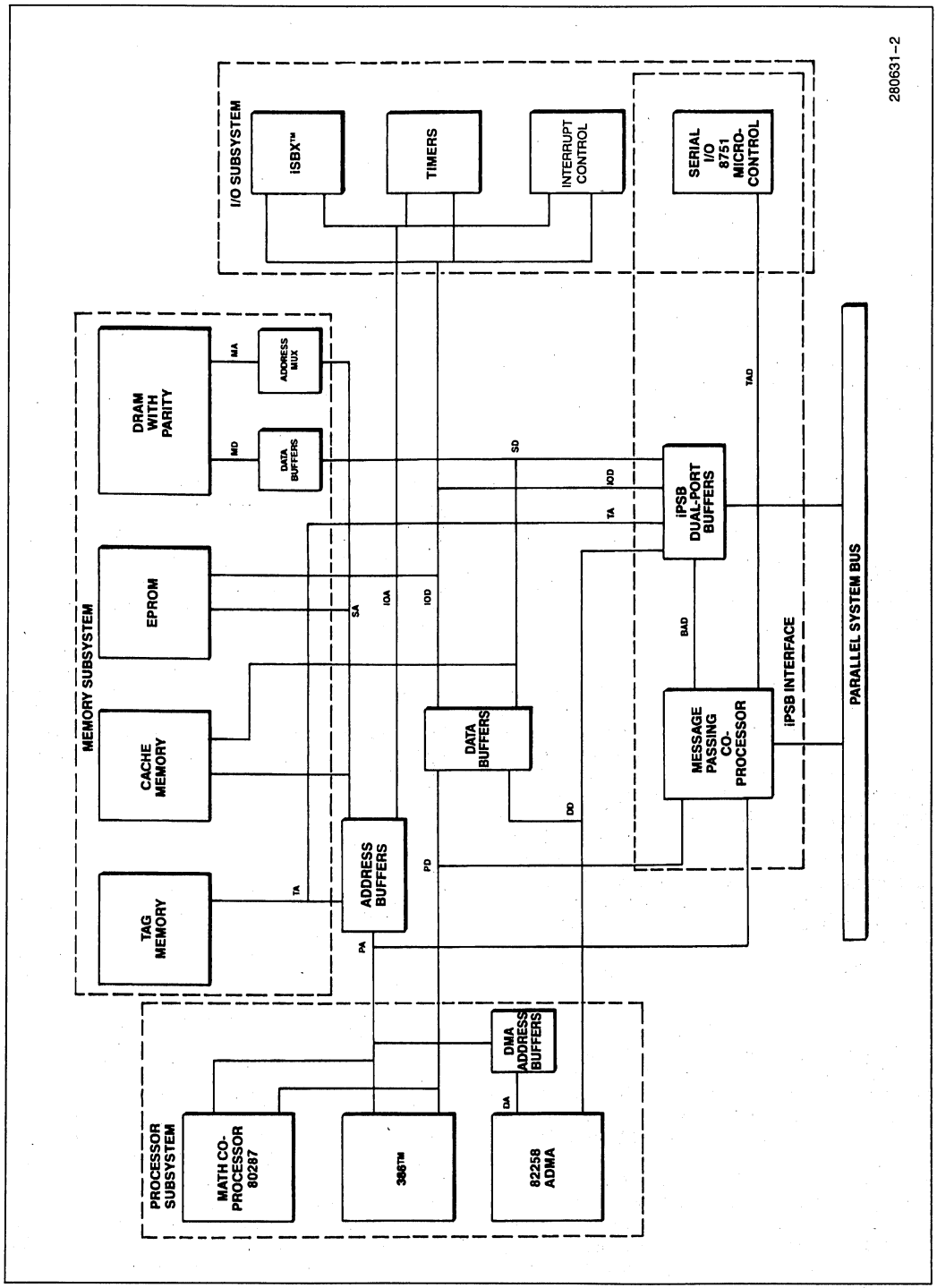


Figure 1. Block Diagram of the iSBC® 386/116, 386/120 Board

input/output programs without processor intervention. This allows the 386 CPU more time for general purpose processing, thus improving total system performance. The 82258 shares ownership of the on-board local bus via the 386 processor's HOLD, HOLD ACKNOWLEDGE co-processor protocol. The maximum percentage of on-board local bus utilization by the 82258 is user programmable.

The four 82258 channels are allocated to iSBC 386/116 or 120 on-board resources as shown in Table 1. Special logic on the boards allows the 82258 to transfer data to and from the message passing co-processor (MPC) 32-bits at a time using single cycle mode. Using this mode, the 82258 (which operates at 8 MHz on 386/116 and 10 MHz on 386/120) can load or unload an MPC solicited message (from or to resident DRAM) at a sustained rate of 10.7M bytes and 13.3 Mbytes per second, respectively.

Table 1. DMA Channel Allocation

Channel	Function
0	iSBX DMA support
1	iSBX DMA support
2	MPC Solicited Message Receive
3	MPC Solicited Message Transmit

DUAL-PORTED DYNAMIC RAM

The iSBC 386/116 and 120 boards include 1, 2, 4 or 8M bytes of DRAM depending upon the version. This memory can be extended to a maximum of 16M bytes through the addition of an Intel iSBC MM01, MM02, MM04 or MM08: 1, 2, 4 or 8M byte memory expansion module. The DRAM refresh control, dual-port control and parity generation/checking logic is physically located on the baseboard, while the actual DRAM components are located on low-profile surface mount expansion boards. Each iSBC 386/116 or 120 board is shipped with one expansion memory module installed and may be expanded to contain two total memory expansion modules. The memory expansion module mechanics are shown in Figure 2.*

***NOTE:**
Only one single-sided memory module (MM01 or MM04) installed onto the iSBC 386/116 or 120 board will fit within one MULTIBUS II slot. A double-sided module (MM02 or MM08) or any stack of two modules will require two MULTIBUS II slots.

Parity error detection is provided on a byte-by-byte basis. The parity logic normally generates and checks for odd parity with detected errors signaled via an on-board LED and a CPU interrupt. Even parity can be forced to generate a parity error for diagnostic purposes.

The DRAM is accessible from both the on-board local bus and the iPSB bus. The amount of memory accessible from the iPSB bus and the iPSB address aliasing values are dynamically configurable via interconnect space registers.

CACHE MEMORY

The cache memory on the iSBC 386/116 and 120 boards allow zero wait-state accesses to memory when the data requested is resident in the cache memory. The static RAM cache has 16,384 32-bit data entries with 8-bit "tag" fields. Each 32-bit DRAM memory location maps to one (and only one) cache data entry. The "tag" fields are used to determine which 32-bits of DRAM memory currently resides in each cache data entry. The combination of a direct mapped cache data array and a tag field ensures data integrity and accurate, high performance identification of cache "hits".

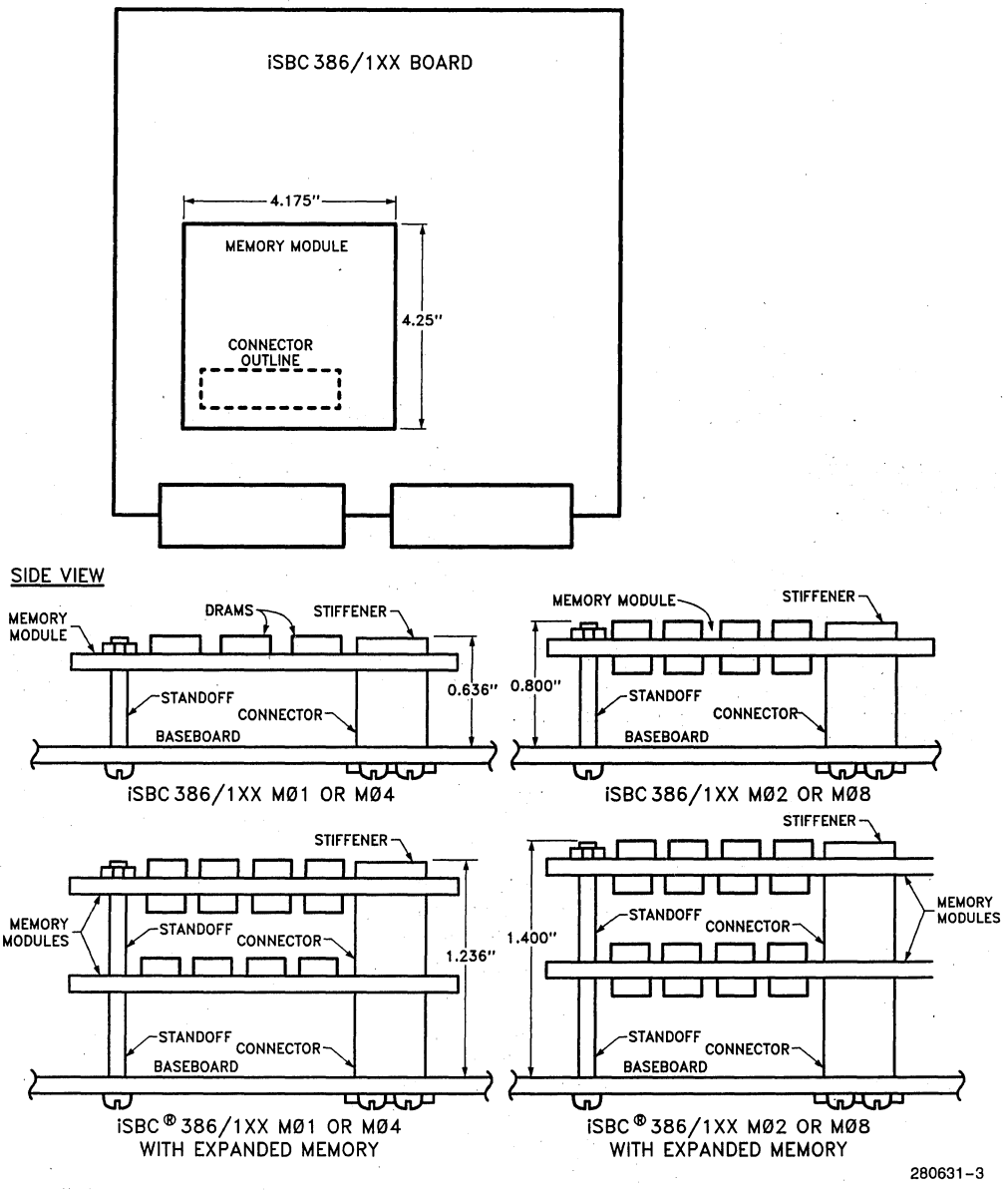
Data integrity is maintained for cache "misses" (DRAM memory READs not in the cache) and DRAM memory WRITEs through a simple, yet effective replacement algorithm. 386 CPU generated cache READ "misses" cause the data field of the cache entry corresponding to the addressed memory to be filled from the DRAM array and the tag field to be updated. All iPSB or ADMA READs are treated as cache "misses", except that the cache is not updated. All WRITE "hits", local and iPSB generated, cause the cache data field to be updated. WRITE "misses" do not update the cache. The cache memory size and replacement algorithm are designed to optimize both the probability of cache "hits" and local bus utilization.

EPROM MEMORY

Two 32-pin JEDEC EPROM sites capable of supporting up to 512K bytes of EPROM (using 27020 EPROMs) are supplied on the iSBC 386/116 and 120 boards. These sites, as shipped, contain built-in-self-test power-up diagnostics residing in two preprogrammed 27512 EPROMs. These EPROMs may be replaced by the user. Jumper configurations allow the use of 2764, 27128, 27256, 27512, 27010, and 27020 EPROMs.

8254 PROGRAMMABLE TIMERS

The iSBC 386/116 and 120 boards contain an Intel 8254 component which provides three independent programmable 16-bit interval timers. These may be used for real-time interrupts or time keeping operations. Outputs from these timers are routed to one of the two 8259A interrupt controllers to provide software programmable real-time interrupts.



NOTE:
1. The iSBC 386/1XX M01 or M04 fits within one MULTIBUS II slot. The iSBC 386/1XX M02 or M08, or any iSBC 386/1XX with a stack of two memory modules will require two MULTIBUS II slots.

Figure 2. iSBC® 386/116 and 120 Boards Memory Module Mechanics

INTERRUPT CONTROL

Two Intel 8259A programmable interrupt controllers on the iSBC 386/116 and 120 boards are used in a master-slave configuration for prioritizing up to 15 separate on-board interrupt sources. The devices and functions are listed in Table 2.

The MULTIBUS II iPSB bus utilizes virtual interrupts (called unsolicited messages) for board-to-board signaling. The bus interface component (MPC) queues-up incoming virtual interrupts from the iPSB bus and generates a single message interrupt (MINT) signal. This signal is connected into one of the 8259A interrupt controllers for prioritization and interruption of the host 386 CPU. Error conditions occurring on the iPSB bus will cause the MPC to generate an error interrupt (EINT) signal. This signal is connected to another 8259A interrupt input.

Other interrupt sources come from the 82258 DMA controller, the 8254 timers, the iSBX interface, the 8751 serial port, and the DRAM parity checker.

SERIAL I/O INTERFACE

One RS 232C compatible serial I/O port is provided via the Intel 8751 microcontroller. This port is configured as a data terminal equipment (DTE) asynchronous serial port. Mechanically, the serial port exits through the iSBC 386/116 or 120 board's front panel via a 9-pin D-shell connector.

iPSB BUS INTERFACE

The MULTIBUS II parallel system bus interface is implemented by Intel's MPC (message passing coprocessor) and a pre-programmed 8751 microcontroller. This interface supports full arbitration, transfer and error checking features as defined in the iPSB specifications. In addition, the interface supports advanced features of the iPSB bus including hardware message passing and autoconfiguration through geographic addressing.

The MPC component contains nine 32-byte buffers which are used to decouple iPSB bus traffic from iSBC 386/116 or 120 local bus traffic through the concept known as message passing. These nine buffers are utilized as follows: four buffers queue-up incoming unsolicited messages, one buffer stores an out-going unsolicited message, two buffers are used to double-buffer an out-going solicited message, and two buffers are used to double-buffer an incoming solicited message. These buffers are capable of transferring data packets over the iPSB bus at its maximum transfer rate. Unsolicited messages include address and type fields and 28 bytes of user-defined data, and are transferred over the iPSB bus in 900 ns. Solicited messages are automatically divided into small packets, with each packet containing address and type fields and 32 bytes of user-defined data. Each solicited message packet is transferred over the iPSB bus in 1000 ns.

Table 2. 8259A Interrupt Sources

Device	Function	Number of Interrupts
MPC-MINT	Signals arrival of virtual interrupt over iPSB bus, solicited input complete, transmit FIFO not full or transmit error	1
MPC-EINT	Signals error condition on the iPSB bus	1
82258 DMA	Transfer complete	1
8254 Timers	Timers 0, 1, 2 outputs, function determined by timer mode	3
8751 Serial Port	Serial diagnostic port requests	1
iSBX Interface	Function determined by iSBX bus multimodule board	4
DRAM Parity Checker	Signals parity error	1

The 8751 component implements the iPSB geographic addressing feature called Interconnect space. Read-only registers are used to hold information such as board type and revision level. Software configurable registers are used for auto-configurability, local or remote diagnostics and software controlled reset. In addition, the 386 CPU executes power-up built-in self tests of the various resources on the iSBC 386/116 and 120 boards. The results of these tests are reported via registers in interconnect space. After successfully completing its BIST routines, the 386 CPU must clear the reset-not-complete register. If, after 30 seconds, the reset-not-complete has not been cleared, the 8751 resets the local bus and holds it in a reset state. In this way, only a few components on the iSBC 386/116 or 120 board must be functional to allow the iPSB bus to operate.

iSBX™ BUS INTERFACE

One iSBX connector, capable of supporting one single- or double-wide, 8- or 16-bit iSBX MULTIMODULE board, is provided on the iSBC 386/116 and 120 boards for the addition of an optional I/O module. Two DMA channels from the 82258 can be used with iSBX modules which require DMA support.

SPECIFICATIONS

Word Size

Instruction — 8-, 16-, 24-, 32-, 40-bit
Data — 8-, 16-, 32-bit
Floating Point Data — 80-bit

Clock Rates

	386/116	386/120
386™ CPU	16 MHz	20 MHz
80387 Numeric Co-processor	16 MHz	20 MHz
82258 DMA	8 MHz	10 MHz

Dual-Port DRAM Memory

DEFAULT CAPACITY

iSBC 386/116 M01—1M byte
iSBC 386/116 M02—2M byte
iSBC 386/116 M04—4M byte
iSBC 386/116 M08—8M byte

iSBC 386/120 M01—1M byte
iSBC 386/120 M02—2M byte
iSBC 386/120 M04—4M byte
iSBC 386/120 M08—8M byte

EXPANSION MODULES

iSBC MM01—1M byte
iSBC MM02—2M byte
iSBC MM04—4M byte
iSBC MM08—8M byte

MAXIMUM CAPACITY—16M BYTES

EPROM Memory

Default — 128K byte using two pre-programmed 27512 EPROMs
Capacity — Two 24-, 28- or 32-pin JEDEC-compatible devices

EPROM	Memory Capacity
2764	16 KB
27128	32 KB
27256	64 KB
27512	128 KB
27010	256 KB
27020	512 KB

Timers

Capability — Three independently programmed 16-bit interval timers
Input Frequency — 1.25 MHz ±0.1%
Output Period — 1.6 μs to 52.4 ms

Interrupt Capability

Incoming Interrupts — 255 individual and 1 broadcast from iPSB bus 12 local sources (see Table 2)
Outgoing Interrupts — 255 individual and 1 broadcast to IPSB bus

Serial Port Interface

RS 232C Electrical
Asynchronous, DTE only
9-pin D-shell connector
Baud rates: 9600, 4800, 2400, 1200, 300, 110 bits/sec

iSBX Interface

Capability — One 8- or 16-bit, single- or double-wide iSBX module
Compliance Code — D16/16 DMA

iPSB Interface

Capability— Requesting and replying agent supporting 8-, 16-, 24- and 32-bit transfers, parity bit generation and checking, unsolicited and solicited message passing, and autoconfiguration through interconnect space.

Physical Dimensions

Length: 220 mm (8.6 in.)
Width: 233 mm (9.2 in.)
Front Panel Height: 19.2 mm (0.76 in.)

Power Requirements

5V: 11.14 Amps
12V: 0.046 Amps
−12V: 0.041 Amps
Voltage tolerance ±5%

Temperature Range and Airflow Requirements

Storage Temperature: −40°C to +70°C
Operating Temperature: 0°C to +55°C
Airflow: 200 LFM minimum

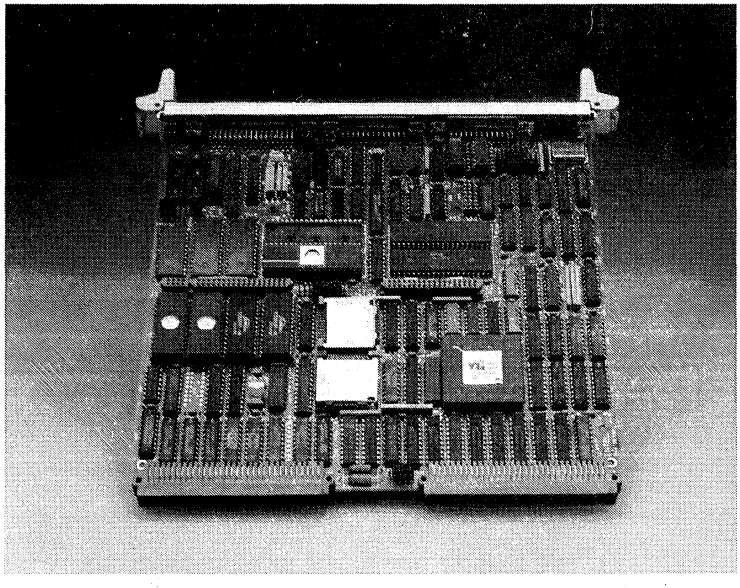
ORDERING INFORMATION

Part Number	Description
SBC 386/116 M01	16 MHz 386 CPU-based MULTIBUS II CPU board with 1M byte memory
SBC 386/116 M02	16 MHz 386 CPU-based MULTIBUS II CPU board with 2M byte memory
SBC 386/116 M04	16 MHz 386 CPU-based MULTIBUS II CPU board with 4M byte memory
SBC 386/116 M08	16 MHz 386 CPU-based MULTIBUS II CPU board with 8M byte memory
SBC 386/120 M01	20 MHz 386 CPU-based MULTIBUS II CPU board with 1M byte memory
SBC 386/120 M02	20 MHz 386 CPU-based MULTIBUS II CPU board with 2M byte memory
SBC 386/120 M04	20 MHz 386 CPU-based MULTIBUS II CPU board with 4M byte memory
SBC 386/120 M08	20 MHz 386 CPU-based MULTIBUS II CPU board with 8M byte memory
SBC MM01	1M byte memory expansion module
SBC MM02	2M byte memory expansion module
SBC MM04	4M byte memory expansion module
SBC MM08	8M byte memory expansion module
451833-001	iSBC 386/116 and 386/120 Single Board Computer Users Guide

iSBC® 286/100A MULTIBUS®II SINGLE BOARD COMPUTER

- 8 MHz 80286 Microprocessor with Optional 80287 Numeric Data Co-Processor
- MULTIBUS® II iPSB (Parallel System Bus) Interface with Full Message Passing Capabilities and up to 4 Gigabytes of Memory Addressability on the Bus
- High-Speed Memory Expansion with MULTIBUS II iLBX II (Local Bus Extension) Interface Addresses up to 16 MBytes of Local and/or Dual Port Memory
- Two iSBX Bus Interface Connectors for I/O Expansion Bus
- Four DMA Channels Supplied by the 82258 Advanced DMA Controller with 8 MBytes/sec Transfer Rate
- MULTIBUS® II Interconnect Space for Software Configurability and Self-Test Diagnostics
- Resident Firmware Supports Self-Test Power-Up Diagnostics and On-Command Extended Self-Test Diagnostics
- Two Programmable Serial Interfaces, one RS232C (DCE or DTE), the other RS232C or RE422A/RS449 Compatible
- Two 28-pin JEDEC Sites for up to 128 KBytes of Local Memory Using SRAM, NVRAM, EEPROM, and EPROM
- 24 Programmable I/O Lines Configurable as SCSI Interface, Centronics Interface, or General Purpose I/O

The iSBC 286/100A Single Board Computer is part of Intel's family of MULTIBUS II CPU boards that utilizes the advanced features of the MULTIBUS II System Architecture. It is ideally suited for a wide range of OEM applications. The combination of the 80286 CPU, the Message Passing Coprocessor (MPC), the MULTIBUS II Parallel System Bus (iPSB bus), and the Local Bus Extension (iLBX II bus) makes the iSBC 286/100A board suited for high performance, multiprocessing system applications in a multimaster environment. The board is a complete microcomputer system on a 220mm x 233mm (8.7 x 9.2 inch) Eurocard form factor with pin and socket DIN connectors.



280076-1

March 1987
Order Number: 280076-004

Overview

The iSBC 286/100A Single Board Computer combines the 80286 microprocessor with the Message Passing Component (MPC) on a single board within the MULTIBUS II system architecture. This offers a message passing based high performance multiprocessing solution for system integrators and designers. Figure 1 shows a typical MULTIBUS II multiprocessing system configuration. Overall system performance is enhanced by the Local Bus Extension (iLBX II) which allows 0 wait state high speed memory execution.

Architecture

All features of the MULTIBUS II architecture are fully supported by the iSBC 286/100A board including the Parallel System Bus (iPSB), interconnect space, Built-In-Self-Tests (BIST) diagnostics, and full message passing. These features are described in the following sections. In addition to taking advantage of the MULTIBUS II system architecture, the iSBC 286/100A board has complete single board computer capability including two iSBX bus expansion connectors, 80287 numeric data coprocessor option, advanced DMA control, JEDEC memory sites, SCSI configurable parallel interface, serial I/O, and programmable timers. Figure 2 shows the iSBC 286/100A board block diagram.

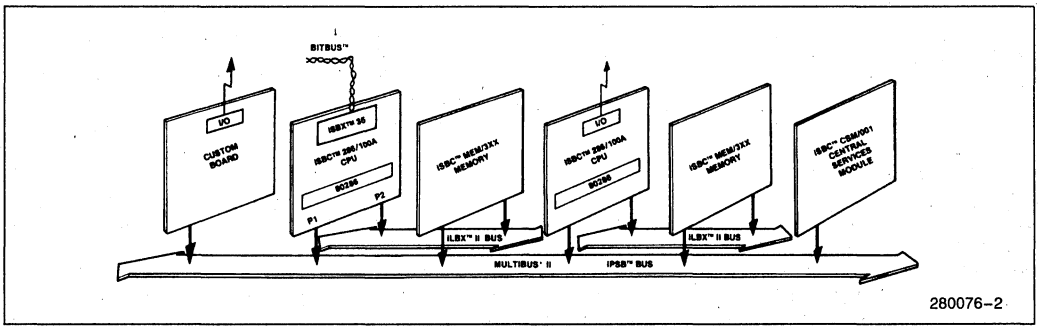


Figure 1. Typical MULTIBUS®II Multiprocessing System Configuration

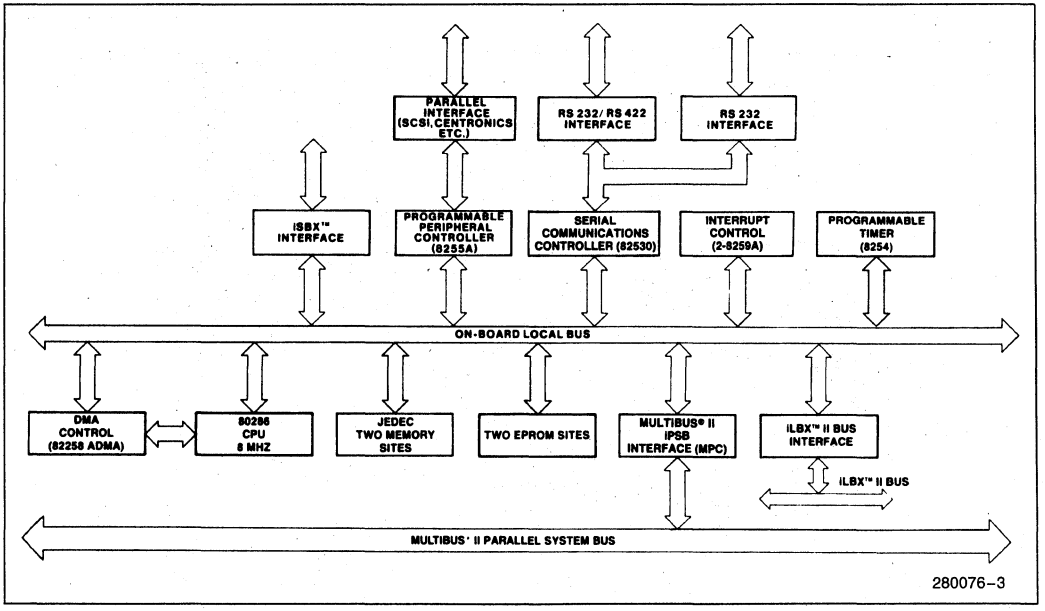


Figure 2. iSBC® 286/100A Board Block Diagram

Central Processing Unit

The central processing unit for the iSBC 286/100A board is the 80286 microprocessor operating at 8.0 MHz clock rate. The 80286 runs 8086 and 80186 code at substantially higher speeds (due to a parallel chip architecture) while maintaining software compatibility with Intel's 8086 and 80186 microprocessors. Numeric processing power may be enhanced with the 80287 numeric data coprocessor. The 80286 CPU operates in two modes: real address mode and protected virtual address mode. In real address mode, programs use real addressing with up to one megabyte of address space. In protected virtual address mode, the 80286 CPU automatically maps 1 gigabyte of virtual address per task into a 16 megabyte real address space. This mode also provides the hardware memory protection for the operating system. The operating mode is selected via CPU instructions.

iPSB Bus Interface

The iSBC 286/100A board has a Message Passing Coprocessor (MPC) component on the base board that contains most of the logic required to operate the Parallel System Bus (iPSB bus) interface. Some of the key functions provided by the MPC include bus arbitration, transfer control, parity generation and checking, and error detection and reporting.

Data transfers between processors via the iPSB bus is defined in the MULTIBUS II architecture through a transfer protocol, a reserved address space, and an information/data block. This interprocessor communication convention is known as message passing. Operations occurring within the reserved address space are called message space operations.

Message passing allows iPSB bus agents to transfer variable amounts of data at rates approaching the maximum bandwidth of the bus. Message passing permits a sustained transfer rate of 2.2 Mbytes per second, and a single message may transfer up to 16 Mbytes from one agent to another. The MPC fully supports message space operations, executes iPSB bus arbitration and executes the message passing protocol independent of the host CPU, leaving the host free to process other tasks.

The MPC supports both solicited and unsolicited message passing capability across the iPSB. An unsolicited message can be thought of as an intelligent interrupt from the perspective of the receiving agent because the arrival of an unsolicited message is unpredictable. Attached to an unsolicited message is one of 255 possible source addresses along with 28 bytes of data attached to the message data field. A solicited message moves large blocks of data between agents on the iPSB bus. The arrival of a solicited message is negotiated between the sending and receiving agents. Data is sent in "packets" with each packet containing four bytes of control information and up to 28 bytes of data. There is no specific limit to the number of packets that may be sent in a single message, but the total message may not transfer more than 16 Mbytes.

The iSBC 286/100A also includes a feature called the iPSB window register that allows the user to selectively access under software control any 256K byte block of memory within the 4 Gigabytes of memory space on the iPSB bus interface.

INTERCONNECT SPACE SUPPORT

Interconnect space is one of four MULTIBUS II address spaces, the other three being memory space, I/O space, and message space. Interconnect space allows software to initialize, identify, configure, and diagnose the boards in a MULTIBUS II system. The Interconnect template consists of 8-bit registers, organized into functional groups called records. There are three types of records, the header record, the function record, and the End of Template record.

The header record provides board and vendor ID information, general status and control information, and diagnostic control. The function record allows the user to configure and/or read the iSBC 286/100A board's hardware configuration via software. The End of Template record identifies the end of the interconnect template.

BUILT IN SELF TEST (BIST) DIAGNOSTICS

MULTIBUS II's Built in Self Test (BIST) diagnostics improve the reliability and error reporting and recovery capability of MULTIBUS II boards. These confidence tests and diagnostics not only improve reliability but also reduce manufacturing and maintenance costs for the OEM user. A yellow LED (LED 1) on the front panel provides a visual indication of the power-up diagnostics status.

Error Reporting and Recovery

The MULTIBUS II Parallel System Bus and the iLBX II bus provides bus transmission and bus parity error detection signals. Error information is logged in the MPC and a bus error interrupt is generated. Information on the error source for reporting or recovery purposes is available to software through the iSBC 286/100A board interconnect space registers.

INTERRUPT CONTROL

In a MULTIBUS II system, external interrupts (interrupts originating off the CPU board) are messages over the bus rather than signals on individual lines. Message based interrupts are handled by the MPC. Two on-board 8259A Programmable Interrupt Controllers (PICs) are used for processing on-board interrupts. One is used as the master and the other as the slave. Table 1 includes a list of devices and functions supported by interrupts.

iSBX® BUS MULTIMODULE™ ON-BOARD EXPANSION

Two iSBX bus MULTIMODULE connectors are provided, one 16- or 8-bit and the other 8-bit. Through these connectors additional on-board I/O functions may be added. The iSBX bus MULTIMODULE boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, and graphics control. The iSBX bus connectors on the iSBC 286/100A board provides all signals necessary to interface to the local on-board bus including 16 data lines and DMA for maximum data transfer rates. MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX bus connectors are also supported. A broad range of iSBX bus MULTIMODULE options are available from Intel. Custom iSBX bus MULTIMODULE boards designed for MULTIBUS or proprietary bus systems are also supported provided the IEEE P959 iSBX bus specification is followed.

NUMERIC DATA CO-PROCESSOR

The 80287 Numeric Data Co-Processor can be installed on the iSBC 286/100A board by the user. The 80287 Numeric Data Co-Processor is connected to dedicated processor signal lines which are pulled to their inactive state when the 80287 Numeric Data Co-Processor is not installed. This enables the user to detect via software that the 80287 socket is occupied. The 80287 Numeric Data Co-Processor runs asynchronously to the 80286 clock. The 80287 Numeric Data Co-Processor operates at 8 MHz and is driven by the 8284A clock generator.

Table 1. Interrupt Devices and Functions

Device	Function	Number of Interrupts
MULTIBUS® II Interface	Message-based Interrupt Request from the iPSB Bus via 84120 Message Interrupt Controller	1 Interrupt from up to 256 sources
8751 Interconnect Controller	BIST Control Functions	1
82530 Serial Controller	Transmit Buffer Empty, Receive Buffer Full and Channel Errors	1 Interrupt from 10 Sources
8254 Timers	Timers 0, 1, 2 Outputs; Function Determined by Timer Mode	3
8255A Parallel I/O	Parallel Port Control	2
iLBX II Bus Interface	Indicates iLBX™ II Bus Error Condition	3
iPSB Bus Interface	Indicates Transmission Error on iPSB Bus	1
iSBX Bus Connector	Function Determined by iSBX Bus MULTIMODULE Board	2
Edge Sense Out	Converts Edge Triggered Interrupt to a Level	1
Bus Error	Indicates Last iPSB Bus Operation Encountered an Error	1
Power-Fail	External/Power-Fail Interrupts	1

DMA CONTROL

Four DMA (Direct Memory Access) channels are supplied on the iSBC 286/100A board by the 82258. The 82258 is an advanced DMA controller designed especially for the 16-bit 80286 microprocessor. It has four DMA channels which can transfer data at rates up to 8 Megabytes per second (8 MHz clock) in an 80286 system. The large bandwidth allows the user to handle very fast data transfer or a large number of concurrent peripherals.

MEMORY CAPABILITIES

The local memory of the iSBC 286/100A board consists of two groups of byte-wide sites. The first group of two sites are reserved for EPROM or ROM and are used for the BIST power-up diagnostic firmware. The second group of two sites support JEDEC standard 28-pin devices.

PARALLEL PERIPHERAL INTERFACE

The iSBC 286/100A board includes a parallel peripheral interface that consists of three 8-bit parallel ports. As shipped, these ports are configured for general purpose I/O. Programmed PAL (Programmable Array Logic) devices and the octal transceiver 74LS640-1 are provided to make it easy to reconfigure the parallel interface to be compatible with the SCSI (Small Computer System Interconnect) peripheral interface. Alternatively, the parallel interface may be reconfigured as a Centronics compatible line printer by adding one PAL and reconfiguring jumpers. Both interfaces may use the 82258 DMA controllers for data transfers.

The SCSI interface allows multiple mass storage peripherals such as Winchester disk drives, floppy disk drives, and tape drives to be connected directly to the iSBC 286/100A board. A sample SCSI application is shown in Figure 3. The SCSI interface is compatible with SCSI controllers such as the Adaptek 4500, DTC 1410, Iomga Alpha 10, Shugart 1601 and 1610, Vermont Research 8403, and Xebec 1410.

The Centronics interface requires very little software overhead since a user-supplied PAL device is used to provide necessary handshake timing. Interrupts are generated for printer fault conditions and a DMA request is issued for every character.

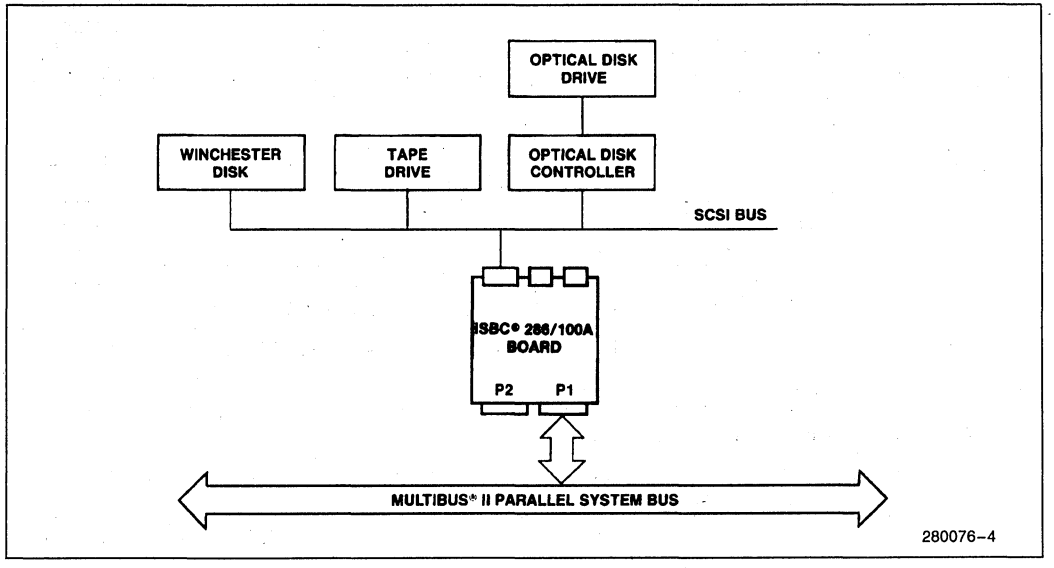


Figure 3. Sample SCSI Applications

SERIAL I/O

The 82530 Serial Communications Controller (SCC) is used to provide two channels of serial I/O. The SCC generates all baudrate clocks and provides loopback capability on both channels. Channel B is RS232C only and is configured as a DCE. Channel A is factory-default configured for DCE RS232C operation. Channel A may be reconfigured by the user for DTE or RS422 operation.

The 82258 ADMA can be programmed to support both channels A and B to perform movement of large bit streams or blocks of data.

PROGRAMMABLE TIMERS

The iSBC 286/100A board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Three of these timers/counters are available to the system designer to generate accurate time intervals under software control. The outputs may be independently routed to the 8259A Programmable Interrupt Controller to count external events. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

SOFTWARE SUPPORT

The iRMX 86 Release 7 Operating System software provides the ability to execute all configurable layers of the iRMX 86 software in the MULTIBUS II environment. Applications in Real Address Mode are supported for the iSBC 286/100A board, including support for the SCSI peripheral interface and all iSBX bus boards. The iRMX 86 Release 7 Operating System also supports all 80286 component applications.

For on-target MULTIBUS II development, use the iSBX 218A or a SCSI controller and a floppy or Winchester drive, or port iRMX application software developed on the System 310, Series II/III, IV to MULTIBUS II hardware.

Language support for the iSBC 286/100A boards real address mode includes Intel's ASM 86, PL/M 86, PASCAL and FORTRAN as well as many third party 8086 languages. Language support for virtual address mode operation includes ASM 286, PL/M 286, PASCAL and C. Programs developed in these languages can be down-loaded from the Intel Series III or Series IV Development System to the iSBC 286/100A board via the iSDM 286 System Debug Monitor Release 2. The iSBX 218A can be used to load iRMX software developed on a System 310. The iSDM 286 monitor also provides on-target program debugging support including breakpoint and memory examination features.

Table 2. Programmable Time Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon request of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

The MULTIBUS II Interconnect Space Registers allow the software to configure boards eliminating much of the need for jumpers and wire wraps. The iSDM 286 Monitor can initialize these registers at configuration time using user-defined variables. The monitor can also automatically configure memory boards, defining the addresses for each board sequentially in relation to the board's physical placement in the card cage. This feature allows for swapping, adding, and deleting of memory boards on a dynamic basis.

SPECIFICATIONS

WORD SIZE

Instruction— 8-, 16-, 24-, 32-, or 40-bits
Data — 8- or 16-bits

SYSTEM CLOCK

CPU — 8.0 MHz
Numeric Co-Processor— 8.0 MHz

CYCLE TIME

Basic Instruction: 8.0 MHz-375 ns; 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., two clock cycles)

Memory Capacity (Maximum)

EPROM: 2732, 8K bytes; 2764, 16K bytes; 27128, 32K bytes; 27256, 64K bytes; 27512, 128K bytes
EEPROM: 2817A, 4K bytes
iRAM: 2186, 16K bytes

NOTE:
Two local sites must contain BIST or user-supplied boot-up EPROM.

I/O CAPABILITY

Parallel: SCSI, Centronics, or general purpose I/O.
Serial: Two programmable channels using one 82530 Serial Communications Controller
Timers: Three programmable timers using one 8254 Programmable Interrupt Controller
Expansion: One 8/16-bit iSBX MULTIMODULE connector and one 8-bit iSBX MULTIMODULE connector

INTERRUPT CAPABILITY

Potential Interrupt Sources— 255 individual and 1 broadcast
Interrupt Levels — 16 vectored requests using two 8259As and the 80286 NMI line

Serial Communications Characteristics

Asynchronous Modes:

— 5–8-bit character; odd, even, or parity; 1, 1.5, or 2 stop bits
— Independent transmit and receive clocks, 1X, 16X, 32X, or 64X programmable sampling rate
— Error Detection: Framing, Overrun and Parity
— Break detection and generation

Bit Synchronous Modes:

— SDLC/HDLC flag generation and recognition
— Automatic zero bit insertion bit and detection
— Automatic CRC generation and detection (CRC 16 or CCITT)
— Abort generation and detection
— I-field residue handling
— SDLC loop mode operation
— CCITT X.25 compatible

Byte Synchronous Modes:

— Internal or external character synchronization (1 or 2 characters)
— Automatic CRC generation and checking (CRC 16 or CCITT)
— IBM Bisync compatible

Common Baud Rates

Baud Rate	Synchronous (x1 Clock)	Asynchronous (x16 Clock)
	Time Constant	Time Constant
64 K	36	—
48 K	49	—
19.2 K	126	6
9600	254	14
4800	510	30
2400	1022	62
1800	1363	83
1200	2046	126
300	8190	510
110	—	1394

Timers

Input Frequencies: 1.23 MHz ±0.1% or 4 MHz ±0.1% (Jumper Selectable)

Output Frequencies/Timing Intervals

	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	500 ns	53.1 ms	1.00 ms	57.9 min
Programmable One-Shot	500 ns	53.1 ms	1.00 ms	57.9 min
Rate Generator	18.8 Hz	2 MHz	0.000290 Hz	1 MHz
Square-Wave Rate Generator	18.8 Hz	2 MHz	0.000290 Hz	1 MHz
Software Triggered Strobe	500 ns	53.1 ms	1.00 ms	57.9 min
Hardware Triggered Strobe	500 ns	53.1 ms	1.00 ms	57.9 min
Event Counter	—	5.0 MHz	—	—

INTERFACES

iPSB Bus: All signals TTL compatible

iLBX II Bus: All signals TTL compatible

iSBX Bus: All signals TTL compatible

SERIAL I/O

Channel A: RS232C/RS422 compatible, configurable as a data set or data terminal

Channel B: RS232C compatible, configured as a data set

Timer: All signals TTI compatible

Interrupt Requests: All signals TTL compatible

CONNECTORS

Location	Function	Part #
P1	iPSB Bus	603-2-IEC-C096-F
P2	iLBX™ II Bus	603-2-IEC-C096-F

PHYSICAL DIMENSIONS

The iSBC 286/100A board meets all MULTIBUS II mechanical specifications as represented in the MULTIBUS II specification (part number 146077).

Double-High Eurocard Form Factor:

Depth:	220 mm (8.7 in.)
Height:	233 mm (9.2 in.)
Front Panel Width:	20 mm (0.784 in.)
Weight:	653 g (1 lb. 7 oz.)

ENVIRONMENTAL REQUIREMENTS

Temperature: (Inlet air) at 200 LFM airflow over boards

Non-operating—−40°C to +70°C

Operating—0 to +55°C

Humidity: Non-operating—95% RH @ 55°C

Operating—90% RH @ 55°C

ELECTRICAL CHARACTERISTICS

The maximum power required per voltage is shown below. These numbers do not include the power required by the optional memory devices, SCSI PALs, or expansion modules.

Voltage (volts)	Max/Typical Current (amps)	Max Power (watts)	BTU	Gram-Calorie
+5	10.31/8.25A	54.39W	3.13	774.2
+12	50/40 mA	630 mW	0.04	9.0
−12	46/37 mA	580 mW	0.03	8.3

REFERENCE MANUALS

ISBC 286/100A Single Board Manual Computer User's Guide (#149093-001)

Intel MULTIBUS II Bus Architecture Specification (#146077)

Manual may be ordered from any Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051

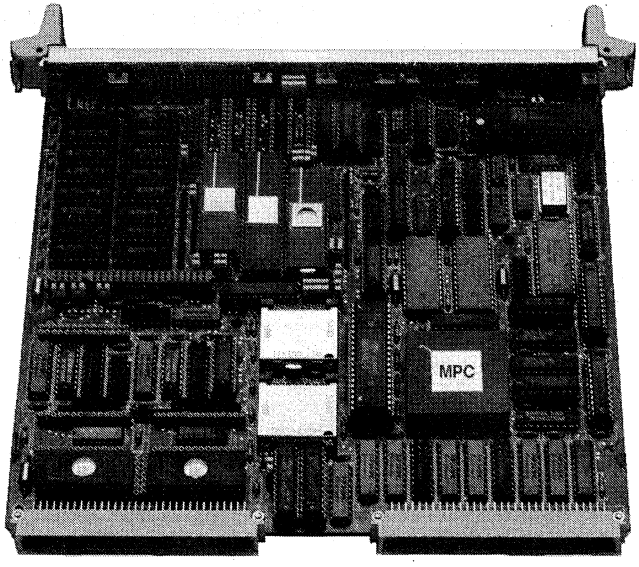
ORDERING INFORMATION

Part Number	Description
SBC 286/100A	MULTIBUS II 80286 based Single Board Computer

iSBC® 186/100 MULTIBUS® II SINGLE BOARD COMPUTER

- **8.0 MHz 80186 Microprocessor with Optional High Speed 8087-1 Numeric Data Coprocessor**
- **Optional 82258 Advanced DMA Controller Providing Four Additional High Peformance DMA Channels**
- **On-Board 512K Bytes DRAM Configurable as Dual Port Memory**
- **MPC (Message Passing Coprocessor) Single Chip Interface to the Parallel System Bus with Full Message Passing Capability**
- **Four (Expandable to Eight) 28-Pin JEDEC Sites for PROM, EPROM, or EEPROM**
- **24 Programmable I/O Lines Configurable as SCSI Interface, Centronics Interface, or General Purpose I/O**
- **Two Programmable Serial Interfaces, One RS 232C and the Other RS 422A with Multidrop Capabilities**
- **Resident Firmware Supporting a Reset Operating Ssytem, a Program Table, and Build-In-Self-Test (BIST) Diagnostics Including Initialization and Power-Up Tests**
- **8- or 16-bit iSBX™ IEEE P959 Interface Connector with DMA Support for I/O Expansion**

The iSBC 186/100 Single Board Computer is a member of Intel's family of microcomputer modules that utilizes the advanced features of the MULTIBUS® II system architecture. The 80186-based CPU board takes advantage of VLSI technology to provide economical, off-the-shelf, computer based solutions for OEM applications. All features of the iSBC 186/100 board, including the single chip bus interface (message passing coprocessor), reside on a 220mm x 233mm (8.7 inches x 9.2 inches) Eurocard printed circuit board and provide a complete microcomputer system. The iSBC 186/100 board takes full advantage of the MULTIBUS II bus architecture and can provide a high performance single CPU system or a powerful element for a highly integrated multi-processing application.



280263-1

*IBM is a registered trademark of International Business Machines

September 1986
Order Number: 280263-001

FUNCTIONAL DESCRIPTION

Overview

The iSBC 186/100 MULTIBUS II Single Board Computer utilizes the 8 MHz 80186 microprocessor to provide a range of solutions for various low cost OEM and end-user applications. Intel's commitment to offering high performance at a cost effective level are evident in the design of the iSBC 186/100 Single Board Computer. The integration of the functions of a general purpose system (CPU, memory, I/O and peripheral control) into a single board computer imply that the total system's board count, power and space requirements, and costs are reduced. Combining these cost advantages with the advanced features of the MULTIBUS II system architecture, the iSBC 1286/100 board is ideal for price sensitive MULTIBUS II multi-processing or single CPU applications. Some of the advanced featues of the MULTIBUS II architecture embodied in the iSBC 186/100 board are distributed arbitration, virtual interrupt capabilities, message passing, iPSB bus parity, and software configurability and diagnostics using interconnect address space.

Architecture

The iSBC 186/100 CPU board supports the iPSB bus features of interconnect address space, Built-In-Self-Test (BIST) diagnostics, solicited and unsolicited message passing, and memory and I/O references. In addition to supporting the iPSB bus architecture, other functions traditionally found on Intel single board computers are included in the iSBC 186/100 board. These traditional capabilities include iSBX bus expansion, high speed 8087-1 numeric coprocessor, advanced DMA control, JEDEC memory site expansion, SCSI, Centronics, or general purpose configurable parallel I/O interface, serial I/O, and programmable timers on the 808186 microprocessor. Figure 1 shows the iSBC 186/100 board block diagram.

Central Processing Unit and DMA

The 80186 is an 8.0 MHz 16-bit microprocessor combining several common system components onto a single chip (i.e., two Direct Memory Access lines, three Interval Timers, Clock Generator, and Programmable Interrupt Controller). The 80186 instruction set is a superset of the 8086 and maintains object code compatiblity while adding additional instructions.

In the basic configuration, Direct Memory Access (DMA) requests are available between the local memory and the bus interface (see Table 1). With the addition of an Advanced DMA (ADMA) 82258 controller, ADMA requests may be generated by either the iSBX interface, the SCSI interface, the bus interface controller, or the serial interface (see Table 2). The addition of the ADMA controller also allows the serial ports to be used in a full-or half-duplex multidrop application.

An additional high performance 8087-1 Numeric Data Coprocessor may be installed by the user to significantly improve the iSBC 186/100 board's numerical processing power. Depending on the application, the high speed 8087-1 will increase the performance of floating point calculations by 50 to 100 times.

Table 1. Basic DMA Configuration

80186	Local Bus
DMA Channel 0	Output DMA iPSB Bus Interface
DMA Channel 1	Input DMA iPSB Bus Interface

Memory Subsystem

The 1M byte memory space of the 80186 is divided into three main sections. The first section is the 512K bytes of installed DRAM, the second section is the window into the global 4G bytes memory space of the iPSB bus (iPSV memory window address space) which starts at 512K bytes and goes up to either 640K bytes or 768K bytes, and the third section is designated for local ROM going from the ending address of the iPSB memory window address space up to, if desired, 1M byte (see Figure 2).

The iSBC 186/100 board comes with 512K bytes of DRAM installed on the board. This memory can be used as either on-board RAM or Dual Port RAM by loading the start and end addresses into the appropriate interconnect registers. The lower boundary address to the iPSB memory window may begin at any 64K byte boundary and the upper boundary address may end at any 64K byte boundary. Refer to the iSBC 186/100 Single Board Computer User's Guide for specific information on programming address spaces into interconnect registers.

The memory subsystem supports 128K bytes or 256K bytes access to the iPSB memory address space. The iPSB memory window base address is fixed at address 512K. The position of the window in the iPSB memory address space is programmable and thus allows the CPU to access the complete 4G byte memory address space of the MULTIBUS II iPSB bus.

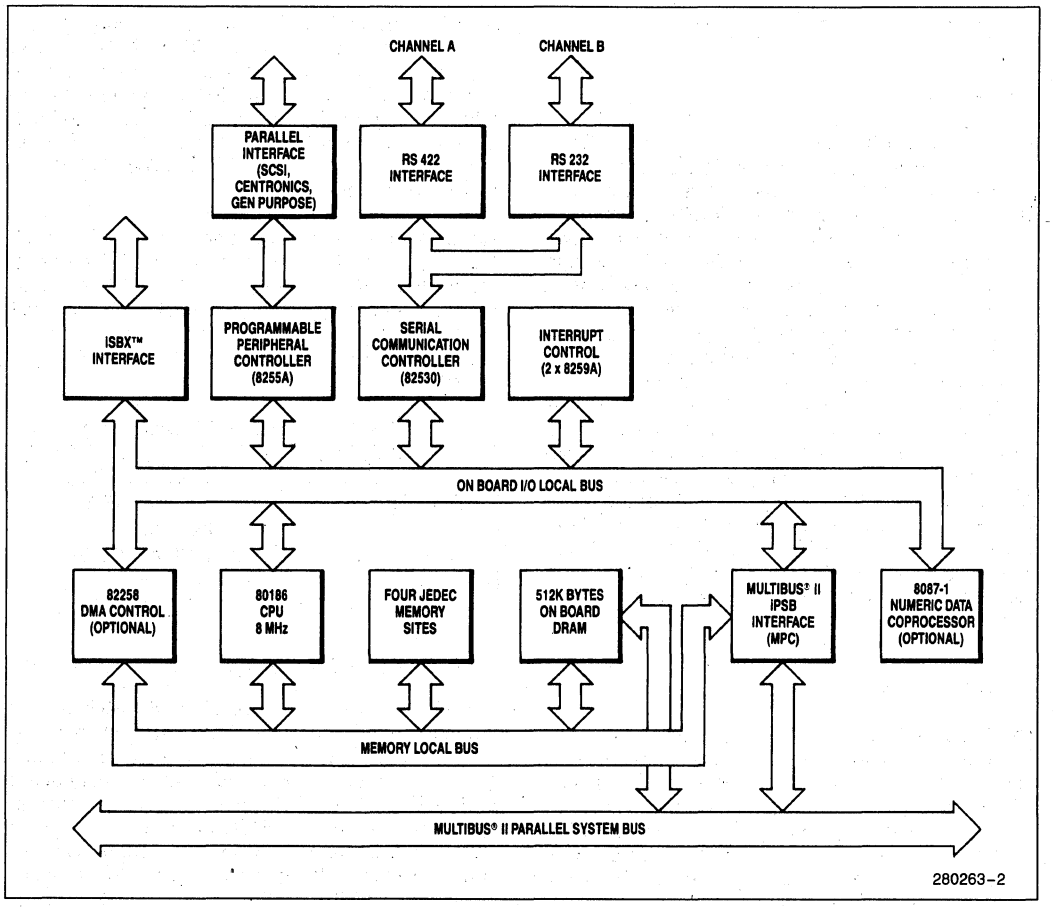


Figure 1. iSBC® 186/100 CPU Board Block Diagram

The ROM space consists of four 28-pin JEDEC sockets which take EPROMs, EEPROMs, or ROMs with 28-pin packages. An iSBC 341 28-pin MULTIMODULE™ EPROM board can be plugged into 2 of the JEDEC sockets and provide up to 512K bytes of ROM memory. Device capacities, which are jumper selectable, are supported from 8K x 8 up to 64K x 8. Once the device capacity is selected, the capacity is uniform for all sockets.

I/O access from the iSBC 186/100 CPU board across the iPSB bus is accomplished by mapping 64K bytes of local I/O access one to one to the iPSB I/O address space. However, only the upper 32K bytes are available to access the iPSB I/O address space because the lower 32K bytes on the iSBC 186/100 board are reserved for local on-board I/O.

On-Board Local Functions

PROGRAMMABLE TIMERS AND INTERRUPT CONTROL

The 80186 microprocessor on the iSBC 186/100 board provides three independent, fully programmable 16-bit interval timers/event counters. In conjunction, two 8259A Programmable Interrupt Controllers (PIC) on the iSBC 186/100 board are used in a master/slave configuration for processing on-board interrupts. At shipment, the 80186 interrupt controller and one PIC are connected as slaves to the master PIC. The first timer on the 80186 microprocessor is routed to the master Programmable Interrupt Controller and the second CPU timer is routed to the slave PIC. This architecture thus supports software

Table 2. DMA Configuration with ADMA Option

80186	Local Bus
DMA Channel 0	Serial Channel B DMA
DMA Channel 1	Serial Channel B DMA or Parallel Port
ADMA 82258	
DMA Channel 0	Input DMA Bus Interface
DMA Channel 1	Output DMA Bus Interface
DMA Channel 2	Half-duplex Fast Serial Interconnect 1 Channel A or Interrupt 1 from iSBX Bus if Used with an iSBC 341 EPROM MULTIMODULE Board
DMA Channel 3	Full-duplex Fast Serial Interconnect 1 Channel A or iSBX Bus DMA Channel if Used with an iSBC 341 EPROM MULTIMODULE board.

NOTE:
When a MULTIMODULE™ expansion board is installed and DMA support is required, then an ADMA controller must also be installed. For additional optional configurations see the *iSBC 186/100 Single Board Computer User's Guide.*

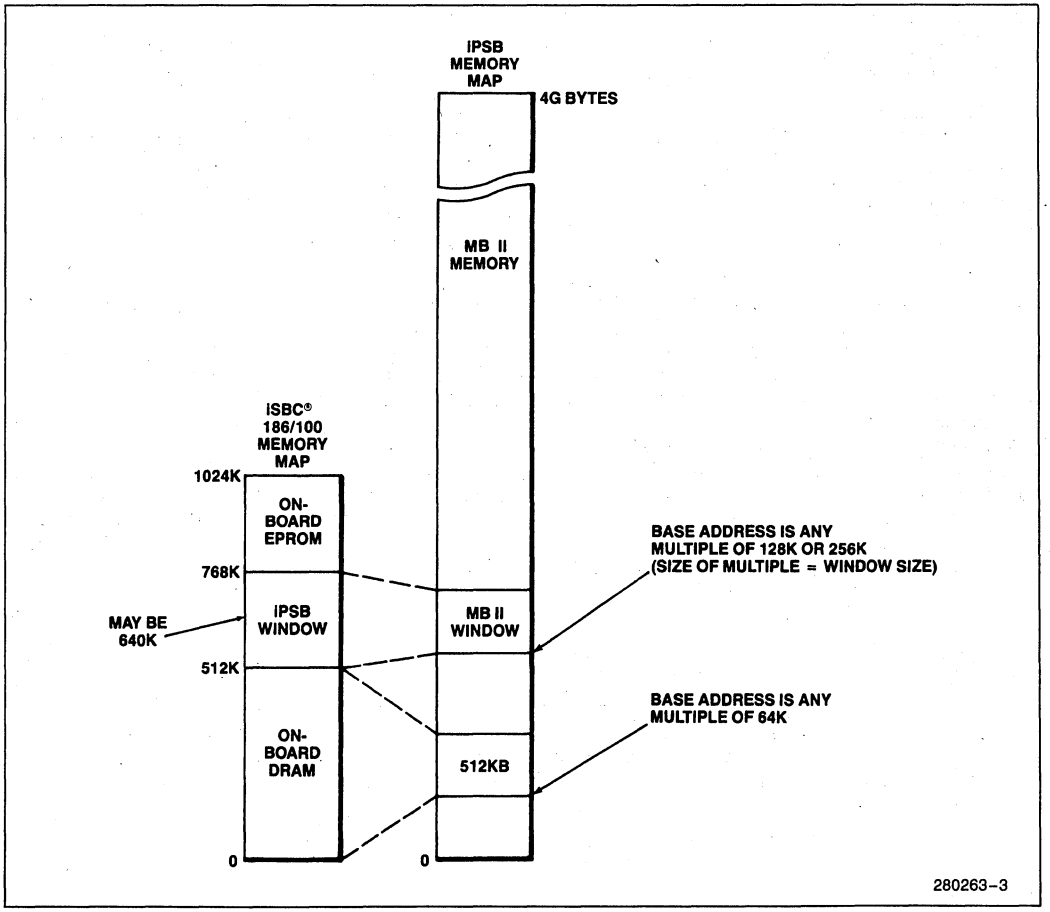


Figure 2. Memory Mapping Diagram

programmable timer interrupts. In addition, direct-vectored interrupt capability of the serial communication controller (SCC) may be used. Figure 3 depicts the interrupts in terms of their priorities.

Interrupt Services	Interrupt Priority
80186 Timer 0	Master Level 0
8087-1 Error Interrupt	1
Message Interrupt	2
iPSB Bus Error Interrupt	3
82530 SCC Interrupt	4
82258 ADMA Interrupt	5
80186 Slave PIC Interrupt	6
8259 Slave PIC Interrupt	7
PPI 0 Interrupt	Slave 0
iSBX Bus Interrupt 0	1
iSBX Bus Interrupt 1	2
Interconnect Space Interrupt	3
80186 Timer 1 Interrupt	4
PPI 1 Interrupt	5
Ground	6 & 7

Figure 3. iSBC® 186/10 Interrupt Priority Scheme

PARALLEL/SCSI PERIPHERAL INTERFACE

The iSBC 186/100 board includes an 8255A parallel peripheral interface that consists of three 8-bit parallel ports. As shipped, these ports are configured for general purpose I/O. Programmed PAL devices (Programmable Array Logic) and the bi-directional octal transceiver 74LS245 are provided to make it easy to reconfigure the parallel interface to be compatible with the SCSI (Small Computer System Interconnect) peripheral interface. Alternatively, the iSBC 186/100 board provides the jumper configuration facilities for operating the parallel interface as an interrupt driven interface for a Centronics compatible line printer by adding one PAL and reconfiguring jumpers. Both interfaces may use the 82258 DMA controller for data transfers if desired.

The SCSI interface allows multiple mass storage peripherals such as Winchester disk drives, floppy disk drives, and tape drives to be connected directly to the iSBC 186/100 board. A sample SCSI application is shown in Figure 4. The SCSI interface is compatible with SCSI controllers such as Adaptek 4500, DTC 1410, Iomega Alpha 10, Shugart 1601 and 1610, Vermont Research 8403, and Xebec 1410.

The Centronics interface requires very little software overhead since a user supplied PAL device is used to provide necessary handshake timing. Interrupts are generated for printer fault conditions and a DMA request is issued for every character.

SERIAL I/O LINES

The iSBC 186/100 board has one 82530 Serial Communciations Controller (SCC) to provide 2 channels of serial I/O. The SCC generates all baudrate clocks and provides loopback capability on both channels. Channel A is configured for RS 422A multidrop DTE application. Channel B is RS 232C only and is configured as DTE.

The multidrop configuration may either full-or half-duplex. A full-duplex multidrop configuration with a single master driving the output lines allow a slave to monitor the data line and to perform tasks in parallel with tasks performed on another slave. However, only the selected slave may transmit to the master. A half-duplex multidrop configuration is more strict in its protocol. Two data lines and a ground line are required between a master and all slaves in the system and although all units may listen to whomever is using the data line, the system software protocol must be designed to allow only one unit to transmit at any given instant.

BUILT-IN-SELF-TEST DIAGNOSTICS

On-board built-in-self-test (BIST) diagnostics are implemented using the 8751 microcontroller and the 80186 microprocessor. On-board tests include initialization tests on DRAM, EPROM, the 80186 microcontroller, and power-up tests. Additional activities performed include a Reset Operating System initialization at power-up and a program table check, a feature allowing users to add custom code in EPROM while still maintaining full use of the factory supplied BISTs.

Immediately after power-up and the 8751 microcontroller is intialized, the 80186 microprocessor begins its own initialization and on-board diagnostics. Upon successful completion of these activities, the Reset Operation System invokes the user-defined program table. A check is made of the program table and the custom programs that the user has defined for his application will then execute sequentially.

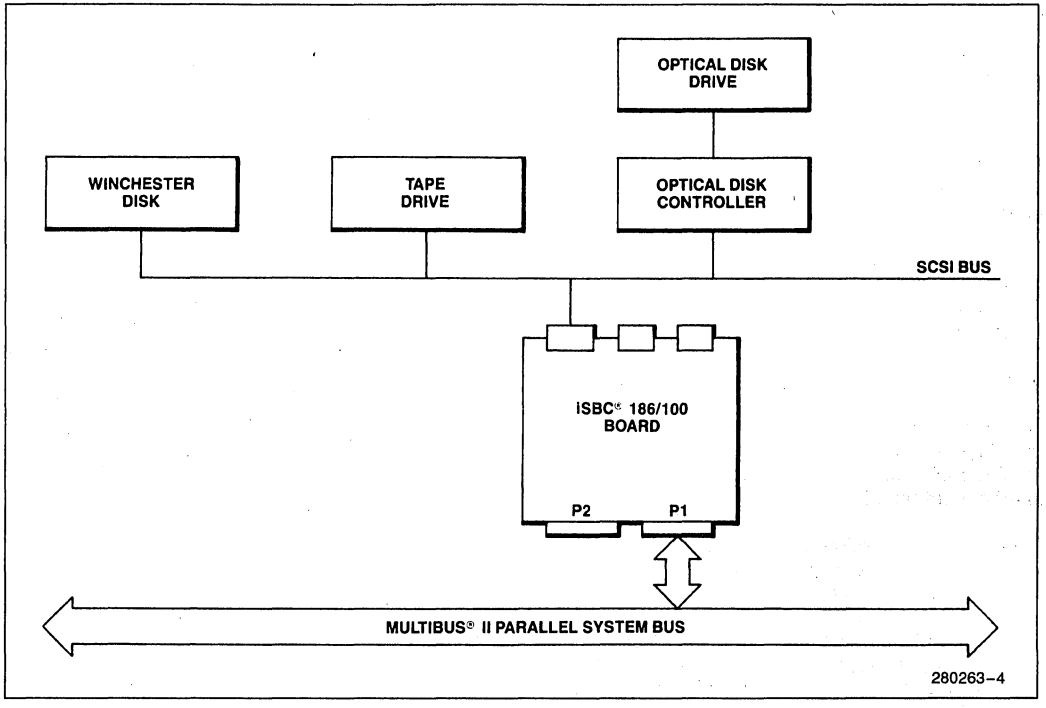


Figure 4. SCSI Application

BISTs improve the reliability, error reporting, and recovery capability of MULTIBUS II boards. In addition, these test and diagnostics reduce manufacturing and maintenance costs for the user. A yellow LED (labeled 'BIST') on the front panel indicates the status of the initialization checks and the power-up tests. It is illuminated if any of the initialization checks fail and remains off if the board successfully completes its tests. The LED also illuminates when the BIST tests start and stays on until the test complete successfully. The results of the BIST diagnostics are stored in the last 6 registers of the Header Record in Interconnect space.

iSBX™ BUS MULTIMODULE™ EXPANSION

One 8-or 16-bit iSBX bus MULTIMODULE connector is provided for I/O expansion. The iSBC 186/100 board supports both 8-bit and 16-bit iSBX modules through this connector. DMA is also supported to the iSBX connector and can be configured by programming the DMA multiplexor attached to the 82258 DMA component. The iSBX connector on the iSBC 186/100 board supports a wide variety of standard MULTIMODULE boards available from Intel and independent hardware vendors. Custom iSBX bus MULTIMODULE boards designed for MULTIBUS or proprietary bus systems are also supported as long as the IEEE P959 iSBX bus specification is followed.

iPSB BUS INTERFACE SILICON

The MPC (message passing coprocessor) provides all necessary iPSB bus interface logic on a single chip. Services provided by the MPC include memory and I/O access to the iPSB by the 80186 processor, bus arbitration, exception cycle protocols, and transfers as well as full message passing support. Dual port architecture may be implemented using the message passing coprocessor.

Interconnect Subsystem

The interconnect subsystem is one of the four MULTIBUS II address spaces, the other three being memory space, I/O space, and message space. The purpose of interconnect space is to allow software to initialize, identify, configure, and diagnose the boards in a MULTIBUS II system. All Intel MULTIBUS II boards support interconnect space.

The interconnect space is organized into a group of 8-bit registers called a template. The interconnect registers are organized into functional groups called records. Each register belongs to only one record, and there are three basic types of interconnect records: a header record, a function record, and an End of Template (EOT) record. The 80186 on the iSBC 186/100 board accesses its own template via the interconnect address space on the iPSB bus.

The header record provides board and vendor ID information, general status and control information, and diagnostic status and control information. The function record contains parameters needed to perform specific functions for the board. For example, an iPSB memory record contains registers that define the start and end address of memory for access across the iPSB bus. The number of function records in a template is determined by the manufacturer. The EOT record simply indicates the end of the interconnect template.

There are two types of registers in the MULTIBUS II interconnect space, read-only and software configurable registers. Read-only registers are used to hold information such as board type, vendor, firmware level, etc. Software configurable registers allow read and write operations under software control and are used for auto-software configurability and remote/local diagnostics and testing. A software monitor can be used to dynamically change bus memory sizes, disable or enable on-board resources such as PROM or JEDEC sites, read if the iSBX bus or PROM are installed as well as access the results of Built-In-Self-Tests or user installed diagnostics. Many of the interconnect registers on the iSBC 186/100 board perform functions traditionally done by jumper stakes. Interconnect space support is implemented with the 8751 microcontroller and iPSB bus interface logic.

SPECIFICATIONS

Word Size

INSTRUCTION: 8-, 16-, 24-, 32-, or 40-bits

DATA: 8-or 16-bits

System Clock

CPU: 8.0 MHz

NUMERIC COPROCESSOR: 8.0 MHz (part number 8087-1)

Cycle Time

BASIC INSTRUCTION: 8.0 MHz - 500 ns for minimum code read

Memory Capacity

LOCAL MEMORY

NUMBER OF SOCKETS: four 28-pin JEDEC sites

	Memory Capacity	Chip Example
EPROM	8K × 8	2764
EPROM	16K × 8	27128
EPROM	32K × 8	27256
EPROM	64K × 8	27512

ON-BOARD RAM

512K bytes 64K × 4 bit Dynamic RAM

I/O Capability

Serial:

— Two programmable channels using one 82530 Serial Communications Controller

— 19.2K baud rate maximum in full duplex in asynchronous mode or 1 megabit per second in full duplex in synchronous mode

— Channel A: RS 422A with DTE multidrop capability

— Channel B: RS 232C compatible, configured as DTE

— Parallel: SCSI, Centronics, or general purpose I/O

— Expansion: One 8-or 16-bit IEEE P959 iSBX MULTIMODULE board connector supporting DMA

Serial Communications Characteristics

ASYNCHRONOUS MODES:

- 19.2K baud rate maximum in full duplex
- 5-8-bit character; odd, even, or parity; 1, 1.5, or 2 stops bits
- Independent transmit and receive clocks, 1X, 16X, 32X, or 64X programmable sampling rate
- Error detection: Framing, Overrun, and Parity
- Break detection and generation

BIT SYNCHRONOUS MODES:

- 1 megabit per second maximum in full duplex
- SDLC/HDLC flag generation and recognition
- Automatic zero bit insertion and detection
- Automatic CRC generation and detection (CRC 16 or CCITT)
- Abort generation and detection
- I-field residue handling
- SDLC loop mode operation
- CCITT X.25 compatible

BYTE SYNCHRONOUS MODES:

- Internal or external character synchronization (1 or 2 characters)
- Automatic CRC generation and checking (CRC 16 or CCITT)
- IBM Bisync compatible

Timers

Three programmable timers on the 80186 microprocessor

INPUT FREQUENCIES:

Frequencies supplied by the internal 80186 16 MHz crystal

Serial chips: crystal driver at 9.8304 MHz divide by two

iSBX connector: 9.8304 crystal driven an 9.8304 MHz

Interrupt Capacity

POTENTIAL INTERRUPT SOURCES:

255 individual and 1 broadcast

INTERRUPT LEVELS:

12 vectored requests using two 8259As, 3 grounded inputs, and 1 input to the master PIC from the slave PIC

INTERRUPT REQUESTS:

All signals TTL compatible **INTERFACES**

IPSB BUS:

As per MULTIBUS II bus architecture specification

iSBX BUS:

As per IEEE P959 specification

CONNECTORS

Location	Function	Part #
P1	iPSB Bus	603-2-IEC-C096-F

Physical Dimensions

The iSBC 186/100 board meets all MULTIBUS II mechanical specifications as presented in the MULTIBUS II specification (#146077)

DOUBLE-HIGH EUROCARD FORM FACTOR:

Depth: 220 mm (8.7 in.)
Height: 233 mm (9.2 in.)
Front Panel Width: 20 mm (0.784 in.)
Weight: 743 g (26 oz.)

Environmental Requirements

Temperature: Inlet air at 200 LFM airflow over all boards
Non-operating: −40° to +70°C
Operating: 0° to +55°C

Humidity: Non-operating: 95% RH @55°C, non-condensing
Operating: 90% RH @ 55°C, non-condensing

Electrical Characteristics

The maximum power required per voltage is shown below. These numbers do not include the power required by the optional memory devices, SCSI PALs, or expansion modules.

Voltage (Volts)	Max Current (Amps)	Max Power (Watts)
+5	6.5 mA	34.13W
+12	50 mA	0.06W
−12	50 mA	0.06W

Reference Manuals

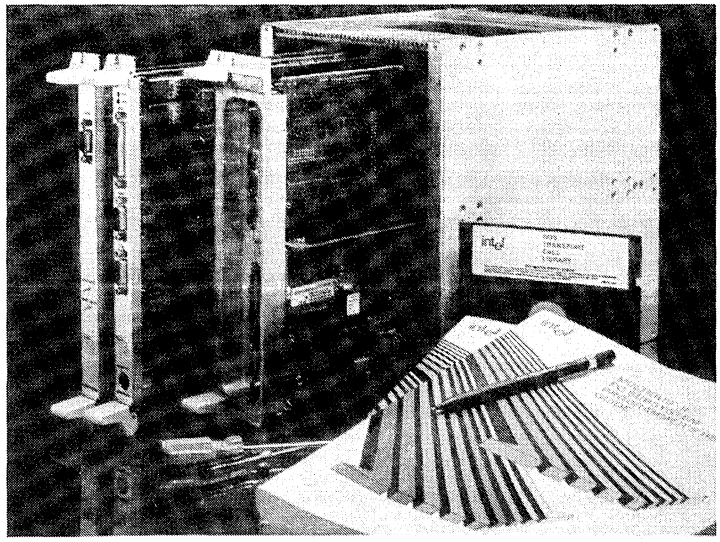
iSBC 186/100 Single Board Computer User's Guide (#148732-001)

Intel MULTIBUS II Bus Architecture Specification (#146077)

Manuals may be ordered from any Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA, 95051.

ORDERING INFORMATION

Part Number	Description
SBC186100	MULTIBUS II 80186-based Single Board Computer



PC/AT COMPATIBILITY COMES TO MULTIBUS II SYSTEMS*

The Intel MULTIBUS II PC Subsystem combines the power of the 386™ microprocessor, the multi-processing capabilities of the MULTIBUS II architecture and the large base of DOS compatible software into a high performance IBM PC/AT compatible two board set. When used with a standard PC/AT compatible keyboard and VGA compatible monitor this subsystem provides an excellent foundation for a human interface with color graphics for MULTIBUS II systems. Running off-the-shelf software packages it is suitable for data acquisition or process monitoring applications, and can be easily customized using a variety of available PC compatible products.

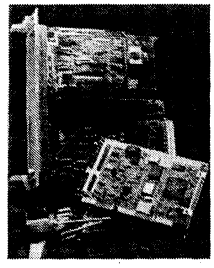
FEATURES

CPU BOARD

- Fully IBM PC/AT compatible subsystem running a 16 Mhz 386 32-bit CPU.
- Includes socket for Intel 80387 or Weitek numeric co-processor chip, 64 K of high speed SRAM cache, 2 serial ports, 1 parallel port, keyboard and floppy drive controllers.
- Completely MULTIBUS II systems architecture compatible including ADMA, MPC and 8751 interconnect controller.

PERIPHERAL COMPANION BOARD

- ST-506/ST-412 compatible Hard Disk Controller
- VGA graphics controller, with VGA, CGA, EGA, and mono-graphics software compatibility
- Built-in CSM functionality



Adaptor board allows standard PC add-on cards to be used.**

386 is a trademark of Intel Corporation

*IBM and PC/AT are trademarks of International Business Machines

**AT-bus add-in cards shown in the photographs are not manufactured or sold by Intel Corporation

September, 1988
Order Number: 280673-001

FEATURES

PART OF THE MULTIBUS®II FAMILY

Now PC/AT compatibility has come to a MULTIBUS II CPU. The MULTIBUS II Parallel System Bus is the bus of choice for Real Time multiprocessing. Its advanced bus architecture includes such features as a high speed (32 Mbytes/sec) Parallel Systems Bus (PSB) with message passing and bus parity detection, virtual interrupts, simplified systems configuration through interconnect space, and extensive power-up testing. Now our MULTIBUS II family is even more complete with DOS complementing iRMX®, iRMK™, and UNIX* operating systems, and bringing with it a complete human interface including keyboard controller and VGA graphics.

386 MICROPROCESSOR SPEED AND PERFORMANCE

The iSBC 386/PC16 CPU board features a 386™ CPU running at 16 Mhz and 64 K of 0 wait state (read hit) cache memory for 32-bit speed and performance. Performance can be even further enhanced by adding an Intel 80387 or Weitek math co-processor in the provided socket.

As much as 16 M-byte of DRAM can be provided on-board using memory expansion modules. Third party software allows this memory to be used as extended or expanded memory per the Lotus/Intel/Microsoft Expanded Memory Specification. For full IBM PC/AT software compatibility the iSBC 386/PC16 comes with an Award BIOS and runs either PC-DOS* or MS-DOS*. As a 386™ microprocessor-based PC platform, UNIX V/386 can also be easily ported to this board.

FULL COMPLEMENT OF PC PERIPHERALS

To minimize the need for add-in cards, the iSBC 386/PC16 CPU board includes 2 serial ports, 1 Centronics compatible parallel port, keyboard controller, and floppy disk controller.

The iSBC PCSYS/100 Peripheral Companion Board adds to that a hard disk controller, and a VGA graphics controller which is software compatible with EGA, CGA, and Hercules* monochrome graphics modes. In addition, it provides built-in MULTIBUS II Central Services Module Functionality.

INTEGRATES EASILY INTO A MULTIBUS II SYSTEM

The iSBC 386/PC16 CPU board was designed to integrate easily into a MULTIBUS II system. Hardware support includes the MULTIBUS II Message Passing Co-processor (MPC), 8751 interconnect space controller, and 82258 ADMA controller to provide full message passing support. It can also access global memory and I/O on the Parallel Systems Bus.

Conforming to the MULTIBUS II Systems Architecture (MSA), the SBC 386/PC16 includes firmware support for BISTs (Built-In Self Tests), IDX (Initialization and Diagnostics eXecutive), and DOS MULTIBUS II Transport Protocol. A DOS Transport Call Library, provided on a floppy disk, allows user implementation of communication and data sharing with other MULTIBUS II CPUs and peripherals.

BACKPLANES AND ADAPTOR BOARD

Rounding out the complement of products in the Intel MULTIBUS II PC Subsystem family are 2 and 4 slot backplanes for the P2/aPC bus (the PC bus brought out on the MULTIBUS II P2 connector) and an Adaptor Board. Intended for development purposes, the iSBC PCSYS/900 Adaptor Board plugs into a MULTIBUS II card cage or chassis and accommodates either four "half size" PC/XT* add-on cards or two "half size" PC/XT and either two PC/AT "full size" or two PC/XT "full size" add-on boards.

HIGH RELIABILITY

Intel has designed the MULTIBUS II PC Subsystem for high reliability. Extensive use of CMOS circuitry keeps the boards running cooler, and since excess heat can cause premature failure, running longer. DIN pin and socket connectors ensure reliable connectivity with the backplane, and parity error checking in the DRAM circuitry and on the Parallel Systems Bus improves overall system integrity. Furthermore the boards conform to Intel's strict design and manufacturing standards.

WORLD WIDE SERVICE AND SUPPORT

Should this or any Intel board ever need service, Intel maintains a world wide network of service and repair facilities to keep you and your customers up and running. In addition, should you need system level design support, our international Systems Engineering organization is available to integrate Intel boards and systems components into your products.

*UNIX is a trademark of AT & T
*PC-DOS and PC/XT are trademarks of International Business Machines
*MS-DOS is a trademark of Microsoft
*Hercules is a trademark of Hercules Computer Technology, Inc.

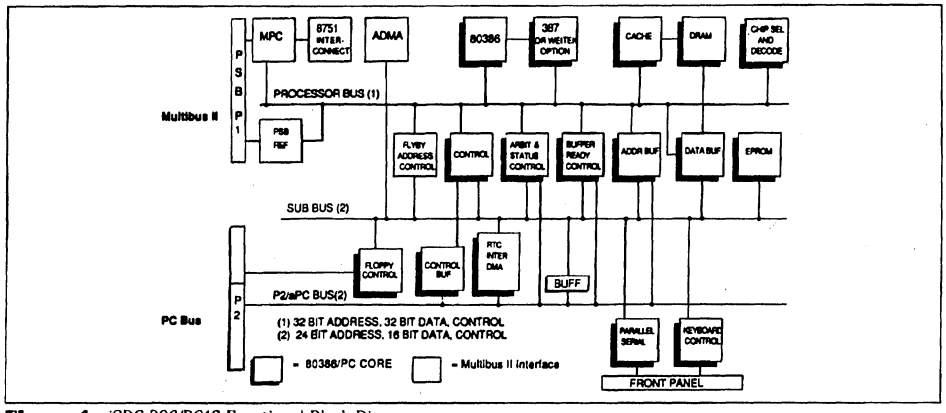


Figure 1: iSBC 386/PC16 Functional Block Diagram

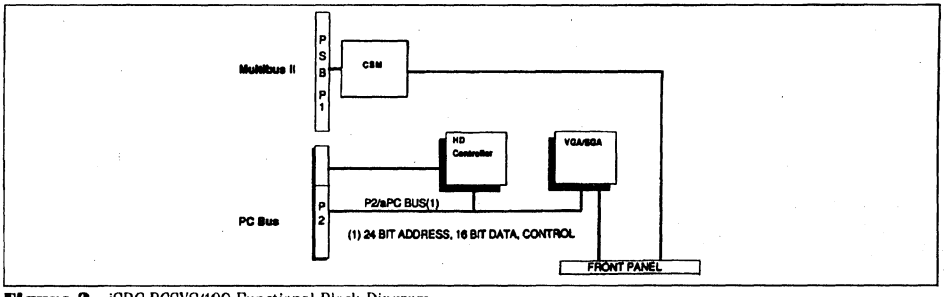


Figure 2: iSBC PCSYS/100 Functional Block Diagram

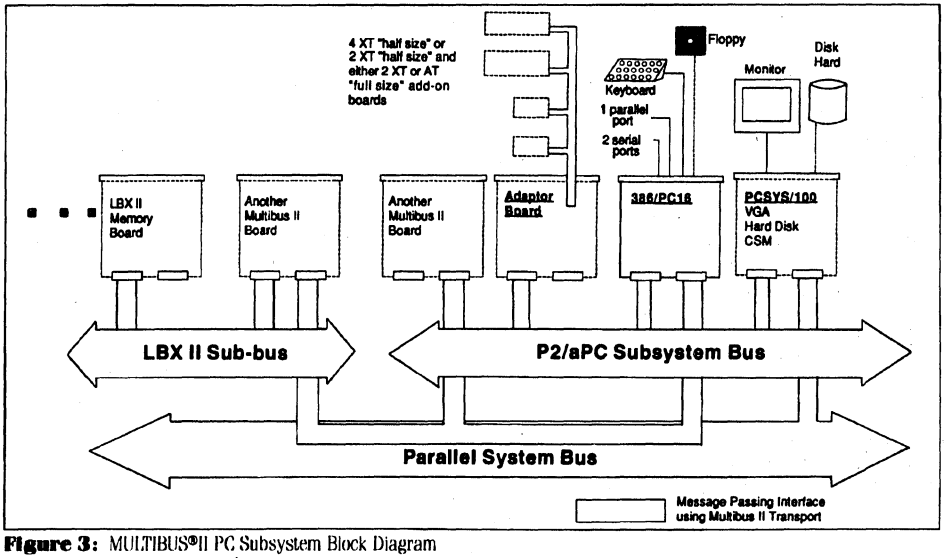


Figure 3: MULTIBUS®II PC Subsystem Block Diagram

CPU BOARD—SBC 386/PC16

CPU
386 microprocessor running at 16Mhz

DRAM Memory
32-bit parity protected memory:

Model	*Supplies*
SBC 386PC16 M01	1 Mb
SBC 386PC16 M02	2 Mb
SBC 386PC16 M04	4 Mb
SBC 386PC16 M08	8 Mb

Note: Model suffixes M02 and M08 require two MULTIBUS II card slots, Model suffixes M01 and M04 require only one MULTIBUS II card slot.

Memory expansion modules—one may be added to base models above

Model	*Supplies*
SBC MM01	1 Mb
SBC MM02	2 Mb
SBC MM04	4 Mb
SBC MM08	8 Mb

SRAM Cache
Capacity: 64K
Speed: 0 wait state on read hit
2 wait states on write
3 wait states on read miss

EPROM Memory
Two 32-pin JEDEC sites containing 256 K of EPROM memory with Award BIOS and MSA firmware.

Two additional 32-pin JEDEC sites provided for user EPROM or EEPROM memory. Circuitry is provided to write as well as read EEPROM memory.

PERIPHERAL COMPANION BOARD—SBC PCSYS/100

Hard Disk Controller
- PC/AT Compatible Winchester Controller
- Supports up to two ST-506/ST-412 drives

Graphics
- Supports VGA, EGA, CGA, and Hercules Compatible graphics
- Four text mode resolutions: 40 × 25, 80 × 25, 132 × 25, 132 × 43
- Three graphics mode resolutions: 640 × 480 with 16 colors, 960 × 720 with 4 colors, and 1280 × 960 monochrome

CSM
- Assigns card slot and arbitration IDs at initialization
- Generates system clock for all agents on the PSB
- Provides system wide reset signals for power-up, warm reset, and power failure
- Detects bus timeouts

P2/aPC BACKPLANES—SBC PCSYS/602 AND SBC PCSYS/604

- Available in 2 and 4 slot versions

ADAPTOR BOARD—SBC PCSYS/900

- Accommodates either four "half size" PC/XT add-on cards or two "half size" PC/XT and either two "full size" PC/AT or two PC/XT "full size" add-on boards
- Adaptor board is 3 MULTIBUS II card slots wide

ENVIRONMENTAL REQUIREMENTS

Storage Temperature:	– 40° to 70°C (0° to 158°F)
Operating Temperature:	0°C to 55°C (32° to 131°F)
Storage Humidity:	5%-95% non-condensing at 55°C
Operating Humidity:	8%-90% non-condensing at 55°C

ORDERING INFORMATION

SBC386PC16M01	386-based PC compatible CPU board with 1 Mb of DRAM
SBC386PC16M02	386-based PC compatible CPU board with 2 Mb of DRAM
SBC386PC16M04	386-based PC compatible CPU board with 4 Mb of DRAM
SBC386PC16M08	386-based PC compatible CPU board with 8 Mb of DRAM
SBCPCSYS100	Companion board with VGA graphics, HD controller and CSM functionality
S301K3	101-key enhanced AT-style keyboard
SBCPCSYS602	2-slot Backplane for the P2/aPC bus
SBCPCSYS604	4-slot Backplane for the P2/aPC bus
SBCPCSYS900	Adaptor Board
SBC MM01	1 Mb Memory Expansion Module
SBC MM02	2 Mb Memory Expansion Module
SBC MM04	4 Mb Memory Expansion Module
SBC MM08	8 Mb Memory Expansion Module

MULTIBUS® II
Memory Expansion Boards

11

iSBC® MM01, MM02, MM04, MM08 HIGH PERFORMANCE MEMORY MODULES

- **Provides High Speed Parity Memory Expansion for Intel's iSBC 386/2X, iSBC 386/3X and iSBC 386/1XX CPU Boards**
- **Available in 1M, 2M, 4M, and 8M Byte Sizes**
- **32 Bits Wide with Byte Parity**
- **Stackable to Provide up to 16M Bytes of High Speed Memory for MULTIBUS I and MULTIBUS II CPU Boards**
- **Supports 32-Bit, 16-Bit and 8-Bit Data Paths**
- **Supports Independent Read/Writes**
- **Easily Installed**

The iSBC MM01, iSBC MM02, iSBC MM04, and iSBC MM08 DRAM memory modules are members of Intel's complete line of iSBC memory and I/O expansion boards. The MM-Series of memory modules use a dedicated interface to maximize CPU/memory performance. The iSBC MM series of memory modules have been designed to provide both the on-board and expansion memory for the iSBC 386/2X, the iSBC 386/3X and the iSBC 386/1XX CPU Boards.

The modules contain (respectively) 1M byte, 2M, 4M, and 8M bytes of read/write memory using surface mounted DRAM components (see Figure 1).

Due to the high speed interface of the memory modules, they are ideally suited in applications where memory performance is critical.

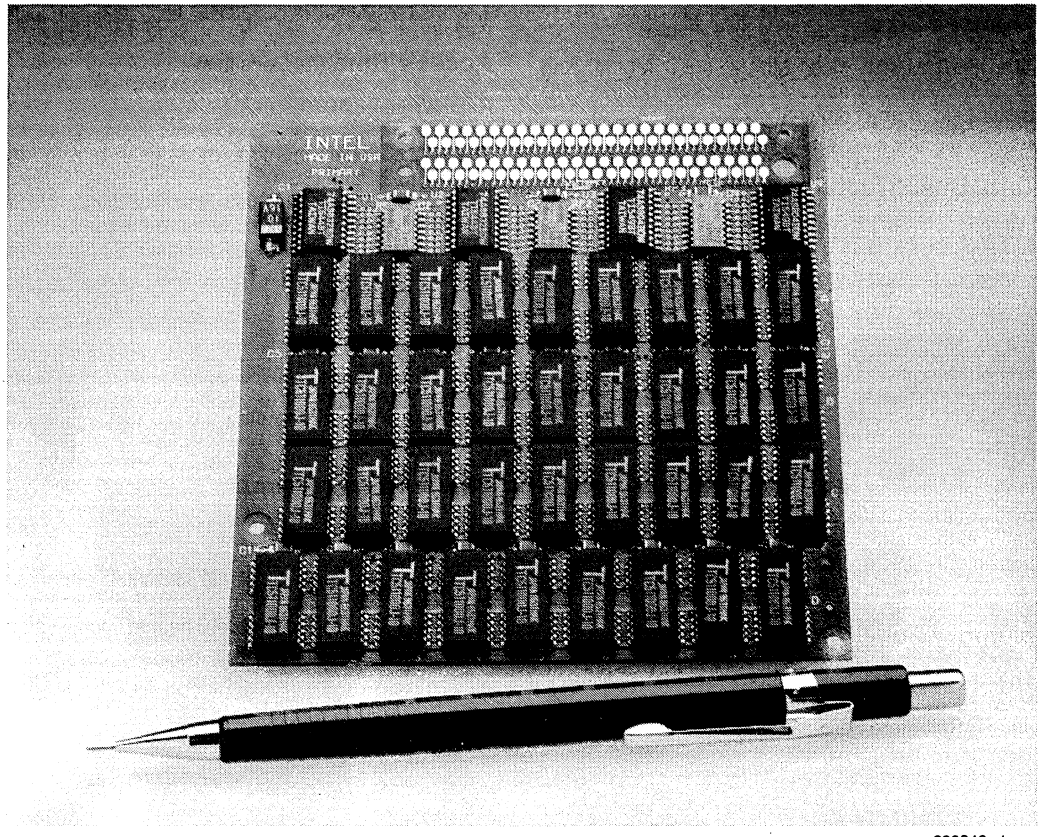


Figure 1. iSBC® MM08 Memory Module

280346-1

September 1988
Order Number: 280346-002

FUNCTIONAL DESCRIPTION

The iSBC MMxx memory modules provide high performance, 32-bit parity DRAM memory for the MULTIBUS I and MULTIBUS II CPU boards. These CPU boards come standard with one MMxx module installed, with memory expansion available through the addition of a second stackable iSBC MMxx module.

Memory Access Capabilities

The dynamic RAM memory of the memory modules is accessed through the dedicated memory module interface.

The MM memory module is designed for direct transfer of data between the CPU and the memory module without accessing the MULTIBUS interface.

MM01/MM02/MM04/MM08 Memory Size

The iSBC MM01, iSBC MM02, iSBC MM04, and iSBC MM08 modules can be stacked on the CPU baseboard in any combination.

Data Bus Structure

The MMxx-series memory modules use a 32-bit wide data path with storage for byte parity that can accommodate 8-bit byte, 16-bit or 32-bit word data transfers. In addition, the data path is capable of independent byte operations. This means that one byte can be written while the other three bytes (or any other combination) can be read.

Parity

One parity bit is provided for each of the four, 8-bit bytes in the 32-bit wide data path. For special applications, the parity bits can serve as data bits making possible 9-, 18-, or 36-bit data transfers.

Memory Function

The module protocol supports standard dynamic RAM READ, WRITE, RAS* only REFRESH cycles, and CAS* before RAS* REFRESH.

Installation

The iSBC MMxx memory modules are easily installed by the user. Each module includes all necessary connectors, screws, and other hardware for installation, either as a second stacked module or as a replacement for a module with less memory.

SPECIFICATIONS

Word Size Supported

8-, 16-, or 32-bits

Memory Size

iSBC MM01	1,048,576 bytes
iSBC MM02	2,097,152 bytes
iSBC MM04	4,194,304 bytes
iSBC MM08	8,388,608 bytes

Access Time (All Densities)

Read/Write — 107 ns (max)

The MMxx-series memory modules run with the iSBC 386/2X and iSBC 386/116 Boards at 16 MHz, and with the iSBC 386/3X and iSBC 386/120 Boards at 20 MHz. Wait state performance information with each of these CPU baseboards is contained in the Hardware Reference Manual for the specific CPU baseboard.

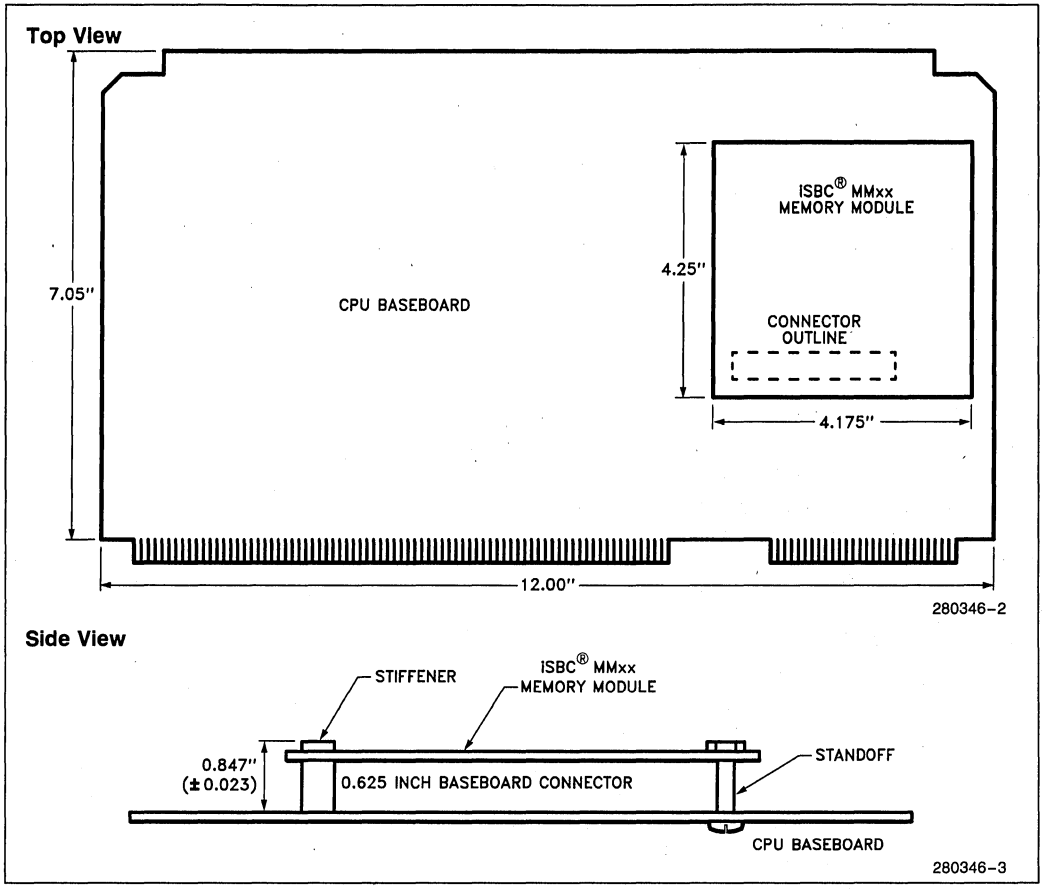
Cycle Time (All Densities)

Read/Write — 200 ns (min)

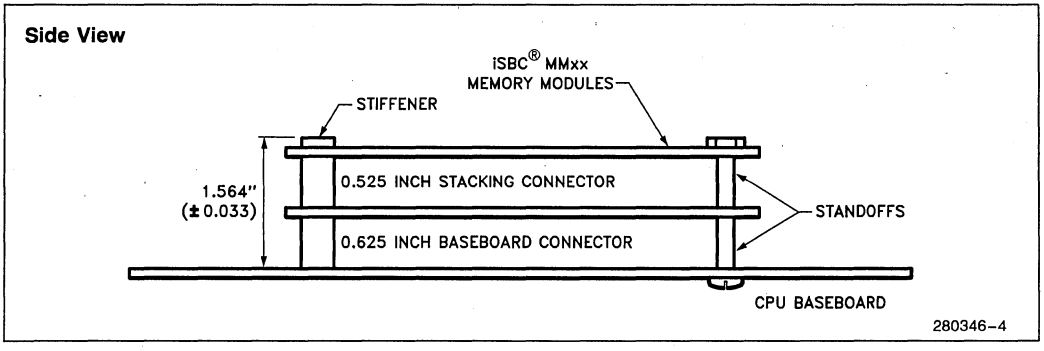
Power Requirements

Voltage −5 VDC ±5%

Memory addressing for the iSBC MMxx memory modules is controlled by the host CPU board over the memory module interface. The maximum system RAM size is 16M Bytes.



Single iSBC® MMxx Memory Module



Stacked iSBC® MMxx Memory Modules

Environmental Requirements

Operating Temperature — 0°C to 60°C

Storage Temperature — 40°C to +75°C

Cooling Requirement — 3 cubic feet per minute of airflow at an ambient temperature of 0°C to 60°C

Operating Humidity — To 95% relative humidity without condensation

Physical Dimensions

Module Alone:

Width — 4.250 inches (10,795 cm)

Length — 4.175 inches (10,604 cm)

Height — 0.500 inches (1,270 cm)

Weight — iSBC MM01/MM04: 2.5 ounces (70.0 gm)
iSBC MM02/MM08: 3.5 ounces (110.0 gm)

ORDERING INFORMATION

Part Number	Description
iSBC MM01	1M Byte RAM Memory Module
iSBC MM02	2M Byte RAM Memory Module
iSBC MM04	4M Byte RAM Memory Module
iSBC MM08	8M Byte RAM Memory Module

The Memory Modules ship with the required hardware (connectors, mounting screws, stand-offs, etc.) to stack a second module on the module already mounted on the base CPU board.

iSBC® MEM/312, 310, 320, 340 CACHE-BASED MULTIBUS® II RAM BOARDS

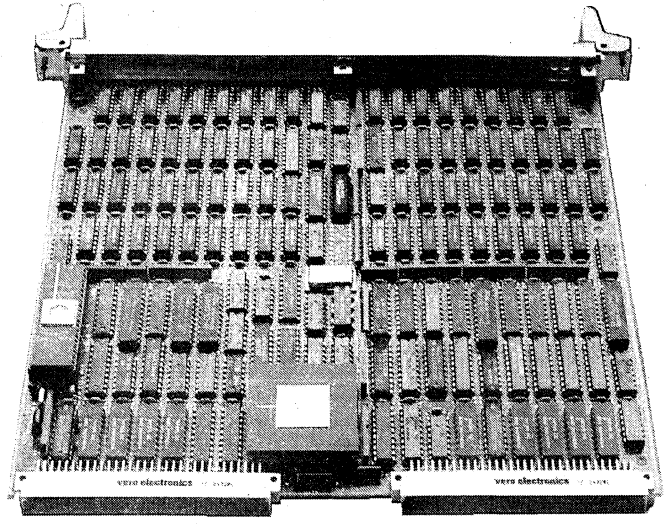
- **iSBC® MEM/3XX MULTIBUS® II Memory Boards Are High-Speed Cache-Based Boards with 8K Bytes of Cache RAM**
- **32-bit MULTIBUS® II Parallel System Bus (iPSB) and Local Bus Extension II (iLBX™ II Bus) Interface Support**
- **Zero Wait State Over iLBX™ on a Cache Hit, One Wait State for Cache Misses and Writes at 8 MHz**
- **Dual Port Memory with Four Versions Available:**

iSBC MEM/312	**½M Byte**
iSBC MEM/310	**1M Byte**
iSBC MEM/320	**2M Bytes**
iSBC MEM/340	**4M Bytes**

- **Double-high Eurocard Standard Form Factor, Pin and Socket DIN Connectors**
- **MULTIBUS II Software Interconnect Support for Dynamic Memory Configuration and Diagnostics with No Jumpers Necessary on the Board**
- **Built-In-Self-Test (BIST) Diagnostics On-Board with Both LED Indicators and Software Access to Error Information**
- **Automatic Memory Initialization at Power-Up and at Power-Fail Recovery**
- **Byte Parity Error Detection**

The iSBC MEM/312, 310, 320, 340 cache-based memory boards are the first Intel memory products to implement the MULTIBUS II system architecture. They have 32-bit architecture throughout, supporting 8-, 16-, and 32-bit central processors. The iSBC MEM/3XX (generally refers to this family of boards) memory boards are dual-ported, with access to the interfaces of both the MULTIBUS II Parallel System Bus (iPSB bus) and the iLBX II (Local Bus Extension).

In addition to the 32-bit memory transfer, the iSBC MEM/3XX high-speed cache control subsystem, standard on these boards, improves performance by allowing zero wait state read access over the iLBX II when data requested is in the cache memory.



280071-1

October 1988
Order Number: 280071-002

FUNCTIONAL DESCRIPTION

General

The iSBC MEM/312, 310, 320, 340 high-speed cache-based memory boards are physically and electrically compatible with the MULTIBUS II iPSB bus standard and the new iLBX II bus (Local Bus Extension) as outlined in the Intel MULTIBUS II specification. Figure 1 illustrates a typical multiprocessing MULTIBUS II system configuraton.

Architecture

The four main subsystems of the iSBC MEM/3XX boards are the cache controller subsystem, the cache memory subsystem, the DRAM memory subsystem, and the interconnect space subsystem (see Figure 2). The following sections describe these subsystems and their capabilities in more detail.

Cache Memory Capabilities

The cache memory system is designed around the 32-bit architecture of the main memory system and reduces read access timers. The 8K Bytes of 45 nsec SRAM allows zero wait state read accesses over the iLBX II bus when data requested is in the cache memory (cache hit). A cache hit takes only two iLBX II bus clocks (250 nsec at 8 MHz).

Each entry in the 8K Byte cache memory subsystem consists of a data field of 32-bits and a tag field of up to 9-bits (depending on board DRAM size). Each byte in the main memory DRAM array directly maps to one and only one entry on the cache array. This direct mapped cache array along with tag labels ensure data integrity and accurate identification of cache hits. The cache memory size and simple but effective replacement algorithm is designed to optimize both the probability of cache hits and the CPU bus utilization. On any miss or write access, the contents of one cache entry are updated to maintain consistency with the corresponding entry in the DRAM memory array.

Dual Port DRAM Capabilities

The iSBC MEM/312 module contains ½M Byte of read/write memory using 64K dynamic RAM compo-

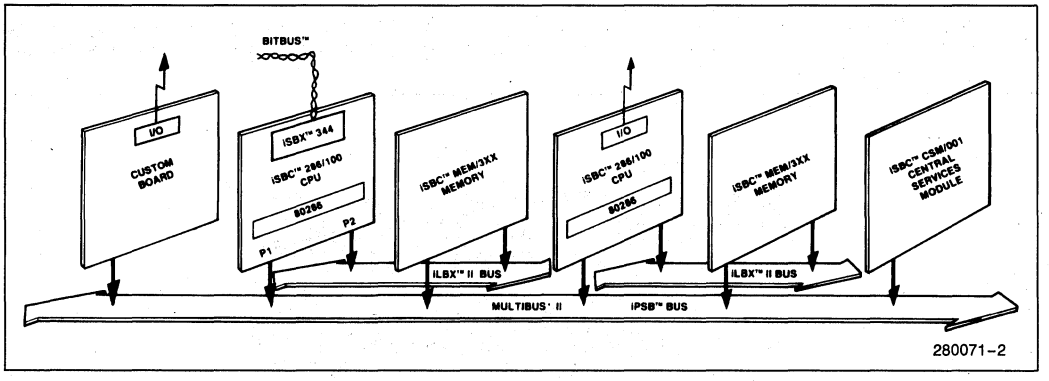


Figure 1. Typical MULTIBUS® II System Configuration

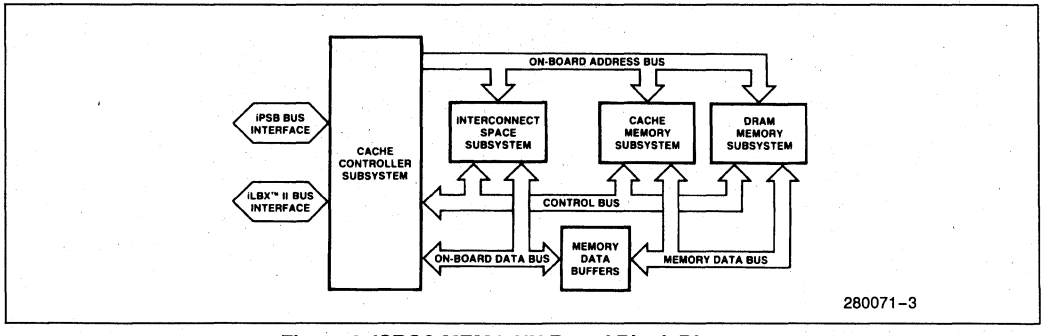


Figure 2. iSBC® MEM/3XX Board Block Diagram

nents. The iSBC MEM/310, MEM/320 and MEM/340 modules respectively contain 1M Byte, 2M Bytes and 4M Bytes of read/write memory using 256K dynamic RAM components.

The dual port capability of the iSBC MEM/3XX boards allows 32-bit access from either the iPSB bus interface or the iLBX II bus interface (see Figure 1). Due to the simple arbitration nature of the iLBX II bus interface and the cache memory subsystem, the iSBC MEM/3XX family allows optimal access to 20M Bytes of DRAM on the iLBX II bus.

System Memory Size

Using this series of memory boards the maximum system memory capacity based on one CPU board and 19 memory boards is 76M Bytes on the iPSB bus. The memory partitioning is independent for the iPSB bus interface and the iLBX II bus interface.

The start address can be on any 64K Byte boundary on the iPSB bus and any 64K Byte boundary on the iLBX II bus. Software configures the start and ending addresses through the interconnect space. No jumpers are needed.

Interconnect Space Capabilities

The iSBC MEM/3XX board module has a set of interconnect registers which allow the system software to dynamically configure and test the status of the memory board, replacing hardwired jumper functions. This interconnect subsystem also provides control and access to the Built-In-Self-Test (BIST) features. During power-up reset, the iSBC MEM/3XX board initializes the memory and cache, sets all interconnect registers to their default values and performs a self-test. Error information from both Built-In-Self-Test (BIST) and parity checking is indicated in front panel LEDs and recorded in interconnect space registers accessible to software.

Built-In-Self-Test (BIST)

Self-test/diagnostics have been built into the heart of the MULTIBUS II system. These confidence tests and diagnostics improve reliability and reduce manufacturing and maintenance costs. LED 1 (labelled BIST) is used to indicate the status of the Built-In Self Test. It is turned on when the BIST starts running and is turned off when the BIST completes successfully. The Built-In-Self-Test performed by the on-board microcontroller at power-up or at software command are:

1. **EPROM Checksum:**

   This test performs a checksum test on its internal EPROM to check operation of the 8751 microcontroller.

2. **Cache Data Test:**

   The microcontroller performs a sliding ones test on the cache memory in hit-only mode.

3. **Cache Address Test:**

   This test verifies that the cache address path is working properly.

4. **Refresh Check:**

   This test performs RAM test on a small portion of DRAM with an elapsed time between the write operation and the verification of the data.

5. **Dynamic RAM Address Test:**

   This test performs Address Rippled RAM test on the board memory (MISS ONLY operation mode).

6. **Dynamic RAM Data Test:**

   This test runs an AA-55 data pattern to check the DRAM data path.

7. **Parity Test:**

   This test injects parity errors in the DRAM array and then verifies that the board detects these errors.

These tests are described in detail in the User's Manual, Section 9–23.

Memory Initialization and Reset

Memory is initialized automatically during power-up. All bytes are set to 00.

Error Detection Using Byte Parity

Parity will detect all single bit parity errors on a byte parity basis and many muiltiple bit errors. LED 2 (labelled Parity) is used to indicate parity errors. LED 2 is turned on when a parity error is detected and turned off when the parity status register within interconnect space is cleared. This same LED turns on and off during power-up to verify operatoin of the LED.

Error information is recorded in interconnect space so it is accessible to software for error reporting.

SPECIFICATIONS

Word Size Supported

8-, 16-, 24-, and 32-bits

Memory Size

½ Megabyte (iSBC MEM/312) board
1 Megabyte (iSBC MEM/310) board
2 Megabytes (iSBC MEM/320) board
4 Megabytes (iSBC MEM/340) board

Access Times (All Densities)

MULTIBUS II Parallel System Bus—iPSB (@ 10 MHz)

Read: 562 ns (avg.)
775 ns (max.)

Write: 662 ns (avg.)
775 ns (max.)

NOTE:
Average access times assume 80% cache hit rates

iLBX™ II Bus—Local Bus Extension

Read: 250 ns (min.)
275 ns (avg.)
375 ns (max.)

Write: 375 ns (avg.)
375 ns (max.)

Base Address

iPSB Bus—any 64K Bytes boundary
iLBX II Bus—any 64K Bytes boundary

Power Requirements

Voltage: 5V DC ±5%

Product	Current
iSBC MEM/312 Board	3.5 A (typ) 6.0 A (max)
iSBC MEM/310 Board	3.5 A (typ) 6.0 A (max)
iSBC MEM/320 Board	3.5 A (typ) 6.0 A (max)
iSBC MEM/340 Board	4.1 A (typ) 6.7 A (max)

ENVIRONMENTAL REQUIREMENTS

Temperature: (inlet air) at 200 LFM airflow over boards
Non-Operating: −40 to +70°C
Operating: 0 to +55°C

Humidity: Non-operating: 95% RH @ 55°C
Operating: 90% RH @ 55°C

Physical Dimensions

The iSBC MEM/3XX boards meet all MULTIBUS II mechanical specifications as presented in the MULTIBUS II specification (#146077).

Double High Eurocard Form Factor:

Depth: 220 mm (8.6 in.)
Height: 233 mm (9.2 in.)
Front Panel Width: 20 mm (0.784 in.)

Weight:

iSBC MEM/312 board: 6720 gm (24 oz.)
iSBC MEM/310 board: 6160 gm (22 oz.)
iSBC MEM/320 board: 6720 gm (24 oz.)
iSBC MEM/340 board: 10080 gm (36 oz.)

Reference Manuals

iSBC MEM/3XX Board Manual (#146707-001)

Manuals may be ordered from any Intel Sales Representative, Distributor Office, or from the Intel Literature Department. 3065 Bowers Ave., Santa Clara, CA 95051.

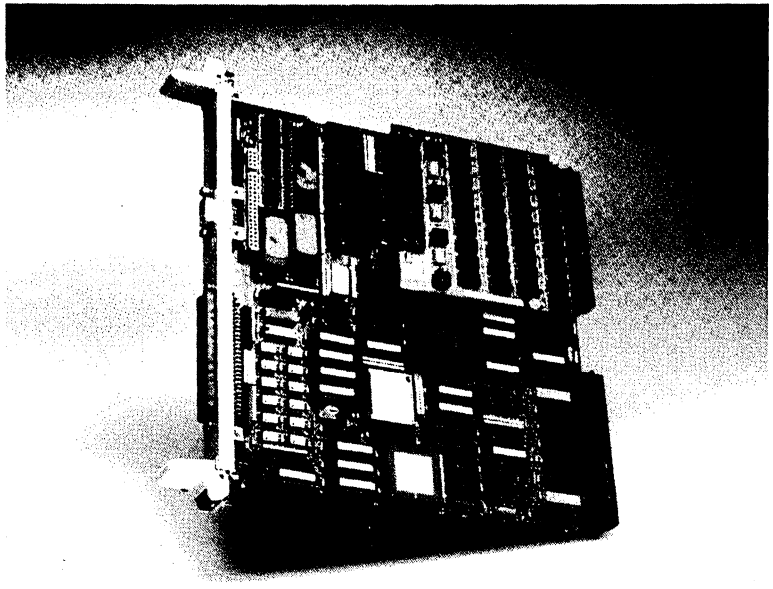
Ordering Information

Part Number	Description
iSBC MEM/312	½M Byte Cache Based MULTIBUS II RAM Board
iSBC MEM/310	1M Byte Cache Based MULTIBUS II RAM Board
iSBC MEM/320	2M Byte Cache Based MULTIBUS II RAM Board
iSBC MEM/340	4M Byte Cache Based MULTIBUS II RAM Board

MULTIBUS® II Peripheral Controllers

12

iSBC® 386/258 PERIPHERAL CONTROLLER



MULTIBUS®II CONTROLLER FOR HIGH-PERFORMANCE, SCSI PERIPHERALS

The iSBC 386/258 is a high-performance peripheral controller that provides a unique combination of powerful I/O performance and access to SCSI peripherals for MULTIBUS II applications. Minicomputer-level I/O performance is achieved by utilizing the 386™ microprocessor and a large data cache. The added power of the 386 processor gives the iSBC 386/258 the potential to off-load tasks from other system CPUs as an I/O server. The SCSI standard has achieved wide acceptance because of its extensive capabilities and excellent performance.

FEATURES

- 16 MHz 386 microprocessor
- 1 or 4 Mbyte data buffer
- Common Command Set (CCS) SCSI peripheral support
- Asynchronous SCSI up to 1.5 Mbytes per second, Synchronous SCSI up to 4.0 Mbytes per second
- Single-ended or differential SCSI options
- 8/16-bit iSBX™ interface connector
- RS232 serial port
- On-board self-test diagnostics

intel

September, 1988
Order Number: 280670-001

FEATURES

COMPLETE SCSI CAPABILITY

The iSBC 386/258 supports communication with up to seven other host/peripheral adapters and up to 56 possible devices. Vendor-unique features of peripherals can be accessed using the pass through capability. Also supported is the ability to be a bus initiator and/or a bus target, and the use of disconnect/reconnect. This extensive SCSI support allows the iSBC 386/258 to be used in applications such as high-speed data transfer between systems.

Peripherals that support the SCSI standard include magnetic hard disk, magnetic tape, floppy disk drive, optical disk, and line printers.

HIGH PERFORMANCE

I/O critical applications are accelerated by the combination of a 16 Mhz 386 processor, a large data buffer for cacheing, and the 4.0 Mbytes per second synchronous transfer rate for SCSI.

WORLDWIDE SERVICE AND SUPPORT

Intel provides support for board repair or on-site service. Development support options include phone support, subscription service, on-site consulting, and customer training.

QUALITY AND RELIABILITY TESTING

The iSBC 385/258 is designed and manufactured in accordance with Intel's high quality standards. We then verify quality through rigorous testing in our state-of-the art Environmental Test Laboratory.

SPECIFICATIONS

INTERFACES

MULTIBUS II: 32-bit Parallel System Bus (IEEE 1296) Interface with Full Message Passing Capability
SCSI: ANSI X3.131 - 1986
iSBX Bus Interface: compliance level D16/16 DMA for single-ended version, compliance level D16/16 for differential version
Serial I/O Port: RS-232-C (subset) interface (DTE), 9-pin D-shell shielded connector. Configurable baud rates: 300, 600, 1200, 2400, 4800, 9600 and 19200

DEVICE DRIVERS

Check the latest release of the following operating systems for details:
iRMX II
UNIX* System V/386

PHYSICAL CHARACTERISTICS

Height: 9.18 in. (233.2 mm)
Depth: 8.65 in. (220 mm)
Front Panel Width: 0.76 in. (19.2 mm)

POWER REQUIREMENTS

Typical: +5V @ 11A
±12 V @ 0.5A
Does not include power for installed iSBX MULTIMODULE boards

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0 to 55 C @ 200 LFM
Non-operating: −40 to 70 C
Humidity: 0 to 85% non-condensing

REFERENCE MANUAL

iSBC 386/258 SCSI Peripheral Controller User's Guide

*UNIX is a registered trademark of AT&T.

ORDERING INFORMATION

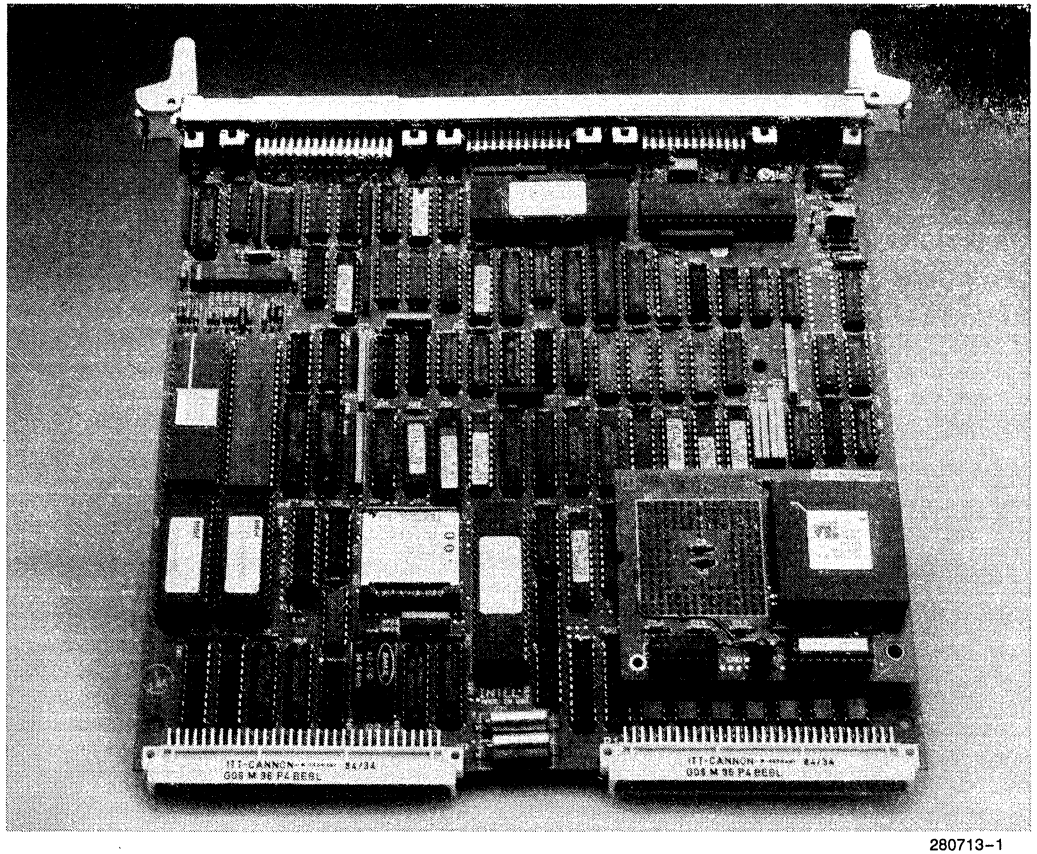
Part Number	Description
SBC 386 258S M01	Single-ended SCSI Peripheral Controller with 1 Mbyte
SBC 386 258S M04	Single-ended SCSI Peripheral Controller with 4 Mbyte
SBC 386 258D M04	Differential SCSI Peripheral Controller with 4 Mbyte

For more information or the number of your nearest Intel sales office, call 800-548-4725 (good in the U.S. and Canada).

iSBC® 186/224A MULTIBUS® II MULTI-PERIPHERAL CONTROLLER SUBSYSTEM

- **Complete I/O Subsystem for Mass Storage Devices**
- **Based on the 80186 Microprocessor**
- **On-Board Firmware Provides Concurrency of Operation**
- **Controls up to Four ST506/412 Winchester Disk Drives, up to Four SA450/460 Floppy Drives, and up to Four QIC-02 Streaming Tape Drives**
- **128K Bytes of On-Board DRAM Allows Multiple Track Caching for High Speed Winchester Data Access**
- **MPC (Message Passing Coprocessor) Single Chip Interface to the Parallel System Bus With Full Message Passing**
- **Software Configurability: Geographic Addressing**
- **Built-In-Self-Test (BIST) Diagnostics On-Board**

The iSBC 186/224A Multi-Peripheral Controller Subsystem supports the full Message Passing protocol of the MULTIBUS II System Architecture and provides peripheral I/O control for a wide variety of OEM applications. The iSBC 186/224A controller serves as a complete peripheral I/O subsystem and supports the predominant types of storage media: Winchester disks, floppy disks, and quarter-inch streaming tapes. On-board firmware for the board provides improved Winchester disk operation through multiple data track caching. This subsystem capability is provided on a single 8.7 x 9.2 inch double-high Eurocard form factor printed circuit board.



280713–1

December 1987
Order Number: 280713-003

ARCHITECTURE

Dual-Bus Architecture On-Board

The iSBC 186/224A controller is designed around a dual bus structure and is supported by real-time, multitasking firmware. The dual bus structure consists of the local bus and the I/O transfer bus. This dual-bus approach offers maximum task concurrency—allowing the 80186 CPU to execute code and/or manipulate data during data transfers to and from the various storage media.

The iSBC 186/224A controller uses the MULTIBUS II Parallel System Bus (iPSB) to transfer commands and data to requesting and sending agents via solicited and unsolicited messages as specified in the MULTIBUS II Bus Architecture Specification Handbook. (See Figure 1 for functional block diagram of the 186/224A board).

The local bus consists of the 80186 microprocessor, the EPROM, MPC (for access to the iPSB), and interrupt control. The 80186 component controls the local bus and manages the interface between the iPSB and the controller. DMA channels internal to the 80186 are used for data transfers between on-board memory and the MPC.

The I/O Transfer bus supports data transfers between the iSBC 186/224A controller and the various peripheral devices. The Winchester, floppy, and tape interfaces reside on the I/O Transfer bus as do the DMA controller and track cache DRAM.

The 8237A-5 DMA controller directly controls four independent DMA channels and provides the capability for performing time-multiplexed, concurrent data transfer operations between the respective device interfaces and the local DRAM.

A total of 128K bytes of zero wait state DRAM is provided on-board. This DRAM is local to the I/O Transfer bus. It is accessible to both the CPU and the DMA controller. It supports the 80186 stack and interrupt vectors and 64K bytes of Winchester track cache. The DRAM is configured for 16-bit (word) access and also supports byte-swapping.

This dual-bus architecture combined with the real-time control firmware and peripheral command protocol allows the concurrent transfer of data between multiple storage devices and the controller and between the controller and the MULTIBUS II Parallel System Bus resulting in improved system level performance.

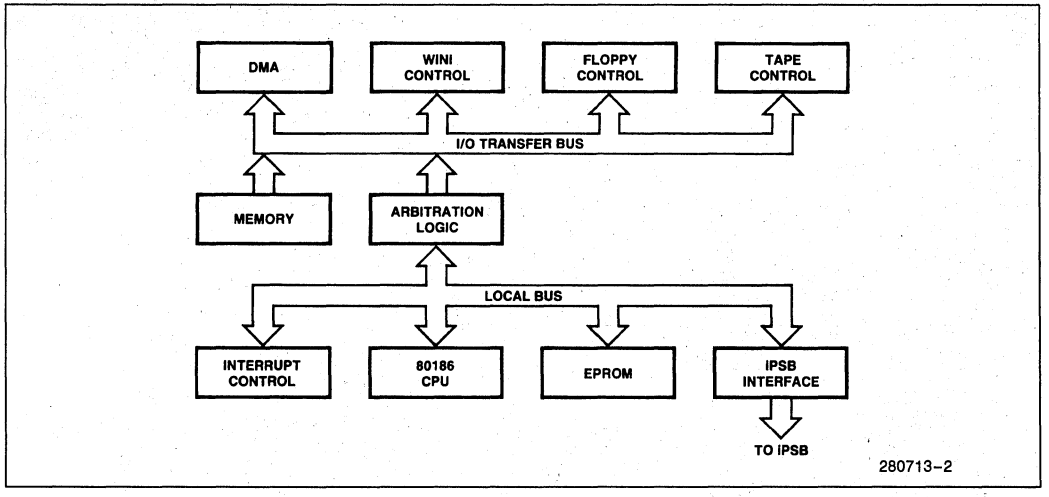


Figure 1. iSBC® 186/24A Board Block Diagram

Interconnect Space Subsystem

MULTIBUS II Interconnect Space is a standardized set of software configurable registers designed to hold and control board configuration information as well as system and board level diagnostics and testing information. Interconnect space is implemented with the 8751 microcontroller and the MPC bus interface silicon.

The read-only registers store information such as, board type, vendor I.D., firmware revision level, etc. The software configurable registers are used for controller options, identifying certain device characteristics, and diagnostics.

Built-In-Self-Test Diagnostics

On-board built-in-self-test (BIST) diagnostics provides confidence testing of the various functional areas of the iSBC 186/224A controller board. The initialization checks are performed by the 8751 microcontroller, while the BIST package is executed by the 80186 microprocessor.

BIST provides valuable testing and error reporting and recovery capability on MULTIBUS II boards, enabling the OEM to reduce manufacturing and maintenance costs. An LED on the board's front panel indicates go/no go status of power-up diagnostics. Further information is available via interconnect space.

Peripheral Communications Interface

A message-based peripheral communications interface provides a software interface to the 186/224A board. This protocol provides a vehicle to issue multiple commands or statuses concurrently. This allows the 186/224A board to accept multiple commands and queue them in on-board memory.

BACKPLANE BUS INTERFACES

P1 Connector: This is used as the standard MULTIBUS II 32-bit parallel system bus. It contains all signals required to implement the full standard interface.

P2 Connector: The P2 connector is not electrically connected internally on the board.

Winchester Connections: One 50-pin D-type, right angle female, high density connector which provides all of the required signals for up top four Winchester disk drives.

Flexible Disk Connections: One 25-pin D-type connection which provides all of the required signals for up to four daisy-chained flexible disk drives.

QIC-02 Streaming Tape Connections: One 25 pin D-type connection which provides the required signals for up to four daisy-chained tape drives.

I/O Connectors: The I/O connections for each interface are on the front panel. In order to provide a reliable connection to the peripheral devices, additional ground lines are included at the connector.

SPECIFICATIONS

CPU: 5 MHz 80186 synchronized to 5 MHz 8237A-5 DMA controller

Memory: 128K bytes DRAM on-board for buffers and track cache

2 PROM sites contain Built-in-Self-Test (BIST) and PCI firmware

Mass Storage Device Compatibility

Winchester—ST506/412 compatible 5¼" drives with up to 1024 cylinders.
Manufacturers include: Quantum, CMI, CDC, Maxtor, Memorex, Atasi.
Densities range from 10 MB to 140 MB.

Floppy—SA450/460 compatible 5¼" drives.
Manufacturers include: Teac, Shugart.
Sizes include half height, full height, 48TPI, 96TPI.

Tape—QIC-02 compatible, ¼" streaming tape drives.
Manufacturers include: Archive, Cipher, Tandberg.

Physical Dimensions

The iSBC 186/224A board meets all the mechanical specifications as presented in the MULTIBUS II specification (order #146077 rev. C).

DOUBLE-EUROCARD FORM FACTOR

Depth: 220 mm (8.6 in)

Height: 233 mm (9.2 in)

Front Panel Width: 20 mm (0.784 in.)

CONNECTORS

Interface	Connector	Part No.
iPSB bus (P1)	96 Pin DIN, Right Angle Female	603-2-IEC-C096-F
P2	96 Pin DIN, Right Angle Female, Not Connected Internally	603-2-IEC-C096-F
ST506/412 (Winchester)	50 Pin D Type, Right Angle Female, High Density (See Note)	
SA450/460 (Floppy)	25 Pin D-Type, Right Angle Female, (See Note)	
QIC-02 (Tape)	25 Pin D-Type, Right Angle Female, (See Note)	

NOTE:
The manufacturers below provide connectors which will plug into the connectors supplied on the iSBC 186/224A board front-panel.

Connector Type	Manufacturer	Pins	Part No.
Flat Ribbon Crimped	T&B Ansley	50	609-50P
	T&B Ansley	25	609-25P
Bulk Cable Solder Cup	Amlan	50	CDS50L
	Amlan	25	CDS25L
	ITT Cannon	50	DD-50P
	ITT Cannon	25	DB-25P
Pin Crimp	AMP	50	206438-1
	AMP	25	205436-1
	ITT Cannon	50	DDC-50P
	ITT Cannon	25	DBC-25P

Reference Manuals

iSBC 186/224A Board Hardware Reference Manual (order number 138272-001)

Intel MULTIBUS II Bus Architecture Specification (order number 146077)

Manual may be ordered from any Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 186/224A	Multiperipheral Controller Subsystem

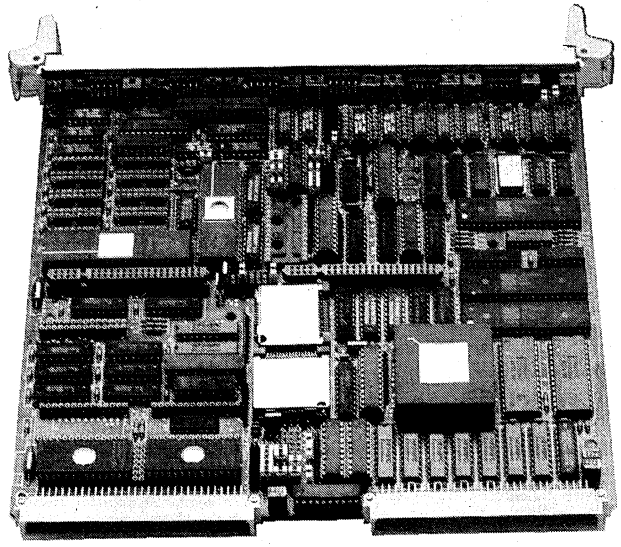
MULTIBUS® II
Serial Communication Board

13

iSBC® 186/410 MULTIBUS® II SERIAL COMMUNICATIONS COMPUTER

- **Six Serial Communication Channels on a Single MULTIBUS® II Board, Expandable to 10 Channels via iSBX™ Bus Connectors**
- **High Integration 8 MHz 80186 Microprocessor**
- **82258 Advanced DMA Controller Provides 4 Independent High Performance DMA Channels**
- **Supports RS232C-Only on 4 Channels, RS422A or RS232C Interface Configurable on 2 Channels**
- **512K Bytes DRAM Provided**
- **MULTIBUS® II iPSB (Parallel System Bus) Interface with Full Message Passing Capability**
- **Four 28-Pin JEDEC Sites, Expandable to 8 Sites with iSBC® 341 MULTIMODULE™ for a Maximum of 512K Bytes EPROM**
- **Two iSBX™ Connectors for Low Cost I/O Expansion**
- **MULTIBUS® II Interconnect Space for Software Configurability and Diagnostics**
- **Resident Firmware to Support Host-to-Controller Download Capability and Built-In-Self-Test (BIST) Diagnostics**

The iSBC 186/410 MULTIBUS II Serial Communications Computer is an intelligent 6-channel communications processor implementing the full, high performance message passing interface of the MULTIBUS II (iPSB) Parallel System Bus. This iSBC board combines an 8 MHz 80186 16-bit microprocessor, with six serial channels (expandable to 10 serial channels on-board via iSBX connectors), up to 512K bytes of DRAM, four 28-pin JEDEC sites, two iSBX connectors, and an 82258 ADMA controller on a single 220 mm x 233 mm (8.7 in. x 9.2 in.) Eurocard printed circuit board. The iSBC 186/410 board supports asynchronous, byte synchronous, and bit-synchronous (HDLC/SDLC) communications protocols on the two full/half duplex RS232C/RS422A channels, and asynchronous-only on the four full/half duplex RS232C-only channels. Acting as a terminal controller or front-end processor, this board adds significant data communications flexibility to an OEM's MULTIBUS II design.



280268-1

October 1987
Order Number: 280268-002

OPERATING ENVIRONMENT

The iSBC 186/410 MULTIBUS II Serial Communications Computer is a powerful data communications sub-system specifically designed to operate in and support the message-based, multi-processor system configurations being implemented on the MULTIBUS II architecture. The board's on-board CPU, an 8 MHz 80186 microprocessor, provides significant intelligence to off-load and distribute the serial communications functions away from one or all of a system's processor boards.

The iSBC 186/410 board was designed with a set of features to address several communications application areas: terminal/cluster controller, or front-end processor.

Terminal/Cluster Controller

A terminal/cluster controller concentrates communications in a central area of a system. Efficient handling of messages coming in or going out of the system requires sufficient buffer space to store messages along with high speed I/O channels to transmit and receive those messages. Sophisticated cluster controller applications also require character and format conversion capabilities to allow attachment of different types of terminals.

The iSBC 186/410 MULTIBUS II Serial Communications Computer is well suited for multi-terminal system applications (see Figure 1). Up to 10 serial channels can be serviced in multi-user or cluster configurations by adding two iSBX 354 Dual Serial Channel MULTIMODULE boards. The on-board 512K byte (expandable to 512K bytes) DRAM array is the buffer area designed to handle incoming and outgoing messages at data rates up to 19.2K baud (asynch). Each serial channel can be individually programmed for different baud rates to allow system configurations with differing terminal types. The on-board 80186 CPU handles the protocols and character manipulation tasks traditionally performed by a system host.

Front-end Processor

A front-end processor off-loads a system's central processor of bandwidth-draining tasks such as data manipulation and text editing of characters collected from the attached serial I/O devices. Since most ter-

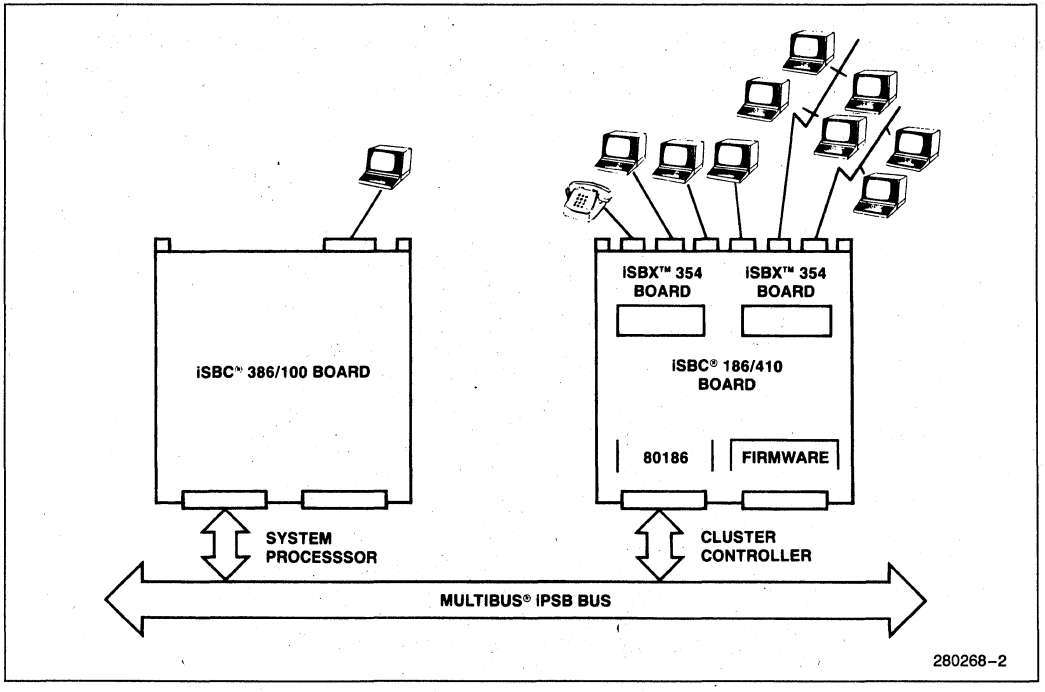


Figure 1. Terminal/Cluster Controller Application

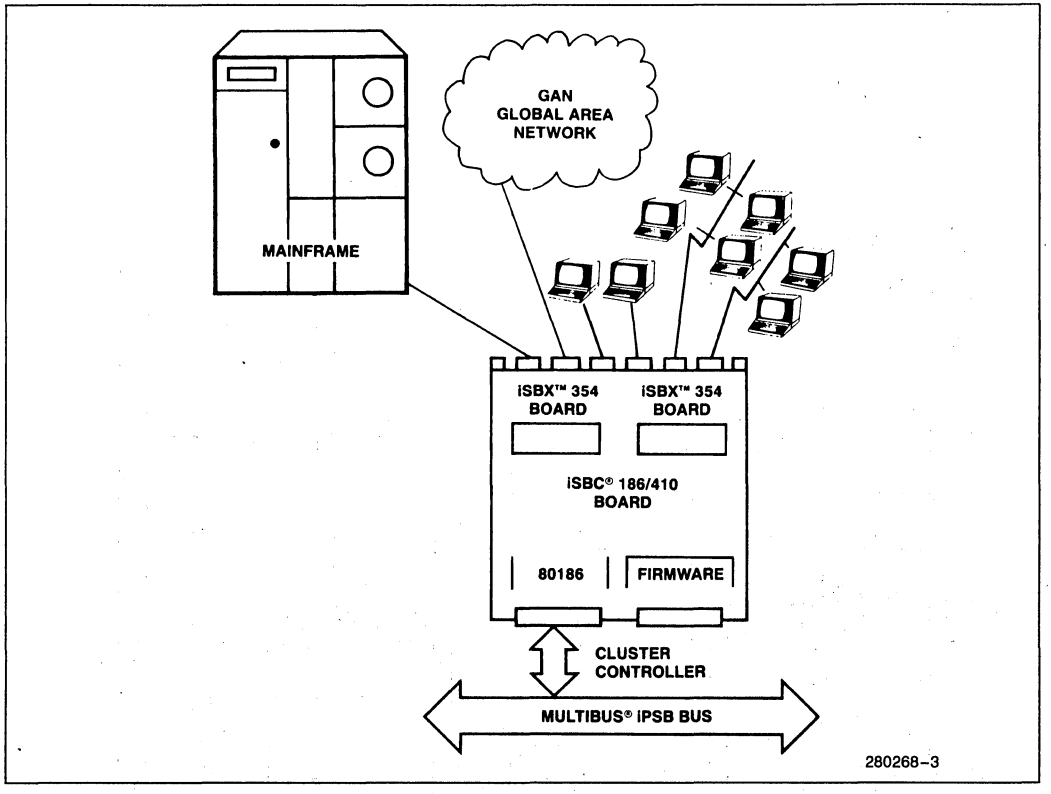


Figure 2. Front-End Processor Application

minal and serial I/O devices require flexible interfaces, program code is often dynamically downloaded to the front-end processor from a system CPU. Downloading code requires sufficient memory space for protocol handling and program code. Flow control and interrupt handling requirements need an efficient real time operating software environment to manage the hardware and software resources on the board.

The iSBC 186/410 board features are designed to provide a high performance solution for front-end processor applications (see Figure 2). A large amount of memory is provided for dynamic storage of program code. Two serial channels (as well as four iSBX expansion serial channels) can be configured for links to mainframe systems, point-to-point terminals, modems or multi-drop designs and four serial channels are for terminal communication, asynchronous RS232C operation only.

ARCHITECTURE

The iSBC 186/410 MULTIBUS II Serial Communications Computer consists of six major subsystem areas: Processor, Serial I/O, Memory, General I/O, iPSB bus interface, and Interconnect (see Figure 3).

Processor Subsystem

80186 PROCESSOR

The central processor unit on the iSBC 186/410 board is Intel's 16-bit 8 MHz 80186 microprocessor. The highly integrated 80186 CPU combines several system components onto a single chip (i.e., two Direct Memory Access lines, three Interval Timers, Clock Generator, and Programmable Interrupt Controller). The 80186 instruction set is a superset of the 8086 and maintains object code compatibility while adding additional instructions.

This high performance component manages the board's multi-user, multi-protocol communications operations. Refer to the Microsystem Components Handbook, Order Number 230843-00X, for more detailed information on the hardware operation and requirements of the 80186 microprocessor component.

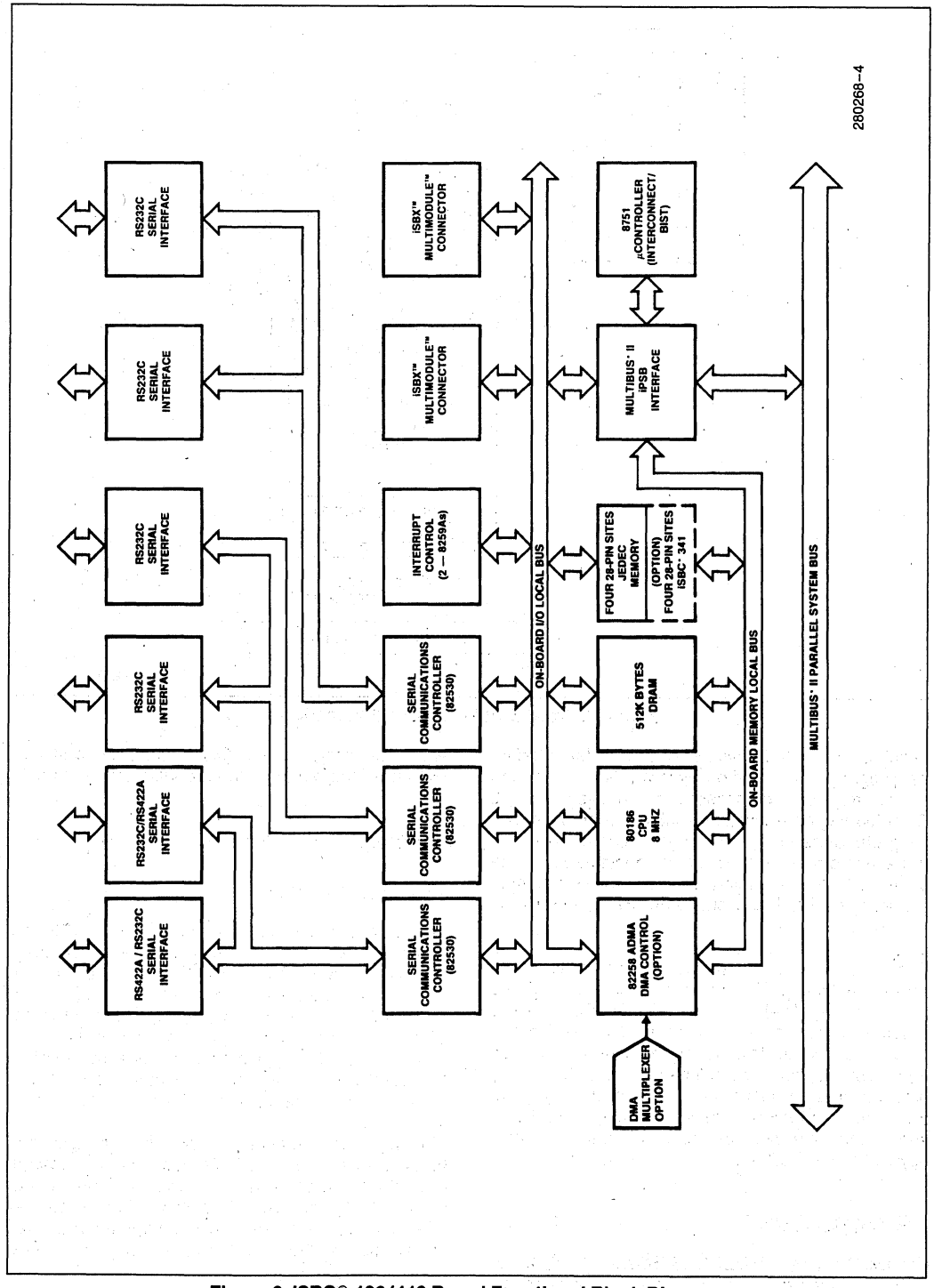


Figure 3. iSBC® 186/410 Board Functional Block Diagram

DIRECT MEMORY ACCESS (DMA) FUNCTION

The iSBC 186/410 board provides 13 channels of DMA to support serial I/O, iPSB interface, and/or iSBX bus transfer operations. The 80186 microprocessor provides two DMA channels, the 82258 Advanced (ADMA) controller supports three "direct" channels of DMA, and the ADMA multiplexer circuit uses the fourth 82258 ADMA channel providing eight additional multiplexed DMA channels. The allocation of the board's DMA channels to on-board resources is listed in Table 1.

SERIAL I/O SUBSYSTEM

Six serial interfaces are provided on the iSBC 186/410 board: two interfaces support full asynchronous, byte-synchronous, and bit-synchronous (HDLC/SDLC) communication and four interfaces support asynchronous-only communication. The two RS422A configurable ports can also be tri-stated to allow multi-drop networks. The board's serial capability can be expanded to 10 channels by adding two iSBX 354 Dual Channel Serial I/O MULTIMODULE boards. Each added iSBX 354 board uses an

Table 1. iSBC® 186/410 Board DMA Channel Allocation

Channel Count		Channel Number	DMA Configuration Local Bus Resource
80186			
1	DMA Channel	0	Half-Duplex High Speed Serial Interface (SCC1 Channel A) (—High Density 15-Pin Connector)
2	DMA Channel	1	Full-Duplex Serial Interface (SCC1 Channel A) or SBX1 DMA Request
82258 ADMA			
3	DMA Channel	0	Input DMA from MPC (Message Passing Coprocessor)
4	DMA Channel	1	Output DMA to MPC
5	DMA Channel	2	Half-Duplex High Speed Serial Interface (SCC1 Channel B) (—High Density 15-Pin Connector) or SBX1 DMA REQ
	DMA Channel	3	Full-Duplex High Speed Serial Interface (SCC1 Channel B) or INT2 DMA REQ from DMA Multiplexer
DMA Multiplexer*			
6	DMA Channel	0	Half-Duplex Serial Interface (SCC2 Chan. A, 9-pin conn.)
7	DMA Channel	1	Full-Duplex Serial Interface (SCC2 Chan. A)
8	DMA Channel	2	Half-Duplex Serial Interface (SCC2 Chan. B, 9-pin conn.)
9	DMA Channel	3	Full-Duplex Serial Interface (SCC2 Chan. B) or SBX1 DMA Request or Half-Duplex SCC1 Channel B.
10	DMA Channel	4	Half-Duplex Serial Interface (SCC3 Chan. A, 9-pin conn.)
11	DMA Channel	5	Full-Duplex Serial Interface (SCC3 Chan. A) or SBX2 DMA Request
12	DMA Channel	6	Half-Duplex Serial Interface (SCC3 Chan. B, 9-pin conn.)
13	DMA Channel	7	Full-Duplex Serial Interface (SCC3 Chan. B) or INT1 SBX1 for SBX344

NOTE:
*ADMA Channel 3 is used to add the DMA Multiplexer.

82530 SCC component to provide two independent full duplex serial channels configurable as either RS232C or RS422A interfaces. It also supports both asynchronous or programmable byte and bit synchronous (HDLC/SDLC) protocols. The HDLC/SDLC interface is compatible with IBM system and terminal equipment and with CCITT's X.25 packet switching interface.

Three 82530 Serial Communications Controllers (SCCs) provide six channels of half/full serial I/O. Two channels are configurable as either RS232C or RS422 on two high density 15-pin female D-shell connectors. Four more channels are RS232C-only using IBM standard 9-pin male D-shell connectors. All six channels directly support the Data Terminal Equipment (DTE) configuration, with the Data Communication Equipment (DCE) pin-out supported by changes in the cable wiring.

The 82530 component is designed to satisfy several serial communications requirements; asynchronous, byte-synchronous, and bit-synchronous (HDLC/SDLC) modes. The increased capability at the serial controller point results in off-loading a CPU of tasks normally assigned to the CPU or its associated hardware. Configurability of the 82530 allows the user to configure it to handle all asynchronous data formats regardless of data size, number of start or stop bits, or parity requirements. An on-chip baud rate generator allows independent baud rates on each channel.

Memory Subsystem

The iSBC 186/410 board's on-board memory subsystem consists of a large DRAM array and a set of universal memory sites. Access to the on-board memory subsystem resources, as well as off-board iPSB bus access, is accomplished by observing the iSBC 186/410 board memory map (see Figure 4). The mapping occurs within the 1 megabyte memory space of the 80186 microprocessor, and is split into three main areas: DRAM reserved, iPSB window, and EPROM reserved. The first 0 to 512K bytes is always reserved for local DRAM, the next 128K or

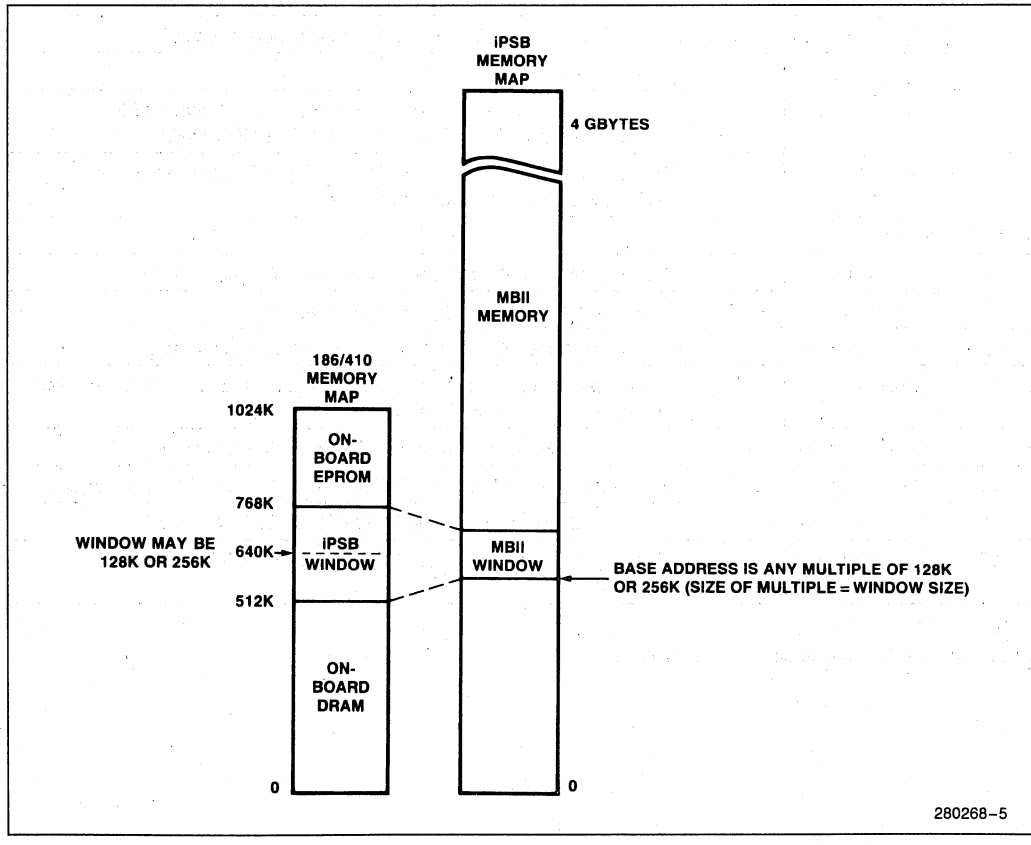


Figure 4. iSBC® 186/410 Board Memory Map Diagram

256K bytes (or up to 768K) is the iSPB window, and the remaining 384K or 256K byte area is reserved for local EPROM. The iPSB window maps a 128K or 256K byte local memory area into the 4 gigabyte global physical address range of the MULTIBUS II iPSB bus. This window is programmable and allows the 80186 processor to access the complete 4 gigabyte memory space of the iPSB bus.

The board's memory map also supports a 64K byte access window for I/O space between local and iPSB bus access. The 64K bytes of local I/O space is mapped 1-to-1 to the iPSB bus' 64K byte I/O space and is not programmable. The upper 32K bytes access the iPSB bus I/O space, and the lower 32K bytes are reserved for local on-board I/O.

DRAM CAPABILITIES

The iSBC 186/410 board comes standard with a 512K byte DRAM memory array on-board.

EPROM MEMORY

A total of four 28-pin JEDEC universal sites reside on the iSBC 186/410 board. These sockets support addition of byte-wide ROM and EPROM devices in densities from 8K bytes (2764) to 64K bytes (27512) per device. Two of the four sockets contain a pair of 27812 EPROM devices installed at the factory(1). These devices contain 128K bytes of firmware providing both the Host-to-controller download routine and the Built-In-Self-Test (BIST) power-up diagnostics routine. The remaining two sockets allow the user to add either two additional devices or an iSBC 341 EPROM MULTIMODULE for a maximum of 512K bytes.

NOTE:
(1) These devices may be removed by the user for access to the two 28-pin sites.

General I/O Subsystem

The I/O subsystem provides timers, interrupt control and two IEEE P959 iSBX connectors for I/O expansion or customization.

PROGRAMMABLE TIMERS AND INTERRUPT CONTROL

The 80186 microprocessor on the iSBC 186/410 board provides three independent, fully programmable 16-bit interval timers/event counters for use by the systems designer to generate accurate time intervals under software control. The outputs may be independently routed to a PIC to count external events. The system software configures each timer independently and can read the contents of each counter at any time during system operation.

In a MULTIBUS II system, external interrupts (interrupts originating from off-board) are interrupt type messages over the iPSB bus rather than signals on individual lines. Interrupt type messages are handled by the bus interface logic, the MPC Message Passing Coprocessor chip. The MPC component interrupts the 80186 processor via an 8259A Programmable Interrupt Controller (PIC) indicating a message has been received. This means that 1 Interrupt line can handle interrupts from up to 255 sources.

Two on-board 8259A PICs are used in a master-slave configuration for processing on-board interrupts. One of the interrupt lines handles the interrupt messages received from the iPSB bus. Table 2 includes a list of devices and functions supported.

iSBX™ BUS I/O EXPANSION

Two 8/16-bit iSBX bus (IEEE P959) connectors are provided for modular, low-cost I/O expansion. The iSBC 186/410 board supports both 8-bit and 16-bit iSBX MULTIMODULEs through these mating, gas-tight pins and socket connectors. DMA is also supported to the iSBX connectors and can be configured by programming the DMA multiplexor attached to the 82258 ADMA component. The iSBX connectors on the iSBC 186/410 board support a wide variety of standard iSBX compatible boards from Intel and other independent vendors providing add-on functions such as, floppy control, ¼" tape control, bubble memory, parallel/serial I/O, BITBUS™ interface, math, graphics, IEEE 488, and analog I/O. Custom iSBX module designs are also supported as per the IEEE P959 iSBX bus specification.

iPSB Bus Interface Subsystem

This subsystem's main component is the Message Passing Coprocessor chip. Subsystem services provided by the MPC bus interface component include full message passing support and memory, I/O, and interconnect access to the iPSB bus by the 80186 processor. The single-chip Message Passing Coprocessor is a highly integrated CHMOS device implementing the full message passing protocol and performing all the arbitration, transfer, and exception cycle protocols specified in the MULTIBUS II Architecture Specification Rev. C., Order Number 146077.

Table 2. ISBC® 186/410 Board Interrupt Devices and Functions

Device	Function	Number of Interrupts
iPSB Bus Interface (MPC)	Message-Based Interrupt Requests from the iPSB bus via MPC Message Passing Coprocessor	1 interrupt for up to 255 sources
8751 Interconnect Controller	Interconnect Space	1
80186 Timers & Interrupt	Timers 0 and 1 and Interrupt Acknowledge 1	3
82530 SCCs (3 devices)	SCC #1 and SCC #2 or SCC #3 for Transmit Buffer Empty, Receive Buffer Full, and Channel Errors	2
iPSB Bus Interface (MPC)	Indicates Transmission Error on iPSB Bus	1
82258 ADMA	DMA Transfer Complete	1
IEEE P959 iSBX Bus Connectors (2)	Functions Determined by iSBX Bus MULTIMODULE Boards	4 (2/connector)
IEEE P959 iSBX Bus Connectors (2)	DMA Interrupt from iSBX (TDMA)	2

Interconnect Subsystem

MULTIBUS II interconnect space is a standardized set of software configurable registers designed to hold and control board configuration information as well as system and board level diagnostics and testing information. Interconnect space is implemented with the 8751 microcontroller and the MPC silicon resident on the iSBC 186/410 board.

The read-only registers store information such as board type, vendor I.D., firmware rev. level, etc. The software configurable registers are used for auto-software configurability and remote/local diagnostics and testing.

Firmware Capability

HOST/CONTROLLER SOFTWARE DOWNLOAD ROUTINE

Resident in ROM on this controller is a host-to-controller software download routine to support the downloading of communication firmware into the iSBC 186/410 Serial Communication Computer. This loader adheres to the MULTIBUS II Download Protocol and responds to commands issued by software running on a host CPU board. The host CPU passes these commands to the loader via registers defined in the board's interconnect space. A download function, a commence execution function, and an examine local memory function are all provided in the routine. Data transfers are supported by both shared memory systems and message based systems. The top 1K of DRAM on the board is reserved for the exclusive use of the download program. Host CPUs must not overwrite this area with download commands.

Software on the host is responsible for accessing the iSBC 186/410 board's firmware on disk or from ROM visible to the host and translating it into linear sequences of bytes suitable for downloading (see Figure 5). After downloading the firmware, the host issues a command for the loader routine on the controller to begin execution of the downloaded software.

BUILT-IN SELF-TEST DIAGNOSTICS

On-board built-in self-test (BIST) diagnostics provide a customer confidence test of the various functional areas on the iSBC 186/410 board. The initialization checks are performed by the 8751 microcontroller, while the BIST package is executed by the 80186 microprocessor. On-board tests included in the BIST package are: DRAM, EPROM, 80186, 82530 SCCs, and the MPC.

Additional activities performed include initialization at power-up using the Initialization and Diagnostics Executive and a program table check, a feature allowing users to add custom code in EPROM while still maintaining full use of factory supplied BISTs. Immediately after power-up and initialization of the 8751 microcontroller, the 80186 microprocessor begins its own initialization and on-board diagnostics. Upon successful completion of these activities, the Initialization and Diagnostics Executive invokes the user-defined program table. A check is made of the program table which then executes user-defined custom programs.

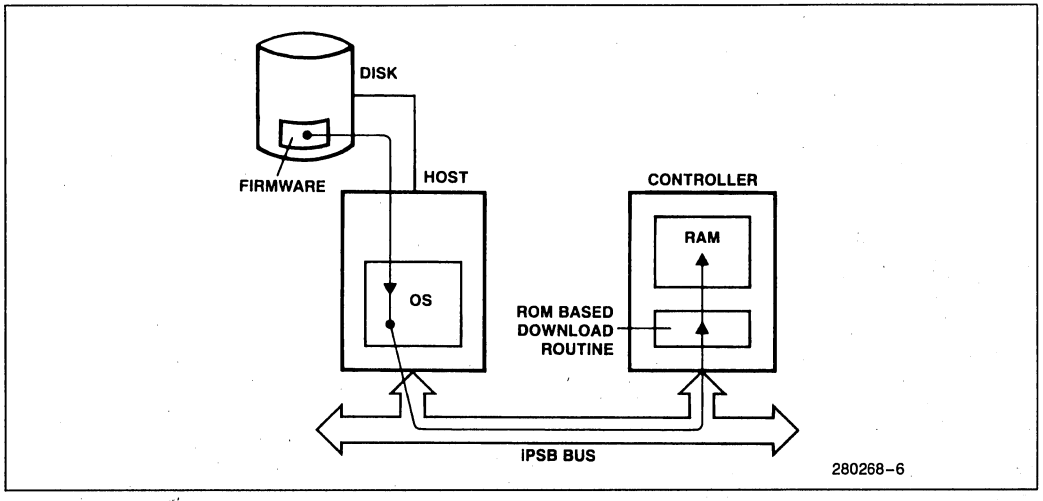


Figure 5. Download Routine

The BIST package provides a valuable testing, error reporting and recovery capability on MULTIBUS II boards enabling the OEM to reduce manufacturing and maintenance costs. An LED on the board's front panel indicates the status of power-up diagnostics. It is on when BIST diagnostics start running and is turned off upon successful completion of the BISTs.

SPECIFICATIONS

Word Size

Instruction: 8-, 16-, 24-, 32-, 40-, or 48-bits

Data: 8- or 16-bits

System Clock

CPU: 8.0 MHz

Cycle Time

Basic Instruction: 8.0 MHz—500 ns

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e., 4 clock cycles).

Memory Capacity

Local Memory

DRAM—512K bytes on-board (64K x 4-bit devices); 8 sockets provided to support additional 256K bytes

EPROM—Number of sockets—four 28-pin JEDEC sites

EPROM	Device Size (Bytes)	Max. Memory Capacity
2764	8K	32K bytes
27128	16K	64K bytes
27256	32K	128K bytes
27512	64K	256K bytes

NOTE:
**EPROM Expansion to up to a maximum of 512K bytes is achieved via attachment of the iSBC 341 EPROM (256K byte) MULTIMODULE board.

I/O Capability

Serial—Six programmable serial channels using three 82530 Serial Communications Controller components.

I/O Expansion—Two 8/16-bit IEEE P959 iSBX connectors (DMA supported). (The board supports either two single wide or one double-wide form factor iSBX module(s).)

Timers—Three programmable timers on the 80186 microprocessor.

Input Frequencies—Frequencies supplied by the internal 80186 16 MHz crystal; 82530 SCCs: crystal driven at 9.8304 MHz div. by two; iSBX Connector: crystal driven at 9.8304 MHz.

Serial Communications Characteristics

Synchronous—Internal or external character synchronization on one or two synchronous characters.

Asynchronous—5—8 data bits and 1, 1½ or 2 stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.

Baud Rates

Synchronous X1 Clock (Channels 0, 1)	
Baud Rate	**82530 Count Value (Decimal)**
64000	36
48000	49
19200	126
9600	254
4800	510
2400	1022
1800	1363
1200	2046
300	8190
Asynchronous X16 Clock (Channels 0–5)	
Baud Rate	**82530 Count Value (Decimal)**
19200	6
9600	14
4800	30
2400	62
1800	83
1200	126
300	510
110	1394

Serial Signals/Pin-Outs

RS232C Interface Pin Assignment for High Density 15-Pin Connectors

J2 Pin	RS-232C Pin Number	RS-232C Signal Name	RS-232C Signal Function
1	1	TXD	Transmit Data
2	2	RTS	Request To Send
3	3	RXD	Receive Data
4	4	CTS	Clear To Send
5	5	RXC	Receive Clock
6	6	DSS	Data Signal Select
7	7	DTR	Data Terminal Ready
8	8	DSR	Data Set Ready
9	9	DCD	Carrier Detect
10	10	STXC	Transmit Clock
11	11	SGD	Signal Ground
12	12	LCLPBK	Local Loopback
13	13	RMLPBK	Remote Loopback
14	14	TSTMD	Test Mode Indicator
15	15	RNG	Not Supported

RS422A Interface Pin Assignment for High Density 15-Pin Connectors

J1 Pin	Signal Name On Board	RS-422A Signal Name	RS-422A Signal Function
1	RS42211	TR (a)	Transmit Data
2		(a)	Control
3	RS4229	RD (a)	Receive Data
4		(a)	Indication
5		(a)	Signal Timing
6	RS42212	TR (b)	Transmit Data
7		(b)	Control
8	RS42290	RD (b)	Receive Data
9		(b)	Indication
10		(b)	Signal Timing
11			Signal Ground
12			Not Used
13			Not Used
14			Not Used
15			Chassis Ground

NOTE:
The iSBC® 186/40 board does not support the unused signals.

RS232C Interface Pin Assignment for IBM® Compatible 9-Pin Connectors

Pin Number	Signal Name	Function	In/Out
1	CD	Carrier Detect	In
2	RXD	Received Data	In
3	TXD	Transmit Data	Out
4	DTR	Data Terminal Ready	Out
5	SG	Signal Ground	
6	DSR	Data Set Ready	In
7	RTS	Request To Send	Out
8	CTS	Clear To Send	In
9	RI	Ring Indicator	Not Supported

Interrupt Capability

Potential Interrupt Sources from iPSB Bus—255 individual and 1 Broadcast

Interrupt Levels—12 vectored requests using two 8259As and 1 input to the master PIC from the slave PIC

Interrupt Requests—All levels TTL compatible

Interfaces

iPSB Bus—Compliance Level RQA/RPA D16M32

iSBX Bus—Compliance Level D8/16 DMA

Serial I/O—2 ch. RS232C or RS422A compatible, configured DTE only; 4 ch. RS232C IBM compatible only, configured DTE only.

Connectors

Interface	Connector	Part #
iPSB bus (P1)	96-pin DIN, right angle female	603-2-IEC-C096-F
RS232C/ RS422A	15-pin high density, D type, right angle female (see note)	
RS232C-only	9-pin IBM compatible, D type, right angle male (see note)	

NOTE:
The manufacturers below provide connectors which will mate with the connectors supplied on the iSBC 186/410 board front-panel.

Mating Connectors, Shells and Cables

Connectors and Shells	Manufacturer	Pins	Part No.
High Density D-type Plug (male)	AMP	15	204501-1
High Density D-type Plug (male)	Positronic	15	DD-15M
D-type Receptacle (female)	AMP	9	205203-3
D-type Receptacle (female)	ITT-Cannon	9	DE-9S
Connector Shells	AMP	(For 15 or	745171-X
	ITT-Cannon	9-pin connect.	DE-51218
	3M	above).	358-2100

Cable Description	Manufacturer	Part No.
15 Conductor—Shield, Round	Alpha	5120/15
15 Conductor—Shield, Round	Beldon	9541
10 Conductor—Shield, Round	Alpha	5120/10
9 Conductor—Shield, Round	Beldon	9539

NOTE:
All cable referenced is available in 100 ft. minimum lengths.

PHYSICAL DIMENSIONS

The iSBC 186/410 board meets all MULTIBUS II mechanical specifications as presented in the MULTIBUS II Architecture Specification Handbook (#146077, Rev. C)

Eurocard Form Factor

Depth: 220 mm (8.7 inches)

Height: 233 mm (9.2 inches)

Front Panel Width: 20 mm (0.76 inches)

Weight: 822 gm (29 ounces)

ENVIRONMENTAL CHARACTERISTICS

Temperature

Inlet air at 200 LFM airflow over all boards
Non-operating: −40°C to +75°C
Operating: 0° to +55°C

Humidity

Non-operating—95% Relative Humidity @ +55°C, non-condensing

Operating—90% Relative Humidity @ +55°C, non-condensing

ELECTRICAL CHARACTERISTICS

The maximum power required per voltage is shown below.

Voltage (volts)	Max. Current (amps)	Max. Power (watts)
+5V	8.22A	43.16W
+12V	150 mA	1.89W
−12V	150 mA	1.89W

REFERENCE MANUALS

iSBC 186/410 Serial Communications Computer User's Guide (#148941-001)

Intel MULTIBUS II Architecture Specification Handbook (#146077)

Manuals may be ordered from any Intel Sales Representative, Distribution Office, or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 186/410	MULTIBUS II Serial Communications Computer

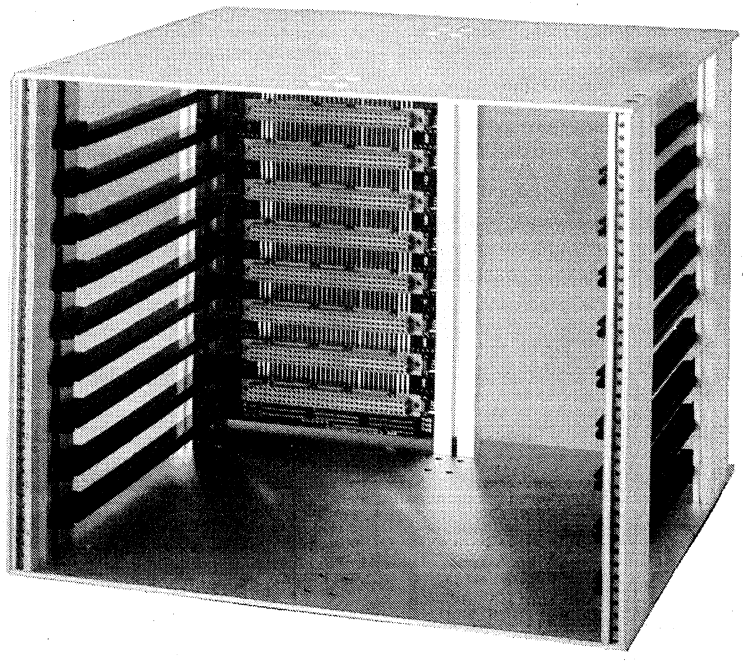
MULTIBUS® II System Packaging and Development Accessories

14

iSBC® PKG/606
iSBC PKG/609
MULTIBUS® II CARDCAGE ASSEMBLIES

- **Available in Two Sizes to Hold Up to 6 or 9 MULTIBUS® II Boards**
- **Designed to Mount Inside a Chassis or Other Enclosure**
- **Accommodates Intel iSBC® PKG/902 and iSBC® PKG/903 2 and 3 Slot iLBX™ II Backplanes**
- **All Lines Fully Terminated per the iPSB MULTIBUS II Specification**
- **Assembly Uses Aluminum Extrusion Construction for Strength and Rigidity**
- **Uses a 6 Layer Parallel System Bus (iPSB) Backplane**

The iSBC PKG/606/609 series of cardcages are designed to mount and interconnect up to 6 or 9 MULTIBUS II boards for small to medium size advanced MULTIBUS II microcomputer systems. The cardcages are compact in size and easily mount in standard or custom enclosures. Extra-wide support extrusions and heavy duty endplates help make the iSBC PKG/606/609 cardcage assemblies especially suited for installation in systems located in high vibration or high shock environments. Installed in the cardcage assembly is a 6 layer iPSB backplane that utilizes separate power and ground planes and fully terminates all signal lines. This layout minimizes system noise and ensures reliable operation even in a fully loaded, multiprocessor-based system.



280075-1

September 1986
Order Number: 280075-002

FUNCTIONAL DESCRIPTION

Mechanical Features

The cardcages accommodate up to 6 (iSBC PKG/606) or 9 (iSBC PKG/609) MULTIBUS II boards spaced at 0.8 inch centers. The assemblies are designed to hold "double high" (6U) Euro form-factor boards (233.4 mm high x 220 mm deep) or a mixture of "single high" (3U) and "double high" boards using additional hardware (not supplied). Each installed board is held in place by two screws supplied as part of the board retainer hardware.

The cardcage frame is built using five support extrusions and two aluminum end plates as shown in figure 1. Both cardcages are 10.5″ wide and 10.1″ deep and vary in height according to model (see specifications section).

The cardcages are designed to mount inside chassis or other enclosures and may be installed so that the MULTIBUS II boards load either horizontally or vertically in the unit. All assembly hardware is countersunk allowing the cardcages to be mounted flush against any internal chassis surface.

A Parallel System Bus (iPSB) backplane is mounted to the P1 side of the assembly, and one or more iLBX™ II backplanes (not supplied) can be mounted to the P2 side.

Electrical Features

The iPSB backplane uses a 6 layer design with separate power and ground layers and a signal routing scheme which minimizes ringing, crosstalk, and capacitive loading on the bus. Mounted on the backplane are 6 or 9, 96-pin, female DIN connectors (depending on model), bus termination resistors, decoupling capacitors, and power terminals. Press-fit technology is used throughout. The PC board is UL recognized for flammability. The card cages themselves are UL recognized components.

Single In-line Package (SIP) style resistors are used to terminate all address, clock, data, and control lines. Each termination consists of two resistors which connects the line to +VCC and ground. Different size resistors are used according to the type of driver connected to the line in an operating system.

The DIN type connectors are female, 96 pins, fully gold plated, and meet IEC standard 603-2-IEC-C096F. The connectors are mounted on 0.8″ centers to match Intel's iPSB (Parallel System Bus) MULTIBUS II backplanes and are keyed to ensure proper mating to the MULTIBUS II board. The connector can provide up to 9 amps of current at +5V to each MULTIBUS II board in addition to the current available over the iLBX II backplane.

Screw terminals on the backplane are provided for connection to +5V, ±12V power and ground. In addition, an extra +5V terminal is provided for connection to a backup battery for memory protection during power fail conditions. These terminals, each of which can handle up to 25 amps of current at 55°C, provide a simple and highly reliable connection method to the system power supply.

The first slot position is designed to accept the Central Services Module (CSM) MULTIBUS II board. All other slots can accept any combination of MULTIBUS II boards.

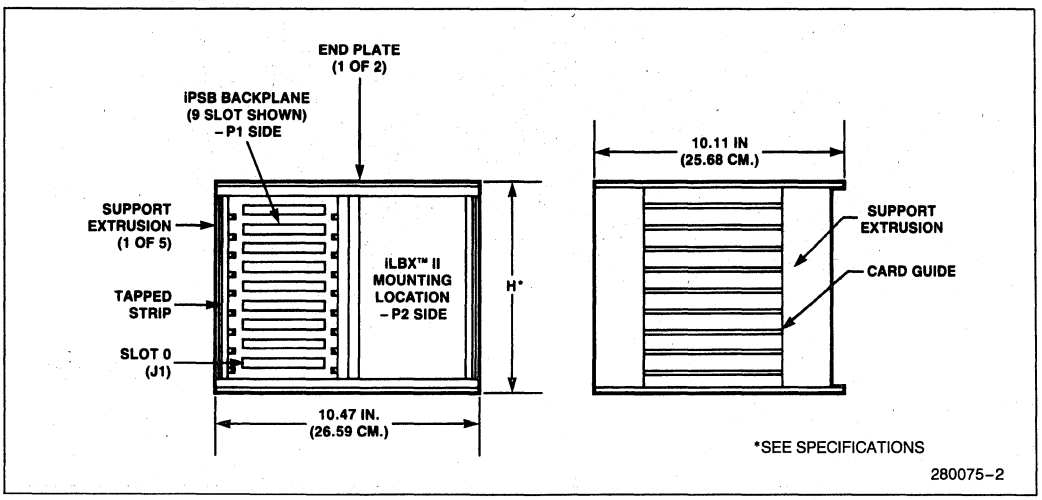


Figure 1. Cardcage Assembly Dimensions (iSBC® PKG/609 shown)

SPECIFICATIONS

Mechanical

Specification	iSBC® PKG/606 Cardcage	iSBC® PKG/609 Cardcage
Board Capacity	6	9
Dimensions Height	15.20 cm (5.98 in.)	21.20 cm (8.38 in.)
Width	26.59 cm (10.47 in.)	26.59 cm (10.47 in.)
Depth	25.93 cm (10.21 in.)	25.93 cm (10.21 in.)
Weight	4 lbs. (1.8 kg)	5 lbs. (2.3 kg)
Board Spacing	0.8 in. (20.3 cm)	
Mounting Hole Locations	See Figure 2	
Construction Materials, Cardcage Frame	Aluminum extrusions and end plates, nylon card guides	
Construction Method iPSB Backplane	Six layer backplane with separate VCC and ground layers; all connectors, power terminals, and resistor/capacitor sockets are press-fit into the backplane	
Connector Type	96 pin "DIN" female, gold plated, meets IEC standard 603-2-IEC-C096-F	

Electrical

iPSB Backplane— Meets Intel MULTIBUS II specification No. 146077 for board dimensions, layout, signal line termination, and transmission characteristics

Power Connections— Type: Screw terminal block, AMP P/N 55181-1, Winchester P/N 121-25698-2, or equivalent

Quantity of Power Terminals and Current Rating:

Voltage	iSBC® PKG/606 Cardcage		iSBC® PKG/609 Cardcage	
	Quantity	Current (amps)	Quantity	Current (amps)
+5	3	54	4	81
+12	1	12	1	18
−12	1	12	1	18
+5BB	1	12	1	18
GND	4	78	5	135

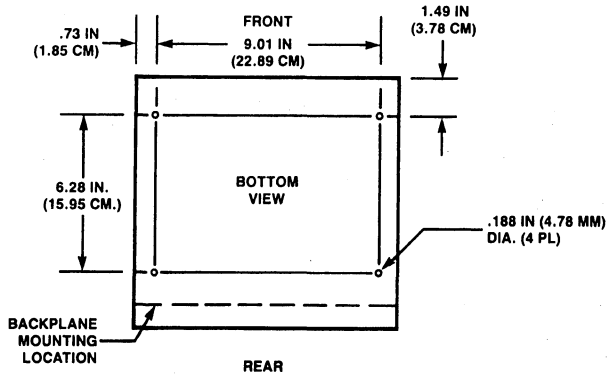


Figure 2. Mounting Hole Locations

Mating Connection: No. 6 locking spade or ring tongue lug

Maximum current available per slot:

Voltage	Current
+ 5V	9A
+12V	2A
−12V	2A
+5BB	2A

Operating Environment:
0–55°C (at 25 amps per power terminal);
0–70°C (at ≤ 18 amps per power terminal);
0% to 95% relative humidity, non-condensing;
0–10,000 ft. altitude.

Reference Manual— MULTIBUS II Cardcage Assembly and iLBX II Backplane User's Guide, P/N 146709-001 (supplied).

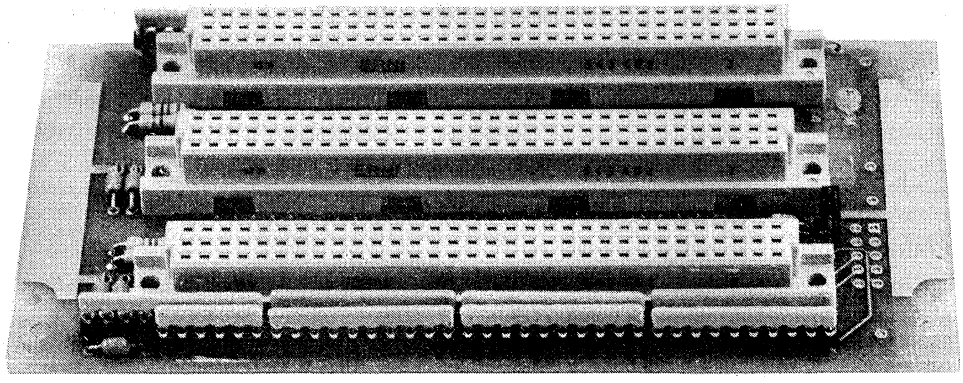
ORDERING INFORMATION

Part Number	Description
iSBC PKG/606	6 slot MULTIBUS II Cardcage Assembly
iSBC PKG/609	9 slot MULTIBUS II Cardcage Assembly

iSBC® PKG/902
iSBC® PKG/903
MULTIBUS® II iLBX™ II BACKPLANES

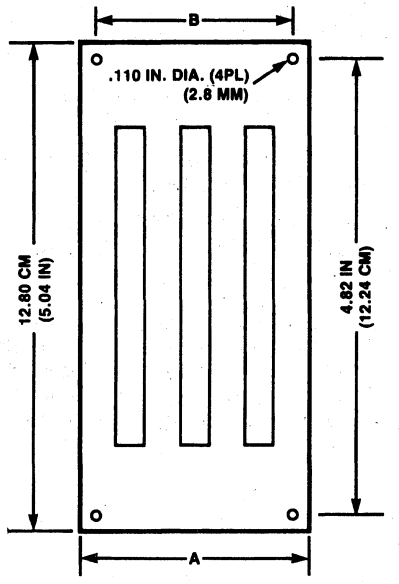
- **Provides iLBX™ II Interconnect for Fastest CPU/Memory Data Transfers**
- **Designed to Mount in MULTIBUS® II Cardcage Assemblies**
- **Meets All Electrical and Mechanical Requirements of the MULTIBUS® II Specifications**
- **Uses a 6 Layer, Fully Terminated Backplane**
- **Includes a 10 Pin Connector for BITBUS™ Applications**
- **Available in 2 Slot (iSBC® PKG/902) and 3 Slot (iSBC® PKG/903) Sizes**

The iSBC PKG/902 and iSBC PKG/903 series of iLBX II backplanes are designed to mount on the P2 side of Intel's MULTIBUS II cardcage assembly or other double Euro (6U) cardcage. One or more backplanes may be installed in a system to allow high speed data transfers between the CPU and memory boards installed in the system. The iLBX II backplane uses a 6 layer PCB with separate power and ground planes and full termination on all signal lines. This design minimizes system noise and ensures reliable operation in all applications.



280074-1

October 1986
Order Number: 280074-002



Dimensions		A	B
iSBC PKG/902	IN	1.55	.80
	CM	3.94	2.03
iSBC PKG/903	IN	2.35	1.60
	CM	5.97	4.06

Figure 1. iLBX™ II Board Dimensions (iSBC® PKG/903 Shown)

FEATURES

Mechanical and Electrical

The iSBC PKG/902 and iSBC PKG/903 iLBX II backplanes use a 6 layer printed circuit board (PCB) with separate power and ground layers and a signal lead routing scheme which minimizes ringing, crosstalk, and capacitive loading on the bus. Mounted on the PCB are two (iSBC PKG/902) or three (iSBC PKG/903) 96 pin DIN connectors, one 10-pin BITBUS connector, terminating resistors, decoupling capacitors, and power terminals. The resistors and capacitors are mounted into sockets, and all parts are press-fit into the backplane. The PCB is UL recognized for flammability.

Single In-line Package (SIP) style resistors are used to terminate all address, clock, data, and control lines. Each termination consists of two resistors which connects the line to +VCC and ground. Different size resistors are used according to the type of driver connected to the line in an operating system. The SIP style resistors help make the board compact in size and allows the designer to mount several backplanes directly adjacent to one another in a system without having to skip slots.

Mounted on the rear of the backplane is a 10-pin BITBUS connector. This connector serves as the serial communication interface for any iSBX 344 BITBUS controller boards installed in the system.

The DIN type connectors are female, 96 pins, fully gold plated, and meet IEC standard 603-2-IEC-C096F. The connectors are mounted on 0.8″ centers to match Intel's iPSB (Parallel System Bus) MULTIBUS II backplanes and are keyed to ensure proper mating to the MULTIBUS II board. The connector can provide up to 6 amps of current at +5V to each MULTIBUS II board in addition to the current available over the Parallel System Bus backplane.

Screw terminals on the backplane are provided for connection to +5V power and ground. These terminals, each of which can handle up to 25 amps of current, provide a simple and highly reliable connection method to the power supply.

SPECIFICATIONS

Mechanical and Environmental

Connector Spacing: 20.3 cm (0.8 in)

Number of Slots: iSBC PKG/902: 2 slots
iSBC PKG/903: 3 slots

Board Dimensions: See Figure 1

Weight: iSBC PKG/902—0.2 kg (8 oz)
iSBC PKG/903—0.3 kg (12 oz)

Connectors:

DIN: 96-pin female, gold plated, meets IEC standard 603-2-IEC-C096-F

BITBUS: 10-pin male, gold plated, T&B Ansley 609-1012M, or equivalent

Constructed Method: Six layer backplane with separate VCC and Ground layers
All connectors, power terminals, and resistor/capacitor sockets are press-fit into the backplane

Mounting Hole Location: See Figure 1

Operating Environment: 0°C–70°C ambient temperature; 0% to 90% relative humidity, non-condensing; 0 ft.–10,000 ft. altitude

Electrical

Backplane Electrical Characteristics and Line Terminations:	Per Intel MULTIBUS II specification 146077, Sec. II, iLBX II

Power Connections

Type: Screw terminal block: AMP P/N 55181-1; Winchester P/N 121-25698-2; or equivalent

Mating Connection: No. 6 locking spade or ring tongue lug

Quantity: 2(VCC, Ground)

Current Rating: iSBC PKG/902: 12 amps; iSBC PKG/903: 18 amps (Power and Ground)

Maximum Current Available Per Slot: 6 amps (over the iLBX II backplane)

REFERENCE MANUAL

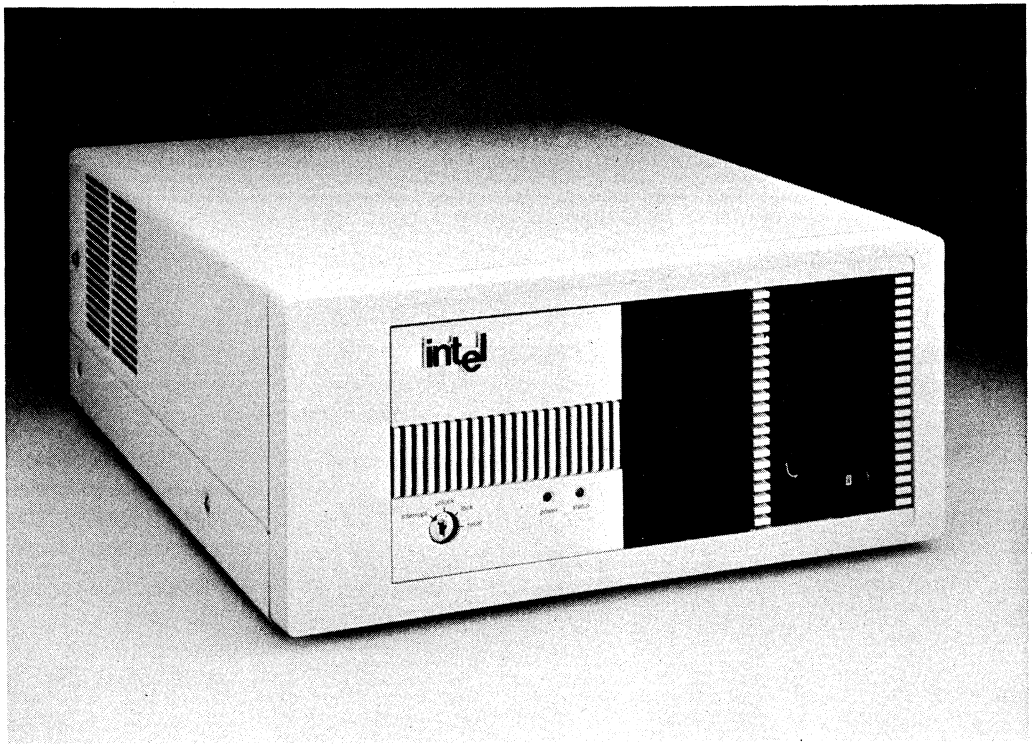
MULTIBUS II Cardcage Assembly and iLBX Backplane User's Guide, P/N 146709-001 (not supplied)

ORDERING INFORMATION

Part Number	Description
iSBC PKG/902	2 slot iLBX II Backplane
iSBC PKG/903	3 slot iLBX II Backplane

SYP 500 MULTIBUS® II SYSTEM CHASSIS

- Full enclosure MULTIBUS® II design development tool or OEM chassis
- Office and industrial applications
- 3 full height/6 half height peripheral bays
- 8 slot MULTIBUS® II cardcage assembly
- 3 slot iLBX™ II backplane
- 535 Watt power supply
- Fully tested: low-noise, shock/vibration and electrostatic resistant



DECEMBER 1986
ORDER NUMBER: 280153-002

The SYP 500 System Chassis is a MULTIBUS II design tool enabling product designers to begin work immediately on MULTIBUS II development projects. It is also ideal for OEM applications. Two front mounted LEDs indicate "Power On" and "Status" (PSB busy) while a keyswitch provides external "reset" capabilities for the chassis. The voltage selector, power-on switch and cardcage opening are located in the rear of the chassis. Three peripheral bays, two of which are accessible from the front of the chassis, support up to three industry standard 5.25" full-height or six half-height peripherals. An eight slot cardcage, Parallel System Bus and iLBX II backplane assembly are integrated with a 535 Watt power supply.

FUNCTIONAL DESCRIPTION

Mechanical Features

Intel's SYP 500 MULTIBUS II Chassis is a full enclosure, off-the-shelf design development tool and OEM chassis. Designers and systems integrators can integrate their MULTIBUS II board set with tape, Wini or floppy peripherals into a complete system. The SYP 500 has three full-height 5.25" peripheral bays. Peripheral power cables, office and industrial environment cooling, and peripheral mounting brackets for industry standard full- or half-height peripherals are provided with the chassis. Access via the front panel allows two of the bays to be configured with removable media peripherals e.g. tape and floppy drives.

This chassis includes an eight-slot MULTIBUS II cardcage assembly with 0.8" centers (slot width). The cardcage is made with heavy duty endplates and extra-wide support extrusions to ensure adequate support for most applications. For industrial applications, this chassis is mountable into any 19" vertical rack.

Two backplanes are installed in the cardcage assembly: the system backplane and the auxiliary backplane. The system backplane is the Parallel System Bus (iPSB) for communications between up to eight MULTIBUS II boards. This backplane utilizes separate power and ground planes and fully terminates all signal lines. The auxiliary backplane, on the other hand, provides direct high speed interconnection between a processor board and memory boards. It contains three iLBX slots. One of these slots has a 10-pin BITBUS connector that serves as a serial interface for any iSBX 344 BITBUS controller board installed in the system. This cardcage conforms to the published MULTIBUS II specification.

Electrical Features

The SYP 500 chassis has a 535 Watt switching power supply with selectable AC power input of 115 V or 220 V at 47-63Hz. The AC input power is externally selectable with a slide switch mounted on the rear of the chassis. A power distribution board is installed in the chassis to allow easy connection to all peripheral bays through six plugs mounted on the power distribution board.

The chassis has been fully tested to ensure low-audible noise emission, resistance to electrostatic discharge and resistance to appropriate levels of vibration and shock in both office and industrial environments.

SPECIFICATIONS:

Electrical Parameters

Maximum Amperage:

Voltage	Current
+ 5V	75A
+12V	10A
−12V	2.5A

Designed to meet: UL 478
CSA C22.2 No. 154
FCC Class B
VDE Level B
IEC 435

Operational Parameters

AC Power Input: 90-132 VAC or
180-264 VAC at 47-63 Hz

Operating Temperature Range: 10°C to 55°C

Storage Temperature: −40°C to 60°C

Operational Humidity: 10% to 85% relative, non-condensing

Physical Parameters

Height: 7.75" (19.7 cm)
Width: 17.5" (44.5 cm)
Depth: 22.25" (56.5 cm)
Weight: 33 lbs. (15 kg.)

Bay Dimensions

3.5" wide × 6" high × 8.5" deep

Acoustical Noise

Less than 50 dbA in office environment (30°C)

Electrostatic Discharge

No hard errors to 12.5 kV

Contents

- 8-slot MULTIBUS II Chassis
- Power cord
- User's guide
- Two keys
- Peripheral mounting brackets & power cables

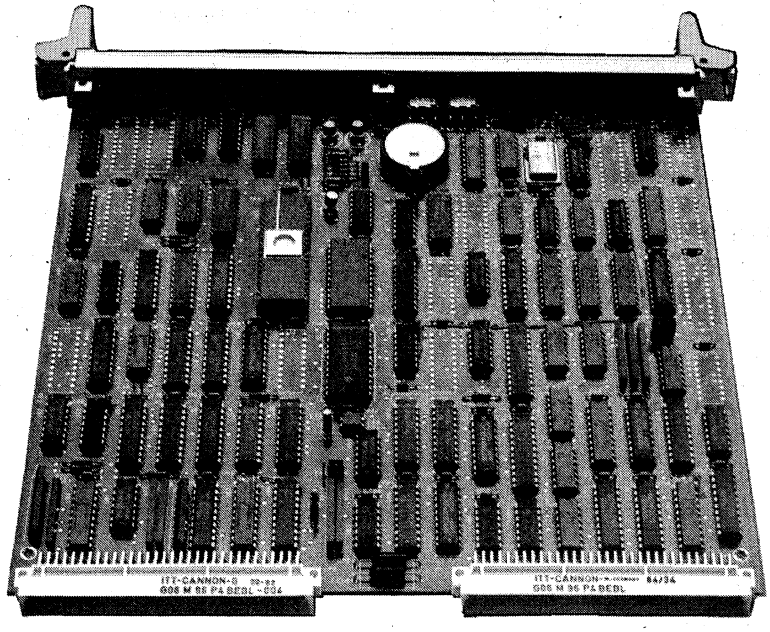
Ordering Information

SYP 500

iSBC® CSM/001
CENTRAL SERVICES MODULE

- **iSBC® CSM/001 Central Services Module Integrates MULTIBUS® II Central System Functions on a Single Board**
- **MULTIBUS® II Parallel System Bus Clock Generation for all Agents Interfaced to the MULTIBUS II iPSB Bus**
- **System-wide Reset Signals for Power-up, Warm Start, and Power Failure/ Recovery**
- **System-wide Time-out Detection and Error Generation**
- **Slot I.D. and Arbitration I.D. Initialization**
- **MULTIBUS II Interconnect Space for Software Configurability and Diagnostics**
- **Built-In Self Test (BIST) Power-up Diagnostics with LED Indicator and Error Reporting Accessible to Software via Interconnect Space**
- **General Purpose Link Interface to Other Standard (MULTIBUS I) or Proprietary Buses**
- **Time-of-day Clock Support with Battery Back-up on Board**
- **Double-high Eurocard Standard Form Factor, Pin and Socket DIN Connectors**

The iSBC CMS/001 Central Services Module is responsible for managing the central system functions of clock generation, power-down and reset, time-out, and assignment of I.D.s defined by the MULTIBUS II specification. The integration of these central functions in a single module improves overall board area utilization in a multi-board system since these functions do not need to be duplicated on every board. The iSBC CMS/001 module additionally provides a time-of-day clock and the general purpose link interface to the other standard (MULTIBUS I) or proprietary buses.



280070-1

November 1986
Order Number: 280070-002

FUNCTIONAL DESCRIPTION

Overall

The iSBC CMS/001 Central Services Module integrates MULTIBUS II central system functions on a single board. Each MULTIBUS II system requires management of these central system functions as defined in the MULTIBUS II specification. Figure 1 illustrates a typical multiprocessing MULTIBUS II system configuration. To perform its central system functions, the iSBC CSM/001 Central Services Module has a fixed slot I.D. and location in the backplane. The iSBC CSM/001 board additionally provides an interface to the MULTIBUS I Link board and a time-of-day clock.

Architecture

The iSBC CSM/001 board is functionally partitioned into 6 major subsystems. The Central System Wide Control subsystem includes MULTIBUS II iPSB bus clock generation and system wide reset signal generation. The Time-Out Control subsystem provides system wide time out detection and error generation. The System Interconnect Space subsystem controls I.D. initialization and software configurable interconnect space. The Link Board interface subsystem provides an interface to the MULTIBUS I Link board or links to other buses. The last two subsystems are of the Time-of-Day clock and the iPSB bus interface. These areas are illustrated in Figure 2.

CENTRALIZED SYSTEM-WIDE CONTROL SUBSYSTEM

Parallel System Bus Clock Generation

The CSM generates the Parallel System Bus clocks. The Bus Clock (BCLK*) 10 MHz signal and the Constant Clock (CCLK*) 20 MHz signal are supplied by CSM to all boards interfaced to the Parallel System Bus. These boards use the Bus Clock 10 MHz signal for synchronization, system timing, and arbitration functions. The Constant Clock is an auxiliary clock. The frequency of the Bus Clock and Constant Clock can be halved via jumpers for diagnostic purposes.

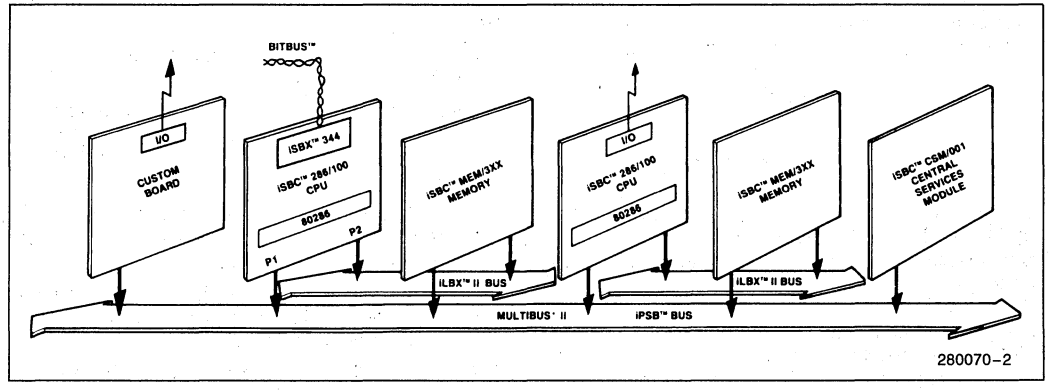


Figure 1. Typical MULTIBUS® II System Configuration

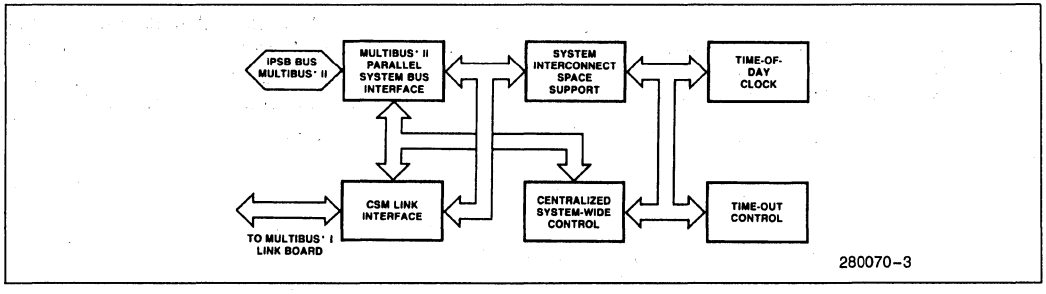


Figure 2. Block Diagram of iSBC® CSM/001 Board

Reset Control and Power-Fail/ Recovery

The CSM sends a system-level reset/initialization signal to all boards interfaced to the Parallel System Bus. The CSM assigns slot I.D. and arbitration I.D. to these boards during this initialization process. It provides this signal upon pressing of the reset switch, restoration of system power or a software request for reset received via the CSM interconnect space. The reset switch may be jumper-configured to cause a power-up or warm reset, with cold reset the default configuration. The reset switch is located on the front panel. Additionally, warm reset and cold reset signals can be input through the P2 connector.

The CSM power supply interface is accomplished via the ACLO input of the P2 connector. ACLO is an open collector input from the power supply which provides advance warning of imminent power fail. If battery backup is not required, a jumper is provided on the CSM to disable the power fail signal ACLO.

TIME-OUT SUBSYSTEM

The TIMOUT* (Time-Out) signal is provided by the CSM whenever it detects the failure of a module to complete a handshake. This TIMOUT* signal is received by all boards interfaced to the iPSB bus and may be disabled via the interconnect space.

INTERCONNECT SUBSYSTEM

The CSM Interconnect subsystem provides arbitration I.D., and slot I.D. initialization, software configurable interconnect space, and on-board diagnostics capability.

At reset, the CSM supplies each board interfaced to iPSB bus with its slot I.D. and its arbitration I.D. The slot I. D. assignment allows user or system software to address any board by its physical position in the backplane.

The interconnect space has both read-only and software configurable facilities. The read-only registers hold information such as vendor number and board type, so that this information is available to the system software. The CSM software configurable interconnect space allows write operations to support board configuration and diagnostics under software control. The CSM also uses interconnect space for system wide functions such as providing a time/date record (from time-of-day clock), software access to diagnostics and software control of the system wide functions.

BUILT-IN-SELF-TEST (BIST) DIAGNOSTICS

Self-test/diagnostics have been built into the heart of the MULTIBUS II system. These confidence tests and diagnostics improve reliability and reduce manufacturing and maintenance costs. LED 1 (labeled BIST) is used to indicate the status of the Built-In-Self-Test. It is turned on when the BIST starts running and is turned off when the BIST completes successfully. In addition, all error information is recorded in interconnect space so it is accessible to software for error reporting.

The Built-In-Self-Tests performed by the on-board microcontroller at power-up or at software command are:

1. PROM Checksum Test—Verifies the contents of the 8751 microcontroller.
2. RAM Test—Verifies that each RAM location of the 8751 microcontroller may store 0's and 1's by complementing and verifying twice each RAM location.
3. Real Time Clock Chip RAM Test—Verifies that reads and writes to the RAM locations on Real Time Clock Chip are functional.
4. Real Time Clock Test—Reads and writes all RAM locations of the RTC chip. Not run at power-up due to destructive nature.
5. Arbitration/Slot I.D. Register Test—Verifies that arbitration and slot I.D.s can be read and written from on-board.
6. 8751 Status Test—Verifies that input pins of the 8751 are at correct level.
7. Clock Frequency Test—Tests accuracy of Real Time Clock to 0.2% against bus clock.

CSM LINK INTERFACE

The CSM Link Interface and the MULTIBUS I iSBC LNK/001 board provides a bridge between MULTIBUS I and MULTIBUS II systems. Hybrid systems can be built for development or target. The CSM Link Interface uses the P2 connector on the iSBC CSM/001 module for transferring commands and data from MULTIBUS II to a MULTIBUS I Link board. The MULTIBUS I Link board (iSBC LNK/001) is purchased separately from the iSBC CSM/001 board and includes the cable which connects the iSBC CSM/001 board and the MULTIBUS I Link board (see Figure 3).

The CSM Link Interface supports 8- or 16-bit transfers via a 16-bit address/data path. The iSBC LNK/001 board resides in the MULTIBUS I system and provides a memory and I/O access window to MULTIBUS I from the MULTIBUS II Parallel System Bus. Only one iSBC LNK/001 board can be connected to the iSBC CSM/001 module.

TIME-OF-DAY CLOCK SUBSYSTEM

The Time-Of-Day Clock subsystem consists of a clock chip, battery, and interface circuitry. The clock provides time keeping to 0.01% accuracy of fractions of seconds, seconds, minutes, hours, day, day of week, month, and year. This information is accessible via the interconnect space. The battery backup for the clock chip provides 2 years of operation.

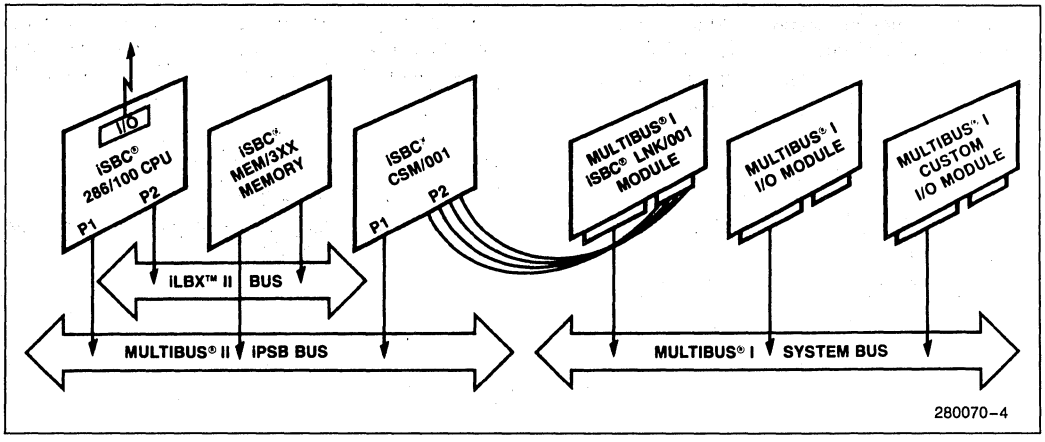


Figure 3. iSBC® CSM/001 Link Interface

SPECIFICATIONS

System Clocks

BCLK* (Bus Clock)	10 MHz
CCLK* (Constant Clock)	20 MHz
LCLK* (Link Clock)	10 MHz

Jumper option available to divide these frequencies in half

Interface Compliance

MULTIBUS II Bus Architecture Specification (#146077)

Link Cable

The Link cable uses a 64-conductor ribbon cable for interconnecting the CSM board to the Link Board. The maximum length for the cable is 1 meter.

Interface Specifications

Location	Function	Part #
P1	iPSB Bus	603-2-IEC-C096F
P2	Link and Remote Services	603-2-IEC-C064-F

PHYSICAL DIMENSIONS

The iSBC CSM/001 board meets all MULTIBUS II mechanical specifications as presented in the MULTIBUS II specification (#146077).

Double-High Eurocard Form Factor:

Depth:	220 mm. (8.7 in.)
Height:	233 mm. (9.2 in.)
Front Panel Width:	20 mm. (0.78 in.)
Weight:	4820 gm. (16.5 oz.)

ENVIRONMENTAL REQUIREMENTS

Temperature: (inlet air) at 200 LFM airflow over boards

Non-operating: −40 to +70°C
Operating: 0 to +55°C

Humidity: Non-operating: 95% RH @ 55°C
Operating: 90% RH @ 55°C

POWER REQUIREMENTS

Voltage (volts)	Current (amps)
+5	6A (max.)
+5 VBB	1A (max.)

BATTERY CHARACTERISTICS

3V nominal voltage; capacity of 160 milliamp hours minimum.

BATTERY DIMENSIONS

Outside dimension	20 mm–23 mm
Height	1.6 mm–3.2 mm

REFERENCE MANUALS

iSBC CSM/001 Board Manual (#146706-001)

Intel MULTIBUS II Bus Architecture Specification (#146077)

Manuals may be ordered from any Sales Representative, Distributor Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051.

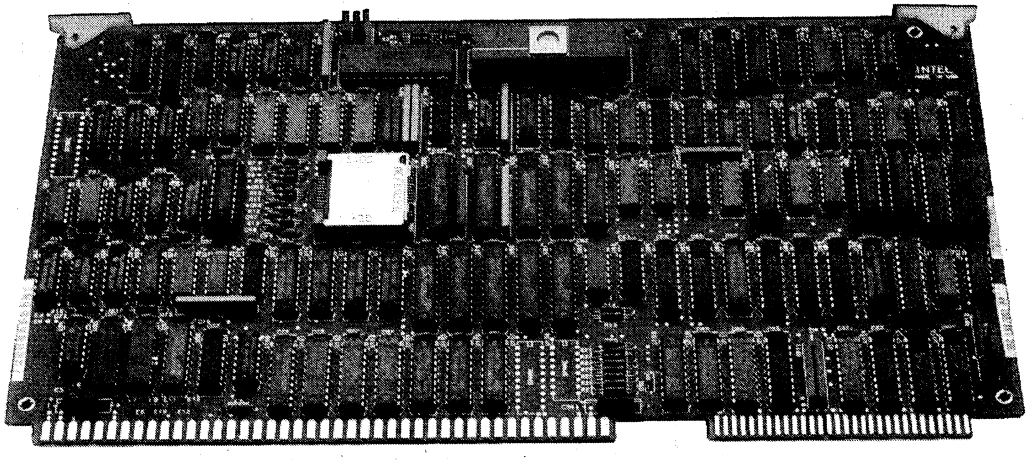
ORDERING INFORMATION

Part Number	Description
iSBC CSM/001	MULTIBUS II Central Services Module

iSBC® LNK/001 BOARD
MULTIBUS® II TO MULTIBUS® I LINK BOARD

- **Development Vehicle Making MULTIBUS® I iSBC® Boards Accessible to MULTIBUS® II Board Designers**
- **On Board 128K Byte Dual Port DRAM Memory**
- **16M Bytes of MULTIBUS® I Memory Mapped into MULTIBUS® II Memory Space Configurable from MULTIBUS® II Interconnect Space**
- **32K Bytes of MULTIBUS® I I/O Mapped into MULTIBUS® II I/O Space Configurable from MULTIBUS® II Interconnect Space**
- **Conversion of MULTIBUS® I Interrupts to MULTIBUS® II Interrupt Messages**
- **MULTIBUS® I Form Factor Board**
- **Connects to MULTIBUS® II Central Services Module (iSBC CSM/001 Board) via a 3 Foot Flat Ribbon Cable**

The iSBC LNK/001 board maps MULTIBUS I memory and I/O space into the MULTIBUS II iPSB bus and converts MULTIBUS I interrupts into MULTIBUS II interrupt messages. Up to 16M Bytes of MULTIBUS I memory and up to 32K Bytes of MULTIBUS I I/O is addressable from MULTIBUS II through the iSBC LNK/001 board. Additionally, 128K Bytes of dual port DRAM memory resides on the iSBC LNK/001 board for use by both MULTIBUS I and MULTIBUS II systems. MULTIBUS II OEM product designers can now speed hardware and software development efforts by using the iSBC LNK/001 board to access standard or custom MULTIBUS I products.



280135-1

November 1988
Order Number: 280135-002

GENERAL DESCRIPTION

The iSBC LNK/001 board makes MULTIBUS I products accessible to MULTIBUS II designers. The iSBC LNK/001 board resides in the MULTIBUS I system and connects to the Central Services Module (iSBC CSM/001 board) via a 3 foot flat ribbon cable. The ribbon cable connects the P2 connector of the iSBC LNK/001 board to the P2 connector on the Central Services Module. The iSBC LNK/001 board supports:

a. 128K Bytes of Dual Port DRAM,

b. 16- and 24-bit addressing into 16M Bytes of MULTIBUS I memory with 8- and 16-bit data paths,

c. 8- and 16-bit addressing into 32K Bytes of MULTIBUS I I/O with 8- and 16-bit data paths,

d. MULTIBUS I interrupt to MULTIBUS II interrupt message conversions of up to eight levels of non bus-vectored interrupts via an 8259A programmable interrupt controller, and

e. initialization tests and Built-In-Self-Test (BIST) using interconnected address space.

APPLICATIONS

The primary application of the iSBC LNK/001 board is in the design development environment. The iSBC LNK/001 board allows designers to start their development efforts by leveraging existing MULTIBUS I products or to begin modular design efforts and preserve investments in custom products. In either case, the use of leverage with existing MULTIBUS I hardware and software allows designers to begin their MULTIBUS II product designs.

MEMORY AND I/O READ/WRITE SEQUENCE

The iSBC LNK/001 board establishes a master/slave relation between a MULTIBUS II system and a MULTIBUS I system. A MULTIBUS II agent requesting a memory transfer involving the iSBC LNK/001 board is directed through the CSM to the iSBC LNK/001 Dual Port memory or a MULTIBUS I slave. If the access address is within the MULTIBUS II Dual Port window, the transaction is acknowledged by the iSBC LNK/001 board and returned to the MULTIBUS II iPSB through the CSM. In the event the address is outside the MULTIBUS II Dual Port window, the transaction is directed to the MULTIBUS I system. Here the iSBC LNK/001 board enters arbitration for the MULTIBUS I system bus to complete the requested transaction. Once the iSBC LNK/001 board is the owner of the MULTIBUS I system bus, data is transferred to or from the iSBC LNK/001 board/Central Services Module connection. The MULTIBUS I slave acknowledges the transfer and the iSBC LNK/001 board passes the acknowledge on through the Central Services Module to the MULTIBUS II iPSB.

MULTIBUS II I/O operations are always directed to the MULTIBUS I I/O slaves and consequently require arbitration for the MULTIBUS I system bus.

INTERCONNECT MAPPING

The function record of the iSBC LNK/001 board, a function record within the Central Services Module interconnect template, appears as a board within a board (see Table 1). The actual iSBC LNK/001 board configuration is done through unique interconnect registers using the same slot ID as the Central Services Module. The iSBC LNK/001 function record begins at an offset of 256 from the start of the CSM template and the EOT (End Of Template) byte is attached as the last function of the iSBC LNK/001 function record.

Dual Port 128K Byte DRAM Memory

A dynamic RAM Dual Port, resident on the iSBC LNK/001 board, provides a 128K Byte media for

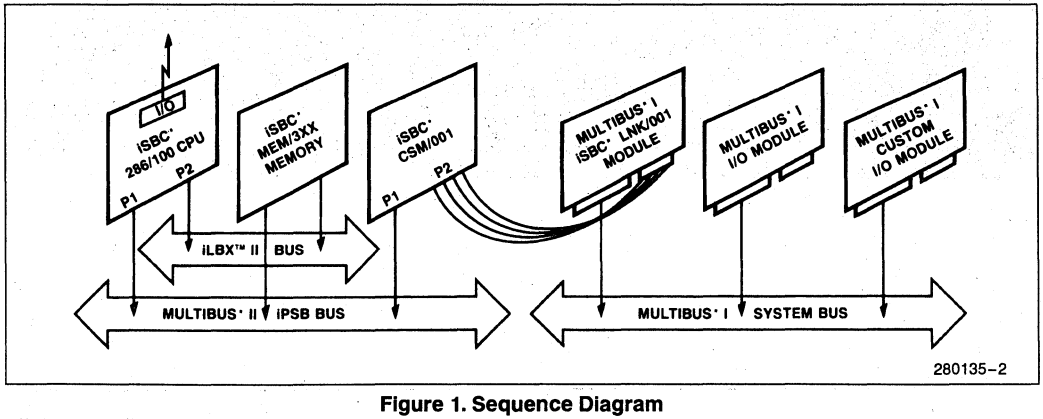


Figure 1. Sequence Diagram

MULTIBUS I and MULTIBUS II agents to pass data efficiently. With both buses sharing the Dual Port memory the need for the MULTIBUS II system to continuously arbitrate for MULTIBUS I system access is eliminated. Consequently, each bus can continue operating at its respective speed when accessing the iSBC LNK/001 Dual Port memory.

MULTIBUS® I Memory Addressability

The MULTIBUS I system views the iSBC LNK/001 Dual Port as a contiguous 128K Byte memory block mapped into the 16M Bytes of MULTIBUS I memory address space starting at the Dual Port Start Address register value. This memory block, configurable on any 64K Byte boundary within the MULTIBUS I memory address space, is set via interconnect accesses to the iSBC LNK/001 function records from the MULTIBUS II system (see Table 1). The first 16M Bytes of MULTIBUS II memory space can be mapped in the 16M Bytes of MULTIBUS I memory address space (see Figure 3).

MULTIBUS® I I/O Addressability

Up to eight 4K Byte blocks of MULTIBUS II I/O space can be mapped into MULTIBUS I I/O space

Table 1. Function Record Overview iSBC® LNK/001 Board

Offset	Description	Offset	Description
0–255	iSBC CSM/001 Header and Function Record	271	MBI Dual Port End Address
		272	MBII Dual Port Start Address
256	Board Specific Record Type	273	MBII Dual Port End Address
257	Record Length	274	MBII Memory Start Address
258	Vendor ID, Low Byte	275	MBII Memory End Address
259	Vendor ID, High Byte	276	I/O 4K Segment Control
260	Link Version Number	277	MBI Interrupt Enable
261	Hardware Revision Test Number	278	Link Interrupt 0 Destination Address
262	Link General Status	279	Link Interrupt 1 Destination Address
263	Link General Control	280	Link Interrupt 2 Destination Address
264	Link BIST Support Level	281	Link Interrupt 3 Destination Address
265	Link BIST Data In	282	Link Interrupt 4 Destination Address
266	Link BIST Data Out	283	Link Interrupt 5 Destination Address
267	Link BIST Slave Status	284	Link Interrupt 6 Destination Address
268	Link BIST Master Status	285	Link Interrupt 7 Destination Address
269	Link BIST Test ID	286	Interrupt Source Address
270	MBI Dual Port Start Address	287	Link Status Register
		288	EOT (End of Template)

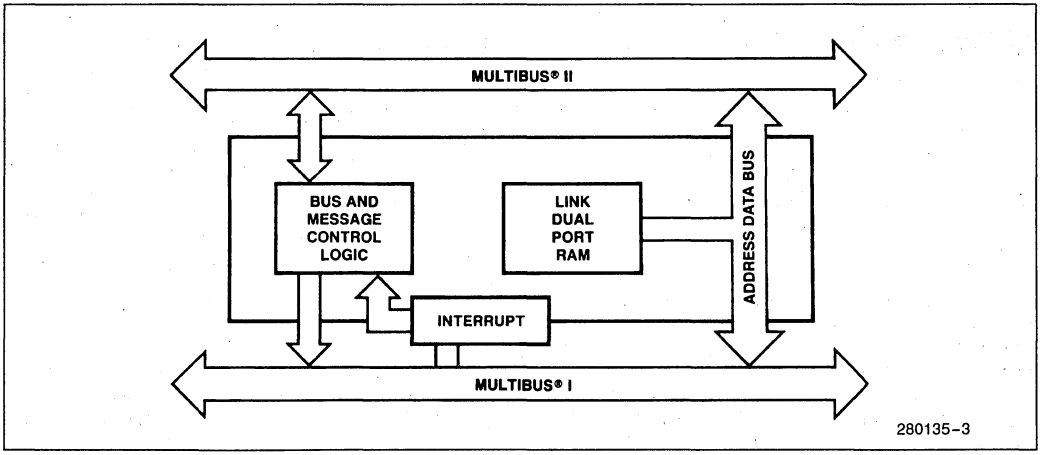


Figure 2. Link Board Dual Port Drawing

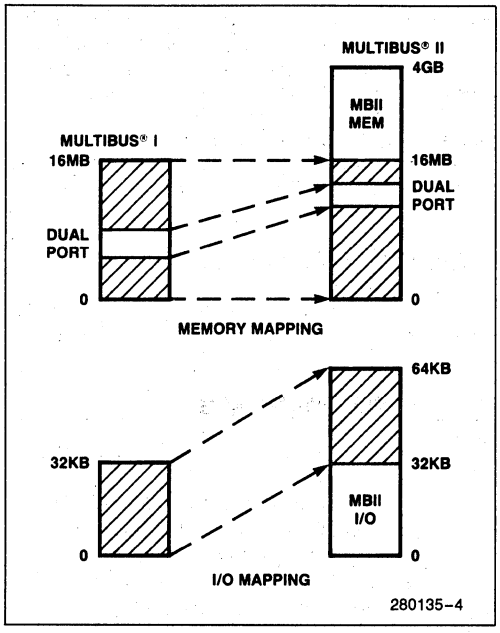


Figure 3. MULTIBUS® I Memory and I/O Mapping Diagram

(see Figure 3). MULTIBUS II I/O accesses must be from 32K Byte to 64K Byte in order to be mapped into MULTIBUS I I/O address space. These blocks are specified through an interconnect access to the "I/O 4K Segment Control" register (see Table 1). Each bit in the register represents a 4K Byte block of I/O addresses. When a bit (or bits) is set, the 4K Byte block of MULTIBUS II I/O space represented by that bit will be dedicated to MULTIBUS I I/O space.

Interrupt to Message Conversion

As the iSBC LNK/001 board receives non-bus vectored interrupts from the MULTIBUS I system, the on-board 8259A programmable interrupt controller (PIC) prioritizes the MULTIBUS I interrupts and initiates the MULTIBUS II unsolicited interrupt message generation process. Up to 8 levels of non-bus vectored interrupts are supported by the iSBC LNK/001 board.

The iSBC LNK/001 board generates the MULTIBUS II interrupt messages and is the Interrupt Source. The iSBC LNK/001 board is assigned a Source ID through interconnect space when the MULTIBUS II system is powered up or when the user programs the source ID register via interconnect space. The Interrupt Destination is the MULTIBUS II board to which the interrupt message is being sent. Each of the eight MULTIBUS I interrupt lines can be programmed to generate a unique MULTIBUS II destination address. These destination addresses are initialized through interconnect space by programming the iSBC LNK/001 Interrupt Destination Address Registers. The message source address is also configurable via interconnect space by writing to the Interrupt 0 Source Address Register with a base value. Once the base value of source Address 0 is established, Source Address 1 through 7 are set for incrementing values by the 8751A interconnect processor. The iSBC LNK/001 board recognizes MULTIBUS II Negative Acknowledge agent errors ("NACK") and performs an automatic retry algorithm.

Initialization Tests and BIST

Self test and diagnostics have been built into the MULTIBUS II system. The BIST LED is used to indicate the result of the Built-In-Self-Test and turns on when BIST starts running and turns off when it has successfully executed. BIST test failure information is recorded in the interconnect space and is accessible to software for error reporting.

PHYSICAL CHARACTERISTICS

Form Factor

The iSBC LNK/001 board is a MULTIBUS I form factor board residing in a MULTIBUS I system. Physical dimensions are identical to all standard MULTIBUS I boards.

Connection to MULTIBUS® II Bus

The iSBC LNK/001 board connects to the iSBC CSM/001 board in the MULTIBUS II system via a 60 pin conductor flat ribbon cable. The physical connection is made on the P2 connector of both the iSBC LNK/001 board and the iSBC CSM/001 board. The cable termination requirements and DC requirements for the signal drivers and receivers are detailed in the iSBC CSM/001 USERS GUIDE, Section 6.6.4. The maximum length of the cable is 3 feet. The cable and the connectors are shipped unassembled to allow user flexibility.

SOFTWARE SUPPORT

To take advantage of iSBC LNK/001 Dual Port architecture, existing software device drivers may require modification. Device driver changes depend on the specific application and vary in complexity depending upon the device driver.

SPECIFICATIONS

Word Size

16- and 24-bit Address Paths
8- and 16-bit Data Paths
Block transfers are not supported

Cable Characteristics

The cable is a 60 pin conductor flat ribbon cable with a maximum length of 3 feet. The P2 connector to the iSBC LNK/001 board is a 30/60 pin board edge connector with 0.100" pin centers, KEL-AM Part Number RF30-2853-5. The connector to the P2 DIN connector on the iSBC CSM/001 board is 3M Part Number 3338-000.

Interface Specifications

Location	Function
P1	MULTIBUS IEEE 796 System Bus
P2	Cable connection to P2 connector of iSBC CSM/001 board

PHYSICAL DIMENSIONS

The iSBC LNK/001 board meets all MULTIBUS I mechanical specifications as presented in the MULTIBUS I specification.

Depth: 17.15 cm (6.75 in.)
Height: 1.27 cm (0.50 in.)
Front Panel Width: 30.48 cm (12.00 in.)
Weight: Estimated 565 g (20 oz.)

ENVIRONMENTAL REQUIREMENTS

Temperature: Inlet air at 200 LFM airflow over boards
Non Operating: −40°C to +75°C
Operating: 0°C to +55°C

Humidity: Non Operating: 0 to 95% RH @ 55°C
Operating: 0 to 95% RH @ 55°C

POWER REQUIREMENTS

Voltage: +5V
Current: 7.14 Amps

REFERENCE MANUALS

iSBC LNK/001 Users Guide (#148756-001)

Intel MULTIBUS II Bus Architecture Specification, Rev C (#146077)

iSBC CSM/001 Users Manual (#146706-001)

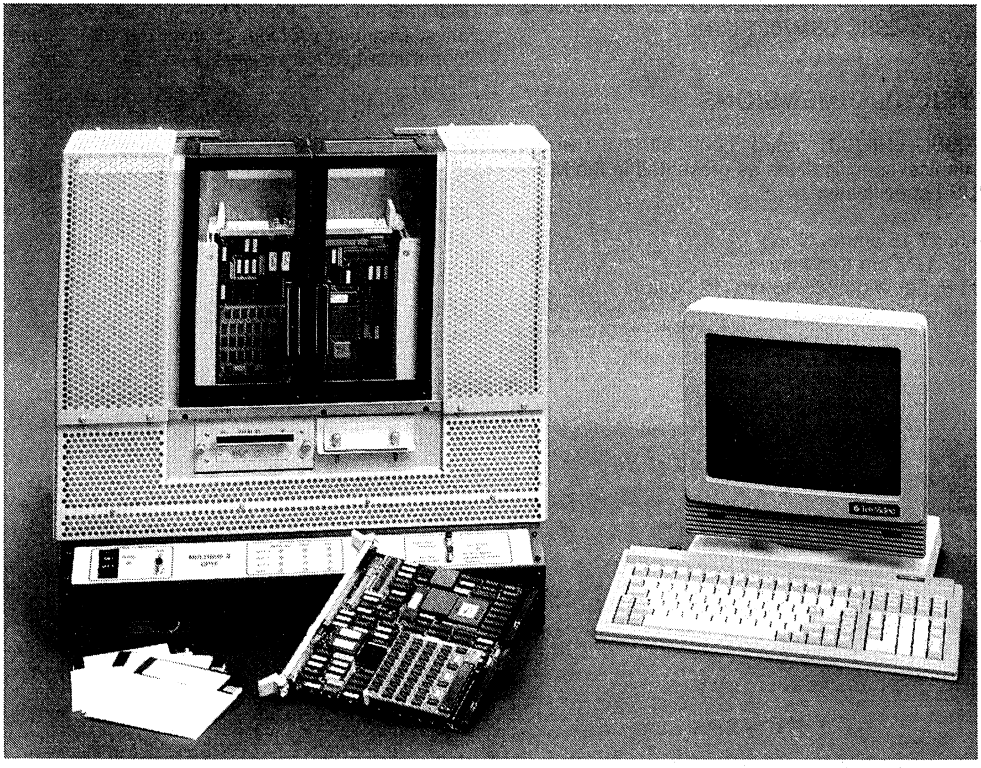
Manuals may be ordered from any Sales Representative, Distributor Office, or from the Intel Literature Department, 3065 Bowers Ave., Santa Clara, CA. 95051.

ORDERING INFORMATION

Part Number	Description
iSBC LKN/001	MULTIBUS II to MULTIBUS I iSBC LNK/001 Interface Board

MULTIBUS® II HIGH PERFORMANCE SBC GENERAL PURPOSE TEST FIXTURE (GPTF)

- Single Board Computer Tester for MULTIBUS® II Boards in a Systems Environment
- Tests up to Four MULTIBUS II Boards Simultaneously in a Range from Ambient Temperature to 70°C
  — Voltage and Temperature Margins are Software Controlled
- Multiprocessor, Multitesting Functional Tester with Totally Automated Test Sequence, Requiring Minimum Human Intervention
- Powerful Command Language for Troubleshooting and Evaluation
- One STBL (System Test Board Level) Test is Included. Additional Test Programs are Available for Intel MULTIBUS II Boards
- GPTF Includes Video Monitor for Error Message Display and Status of Testing, Also, a Comprehensive Installation Guide and Users Manual
- Bus Drawer Feature on P2 Connector Allows User Flexibility to Test Boards with Different Types of P2 Interfaces
- Available in Either USA, Japan or International Power Configuration
- Safety Features Including Thermal Cut Out at 90°C



280189-1

October 1988
Order Number: 280189-002

TESTER OVERVIEW

The MULTIBUS II General Purpose Test-Fixture (MULTIBUS II GPTF) is a state-of-the-art high performance tester used to test MULTIBUS II boards in a typical systems environment. The System Test Board Level or STBL, as it is usually referred to, is done using the MULTIBUS II GPTF. The STBL is used to validate that the iSBC board will perform in a system environment under a variety of temperature and voltage conditions. The MULTIBUS II GPTF is a fully automated tester with minimum operator intervention required. It can test from one to four boards of the same type at a time. A full range of keyboard commands are available for troubleshooting. The human interface is through the Front Panel and the CRT terminal. The MULTIBUS II GPTF requires the use of a Televideo 955 terminal which is included with the GPTF order.

The users manual is written at the operator's level and thus does not require a technician to perform tests. The users manual is written in two parts; operator's instructions and technician's troubleshooting section. An installation guide is also furnished.

The MULTIBUS II GPTF does not require any special Test EPROMs to do the STBL. The STBL can be loaded and stored in the hard drive using either the floppy drive or downloaded from an Intel Series III Development System. Once the STBLs are loaded into the hard drive, reconfiguration time (when testing different types of boards) is typically limited to exchanging the bus drawer. The STBLs for the most part use the Built-In Self Tests (BISTs) which are part of the MULTIBUS II Board Product Firmware, to test the Unit Under Test (UUT).

The MULTIBUS II GPTF adheres to MULTIBUS II architecture and follows the Intel Interconnect Interface Specification (IIS) and the Intel Initialization and Diagnostics eXecutive (IDX).

HARDWARE OVERVIEW

The MULTIBUS II GPTF is uniquely designed for ease of maintainability with three enclosures. The front enclosure is the heat chamber that houses the UUTs. Behind the heat chamber are the two computer systems; the Test Computer System and the Control Computer System. Each system has its own power supply.

The **Test Computer System**, which is MULTIBUS II based, is located immediately behind the heat chamber. It is the slave system to the Control Computer System. Its function is to perform the testing and report test status back to the Control Computer System. The Test Computer System contains three HOST MULTIBUS II boards which always reside in the GPTF.

The **Hot Box Test Chamber** has slots for testing one to four UUT's simultaneously. Both the +5V and temperature can be varied by the Control Computer (or the user) to test the boards in a worst case condition. The +5V voltage can be margined ±10%, and the temperature can be raised from room temperature to 70°C.

The **Control Computer System** is located in the rear of the GPTF and is a MULTIBUS I based system. Its function is to control and manage the Test Computer System. This system controls the AC power to the Test Computer System, has the capability to margin the DC voltages to the UUT, controls the heat chamber heater coils, reset and interrupt lines to the iSBC CSM/001 board, and controls the I/O to the CRT video display, front panel, and the secondary storage. The Control Computer contains an 8-slot MULTIBUS I backplane and five iSBC boards.

The secondary storage consists of a 3.5", 40 Mbyte winchester hard drive and a 5.25", 48 TPI floppy drive. Both iRMX86™ and PC-DOS™ format floppy diskettes can be used. The hard drive and the floppy drive are controlled by the Intel iSBC 214 Peripheral Controller board. Additional 3.5" and 5.25" Peripheral Controller board. Additional 3.5" and 5.25" peripheral bays are designed in for future Intel use.

Variable P2 Interface capability in the MULTIBUS II architecture allows for variable use of the P2 connector on iSBC boards. The iLBX™ II connector is used on some boards, like the iSBC 286/100 and the iSBC MEM/3XX boards, SCSI is used on boards like iSBC 386/258 etc. The MULTIBUS II GPTF has the bus drawer feature in the Test Computer System to support the variable P2 interface. Each bus drawer is designed for a specific P2 interface. For example, the CODE1 bus drawer, shipped with the GPTF, supports iLBX II. The bus drawers are easy to install—slide it in and tighten the two thumb screws. Only two types are shipped with the product. All the parts of the bus drawer are generic except the P2 connector itself. Each bus drawer is coded so that it can be recognized by the STBL software.

SOFTWARE OVERVIEW

The MULTIBUS II GPTF runs on iRMX 86 software specially configured for the GPTF. The operating system resides on the hard drive Control Computer System. The DIR command will assist in locating the various directories on the hard drive.

The Tester Control Program (TCP), also iRMX 86-based Operating System, resides on the hard drive and runs on the Control Computer System (iSBC

186/51 board). The TCP resembles a mini operating system. It supports a range of keyboard commands which are useful to run STBL and to troubleshoot suspect boards. A set of ten command strings can be stored in the STBL software and may be invoked at run time by the operator.

Using TCP commands, the operator can control the functions of the GPTF. TCP also responds to the front panel buttons, (START & QUIT) thus, making the GPTF automated. The CRT displays dedicated fields to indicate corresponding status of the testing such as: UUT board ID, UUT power supply status, voltage margin as percent of nominal voltage, and slot location of UUT.

The TCP operates in two modes, PRODUCTION TEST MODE (default) and TROUBLESHOOTING MODE. These modes allow the GPTF to be operated in a fully automated mode or a manually controlled mode. The PRODUCTION TEST MODE is turned off while troubleshooting with just a simple keyboard command.

The TCP works in conjunction with the firmware on the Host CPU board in the Test Computer System. The firmware is usually referred to as Host Firmware (HFW). Apart from communicating with the TCP, the HFW is an implementation of the Master Test Handler, as defined in the IDX. The Host firmware under the control of the TCP performs the testing of the UUTs.

The STBL can have tests of three different types. TYPE 1 tests run on the HOST only, TYPE 2 tests run on UUT only and TYPE 3 tests have both UUT and HOST code and can run on both. When testing more than one UUT, the TYPE 2 tests are executed in parallel by the UUTs. A given STBL can have any mixture of these three types of tests.

TESTER BLOCK DIAGRAM

Figure 1 shows a block diagram of the tester, in a level of detail sufficient to understand basic tester operation. The top of the sketch shows the MULTIBUS II system where testing takes place. On the left are the UUT slots, and on the right the host boards. Both iPSB and iLBX II busses are shown. The iLBX II backplane is physically installed in a removable bus drawer. Important communication paths shown are: a fast parallel path between host processor and control computer, and serial channels to the terminal and Series III development system. Details omitted for clarity include the heaters; most cabling; temperature sensors; +5B and heater relays.

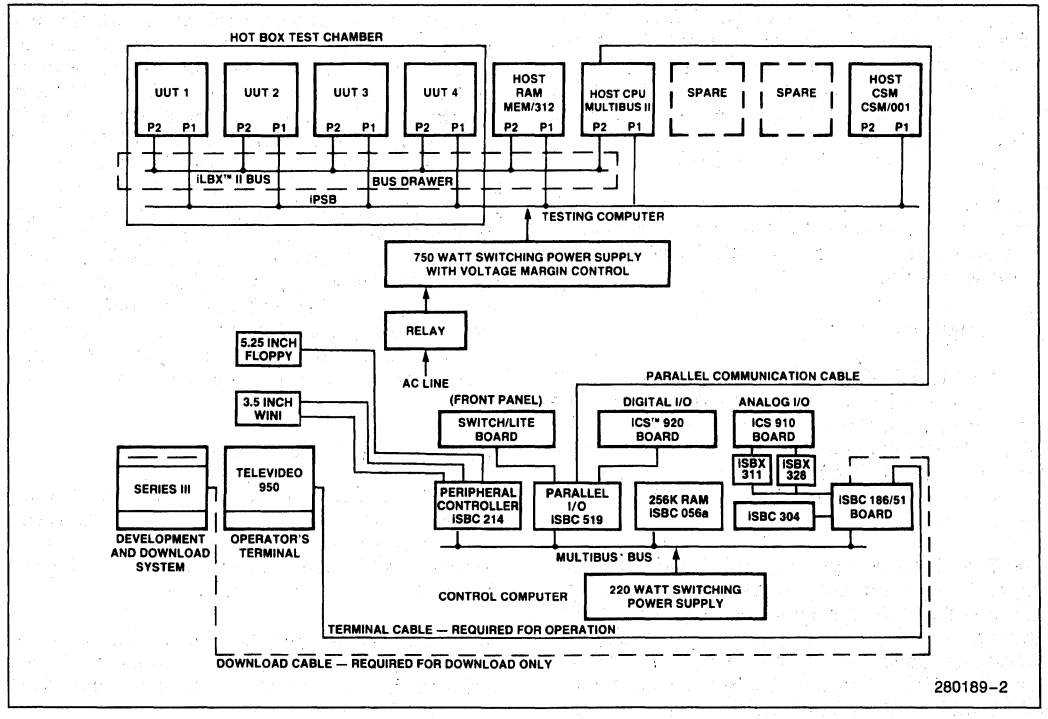


Figure 1. Tester Block Diagram

SPECIFICATIONS

Size: 25" W x 38" D x 24.5" H

Weight: 90 lbs.

Power Ratings	USA Units	International Units	Japan Units
Nominal Voltage Rating	110 volts	220 volts	100 volts
Current Rating	30 amperes	15 amperes	30 amperes
Frequency Rating	60 hertz	50 hertz	50/60 hertz

FUSE RATINGS

Power Ratings	USA/Japan	International
F1—Heater Coil 1 Fuse	10A @ 250V	5A @ 250V
F2—Heater Coil 2 Fuse	6A @ 250V	3A @ 250V
F3—MULTIBUS I Power Supply Fuse	7A @ 125V	4A @ 250V
F4—MULTIBUS II Power Supply Fuse	15A @ 250V	10A @ 250V

HEATER COIL RATINGS

Power Ratings	USA/Japan	International
Heater Coil 1	1000W 110V	1000W 220V
Heater Coil 2	660W 110V	660W 220V

Heater Coil 1 is to your right when you face the GPTF.

POWER SUPPLY RATINGS

Power Ratings	USA/Japan		International	
	*Input V	Output W	Input V	Output W
1. Control Computer System Power Supply	90–132V	220W	180–264V	220W
2. Test Computer System Power Supply	90–132V	750V	180–264V	750W

*"Input V" is the input voltage and the "Output W" is the output power.

POWER PLUGS

USA—The MULTIBUS II GPTF comes with a factory installed power plug which is a TWIST LOCK 30A, 125V PLUG.

INTERNATIONAL AND JAPAN—The MULTIBUS II GPTF is shipped WITHOUT a power plug because of the varied nature of the power outlets in other countries. CHOOSE A PLUG WHICH MEETS THE ELECTRICAL REQUIREMENTS OF THE TESTER. The GPTF is rated at 15A for INTERNATIONAL use and 30A for JAPAN.

The power outlet should be of proper rating. THIS APPLIES TO BOTH USA AND INTERNATIONAL UNITS. PLEASE USE THE FOLLOWING GUIDELINES:

INTERNATIONAL—A 15A drop with a receptacle of equivalent rating.

USA AND JAPAN—A 30A drop with a receptacle of equivalent rating.

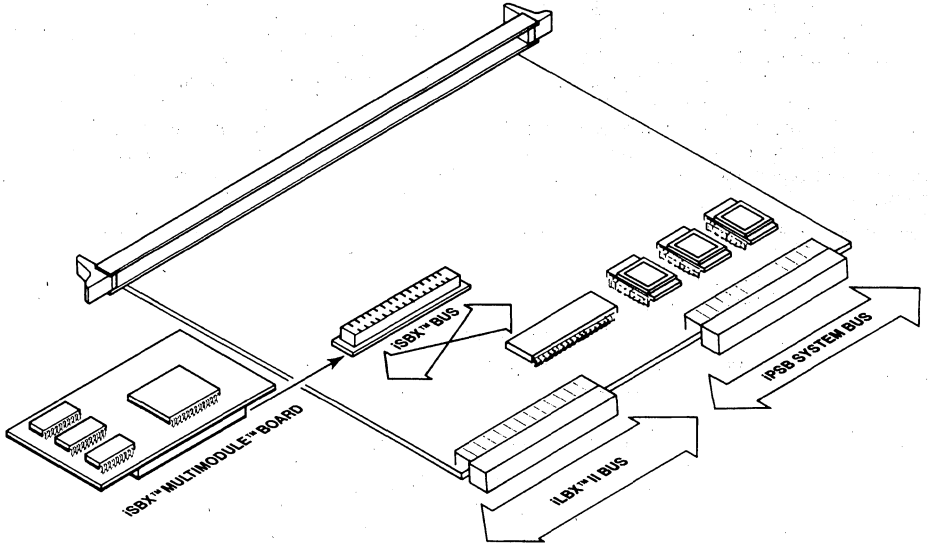
MULTIBUS® II Architecture

15

MULTIBUS® II
iPSB PARALLEL SYSTEM BUS

- **IEEE 1296 Industry Standard Bus**
- **Very High Bandwidth**
  - **— 40 Megabytes/Sec Using Burst Transfers**
  - **— 20 Megabytes/Sec with Single Cycles**
- **4 Gigabyte (32-bit) Addressing**
- **8-, 16-, 24-, and 32-bit Data Transfers over a 32-bit Path**
- **Pin-Efficient Multiplexed Structure**
- **Reliable Synchronous Clocking at 10 Megahertz with Full Handshaking for Data**
- **Distributed Arbitration with Up to 20 Bus Masters**
- **Full Parity Protection for Data Transfer Integrity**
- **Message Passing Facility for Intermodule Communication**
- **Geographic Addressing Facility for Software Indentification and Configuration of Boards**
- **Industry Standard Eurocard Form Factors—233 mm × 220 mm and 100 mm × 220 mm**

The MULTIBUS II iPSB Parallel System Bus is the foundation of the MULTIBUS II Bus Architecture. It is a general-purpose, processor independent structure which fully supports 8-, 16-, and 32-bit microprocessors. This very high bandwidth structure is defined on a single 96-pin IEC 603-2 (DIN) connector. All data movement functions required in a microcomputer system are defined including such advanced functions as an integrated message passing protocol and a geographic addressing facility which allows software to address a board by its slot position for software-based board identification and configuration.



280387-1

MULTIBUS® II Physical Diagram

September 1987
Order Number: 280387-002

FUNCTIONAL DESCRIPTION

Architectural Overview

The MULTIBUS II iPSB Parallel System Bus is the foundation of the MULTIBUS II bus architecture (see Figure 1). As a system bus, it is a very high bandwidth (40 megabytes/sec) bus optimized for intermodule communication; however, it also defines the complete set of basic bus functions required in a microcomputer system: memory accesses for execution of data, accesses to I/O for control of I/O functions, plus intermodule signalling. These basic functions are supplemented with additional functions supporting geographic (by slot) addressing and an integral message passing protocol.

Geographical addressing allows addressing of individual boards via their physical position in the backplane. Software can determine what boards are being used and configure itself appropriately. Software also can configure the hardware characteristics of the board (e.g., the starting address of a memory board). This can substantially reduce or even eliminate hardware jumper options and DIP switches for board configuration. Geographical addressing is a function of the interconnect address space.

MULTIBUS II's integral message passing protocol defines a standard and uniform way for modules to communicate over either the iPSB or iSSB buses. Integrating the protocol at the bus structure level lets the designer provide hardware support to increase system inter-module communication performance and opens the door for VLSI solutions. Standardizing the interface ensures a uniform software interface so that users can take advantage of new advances in technology without having to rewrite software.

Structural Features

OVERVIEW

The iPSB bus structure is a processor-independent general-purpose bus designed to support 8-, 16-, and 32-bit processors. It is designed to operate at a maximum bandwidth of 40 megabytes/sec while using off-the-shelf components.

Special attention has been given to how the bus structure, both electrically and mechanically, impacts system reliability. Synchronous sampling of all bus signal lines assures good immunity from crosstalk and noise. Full byte parity generation and checking protects all transfers on the bus to ensure that any bus error is detected. Signal quality on the bus is excellent due to the large number of interlaced ground lines. Mechanically, the iPSB bus is defined on a two-piece 96-pin IEC 603-2 connector to ensure good connector reliability.

MULTIPLEXING

The iPSB bus is highly multiplexed. The 32-bit address and data paths are multiplexed and the eight system control lines have different uses depending upon the phase of the transfer cycle. The six arbitration lines also serve dual purposes between system initialization and normal operation.

This multiplexed structure has several benefits. The entire 32-bit iPSB bus is defined on a single connector. This allows a full 32-bit iPSB bus interface on even the smaller, single connector, form factor board and opens the possibility of low cost 32-bit systems. Multiplexing also reduces by half the number of high current drivers required for the interface

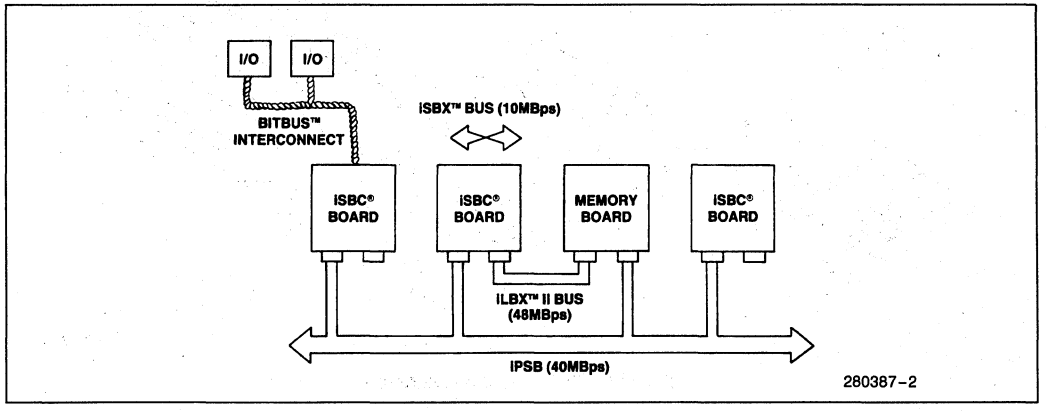


Figure 1. MULTIBUS® II Bus Architecture

which significantly reduces a board's current requirements. The routing of signal lines between the bus interface and connector is simplified.

ERRORS

The iPSB bus defines a complete set of bus error reporting mechanisms. Serious errors, such as a parity error or the failure of a module to complete the data handshake, are flagged on unique bus signal lines and are seen by all modules on the bus. These errors induce a recovery time in which the bus is allowed to stabilize before further transfer cycles may begin.

The iPSB bus also provides mechanisms for signaling less serious operational errors. Operational errors, such as attempting to perform a 32-bit access to a 8-bit device or writing to read-only memory, are signaled as agent errors. These errors may induce retry operations by an intelligent bus interface or may be passed to the on-board processor as errors.

INTERCONNECT ADDRESS SPACE

The ability to address a board by its physical position in the backplane is also supported in the iPSB bus. This facility allows board manufacturers to code such items as their vendor number, board type, board revision number, and serial number on the board. This information is available to the system software. This facility is defined in the iPSB bus interconnet address space.

Aside from this read-only information, the interconnect space allows write operations to support board configuration and diagnostics under software control. This facility can help reduce or eliminate hardware-based jumper options and DIP switches.

INTERRUPTS

The iPSB bus supports up to 255 distinct interrupt sources and 255 interrupt destinations. Rather than the user of the traditional method of dedicated interrupt signal lines on the bus, the iPSB bus defines a special bus cycle to convey interrupt information. This special bus cycle (actually part of the message passing protocol discussed below) redefines the meaning of the address; instead of a byte location in memory for example, 16 of the 32 lines encode 8 bits for the source module generating the interrupt and 8 bits for the destination module to service the interrupt.

This technique overcomes the significant problem of interrupt configuration found in traditional buses. Dedicated lines usually imply that only one particular destination can service one particular interrupt source. If an interrupt source wishes to target some interrupts to one destination and some to a different destination, separate bus interrupt lines are required for each destination. This can quickly consume all dedicated interrupt lines in even a moderate size system.

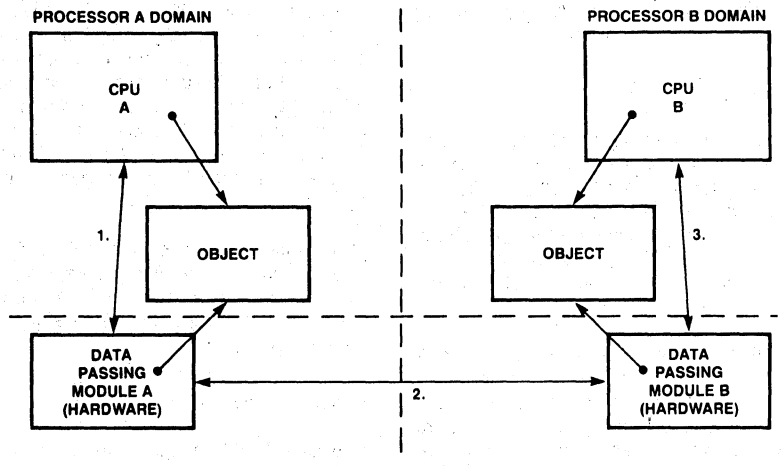
Using interrupt bus cycles with embedded source and destination module addressing removes the need for dedicated interrupt lines at the same time it allows any interrupt source to signal any interrupt destination.

MESSAGE PASSING

With the trend in microcomputer systems toward multiprocessing, it is important to provide the facilities and mechanisms to lend support for inter-module communication. The iPSB bus includes such mechanisms and defines the protocol for greatly enhanced performance in inter-module communication. This protocol is called MULTIBUS II Message Passing.

Most multiprocessor systems use either a "pass by reference" or a "pass by value" protocol for inter-module communication. In the "pass by reference" case, the two modules share a common memory resource and pass pointers or tokens to extend addressability of a desired data structure to the other module. In "pass by value", the modules exchange a copy of the desired data structure. Each of these protocols has a set of advantages and disadvantages associated with performance, data security, extendability to additional modules, and ease of use.

MULTIBUS II Message Passing takes the best of both methods and lends hardware support. Message passing uses a hardware "pass by value" interface that gives the performance of a "pass by reference" system. It replaces the software module used by the "pass by value" method with a specialized message passing interface. The processor "passes by reference" the reference to the data structure to the message passing co-processor interface. This interface communicates with the destination module's message passing interface to transfer the data without processor intervention. This data transfer is performed in the message address space. This is illustrated in Figure 2. (In many ways, it is helpful to think of the two communication message passing interfaces as a distributed, smart, DMA controller.)



NOTES:
1. CPU A Requests Transfer of Object (Pass by Reference).
2. Data Movement is Negotiated; Data Movement is Independent of Either Processor.
3. Processor B Assigns Memory for Object and is Signaled of Object Availability.

Figure 2. MULTIBUS® II Message Passing

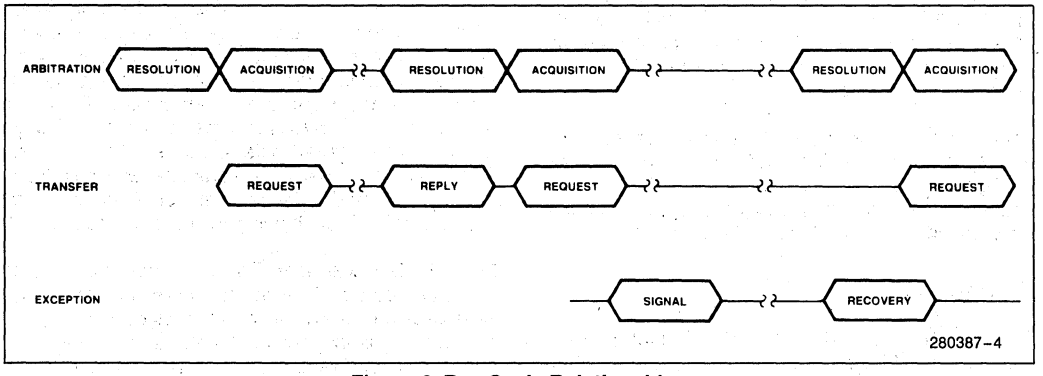


Figure 3. Bus Cycle Relationships

There are several significant benefits to this approach. First of all, the message passing interfaces can take advantage of the full capabilities of the bus (i.e., 32-bit data and burst transfer) independent of the type or nature of the controlling processor. Even 8-bit processor or I/O boards can take full advantage of the bus. This means significantly higher inter-module communication performance over a completely software-base method. Another benefit is the elimination of any shared memory. Dual-ported memory structures are no longer needed nor are global memory boards. The other primary benefit is that MULTIBUS II message passing presents a uniform software interface for all modules. Modules can be replaced with new modules containing newer technology (e.g., moving from a single density to a double density disk controller) without any software changes required in the controlling module. This makes it easy for users to integrate new technology without the problem of completely rewriting the driver software.

CENTRAL SERVICES MODULE

The iPSB bus specification defines the central system functions as the Central Services Module (CSM). The minimal set of functions are: clock generation, power-down and reset, time-out, and assignment of slot IDs. Collecting these functions in a single module improves overall board area utilization, since the functions are not duplicated on every board and then only used on one. The system designer is free to implement the CSM on a separate board or to include the functions as just one of several modules on another board.

Bus Cycle Overview

The iPSB bus defines three types of bus cycles: arbitration, transfer, and exception cycles. Each cycle is made up of one or more phases. Figure 3 illustrates the relationship among these cycles and phases.

ARBITRATION CYCLE

The arbitration cycle is made up of a resolution phase and an acquisition phase. The resolution phase is the time-period in which all requesting agents collectively arbitrate for access rights to the bus. Depending on the arbitration algorithm, the agents decide among themselves which of them is going to control the bus after the current bus owner is done. This arbitration method is referred to as self-selecting since the agents decide ownership among themselves.

The agent that wins the arbitration and obtains access rights to the bus begins the acquisition phase; that agent becomes the bus owner. This agent begins its transfer cycle and holds the arbitration logic in the resolution phase (resolving for the next access rights) until the transfer cycle is completed.

TRANSFER CYCLE

Starting the transfer cycle is the request phase. In this phase, the bus owner (requesting agent) places address and command information on the bus. This information defines the replying agent(s), the type of operation, and the type of address space. The request phase lasts one bus clock cycle.

The reply phase starts immediately after the request phase, during this phase, the requesting and replying agents engage in a handshake that synchronizes the data transfer sequence. The reply phase can contain one or more data cycles. The final data transfer is signaled by the requesting agent. During this final transfer, the requesting agent releases ownership of the bus allowing the new bus owner to use the bus immediately. Note how the transfer cycle overlaps the resolution phase of the arbitration cycle to minimize bus dead time.

EXCEPTION CYCLE

If an agent detects an error during a transfer cycle, it immediately begins an exception cycle. The exception cycle terminates any arbitration cycles and transfer cycles in progress. The exception cycle starts with the signal phase in which the detecting agent activates one of the exception lines. This notifies all agents of the problem causing them to terminate any arbitration or transfer cycles. Next the recovery phase begins. During this phase, all agents idle; this allows the bus a fixed amount of idle-time to stabilize before resuming normal operation.

Signal Groups

OVERVIEW

The iPSB bus contains five groups of signals, Figure 4, over which the requesting and replying agents can enact the protocol. An asterisk following the signal name indicates that the particular signal or group of signals are active when at their electrical low.

ARBITRATION GROUP

The arbitration signals on the iPSB bus determine which agent gains exclusive access to the bus (which agent is the bus owner). All requesting agents that require access to the bus resources must arbitrate for use of the bus. On being granted bus ownership, an agent begins using the address/data lines to perform a transfer cycle. There are seven signals in the arbitration group: BREQ* and ARB5* through ARB0*.

BREQ* (Bus Request) is an OR-tied signal which is bused on the backplane. All agents that require access to the bus assert the BREQ* signal.

A particular agent's arbitration ID number is coded on lines **ARB4* through ARB0*** (Arbitration). An agent requiring use of the iPSB bus asserts BREQ* and drives its arbitration ID onto the OR-tied ARB lines. The ARB5* line selects one of two arbitration algorithms: fairness or high priority.

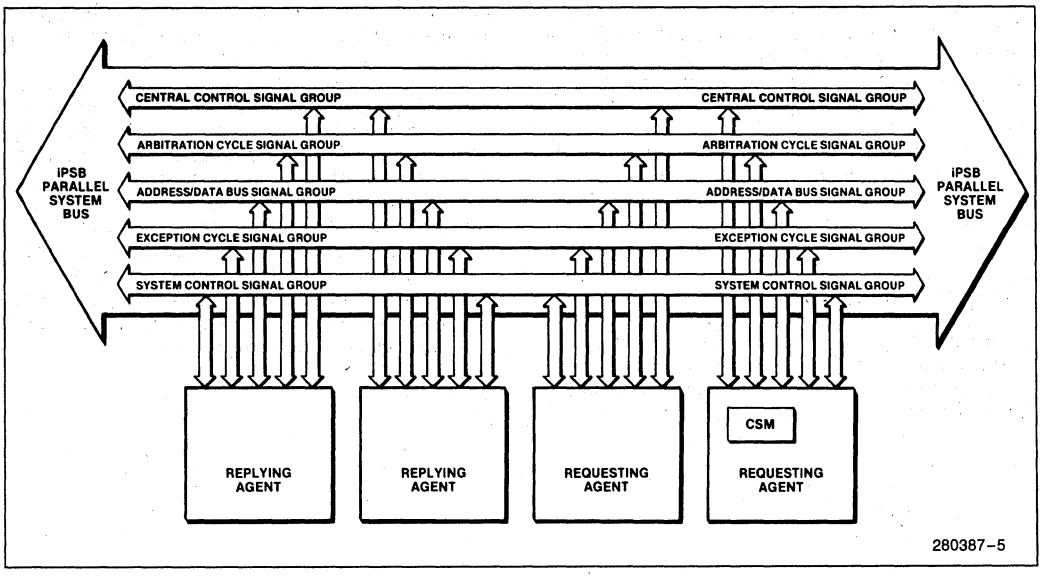


Figure 4. iPSB Bus Signal Groups

Table 1. System Control Definition

Signal	Function	
	Request Phase	Reply Phase
SC0	Request Phase	Request Phase
SC1	Lock	Lock
SC2	Data Width 0	End-of-Cycle
SC3	Data Width 1	Requesting Agent Ready
SC4	Address Space 0	Replying Agent Ready
SC5	Address Space 1	Agent Error 0
SC6	Read/Write	Agent Error 1
SC7	Reserved	Agent Error 2
SC8	Parity (SC7–4)	Parity (SC7–4)
SC9	Parity (SC3–0)	Parity (SC3–0)

ADDRESS/DATA BUS GROUP

This signal group contains the lines used to transfer the address and data information plus their respective byte parity lines. The **AD31* through AD0*** (Address/Data) lines are multiplexed and serve a dual purpose depending upon the phase of the transfer cycle.

During the request phase, they contain the address for the ensuing transfer. This address refers to the byte location for memory and I/O spaces, a processing agent module in message space, and a board slot location in interconnect space. The requesting agent drives these lines during the request phase.

During the reply phase, they contain either eight, sixteen, twenty-four, or thirty-two bits of data. They are driven by the requesting agent for write transfers and by the replying agent for read transfers.

The **PAR3* through PAR0*** (Parity) lines are the byte parity lines associated with the respective bytes of the AD lines. They form even parity with their respective address/data byte.

SYSTEM CONTROL SIGNAL

The transfer signal group consists of ten signals, SC9* through SC0((System Control). Agents use these signals to define commands or to report status, depending on the phase of the transfer cycle.

During the request phase, the requesting agent drives SC9* through SC0*. The SC lines provide command information to the replying agent(s). During the reply phase, the requesting agent drives SC9* and SC3* through SC0* with its handshake and additional control information. The replying agent drives the remainder with its handshake and status. Table 1 lists the request and reply phase functions for this group.

EXCEPTION SIGNAL GROUP

The iPBS bus provides a group of two signals for passing indications of exception errors to all agents: **BUSERR*** (Bus Error), and **TIMOUT*** (Time-out).

An agent activates BUSERR* to indicate its detection of a data integrity problem during a transfer. Parity errors on the AD or SC lines are typical of errors signaled on BUSERR. Any agent detecting such errors must signal BUSERR* and all agents must receive BUSERR*.

TIMOUT* is signaled by the CSM whenever it detects the failure of a module to complete a handshake. TIMOUT* is received by all agents on the bus.

CENTRAL CONTROL GROUP

The system control group provides status concerning the operating state of the entire iPSB bus environment. It consists of seven signals plus the power and ground lines.

The **RST*** (Reset) signal is a system-level initialization signal sent to all agents by the CSM.

The **RSTNC*** (Reset Not Complete) signal is an OR-tied line driven by any agent whose internal initialization sequence is longer than that provided by the RST* signal itself. Due to its OR-tying, RSTNC* remains active until every agent has completed its initialization sequence. Agents cannot perform bus transfer cycles until RSTNC* is inactive.

The CSM provides a **DCLOW** (DC Power Low) signal to all agents as a warning of an imminent loss of DC power. DCLOW is typically generated from a signal supplied by the system power supply on the loss of AC power. Any agent needing to preserve state

information in battery backed-up resources should do so upon receiving an active DCLOW.

Accompanying DCLOW for power-down sequencing is the **PROT*** (Protect) signal. The CSM drives PROT* active a short time after it activates DCLOW to inform all bus interfaces to ignore any transitions on the bus as power is lost.

The **BCLK*** (Bus Clock) and **CCLK*** (Constant Clock) signals are supplied by the CSM to all agents. Agents use the BCLK to drive the arbitration and timing state machines on the iPSB bus. The active going edge of BCLK* provides all system timing references. The CCLK* is an auxiliary clock at twice the frequency of BCLK.

An agent user its **LACHn*** (ID Latch) signal to save the slot ID it receives from the CSM at reset time via the ARB4* through ARB0* lines. The ID latch signal is called LACHn* where the "n" is the card slot to which the ID is assigned. At each card slot, the LACHn* signal is connected to the AD line of the same number. As an example, card slot 7 has a LACH7* signal that is connected to AD7*.

When RST* is active, the CSM sends successive slot ID's (0 through 19) on the ARB4* through ARB0* lines while activating the corresponding AD line. Agents know when the ARB lines contain the correct slot number when they see their LACHn* line go active.

POWER

System power supplied in the iPSB connector includes +5 volts, +12 volts, −12 volts, and facilities for +5 volt battery back-up. Also defined are numerous ground lines some of which are interlaced throughout the connector.

iPSB Bus Protocol

OVERVIEW

In the MULTIBUS II specification, both timing diagrams and state-flow diagrams describe the iPSB bus protocol. The state-flow diagrams present the lowest-level and most rigorous definition while the timing diagrams help conceptual understanding. For the purposes of this data book, only the timing diagram description is used.

ARBITRATION CYCLE

An agent that wishes to transfer data on the iPSB bus must begin by performing an arbitration cycle. The cycle performs two functions: first, it gives all agents the opportunity to be granted access to the bus, and second, it eliminates the possibility of more than one agent trying to transfer data on the bus at any one instant. In the case where more than one agent requests access to the bus at the same instant, the arbitration cycle grants access to the agents based upon one of two arbitration algorithms: normal or high priority.

Normal priority mode provides "fairness" or "no starvation", which means each agent has an equal opportunity to grant access to the bus. For example, assume all agents request the bus at the same instant. In the normal priority mode, each agent is granted the bus, one by one, until all requests have been serviced. If an already serviced agent desires to use the bus again before all of the original agents are serviced, it will wait until all of original requesting agents have their request granted. This "round-robin" granting of access ensures that any agent requesting the bus will eventually get it.

The high priority mode allows an agent with high priority to force its way into the arbitration and be granted the bus before agents with lesser priority. This means that a high priority agent gets access to the bus quickly; however, it can also consume so much of the bus that agents with less priority never gain access; they will "starve".

At reset, the CSM supplies each agent with its slot ID and its arbitration ID. An agent making a normal priority request activates BREQ*, holds ARB5* inactive, and drives its arbitration ID onto ARB4* through ARB0*. If the ARB lines hold its ID after a specified time (3 bus clocks), this agent won the arbitration and can use the bus once any ongoing transfer completes. However, if the ARB lines do not match its ID (after all, other agents might be also requesting the bus and driving the ARB lines), another agent won the arbitration. The losing agent removes its ID and waits for the next resolution phase before trying again.

An agent makes a high priority request by activating BREQ*, holding ARB5* active (ARB5* selects the arbitration mode), and driving its arbitration ID onto the ARB lines. The high priority algorithm requires that when a high priority request enters during an arbitration cycle, the request immediately enters the next resolution phase rather than waiting for the next bus request cycle as do normal priority requests. ARB5* being active causes the other requesting agents to remove their requests guaranteeing the high priority agent access to the bus before any simultaneous normal priority requests. When more than one agent simultaneously makes a high priority request, the agent with the higher priority (lower numerical value) arbitration ID will go first. Figure 5 illustrates the logic required to implement the iPSB bus arbitration. With either priority mode, once an agent owns the bus, it can perform any number of transfer cycles until force off by arbitration. This characteristic of the arbitration algorithms is called "bus parking".

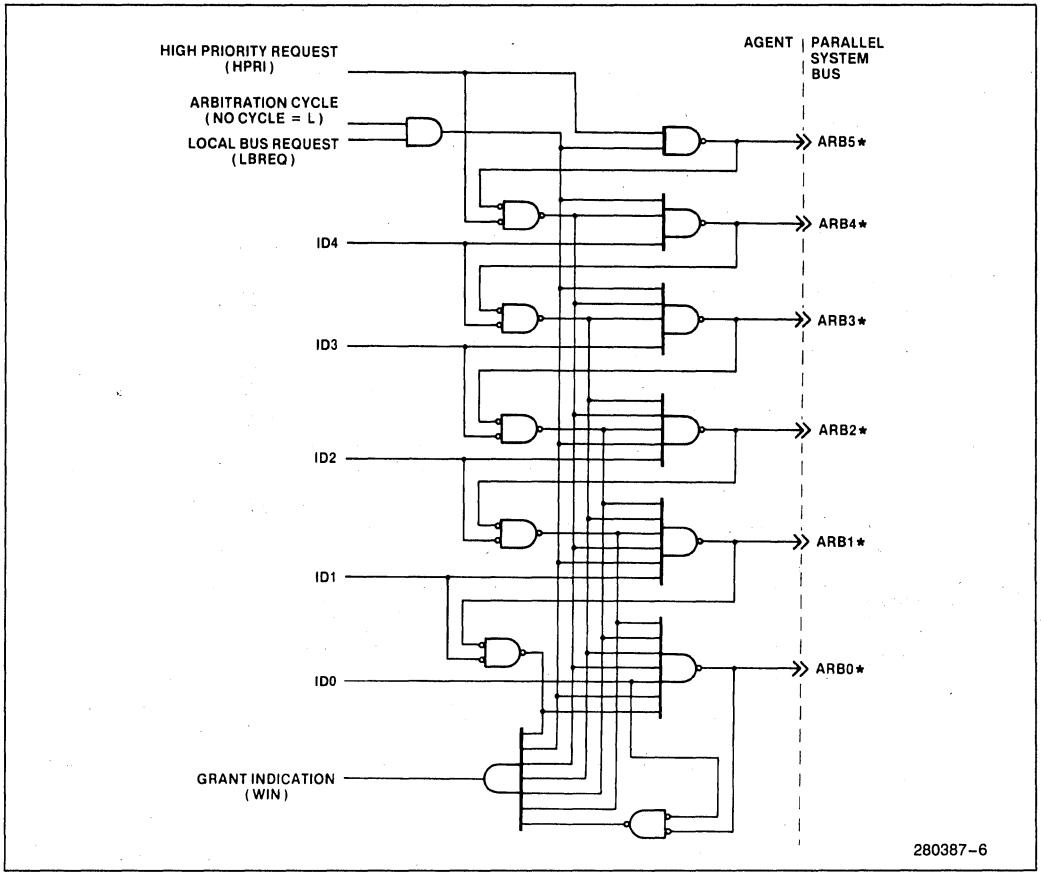


Figure 5. iPSB Bus Arbitration Cycle

TRANSFER CYCLE

Transfer cycles consist of two phases: request and reply. For illustration, an example of an access read cycle is shown in Figure 6. During the request phase, the bus owner (requesting agent) uses the transfer cycle signal group (SC lines) to notify the replying agent of the address space (memory, I/O, interconnect, or message), the data width (8-, 16-, 24- or 32-bit), and whether the cycle is read or write. The AD lines contain the desired address for the selected address space. Replying agents know the SC lines contain this request information by the requesting agent activating SC0* (Request Phase). The request phase lasts one clock cycle. All potential replying agents use the request phase to determine whether they contain the addressed resource.

The reply phase starts immediately following the request phase. During this phase the agent with the addressed resource (replying agent) and the requesting agent exchange data and status. Both the requesting and replying agent must agree that the data on the AD lines and the status on the appropriate SC lines are valid via the RQRDY (Requesting agent read—SC3*) and RPRDY (Replying agent read— SC4*) handshake lines. Either agent can

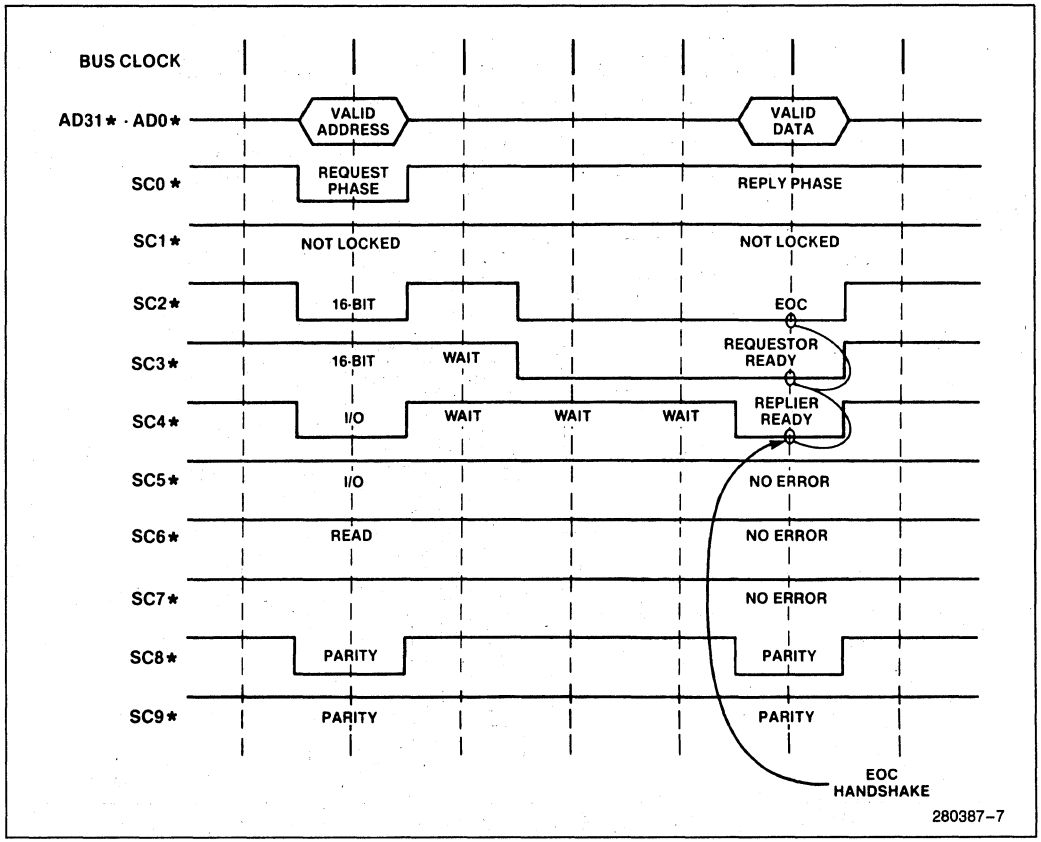


Figure 6. Transfer Cycle Example

hold off the transfer by deactivating its ready line. This handshaking supports any speed requesting or replying agent.

The transfer cycle is complete when the requesting agent signals the last data transfer via the End-Of-Cycle (EOC—SC2*). The last bus clock cycle of the transfer is when EOC, RQRDY, and RPRDY are all active simultaneously.

The replying agent has the opportunity to tell the requesting agent if it does not support the requested operation via the agent error (SC5*, SC6*, and SC7*) lines. These lines encode five types of errors: width violation, continuation error, data error, illegal operation, and negative acknowledgement of a message. Trying to extract 32-bits of data from an 8-bit peripheral is an example of a data width violation. Continuation errors occur when attempting sequential access from an agent which does not support them or running off the ending address of a memory board. Writing to a read-only memory is an example of an illegal operation. A parity or ECC error in a memory board is an example of a data error. A replying agent signals a negative acknowledgement to a message transfer cycle if its destination queue is full (the source most perform source queuing). The transfer cycle is terminated by the requesting agent when it detects that the replier is signalling an agent error. If the bus interface is intelligent, it might retry the operation with a different type that the replying agent can support. Other aspects of transfer cycle include the ability of a requesting agent to LOCK the bus via the SC1* line. SC1* is a non-multiplexed signal which inhibits alternate ports of any multi-ported resource being addressed. By locking the bus, the requesting agent can guarantee itself exclusive access to a multi-ported bus resource and retains bus ownership for more than one transfer cycle.

As noted in the figure, in addition to parity protection on the address/data lines, the SC lines are also protected by parity. The requesting agent is responsible for the SC parity bits (SC8* and SC9*) during the request phase (it drives all SC lines). The reply phase requires two parity bits: one for those lines driven by the requesting agent and one for those driven by the replier. This ensures all aspects of the transfer cycle have parity protection.

EXCEPTION CYCLE

The exception cycle is an error reporting mechanism. An agent or the CSM initiates an exception cycle as a result of sensing an exception. If no exception occurs, no exception cycles occur.

The exception cycle has two purposes in the protocol: first, it provides systematic termination of activity on the iPSB bus and second, it provides a stabilization time before allowing agents to resume operation. These two purposes correspond directly to the two phases of the exception cycle: the signal and recovery phases.

The signal phase begins when an agent or a module senses an exception and activates one of the bus error lines. One receiving a bus error, all agents terminate any transfer or arbitration cycles in progress. The net effect of the signal phase is to terminate all bus activity. The signal phase continues until the error-detecting module deactivates the bus error line.

The recovery phase begins after the bus error line becomes inactive. The recovery phase is a fixed-duration delay (in terms of bus clock cycles) that allows time for the iPSB bus signals to settle before starting more transfer cycles.

There are two types of bus exceptions supported by the iPSB bus: timeout and bus error. The CSM monitors the bus to ensure that all data handshakes complete. If for some reason the handshake hangs and exceeds a maximum time limit, the CSM activates the TIMOUT* (Time Out) bus exception line to begin the exception cycle.

An agent sends a bus error exception whenever it determines that the information on the address/data (AD) or the transfer control (SC) lines is in error. Once an error is detected, the agent activates the BUSERR* (Bus Error) signal line to begin the exception cycle.

Mechanical

The MULTIBUS II boards, board accessories, and backplanes conform to mechanical standards defined by the International Electromechanical Commission (IEC); these standards are commonly referred to as the Eurocard mechanical standards. This mechanical system offers modular board sizes as defined in standard IEC-297-3 and reliable two-piece connectors as defined in IEC-603-2.

FORM FACTOR

The MULTIBUS II specification calls out two modular board form factors: 233 × 220 mm and 100 × 200 mm (see Figure 7). The iPSB bus and iLBX II bus portions of the MULTIBUS II system architecture are always defined on the P1 and P2 connectors respectively. However, the user can optionally define the use of the P2 connector if the iLBX II bus is not supported. (The iSSB bus is additionally defined on the P1 connector.)

Connector

MULTIBUS II boards and backplanes use two-piece, 96-pin connectors for both the iPSB bus and iLBX II bus. The right-angle connectors on the printed board are IEC standard 603-2-IEC-C096-M; the receptacle connectors on the backplane are IEC standard 6-03-2-IEC-C096-F (Figure 8). This connector family is noted for its reliability, availability, and low cost.

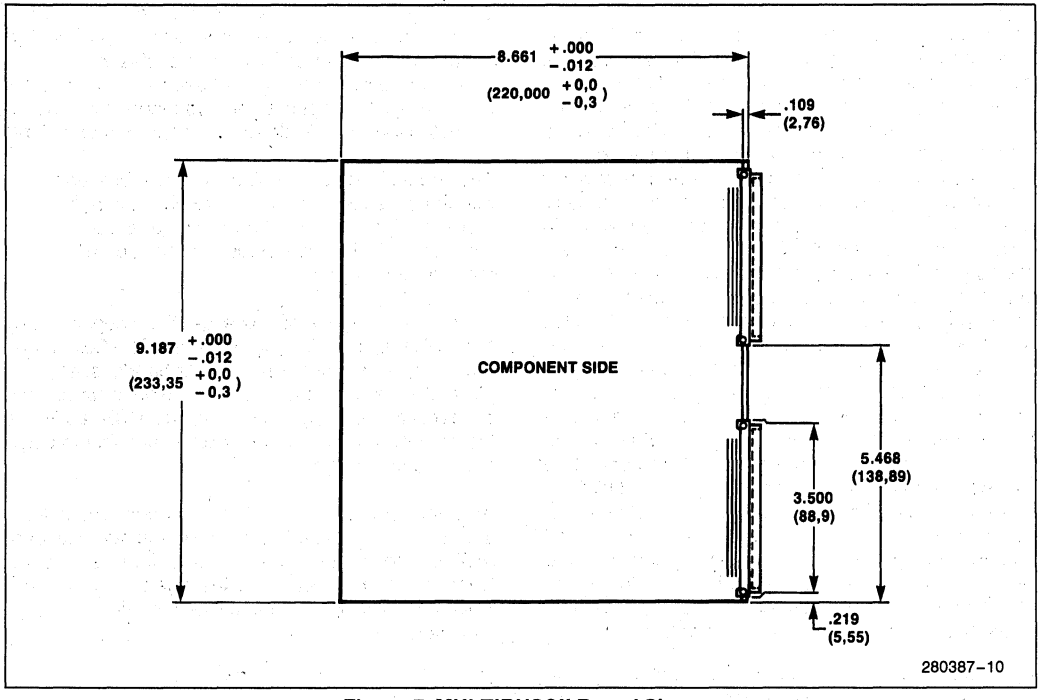


Figure 7. MULTIBUS®II Board Sizes

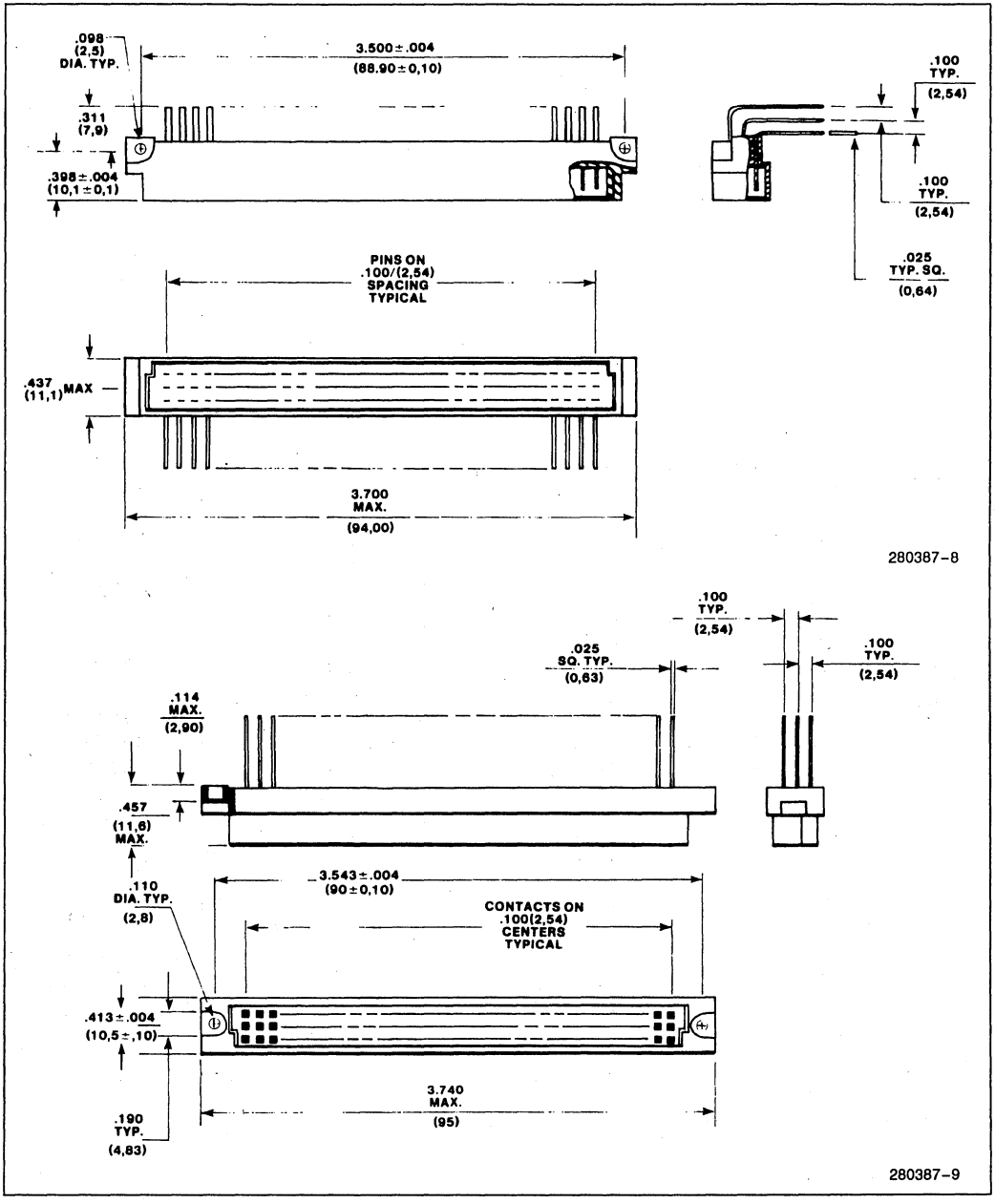


Figure 8. MULTIBUS®II Connectors

The pin assignment for the iPSB bus on P1 is shown in Table 2.

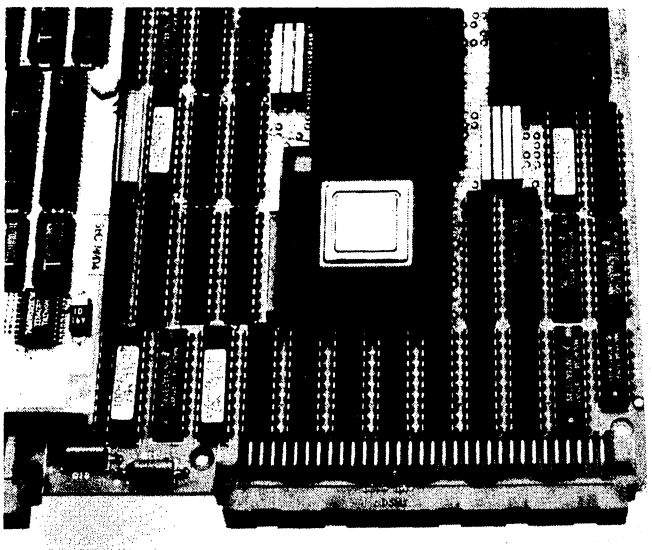
Please refer to Intel's MULTIBUS II Bus Architecture Specification Handbook for more detailed information.

Table 2. iPSB Bus Pin Assignments

Connector Pin Number	Row A	Row B	Row C
1	0 Volts	PROT*	0 Volts
2	+5 Volts	DCLOW*	+5 Volts
3	+12 Volts	+5 Battery	+12 Volts
4	(Note 2)	SDA (Note 3)	BCLK*
5	TIMOUT*	SDB (Note 3)	0 Volts
6	(Note 1) LACHn	0 Volts	CCLK*
7	AD0*	AD1*	0 Volts
8	AD2*	0 Volts	AD3*
9	AD4*	AD5*	AD6*
10	AD7*	+5 Volts	PAR0*
11	AD8*	AD9*	AD10*
12	AD11*	+5 Volts	AD12*
13	AD13*	AD14*	AD15*
14	PAR1*	0 Volts	AD16*
15	AD17*	AD18*	AD19*
16	AD20*	0 Volts	AD21*
17	AD22*	AD23*	PAR02*
18	AD24*	0 Volts	AD25*
19	AD26*	AD27*	AD28*
20	AD29*	0 Volts	AD30*
21	AD31*	Reserved	PAR3*
22	+5 Volts	+5 Volts	Reserved
23	BUSREQ*	RST*	BUSERR*
24	ARB5*	+5 Volts	ARB4*
25	ARB3*	RSTNC*	ARB2*
26	ARB1*	0 Volts	ARB0*
27	SC9*	SC8*	SC7*
28	SC6*	0 Volts	SC5*
29	SC4*	SC3*	SC2*
30	−12 Volts	+5 Battery	−12 Volts
31	+5 Volts	SC1*	+5 Volts
32	0 Volts	SC0*	0 Volts

NOTES:
1. LACHn* for all agents but the one driving CCLK*; line contains a second CCLK* signal in systems that have more than 12 cardslots.
2. 0 Volts for all agents but the one driving BCLK*; line contains a second BCLK* signal in systems that have more than 12 cardslots.
3. Signal lines SDA and SDB are reserved for the Serial System Bus.

MULTIBUS®II MESSAGE PASSING COPROCESSOR—82389



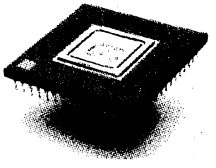
THE SINGLE CHIP INTERFACE FOR MULTIBUS II BOARDS

The MULTIBUS II Message Passing Coprocessor (MPC) is a highly integrated CMOS device implementing the full message passing protocol as well as arbitration, transfer and exception cycle protocols of the Parallel System Bus (PSB) interface as defined in the IEEE/ANSI 1296 MULTIBUS II specification.

The Message Passing Coprocessor gives designers a single chip bus interface which substantially simplifies board and system design. Using the MPC increases overall system performance by allowing both the Parallel System Bus and the local on-board bus to operate at maximum speeds.

FEATURES

- The single chip interface to the MULTIBUS II Parallel System Bus of the IEEE/ANSI 1296 specification
- Implements complete message passing capabilities
- Offloads the CPU from managing bus arbitration, transfer and exception cycles
- Maximizes performance on Parallel System Bus and local on-board bus
- Processor independent
- Supports Central Services Module capabilities



The MPC comes in a 149-pin PGA package.

intel

September, 1988
Order Number: 280677-001

FEATURES

COMPLIANCE TO STANDARDS

The Message Passing Coprocessor is the single chip interface to the Parallel System Bus of the IEEE/ANSI 1296 specification. By complying to an industry standard bus specification, users are assured of stability of design and interoperability of all MULTIBUS II products using the Message Passing Coprocessor.

THE LEADER IN MESSAGE PASSING

The message address space in MULTIBUS II is defined for high performance standardized communication of multiple processor systems. The Message Passing Coprocessor, by decoupling the local on-board bus activities from the Parallel System Bus activities, eliminates an interface bottleneck present in the tight coupling of dual port architectures. The freedom in not waiting for arbitration cycles and allowing each transfer to occur at the full bandwidth of the individual buses, substantially increases overall system performance.

COMPLETE FUNCTIONAL INTERFACE

The Message Passing Coprocessor offloads the CPU from managing bus arbitration, transfer and exception cycles required in interfacing to the Parallel System Bus. These functions include handshaking protocols, parity checks, message retrys, error reporting and normal fairness and high priority arbitration modes.

SUPPORTS EXTENDED CAPABILITIES

Other capabilities of the Message Passing Coprocessor includes simplifying the interconnect space implementations for both the local on-board bus and Parallel System Bus. The Message Passing Coprocessor supports Central Services Module capabilities such as slot assignment, arbitration ID's and bus timeouts.

INTEL QUALITY AND RELIABILITY

The Message Passing Coprocessor is designed and manufactured in accordance with Intel's high quality standards. Quality is assured through design verification, process and product qualification, rigorous testing and ongoing reliability monitoring.

SERVICE AND SUPPORT

The Message Passing Coprocessor is fully supported by Intel's worldwide customer support operation with free mail-in exchange service during the initial 90-day warranty period. Intel provides a wide selection of seminars, classes, workshops, and on-site support contracts on Intel products. For more information, please contact your local sales or service representative.

SPECIFICATIONS

PACKAGING

149-pin Ceramic Pin Grid Array (PGA)

ELECTRICAL MAXIMUM RATINGS

Operating Temperature	– 10C to + 95C
Storage Temperature	– 65C to + 150C
Voltage on any Pin	– 0.5V to Vcc + 0.5 V
Power Dissipation	2.5W

ORDERING INFORMATION

Product Code	Description
A82389	Message Passing Coprocessor for MULTIBUS II

RELATED LITERATURE

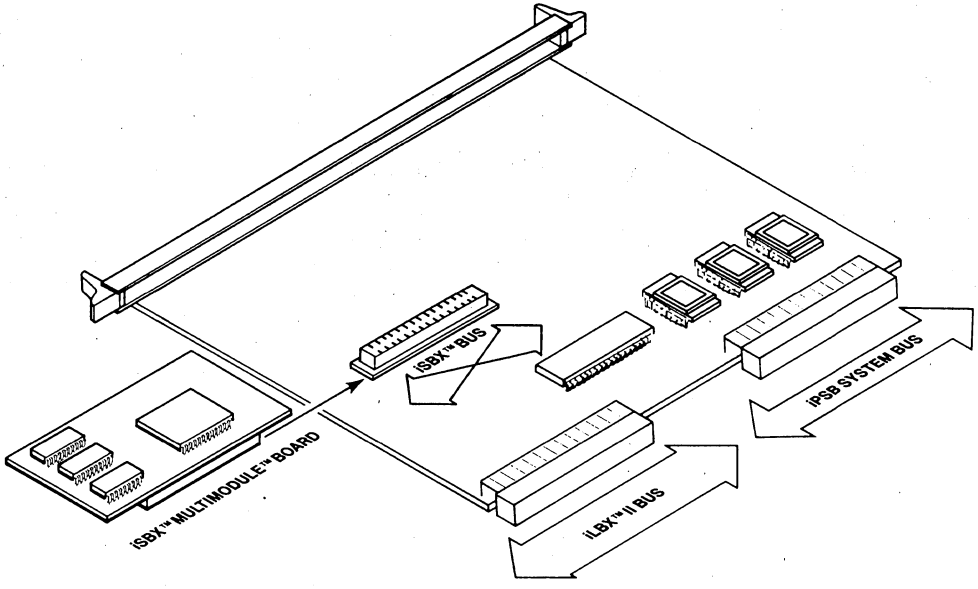
Order Number	Description
290145-002	Message Passing Coprocessor Datasheet
176526-001	Message Passing Coprocessor User's Manual
280717-001	Message Passing in the MULTIBUS II Architecture
149299-002	Interconnect Interface Specifications
280640-001	The MULTIBUS II Interconnect Design Guide

For more information or the number of your nearest Intel sales office, call 800-548-4725 (good in the U.S. and Canada).

MULTIBUS® II
iLBX™ II LOCAL BUS EXTENSION

- **High Bus Bandwidth—**
  —48 Megabytes/sec
- **64 Megabyte (26-bit) Addressing**
- **8-, 16-, 24-, and 32-bit Data Transfers**
- **Reliable Synchronous Clocking up to 12 Megahertz**
- **Burst Transfers up to 64 Kilobytes Per Transfer**
- **Primary and Secondary Bus Master Exchange Capabilities**
- **Supports up to 6 iLBX™ II Compatible Device Per Bus**
- **Pipelined Protocol for Highest Performance**
- **Optional Parity Protection for Address and Data**

The iLBX™ II Local Bus Extension is one of the family of standard bus structures resident within Intel's MULTIBUS® II Bus Architecture. The iLBX II bus is a dedicated execution bus capable of significantly increasing system performance by removing most processor execution activity from the main iPSB™ Parallel System Bus. It extends the processor board's on-board local bus to off-board resources. Acting in conjunction with the processor board, the iLBX II resources form a multiple board "virtual single board computer". The iLBX II bus preserves advantages in performance and architecture of on-board local memory, while allowing memory configurations larger than those possible on a single board.



280376-1

MULTIBUS® II Physical Diagram

September 1987
Order Number: 280376-002

FUNCTIONAL DESCRIPTION

Architectural Overview

The iLBX II bus is an architectural solution for supporting large amounts of off-board memory with the same performance advantage enjoyed by on-board memory (see Figure 1). It allows the CPU board selection to be decoupled from the on-board memory requirement and still maximizes the processor's performance potential. It eliminates the processor's need to access its off-board memory resources solely over the iPSB system bus. In most systems, the processor is the only master on the iLBX II bus, so no time is required to arbitrate for the bus. This means the processor sees significantly lower memory latency than is possible if it were accessing memory over the multiple master system bus. Lower memory latency translates to higher individual processor performance.

In inclusion of the iLBX II bus in the architecture means not just higher single processor performance but higher system performance as well. The movement of execution traffic from the system bus to the iLBX II execution bus makes that much additional system bus bandwidth available to other system resources such as processors not using an execution bus or I/O devices.

For those applications which require a high bandwidth local path to I/O, such as an intelligent disk controller local to a particular processor, the iLBX II bus supports one additional bus master. This architectural enhancement allows a processor to "own" an intelligent I/O controller. All data transfers between these two modules (the processor and the controller) can occur over the low latency iLBX II bus path without distributing activity on the system bus.

Structural Features

OVERVIEW

The iLBX II bus uses a non-multiplexed, processor independent structure supporting 8-, 16-, and 32-bit processors. It supports 8-, 16-, 24-, and 32-bit data transfers over a 26-bit (64 megabyte) addressing range with a maximum bandwidth of 48 megabytes/sec.

All events performed on the bus are synchronous to a reference bus clock. This is not a fixed frequency clock as in the iPSB bus; the iLBX II bus clock runs at the basic processor bus frequency. In other words, a processor whose bus interface runs at 8 megahertz would drive the iLBX II bus at that frequency. This characteristic helps match the iLBX II bus timing to that of the processor transfer rate for best performance. The maximum iLBX II bus clock frequency is 12 megahertz. (Be careful not to confuse a processor's clock input frequency with its basic bus frequency. Many processors internally divide down their clock input by 2, 3, or 4 to obtain the basic bus frequency. It is this basic bus frequency which defines their transfer rate and which drives the iLBX II bus clock.)

NON-MULTIPLEXED STRUCTURED

The iLBX II bus structure is non-multiplexed in order to simplify the interface and obtain maximum performance. The separate address, data, and control paths allow overlapped operation. This overlapping, called pipelining, means that data from a previous operation can be overlapped with the address and command information of the current operation. This characteristic substantially improves bus utilization for those processor-memory subsystems which support the feature.

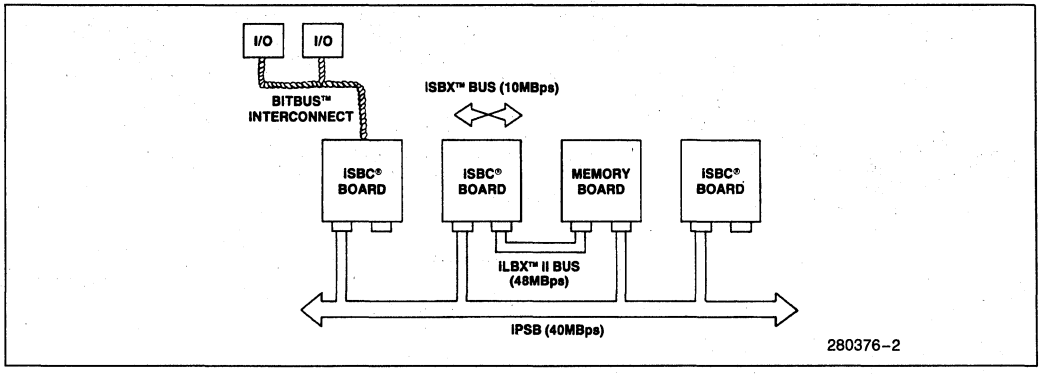


Figure 1. MULTIBUS® II Bus Architecture

INTERCONNECT ADDRESS SPACE

The iLBX II bus supports the slot-addressing concept of the interconnect address space found in the iPSB bus. Including this facility in the iLBX II bus allows the system to identify and configure iLBX II bus boards even though they may not contain a iPSB bus port. (Please refer to the iPSB bus data sheet for additional information on the interconnect address space.)

DUAL BUS MASTER

In order to support a wide range of system configurations, the iLBX II bus defines support for two bus masters. One master is called the Primary master; the other is known as the Secondary master. The Primary master normally "owns" the bus and does not have to spend any time arbitrating for access rights. The Secondary master must ask the Primary master for access rights. The Primary releases the bus at the first opportune time. This hierarchical structure ensures that the Primary master enjoys good memory latency while at the same time gives the Secondary the opportunity to access memory when it needs to.

The iLBX II bus also includes a dedicated interrupt line to facilitate signalling between the two masters for commands and status, and between the memory boards and the Primary master for things such as non-recoverable memory errors.

BUS CYCLE OVERVIEW

Like the iPSB bus, the iLBX II bus protocol consists of three types of bus cycles: arbitration, transfer, and exception.

ARBITRATION CYCLE

The arbitration cycle ensures that one and only one requesting agent is allowed access to the bus at any given time. When a requesting agent determines the need for a bus operation, it enters the arbitration cycle. For either requesting agent, this cycle lasts until it acquires the right to use the bus. In configurations with only a primary requesting agent, no time is spent for this cycle; the agent always has rights to the bus. In configurations where there are both a primary and secondary agent, the primary agent has to arbitrate for the bus only when the bus is busy under the secondary agent's control. Figure 2 illustrates the arbitration cycle.

TRANSFER CYCLE

The transfer cycle is the event where the request (address and command) and reply (data) information is exchanged between the bus agents. Like the iPSB bus, it consists of a request and a reply phase. During block transfers, the termination of the transfer cycle is controlled by the requesting agent. In non-block transfer cycles, the cycle's termination is implicitly recognized by both agents. Figure 3 shows a transfer cycle example.

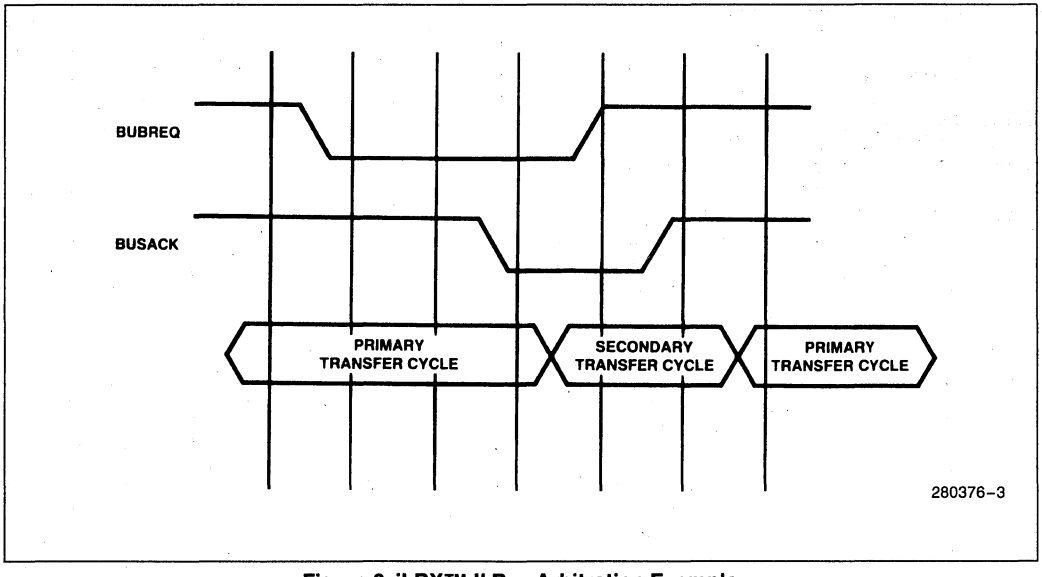


Figure 2. iLBX™ II Bus Arbitration Example

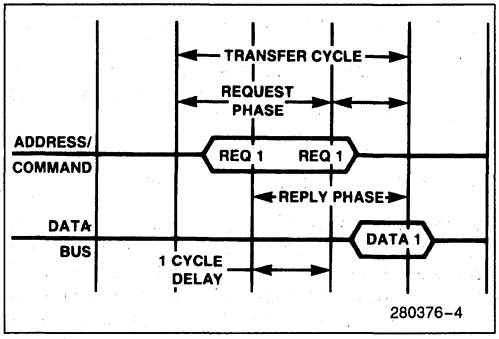


Figure 3. iLBX™ II Transfer Cycle

EXCEPTION CYCLE

Exception cycles allow the bus agents to signal any detected error or exceptional condition which might arise during a transfer cycle. Typical exceptions are uncorrectable ECC errors, parity errors, or physical boundary overflows.

Signal Groups

OVERVIEW

There are five categories of signals used in the iLBX II bus: address/command, data transfer, access control/status, bus control/status, and miscellaneous. An asterisk following the signal name or group indicates that the signal or group use their low electrical state as the active state.

ADDRESS/COMMAND

The requesting agent uses this group of signals to transfer address and command information to the potential replying agents during the request phase of a transfer cycle. This signal group consists of the non-multiplexed address lines, **XA25 through XA00** (Extension bus address), the command specification lines, **XC3 through XC0** (Extension bus command), and an associated parity line, **XAPAR** (Extension bus address/command parity).

The XA25 through XA00 lines define the starting physical byte address. The command specification lines select the address space (memory or interconnect), data width (1, 2, 3, or 4 bytes), and whether the operation is a read or write cycle. The command encodings for XC3 through XC0 are shown in Figure 4.

XC3*	XC2*	XC1*	XC0*
Address Space	**Access Type**	**Width Specification**	
Memory	Read	1 byte 2 bytes 3 bytes 4 bytes	
Interconnect	Write		

Figure 4. iLBX™ Ii Command Encoding

Parity for the address/command group is not required. The bus does allow for a single parity bit covering the address and command lines as a compliance level. The iLBX II bus environment is much different than that of the iPSB system bus. It extends only a short distance (6 card slots maximum) and employs lower switching currents. This more restrictive environment reduces the need for data integrity protection in all but the larger systems.

DATA TRANSFER GROUP

This signal category consists of the 32 bi-directional data lines and their optional parity line. **XD31 through XD0** (Extension bus data) transfer the read or write data between the requesting and replying agents. Each byte in the iLBX II bus memory is mapped to one of the four byte locations of the XD lines. This technique is commonly referred to as "byte lanes" and is illustrated in Figure 5.

Like with the address/command group, the **XDPAR** (Extension bus data parity) line is optional.

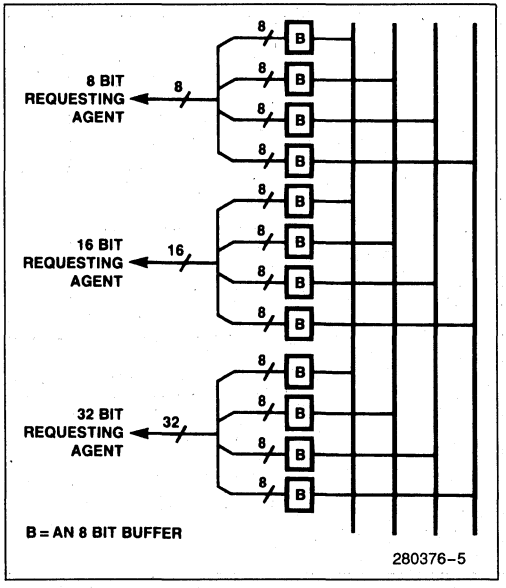


Figure 5. iLBX™ II Data Bus Alignment Interface Requirements

ACCESS CONTROL/STATUS GROUP

This signal category consists of 5 lines which determine the start of an access request, its execution, and finally, its termination.

The **XACCREQ*** (Extension bus access request) signal indicates that the address/command information is valid during the current and next bus clock cycles. It signals the presence of the request phase of the transfer cycle. Replying agents which require more time to decode the command information can extend XACCREQ* using the XWAIT* handshake line.

The **XWAIT*** (Extension bus wait) signal has a two-fold meaning in the access protocol: it can extend the duration of the request phase and it serves as a "not ready" replier indication during the reply phase. If asserted in the first clock cycle of the request phase, it extends the phase, otherwise, it will signal "not ready" during the reply phase.

In many system configurations the iLBX II bus memory boards are dual-ported to both the iLBX II and iPSB buses. This requires a mutual exclusion facility when implementing semaphores and other data structures in this shared memory. The **XLOCK*** (Extension bus lock) signal allows the iLBX II bus requesting agents to lock out the other port while performing indivisible accesses to shared structures.

To perform block transfers on the iLBX II bus, the requesting agent asserts the **XBTCTL*** (Extension bus block transfer control) signal. This line informs the replying agents that two or more data transfer periods will accompany a single request phase. XBTCTL* is de-asserted by the requesting agent to signal the end of the block transfer.

BUS CONTROL/STATUS GROUP

The signals in this group control the passing of bus ownership between the primary and secondary requesting agents. When the bus is in use, they also indicate which agent is in control.

The **XBUSREQ*** (Extension bus request) signal is driven by the secondary requesting agent to acquire the bus from the primary agent. Only the primary requesting agent receives this signal. When the primary detects that the secondary is requesting the bus, it replies with the **XBUSACK*** (Extension bus acknowledge) signal to inform the secondary that the bus is now his. This bus exchange occurs at the discretion of the primary.

The secondary owns the bus after asserting XBUSREQ* and receiving XBUSACK* active. The primary can request that the bus be returned at any time by removing XBUSACK*. The secondary must return the bus at the earliest time; typically when it completes its current transfer cycle.

MISCELLANEOUS CONTROL GROUP

The **XRESET*** (Extension bus reset) is driven by the primary requesting agent to locally initialize its iLBX II bus environment. It is typically asserted after the agent receives a reset indication on the iPSB system bus.

The **XINT*** (Extension bus interrupt) allows the secondary requesting agent and any of the replying agents to signal the primary requesting agent for inter-module communication. Since the secondary agent is usually performing tasks on behalf of the primary agent, this interrupt line removes the need for the primary to continuously poll the secondary for completion of its tasks.

The **XID2* through XID0*** (Extension bus identify) lines are hardwired lines on the backplane to allow any iLBX II bus board to determine its position on the bus. They encode the interconnect space least significant three bits of the slot ID field. (See the iPSB bus data sheet for an explanation of the interconnect address space.)

The final line is the **XBCLK*** (Extension bus clock) line. It provides the reference timing signal for the synchronous bus operations. It is driven by the primary requesting agent at its processor bus frequency.

The iLBX II bus also defines additional +5 volt and ground pins.

Bus Protocol

In the MULTIBUS II specification, both timing diagrams and state-flow diagrams describe the iLBX II bus protocol. The state-flow diagrams present the lowest level and most rigorous definition while the timing diagrams help conceptual understanding. For the purposes of this data sheet, only the timing diagram description is used. The following sections use Figure 6 as an example of the protocol.

ARBITRATION CYCLE

With only two potential requesting agents contending for access rights to the bus, the arbitration cycle is very simple. The figure illustrates the secondary requesting agent requesting the bus from the primary and then running a simple transfer cycle. The secondary requesting agent makes its request by asserting XBUSREQ*. The primary gives up the bus

by returning XBUSACK* active. In this example, the secondary uses the bus for only a single transfer cycle so it de-asserts XBUSREQ* when complete. The primary agent responds by withdrawing XBUSACK* to indicate it now owns the bus.

TRANSFER CYCLE

Like in the iPSB bus, the transfer cycle proceeds as a request phase and a reply phase. The requesting agent (either the primary or the secondary depending upon who currently owns the bus) informs the potential replying agents of the request phase by driving valid information on the address/command signal group and asserting **XACCREQ*.** The request phase normally lasts two clock cycles although the replying agents have the opportunity to extend the phase as long as necessary by asserting XWAIT* during the first clock period of the phase. The phase is extended as long as XWAIT* is active. In the example, the request phase is extended one additional clock.

The reply phase begins when XWAIT* is de-asserted. At this point, the meaning of XWAIT* changes to become a "not ready" indication from the selected replying agent. In the example, the replying agent requires one additional clock period to supply the data so XWAIT* is asserted for one clock. The reply phase terminates on the same clock that data is valid.

EXCEPTION CYCLE

If transfer integrity checking is implemented on the iLBX II bus, errors are signalled on the clock following the last valid information period. In example, errors detected on the address/command lines during the request phase are signalled on the clock following the removal of valid request information. The same applies to errors detected on the data lines during the reply phase.

Mechanical

The iLBX II bus is defined on the P2 connector of two-connector MULTIBUS II boards. Since the iLBX II bus environment is local to a particular processor board, the iLBX II bus backplane does not extend the entire length of the iPSB bus backplane. This allows for multiple iLBX II bus environments in a given system.

The pin assignment for the iLBX II bus on P2 is shown in iLBX II specification section in the MULTIBUS II Bus Architecture Specification Handbook.

Please refer to Intel's MULTIBUS II Bus Architecture Specification Handbook for more detailed information.

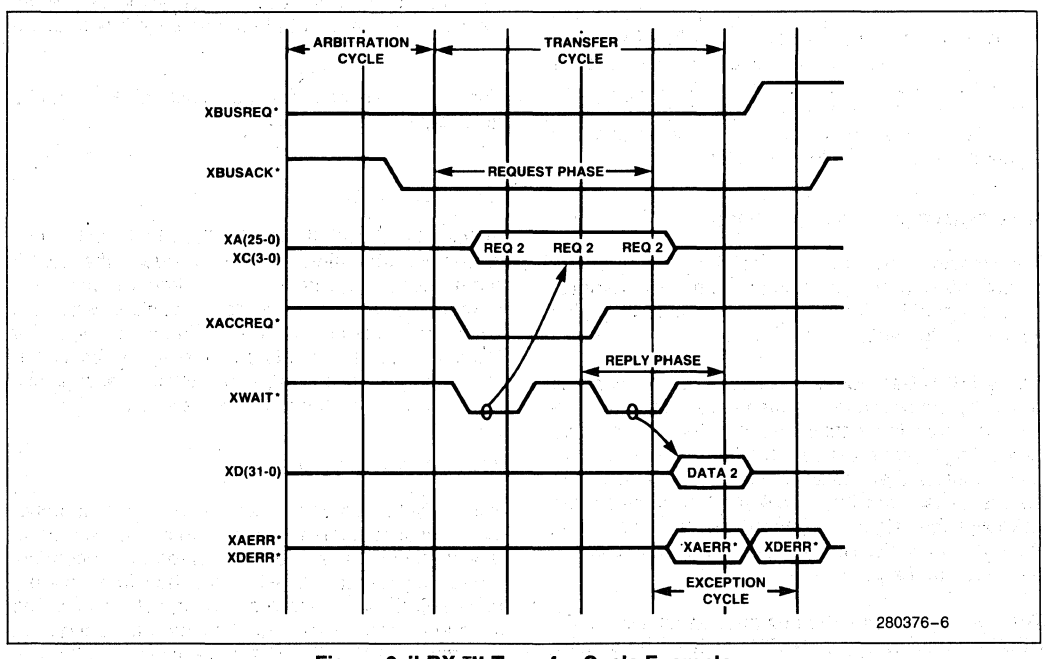


Figure 6. iLBX ™ Transfer Cycle Example

ENHANCING SYSTEM PERFORMANCE WITH THE MULTIBUS® II ARCHITECTURE

Although the MULTIBUS® II architecture can accommodate systems with a wide range of performance, systems that take advantage of its multiprocessing capabilities can achieve new performance levels while maintaining reasonable price/performance ratios. Today, multiprocessing provides an easy path to increased functionality and processing power largely because of the availability of inexpensive memory and CPUs.

The low cost of high-performance microprocessors and RAM chips has drastically altered the cost dynamics of systems design. The material cost of a CPU and its memory are typically a small portion of the total system cost, in sharp contrast to mini and mainframe computers where the cost of the CPU and memory is the majority of system cost. The decreased cost factor means today's designer can optimize a system's price/performance by dedicating a CPU to each function in the system.

This product brief will discuss the MULTIBUS II multiprocessing capabilities and their user benefits. The capabilities include:

- A high-speed local environment
- An efficient burst transfer capability
- A hardware-based message passing facility

Higher Performance Through Multiprocessing

The key to high performance in multiprocessing systems is allowing all of the processors to run concurrently in their own private environments. For this to occur, each functional module must contain its own CPU, memory and I/O resources. It also means that the system bus is primarily used for passing commands and data between modules.

A system using this approach might consist of a host processing board and intelligent disk controller, a terminal concentrator and LAN controller boards (Figure 1). Each

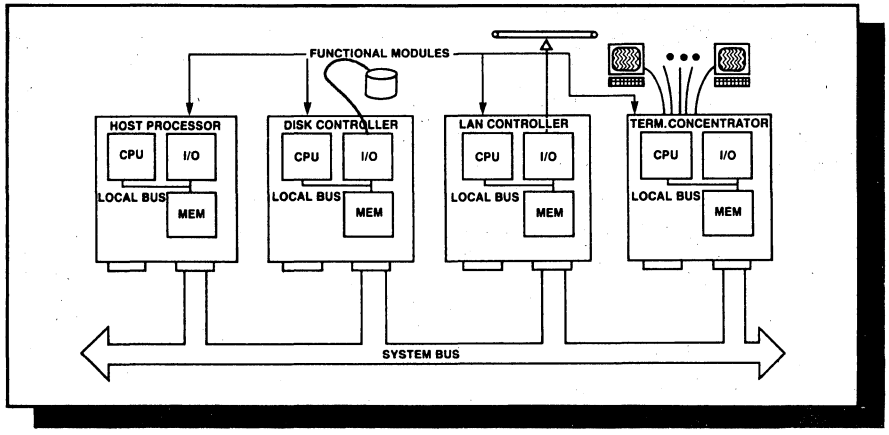


Figure 1. Functional Partitioning is the Distribution of CPU, Memory & I/O Resources to Support Different Functions in a System

functional module would contain the resources required to perform its assigned function. Further, each module would operate over its own private local bus which is decoupled from the system bus. This enables the modules to operate concurrently with each other and leaves the system bus open for communication between the intelligent modules.

High-Speed Local Environment Optimizes On-Board Resources

In multiprocessing systems, performance is optimized when all execution code and data is accessed in a local environment. The most important performance factors in a local environment are the CPU clock speed, the number of CPU clocks per instruction, the CPU instruction set, and the number of memory wait states. While the CPU choice dictates the CPU performance factors, the bus architecture can assist in providing a good CPU-memory and I/O environment.

The MULTIBUS II architecture provides a high-speed local environment through its moderate size board form factor and a local memory bus extension. The MULTIBUS II board form factor is the Eurocard Standard 233mm by 220mm (9.1″×9.0″), chosen because it allows most functional modules to completely fit on one board. This factor is critical to system performance because on-board resources can be optimized to run at their full potential without impacting the system bus. A smaller board size would force a particular function onto multiple boards with a resulting decrease in performance.

Burst Transfers

A key development to optimizing the iPSB bus for multiprocessor communications is the high-speed burst transfer capability. Since address information is transferred over the bus only once for the entire burst, performance is greatly enhanced.

The synchronous handshake capabilities of the iPSB bus nearly double the speed of burst transfers compared to traditional asynchronous handshakes (Figure 2). Burst

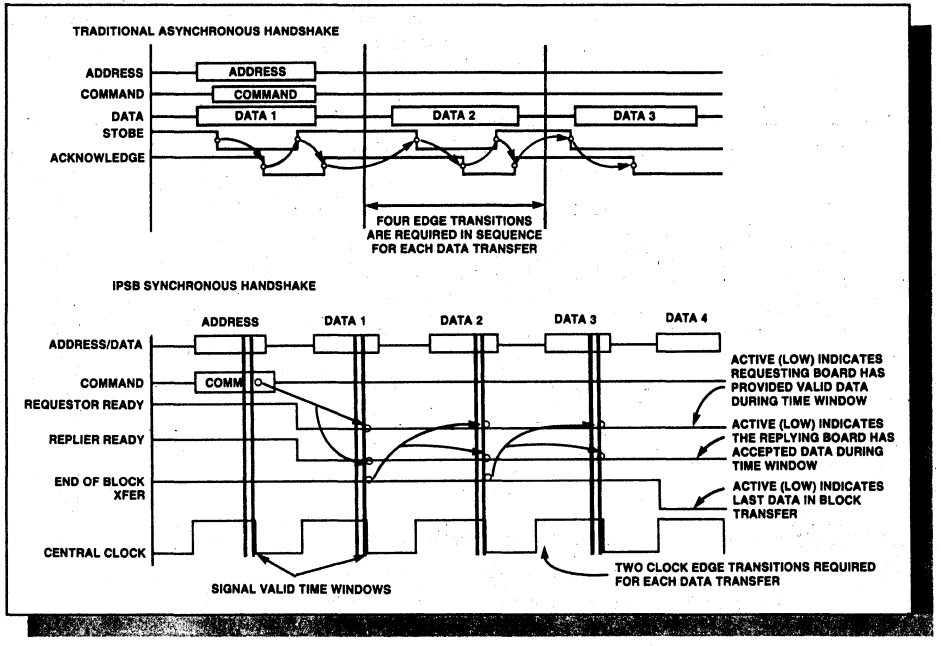


Figure 2. iPSB Synchronous Handshake Compared to Asynchronous Handshake

transfers allow boards to transfer blocks of data over the iPSB bus at speeds up to 40 Mbytes/s. This speed approaches the limit of what can be expected from TTL technology when propagation across a 20-slot backplane is required.

In the iPSB bus, a burst transfer consists of one address clock followed by multiple data transfers. The receiving board takes care of actual memory location placement (ie., auto-increments the memory address, as necessary). The actual speed of the burst transfer will depend on the abilities of the communicating boards. For example, burst transfers from an intelligent board to dual-port memory will typically be only marginally faster than single-cycle writes, due to the long access times from the system bus side of dual-port memory boards.

To achieve the true performance benefits of burst transfers, each board needs the ability to send and receive small bursts at the full bandwidth of the system bus. This can be accomplished by bus interface logic containing high-speed buffers and the ability to format and send 32-bit-wide data bursts.

In the MULTIBUS II architecture, the interface bus logic to the iPSB is defined with burst capability in a message-passing scheme. This ensures that boards developed by various manufacturers will all be able to communicate compatibly at tremendous speeds.

Message passing, as defined in the MULTIBUS II protocol, allows modules to communicate directly. In other words, one module sends a message (data) over the iPSB bus to the address of another module. This differs from the normal CPU functions of reading or writing only from memory or I/O.

Since conventional CPUs do not contain facilities to perform direct CPU-to-CPU communication, additional hardware logic is required. The hardware can be thought of as a coprocessor to the primary CPU, e.g., a coprocessor that adds the function of direct module-to-module communication at speeds many times that which the primary CPU could perform. The coprocessor logic for message passing resides in the bus interface.

An example best illustrates how message passing works (Figure 3). Assume Board A wants to send 1 Kbyte of data to Board B. First, the CPU on Board A would instruct its message passing unit to send 1 Kbyte of data (with the assistance of a DMA device), beginning at a particular location in local memory, to Board B. Next, the message passing coprocessor on Board A takes over so the CPU

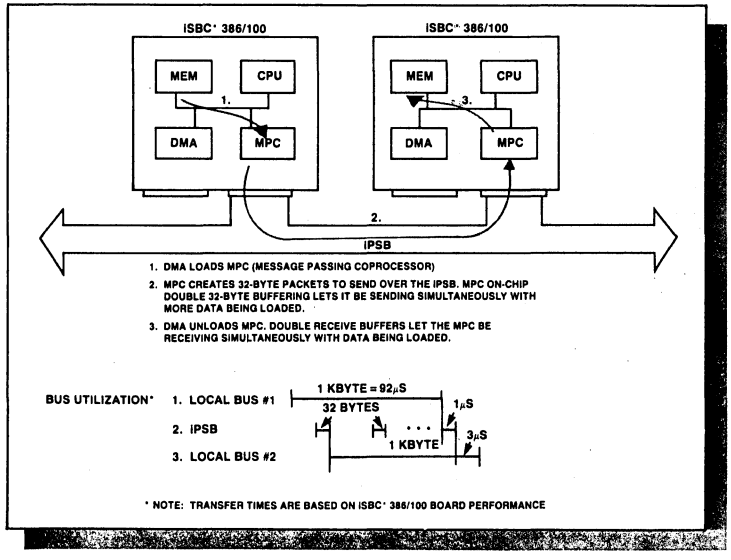


Figure 3. A Message Passing Example

can perform other processing. At this point, the DMA device loads the data into the message passing coprocessor on Board A. Once enough data has been loaded (typically 32 bytes), the coprocessor arbitrates for the bus and sends the first packet of data as a burst transfer to the message-passing logic on Board B.

While the message passing logic on Board B is unloading the first packet out of its high-speed buffers into local RAM, the message-passing logic on Board A is reading the next piece of data into its high-speed buffers. Meanwhile, the system bus is free of traffic and available for another pair of boards to communicate over.

The message-passing logic on Board A continues to build and send small packets of data to Board B's message-passing logic, and Board B continues to unload this data into its local memory until the entire 1 Kbyte has been transferred. At the completion of the transfer, the message-passing logic on both boards interrupts their respective CPUs to notify them that the transfer is complete.

Summary

Five important performance benefits result from the MULTIBUS II multiprocessing capabilities and specifically from hardware-assisted message passing. First, all single-cycle memory/IO transfers can be designed to occur in local CPU environments. These environments are optimized for single-cycle transfers over their local memory buses and usually run at few or no wait states, compared to substantial wait state delays over a system bus.

Second, transfers over the iPSB bus can be done as burst transfers between message-passing logic containing high-speed buffers, thereby transferring data at the maximum bus data rate. Third, the iPSB bus is not in use between data packets and is available for other traffic. Fourth, each CPU does not need direct access into the other board's local environment. That is, no dual port memory (which is slower than single port memory) is required. And fifth, each CPU is available to process other tasks while the data transfer is occurring.

INCREASING SYSTEM RELIABILITY WITH THE MULTIBUS® II BUS ARCHITECTURE

System reliability is more than just mechanical factors like Eurocard and DIN connectors. It involves many design factors often overlooked in traditional buses. The MULTIBUS®II bus architecture addresses the problem of system reliability not only from a mechanical point of view, but from protocol and electrical factors as well. This product brief will discuss how the following MULTIBUS II features resolve specific reliability problems while enhancing overall system reliability:

- Synchronous Timing
- Bus Parity
- Protocol Error Handling
- Bus Timeout
- Power Sequencing
- Eurocard/DIN Connectors
- Front Panel Design
- Backplane Design

INCREASING ELECTRICAL RELIABILITY

Synchronous Timing for Enhanced Noise Immunity

Traditional buses, such as MULTIBUS I and VME, are based on asynchronous timing where the edges or transitions of the bus-control signals cause the bus to perform its functions. Unfortunately, edge-sensitive timing is susceptible to external disturbances and noise. If noise causes a signal to look as though it made a transition, the transition is misinterpreted and a failure results.

The MULTIBUS II architecture addresses this problem by using synchronous sampling of all signal lines. Both the MULTIBUS II Parallel System Bus (iPSB) and the Local Bus Extension (iLBX™ II bus) employ synchronous sampling for enhanced noise immunity. The iPSB serves as a good example of the benefits of synchronous sampling.

In the iPSB bus, all signals (address, data, control, and arbitration) are driven and sampled with respect to a 10 MHz bus clock. The 10 MHz clock breaks the bus activity into 100ns increments with signals sampled at the end of each period. This method avoids looking at the signal while transitions caused by reflections and crosstalk are occurring. Therefore, signals are vulnerable only during the small sampling window.

Figure 1 shows the iPSB timing with the 100ns period divided into three intervals: driver timing, bus propagation, and receiver timing. The 40ns driver timing interval takes into account driver logic delays and the capacitive loading for a maximum of 20 loads spaced over 16.8 inches.

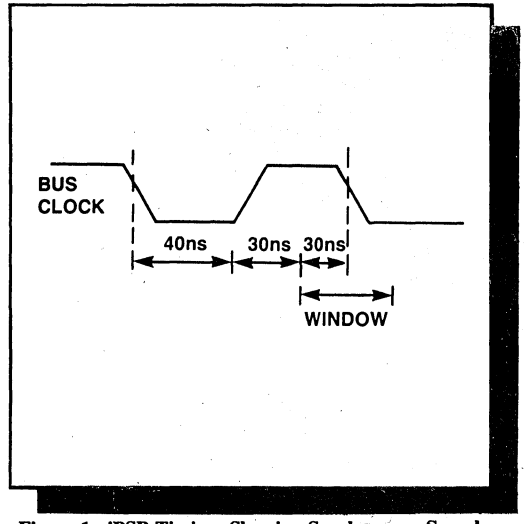


Figure 1. iPSB Timing, Showing Synchronous Sample Driving Stable Data Window

The bus propagation interval accounts for 25ns of signal transit time and 5ns of potential clock skew. A signal traveling on the backplane creates reflections on itself and crosstalk on other signals. The signal transit time allows the signal to propagate down and back on the backplane. It also allows time for crosstalk to subside. This guarantees that the signals have stabilized in spite of distance and interference from other signals.

The receiver interval consists of a 30ns receiver setup time plus 5ns of hold time which extends into the next cycle. This interval is the time the signal is stable prior to sampling on the falling edge of the clock.

Thus, the MULTIBUS II parallel bus timing creates a 65ns interval (driver timing plus bus propagation) when the bus is completely immune to noise or external disturbances. That means during 65% of the time interval, noise causing a transition or level change is simply ignored. It is only during the 35ns receiver setup and hold interval that the bus timing is vulnerable to noise. During this interval, however, the bus contains parity protection (to be discussed in another section).

Comparable Performance at Higher Speeds

A common complaint about synchronous buses is that fixed time increments limit performance compared to asynchronous buses. This may be true at slower bus clock speeds. However, at 10 MHz the differences diminish. If both an asynchronous and a synchronous bus use similar TTL technology for the bus drivers and receivers over the same backplane length, they possess roughly the same bus timing. In other words, the driver timing, bus propagation, and receiver intervals of both buses will be approximately the same with nearly equal performance. However, as we've seen, a synchronous bus offers a significant improvement in system reliability that easily justifies its use.

Guaranteed Electrical Compatibility

Synchronous sampling also has a less obvious benefit — guaranteed electrical compatibility among boards. The 100ns timing of the iPSB is based upon a worst-case environment of 20 boards over a backplane length of 16.8 inches (0.8 inch separation). All derating for loading, voltage margin, and skew is included. Thus, any number of boards, up to 20, are guaranteed to work together.

Electrical compatibility is much harder to achieve in asynchronous buses. Because they are edge-sensitive, asynchronous boards are naturally susceptible to changes in signal edge rates and timing. When the number of boards in a system change, edge rates and timing also change, in some cases adversely affecting system reliability.

The synchronous nature of the bus moves the point of synchronization to the local bus of each board. When two asynchronous CPUs communicate, synchronization between them occurs between each CPU and its interface. This provides a better electrical environment for dealing with reliability problems caused by metastability.

Bus Parity Versus Memory Parity

At this point, it is important to distinguish between BUS parity and MEMORY parity. (See Figure 2.) Both allow the detection of errors. Memory parity protects *data* while it is resident on a memory board. Bus parity, on the other hand, protects *address, control,* and *data* while in transit on the bus. In a sense, one complements the other in reliable systems. In both cases, it is possible to handle errors via retry or other mechanisms.

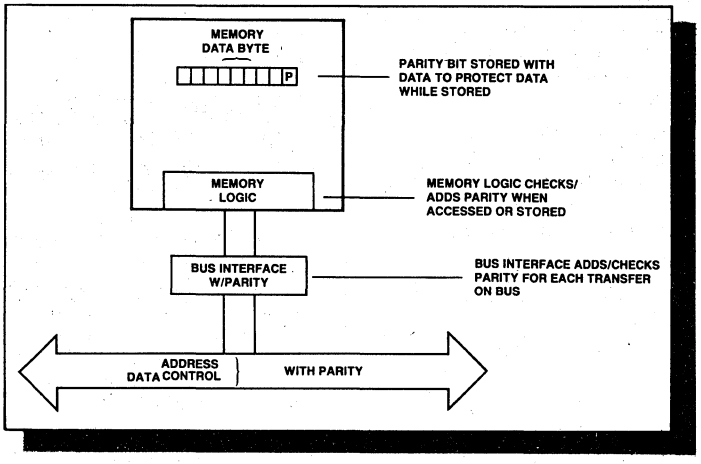


Figure 2. Parity Protects Address Data and Control from Errors which could be Incurred on the iPSB Bus

Bus parity in the MULTIBUS II architecture provides another level of electrical reliability by protecting the bus from noise and external disturbances during the receiver timing interval. It also protects the bus from failed interface components.

On the iPSB bus, the board driving the bus generates bus parity. Address and data lines use byte parity, while control lines use nibble (4-bit) parity. All receiving boards check parity during the receiver timing sampling interval. If an error is detected, the BUS ERROR line is activated. This stops activity on the bus and puts the bus into a predefined known state.

At this point, the system designer has a number of options: retry the transfer, swap in a hot spare, log the error, ignore it, or shut down the system gracefully. Which option he chooses depends on his specific system requirements. Basically, the protocol gives him the opportunity to evaluate the situation and take appropriate action.

PROTOCOL RELIABILITY

Board-to-Board Error Indications

Not all errors occur because of noise or component failure. Sometimes they occur when one board asks another to do something it is not capable of doing. Although traditional buses typically ignore these kinds of errors, they can cause system failure just as noise can. The MULTIBUS II architecture offers a solution.

In the iPSB bus protocol, when one board cannot perform the request, it simply informs the requesting board and allows it to attempt a retry. Five types of error indications are supported: data, transfer width, continuation, not-understood, and negative acknowledge.

A *data error* indicates that the replying board has detected an error with the requested data, for example a memory parity error. *Data transfer errors* occur when the replying board does not support the requested data width. For example, the requesting board might ask for a 32-bit transfer from an 8-bit device. After the replying board indicates the error has occurred, the requesting board can retry the transfer with an 8-bit width.

Although the iPSB bus protocol allows for burst transfers (multiple data cycles following one address cycle), not all boards need to support this capability. If a requesting board attempts a burst transfer with a board which does not support bursts, the replying board will return a *continuation error*. The requesting board can recover by simply retrying with the necessary address cycles.

Trying to write to a read-only memory board is a good example of a *transfer-not-understood error*. This type of error occurs when the replying board does not support the requested operation. As with other board-to-board errors, the requesting board many retry with another request.

The last kind of error, called a *negative acknowledge error*, occurs during a message transfer when resources are not available in the receiving board. This is used for flow control in the MULTIBUS II message passing protocol, a queue-based data movement protocol. Negative acknowledge errors instruct the requesting board to retry the operation at a later time, giving the replying board time to process the data in its queue.

Bus Timeout

Another protocol reliability feature in the MULTIBUS II architecture is the BUS TIMEOUT monitor in the Central Services Module (CSM). If a bus transfer fails to complete within a specified time (e.g., a failed board), the CSM, which monitors all bus activity, activates the BUS TIMEOUT line. This stops all bus activity and places the bus in a predefined known state for recovery. At this point, the error is logged and normal bus activity can resume. As an added feature, designers may define their own timeout error handling policy.

POWER SEQUENCING

The iPSB bus protocol also contains a mechanism for orderly handling of power-up and power-down sequencing. For normal power on/off and unexpected power failures, timing of the RESET, DCLOW, and PROTect signals coordinate the sequencing. The combination of the RESET and DCLOW lines signal whether the power-up operation is a warm or cold start of the system.

Once the system is running, the DCLOW signal (driven by the CSM) is used to indicate imminent loss of DC power (Figure 3). At this time, the system has a predetermined time to save state information. After that interval,

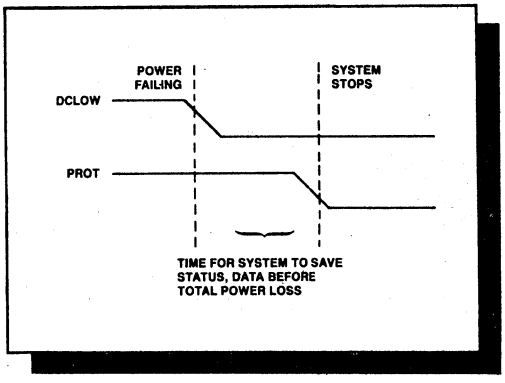


Figure 3. Power Failure Control Lines

the CSM activates the PROTect line which prevents transitions on bus lines from affecting the system during power loss.

MECHANICAL RELIABILITY

The MULTIBUS II mechanical specification is based upon the Eurocard form factor and DIN connectors. However, unlike traditional bus architectures, it goes beyond these mechanical standards with a front panel design that helps the system designer solve EMI (Electro-Magnetic Interference) and ESD (Electro-Static Discharge) problems.

Eurocard and DIN Connectors

The Eurocard family of mechanical specifications is noted for its high reliability in rugged and industrial environments. The MULTIBUS II specification calls out the two-connector 233mm by 220mm and single-connector 100mm by 220mm size boards. The two connector board contains almost the same board area as the 6.75 by 12 inch MULTIBUS I board. That is, it is large enough to allow the implementation of single-board computers with I/O, CPU, and memory onboard, even for 32-bit CPUs.

The DIN 41612 (also known as IEC 603.2) connectors are 96-pin two-piece connectors where each pin consists of a blade mating with two contact points on each side of the blade. This connector approach offers advantages over the board-edge style connectors. Among them are tighter dimensional tolerances, reduced sensitivity to vibration, improved protection from environmental contaminants, and a larger number of cycles for insertion and removal.

FRONT PANEL SYSTEM

The MULTIBUS II front panel system (Figure 4), while dimensionally compatible with standard Eurocard front panels, offers several important advantages.

(Note that while this front panel technology is different from normal Eurocard practice, the dimensioning is such that MULTIBUS II boards fit in any standard Eurocard packaging.)

Standard Eurocard front panels make it difficult to comply with EMI and ESD regulations without the use of additional shielding. Adjacent front panels form small, narrow slits between boards which function like a slot antenna at some frequencies. Through these narrow slits, EMI can enter or exit the system and additional shielding is usually required.

To solve this problem, the MULTIBUS II front panel is U-shaped. From an EMI point-of-view, this makes the front panel electrically thicker. While the size of the slit between adjacent boards is the same as the standard Eurocard front panel, the electrically thicker front panel attenuates EMI which satisfies FCC EMI regulations and protects the system from external EMI.

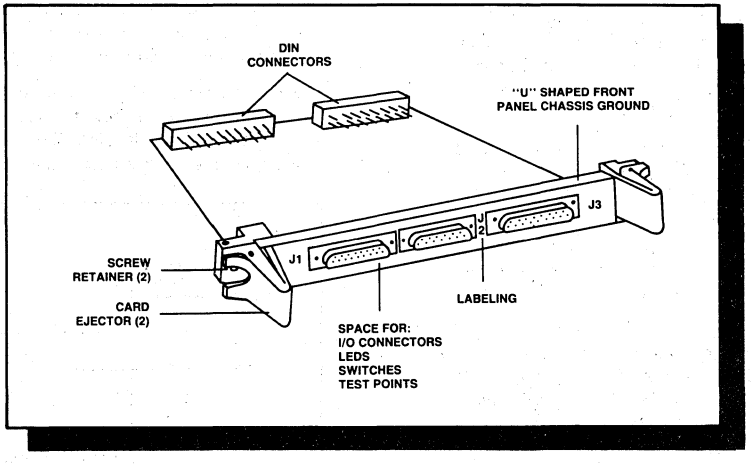


Figure 4. MULTIBUS® II Front Panel System

The U-shaped front panel also adds structural rigidity to the board and has captive retaining screws for securing the board to the system. Shielded I/O connectors located through the front panel eliminate the need for intermediary cables and connectors. In addition, the front panel is at chassis ground for protection against static discharge.

BACKPLANE DESIGN

Designed for reliability, the iPSB bus backplane consists of six layers — three signal layers sandwiched between three power and ground planes (Figure 5). The power and ground planes provide for good power distribution. Moreover, since they are in between each signal layer, they reduce the opportunity for crosstalk due to coupling between the signal layers.

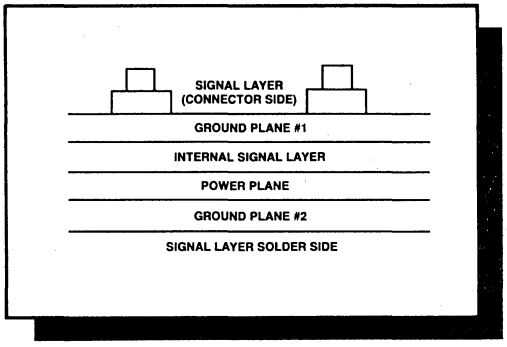


Figure 5. Backplane Design

On each signal layer, signal lines are laid out identically to minimize signal skew across the backplane. To control reflections, each signal line is passively terminated.

Both power and ground connections are evenly distributed across the connectors with 9 pins allocated for +5 volts and 15 for ground providing ample current and good ground return paths.

SUMMARY

Because the MULTIBUS II architecture addresses the problems of electrical, protocol and mechanical reliability, it is superior to traditional buses in achieving overall system reliability. Besides the mechanical reliability of its Eurocard form factor, DIN connectors, and backplane design, the MULTIBUS II electrical protocol is highly immune to noise and external disturbances because of its synchronous sampling and bus parity. In addition, the agent error capability catches common operational errors. Other operational concerns such as bus time-out and power sequencing are fully specified.

GEOGRAPHIC ADDRESSING IN THE MULTIBUS® II ARCHITECTURE

Although microcomputer board designers and system integrators have different sets of requirements for building their products, some degree of overlap exists. Board designers are concerned about factors like function and life cycle costs, testing procedures, development time, and manufacturing costs. System integrators need fast turnaround as well, but they are also faced with the challenge of trying to customize a single board design by configuring it slightly differently for each application. Like the board designer, system integrators are also concerned with testing procedures and inventory costs.

The MULTIBUS®II architecture satisfies the requirements of both board and system designers by defining a unique address space called interconnect space which provides geographic addressing. The following discussion will center on the advantages that interconnect space and geographical addressing bring to system integration and single-board computer design:

- Easy system configuration
- Improved board testing productivity
- Efficient system testing
- Reduced inventory costs

System Configuration Simplified

In traditional bus architectures, system configuration is typically an arduous and complex process. The configurable features of boards are selected manually with jumper stakes connected by wirewrap, a jumper plug or DIP switches. With complex boards, the number of jumper stakes often exceeds 150 and can exceed 300. Getting the jumpers correctly connected is rarely accomplished the first time.

Interconnect space greatly simplifies system configuration through geographic addressing (Figure 1). Critically important is the system's ability to identify which boards are installed in each slot. This allows two identical boards to be uniquely addressed and configured separately. Each board is identified through one or more data bytes accessed through interconnect space addresses. For example, the manufacturer, the board name, the board type, and other parameters are accessible in each board's interconnect space. Further information (e.g. memory size, memory protection) that is available in each board's interconnect space categorizes the exact configuration.

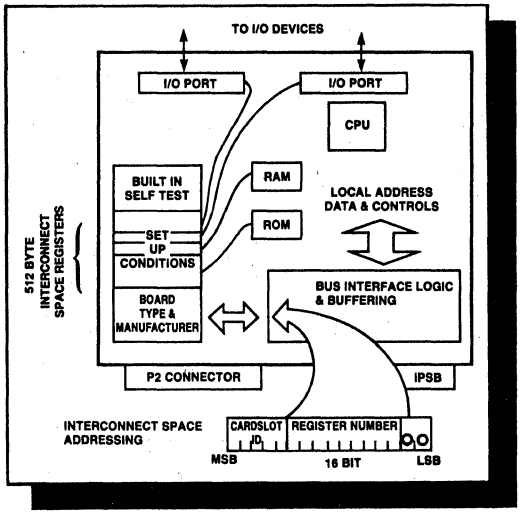


Figure 1. Board Configuration Using Interconnect Space.

Since system software can write the board parameters over the Parallel System Bus (iPSB bus), jumper stakes are virtually eliminated. If jumpers are required, as in switching from RS 232 to RS 422 drivers for example, software can still read the jumpers to verify they were installed correctly.

Another benefit of auto-configuration, is that only one version of the host operating system is needed to run several configurations of the system. For example, if a particular communications board is installed, the operating system detects the board and properly configures it into the system. Moreover, the slot picked to install the new board is irrelevant because arbitration priority and interrupt control are configured independent of the slot in which the board resides.

In addition, a level of fault-tolerant systems can be built using geographic addressing. Redundant hot spare boards can be installed into the system, but not configured by the operating system until needed. Thus, in the normal operating mode, the redundant boards are not active on the backplane. If a board fails, the operating system can isolate the board from the bus, and then configure in the new board. Again, human intervention is not needed to complete the swap.

More Productive Board Testing

Besides simplifying system configuration, interconnect space supports registers for Built-in-Self-Tests (BISTs). Diagnostic software resides on each board (in a PROM) enabling an independent processor to execute the code. That is, a secondary microcontroller and/or the primary CPU can execute board level tests and store the results in interconnect registers. The results can be accessed by any other board in the system and displayed on each board's front panel LED.

Geographic addressing also makes board testing procedures more productive. This is because one general-purpose test suite is all that is required to test many different boards. The test software goes out on the iPSB bus, identifies each board, and reads the results of the BIST for each board. It can then report to the test engineer which board failed what test. Additionally, because the same test program executes for all boards, boards can be mixed and matched on a single backplane.

Test procedure productivity also improves because several configurations of a particular board can be tested in the same general test suite. Since stake pin jumpers are minimized, the test software can actually reconfigure a board several times during the same test. For example, a 1 Mbyte memory board can be tested in an entire 16 Mbyte address range. Moreover, because human intervention is not required, tests execute more smoothly.

More Efficient System Testing

Once individual boards have passed board-level tests, they still must be tested in the systems environment. System-level testing becomes significantly more efficient because of geographic addressing. For example, just one System Confidence Test (SCT) could potentially exist for all MULTIBUS II systems. The SCT can look at all the boards in the system, examine BIST results, and execute system test software based on the BISTs. In fact, detailed results, including configuration parameters, can be displayed on a console (Figure 2).

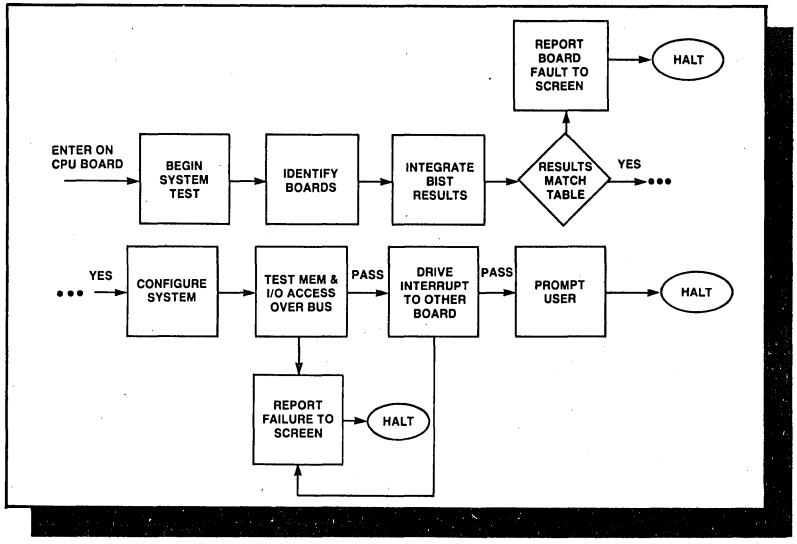


Figure 2. System Confidence Test (SCT) Flow Diagram.

System integrators in particular can capitalize on the advantages of MULTIBUS II system testing. Typically, many configurations of a base system are available from a system vendor. The system integrator only needs one system test program (much like the board vendor described above needs only one general-purpose test suite) to test all of his different systems.

Another benefit of geographic addressing is remote diagnostics. Since interconnect registers are accessible over the iPSB bus to any board, a remote terminal can address the registers through a GAN (Global Area Network) card. Thus, modem communication to a serial port in a system gives the system designer a more versatile test environment.

Lower Inventory Costs

Geographic addressing aids the industrial engineer in managing board inventories. Since board vendors typically stock a few configurations of each basic board, jumpering boards is necessary for each individual configuration. In the MULTIBUS II architecture, however, different board configurations look the same so separate bins of board inventory are not necessary. Thus, the cost and effort required for inventory management can be dramatically reduced.

The system builder stocks boards in the incoming parts warehouse. Like the board vendor above, he can now stock all the boards in the same bin, also reducing his inventory efforts. Then when the system engineers integrate their system, software configures the board to the needs of the application. Because jumpering is reduced, there is less confusion regarding which configuration is standard from the vendor, or which configuration is appropriate for the application.

Summary

Geographic addressing offers many important benefits to single-board computer designers and system integrators alike. All configuration parameters are stored in interconnect registers that sit on each board. Because the registers are accessible over the iPSB bus, a single operating system can configure the system without operator intervention. Both board and system level testing procedures are improved, as only one general test suite is needed. Finally, inventories are managed more efficiently because there are less board configurations not requiring separate bins.

APPENDIX 1. MEMORY BOARD INTERCONNECT SPACE LAYOUT

Register Number	Register Description	Format	Global Access	Local Access	Default Value			
					312	310	320	340
Header Record								
0 (00H)	Vendor ID, Low Byte	Binary	R/O	R/O	01H	01H	01H	01H
1 (01H)	Vendor ID, High Byte	Binary	R/O	R/O	00H	00H	00H	00H
2 (02H)	Board ID, character 1	ASCII	R/O	R/O	4DH	4DH	4DH	4DH
3 (03H)	Board ID, character 2	ASCII	R/O	R/O	45H	45H	45H	45H
4 (04H)	Board ID, character 3	ASCII	R/O	R/O	4DH	4DH	4DH	4DH
5 (05H)	Board ID, character 4	ASCII	R/O	R/O	2FH	2FH	2FH	2FH
6 (06H)	Board ID, character 5	ASCII	R/O	R/O	33H	33H	33H	33H
7 (07H)	Board ID, character 6	ASCII	R/O	R/O	31H	31H	32H	34H
8 (08H)	Board ID, character 7	ASCII	R/O	R/O	32H	30H	30H	30H
9 (09H)	Board ID, character 8	ASCII	R/O	R/O	00H	00H	00H	00H
10 (0AH)	Board ID, character 9	ASCII	R/O	R/O	00H	00H	00H	00H
11 (0BH)	Board ID, character 10	ASCII	R/O	R/O	00H	00H	00H	00H
12 (0CH)	Intel Reserved	BCD +	R/O	R/O	†	†	†	†
13 (0DH)	Intel Reserved	BCD +	R/O	R/O	†	†	†	†
14 (0EH)	Intel Reserved	BCD +	R/O	R/O	†	†	†	†
15 (0FH)	Intel Reserved	BCD +	R/O	R/O	†	†	†	†
16 (10H)	Hardware Test Revision #	BCD +	R/O	R/O	†	†	†	†
17 (11H)	Class ID	Binary	R/O	R/O	13H	13H	13H	13H
18 (12H)	RFU	Binary	R/O	R/O	00H	00H	00H	00H
19 (13H)	RFU	Binary	R/O	R/O	00H	00H	00H	00H
20 (14H)	RFU	Binary	R/O	R/O	00H	00H	00H	00H
21 (15H)	RFU	Binary	R/O	R/O	00H	00H	00H	00H
22 (16H)	RFU	Binary	R/O	R/O	00H	00H	00H	00H
23 (17H)	RFU	Binary	R/O	R/O	00H	00H	00H	00H
24 (18H)	General Status	Binary	R/O	R/O	00H	00H	00H	00H
25 (19H)	General Control	Binary	R/W	R/W	00H	00H	00H	00H
26 (1AH)	BIST-SUPPORT-LEVEL ††	Binary	R/O	R/W	01H	01H	01H	01H
27 (1BH)	BIST-DATA-IN	Binary	R/W	R/W	00H	00H	00H	00H
28 (1CH)	BIST-DATA-OUT ††	Binary	R/O	R/W	00H	00H	00H	00H
29 (1DH)	BIST-SLAVE-STATUS ††	Binary	R/O	R/W	00H	00H	00H	00H
30 (1EH)	BIST-MASTER-SLAVE	Binary	R/W	R/W	20H	20H	20H	20H
31 (1FH)	BIST-TEST-ID ††	Binary	R/O	R/W	00H	00H	00H	00H
Protection Record								
32 (20H)	Protection Record Type	Binary	R/O	R/O	0BH	0BH	0BH	0BH
33 (21H)	Record Length	Binary	R/O	R/O	02H	02H	02H	02H
34 (22H)	Protection Level Register	Binary	R/O	R/W	00H	00H	00H	00H
35 (23H)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H

APPENDIX 1. MEMORY BOARD INTERCONNECT SPACE LAYOUT (Con't)

Register Number	Register Description	Format	Global Access	Local Access	Default Value			
					312	310	320	340
Memory Record								
36 (24H)	Memory Record Type	Binary	R/O	R/O	01H	01H	01H	01H
37 (25H)	Record Length	Binary	R/O	R/O	05H	05H	05H	05H
38 (26H)	Memory Size — 1 low byte	Binary	R/O	R/O	07H	0FH	1FH	3FH
39 (27H)	Memory Size — 1 high byte	Binary	R/O	R/O	00H	00H	00H	00H
40 (28H)	Memory Control Register	Binary	R/W	R/W	01H	01H	01H	01H
41 (29H)	Memory Status Register	Binary	R/O	R/O	A1H	A1H	A1H	A1H
42 (2AH)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H
iPSB Control Board								
43 (2BH)	iPSB Control Record Type	Binary	R/O	R/O	06H	06H	06H	06H
44 (2CH)	Record Length	Binary	R/O	R/O	06H	06H	06H	06H
45 (2DH)	iPSB Slot ID	Binary	R/O	R/O	FFH	FFH	FFH	FFH
46 (2EH)	iPSB Arbitration ID	Binary	R/W	R/W	00H	00H	00H	00H
47 (2FH)	iPSB Error Register	Binary	R/W	R/W	00H	00H	00H	00H
48 (30H)	iPSB Control/Status Register	Binary	R/W	R/W	00H	00H	00H	00H
49 (31H)	iPSB Diagnostic Register	Binary	R/W	R/W	00H	00H	00H	00H
50 (32H)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H
iPSB Memory Record								
51 (33H)	iPSB Memory Record Type	Binary	R/O	R/O	02H	02H	02H	02H
52 (34H)	Record Length	Binary	R/O	R/O	05H	05H	05H	05H
53 (35H)	*iPSB Start Address low byte*	*Binary*	*R/W*	*R/W*	*FFH*	*FFH*	*FFH*	*FFH*
54 (36H)	*iPSB Start Address high byte*	*Binary*	*R/W*	*R/W*	*FFH*	*FFH*	*FFH*	*FFH*
55 (37H)	*iPSB End Address low byte*	*Binary*	*R/W*	*R/W*	*00H*	*00H*	*00H*	*00H*
56 (38H)	*iPSB End Address high byte*	*Binary*	*R/W*	*R/W*	*00H*	*00H*	*00H*	*00H*
57 (39H)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H
iLBX™ II Memory Board								
58 (3AH)	iLBX II Memory Record Type	Binary	R/O	R/O	03H	03H	03H	03H
59 (3BH)	Record Length	Binary	R/O	R/O	07H	07H	07H	07H
60 (3CH)	*iLBX II Start Address low byte*	*Binary*	*R/W*	*R/W*	*FFH*	*FFH*	*FFH*	*FFH*
61 (3DH)	*iLBX II Start Address high byte*	*Binary*	*R/W*	*R/W*	*03H*	*03H*	*03H*	*03H*
62 (3EH)	*iLBX II End Address low byte*	*Binary*	*R/W*	*R/W*	*00H*	*00H*	*00H*	*00H*
63 (3FH)	*iLBX II End Address high byte*	*Binary*	*R/W*	*R/W*	*00H*	*00H*	*00H*	*00H*
64 (40H)	*iLBX II Clock Frequency*	*Binary*	*R/W*	*R/W*	*DCH*	*DCH*	*DCH*	*DCH*
65 (41H)	iLBX II Slot ID	Binary	R/O	R/O	00H	00H	00H	00H
66 (42H)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H

APPENDIX 1. MEMORY BOARD INTERCONNECT SPACE LAYOUT (Con't)

Register Number	Register Description	Format	Global Access	Local Access	Default Value			
					312	310	320	340
Memory Parity Record								
67 (43H)	Memory Parity Record Type	Binary	R/O	R/O	04H	04H	04H	04H
68 (44H)	Record Length	Binary	R/O	R/O	08H	08H	08H	08H
69 (45H)	Parity Control Register	Binary	R/W	R/W	03H	03H	03H	03H
70 (46H)	Parity Status Register	Binary	R/O	R/O	00H	00H	00H	00H
71 (47H)	Bank Status Register	Binary	R/O	R/O	00H	00H	00H	00H
72 (48H)	Error Offset byte 0	Binary	R/O	R/O	00H	00H	00H	00H
73 (49H)	Error Offset byte 1	Binary	R/O	R/O	00H	00H	00H	00H
74 (4AH)	Error Offset byte 2	Binary	R/O	R/O	00H	00H	00H	00H
75 (4BH)	Error Offset byte 3	Binary	R/O	R/O	00H	00H	00H	00H
76 (4CH)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H
Cache Memory Board								
77 (4DH)	Cache Memory Record Type	Binary	R/O	R/O	05H	05H	05H	05H
78 (4EH)	Record Length	Binary	R/O	R/O	05H	05H	05H	05H
79 (4FH)	Cache Size — 1 low byte	Binary	R/O	R/O	1FH	1FH	1FH	1FH
80 (50H)	Cache Size — 1 high byte	Binary	R/O	R/O	00H	00H	00H	00H
81 (51H)	Cache Entry Size — 1	Binary	R/O	R/O	03H	03H	03H	03H
82 (52H)	Cache Control Register	Binary	R/W	R/W	00H	00H	00H	00H
83 (53H)	Reserved for Future Use	Binary	R/O	R/O	00H	00H	00H	00H
End of Template Record								
84 (54H)	EOT Record Type	Binary	R/O	R/O	FFH	FFH	FFH	FFH

Note:

† These registers are defined for Intel's use. The values in these registers are dependent upon the revision of the board and are subject to change.

†† The BIST_DATA_OUT and the BIST_SLAVE_STATUS registers are R/W registers locally. However, the Test Handler that resides on the iSBC® MEM/3XX board does not allow off-board writes to these registers.

††† BCD+ has the same encoding as a normal BCD signal except that 0FH denotes a null, and the remaining unused encodings are reserved.

†††† The registers indicated with the *italicized type* are the nine registers that *must* be programmed before the board can operate in a system. Refer to the Configuration Sequence section for more information.

R/O = READ/ONLY
R/W = READ/WRITE
DEFAULT VALUE = POWER UP DEFAULT

MESSAGE PASSING IN THE MULTIBUS® II ARCHITECTURE

The demand for increased functionality and processing power in microcomputer systems is growing faster than single-processor solutions can satisfy. Multiprocessing, which allocates individual microprocessors to different functions within a system, has proven to be a viable solution, largely because of the advent of inexpensive memory and CPUs. Today, multiprocessing is highly evident in computers where microprocessors are found not only on general-purpose CPU boards, but on intelligent disk controller boards, communication boards, and other specialized boards.

To build multiprocessor computer systems, a designer selects a set of boards that solves his application requirements. The system bus is the vehicle for connecting the boards together and the medium through which intelligent boards communicate. Unfortunately, until now, conventional buses have not addressed this communication need with the idea of improving system performance and reducing complexity.

The MULTIBUS® II architecture employs an innovative mechanism called message passing to improve performance and simplify the implementation of multiprocessing computer systems. This product brief will discuss message passing and the benefits it brings to system design.

Functional Partitioning and Microprocessor Communications

There are two general types of multiprocessing: one that employs transparent multiprocessing in a tightly coupled system architecture and another that uses a heterogeneous mix of processors in a loosely coupled architecture (Figure 1).

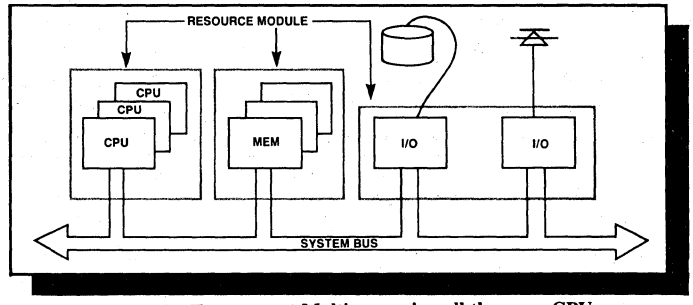


Figure 1A. Transparent Multiprocessing all the same CPUs

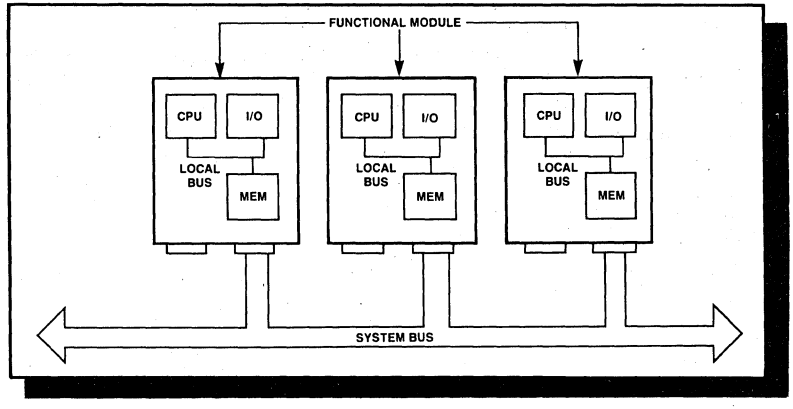


Figure 1B. Heterogenous Mix of Processors-Different Processors Selected to Satisfy Different Aspects of an Application

A functionally partitioned system is characterized by the use of a separate CPU and memory on a board with an optimized local environment. Other boards communicate via an interface which is independent of the implementation of the board. Therefore, future enhancements in the functional module can be easily integrated without redesigning the entire system. Also, since I/O, CPU, and memory technology evolve at different rates, a functionally partitioned system can be upgraded as technology allows, so the system integrator's products stay on the technological treadmill.

Key to the success of a functionally partitioned system is the mechanism for communication between the various functions. The MULTIBUS II message-passing feature was designed to resolve the problems of communication in multiprocessing systems by providing a unique approach to intermodule interrupts and data movement. In addition, the MULTIBUS II solution can be implemented in a single coprocessor device that augments the CPU, providing a cost-effective solution as well.

Solving the N x N Interrupt Problem

In traditional systems, interrupts are propagated via discrete interrupt lines. To get n processors to signal one another unambiguously, the bus needs $n \times (n-1)$ interrupt lines (this phenomenon is called the N×N problem). Since existing buses usually provide 7 or 8 interrupt lines, multiple sources of interrupts are assigned to a line, and the interrupted processor must poll to determine the source.

In contrast, the MULTIBUS II architecture uses message passing in a virtual interrupt scheme to resolve N×N problems as well as to facilitate the more complex feature of intertask communications required for a multitasking operating system. A virtual interrupt is a message that contains a destination and a source address and two bytes of qualifying information (Figure 2). In addition, up to 28 bytes of user data can be included in the interrupt. The entire message is sent as one packet on the system bus at the 40-megabyte-per-second maximum bus rate.

When the entire process of interrupt signaling is evaluated, including the software involved, sending a virtual interrupt with user data can be faster than an interrupt line approach.

Data Sharing

Traditionally, processors share data on a bus through a common memory area. This memory area is either globally available or a dual-port into one of the processors' local memories. There are several performance issues with these approaches.

First, it is necessary for one or both of the processors to use the system bus to reach the memory. When a processor uses the bus, it typically incurs an arbitration delay and the possibility of having to wait for other bus users to complete their activities.

In a dual-port approach, only one processor incurs the bus delay. However, the local processor performance is adversely affected by two factors. The first is the dual-port control logic. The second is contention from the processor accessing the local memory through the dual-port from the system bus.

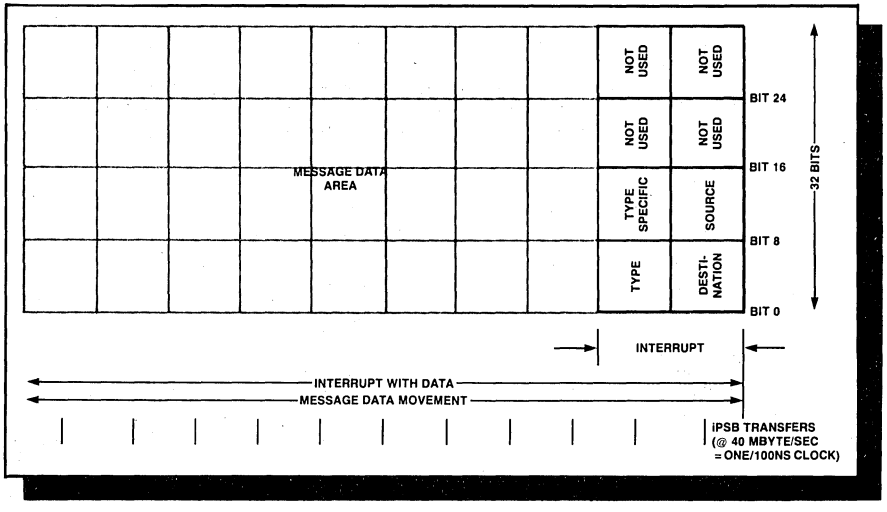


Figure 2. Message Format-Virtual Interrupt is First Two Transfers with Optional Data

In the MULTIBUS II architecture, the mechanism for moving data from one board to another is built into the MULTIBUS II bus interface hardware. The component which supports the requirements of message passing is referred to as the message passing coprocessor (MPC). A pair of MPC devices, one on each communicating intelligent board, moves the data from one board to another. Figure 3 shows a typical message-passing system with a host CPU and a disk controller using MPC devices to communicate.

For systems where the data to be shared is small and infrequently accessed, the performance impact may be trivial. However, as shared data needs increase, the CPUs pay a noticeable penalty. At this point, the system bus can also become a bottleneck. When systems software is required to coordinate and communicate the location of the shared memory, performance can further degrade. Finally, shared memory designs are also wasteful of bus bandwidth, complicated to debug, and are not easily extensible to beyond a single pair of communicating CPUs.

The MULTIBUS® II Solution

The ideal shared data system would have one CPU signal to another that it has data to share, followed by it becoming available to the second processor within its local memory. An example might be a disk system with a program or a set of data that a second processor spends a large portion of its time accessing. Getting the program or data quickly into the local memory of the second CPU is the key to achieving a performance improvement.

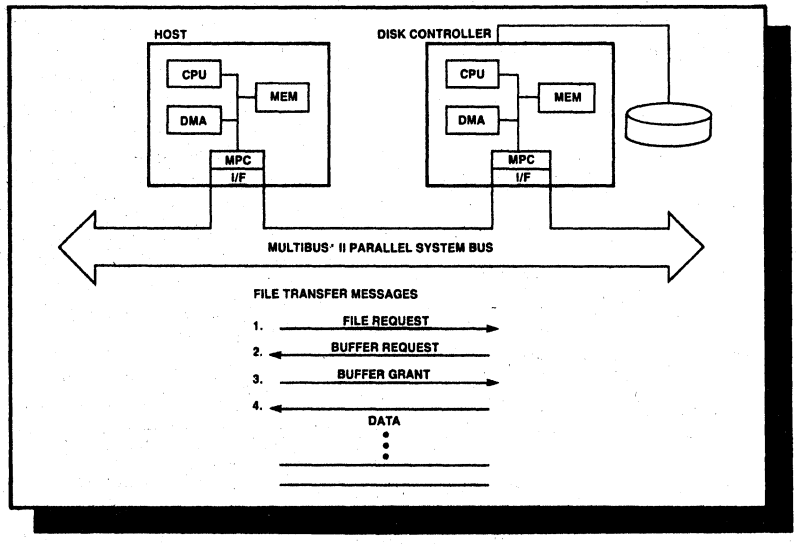


Figure 3. File Transfer Using Messages

In this example, the following is the sequence of events that occurs when the host desires a file:

1. The host requests the file using an interrupt message that uses the data field to describe the file.
2. The disk controller responds back to the host after retrieving the file with a request for memory.
3. The data is then arranged into 32-byte packets, and each packet is transmitted over the bus until all the data is at the host. The transfer is then complete.

The packets that are communicating and moving data between the MPC devices are transferring data at maximum bus bandwidths — 40 megabytes per second or 100ns per 32 bits. This constitutes a significant performance improvement, over traditional global memory and dual-port memory transfers.

By comparing this rate of data movement with today's VLSI devices, 40 megabytes/second is about five times as fast as the fastest microprocessor devices. The MPC performs a speed-matching function between the bus and the

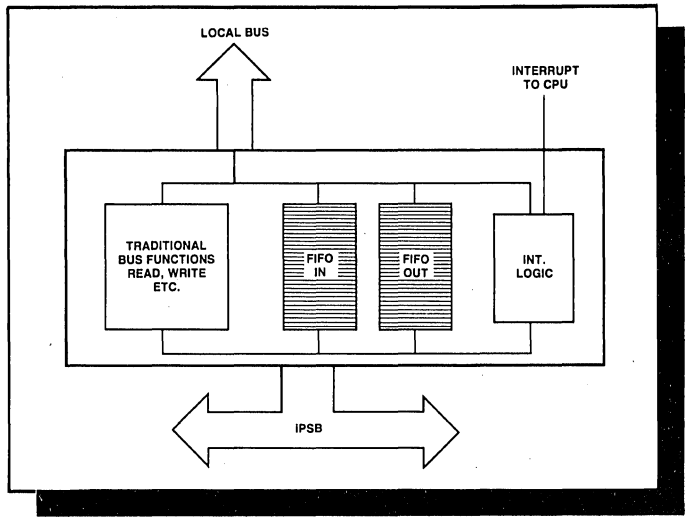


Figure 4. Message Passing Coprocessor Dataflow

local microprocessor environment. Between the system bus and the local bus, first-in first-out memories perform the speed matching. Figure 4 shows the data flow in an MPC device.

Data messages are broken into 32-byte packets because of the speed difference between the bus and the data rate that can be supported on a board. Since even the fastest microprocessor DMA devices cannot keep pace with these data rates, and real-time performance is affected if the packets are too large, it is advantageous to break a large data movement into small pieces and let the bus interface reconnect the pieces.

A 32-byte message packet only takes one microsecond of bus time (2-cycle header plus 8 cycles data × 100 ns/cycle). This allows other boards to use the bus between the packets that make up a large data movement. Also, the system bus is not tied up for long periods of time when large data movements occur. For real-time applications, interrupts may be sent without having to wait for a long data transfer to complete.

Examining the Performance Benefits

A closer look at the example in Figure 3 shows the impact message passing has on system performance. Note that during the disk file request and transfer, neither CPU has to access the bus. The interrupt-like messages that request and set up the transfer as well as the transfer itself all occur through the MPC. When the MPC sends a message, message, it is packetized and moved at 40 megabytes per second over the iPSB bus. As a result, any bus overhead is paid only once per interrupt message or once per 32 bytes of the data transfer.

In addition, the CPUs never pay a penalty for arbitration or contention on the bus, nor does either CPU incur any performance penalties associated with dual port memory operation. The wait states that a CPU would traditionally incur are either greatly reduced or eliminated. Furthermore, if the boards in our example have a local DMA device, the CPUs are free to perform other tasks while the transfer is occurring.

One final point — it is important to understand that the MULTIBUS II architecture also supports the traditional methods of communication such as dual-port and global memories. Message passing is an incremental capability.

Summary

The original design goals for message passing were to provide a performance enhancement and make it easier to implement multiprocessing systems. The achievement of these goals have resulted in the following benefits: message passing has solved the N×N interrupt problem; it has provided a high-performance solution to functionally partitioned systems; and finally, MULTIBUS II message passing can be implemented in a single-chip solution, thereby providing a cost-effective answer for today's system design.

iSBX™ Expansion Modules 16

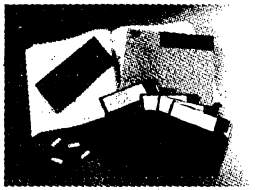
iSBX™ 279 DISPLAY SUBSYSTEM

HIGH-SPEED GRAPHICS/WINDOWING FOR iRMX® II SYSTEMS

The iSBX 279 is a complete graphics subsystem designed to provide users of Intel's iRMX II real-time systems with advanced interactive graphics functions. Based on Intel's 82786 Display Processor, the iSBX 279 efficiently off-loads bitmap and window manipulation from the application CPU, preserving real-time system performance. High-speed windowing, ASCII terminal emulation with system console support, and powerful drawing commands are provided in a convenient system expansion package. Complete software support, including iRMX II Device Driver, Application Interface Libraries for C-286 and PL/M 286, and loadable fonts, provides a high-level, network transparent interface, allowing application portability across Intel's real-time platforms and shortening application development time.

FEATURES:

- Intel 82786 Display Processor
- iRMX II Operating System Device Driver
- High-Level Language Interface
- System Console Support Kits
- Windowed User Interface
- Terminal Emulator
- Standard Graphics Command Interpreter
- Network Transparent Graphics Protocol



intel

The iSBX 279 Display Subsystem

September, 1988

Order Number: 280667-001

FEATURES

INTEL 82786 DISPLAY PROCESSOR

The Intel 82786 Display Processor is used to provide nearly instantaneous window manipulation. Together with the iSBX 279 firmware and iRMX II software, this allows multiple overlapping windows displaying graphical information or terminal sessions to be presented simultaneously.

iRMX II OPERATING SYSTEM DEVICE DRIVER

The iRMX II Interactive Configuration Utility provides the screens needed to configure the iSBX 279. The device driver is provided as part of the iSBX 279 upgrade kit. The device driver manages the device interface and performs I/O on behalf of application requests through device/file connections in the iRMX II IOS. The device driver is compatible with iRMX II Terminal Support. This speeds development by allowing the programmer to remain unaware of the device interface, instead concentrating on the application code needed for the target system.

HIGH-LEVEL LANGUAGE INTERFACE

Application interface libraries are provided for C-286 and PL/M 286. The application interface is a rich set of graphics and windowing primitives that provide standard drawing functions with complete control of bitmaps and windows. This allows the application programmer to quickly begin writing sophisticated real-time graphics applications using a portable interface for iRMX II systems.

SYSTEM CONSOLE SUPPORT KITS

The iSBX 279 is designed to be the system console for iRMX II MULTIBUS® systems based on iSBC® 286/1X and iSBC 386/XX CPU's. EPROM's containing System Confidence Tests, System Debug Monitor, and Bootstrap Loader are provided to allow the iSBX 279 to operate as a system console.

WINDOWED USER INTERFACE

The user may interactively MOVE, RESIZE, PUSH, POP, and SELECT windows using the mouse and an easy-to-use menu provided for this purpose. Several terminal sessions and interactive graphics applications can be managed from a single console. Window and bitmap manipulation is performed locally by the iSBX 279, allowing complex user-interface operations to proceed in parallel with time-critical real-time tasks on the host-CPU.

TERMINAL EMULATOR

The terminal emulator allows existing applications to run in a window without modification. The terminal emulator is compatible with the iRMX II Human Interface, the AEDIT text editor, iRMX Virtual Terminal software, and other terminal oriented programs that can be configured to operate with a smart CRT. By using the virtual terminal capability, it is possible to access any host on an OpenNET™ network from a single display.

STANDARD GRAPHICS COMMAND INTERPRETER

The graphics command interpreter is an implementation of the Computer Graphics Interface (CGI), providing an interface that is consistent with current ISO-CGM and ANSI-CGI standardization efforts, while extending this interface to include window and bitmap manipulation functions. The interface is fully compatible with Intel's existing iVDI 720 R1.8 interface providing a direct upgrade for iSBC 186/78A applications.

NETWORK TRANSPARENT GRAPHICS PROTOCOL

Using OpenNET it is possible to display images stored on remote nodes, run interactive applications from any node on the network, allow multiple applications on several processors to share a single display, and access other displays from a local application processor. Network transparency allows distributed applications to be controlled from a single console.

INTEL QUALITY AND RELIABILITY

The components of the iSBX 279 subsystem are designed and manufactured in accordance with Intel's high quality standards. Quality is assured through rigorous testing in our state-of-the-art Environmental Testing Laboratory.

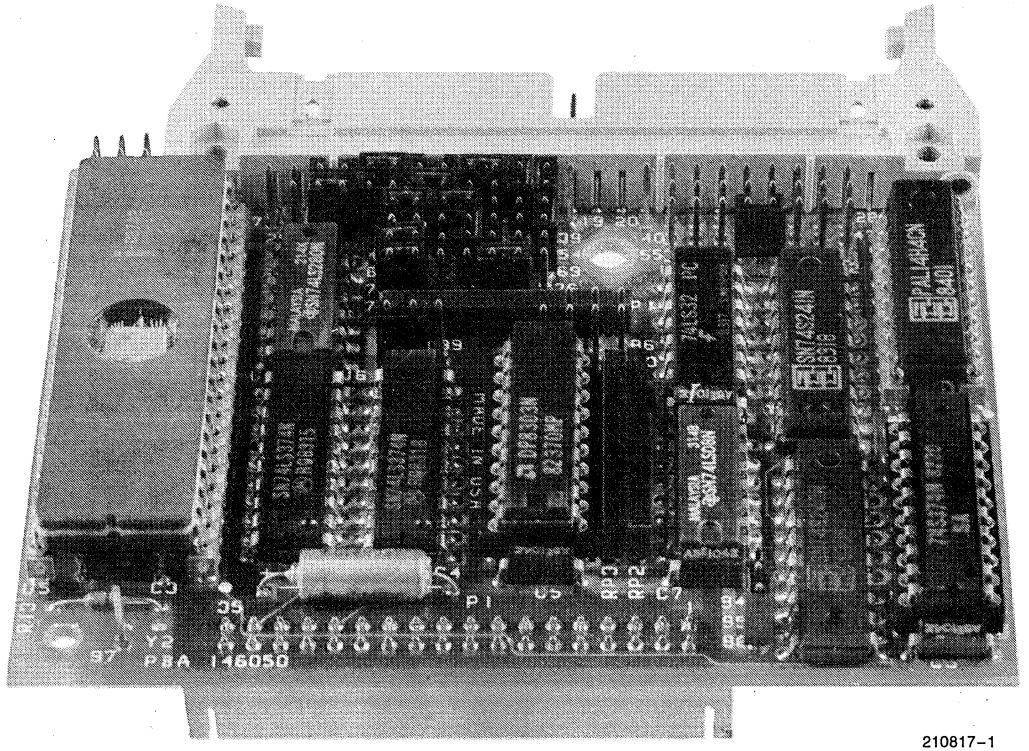
WORLDWIDE SERVICE AND SUPPORT

Intel provides support for repair or on-site service. Development support options include phone support, subscription service, on-site consulting, and customer training.

iSBX™ 217C ¼-INCH TAPE DRIVE INTERFACE MULTIMODULE™ BOARD

- **iSBX™ MULTIMODULE™ Interface Provides Tape Backup Capability for iSBC® 215 Generic Winchester Controller**
- **Configurable to Interface with up to Four QIC-02 Compatible or 3M HCD-75 Compatible Tape Drives**
- **Implements the QIC-02 with Parity Streaming Tape Interface Standard**
- **Supports Transfer Rates of 90K, 30K or 17K Bytes per Second Depending on Tape Speed**
- **Supported by iRMX™ 86 and XENIX* Operating Systems when Used on iSBC® 215 Generic Winchester Controller Board**
- **+5 Volt Only Operation**

The iSBX 217C ¼-Inch Tape Drive Interface module is a member of Intel's family of iSBX bus compatible MULTIMODULE products. iSBX MULTIMODULE boards plug directly onto any iSBX bus compatible host board, offering incremental on-board I/O expansion. The module is particularly useful for implementing cartridge tape back-up capability directly on the iSBC 215 Generic Winchester Disk Controller via DMA. The iSBX 217C board can also provide a low-cost tape storage interface for any Intel single board computer, with an iSBX connector, via programmed I/O. The iSBX 217C module interfaces with up to four streaming tape drives. Typically, these drives provide 20 to 45 megabytes of storage each. When used in conjunction with these drives and the iSBX 215 board, the module can transfer 20 megabytes of data from disk to tape in about fourteen minutes. Alternatively, the iSBX 217C board can interface with up to four 3M Company HCD-75 compatible start/stop tape drives, for those applications requiring access to individual data files on tape.



210817-1

*XENIX™ is a trademark of Microsoft Corporation.

October 1986
Order Number: 210817-002

FUNCTIONAL DESCRIPTION

The iSBX 217C module implements an interface between a host iSBC board and a cartridge ¼-inch magnetic tape drive, with a minimum of host software overhead. Data transfers may occur in either a direct memory access (DMA) or programmed I/O mode. The DMA mode is available only with host iSBC boards which have DMA capability. In both modes, the host must be able to transfer data at a rate of 90K, 30K or 17K bytes per second, depending on the speed of the tape drive.

Communication with the iSBC® Host

A command plus one-to-five parameter bytes are issued by the host iSBC board to the iSBX 217C module to initiate any tape interface operation. Commands for the QIC-02 and 3M interfaces are summarized in Table 1. If the function is a Read or a Write operation, the host must then be ready to transfer data a byte at a time to or from the module. In programmed I/O mode, with QIC-02 drives, the host polls the iSBX 217C status port to learn when the tape interface is ready for the next 512 byte data block. During the data block transfer, the host is interrupted by MWAIT/ when the interface is ready to transfer a data byte. With 3M tape drives, the host may be interrupted or use MDRQT to detect when the module is ready for the next byte transfer. In DMA mode, the host board uses the DMA Request signal (MDRQT) of the iSBX bus to synchronize the data transfer. At the conclusion of a tape operation, the iSBC host must read one or more of the iSBX 217C module's Sense Bytes to receive status information on the completed opeation. When the iSBX 217C module is used on the iSBC 215 Generic Winchester Controller board, these host requirements are fulfilled by the standard on-board firmware and are transparent to the user.

Table 1. Commands required by QIC-02 and 3M tape drives. Number indicates the parameter bytes required by the command. N indicates the command is not supported by the drive.

Hex Code	Command	Parameter Bytes		Type of Command
		QIC-2	3M	
00	Reset iSBX 217C Board	1	1	a
01	Initialize Drive	1	1	a
02	Write A Block	1	3	b
03	Write a File Mark	1	1	a
04	Read a Block	1	3	b
05	Read File Mark Command	1	N	a
06	Read Status	1	1	a
07	Rewind	1	N	a
08	Retension	1	N	a
09	Erase Tape	1	N	a
0C	Unload Tape	N	1	a
14	Continue	N	1	a
15	Write RAM	N	5	b
16	Read RAM	N	5	b
17	Verify	N	5	a
18	Run Selftest 1	1	N	a
1A	Read Extended Status	1	N	a
1B	Set Alternate Select Mode	1	N	a
1C	Return Raw Drive Status	1	N	a
20	Reset Bad Parity Flag	0	N	c
40	Start of Transfer (SOT)	1	1	c
80	End of Transfer (EOT)	1	1	c
81	Pause Command	1	N	c
82	Please Pause Command	1	N	c

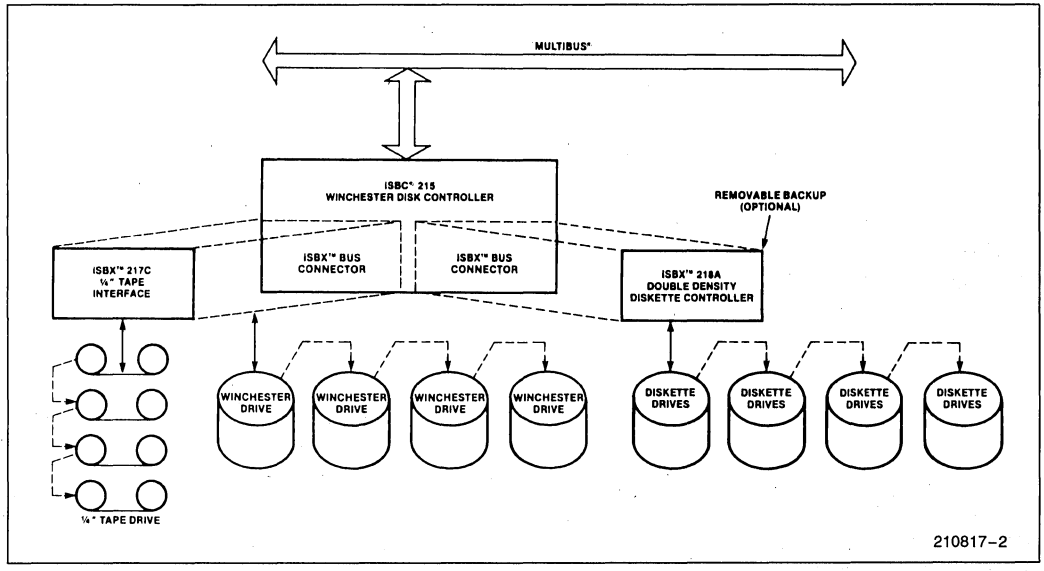


Figure 1. Subsystem Configuration (with optional Diskette and ¼" Tape Backup)

SPECIFICATIONS

Compatibility

Host—Any iSBC signal board computer or peripheral controller with an iSBX connector. The iSBC 215 Generic Winchester Controller includes on-board firmware to support the iSBX 217C under either the iRMX 86 or XENIX Operating Systems. The firmware on the iSBC 215A and iSBX 215B Winchester Controllers cannot support the iSBX 217C module.

Drives—Any QIC-02 or 3M HCD-75 interface compatible cartridge ¼-inch magnetic tape drive.

Transfer Rate

90K (one byte every 11 microseconds), 30K (one byte every 33 microseconds) or 17K (one byte every 53 microseconds) depending on tape drive speed.

Equipment Supplied

iSBX 217C Interface Module
Reference Schematic

Controller-to-drive cabling and connectors are not supplied. Cables can be fabricated with flat cable and commercially-available connectors as described in the Hardware Reference Manual.

Nylon mounting bolts

Physical Characteristics

Width: 3.08 inches (7.82 cm)
Height: 0.809 inches (2.05 cm)
Length: 3.70 inches (9.40 cm)
Shipping Weight: 3.5 ounces (99.2 gm)
Mounting: Occupies one single-wide iSBC MULTIMODULE position on boards

Electrical Characteristics

Power Requirements: +5 VDC @ 1.5A

Environmental Characteristics

Temperature: 0°C to +55°C (operating) @200 LFM; −55°C to +85°C (non operating)

Humidity: Up to 90% relative humidity without condensation (operating); all conditions without condensation or frost (non-operating)

Reference Manual

D146704-001— iSBX 217C Board Hardware Reference Manual (NOT SUPPLIED)

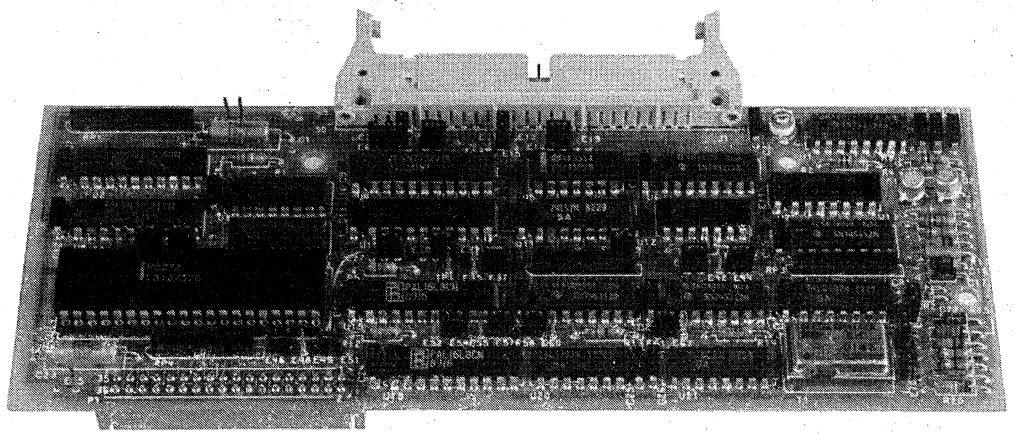
ORDERING INFORMATION

Part Number	Description
SBX 217C	Cartridge ¼-inch Tape Drive Interface

iSBX™ 218A
FLEXIBLE DISK CONTROLLER

- **iSBX™ Bus Compatible 8″ or 5.25″ Floppy Diskette Controller Module**
- **Hardware and Software Compatible with iSBX 218 Module**
- **Controls Most Single/Double Density and Single/Double Sided Floppy Drives**
- **User Programmable Drive Parameters Allow Wide Choice of Drives**
- **Motor On/Off Latch Under Program Control**
- **Drive-Ready Timeout Circuit for 5.25 Inch Floppy Drives**
- **Phase Lock Loop Data Separator Assures Data Integrity**
- **Read and Write on Single or Multiple Sectors**
- **Single +5 Volt Supply Required**

The Intel iSBX 218A Flexible Disk Controller module is a software and hardware compatible replacement for the iSBX 218 module and provides additional features. The iSBX 218A module is a double-wide iSBX module floppy disk controller capable of supporting virtually any soft-sectored, single/double density and single/double sided floppy drives. The controller can control up to four drives. In addition to the standard IBM 3740 and IBM system 34 formats, the controller supports sector lengths up to 8192 bytes. The iSBX 218A module's wide range of drive compatibility is achieved without compromising performance. The operating characteristics are specified under user control. The controller can read and write either single or multiple sectors.



503810-1

October 1986
Order Number: 503810-002

FUNCTIONAL DESCRIPTION

Intel's 8272 floppy Disk Controller (FDC) chip is the heart of the iSBX 218A Controller. On-board data separation logic performs standard MFM (double density) and FM (single density) encoding and decoding, eliminating the need for external separation circuitry at the drive. Data transfers between the controller and memory are managed by the intelligent device on the host board (usually an Intel 8-bit or 16-bit CPU). A block diagram of the iSBX 218A Controller is shown in Figure 1.

Universal Drive and iSBX™ 218A Controller

Because the iSBX 218A Controller has universal drive compatibility, it can be used to control virtually any standard-or mini-sized diskette drive. Moreover, the iSBX 218A Controller fully supports the iSBX bus and can be used with any single board computer which provides this bus interface. Because the iSBX 218A Controller is programmable, its performance is not compromised by its universal drive compatibility. The track-to-track access, head-load, and head-unload characteristics of the selected drive model are program specified. Data may be organized in sectors up to 8192 bytes in length.

Interface Characteristics

The standard iSBX 218A Controller includes an Intel 8272 Floppy Disk Controller chip which supports up to four drives, single or double sided.

SIMPLIFIED INTERFACE—The cable between the iSBX 218A Controller and the drive(s) may be low cost, flat ribbon cable with mass termination connectors. The mechanical interface to the board

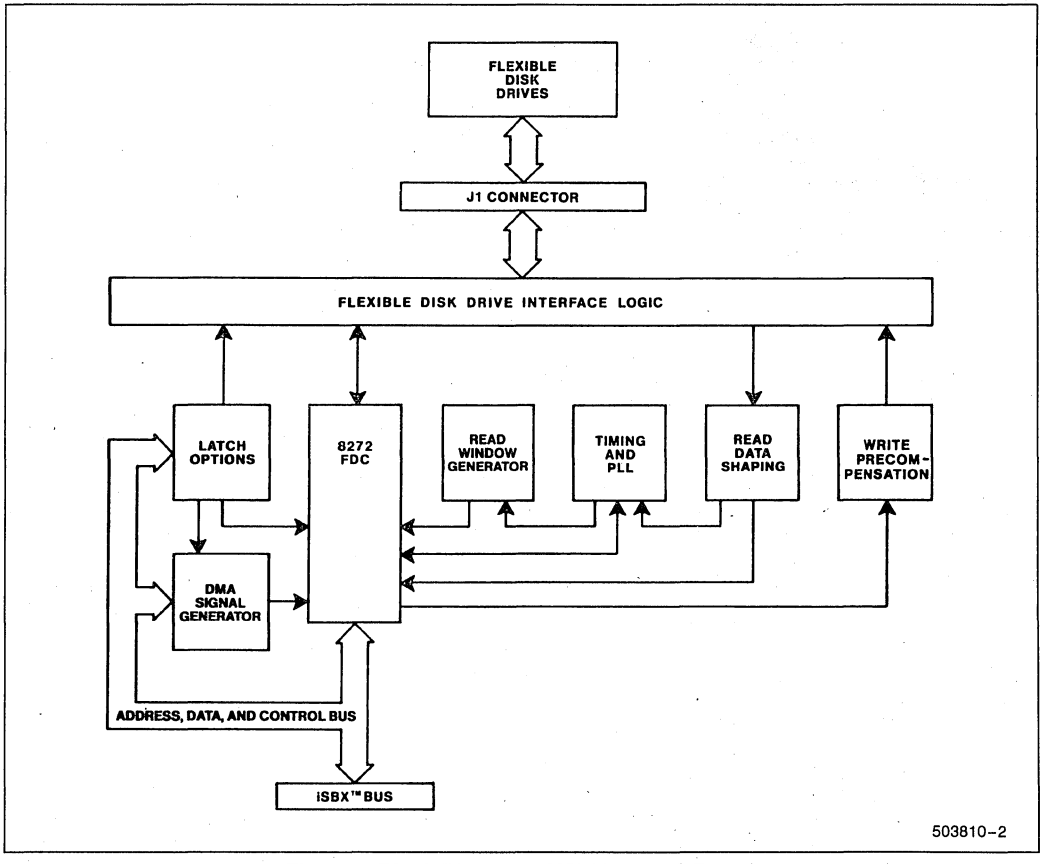


Figure 1. Block Diagram of iSBX™ 218A Board

is a right-angle header with locking tabs for security of connection.

PROGRAMMING—The powerful 8272 FDC circuit is capable of executing high-level commands that simplify system software development. The device can read and write both single and multiple sectors. CRC characters are generated and checked automatically. Recording density is selected at each Read and Write to support the industry standard technique of recording basic media information on Track 0 or Side 0 in single density, and then switching to double density (if necessary) for operations on other tracks.

PROGRAM INITIATION—All diskette operations are initiated by standard iSBX bus input/output (I/O) operations through the host board. System software first initializes the controller with the operating characteristics of the selected drive. The diskette is then formatted under program control. Data transfers occur in response to commands output by the CPU.

DATA TRANSFER—Once a diskette transfer operation has been initiated, the controller will require a data transfer every 13 microseconds (double density) or 26 microseconds (single density). Most CPUs will operate in a polled mode, checking controller status and transferring bytes when the controller is ready. Boards utilizing the Intel 8080 chip, such as the iSBC 80/10B board, will be restricted to single density operation with the iSBX 218A Controller, due to these speed requirements.

DMA OPERATION—The iSBX 218A module can be used either with or without a DMA controller on the host board. Standard DMA controllers provide a DACK (DMA Acknowledge) signal for proper DMA operation with the 8272. The iSBX 218A's on-board DACK generator provides the interface to allow the iSBX 218A module to be used with DMA controllers such as Intel's 8089 and 80186 processors that do not provide a DACK signal.

SPECIFICATIONS

Compatibility

CPU—Any single board computer or I/O board implementing the iSBX bus interface and connector.

Devices—Double or single density standard (8") and mini (5¼") flexible disk drives. The drives may be single or double sided. Drives known to be compatible are indicated in the table to the right.

Standard (8")		Mini (5¼")	
Caldisk	143M	Shugart	450/400
Remex	RFD 4000	Shugart	460/410
Memorex	550	Micropolis	1015-IV
MFE	700	Pertec	250
Siemens	FDD 200-8	Siemens	200-5
Shugart	SA 850/800	Tandon	TM-100
Shugart	SA 860/810	CDC	9409
Pertec	FD650	MPI	51/52/91/92
CDC	9406-3		

Data Organization and Capacity

Standard Size Drives

	Double Density						Single Density					
	IBM System 34			Non-IBM			IBM System 3740			Non-IBM		
Bytes per Sector	256	512	1024	2048	4096	8192	128	256	512	1024	2048	4096
Sectors per Track	26	15	8	4	2	1	26	15	8	4	2	1
Tracks per Diskette	77			77			77			77		
Bytes per Diskette (Formatted, per diskette surface)	512,512 (256 bytes/sector) 591,360 (512 bytes/sector) 630, 784 (1024 bytes/sector)			630,784			256,256 (128 byte/sector) 295,680 (256 bytes/sector) 315, 392 (512 bytes/sector)			315,392		

Diskette—Unformatted IBM Diskette 1 (or equivalent single-sided media); unformatted IBM Diskette 2D (or equivalent double-sided).

Equipment Supplied

iSBX 218A Controller

Reference Schematic

Controller-to-drive cabling and connectors are not supplied with the controller. Cables can be fabricated with flat cable and commercially-available connectors as described in the iSBX 218A Hardware Reference Manual.

Nylon Mounting Screws and Spacers

Physical Characteristics

Width: 3.15 inches (8.0 cm)

Height: 0.83 inches (2.1 cm)

Length: 7.5 ounces (19.1 cm)

Weight: 4.5 ounces (126 gm)

Mounting: Occupies one double-wide iSBX MULTIMODULE™ position on boards; increases board height (host plus iSBX board) to 1.13 inches (2.87 cm).

Electrical Characteristics

Power Requirements: +5VDC @ 1.7A max.

Environmental Characteristics

Temperature: 0°C to +55° (operating); −55°C to +85°C (non-operating).

Humidity: Up to 90% Relative Humidity without condensation (operating); all conditions without condensation or frost (non-operating).

Reference Manual

145911-001— iSBX 218A Flexible Disk Controller Hardware Reference Manual (NOT SUPPLIED).

Reference manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

Drive Characteristics

	Standard Size	Mini Size
	Double/Single Density	**Double/Single Density**
Transfer Rate (K bytes/sec)	62.5/31.25	31.25/15.63
Disk Speed (RPM)	360	300
Step Rate Time (Programmable)	1 to 16 ms/track in 1 ms increments	2 to 32 ms/track in 2 ms increments
Head Load Time (Programmable)	2 to 254 ms in 2 ms increments	4 to 508 ms in 4 ms increments
Head Unload Time (Programmable)	16 to 240 ms in 16 ms increments	32 to 480 ms in 32 ms increments

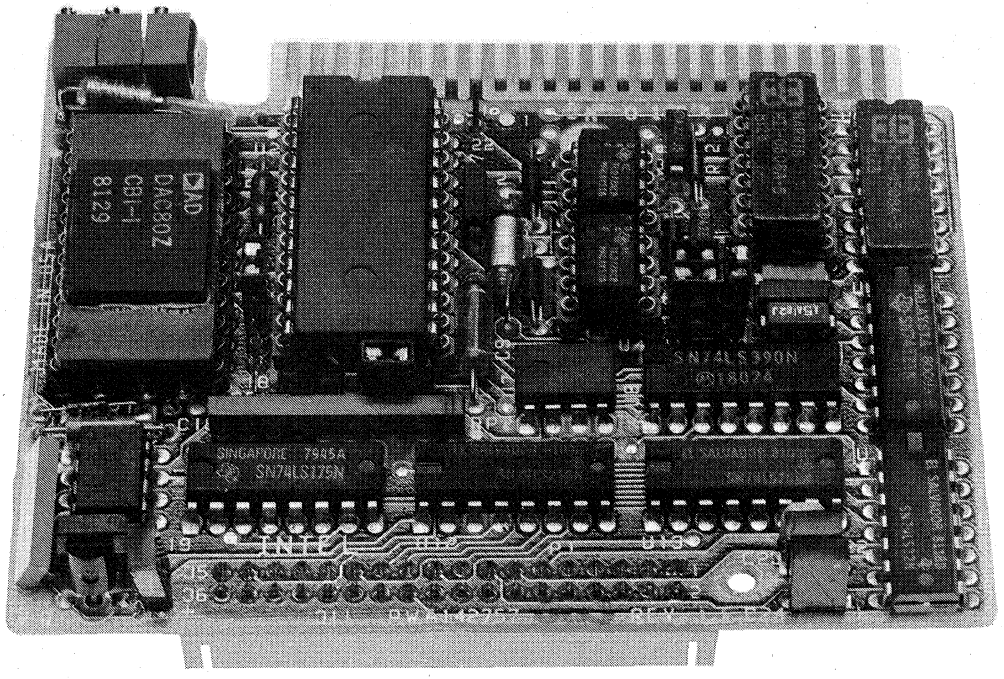
ORDERING INFORMATION

Part Number	Description
SBX 218A	Flexible Disk Controller

iSBX™ 311
ANALOG INPUT MULTIMODULE™ BOARD

- **Low Cost Analog Input Via iSBX™ MULTIMODULE™ Connector**
- **8 Differential/16 Single-Ended, Fault Protected Inputs**
- **20 mV to 5V Full Scale Input Range, Resistor Gain Selectable**
- **Unipolar (0 to +5V) or Bipolar (−5V to +5V) Input, Jumper Selectable**
- **12-Bit Resolution Analog-To-Digital Converter**
- **18 KHz Samples Per Second Throughput to Memory**

The Intel iSBX 311 Analog Input MULTIMODULE board provides simple interfacing of non-isolated analog signals to any iSBC board which has an iSBX compatible bus and connectors. The single-wide iSBX 311 plugs directly onto the iSBC board, providing data acquisition of analog signals from eight differential or sixteen single-ended voltage inputs, jumper selectable. Resistor gain selection is provided for both low level (20 mV full scale range) and high level (5 volt FSR) signals. Incorporating the latest high quality IC components, the iSBX 311 MULTIMODULE board provides 12 bit resolution, 11 bit accuracy, and a simple programming interface, all on a low cost iSBX MULTIMODULE board.



280233-1

October 1986
Order Number: 280233-002

FUNCTIONAL DESCRIPTION

The iSBX 311 Analog Input MULTIMODULE board is a member of Intel's growing family of MULTIMODULE expansion boards, designed to allow quick, easy, and inexpensive expansion for the Intel single board computer product line. The iSBX 311 Analog Input MULTIMODULE Board shown in Figure 1, is designed to operate with a variety of microcomputer modules that contains an iSBX bus connector (P1). The board provides 8 differential or 16 single-ended analog input channels that may be jumper-selected as the application requires. The MULTIMODULE board includes a user-configurable gain, and a user-selectable voltage input range (0 to +5 volts, or −5 to +5 volts). The MULTIMODULE board receives all power and control signals through the iSBX bus connector to initiate channel selection, sample and hold operation, and analog-to-digital conversion.

Input Capacity

Sixteen separate analog signals may be randomly or sequentially sampled in single-ended mode with the sixteen input multiplexers and a common ground. For noisier environments, differential input mode can be configured to achieve 8 separate differential signal inputs, or 16 pseudo-differential inputs.

Resolution

The iSBX 311 MULTIMODULES provide 12-bit resolution with a successive approximation analog-to-digital converter. For bipolar operation (−5 to +5 volts) it provides 11 bits plus sign.

Speed

To A-to-D converter conversion, speed is 35 microseconds (28 KHz samples per second). Combined with the sample and hold, settling times and the programming interface, maximum throughput via the iSBX bus and into memory will be 54 microseconds per sample, or 18 KHz samples per second, for a single channel, a random channel, or a sequential channel scan. A-to-D conversion is initiated via the iSBX connector and programmed command from the iSBC base board. Interrupt on end-of-conversion is a standard feature to ease programming and timing constraints.

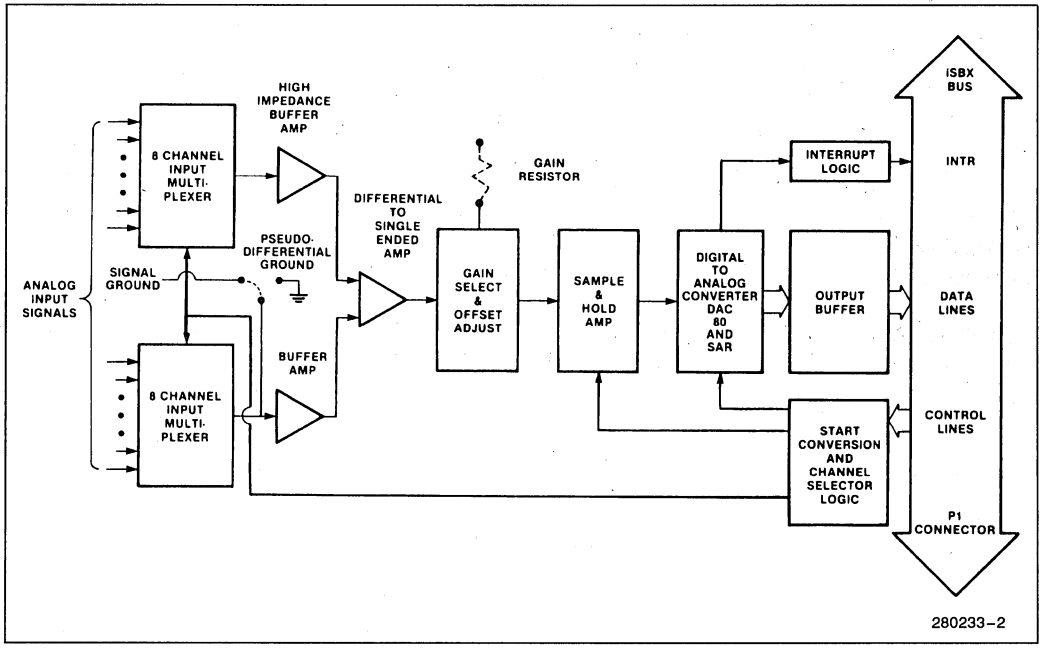


Figure 1. iSBX™ 311 Analog Input MULTIMODULE™ Board

Accuracy

High quality components are used to achieve 12 bits resolution and accuracy of 0.035% full scale range ±½ LSB. Offset and gain are adjustable to ±0.024% FSR ±½ LSB accuracy at any fixed temperature between 0°C (gain = 1). See specifications for other gain accuracies.

Gain

To allow sampling of millivolt level signals such as strain gauges and thermocouples, gain is made configurable via user inserted gain resistors up to 250 x (20 millivolts, full scale input range). User can select any other gain range from 1 to 250 to match his application.

OPERATIONAL DESCRIPTION

The host iSBC microcomputer addresses the iSBX 311 MULTIMODULE board by executing IN or OUT instructions to the iSBX 311 MULTIMODULE as one of the legal port addresses. Analog-to-digital conversions can be programmed in either of two modes: 1. start conversion and poll for end-of-conversion (EOC), or 2. start conversion and wait for interrupt (INTRO/) at end of conversion. When conversion is complete as signaled by one of the above techniques, INput instruction read two bytes (low and high bytes) containing the 12 bit data word plus status information as shown below.

OUTput Command—Select input channel and start conversion.

Bit Position	7	6	5	4	3	2	1	0
Input Channel					C3	C2	C1	C0

INput Data—Read converted data and status (low byte) or Read converted data (high byte). Reads can be with or without reset of interrupt request line (INTRO/).

Bit Position	7	6	5	4	3	2	1	0
Low/Status Byte	D3	D2	D1	D0		start/	busy/	EOC/

High Byte	D11	D10	D9	D8	D7	D6	D5	D4

Fastest data conversion and transfer to memory can be obtained by dedicating the microcomputer to setting the channel address/starting conversion, polling the status byte for EOC/, and when it comes true, read the two bytes of the conversion and send the start conversion/next channel address command. For multitasking situations it may be more convenient to use the interrupt mode, reading in data only after an interrupt signals end of conversion.

SPECIFICATIONS

Inputs—8 differential. 16 single-ended. Jumper selectable.

Full Scale Input
Voltage Range—−5 to +5 volts (bipolar). 0 to +5 volts (unipolar). Jumper selectable.

Gain—User-configurable through installation of two resistors. Factory-configured for gain of X1.

Resolution—12 bits over full scale range (1.22 mV at 0–5V, 5 μV at 0–20 mV).

Accuracy—

Gain	Accuracy at 25°C
1	±0.035% ± ½ LSB
5	±0.035% ± ½ LSB
50	±0.035% ± ½ LSB
250	±0.035% ± ½ LSB

NOTE:
Figures are in percent of full scale reading. At any fixed temperature between 0° and 60°C, the accuracy is adjustable to ±0.035% of full scale.

Dynamic Error—±0.015% FSR for transitions.

Gain TC (at Gain = 1): 30 PPM per degree centigrade (typical); 56 PPM per degree centigrade (max).

Offset TC (in percent of FSR/°C):

Gain	Offset
1	0.0018
5	0.0036
50	0.024
250	0.116

Offset is measured with user-supplied 10 PPM/°C gain resistors installed.

Input Protection—±30 volts.

Input Impedance—20 MΩ (minimum).

Conversion Speed—50 ms (nominal).

Common Mode Rejection Ratio—60 db (minimum).

Sample and hold—sample time 15 ms.

Aperture—hold aperture time: 120 ns.

Connectors—

Interface	Pins (Qty)	Centers		Mating Connectors
		in	cm	
P1 iSBX Bus	36	0.1	0.254	iSBC iSBX connector
J1 8/16 Channels Analog	50	0.1	0.254	3m 3415-000 or T1 H312125 or iCS 910 cable

Physical Characteristics

Width: 9.40 cm (3.7 inches)

Length: 6.35 cm (2.5 inches)

Height: 2.03 cm (0.80 inch) MULTIMODULE board only

2.82 cm (1.13 inches) MULTIMODULE and iSBC board

Weight: 68.05 gm (2.4 ounces)

Electrical Characteristics (from iSBX connector)

V_{cc} = ±5 volts (±0.25V), I_{cc} = 250 mAmax
V_{dd} = +12 volts (±0.6V), I_{dd} = 50 mAmax
V_{ss} = −12 volts (±0.6V), I_{ss} = 55 mAmax

Environmental Characteristics

Operating Temperature: 0° to 60°C (32° to 140°C)

Relative Humidity: to 90% (without condensation)

Reference Manuals

142913— iSBX 311 Analog Input MULTIMODULE Board Hardware Reference Manual (order separately)

Related Literature

230973—Distributed Control Data Book

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

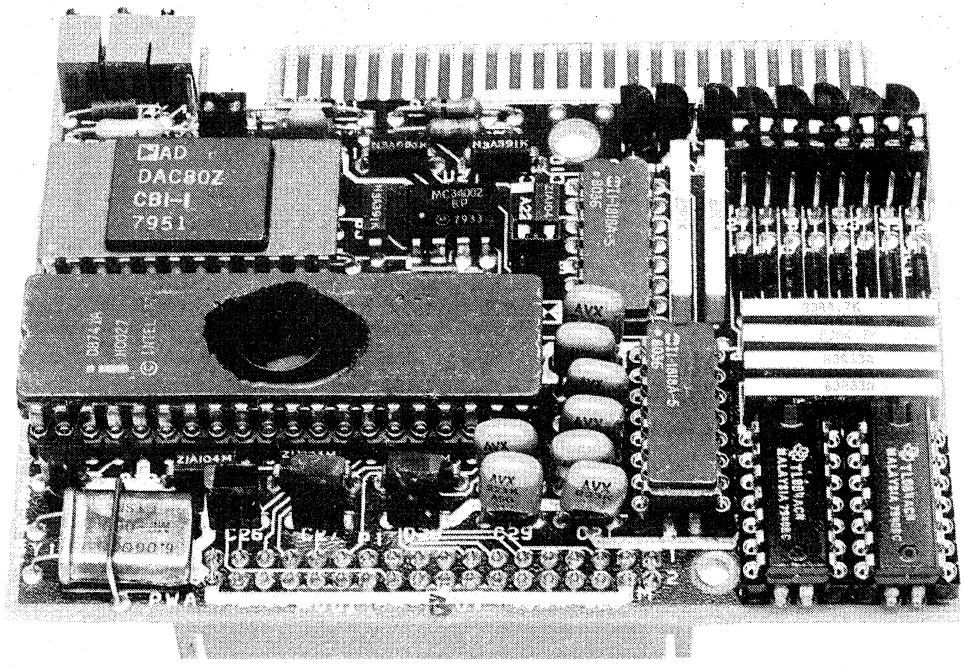
ORDERING INFORMATION

Part Number	Description
SXB 311	Analog Input MULTIMODULE Board

iSBX™ 328
ANALOG OUTPUT MULTIMODULE™ BOARD

- **Low Cost Analog Output Via iSBX™ MULTIMODULE™ Connector**
- **8 Channel Output, Current Loop or Voltage in any Mix**
- **4–20 mA Current Loop; 5V Unipolar or Bipolar Voltage Output**
- **12-Bit Resolution**
- **0.035% Full Scale Voltage Accuracy @ 25°C**
- **Programmable Offset Adjust in Current Loop Mode**

The Intel iSBX 328 MULTIMODULE board provides analog signal output for any intelligent board having an iSBX compatible bus and connector. The single-wide iSBX 328 plugs directly onto the host board, providing eight independent output channels of analog voltage for meters, programmable power supplies, etc. Voltage output can be mixed with current loop output for control of popular 4–20 mA industrial control elements. By using an Intel single chip computer (8041) for refreshing separate sample-hold amplifiers through a single 12 bit DAC, eight channels are contained on a single MULTIMODULE board for high density and low cost per channel. High quality analog components provide 12 bit resolution, and slew rates per channel of 0.1V per microsecond. Maximum channel update rates are 5 KHz on a single channel to 1 KHz on all eight channels.



280234-1

October 1986
Order Number: 280234-001

FUNCTIONAL DESCRIPTION

The iSBX 328 MULTIMODULE board, shown in Figure 1 is designed to plug onto any host iSBC microcomputer that contains an iSBX bus connector. The board uses an Intel 8041 microcontroller to manage eight analog output channels that may be user-configured through jumpers to operate in either bipolar voltage output mode (−5V to +5V), unipolar voltage output mode (0 to +5V), or current loop output mode (4 to 20 mA) applications. Channels may be individually wired for simultaneous operation in both current loop output and voltage output applications. The outputs feed to a 50-pin edge connector (J1) on the iSBX 328 MULTIMODULE board.

Interfacing through the Intel iSBX Bus

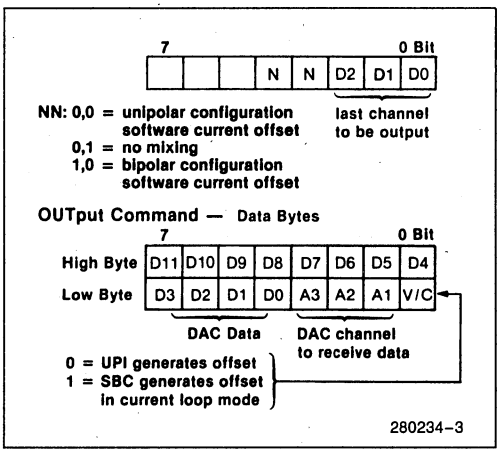
All data to be output through the MULTIMODULE board is transferred from the host microcomputer to the MULTIMODULE board via the iSBX bus connector. The iSBX 328 board accepts the binary digital data and generates a 12-bit data word for the Digital-to-Analog Converter (DAC) and a four bit channel decode/enable for selecting the output channel. The DAC transforms the data into analog signal outputs for either voltage output mode or current loop output mode. Offsetting of the DAC voltage in current output mode may be performed by the UPI software offset routine or by the hardware offset adjustments included on the board. The MULTIMODULE board status is available via the iSBX bus connector, to determine if the UPI is ready to receive updates to analog output channels.

OPERATIONAL DESCRIPTION

The host iSBC microcomputer addresses the MULTIMODULE board by executing IN or OUT instructions specifying the iSBX 328 MULTIMODULE as a port address. The iSBX 328 is initialized to select whether software or hardware offset is to be used and how many channels will be active. Then a 2 byte transfer to each active channel sets the 12 bit output value, the channel selected and the current or voltage mode.

Commands

OUTput Command—Initialization of UPI/iSBX 328



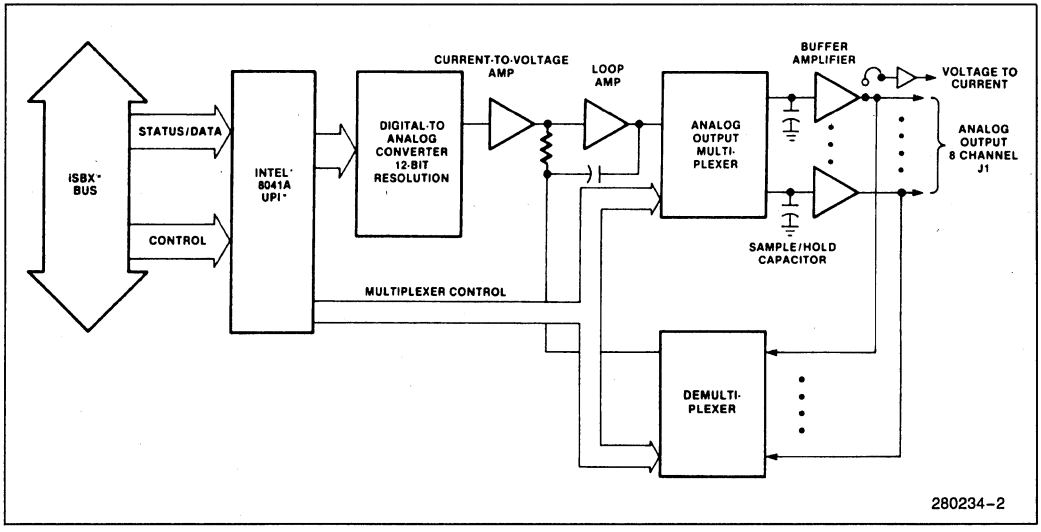
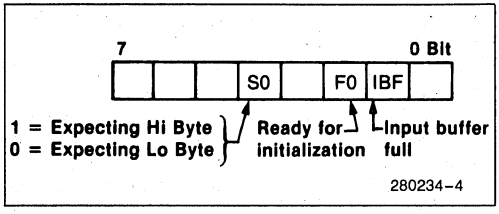


Figure 1. iSBC® 328 Analog Output MULTIMODULE™ Board Block Diagram

INput Command—Status Buffer Read



Interrupts

No interrupts are issued from the iSBX 328 to the host iSBC microcomputer. Data coordination is handled via iSBC software polls of the status buffer.

SPECIFICATIONS

Outputs — 8 non-isolated channels, each independently jumpered for voltage output or current loop output mode.

Voltage Ranges — 0 to +5V (unipolar operation) −5 to +5V (bipolar operation)

Current Loop Range — 4 to 20 mA (unipolar operation only)

Output Current — ±5 mA maximum (voltage mode-bipolar operation)

Load Resistance — 0 to 250Ω with on-board iSBX power. 1000Ω minimum with 30 VDC max. external supply

Compliance Voltage — 12V using on-board iSBX power. If supplied by user, up to 30 VDC max

Resolution — 12 bits bipolar or unipolar

Slew Rate — 0.1V per microsecond minimum

Single Channel Update Rate — 5 KHz

Eight Channel Update Rate — 1 KHz

Output Impedance — 0.1Ω. Drives capacitive loads up to 0.05 microfarads. (approx. 1000 foot cable)

Temperature Coefficient — 0.005%/°C

Refresh and Throughput Rates**	
Refresh 1 channel (no new data):	80 μs
Refresh all 8 channels (no new data):	650 μs
Update and refresh 1 channel with new data: firmware program 2	150 μs
for each additional channel	130 μs
Update and refresh 1 channel with new data: firmware program 1 or 3	200 μs
for each additional channel	155 μs
Update and refresh all 8 channels (all new data): firmware program 2	1,050 ms
per channel of new data	50 μs
Update and refresh all 8 channels (all new data): firmware program 1or 3	1,280 ms
per channel of new data	80 μs

**All times nominal

Accuracy—

Mode	Accuracy	Ambient Temp
Voltage-Unipolar, typical	± 0.025% FSR	@ 25°C
Voltage-Unipolar, maximum	± 0.035% FSR	@ 25°C
Voltage-Unipolar, typical	± 0.08% FSR	@ 0° to 60°C
Voltage-Unipolar, maximum	± 0.19% FSR	@ 0° to 60°C
Voltage-Bipolar, typical	± 0.025% FSR	@ 25°C
Voltage-Bipolar, maximum	± 0.035% FSR	@ 25°C
Voltage-Bipolar, typical	± 0.09% FSR	@ 0° to 60°C
Voltage-Bipolar, maximum	± 0.17% FSR	@ 0° to 60°C
Current Loop, typical	± 0.07% FSR	@ 25°C
Current Loop, maximum	± 0.08% FSR	@ 25°C
Current Loop, typical	± 0.17% FSR	@ 0° to 60°C
Current Loop, maximum	± 0.37% FSR	@ 0° to 60°C

Connectors—

Interface	Pins (Qty)	Centers in	Centers cm	Mating Connectors
P1 iSBX Bus	36	0.1	0.254	iSBC iSBX connector
J1 8/16 channels analog	50	0.1	0.254	3m 3415-000 or T1 H312125 or iCS 910 cable

Physical Characteristics

Width: 9.40 cm (3.7 inches)

Length: 6.35 cm (2.5 inches)

Height: 1.4 cm (0.56 inch) MULTIMODULE board only

2.82 cm (1.13 inches) MULTIMODULE and iSBC board.

Weight: 85.06 gm (3.0 ounces)

Electrical Characteristics

V_{CC} = ±5V (0.25V), I_{CC} = 140 mA max

V_{DD} = ±12V (±0.6V), I_{DD} = 45 mA max (voltage mode)

= 200 mA max (current loop mode

V_{SS} = −12V (±0.6V), I_{SS} = 55 mA max

Environmental Characteristics

Operating Temperature: 0° to 60°C (32° to 140°C)

Relative Humidity: to 90% (without condensation)

Reference Manuals

142914— iSBX 328 Analog Output MULTI-MODULE Board Hardware Reference Manual (Order Separately)

230973— Distributed Control Modules Databook

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

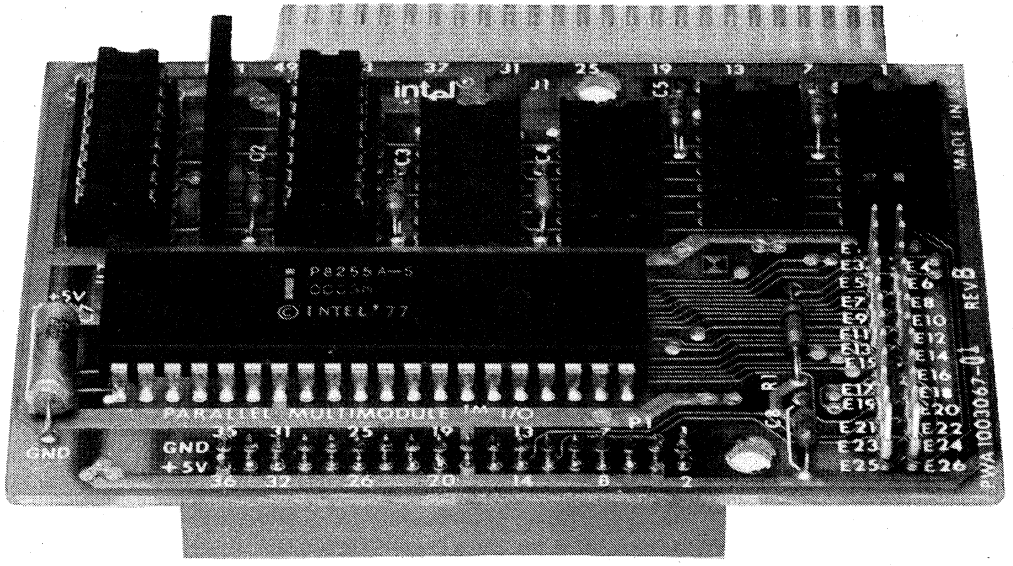
ORDERING INFORMATION

Part Number	Description
SBX 328	Analog Output MULTIMODULE Board

iSBX™ 350
PARALLEL I/O MULTIMODULE™ BOARD

- **iSBX™ Bus Compatible I/O Expansion**
- **24 Programmable I/O Lines with Sockets for Interchangeable Line Drivers and Terminators**
- **Three Jumper Selectable Interrupt Request Sources**
- **Accessed as I/O Port Locations**
- **Single +5V Low Power Requirement**
- **iSBX Bus On-Board Expansion Eliminates MULTIBUS® System Bus Latency and Increases System Throughput**

The Intel iSBX 350 Parallel I/O MULTIMODULE Board is a member of Intel's line of iSBX bus compatible MULTIMODULE products. The iSBX MULTIMODULE board plugs directly into any iSBX bus compatible host board offering incremental on-board expansion. The iSBX 350 module provides 24 programmable I/O lines with sockets for interchangeable line drivers and terminators. The iSBX board is closely coupled to the host board through the iSBX bus, and as such, offers maximum on-board performance and frees MULTIBUS system traffic for other system resources. In addition, incremental power dissipation is minimal requiring only 1.6 watts (not including optional driver/terminators).



280235-1

September 1986
Order Number: 280235-001

FUNCTIONAL DESCRIPTION

Programmable Interface

The iSBX 350 module uses an Intel 8255A-5 Programmable Peripheral Interface (PPI) providing 24 parallel I/O lines. The base-board system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the flexibility of the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and driver/termination characteristics for each application. In addition, inverting bidirectional bus drivers (8226) are provided on sockets to allow convenient optional replacement to non-inverting drivers (8216). The 24 programmable I/O lines, signal ground, and +5 volt power (jumper configurable) are brought to a 50-pin edge connector that mates with flat, woven, or round cable.

Interrupt Request Generation

Interrupt requests may originate from three jumper selectable sources. Two interrupt requests can be automatically generated by the PPI when a byte of information is ready to be transferred to the base board CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). A third interrupt source may originate directly from the user I/O interface (J1 connector).

Installation

The iSBX 350 module plugs directly into the female iSBX connector on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figure 1 and Figure 2).

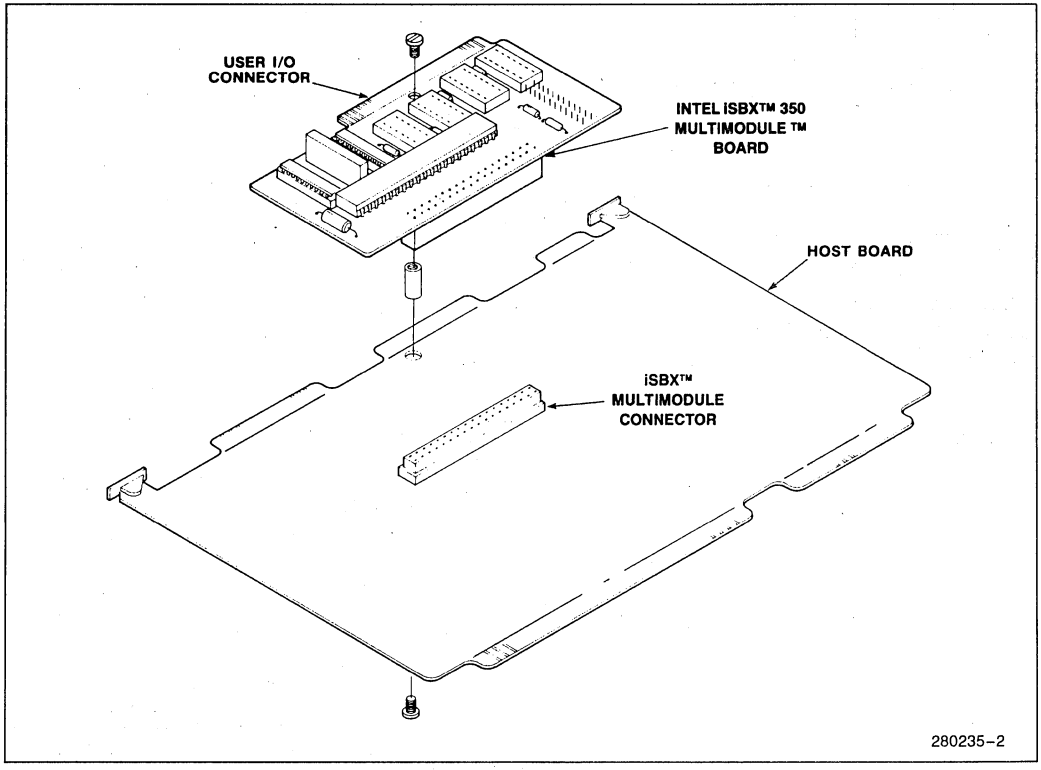


Figure 1. Installation of iSBX™ 350 Module on a Host Board

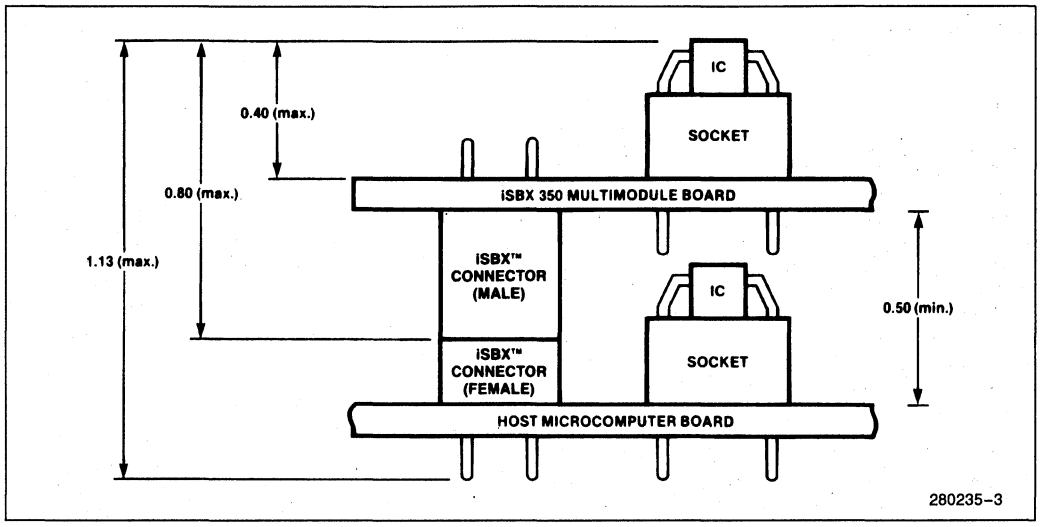


Figure 2. Mounting Clearances (inches)

Table 1. Input/Output Port Modes of Operation

Port	Lines (qty)	Mode of Operation					Control
		Unidirectional				Bidirectional	
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
A	8	X	X	X	X	X	
B	8	X	X	X	X		
C	4	X		X			X(1)
	4	X		X			X(1)

NOTE:
1. Part of Port C must be used as a control port when either Port A or Port B are used as a latched and strobed input or a latched and strobed output port or Port A is used as a bidirectional port.

SPECIFICATIONS

Word Size

Data: 8 Bits

I/O Addressing

8255A-5 Ports	iSBX 350 Address
Port A	X0 or X4
Port B	X1 or X5
Port C	X2 or X6
Control	X3 or X7
Reserved	X8 to XF

NOTE:
The first digit of each port I/O address is listed as "X" since it will change dependent on the type of host iSBC microcomputer used. Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the first digit of the port address.

I/O Capacity

24 programmable lines (see Table 1)

Access Time

Read: 250 ns max.

Write: 300 ns max.

NOTE:
Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Interrupts

Interrupt requests may originate from the programmable peripheral interface (2) or the user specified I/O (1).

Interfaces

iSBX™ Bus—All signals TTL compatible

Parallel I/O—All signals TTL compatible

Parallel Interface Connectors

Interface	No. of Pairs/ Pins	Centers (in.)	Connector Type	Vendor	Vendor Part No.
Parallel I/O Connector	25/50	0.1	Female	3M	3415-0001 with Ears
Parallel I/O Connector	25/50	0.1	Female Soldered	GTE Sylvania	6AD01251A1DD

NOTE:
Connector compatible with those listed may also be used.

Line Drivers and Teminators

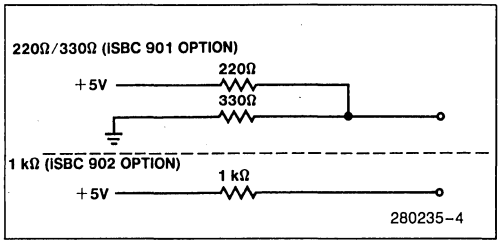
I/O Drivers—The following line drivers and terminators are all compatible with the I/O driver sockets on the iSBX 350.

Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

NOTE:
I = Inverting, NI = Non-Inverting, OC = Open Collector

Port 1 has 25 mA totem pole drivers and 1 kΩ terminators.

I/O Terminators—220Ω/330Ω divider or 1 kΩ pull up.



Physical Characteristics

Width: 7.24 cm (2.85 in.)

Length: 9.40 cm (3.70 in.)

Height*: 2.04 cm (0.80 in.) iSBX 350 Board

2.86 cm (1.13 in.) iSBX 350 Board + Host Board

Weight: 51 gm (1.79 oz)

*See Figure 2

Electrical Characteristics

DC Power Requirements

Power Requirements	Configuration
+5 @ 320 mA	Sockets XU3, XU4, XU5, and XU6 empty (as shipped).
+5V @ 500 mA	Sockets XU3, XU4, XU5, and XU6 contain 7438 buffers.
+5V @ 620 mA	Sockets XU3, XU4, XU5, and XU6 contain iSBC 901 termination devices.

Environmental

Operating Temperature: 0°C to +55°C

Reference Manual

9803191-01—iSBX 350 Parallel I/O MULTIMODULE Manual (NOT SUPPLIED)

Reference Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California 95051.

ORDERING INFORMATION

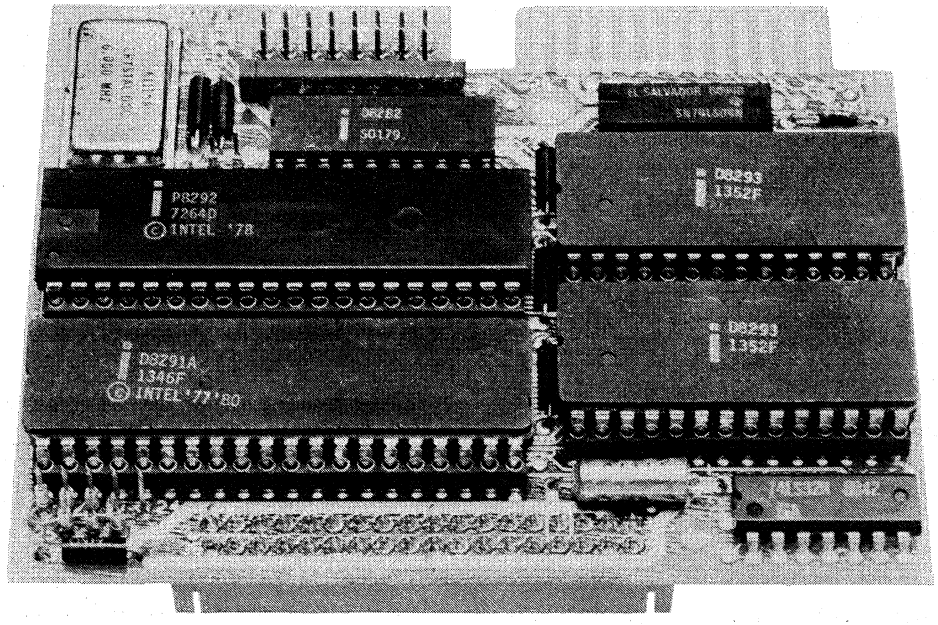
Part Number	Description
SBX 350	Parallel I/O MULTIMODULE Board

iSBX™ 488
GPIB MULTIMODULE™ BOARD

- **Complete IEEE 488-1978 Talker/ Listener Functions Including:**
  - **— Addressing, Handshake Protocol, Service Request, Serial and Parallel Polling Schemes**
- **Complete IEEE 488-1978 Controller Functions Including:**
  - **— Transfer Control, Service Requests and Remote Enable**
- **Simple Read/Write Programming**
- **Software Functions Built into VLSI Hardware for High Performance, Low Cost and Small Size**
- **Standard iSBX Bus Interface for Easy Connection to Intel iSBC™ Boards**
- **IEEE 488-1978 Standard Electrical Interface Transceivers**
- **Five Volt Only Operation**

The Intel iSBX 488 GPIB Talker/Listener/Controller MULTIMODULE board provides a standard interface from any Intel iSBC board equipped with an iSBX connector to over 600 instruments and computer peripherals that use the IEEE 488-1978 General Purpose Interface Bus. By taking full advantage of Intel's VLSI technology the single-wide iSBX 488 MULTIMODULE board implements the complete IEEE 488-1978 Standard Digital Interface for Programmable Instrumentation on a single low cost board. The iSBX 488 MULTIMODULE board includes the 8291A GPIB Talker/Listener, 8292 GPIB Controller and two 8293 GPIB Transceiver devices. This board represents a significant step forward in joining microcomputers and instrumentation using industry standards such as the MULTIBUS® system bus, iSBX bus and IEEE 488-1978. The high performance iSBX 488 MULTIMODULE board mounts easily on Intel iSBX bus compatible single board computers.

A simple user programming interface for easy reading, writing and monitoring of all GPIB functions is provided. This intelligent interface minimizes the impact on host processor bandwidth.



143580-1

October 1986
Order Number: 143580-001

FUNCTIONAL DESCRIPTION

The iSBX 488 MULTIMODULE board is a single-wide iSBX bus compatible I/O expansion board that provides a complete implementation of the IEEE 488-1978 Standard Digital Interface for Programmable Instrumentation. The iSBX 488 MULTIMODULE board may be configured to be a GPIB controller, talker, listener or talker/listener. The hardware implementation of the iSBX 488 board takes full advantage of Intel's VLSI capability by using the Intel 8292 GPIB controller, 8291A talker/listener and two (2) 8293 bus transceivers. All communication between the host iSBC board and the iSBX 488 MULTIMODULE board is executed via the Intel standard iSBX connector. Many of the functions that previously were performed by user software have been incorporated into VLSI hardware for high performance and simple programming. Both the Intel 8291A GPIB Talker/Listener device and the 8292 device can each communicate independently with the host processor on the iSBC board depending on configuration. Communication from the host iSBC board to either device on the iSBX 488 board is flexible and may be either interrupt or poll driven depending on user requirements. Data transfers to or from the GPIB may be executed by the host processor's I/O Read and I/O Write commands or with DMA handshaking techniques for very high speed transfers.

GPIB Talker/Listener Capabilities

The Intel 8291A device on the iSBX 488 MULTIMODULE board handles all talker/listener communications between the host iSBC processor board and the GPIB. Its capabilities include data transfer, bus handshake protocol, talker/listener addressing procedures, device clearing and triggering, service requests, and both serial and parallel polling schemes. In executing most procedures the iSBX 488 board does not interrupt the microprocessor on the iSBC processor board unless a byte of data is waiting on input or a byte is sent to an empty output buffer, thus offloading the host CPU of GPIB overhead chores.

SIMPLE PROGRAMMING INTERFACE

The GPIB talker/listener functions can be easily programmed using the high level commands made available by the Intel 8291A on the iSBX 488 MULTIMODULE board. The 8291A device architecture includes eight registers for input and eight registers for output. One each of these read and write registers is used for direct data transfers. The remaining write registers are used by the programmer to control the various interface features of the Intel 8291A device. The remaining read registers provide the user with a monitor of GPIB states, bus conditions and device status.

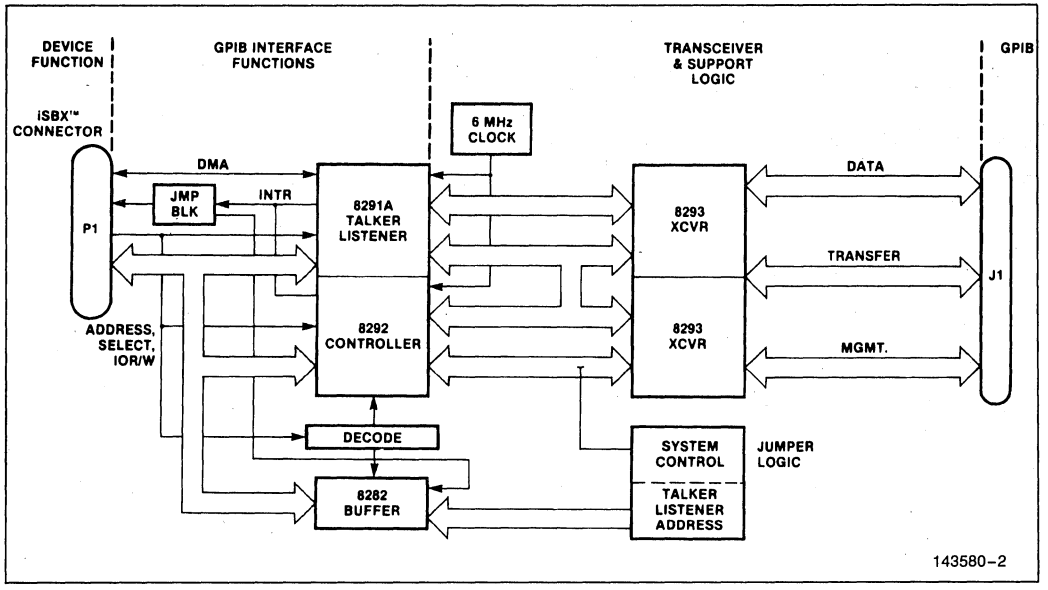


Figure 1. iSBX™ 488 MULTIMODULE™ Board Block Diagram

SOFTWARE FUNCTIONS BUILT INTO VLSI HARDWARE

Additional features that have migrated from discrete logic and software into Intel VLSI include programmable data transfer rate and three addressing modes that allow the iSBX board to be addressed as either a major or a minor talker/listener with primary or secondary addressing. The iSBX 488 MULTIMODULE board can be programmatically configured into almost any bus talker, listener, or talker/listener configuration. Writing software to control these and other iSBX 488 board functions is simply a matter of reading or writing the control registers.

IEEE 488-1978 Functions(1)

Function	ISBX™ 488 Supported IEEE Subsets
Source Handshake (SH)	SH0, SH1
Acceptor Handshake (AH)	AH0, AH1
Talker (T)	T0 through T8
Extended Talker (TE)	TE0 through TE8
Listener (L)	L0 through L4
Extended Listener (LE)	LE0 through LE9
Service Request (SR)	SR0, SR1
Remote Local (RL)	RL0, RL1
Parallel Poll (PP)	PP0, PP1, PP2
Device Clear (DC)	DC0 through DC2
Device Trigger (DT)	DT0, DT1
Controller (C)	C0 through C28

NOTE:
1. For detailed information refer to IEEE Standard Digital Interface for Programmable Instrumentation published by The Institute of Electrical and Electronics Engineers, Inc. 1978.

Controller Capabilities

The GPIB controller functions supplied by the iSBX 488 board are provided by the Intel 8292 GPIB controller device. The 8292 is actually an Intel 8041A eight bit microcomputer that has been preprogrammed to implement all IEEE 488-1978 controller functions. The internal RAM in the 8041A is used as a special purpose register bank for the 8292 GPIB Controller. Just as with the 8291A GPIB Talker/Listener device, these registers are used by the programmer to implement controller monitor, read and write commands on the GPIB.

When configured as a bus controller the iSBX 488 board will respond to Service Requests (SRQ) and will issue Serial Polls. Parallel Polls are also issued to multiple GPIB instrument devices for receiving simultaneous responses. In applications requiring multiple bus controllers, several iSBX 488 boards may each be configured as a controller and pass the active control amongst each other. An iSBX 488 board configured for a System Controller has the capability to send Remote Enable (REN) and Interface Clear (IFC) for initializing the bus to a known state.

GPIB Physical Interface

The iSBX 488 MULTIMODULE board interfaces to the GPIB using two Intel 8293 bidirectional transceivers. The iSBX 488 board meets or exceeds all of the electrical specifications defined in IEEE 488-1978 including bus termination specifications. In addition, for direct connection to the GPIB, the iSBC 988 cable, a 26 conductor 0.5 meter GPIB interface cable is also available from Intel. The cable is terminated with a 26-pin edge connector at the iSBX end and a 24-pin GPIB connector at the other. The cable is also supplied with shield lines for simple grounding in electrically noisy environments.

Installation

The iSBX 488 MULTIMODULE board plugs directly onto the female iSBX connector available on many Intel iSBC boards. The MULTIMODULE board is then secured at one additional point with nylon hardware (supplied) to insure the mechanical security of the assembly.

SPECIFICATIONS

Interface Information

iSBX™ Bus—All signals TTL compatible

26-pin Edge Connector—Electrical levels compatible with IEEE 488-1978.

Physical Characteristics

Width: 3.70 in (0.94 cm)
Length: 2.85 in (7.24 cm)
Height: 0.8 in (2.04 cm)
Weight: 3.1 oz (87.8 gm)

GPIB Data Rate*

300K bytes/sec transfer rate with DMA host iSBC board

50K bytes/s transfer rate using programmed I/O
730 ns Data Accept Time

*Data rates are iSBX board maximum. Data rates will vary and can be slower depending on host iSBC board and user software driver.

Electrical Characteristics

DC Power Requirements: V_{CC} = +5 VDC ±5%

I_{CC} = 600 milliamps maximum

GPIB Electrical and Mechanical Specifications

Conforms to IEEE 488-1978 standard electrical levels and mechanical connector standard when purchased with the iSBC 988 GPIB cable.

Environmental Characteristics

Operating Temperature: 0° to 60°C (32° to 140°F)

Relative Humidity: Up to 90% R.H. without condensation.

Reference Manual

143154-001— iSBX 488 GPIB MULTIMODULE Board Hardware Reference Manual (not supplied).

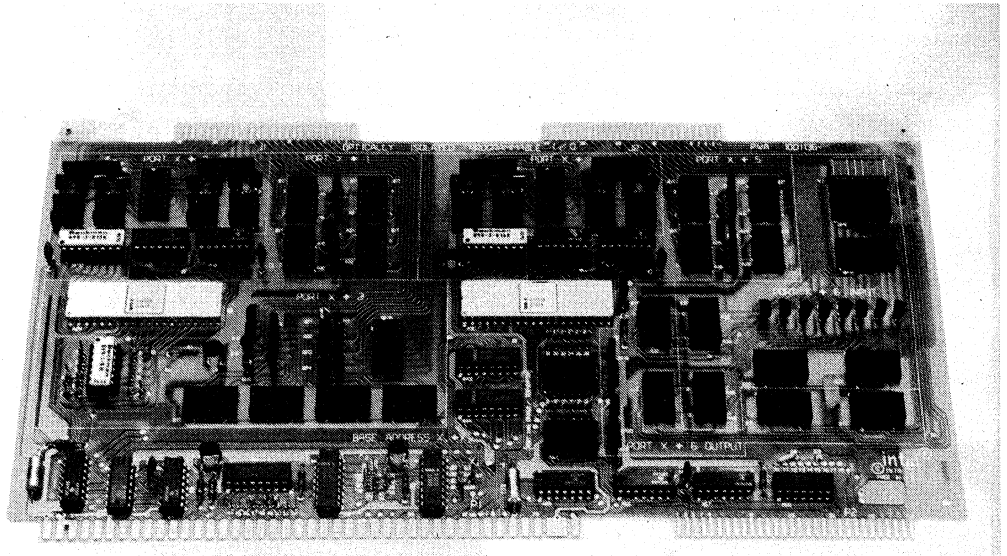
ORDERING INFORMATION

Part Number	Description
SBX488	GPIB MULTIMODULE
SBC988	0.5 meter GPIB cable for iSBX 488 MULTIMODULE Board

iSBC® 556
OPTICALLY ISOLATED I/O BOARD

- **Up to 48 Digital Optically Isolated Input/Output Data Lines for MULTIBUS® Systems**
- **Choice of**
  - **— 24 Fixed Input Lines**
  - **— 16 Fixed Output Lines**
  - **— 8 Programmable Lines**
- **Provisions for Plug-In, Optically Isolated Receivers, Drivers, and Terminators**
- **Voltage/Current Levels**
  - **— Input up to 48V**
  - **— Output up to 30V, 60 mA**
- **Common Interrupt for up to 8 Sources**
- **+5V Supply Only**

The iSBC 556 Optically Isolated I/O Board provides 48 digital input/output lines with isolation between process application or peripheral device and the system CPU board(s). The iSBC 556 contains two 8255A programmable interface devices, and sockets for user supplied optically isolated drivers, receivers, and input resistor terminators, together with common interrupt logic and interface circuitry for the system bus. Input signals can be single-ended or differential types with user defined input range (resistor terminator and opto-isolated receiver selection), allowing flexibility in design of voltage and threshold levels. The output allows user selection of Opto-Isolated Darlington Pair which can be used as an output driver either as an open collector or current switch.



280231-1

November 1986
Order Number: 280231-001

Table 1. I/O Ports Opto-Isolator Receivers, Drivers, and Terminators

Port No. X = I/O Base Address	Type of I/O	Lines (qty)	Resistor Terminator Pac-Rp 16-Pin DIP Bourns 4116R-00 or Equivalent	Dual Opto-Isolator 8-Pin DIP Monsanto MC T66 or Equivalent	Driver 7438 or Equivalent	Pull-Up iSBC® 902
X + 0	Input	8	1	4	—	
X + 1	Output	8	—		—	
X + 2	Input/ Control	8	1		—	
X + 4	Input	8	1	4	—	
X + 5	Output	8			—	
X + 6	Input/ Output	8	1 if input		2 if input	2 if input
X + 7	Control					

SPECIFICATIONS

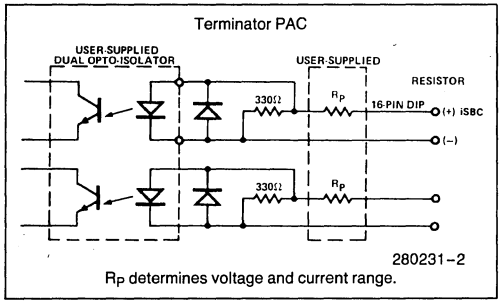
Number of Lines

24 input lines
16 output lines
8 programmable lines: 4 input — 4 output

I/O Interface Characteristics

Line-to-Line Isolation: 235V DC or peak AC

Input/Output Isolation: 500V DC or peak AC



RP determines voltage and current range.

Bus Interface Characteristics

All data address and control commands are iSBC 80 bus compatible.

I/O Addressing

Port	8255 #1			Control	8255 #2			Control
	A	B	C		A	B	C	
Address	X+0	X+1	X+2	X+3	X+4	X+5	X+6	X+7

Where: base address is from 00H to 1FH (jumper selectable)

Connectors

Interface	Pins qty.	Centers in.	Centers cm	Mating Connectors
P1 iSBC bus	86	0.156		Viking 3KH43/9AMK12
J1 16 fixed input & 8 fixed output lines	50	0.1		3M 3415-000 or TI M312125
J2 8 fixed input, 8 fixed output, & 8 program-mable input/ output lines	50	0.1		3M 3415-000 or TI M312125

Physical Characteristics

Width: 12.00 in. (30.48 cm)
Height: 6.75 in. (17.15 cm)
Depth: 0.50 in. (1.27 cm)
Weight: 12 oz. (397.3 gm)

Electrical Characteristics

Average DC Current

V_{CC} = +5V ±5%, 1.0A without user supplied isolated receiver/driver

I_{CC} = 1.6A max with user supplied isolator receiver/driver

Environmental Characteristics

Temperature: 0°C to 55°C

Relative Humidity: 0% to 90%, non-condensing

Reference Manual

502170— iSBC 556 Hardware Reference Manual (Order Separately)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

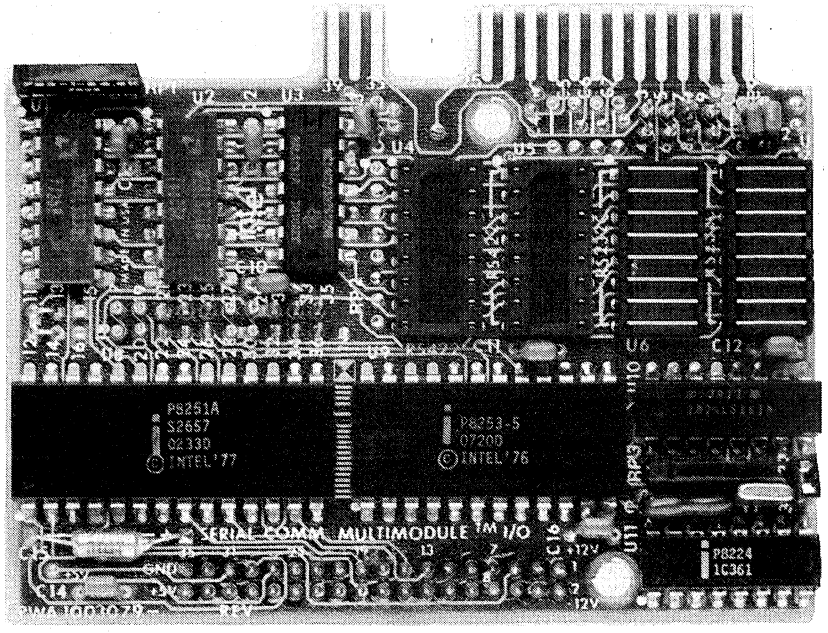
ORDERING INFORMATION

Part Number	Description
SBC 556	Optically Isolated I/O Board

iSBX™ 351
SERIAL I/O MULTIMODULE™ BOARD

- **iSBX™ Bus Compatible I/O Expansion**
- **Programmable Synchronous/ Asynchronous Communications Channel with RS232C or RS449/422 Interface**
- **Software Programmable Baud Rate Generator**
- **Two Programmable 16-Bit BCD or Binary Timer/Event Counters**
- **Four Jumper Selectable Interrupt Request Sources**
- **Accessed as I/O Port Locations**
- **Low Power Requirements**
- **Single +5V when Configured for RS449/422 Interface**
- **iSBX Bus On-Board Expansion Eliminates MULTIBUS® System Bus Latency and Increases System Throughput**

The Intel iSBX 351 Serial I/O MULTIMODULE board is a member of Intel's new line of iSBX bus compatible MULTIMODULE products. The iSBX MULTIMODULE board plugs directly into any iSBX bus compatible host board offering incremental on-board I/O expansion. The iSBX 351 module provides one RS232C or RS449/422 programmable synchronous/asynchronous communications channel with software selectable baud rates. Two general purpose programmable 16-bit BCD or binary timers/event counters are available to the host board to generate accurate time intervals under software control. The iSBX board is closely coupled to the host board through the iSBX bus, and as such, offers maximum on-board performance and frees MULTIBUS system traffic for other system resources. In addition, incremental power dissipation is minimal requiring only 3.0 watts (assumes RS232C interface).



280236–1

September 1986
Order Number: 280236-001

FUNCTIONAL DESCRIPTION

Communications Interface

The iSBX 351 module uses the Intel 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) providing one programmable communications channel. The USART can be programmed by the system software to individually select the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of operation (i.e., synchronous or asynchronous), data format, control character format, parity, and baud rate are all under program control. The 8251A provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The command lines, serial data lines, and signal ground lines are brought out to a double edge connector configurable for either an RS232C or RS449/422 interface (see Figure 3). In addition, the iSBX 351 module is jumper configurable for either point-to-point or multidrop network connection.

16-Bit Interval Timers

The iSBX 351 module uses an Intel 8253 Programmable Interval Timer (PIT) providing 3 fully programmable and independent BCD and binary 16-bit interval timers. One timer is available to the system designer to generate baud rates for the USART under software control. Routing for the outputs from the other two counters is jumper selectable to the host board. In utilizing the iSBX 351 module, the systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given baud rate or time delay is needed, software commands the programmable timers to select the desired function. The functions of the timers are shown in Table 1. The contents of each counter may be read at any time during system operation.

Interrupt Request Lines

Interrupt requests may originate from four sources. Two interrupt requests can be automatically generated by the USART when a character is ready to be transferred to the host board (i.e., receive buffer is full) or a character has been transmitted (i.e., transmit buffer is empty). In addition, two jumper selectable requests can be generated by the programmable timers.

Installation

The iSBX 351 module plugs directly into the female iSBX connector on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly (see Figures 1 and 2).

Table 1. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

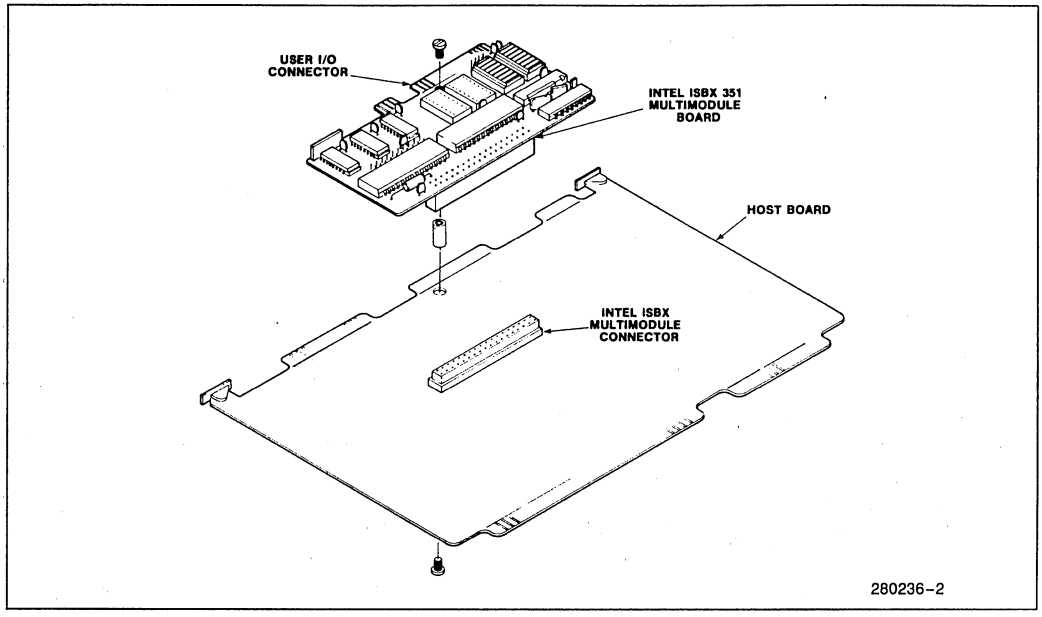


Figure 1. Installation of iSBC® 351 Module on a Host Board

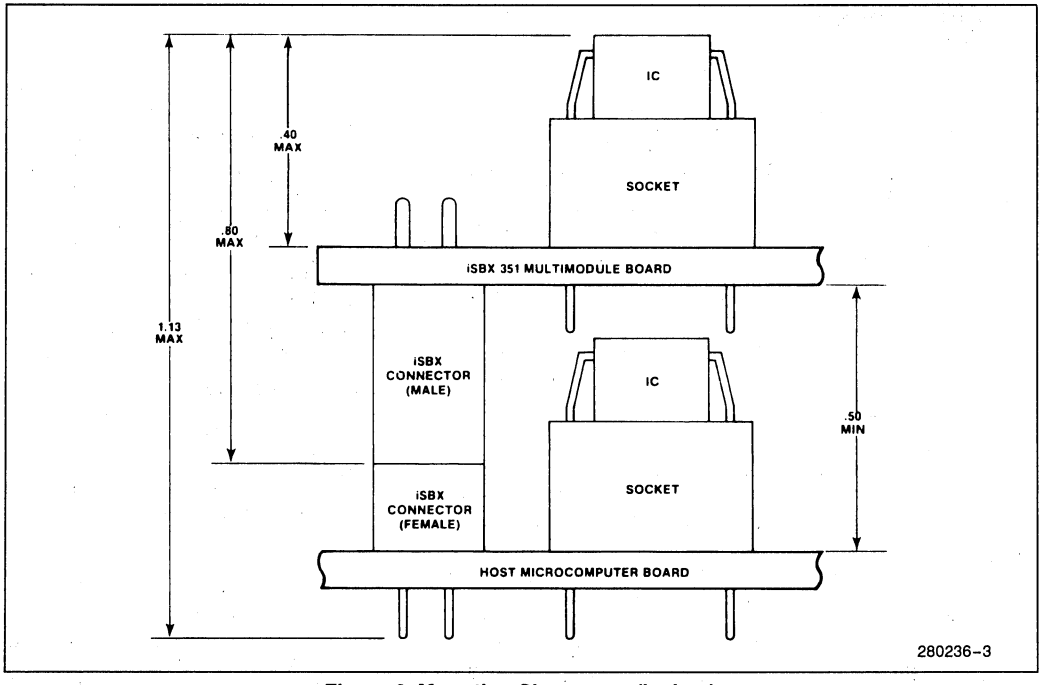


Figure 2. Mounting Clearances (inches)

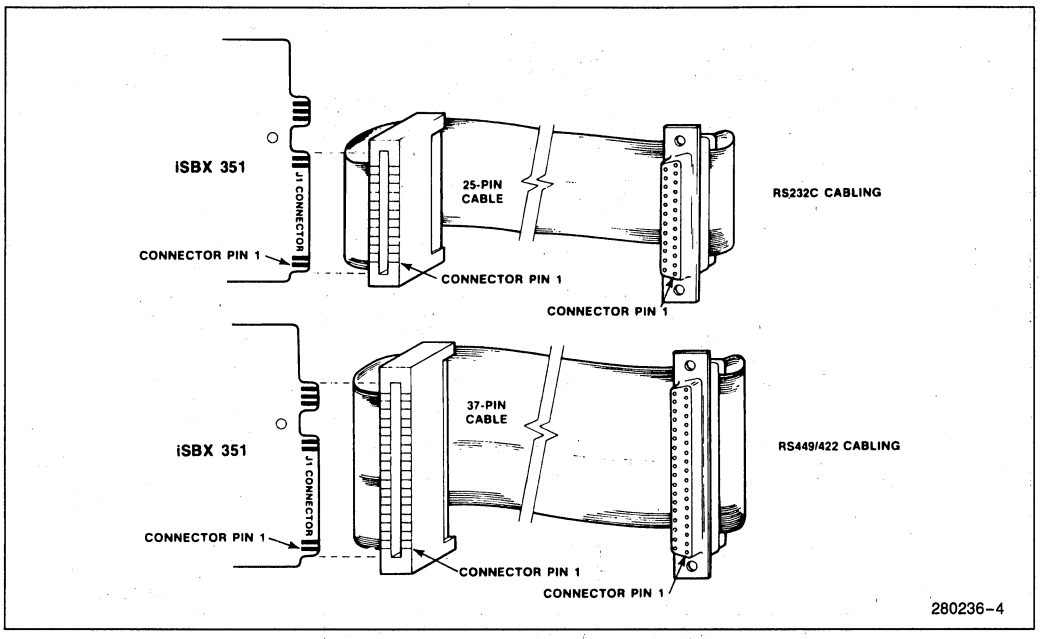


Figure 3. Cable Construction and Installation for RS232C and RS449/422 Interface

SPECIFICATIONS

I/O Addressing

I/O Address for an 8-Bit Host	I/O Address for a 16-Bit Host	Chip Select	Function
X0, X2, X4 or X6	Y0, Y4, Y8 or YC	8251A USART	Write: Data Read: Data
X1, X3, X5 or X7	Y2, Y6, YA or YE	MCS0/ Activated (True)	Write: Mode or Command Read: Status
X8 or XC	Z0 or Z8	8253 PIT	Write: Counter 0 Load: Count (N) Read: Counter 0
X9 or XD	Z2 or ZA	MSC1/Activated (True)	Write: Counter 1 Load: Count N Read: Counter 1
XA or XE	Z4 or ZC		Write: Counter 2 Load: Count (N) Read: Counter 2
XB or XF	Z6 or ZE		Write: Control Read: None

NOTE:
X = The iSBX base address that activates MCS0 & MSC1 for an 8-bit host.
Y = The iSBX base address that activates MCS0 for a 16-bit host.
Z = The iSBX base address that activates MCS1 for a 16-bit host.
The first digit, X, Y or Z, is always a variable, since it will depend on the type of host microcomputer used. Refer to the Hardware Reference Manual for your host microcomputer to determine the first digit of the I/O base address.
The first digit of each port I/O address is listed as "X" since it will change depending on the type of host iSBC microcomputer used. Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the first digit of the I/O address.

Word Size

Data—8 bits

Access Time

Read—250 ns max
Write—300 ns max

NOTE:
Actual transfer speed is dependent upon the cycle time of the host microcomputer.

Serial Communications

Synchronous—5–8-bit characters; internal character synchronization; automatic sync insertion; even, odd or no parity generation/detection.

Asynchronous—5–8-bit characters; break character generation and detection; 1, 1½, or 2 stop bits; false start bit detection; even, odd or no parity generation/detection.

Interval Timer and Baud Rate Generator

Input Frequency (selectable):

1.23 MHz ±0.1% (0.813 μs period nominal)
153.6 kHz ±0.1% (6.5 μs period nominal)

Sample Baud Rate

8253 PIT(1) Frequency (kHZ, Software Selectable)	8251 USART Baud Rate (Hz)(2)		
	Synchronous	Asynchronous	
		÷16	÷64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

NOTES:
1. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.
2. Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as frequency divider).

Output Frequency

	Rate Generator (Frequency)		Real-Time Interrupt (Interval)	
	Min	Max	Min	Max
Single Timer(1)	18.75 Hz	614.4 kHz	1.63 μs	53.3 ms
Single Timer(2)	2.34 Hz	76.8 kHz	13.0 μs	426.7 ms
Dual Timer(3) (Counters 0 and 1 in Series)	0.000286 Hz	307.2 kHz	3.26 μs	58.25 min
Dual Timer(4) (Counters 0 and 1 in Series)	0.0000358 Hz	38.4 kHz	26.0 μs	7.77 hrs

NOTES:
1. Assuming 1.23 MHz clock input.
2. Assuming 153.6 kHz clock input.
3. Assuming Counter 0 has 1.23 MHz clock input.
4. Assuming Counter 0 has 153.6 kHz clock input.

Interrupts

Interrupt requests may originate from the USART (2) or the programmable timer (2).

Interfaces

iSBX Bus—all signals TTTL compatible.

Serial—configurable of EIA Standards RS232C or RS449/422

EIA Standard RS232C signals provided and supported.

Clear to Send (CTS)
Data Set Ready (DSR)
Data Terminal Ready (DTR)
Request to Send (RTS)
Receive Clock (RXC)
Receive Data (RXD)
Transmit Clock (DTE TXC)
Transmit Data (TXD)

EIA Standard RS449/422 signals provided and supported.

Clear to Send (CS)
Data Mode (DM)
Terminal Ready (TR)
Request to Send (RS)
Receive Timing (RT)
Receive Data (RD)
Terminal Timing (TT)
Send Data (SD)

Physical Characteristics

Width: 7.24 cm (2.85 inches)

Length: 9.40 cm (3.70 inches)

Height*: 2.04 cm (0.80 inches)
iSBX 351 Board
2.86 cm (1.13 inches)
iSBX 351 Board and Host Board

Weight: 51 grams (1.79 ounces)
*(See Figure 2)

Serial Interface Connectors

Configuration	Mode(2)	MULTIMODULE™ Edge Connector	Cable	Connector(8)
RS232C	DTE	26-pin(5), 3M-3462-0001	3M(3)-3349/25	25-pin(7), 3M-3482-1000
RS232C	DCE	26-pin(5), 3M-3462-0001	3M(3)-3349/25	25-pin(7), 3M-3483-1000
RS449	DTE	40-pin(6), 3M-3464-0001	3M(4)-3349/37	37-pin(1), 3M-3502-1000
RS449	DCE	40-pin(6), 3M-3464-0001	3M(4)-3349/37	37-pin(1), 3M-3503-1000

NOTES:
1. Cable housing 3M-3485-4000 may be used with the connector.
2. DTE—Data Terminal mode (male connector), DCE—Data Set mode (female connector).
3. Cable is tapered at one end to fit the 3M-3462 connector.
4. Cable is tapered to fit 3M-3464 connector.
5. Pin 26 of the edge connector is not connected to the flat cable.
6. Pins 37, 39, and 40 of the edge connector are not connected to the flat cable.
7. May be used with cable housing 3M-3485-1000.
8. Connectors compatible with those listed may also be used.

Electrical Characteristics

DC Power Requirements

Mode	Voltage	Amps (Max)
RS232C	+5V ±0.25V	460 mA
	+12V ±0.6V	30 mA
	−12V ±0.6V	30 mA
RS449/422	+5V ±0.25V	530 mA

Environmental Characteristics

Temperature: 0°C–55°C, free moving air across the base board and MULTIMODULE board.

Reference Manual

9803190-01— iSBX 351 Serial I/O MULTIMODULE Manual (NOT SUPPLIED)

Reference Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Ave., Santa Clara, California, 95051.

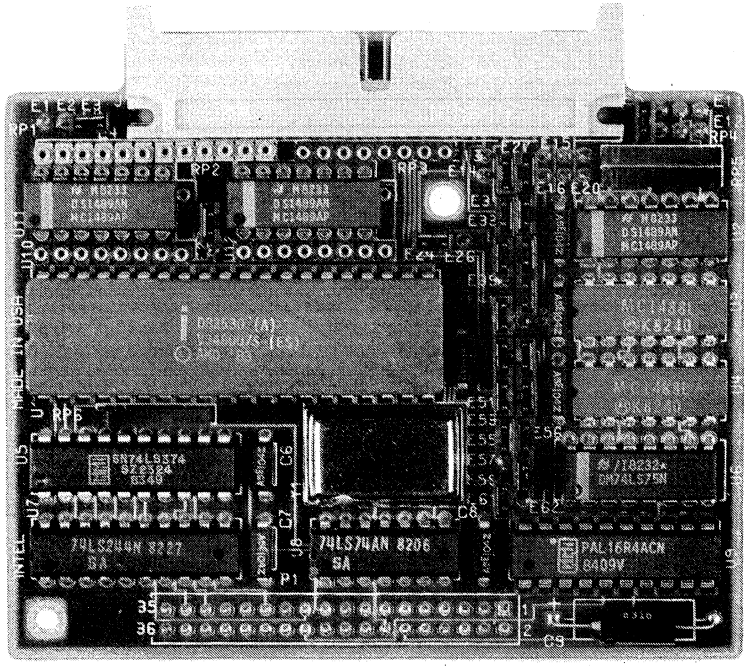
ORDERING INFORMATION

Part Number	Description
SBX 351	Serial I/O MULTIMODULE Board

iSBX™ 354 DUAL CHANNEL SERIAL I/O MULTIMODULE™ BOARD

- **Two RS232C or RS422A/449 Programmable Synchronous/ Asynchronous Communications Channels**
- **Programmable Baud Rate Generation for Each Channel**
- **Full Duplex Operation**
- **iSBX™ Bus Compatible I/O Expansion**
- **Supports HDLC/SDLC, NRZ, NRZI or FM Encoding/Decoding**
- **Three Interrupt Options for Each Channel**
- **Low Power Requirements**

The Intel iSBX 354 Serial I/O MULTIMODULE board is a member of Intel's line of iSBX compatible MULTIMODULE products. The iSBX MULTIMODULE board plugs directly into any iSBX bus compatible host board offering incremental on-board I/O expansion. Utilizing Intel's 82530 Serial Communications Controller component, the iSBX 354 module provides two RS232C or RS422A/449 programmable synchronous/asynchronous communications channels. The 82530 component provides two independent full duplex serial channels, on chip crystal oscillator, baud-rate generator and digital phase locked loop capability for each channel. The iSBX board connects to the host board through the iSBX bus. This offers maximum on-board performance and frees the MULTIBUS® System bus for use by other system resources.



280045-1

September 1987
Order Number: 280045-003

FUNCTIONAL DESCRIPTION

Communications Interface

The iSBX 354 module uses the Intel 82530 Serial Communications Controller (SCC) component providing two independent full duplex serial channels. The 82530 is a multi-protocol data communications peripheral designed to interface high speed communications lines using Asynchronous, Byte-Synchronous and Bit-Synchronous protocols to Intel's microprocessor based board and system level products. The mode of operation (i.e. asynchronous or synchronous), data format, control character format, and baud-rate generation are all under program control. The 82530 SCC component can generate and check CRC codes in any Synchronous mode and can be programmed to check data integrity in various modes. The command lines, serial data lines, and signal ground lines are brought out to a double edge connector.

The iSBX 354 module provides a low cost means to add two serial channels to iSBC® boards with 8 or 16 bit MULTIMODULE interfaces. In the factory default configuration, the iSBX 354 module will support two RS232C interfaces. With user supplied drivers and termination resistors, the iSBX 354 module can be reconfigured to support RS422A/449 communication interfaces with support on Channel A only for multidrop control from the base board. Both channels can be configured as DTE or DCE with RS232C interfaces.

Interrupt Request Line

The 82530 SCC component provides one interrupt to the MINTRO signal of the iSBX interface. There are six sources of interrupts in the SCC component (Transmit, Receive and External/Status interrupts in both channels). Each type of interrupt is enabled under program control with Channel A having higher priority than Channel B, and with Receive, Transmit

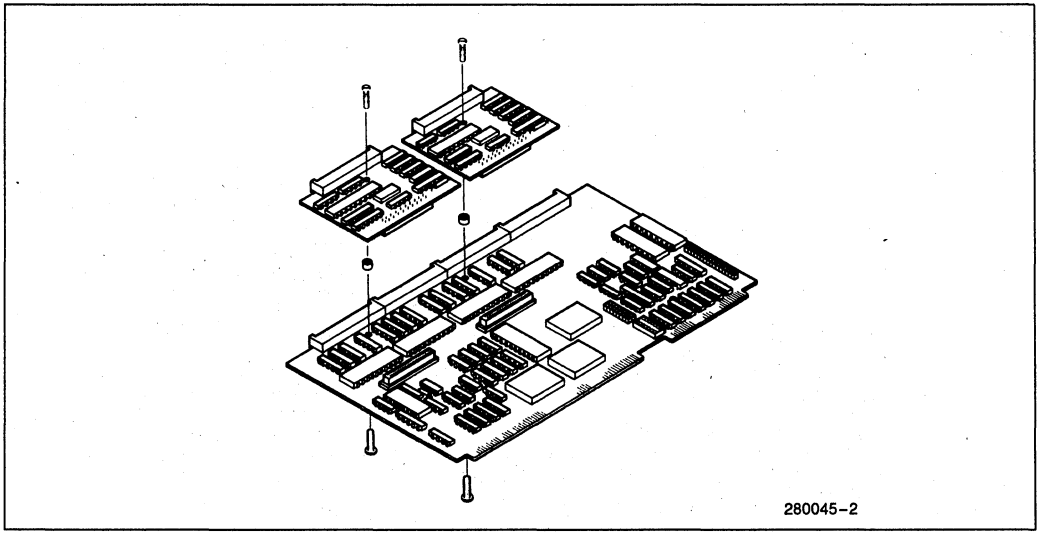


Figure 1. Installation of 2 iSBX™ 354 MULTIMODULE™ Boards on an iSBC® Board

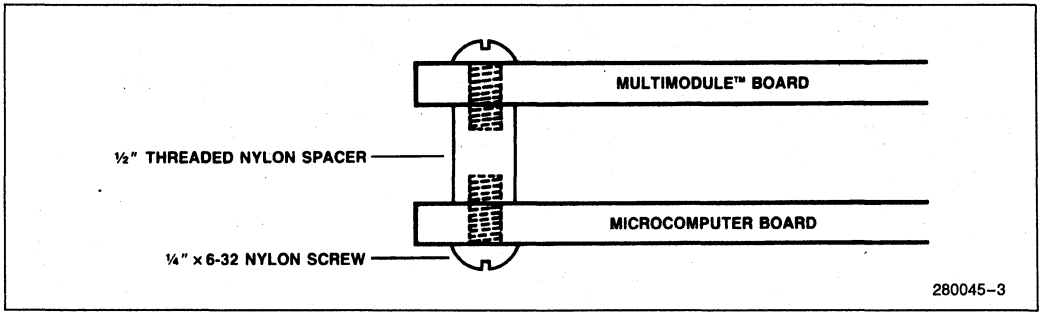


Figure 2. Mounting Technique

and External/Status interrupts prioritized in that order within each channel.

Installation

The iSBX 354 module plugs directly into the female iSBX connector on the host board. The module is then secured at one additional point with nylon hardware to insure the mechanical security of the assembly. Figures 1 and 2 demonstrate the installation of the iSBX 354 MULTIMODULE board on a Host Board. Figures 3 and 4 provide cabling diagrams.

Programming Considerations

The Intel 82530 SCC component contains several registers that must be programmed to initialize and control the two channels. Intel's iSBX 354 Module Hardware Reference Manual (Order #146531-001) describes these registers in detail.

RS232C DB-25 CONNECTORS

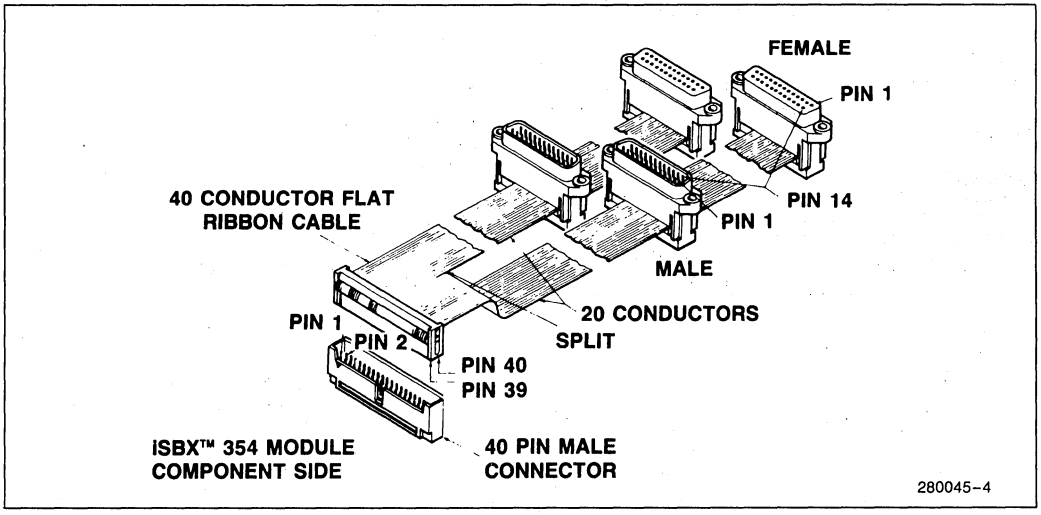


Figure 3. RS232C Cable Construction

RS422A/449 DB-37 CONNECTORS

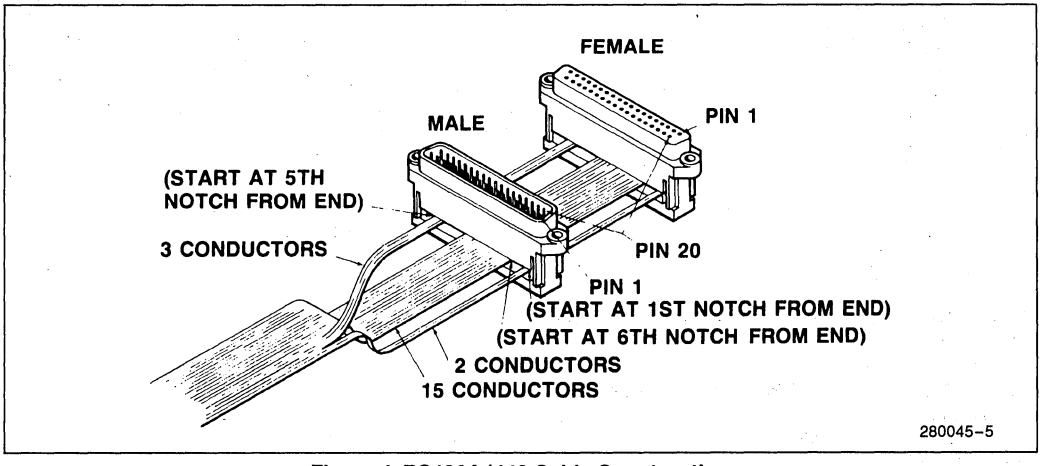


Figure 4. RS422A/449 Cable Construction

SPECIFICATIONS

Word Size

Data—8 bits

Clock Frequency

4.9152 MHz

Serial Communications

Synchronous—Internal or external character synchronization on one or two synchronous characters

Asynchronous—5–8 bits and 1, 1½ or 2 stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection

Sample Baud Rate:

Synchronous X1 Clock	
Baud Rate	**82530 Count Value (Decimal)**
64000	36
48000	49
19200	126
9600	254
4800	510
2400	1022
1800	1363
1200	2046
300	8190
Asynchronous X16 Clock	
Baud Rate	**82530 Count Value (Decimal)**
19200	6
9600	14
4800	30
2400	62
1800	83
1200	126
300	510
110	1394

INTERFACES

iSBX™ Bus: Meets the iSBX Specification, Compliance Level: D8 F

Serial: Meets the EIA RS232C standard on Channels A and B. Meets the EIA RS422A/449 standard on Channels A and B, Multi-drop capability on Channel A only.

Signals Provided

RS232C DTE

-Transmit Data
-Receive Data
-Request to Send
-Clear to Send
-Data Set Ready
-Signal Ground
-Carrier Detect
-Transmit Clock (2)
-Receive Clock
-Data Terminal Ready
-Ring Indicator

RS232C DCE

-Transmit Data
-Receive Data
-Clear to Send
-Data Set Ready
-Signal Ground
-Carrier Detect
-Transmit Clock (2)
-Receive Clock
-Ring Indicator

RS422A/449

-Send Data
-Receive Timing
-Receive Data
-Terminal Timing
-Receive Common

I/O Port Addresses

Port Address		Function
8-Bit	16-Bit	
X0		Read Status Channel B Write Command Channel B
X2		Read Data Channel B Write Data Channel B
X4		Read Status Channel A Write Command Channel A
X6		Read Data Channel A Write Data Channel A
Y0		Read Disable RS422A/449 Buffer Write Enable RS422A/449 Buffer

NOTES:
1. The "X" and "Y" values depend on the address of the iSBX interface as viewed by the base board.
2. "X" corresponds with Activation of the MCS0/interface signal; "Y" corresponds with Activation of the MCS1/interface signal.

Power Requirements

+5V at 0.5A
+12V at 50 mA
−12V at 50 mA

Physical Characteristics

Width: 2.85 inches
Length: 3.70 inches
Height: 0.8 inches
Weight: 85 grams

ENVIRONMENTAL CHARACTERISTICS

Temperature: 0°C to 55°C operating at 200 linear feet per minute across baseboard and MULTIMODULE board

Humidity: To 90%, without condensation

ORDERING INFORMATION

Part Number	Description
iSBX 354	Dual Channel I/O MULTIMODULE

REFERENCE MANUAL

146531-001—iSBX 354 Channel Serial I/O Board Hardware Reference Manual

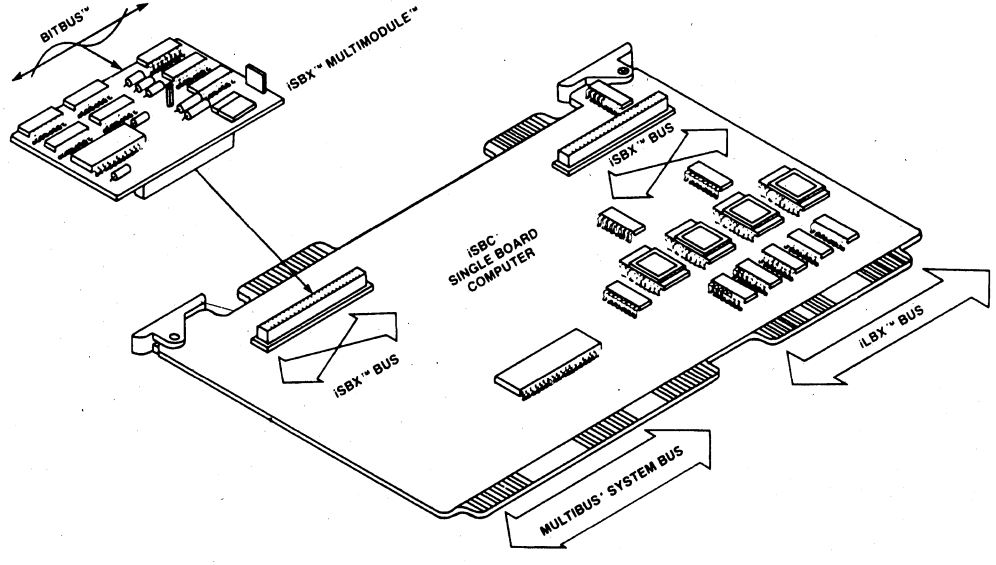
Reference manuals may be ordered from any Intel sales representative, distributor office, or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

iSBX™ I/O EXPANSION BUS

- **IEEE 959-88 Industry Standard I/O Expansion Bus**
- **Provides On-Board Expansion of System Resources**
- **Small iSBX™ MULTIMODULE™ Boards Plug Directly into iSBC® Boards**
- **Supports Compatible 8- and 16-Bit Data Transfer Operations**
- **Part of Intel's Total System Architecture: MULTIBUS®, iLBX™ and iSBX™**
- **Low-Cost "Vehicle" to Incorporate the Latest VLSI Technology into iSBC®-Based Systems**
- **Provides Increased Functional Capability and High Performance**
- **Supported by a Complete Line of iSBC® Base Boards and iSBX™ MULTIMODULE™ Boards, Providing Analog and Digital I/O, High-Speed Math, Serial and Parallel I/O, Video Graphics, and Peripheral Controllers**

The iSBX™ I/O Expansion Bus is one of a family of standard bus structures resident within Intel's total system architecture. The iSBX bus is a modular, I/O expansion bus capable of increasing a single board computer's functional capability and overall performance by providing a structure to attach small iSBX MULTIMODULE™ boards to iSBC® base boards. It provides for rapid incorporation of new VLSI into iSBC MULTIBUS® systems, reducing the threat of system obsolescence. The iSBX bus offers users new economics in design by allowing both system size and system cost to be kept at minimum. As a result, the system design achieves maximum on-board performance while allowing the MULTIBUS interface to be used for other system activities. The iSBX bus enables users to add-on capability to a system as the application demands it by providing off-the-shelf standard MULTIMODULE boards in the areas of graphics controllers, advanced mathematics functions, parallel and serial I/O, disk and tape peripheral controllers, and magnetic bubble memory. A full line of MULTIBUS boards and iSBX MULTIMODULE boards are available from Intel and other third party sources in the industry.

Its success as an industry standard has been reinforced by adoption of the SBX specification by the Institute of Electrical & Electronic Engineers — IEEE 959-88.



280255-1

September 1988
Order Number: 280255-001

FUNCTIONAL DESCRIPTION

Bus Elements

The iSBX™ MULTIMODULE™ system is made up of two basic elements: base boards and iSBX MULTIMODULE boards. In an iSBX system, the role of the base board is simple. It decodes I/O addresses and generates the chip selects for the iSBX MULTIMODULE boards.

The iSBX bus supports two classes of base boards, those with direct memory access (DMA) support and those without. Base boards with DMA support have DMA controllers that work in conjunction with an iSBX MULTIMODULE board (with DMA capability) to perform direct I/O to memory or memory to I/O operations. Base boards without DMA support use a subset of the iSBX bus and simply do not use the DMA feature of the iSBX MULTIMODULE board.

The iSBX MULTIMODULE boards are small, specialized, I/O mapped boards which plug into base boards. The iSBX boards connect to the iSBX bus connector and convert iSBX bus signals to a defined I/O interface.

Bus Interface/Signal Line Descriptions

The iSBX bus interface can be grouped into six functional classes: control lines, address and chip select lines, data lines, interrupt lines, option lines, and power lines. The iSBX bus provides nine control lines that define the communications protocol between base board and iSBX MULTIMODULE boards. These control lines are used to manage the general operation of the bus by specifying the type of transfer, the coordination of the transfer, and the overall state of the transfer between devices. The five address and chip select signal lines are used in conjunction with the command lines to establish the I/O port address being accessed, effectively selecting the proper iSBX MULTIMODULE. The data lines on the iSBX bus can number 8 or 16, and are used to transmit or receive information to or from the iSBX MULTIMODULE ports. Two interrupt lines are provided to make interrupt requests possible from the iSBX board to the base board. Two option lines are reserved on the bus for unique user requirements, while several power lines provide +5 and ±12 volts to the iSBX boards.

Bus Pin Assignments

The iSBX bus uses widely available, reliable connectors that are available in 18/36 pin for 8-bit devices and 22/44 pin for 16-bit devices. The male iSBX connector is attached to the iSBX MULTIMODULE board and the female iSBX connector is attached to the base board. Figure 2 shows the dimensions and pin numbering of the 18/36 pin iSBX connector, while Figure 3 does the same for the 22/44 pin iSBX connector. A unique scheme allows the 16-bit female connector to support 8 or 16-bit male MULTIMODULE boards. Table 1 lists the signal/pin assignments for the bus.

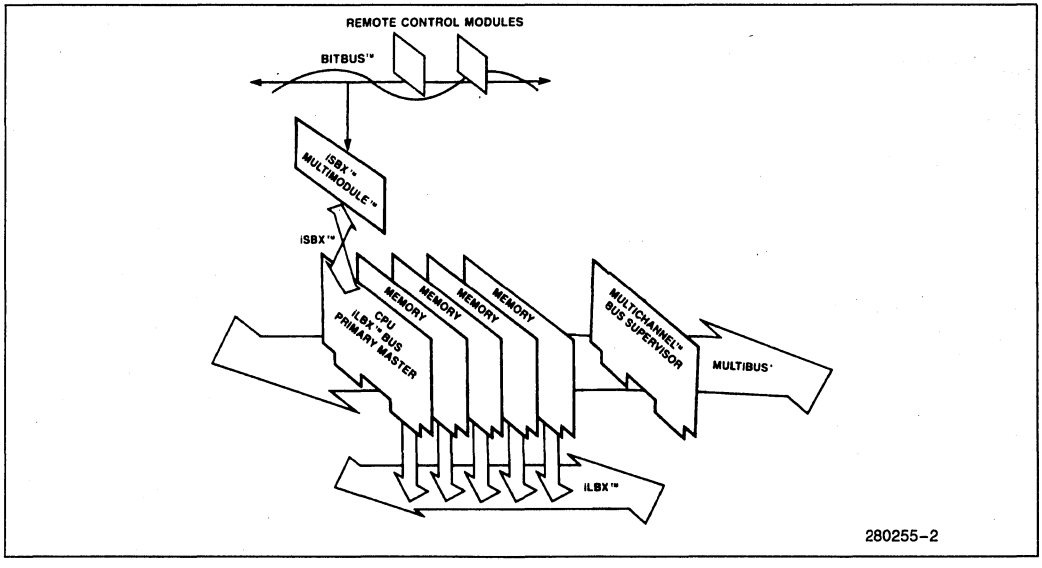


Figure 1. MULTIBUS® System Architecture

Table 1. iSBX™ Signal/Pin Assignments

Pin(1)	Mnemonic	Description	Pin(1)	Mnemonic	Description
43	MD8	MDATA Bit 8	44	MD9	MDATA Bit 9
41	MDA	MDATA Bit A	42	MDB	MDATA Bit F
39	MDC	MDATA Bit C	40	MDD	MDATA Bit D
37	MDE	MDATA Bit E	38	MDF	MDATA Bit F
35	GND	Signal Gnd	36	+5V	+5V
33	MD0	MDATA Bit 0	34	MDRQT	M DMA Request
31	MD1	MDATA Bit 1	32	MDACK/	M DMA Acknowledge
29	MD2	MDATA Bit 2	30	OPT0	Option 0
27	MD3	MDATA Bit 3	28	OPT 1	Option 1
25	MD4	MDATA Bit 4	26	TDMA	Terminate DMA
23	MD5	MDATA Bit5	24		Reserved
21	MD6	MDATA Bit 6	22	MCS0/	M Chip Select 0
19	MD7	MDATA Bit 7	20	MCS/1	M Chip Select 1
17	GND	Signal Gnd	18	+5V	+5V
15	IORD/	I/O Read Cmd	16	MWAIT/	M Wait
13	IOWRT/	I/O Write Cmd	14	MINTRO	M Interrupt 0
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
9	MA1	M Address 1	10		Reserved
7	MA2	M Address 2	8	MPST/	iSBX Multimodule Board Present
5	RESET	Reset	6	MCLK	M Clock
3	GND	Signal Gnd	4	+5V	+5V
1	+12V	+12V	2	−12V	−12V

NOTES:
1. Pins 37–44 are used only on 8/16-bit systems.
2. All undefined pins are reserved for future use.

Bus Operation Protocol

COMMAND OPERATION

The iSBX bus supports two types of transfer operations between iSBX elements: I/O Read and I/O Write. An iSBX board can respond to these I/O transfers using either full speed mode or extended mode.

For a full speed I/O Read (Figure 4) the base board generates a valid I/O address and a valid chip select for the iSBX MULTIMODULE board. After setup, the base board activates the I/O Read line causing the iSBX board to generate valid data from the addressed I/O port. The base board then reads the data and removes the read command, address, and chip select. The full speed I/O Write (Figure 5) operation is similar to the I/O Read except that the base board generates valid data on the lines and keeps the write command line active for the specified hold time.

The extended Read operation (Figure 6) is used by iSBX MULTIMODULE boards that aren't configured to meet full speed specifications. It's operation is similar to full speed mode, but must use a wait signal to ensure proper data transfer. The base board begins the operation by generating a valid I/O address and chip select. After setup, the base board activates the Read line causing the iSBX board to generate a Wait signal. This causes the CPU on the base board to go into a wait state. When the iSBX board has placed valid Read data on the data lines, the MULTIMODULE board will remove the Wait signal and release the base board CPU to read the data

and deactivate the command, address, and chip select. The extended Write operation (Figure 7) is similar to the extended Read except that the Wait signal is generated after the base board places valid Write data on the data lines. The iSBX board removes the Wait signal when the write pulse width requirements are satisfied, and the base board can then remove the write command after the hold time is met.

DMA OPERATION

An iSBX MULTIMODULE system can support DMA when the base board has a DMA controller and the iSBX MULTIMODULE board can support DMA mode. Burst mode DMA is fully supported, but for clarity and simplicity, only a single DMA transfer for an 8-bit base board is discussed.

A DMA cycle (Figure 8) is initiated by the iSBX board when it activates the DMA request line going to the DMA controller on the base board. When the DMA controller gains control of the base board bus, it acknowledges back to the iSBX board and activates an I/O or Memory Read. The DMA controller then activates an I/O or Memory Write respectively. The iSBX board removes the DMA request during the cycle to allow completion of the DMA cycle. Once the write operation is complete, the DMA controller is free to deactivate the write and read command lines after a data hold time.

INTERRUPT OPERATION

The iSBX MULTIMODULE board on the iSBX bus can support interrupt operations over its interrupt lines. The iSBX board initiates an interrupt by activating one of its two interrupt lines which connect to the base board. The CPU processes the interrupt and executes the interrupt service routine. The interrupt service routine signals the iSBX MULTIMODULE board to remove the interrupt, and then returns control to the main line program when the service routine is completed.

Please refer to the Intel iSBX Bus Specification for more detailed information on its operation and implementation.

SPECIFICATIONS

Word Size

Data: 8, 16-bit

Power Supply Specifications

Table 3.

Minimum (volts)	Nominal (volts)	Maximum (volts)	Maximum (current)*
+4.75	+5.0	+5.25	3.0A
+11.4	+12	+12.6	1.0A
−12.6	−12	−11.4	1.0A
—	GND	—	3.0A

NOTE:
*Per iSBX MULTIMODULE board mounted on base board.

Port Assignments

Table 2. iSBX™ MULTIMODULE™ Base Board Port Assignments

iSBX™ Connector Number	Chip Select	8-Bit Base Board Address	16-Bit Base Board Address (8-bit mode)	16-Bit Base Board Address (16-bit mode)
iSBX1	MCS0/ MCS1/	F0–F7 F8–FF	0A0–0AF 0B0–0BF	0A0,2,4,6,8, A,C,E 0A1,3,5,7,9, B,D,F
iSBX2	MCS0/ MCS1/	C0–C7 C8–CF	080–08F 090–09F	080,2,4,6,8 A,C,E 081,3,5,7,9, B,D,F
iSBX3	MCS0/ MCS1/	B0–B7 B8–BF	060–06F 060–06F	060,2,4,6,8 A,C,E 061,3,5,7,9, B,D,F

DC Specifications

Table 4. iSBX™ MULTIMODULE™ Board I/O DC Specifications

Output[1]

Bus Signal Name	Type[2] Drive	I_{OL} Max −Min (mA)	@Volts (V_{OL} Max)	I_{OH} Max −Min (μA)	@ Volts (V_{OH} Min)	C_O (Min) (pf)
MD0–MDF	TRI	1.6	0.5	−200	2.4	130
MINTR0-1	TTL	2.0	0.5	−100	2.4	40
MDRQT	TTL	1.6	0.5	−50	2.4	40
MWAIT/	TTL	1.6	0.5	−50	2.4	40
OPT1–2	TTL	1.6	0.5	−50	2.4	40
MPST/	TTL	Note 3				

Input[1]

Bus Signal Name	Type[2] Receiver	I_{IL} Max (mA)	@V_{IN} MAX (volts) Test Cond.	I_{IH} Max (μA)	@V_{IN}MAX (volts) Test Cond.	C_IMax (pf)
MD0–MDF	TRI	−0.5	0.4	70	2.4	40
MA0–MA2	TTL	−0.5	0.4	70	2.4	40
MCS0/–MCS1/	TTL	−4.0	0.4	100	2.4	40
MRESET	TTL	−2.1	0.4	100	2.4	40
MDACK/	TTL	−1.0	0.4	100	2.4	40
IORD/ IOWRT/	TTL	−1.0	0.4	100	2.4	40
MCLK	TTL	−2.0	0.4	100	2.4	40
OPT1–OPT2	TTL	−2.0	0.4	100	2.4	40

NOTES:
1. Per iSBX MULTIMODULE I/O board.
2. TTL = standard totem pole output. TRI = Three-state.
3. iSBX MULTIMODULE board must connect this signal to ground.

All Inputs: Max V_{IL} = 0.8V
Min V_{IH} = 2.0V

Connectors

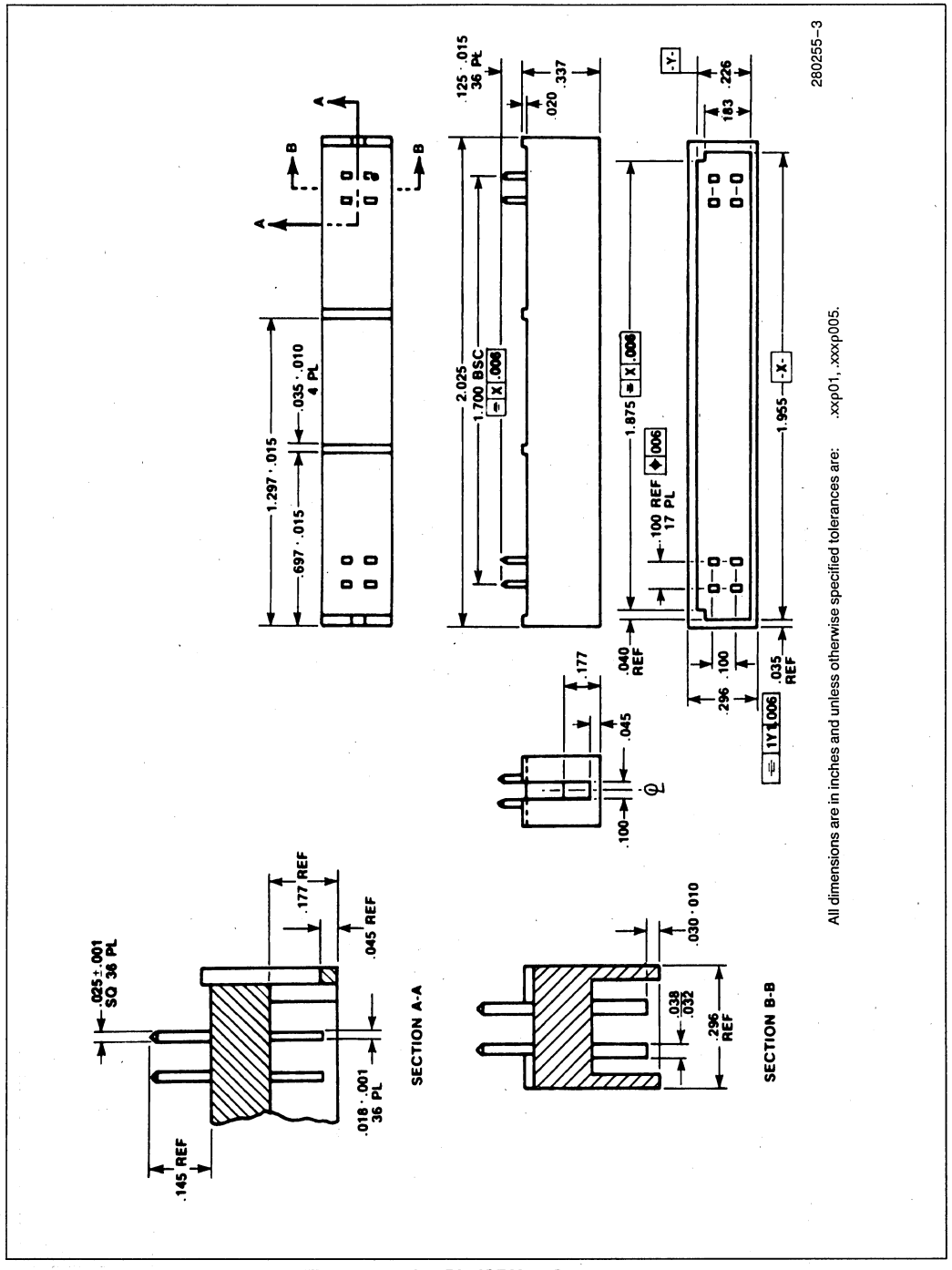


Figure 2. 18/36 Pin iSBX™ Connector

Connectors (Continued)

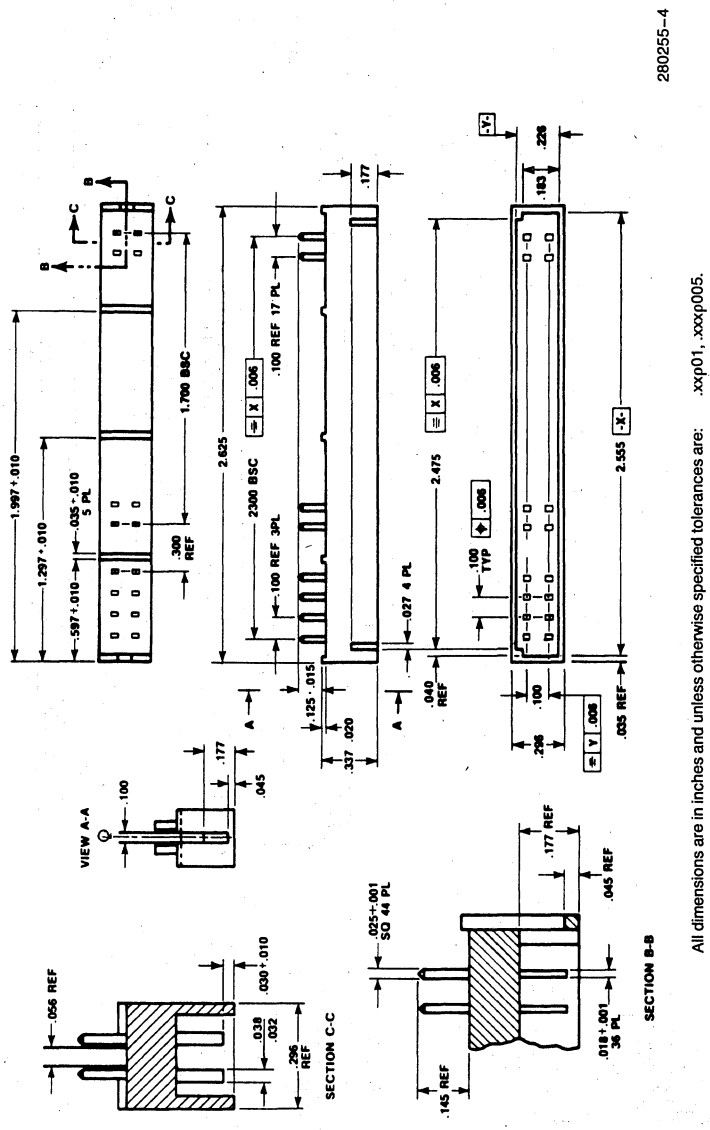


Figure 3. 22/44 Pin iSBX™ Connector

Bus Timing Diagrams

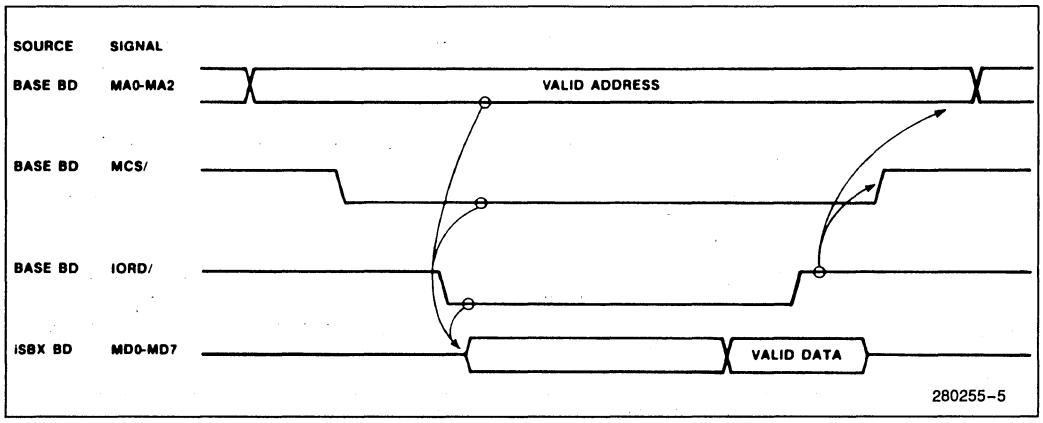


Figure 4. iSBX™ MULTIMODULE™ Read, Full Speed

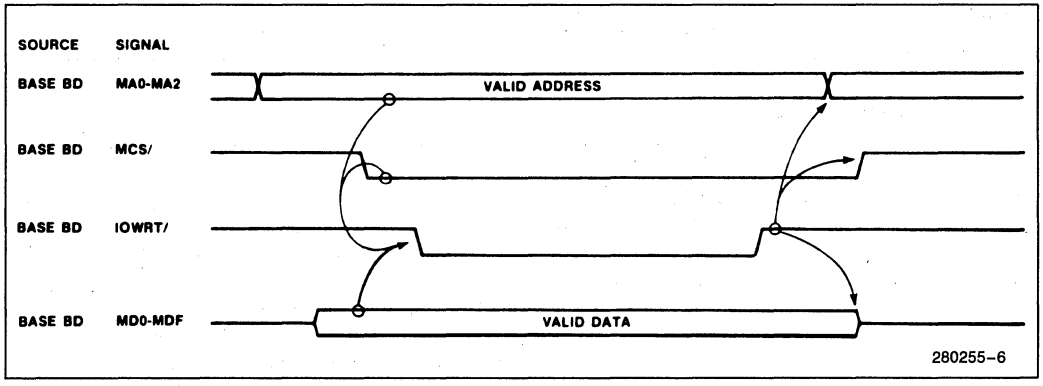


Figure 5. iSBX™ MULTIMODULE™ Board Write, Full Speed

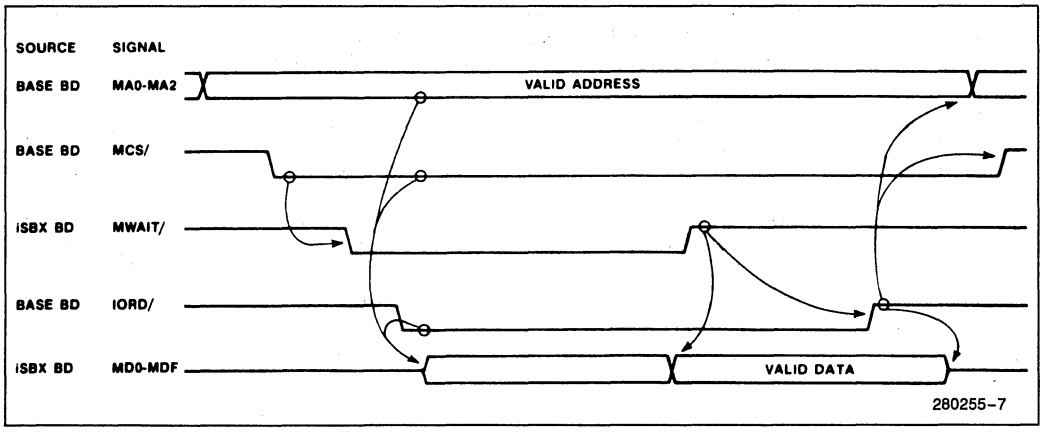


Figure 6. iSBX™ MULTIMODULE™ Board Extended Read

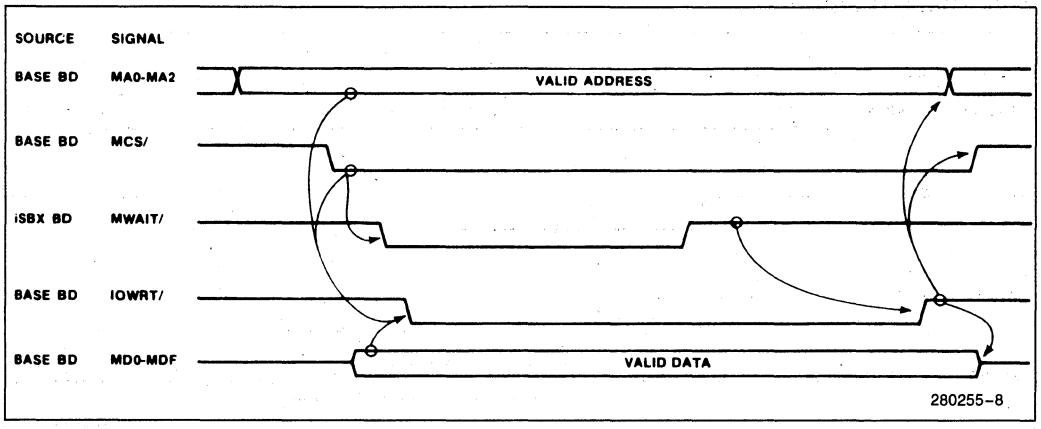


Figure 7. iSBC® MULTIMODULE™ Board Extended Write

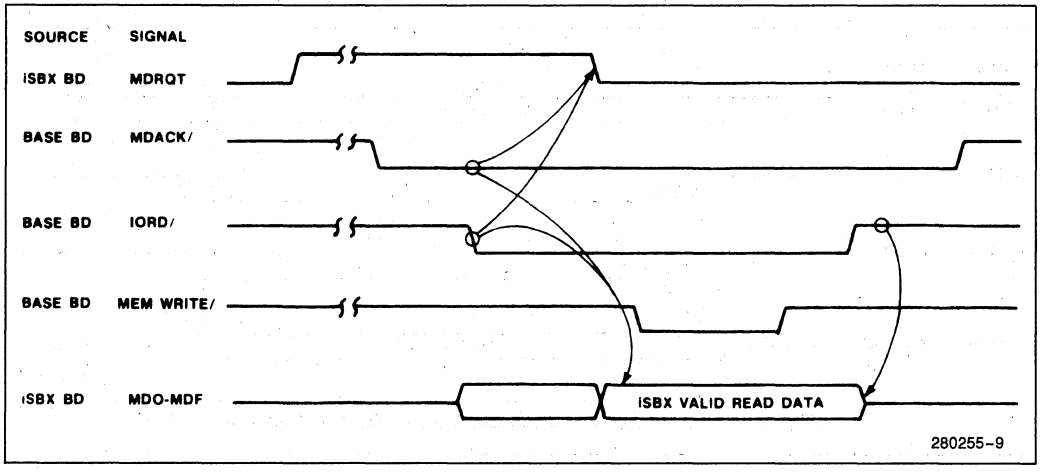


Figure 8. iSBX™ MULTIMODULE™ Board DMA Cycle
(iSBX™ MULTIMODULE™ to Base Board Memory)

Board Outlines

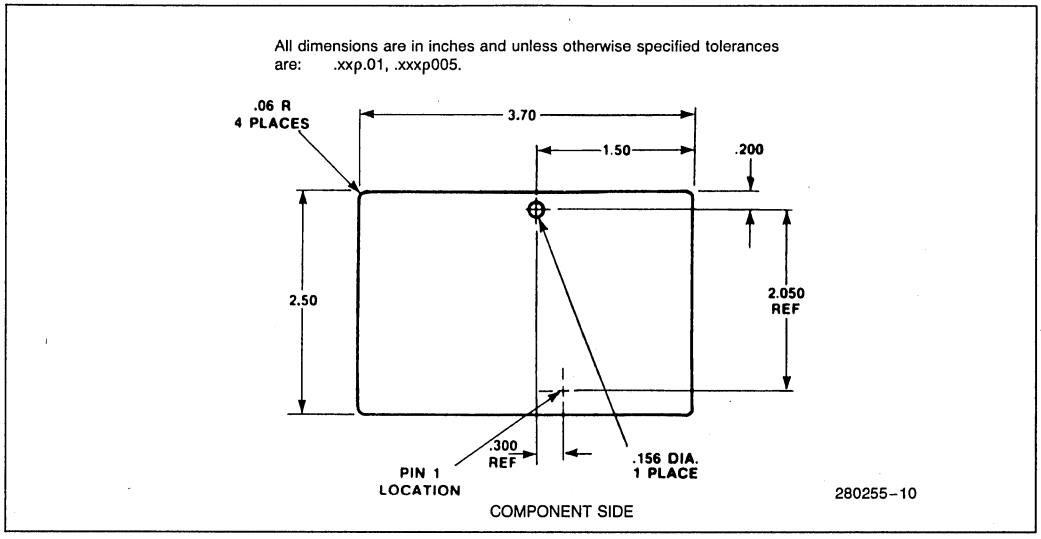


Figure 9. iSBX™ Board Outline

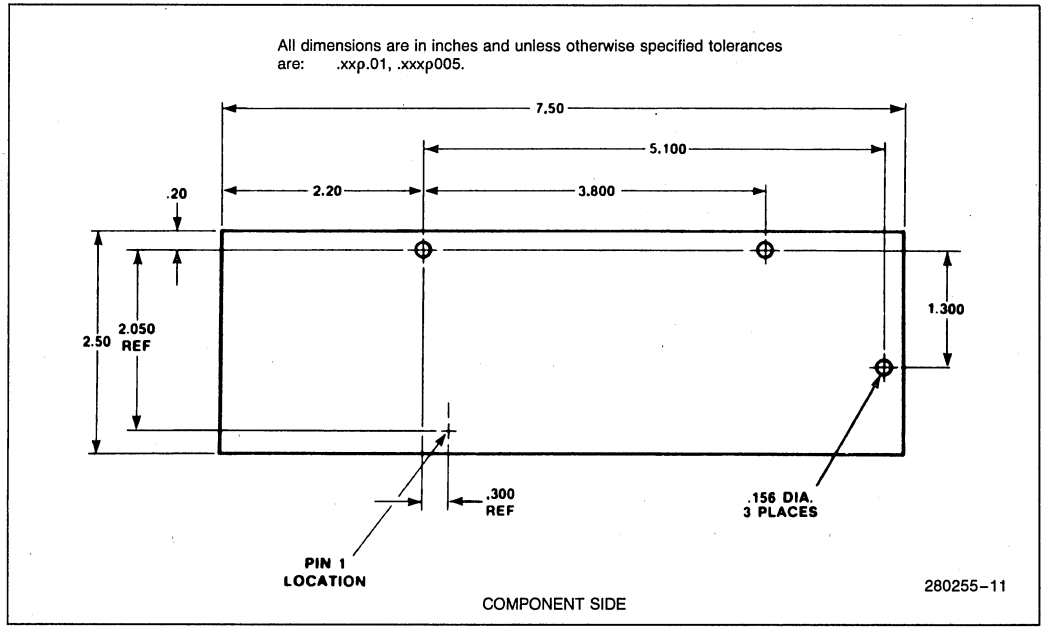


Figure 10. Double Wide iSBX™ Board Outline

Environmental Characteristics

Operating Temperature: 0°C to 55°C

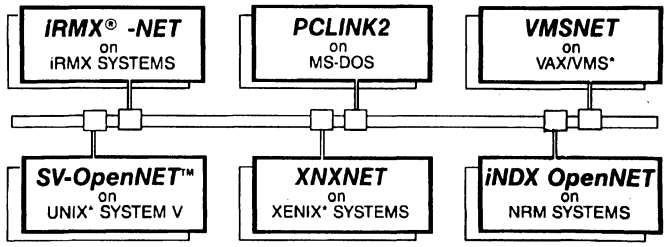
Humidity: 90% maximum relative; non-condensing

Reference Manuals

210883-002—MULTIBUS Architecture Reference Book

Local Area Network Boards and Software

17



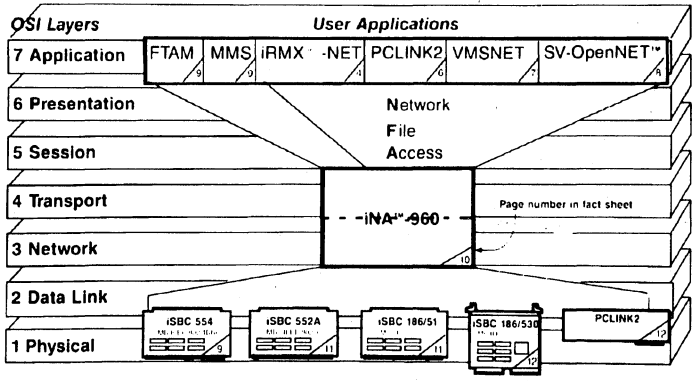
OpenNET™: THE COMPLETE OPEN NETWORK SOLUTION

The OpenNET family provides the OEM with complete *Open Network* solutions for an enterprise-wide, multi-vendor network based on international standards.

FEATURES:

- Interoperability between the factory, office, and engineering environments
- Complete hardware and software network solutions
- On-going customer support through extensive training and application development

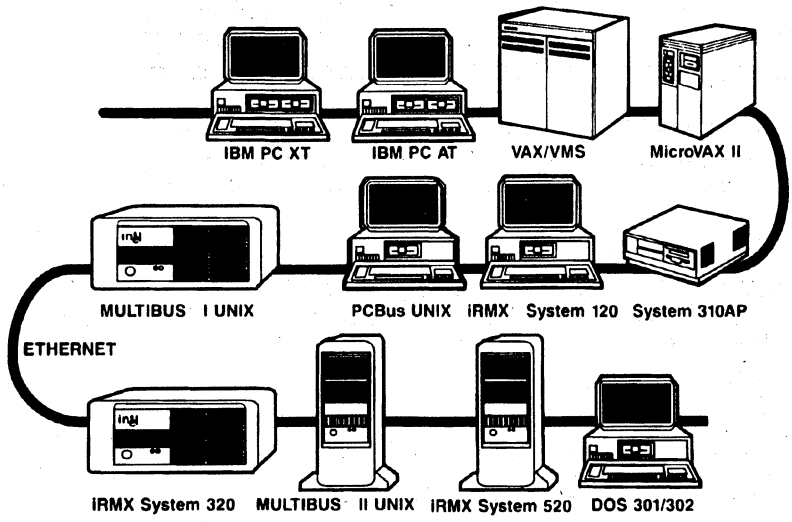
GUIDE TO THE OpenNET™ PRODUCTS



September, 1988
Order Number: 280669-001

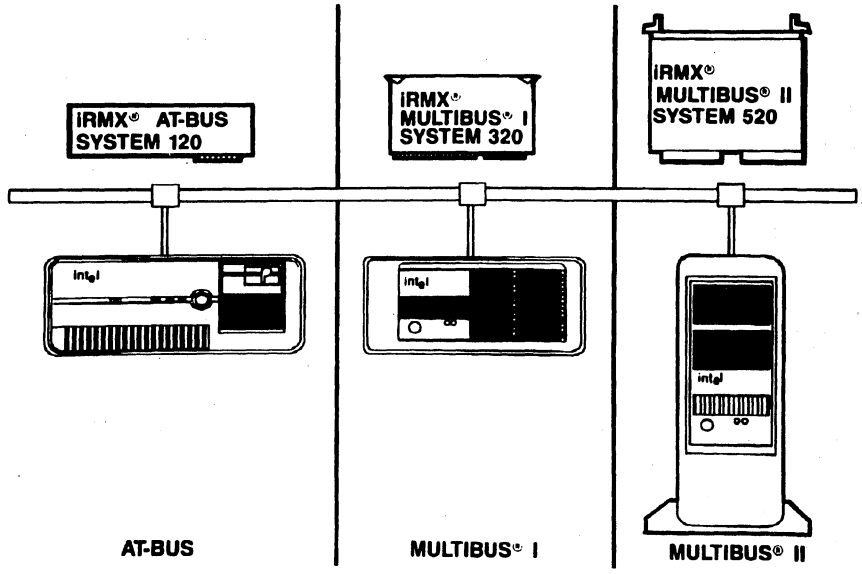
OpenNET™ OVERVIEW

OpenNET™ MEANS OPEN NETWORKS



Users are placing increasing demands for data communications capabilities on their computing applications. The OpenNET family of networking products supplies those capabilities to let OEMs offer solutions to communications-intensive requirements, based on Intel's real-time computing products.

- Open to multiple media
  - —IEEE 802.3/Ethernet
  - —Thin-wire Ethernet
  - —IEEE 802.4
  - —X.25
- Open to different Operating Systems
  - —iRMX
  - —MS-DOS*
  - —PC-DOS
  - —UNIX SYSTEM V*
  - —VAX/VMS*
  - —XENIX*
  - —iNDX
- Open to expansion
- Open to different hardware
  - —MULTIBUS®I
  - —MULTIBUS®II
  - —PC XT/AT Bus
- Open to different environments
  - —Factory
  - —Office
  - —Lab
  - —Engineering Workstation
- Open to multi-vendor solutions
- Open to future upgrades



COMPLETE OpenNET™ SOLUTION FOR REAL-TIME SYSTEMS

Real-Time computer systems require a real-time operating system. The iRMX operating system from Intel is the world's most popular operating system for real-time systems.

Many real-time applications require network communication. Intel's iRMX-NET Release 3.0 delivers a rich set of networking capabilities and a full range of iRMX platform support:

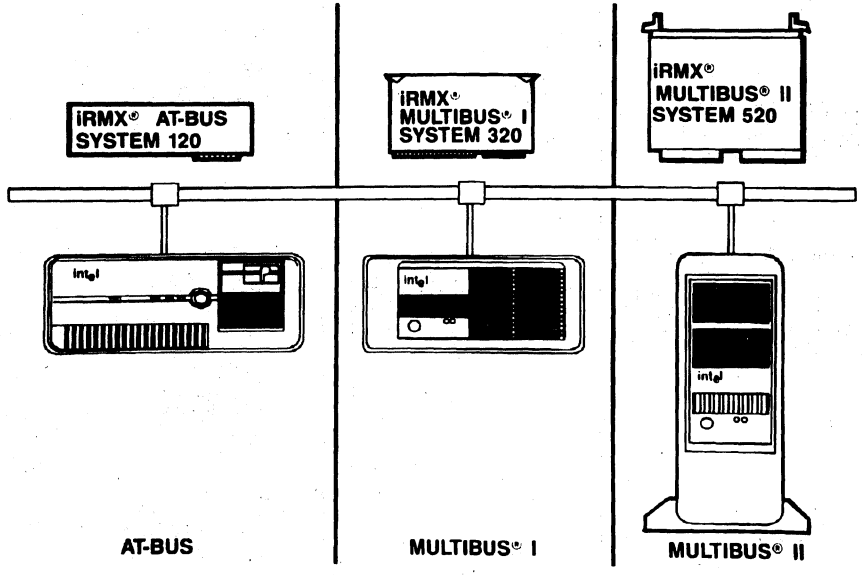
- Transparent Network File Access
- Transport and Distributed Name Server Software with Programmatic Access
- iRMX System 120 (AT-bus), 320 (MULTIBUS I) and 520 (MULTIBUS II) Connections
- Remote Boot for Diskless Systems

Networked iRMX systems serve in a wide range of real-time application areas including data acquisition, factory automation, financial workstations, military, medical instrumentation, simulation and process control.

TRANSPARENT NETWORK FILE ACCESS

iRMX-NET implements the NFA protocol to provide transparent file access capabilities among iRMX, DOS, VAX/VMS, UNIX, XENIX and iNDX systems on the OpenNET network. Remote files are accessed as if they resided on the local iRMX system. iRMX-NET can be configured as a network file consumer, file server, or both, depending on the application's requirements.

The iRMX operating system provides a rich set of human interface commands and system calls for accessing local files. With the addition of iRMX-NET, these commands and system calls are transparently extended to remote access as well. Transparency means that applications using the iRMX Human Interface commands or BIOS system calls do not need to know whether the files they access reside locally or on some remote system.



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iRMX®-NET OpenNET™ NETWORKING SOFTWARE

OSI TRANSPORT AND DISTRIBUTED NAME SERVER WITH PROGRAMMATIC INTERFACE

The iRMX-NET R3.0 product includes iNA 960 R3 OSI Transport and Network software preconfigured for a variety of Intel Network Interface Adapters.

iRMX-NET R3.0 also includes the iRMX-NET Distributed Name Server software. The Distributed Name Server software maintains and provides access to a network directory database. The database is distributed across the network with each system maintaining its own logical piece of the directory. The Distributed Name Server software provides a full set of network directory services and is used to perform such tasks as logical name to network address mapping for establishing network connections between systems.

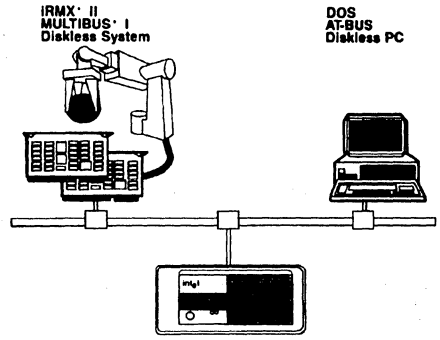
The combination of transparent network file access with iRMX commands and system calls, plus direct programmatic access to the iNA 960 Transport and iRMX-NET Distributed Name Server software gives the programmer a powerful set of capabilities for developing real-time network applications.

iRMX® SYSTEM 120, 320 AND 520 CONNECTIONS

iRMX-NET R3.0 provides networking support for the full range of Intel real-time Systems, from the low-cost AT-Bus System 120, through the MULTIBUS I System 320, to the high-end multiprocessing MULTIBUS II System 520. iRMX-NET R3.0 also supports iRMX board-level designs built around Intel's family of host CPU boards and Network Interface Adapters. Consistent operating system and networking software interfaces provide for easy development of network applications that span the various iRMX platforms.

REMOTE BOOT FOR DISKLESS SYSTEMS

iRMX-NET R3.0 supports networked diskless systems by providing network Boot Consumer, Boot Server and File Server capabilities.



PRODUCT CODES

RMXINET	iRMX-NET Networking Software for the iRMX 86 operating system.
RMXIINET	iRMX-NET Networking Software for the iRMX II operating system.

REAL-TIME BOARD AND SYSTEM LEVEL SUPPORT

	iRMX® 86	iRMX® II		
	MULTIBUS® I	AT-BUS	MULTIBUS® I	MULTIBUS® II
SYSTEM	SYSTEM 310AP	SYSTEM 120	SYSTEM 310AP, 320	SYSTEM 520
HOST BOARD	iSBC 86/30 iSBC 86/35 iSBC 86/C38 iSBC 286/10(A) iSBC 286/12, 14, 16	SYSTEM 120	iSBC 286/10A iSBC 286/12, 14, 16 iSBC 386/12 iSBC 386/2X iSBC 386 3X	iSBC 386/116 iSBC 386/120 iSBC 386/258
NETWORK INTERFACE ADAPTER	iSBC 552(A) iSBC 186/51*	PCLINK2	iSBC 552(A)	iSBC 186/530

* iSBC 186/51 support requires separate purchase of iNA 960 R30

PCLINK2, NetBIOS, AND MS-NET ACCESS FOR THE PC

COMPLETE OpenNET™ SOLUTION FOR THE PC

Users of IBM PC AT, PC XT and other compatible computers can access Intel's OpenNET networking system through the OpenNET PC Link2 family of hardware and software products. The hardware connection is provided by an 80186/82586-based intelligent expansion board, the PCLINK2 Network Interface Adapter (PCLINK2NIA). The software package incorporates: MS-NET for transparent file access under DOS, iNA 961, NetBIOS interface, dynamic name resolution and user-friendly installation software.

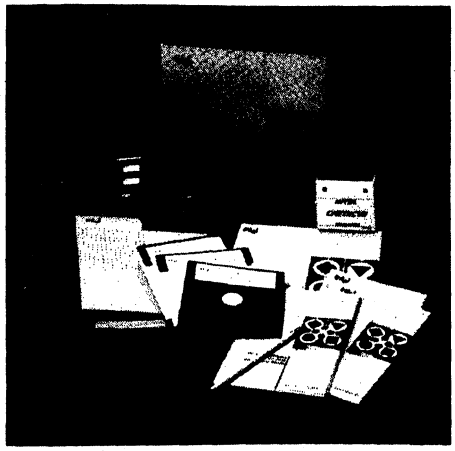
The NetBIOS interface provides the flexibility to use the PCLINK2NIA with commercially available NetBIOS compatible applications, such as IBM's PC-LAN program. Optionally, MS-NET networking software is available for the upper layers.

TRANSPARENT NETWORKING FILE ACCESS

OpenNET/PCLINK2 gives users the freedom to network PCs as consumer workstations or as file servers. PCLINK2 with MS-NET implements the NFA Protocol for easy access to files on other operating systems, such as iNDX, XENIX, UNIX, iRMX, or VAX/VMS.

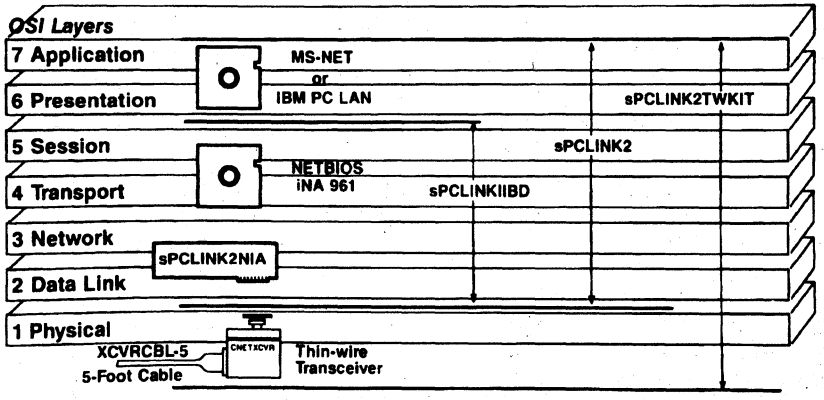
REMOTE BOOT FOR DISKLESS SYSTEM

Diskless workstation support for the PC is provided by on-board firmware, an iRMX-NET Boot Server and any OpenNET File Server on the network.



PRODUCT CODES

sPCLINK2NIA	PC Link2 Network Interface Adapter, hardware only
sPCLINK2	Seven-layer solution with: sPCLINK2NIA, iNA961, NetBIOS interface, MS-NET
sPCLINKIIBD	Five-layer solution with: sPCLINK2NIA, iNA961, NetBIOS interface
sPCLINK2TWKIT	Seven-layer thin-wire solution with: sPCLINK2, CNETXCVR, XCVRCBL-5
sPCLINK2DEVKIT	NetBIOS Developer's Kit with: 2-sPCLINK2CNETKITs, NetBIOS programmer kit
PCLDOSRBIRO	Request Block Developer's Software with iNA 961 for PCLINK2



VAX/VMS* OpenNET™ NETWORKING SOFTWARE

COMPLETE OpenNET™ SOLUTION FOR THE VAX

VAX/VMS Networking software (VMSNET) provides the OpenNET connection for a VAX* or MicroVAX II* system to iRMX, XENIX, MS-DOS, UNIX System V and iNRM systems.

VMSNET enables a MicroVAX or VAX system to act as an OpenNET file server system allowing any OpenNET consumer node transparent file access to files on the MicroVAX or VAX.

The VMSNET product includes one of two types of Ethernet controller boards: a UNIBUS* board for the VAX or a Q-bus* board for the MicroVAX.

VMSNET software performs the OpenNET functions via an implementation of the Network File Access (NFA) file server protocols, VMS consumer bi-directional file transfer utilities, and Intel's iNA 960 transport layer software running on the supplied intelligent LAN controllers.

A set of network management utilities provide (Micro)VAX users with information and statistics about VMSNET activities.

FILE ACCESS

- Transparent file access between a VAX/VMS server and MS-DOS, iRMX, XENIX, UNIX System V and iNRM systems
- DECnet compatibility: consumer nodes may access remote files using VMS logical names over DECnet (no file locking or compatibility mode opens)

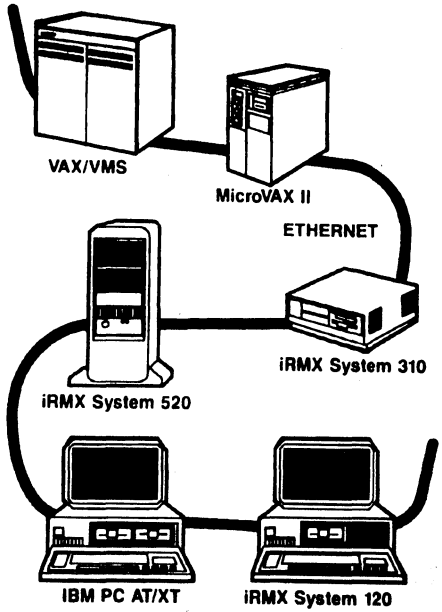
HOST REQUIREMENTS

- VAX 750, 780, 782, 785
- VAX 8200, 8250, 8500, 8530, 8600, 8650
- MicroVAX II
- (Micro)VMS versions 4.2-5.0

HARDWARE FEATURES

- 80186/82586-based LAN Boards
- Unibus power requirements: + 5 VDC at 4.5 amps, 6 amps maximum, – 15 VDC at .5 amps, 3 amp surge
- Qbus power requirements: + 5 VDC at 6 amps, 6 amps maximum.
- Internal cables, mounting hardware and user manuals are included.

Hardware installation and service contracts should be arranged with Digital Equipment Service Personnel.



PRODUCT CODES

VMSNET	VAX/VMS Networking Software for VAX family
MVMSNET	VAX/VMS Networking Software for MicroVAX II

INTEL SYSTEM V OpenNET™ NETWORKING SOFTWARE

COMPLETE OpenNET™ SOLUTION FOR UNIX SYSTEM V

SV-OpenNET connects Intel SYSTEM V/386 systems with all the OpenNET nodes. SV-OpenNET is available for MULTIBUS I and MULTIBUS II. The product includes a complete solution: communications board, Mail, VT, print spooling, nameserver interface library (NSI), and network management.

SV-OpenNET allows application interfacing through the UNIX TLI library. Applications may also access SV-OpenNET via the higher-level NSI library. SV-OpenNET can also coexist with the UNIX network, RFS.

FEATURES

Network File Access (NFA) based

- Core, Extended, and Intel protocols supported
- Both Server and Consumer functionality supported
- Remote Batch Execution (RBE) through "rexec"

NETWORK ADMINISTRATION AND MANAGEMENT

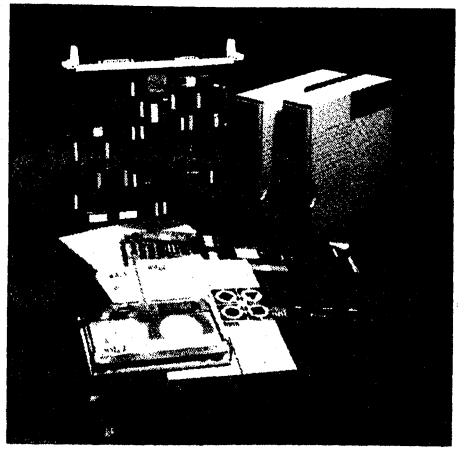
- Compatible with XENIX-NET
- File-based Nameserver compatible with XENIX-NET /net/data files

MAIL

- Supports MMDF (4.2BSD UNIX mail)
- Interoperates with XENIX-NET

VIRTUAL TERMINAL (VT)

- OpenNET/MS-NET VT protocols supported
- Both Server and Consumer functionality supported



PRINT SPOOLING

- Interface through "rprint"
- Supports Core printer spooling protocol

UNIX STANDARD INTERFACE

- Interface via AT&T supplied TLI (Streams) library, allowing all TLI applications to interoperate with SV-OpenNET
- SV-OpenNET provides a library, NSI, for high-level Virtual Circuit (VC) creation and name to address translation. The NSI then communicates directly with the UNIX TLI

HOST REQUIREMENTS

Intel SYSTEM V.3.1 UNIX Operating System on MULTIBUS I or MULTIBUS II

PRODUCT CODES

SVNET552A	SV-OpenNET with iSBC 552A on MULTIBUS I
SVNET530	SV-OpenNET with iSBC 186/530 on MULTIBUS II

MAP/TOP OpenNET™ NETWORKING SOFTWARE

ISO/OSI CONFORMANT NETWORK SOFTWARE

Intel's MAPNET™ provides all seven layers of the industry-standard ISO/OSI specification for both Broadband (IEEE 802.4) and Ethernet (IEEE 802.3) environments.

The MAPNET software comes preconfigured or configurable to allow the OEM to change parameters as necessary. In addition, MAPNET provides multiple implementation methods (MAP on Broadband, MAP on Ethernet, and the coexistence of Broadband and Ethernet) to get started with MAP. The open software architecture allows an easy port to other operating systems and hardware.

PRECONFIGURED MAP21SXM

The preconfigured form (MAP21SXM) provides ISO/OSI Layers 3 through 7 of the MAP2.1 specification. It is preconfigured with iNA 960 to run on Intel's iSBC-554 IEEE 802.4 Token Bus MAP board to provide a seven layer solution. The preconfigured MAP21SXM software product is supplied with iRMX device drivers, user interface utilities, and the conformance tested MAPNET software.

CONFIGURABLE MAPNET21

The configurable MAPNET21 implements layers 5 through 7 of the MAP2.1 specification. MAPNET21 is designed to interface with iNA 960 and the iSBC-554 to provide a complete seven layer configurable MAP solution for OEMs.

FEATURES

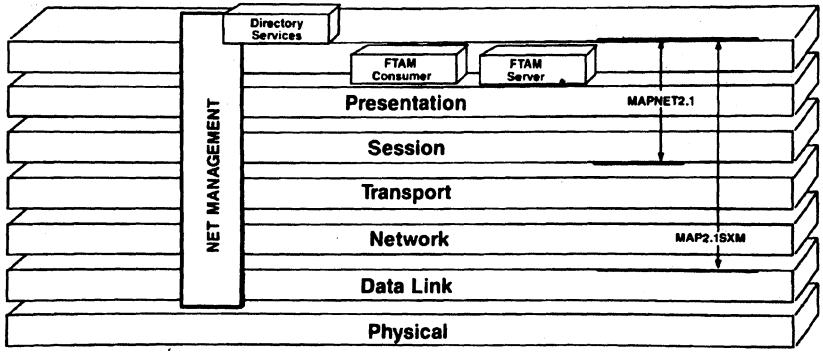
The MAPNET products provide session services, directory services, network management, FTAM, and CASE as specified in the MAP2.1 specification.

Using the services of MAPNET, users can initiate communications with other users on a MAP network, access information regarding resources available on the network, transfer files across the network, and address others by logical names rather than numbered addresses.

The Manufacturing Messaging Specification (RS-511 or MMS) for MAPNET on iRMX-86 is also available from independent software vendors.

PRODUCT CODES

MAPNET21	Configurable ISO/OSI Layers 5 through 7 of the MAP2.1
MAP21SXMR0	Preconfigured ISO/OSI Layers 3 through 7 of the MAP2.1



iNA 960 OpenNET™ NETWORKING SOFTWARE

FULLY COMPLIANT ISO/OSI TRANSPORT AND NETWORK

iNA 960 is a complete Network and Transport (ISO/OSI Layers 3 and 4) software system plus a comprehensive set of network management functions. Data Link (OSI Layer 2) drivers for IEEE 802.3 Ethernet and IEEE 802.4 Token Bus (MAP), and system environment features.

FLEXIBLE AND HIGHLY CONFIGURABLE

iNA 960 is a mature, flexible, and ready-to-use software building block for OEM suppliers of networked systems for both manufacturing and office applications (e.g., MAP and TOP).

This software is highly configurable for designs based on the 82586 and 82588 LAN controllers, 82501 and 82502 Ethernet serial interface and transceiver, and the 8086 family of microprocessors.

CONFIGURABLE AT THE OBJECT CODE LEVEL

Consisting of linkable object modules, the iNA 960 software can be configured to implement a range of capabilities and interface protocols. iNA 960 has a large installed base and has been used reliably in a variety of systems from IBM PC XT/ATs to VAX/VMS to IBM mainframes.

BASED ON INTERNATIONAL STANDARDS

Based on the ISO/OSI seven layer model for network communications, iNA 960 implements ISO 8073 Transport Class 4 providing reliable full-duplex message delivery service on top of the internet capabilities offered by the network layer. The iNA 960 network layer is an implementation of the ISO 8473 Network Class 3 Connectionless Network Protocol and supports ISO 9542 End System to Intermediate System Network Dynamic Routing. iNA 960 also supports ISO 8602 Connectionless Transport Protocol (Datagram).

PRECONFIGURED iNA 961

iNA 960 contains the preconfigured iNA 961 which includes support for the iSBC 552A, iSBC 186/530, and the iSBC 554.

REMOTE BOOT SERVER SUPPORT

iNA 960 provides basic boot server capabilities that will transmit predefined images to diskless network nodes that request them.

MULTI-SERVER/CONSUMER SUPPORT

iNA 960 supports the powerful MULTIBUS II feature of multiple host and communications boards. Ideal for LAN load balancing and redundant networks for fault-tolerant systems.

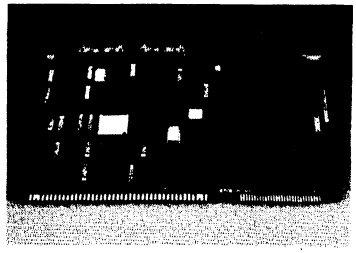
FEATURES

- Certified ISO/OSI Transport and Network Layer Software
- ISO 8072/8073 Transport Class 4
- ISO 8602 Connectionless Transport
- ISO 8348/8473 Connectionless Network
- ISO 9542 End System to Intermediate System Dynamic Routing
- Comprehensive Network Management Functions
- Remote Boot Server for diskless workstations
- Data Link Drivers for iSBC 552A, iSBX 586, iSBC 186/530, iSBC 554, and iSBC 186/51

PRODUCT CODES

INA960J	Includes INA 961 on RMX diskette format

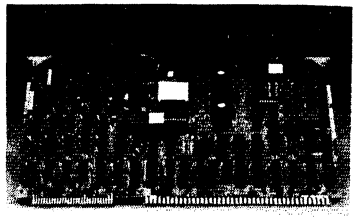
iSBC® 186/51 MULTIBUS I IEEE 802.3/ETHERNET COMMUNICATION COMPUTER



- 82586 LAN coprocessor for Ethernet/IEEE 802.3 communication
- Two serial interfaces, RS232C and RS422A/RS449 compatible
- 6 MHz 80186 microprocessor
- 128K bytes of dual-port RAM expandable on-board to 256K bytes
- Sockets for up to 192K bytes of JEDEC 28-pin standard memory devices
- Product Code: sSBC18651

CPU	80186 (6 MHz)
RAM (Bytes)	128K/256K dual port
EPROM (Bytes)	192K (27256), 96K (27128), 48K (2764), 4K (2732)
Serial I/O	2 ports, 26-pin 3M connector (RS232C/422A/449)
Ethernet I/O	1 port, 10-pin AMP connector
Baud rates (RS232/422/449)	75–9600 baud (async.) 1.76–38.4K baud (sync.)
Timers	3
Interrupts	9 levels, 28 sources
iSBX™ Connectors	2
Software Support	iRMX® 86 O.S., iNA 960, iRMX®-NET
Power Requirements +5V	7.45 A
+12V	40 mA
−12V	40 mA

iSBC®/iSXM™ 552A MULTIBUS I IEEE 802.3/ETHERNET NETWORK INTERFACE ADAPTER

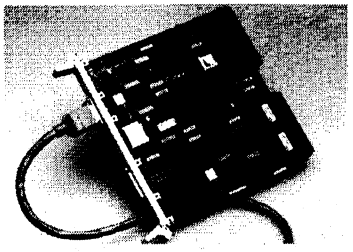


- High Performance IEEE 802.3/Ethernet compatible network front-end processor
- Resident network software can be downloaded over the bus or the LAN
- On-board diagnostic and boot firmware
- iSXM™ 552A version is a preconfigured controller for executing iNA 961 (ISO 8073 Transport and ISO 8473 Network software) in System 310 and 320 family products
- Product Code: pSBC552A, pSXM552A

CPU	80186 (8 MHz)
LAN Coprocessor	82586
RAM (Bytes)	256K
EPROM (Bytes)	128K (27512), 16K (2764)
MULTIBUS® Address	Any 64 KB boundary with a 16 MB address space
Software Support	iNA 960/961
Power Requirements +5V	6.2 A
+12V	0.5 A

MULTIBUS®II OpenNET™ NETWORKING HARDWARE

iSBC® 186/530 MULTIBUS®II IEEE 802.3/ETHERNET NETWORK INTERFACE ADAPTER

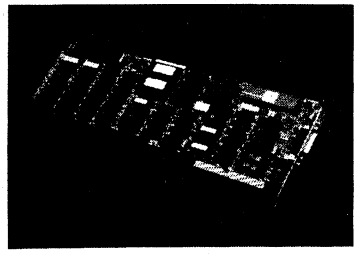


- Provides Ethernet® (IEEE 802.3) compatible networking capability for all MULTIBUS®II systems
- MULTIBUS®II iPSB (Parallel System Bus) interface with full Message Passing capability
- Resident firmware to support Built-in-Self-Test (BIST) power-up diagnostics, and host-to-controller software download
- Four 28-pin JEDEC sites, expandable to 8 sites with iSBC® 341 MULTIMODULE® for a maximum of 512K bytes of EPROM
- Provides one RS232C serial port for use in debug and testing
- Product Code: pSBC186530

CPU		80186 (8 MHz)
DRAM		512 KB on-board
EPROM		4 28-pin JEDEC sites, up to 256 KB (max.) using 27512 devices, up to 512 KB (total) using iSBC® 341 module
Ethernet I/O		1 channel 15-pin connector
	Controller	82586 LAN Coprocessor
Serial I/O		1 channel RS232C, 15-pin connector
	Controller	8031
	Leads Supported	TD, RD
Timers		3
Interrupts		5 levels with 5 on-board sources and 255 sources from iPSB Bus
Power Requirements	+5V	8.8 A (excludes power for user-installed memory devices)
	+12V	50 mA
	−12V	50 mA

PC BUS OpenNET™ NETWORKING HARDWARE

PC LINK2 NETWORK INTERFACE ADAPTER (PC LINK2 NIA)

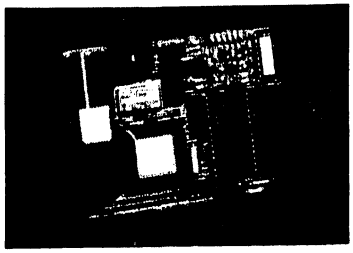


CPU		80186 (8 MHz)
LAN Communications Controller		82586
Ethernet Interface		15-pin connector, 82501 serial interface
DRAM		256 KB (dual-port), 0 wait-state memory access by the CPU
EPROM		16 KB
Size		4.15 in H x 13.3 in W
Power Requirements	+5V	2.0 A
	+12V	0.5 A

- Intelligent high performance hardware with on-board microprocessor, 16K bytes EPROM and 256K bytes RAM.
- Full slot PC AT, PC XT (or compatible computer system) board
- 80186 microprocessor, 82586 LAN coprocessor, 8 MHz zero-wait-state memory access.
- RAM shared by the PC host and PC Link2 board via an 8K memory window.
- Jumper selection for Ethernet or IEEE 802.3.
- Effective self diagnostics.
- Product Code: sPCLINK2NIA

OpenNET™ NETWORKING ACCESSORIES

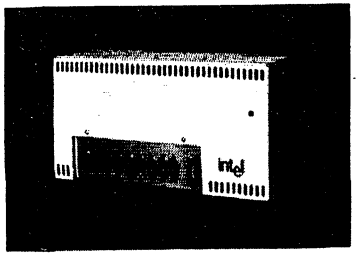
iSBX™ 586 DATA LINK ENGINE MULTIMODULE® BOARD



LAN Coprocessor ..... 82586 (8 MHz)
RAM (Bytes) ..... 16K (dual-port)
Software Support ..... iNA 960/961
Power Requirements +5V ..... 2.0 A
+12V ..... 1.0 A

- Provides an IEEE 802.3/Ethernet compatible connection for 8086 and 80186-based host boards over a 16-bit iSBX™ interface
- Single-wide iSBX™ MULTIMODULE™
- Compatible with iNA 960/961 ISO 8073 Transport and ISO 8473 Network software
- Provides an IEEE 802.3 to IEEE 802.4 Router capability when used with the iSBC® 554 IEEE 802.4 LAN controller
- Product Code: sSBX586

iDCM 911-1 INTELLINK™ FAN-OUT UNIT



Size ..... 14 in. W x 7.8 in. H x 5.5 in. D
Power Requirements ..... 100/120/220/240 VAC, 47–64 Hz

- Connects up to nine Ethernet compatible workstations without the need for transceivers or coaxial cable
- Connects directly to the Ethernet coaxial cable through a standard transceiver cable
- Cascadable to support 17–81 workstations
- Product Code: pDCM9111

ETHERNET/IEEE 802.3 THIN-WIRE TRANSCEIVER

Size ..... 2.8 in. x 3.6 in. x 3.8 in.
Power Requirements +12V ..... .375 mA
(from transceiver cable)

- Die-cast metal case for protection, reduced EMI, and efficient heat dissipation
- Low inrush current at power-up, auto shutdown when low-input voltage occurs, and surge protection
- IEEE 802.3-compliant, Ethernet V1.0/V2.0 compatible
- Three LEDs monitor power status, packet collisions and signal quality
- Removable BNC type cable tap
- User-configurable for use with or without heartbeat
- Product Code: CNETXCVR

OpenNET™ NETWORKING ORDERING INFORMATION

Code	Description
iRMX-NET OpenNET PRODUCTS	
RMXINET	iRMX-NET for iRMX 86 operating system
RMXIINET	iRMX-NET for iRMX II operating system
PCLINK2 OpenNET PRODUCTS	
sPCLINK2NIA	PC Link2 Network Interface Adapter Hardware only
sPCLINK2	Seven-layer Solution with sPCLINK2NIA, iNA961, NetBIOS interface, MS-NET
sPCLINKIIBD	Five-layer Solution with sPCLINK2NIA, iNA961, NetBIOS interface
sPCLINK2TWKIT	Seven-layer Thin-wire Solution with sPCLINK2, CNETXCVR, XCVRCBL-5
sPCLINK2DEVKIT	NetBIOS Developer's Kit with 2-sPCLINK2CNETKITs, NetBIOS programmer kit
PCLDOSRBIRO	Request Block Developer's Software with iNA 961 for PCLINK2
PCLDOSRBIRF	Royalty fee for PCLDOSDRBIRO
PCLNKSWUPRO	iNA961 R1 to R2 migration software for PC Link and R1 to R3 for PC Link2
PCLNKSWUPRF	Royalty fee for PCLNKSWUPRO
VAX/VMS OpenNET PRODUCTS	
VMSNET	Networking Software for VAX family
MVMSNET	VAX/VMS Networking Software for MicroVAX II
UNIX SYSTEM V OpenNET PRODUCTS	
SVNET552A	UNIX SV-OpenNET with iSBC 552A on MULTIBUS I
SVNET530	UNIX SV-OpenNET with iSBC 186/530 on MULTIBUS II
MAP/TOP OpenNET PRODUCTS	
MAPNET21	Configurable ISO/OSI Layers 5 through 7 of the MAP2.1
MAPNET21RF	Royalty fee for MAPNET21
MAP21SXMRO	Preconfigured ISO/OSI Layers 3 through 7 of the MAP2.1, includes license
MAP21SXMRF	Royalty fee for MAP21SXM
SBC5541	iSBC554-1 MULTIBUS I MAP Communications Engine, Xmit: CH 3', 4' Rcv: CH P, Q
SBC5543	iSBC554-3 MULTIBUS I MAP Communications Engine, Xmit: CH6', FM1' Rcv: CH T, U
iNA 960 OpenNET ISO/OSI PRODUCTS	
INA960J	ISO/OSI Transport and Network layers, includes iNA961
INA960RF	Royalty fee for INA960
MULTIBUS I AND MULTIBUS II IEEE 802.3/ETHERNET PRODUCTS	
sSBC18651	iSBC 186/51 MULTIBUS I IEEE 802.3/Ethernet Communication Computer
pSBC552A	iSBC 552A MULTIBUS I IEEE 802.3/Ethernet Network Interface Adapter
pSXM552A	iSBC 552A preconfigured for Intel System 310 and 320, includes iNA 961 royalty
pSBC186530	iSBC 186/530 MULTIBUS II IEEE 802.3/Ethernet Network Interface Adapter
OpenNET NETWORKING ACCESSORIES	
sSBX586	iSBX 586 MULTIMODULE IEEE 802.3/Ethernet Data Link board
pDCM9111	iDCM 911-1 Intellink Fan-out Unit
CNETXCVR	Thin-wire transceiver. Requires transceiver cable (XCVRCBL-5)
XCVRCBL-5	Five-foot transceiver cable

OpenNET™ NETWORKING LITERATURE

Code	Description
iRMX-NET OpenNET PRODUCTS	
462040-001	iRMX-NET Software Release 3.0 Installation and Configuration Guide
462041-001	iRMX-NET Software Release 3.0 User's Guide
PCLINK2 OpenNET PRODUCTS	
460665-001	MS-NET User's Guide
450772-001	PCLINK2 Hardware Reference Manual
462305-001	PCLINK2 NIA Hardware Installation Guide
462311-001	PCLINK2 Software Developer's Manual
462308-001	PCLINK R3.0 Software For DOS—Installation Guide
VAX/VMS OpenNET PRODUCTS	
480071-001	VAX/VMS OpenNET User's Manual
UNIX SYSTEM V OpenNET PRODUCTS	
462740-001	SV-OpenNET User's Manual
462741-001	SV-OpenNET Installation and Administration Guide
MAP/TOP OpenNET PRODUCTS	
461298-001	MAPNET User's Guide
454209-001	iSBC 554 Network Interface Adapter Hardware Reference Manual
460432-001	MAP Broadband Starter Kit Guide
iNA 960 OpenNET ISO/OSI PRODUCTS	
462250-001	iNA 960 R3 Programmer's Reference Manual
462252-001	iNA 960 R3 Installation and Configuration Guide
MULTIBUS I AND MULTIBUS II IEEE 802.3/ETHERNET PRODUCTS	
122330-001	iSBC 186/51 COMMputer Board Hardware Reference Manual
149228-001	iSBC 552A IEEE 802.3 Communications Controller User's Guide
149226-002	iSBC 186/530 Network Interface Adapter User's Guide
OpenNET NETWORKING ACCESSORIES	
122290-001	iSBX 586 MULTIMODULE Ethernet Communication Controller Hardware Reference Manual
122074-002	iDCM 911-1 Intellink Cluster Module Reference Manual
280665-001	Ethernet/IEEE 802.3 Thin-wire Transceiver Factsheet

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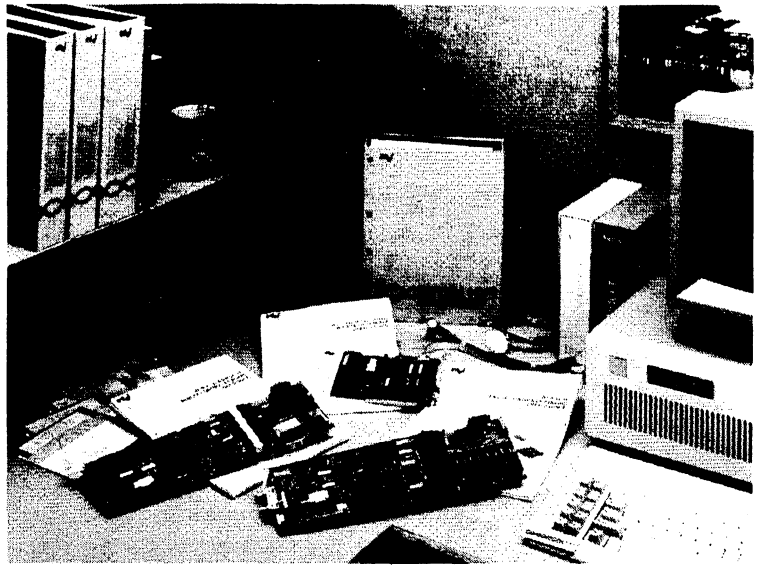
Distributed Control Modules 18



A COMPLETE BITBUS™ NETWORK YOU CAN HAVE UP AND RUNNING IN TWO HOURS

The BITBUS™ Starter Kit is a complete hardware/software kit containing BITBUS analog and digital boards, tailored application software, and all the accessories (e.g., power supply and cables) required to set up a simple but functional BITBUS network. A first-time user can construct a BITBUS network and execute sample application programs within two hours of opening the box. He can then incorporate this basic network into his own distributed control application.

FEATURES:

- Self-contained BITBUS kit requiring only an IBM PC or compatible host.
- BITBUS analog and digital boards, plus PC Gateway to the BITBUS network.
- Sample application software with built-in installation, configuration, and diagnostic software.
- No BITBUS experience necessary.

REAL-TIME INTERCONNECT FOR DISTRIBUTED CONTROL

The Intel BITBUS network provides the optimal solution for building real-time distributed control systems. The BITBUS serial bus architecture overcomes many of the limitations inherent in traditional industrial connection methods to give you increased performance, reliability, and flexibility and lower implementation costs.

DESIGNED FOR FIRST-TIME BITBUS USERS

The BITBUS Starter Kit is the ideal way for first-time BITBUS users to learn about the BITBUS architecture. Shortly after unpacking this kit, you can be confidently executing your first BITBUS distributed control application.

EVERYTHING YOU NEED

Based on standard Intel products, the BITBUS Starter Kit includes the BITBUS analog board, the BITBUS digital board, the PC Gateway into the BITBUS network, power supply and cables. Supporting the standard product are demonstration boards that the user can manipulate to display analog or digital functionality.

BUILT-IN INSTALLATION AND DIAGNOSTIC SOFTWARE

Application software included with the BITBUS Starter Kit provides network setup information, as well as comprehensive error-checking software to verify that the network is configured correctly. If there is an error, the software directs you to the problem and suggests a correction. Once the network is working properly, the software steps you through optional configurations, from a host-based centralized control system to a node-based distributed control scheme. Each configuration allows you to interact with the network.

SERVICE, SUPPORT AND TRAINING

Intel provides worldwide support for repair, on-site service, network design, and installation. Development support options include phone support, subscription service, on-site consulting, and customer training.

INTEL QUALITY AND RELIABILITY

The BITBUS Starter Kit is designed and manufactured in accordance with Intel's high quality standards. We then verify quality through rigorous testing in our state-of-the-art Environmental Test Laboratory.

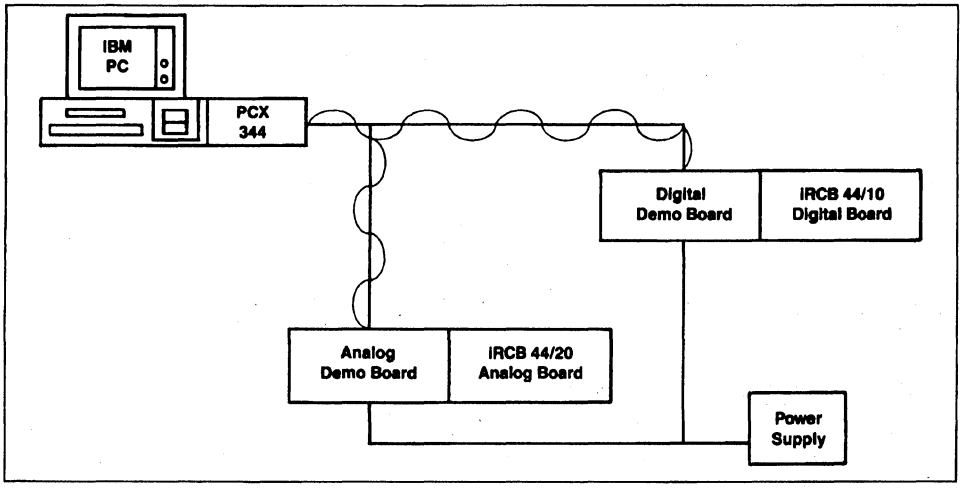


Figure 1: BITBUS Starter Kit

ORDERING INFORMATION

Product Code	Qty	Product Content
BITBUSKIT		Basic Starter Kit which includes the following items:
	1	BITBUS Starter Kit User's Guide
		HARDWARE
	1	iPCX 344A—BITBUS IBM PC Interface Board—PC Gateway to BITBUS Network
	1	iRCB 4410A—BITBUS Digital I/O Remote Controller Board
	1	iRCB 4420A—BITBUS Analog I/O Remote Controller Board
	1	Digital Demonstration Board
	1	Analog Demonstration Board
	1	Power Supply, 25 Watt, UL, VDE, CSA approved
	1	Required Cables, SRAMS, Jumpers, etc.
		SOFTWARE
	1	iDCS100—BITBUS Toolbox—The set of six software utilities that simplify development of host application software
	1	iDCS110—Bitware—iDCX 51 interface library and declaration files
	1	Starter Kit Application Software
BITBUSKITPLUS		Expanded version of the BITBUSKIT providing programming languages used to develop host (8086 environment) and node code (8051 environment) in addition to the basic BITBUS network.

SPECIFICATIONS

Table 1. Standard BITBUS™ Interfaces

Interface	Specification
Electrical	RS485
Cable	10-conductor flat ribbon or 1 to 2 wire shielded twisted pair
Back-plane connector	64-pin Standard DIN
Control-board form-factor	Single-height, Double-depth Eurocard
Data Link control	Synchronous Data-link Control (SDLC)
Data transfer rate	62.5K baud, 375K baud and 500K to 2.4M baud
Message formats	Compatible with iDCX format command/response/status
Common command sequences	Integral Remote Access and Control (RAC) function
Operating systems	Interface libraries for iRMX 86, 88, 286R, MS-DOS, and ISIS (for iPDS only)

Table 2. BITBUS™ Microcontroller Interconnect Modes Of Operation

	Speed Kb/S	Maximum Distance Between Repeaters M/ft	Maximum # Nodes Per Segment*	Maximum # Repeaters Between A Master And Any Slave
Synchronous	500–2400	30/100	28	0
Self Clocked	375 62.5	300/1000 1200/4000	28 28	2 10

RELATED LITERATURE

iPCX 344A fact sheet
(Order #: 280414-002)

iRCB 44/10A fact sheet
(Order #: 280213-003)

iRCB 44/20A fact sheet
(Order #: 280721-2)

BITBUS Software Development Environment fact sheet
(Order #: 280622-001)

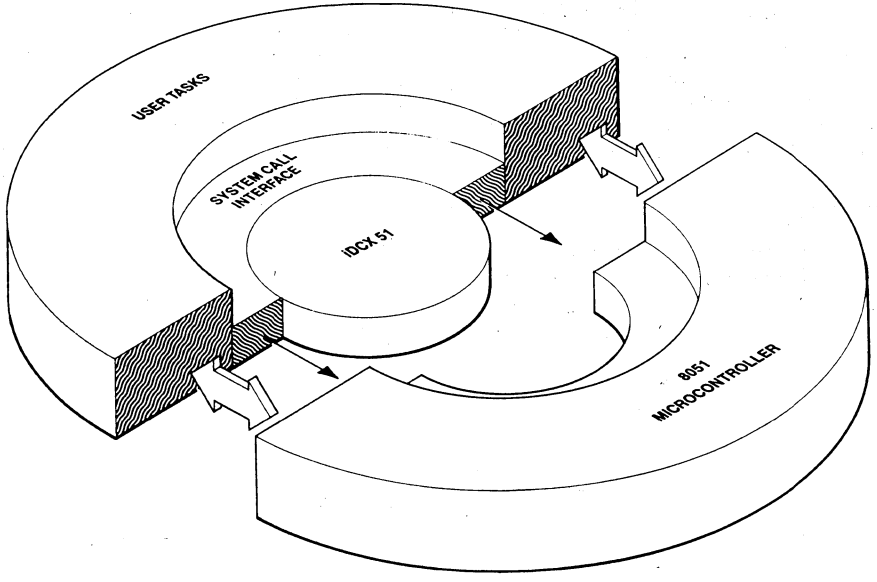
iDCX 51
DISTRIBUTED CONTROL EXECUTIVE

- **Supports MCS®-51 and RUPI™-44 Familes of 8-Bit Microcontrollers**
- **Real-Time, Multitasking Executive — Supports up to 8 Tasks at Four Priority Levels**
- **Local and Remote Task Communication**
- **Small—2.2K Bytes**
- **Reliable**
- **Simple User Interface**
- **Dynamic Reconfiguration Capability**
- **Compatible with BITBUS™/Distributed Control Modules (iDCM) Product Line**

The iDCX 51 Executive is compact, easy to use software for development and implementation of applications using the high performance 8-bit family of 8051 microcontrollers, including the 8051, 8044, and 8052. Like the 8051 family, the iDCX 51 Executive is tuned for real-time control applications requiring manipulation and scheduling of more than one task, and fast response to external stimuli.

The MCS-51 microcontroller family coupled with iDCX 51 is a natural combination for applications such as data acquisition and monitoring, process control, robotics, and machine control. The iDCX 51 Executive can significantly reduce applications development time, particularly BITBUS distributed control environments.

The iDCX 51 Executive is available in two forms, either as configurable software on diskette or as preconfigured firmware within the 8044 BEM BITBUS microcontroller.



280176-1

Figure 1. iDCX 51 Distributed Control Executive

*XENIX™ is a trademark of Microsoft Corporation.

October 1987
Order Number: 280176-003

MICROCONTROLLER SUPPORT

The iDCX 51 Executive is designed to support the MCS-51 and RUPI-44 families of 8-bit microcontrollers. MCS-51 microcontrollers that are supported include the 8051, 80C51, 8052, 8031, 8032, and 8751 devices. The RUPI-44 microcontrollers include the 8044, 8344, and 8744 devices. All of these microcontrollers share a common 8051 core.

ARCHITECTURE

Real-time and Multitasking

Real-time control applications must be responsive to the external environment and typically involve the execution of more than one activity (task or set of tasks) in response to different external stimuli. Control of an industrial drying process is an example. This process could require monitoring of multiple temperatures and humidity; control of fans, heaters, and motors that must respond accordingly to a variety of inputs. The iDCX 51 Executive fully supports applications requiring response to stimuli as they occur, i.e., in real-time. This real-time response is supported for multiple tasks often needed to implement a control application.

Some of the facilities precisely tailored for development and implementation of real-time control application systems provided by the iDCX 51 Executive are: task management, interrupt handling, message passing, and when integrated with communications support, message passing with different microcontrollers. Also, the iDCX 51 Executive is driven by events: interrupts, timers, and messages ensuring the application system always responds to the environment appropriately.

Task Management

A task is a program defined by the user to execute a particular control function or functions. Multiple programs or tasks may be required to implement a particular function such as "controlling Heater 1". The iDCX 51 Executive recognizes three different task states as one of the mechanisms to accomplish scheduling of up to eight tasks. Figure 2 illustrates the different task states and their relationship to one another.

The scheduling of tasks is priority based. The user can prioritize tasks tc reflect their relative importance within the overa'l control scheme. For instance, if Heater 1 must go off line prior to Heater 2 then the task associated with Heater 1 shutdown could be assigned a higher priority ensuring the correct shutdown sequence. The RQ WAIT system call is also a scheduling tool. In this example the task implementing Heater 2 shutdown could include an instruction to wait for completion of the task that implements Heater 1 shutdown.

The iDCX 51 Executive allows for PREEMPTION of a task that is currently being executed. This means that if some external event occurs such as a catastrophic failure of Heater 1, a higher priority task associated with the interrupt, message, or timeout resulting from the failure will preempt the running task. Preemption ensures the emergency will be responded to immediately. This is crucial for real-time control application systems.

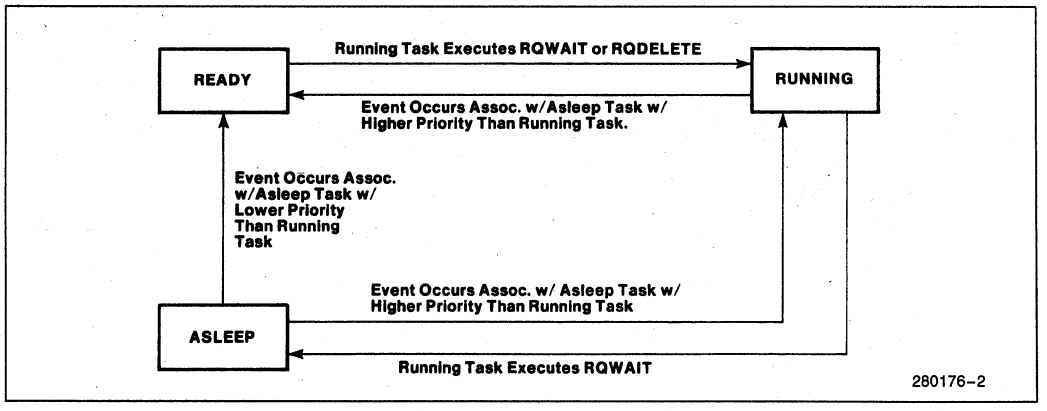


Figure 2. Task State Transition Diagram

Interrupt Handling

The iDCX 51 Executive supports five interrupt sources as shown in Table 1. Four of these interrupt sources, excluding timer 0, can be assigned to a task. When one of the interrupts occurs the task associated with it becomes a running task (if it were the highest priority task in a ready state). In this way, the iDCX 51 Executive responds to a number of internal and external stimuli including time intervals designed by the user.

Table 1. iDCX 51 Interrupt Sources

Interrupt Source	Interrupt Number
External Request 0	00H
Timer 0	01H
External Request 1	02H
Timer 1	03H
Internal Serial Port 1	04H

Message Passing

The iDCX 51 Executive allows tasks to interface with one another via a simple message passing facility. This message passing facility can be extended to different processors when communications support is integrated within a BITBUS/iDCM system, for example. This facility provides the user with the ability to link different functions or tasks. Linkage between tasks/functions is typically required to support development of complex control applications with multiple sensors (input variables) and drivers (output variables). For instance, the industrial drying process might require a dozen temperature inputs, six moisture readings, and control of: three fans, two conveyor motors, a dryer motor, and a pneumatic conveyor. The data gathered from both the temperature and humidity sensors could be processed. Two tasks might be required to gather the data and process it. One task could perform a part of the analysis, then include a pointer to the next task to complete the next part of the analysis. The tasks could continue to move between one another.

REMOTE TASK COMMUNICATION

The iDCX 51 Executive system calls can support communication to tasks on remote controllers. This feature makes the iDCX 51 Executive ideal for applications using distributed architectures. Providing communication support saves significant application development time and allows for more effective use of this time. Intel's iDCM product line combines hardware and software to provide this function.

In an iDCM system, communication between nodes occurs via the BITBUS microcontroller interconnect. The BITBUS microcontroller interconnect is a high performance serial control bus specifically intended for use in applications built on distributed architectures. The iDCX 51 Executive provides BITBUS support.

BITBUS™/iDCM COMPATIBLE

A pre-configured version of the iDCX 51 Executive implements the BITBUS message format and provides all iDCX 51 facilities mentioned previously: task management, interrupt handling, and message passing. This version of the Executive is supplied in firmware on the 8044 BEM with the iDCM hardware products: the iSBX™ 344A BITBUS Controller MULTIMODULE™; the iDCX 344A BITBUS controller board for the PC; and the iRCB boards.

Designers who want to use the iDCX executive on an Intel BITBUS board should purchase either DCS110 or DSC120 BITBUS software. Both of these products include an interface library to iDCX 51 procedures and other development files. It is not necessary to purchase the iDCX 51 Executive.

SIMPLE USER INTERFACE

The iDCX 51 Executive's capabilities are utlilized through system calls. These interfaces have been defined for ease of use and simplicity. Table 2 includes a listing of these calls and their functions. Note that tasks may be created at system initialization or run-time using the CREATE TASK call.

Other Functions such as GET FUNCTION IDS, ALLOCATE/DEALLOCATE BUFFER, and SEND MESSAGE, support communication for distributed architectures.

Table 2. iDCX 51 System Calls

Call Name	Description
TASK MANAGEMENT CALLS	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION$IDS	Obtain the function IDs of tasks currently in the system.
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.
MEMORY MANAGEMENT CALLS	
RQGETMEM	Get available system memory pool memory.
RQ$RELEASE$MEM	Release system memory pool memory.
INTERRUPT MANAGEMENT CALLS	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RQ$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
TIMER MANAGEMENT CALLS	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

Another feature that eases application development is automatic register bank allocation. The Executive will assign tasks to register banks automatically unless a specific request is made. The iDCX 51 Executive keeps track of the register assignments allowing the user to concentrate on other activities.

SYSTEM CONFIGURATION

The user configures an iDCX 51 system simply by specifying the initial set of task descriptors and configuration values, and linking the system via the RL 51 Linker and Locator Program with user programs.

Each task that will be running under control of the executive has an Initial Task Description (ITD) that describes it. The ITD specifies to the executive the amount of stack space to reserve, the priority level of the task (1–4), the internal memory register bank to be associated with the task, the internal or external interrupt associated with the task, and a function ID (assigned by the user) that uniquely labels the task. The ITD can also include a pointer to the ITD for the next task. In this way an ITD "chain" can be formed. For example, if four ITD's are chained together, then when the system is initialized, all four tasks will be put into a READY state. Then, the highest priority task will run.

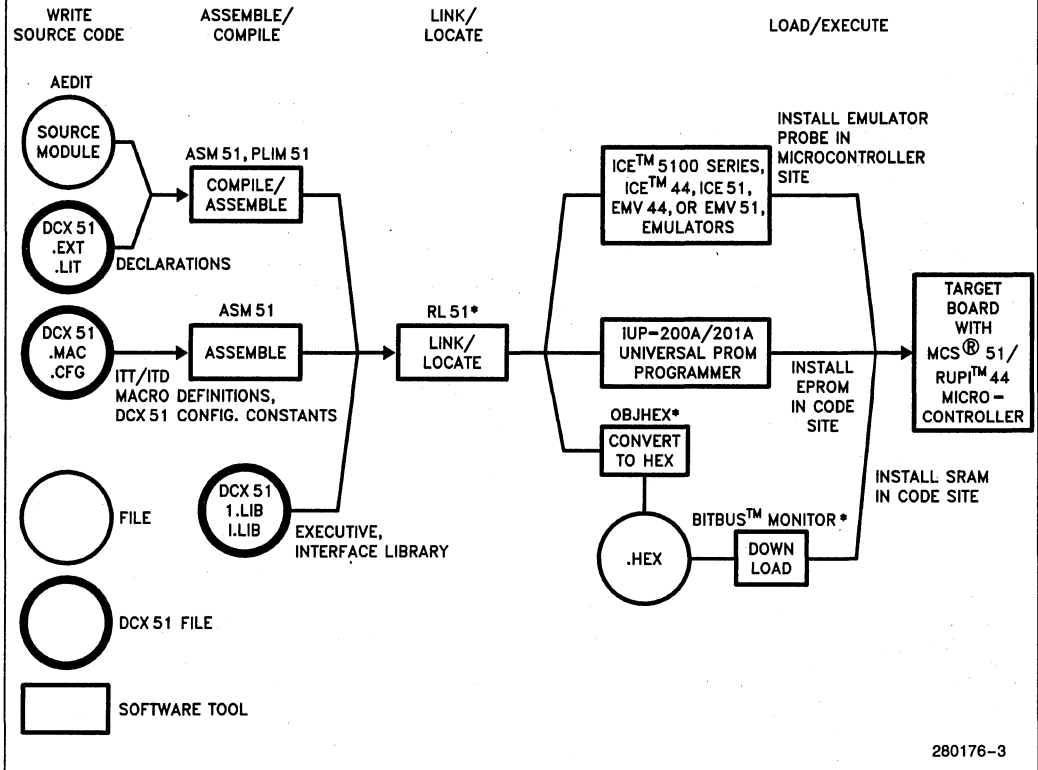
The DCX 51 user can control several system constants during the configuration process (Table 3). Most of these constants are fixed, but by including an Initial Data Descriptor (IDD) in an ITD chain, the system clock priority, clock time unit, and buffer size can be modified at run-time.

This feature is useful for products that use the same software core, but need minor modification of the executive to better match the end application. The initial data descriptor also allows the designer, who is using an 8044 BEM BITBUS Microcontroller, to modify the preconfigured (on-chip) iDCX 51 Executive.

Programs may be written in ASM 51 or PL/M 51. Intel's 8051 Software Development Package contains both ASM 51 and RL 51. Figure 3 shows the software generation process.

Table 3. DCX 51 Configuration Constants

Constant Name	Description
RQ CLOCK PRIORITY	The priority level of the system clock.
RQ CLOCK TICK	The number of time cycles in the system clock basic time unit (a "tick").
RQ FIRST ITD	The absolute address of the first ITD in the ITD chain.
RQ MEM POOL ADR	The start address of the System Memory Pool (SMP) in Internal Data RAM.
RQ MEM POOL LEN	The length of the SMP.
RQ RAM IDD	The absolute RAM address of where iDCX 51 checks for an Initial Data Descriptor (IDD) during initialization.
RQ SYS BUF SIZE	The size, in bytes, of each buffer in the system buffer pool.



NOTE:
*RL 51 is included with ASM51 and PL/M 51; OBJHEX and the BITBUS Monitor are part of the DCS100 BITBUS Toolbox.

Figure 3. Software Generation Process

SOPHISTICATED INTERNAL MEMORY MANAGEMENT

The amount of internal memory available ranges from 128 to 256 bytes depending on the type of microcontroller used.

Internal memory is used for the executive, stack spare for "running" tasks, space for message buffers, and reserved memory for variables storage. Other memory is used for register space. Except for register space, the allocation of internal memory is controlled by the executive, user-specified task/data descriptors and system configuration constants.

To optimize use of this limited resource, iDCX 51 provides dynamic (run-time) memory management.

INITIALIZATION AND DYNAMIC MEMORY MANAGEMENT

At initialization (see Figure 4), the iDCX 51 Executive creates the System Memory Pool (SMP) out of the remaining initial free space (i.e. memory not used by the iDCX 51 Executive or for register space). Next, stack space is created for each of the initial tasks that will be running on the system. If reserved memory is requested (using an IDD), that memory is also set aside. Finally, multiple buffers (size specified during iDCX 51 configuration or using an IDD) are allocated from any remaining memory. These buffers form the System Buffer Pool (SBP) that can be used to create additional stack space or to locate messages sent between tasks.

During run-time, the iDCX 51 Executive dynamically manages this space. If a task is deleted, its stack space is returned to the System Buffer Pool for use by other tasks or as a message buffer.

As new tasks are dynamicallly created, the executive reserves the needed stack space. If no space is available, the executive deallocates a buffer from the System Buffer Pool and then allocates the needed stack space.

To send or receive a message, the executive allocates one or more buffers from the SBP for space to locate the message. With iDCX 51, messages can be optionally located in external (off-chip) memory. The pre-configured executive in the 8044 BEM BITBUS microcontroller, however, always locates messages in internal memory.

RELIABLE

Real-time control applications require reliability. The nucleus requires about 2.2K bytes of code space, 40 bytes on-chip RAM, and 218 bytes external RAM.

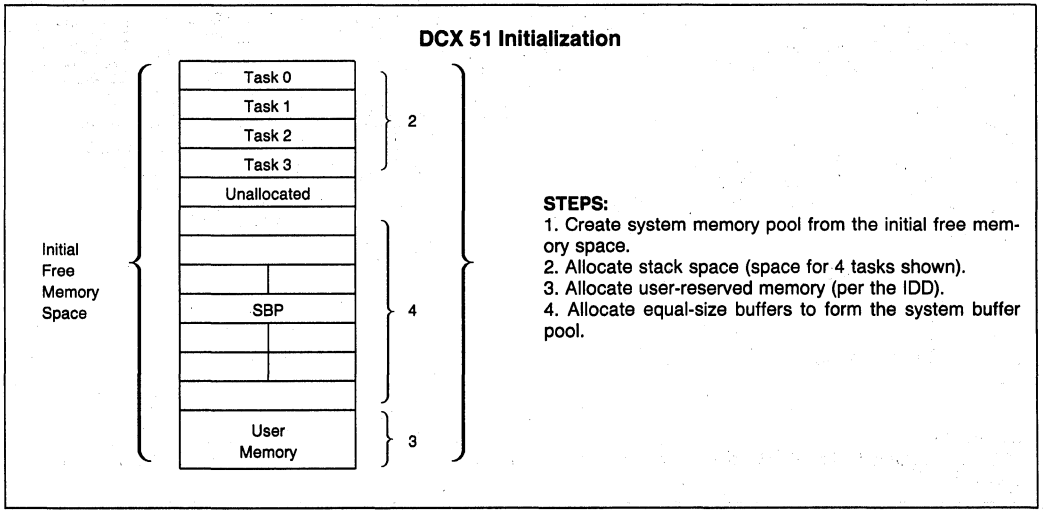


Figure 4. iDCX 51 Initialization of Internal Memory

Streamlined code increases performance and reliability, and flexibility is not sacrificed as code may be added to either on-chip or external memory.

The iDCX 51 architecture and simple user interface further enhance reliability and lower cost. For example, the straightforward structure of the user interfaces, and the transparent nature of the scheduling process contribute to reliability of the overall system by minimizing programming effort. Also, modularity increases reliability of the system and lowers cost by allowing user tasks to be refined independent of the system. In this way, errors are identified earlier and can be easily corrected in each isolated module.

In addition, users can assign tasks a Function ID that allows tracking of the tasks associated with a particular control/monitorig function. This feature reduces maintenance and trouble shooting time thus increasing system run time and decreasing cost.

OPERATING ENVIRONMENT

The iDCX 51 Executive supports applications development based on any member of the high performance 8051 family of microcontrollers. The Executive is available on diskette with user linkable libraries or in the 8044 BITBUS Enhanced Microcontroller preconfigured in on-chip ROM. (The 8044 BEM is an 8044 component that consists of an 8051 microcontroller and SDLC controller on one chip with integral firmware.)

When in the iDCM environment (Figure 5), the preconfigured iDCX 51 Executive can communicate with other BITBUS series controller boards. The BITBUS board at the master node can be associated with either an iRMX™, PC-DOS or XENIX* host system.

DEVELOPMENT ENVIRONMENT

Intel provides a complete development environment for the MCS-51 and RUPI-44 families of microcontrollers. The iDCX 51 Executive is only one of many of the software development products available. The executive is compatible with the following software development utilities available from Intel:

- 8051 Macro Assembler (ASM 51)
- PL/M 51 Compiler
- RL 51 Linker and Relocator Program
- LIB 51

Intel hardware development tools currently available for MCS-51 and RUPI-44 microcontroller development are:

- ICE-5100/252 Emulator for the MCS-51 family of microcontrollers
- ICE-5100/044 Emulator for the RUPI-44 family of microcontrollers (8044, 8344, 8744)
- iUP-200A/201A PROM Programmer, 21X software, and iUP programming modules

The DCX 51 Executive is also compatible with older hardware development tools (no longer available), which include:

- EMV-51/44 Emulation Vehicles
- ICE-51/44 In-Circuit Emulators

Table 4 shows the possible MCS-51 and RUPI-44 families development environments: host systems, operating systems, available software utilities, and hardware debug tools.

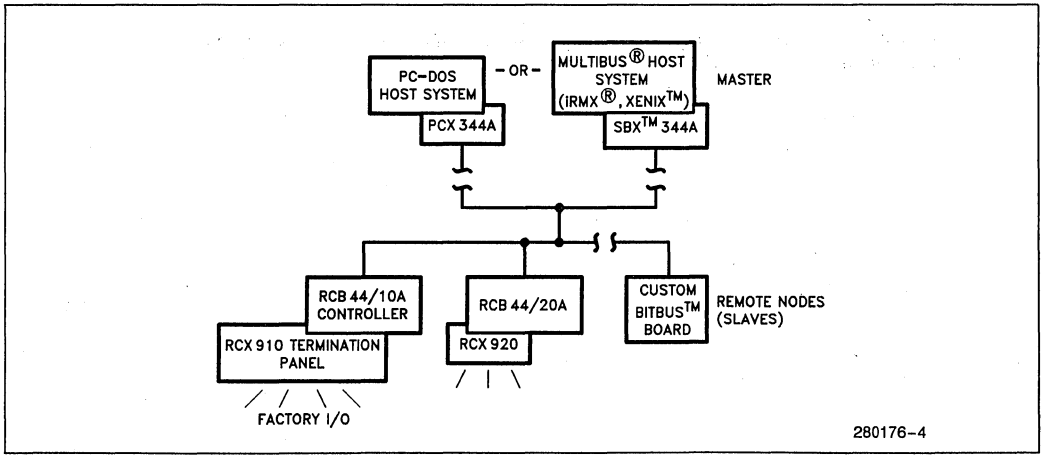


Figure 5. iDCM Operating Environment

SPECIFICATIONS

Supported Microcontrollers

8031	80C31
8051	80C51
8032	8751
8744	8044
8344	8052

Compatible DCM BITBUS™ Software

DCS 100 BITBUS Toolbox Host Software Utilities

DCS 110 BITWARE DCM44 Code for BITBUS emulation

Reference Manual (Supplied)

460367-001— iDCX 51 Distributes Control Executive User's Guide for Release 2.0.

ORDERING INFORMATION

Part Number	Description
DCX51SU	Executive for 8051 Family of Microcontrollers. Single User License, Development Only. Media Supplied for All Host Systems (Table 3).
DCX51RF	Royalty (Incorporation) Fee for iDCX Executive. Set of 50 incorporations. IDCX 51 RF does not ship with software (Order DCX 51SU).

Table 4. MCS®-51/RUPI™-44 Families Development Environments

Development Utilities	Host Systems				
	PC/MS-DOS	iRMX® 86	iPDS™	Intellec®	
				Series II	Series III/IV
SOFTWARE					
ASM 51 + Utilities(1)	✓	✓	✓	✓	✓
PL/M 51 + Utilities(1)	✓	✓	✓	✓	✓
iDCX 51 Executive	✓	✓	✓		✓
HARDWARE					
ICE-5100/044/252	✓				✓
iUP-200A/201A	✓				✓
EMV-51(2), EMV-44(2)				✓	✓
ICE-51(2), ICE-44(2)				✓	✓
iPDS + iUP-F87/44A PROM Programmer			✓		

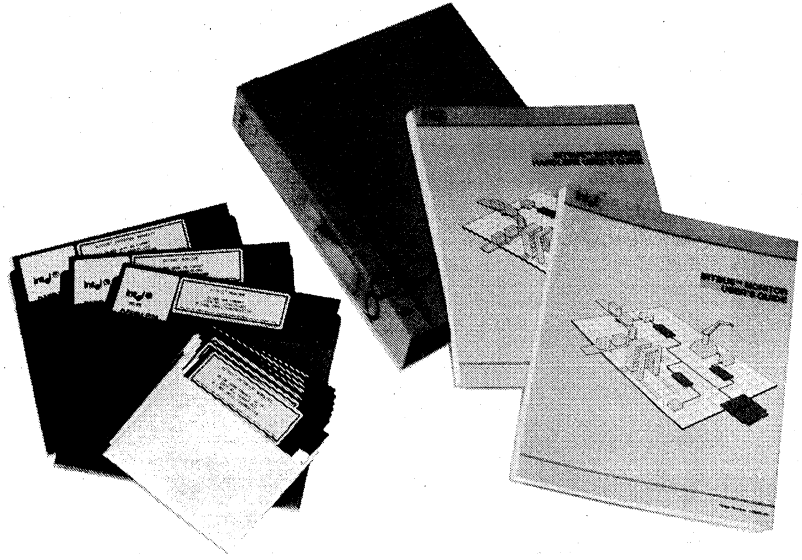
NOTES:
1. Utilities include RL 51, LIB 51, and AEDIT. Software for Series II systems is down-revision version.
2. These products are no longer available.

DCS100 BITBUS™ TOOLBOX HOST SOFTWARE UTILITIES

- **Six Utilities Simplify Development of Host Software for Controlling BITBUS™-Based Systems**
- **Includes the BITBUS™ Monitor Which Provides On-Line Monitoring and Control of a BITBUS™ System**
- **Reliable and Easy to Use**
- **Universal BITBUS™ Interface and BITBUS™ Interface Handler Libraries Provide 32 System Management/ Control Procedure**
- **Compatible with Intel's C, PL/M and ASM Languages**
- **For DOS, iRMX® 86/286, XENIX*, and iPDS™ Host Systems**

The BITBUS Toolbox provides a set of utilities designed to simplify development of host system software for controlling a BITBUS network. The Toolbox includes: two libraries of procedures that can be called from the host code; an on-line program called the BITBUS Monitor which is invaluable for troubleshooting, monitoring, and manually controlling a system; and code conversion/communication software to support applications software development on a PC.

The procedure libraries contain common procedures used by the host to read or write data to remote node I/O ports, download or upload programs and data, start and stop tasks (program modules) running on the nodes, send and receive messages, and perform a variety of system status and control functions. By using these libraries, the programmer's task of generating BITBUS host code is substantially reduced.



280732-1

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*XENIX is a trademark of Microsoft Corporation.

October 1987
Order Number: 280732-001

THE BITBUS™ TOOLBOX—PRODUCT DESCRIPTION

The BITBUS Toolbox is used to develop host code for controlling a BITBUS network, and is an essential tool for both centralized and distributed control applications.

With centralized control, the host code sends commands to a node to read and update the I/O. All the decisions are made at the host. Normally, this kind of system would require extensive host code. However, the Toolbox includes the UBI and BIH procedure libraries that can be called to perform simple or complex control procedures.

In addition to the Toolbox, all BITBUS boards include, in firmware, a set of procedures known as Remote Access and Control (RAC). By sending simple messages to these procedures, basic I/O functions can be performed. The RAC procedures are listed in Table 1.

With distributed control systems, programs run on the remote BITBUS boards (nodes) and offload the host system of most decision making responsibilities. Using UBI calls or the BITBUS Monitor, commands can be sent to the nodes to control tasks or to periodically upload data for further analysis or storage. The software tools in the BITBUS Toolbox reduce the time and effort necessary to develop host code for these applications.

In addition to the DCS100 BITBUS Toolbox, other host code tools include a full set of host software compilers, libraries, debuggers, and in-circuit emulators. The BITBUS Toolbox is described in detail in the sections that follow.

Table 1. Remote Access and Control Procedures

Name	Function
RESET_STATION	Perform a software reset.
CREATE_TASK	Perform an RQ$CREATE$TASK system call.
DELETE_TASK	Perform an RQ$DELETE$TASK system call.
GET_FUNCTION_ID	Perform an RQGETFUNCTION$IDS call.
RAC_PROTECT	Suspend or resume RAC services.
READ_I/O	Return values from specified I/O ports.
WRITE_I/O	Write to the specified I/O ports.
UPDATE_I/O	Update the specified I/O ports.
UPLOAD_MEMORY	Return the values in specified memory area.
DOWNLOAD_MEMORY	Write values to specified memory area.
OR_IO	OR values into specified I/O ports.
AND_IO	AND values into specified I/O ports.
XOR_IO	XOR values into specified I/O ports.
READ_INTERNAL	Read values at specified internal RAM areas.
WRITE_INTERNAL	Write values to specified internal RAM areas.
NODE_INFO	Return device related information.
OFFLINE	Set node offline.
UPLOAD_CODE	Read values from code memory space.
DOWNLOAD_CODE	Write values to specified EEPROM memory.

BITBUS™ TOOLBOX UTILITIES

The DCS100 BITBUS Toolbox includes six host software utilities. They include:

- Universal BITBUS Interface (UBI)—a set of 28 procedures for implementing remote I/O and controlling a BITBUS network.
- BITBUS Interface Handlers (BIH)—four basic procedures for sending/receiving messages over a BITBUS network.
- BITBUS Monitor (BBM)—An on-line program with 36 commands that enable a user to configure, troubleshoot, monitor, and manually control a BITBUS network.
- PC Bridge—Communications program for the PC to support software development on a PC and download into an iRMX or XENIX-hosted BITBUS network.
- OBJHEX Conversion Utility—Converts an object file to hex format for downloading code.
- UDI2DOS—Converts Intel object code programs to .exe format for execution on the PC.

Universal BITBUS™ Interface

UBI is a library of 28 procedures called by the host program to manage the I/O, download or upload code and data, manage tasks on a node, send and receive messages, and perform an assortment of miscellaneous functions. These procedures are listed in Table 2, below.

Table 2. UBI Procedure Calls

I/O	
BQANDI/O	AND I/O
BQORI/O	OR I/O
BQXORI/O	Excl. OR I/O
BQ$WRITE$I/O	Write I/O
BQ$READ$I/O	Read I/O
BQ$UPDATE$I/O	Write I/O and read back
MEMORY MANAGEMENT	
BQABSLOAD	Download program to code memory
BQ$WRITE$CODE$MEM	Write to code memory
BQ$READ$CODE$MEM	Read code memory
BQ$WRITE$INT$MEM	Write to internal data memory
BQ$READ$INT$MEM	Read internal data memory
BQ$WRITE$EXT$MEM	Write to external data memory
BQ$READ$EXT$MEM	Read external data memory
TASK MANAGEMENT	
BQ$CREATE$TASK	Create task
BQ$DELETE$TASK	Delete task
BQGETFUNCTION$IDS	Read task function IDs
MESSAGE MANAGEMENT	
BQ$FLUSH	Clear an iSBX/iPCX interface
BQ$RECEIVE$MESSAGE	Receive a message
BQ$SEND$MESSAGE	Send a message

Table 2. UBI Procedure Calls (Continued)

MISCELLANEOUS CALLS	
BQ$DELAY	Perform a time delay
BQ$NODE$INFO	Return node information
BQ$PROBE$SBX	Check for BITBUS iSBX board
BQ$PROTECT$RAC	Lockout (protect) a node
BQ$RESET$DEVICE	Initiate a software reset
BQ$RESYNC$NODE	Set a node offline, prep. to resync
BQSETPORT	Set port I/O address
BQSETSBX	Set port I/O address
BQ$SHELL	Shell escape and then return

The UBI utility includes libraries interfacing with PL/M and C host code running within DOS, iRMX, and XENIX environments. Also included are declaration files for the procedures.

To use these procedures, the UBI calls are incorporated into the source code modules together with parameters needed by the procedures (e.g. node address, port address, memory location, task number, and data). The source module and UBI declaration files are then compiled and linked with the UBI library.

When the call executes, the called procedure will be performed, data will be returned (in the case of READ or UPLOAD procedures) together with an error code. These error codes can help the host system take corrective action.

BITBUS™ Interface Handlers (BIH)

BIH is a library of four basic procedures for sending and receiving messages between the host and network nodes. These procedures, listed in Table 3, are most useful when generating custom UBI-like procedures. The BIH utility includes procedure libraries and declaration files for DOS, iRMX 86/88/286, and ISIS-PDS (iPDS)-based systems.

Table 3. BIH Procedure Calls

Call Name	Description
CQDCMINIT	Performs any initialization required by the BITBUS Interface Handlers.
CQDCMRECEIVE	Receives one message from any BITBUS node.
CQDCMSTATUS$CHECK	Determines whether a BITBUS message is available to receive.
CQDCMTRANSMIT	Transmits one message to any BITBUS node.

To use these libraries, the appropriate declaration file is included with the host source code. The modules are then compiled and the resultant object module is linked to the BIH library.

BITBUS™ Monitor

The BITBUS Monitor (BBM) is an on-line program that is invaluable for troubleshooting and testing a BITBUS system and can also be used to manually control a system. BBM commands are listed in Table 4.

Table 4. BITBUS™ Monitor Commands

I/O	
AIO	And I/O
OIO	Or I/O
RIO	Read I/O
UIO	Update I/O
WIO	Write to I/O
XIO	Exclusive OR I/O
MEMORY MANAGEMENT	
LOAD	Download to code memory
RCMEM	Read code memory
RIMEM	Read internal memory
RXMEM	Read data memory
WCMEM	Write to code memory
WIMEM	Write to internal memory
WXMEM	Write to data memory
TASK MANAGEMENT	
CTASK	Create a task
DTASK	Delete a task
SYS	Display node task status

MESSAGE MANAGEMENT	
DMSG	Display a message
RMSG	Receive a message
SMSG	Send a message
TMSG	Sends, receives, displays a message
MISCELLANEOUS COMMANDS	
DELAY	Suspend Activity
EXIT	Exit BBM
FLUSH	Clears an iSBX/iPCX interface
HELP	Provide on-line help
INCLUDE	Open/execute a BBM file
LIST	Creates a copy of the BBM session
LOCK	Lockout (protect) a node
NODEINFO	Node information
PAUSE	Wait until <CR>
RESET	SW reset at a node
RESYNC	Set a node offline
SETPORT/ SETSBX	Set port I/O address
SHELL	XENIX/DOS shell escape from BBM
SYMBOLS	Display/create/change the value of a user symbol
UNLOCK	Unprotect
VERBOSE	Controls echo and prompts

I/O ACCESS

Six commands are provided for writing to and reading from I/O ports on remote nodes. With these commands, an operator can test the I/O connected to a BITBUS node or monitor the status of an input port. The I/O commands allow an operator to quickly isolate a problem at a remote node.

MEMORY ACCESS

Seven memory access commands are provided. These commands allow the operator to download and upload both code (programs) and data (variables) between the host system and remote BITBUS nodes. Internal RAM memory within the 8044BEM microcontroller can also be accessed. In addition, the BBM supports code download to both static RAM and E^{2}PROM devices. The memory access commands are especially useful for on-target application development.

The BITBUS Monitor enables the user to reference a memory location by using a symbolic reference or label. For example, if a task running on a node includes a program variable called "rate", the operator can modify this variable simply by typing:

```
WIMEM <node address> .rate 6CH
```

In this case, the program will execute with a value of 6C hex for "rate".

Symbolic references can also be used for other BBM parameters, such as node address, port address, and data. Symbolic access allows the user to more easily test and modify programs at run time.

TASK MANAGEMENT

Four commands are available to monitor and control the running of tasks on the nodes.

The DCX 51 real time multitasking executive found on all BITBUS boards can support up to 7 user tasks (in addition to the RAC task). Each of these tasks have an initial Task Descriptor (ITD) which assigns a function ID to the task plus other important run-time parameters used by the executive. By chaining ITDs together, multiple tasks can become active upon power up.

The BBM commands allow tasks to selectively be made active (CTASK) or inactive (DTASK). In addition, the SYS command can be used to display which nodes are present and operational in a system and display the function IDs for active tasks on each node. The task management commands are especially useful when developing/troubleshooting multitasking control programs.

MESSAGE OPERATIONS

These four commands are used to send and receive messages to and from tasks on remote nodes.

MISCELLANEOUS COMMANDS

The BBM includes 15 commands that are used to control the operating status of nodes, and to support various troubleshooting functions. These commands include:

The HELP command—an on-line facility that displays the complete BBM command directory or detailed information on using the commands.

The SHELL command—allows an operator to do a shell escape to DOS or XENIX, perform the needed operating system function, and return to the monitor.

The RESET, FLUSH, and RESYNC commands—used to clear a node that is hung.

OPERATING ENVIRONMENT

The BITBUS Monitor will run on DOS, iRMX 86/286, XENIX and iPDS-based systems. Both 5¼" and 8" media is provided for iRMX and XENIX systems. The iPDS version of the monitor does not include the following BBM commands (or equivalent UBI calls): DELAY, LIST, PAUSE, RCMEM, RESYSC, SETPORT, SYMBOLS, TMSG, VERBOSE, WCMEM.

PC Bridge

The PC Bridge is a communications program that runs on a PC-DOS or MS-DOS system, and is used to establish a communication link between the PC and an Intel iRMX 86/286 or XENIX-based microcomputer system. The software engineer can use the Bridge in two ways. First, he can develop host or node programs on the PC and download the code to the host system or remote nodes. He can also use the PC as a virtual terminal to the host system. The PC Bridge effectively expands the development environment for the software engineer.

The link between the PC and the host microcomputer can either be over an RS232 cable (supplied) or via a modem link. The PC Bridge transfers data at up to 19.2K baud (asynchronous) and supports XON/XOFF flow control.

OBJHEX

OBJHEX is an object code to hex code conversion utility similar to the OH51 hex converter supplied with Intel "8051" languages. OBJHEX has the additional ability to retain the object module's symbol table during the conversion process. The table is stored at the host system and enables the BITBUS Monitor to symbolically access program memory. OBJHEX runs on both DOS and iRMX86 (5¼", 8" media)-based systems.

UDI2DOS

UDI2DOS converts Intel object code (8086 OMF) to the .exe format so that it will run within a DOS environment.

SPECIFICATIONS

Media Provided

	BBM	UBI	BIH	PC Bridge	OBJHEX	UDI2DOS
Series II						
III			X			
IV						
iPDS	A	A	A			
IRMX 5¼"	X	X	X	X	X	
8"	X	X	X	X	X	
XENIX 5¼"	X	X		B	X	
8"	X	X		B	X	
DOS	X	X	X	X	X	X

NOTES:
A. iPDS uses Release 1 Toolbox.
B. Supports operation with XENIX. XENIX disks not required.

Documentation (supplied)

BITBUS Toolbox Overview and Installation Guide	460235-001
BITBUS Monitor User's Guide	148686-002
Universal BITBUS Interface User's Guide	460236-001
BITBUS Interface Handlers User's Guide	148685-002
PC Bridge Communications Utility User's Guide	149236-001
BITBUS OBJHEX Conversion Utility User's Guide	460237-001

Compatible Software

Intel ASM, PL/M, and C languages (8086/80286/80386 versions)

Order Codes

Order Number	Description
DCS100SU	BITBUS Toolbox Host Software Utilities, single-use license for development only. Includes RS232 cables to connect an Intel microcomputer system with an IBM* PC-XT* or PC-AT*, and full documentation. See above for media provided.
DCS100BY	BITBUS Toolbox Host Software Utilities. Same as above, except sold with a buyout license. Allows incorporation of UBI and BIH procedure libraries—no additional incorporation fee is required.

DCS110 BITWARE
DCS120 PROGRAMMERS SUPPORT PACKAGE

- **Supports Calls to the 8044BEM Microcontroller On-Chip, Multitasking DCX 51 Executive**
- **Fully Compatible with Intel's ASM51 and PL/M51 Languages**
- **DCS110 also Includes DCM44 Code to Support Emulation/Debug of BITBUS™ Node Code using Intel In-Circuit Emulators**
- **For DOS, iRMX®, iPDS™, and Series III/IV Development Environments**

The DCS110 and DCS120 packages are designed to support software development of distributed control BITBUS applications. Both products include a DCX51 interface library so that BITBUS application programs can make calls to the DCX51 Executive. DCS110 also includes a DCM44 downloadable file that enables an Intel in-circuit emulator such as the ICE™ 5100/044 to emulate a BITBUS environment. By using an in-circuit emulator together with DCS110, the developer can easily and quickly debug BITBUS application code.

280731-1

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DCX 51 ENVIRONMENT

The 8044BEM microcontroller, used on every BITBUS board, includes in firmware a preconfigured version of the DCX 51 Executive. DCX 51 provides a variety of services to the application code, including: task management; interrupt management; inter-task communications; memory management; and timing services. Up to 7 user tasks can run concurrently under DCX 51. Each task has a unique Initial Task Descriptor (ITD) that describes to the executive several run-time parameters (e.g. stack space, priority level, etc.). By also specifying an Initial Data Descriptor (IDD), the executive can be partially reconfigured. Modifiable run-time constants include the system clock rate, clock priority, internal memory buffer size, and user (internal) memory size. DCX 51 calls are listed in Table 1.

By running applications under DCX 51, the designer can make optimal use of the 8044BEM microcontroller. If a task needs to wait for a message, an interrupt, or a time period, DCX 51 will temporarily assign access to the 8044 to another task. In this way, multiple tasks can access the microcontroller.

Table 1. DCX 51 Procedure Calls

Call Name	Description
Task Management Calls	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION$IDS	Obtain the function IDs of tasks currently in the system.
Intertask Communication Calls	
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.
Memory Management Calls	
RQGETMEM	Get available memory from the system memory pool.
RQ$RELEASE$MEM	Release memory to the system memory pool.
Interrupt Management Calls	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RQ$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
Timer Management Calls	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

Interfacing to the DCX 51 Executive

To interface with the executive, DCS110 and DCS120 both include a DCX 51 interface library plus a set of "include" files. The interface library, which is linked to the application modules, allow the code to access DCX 51 procedures. The "include" files consist of DCX 51 declaration and macro definition files that help simplify source code development. These files are listed in Table 2.

DCS110 Bitware Software Package

In addition to the DCX 51 interface files, DCS110 also includes a DCM44 object file to support debug of node code using an Intel in-circuit emulator. DCM44 is the firmware found in all 8044BEM BITBUS microcontrollers and together with an Intel in-circuit emulator, successfully duplicates the 8044BEM environment. Emulators that are supported include the ICE™ 5100/044, the ICE 44, and the EMV 44.

Developing Applications Software

Using DCS110 or DCS120 software to develop BITBUS applications software is a straightforward, multi-step process as diagrammed in Figure 1. The designer uses a text editor to write the application code either in ASM 51 or PL/M 51. The source code modules are then assembled/compiled along with the DCX 51 "include" files. The final step is to link together all of the modules, the DCX 51 interface library, and the DCM44I.LIB file. The linked/located absolute object module can then be downloaded to the target board or burned into EPROM.

Table 2. DCS110/120 Files

Filename	Description
DCX 51 Support Files:	
DCX51I.LIB	Interface library to the DCX 51 executive. Provides the linker with the address of data variables and entry points for DCX51 procedures called from other object modules.
DCX51A.EXT DCX51A.LIT DCX51P.LIT	External and literal declaration files. These files support DCX 51 calls from ASM 51 and PL/M 51 code.
DCXB0P.EXT DCXB1P.EXT DCXB2P.EXT DCXB3P.EXT	DCX 51 External procedure declarations for PL/M 51 modules using 8044 register banks 0, 1, 2 or 3.
DCX51A.MAC	Initial Task Descriptor (ITD) and Initial Data Descriptor (IDD) macro definitions.
APPL1.A51 APPL2.A51	Sample application, parts 1 and 2; template for generating ITDs and IDD.
DCM44I.LIB	This file maps out reserved memory needed by the 8044BEM firmware and is linked to other user object modules using the RL51 Linker.
DCM44 Firmware Files (DCS110 Only):	
DCM44	DCM44 (BITBUS) code for Intel ICE™/EMV emulators.

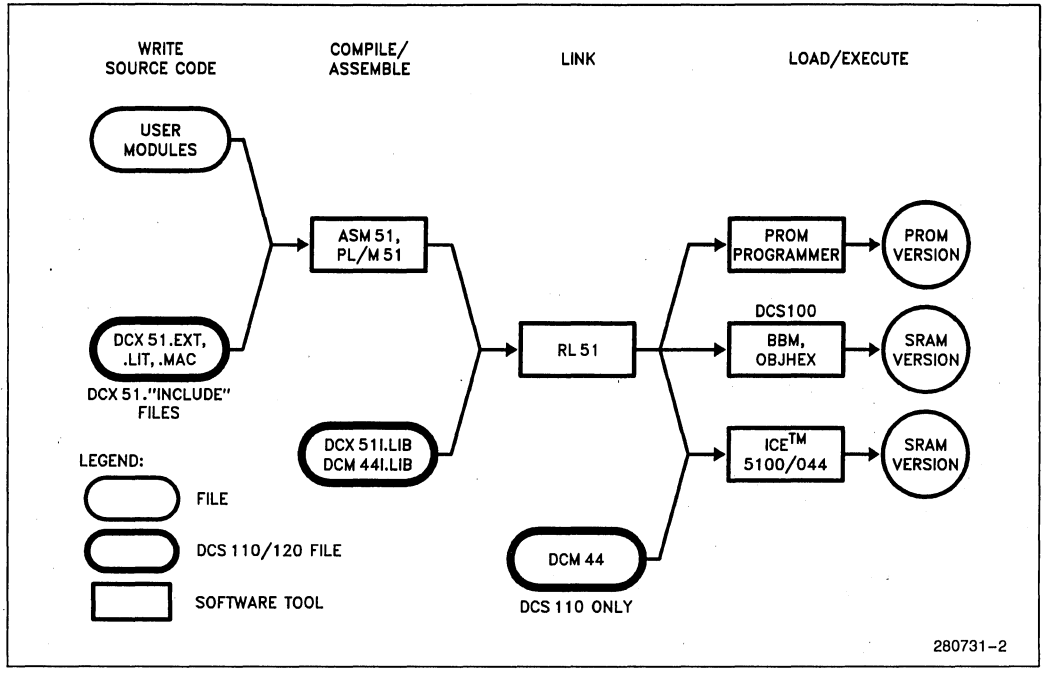


Figure 1. DCS110/120 Software Development Environment

Development Environments

Both DCS110 and DCS120 are shipped with media to support software development on PC/MS-DOS, iRMX 86, iPDS, and Intellec® Series III/IV systems. DCS110 is available with a single-use license for application development and debug. Designers planning to incorporte DCX 51 files in their application should purchase the DCS120 "buyout" product.

Order Codes	Description
DCS110SU	Bitware Software Package. Includes DCM44 code to emulate a BITBUS environment when using an Intel in-circuit emulator and interface files to support procedure calls to DCX 51. Provided with documentation and PC-DOS, iRMX 86 (5¼", 8"), iPDS, and Series III/IV media. Single-use license.
DCS120BY	Programmers Support Package. Includes interface files to support procedure calls to DCX 51. Provided with documentation and PC-DOS, iRMX 86 (5¼", 8"), iPDS, and Series III/IV media. Buyout license allows incorporation of software into product—no additional incorporation fee is required.

COMPATIBLE SOFTWARE TOOLS

DCS100	BITBUS Toolbox Host Software Utilities for PC/MS-DOS, iRMX 86/286, XENIX*, iPDS, and Series III/IV host systems.
AEDIT	Source Code and Text Editor for all Intel host environments (consult data sheet for order codes).

*XENIX is a trademark of Microsoft Corp.

8051 LANGUAGES

(Note: All products also include RL51 Linker/Relocator, LIB51 Librarian, and OH51 object to hex code converter)

D86ASM51	ASM 51 Assembler for PC-DOS host system
R86ASM51	ASM 51 Assembler for iRMX 86 host system
I86ASM51	ASM 51 Assembler for Series III/IV host systems
MC151ASM	ASM 51 Assembler for iPDS and Series II host systems
D86PLM51	PL/M 51 Compiler for PC-DOS host system
R86PLM51	PL/M 51 Compiler for IRMX 86 host system
I86PLM51	PL/M 51 Compiler for Series III/IV host systems
iMDX352	PL/M 51 Compiler for iPDS and Series II host systems

IN-CIRCUIT EMULATORS AND PROM PROGRAMMERS

(Note: + indicates that the product is no longer available)

ICE5100/044	In-Circuit Emulator for the RUPI™-44 Family (hosted on PC-DOS, and Series III/IV—see data sheet for order codes)
ICE-44+	8044 In-Circuit Emulator (hosted on Series II–IV systems)
iPDSEMV44CON+	Kit to add 8044 support to an EMV-51/51A emulator (iPDS host)
iUP-200A, iUP-201A	Universal PROM programmer (hosted on PC-DOS, iPDS, and Series III/IV; see data sheet for order codes)

8051
SOFTWARE PACKAGES

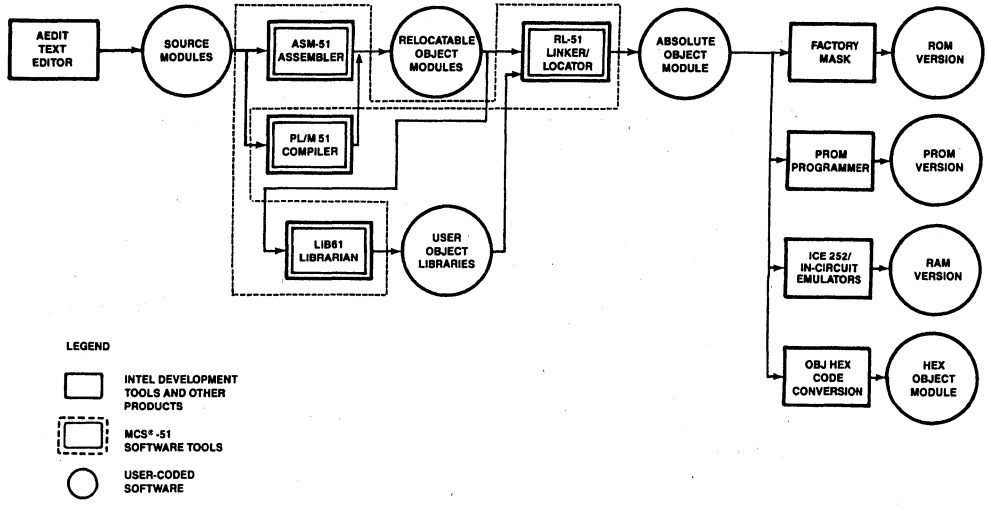
- **Choice of hosts: PCDOS 3.0 based IBM* PC XT/AT* and iRMX®86**
- **Supports all members of the Intel MCS® -51 architecture**

PL/M51 Software Package Contains the following:

- **PL/M51 Compiler which is designed to support all phases of software implementation**
- **RL51 Linker and Relocator which enables programmers to develop software in a modular fashion**
- **LIB51 Librarian which lets programmers create and maintain libraries of software object modules**

8051 Software Development Package Contains the following:

- **8051 Macro Assembler which gives symbolic access to 8051 hardware features**
- **RL51 Linker and Relocator program which links modules generated by the assembler**
- **LIB51 Librarian which lets programmers create and maintain libraries of software object modules**



162771-1

Figure 1. MCS® -51 Program Development Process

*IBM and AT are registered trademarks of International Business Machines Corporation.

November 1988
Order Number: 162771-006

PL/M 51 SOFTWARE PACKAGE

- **High-level programming language for the Intel MCS® -51 single-chip microcomputer family**
- **Enhanced to support boolean processing**
- **Tailored to provide an optimum balance among on-chip RAM usage, code size and code execution time**
- **Produces relocatable object code which is linkable to object modules generated by all other 8051 translators**
- **Allows programmer to have complete control of microcomputer resources**
- **Extends high-level language programming advantages to microcontroller software development**
- **Improved reliability, lower maintenance costs, increased programmer productivity and software portability**
- **Includes the linking and relocating utility and the library manager**
- **Supports all members of the Intel MCS® -51 architecture**

PL/M 51 is a structured, high-level programming language for the Intel MCS-51 family of microcomputers. The PL/M 51 language and compiler have been designed to support the unique software development requirements of the single-chip microcomputer environment. The PL/M language has been enhanced to support Boolean processing and efficient access to the microcomputer functions. New compiler controls allow the programmer complete control over what microcomputer resources are used by PL/M programs.

PL/M 51 is the high-level alternative to assembly language programming for the MCS-51. When code size and code execution speed are not critical factors, PL/M 51 is the cost-effective approach to developing reliable, maintainable software.

The PL/M 51 compiler has been designed to support efficiently all phases of software implementation with features like a syntax checker, multiple levels of optimization, cross-reference generation and debug record generation.

ICE™ 5100 is available for on-target debugging.

Software available for PC DOS 3.0 based IBM* PC XT/AT* Systems.

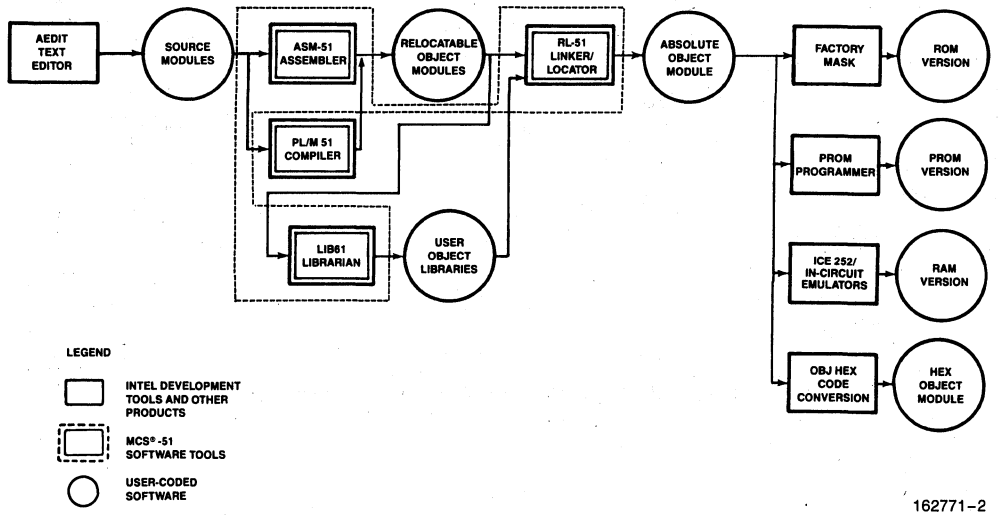


Figure 2. PL/M51 Software Package

PL/M 51 COMPILER

FEATURES

Major features of the Intel PL/M 51 compiler and programming language include:

Structured Programming

PL/M source code is developed in a series of modules, procedures, and blocks. Encouraging program modularity in this manner makes programs more readable, and easier to maintain and debug. The language becomes more flexible, by clearly defining the scope of user variables (local to a private procedure, for example).

Language Compatibility

PL/M 51 object modules are compatible with object modules generated by all other MCS-51 translators. This means that PL/M programs may be linked to programs written in any other MCS-51 language.

Object modules are compatible with In-Circuit Emulators and Emulation Vehicles for MCS-51 processors: the DEBUG compiler control provides these tools with symbolic debugging capabilities.

Supports Three Data Types

PL/M makes use of three data types for various applications. These data types range from one to sixteen bits and facilitate various arithmetic, logic, and address functions:

— Bit: a binary digit

— Byte: 8-bit unsigned number or,

— Word: 16-bit unsigned number.

Another powerful facility allows the use of BASED variables that map more than one variable to the same memory location. This is especially useful for passing parameters, relative and absolute addressing, and memory allocation.

Two Data Structuring Facilities

PL/M 51 supports two data structuring facilities. These add flexibility to the referencing of data stored in large groups.

— Array: Indexed list of same type data elements

— Structure: Named collection of same or different type data elements

— Combinations of Both: Arrays of structures or structures of arrays.

Interrupt Handling

A procedure may be defined with the INTERRUPT attribute. The compiler will generate code to save and restore the processor status, for execution of the user-defined interrupt handler routines.

Compiler Controls

The PL/M 51 compiler offers controls that facilitate such features as:

— Including additional PL/M 51 source files from disk

— Cross-reference

— Corresponding assembly language code in the listing file

Program Addressing Control

The PL/M 51 compiler takes full advantage of program addressing with the ROM (SMALL/MEDIUM/LARGE) control. Programs with less than 2 KB code space can use the SMALL or MEDIUM option to generate optimum addressing instructions. Larger programs can address over the full 64 KB range.

Code Optimization

The PL/M 51 compiler offers four levels of optimization for significantly reducing overall program size.

— Combination or "folding" of constant expressions; "Strength reductions" (a shift left rather than multiply by 2)

— Machine code optimizations; elimination of superfluous branches

— Automatic overlaying of on-chip RAM variables

— Register history: an off-chip variable will not be reloaded if its value is available in a register.

Error Checking

The PL/M 51 compiler has a very powerful feature to speed up compilations. If a syntax or program error is detected, the compiler will skip the code generation and optimization passes. This usually yields a 2X performance increase for compilation of programs with errors.

A fully detailed set of programming and compilation error messages is provided by the compiler and user's guide.

BENEFITS

PL/M 51 is designed to be an efficient, cost-effective solution to the special requirements of MCS-51 Microsystem Software Development, as illustrated by the following benefits of PL/M use:

Low Learning Effort

PL/M 51 is easy to learn and to use, even for the novice programmer.

Earlier Project Completion

Critical projects are completed much earlier than otherwise possible because PL/M 51, a structured high-level language, increases programmer productivity.

Lower Development Cost

Increases in programmer productivity translate immediately into lower software development costs because less programming resources are required for a given programmed function.

Increased Reliability

PL/M 51 is designed to aid in the development of reliable software (PL/M programs are simple statements of the program algorithm). This substantially reduces the risk of costly correction of errors in systems that have already reached full production status, as the more simply stated the program is, the more likely it is to perform its intended function.

Easier Enhancements and Maintenance

Programs written in PL/M tend to be self-documenting, thus easier to read and understand. This means it is easier to enhance and maintain PL/M programs as the system capabilities expand and future products are developed.

RL51 LINKER AND RELOCATOR

- **Links modules generated by the assembler and the PL/M compiler**
- **Locates the linked object to absolute memory locations**
- **Enables modular programming of software-efficient program development**
- **Modular programs are easy to understand, maintainable and reliable**

The MCS-51 linker and relocator (RL51) is a utility which enables MCS-51 programmers to develop software in a modular fashion. The utility resolves all references between modules and assigns absolute memory locations to all the relocatable segments, combining relocatable partial segments with the same name.

With this utility, software can be developed more quickly because small functional modules are easier to understand, design and test than large programs.

The total number of allowed symbols in user-developed software is very large because the assembler number of symbols' limit applies only per module, not to the entire program. Therefore programs can be more readable and better documented. RL51 can be invoked either manually or through a batch file for improved productivity.

Modules can be saved and used on different programs. Therefore the software investment of the customer is maintained.

RL51 produces two files. The absolute object module file can be directly executed by the MCS-51 family. The listing file shows the results of the link/locate process.

LIB51 LIBRARIAN

The LIB51 utility enables MCS-51 programmers to create and maintain libraries of software object modules. With this utility, the customer can develop standard software modules and place them in libraries, which programs can access through a standard interface. When using object libraries, the linker will call only object modules that are required to satisfy external references.

Consequently, the librarian enables the customer to port and reuse software on different projects—thereby maintaining the customer's software investment.

ORDERING INFORMATION

Order Code	Operating Environment
D86PLM51	PL/M51 Software for PC DOS 3.0 Systems
R86PLM51	PL/M51 Software for iRMX 86 Systems

Documentation Package

PL/M 51 User's Guide

MCS-51 Utilities User's Guide

SUPPORT:

Hotline Telephone Support, Software Performance Report (SPR), Software Updates, Technical Reports, and monthly Technical Newsletters are available.

8051 SOFTWARE DEVELOPMENT PACKAGE

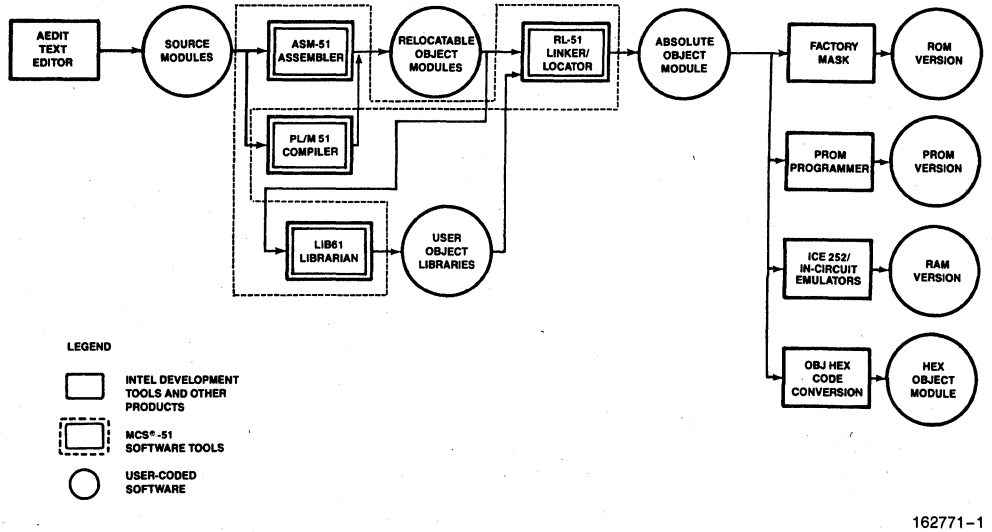
- **Symbolic relocatable assembly language programming for 8051 microcontrollers**
- **Produces Relocatable Object Code which is linkable to other 8051 Object Modules**
- **Encourage modular program design for maintainability and reliability**
- **Macro Assembler features conditional assembly and macro capabilities**
- **Supports all members of the Intel MCS® 51 architecture**

The 8051 software development package provides development system support for the powerful 8051 family of single chip microcomputers. The package contains a symbolic macro assembler and relocation/linkage utilities.

The assembler produces relocatable object modules from 8051 macro assembly language instructions. The object code modules can be linked and located to absolute memory locations. This absolute object code may be used to program the 8751 EPROM version of the chip. The assembler output may also be debugged using the family of ICE 5100.

The converter translates 8048 assembly language instructions into 8051 source instructions to provide software compatibility between the two families of microcontrollers.

Software available for PC DOS 3.0 based IBM* PC XT/AT Systems.



162771-1

Figure 1. MCS® -51 Program Development Process

8051 MACRO ASSEMBLER

- **Gives symbolic access to powerful 8051 hardware features**
- **Produces object file, listing file and error diagnostics**
- **Object files are linkable and locatable**
- **Provides software support for many addressing and data allocation capabilities**
- **Symbolic Assembler supports symbol table, cross-reference, macro capabilities, and conditional assembly**

The 8051 Macro Assembler (ASM51) translates symbolic 8051 macro assembly language modules into linkable and locatable object code modules. Assembly language mnemonics are easier to program and are more readable than binary or hexadecimal machine instructions. By allowing the programmer to give symbolic names to memory locations rather than absolute addresses, software design and debug are performed more quickly and reliably. Furthermore, since modules are linkable and relocatable, the programmer can do his software in modular fashion. This makes programs easy to understand, maintainable and reliable.

The assembler supports macro definitions and calls. This is a convenient way to program a frequently used code sequence only once. The assembler also provides conditional assembly capabilities.

Cross referencing is provided in the symbol table listing, showing the user the lines in which each symbol was defined and referenced.

ASM51 provides symbolic access to the many useful addressing features of the 8051 architecture. These features include referencing for bit and byte locations, and for providing 4-bit operations for BCD arithmetic. The assembler also provides symbolic access to hardware registers, I/O ports, control bits, and RAM addresses. ASM51 can support all members of the 8051 family.

Math routines are enhanced by the MULtiply and DIVide instructions.

If an 8051 program contains errors, the assembler provides a comprehensive set of error diagnostics, which are included in the assembly listing or on another file.

ICE 5100 is available for program debugging.

RL51 LINKER AND RELOCATOR PROGRAM

- **Links modules generated by the assembler**
- **Locates the linked object to absolute memory locations**
- **Enables modular programming of software for efficient program development**
- **Modular programs are easy to understand, maintainable and reliable**

The 8051 linker and relocator (RL51) is a utility which enables 8051 programmers to develop software in a modular fashion. The linker resolves all references between modules and the relocator assigns absolute memory locations to all the relocatable segments, combining relocatable partial segments with the same name.

With this utility, software can be developed more quickly because small functional modules are easier to understand, design and test than large programs.

The number of symbols in the software is very large because the assembler symbol limit applies only per module not the entire program. Therefore programs can be more readable and better documented.

Modules can be saved and used on different programs. Therefore the software investment of the customer is maintained.

RL51 produces two files. The absolute object module file can be directly executed by the 8051 family. The listing file shows the results of the link/locate process.

LIB51 LIBRARIAN

The LIB51 utility enables MCS-51 programmers to create and maintain libraries of software object modules. With this utility, the customer can develop standard software modules and place them in libraries, which programs can access through a standard interface. When using object libraries, the linker will call only object modules that are required to satisfy external references.

Consequently, the librarian enables the customer to port and reuse software on different projects—thereby maintaining the customer's software investment.

ORDERING INFORMATION

Order Code	Operating Environment
D86ASM51	8051 Assembler for PCDOS 3.0 Systems
R86ASM51	8051 Assembler for iRMX 86 Systems

Documentation Package:

MCS-51 Macro Assembler User's Guide

MCS-51 Utilities User's Guide for 8080/8085 Based Development System

SUPPORT:

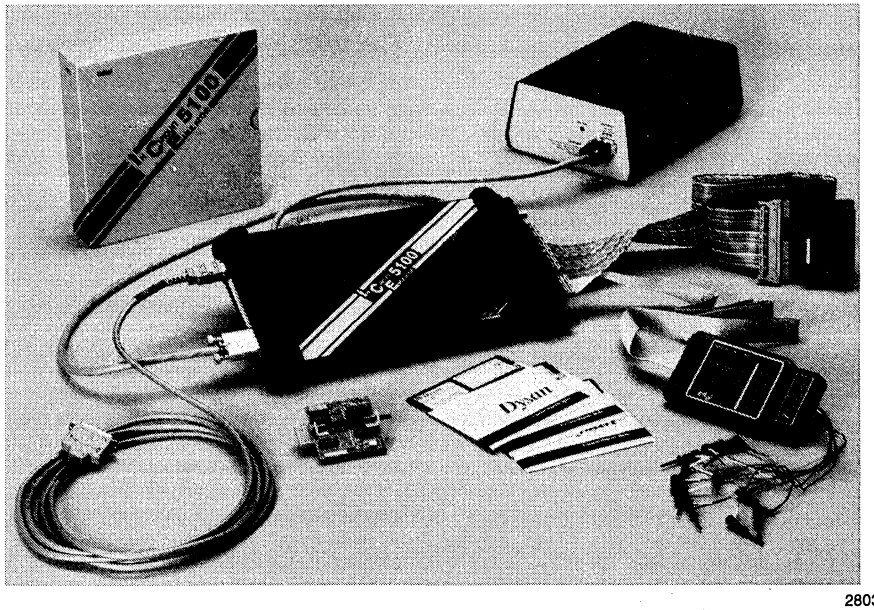
Hotline Telephone Support, Software Performance Reporting (SPR), Software Updates, Technical Reports, Monthly Newsletter available.

ICE™-5100/044 In-Circuit Emulator for the RUPI™-44 Family

- **Precise, Full-Speed, Real-Time Emulation of the RUPI™-44 Family of Peripherals**
- **64 KB of Mappable High-Speed Emulation Memory**
- **254 24-bit Frames of Trace Memory (16 Bits Trace Program Execution Addresses and 8 Bits Trace Eternal Events)**
- **Serial Link to IBM* PC AT or PC XT (and PC DOS Compatibles)**
- **ASM-51 and PL/M-51 Language Support**
- **Built-in CRT-Oriented Text Editor**
- **Source Code Display**
- **Symbolic Debugging Enables Access to Memory Locations and Program Variables**
- **Four Address Breakpoints Plus In-Range, Out-of-Range, and Page Breaks**
- **Equipped with the Integrated Command Directory (ICD™) That Provides**
  - **— On-Line Help**
  - **— Syntax Guidance and Checking**
  - **— Command Recall**
- **On-Line Disassembler and Single-Line Assembler to Help with Code Patching**
- **Provides an Ideal Environment for Debugging BITBUS™ Applications Code**
- **Symbolic Debug**

The ICE™-5100/044 in-circuit emulator is a high-level, interactive debugger that is used to develop and test the hardware and software of a target system based on the RUPI™-44 family of peripherals. The ICE-5100/044 emulator can be serially linked to an Intellec® Series III/IV or an IBM PC AT or PC XT. The emulator can communicate with the host system at standard baud rates up to 19.2K. The design of the emulator supports all of the RUPI-44 components at speeds up to and including 12 MHz.

*IBM is a registered trademark of International Business Machines Corporation. Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel.



280325-1

September 1988
Order Number: 280325-002

PRODUCT OVERVIEW

The ICE-5100/044 emulator provides full emulation support for the RUPI-44 family of peripherals, including 8044-based BITBUS™ board products. The RUPI-44 family consists of the 8044, the 8744, and the 8344.

The ICE-5100/044 emulator enables hardware and software development to proceed simultaneously. With the ICE-5100/044, prototype hardware can be added to the system as it is designed and software can be developed prior to the completion of the hardware prototype. Software and hardware integration can occur while the product is being developed.

The ICE-5100/044 emulator assists four stages of development:

- Software debugging
- Hardware debugging
- System integration
- System test

Software Debugging

The ICE-5100/044 emulator can be operated without being connected to the target system and before any of the user's hardware is available (provided external data RAM is not needed). In this stand-alone mode, the ICE-5100/044 emulator can be used to facilitate program development.

Hardware Debugging

The ICE-5100/044 emulator's AC/DC parametric characteristics match the microcontroller's. The emulator's full-speed operation makes it a valuable tool for debugging hardware, including time-critical serial port, timer, and external interrupt interfaces.

System Integration

Integration of software and hardware can begin when the emulator is plugged into the microcontroller socket of the prototype system hardware. Hardware can be added, modified, and tested immediately. As each section of the user's hardware is completed, it can be added to the prototype. Thus, the hardware and software can be system tested in real-time operation as each section becomes available.

System Test

When the prototype is complete, it is tested with the final version of the system software. The ICE-5100/044 emulator is then used for real-time emulation of the microcontroller to debug the system as a completed unit.

The final product verfication test can be performed using the ROM or EPROM version of the microcontroller. Thus, the ICE-5100/044 emulator provides the ability to debug a prototype or production system at any stage in its development without introducing extraneous hardware or software test tools.

PHYSICAL DESCRIPTION

The ICE-5100/044 emulator consists of the following components (see Figure 1):

- Power supply
- AC and DC power cables
- Controller pod
- Serial Cable (host-specific)
- User probe assembly (consisting of the processor module and the user cable)
- Crystal power accessory (CPA)
- 40-pin target adaptor
- Clips assembly
- Software (includes the ICE-5100/044 emulator software, diagnostic software, and a tutorial)

The controller pod contains 64 KB of emulation memory, 254- by 24-bit frames of trace memory, and the control processor. In addition, the controller pod houses a BNC connector that can be used to connect up to 10 multi-ICE compatible emulators for synchronous starting and stopping of emulation.

The serial cable connects the host system to the controller pod. The serial cable supports a subset of the RS-232C signals.

The user probe assembly consists of a user cable and a processor module. The processor module houses the emulation processor and the interface logic. The target adaptor connects to the processor module and provides an electrical and mechanical interface to the target microcontroller socket.

The crystal power accessory (CPA) is a small, detachable board that connects to the controller pod and enables the ICE-5100/044 emulator to run in stand-alone mode. The target adaptor plugs into the socket on the CPA; the CPA then supplies clock and power to the user probe.

The clips assembly enables the user to trace external events. Eight bits of data are gathered on the rising edge of $\overline{\text{PSEN}}$ during opcode fetches. The clips information can be displayed using the CLIPS option with the PRINT command.

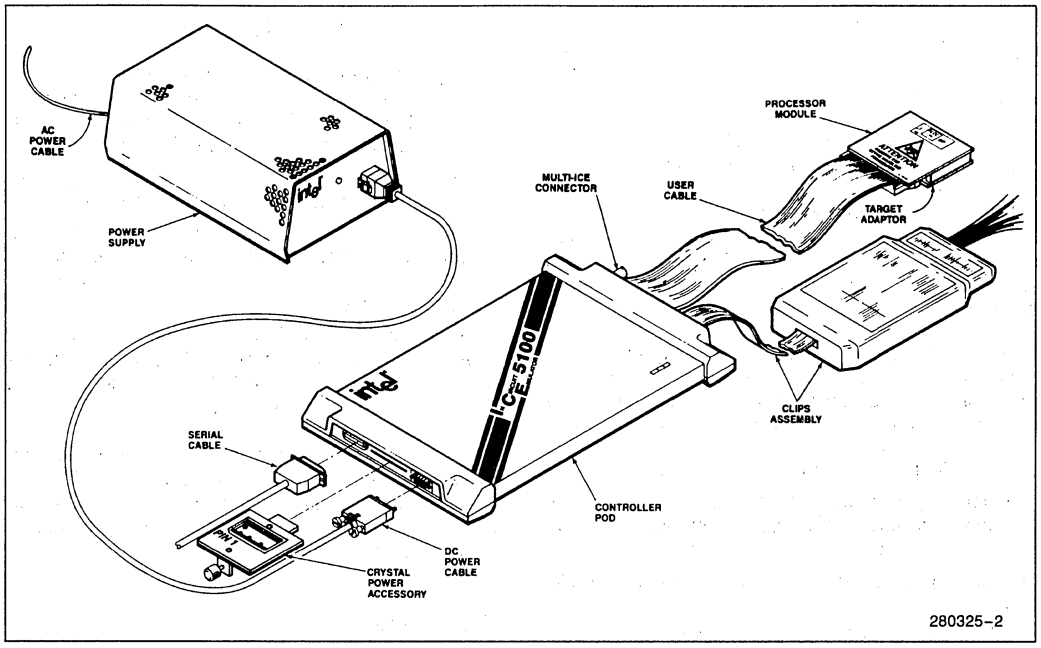


Figure 1. The ICE™-5100/044 Emulator Hardware

The ICE-5100-044 emulator software supports mnemonics, object file formats, and symbolic references generated by Intel's ASM-51 and PL/M-51 programming languages. Along with the ICE-5100/044 emulator software is a customer confidence test disk with diagnostic routines that check the operation of the hardware.

The on-line tutorial is written in the ICE-5100 command language. Thus, the user is able to interact with and use the ICE-5100/044 emulator while executing the tutorial.

A comprehensive set of documentation is provided with the ICE-5100/044 emulator.

ICE™-5100/044 EMULATOR FEATURES

The ICE-5100/044 emulator has been created to assist a product designer in developing, debugging and testing designs incorporating the RUPI-44 family of peripherals. The following sections detail some of the ICE-5100/044 emulator features.

Emulation

Emulation is the controlled execution of the user's software in the target hardware or in an artificial hardware environment that duplicates the microcontroller of the target system. Emulation is a transparent process that happens in real-time. The execution of the user software is facilitated with the ICE-5100/044 command language.

Memory Mapping

There is a 64 KB of memory that can be mapped to the CODE memory space in 4 KB blocks on 4 KB boundaries. By mapping memory to the ICE-5100/044 emulator, software development can proceed before the user hardware is available.

Memory Examination and Modification

The memory space for the 8044 microcontroller and its target hardware is fully accessible through the emulator. The ICE-5100/044 emulator refers to four physically distinct memory spaces, as follows:

- CODE—references program memory
- IDATA—references internal data memory
- RDATA—references special function register memory
- XDATA—references external data memory

ICE-5100/044 emulator commands that access memory use one of the special prefixes (e.g., CODE) to specify the memory space.

The microcontroller's special function registers and register bits can be accessed mnemonically (e.g., DPL, TCON, CY, P1.2) with the ICE-5100/044 emulator software.

Data can be displayed or modified in one of three bases: hexadecimal, decimal, or binary. Data can also be displayed or modified in one of two formats: ASCII or unsigned integer. Program code can be disassembled and displayed as ASM-51 assembler mnemonics. Code can be modified with standard ASM-51 statements using the built-in single-line assembler.

Symbolic references can be used to specify memory locations. A symbolic reference is a procedure name, line number, program variable, or label in the user program that corresponds to a location.

Some typical symbolic functions include:

- Changing or inspecting the value of a program variable by using its symbolic name to access the memory location.
- Defining break and trace events using symbolic references.
- Referencing variables as primitive data types. The primitive data types are ADDRESS, BIT, BOOLEAN, BYTE, CHAR (character), and WORD.

The ICE-5100/044 emulator maintains a virtual symbol table (VST) for program symbols. A maximum of 61 KB of host memory space is available for the VST. If the VST is larger than 61 KB, the excess is stored on available host system disk space and is paged in and out as needed. The size of the VST is limited only by the disk capacity of the host system.

Breakpoint Specifications

Breakpoints are used to halt a user program in order to examine the effect of the program's execution on the target system. The ICE-5100/044 emulator supports three different types of break specifications:

- Specific address break—specifying a single address point at which emulation is to be stopped.
- Range break—an arbitrary range of addresses can be specified to halt emulation. Program execution within or, optionally, outside the range halts emulation.
- Page break—up to 256 page breaks can be specified. A page break is defined as a range of addresses that is 256-bytes long and begins on a 256-byte address boundary.

Break registers are user-defined debug definitions used to create and store breakpoint definitions. Break registers can contain multiple breakpoint definitions and can optionally call debug procedures when emulation halts.

Trace Specifications

Tracing can be triggered using specifications similar to those used for breaking. Normally, the ICE-5100/044 emulator traces program activity while the user program is executing. With a trace specification, tracing can be triggered to occur only when specific conditions are met during execution. Up to 254 24-bit frames of trace information are collected in a buffer during emulation. Sixteen of the 24 bits trace instruction execution addresses, and 8 bits capture external events (CLIPS).

```
        /* Print newest four instructions in the buffer */
hlt>PRINT NEWEST 4
FRAME    ADDR      CODE      INSTRUCTIONS
(28)     300A      C02A      PUSH      2AH
(30      300C      2532      ADD       A, 32H
(32)     300E      F52A      MOV       2AH, A
(34)     3010      B53210    CJNE      A,32H, $+10H
hlt>
hlt>PRINT CLIPS OLDEST 2     /* Buffer display showing clips */
FRAME    ADDR      CODE      INSTRUCTIONS   CLIPS     (76543210)
(00)     007AH     0508      INC  INDX PTR             10101111
(01)     007CH     80E6      SJMP (#28)                00100010
```

280325-3

Figure 2. Selected Trace Buffer Displays

The trace buffer display is similar to an ASM-51 program listing as shown in Figure 2. The PRINT command enables the user to selectively display the contents of the trace buffer. The user has the option of displaying the clips information as well as dissassembled instructions.

Procedures

Debugging procedures (PROCs) are a user-defined group of ICE-5100/044 commands that are executed as one command. PROCs enable the user to define several commands in a named block structure. The commands are executed by entering thename of the PROC. The PROC bodies are a simple DO . . . END construct.

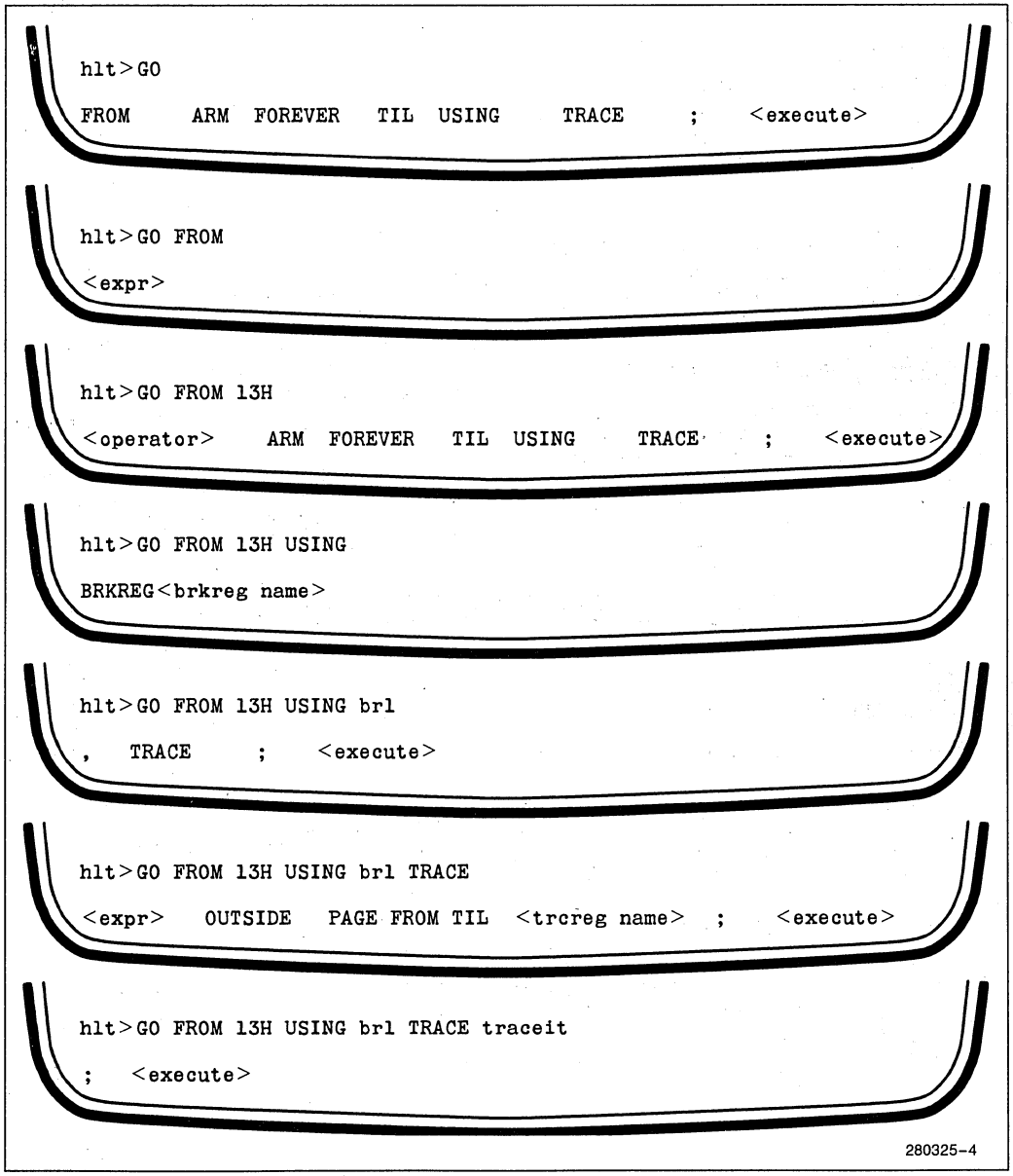


Figure 3. The Integrated Command Directory for the GO Command

PROCs can simulate missing hardware or software, set breakpoints, collect debug information, and execute high-level software patches. PROCs can be copied to text files on disk, then recalled for use in later test sessions. PROCs can also serve as program diagnostics, implementing ICE-5100/044 emulator commands or user-defined definitions for special purposes.

On-Line Syntax Menu

A special syntax menu, called the Integrated Command directory (ICD), similar to the one used for the I²ICE™ system and the VLSiCE-96 emulator, aids in creating syntactically correct command lines. Figure 3 shows an example of the ICD and how it changes to reflect the options available for the GO command.

Help

The HELP command provides ICE-5100/044 emulation command assistance via the host system terminal. On-line HELP is available for the ICE-5100/044 emulator commands shown in Figure 4.

BITBUS™ Applications Support

The ICE-5100/044 emulator provides an ideal environment for developing applications code for BITBUS board products such as the RCB-44/10, the RCB-44/20, the PCX-344, and the iSBX™-344 board.

The BITBUS firmware, available separately as BITWARE, can be loaded into the ICE-5100/044 emulator's memory along with the user's code to enable rapid debug of 8044 BITBUS applications code.

DESIGN CONSIDERATIONS

The height of the processor module and the target adaptor need to be considered for target systems. Allow at least 1½ inches (3.8 cm) of space to fit the processor module and target adaptor. Figure 5 shows the dimensions of the processor module.

Execution of user programs that contain interrupt routines causes incorrect data to be stored in the trace buffer. When an interrupt occurs, the next instruction to be executed is placed into the trace buffer before it is actually executed. Following completion of the interrupt routine, the instruction is executed and again placed into the trace buffer.

ELECTRICAL CONSIDERATIONS

The emulation processor's user-pin timings and loadings are identical to the 8044 component, except as follows.

- Up to 25 pF of additional pin capacitance is contributed by the processor module and target adaptor assemblies.
- Pin 31, $\overline{EA}$, has approximately 32 pF of additional capacitance loading due to sensing circuitry.
- Pins 18 and 19, XTAL1 and XTAL2 respectively, have approximately 15-16 pF of additional capacitance when configured for crystal operation.

```
hlt>HELP

HELP is available for:

ADDRESS    APPEND   ASM        BASE       BIT        BOOLEAN     BRKREG
BYTE       CHAR     CI         CNTL_C     COMMENTS   CONSTRUCTS  COUNT
CURHOME    CURX     CURY       DCI        DEBUG      DEFINE      DIR
DISPLAY    DO       DYNASCOPE  EDIT       ERROR      EVAL        EXIT
EXPRESSION GO       HELP       IF         INCLUDE    INVOCATION  ISTEP
KEYS       LABEL    LINES      LIST       LITERALLY  LOAD        LSTEP
MAP        MENU     MODIFY     MODULE     MSPACE     MTYPE       NAMESCOPE
OPERATOR   PAGING   PARTITION  PRINT      PROC       PSEUDO_VAR  PUT
REFERENCE  REGS     REMOVE     REPEAT     RESET      RETURN      SAVE
STRING     SYMBOLIC SYNCSTART  TEMPCHECK  TRCREG     TYPES       VARIABLE
VERIFY     VERSION  WAIT       WORD       WRITE
hlt>
```

280325-5

Figure 4. HELP Menu

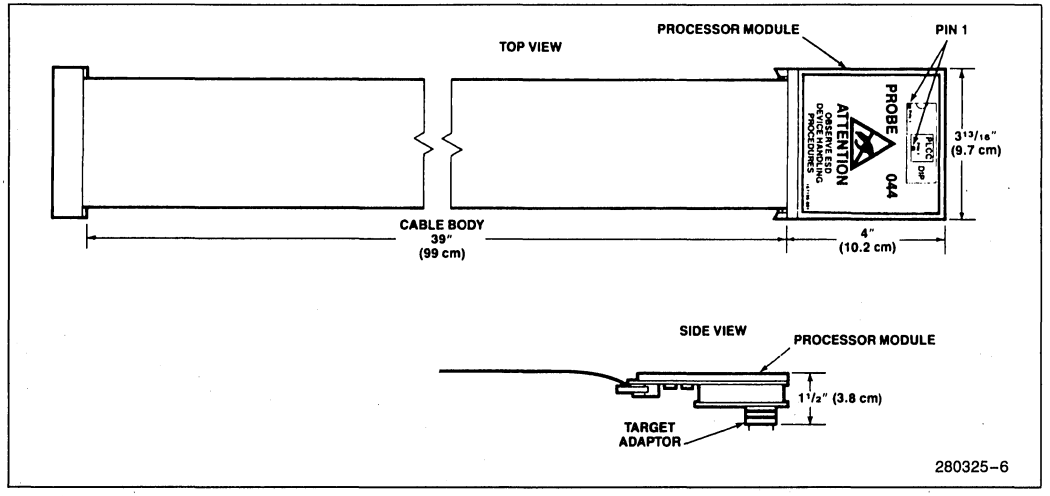


Figure 5. Processor Module Dimensions

HOST REQUIREMENTS

- IBM PC AT or PC XT (or PC DOS compatible) with 512 KB of available RAM and a hard disk running under the DOS 3.0 (or later) operating system.
- Disk drives—dual floppy or one hard disk and one floppy drive required.

ICE™-5100/044 EMULATOR SOFTWARE PACKAGE

- ICE-5100/044 emulator software
- ICE-5100/044 confidence tests
- ICE-5100 tutorial software

EMULATOR PERFORMANCE

Memory

Mappable full-speed emulation code memory	64 KB	Mappable to user or ICE-5100/044 emulator memory in 4 KB blocks on 4 KB boundaries.
Trace memory		254 x 24 bit frames
Virtual Symbol Table		A maximum of 61 KB of host memory space is available for the virtual symbol table (VST). The rest of the VST resides on disk and is paged in and out as needed.

PHYSICAL CHARACTERISTICS

Controller Pod

Width: 8-1/4" (21 cm)
Height: 1-1/2" (3.8 cm)
Depth: 13-1/2" (34.3 cm)
Weight: 4 lbs (1.85 kg)

User Cable

The user cable is 3 feet (approximately 1 m)

Processor Module

(With the target adaptor attached)
Width: 3-13/16" (9.7 cm)
Height: 4" (10.2 cm)
Depth: 1-1/2" (3.8 cm)

Power Supply

Width: 7-5/8" (18.1 cm)
Height: 4" (10.06 cm)
Depth: 11" (27.97 cm)
Weight 15 lbs (6.1 kg)

Serial Cable

The serial cable is 12 feet (3.6 m).

ELECTRICAL CHARACTERISTICS

Power Supply

100-120V or 200-240V (selectable)
50-60 Hz
2 amps (AC max) @ 120V
1 amp (AC max) @ 240V

ENVIRONMENTAL CHARACTERISTICS

Operating temperature	+10°C to +40°C (50°F to 104°F)
Operating humidity	Maximum of 85% relative humidity, non-condensing

ORDERING INFORMATION

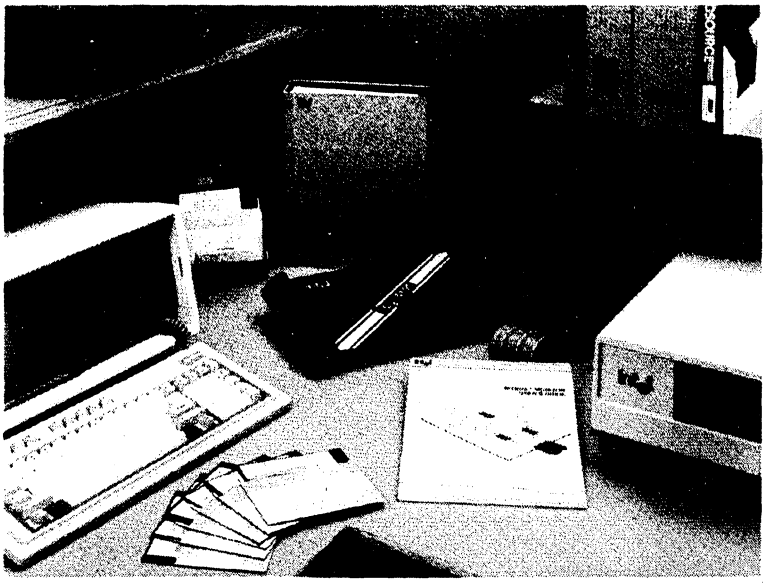
Emulator Hardware and Software

Order Code	Description
I044KITAD	This kit contains the ICE-5100/044 user probe assembly, power supply and cables, serial cables, target adaptor, CPA, ICE-5100 controller pod, software, and documentation for use with an IBM PC AT or PC XT. The kit also includes the 8051 Software Development Package and the AEDIT text editor for use on DOS systems. [Requires software license.]
I044KITD	This kit is the same as the I044KITAD excluding the 8051 Software Development Package and the AEDIT text editor. [Requires software license.]

Other Useful Intel® MCS®-51 Debug and Development Support Products

Order Code	Description
D86ASM51	**8051 Software Development Package** (DOS version)—Consists of the ASM-51 macro assembler which gives symbolic access to 8051 hardware features; the RL51 linker and relocator program that links modules generated by ASM-51; CONV51 which enables software written for the MCS-48 family to be up-graded to run on the 8051, and the LIB51 Librarian which programmers can use to create and maintain libraries of software object modules. Use with the DOS operating system (version 3.0 or later).
D86PLM51	**PL/M-51 Software Package** (DOS version)—Consists of the PL/M-51 compiler which provides high-level programming language support; the LIB51 utility that creates and maintains libraries of software object modules, and the RL51 linker and relocator program that links modules generated by ASM-51 and PL/M-51 and locates the linked object modules to absolute memory locations. Use with the DOS operating system (version 3.0 or later).
D86EDINL	AEDIT text editor for use with the DOS operating system.

BITBUS™ SOFTWARE DEVELOPMENT ENVIRONMENT

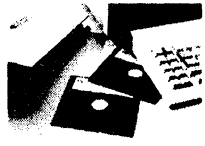


Intel has all the software tools you'll need to implement high-performance applications using Intel BITBUS™ products. Tools include assemblers and compilers for host and BITBUS node code development, debug monitors, in-circuit emulators, and specialized BITBUS software. Intel's software tools are full-featured, easy-to-use, and help generate reliable, easily maintained code in a minimum amount of time. Intel's complete solution helps get your BITBUS-based distributed network quickly to market.

BITBUS NETWORK CONFIGURATIONS

A BITBUS network usually consists of a master (or supervisory) node and multiple remote nodes as shown on figure 1. All BITBUS host interface boards and remote control boards use the 8044 BITBUS Enhanced Microcontroller (8044BEM). The 8044BEM has built-in communications software, memory management and I/O control procedures together with a multitasking operating system. This built-in software, known as DCM44, greatly simplifies the programmer's software design task.

BITBUS networks can be configured in two ways, either as distributed I/O systems with centralized control, or as distributed control systems.



intel

June, 1987
Order Number: 280622-001

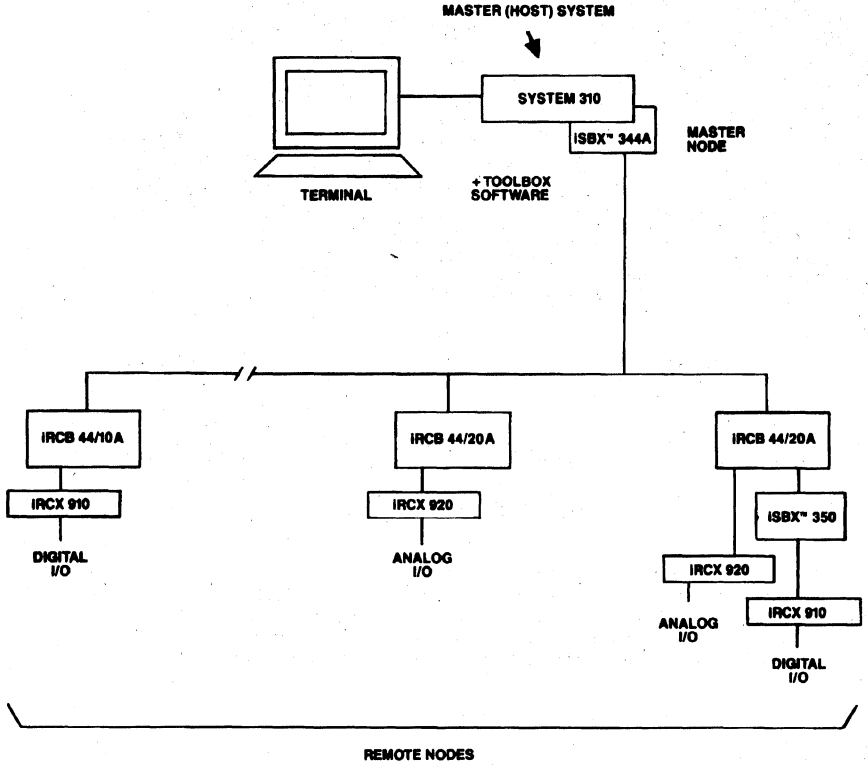


Figure 1: BITBUS™ Network

BUILT-IN RAC PROCEDURES SIMPLIFY DISTRIBUTED I/O APPLICATIONS

Distributed I/O systems are easy to design. Node code (code that runs on the remote BITBUS board) is not required because the network is controlled by the master (host) system. To simplify host code, each BITBUS board comes with a built-in set of procedures known as Remote Access and Control (RAC). The master sends out commands to the nodes and uses these RAC procedures to collect data or to turn on and off motors, valves, indicator lights, and other output devices.

DISTRIBUTED CONTROL BOOSTS PERFORMANCE AND RELIABILITY

Besides using BITBUS for distributed I/O, BITBUS can also be used to implement powerful distributed control systems. With distributed control, the system can more easily control rapidly changing, complex processes (e.g. robotics) and gain the added benefit of higher network reliability that is inherent in distributed control systems.

With distributed control, each board functions as a controller performing a set of dedicated tasks. On a periodic basis, the master can send a command to a remote board to collect process control data or request that a new task start running on a remote board. The built-in DCX 51 multitasking executive on the 8044 BITBUS microcontroller allows up to 7 user tasks to run on the node at the same time. The 12 MHz 8044 8-bit microcontroller, together with the multitasking executive, allows each BITBUS remote board to easily control multiple, complex processes.

HOST SOFTWARE TOOLS

Intel's host software development tools include the BITBUS Toolbox, a wide range of compilers and assemblers for all of Intel's microprocessors, software debug monitors, and in-circuit emulators.

BITBUS™ Toolbox—The Software Tool for All Applications

The BITBUS Toolbox is a set of six software utilities that greatly simplify development of host applications software for BITBUS systems. The utilities include: the BITBUS Monitor; two procedure libraries known as the Universal BITBUS Interface and the BITBUS Interface Handlers; PC Bridge communications software; and the OBJHEX and UDI2DOS code converters.

BITBUS™ Monitor. The BITBUS Monitor provides the designer an on-line "window" into the BITBUS network. Over 35 commands are available allowing an operator to check on the operation of various nodes, turn I/O either on or off, connect or disconnect nodes from the network, start or stop tasks running on a node, and download/upload code to/from remote boards. The Monitor is invaluable when first installing the BITBUS system, and is useful later to troubleshoot a node or the equipment connected to it.

Universal BITBUS™ Interface and BITBUS Interface Handlers. The Universal BITBUS Interface (UBI) is similar in function to the BITBUS Monitor, except that UBI calls can be made directly from the user's host application program rather than from an operator's terminal. Procedures are included that duplicate most of the BITBUS Monitor commands. The UBI is most useful for downloading code to a node, uploading data to the host, starting and stopping tasks running on the node, and writing/reading data to/from the BITBUS boards' I/O ports.

If a programmer wants to develop custom, UBI-like procedures, the Toolbox includes the BITBUS Interface Handlers, which are a set of 4 basic procedures that support communication with a BITBUS node.

PC Bridge, OBJHEX, and UDI2DOS—The Personal Computer Gateway to BITBUS™. The BITBUS Toolbox also includes the PC Bridge communications software and the OBJHEX conversion utility. Many BITBUS networks will use an Intel 310 system as the host in order to take advantage of the system's performance or multitasking capabilities. The PC Bridge and OBJHEX utilities enable the designer to use a PC to generate BITBUS node code, and then download the code through the 310 system to any node on the BITBUS network. The software also allows an operator to use a PC as a virtual terminal to the 310 system.

Some designers may choose to use their PC as the host system for the BITBUS network. To support these networks, the Toolbox includes the UDI2DOS utility, which is used to convert object code, developed using Intel tools, to a ".exe" format so that it will run on a PC.

The BITBUS Toolbox can be used on DOS, iRMX® 86/286, XENIX*, and iPDS™ based systems.

Host Code Compilers, Assemblers, and Other Tools

Intel's languages include PL/M, Fortran, PASCAL, C, and assembler for most of Intel's family of 8, 16, and 32-bit microprocessors. For debug support, PSCOPE, iSDM™, and Soft-Scope*, which are available in several versions, provide the programmer powerful software tools to rapidly isolate and correct faulty host code. These tools are supported on a variety of host systems, including DOS, iRMX 86/286, and XENIX.

For programmers who need an even fuller featured debug environment, Intel's I²ICE™ system combines the capabilities of an in-circuit emulator together with the PSCOPE 86 debug monitor and a 16-channel logic analyzer. The I²ICE system supports 8086, 8088, 80186, 80188, and 80286 code development. For programmers who are designing 80386 code, Intel provides the ICE™ 386 in-circuit emulator. The I²ICE and ICE 386 emulators are supported on DOS and Intel Series III/IV development systems.

SOFTWARE TOOLS FOR BITBUS™ CONTROLLER BOARDS

By adding node programs to BITBUS boards, the designer can take full advantage of the BITBUS boards' 8044 microcontroller's processing abilities. Programmed remote boards enable the designer to configure powerful, distributed control systems with a minimum investment in hardware.

Developing node code for remote BITBUS boards is just as easy as developing host code. Instead of using iAPX-based software, BITBUS boards run programs developed using "8051" tools. These tools include PL/M 51 and ASM 51 languages, RL51/LIB51 Linker/Locator/Librarian, and the ICE 5100/044 in-circuit emulator. BITBUS-specific software tools include DCS110 BITWARE and the DCS120 Programmer's Support Package.

PL/M 51 and ASM 51 Languages

The programmer can write node code using either PL/M 51 or the ASM 51 assembler. Many programs are written using PL/M 51 because the language's higher level statements reduce programming time and produce reliable, easy-to-maintain code. If necessary, speed-critical code is written using ASM 51.

*XENIX is a trademark of Microsoft Inc.; Soft-Scope is a registered trademark of Concurrent Sciences, inc.

Multitasking Executive and DCS120 Maximize System Performance

Included in the 8044BEM microcontroller on every BITBUS board is the DCX 51 multitasking executive, which allows up to 7 user tasks plus the RAC task to run on the board concurrently. If the programmer is writing code for a remote board that controls several interrelated tasks, he can segment the code into separate tasks and increase overall performance by using the multitasking management provided by the executive. Twelve DCX 51 calls are available providing tasks with timing services, communications to other tasks on the board, memory management services, and the ability to dynamically create and delete running tasks.

To access DCX 51 services, Intel provides the DCS120 Programmer's Support Package, which includes an interface library to DCX 51 plus DCX 51 Procedure declaration files. To use DCS120, the programmer adds the declaration files to the source code. Then, after the source modules are compiled, the interface library is linked with the object modules and any other user libraries.

ICE 5100/044 and DCS110— The Bug Chasers

To provide debug support for node code development, Intel provides the ICE 5100/044 in-circuit emulator and the DCS110 BITWARE product. ICE 5100/044 includes an 8044 probe that plugs into the BITBUS board in place of the BITBUS 8044 microcontroller. BITWARE, which is DCM44 firmware, provides the necessary software so the ICE 5100/044 can emulate a BITBUS environment. DCS110 also includes the DCX 51 interface library and declaration files that are provided in the DCS120 product.

INTEL SOFTWARE DEVELOPMENT TOOLS—COMPLETE IN EVERY WAY

Intel provides a complete set of tools for the software designer ranging from compilers and debug monitors for the host system and BITBUS nodes to specialized BITBUS software, like the BITBUS Toolbox and BITWARE. These tools are available for a wide variety of development environments, including Intel's system 310 and the PC as shown in Table 1.

	BITBUS™ TOOLS — TOOLBOX — BBM	UBI	BII	PC Bridge	ORBIIEX	UDI2DOS	BITWARE	Prog. Spt. Pkg.	NODE CODE ASM 51	PLM 51	RL 51, LIB 51	ICE™ ICE 5100/044	ICE 44	EMV 44	EPROM PROG. iUP200A/201A with iUPP87/44A module and iPPS sw	iPDS with iUPP87/44A module and iPPS sw
Series II									C	C	C		E		X	
III			X				X	X	X	X	X	X	E		X	
IV							X	X	X	X	X	X	E		X	
iPDS	A	A	A				X	X	C	C	C			E		X
iRMX 5¼"	X	X	X	X	X		X	X	D	D	D					
8"	X	X	X	X	X		X	X	D	D	D					
XENIX 5¼"	X	X		B	X											
8"	X	X		B	X											
DOS	X	X	X	X	X	X	X	X	X	X	X	X			X	

Notes:
A iPDS uses Release 1 Toolbox
B Supports operation with XENIX. XENIX disks not required
C Down-revision version
D Available for iRMX® 86
E ICE 44 and EMV 44 have been replaced by the ICE™ 5100/044

Table 1

ORDERING INFORMATION

Want to Know More?

Intel publishes several databooks that provide detailed technical information on these and other software products together with application data. If you would like more information about Intel software for BITBUS applications, contact your local Intel sales office or distributor for the following literature:

- Distributed Control Modules Databook 230973
- Development Tools Handbook 210940
- Embedded Controller Handbook 210918

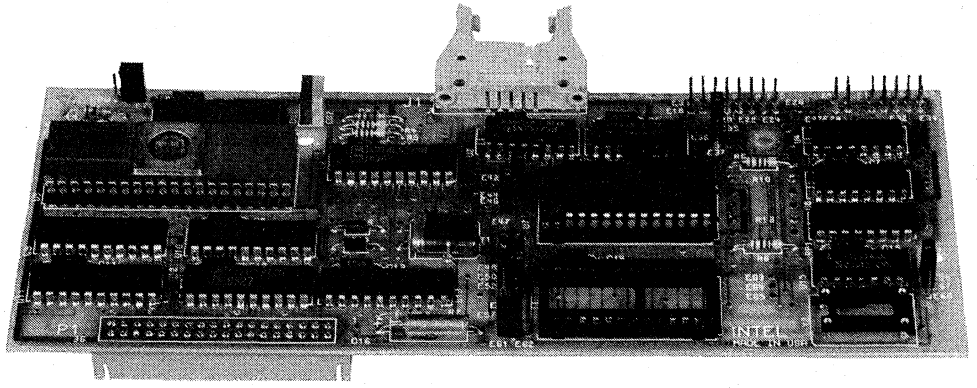
BITBUS Software Products Order Codes:

Product	**Order Code**
BITBUS Toolbox	iDCS100
BITWARE	iDCS110
Programmer's Support Package	iDCS120

iSBX™ 344A
BITBUS™ INTELLIGENT MULTIMODULE™ BOARD

- **High Performance 12 MHz 8044 Controller**
- **Integral Firmware Including the iDCX 51 Executive Optimized for Real-Time Control Applications**
- **Full BITBUS™ Support**
- **2 28-Pin JEDEC Memory Sites for User's Control Functions**
- **Low Cost, Double-Wide iSBX™ BITBUS Expansion MULTIMODULE™ Board**
- **Power Up Diagnostics**

The iSBX 344A BITBUS Intelligent MULTIMODULE board is the BITBUS gateway to all Intel products that support the iSBX I/O Expansion Interface. Based on the highly integrated 8044 component (an 8-bit 8051 microcontroller and an SDLC-based controller on one chip) the iSBX 344A MULTIMODULE board extends the capability of other microprocessors via the BITBUS interconnect. With the other members of Intel's Distributed Control Modules (iDCM) family, the iSBX 344A MULTIMODULE board expands Intel's OEM microcomputer system capabilities to include distributed real-time control. Like all members of the iDCM family, the iSBX 344A MULTIMODULE board includes many features that make it well suited for industrial control applications such as: data acquisition and monitoring, process control, robotics, and machine control.



280247-1

March 1988
Order Number: 280247-002

OPERATING ENVIRONMENT

Intel's Distributed Control Modules (iDCM) product family contains the building blocks to implement real-time distributed control applications. The iDCM family incorporates the BITBUS interconnect to provide standard high speed serial communication between microcontrollers. The iDCM hardware products: including the iSBX 344A MULTIMODULE board, iPCX 344A board and all iRCB BITBUS Remote Controller Boards communicate in an iDCM system via the BITBUS interconnect as shown in Figure 1.

As a member of the iDCM product line the iSBX 344A MULTIMODULE board fully supports the BITBUS microcontroller interconnect. Typically, the iSBX 344A MULTIMODULE board would be part of a node (master or slave) on the BITBUS interconnect in an iDCM system. As shown in Figure 2 the iSBX 344A MULTIMODULE board plugs into any iSBC® board with an iSBX connector.

The iSBX 344A MULTIMODULE board is the hardware interface between Intel's MULTIBUS® and the BITBUS environment. With this interface the user can harness the capabilities of other Intel microprocessors e.g. 80386, 80286, 80186, 8086, 80188, 8088 in a iDCM system or extend an existing MULTIBUS system with the iDCM family.

MULTIBUS® Expansion

Typically, MULTIBUS iSBC boards have a maximum of two iSBX I/O expansion connectors. These connectors facilitate addition of one or two iSBX I/O MULTIMODULE boards with varying numbers of I/O lines. The iSBX 344A MULTIMODULE board increases the number of I/O lines that can be accommodated by a MULTIBUS system by at least an order of magnitude.

Extending BITBUS™/iDCM System Processing Capability

The iSBX 344A MULTIMODULE board allows utilization of other processors in a iDCM system to accommodate particular application requirements. The MULTIMODULE board is compatible with any iSBX connector so that any board having a compatible connector can potentially enhance system performance. Intel's DCS100 BITBUS Toolbox Software provides easy to use high performance software interfaces for iSBC boards. The iSBC 86/35, 286/12, and 188/48 boards are a few examples. Custom configurations are also possible with user customized software.

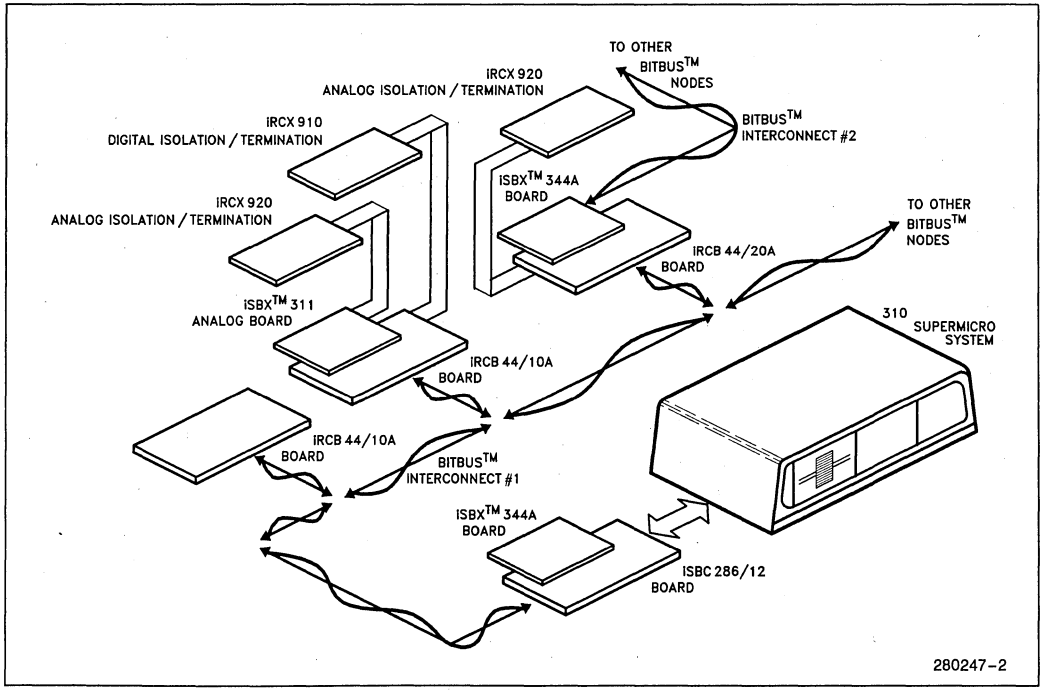


Figure 1. iDCM Operating Environment

ARCHITECTURE

Figure 3 illustrates the major functional blocks of the iSBX 344A board: 8044 BITBUS Enhanced Microcontroller (BEM), memory, BITBUS microcontroller interconnect, Byte FIFO interface, initialization and diagnostic logic.

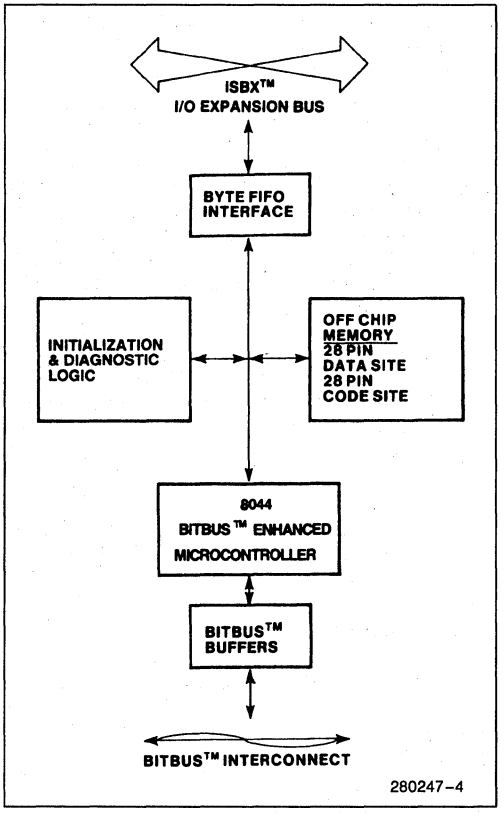


Figure 3. iSBX™ 344A Block Diagram

iDCM Controller

The heart of the iSBX 344A MULTIMODULE board's controlling and communication capability is the highly integrated 12 MHz 8044 microcontroller. The 8044 consists of the advanced 8-bit, 8051 microcontroller and a SDLC-based controller called the Serial Interface Unit (SIU). This dual processor architecture allows complex control and high speed communication to be realized cost effectively.

The 8044 BEM microcontroller also includes built-in firmware known as DCM44. This firmware includes a set of functions called Remote Access and Control (RAC), a preconfigured version of the DCX51 Executive, communications software, and a power-up test procedure.

Memory

The iSBX 344A MULTIMODULE board memory consists of two internal and external memory. Internal memory is located in the on-chip memory of the iDCM controller. The iDCX 51 Executive and the remaining 8044 BEM firmware ration this resource. However, eight bytes of bit addressable internal memory are reserved for the user. Ample space is reserved for user programs and data in the iSBX 344A MULTIMODULE board external memory.

Two 28-pin JEDEC sites comprise the iSBX 344A MULTIMODULE board external memory. One site has been dedicated for data; the other for code. Table 1 lists the supported memory devices for each site. Intel's 2764 and 27128 are examples. The user may choose one of two memory configurations and specify different memory sizes by placing the proper jumpers at system initialization. The most flexible configuration option provides the user with access to the code site for program download or upload. This feature ensures expansion of an existing system is easily accommodated. For example, the addition of another conveyor to a material handling system would require adding another controller or controllers and changes to existing applications code and addition of new code.

Table 1. Supported Memory Devices

Device	Data Site	Code Site
4K x 8–64K x 8 EPROM/ROM	No	Yes
2K x 8–32K x 8 SRAM	Yes	Yes
2K x 8–16K x 8 NVRAM and E2PROM	No	Yes

BITBUS™ Microcontroller Interconnect

The iSBX 344A MULTIMODULE board fully supports the BITBUS microcontroller interconnect. The BITBUS interconnect is a serial bus optimized for control applications. The interconnect supports both synchronous and self-clocked modes of operation. These modes of operation are selectable dependent on application requirements as are the transmission rates. Table 2 shows different combinations of modes of operations, transmission rates, and distances. The SDLC-based protocol, BITBUS message format, and compatibility with Intel's other software and hardware products comprise the remainder of this established architecture. These features contribute to BITBUS reliability and usefulness as a microcontroller interconnect.

The BITBUS connection consists of one or two differential pair(s) of wires. The BITBUS interface of the iSBX 344A MULTIMODULE board consists of a half-duplex RS 485 transceiver and an optional clock source for the synchronous mode of operation.

Byte FIFO Interface

The Byte FIFO Interface on the iSBX 344A MULTIMODULE board implements the required hardware buffering between the 8044 BEM and an extension. An extension is defined as a device attached to the iSBX I/O expansion interface on the iSBX 344A MULTIMODULE board. In an iDCM system, an example of an extension is an iSBC 286/12 board which may be considered the host board in a MULTIBUS system. When used with the software handlers in the BITBUS Toolbox, implementation of this interface is complete.

For particular applications, the user may wish to develop a custom software interface to the extension or host board. On the iSBX 344A MULTIMODULE board side of the interface the iDCM firmware automatically accepts messages for the FIFO. No user code is required, increasing the time available for application system development.

The Byte FIFO supports both byte and message transfer protocol in hardware via three register ports: data, command, and status. The extension side supports polled, interrupt, and limited DMA modes of operation (e.g. 80186 type DMA controllers).

Initialization and Diagnostic Logic

Like the other members of Intel's Distributed Control Modules (iDCM) product line, the iSBX 344A MULTIMODULE board includes many features which make it well suited for industrial control applications. Power up diagnostics is just one of these features. Diagnostics simplify system startup considerably, by immediately indicating an 8044 BEM or external bus failure. The LEDs used for power up diagnostics are available for user diagnostics after power up as well as to further contribute to reliable operation of the system.

Initial iSBX 344A MULTIMODULE board parameters are set by positioning jumpers. The jumpers determine the BITBUS mode of operation: synchronous, self-clocked, transmission rate, and address of the iSBX module in the BITBUS system. This minimizes the number of spare boards to be stocked for multiple nodes, decreasing stocking inventory and cost.

INTEGRAL FIRMWARE

Resident firmware located in the 8044 BEM includes: a pre-configured iDCX 51 Executive for user program development; a Remote Access and Control (RAC) function that enables user communication and control of different microcontrollers and I/O points; a communications gateway to connect the BITBUS interconnect, iSBX bus, and iDCX 51 Executive tasks; and power up diagnostics.

Table 2. BITBUS™ Microcontroller Interconnect Modes of Operation

	Speed Kb/s	Maximum Distance Between Repeaters M/ft	Maximum # Nodes Per Segment	Maximum # Repeaters Between a Master and Any Slave
Synchronous	500–2400	30/100	28	0
Self Clocked	375 62.5	300/1000 1200/4000	28 28	2 10

Segment: Distance between master and repeater or a repeater and a repeater.
Synchronous mode requires user supplied crystal.

The iDCX 51 Executive is an event-driven software manager that can respond to the needs of multiple tasks. This real-time multitasking executive provides: task management, timing, interrupt handling, and message passing services. Table 3 shows the iDCX 51 calls. Both the executive and the communications gateway allow for the addition of up to seven user tasks at each node while making BITBUS operations transparent.

The Remote Access and Control Function is a special purpose task that allows the user to transfer commands and program variables to remote BITBUS controllers, obtain the status of a remote I/O line(s), or reverse the state of a remote I/O line. Table 4 provides a complete listing of the RAC services. No user code need be written to use this function.

The services provided by the iSBX 344A MULTIMODULE board integral firmware simplify the development and implementation of complex real-time control application systems. All iDCM hardware products contain integral firmware thus supplying the user with a total system solution.

DEVELOPMENT ENVIRONMENT

Intel provides a complete development environment for the iSBX 344A MULTIMODULE board. Software development support consists of: the 8051 Software Development Package, the DCS100 BITBUS Toolbox Host Software Utilities, the DSC110 Bitware for ICE™ Support, and the DCS120 Programmer's Support Package. The 8051 Software Development Package provides the RL 51 Linker and Relocator Program, and ASM 51. PL/M 51 is also available. Hardware tools consist of the In-Circuit Emulator (ICE 5100/044).

Table 3. iDCX 51 Calls

Call Name	Description
TASK MANAGEMENT CALLS	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION$IDS	Obtain the function IDs of tasks currently in the system.
INTERTASK COMMUNICATION CALLS	
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.
MEMORY MANAGEMENT CALLS	
RQGETMEM	Get available SMP memory.
RQ$RELEASE$MEM	Release SMP memory.
INTERRUPT MANAGEMENT CALLS	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RQ$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
TIMER MANAGEMENT CALLS	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

Table 4. RAC Services

RAC Service	Action Taken by Task 0
RESET_STATION	Perform a software reset.
CREATE_TASK	Perform an RQ$CREATE$TASK system call.
DELETE_TASK	Perform an RQ$DELETE$TASK system call.
GET_FUNCTION_ID	Perform an RQGETFUNCTION$IDS call.
RAC_PROJECT	Suspend or resume RAC services.
READ_I/O	Return values from specified I/O ports.
WRITE_I/O	Write to the specified I/O ports.
UPDATE_I/O	Update the specified I/O ports.
UPLOAD_MEMORY	Return the values in specified memory area.
DOWNLOAD_MEMORY	Write values to specified memory area.
OR_I/O	OR values into specified I/O ports.
AND_I/O	AND values into specified I/O ports.
XOR_I/O	XOR values into specified I/O ports.
READ_INTERNAL	Read values at specified internal RAM areas.
WRITE_INTERNAL	Write values to specified internal RAM areas.
NODE_INFO	Return device related information.
OFFLINE	Set node offline.
UPLOAD_CODE	Read values from code memory space.
DOWNLOAD_CODE	Write values to specified EEPROM memory.

NOTE:
Internal memory locations are included in the 192 bytes of data RAM provided in the microcontroller. External memory refers to memory outside the microcontroller — the 28-pin sockets of the iSBX 344A module and the iRCB 44/10A board. Each RAC Access Function may refer to multiple I/O or memory locations in a single command.

SPECIFICATIONS

CPU

8044 BITBUS Enhanced Microcontroller (BEM)

Word Size

Instruction: 8 bits
Data: 8 bits

Processor Clock 12 MHz

Instruction Execution Times

1 μs 60% instructions
2 μs 40% instructions
4 μs Multiply & Divide

Memory Capacity/Addressing

iDCM Controller: Up to 64 Kbytes code

Address Range

	Option A	Option B
External Data Memory	0000H–7FFFH	0000H–7FFFH
External Code Memory	1000H–0FFFFH	8000H–0FEFFH
Internal Code Memory	0000H–0FFFH	0000H–0FFFH

Option A: Supports maximum amount of external EPROM code memory.
Option B: Supports downloading code into external RAM or EEPROM memory.

Terminations

Sockets provided on board for ¼ Watt 5% Carbon type resistors. Resistor value to match characteristic impedance of cable as closely as possible—120Ω or greater.

Message Size

54 bytes max

8044 BITBUS™ Enhanced Microcontroller (8044 + Firmware) I/O Addressing as Viewed from the 8044

Function	Address	Read	Write	Bit	Comments
Data	FF00H	✓	✓		
Command	FF01H	✓	✓		Write sets command to extension — Read clears command from extension
Status					
-RFNF*	B3H	✓		✓	Also INT1 Input
-TFNE*	B2H	✓		✓	Also INT0 Input
-TCMD*	92H	✓		✓	
LED #1	90H	✓	✓	✓	
LED #2	91H	✓	✓	✓	
RDY/NE*	B4H	✓	✓	✓	
Node Address	FFFFH	✓			
Configuration	FFFEH	✓			

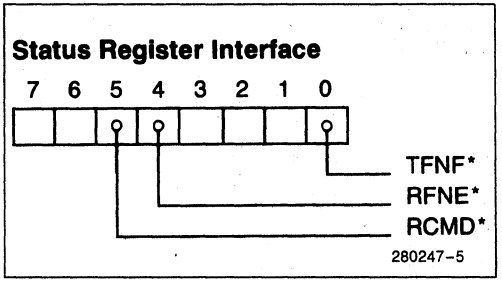
iSBX™ 344A MULTIMODULE™ Board I/O Addressing as Viewed from the iSBX™ 344A MULTIMODULE™ Board

Register Function	Address	Comments
Data	Base′	Read/Write
Command	Base′ + 1	Write sets command from extension Read clears command to extension
Status	Base′ + 2	Read Only

Interrupt/DMA Lines

Signal	Location	Interface Option
RINT	MDRQ/MINT0	INT
TINT	MINT1	INT
RCMI	OPT0	INT or DMA
RDRQ	MDRQ/MINT0	DMA
TDRQ	MINT1	DMA

Status Register Interface



Connector Options

10 Pin Plug

Flat Cable: 3M 3473-6010, TB Ansley 609-1001M, or equal

Discrete Wire: BERG 65846-007, ITT Cannon 121-7326-105, or equal

Pinout

Pin	Signal
1	+12V
2	+12V
3	GND
4	GND
5	DATA*
6	DATA
7	DCLK*/RTS*
8	DCLK/RTS
9	RGND
10	RGND

Electrical Characteristics

Interfaces

iSBX™ I/O Expansion Bus: supports the standard I/O Expansion Bus Specification with compliance level IEEE 959.

Memory Sites: Both code and data sites support the standard 28-pin JEDEC site.

BITBUS™ Interconnect: Fully supported synchronous mode at 2.4 Mbits/sec and self clocked mode for 375 kbits/sec and 62.5 kbits/sec

The iSBX 344A MULTIMODULE board presents one standard load to the BITBUS bus

Power Requirements

0.9A at +5V ±5% (does not include power to the memory devices)

Physical Characteristics

Double-wide iSBX™ MULTIMODULE™ Form Factor

Dimensions

Height: 10.16 mm (0.4 in) maximum component height

Width: 63.5 mm (2.50 in)

Length: 190.5 mm (7.50 in)

Weight: 113 gm (4 ounces)

Environmental Characteristics

Operating Temperature: 0°C to 55°C at 200 Linear Feet/Minute Air Velocity

Humidity: 90% non-condensing

Reference Manual (NOT Supplied)

148099— iSBX 344A Intelligent BITBUS Interface Board User's Guide

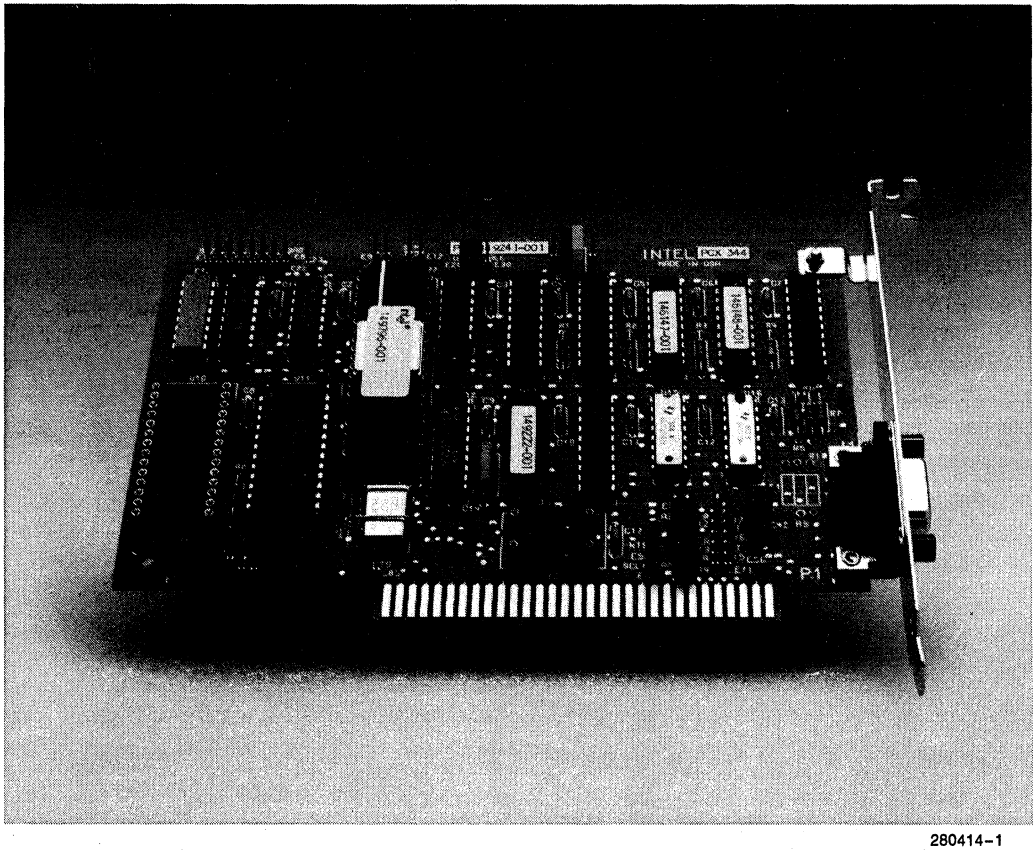
Ordering Information

Part Number	Description
iSBX 344A	BITBUS Intelligent MULTIMODULE board

iPCX 344A
BITBUS™ IBM* PC INTERFACE BOARD

- **High Performance 12 MHz 8044 Single-Chip Microcontroller**
- **Integral Firmware Optimized for Real-Time Control Applications Using the BITBUS™ Interconnect**
- **Fully Supports Intel's Complete Remote Control Board Product Line (iRCB)**
- **Compatible with Intel's DOS-Based Development Tools**
- **External Memory Sites for User's Control Programs**
- **IBM PC System Form Factor Board**
- **Power Up Diagnostics**

The iPCX 344A BITBUS IBM PC INTERFACE board provides the BITBUS gateway to IBM's family of Personal and Industrial Computers. Based on Intel's highly integrated 8044 (an 8051 microcontroller and an SDLC controller on one chip) the iPCX 344A IBM PC INTERFACE board extends the real-time control capability of the IBM PC via the BITBUS interconnect. The PC system performs the human interface functions for the BITBUS interconnect. Like all members of Intel's Distributed Control Modules (iDCM) family, the iPCX 344A IBM PC INTERFACE board includes features that make it well suited for Industrial Control applications such as: data acquisition and monitoring, process control, machine control, and statistical process control (SPC).



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*IBM is a trademark of International Business Machines.

March 1988
Order Number: 280414-002

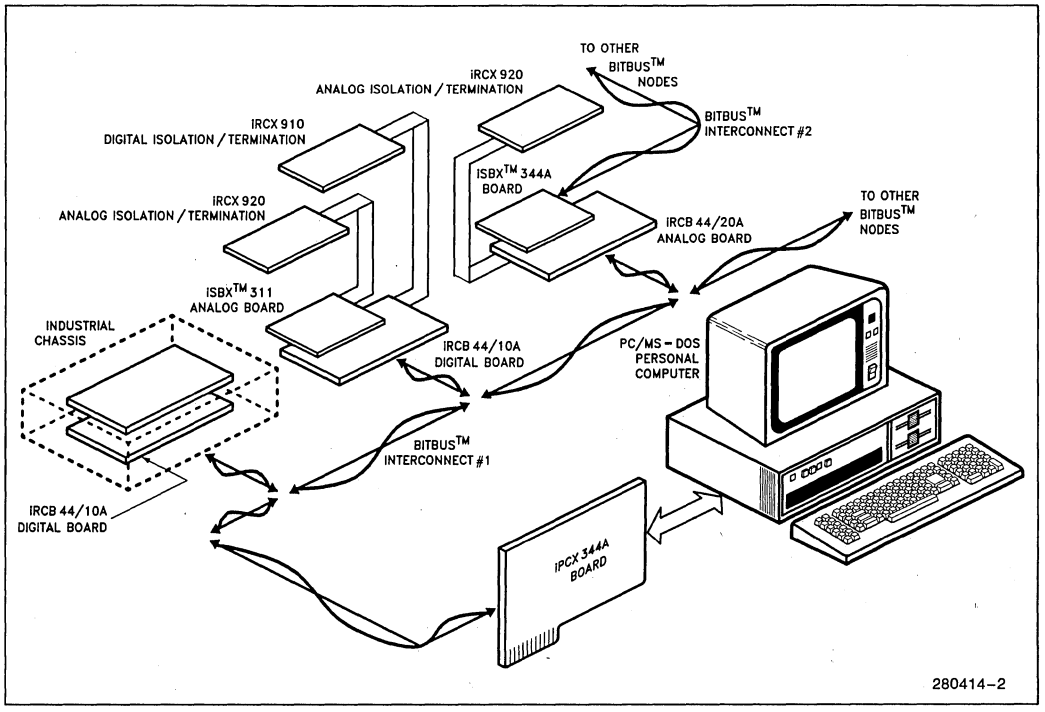


Figure 1. iDCM Operating Environment

OPERATING ENVIRONMENT

Intel's Distributed Control Modules (iDCM) product family provides the building blocks to implement real-time distributed I/O control applications. All of the iDCM family utilizes the BITBUS interconnect to provide standard high speed serial communication between microcontrollers. The iDCM hardware products: including the iPCX 344A board, iSBX™ 344A MULTIMODULE™ board and all iRCB BITBUS Remote Controller Boards communicate in an iDCM system via the BITBUS interconnect as shown in Figure 1.

As a member of the iDCM Product line, the iPCX 344A IBM PC INTERFACE board fully supports the BITBUS microcontroller interconnect. Typically, the iPCX 344A IBM PC System INTERFACE board will be part of a node (master or slave) on the BITBUS interconnect. The iPCX 344A board plugs into the PC add-in slot.

The iPCX 344A IBM PC INTERFACE board is the hardware interface between the PC system and the BITBUS environment. With this interface the user can utilize the human interface and application software of the PC and extend the I/O range of the PC to include real-time distributed control.

ARCHITECTURE

Figure 2 illustrates the major functional blocks of the iPCX 344A IBM PC INTERFACE board: 8044 BITBUS ENHANCED MICROCONTROLLER, memory, BITBUS interconnect, PC System Interface, and initialization/diagnostic logic.

Memory, mode of operation, and bus transmission rate options are easily selected by the user, thereby decreasing inventory levels and associated costs.

8044 BITBUS™ Enhanced Microcontroller (BEM)

The source of the iPCX 344A IBM PC INTERFACE board's controlling and communication capability is Intel's highly integrated 12 MHz 8044 microcontroller. The 8044 consists of the advanced 8-bit, 8051 microcontroller and a SDLC controller called the Serial Interface Unit (SIU). This dual processor architecture provides complex control and high speed communications in a cost-effective, single chip implementation.

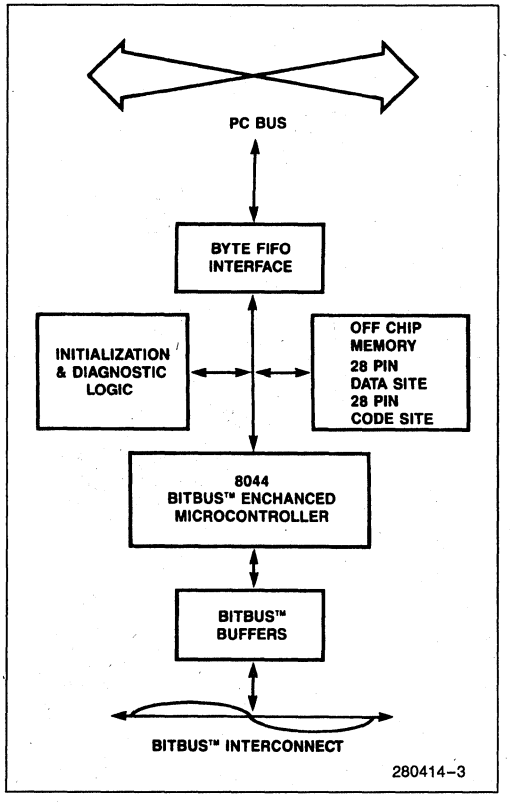


Figure 2. iPCX 344A Block Diagram

Another essential part of the 8044 controller is the integral firmware residing on-chip to implement the BITBUS interface. In the operating environment of the iPCX 344A board, the 8044's SIU acts as an SDLC controller offloading the on-chip 8051 microcontroller of communication tasks; freeing the 8051 to concentrate on real-time control.

The 8044 BEM (8044 microcontroller and on-chip firmware) provides in one package a simple user interface, and high performance communications and control capabilities to efficiently and economically build a complex control system.

Memory

The iPCX 344A IBM PC System INTERFACE board contains both internal and external memory. Internal memory is located in the on-chip memory of the 8044 BEM. The BITBUS firmware includes Intel's powerful iDCX 51, real-time, multitasking, executive. Eight bytes of bit-addressable internal memory are reserved for the user. Additional space is reserved for user programs and data in the board's external memory.

Two 28-pin JEDEC sites comprise the iPCX 344A board's external memory. One site is dedicated to data; the other to code. Table 1 lists the supported memory devices for each site. Intel's 2764 and 27128 are examples. The user can choose one of two memory configurations and specify different memory sizes by configuring the correct jumpers. This configurability provides the user with access to the code site for program download or upload and ensures that an existing system is easily expanded.

Table 1. Supported Memory Devices

Device	Data Site	Code Site
4K x 8–64K x 8 EPROM/ROM	No	Yes
2K x 8–32K x 8 SRAM	Yes	Yes
2K x 8–16K x 8 NVRAM and E^2PROM	No	Yes

BITBUS™ Microcontroller Interconnect

The iPCX 344A IBM PC INTERFACE board fully supports the BITBUS microcontroller interconnect. The BITBUS interconnect is a serial bus optimized for control applications and supports both synchronous and self-clocked modes of operation. Each mode of operation and the different transmission rates are jumper selectable dependent on application requirements.

Table 2 shows different combinations of mode of operation, transmission rate, and distance. The SDLC protocol, BITBUS message format, and compatibility with Intel's other software and hardware products comprise the remainder of this established architecture. These features contribute to BITBUS reliability and usefulness as a microcontroller interconnect.

The BITBUS connection consists of one or two differential user selected pair(s) of wires. The BITBUS interface on the iPCX 344A board consists of a half-duplex RS485 transceiver and an optional clock source for the synchronous mode of operation.

PC System Interface

The iPCX 344A board will operate in any IBM PC XT, PC AT, or compatible system that meets the following requirements:

— An IBM PC, PC XT with an oscillator running at 4.77 MHz (processor running at 4.77 MHz also)

— An IBM PC AT with an oscillator running at 12 or 16 MHz (processor running at 6 or 8 MHz)

— An available I/O channel with addresses that are *not* used by any other boards in the system in the range of 200H to 3FFH on even addresses

— At least one available system interrupt (required ONLY if running the iPCX 344A board in interrupt mode; user selectable from PC Interrupts 2, 3, 4, 5, 6, or 7)

All IBM guidelines have been followed to ensure complete IBM PC system compatibility.

Initialization and Diagnostic Logic

Like the other members of Intel's Distributed Control Modules (iDCM) product line, the iPCX 344A BITBUS IBM PC INTERFACE board includes many features making it well suited for industrial control applications. Power on diagnostics simplify system startup considerably by immediately indicating an 8044 BEM or external bus failure.

INTEGRAL FIRMWARE

The iPCX 344A BITBUS PC-BUS INTERFACE board contains resident firmware located in the 8044 BITBUS ENHANCED MICROCONTROLLER. This on-chip firmware consists of: a pre-configured iDCX 51 Executive for real-time, multitasking control; DCM 44, a Remote Access and Control (RAC) program that enables BITBUS communication and control of I/O points on the BITBUS interconnect; and power up diagnostics.

The iDCX 51 Executive is an event-driven software manager that can respond to the needs of multiple tasks. This real-time multitasking executive provides: task management, timing, interrupt handling, and message passing services. Table 3 shows the iDCX 51 operating system calls. The executive supports up to seven user tasks at each node while making BITBUS operations transparent.

Remote Access and Control (RAC) is a special purpose task that allows the user to transfer commands and program variables to and from BITBUS controllers to obtain the status of I/O or data line(s), or reverse the state of an I/O line or read and write memory, etc. No user code need be written to use this function. See Table 4 for a complete listing of RAC services.

The services provided by the iPCX 344A board's integral firmware simplify the development and implementation of complex real-time control systems.

DEVELOPMENT ENVIRONMENT

Intel provides a variety of development environments for BITBUS applications. Intel's Development Systems and OEM Systems Handbooks provide details on the following development tools.

— BITBUS TOOLBOX—BITBUS Monitor and Interface Handlers

— ASM/PLM 51—Low and High level languages for application code generation on 8044

Table 2. BITBUS™ Microcontroller Interconnect Modes of Operation

	Speed Kb/s	Maximum Distance Between Repeaters M/ft	Maximum # Nodes Per Segment*	Maximum # Repeaters Between a Master and Any Slave
Synchronous	500–2400	30/100	28	0
Self Clocked	375 62.5	300/1000 1200/4000	28 28	2 10

*Segment: Distance between master and repeater or repeater and repeater.
Synchronous mode requires user supplied crystal.

Table 3. iDCX 51 Systems Calls

Call Name	Description
TASK MANAGEMENT CALLS	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION IDS	Obtain the function IDs of tasks currently in the system.
INTERTASK COMMUNICATION CALLS	
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.

Table 3. iDCX 51 Systems Calls (Continued)

Call Name	Description
MEMORY MANAGEMENT CALLS	
RQGETMEM	Get available SMP memory.
RQ$RELEASE$MEM	Release SMP memory.
INTERRUPT MANAGEMENT CALLS	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RE$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
TIMER MANAGEMENT CALLS	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

Table 4. RAC Services

RAC Service	Action Taken by Task 0
RESET_STATION	Perform a software reset.
CREATE_TASK	Perform an RQ$CREATE$TASK system call.
DELETE_TASK	Perform an RQ$DELETE$TASK system call.
GET_FUNCTION_ID	Perform an RQGETFUNCTION$IDS call.
RAC_PROJECT	Suspend or resume RAC services.
READ_I/O	Return values from specified I/O ports.
WRITE_I/O	Write to the specified I/O ports.
UPDATE_I/O	Update the specified I/O ports.
UPLOAD_MEMORY	Return the values in specified memory area.
DOWNLOAD_MEMORY	Write values to specified memory area.
OR_I/O	OR values into specified I/O ports.
AND_I/O	AND values into specified I/O ports.
XOR_I/O	XOR values into specified I/O ports.
READ_INTERNAL	Read values at specified internal RAM areas.
WRITE_INTERNAL	Write values to specified internal RAM areas.
NODE_INFO	Return device related information.
OFFLINE	Set node offline.
UPLOAD_CODE	Read values from code memory space.
DOWNLOAD_CODE	Write values to specified EEPROM memory.

SPECIFICATIONS

CPU

8044 BITBUS Enhanced Microcontroller (BEM)

Word Size

Instruction—8 bits
Data—8 bits

Processor Clock

12.0 MHz

Instruction Execution Time

1 μs 60% instructions
2 μs 40% instructions
4 μs Multiply and Divide

Memory Capacity Addressing

iDCM Controller: Up to 64 Kbytes code.

Device	Data	Code
EPROM/ROM		
4K x 8—64K x 8	No	Yes
SRAM		
2K x 8—32K x 8	Yes	Yes
NVRAM and E2PROM		
2K x 8—16K x 8	No	Yes

External I/O Space

0FF00H–0FFFFH (mapped into data memory space)

Termination

Minimum 120Ω each end of BITBUS interconnect with user supplied resistors

Address Ranges

	Option A	Option B
External Data Memory Site	0000H–7FFFH	0000H–7FFFH
External Code Memory Site	1000H–0FFFFH (0000H–0FFFFH If EA Active)	8000H–0FEFFH
Internal Code Memory	0000H–0FFFH	0000H–0FFFH

Option A: Supports maximum amount of external EPROM code memory.
Option B: Supports downloading code into external RAM or EEPROM memory.

Message Size:

Up to 54 bytes

Connectors

Standard 9-pin—D Subminiature socket

Physical Characteristics

IBM PC ADD-ON FORMAT
Height: 3.98 in.
Depth: 6 in.

Interfaces

BITBUS Interconnect: Fully supports synchronous mode at 500 Kbps to 2.4 Mbs and self-clocked modes at 375 Kbs or 62.5 Kbs

Note: On-board ALE clock supports 1 Mbps synchronous operation. All other synchronous mode speeds require user-supplied 2.0 MHz–9.6 MHz crystal.

PC System: Two unidirectional, one-byte-deep, nine-bit FIFO buffers (ninth bit distinguishes between data and command)

Power Requirements

0.9A at +5V ±5% (memory not included)

Environmental Requirements

Operating Temperature: 16°C to 32°C at no air flow
0°C to 55°C at 200 Linear Feet/Minute air velocity

Operating Humidity: 90% Noncondensing

Storage Temperature: −40°C to +70°C

Storage Humidity: 95% Noncondensing

REFERENCE MANUAL

149235-001— iPCX 344A BITBUS IBM PC System Interface Board User's Guide

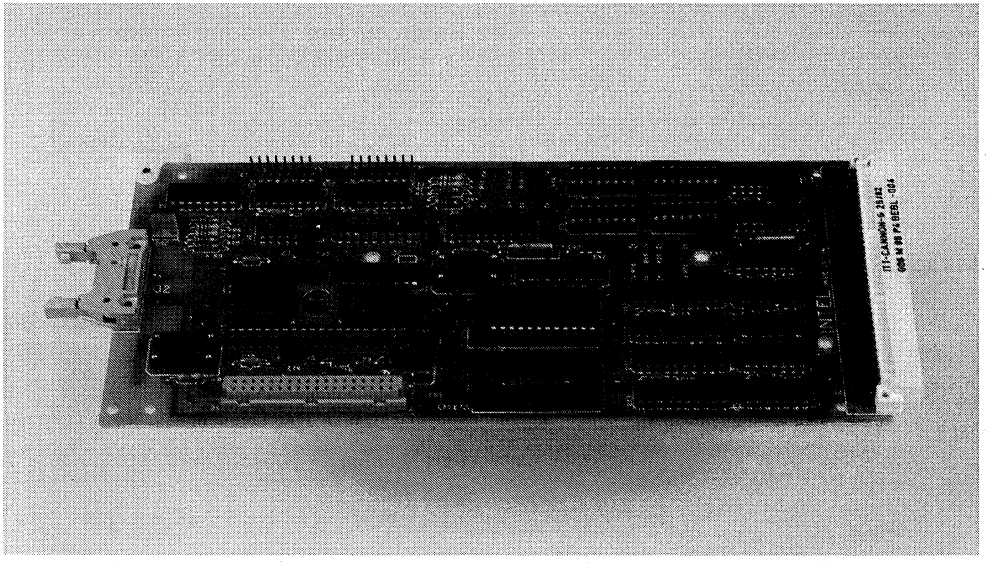
ORDERING INFORMATION

Part Number	Description
iPCX 344A	BITBUS IBM PC System INTERFACE Board

iRCB 44/10A
BITBUS™ DIGITAL I/O REMOTE CONTROLLER BOARD

- **High Performance 12 MHz 8044 Controller**
- **Integral Firmware: iDCX Executive, Optimized for Real-Time Control**
- **Full BITBUS™ Support**
- **Standard Industrial Packaging: Eurocard, DIN Connector**
- **2 28-Pin JEDEC Memory Sites for User's Control Functions**
- **I/O Expansion with 8-Bit iSBX™ Connector**
- **Programmable Control/Monitoring Using 24 Digital I/O Lines**
- **Power Up Diagnostics**
- **Compatible with iRCX 910 Digital Signal Isolation and Termination Module**

The iRCB 44/10A BITBUS™ Digital I/O Remote Controller Board is an intelligent real-time controller and a remote I/O expansion device. Based on the highly integrated 8044 component (an 8 bit 8051 microcontroller and an intelligent SDLC-based controller on one chip) the iRCB 44/10A board provides high performance control capability at low cost. The iRCB 44/10A board can expand Intel's OEM microcomputer system capabilities to include distributed real-time control. Like all members of the iDCM family, the iRCB 44/10A board is well suited for industrial control applications such as data acquisition and monitoring, process control, robotics, and machine control.



280213–1

March 1988
Order Number: 280213-003

OPERATING ENVIRONMENT

Intel's Distributed Control Modules (iDCM) product family contains the building blocks to implement real-time distributed control applications. The iDCM family incorporates the BITBUS interconnect to provide standard high speed serial communication between microcontrollers. The iDCM hardware products, which include the iPCX 344A board, iSBX 344A MULTIMODULE™ board and the iRCB 44/10A BITBUS Remote Controller Board (and other iRCB boards), communicate in an iDCM system via the BITBUS interconnect as shown in Figure 1.

The iRCB 44/10A board can be used as an intelligent remote controller or an I/O expansion device. When performing as an intelligent controller the iRCB 44/10A board not only monitors the status of multiple process points, but it can execute varied user supplied control algorithms. When functioning as an I/O expansion device, the iRCB 44/10A board simply collects data from multiple I/O ports and transmits this information via the BITBUS or iSBX bus interface to the system controller for analysis or updating purposes.

As a member of the iDCM product line, the iRCB 44/10A board fully supports the BITBUS microcontroller interconnect. Typically, the iRCB 44/10A board would be a node in a BITBUS system. The iRCB 44/10A board could be a master or slave node. (The BITBUS system supports a multidrop configuration: one master, many slaves.)

ARCHITECTURE

Figure 2 illustrates the major functional blocks of the iRCB 44/10A board: 8044 BITBUS Enhanced Microcontroller, memory, BITBUS microcontroller interconnect, parallel I/O, iSBX expansion, initialization and diagnostic logic.

8044 BITBUS™ Enhanced Microcontroller

The heart of the iRCB 44/10A board's controlling and communication capability is the highly integrated 12 MHz 8044 microcontroller. The 8044 consists of the advanced 8-bit 8051 microcontroller and a SDLC controller called the Serial Interface Unit (SIU). This dual processor architecture allows complex control and high speed communication functions to be realized cost effectively. The 8044's SIU acts as a SDLC-based controller which offloads the on-chip 8051 microcontroller of communication tasks; freeing the 8051 to concentrate on real-time control.

The 8044 BEM microcontroller also includes, in firmware, a set of procedures known as Remote Access and Control (RAC), a preconfigured version of the DCX 51 Executive, communications software, and power-up diagnostics.

The BEM (8044 microcontroller and on-chip firmware) provides, in one package, a simple user interface, and high performance communications and control capabilities to efficiently and economically build a complex control system.

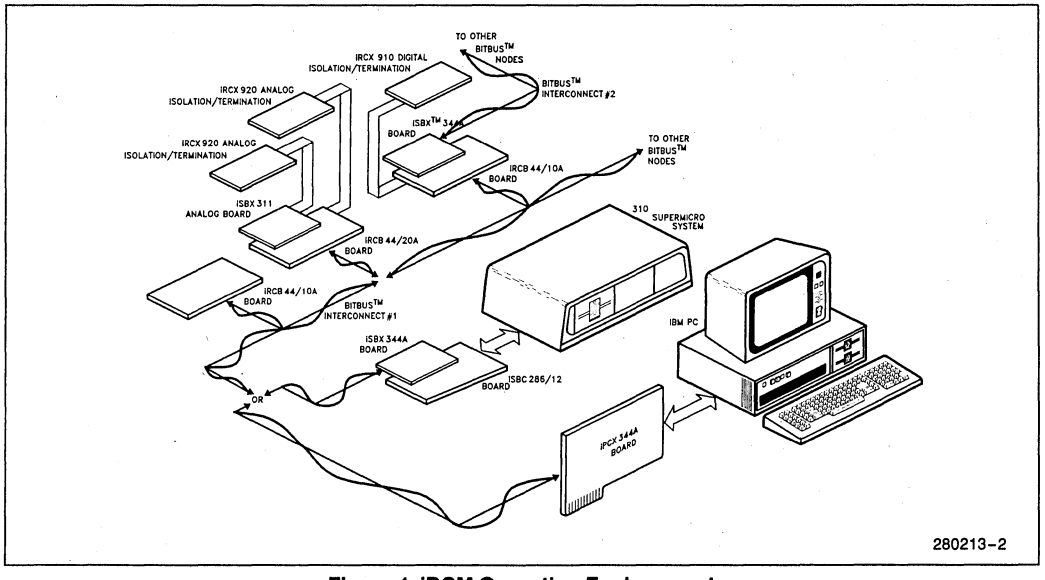


Figure 1. iDCM Operating Environment

Memory

The iRCB 44/10A board memory consists of two sections: internal and external. Internal memory is located in the on-chip memory of the BEM. The iDCX51 Executive and the remaining BEM firmware ration this resource. However, eight bytes of bit addressable internal memory are reserved for the user. Ample space is reserved for user programs and data in the iRCB 44/10A board external memory.

Two 28 pin JEDEC sites comprise the iRCB 44/10A board external memory. One site has been dedicated for data, the other for code. Table 1 lists the supported memory devices for each site. Intel's 2764, and 27128 are examples. The user may choose one of two memory configurations and specify different memory sizes by placing the proper jumpers at system initialization. The most flexible configuration option provides the user with access to the code site for program download or upload. This feature ensures expansion of an existing system is easily accommodated.

Table 1. Supported Memory Devices

Device	Data Site	Code Site
4K × 8-64K × 8 EPROM/ROM	NO	YES
2K × 8-32K × 8 SRAM.	YES	YES
2K × 8-16K × 8 NVRAM and E2PROM	NO	YES

BITBUS™ Microcontroller Interconnect

The iRCB 44/10A board serial interface fully supports the BITBUS microcontroller interconnect. The BITBUS interconnect is a serial bus optimized for

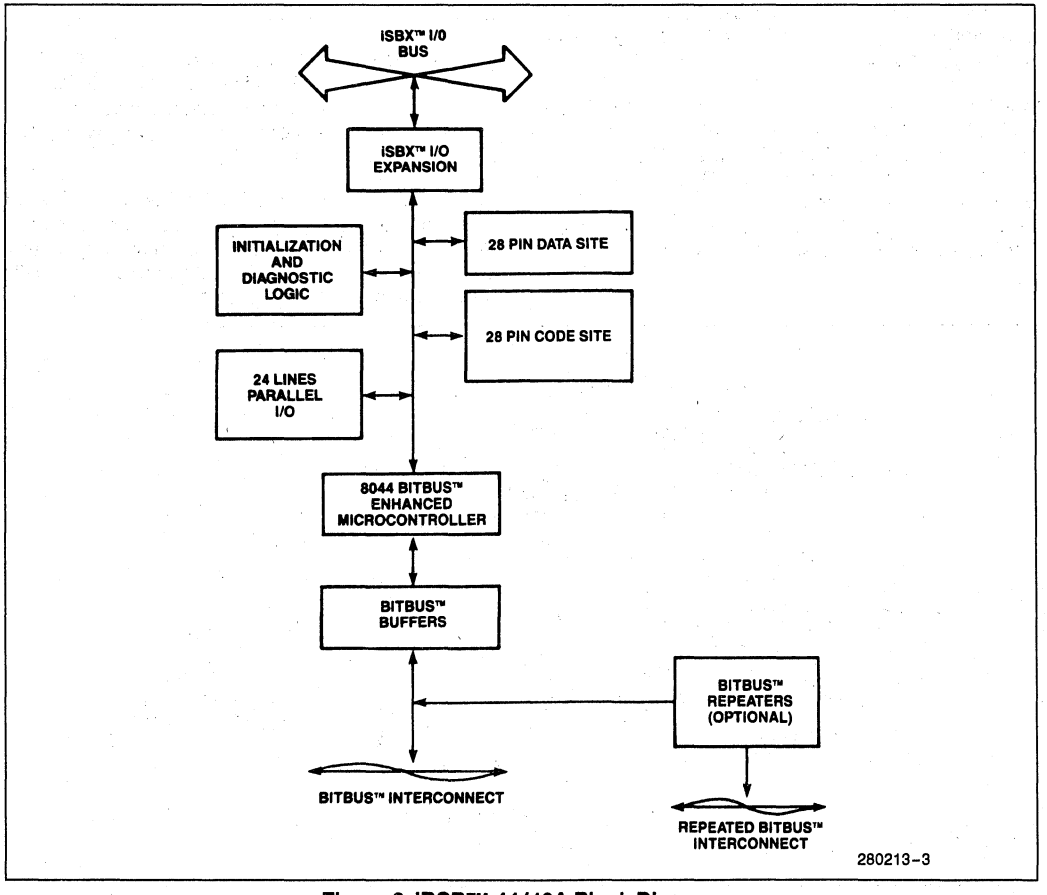


Figure 2. iRCB™ 44/10A Block Diagram

control applications. The bus supports both synchronous and self-clocked modes of operation. These modes of operation are selectable dependent on application requirements as are the transmission speeds. Table 2 shows the different combinations of modes of operation, transmission speeds, and distances. The SDLC-based protocol, BITBUS message format, and compatibility with Intel's other software and hardware products comprise the remainder of the BITBUS architecture. These features contribute to BITBUS system reliability and usefulness as a microcontroller interconnect.

The BITBUS connection consists of one or two differential pair(s) of wires. The serial (BITBUS) interface of the iRCB 44/10A board consists of: a half-duplex RS 485 transceiver, an optional BITBUS repeater and an optional clock source for the synchronous mode of operation.

Digital Parallel I/O

In order to provide an optimal parallel I/O interface for control applications, the iRCB 44/10A board supports 24 software programmable parallel I/O lines. This feature supplies the flexibility and simplicity required for control and data acquisition systems. Sixteen of these lines are fully programmable as inputs or outputs, with loopback, on a bit by bit basis so that bit set, reset, and toggle operations are streamlined. The remaining eight lines are dedicated as inputs. Figure 3 depicts the general I/O port structure.

The parallel I/O lines can be manipulated by using the Remote Access and Control (RAC) function (in BEM firmware) from a supervisory node or locally by a user program. The user program can also access the RAC function or directly operate the I/O lines. Input, output, mixed— input and output, and bit operations are possible simply by reading or writing a particular port.

iSBX™ Expansion

One iSBX I/O expansion connector is provided on the iRCB 44/10A board. This connector can be used to extend the I/O capability of the board. In addition to specialized and custom designed iSBX boards, a full line of compatible high speed, 8-bit expansion MULTIMODULE boards, both single and double wide, are available from Intel. The only incompatible modules are those that require the MWAIT* signal or DMA operation. A few of Intel's iRCB 44/10A board compatible iSBX MULTIMODULE boards include: parallel I/O, serial I/O, BITBUS expansion, IEEE 488 GPIB, analog input and analog output.

With the iSBX 344A BITBUS Controller MULTIMODULE board and user supplied software, the iRCB 44/10A board can act as an intelligent BITBUS repeater facilitating the transition between two BITBUS segments operating at different speeds.

Initialization and Diagnostic Logic

Like the other members of Intel's Distributed Control Modules (iDCM) product line, the iRCB 44/10A board includes many features which make it well suited for industrial control applications. Power up diagnostics is just one of these features. Diagnostics simplify system startup considerably, by immediately indicating an iDCM controller or external bus failure. The LEDs used for power up diagnostics are

Table 2. BITBUS™ Microcontroller Interconnect Modes of Operation

	Speed Kb/s	Maximum Distance Between Repeaters M/ft	Maximum #Nodes Per Segment*	Maximum # Repeaters Between A Master And Any Slave
Synchronous	500–2400	30/100	28	0
Self Clocked	375 62.5	300/1000 1200/4000	28 28	2 10

*Segment: Distance between master and repeater or repeater and repeater. Synchronous mode requires user supplied crystal.

available for user diagnostics after power up as well to further contribute to reliable operation of the system.

Initial iRCB 44/10A board parameters are set by positioning jumpers. The jumpers determine the BITBUS mode of operation: synchronous, self clocked, transmission speed, and address of the iRCB 44/10A board in the BITBUS system. This minimizes the number of spare boards to be stocked for multiple nodes, decreasing stocking inventory and cost.

INTEGRAL FIRMWARE

The iRCB 44/10A board contains resident firmware located in the 8044 BEM. The on-chip firmware consists of: a pre-configured iDCX 51 Executive for user program development; a Remote Access and Controller (RAC) function that enables user communication and control of different microcontrollers and I/O points; a communications gateway to connect the BITBUS interconnect, iSBX bus, iPCX bus and iDCX 51 tasks; and power up diagnostics.

Table 3. iDCX 51 Executive Calls

Call Name	Description
TASK MANAGEMENT CALLS	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION$IDS	Obtain the function IDs of tasks currently in the system.
INTERTASK COMMUNICATION CALLS	
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.
MEMORY MANAGEMENT CALLS	
RQGETMEM	Get available SMP memory.
RQ$RELEASE$MEM	Release SMP memory.
INTERRUPT MANAGEMENT CALLS	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RQ$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
TIMER MANAGEMENT CALLS	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

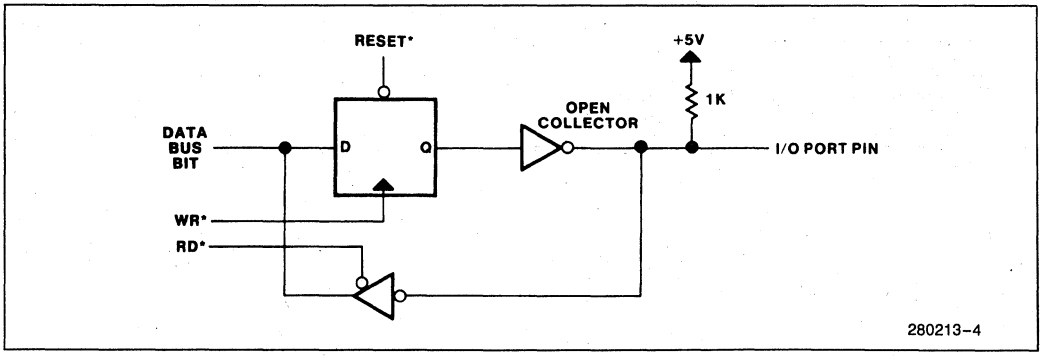


Figure 3. I/O Port Structure

The iDCX 51 Executive is an event-driven software manager that can respond to the needs of multiple tasks. This real-time multitasking executive provides: task management, timing, interrupt handling, and message passing services. Table 3 shows the iDCX 51 calls. Both the Executive and the communications gateway allow for the addition of up to seven user tasks at each node while making BITBUS operation transparent.

The Remote Access and Control Function is a special purpose task that allows the user to transfer commands and program variables to remote BITBUS controllers, obtain the status of a remote I/O line(s), or reverse the state of a remote I/O line. Table 4 provides a complete listing of the RAC services. No user code need be written to use this function. Power up tests provide a quick diagnostic service.

The services provided by the iRCB 44/10A board integral firmware simplify the development and implementation of complex real-time control application systems. All iDCM hardware products contain integral firmware thus supplying the user with a total system solution.

Table 4. RAC Services

RAC Service	Action Taken by Task 0
RESET_STATION	Perform a software reset.
CREATE_TASK	Perform an RQ$CREATE$TASK system call.
DELETE_TASK	Perform an RQ$DELETE$TASK system call.
GET_FUNCTION_ID	Perform an RQGETFUNCTION$IDS call.
RAC_PROTECT	Suspend or resume RAC services.
READ_IO	Return values from specified I/O ports.
WRITE_IO	Write to the specified I/O ports.
UPDATE_IO	Update the specified I/O ports.
UPLOAD_MEMORY	Return the values in specified memory area.
DOWNLOAD_MEMORY	Write values to specified memory area.
OR_I/O	OR values into specified I/O ports.
AND_I/O	AND values into specified I/O ports.
XOR_I/O	XOR values into specified I/O ports.
READ_INTERNAL	Read values at specified internal RAM areas.
WRITE_INTERNAL	Write values at specified internal RAM areas.
NODE_INFO	Return device related information.
OFFLINE	Set node offline.
UPLOAD_CODE	Read values from code memory space.
DOWNLOAD_CODE	Write values to specified EEPROM memory.

INDUSTRIAL PACKAGING

The iRCB 44/10A form factor is a single high, 220 mm deep Eurocard and supports most standard industrial packaging schemes as well as Intel's RCX 910 Digital Signal Conditioning, Isolation and Termination Module (see below). The Eurocard form factor specifies reliable DIN connectors. A standard 64 pin connector is included on the iRCB 44/10A board.

Physical Characteristics

Single high, 220 mm deep Eurocard Form Factor

Dimensions

Width: 13.77 mm (0.542 in) maximum component height

Height: 100 mm (3.93 in.)

Depth: 220 mm (8.65 in.)

Weight: 169 gm (6 ounces)

DIGITAL SIGNAL CONDITIONING, ISOLATION, AND TERMINATION

The RCB 44/10A is fully compatible with the RCX 910 Digital Signal Conditioning, Isolation and Termination Panel. The RCX 910 panel provides integral mounting for one RCB 44/10A, with connectors for power, the BITBUS interconnect signals, and 24 Industry Standard I/O isolation and signal conditioning modules. These modules, available from a number of vendors worldwide, typically provide greater than 1500V isolation and support signal conditioning in a number of voltages including 5–60 VDC, 120 and 240 VAC.

SPECIFICATIONS

Word Size

Instruction: 8 bits

Data: 8 bits

Processor Clock 12 MHz

Instruction Execution Times

1 μsec 60% instructions
2 μsec 40% instructions
4 μsec Multiply & Divide

Memory Capacity/Addressing

iDCM Controller: Up to 64 Kbytes code

DEVELOPMENT ENVIRONMENT

Intel provides a complete development environment for the iRCB 44/10A board.

BITBUS™ Development Environments

	BITBUS™ TOOLS								NODE CODE			ICE™	EPROM PROG.	
	DCS 100 TOOLBOX													
	BBM	UBI	BIH	PC Bridge	OBJHEX	UDI2DOS	DCS 110	DCS 120	ASM 51	PL/M 51	RL 51, LIB 51	ICE 5100/044	iUP200A/201A with iUPF87/44A module and iPPS sw	iPDS with iUPF87/44A module and iPPS sw
Series II									C	C	C		X	
III			X				X	X	X	X	X	X	X	
IV							X	X	X	X	X	X	X	
iPDS	A	A	A				X	X	C	C	C			X
iRMX 5¼"	X	X	X	X	X		X	X	D	D	D			
8"	X	X	X	X	X		X	X	D	D	D			
XENIX 5¼"	X	X		B	X									
8"	X	X		B	X									
DOS	X	X	X	X	X	X	X	X	X	X	X	X	X	

NOTES:
A. iPDS uses Release 1 Toolbox.
B. Supports operation with XENIX. XENIX disks not required.
C. Down-revision version.
D. Available for iRMX® 86.

Address Ranges

Memory	Option A	Option B
External —Data	0000H-7FFFH	0000H-7FFFH
—Code	1000H-0FFFFH	8000H-0FEFFH
Internal	0000H-0FFFH	0000H-0FFFH

NOTES:
Option A: Supports maximum amount of external EPROM code memory.
Option B: Supports downloading code into RAM or EEPROM memory.

Interrupt Sources

Two external: iSBX I/O Expansion bus sources or other sources.
BITBUS Microcontroller Interconnect.

8044 BITBUS™ Enhanced Microcontroller I/O Addressing

Function	Address	Read	Write	Bit
PORT A	FFCOH	✓	✓	
PORT B	FFC1H	✓		
PORT C	FFC2H	✓	✓	
MCSO	FF80H-FF87H FF00, FF01	✓	✓	
MSC1	FF88H-FF8F	✓	✓	
LED #1	90H	✓	✓	✓
LED #2	91H	✓	✓	✓
RDY/NE*	B4H	✓	✓	✓
NODE ADDRESS	FFFFH	✓		
CONFIGURATION	FFFEH	✓		
OPT0	92H	✓	✓	✓
OPT1	93H	✓	✓	✓
INT0	B2H	✓		✓
INT1	B3H	✓		✓

PARALLEL I/O

Number: 2 8-Bit Bi-directional Ports
1 8-Bit Input Port

Table 5. Parallel I/O Electrical Specification

Parameter	Condition	Min	Max	Units
V_{OL}	$I_{OL}=16$ mA		0.5	V
V_{OH}	$I_{OH}=-2$ mA	2.4		V
V_{IH}		2.0	7.0	V
V_{IL}		−1.0	0.8	V
I_{IL}	$V_{IL}=0.5V$		6.0	mA
I_{IH}	$V_{IH}=$ logic high		0.0	mA
I_I	$V_{IH}=7V$		−2.2	mA

Terminations

Sockets provided on board for 1/4 Watt 5% Carbon type resistors. Resistor value to match characteristic impedance of cable as closely as possible—120Ω or greater.

Repeaters

Sockets provided on board: Devices 75174 and 75175

Connector Options

10 PIN PLUG

Flat Cable: 3M 3473-6010, TB Ansley 609-1001M, or equal

Discrete Wire: BERG 65846-007, ITT Cannon 121-7326-105, or equal

DIN CONNECTOR PLUG

Flat Cable: GW Elco 00-8259-096-84-124, Robinson Nugent RNE-IDC64C-TG30, or equal

Discrete Wire: ITT Cannon G06 M96 P3 BDBL-004 GW Elco 60 8257 3017, or equal

10 Pin Repeater Connector Pin Out

Pin	Signal
1	+12V
2	+12V
3	GND
4	GND
5	DATA*
6	DATA
7	DCLK*/RTS*
8	DCLK/RTS
9	RGND
10	RGND

Electrical Characteristics

Interfaces

iSBX I/O expansion bus: supports the standard I/O Expansion Bus Specification with compliance level D8/8F

Memory Sites: Both code and data sites support the electrical Universal Memory Site specification

BITBUS™ Interconnect: The iRCB 44/10A Remote Controller Board supports the BITBUS Specification as follows:

Fully supported synchronous mode at 2.4 Mbits/second and self clocked mode for 375 kbits/second and 62.5 kbits/second

The iRCB 44/10A Remote Controller Board presents one standard load to the BITBUS without repeaters, with repeaters two standard loads

Message length up to 54 bytes supported

RAC Function support as shown in Table 4

Parallel I/O: See the Table 5 for Electrical Specifications of the interface.

Power Requirements

0.9A at +5V ±5% iRCB 44/10 board only (power to memory, repeater, or iSBX board NOT included)

Environmental Characteristics

Operating Temperature: 0°C to 55°C at 200 Linear Feet/Minute Air Velocity

Humidity: 90% non-condensing

Reference Manual (NOT Supplied)

iRCB 44/10 Digital I/O Remote 148100-001 Controller Board User's Guide

Ordering Information

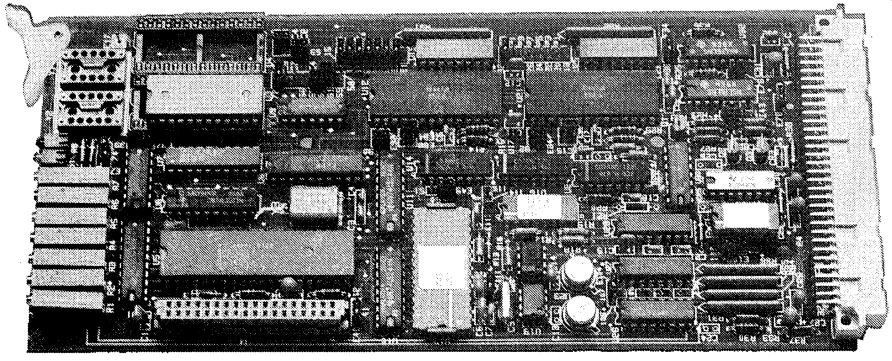
Part Number	Description
iRCB 44/10A	BITBUS Digital I/O Remote Controller Board

iRCB 44/20A
ANALOG I/O CONTROLLER

- **Distributed Intelligence via BITUS™ Serial Bus**
- **8044 8-bit Microcontroller at 12 MHz**
- **12-bit Analog Resolution**
- **Up To 20 KHz Aquisition Rate (50 ms)**
- **Software Programmable Gain: 1, 10, 100, 500**
- **Two 28-pin JEDEC Memory Sites**
- **16 Single-ended or 8 Differential Input Channels**
- **2 Outputs Channels**
- **±10V Range or 4–20 mA Current Loop**
- **I/O Expandable via iSBX™ Connector**
- **Compact Single-Eurocard Packaging**
- **Low Power Consumption**
- **Compatible with iRCX 920 Analog Signal Conditioning, Isolation and Termination Panel**

The iRCB 44/20A is a fully programmable analog I/O subsystem on a single-Eurocard form-factor board. The resident 8044 microcontroller operating at 12 MHz provides a means of executing data aquisition and control routines remote from the host computer. Real-time capability is made possible by the iDCX 51 Distributed Control Executive, resident in the 8044 microcontroller. Distribution of real-time control is implemented by the BITBUS Serial Bus protocol, which is also managed integrally by the 8044.

Offering high performance, low-cost, and improved system bandwidth via distributed intelligence, the iRCB 44/20A Analog I/O Controller is ideal for data acquisition and control in both laboratory and industrial environments.



280721-1

MULTIMODULE™ is a trademark of Intel Corporation.

IBM® PC is a registered trademark of International Business Machines Corporation.

November 1988
Order Number: 280721-002

APPLICATION ENVIRONMENT

Intel's Distributed Control Modules (iDCM) product family contains the building blocks to implement real-time distributed control applications. The iDCM family incorporates the BITBUS interconnect to provide standard high-speed serial communication between microcontrollers. The iRCB 44/20A may communicate with other nodes in a distributed system via the BITBUS interconnect as shown in Figure 1. Other nodes in the system may be the iSBX 344A BITBUS Controller MULTIMODULE™, the iPCX 344A BITBUS IBM® PC Interface, the iRCB 44/10A BITBUS Digital I/O Controller Board, or other BITBUS compatible products.

The iRCB 44/20A board, can be used as an intelligent remote controller or an I/O expansion device. When performing as an intelligent controller the iRCB 44/20A board not only monitors the status of multiple sensors, it can also locally execute user developed control algorithms. When functioning as an I/O expansion device the iRCB 44/20A board manages the multiple I/O ports, transmitting this information via the BITBUS bus or iSBX interface to the system controller for analysis or data logging purposes.

Typically, the iRCB 44/20A board will operate as a node in a BITBUS system. BITBUS communication supports a multidrop configuration with one master, and multiple subordinate nodes. The iRCB 44/20A board may be either a master or slave node to manage a wide variety of analog input or output tasks.

FUNCTIONAL DESCRIPTION

The major functional blocks of the iRCB 44/20A board, shown in Figure 2, include the 8044 microcontroller and BITBUS interconnect, local memory, Analog I/O, and iSBX expansion.

Distributed Intelligence

The heart of the iRCB 44/20A board's controlling and communication capability is the highly integrated 8044 microcontroller which operates at 12 MHz. The 8044 contains the advanced 8-bit, 8051 microcontroller and a complimentary SDLC controller, called the Serial Interface Unit (SIU). This dual processor architecture provides complex control and high speed communication functions at a low cost.

Another essential part of the 8044 controller is the on-chip firmware that exercises the BITBUS interface. The 8044's SIU acts as an SDLC controller, off loading the on-chip microcontroller of communication tasks so it may concentrate on real-time control.

The 8044 microcontroller simplifies the user interface, and offers high performance communications and control capabilities in a single component package. Many interconnected Distributed Control Modules can form a powerful platform to efficiently and economically administer a complete control system.

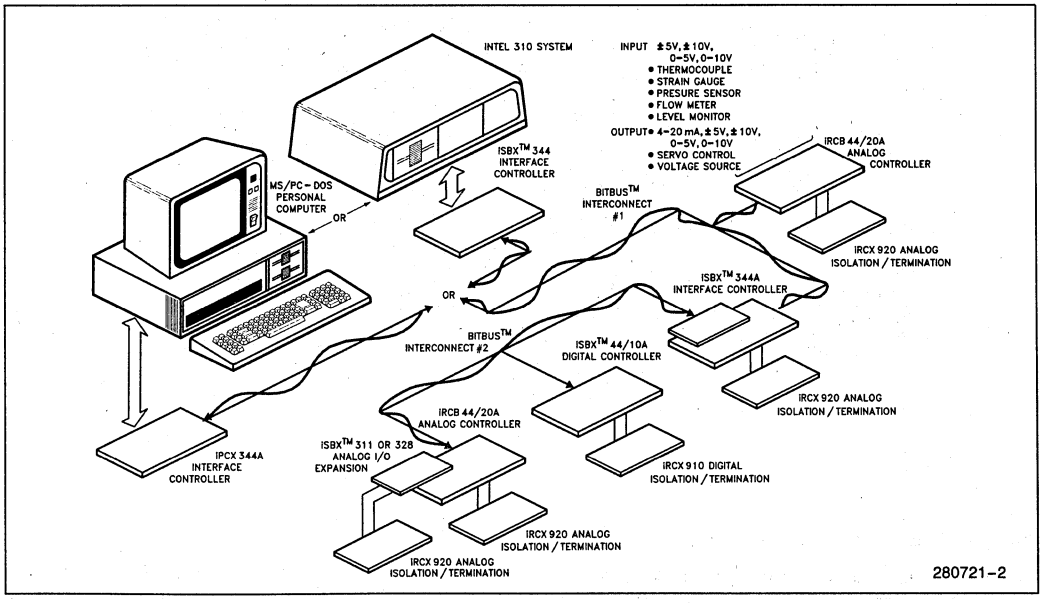


Figure 1. BITBUS Distributed Control Example

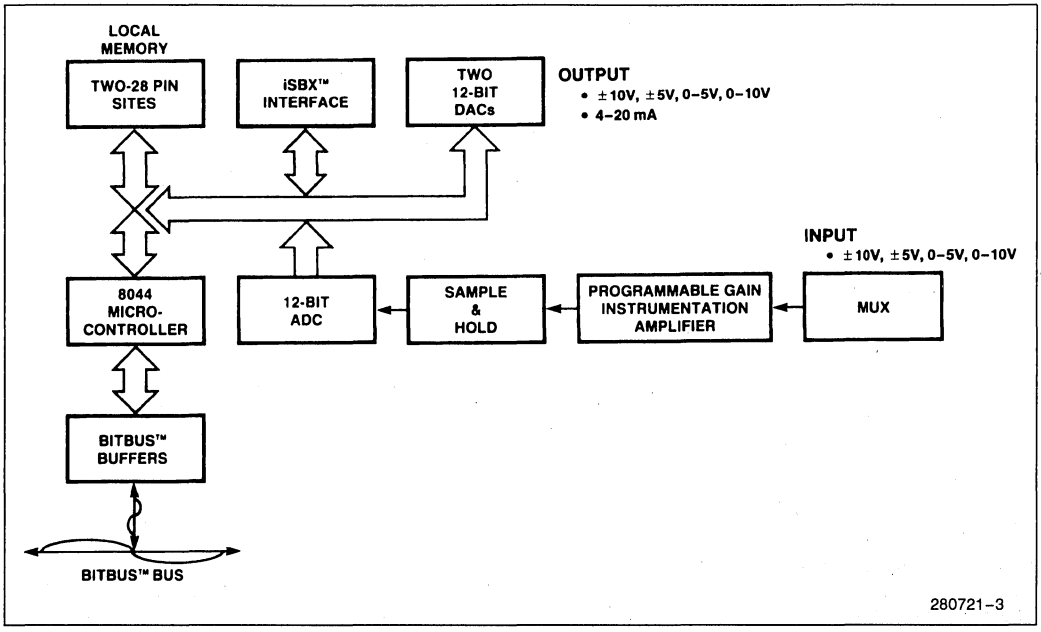


Figure 2. iRCB 44/20A Functional Diagram

BITBUS™ Microcontroller Interconnect

The iRCB 44/20A board fully supports the BITBUS microcontroller interconnect. BITBUS is a serial bus optimized for control applications. Both synchronous and self-clocked modes of operation are supported as well as multiple transmission rates. Table 1 shows the different combinations of modes of operation, transmission speeds, and distances. The SDLC protocol and BITBUS message format comprise the data-link level of the BITBUS architecture. Use of these standards maximizes system reliability and flexibility.

The physical connection to BITBUS uses either one or two pairs of wires across which differential signals travel. The iRCB 44/20A board contains a half-duplex RS 485 tranceiver and an optional clock source for the synchronous mode of operation.

Local Memory

The iRCB 44/20A board contains both internal and external local memory. Internal memory is located within the 8044 controller and is used by the iDCX 51 Executive and the SIU. Eight bytes of bit-addressable internal memory have been reserved for the user.

Two 28-pin JEDEC sites provide the iRCB 44/20A board with memory that is external to the 8044. One site has been dedicated for data, the other for application code. Table 2 lists the supported memory devices for each site. The user may select one of two memory configurations using jumpers. One option provides the user with access to the application code site for uploading or downloading programs, which allows expansion or modification of an existing system from a remote site.

Table 1. BITBUS™ Microcontroller Interconnect Modes Of Operation

	Speed Kb/S	Maximum Distance Between Repeaters M/ft	Maximum # Nodes Per Segment*	Maximum # Repeaters Between A Master And Any Slave
Synchronous	500–2400	30/100	28	0
Self Clocked	375 62.5	300/1000 1200/4000	28 28	2 10

* Segment: Distance between master and repeater or repeater and repeater. Synchronous Mode requires user supplied crystal.

Table 2. Supported Memory Devices

Device	Data Site	Code Site
4K x 8–64K x 8 EPROM/ROM	NO	YES
2K x 8–32K x 8 SRAM	YES	YES
2K x 8–16K x 8 NVRAM and E2PROM	NO	YES

Analog I/O

The iRCB 44/20A has been designed to manage a wide variety of analog functions. The jumper-selectable voltage or current ranges plus software programmable gain allows the iRCB 44/20A to acquire data from a combination of up to 16 thermocouples, strain gauges, pressure transducers, flow meters, level sensors, or any devices that operate on a 4–20 mA current loop. Two analog output channels provide the capability to adjust system parameters locally through servo control, voltage-driven devices, or other actuators that respond to 4–20 mA signals.

The 8044 microcontroller on the iRCB 44/20A allows Proportional Integral/Derivative (PID) algorithms, event timing, or averaging tasks to operate independent of the host computer or programmable controller. By off-loading the host in this manner, the overall system performance can be improved significantly.

The analog I/O lines can be manipulated from a remote supervisor by communicating with the Remote Access and Control (RAC) functions, which are included in the 8044 controller firmware. The local application program running on the iRCB 44/20A can also access the RAC functions or directly operate the I/O lines.

iSBX™ Expansion

One 8-bit iSBX I/O expansion connector is provided to expand the functionality of the iRCB 44/20A board. A full line of compatible expansion MULTIMODULE boards are available from Intel; both single- and double-wide versions are supported by the iRCB 44/20A. Parallel I/O, serial I/O, IEEE 488, magnetic-bubble memory, or additional analog I/O may be added in this manner.

Also, the iSBX 344A BITBUS Controller MULTIMODULE can be used to implement another BITBUS hierarchy with the iRCB 44/20A functioning as the master. With user supplied software, this product combination can operate as an intelligent BITBUS repeater, facilitating the transmission between two BITBUS segments operating at different speeds.

Initialization and Diagnostic Logic

Like the other members of the Intel's Distributed Control Modules (iDCM) product line, the iRCB 44/20A board includes many features which make it well suited for industrial control applications. Power-up diagnostics simplify system initialization by immediately indicating a failure in either the 8044 microcontroller or external bus. On-board LEDs indicate diagnostic status and are available after power-up for user developed diagnostic routines.

Initial iRCB 44/20A board parameters are manually set with jumpers. These jumpers specify the mode of operation (synchronous or self clocked), and transmission speed. The address of the iRCB 44/20A board within the BITBUS system is also declared in this manner. Therefore, spare board inventory is reduced, since the iRCB 44/20A may be positioned at any node address.

INTEGRAL iDCX 51 FIRMWARE

The iRCB 44/20A board contains resident firmware located within the 8044 controller. This on-chip firmware, known as DCM 44, consists of a pre-configured iDCX 51 Distributed Control Executive for user program development and execution, a library of Remote Access and Control (RAC) functions for internode communications and I/O control, plus an iSBX communications gateway, and power-up diagnostics.

The iDCX 51 Executive is an event-driven software manager that can respond to the needs of multiple tasks. This real-time multitasking executive provides task management and timing, interrupt handling, and message passing services. Table 3 shows the iDCX 51 user command library. Both the executive and the communications gateway allow for the addition of seven user tasks at each node that are independent of BITBUS bus management operations.

Remote Access and Control (RAC) functions are special purpose tasks that allow the host system to transfer commands and program variables to remote BITBUS controllers and read/write to the remote I/O lines. Table 4 provides a complete listing of the RAC commands. No user code need be written to use this function. Power-up tests provide a quick diagnostic service.

The DCM 44 firmware, integral to the iRCB 44/20A board, simplifies the development and implementation of complex real-time control applications. All iDCM hardware products contain this integral firmware, providing the user with application code portability.

Table 3. iDCX 51 Executive Calls

Call Name	Description
TASK MANAGEMENT CALLS	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION$IDS	Obtain the function IDs of tasks currently in the system.
INTERTASK COMMUNICATION CALLS	
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.
MEMORY MANAGEMENT CALLS	
RQGETMEM	Get available SMP memory.
RQ$RELEASE$MEM	Release SMP memory.
INTERRUPT MANAGEMENT CALLS	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RQ$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
TIMER MANAGEMENT CALLS	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

Table 4. RAC Services

RAC Service	Action Taken by Task 0
RESET_STATION	Perform a software reset.
CREATE_TASK	Perform an RQ$CREATE$TASK system call.
DELETE_TASK	Perform an RQ$DELETE$TASK system call.
GET_FUNCTION_ID	Perform an RQGETFUNCTION$IDS call.
RAC_PROTECT	Suspend or resume RAC services.
READ_IO	Return values from specified I/O ports.
WRITE_IO	Write to the specified I/O ports.
UPDATE_IO	Update the specified I/O ports.
UPLOAD_MEMORY	Return the values in specified memory area.
DOWNLOAD_MEMORY	Write values to specified memory area.
OR_I/O	OR values into specified I/O ports.
AND_I/O	AND values into specified I/O ports.
XOR_I/O	XOR values into specified I/O ports.
READ_INTERNAL	Read values at specified internal RAM areas.
WRITE_INTERNAL	Write values to specified internal RAM areas.
NODE_INFO	Return device related information.
OFFLINE	Set node offline.
UPLOAD_CODE	Read values from code memory space.
DOWNLOAD_CODE	Write values to specified EEPROM memory.

NOTES:
Internal memory locations are included in the 192 bytes of data RAM provided in the microcontroller. External memory refers memory outside the microcontroller—the 28-pin sockets of iRCB 44/20A board. Each RAC Access Function may refer to 1, 2, 3, 4, 5 or 6 individual I/O or memory locations in a single command.

INDUSTRIAL PACKAGING

The iRCB 44/20A board conforms to a single-wide (3V), 220 mm deep Eurocard form-factor. This allows the iRCB 44/20A to fit within standard industrial racks or chassis as well as Intel's RCX 920 Analog Signal Conditioning, Isolation & Termination Panel (see below). The Eurocard specification references DIN 41612 connectors, which are used on the iRCB 44/20A board.

ANALOG SIGNAL CONDITIONING, ISOLATION AND TERMINATION

The RCB 44/20A is fully compatible with the RCX 920 Analog Signal Conditioning, Isolation and Termination Panel. The RCX 920 panel provides integral mounting for one RCB 44/20A, with connectors for power, the BITBUS interconnect signals, and 18 Analog Devices 5B Series Signal Conditioning and Isolation Modules. These modules provide 240V RMS field wiring protection, and 1500V RMS common mode voltage isolation and support signal conditioning in a wide range of analog voltages and currents including thermocouple and RTD sensors, millivolt and volt inputs and 4–20 mA and 0–20 mA outputs.

SPECIFICATIONS

CPU

8044 BITBUS Enhanced Microcontroller (BEM)

Word Size

Instruction—8 bits
Data—8 bits

Processor Clock

12 MHz

Instruction Execution Times

1 μsec 60% instructions
2 μsec 40% instructions
4 μsec Multiply & Divide

Memory Addressing

iDCM Controller
Up to 64K bytes code

Address Ranges

	Option A	Option B
External Data Memory Site	0000H–7FFFH	0000H–7FFFH
External Code Memory Site	1000H–0FFFFH (0000H–0FFFFH if EA Active)	8000H–0FFEFH
Internal Code Memory	0000H–0FFFH	0000H–0FFFH

NOTES:
Option A: Supports maximum amount of external EPROM code memory
Option B: Supports downloading code into external RAM or EEPROM memory

BITBUS™ Development Environments

HOST SYSTEM	BITBUS™ TOOLS								NODE CODE			ICE™	EPROM PROG.	
	DCS 100 TOOLBOX													
	BBM	UBI	BIH	PC Bridge	OBJHEX	UDI2DOS	DCS 110	DCS 120	ASM 51	PL/M 51	RL 51, LIB 51	ICE 5100/044	iUP200A/201A with iUPF87/44A module and iPPS sw	iPDS with iUPF87/44A module and iPPS sw
Series II									C	C	C		X	
III			X				X	X	X	X	X	X	X	
IV							X	X	X	X	X	X	X	
iPDS™	A	A	A				X	X	C	C	C			X
iRMX® 5¼"	X	X	X	X	X		X	X	D	D	D			
8"	X	X	X	X	X		X	X	D	D	D			
XENIX 5¼"	X	X		B	X									
8"	X	X		B	X									
DOS	X	X	X	X	X	X	X	X	X	X	X	X	X	

NOTES:
A. iPDS™ uses Release 1 Toolbox.
B. Supports operation with XENIX. XENIX disks not required.
C. Down-revision version.
D. Available for iRMX® 86.

I/O Capability

Analog—16 single-ended or 8 differential channels and 2 outputs channels

Expansion—one single-or double-wide iSBX MULTIMODULE (MWAIT * or DMA not supported by iRCB 44/20)

Interrupt Sources

Two external: iSBX I/O Bus or BITBUS Interconnect sources

Bus Termination

Jumper selectable resistors provide termination capability for cable with an impedance of 120Ω or greater.

Analog Input Specifications

Number of channels—16 single-ended or 8 differential
Input ranges—0 to 5V, 0 to 10V (unipolar) ±5V, ±10V (bipolar)
Gain ranges—1, 10, 100, 500, (software programmable)
Input impedance—100MΩ
Input bias current—±50 nA
Overvoltage protection—±32V power on
±20V power off

Accuracy

Resolution—12 bits
Linearity and Noise—±¾ LSB (trimmable)
System Accuracy
Gain = 1—±0.035% full-scale range (trimmable)
Gain = 500—±0.15% full-scale range (trimmable)

Stability

Gain tempco—32 ppm/°C (gain = 11)
75 ppm/°C (gain = 500)
Offset tempco—100 microvolts/°C max.

Dynamic Performance

Aggregate throughout—20 KHz (gain = 1, 10)
7.5 KHz (gain = 100, 500)
Common mode rejection—70 dB (gain = 1)
100 dB (gain = 500)
A/D conversion time—30 microseconds

Analog Output Specifications

Number of channels—2
Output ranges—0 to 5V, 0 to 10V (unipolar) ±5V, ±10V (bipolar)
Current-loop range—4 to 20 mA (unipolar mode only)
Output impedance—0.2Ω min. (voltage)
5 MΩ max. (current)
Output current—±5 mA (short-circuit protected)

Accuracy

Resolution—12 bits
Linearity and Noise—±¾ SB (trimmable)
System Accuracy—
Gain = 1—−0.35% full-scale range (trimmable)
Gain = 500—±0.15% full-scale range (trimmable)

Stability

Full-scale temperature coefficient
150 microvolts/°C (unipolar)
300 microvolts/°C (bipolar)
0.6 microamps/°C (current-loop)
Offset temperature coefficient
30 microvolts/°C (unipolar)
180 microvolts/°C (bipolar)
0.3 microamps/°C (current-loop)

Mating Connectors

Function	# of Pins	Type	Vendor	Part Number
BITBUS Connector	64	Flat Cable	GW Elco Robinson Nugent	00-8259-096-84-124 RNE-IDC-64C-TG30
iSBX Connector	36	Wire Wrap	ITT Cannon GW Elco	G06 M96 P3 BDBL-004 60 8257 3017
		Solder	Viking	000292-0001

Dynamic Performance

Aggregate throughput—20 KHz (gain = 1, 10)
7.5 KHz (gain = 100, 500)
Settling Time—15 microseconds to ±½ LSB

Electrical Characteristics

Interface Compliance

iSBX BUS (through level D8/8F):
Memory sites—code and data sites are JEDEC compatible

BITBUS:

— Synchronous and self-clocked mode support for 500 Kbps to 2.4 Mbps, 375K and 62.5K bits/sec

NOTE:
On-board ALE clock supports 1 Mbps synchronous operation. All other synchronous mode speeds require user-supplied 2.0–9.6 MHz crystal.

— Equivalent to 1.1 standard (RS 485) loads

— Message length up to 54 bytes maximum

Power Requirement (exclusive of optional memory or iSBX MULTIMODULE)

Voltage	Current (amps)	Max, Power (watts)
+5V ±5% +12V ±5% −12V ±5%	0.9 max. 0.7 typ 100 mA max. 100 mA max.	4.5

NOTE:
+15V and −15V required for 0 to 10V and ±10V ranges; for ±15V operation, the iRCB 44/20A cannot be used with iSBX MULTIMODULES that use ±12V power sources.

Physical Characteristics

Width: 3.77 mm (0.542 in) maximum component height
Height: 100 mm (3.93 in)
Depth: 220 mm (8.65 in)
Weight: 169 gm (6 ounces)

Environmental Characteristics

Operating Temperature: 0°C to +60°C at 0.8 CFM air volume
Relative Humidity: 90% non-condensing

Reference Manual (Not Supplied)

148816— iRCB 44/20A Hardware Reference Manual

ORDERING INFORMATION

Part Number	Description
iRCB 44/20A	BITBUS Analog I/O Controller Board

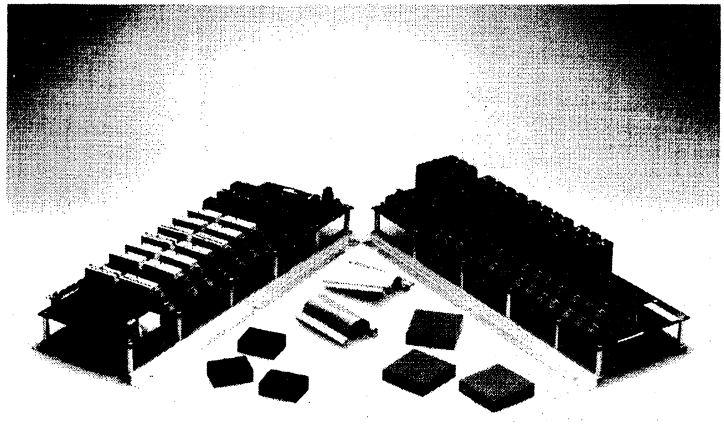
iRCX 910/920 DIGITAL/ANALOG SIGNAL CONDITIONING ISOLATION AND TERMINATION PANELS

iRCX-910

- Digital termination for BITBUS™ iRCB 44/10A digital remote controller board, iSBX™ 350 digital MULTIMODULE™ and Multibus® digital I/O single board computers (SBCs)
- Sockets for 24 industry-standard, optically coupled isolation and signal conditioning I/O modules
- LEDs indicate status of each module
- Separate connectors for BITBUS, Power, RCB and Expansion I/O
- Integral mounting site for one 24 channel digital iRCB 44/10A

iRCX 920

- Analog termination for iRCB 44/20A, iSBX 311, iSBX 328, and iSBC 88/40
- Sockets accepting up to 18 Analog Devices Corporation's 5B Series of isolation and signal conditioning modules
- Separate connectors for BITBUS, Power, RCB and Expansion I/O
- Integral mounting site for one 18-channel analog iRCB 44/20A



AUGUST 1988
ORDER NUMBER: 280443-001

More Convenient BITBUS™ System Integration

Intel now provides one more building block for developing BITBUS™ networks: the iRCX 910/920 Digital/Analog Signal Isolation and Termination Panels. These boards provide remote node termination and isolation in a design that's easy to install and service. They work with Intel's RCB 44/10A and 44/20A, which provide analog/digital control, and with Intel's BITBUS Monitor, DCX-51 Real-time Multitasking Executive and BITBUS Toolbox, which provide the software support.

Intel makes BITBUS system integration easier and more convenient than ever.

Compatible With a Wide Range of Intel MULTIBUS® Boards

The iRCX 910 and iRCX 920 not only work with the iRCB 44/10A and 44/20A controller boards but also with a wide range of MULTIBUS® boards both from Intel and MULTIBUS Manufacturing Group vendors. The 50-pin expansion connection on the iRCX panels makes iSBC and iSBX board connection easy.

Table 1 shows the Intel iSBC and iSBX boards currently compatible with the iRCX products.

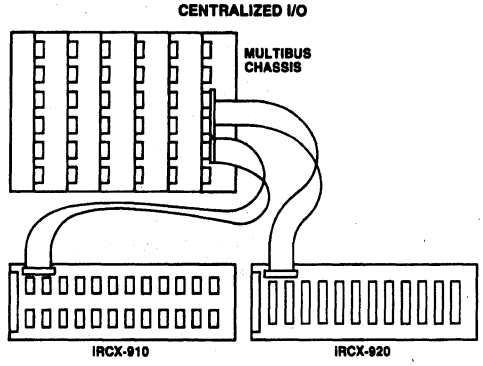
iRCX 910: Compatible With Industry-Standard I/O Modules

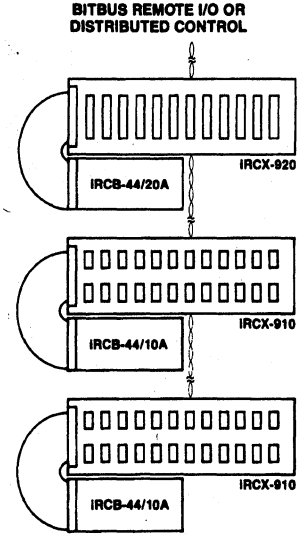
The iRCX 910 provides sockets for 24 channels of user-provided digital I/O to perform AC or DC switching and isolation. The user can configure up to 24 I/O channels, filling only the channels needed for the application. The iRCX 910 accepts a wide range of industry-standard I/O modules, including those from Gordos, Opto 22, Crydom, Potter-Brumfield and others[1]. The input modules convert high-level inputs from such sources as limit or proximity switches to TTL levels. The output modules convert TTL to high-level signals for driving motor starters, solenoids, indicating lights, and the like. Regardless of whether input or output, these modules typically provide greater than 1500 volt isolation, 2-3 KV of transient noise protection, and signal conditioning in a wide range of voltages. An LED for each channel shows on/off status, and a 5 amp fuse provides overcurrent protection.

[1]Mention of these companies in no way constitutes an endorsement by Intel of their products.

Table 1: Intel Boards Compatible with iRCX 910 and iRCX 920.

iRCX 910		iRCX 920	
Intel iSBCs	iSBX	Intel iSBC	Intel iSBX
80/10B 80/20-4 80/24A 80/30 80/05A 86/14 86/30 86/35 88/25 88/40A 517 519	350	88/40A	311 328





Examples of how iRCX 910 and 920s can be used in MULTIBUS and BITBUS systems.

iRCX 920: Uses Analog Devices Corporation Modules to Provide State-of-the-Art Signal Conditioning and Isolation

The iRCX 920 terminates 18 analog signals going to and from field wiring and provides signal conditioning and isolation using Analog Devices Corporation's 5B Series of analog isolation and signal conditioning modules (purchased separately). These modules provide 240 volt RMS field wiring protection, 1500 volt RMS common mode voltage isolation and signal conditioning in a wide range of analog voltage and currents, including thermocouple and RTD sensors, millivolt and volt inputs, and 0-20 ma and 4-20 ma process current outputs. Possible connections include temperature and pressure sensors, frequency counters and many others. The iRCB 44/20A when used in conjunction with the iRCX 920 provides up to 16 analog inputs and 2 analog outputs.

The iRCX 920 also contains an integral temperature sensor isothermal barrier strip (RTD) to provide a temperature reference for thermocouple modules doing cold junction compensation. Because this compensation is implemented in hardware rather than software, it simplifies the controller software's task, allowing superior software performance.

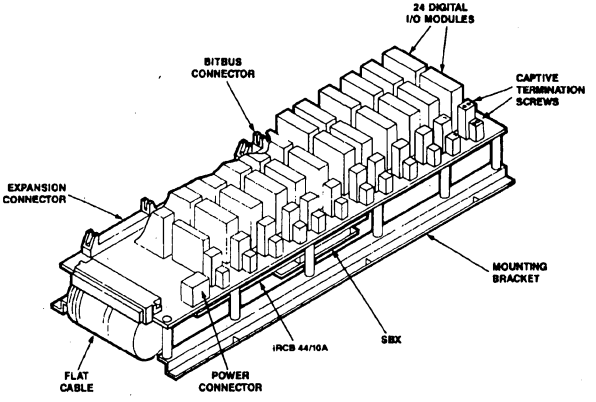
Easy to Install, Easy to Use

The iRCX panels provide a quick and easy, plug-in solution to remote node BITBUS interconnection. They can be mounted to an industrial panel or in a standard RETMA 19" rack when used with a customer provided 19"L × 7"W pan. Quick access to the RCB 44/10A and 44/20A boards is accomplished by loosening six screws and shifting the iRCX slightly. Field wiring connections are made using captive screw terminals, positioned to allow easy wire routing. Installation is quick, service is easy.

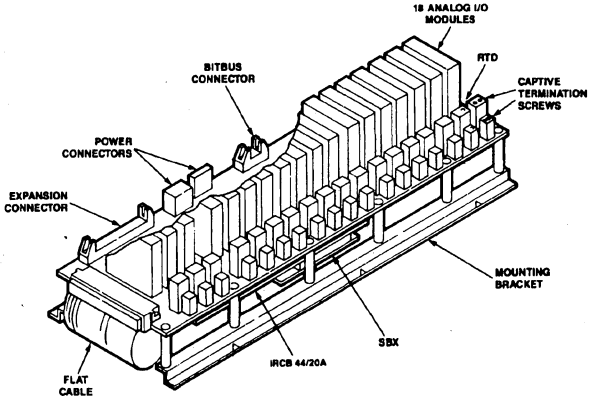
The I/O modules on the iRCX 910 are color-coded for easy identification. LEDs provide on/off status, allowing the operator a quick verification of I/O operation, and are also useful for start-up testing, debugging and trouble-shooting a process or machine breakdown.

Increased Reliability

The iRCX 910 and 920 feature improved noise immunity through judicious component placement and the inclusion of a ground terminal. Also, they're mounted in front of the iRCB 44/10A and 44/20A boards, protecting the heart of the remote node from accidental damage.



iRCX 910: The Complete Remote Node Solution for Distributed I/O and Control.



iRCX 920: The Complete Remote Node Solution for Distributed I/O and Control.

Specifications

POWER REQUIREMENTS (TYPICAL)

RCX 910

V_{cc} = +5 VDC ±5%
I_{cc} = 0.03 a/module installed
+1.00 a (if RCB 44/10A installed)
+ current requirements of any installed SBX

RCX 920

V_{cc} = + 5 VDC ±5%
I_{cc} = 0.03 a/input module
+0.17 a/output module
+1.00 a (if RCB 44/20A is installed)
+ current requirements of any installed SBX

Additional Power Requirements when used with RCB 44/20A
100 ma @ +12 VDC ±4%
100 ma @ −12 VDC ±4%

DIMENSIONS

RCX 910
Width: 17.00" (43.18 cm)
Height: 6.20" (15.75 cm)
Depth: 3.25" (8.26 cm) with user-provided modules installed

RCX 920
Width: 17.00" (43.18 cm)
Height: 6.20" (15.75 cm)
Depth: 4.25" (10.80 cm) with user-provided modules installed

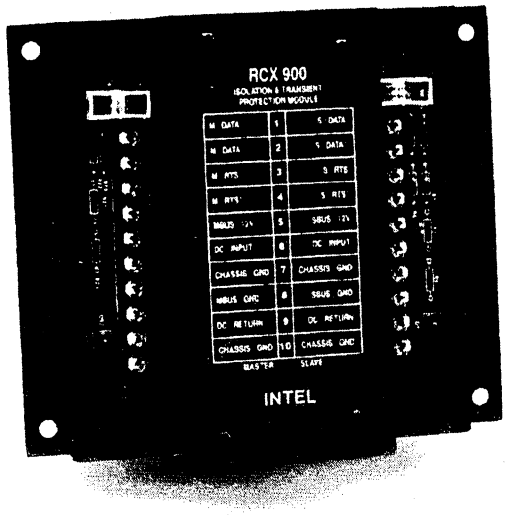
ENVIRONMENTAL REQUIREMENTS

RCX 910/RCX 920 Standalone
Operating Temperature: 0° to 70° C (32° to 158° F)
Operating Humidity: 0–90% R.H. (non-condensing)

RCX 910/RCX 920 with mounted RCB
In still air:
0° to 55° C (32° to 131° F)
With 200 linear feet/minute forced air:
0° to 60° C (32° to 140° F)

Ordering Information

Part Name	Description
iRCX 910	BITBUS Digital Signal Conditioning, Isolation, and Termination Panel
iRCX 920	BITBUS Analog Signal Conditioning, Isolation, and Termination Panel
Analog I/O Modules	Analog Devices 5B Series To order contact: Analog Devices Corporation One Technology Way Norwood, MA 02062 (617) 329-4700



ISOLATION AND TRANSIENT PROTECTION FOR BITBUS™ NETWORKS

The Intel iRCX 900 Isolation Module protects against ground loops, voltage differences between nodes, and transient voltage spikes in BITBUS™ networks operating in the 62.5 to 375 Kbps asynchronous (self-clocked) modes. The iRCX 900 also serves as an isolated, standalone repeater, driving up to 28 remote BITBUS nodes.

FEATURES:

- Common-mode isolation of 1500 VAC for a working voltage of 480 VAC.
- Transient protection meeting the IEEE 472/ ANSI-C37.90a-1974 Surge Withstand Compatibility Test.
- On-board DC-DC switching voltage regulator with 1500 VAC isolation.
- Power-on indicator LEDs.
- Rugged industrial packaging with multiple mounting options.
- Dual termination with 10-pin BITBUS connector and 10-position terminal block.

FEATURES

STANDALONE ISOLATION AND TRANSIENT PROTECTION

The iRCX 900 provides BITBUS network protection against voltage surges and transients in industrial environments. This protection is provided through the use of optocouplers, transient suppressors, and an isolated DC-DC voltage regulator.

DOUBLES AS A NETWORK REPEATER

The iRCX 900 also serves as a network repeater, with each iRCX 900 module capable of driving up to 28 remote BITBUS nodes. The iRCX 900 can be powered either from the 12V BITBUS signal line or a separate 12-24V power source.

EASY TO INSTALL AND UPDATE

Installation and change of configuration are easy, because the iRCX 900 is a standalone module. It can be placed anywhere in the network without piggybacking it to another board. The iRCX 900 can be panel-mounted or placed on a desk or lab benchtop. Wiring instructions are clearly outlined on the module packaging.

SERVICE, SUPPORT AND TRAINING

Intel provides worldwide support for board repair or on-site service.

INTEL QUALITY AND RELIABILITY

The iRCX 900 is designed and manufactured in accordance with Intel's high quality standards. We then verify quality through rigorous testing in our state-of-the-art Environmental Test Laboratory.

SPECIFICATIONS

POWER REQUIREMENTS

Input Voltage: 10.8–26.4 VDC
Input Power: 2.0 watts (typical)

May be powered from a remote BITBUS node or from a user-provided power supply.

DIMENSIONS:

Width:	6.48 in. (16.46 cm)
Height:	5.7 in. (14.48 cm)
Depth:	1.78 in. (4.52 cm)

ENVIRONMENTAL REQUIREMENTS

Storage Temperature:	–40° to 70°C (–40° to 158°F)
Operating Temperature:	0° to 55°C (32° to 131°F)
Storage Humidity:	5%–95% non-condensing at 55°C
Operating Humidity:	8%–90% non-condensing at 55°C

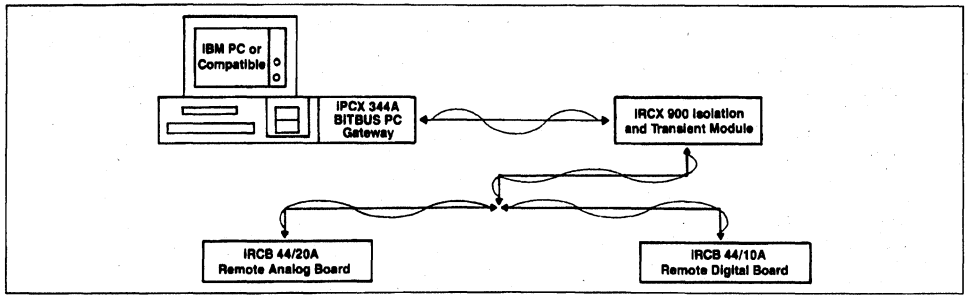
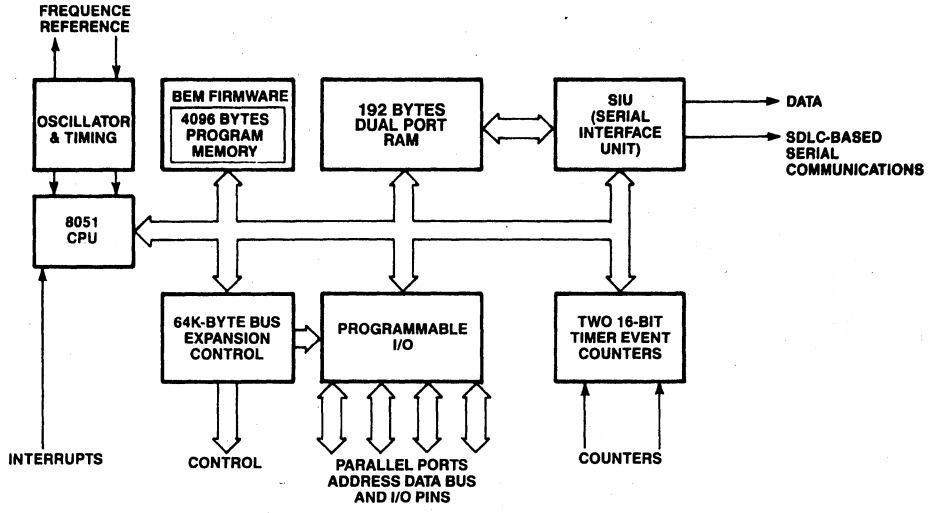


Figure 1: Example Configuration

8044 BITBUS™ ENHANCED MICROCONTROLLER

- **Dual Processor Microcontroller Architecture**
- **High Performance 8-Bit CPU**
- **Embedded Parallel Communications Firmware**
- **Tuned for Distributed Real-Time Control**
- **BITBUS™ Firmware Included On-Chip**
- **Power-Up Diagnostics**
- **DCX 51 Distributed Control Executive Included On-Chip**
- **MCS®-51 Software Compatible**

The 8044 BITBUS Enhanced Microcontroller (BEM) is a powerful 8-bit microcontroller with on-chip firmware. The dual processor architecture of the 8044 combined with the inherent the processing power of an 8051 CPU is well suited for distributed data acquisition and control applications in both the factory and laboratory. The firmware integral includes facilities for: diagnostics, task management, message passing, and user-transparent parallel and serial communication services.



280129-1

Figure 1. BEM Block Diagram

*IBM is a trademark of International Business Machines Corporation.

October 1987
Order Number: 280129-003

OPERATING ENVIRONMENT

Introduction

The BITBUS Interconnect Serial Control Bus Specification defines an integrated architecture optimized for implementing real-time distributed control systems. The architecture includes a message structure and protocol for multitasking environments, and a predefined interface for I/O access and control. As with traditional bus specifications the mechanical, electrical, and data protocols have been defined. Over a twisted pair of wires the bus can support up to 250 nodes at three different bit rates dependent on application performance requirements. Figure 2 illustrates the BITBUS Interconnect architecture.

The 8044 BITBUS Enhanced Microcontroller (BEM) or DCM Controller provides the user with the smallest BITBUS building block—a BITBUS component solution. With its dual processor architecture, this unique single chip provides both communication and computational engines (Figure 3). Real-time control and computational power are provided by the on-chip 8-bit 8051 CPU. The Serial Interface Unit (SIU) executes a majority of the communications functions in hardware resulting in a high performance solution for distributed control applications where communication and processing power are equally important. The BEM's firmware implements the BITBUS message structure and protocol, and the pre-defined I/O command set.

Firmware

The 8044 microcontroller requires specific hardware to interface to BITBUS. The BEM's firmware also requires a particular hardware environment in order to execute correctly, just as the iDCX 86 Operating System or other operating systems required a specific hardware environment, i.e., interrupt controller, timers, etc. Based upon the hardware provided, Basic or Extended firmware environments result.

The Basic firmware environment supports the minimum configuration for the BEM to execute as a

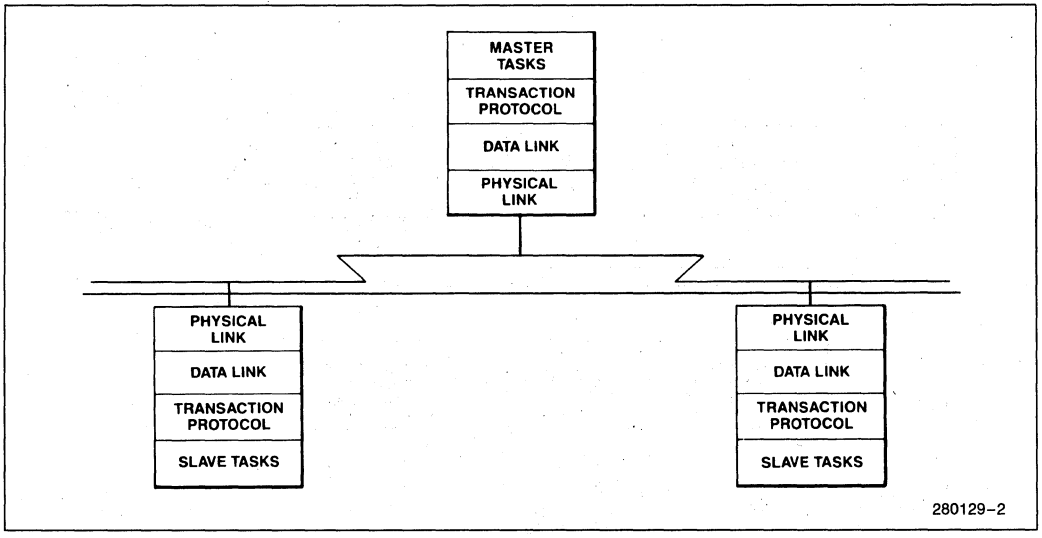


Figure 2. BITBUS™ Architecture

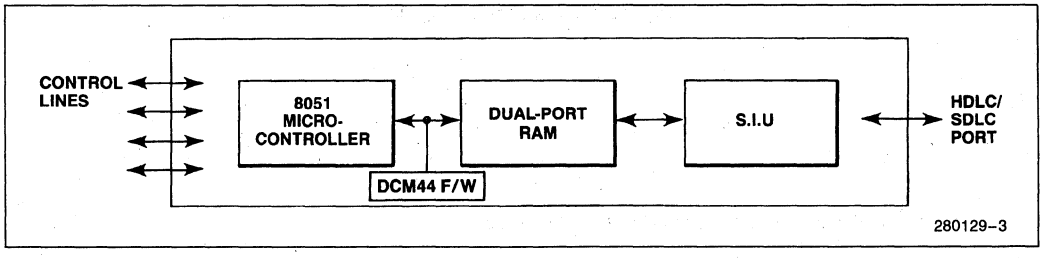


Figure 3. 8044's Dual Processor Architecture

BITBUS device. The Extended firmware environment requires hardware incremental to the Basic environment and allows the user to take full advantage of all the features included in the BEM's firmware. The designer may implement the Basic or Extended firmware environment as desired as long as the programmatic requirements of the firmware are met (see below).

Figure 4 shows one example of an Extended firmware environment. This particular example represents the BITBUS Core as used on Intel's iSBX™ 344A BITBUS Controller MULTIMODULE™ Board and iRCB 44/10A BITBUS Remote Controller Board.

BASIC FIRMWARE ENVIRONMENT	
Memory Bus	Parallel ports of 8044
BITBUS Node Address	0FFFFH external data space
Configuration	0FFFEH external data space
System RAM	0–02FFH external data space
Diagnostic LED #1	Port 1.0 (Pin 1)
Diagnostic LED #2	Port 1.1 (Pin 2)
EXTENDED FIRMWARE ENVIRONMENT	
Memory Bus	Parallel ports of 8044
BITBUS Node Address	0FFFFH external data space

EXTENDED FIRMWARE ENVIRONMENT (Continued)	
Configuration	0FFFEH external data space
System RAM	0–02FFH external data space
Diagnostic LED #1	Port 1.0 (Pin 1)
Diagnostic LED #2	Port 1.1 (Pin 2)
User Task Interface	First Task Descriptor—0FFF0H to 0FFFFH in External data space Other Task Descriptors and User Code—01000H to 0FFEFH in external code space
User RAM Availability	On-Chip—02AH to 02FH bit space Off-Chip—BITBUS Master: 0400H to 0FFEFH external data space BITBUS Slave: 0100H to 0FFEFH external data space
Remote Access and Control Interface	Memory-Mapped I/O—0FF00H to 0FFFFH external data space

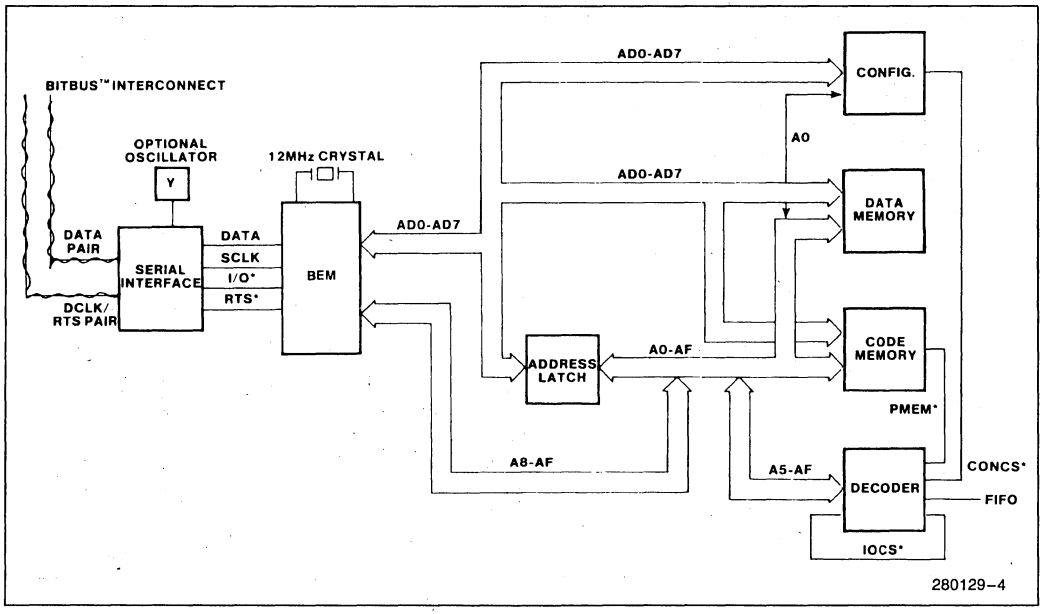


Figure 4. Extended Firmware Environment Example

EXTENDED FIRMWARE ENVIRONMENT (Continued)	
Parallel Interface to Extension Device	FIFO Command Byte—0FF01H external data space FIFO Data Byte—0FF00H external data space Receive Data Intr—INT0 (pin 12) Transmit Data Intr—INT1 (pin 13) Command/Data Bit—P1.2

FUNCTIONAL DESCRIPTION

High Performance 8044 Microcontroller

The 8044 combines the powerful 8051 microcontroller with an intelligent serial communications controller to provide a single-chip solution that efficiently implements distributed processing or distributed control systems. The microcontroller is a self-sufficient unit containing ROM, RAM, ALU, and peripherals. The 8044's architecture and instruction set are identical to the 8051's. The serial interface of the 8051 is replaced with an intelligent communications processor, the Serial Interface Init (SIU), on the 8044. This unique dual processor architecture results in high performance and reliability for distributed control and processing environments. The intelligent SIU offloads the CPU from communication tasks, thus dedicating more of its compute power to external processes.

Major features of the 8051 microcontroller are:

- 8-bit CPU
- On-chip oscillator
- 4K bytes of RAM
- 192 bytes of ROM
- 32 I/O lines
- 64K address space external data memory
- 64K address space external program memory
- Two Programmable 16-bit counters
- Five source interrupt structure with two priority levels
- Bit addressability for Boolean functions
- 1 μs instruction cycle time for 60% instructions
  2 μs instruction cycle time for 40% instructions
- 4 μs cycle time for 8 by 8 unsigned multiple and divide

As noted in the Operating Environment discussion, the BITBUS firmware requires various CPU resources, i.e., memory, timers, and I/O dependent upon the firmware environment selected.

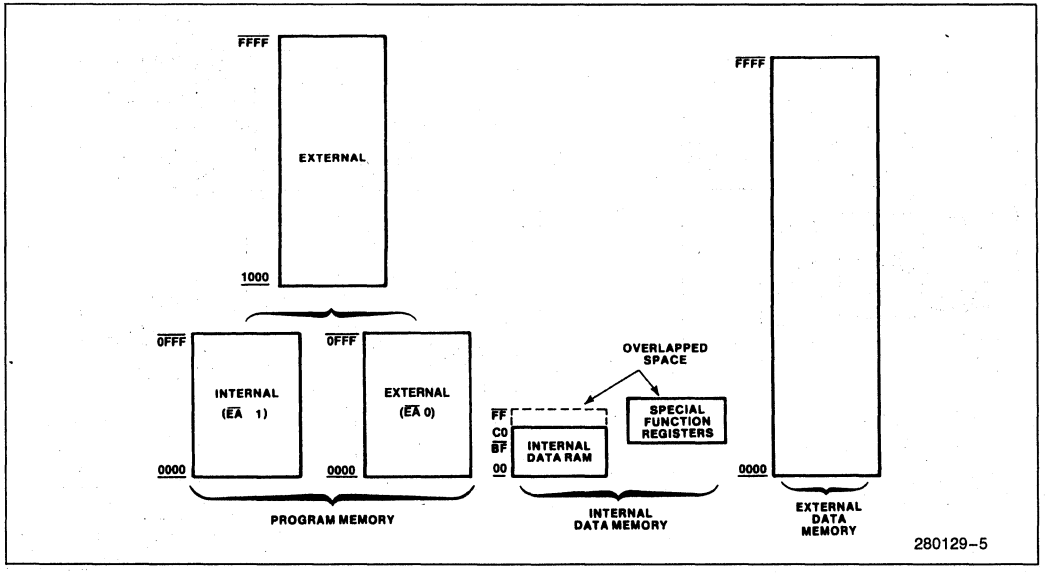


Figure 5. BEM Memory Map

Memory Architecture

The 8044 microcontroller maintains separate data and code memory spaces. Internal data memory and program memory reside on the controller. External memory resides outside the controller. The BEM firmware uses the available internal code memory space and most of the remaining internal data memory with the exception of bit space 02AH to 02FH. Figure 5 shows the BEM's memory map.

I/O ADDRESSING REQUIREMENTS

The table below provides the BEM's I/O port addresses.

Table 1. BEM I/O Addressing

Function	Address	Bit	Byte
Red LED P1.0	90H	X	
Green LED P1.1	91H	X	
TCMD	92H	X	
RFNF#	B3H	X	
TFNF#	B2H	X	
RDY/NE*	B4H	X	
Node Address	FFFFH		X
Configuration	FFFEH		X
Reserved	FFE0H–FFFDH		X
Digital I/O	FFC0H–FFDFH		X
SBX #4	FFB0H–FFBFH		X
SBX #3	FFB0H–FFAFH		X
SBX #2	FF90H–FF9FH		X
SBX #1	FF80H–FF8FH		X
User Defined	FF40H–FF7FH		X
Reserved	FF02H–FF3FH		X
FIFO Command	FF01H		X
FIFO Data	FF00H		X

SIGNAL FUNCTIONS

The 8044 BEM's pin configuration and pin description follow.

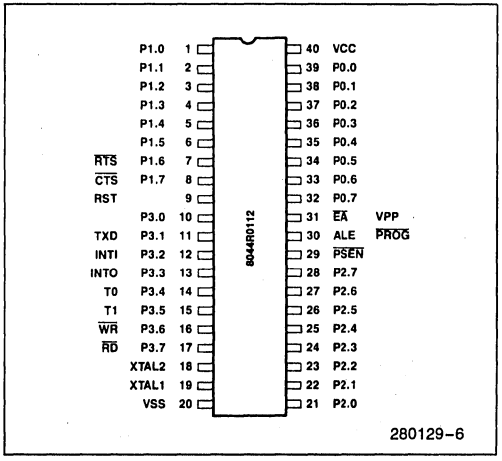


Figure 6A. BEM DIP Pin Configuration

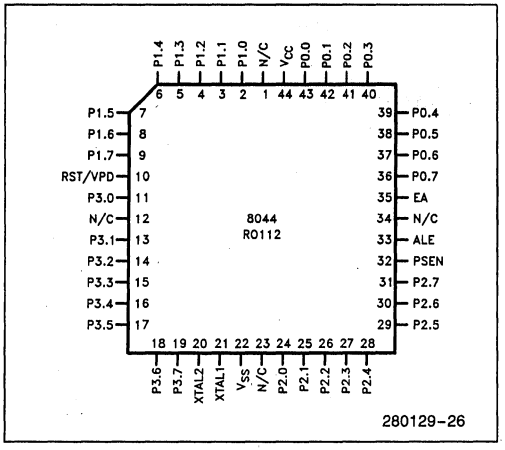


Figure 6B. BEM PLCC Pin Configuration

Table 2. BEM Pin Description

Name	Description
VSS	Circuit ground potential.
V_{CC}	+5V power supply during operation and program verification.
PORT 0	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
PORT 1	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. In non-loop mode two of the I/O lines serve alternate functions: —$\overline{RTS}$ (P1.6) Request-to Send output. A low indicates that the 8044 is ready to transmit. —$\overline{CTS}$ (P1.7) Clear-to-Send input. A low indicates that a receiving station is ready to receive.

Table 2. BEM Pin Description (Continued)

Name	Description
PORT 2	Port 2 is an 8-bit quasi-bidirection I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
PORT 3	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. In addition to I/O some of the pins also serve alternate functions as follows: • I/$\overline{O}$ R x D (P3.0). In point-to-point or multipoint configurations, this pin controls the direction of pin P3.1. Serves as Receive Data input in loop and diagnostic modes. • DATA T x D (P3.1). In point-to-point or multipoint configurations, this pin functions as data input/output. In loop mode, it serves as transmit pin. A '0' written to this pin enables diagnostic mode. • $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. • $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. • TO (P3.4). Input to counter 0. • SCLK T1 (P3.5). In addition to I/O, this pin provides input to counter 1 or serves as SCLK (serial clock) input. • $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. • $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
RST	A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx$ 8.2 KΩ) from RST to VSS permits power-on reset when a capacitor ($\approx$ 10 μf) is also connected from this pin to V_{CC}.
ALE/$\overline{PROG}$	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. It also receives the program pulse input for programming the EPROM version.
$\overline{PSEN}$	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
$\overline{EA}$/VPP	When held at a TTL high level, the 8044 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the 8044 fetches all instructions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage on the 8744.
XTAL 1	Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2.
XTAL 2	Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

Firmware

The BEM's Basic firmware environment provides two services: BITBUS Communications and Power-Up Diagnostics. The Extended firmware environment provides the Basic firmware services plus Parallel Communications and User Software Services (iDCX 51 Executive, Remote Access and Control functions). A discussion of each service follows.

Basic Firmware Services

POWER-UP DIAGNOSTICS INCREASE RELIABILITY

For added reliability and simplified system start up, the BEM firmware includes power-up diagnostics. At chip reset the BEM diagnostic firmware checks the integrity of the 8044's instruction set, ROM, internal

RAM, and external RAM. LED indicator lights may be used to show the progress of the diagnostics. Intel's BITBUS boards use one red LED, and one green LED as indicators for test progress. Since the test halts if a fault is found, the last LED state indicates the trouble area.

No programmatic interface exists for the power-up diagnostics. Only LEDs (or other indicators) connected to the outputs of Port 1 of the 8044 are required. For the test sequence shown in Table 3, the red LED is connected to pin P1.0, and the green LED is connected to pin P1.1.

Table 3. Power-Up Test Sequence

Test Sequence	State of Port* After Test Completion	
	Red LED (Pin 1.0)	Green LED (Pin 1.1)
Power-on	On	On
Prior to Start of Tests	Off	Off
Test 1—Instruction Set	On	On
Test 2—ROM Checksum Test	On	Off
Test 3—Internal RAM	Off	Off
Test 4—External RAM	Off	On

*Ports are Active Low.

BITBUS™ INTERFACE SIMPLIFIES DESIGN OF DISTRIBUTED CONTROL SYSTEMS

The BITBUS Serial Control Bus is a serial bus optimized for high speed transfer of short messages in a hierarchical system. From the perspective of systems using the BITBUS bus there are three external protocols that must be adhered to: physical, data link, and transaction control as shown in Figure 2. The physical interface includes all bus hardware requirements, e.g. cable and connector definition, transceiver specification. The data link interface refers to the device to device transfer of frames on the bus. The transaction control interface indentifies the rules for transmitting messages on the bus as well as the format of the messages passed.

For maximum reliability and to facilitate standardization the following existing standards were chosen as portions of the BITBUS Specification: International Electrotechnical Commission (IEC) mechanical board and connector specifications, the Electronic Industry Association (EIA) RS-485 Electrical Specification and IBM*'s Serial Data Link Control protocol for the physical and data link levels of the BITBUS interface.

BITBUS™ Physical Interface

Implementation of the electrical interface to BITBUS requires external hardware. Specifically, an EIA Standard RS-485 driver and transceiver and an optional clock source for the synchronous mode of operation. A self clocked mode of operation is also available. Different modes of operation facilitate a variety of performance/distance options as noted in Table 4. Figure 7 illustrates the BEM's BITBUS interface hardware requirements.

Table 4. BITBUS™ Interconnect Modes of Operation

	Speed Kb/s	Max. Dist Between Repeaters M/ft	Max # Nodes Between Repeaters	Max # Repeaters
Synchronous	2400	30/100	28	0
Self-Clocked	375 62.5	300/1000 1200/4000	28 28	2 10

BITBUS™ Data Link Service

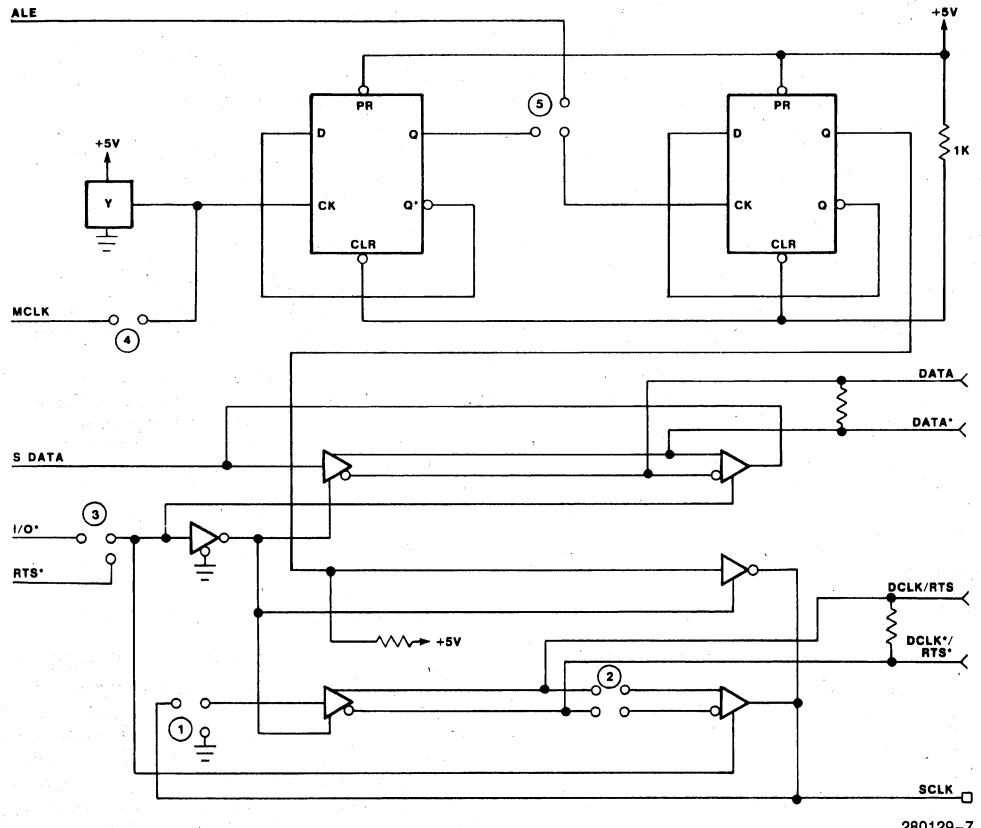
The 8044's serial interface unit (SIU) implements a majority of the data link interface, a subset of IBM's Serial Data Link Protocol (SDLC), in hardware resulting in a significant performance advantage compared with multichip solutions. Multichip solutions require both hardware and software glue that degrade performance, decrease reliability, and increase cost. This portion of the BITBUS interface requires no user involvement for execution.

For a detailed discussion of the protocol executed by the BITBUS data link service refer to "The BITBUS Interconnect Serial Control Bus Specification". A basic subset of SDLC with the REJECT option is implemented. The standard frame format transferred across the BITBUS is shown in Figure 8. The information field carries the BITBUS message.

BITBUS™ Transaction Control Service

For added reliability, the BITBUS interface incorporates error checking at the message level in addition to the imbedded error checking provided by SDLC at the data link level. The message control interface defines the format and function of messages transmitted in frames across the BITBUS bus. (Figure 9)

The transaction protocol requires that for every order message transmitted across the bus a reply message must be transmitted in return. Error types and error detection mechanisms are also designated by this interface.



NOTES:
1. Connect to ground for self-clocked mode and SCLK for synchronous mode.
2. Remove for self-clocked operation with repeater(s).
3. Connect to RTS* for synchronous mode or I/O* for self-clocked mode.
4. Selects MCLK as serial clock source.
5. Selects ALE or oscillator as serial clock source.

Figure 7. BITBUS™ Interface Hardware Requirements

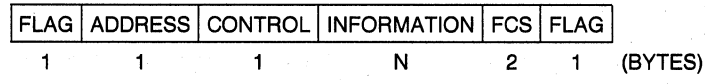


Figure 8. BITBUS™ Frame Format

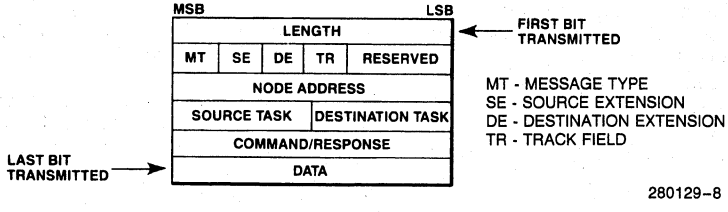


Figure 9. BITBUS™ Message Format

BITBUS™ Interface Configuration

The BEM's firmware also simplifies designation of the bus mode of operation (Speed/distance option) as well as the node address, memory configuration and parallel interface parameters by reading two external locations for this information as shown in Figure 10. The designer no longer needs to directly manipulate the 8044's serial mode register (SMD), status/command register (STS), and send/receive counter register (NSNR). These two 8-bit locations are derived by multiplexing the 8044's port 0 address lines AD0–AD7.

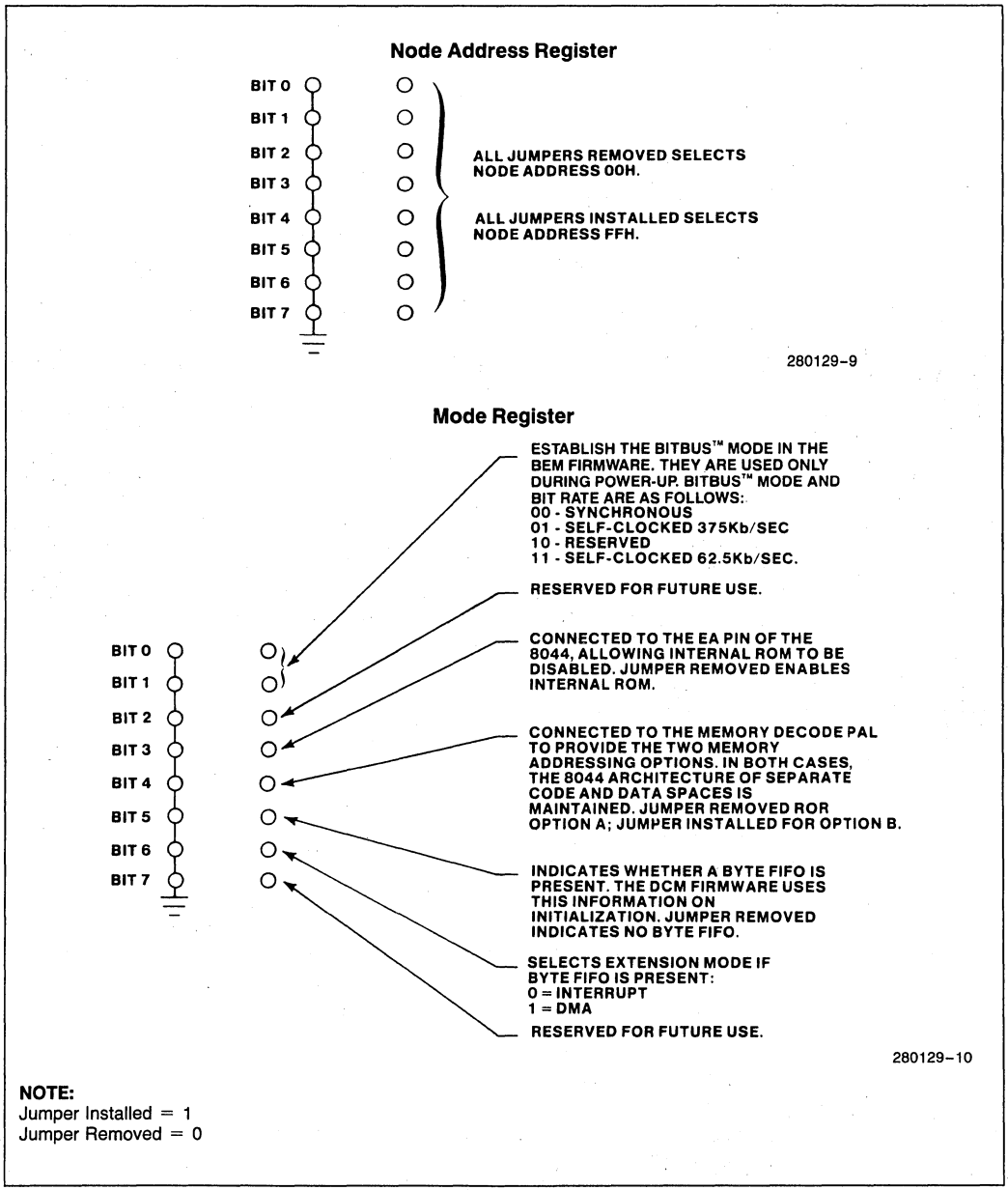


Figure 10. BITBUS™ Firmware Configuration

Extended Firmware Services

PARALLEL COMMUNICATION INTERFACE EXTENDS DISTRIBUTED CONTROL CAPABILITY

The BEM's firmware also includes a parallel interface for expanding the capabilities of distributed systems. For example, this interface allows other processors to be employed in BITBUS systems if more processing power is required as shown in Figure 11. This interface provides the means for connection to other buses: iSBX bus, STD bus, IBM's PC bus.

The interface consists of a byte-FIFO queue through which BITBUS messages can be passd via embedded communications firmware. From the BEM's perspective the user simply designates the correct routing information in the BITBUS message header and the message is directed to the communications firmware and passed through the parallel interface. One example of an implementation that uses this interface is the iSBX BITBUS Controller MULTIMODULE Board via the iSBX bus.

Parallel Interface Hardware

To implement the Parallel Interface, the user must provide hardware for two FIFOs (one byte minimum) in external data memory, and control signals to/from the 8044's Pins: INT0 (P3.2), INT1 (P3.3), and P1.2. Key hardware elements required are: decoder for the registers' external addresses, temporary storage for bytes passing through the interface, a way to designate bytes as command or data, and a means to generate the control signals. FIFO's must be used to move the data through the interface although the depth of the FIFO need not exceed one byte.

Interface hardware must also be provided for the "extension" side of the interface. Implementation of this hardware is left to the user with the restriction that the operation of the BEM side remains independent.

Parallel Byte Stream and Message Protocol

The two byte registers (FIFOs) provide the path for bytes to move through the parallel interface. Bytes are read or written from the registers designated: FIFO Data Byte (FF00H) and FIFO Command Byte (FF01H). INT0, INT1 and P1.2 provide control signals to the firmware for moving the bytes through the registers. These signals are referred to as the Parallel Interface Control Bits:

Pin	Function	Internal Bit Address
INT0	RFNF	B3H
INT1	TFNE	B2H
P1.2	TCMD	92H

The hardware uses RFNF to control the output of bytes from the BEM. RFNF is set when the FIFO Data or FIFO Command Byte Registers can receive information. RFNF remains clear when the FIFO Data or Command Bytes are not available. Transmission of a BITBUS message across the parallel interface consists of successively outputing message bytes to the FIFO Data Byte Register until all bytes are sent. The firmware then writes a value of 0 to the Command Byte register indicating all the message bytes have been sent. The first data byte in the message indicates the number of bytes in the message.

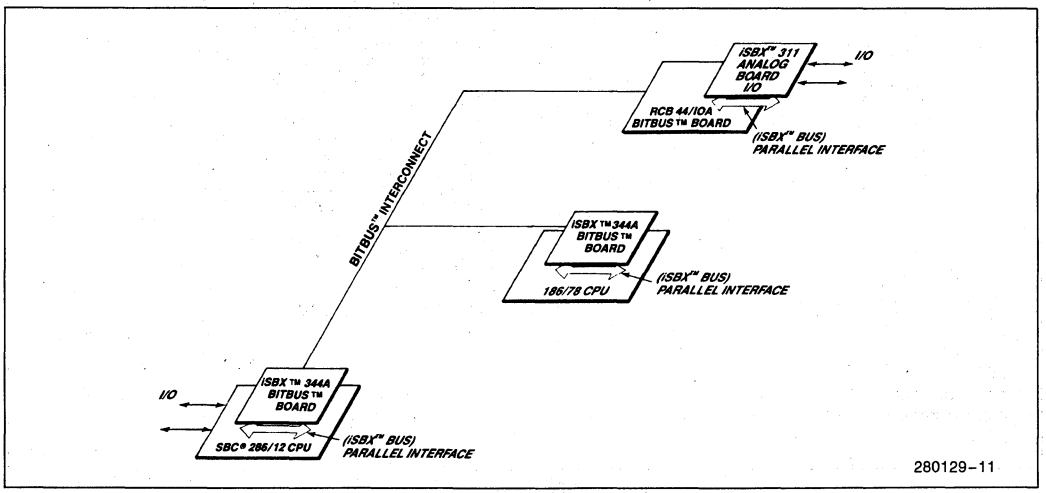


Figure 11. Extending the Capability of BITBUS™ System with the Parallel Communications Interface

TFNE controls the input of data bytes to the BEM. This bit is set when bytes are available for reading. When no bytes are available this bit is clear. TCMD indicates whether the next byte read is a Data Byte or Command Byte. BITBUS messages are received by inputing data bytes until a command byte is received. Data bytes are read from the FIFO Data Byte Register. Command Bytes are read from the FIFO Command Byte Register.

Figure 12 provides one example of a Byte FIFO Interface. This specific example illustrates the interface provided on the iSBX 344A BITBUS Controller MULTIMODULE Board. Figure 13 shows transmission of bytes from the BEM across the parallel interface. Figure 14 shows transmission of bytes to the BEM.

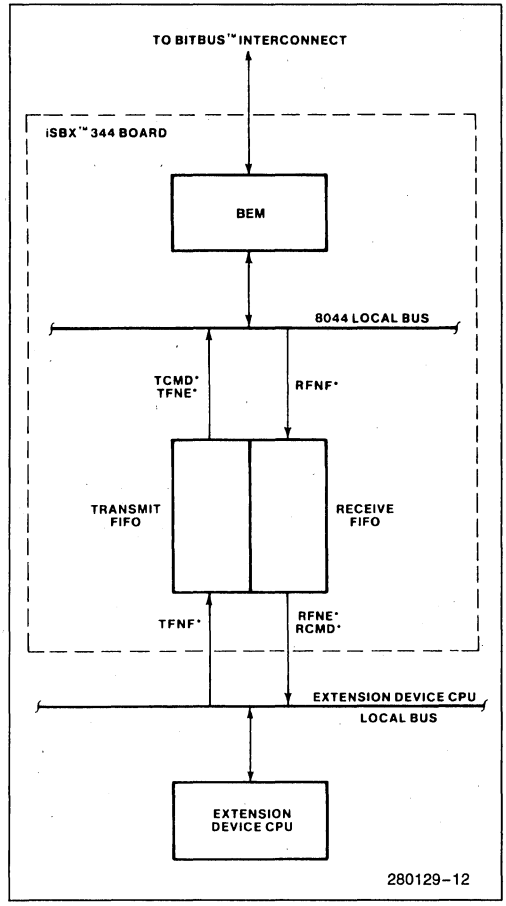


Figure 12. Byte FIFO Interface Example

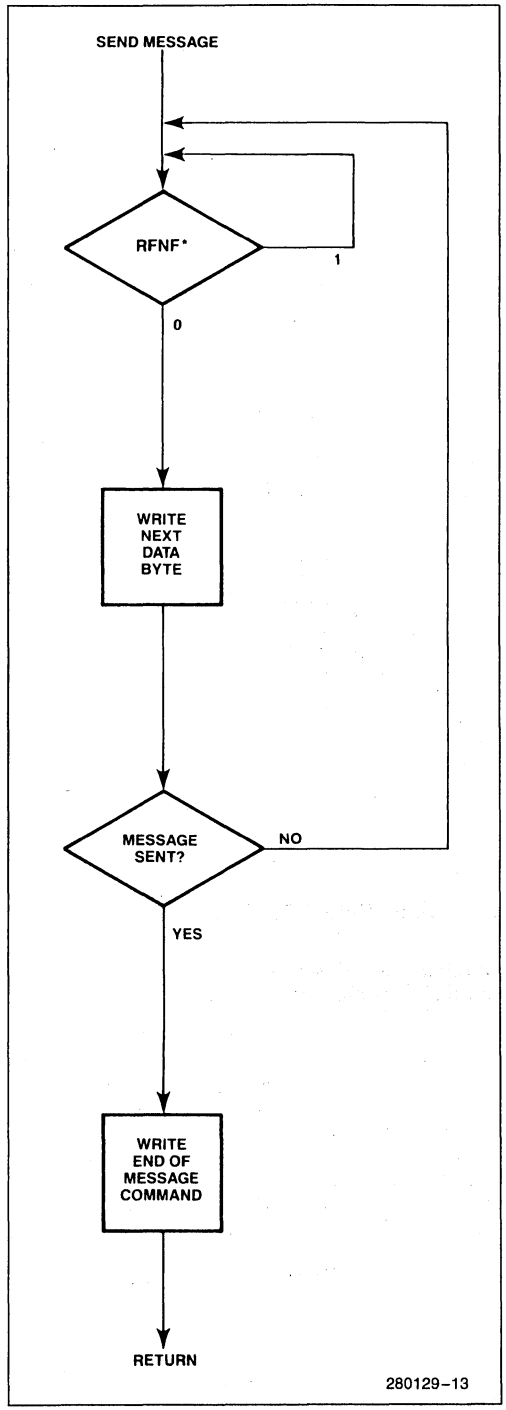


Figure 13. Transmitting a Message from BEM

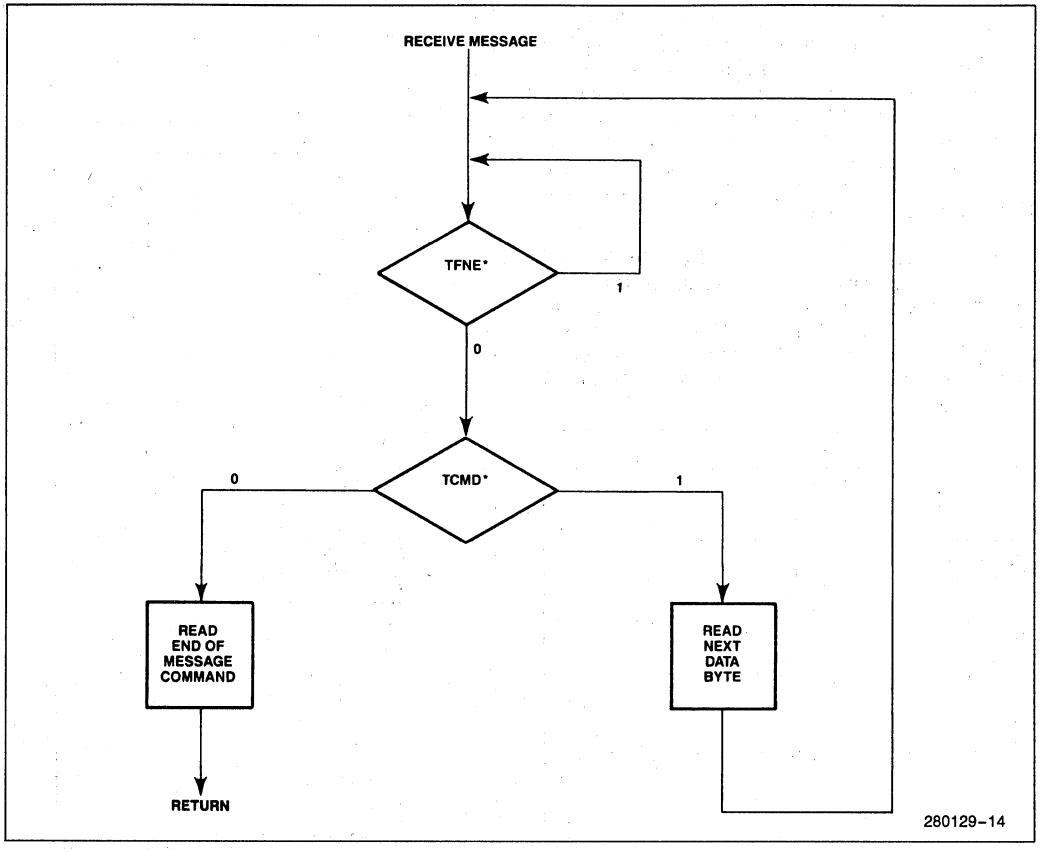


Figure 14. Transmitting a Message to BEM

USER SOFTWARE SERVICES

Multitasking, I/O Access and Control Capabilities

The Extended firmware environment of the BEM provides a multitasking facility via the iDCX 51 Real-time, Multitasking Executive. Operating system calls are listed in Table 5. Other services provided by the Executive: interrupt handling, task scheduling, and intertask communication facilitate smooth development of distributed systems. In addition to the Executive's intertask communication service provided by the RQSENDMESSAGE call, other portions of the firmware extend the communication capability across the parallel and BITBUS interfaces. This embedded communications firmware greatly simplifies and speeds sending messages to different microcontrollers or microprocessors in the system.

To further ease the development of distributed control applications, a pre-defined task (Remote Access and Control Task) provides the means of invoking iDCX 51 Executive services, or accessing I/O and memory from tasks on other devices. The Remote Access and Control functions execute under the iDCX 51 Executive as Task 0. Figure 13 illustrates this concept in a BITBUS system. Table 6 shows the functions provided by the RAC task. All I/O command accesses are memory mapped to locations 0FF00H to 0FFFFH in the BEM's external memory.

Table 5. iDCX™ 51 Calls

Call Name	Description
TASK MANAGEMENT CALLS	
RQ$CREATE$TASK	Create and schedule a new task.
RQ$DELETE$TASK	Delete specified task from system.
RQGETFUNCTION$IDS	Obtain the function IDs of tasks currently in system.
INTERTASK COMMUNICATION CALLS	
RQ$ALLOCATE	Obtain a message buffer from the system buffer pool.
RQ$DEALLOCATE	Return a message buffer to the system buffer pool.
RQ$SEND$MESSAGE	Send a message to specified task.
RQ$WAIT	Wait for a message event.
MEMORY MANAGEMENT CALLS	
RQGETMEM	Get available system memory pool memory.
RQ$RELEASE$MEM	Release system memory pool memory.
INTERRUPT MANAGEMENT CALLS	
RQ$DISABLE$INTERRUPT	Temporarily disable an interrupt.
RQ$ENABLE$INTERRUPT	Re-enable an interrupt.
RQ$WAIT	Wait for an interrupt event.
TIMER MANAGEMENT CALLS	
RQSETINTERVAL	Establish a time interval.
RQ$WAIT	Wait for an interval event.

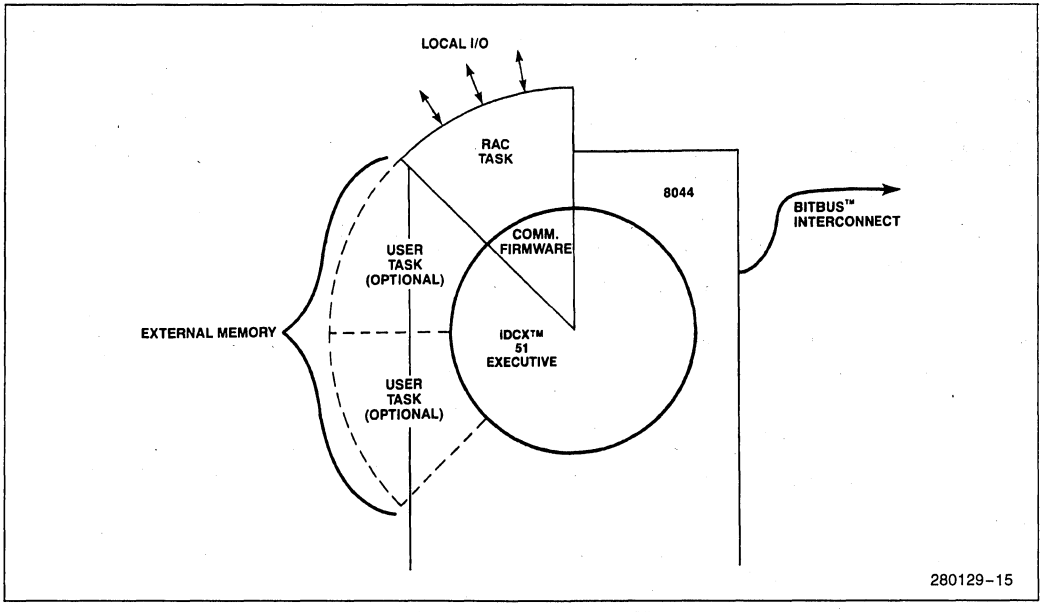


Figure 15. BEM Communication Firmware

Table 6. RAC Functions

Name	Function
RESET_STATION	Perform a software reset.
CREATE_TASK	Perform an RQ$CREATE$TASK system call.
DELETE_TASK	Perform an RQ$DELETE$TASK system call.
GET_FUNCTION_ID	Perform an RQGETFUNCTION$IDS call.
RAC_PROTECT	Suspend or resume RAC services.
READ_IO	Return values from specified I/O ports.
WRITE_IO	Write to the specified I/O ports.
UPDATE_IO	Update the specified I/O ports.
UPLOAD_MEMORY	Return the values in specified memory area.
DOWNLOAD_MEMORY	Write values to specified memory area.
OR_I/O	OR values into specified I/O ports.
AND_I/O	AND values into specified I/O ports.
XOR_I/O	XOR values into specified I/O ports.
READ_INTERNAL	Read values at specified internal RAM areas.
WRITE_INTERNAL	Write values to specified internal RAM areas.
NODE_INFO	Return device related information.
OFFLINE	Set node offline.
UPLOAD_CODE	Read values from code memory space.
DOWNLOAD_CODE	Write values to specified EEPROM memory.

NOTES:
Internal memory locations are included in the 192 bytes of data RAM provided in the microcontroller. External memory refers memory outside the microcontroller—the 28-pin sockets of the iSBX 344A module and the iRCB 44/10A and iRCB 44/20A boards. Each RAC Access Function may refer to 1, 2, 3, 4, 5, or 6 individual I/O or memory locations in a single command.

In addition to allowing creation and deletion of tasks on remote system nodes, the RAC functions allow memory upload and download. This feature eases programming changes in distributed systems and enhances overall system flexibility. Diagnostics can also be downloaded to remote nodes to facilitate system debug.

Another feature optimized for distributed control environments is the GET FUNCTION IDS service. The function ID capability provides the user with the ability to identify specific tasks by function rather than node address and task number. This constant identifier facility remains valid even if functions are moved to different physical locations, eg. another system node.

Aside from the iDCX 51 Executive system calls the user interfaces to the BEM through the task initialization interface; the Initial Task Descriptor. The first user task descriptor must be located at location 0FFF0H in external memory code space so that on power up user code may be automatically detected.

The Initial Task Descriptor (ITD) allows the user to specify the original attributes of a task. Table 7 shows the ITD task structure.

Table 7. ITD Structure

Pattern	Word	value identifying an ITD: "AA55H"
Initial PC	Word	address of first task instruction
Stack-Length	Byte	# bytes of system RAM for tasks stack
Function ID	Byte	value 1–255 associates task w/function
Register Bank	Bit(4)	assigns one register bank to task
Priority	Bit(4)	task priority level
Interrupt Vector	Word	specifies interrupt associated w/task
Next ID	Word	address of the next ITD in linked-list

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0 to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on Any Pin with
Respect to Ground (V_{SS}) .....−0.5V to +7V
Power Dissipation .....2 Watts

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V

Symbol	Parameter	Min	Max	Units	Test Conditions
VIL	Input Low Voltage	−0.5	0.8	V	
VIH	Input High Voltage (Except RST and XTAL2)	2.0	V_{CC} + 0.5	V	
VIH1	Input High Voltage to PST For Reset, XTAL2	2.5	V_{CC} + 0.5		XTAL1 = V_{SS}
VOL	Output Low Voltage Ports 1, 2, 3 (Note 1)		0.45	V	I_{OL} = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, \PSEN (Note 1)		0.45	V	I_{OL} = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4		V	I_{OH} = −80 μA
VOH1	Output High Voltage Port 0, ALE, \PSEN	2.4		V	I_{OH} = −400 μA
IIL	Logical 0 Input Current Ports 1, 2, 3		−500	μA	XTAL1 at V_{SS} Vin = 0.45V
IIH1	Input High Current to RST/VPD For Reset		500	μA	Vin < V_{CC} − 1.5V
ILI	Input Leakage Current to Port 0, \EA		±10	μA	0.45V<Vin<V_{CC}
ICC	Power Supply Current		170	mA	All Outputs Disconnected, EA = V_{CC}
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz
IIL2	Logical 0 Input Current XTAL2		−3.6	mA	XTAL1 at V_{SS} Vin = 0.45V

NOTE:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

A.C. CHARACTERISTICS T_A to 0°C to 70°C, V_{CC} = 5V ±10%, V_{SS} = 0V, C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Other Outputs = 80 pF

PROGRAM MEMORY

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TLHLL	ALE Pulse Width	127		ns	2TCLCL−40		ns
TAVLL	Address Setup to ALE	43		ns	TCLCL−40		ns
TLLAX(1)	Address Hold after ALE	48		ns	TCLCL−35		ns
TLLIV	ALE to Valid Instr in		233	ns		4TCLCL−100	ns
TLLPL	ALE to $\overline{PSEN}$	58		ns	TCLCL−25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		ns	3TCLCL−35		ns
TPLIV	$\overline{PSEN}$ to Valid Instr in		125	ns		3TCLCL−125	ns
TPXIX	Input Instr Hold after $\overline{PSEN}$	0		ns	0		ns
TPXIZ(2)	Input Instr Float after $\overline{PSEN}$		63	ns		TCLCL−20	ns
TPXAV(2)	Address Valid after $\overline{PSEN}$	75		ns	TCLCL−8		ns
TAVIV	Address to Valid Instr in		302	ns		5TCLCL−115	ns
TAZPL	Address Float to $\overline{PSEN}$	−25		ns	−25		ns

NOTES:
1. TLLAX for access to program memory is different from TLLAX for data memory.
2. Interfacing RUPI-44 devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

EXTERNAL DATA MEMORY

Symbol	Parameter	12 MHz Clock			Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		
		Min	Max	Units	Min	Max	Units
TRLRH	$\overline{RD}$ Pulse Width	400		ns	6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		ns	6TCLCL−100		ns
TLLAX(1)	Address Hold after ALE	48		ns	TCLCL−35		
TRLDV	$\overline{RD}$ to Valid Data in		252	ns		5TCLCL−165	ns
TRHDX	Data Hold after $\overline{RD}$	0		ns	0		ns
TRHDZ	Data Float after $\overline{RD}$		97	ns		2TCLCL−70	ns
TLLDV	ALE to Valid Data in		517	ns		8TCLCL−150	ns
TAVDV	Address to Valid Data in		585	ns		9TCLCL−165	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	ns	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203		ns	4TCLCL−130		ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	43	123	ns	TCLCL−40	TCLCL+40	ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		ns	TCLCL−60		ns
TQVWH	Data Setup before $\overline{WR}$	433		ns	7TCLCL−150		ns
TWHQX	Data Hold after $\overline{WR}$	33		ns	TCLCL−50		ns
TRLAZ	RD Low to Address Float		25	ns		25	ns

NOTE:
1. TLLAX for access to program memory is different from TLLAX for access data memory.

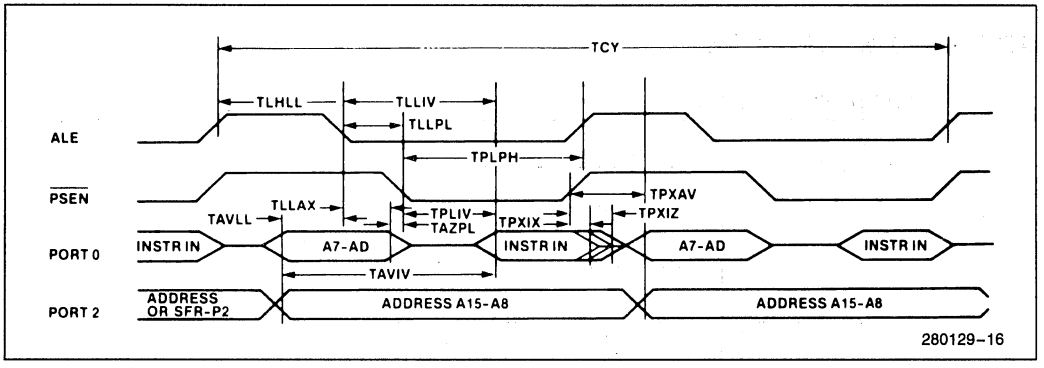
SERIAL INTERFACE

Symbol	Parameter	Min	Max	Units
TDCY	Data Clock	420		ns
TDCL	Data Clock Low	180		ns
TDCH	Data Clock High	100		ns
tTD	Transmit Data Delay		140	ns
tDSS	Data Setup Time	40		ns
tDHS	Data Hold Time	40		ns

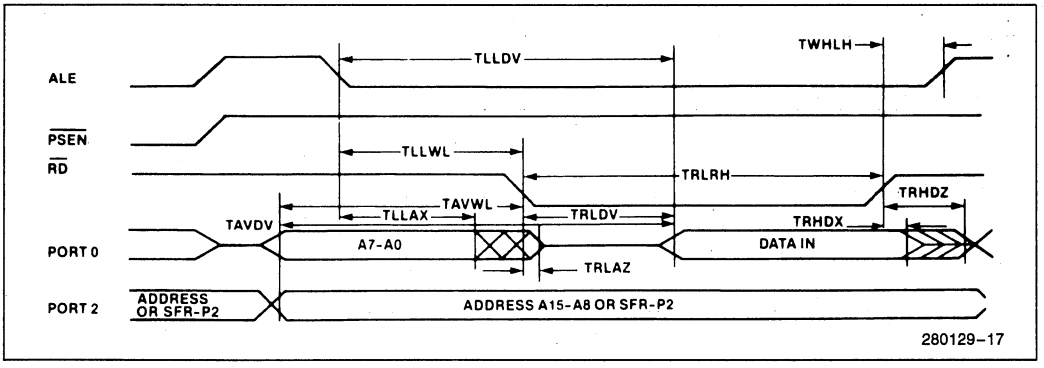
WAVEFORMS

Memory Access

PROGRAM MEMORY READ CYCLE

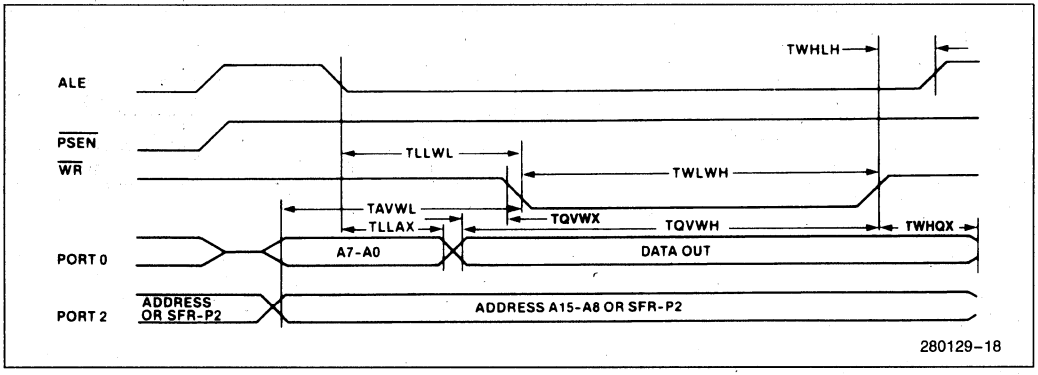


DATA MEMORY READ CYCLE



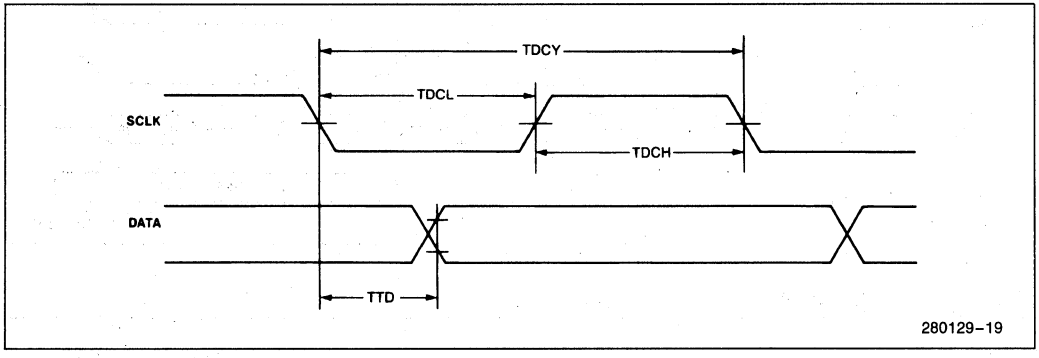
WAVEFORMS (Continued)

DATA MEMORY WRITE CYCLE

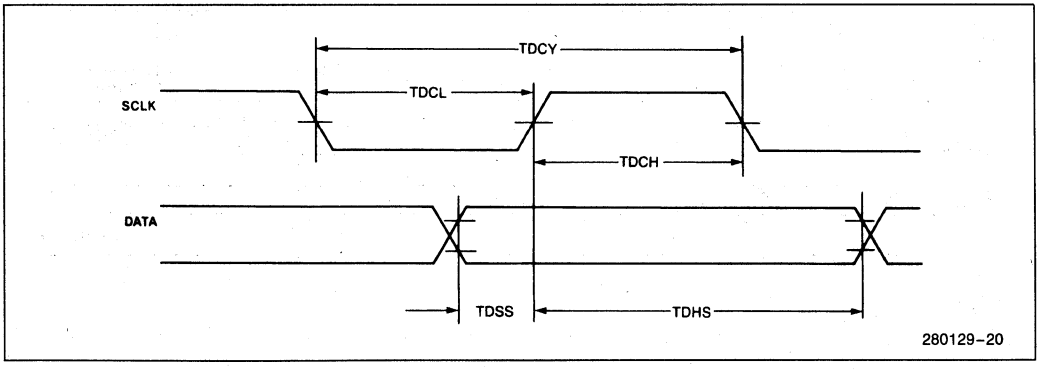


SERIAL I/O WAVEFORMS

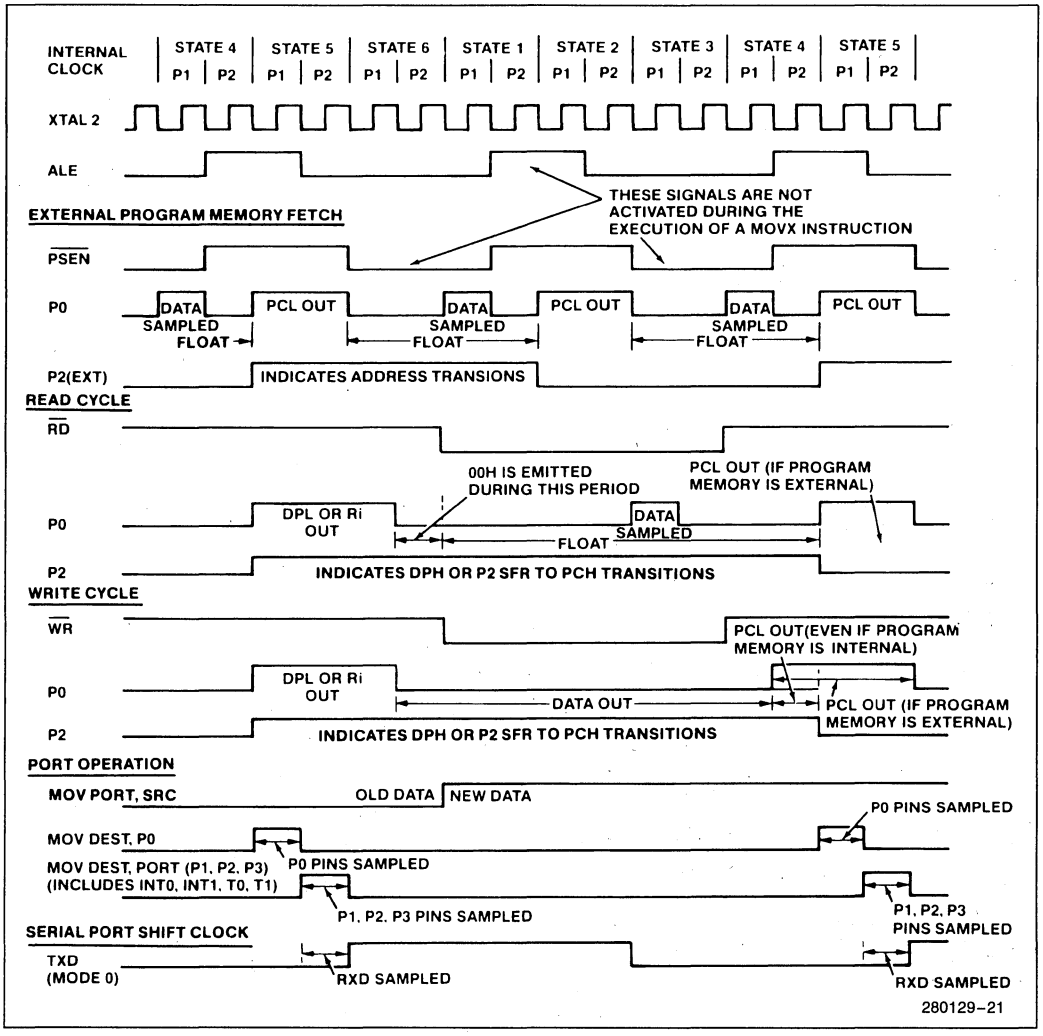
SYNCHRONOUS DATA TRANSMISSION



SYNCHRONOUS DATA RECEPTION

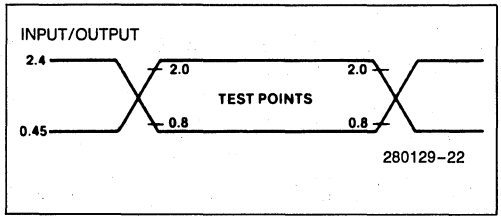


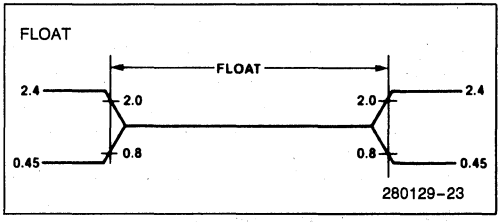
CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

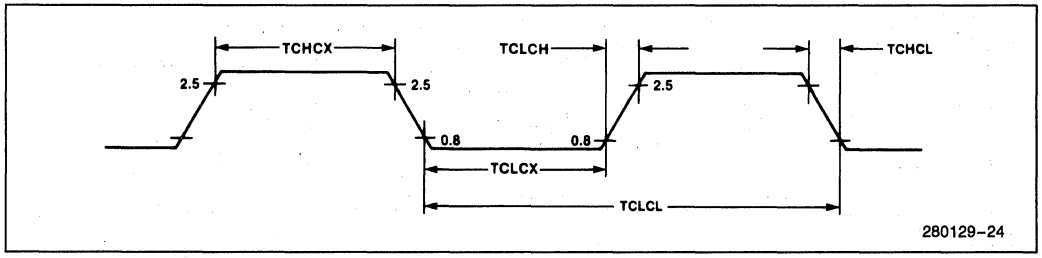
A.C. TESTING INPUT, OUTPUT, FLOAT WAVEFORMS





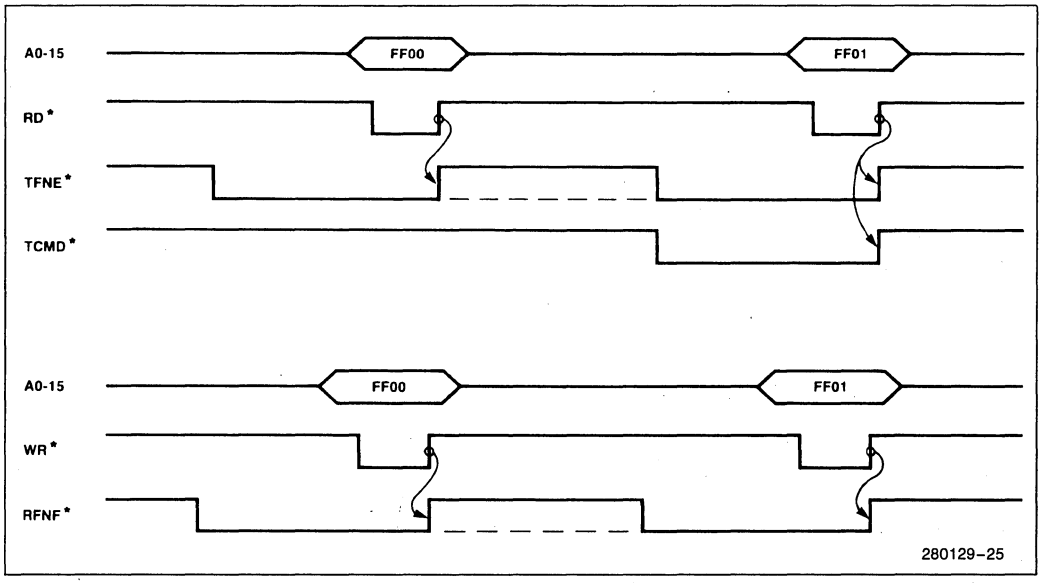
NOTES:
1. A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
2. Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".

EXTERNAL CLOCK DRIVE XTAL2



Symbol	Parameter	Variable Clock Freq = 3.5 MHz to 12 MHz		Units
		Min	Max	
TCLCL	Oscillator Period	83.3	285.7	ns
TCHCX	High Time	30	TCLCL−TCLCX	ns
TCLCX	Low Time	20	TCLCL−TCHCX	ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

BEM PARALLEL INTERFACE LOGIC TIMING



SPECIFICATIONS

Package: 40 pin DIP, 44 pin PLCC
Process: +5V, silicon gate HMOSII

Related Documents (Not Supplied)

Order Number

146312-001— Guide to Using the Distributed Control Modules

231663-002— 8044AH/8344AH/8744H Data Sheet

210941-002 — OEM System Handbook

210918-006 — Embedded Controller Handbook

231166-001 — VLSI Solutions for Distributed Control Applications

ORDERING INFORMATION

Part Number	Description
P,N8044AH,R 0112	BITBUS Enhanced Microcontroller

8044AH/8344AH/8744H
HIGH PERFORMANCE 8-BIT MICROCONTROLLER WITH ON-CHIP SERIAL COMMUNICATION CONTROLLER

- **8044AH—Includes Factory Mask Programmable ROM**
- **8344AH—For Use with External Program Memory**
- **8744H—Includes User Programmable/Eraseable EPROM**

8051 MICROCONTROLLER CORE

- **Optimized for Real Time Control 12 MHz Clock, Priority Interrupts, 32 Programmable I/O Lines, Two 16-bit Timer/Counters**
- **Boolean Processor**
- **4K × 8 ROM, 192 × 8 RAM**
- **64K Accessible External Program Memory**
- **64K Accessible External Data Memory**
- **4 μs Multiply and Divide**

SERIAL INTERFACE UNIT (SIU)

- **Serial Communication Processor that Operates Concurrently to CPU**
- **2.4 Mbps Maximum Data Rate**
- **375 Kbps using On-Chip Phase Locked Loop**
- **Communication Software in Silicon:**
  - **Complete Data Link Functions**
  - **Automatic Station Response**
- **Operates as an SDLC Primary or Secondary Station**

The RUPI-44 family integrates a high performance 8-bit Microcontroller, the Intel 8051 Core, with an Intelligent/high performance HDLC/SDLC serial communication controller, called the Serial Interface Unit (SIU). See Figure 1. This dual architecture allows complex control and high speed data communication functions to be realized cost effectively.

Specifically, the 8044's Microcontroller features: 4K byte On-Chip program memory space; 32 I/O lines; two 16-bit timer/event counters; a 5-source; 2-level interrupt structure; a full duplex serial channel; a Boolean processor; and on-chip oscillator and clock circuitry. Standard TTL and most byte-oriented MCS-80 and MCS-85 peripherals can be used for I/O amd memory expansion.

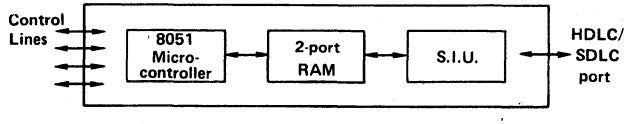
The Serial Interface Unit (SIU) manages the interface to a high speed serial link. The SIU offloads the On-Chip 8051 Microcontroller of communication tasks, thereby freeing the CPU to concentrate on real time control tasks.

The RUPI-44 family consists of the 8044, 8744, and 8344. All three devices are identical except in respect of on-chip program memory. The 8044 contains 4K bytes of mask-programmable ROM. User programmable EPROM replaces ROM in the 8744. The 8344 addresses all program memory externally.

The RUPI-44 devices are fabricated with Intel's reliable +5 volt, silicon-gate HMOSII technology and packaged in a 40-pin DIP.

The 8744H is available in a hermetically sealed, ceramic, 40-lead dual in-line package which includes a window that allows for EPROM erasure when exposed to ultraviolet light (See Erasure Characteristics). During normal operation, ambient light may adversely affect the functionality of the chip. Therefore applications which expose the 8744H to ambient light may require an opaque label over the window.

8044's Dual Controller Architecture



231663-1

Figure 1. Dual Controller Architecture

October 1987
Order Number: 231663-004

Table 1. RUPI™-44 Family Pin Description

VSS

Circuit ground potential.

VCC

+5V power supply during operation and program verification.

PORT 0

Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads (six in 8744).

PORT 1

Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.

In non-loop mode two of the I/O lines serve alternate functions:

— $\overline{RTS}$ (P1.6). Request-to-Send output. A low indicates that the RUPI-44 is ready to transmit.

— $\overline{CTS}$ (P1.7) Clear-to-Send input. A low indicates that a receiving station is ready to receive.

PORT 2

Port 2 is an 8-bit quasi-bidirection I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

PORT 3

Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and RD and WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS LTT loads.

In addition to I/O, some of the pins also serve alternate functions as follows:

— I/$\overline{O}$ RxD (P3.0). In point-to-point or multipoint configurations, this pin controls the direction of pin P3.1. Serves as Receive Data input in loop and diagnostic modes.

— DATA TxD (P3.1) In point-to-point or multipoint configurations, this pin functions as data input/output. In loop mode, it serves as transmit pin. A '0' written to this pin enables diagnostic mode.

— $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0.

— $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1.

— TO (P3.4). Input to counter 0.

— SCLK T1 (P3.5). In addition to I/O, this pin provides input to counter 1 or serves as SCLK (serial clock) input.

— $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.

— $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.

RST

A high on this pin for two machine cycles while the oscillator is running resets the device. A small external pulldown resistor ($\approx$8.2KΩ) from RST to V_{SS} permits power-on reset when a capacitor ($\approx 10\mu f$) is also connected from this pin to V_{CC}.

ALE/$\overline{PROG}$

Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access. It also receives the program pulse input for programming the EPROM version.

$\overline{PSEN}$

The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

$\overline{EA}$/VPP

When held at a TTL high level, the RUPI-44 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the RUPI-44 fetches all instructions from external Program Memory. The pin also receives the 21V EPROM programming supply voltage on the 8744.

Table 1. RUPI™-44 Family Pin Description (Continued)

XTAL 1	XTAL 2
Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2.	Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.

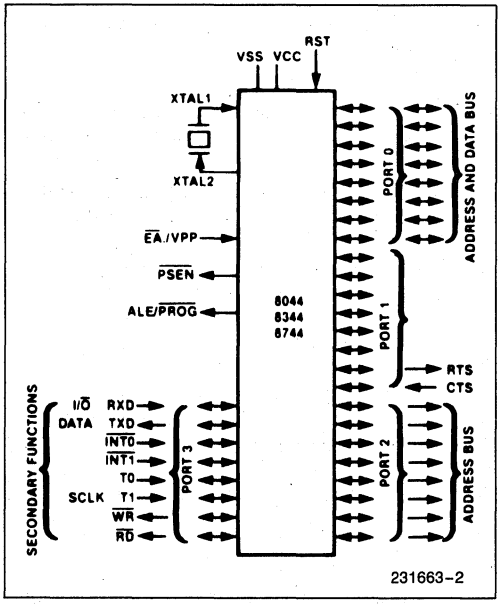


Figure 2. Logic Symbol

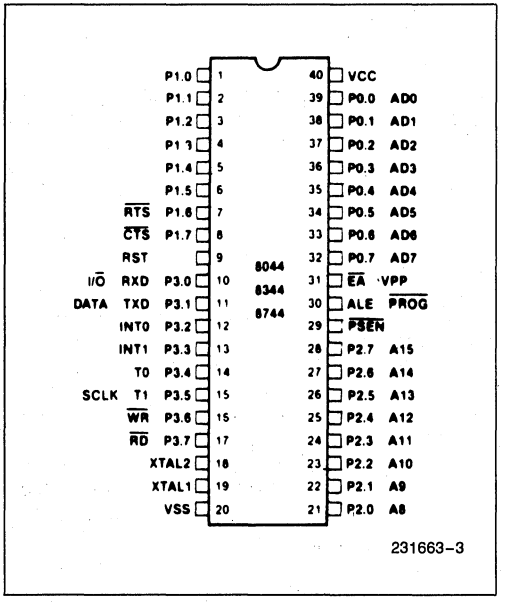


Figure 3A. DIP Pin Configuration

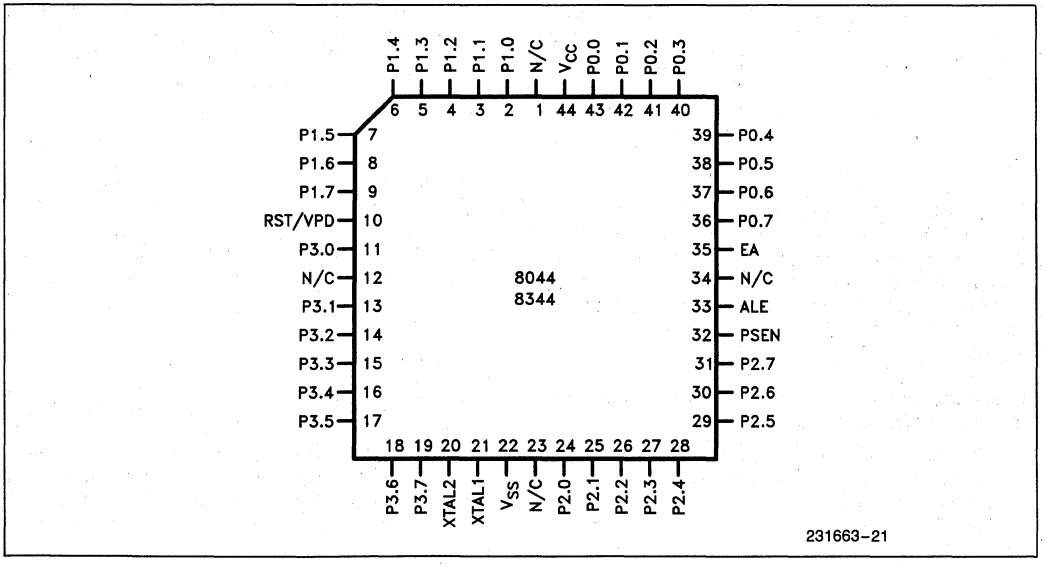


Figure 3B. PLCC Pin Configuration

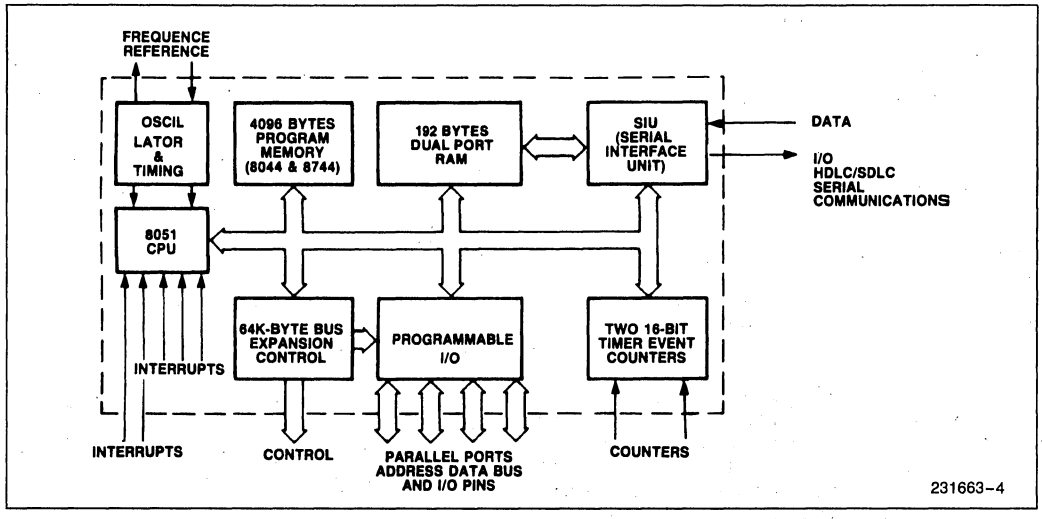


Figure 4. Block Diagram

FUNCTIONAL DESCRIPTION

General

The 8044 integrates the powerful 8051 microcontroller with an intelligent Serial Communication Controller to provide a single-chip solution which will efficiently implement a distributed processing or distributed control system. The microcontroller is a self-sufficient unit containing ROM, RAM, ALU, and its own peripherals. The 8044's architecture and instruction set are identical to the 8051's. The 8044 replaces the 8051's serial interface with an intelligent SDLC/HDLC Serial Interface Unit (SIU). 64 more bytes of RAM have been added to the 8051 RAM array. The SIU can communicate at bit rates up to 2.4 M bps. The SIU works concurrently with the Microcontroller so that there is no throughput loss in either unit. Since the SIU possesses its own intelligence, the CPU is off-loaded from many of the communications tasks, thus dedicating more of its computing power to controlling local peripherals or some external process.

The Microcontroller

The microcontroller is a stand-alone high-performance single-chip computer intended for use in sophisticated real-time application such as instrumentation, industrial control, and intelligent computer peripherals.

The major features of the microcontroller are:

- 8-bit CPU
- on-chip oscillator
- 4K bytes of ROM
- 192 bytes of RAM
- 32 I/O lines
- 64K address space for external Data Memory
- 64K address space for external Program Memory
- two fully programmable 16-bit timer/counters
- a five-source interrupt structure with two priority levels
- bit addressability for Boolean processing

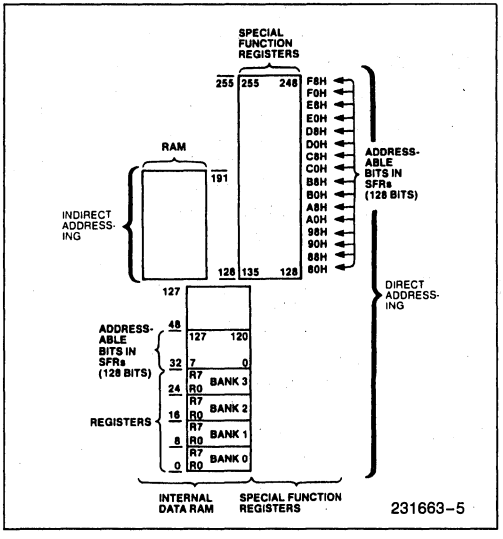


Figure 5. Internal Data Memory Address Space

- 1 μs instruction cycle time for 60% of the instructions 2 μs instruction cycle time for 40% of the instructions
- 4 μs cycle time for 8 by 8 bit unsigned Multiply/Divide

INTERNAL DATA MEMORY

Functionally the Internal Data Memory is the most flexible of the address spaces. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address space and a 128-bit Special Function Register address space as shown in Figure 5.

The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit locations of the on-chip RAM are accessible through Direct Addressing. These bits reside in Internal Data RAM at byte locations 32 through 47. Currently locations 0 through 191 of the Internal Data RAM address space are filled with on-chip RAM.

Parallel I/O

The 8044 has 32 general-purpose I/O lines which are arranged into four groups of eight lines. Each group is called a port. Hence there are four ports; Port 0, Port 1, Port 2, and Port 3. Up to five lines from Port 3 are dedicated to supporting the serial channel when the SIU is invoked. Due to the nature of the serial port, two of Port 3's I/O lines (P3.0 and P3.1) do not have latched outputs. This is true whether or not the serial channel is used.

Port 0 and Port 2 also have an alternate dedicated function. When placed in the external access mode, Port 0 and Port 2 become the means by which the 8044 communicates with external program memory. Port 0 and Port 2 are also the means by which the 8044 communicates with external data memory. Peripherals can be memory mapped into the address space and controlled by the 8044.

Table 2. MCS®-51 Instruction Set Description

Mnemonic		Description	Byte	Cyc
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB	A,#data	Subtract immed data from A with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic		Description	Byte	Cyc
LOGICAL OPERATIONS				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@RI	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@RI	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1

Mnemonic		Description	Byte	Cyc
LOGICAL OPERATIONS (Continued)				
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@RI	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic		Description	Byte	Cyc
DATA TRANSFER (Continued)				
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit) addr	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind RAM w A	1	1
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry Flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry Flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C/bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,/bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2
PROGRAM AND MACHINE CONTROL				
ACALL	addr11	Absolute Subroutine Call	2	2
LCALL	addr16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Absolute Jump	2	2
LJMP	addr16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp, immed, to A & Jump if Not Equal	3	2

Table 2. MCS®-51 Instruction Set Description (Continued)

Mnemonic	Description	Byte	Cyc
PROGRAM AND MACHINE CONTROL (Continued)			
CJNE Rn,#data,rel	Comp, immed, to reg & Jump if Not Equal	3	2
CJNE @Ri,#data, rel	Comp, immed, to ind. & Jump if Not Equal	3	2
DJNZ Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP	No operation	1	1

Notes on data addressing modes:

Rn — Working register R0-R7

direct — 128 internal RAM locations, any I/O port, control or status register

@Ri — Indirect internal RAM location addressed by register R0 or R1

Notes on data addressing modes: (Continued)

#data — 8-bit constant included in instruction

#data16 — 16-bit constant included as bytes 2 & 3 of instruction

bit — 128 software flags, any I/O pin, controll or status bit

Notes on program addressing modes:

addr16 — Destination address for LCALL & LJMP may be anywhere within the 64-K program memory address space

Addr11 — Destination address for ACALL & AJMP will be within the same 2-K page of program memory as the first byte of the following instruction

rel — SJMP and all conditional jumps include an 8-bit offset byte, Range is +127 −128 bytes relative to first byte of the following instruction

Timer/Counters

The 8044 contains two 16-bit counters which can be used for measuring time intervals, measuring pulse widths, counting events, generating precise periodic interrupt requests, and clocking the serial communications. Internally the Timers are clocked at 1/12 of the crystal frequency, which is the instruction cycle time. Externally the counters can run up to 500 KHz.

Interrupt System

External events and the real-time driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two priority level, nested interrupt system is provided. Interrupt response latency ranges from 3 μsec to 7 μsec when using a 12 MHz clock.

All five interrupt sources can be mapped into one of the two priority levels. Each interrupt source can be enabled or disabled individually or the entire interrupt system can be enabled or disabled. The five interrupt sources are: Serial Interface Unit, Timer 1, Timer 2, and two external interrupts. The external interrupts can be either level or edge triggered.

Serial Interface Unit (SIU)

The Serial Interface Unit is used for HDLC/SDLC communications. It handles Zero Bit Insertion/Deletion, Flags automatic access recognization, and a 16-bit cyclic redundancy check. In addition it implements in hardware a subset of the SDLC protocol certain applications it is advantageous to have the CPU control the reception or transmission of every single frame. For this reason the SIU has two modes of operation: "AUTO" and "FLEXIBLE" (or "NON-AUTO"). It is in the AUTO mode that the SIU responds to SDLC frames without CPU intervention; whereas, in the FLEXIBLE mode the reception or transmission of every single frame will be under CPU control.

There are three control registers and eight parameter registers that are used to operate the serial interface. These registers are shown in Figure 5 and Figure 6. The control register set the modes of operation and provide status information. The eight parameter registers buffer the station address, receive and transmit control bytes, and point to the on-chip transmit and receive buffers.

Data to be received or transmitted by the SIU must be buffered anywhere within the 192 bytes of on-chip RAM. Transmit and receive buffers are not allowed to "wrap around" in RAM; a "buffer end" is generated after address 191 is reached.

REGISTER NAMES	SYMBOLIC ADDRESS	BIT ADDRESS	BYTE ADDRESS	
B REGISTER	B	247 through 240	240	(F0H)
ACCUMULATOR	ACC	231 through 224	224	(E0H)
*THREE BYTE FIFO	FIFO		223	(DFH)
	FIFO		222	(DEH)
	FIFO		221	(DDH)
TRANSMIT BUFFER START	TBS		220	(DCH)
TRANSMIT BUFFER LENGTH	TBL		219	(DBH)
TRANSMIT CONTROL BYTE	TCB		218	(DAH)
* SIU STATE COUNTER	SIUST		217	(D9H)
SEND COUNT RECEIVE COUNT	NSNR	223 through 216	216	(D8H)
PROGRAM STATUS WORD	PSW	215 through 208	208	(D0H)
*DMA COUNT	DMA CNT		207	(CFH)
STATION ADDRESS	STAD		206	(CEH)
RECEIVE FIELD LENGTH	RFL		205	(CDH)
RECEIVE BUFFER START	RBS		204	(CCH)
RECEIVE BUFFER LENGTH	RBL		203	(CBH)
RECEIVE CONTROL BYTE	RCB		202	(CAH)
SERIAL MODE	SMD		201	(C9H)
STATUS REGISTER	STS	207 through 200	200	(C8H)
INTERRUPT PRIORITY CONTROL	IP	191 through 184	184	(B8H)
PORT 3	P3	183 through 176	176	(B0H)
INTERRUPT ENABLE CONTROL	IE	175 through 168	168	(A8H)
PORT 2	P2	167 through 160	160	(A0H)
PORT 1	P1	151 through 144	144	(90H)
TIMER HIGH 1	TH1		141	(8DH)
TIMER HIGH 0	TH0		140	(8CH)
TIMER LOW 1	TL1		139	(8BH)
TIMER LOW 0	TL0		138	(8AH)
TIMER MODE	TMOD		137	(89H)
TIMER CONTROL	TCON	143 through 136	136	(88H)
DATA POINTER HIGH	DPH		131	(83H)
DATA POINTER LOW	DPL		130	(82H)
STACK POINTER	SP		129	(81H)
PORT 0	P0	135 through 128	128	(80H)

SFR's CONTAINING DIRECT ADDRESSABLE BITS

231663-6

NOTE:
*ICE Support Hardware registers. Under normal operating conditions there is no need for the CPU to access these registers.

Figure 5. Mapping of Special Function Registers

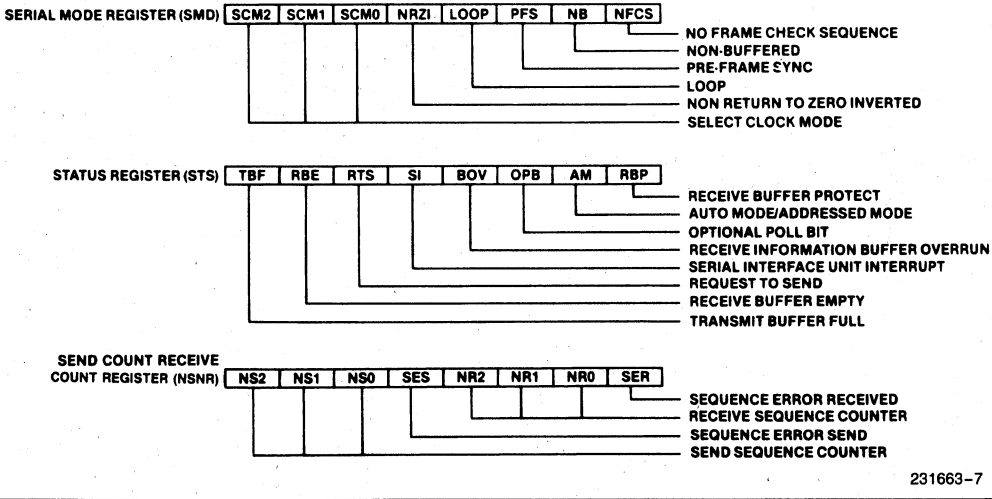


Figure 6. Serial Interface Unit Control Registers

With the addition of only a few bytes of code, the 8044's frame size is not limited to the size of its internal RAM (192 bytes), but rather by the size of external buffer with no degradation of the RUPI's features (e.g. NRZI, zero bit insertion/deletion, address recognition, cyclic redundancy check). There is a special function register called SIUST whose contents dictates the operation of the SIU. At low data rates, one section of the SIU (the Byte Processor) performs no function during known intervals. For a given data rate, these intervals (stand-by mode) are fixed. The above characteristics make it possible to program the CPU to move data to/from external RAM and to force the SIU to perform some desired hardware tasks while transmission or reception is taking place. With these modifications, external RAM can be utilized as a transmit and received buffer instead of the internal RAM.

AUTO Mode

In the AUTO mode the SIU implements in hardware a subset of the SDLC protocol such that it responds to many SDLC frames without CPU intervention. All AUTO mode responses to the primary station will comform to IBM's SDLC definition. The advantages of the AUTO mode are that less software is required to implement a secondary station, and the hardware generated response to polls is much faster than doing it in software. However, the Auto mode can not be used at a primary station.

To transmit in the AUTO mode the CPU must load the Transmit Information Buffer, Transmit Buffer Start register, Transmit Buffer Length register, and set the Transmit Buffer Full bit. The SIU automatically responds to a poll by transmitting an information frame with the P/F bit in the control field set. When the SIU receives a positive acknowledgement from the primary station, it automatically increments the Ns field in the NSNR register and interrupts the CPU. A negative acknowledgement would cause the SIU to retransmit the frame.

To receive in the AUTO mode, the CPU loads the Receive Buffer Start register, the Receive Buffer Length register, clears the Receive Buffer Protect bit, and sets the Receive Buffer Empty bit. If the SIU is polled in this state, and the TBF bit indicates that the Transmit Buffer is empty, an automatic RR response will be generated. When a valid information frame is received the SIU will automatically increment Nr in the NSNR register and interrupt the CPU.

While in the AUTO mode the SIU can recognize and respond to the following commands without CPU intervention: I (Information), RR (Receive Ready), RNR (Receive Not Ready), REJ (Reject), and UP (Unnumbered Poll). The SIU can generate the following responses without CPU intervention: I (Information), RR (Receive Ready), and RNR (Receive Not Ready).

When the Receive Buffer Empty bit (RBE) indicates that the Receive Buffer is empty, the receiver is enabled, and when the RBE bit indicates that the Receive Buffer is full, the receiver is disabled. Assuming that the Receiver Buffer is empty, the SIU will respond to a poll with an I frame if the Transmit Buffer is full. If the Transmit Buffer is empty, the SIU will respond to a poll with a RR command if the Receive Buffer Protect bit (RBP) is cleared, or an RNR command if RBP is set.

FLEXIBLE (or NON-AUTO) Mode

In the FLEXIBLE mode all communications are under control of the CPU. It is the CPU's task to encode and decode control fields, manage acknowledgements, and adhere to the requirements of the HDLC/SDLC protocols. The 8044 can be used as a primary or a secondary station in this mode.

To receive a frame in the FLEXIBLE mode, the CPU must load the Receive Buffer Start register, the Receive Buffer Length register, clear the Receive Buffer Protect bit, and set the Receive Buffer Empty bit. If a valid opening flag is received and the address field matches the byte in the Station Address register or the address field contains a broadcast address, the 8044 loads the control field in the receive control byte register, and loads the I field in the receive buffer. If there is no CRC error, the SIU interrupts the CPU, indicating a frame has just been received. If there is a CRC error, no interrupt occurs. The Receive Field Length register provides the number of bytes that were received in the information field.

To transmit a frame, the CPU must load the transmit information buffer, the Transmit Buffer Start register, the Transmit Buffer Length register, the Transmit Control Byte, and set the TBF and the RTS bit. The SIU, unsolicited by an HDLC/SDLC frame, will transmit the entire information frame, and interrupt the CPU, indicating the completion of transmission. For supervisory frames or unnumbered frames, the transmit buffer length would be 0.

CRC

The FCS register is initially set to all 1's prior to calculating the FCS field. The SIU will not interrupt the CPU if a CRC error occurs (in both AUTO and FLEXIBLE modes). The CRC error is cleared upon receiving of an opening flag.

Frame Format Options

In addition to the standard SDLC frame format, the 8044 will support the frames displayed in Figure 7. The standard SDLC frame is shown at the top of this figure. For the remaining frames the information field will incorporate the control or address bytes and the frame check sequences; therefore these fields will be stored in the Transmit and Receive buffers. For example, in the non-buffered mode the third byte is treated as the beginning of the information field. In the non-addressed mode, the information field begins after the opening flag. The mode bits to set the frame format options are found in the Serial Mode register and the Status register.

FRAME OPTION	NFCS	NB	AM[1]	FRAME FORMAT
Standard SDLC NON-AUTO Mode	0	0	0	F A C I FCS F
Standard SDLC AUTO Mode	0	0	1	F A C I FCS F
Non-Buffered Mode NON-AUTO Mode	0	1	1	F A I FCS F
Non-Addressed Mode NON-AUTO Mode	0	1	0	F I FCS F
No FCS Field NON-AUTO Mode	1	0	0	F A C I F
No FCS Field AUTO Mode	1	0	1	F A C I F
No FCS Field Non-Buffered Mode NON-AUTO Mode	1	1	1	F A I F
No FCS Field Non-Addressed Mode NON-AUTO Mode	1	1	0	F I F

Mode Bits:
AM — "AUTO" Mode/Addressed Mode
NB — Non-Buffered Mode
NFCS — No FCS Field Mode

Key to Abbreviations:
F = Flag (01111110)
A = Address Field
C = Control Field
I = Information Field
FCS= Frame Check Sequence

Note 1:
The AM bit function is controlled by the NB bit. When NB = 0, AM becomes AUTO mode select, when NB = 1, AM becomes Address mode select.

Figure 7. Frame Format Options

Extended Addressing

To realize an extended control field or an extended address field using the HDLC protocol, the FLEXIBLE mode must be used. For an extended control field, the SIU is programmed to be in the non-buffered mode. The extended control field will be the first and second bytes in the Receive and Transmit Buffers. For extended addressing the SIU is placed in the non-addressed mode. In this mode the CPU must implement the address recognition for received frames. The addressing field will be the initial bytes in the Transmit and Receive buffers followed by the control field.

The SIU can transmit and receive only frames which are multiples of 8 bits. For frames received with other than 8-bit multiples, a CRC error will cause the SIU to reject the frame.

SDLC Loop Networks

The SIU can be used in an SDLC loop as a secondary or primary station. When the SIU is placed in the Loop mode it receives the data on pin 10 and transmits the data one bit time delayed on pin 11. It can also recognize the Go ahead signal and change it into a flag when it is ready to transmit. As a secondary station the SIU can be used in the AUTO or FLEXIBLE modes. As a primary station the FLEXIBLE mode is used; however, additional hardware is required for generating the Go Ahead bit pattern. In the Loop mode the maximum data rate is 1 Mbps clocked or 375 Kpbs self-clocked.

SDLC Multidrop Networks

The SIU can be used in a SDLC non-loop configuration as a secondary or primary station. When the SIU is placed in the non-loop mode, data is received and transmitted on pin 11, and pin 10 drives a tri-state buffer. In non-loop mode, modem interface pins, RTS and CTS, become available.

Data Clocking Options

The 8044's serial port can operate in an externally clocked or self clocked system. A clocked system provides to the 8044 a clock synchronization to the data. A self-clocked system uses the 8044's on-chip Digital Phase Locked Loop (DPLL) to recover the clock from the data, and clock this data into the Serial Receive Shift Register.

In this mode, a clock synchronized with the data is externally fed into the 8044. This clock may be generated from an External Phase Locked Loop, or possibly supplied along with the data. The 8044 can transmit and receive data in this mode at rates up to 2.4 Mbps.

This self clocked mode allows data transfer without a common system data clock. An on-chip Digital Phase Locked Loop is employed to recover the data clock which is encoded in the data stream. The DPLL will converge to the nominal bit center within eight bit transitions, worst case. The DPLL requires a reference clock of either 16 times (16x) or 32 times (32x) the data rate. This reference clock may be externally applied or internally generated. When internally generated either the 8044's internal logic clock (crystal frequency divided by two) or the timer 1 overflow is used as the reference clock. Using the internal timer 1 clock the data rates can vary from 244 to 62.5 Kbps. Using the internal logic clock at a 16x sampling rate, receive data can either be 187.5 Kbps, or 375 Kbps. When the reference clock for the DPLL is externally applied the data rates can vary from 0 to 375 Kbps at a 16x sampling rate.

To aid in a Phase Locked Loop capture, the SIU has a NRZI (Non Return to Zero Inverted) data encoding and decoding option. Additionally the SIU has a preframe sync option that transmits two bytes of alternating 1's and 0's to ensure that the receive station DPLL will be synchronized with the data by the time it receives the opening flag.

Control and Status Registers

There are three SIU Control and Status Registers:

Serial Mode Register (SMD)

Status/Command Register (STS)

Send/Receive Count Register (NSNR)

The SMD, STS, and NSNR, registers are all cleared by system reset. This assures that the SIU will power up in an idle state (neither receiving nor transmitting).

These registers and their bit assignments are described below.

SMD: Serial Mode Register (byte-addressable)

Bit 7:	6	5	4	3	2	1	0
SCM2	SCM1	SCM0	NRZI	LOOP	PFS	NB	NFCS

The Serial Mode Register (Address C9H) selects the operational modes of the SIU. The 8044 CPU can both read and write SMD. The SIU can read SMD but cannot write to it. To prevent conflict between CPU and SIU access to SMD, the CPU should write SMD only when the Request To Send (RTS) and

Receive Buffer Empty (RBE) bits (in the STS register) are both false (0). Normally, SMD is accessed only during initialization.

The individual bits of the Serial Mode Register are as follows:

Bit #	Name	Description
SMD.0	NFCS	No FCS field in the SDLC frame.
SMD.1	NB	Non-Buffered mode. No control field in the SDLC frame.
SMD.2	PFS	Pre-Frame Sync mode. In this mode, the 8044 transmits two bytes before the first flag of a frame, for DPLL synchronization. If NRZI is enabled, 00H is sent; otherwise, 55H is sent. In either case, 16 preframe transitions are guaranteed.
SMD.3	LOOP	Loop configuration.
SMD.4	NRZI	NRZI coding option. If bit = 1, NRZI coding is used. If bit = 0, then it is straight binary (NRZ).
SMD.5	SCM0	Select Clock Mode—Bit 0
SMD.6	SCM1	Select Clock Mode—Bit 1
SMD.7	SCM2	Select Clock Mode—Bit 2

The SCM bits decode as follows:

SCM				Data Rate
2	1	0	Clock Mode	(Bits/sec)*
0	0	0	Externally clocked	0-2.4M**
0	0	1	Reserved	
0	1	0	Self clocked, timer overflow	244-62.5K
0	1	1	Reserved	
1	0	0	Self clocked, external 16x	0-375K
1	0	1	Self clocked, external 32x	0-187.5K
1	1	0	Self clocked, internal fixed	375K
1	1	1	Self clocked, internal fixed	187.5K

NOTES:
*Based on a 12 Mhz crystal frequency
**0-1 M bps in loop configuration

STS: Status/Command Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	TBF	RBE	RTS	SI	BOV	OPB	AM	RBP

The Status/Command Register (Address C8H) provides operational control of the SIU by the 8044 CPU, and enables the SIU to post status information for the CPU's access. The SIU can read STS, and can alter certain bits, as indicated below. The CPU can both read and write STS asynchronously. However, 2-cycle instructions that access STS during both cycles ('JBC/B, REL' and 'MOV/B, C.') should not be used, since the SIU may write to STS between the two CPU accesses.

The individual bits of the Status/Command Register are as follows:

Bit #	Name	Description
STS.0	RBP	Receive Buffer Protect. Inhibits writing of data into the receive buffer. In AUTO mode, RBP forces an RNR response instead of an RR.
STS.1	AM	AUTO Mode/Addressed Mode. Selects AUTO mode where AUTO mode is allowed. If NB is true, (= 1), the AM bit selects the addressed mode. AM may be cleared by the SIU.
STS.2	OPB	Optional Poll Bit. Determines whether the SIU will generate an AUTO response to an optional poll (UP with P = 0). OPM may be set or cleared by the SIU.
STS.3	BOV	Receive Buffer Overrun. BOV may be set or cleared by the SIU.
STS.4	SI	SIU Interrupt. This is one of the five interrupt sources to the CPU. The vector location = 23H. SI may be set by the SIU. It should be cleared by the CPU before returning from an interrupt routine.
STS.5	RTS	Request To Send. Indicates that the 8044 is ready to transmit or is transmitting. RTS may be read or written by the CPU. RTS may be read by the SIU, and in AUTO mode may be written by the SIU.
STS.6	RBE	Receive Buffer Empty. RBE can be thought of as Receive Enable. RBE is set to one by the CPU when it is ready to receive a frame, or has just read the buffer, and to zero by the SIU when a frame has been received.
STS.7	TBF	Transmit Buffer Full. Written by the CPU to indicate that it has filled the transmit buffer. TBF may be cleared by the SIU.

NSNR: Send/Receive Count Register (bit-addressable)

Bit:	7	6	5	4	3	2	1	0
	NS2	NS1	NS0	SES	NR2	NR1	NR0	SER

The Send/Receive Count Register (Address D8H) contains the transmit and receive sequence numbers, plus tally error indications. The SIU can both read and write NSNR. The 8044 CPU can both read and write NSNR asynchronously. However, 2-cycle instructions that access NSNR during both cycles ('JBC /B, REL,' and 'MOV /B,C') should not be used, since the SIU may write to NSMR between the two 8044 CPU accesses.

The individual bits of the Send/Receive Count Register are as follows:

Bit #	Name	Description
NSNR.0	SER	Receive Sequence Error: NS (P) ≠ NR (S)
NSNR.1	NR0	Receive Sequence Counter—Bit 0
NSNR.2	NR1	Receive Sequence Counter—Bit 1
NSNR.3	NR2	Receive Sequence Counter—Bit 2
NSNR.4	SES	Send Sequence Error: NR (P) ≠ NS (S) and NR (P) ≠ NS (S) + 1
NSNR.5	NS0	Send Sequence Counter—Bit 0
NSNR.6	NS1	Send Sequence Counter—Bit 1
NSNR.7	NS2	Send Sequence Counter—Bit 2

Parameter Registers

There are eight parameter registers that are used in connection with SIU operation. All eight registers may be read or written by the 8044 CPU. RFL and RCB are normally loaded by the SIU.

The eight parameter registers are as follows:

STAD: Station Address Register (byte-addressable)

The Station Address register (Address CEH) contains the station address. To prevent acess conflict, the CPU should access STAD only when the SIU is idle (RTS = 0 and RBE = 0). Normally, STAD is accessed only during initialization.

TBS: Transmit Buffer Start Address Register (byte-addressable)

The Transmit Buffer Start address register (Address DCH) points to the location in on-chip RAM for the beginning of the I-field of the frame to be transmitted. The CPU should access TBS only when the SIU is not transmitting a frame (when TBF = 0).

TBL: Transmit Buffer Length Register (byte = addressable)

The Transmit Buffer Length register (Address DBH) contains the length (in bytes) of the I-field to be transmitted. A blank I-field (TBL = 0) is valid. The CPU should access TBL only when the SIU is not transmitting a frame (when TBF = 0).

NOTE:
The transmit and receive buffers are not allowed to "wrap around" in the on-chip RAM. A "buffer end" is automatically generated if address 191 (BFH) is reached.

TCB: Transmit Control Byte Register (byte-addressable)

The Transmit Control Byte register (Address DAH) contains the byte which is to be placed in the control field of the transmitted frame, during NON-AUTO mode transmission. The CPU should access TCB only when the SIU is not transmitting a frame (when TBF = 0). The N_S and N_R counters are not used in the NON-AUTO mode.

RBS: Receive Buffer Start Address Register (byte-addressable)

The Receive Buffer Start address register (Address CCH) points to the location in on-chip RAM where the beginning of the I-field of the frame being received is to be stored. The CPU should write RBS only when the SIU is not receiving a frame (when RBE = 0).

RBL: Receive Buffer Length Register (byte-addressable)

The Receive Buffer Length register (Address CBH) contains the length (in bytes) of the area in on-chip RAM allocated for the received I-field. RBL = 0 is valid. The CPU should write RBL only when RBE = 0.

RFL: Receive Field Length Register (byte-addressable)

The Receive Field Length register (Address CDH) contains the length (in bytes) of the received I-field that has just been loaded into on-chip RAM. RFL is loaded by the SIU. RFL = 0 is valid. RFL should be accessed by the CPU only when RBE = 0.

RCB: Receive Control Byte Register (byte-addressable)

The Received Control Byte register (Address CAH) contains the control field of the frame that has just been received. RCB is loaded by the SIU. The CPU can only read RCB, and should only access RCB when RBE = 0.

ICE Support

The 8044 In-Circuit Emulator (ICE-44) allows the user to exercise the 8044 application system and monitor the execution of instructions in real time.

The emulator operates with Intel's Intellec™ development system. The development system interfaces with the user's 8044 system through an in-cable buffer box. The cable terminates in a 8044 pin-compatible plug, which fits into the 8044 socket in the user's system. With the emulator plug in place, the user can excercise his system in real time while collecting up to 255 instruction cycles of real-time data. In addition, he can single-step the program.

Static RAM is available (in the in-cable buffer box) to emulate the 8044 internal and external program memory and external data memory. The designer can display and alter the contents of the replacement memory in the buffer box, the internal data memory, and the internal 8044 registers, including the SFR's.

SIUST: SIU State Counter (byte-addressable)

The SIU State Counter (Address D9H) reflects the state of the internal logic which is under SIU control. Therefore, care must be taken not to write into this register. This register provides a useful means for debugging 8044 receiver problem.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature.....−65°C to −150°C
Voltage on $\overline{EA}$, VPP Pin to VSS...−0.5V to −21.5V
Voltage on Any Other Pin to VSS....−0.5V to −7V
Power Dissipation 2W

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter		Min	Max	Unit	Test Conditions
VIL	Input Low Voltage (Except $\overline{EA}$ Pin of 8744H)		−0.5	0.8	V	
VIL1	Input Low Voltage to $\overline{EA}$ Pin of 8744H		0	0.8	V	
VIH	Input High Voltage (Except XTAL2, RST)		2.0	VCC + 0.5	V	
VIH1	Input High Voltage to XTAL2, RST		2.5	VCC + 0.5	V	XTAL1 = VSS
VOL	Output Low Voltage (Ports 1, 2, 3)*			0.45	V	IOL = 1.6mA
VOL1	Output Low Voltage (Port 0,ALE,$\overline{PSEN}$)*					
		8744H		0.60 0.45	V V	IOL = 3.2 mA IOL = 2.4 mA
		8044AH/8344AH		0.45	V	IOL = 3.2 mA
VOH	Output High Voltage (Ports 1, 2, 3)		2.4		V	IOH = −80 μA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)		2.4		V	IOH = −400 μA
IIL	Logical 0 Input Current (Ports 1, 2, 3)			−500	μA	Vin = 0.45V
IIL1	Logical 0 Input Current to $\overline{EA}$ Pin of 8744H only			−15	mA	
IIL2	Logical 0 Input Current (XTAL2)			−3.6	mA	Vin = 0.45V
ILI	Input Leakage Current (Port 0) 8744H 8044AH/8344AH			 ±100 ±10	 μA μA	 0.45 < Vin < VCC 0.45 < Vin < VCC
IIH	Logical 1 Input Current to $\overline{EA}$ Pin of 8744H			500	μA	
IIH1	Input Current to RST to Activate Reset			500	μA	Vin < (VCC − 1.5V)
ICC	Power Supply Current: 8744H 8044AH/8344AH			 285 170	 mA mA	All Outputs Disconnected: $\overline{EA}$ = VCC
CIO	Pin Capacitance			10	pF	Test Freq. = 1MHz(1)

***NOTES:**
1. Sampled not 100% tested. T_A = 25°C.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pin when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, VCC = 5V ± 10%, VSS = 0V, Load Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		ns
TAVLL	Address Valid to ALE Low	43		TCLCL-40		ns
TLLAX[1]	Address Hold After ALE Low	48		TCLCL-35		ns
TLLIV	ALE Low to Valid Instr in 8744H 8044AH/8344AH		 183 233		 4TCLCL-150 4TCLCL-100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	58		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width 8744H 8044AH/8344AH	 190 215		 3TCLCL-60 3TCLCL-35		 ns ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr in 8744H 8044AH/8344AH		 100 125		 3TCLCL-150 3TCLCL-125	 ns ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ[2]	Input Instr Float After $\overline{PSEN}$		63		TCLCL-20	ns
TPXAV[2]	$\overline{PSEN}$ to Address Valid	75		TCLCL-8		ns
TAVIV	Address to Valid Instr in 8744H 8044AH/8344AH		 267 302		 5TCLCL-150 5TCLCL-115	 ns ns
TAZPL	Address Float to $\overline{PSEN}$	−25		−25		ns

NOTES:
1. TLLAX for access to program memory is different from TLLAX for data memory.
2. Interfacing RUPI-44 devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Clock 1/TCLCL = 3.5 MHz to 12 MHz		Unit
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL-100		ns
TLLAX	Address Hold after ALE	48		TCLCL-35		ns
TRLDV	$\overline{RD}$ Low to Valid Data in		252		5TCLCL-165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL-50	3TLCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL-130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition					
	8744H	13		TCLCL-70		ns
	8044AH/8344AH	23		TCLCL-60		ns
TQVWH	Data Setup Before $\overline{WR}$ High	433		7TCLCL-150		ns
TWHQX	Data Held After $\overline{WR}$	33		TCLCL-50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		25		25	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High					
	8744H	33	133	TCLCL-50	TCLCL+50	ns
	8044AH/8344AH	43	123	TCLCL-40	TCLCL+50	ns

NOTE:
1. TLLAX for access to program memory is different from TLLAX for access data memory.

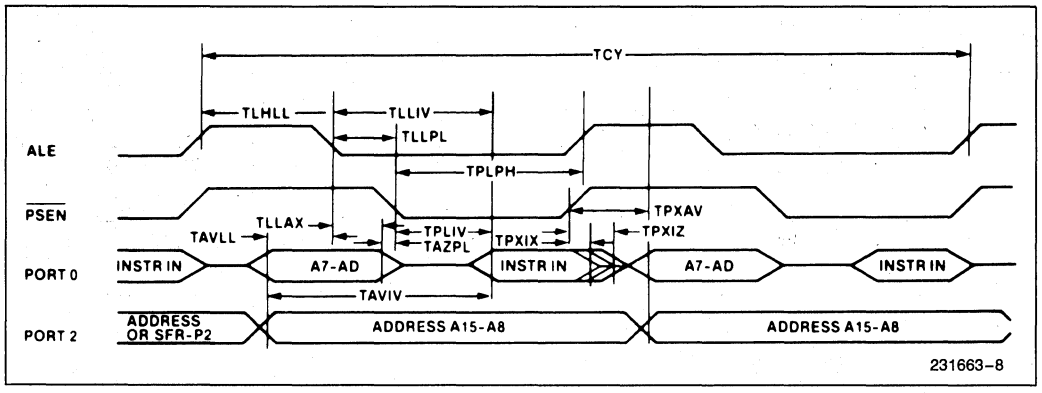
Serial Interface Characteristics

Symbol	Parameter	Min	Max	Unit
TDCY	Data Clock	420		ns
TDCL	Data Clock Low	180		ns
TDCH	Data Clock High	100		ns
tTD	Transmit Data Delay		140	ns
tDSS	Data Setup Time	40		ns
tDHS	Data Hold Time	40		ns

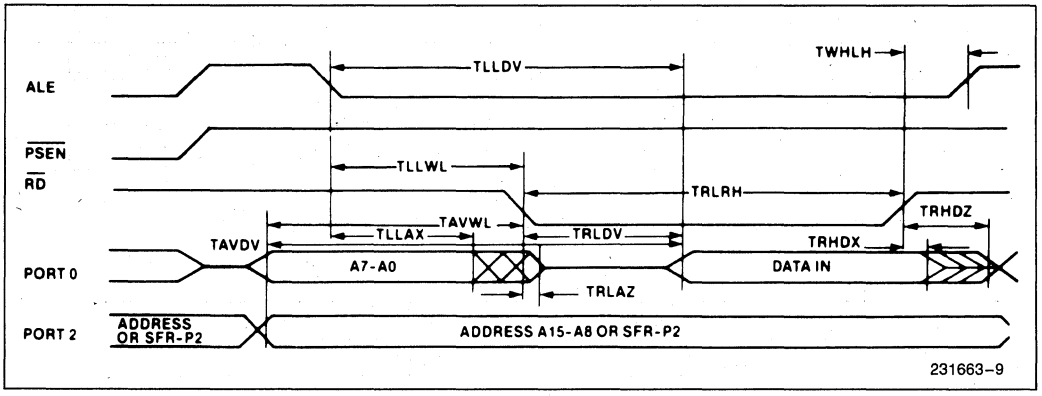
WAVEFORMS

Memory Access

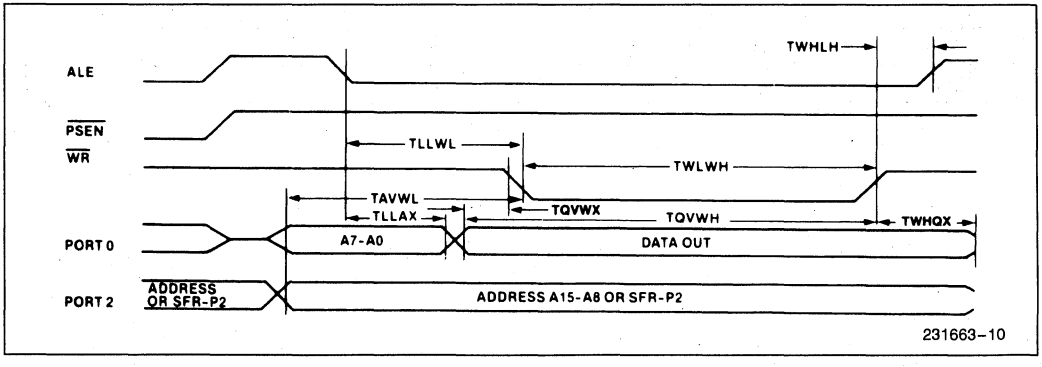
PROGRAM MEMORY READ CYCLE



DATA MEMORY READ CYCLE

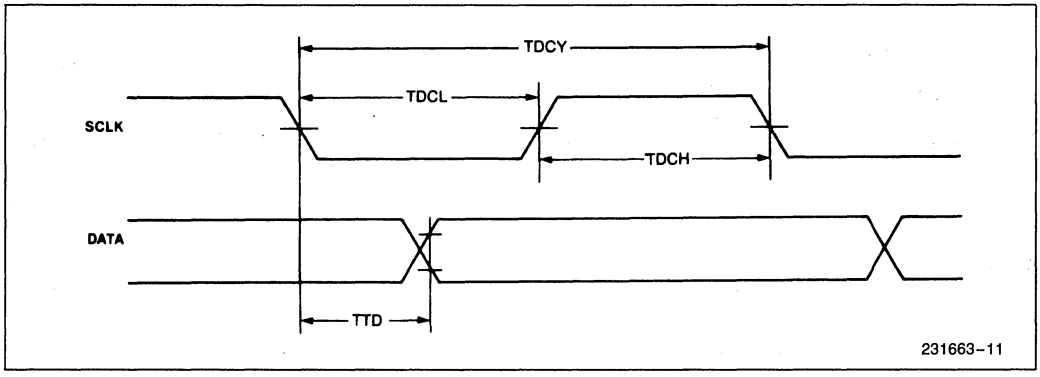


DATA MEMORY WRITE CYCLE

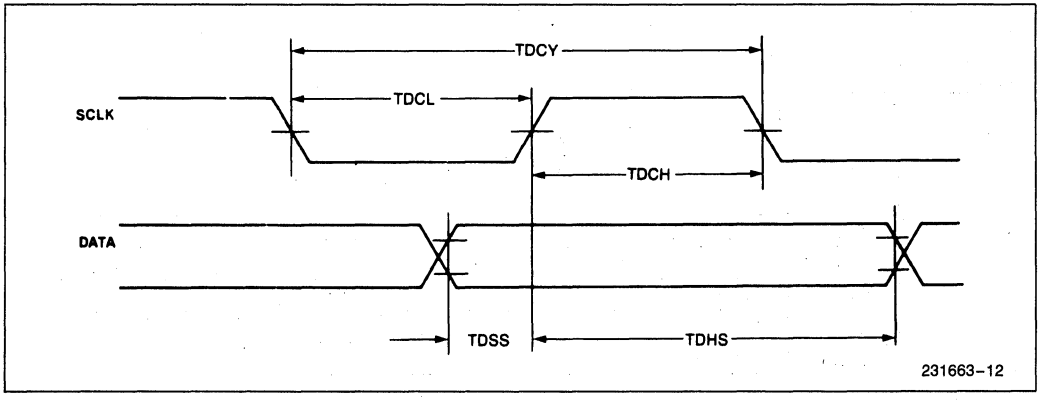


SERIAL I/O WAVEFORMS

SYNCHRONOUS DATA TRANSMISSION

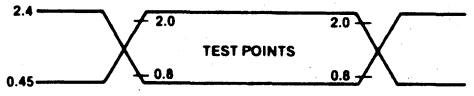


SYNCHRONOUS DATA RECEPTION



AC TESTING INPUT, OUTPUT, FLOAT WAVEFORMS

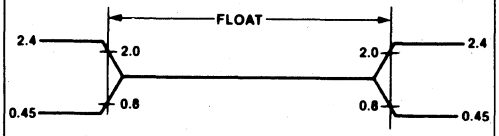
INPUT/OUTPUT



231663-13

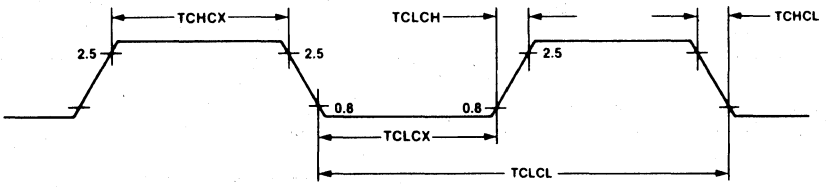
AC testing inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0" Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

FLOAT



231663-14

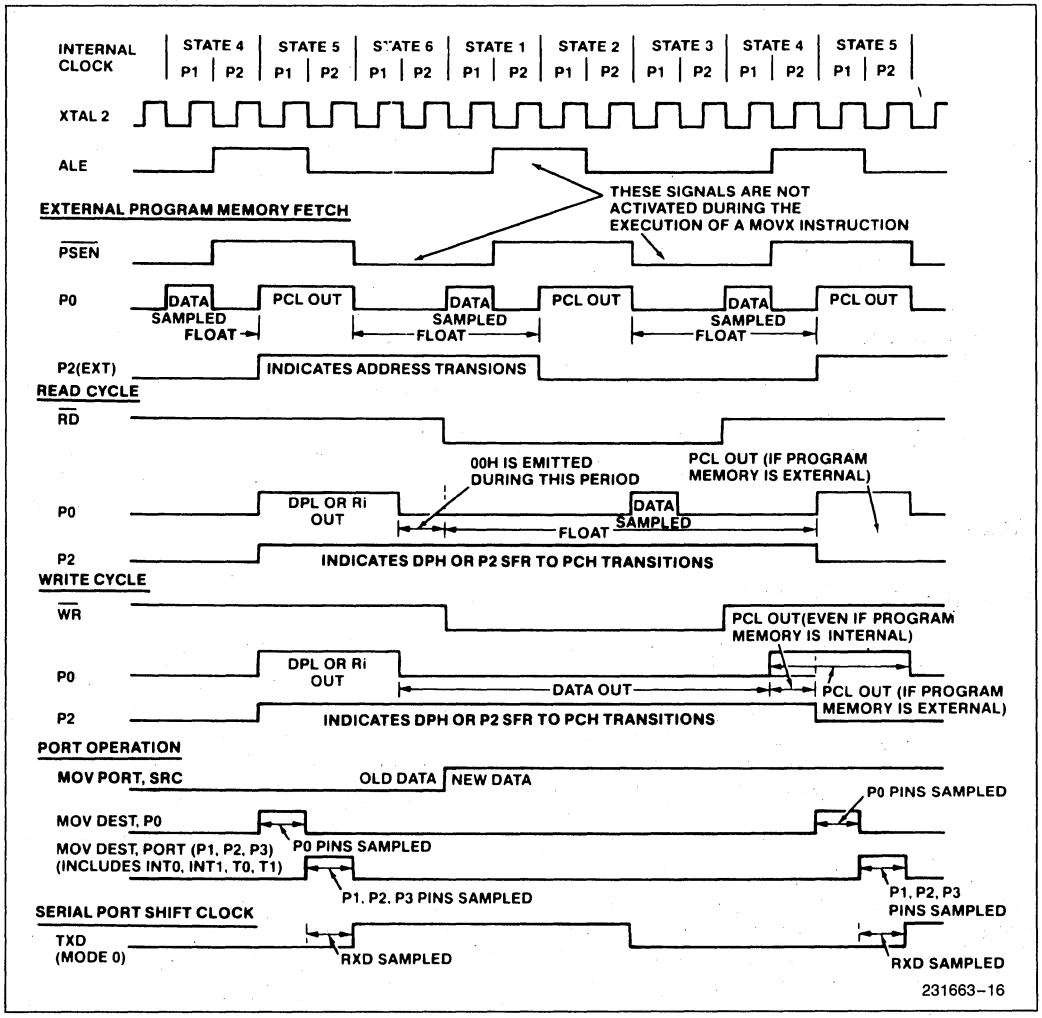
EXTERNAL CLOCK DRIVE XTAL2



231663-15

Symbol	Parameter	Variable Clock Freq = 3.5 MHz to 12 MHz		Unit
		Min	Max	
TCLCL	Oscillator Period	83.3	285.7	ns
TCHCX	High Time	20	TCLCL-TCLCX	ns
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though, (T_A = 25°C, fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

8744H EPROM CHARACTERISTICS

Erasure Characteristics

Erasure of the 8744H Program Memory begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Ångstroms. Since sunlight and fluorescent lighting have wavelengths in this range, constant exposure to these light sources over an extended period of time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause unintentional erasure. If an application subjects the 8744H to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Ångstroms) to an integrated dose of at least 15 W-sec/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1s state.

Programming the EPROM

To be programmed, the 8744H must be running with a 4 to 6 MHz oscillator. (The reason the oscillator needs to be running is that the internal bus is being used to transfer address and program data to appropriate registers.) The address of an EPROM location to be programmed is applied to Port 1 and pins P2.0-P2.3 of Port 2, while the data byte is applied to Port 0. Pins P2.4-P2.6 and $\overline{PSEN}$ should be held low, and P2.7 and RST high. (These are all TTL levels except RST, which requires 2.5V for high.) $\overline{EA}$/VPP is held normally high, and is pulsed to +21V. While EA/VPP is at 21V, the ALE/$\overline{PROG}$ pin, which is normally being held high, is pulsed low for 50 msec. Then EA/VPP is returned to high. This is illustrated in Figure 8. Detailed timing specifications are provided in the EPROM Programming and Verification Characteristics section of this data sheet.

Program Memory Security

The program memory security feature is developed around a "security bit" in the 8744H EPROM array. Once this "hidden bit" is programmed, electrical access to the contents of the entire program memory array becomes impossible. Activation of this feature is accomplished by programming the 8744H as described in "Programming the EPROM" with the exception that P2.6 is held at a TTL high rather than a TTL low. In addition, Port 1 and P2.0-P2.3 may be in any state. Figure 9 illustrates the security bit programming configuration. Deactivating the security feature, which again allows programmability of the EPROM, is accomplished by exposing the EPROM to ultraviolet light. This exposure, as described in "Erasure Characteristics," erases the entire EPROM array. Therefore, attempted retrieval of "protected code" results in its destruction.

Program Verification

Program Memory may be read only when the "security feature" has not been activated. Refer to Figure 10 for Program Verification setup. To read the Program Memory, the following procedure can be used. The unit must be running with a 4 to 6 MHz oscillator. The address of a Program Memory location to be read is applied to Port 1 and pins P2.0-P2.3 of Port 2. Pins P2.4-P2.6 and $\overline{PSEN}$ are held at TTL low, while the ALE/$\overline{PROG}$, RST, and $\overline{EA}$/VPP pins are held at TTL high. (These are all TTL levels except RST, which requires 2.5V for high.) Port 0 will be the data output lines. P2.7 can be used as a read strobe. While P2.7 is held high, the Port 0 pins float. When P2.7 is strobed low, the contents of the addressed location will appear at Port 0. External pullups (e.g., 10K) are required on Port 0 during program verification.

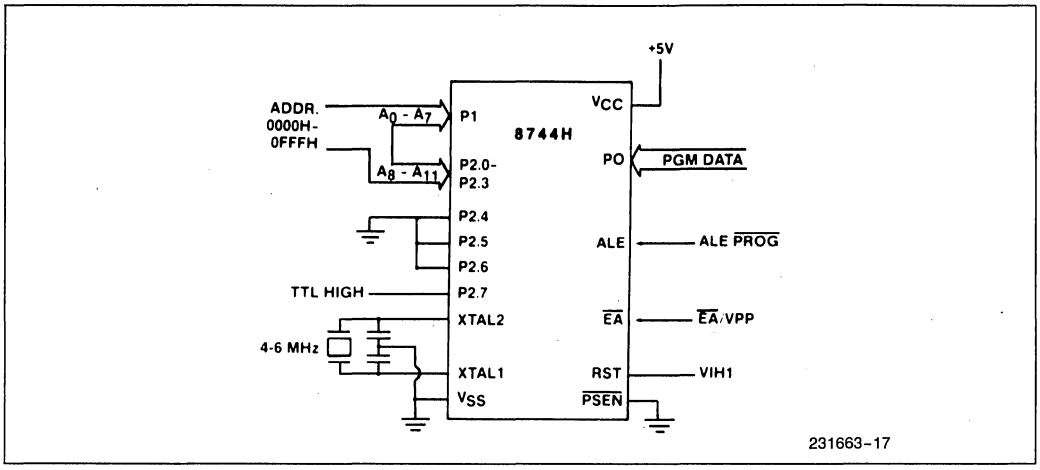


Figure 8. Programming Configuration

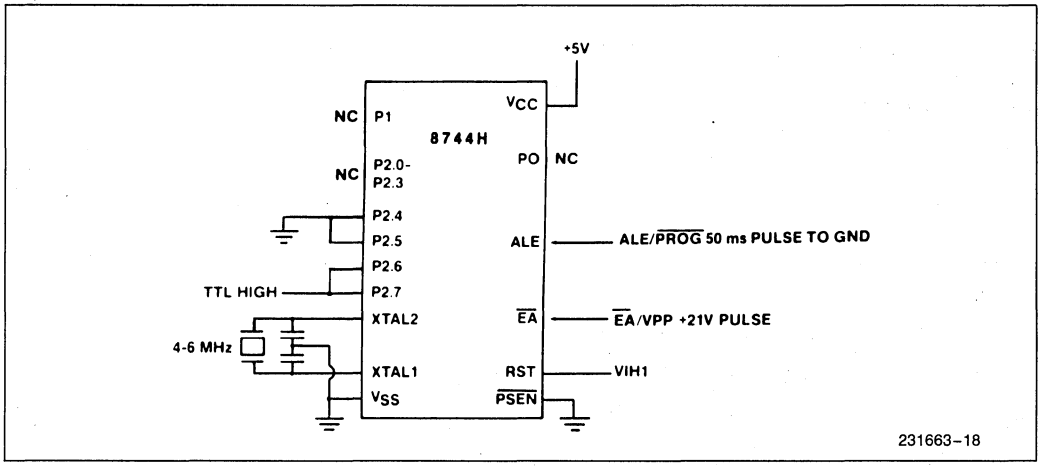


Figure 9. Security Bit Programming Configuration

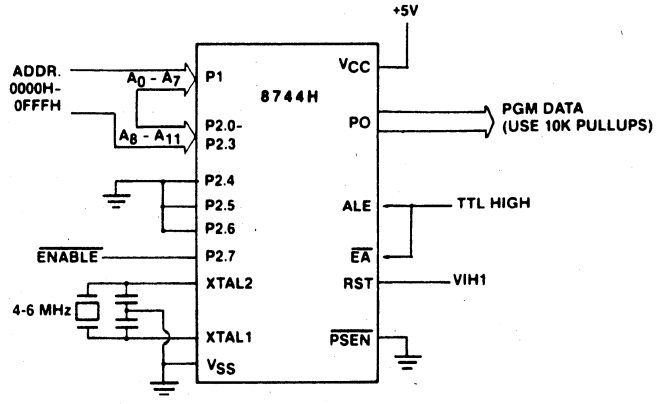


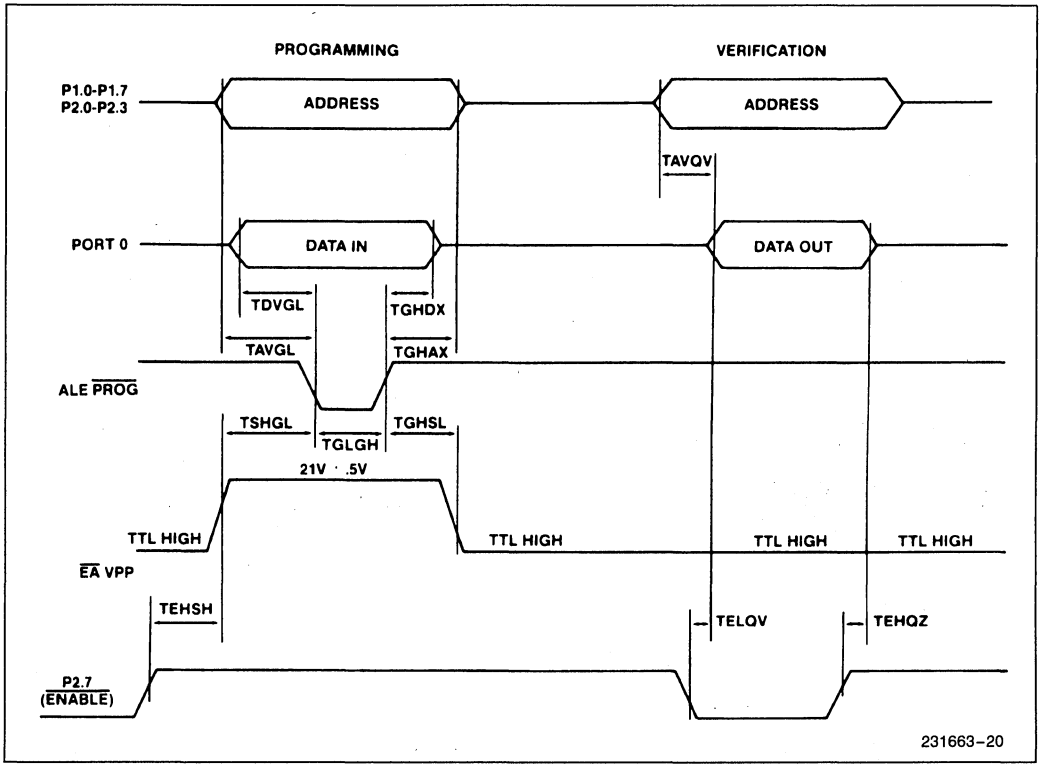
Figure 10. Program Verification Configuration

EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION CHARACTERISTICS

TA = 21°C to 27°C, V_{CC} = 4.5V to 5.5V, V_{SS} = 0V

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	20.5	21.5	V
IPP	Programming Current		30	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$	48TCLCL		
TGHAX	Address Hold after $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$	48TCLCL		
TGHDX	Data Hold after $\overline{PROG}$	48TCLCL		
TEHSH	$\overline{ENABLE}$ High to Vpp	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$	10		μsec
TGHSL	V_{PP} Hold after $\overline{PROG}$	10		μsec
TGLGH	$\overline{PROG}$ Width	45	55	msec
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ to Data Valid		48TCLCL	
TEHQZ	Data Float after $\overline{ENABLE}$	0	48TCLCL	

EPROM PROGRAMMING, SECURITY BIT PROGRAMMING AND VERIFICATION WAVEFORMS



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  - — Furnish a well documented source code and listing.
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  - — Assure validity by inclusion of a demonstration program.
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Program Order Form

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☐ Single Density ☐ Single Density ☐ Listing

☐ iPDS ☐ iPDS

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For Information Contact:

Catherine Moon
iRUG Coordinator
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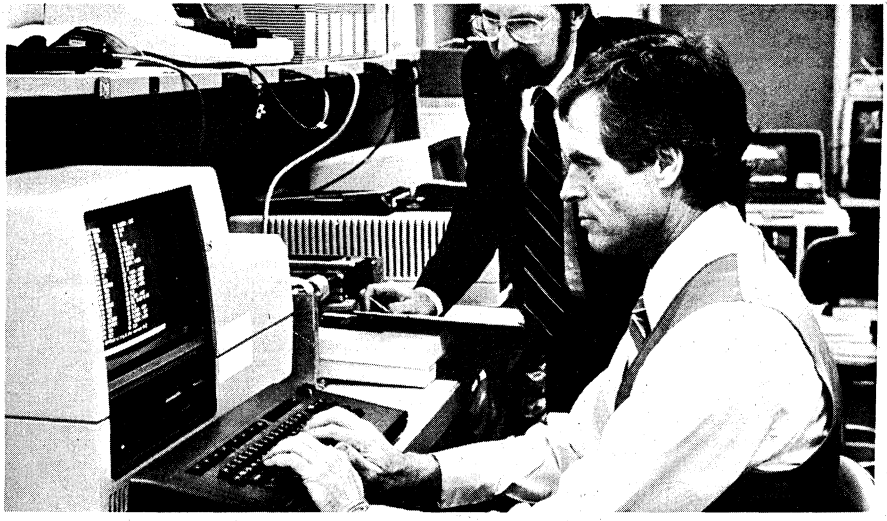

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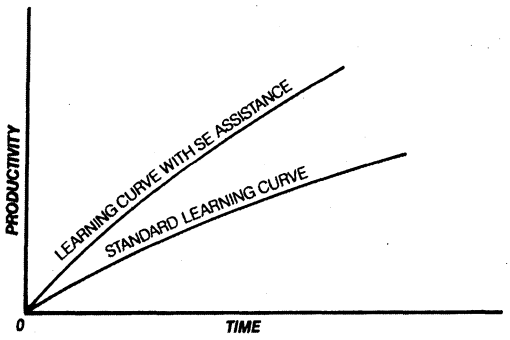

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80386 Programming Using ASM 386; 80386 System Software; 80386 Hardware Design; 80286 Microprocessors; 8086, 8088, 80186, 80188 Microprocessors Base Architecture; 8086, 8088, 80186, 80188 Advanced Microprocessors (including 8087); Introduction to Microprocessors; MCS™-80/85 Microprocessors; I2ICE User's Workshop; MCS™-51 Microcontrollers; MCS™-96 16-bit Microcontroller and Bitbus.

Operating Systems and Programming Workshops

PL/M Programming; iRMX® 86 Operating System Part 1; iRMX 86 Operating System Part 2; iRMX 286 Operating System; iRMX Application and Debug; Fundamentals of XENIX*; XENIX Shell Programming; XENIX System Administration; Introduction to C Programming; System Programming in C for XENIX and iDIS.

Local Area Networking Workshops

LAN Overview; Map-NET; iNA 960; LAN Applications/iRMX-NET and LAN Applications/XENIX-NET.

End-User Workshops

Office Automation/Introduction; Office Automation/Advanced; System Administration 1; System Administration 2; and Network Administration 1 (Local Area Networks and OpenNET™).

Training Locations And Dates

Workshops are offered nearly every week at Intel Training Centers. A Customer Training Workshop Catalog that details scheduled dates and locations of specific workshops is distributed twice a year. You may obtain your catalog from Intel's Literature Department, your nearest Intel Sales Office, or by calling your local Intel Training Center.

Workshop Options

Customer Site Workshops

Training workshops may also be held at your site. All instructional materials and laboratory equipment are brought in by Intel, together with a qualified Intel instructor to conduct the session.

Customer-Site Workshops offer the following benefits:

- Intensive, personalized training focused on your staff
- Adjustments to the courses/sessions to fit the backgrounds and needs of the participants
- Improved learning atmosphere as a result of co-workers training together and receiving quality, uniform instruction
- Convenience, because the class can be scheduled according to your needs.
- Cost-effectiveness, because more personnel can be trained at a lower cost per person.

Custom Workshops

Should you require a more customized workshop to meet a special need or fit a specific product line, we will tailor a program that will do the job for you efficiently and effectively. Such workshops may be conducted either in one of Intel's Training Centers or on-site at your facility.

Intel's Introduction to Microprocessors course is available in a self-paced instruction kit (as well as in publicly held classes).

Workshop Tuition

Standard Tuition

This basic package fee includes course notebook, literature and materials (such as the SDK-85 kit for the Introduction to Microprocessors Workshop).

Group Rate Tuition

When an organization enrolls three or more individuals in the same workshop (held on the same date in the same location) the company becomes eligible for a special group rate and a savings on the overall cost of tuition. To receive the discount, three individuals must attend the class.

Enrollment Information

Call the Intel Training Center nearest you between 8:30-12:00 and 1:00-4:30. Since enrollment is limited, registration 4-8 weeks in advance is recommended. A confirmation letter will be issued upon registration, which guarantees enrollment.

Worldwide Training Centers

Boston
Three Carlisle Road
First Floor
Westford, MA 01866
(617) 692-1000

Chicago
300 N. Martingale Road
Suite 300
Schaumburg, IL 60173
(312) 310-5700

Los Angeles
Call Santa Clara
(408) 970-1700

Santa Clara
2700 San Tomas Expressway
Santa Clara, CA 95051
(408) 970-1700
TWX 910-379-5082

Washington, D.C. Area
7833 Walker Drive
Fourth Floor
Greenbelt, MD 20770
(301) 220-3380
TWX 910-997-0428

Copenhagen
Glentevej 61—3rd Floor
DK-2400 Copenhagen
(01) 19 80 33
Telex 19567

Hong Kong
1701-3 Connaught Centre
1 Connaught Road, Central
5-2153117
Telex 60410 ITLHK HX

Milan
Milanofiori Palazzo E/3
20090 Assago, Milan, Italy
39-2-82-44-071

Munich
Nymphenburger Strass I/III
8000 Muenchen 2, West Germany
(089) 5389-0
Telex 523177

Osaka
Ryokuchi-Eki Building
2-4-1, Terauchi
Toyonaka-shi, Osaka, Japan
03-437-6611

Paris
1 Rue Edison
B.P. 303
78504 St. Quentin-en-Yvelines
Paris, France
30-57-7000
Telex 270475

Rotterdam
Marten Meesweg 93
3068 Av Rotterdam
The Netherlands
(10) 21.23.77
Telex 22283

Stockholm
Dalvagen 24
S-171 36 Solna, Sweden
(468) 734-01-00

Swindon
Units F & G
Dorcan Complex
Faraday Road
Swindon, Wiltshire, England
793-696-000
Telex 44447

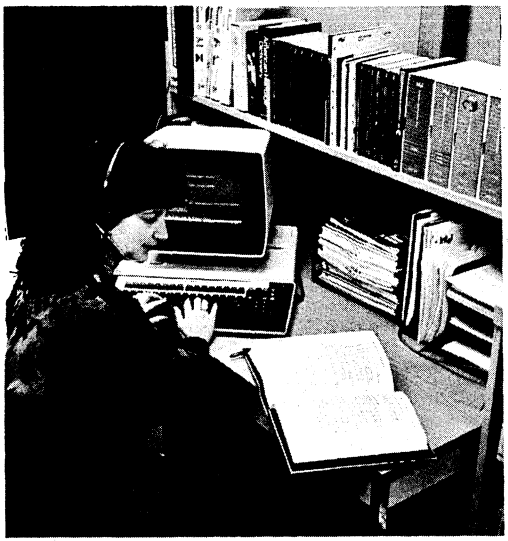
Tel Aviv
Atidim Industrial Park
Neve Sharet, Dvora Havevia
Tel Aviv 61430
3-491099

Tokyo
Matsuoka-Tamura-cho Bldg.
22-10, 5-chome, Shinbashi
Minato-ku, Tokyo, 105 Japan
03-437-6611

Toronto
Call Boston
(617) 692-1000
Telex (710) 343-6333

*XENIX is a trademark of Microsoft Corporation.

- ☐ ***Comprehensive software support to address your most frequent questions***
- ☐ ***Two levels of support: Standard Service or Basic Service***
- ☐ ***Updates ensure that you have the latest released version of Intel software, manuals and documentation for all covered products as they are released***
- ☐ ***Users kept up to date with regularly published software data***
- ☐ ***Direct telephone access to Intel's trained Software Support staff to help isolate and resolve problems***



Most Commonly Requested Support Services For An Easy-To-Budget Monthly Charge

STANDARD SERVICE

TIP SERVICE	BASIC SERVICE
UPDATES	UPDATES
SUBSCRIPTIONS	SUBSCRIPTIONS

Intel's Software Support Service provides updates, manuals and documentation for covered products as released; Intel's ;COMMENTS technical newsletter; product-specific technical reports; written responses to customer inquiries under our Software Problem Reporting (SPR) Service; and access to TIP Service phone support.

Packaged in a convenient "environment" form, the Standard and Basic Software Contracts cover all supported software products that run in a particular environment.

Additional software products purchased at a later date which run in the covered environment may be added at no extra charge by simply registering the product.

A basic monthly fee is set for the first system covered. All additional systems are covered at a reduced rate per system. You are entitled to updates and subscriptions equivalent to the total number of systems covered under the contract.

Standard level service includes TIP support, for two callers for each system covered under the contract.

Contracts have a minimum one-year term and continue in force until cancelled with 30 days' written notice.

TIP Service Provides Telephone Access To Trained Software Engineers

TIP Service is a product-specific telephone information service designed to address time-critical product inquiries by providing direct access to Intel's trained Software Engineering staff. This direct response mechanism aids in obtaining maximum utilization of your Intel software products. TIP Service provides a timely response to those time-critical product questions that could not be answered by the product documentation, the Software Problem Reporting Service or the regularly published Technical Reports.

The two designated callers will have, by phone, direct access to Intel's trained Software Engineering staff within Intel's Central Customer Support Center during normal working hours (7:00 a.m. to 6:00 p.m. MST).

When you call TIP Service, the receptionist will initiate a numbered Incident Report and provide you with this assigned number for future reference. At this point, you will be able to speak with a member of Intel's Software Engineering staff. If one is not immediately available, the call will be returned within two hours.

Any new symptom, problem or work-around identified by you or the Software Engineer is added to the Software Problem Report (SPR) Service for future reference and incorporated into the appropriate Troubleshooting Guide.

Upon conclusion of the incident, the Incident Report is closed and permanently logged and filed.

Software Engineers Help Isolate And Solve Problems

Intel's Software Engineering staff is a group specifically established to provide the following services to users of Intel software and system products:

- Centralized access to Intel's engineering and support resources
- The latest technical information on Intel defined and documented product problems and deficiencies, and their associated work-arounds, temporary fixes, patches or other solutions
- Technical assistance in isolating the cause or source of a suspected product problem
- A central Software Problem Reporting (SPR) Service

Updates Ensure That You Have The Latest Released Version Of Any Intel Software

Under the terms of the contract, Intel will provide manuals, documentation, diskettes or other media of your choice for all covered updates as they are released.

When you obtain contractual coverage for your Intel software products, you must designate a primary and a secondary person for Intel to contact. Intel will send a software registration packet that will allow Intel to verify that the software to be supported is at the current release level. Intel will then record the returned information and assemble and mail any required updates, manuals and supporting documentation to the designated contact.

Subscription Service Keeps You Up-To-Date And Up-To-Speed

Intel's Subscription Service is an efficient communications mechanism intended to provide you with the latest Intel software and system product data, as well as information regarding product and documentation inconsistencies.

It is also a mechanism to enable you to report suspected product problems to Intel's engineering organization.

Subscription Service includes:

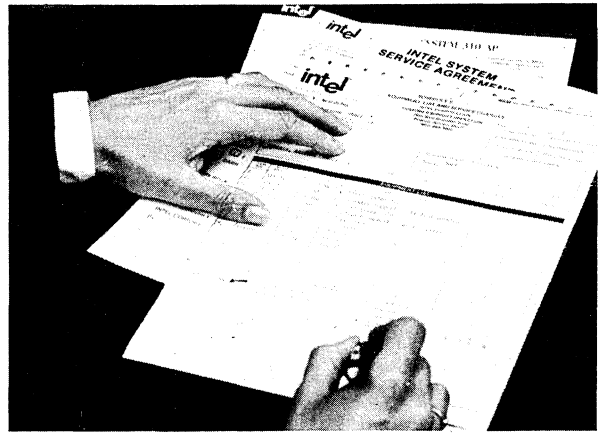
- ;COMMENTS—a technical bulletin which contains operational tips, programming techniques and other technical information.
- Troubleshooting Guides—technical information regarding current software problems, interim programming solutions and application articles. Published periodically, by product or product family.
- Software Problem Reporting (SPR) Service is a written communications vehicle for you to use to inquire about or to report suspected product problems, or to suggest product improvements. All Software Problem Reports (SPRs) are reviewed by a member of the Software Support Staff, and are answered in writing as quickly and completely as possible.

Ordering Information

Software support contracts are placed in effect by completing an Intel System Service Agreement. Eligible contract environments are listed in the current Intel price book.

Contact your local Intel Sales or Service Office to sign up for support.

- ☐ ***Backed by a 15-year service organization***
- ☐ ***Comprehensive hardware support options that include all necessary parts, labor and installation of engineering changes***
- ☐ ***Personalized attention from your Intel Customer Engineer***
- ☐ ***Extended coverage options to provide you support up to seven days per week and twenty-four hours per day***
- ☐ ***Preferential, priority dispatch of your Customer Engineer to your site***



Comprehensive Hardware Support Options

Intel's Customer Support Operation is an International Organization with the expertise and resources to provide on-site service on a worldwide basis.

Intel's Standard Hardware Maintenance Service is designed to keep your system running at maximum efficiency. Intel provides remedial maintenance, preventive maintenance and parts replacement, or exchange for a fixed amount. The contract includes all parts and labor during the contract hours selected at your site.

Maintenance charges are based on individual contracts, subject to applicable zoning policies and optional parts and coverage. It is recommended that all interconnected products be included in the maintenance agreement. Extended Service coverage and installation are also available.

Intel utilizes a sophisticated Central Dispatch System that promptly dispatches personnel, monitors call progress and tracks each piece of equipment you have under contract. During emergency calls you are protected by the automatic problem escalation system. Central dispatch closely monitors the situation and will escalate problems to the appropriate management and technical people. The system maintains a complete history file on each piece of equipment under contract. This assures you that the equipment will be maintained at the highest level with engineering change orders and appropriate spares stocked locally.

Preventive Maintenance Avoids Problems

Intel's Preventive Maintenance (PM) programs are designed to increase your system availability by identifying potential problems before a malfunction occurs. Your assigned Customer Engineer not only performs the preventive maintenance specified by Intel or the original manufacturer, but also will augment the service with personal experience with your products and applications. The PM services include reviewing performance, history of the equipment, executing the diagnostics to identify potential problems, making any necessary electronic and mechanical adjustments and replacing any worn or defective parts as required.

Remedial Maintenance Receives Priority

If unscheduled maintenance becomes necessary, the assigned Customer Engineer will be on-site within the contracted response time. The Customer Engineer will call the same day of your request for service to discuss the symptoms observed, ensuring that all logistical items are available to resolve the problem. Verification of the equipment being back in service will be accomplished by executing diagnostics. The Customer Engineer will then update the device history file with the corrective action taken.

Engineering Changes Installed At No Extra Cost

Assuring you of the latest engineering improvements is a standard feature of Intel Standard Hardware Maintenance Service. The changes ensure not only that the equipment operates at the highest standards but has continued compatibility with Intel supplied software and replacement parts. Engineering changes are installed during a preventive or remedial maintenance call.

Service Specifications And Options

Term

Maintenance agreements are written for a minimum of a one-year term and continue month to month thereafter until cancelled by either party with 30 days' notice.

Standard billing is monthly but flexible options are available.

Period of Coverage

9/5—9 continuous hours between the hours of 7:00 a.m. to 6:00 p.m., Monday through Friday, excluding local Intel holidays.

16/5—16 continuous hours between the hours of 7:00 a.m. to 12:00 Midnight, Monday through Friday, excluding local Intel holidays.

24/5—24 hour coverage commencing 7:00 a.m., Monday through 7:00 a.m. Saturday, excluding local Intel holidays.

24/7—24 hours coverage, 7 days a week, excluding local Intel holidays.

Maintenance Price Grid:

9/5	16/5	24/5	24/7
Standard	11%	130%	150%

Maintenance Service Response Time/Cost Grid

The time/cost grid for maintenance agreement coverage lists the available response time within service zones. As equipment location moves farther in distance from the service center, response times are extended and contract coverage cost increases by the percentage quoted below the response time. For response time of less than 8 hours or distance greater than 150 miles, contact your local Field Service Office.

Parts

Maintenance parts required for on-site service will be furnished by Intel on an exchange basis; replaced parts become the property of Intel.

Ordering Information

Contact your local Intel Field Sales or Service Office.

Class	*0-50 mi*	*51-100 mi*	*101-150 mi*	*Comments*
Standard	8-hr response	16-hr response	24-hr response	On-site
	100%	125%	150%	

intel

SOFTWARE SUPPORT SERVICES
PC-DOS*

- **Comprehensive software support to address your most frequent questions**
- **Unlimited telephone access for problem resolution**
- **Packaged by architecture for greater flexibility**
- **Substantially reduced rates for updates**

Most Commonly Requested Support Services

Intel's Software Support Service provides comprehensive coverage for all Intel products running on your PC-DOS based system. Six packages defined by architecture provide flexibility so that you only purchase the package you need. Benefits of Software Support Service include: access to unlimited telephone support (TIPS), subscription to ; **COMMENTS** monthly newsletter, product specific technical reports, written responses to software problem inquiries, updates at greatly reduced prices, and Insite Library Membership.

Packaged in a kit form, the standard contract covers all supported products that run under a particular architecture. Additional software products purchased at a later date which run in the covered architecture may be added at no extra charge by simply registering the product.

The monthly fee is set for each system covered. You are entitled to subscriptions and to purchase updates equivalent to the total number of systems covered under your contract. Contracts have a minimum one-year term and continue in force until cancelled with 30 days' written notice.

For networked PCs, a substantial discount in the form of a price cap is offered. (Support of the network itself is covered under a separate environment.)

TIPS Service Provides Telephone Access To Trained Software Engineers

TIPS Service is a product specific telephone information service designed to address time-critical product inquiries by providing access to Intel's trained Software Engineering (SE) staff. This response mechanism aids in obtaining maximum utilization of your Intel software products for those product questions that could not be answered by product documentation, the Software Problem Reporting Service, or the regularly published Technical Reports.

Two designated callers will have direct access to Intel's Central Customer Support center during normal working hours (8:00 a.m. to 5:00 p.m. MST). When you call our toll free number, the dispatcher will initiate a numbered Incident Report and provide you with this number for future reference. A software engineer will return your call within one hour.

Support includes verification of the reported bug and providing work-arounds on a best efforts basis. Any new symptom, problem, or work-around identified by you or the Software Engineer is added to our software problem data base and incorporated into the appropriate Troubleshooting Guide for future reference. Upon conclusion of the incident, it is closed and permanently logged and filed.

Telephone support will be provided for down-rev products for six months following the first release of its successor on the same host. Support includes verifying the reported bug in the down-rev product and providing a work-around, on a best efforts basis. If the bug appears in the current product, TIPS will provide any known work-around first and will attempt to find a work-around with the down-rev product second.

Subscription Service Keeps You Up-To-Date and Up-To-Speed

Intel's Subscription Service is an efficient communications mechanism intended to provide you with the latest Intel software and system product data, as well as information regarding product and documentation inconsistencies. It is also a mechanism to enable you to report suspected product problems to Intel's engineering organization.

Subscription Service includes:

- ; **COMMENTS** - a monthly technical bulletin which contains operational tips, programming techniques, and other technical information.
- Troubleshooting Guides - technical information regarding current software problems and interim programming solutions.
- Software Problem Reporting Service - a written communications vehicle for you to use to inquire about or report suspected product problems. All SPRs are answered in writing as quickly and completely as possible.
- Insite Library Membership - includes programs submitted by users of Intel products.

Updates Ensure That You Have The Latest Released Version of Any Intel Software

Under the terms of the contract, Intel will offer manuals, documentation, diskettes or other media of your choice for all covered updates as they are released, at a substantial reduction from individual update prices.

*PC-DOS is a trademark of Microsoft Corporation

March 1988
Order Number: 270589-001

SERVICE SPECIFICATIONS AND OPTIONS

Terms

Maintenance agreements are written for a minimum of one year and continue month to month thereafter until cancelled by either party with a 30 days' written notice.

Period of Coverage

8:00 a.m. - 5:00 p.m. (MST) excluding weekends and Intel holidays

Product Codes

SSCD51KIT . . . . . Applies to DOS hosted products targeted to 8051 Architecture

SSCD96KIT . . . . . Applies to DOS hosted products targeted to 8096 Architecture

SSCD86KIT . . . . . Applies to DOS hosted products targeted to 8086/80186 Architecture

SSCD286KIT . . . . . Applies to DOS hosted products targeted to 80286 Architecture

SSCD386KIT . . . . . Applies to DOS hosted products targeted to 80386 Architecture

SSCD700KIT . . . . . Applies to DOS hosted products targeted to all Architectures

A current listing of products covered in each kit appears in the Intel Product Catalog and ; **COMMENTS** magazine.

■ Ordering Information

Software Support Contracts are placed in effect by completing an Intel System Service Agreement. Contact your local Intel Sales or Service Office to sign up for support, or simply call 1-800-INTEL 4 U. Once your products are registered, support will begin immediately.

NETWORK SERVICES

- **One-stop shopping for your network**
- **Complete physical and logical network design**
- **Network installation management**
- **Network user and administrator training**
- **Worldwide service and support**

One-stop Shopping

As part of the commitment to meet your total networking needs, Intel offers a full set of services to provide you with convenient one-stop shopping for all your networking requirements. This provides a single point of responsibility for installation of your network and frees your resources to concentrate on your specific applications.

Complete Network Design

Today's networking products are powerful and extremely flexible. The return they can provide on your investment via increased productivity and reduced costs can be very substantial. However, in order to obtain both maximum equipment utilization and user productivity, they need to be custom configured to your specific organizational and usage requirements. Whether installing your first network or adding to an existing one, Intel's Networking Specialist can perform this design service for you.

Physical Network Design: When planning and designing the physical layout of a network, issues such as type of building, local fire and building codes, adherence to various specifications (e.g., Ethernet, IEEE, RS232) must be taken into consideration. Intel's Physical Network Design Service can provide this for you. In addition to the most efficient cable routing and recommendation of the most reliable components, a complete bill of materials and cost information for the physical network is produced.

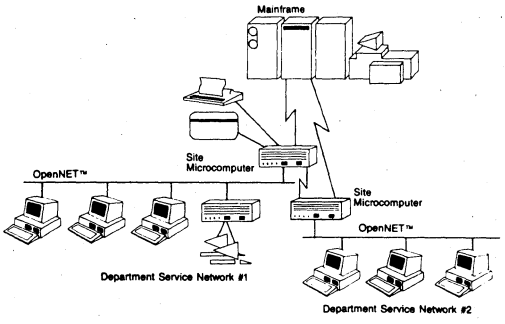
Logical Network Design: Because every organization is unique and has its own set of requirements, the network that serves it must be logically designed and configured to meet these requirements. Just as there is no generic data base design, there is no generic network design. Issues such as the most efficient use of file and print servers, host communication servers, network security, and system and network administration must be taken into consideration. An Intel Networking Specialist will interview your users to understand their requirements and then logically design the network to meet those requirements. This Logical Network Design Service produces the software "blueprint" to be used by the network installers and ensures immediate use of your network upon completion of its installation.

Network Installation Management

Once the physical and logical design of your network has been completed and agreed upon, the implementation phase begins. An Intel team will manage the installation of the physical network, set up and install all nodes, and install and configure all software according to the logical design "blueprint" produced as a result of the Logical Network Design Service. Before the installation team leaves, they will ensure that your network is fully operational.

Network User and Administrator Training

Just as the design of the network is critical to its maximum utilization and productivity so is the proper training of your users. Intel's Customer Training provides a comprehensive selection of courses for both your end users and network administrators. By training your staff in parallel with network installation, they will be in a position to start using the network immediately upon its installation.



June 1987
Order Number: 270309-02

■ Worldwide Service and Support

Because a network can be equated to a large multiuser mainframe, ensuring maximum network uptime, operational efficiency and timely repair is extremely important. Intel's Customer Service provides a full range of network maintenance services that can be tailored to meet your specific needs. Among these are Software Support which includes free updates to all Software, and Hardware Maintenance of all system nodes, PCs and attached peripherals as well as the network "backbone" cable, transceivers, transceiver cables, connectors and repeaters. In the event of network problems, Intel's Customer Service personnel are equipped with proprietary software diagnostic tools which help to locate and analyze any problems quickly. These same tools can also be used to conduct a periodic performance "tune up" of your network. Options as to level of service, response time and hours of coverage are also available.

Over 865 trained professionals in 80 service locations are dedicated to providing you with top quality, world class service.

■ Custom Network Management Services

If you have a large network installation, Intel's team of Network Specialists can put together a custom proposal that will provide a wide range of Network Management Services to meet your specific needs. These include, but are not limited to, the following:

- Network administration
- Coordination and administration of customer user groups
- On-site first level support
- Node relocation management
- Consulting and application development

PC AT 386 CONVERSION

- **Converts an IBM* PC AT to a 386 PC**
- **2-3 times faster software execution**
- **Retains compatibility with AT**
- **Conversion done at your site by Intel**
- **Converted AT covered by one-year warranty**
- **Includes high-speed math coprocessor**

The Way to Grow

Intel's PC AT 386 Conversion provides the answer for PC power users who need to grow but want to retain their PC AT investment. It is a complete package of hardware and service that converts IBM PC ATs into 386 PCs fully compatible with the original PCs. The advantages include:

- Applications run 2-3 times faster
- Quality service on the converted PCs
- Compatible with current and future PC AT software and hardware
- Up to 16MB of 32-bit memory can be added to the system

Intel Does Conversion

The conversion replaces the AT's base board with Intel's 386 AT Base Board. This simple, fast procedure exchanges the PC's original 80286 microprocessor for an 80386. It also switches the original 16-bit base memory for more efficient 32-bit base memory and adds connectors for expanding 32-bit memory to 16MB.

All conversions will be done at your site by an Intel Customer Engineer experienced with servicing PC ATs. For volume conversions, Intel will plan the process with you to minimize disruption.

80386 Power Means Fast Execution

The 80386 microprocessor installed in each converted PC runs at a fast 16MHz. That's between two and three times faster than the PC AT's 80286 microprocessor. Whatever you run on your PCs — spreadsheets, CAD packages, database programs, compilers — executes 2-3 times faster. The time you used to wait for your PC to catch up with you can now be spent more productively.

Compatibility Retains Your Investment

The 80386 is the most advanced member of the Intel family of microprocessors that have powered IBM's PCs. The 80386 can execute virtually all software written for the PC, PC XT, and PC AT. It just does so faster.

The 386 AT Base Board extends that compatibility by duplicating the functions of the PC AT's base board. Your expansion cards and the rest of the PC AT system work with the new 386 AT Base Board as they did with the original. Most importantly, the data on your hard disk remains unchanged.

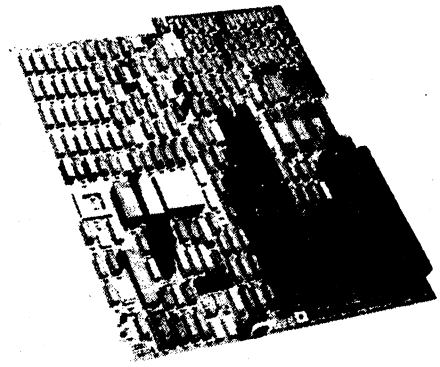
Intel Warrants the Converted 386 PC

Intel knows that reliable operation remains as important after the conversion as it was before. To ensure a minimum of down time, Intel provides a one-year, on-site warranty for the converted IBM PC AT, not just for the converted base board. The warranty is backed by an organization that has 15 years' experience servicing computers from over 80 locations worldwide.

The warranty covers the 386 AT Base Board plus the AT's original basic hardware (Model 5170):

- 386 AT Base Board
- Power supply
- Disk controller
- Winchester disk drive (20 or 30MB)
- Floppy disk drive (360KB or 1.2MB)
- Keyboard
- IBM Monitor
- IBM Color Graphics Adapter

Additional items such as many popular expansion cards and peripherals can be covered at an additional cost.



* IBM is a registered trademark of International Business Machines Corporation

June 1987
Order Number: 270301-02

■ 386 AT Base Board Specifications

- Compatible with IBM PC AT base board including BIOS compatibility
- 16MHz 80386 microprocessor; switchable to 6MHz with keyboard command
- 10MHz 80287 Math Coprocessor installed
- 512KB of 32-bit memory installed on Base Board
- Two connections for 32-bit memory expansion
- Two PC-compatible 8-bit bus slots and four PC AT-compatible 16-bit bus slots

■ 32-Bit Memory Expansion

Up to 16MB of 32-bit memory can be added to the system in increments of 2 or 16 megabytes by adding Intel 386 PC memory boards to the 386 AT Base Board's 32-bit memory expansion connectors.

ORDERING INFORMATION

386 AT Conversion Kits

All conversion packages include Intel's 386 AT Base Board, 287 math coprocessor, installation, and warranty. (See restrictions on installation and warranty below.) Packages differ only in the amount of additional 32-bit memory above the base 512KB.

Minimum order is 50 conversions.

Order Code	Total 32-Bit Memory	Expected Availability
386ATCON	0.5MB	Now
386ATCON2M	2.5MB	Now
386ATCON4M	4.5MB	Now
386ATCON8M	8.5MB	mid-1987

Add-on 32-bit Memory

Installation not included unless ordered as part of the original conversion. These boards work only with the 386 AT Base Board.

Order Code	Description	Expected Availability
386AT2MB	32-bit 2MB memory board*	Now
386AT8MB	32-bit 8MB memory board*	mid-1987

Restrictions

1. Installation and warranty of converted PC and on-site service not available in certain areas. Mail-in warranty on boards sold by Intel available in these areas.

2. Warranty on converted PC not available unless conversion done by Intel. Mail-in warranty on boards sold by Intel available for customers who do their own conversion.

* Can be used only with the 80386 Base Board

PC AND PERIPHERAL HARDWARE MAINTENANCE

- **On-site hardware maintenance service**
- **One-stop shopping for maintenance on IBM* and other major brand personal computers and peripherals**
- **Includes all parts and labor required for remedial and preventive maintenance**
- **Fixed budgetable monthly maintenance fee**
- **Personalized attention from a Customer Engineer**
- **Professional maintenance management ensuring prompt problem resolution**
- **Extended coverage options to meet your support needs**
- **Priority service and response above those who are not on contract**

Comprehensive Maintenance Support

Intel's Customer Support is an international organization with the expertise and resources to provide on-site service on a worldwide basis.

Intel's PC and Peripheral Hardware Maintenance service is designed to keep your system running at maximum efficiency. Intel provides remedial maintenance, preventive maintenance and parts replacement or exchange for a fixed amount at your site. All parts and labor during the contract hours selected are included.

Maintenance charges are based on individual customer services, subject to applicable zoning policies and optional parts and coverage. It is recommended that all interconnected products be included in the maintenance agreement. Extended service coverage and installation are also available.

Intel utilizes a sophisticated Central Dispatch System to efficiently dispatch personnel for fast response.

As an Intel customer you receive automatic problem escalation protection. The Central Dispatch System allows for close monitoring of service requests and call status. Close monitoring assures you that any discrepancy will be escalated through the technical and management structures to mobilize the necessary resources. Intel's problem escalation protection is designed to keep your business operating smoothly.

Preventive Maintenance Avoids Problems

Intel's Preventive Maintenance (PM) programs are specifically designed to identify potential problems before malfunctions occur, thus providing increased system availability. Your assigned Customer Engineers not only perform the preventive maintenance specified by Intel and/or the equipment manufacturer, but will augment the service with personal experience with your products and applications. The PM services include reviewing performance, maintaining a history of the equipment, executing the diagnostics to sequentially identify potential problems, making any necessary electronic and mechanical adjustments and replacing any worn or defective parts as required.

Remedial Maintenance Receives Priority

If unscheduled maintenance becomes necessary, the assigned Customer Engineer will be on-site within the response time and coverage contracted for. The Customer Engineer will call the same day of your request for service to discuss the symptoms observed, ensuring that all logistical items are available to correctly resolve the problem. Verification of the equipment being back in service will be accomplished by executing diagnostics. The Customer Engineer will then update the device history file with the corrective action taken.

* IBM is a registered trademark of International Business Machines Corporation.

March 1987
Order Number: 270302-01

SERVICE SPECIFICATIONS AND OPTIONS

Terms

Maintenance agreements are written for a minimum of one year and continue month to month thereafter until cancelled by either party with 30 days' notice.

Standard billing is monthly, but flexible options are available.

Period of Coverage

9/5 - 9 continuous hours between 7:00 A.M. and 6:00 P.M., Monday through Friday, excluding local Intel holidays.

16/5 - 16 continuous hours between 7:00 A.M. and 12:00 Midnight, Monday through Friday, excluding local Intel holidays.

24/5 - 24 hours of coverage commencing 7:00 A.M. Monday through 7:00 A.M. Saturday, excluding local Intel holidays.

24/7 - 24 hours of coverage 7 days a week, excluding local Intel holidays.

Maintenance Price Grid

9/5	16/5	24/5	24/7
Base	115%	130%	150%

Maintenance Service Response Time/Cost

The time/cost grid below for maintenance agreement coverage shows the available response time within service zones. As equipment location moves further in distance from the service center, response times are extended and contract coverage cost increases by the percentage quoted below the response time.

Response Time/Cost

Zone 1 0 - 50 miles	Zone 2 51 - 100 miles	Zone 3 101 - 150 miles
4 contract hours 100%	8 contract hours 120%	8 contract hours 140%

Parts

Maintenance parts required for on-site service will be furnished by Intel on an exchange basis; replaced parts become the property of Intel.

OEM Boards and Systems Handbook

PRODUCT LIST SUPPLEMENT

Order Number: 280689-001

Any of the following products may appear in this publication. If so, it must be noted that such products have counterparts manufactured by Intel Puerto Rico, Inc., Intel Puerto Rico II, Inc., and/or Intel Singapore, Ltd. The product codes/part numbers of these counterpart products are listed below next to the corresponding Intel Corporation product codes/part numbers.

Intel Corporation Product Codes/ Part Numbers	Intel Puerto Rico, Inc. Intel Puerto Rico II, Inc. Product Codes/ Part Numbers	Intel Singapore, Ltd. Product Codes/ Part Numbers
376SKIT	p376SKIT	
903	p903	
904	p904	
913	p913	
914	p914	
923	p923	
924	p924	
952	p952	
953	p953	
954	p954	
ADAICE	pADAICE	
B386M1	pB386M1	
B386M2	pB386M2	
B386M4	pB386M4	
B386M8	pB386M8	
C044KIT	pC044KIT	
C252KIT	pC252KIT	
C28	pC28	
C32	pC32	
C452KIT	pC452KIT	
D86ASM	pD86ASM	
D86C86	pD86C86	
D86EDI	pD86EDI	
DCM9111	pDCM9111	
DOSNET	pDOSNET	
F1	pF1	
GUPILOGICIID	pGUPILOGICIID	
H4	pH4	
I044	pI044	
I252KIT	pI252KIT	
I452KIT	pI452KIT	
I86ASM	pI86ASM	
ICE386	pICE386	
III010	pIII010	
III086	pIII086	
III086	TIII086	
III111	pIII111	
III186	pIII186	
III186	TIII186	
III198	pIII198	
III212	pIII212	
III286	pIII286	
III286	TIII286	
III515	pIII515	
III520	TIII520	
III520	pIII520	
III531	pIII531	
III532	pIII532	
III533	pIII533	
III621	pIII621	
III707	pIII707	
III707	TIII707	
III815	pIII815	
INA961	pINA961	
IPAT86	pIPAT86	
KAS	pKAS	
KC	pKC	
KH	pKH	
KM1	pKM1	

Intel Corporation Product Codes/ Part Numbers	Intel Puerto Rico, Inc. Intel Puerto Rico II, Inc. Product Codes/ Part Numbers	Intel Singapore, Ltd. Product Codes/ Part Numbers
KM2	pKM2	
KM4	pKM4	
KM8	pKM8	
KNLAN	pKNLAN	
KT60	pKT60	
KW140	pKW140	
KW40	pKW40	
KW80	pKW80	
M1	pM1	
M2	pM2	
M4	pM4	
M8	pM8	
MDS610	pMDS610	
MDX3015	pMDX3015	
MDX3015	pMDX3015	
MDX3016	pMDX3016	
MDX3016	pMDX3016	
MDX457	pMDX457	
MDX457	pMDX457	
MDX458	pMDX458	
MDX458	pMDX458	
MSA96	pMSA96	
NLAN	pNLAN	
PCLINK		sPCLINK
PCX344A	pPCX344A	
R286ASM	pR286ASM	
R286EDI	pR286EDI	
R286PLM	pR286PLM	
R286SSC	pR286SSC	
R86FOR	pR86FOR	
RCB4410		sRCB4410
RCX920	pRCX920	
RMX286	pRMX286	
RMXNET	pRMXNET	
S301	pS301	
S386	pS386	
SBC010	pSBC010	
SBC012	pSBC012	sSBC012
SBC020	pSBC020	
SBC028	pSBC028	
SBC040	pSBC040	
SBC056	pSBC056	
SBC108	pSBC108	
SBC116	pSBC116	
SBC18603	pSBC18603	sSBC18603
SBC186410	pSBC186410	
SBC18651	pSBC18651	sSBC18651
SBC186530	pSBC186530	
SBC18678	pSBC18678	
SBC18848	pSBC18848	sSBC18848
SBC18856	pSBC18856	sSBC18856
SBC208	pSBC208	sSBC208
SBC214	pSBC214	
SBC215	pSBC215	
SBC220	pSBC220	sSBC220
SBC221	pSBC221	
SBC28610	pSBC28610	sSBC28610
SBC28612	pSBC28612	
SBC28614	pSBC28614	

Intel Corporation Product Codes/ Part Numbers	Intel Puerto Rico, Inc. Intel Puerto Rico II, Inc. Product Codes/ Part Numbers	Intel Singapore, Ltd. Product Codes/ Part Numbers
SBC28616	pSBC28616	
SBC300	pSBC300	
SBC301	pSBC301	
SBC302	pSBC302	
SBC304	pSBC304	
SBC307	pSBC307	
SBC314	pSBC314	
SBC322	pSBC322	
SBC324	pSBC324	
SBC337	pSBC337	
SBC341	pSBC341	
SBC386	pSBC386	sSBC386
SBC386116	pSBC386116	
SBC386120	pSBC386120	
SBC38621	pSBC38621	
SBC38622	pSBC38622	
SBC38624	pSBC38624	
SBC38628	pSBC38628	
SBC38631	pSBC38631	
SBC38632	pSBC38632	
SBC38634	pSBC38634	
SBC38638	pSBC38638	
SBC428	pSBC428	sSBC428
SBC464	pSBC464	
SBC517	pSBC517	
SBC519	pSBC519	sSBC519
SBC534	pSBC534	sSBC534
SBC548	pSBC548	
SBC550	TSBC550	
SBC550	pSBC550	
SBC550	pSBC550	
SBC552	pSBC552	
SBC556	pSBC556	sSBC556
SBC569	pSBC569	
SBC589	pSBC589	
SBC604	pSBC604	
SBC608	pSBC608	
SBC614	pSBC614	
SBC618	pSBC618	
SBC655	pSBC655	
SBC6611	pSBC6611	
SBC8010	pSBC8010	
SBC80204	pSBC80204	
SBC8024	pSBC8024	sSBC8024
SBC8030	pSBC8030	
SBC8605	pSBC8605	sSBC8605
SBC8612	pSBC8612	
SBC8614	pSBC8614	
SBC8630	pSBC8630	sSBC8630
SBC8635	pSBC8635	sSBC8635
SBC86C38		sSBC86C38
SBC8825	pSBC8825	sSBC8825
SBC8840	pSBC8840	
SBC8845	pSBC8845	sSBC8845
SBC905	pSBC905	
SBCLNK001	pSBCLNK001	

Intel Corporation Product Codes/ Part Numbers	Intel Puerto Rico, Inc. Intel Puerto Rico II, Inc. Product Codes/ Part Numbers	Intel Singapore, Ltd. Product Codes/ Part Numbers
SBCMEM310	pSBCMEM310	
SBCMEM312	pSBCMEM312	
SBCMEM320	pSBCMEM320	
SBCMEM340	pSBCMEM340	
SBE96	pSBE96	
SBX217	pSBX217	
SBX218	pSBX218	
SBX270	pSBX270	
SBX311	pSBX311	
SBX328	pSBX328	
SBX331	pSBX331	
SBX344	pSBX344	
SBX350	pSBX350	
SBX351	pSBX351	
SBX354	pSBX354	
SBX488	pSBX488	
SBX586		sSBX586
SCHEMAIIPLD	pSCHEMAIIPLD	
SCOM	pSCOM	
SDK51	pSDK51	
SDK85	pSDK85	
SDK86	pSDK86	
SXM217	pSXM217	
SXM28612	pSXM28612	
SXM386	pSXM386	
SXM544	pSXM544	
SXM552	pSXM552	
SXM951	pSXM951	
SXM955	pSXM955	
SYP120	pSYP120	
SYP301	pSYP301	
SYP302	pSYP302	
SYP31090	pSYP31090	
SYP311	pSYP311	
SYP3847	pSYP3847	
SYR286	pSYR286	
SYR86	pSYR86	
SYS120	pSYS120	
SYS310	pSYS310	
SYS311	pSYS311	
T60	pT60	
TA096	pTA096	
TA252	pTA252	
TA452	pTA452	
W140	pW140	
W280	pW280	
W40	pW40	
W80	pW80	
XNX286DOC	pXNX286DOC	
XNX286DOCB	pXNX286DOCB	
XNXIBASE	pXNXIBASE	
XNXIDB	pXNXIDB	
XNXIDESK	pXNXIDESK	
XNXIPLAN	pXNXIPLAN	
XNXIWORD	pXNXIWORD	

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