Data Book

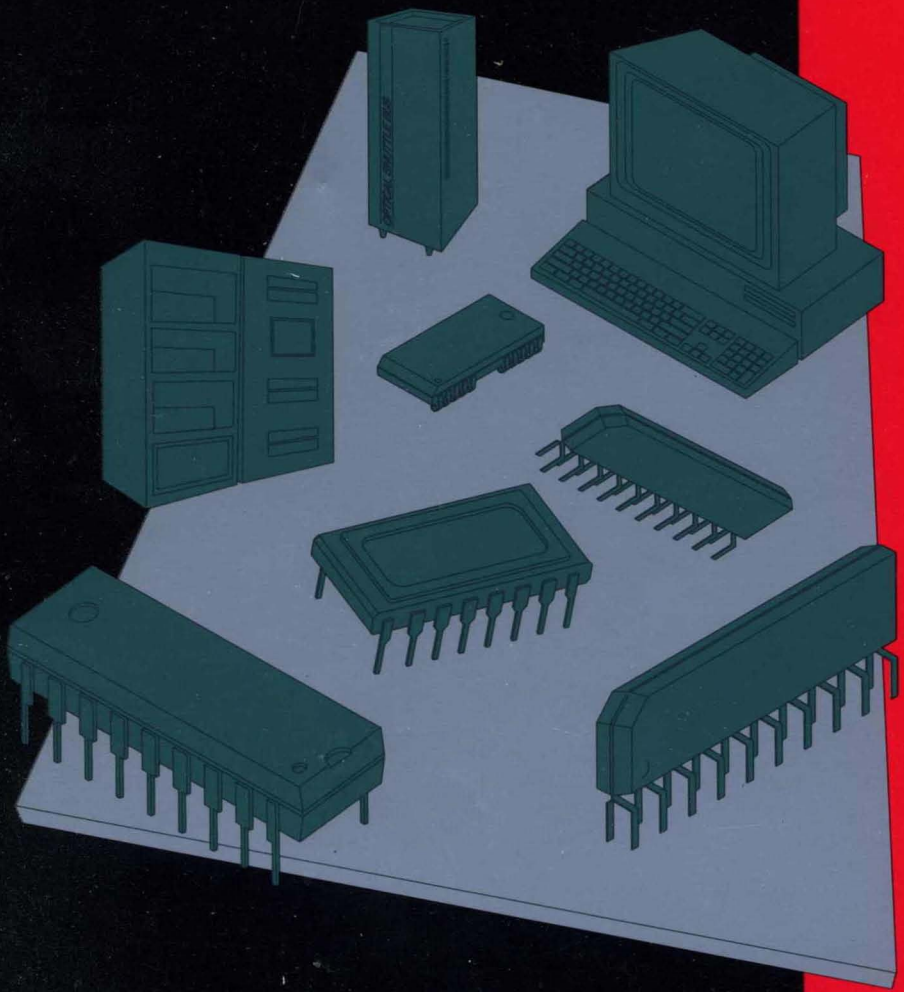
Dynamic RAM Products

1990

FUJITSU

Dynamic RAM Products

1990
DATA
BOOK



FUJITSU

FUJITSU

Dynamic RAM Products

1990
Data
Book

Fujitsu Limited
Tokyo, Japan

Fujitsu Microelectronics, Inc.
San Jose, California, U.S.A.

Fujitsu Mikroelectronik GmbH
Frankfurt, F.R. Germany

Fujitsu Microelectronics Asia PTE Limited
Singapore

This document is published by the Publications Department, Fujitsu Microelectronics, Inc.,
3545 North First Street, San Jose, California, U.S.A. 95134–1804; U.S.A.

Printed in the U.S.A.

Edition 1.0

Contents and Alphanumeric Product List

DRAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

DRAM PRODUCTS

Contents and Alphanumeric Product List (Continued)

DRAM PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

Introduction

Fujitsu's Dynamic RAM Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high–speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic RAMs.

The Dynamic RAM product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

This data book includes product information on the following DRAM products:

NMOS and CMOS DRAMs

Fujitsu manufactures a complete family of leading technology dynamic random access memories for the data processing, telecom, and industrial markets. This family consists of the highest density devices currently available with a broad selection of organizations, access modes, and packages.

Application-Specific DRAMs

Fujitsu offers a family of dual-port dynamic random access memories tailored for video imaging and graphics applications. These devices adhere to JEDEC standards where applicable and are available in the popular packages.

MOS and CMOS DRAM Modules

Fujitsu manufactures a complete family of reliable MOS and CMOS dynamic RAM memory modules for those applications requiring high density and large memory storage capability. Fujitsu's family of memory modules are pin-compatible with JEDEC standards.

Section 1

NMOS DRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options		
1–3	MB81256–10	100	262144 bits	16-pin	Plastic	DIP, ZIP
	–12	120	(262144w x 1b)	16-pin	Ceramic	DIP
				18-pin	Plastic	LCC
	–15	150		18-pad	Ceramic	LCC
1–25	MB81257–10	100	262144 bits	16-pin	Plastic	DIP, ZIP
	–12	120	(262144w x 1b)	16-pin	Ceramic	DIP
	–15	150		18-pin	Plastic	LCC
				18-pad	Ceramic	LCC
1–49	MB81464–10	100	262144 bits	18-pin	Plastic	DIP, LCC
	–12	120	(65536w x 4b)	18-pin	Ceramic	DIP
	–15	150		20-pin	Plastic	ZIP

1

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81256-10
MB 81256-12
MB 81256-15

December 1985
Edition 4.1

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

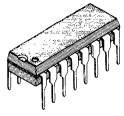
The Fujitsu MB 81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permits the MB 81256 to be housed in a standard 16 pin DIP/ZIP and 18 pad LCC. Pin-out conform to the JEDEC approved pin out. Additionally, the MB 81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability. The MB 81256 also features "page mode" which allows high speed random access to up to 512 bits within a same row.

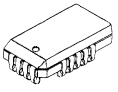
The MB 81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply torelance is very wide. All inputs are TTL compatible.

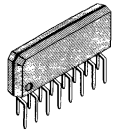
- 262,144 x 1 RAM, 16 pin DIP and ZIP/18 pad LCC
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row access time,
  100 ns max. (MB 81256-10)
  120 ns max. (MB 81256-12)
  150 ns max. (MB 81256-15)
- Cycle time,
  200 ns min. (MB 81256-10)
  220 ns min. (MB 81256-12)
  260 ns min. (MB 81256-15)
- Page cycle time,
  100 ns max. (MB 81256-10)
  120 ns max. (MB 81256-12)
  145 ns max. (MB 81256-15)
- Single +5V Supply, ±10% tolerance
- Low power,
  385 mW max. (MB 81256-10)
  358 mW max. (MB 81256-12)
  314 mW max. (MB 81256-15)
  25 mW max. (standby)
- 256 refresh cycles every 4ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-while-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD}, are eliminated
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-pin Ceramic (Seam Weld) DIP (Suffix: -C)
  Standard 16-pin Ceramic (Cerdip) DIP (Suffix: -Z)
  Standard 16-pin Plastic DIP (Suffix: -P)
  Standard 18-pad Ceramic LCC (Suffix: -TV)
  Standard 18-pin plastic LCC (Suffix: -PV)
  Standard 16-pin Plastic ZIP (Suffix. -PSZ)



PLASTIC PACKAGE
DIP-16P-M03



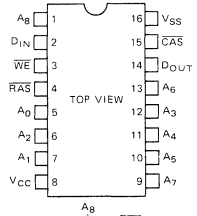
PLASTIC PACKAGE
LCC-18P-M04

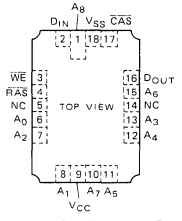


PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 17
DIP-16C-A04: See Page 18
DIP-16C-C04: See Page 19
LCC-18C-F04: See Page 24

PIN ASSIGNMENT





Pin assignment for ZIP: See Page 21

ABSOLUTE MAXIMUM RATINGS (See NOTE)

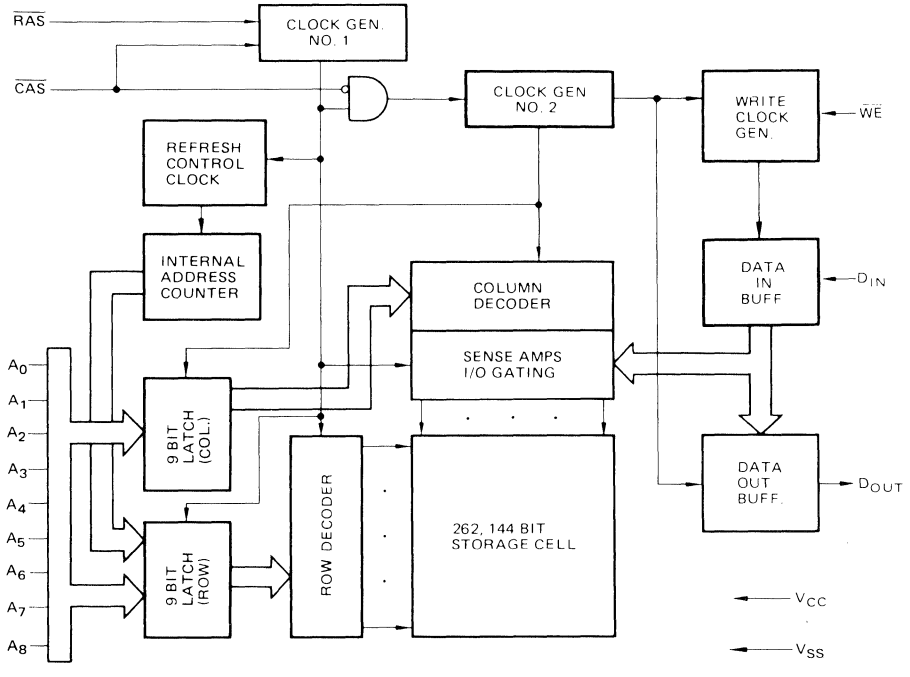
Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81256 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		10	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81256-10	I_{CC1}			70	mA
	MB 81256-12				65	
	MB 81256-15				57	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$=V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81256-10	I_{CC3}			60	mA
	MB 81256-12				55	
	MB 81256-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	MB 81256-10	I_{CC4}			35	mA
	MB 81256-12				30	
	MB 81256-15				25	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81256-10	I_{CC5}			65	mA
	MB 81256-12				60	
	MB 81256-15				55	
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output high Voltage (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE * : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1, 2, 3

Parameter	NOTES	Symbol	MB 81256-10		MB 81256-12		MB 81256-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time		t_{RC}	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	200		220		260		ns
Access Time from $\overline{RAS}$	4, 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5, 6	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7, 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		20		ns
Write Command Set Up Time	10	t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

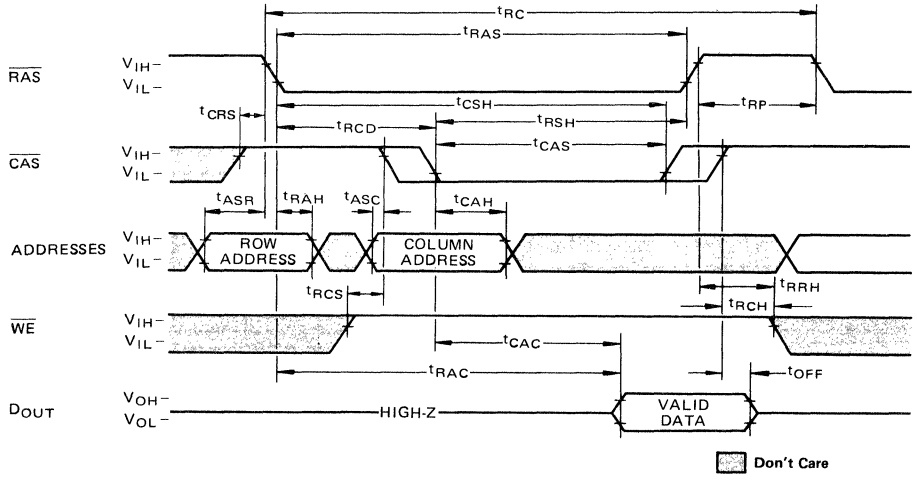
Parameter	NOTES	Symbol	MB 81256-10		MB 81256-12		MB 81256-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Page Mode Read/Write Cycle Time		t_{PC}	100		120		145		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	100		120		145		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	40		50		60		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		375		430		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		60		70		ns

Notes:

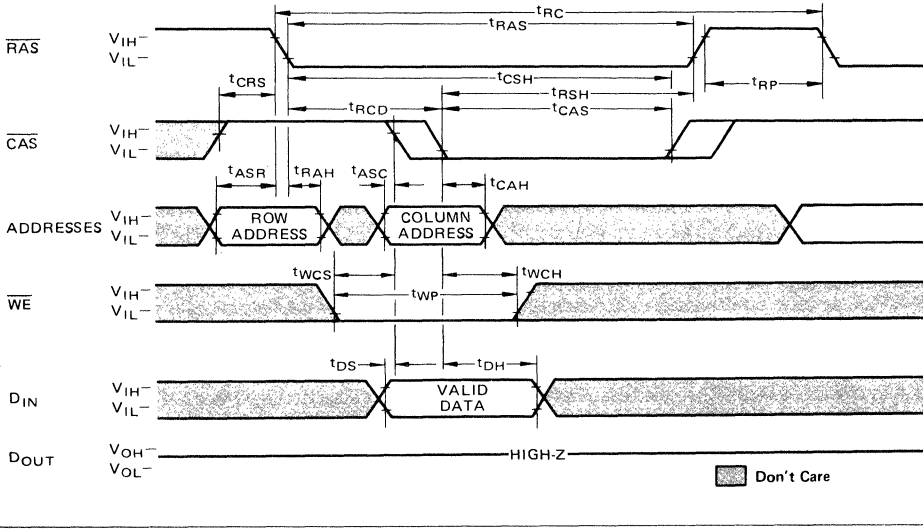
1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.) If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5ns) + t_{ASC} (min).
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
    If $t_{CWD} \geqq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

1

Read Cycle

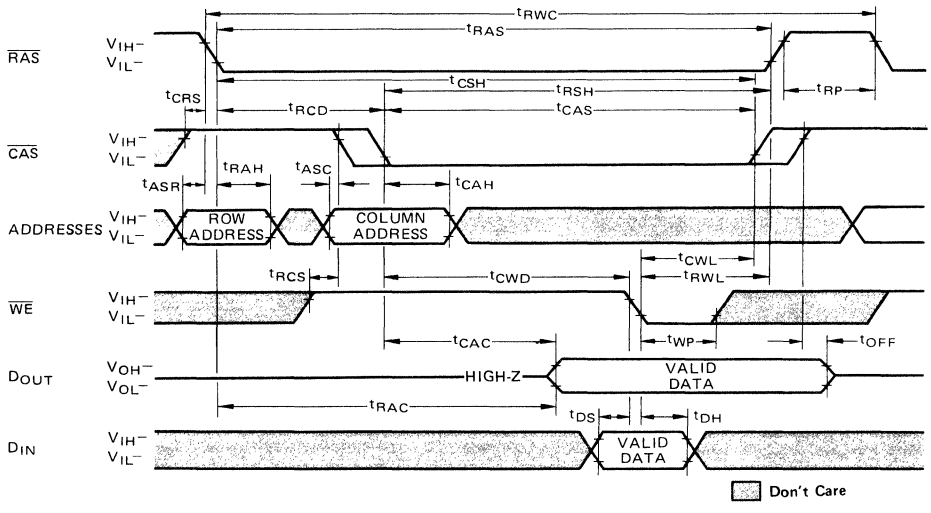


Write Cycle (Early Write)

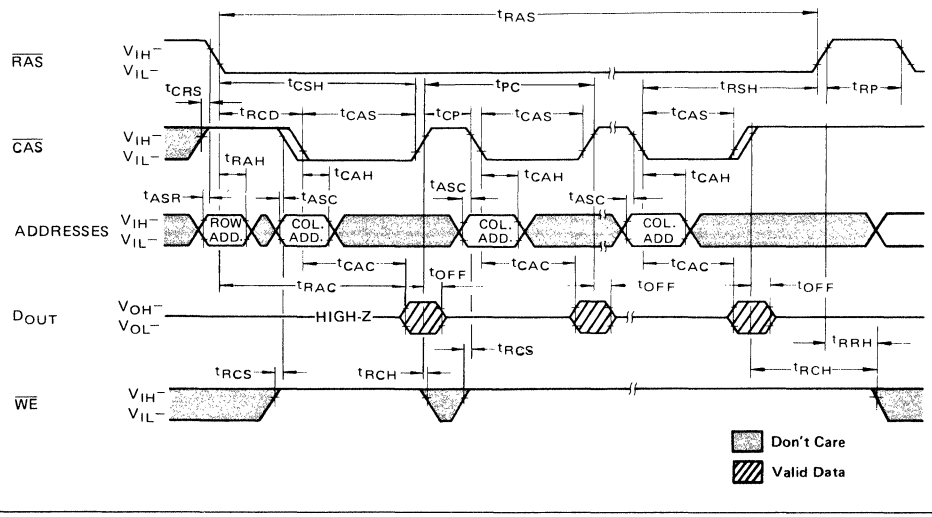


1

Read–Write/Read–Modify–Write Cycle

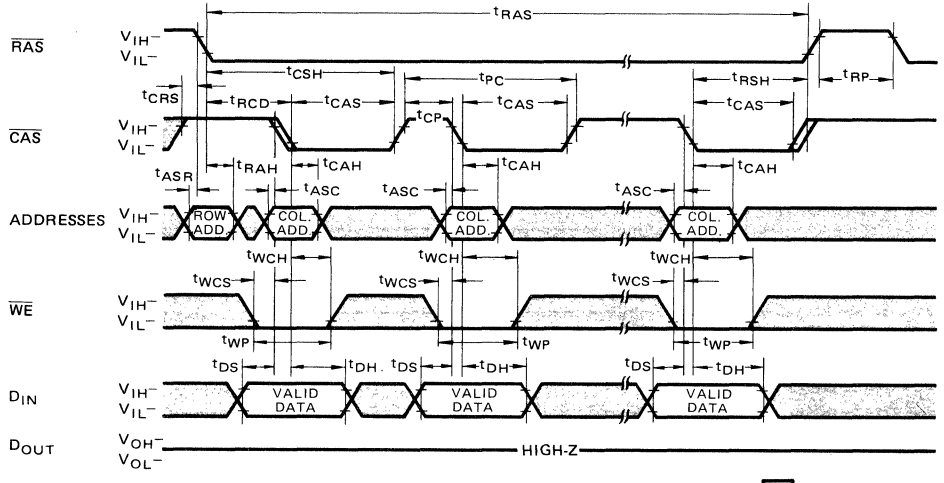


Page Mode Read Cycle

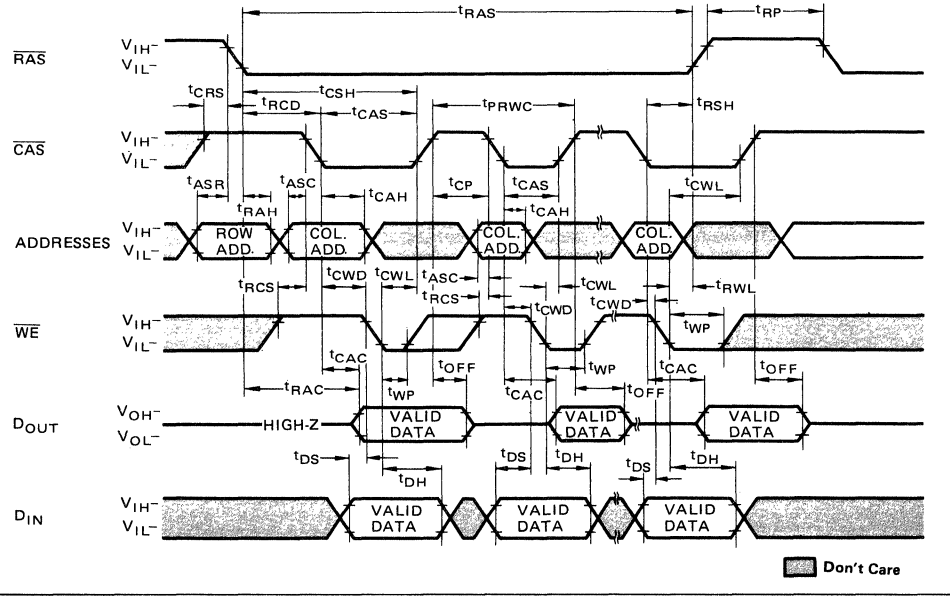


1

Page Mode Write Cycle



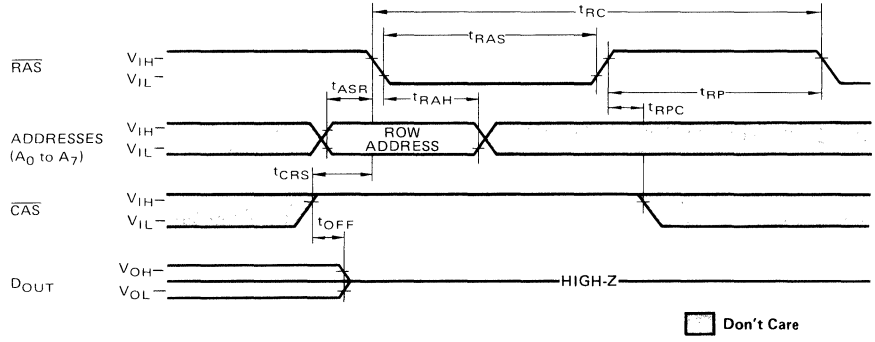
Page Mode Read-Write Cycle



1

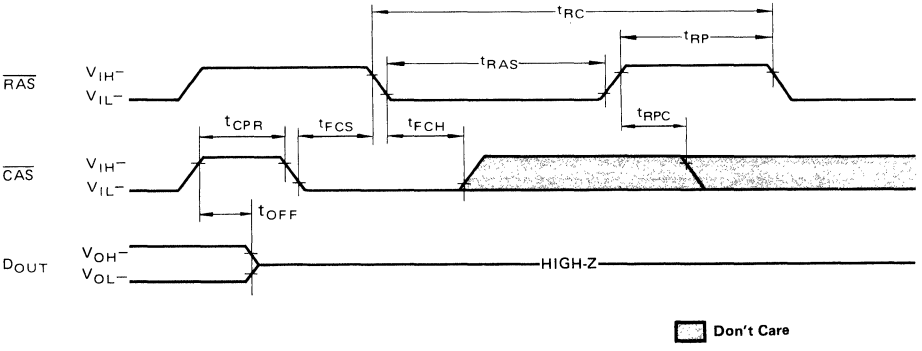
$\overline{RAS}$-only Refresh cycle

NOTE: $\overline{WE}$, D_{IN} = Don't care, $A_8 = V_{IH}$ or V_{IL}



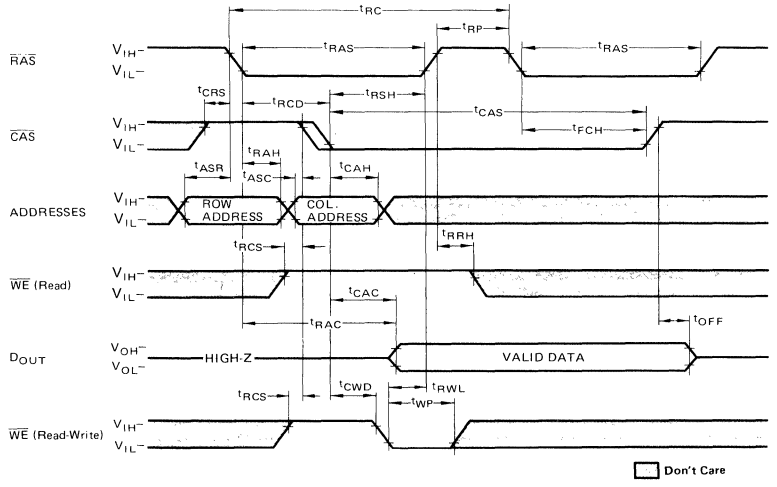
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Address, $\overline{WE}$, D_{IN} = Don't care

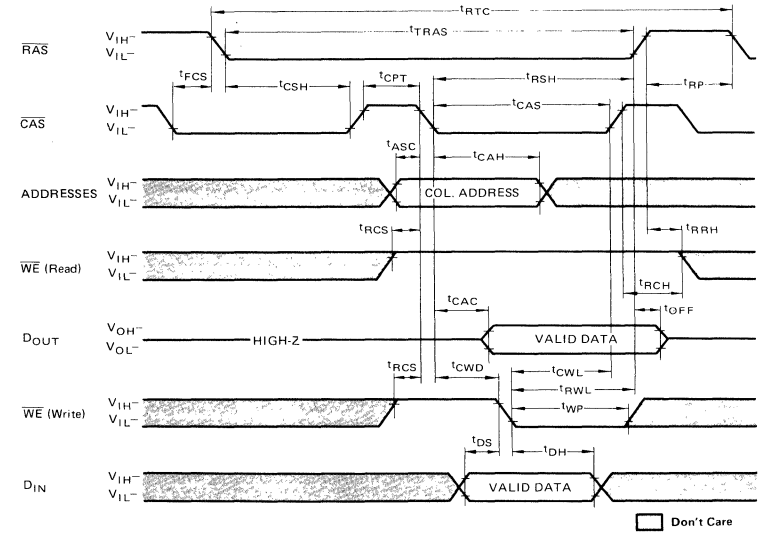


1

Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement

The MB 81256 has improved circuitry that eases timing requirements for high speed access operations. The MB 81256 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81256 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ nonrestrictive and deleted them from the data sheet, these include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81256. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-address.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode; low selects write mode. The data input is disable when read mode is selected.

Data input:

Data is written into the MB 81256 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle

The MB 81256 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle (t_{RWC} = t_{RC}) is possible with the MB 81256.

Page Mode:

Page-mode operation permits strobing the row-address into the MB 81256 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4ms. The MB 81256 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;

$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low.

Strobing each of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;

A hidden refresh cycle may takes place while maintaining the latest valid data at the output by extending $\overline{CAS}$ active time.

For the MB 81256 a hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$-

1

before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-befor-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and then goes to low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and column address (9 bits) to be accessed can be defined as follows:

*A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.

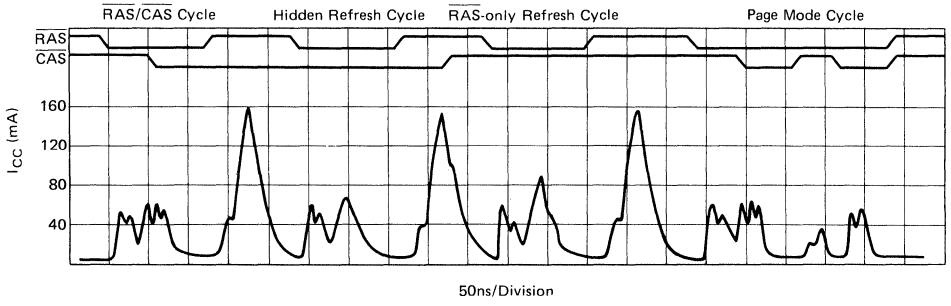
*A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test cycles is used for the following operations:

(1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
(2) Throughout the test, use the same column address, and keep RA8 high.
(3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
(4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
(5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
(6) Complement the test pattern and repeat step 3), 4) and 5).

Fig. 2 – CURRENT WAVEFORM (V_{CC}=5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

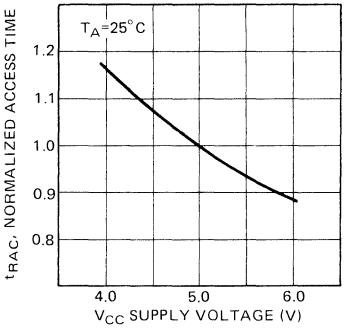


Fig. 4 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

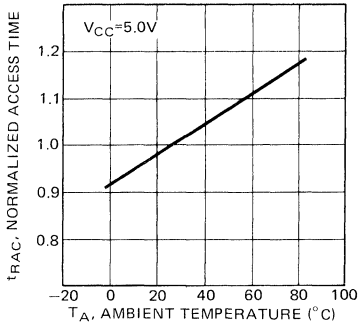


Fig. 5 – OPERATING CURRENT vs CYCLE RATE

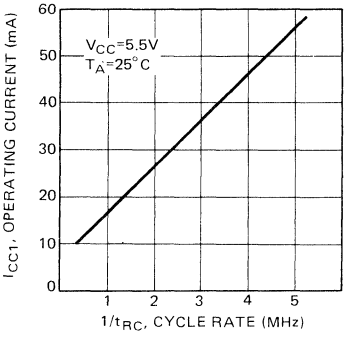


Fig. 6 – OPERATING CURRENT vs SUPPLY VOLTAGE

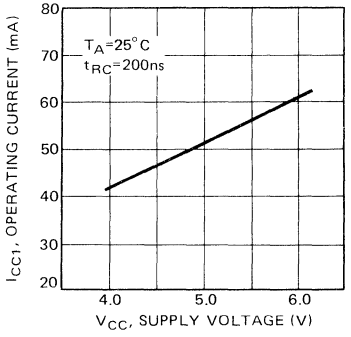


Fig. 7 – OPERATING CURRENT vs AMBIENT TEMPERATURE

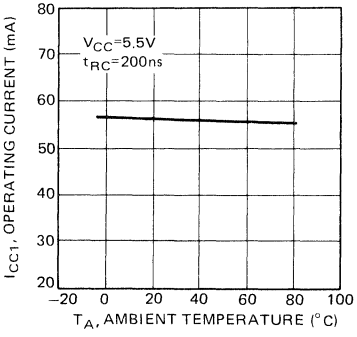
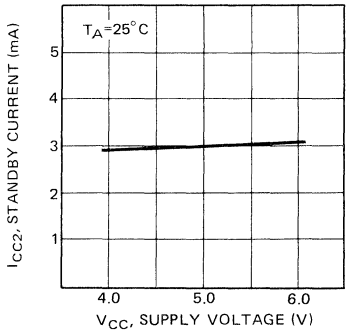


Fig. 8 – STANDBY CURRENT vs SUPPLY VOLTAGE



1

Fig. 9 – STANDBY CURRENT vs AMBIENT TEMPERATURE

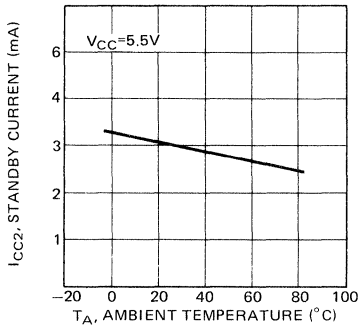


Fig. 10 – REFRESH CURRENT 1 vs CYCLE RATE

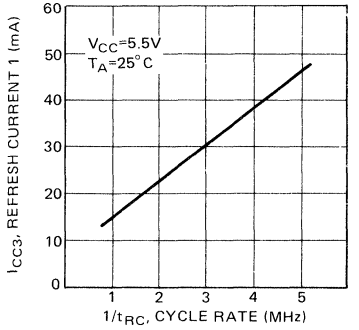


Fig. 11 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

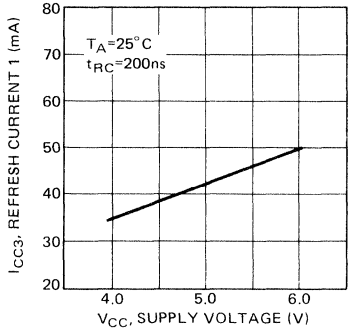


Fig. 12 – PAGE MODE CURRENT vs CYCLE RATE

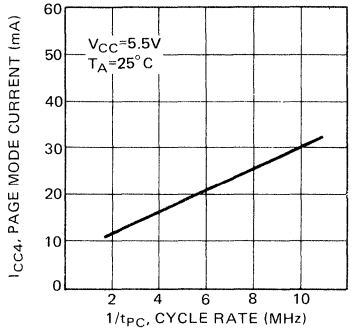


Fig. 13 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

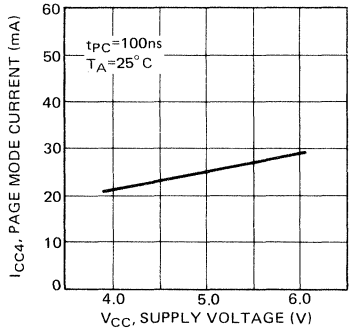


Fig. 14 – REFRESH CURRENT 2 vs CYCLE RATE

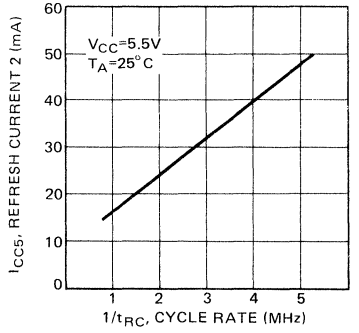


Fig. 15 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

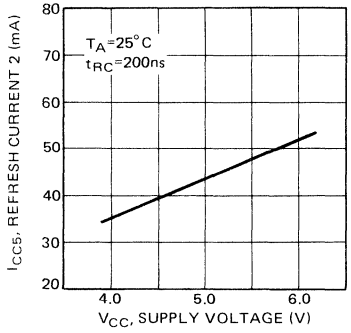


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

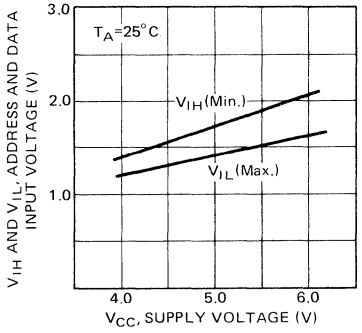


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

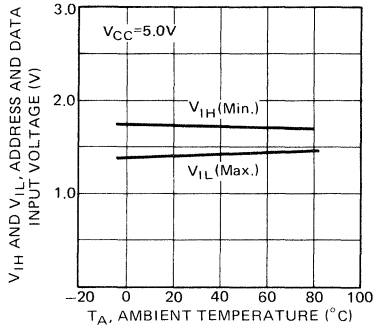


Fig. 18 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

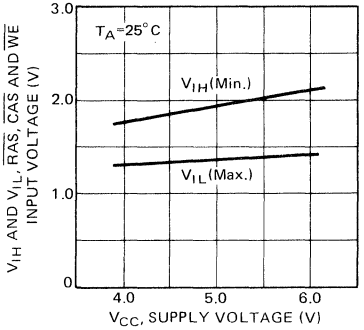


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

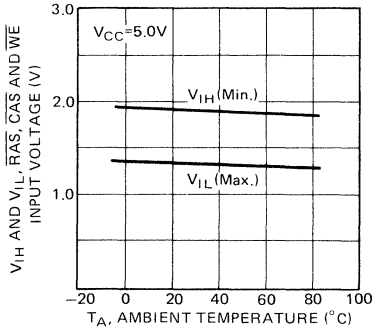
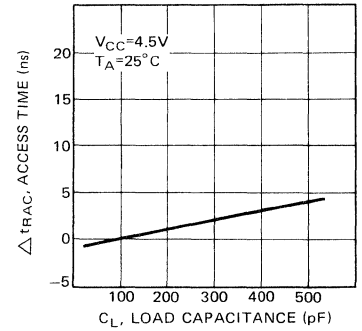


Fig. 20 – ACCESS TIME vs LOAD CAPACITANCE



1

Fig. 21 – OUTPUT CURRENT vs OUTPUT VOLTAGE

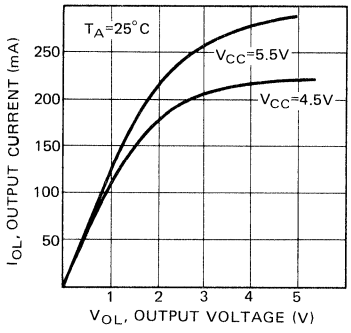


Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

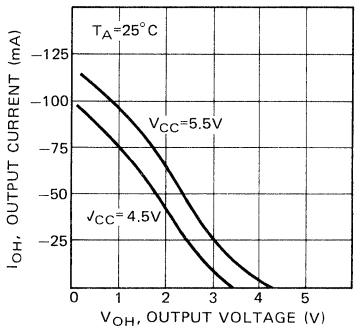


Fig. 23 – CURRENT WAVEFORM DURING POWER UP

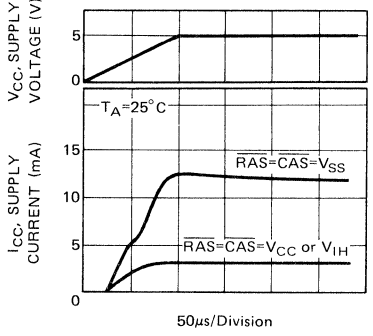
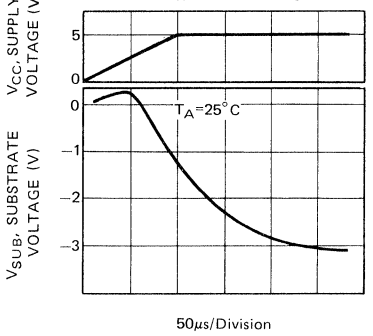
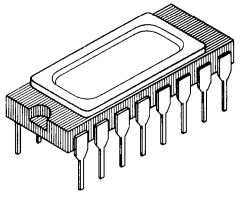


Fig. 24 – SUBSTRATE VOLTAGE DURING POWER UP



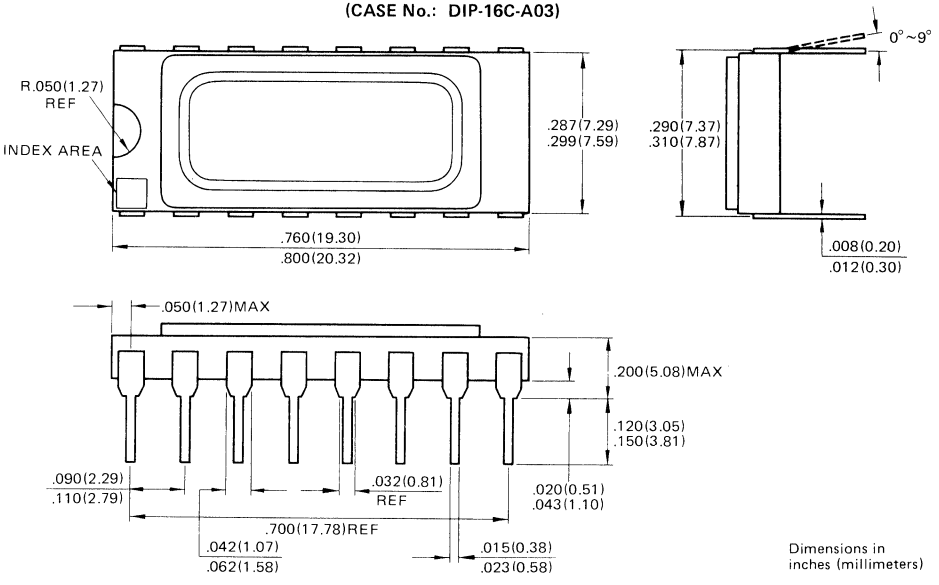
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A03

16-DEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)

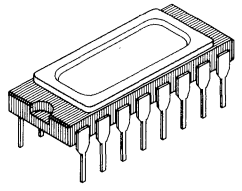


Dimensions in inches (millimeters)

1

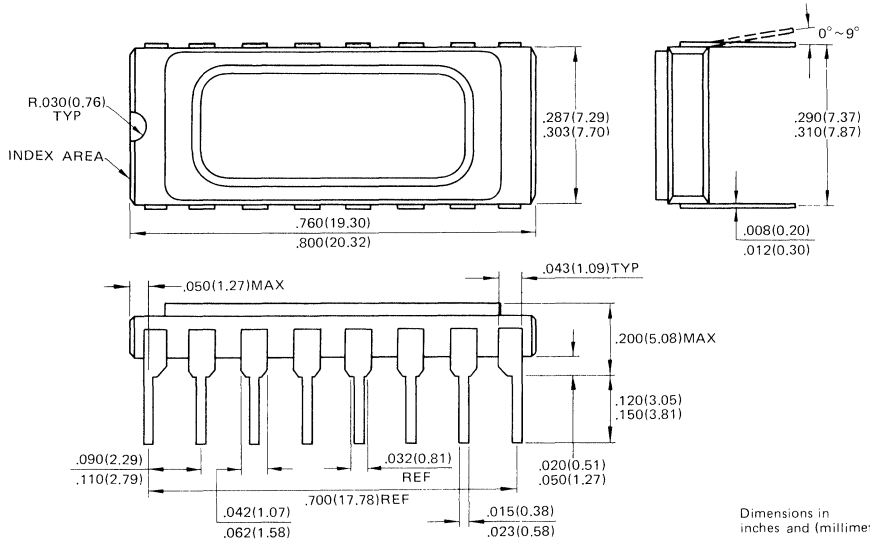
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A04

16-LEAD SEAM WELD DIP PACKAGE
(CASE No.: DIP-16C-A04)

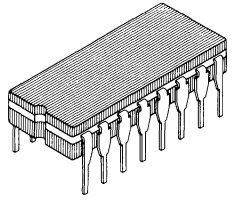


Dimensions in inches and (millimeters)

1

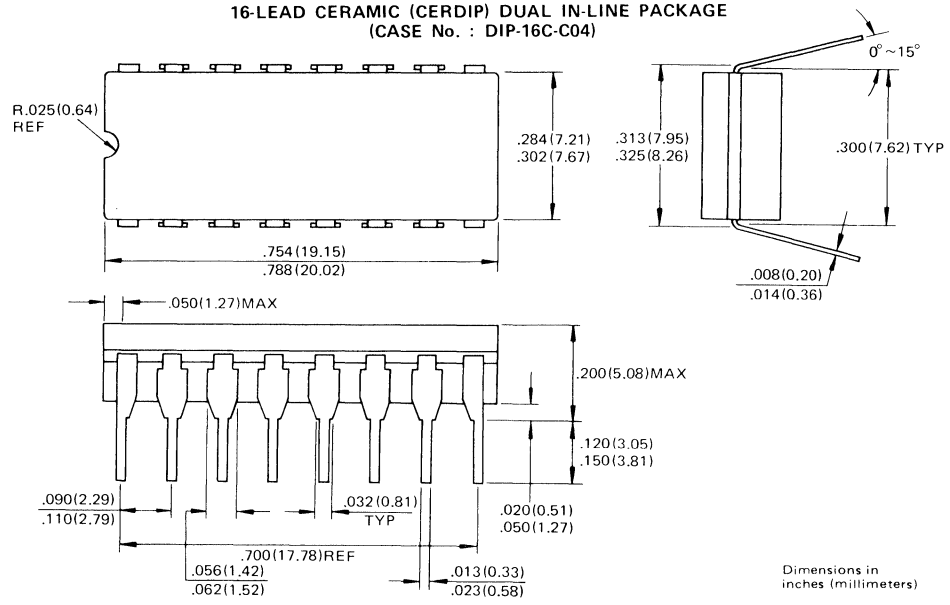
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -Z)



DIP-16C-C04

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C04)



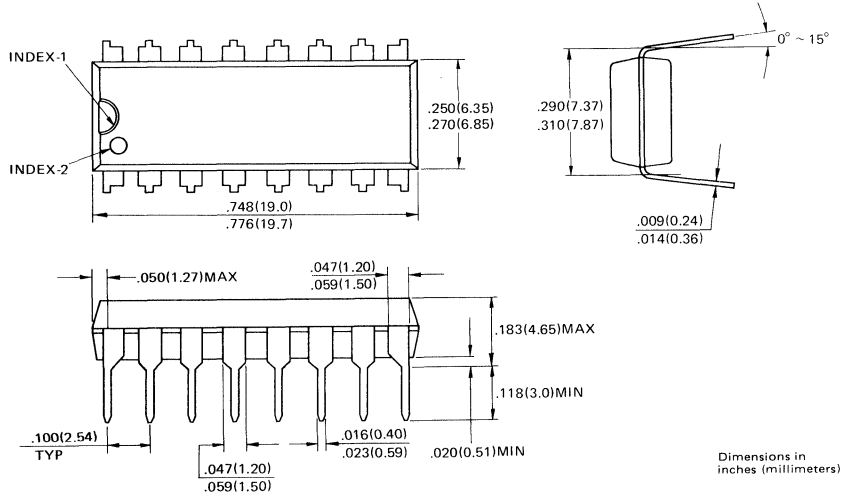
Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)

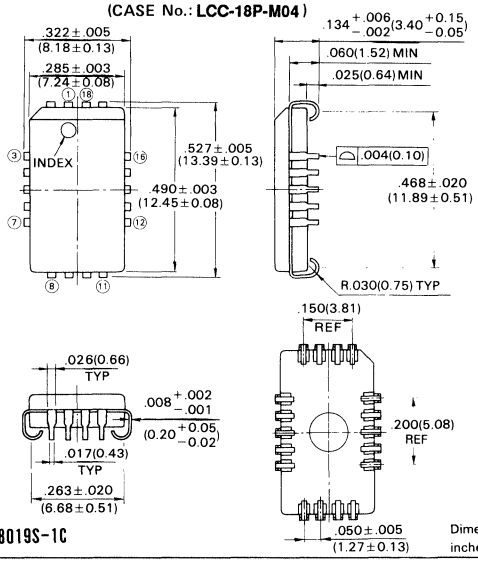
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in inches (millimeters)

Standard 18-pin Plastic LCC (Suffix: -PV)

18-LEAD PLASTIC CHIP CARRIER
(CASE No.: **LCC-18P-M04**)

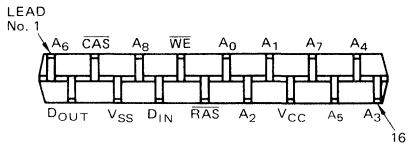


(No.): LEAD No.
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

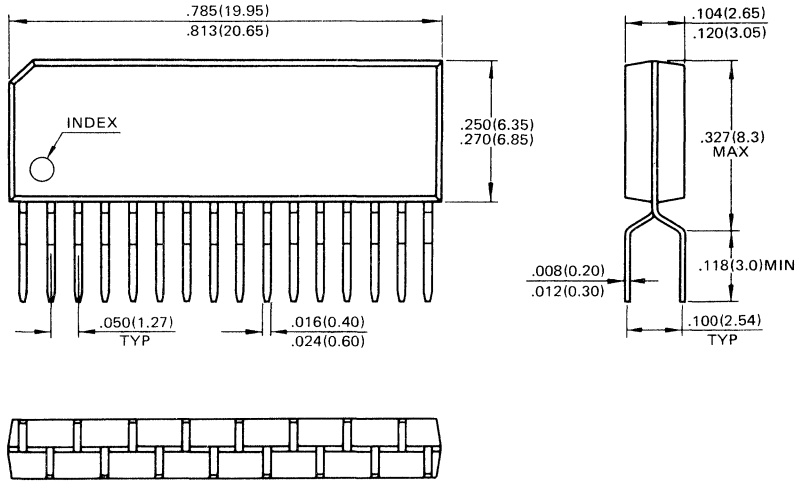
Standard 16-pin Plastic ZIP (Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)

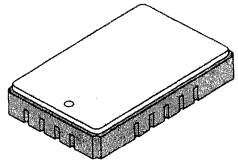


Dimensions in
inches (millimetres)

1

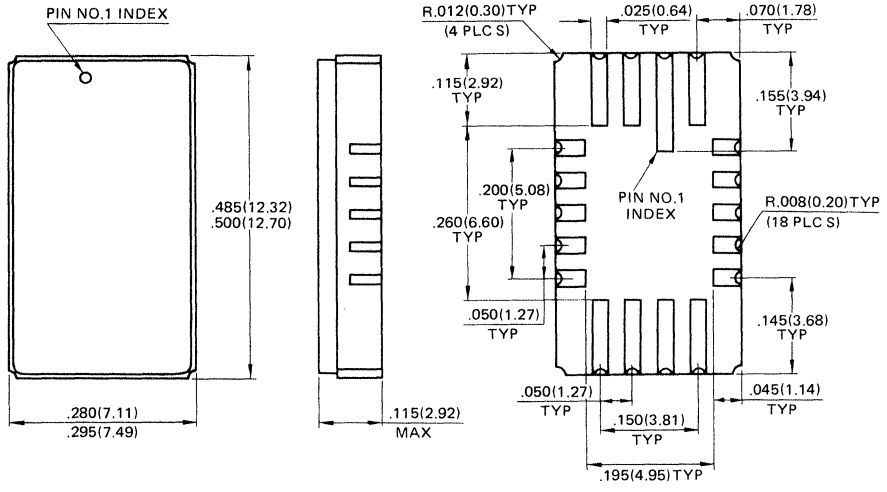
PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Suffix: -TV)



LCC-18C-F04

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F04)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches (millimeters).

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81257-10
MB 81257-12
MB 81257-15

September 1985
Edition 4.0

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY

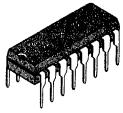
The Fujitsu MB 81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 81257 to be housed in a standard 16 pin DIP/ZIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MB 81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is an upward compatible version of MB 8266A. The MB 81257 also features "Nibble Mode" which allows high speed serial access to up to 4 bits of data.

The MB 81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

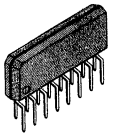
Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 262,144 x 1 RAM, 16 pin DIP and ZIP/18 pad LCC
- Silicon-gate, Triple Poly NMOS, single transistor cell
- Row access time,
  - 100 ns max. (MB 81257-10)
  - 120 ns max. (MB 81257-12)
  - 150 ns max. (MB 81257-15)
- Cycle time,
  - 200 ns min. (MB 81257-10)
  - 220 ns min. (MB 81257-12)
  - 260 ns min. (MB 81257-15)
- Nibble cycle time,
  - 45 ns max. (MB 81257-10)
  - 50 ns max. (MB 81257-12)
  - 60 ns max. (MB 81257-15)
- Single +5V Supply, ±10% tolerance
- Low power,
  - 385 mW max. (MB 81257-10)
  - 358 mW max. (MB 81257-12)
  - 314 mW max. (MB 81257-15)
  - 25 mW max. (standby)
- 256 refresh cycles every 4ms
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh capability
- High speed Read-white-Write cycle
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} are eliminated
- Output unlatched at cycle end allows two-dimensional chip select
- Common I/O capability using Early Write operation
- On-chip latches for Addresses and Data-in
- Standard 16-pin Ceramic (Seam Weld) DIP (Suffix:-C)
  Standard 16-pin Ceramic (Cerdip) DIP (Suffix: -Z)
  Standard 16-pin Plastic DIP (Suffix: -P)
  Standard 18-pad Ceramic LCC (Suffix: -TV)
  Standard 18-pin Plastic LCC (Suffix: -PV)
  Standard 16-pin Plastic ZIP (Suffix: -PSZ)



PLASTIC PACKAGE
DIP-16-M03

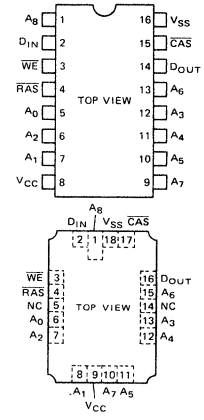
PLASTIC PACKAGE
LCC-18P-M04



PLASTIC PACKAGE
ZIP-16P-M01

DIP-16C-A03: See Page 19
DIP-16C-A04: See Page 20
DIP-16C-C04: See Page 21
LCC-18C-F04: See Page 24

PIN ASSIGNMENT



Pin assignment for ZIP: See page 23

ABSOLUTE MAXIMUM RATINGS (See NOTE)

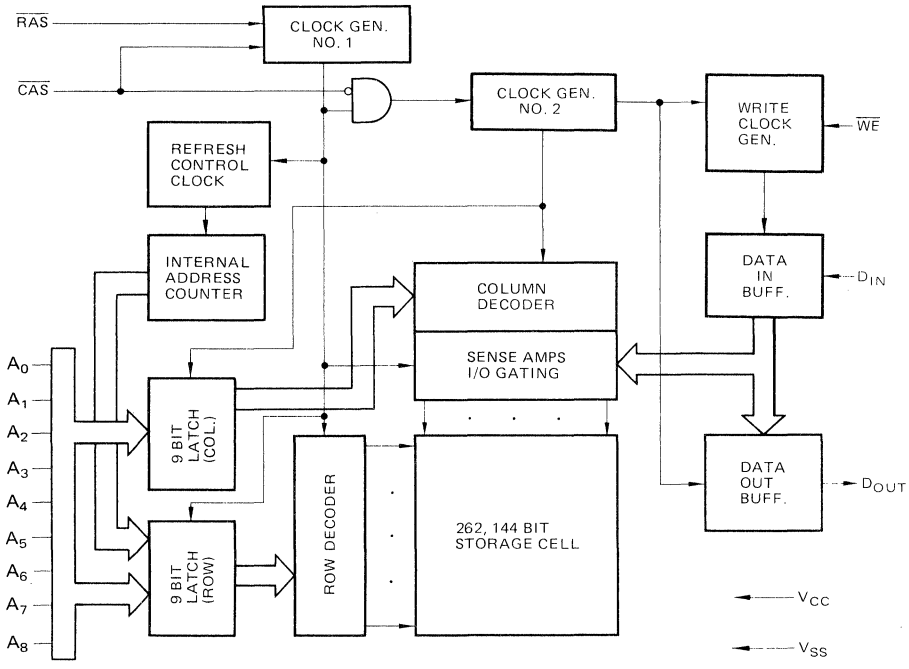
Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81257 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8, D_{IN}	C_{IN1}		7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	-2.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	MB 81257-10	I_{CC1}			70	mA
	MB 81257-12				65	
	MB 81257-15				57	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		I_{CC2}			4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	MB 81257-10	I_{CC3}			60	mA
	MB 81257-12				55	
	MB 81257-15				50	
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = Min.)	MB 81257-10	I_{CC4}			22	mA
	MB 81257-12				20	
	MB 81257-15				18	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB 81257-10	I_{CC5}			65	mA
	MB 81257-12				60	
	MB 81257-15				55	
INPUT LEAKAGE CURRENT any input (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10		10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}			0.4	V
OUTPUT LEVEL Output high Voltage (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE * : I_{CC} is depended on output loading and cycle rates. Specified values are obtained with the output open.

1

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle time		t_{RC}	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	200		220		260		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		20		ns
Write Command Set Up Time	10	t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		30		25		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	10	t_{CWD}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

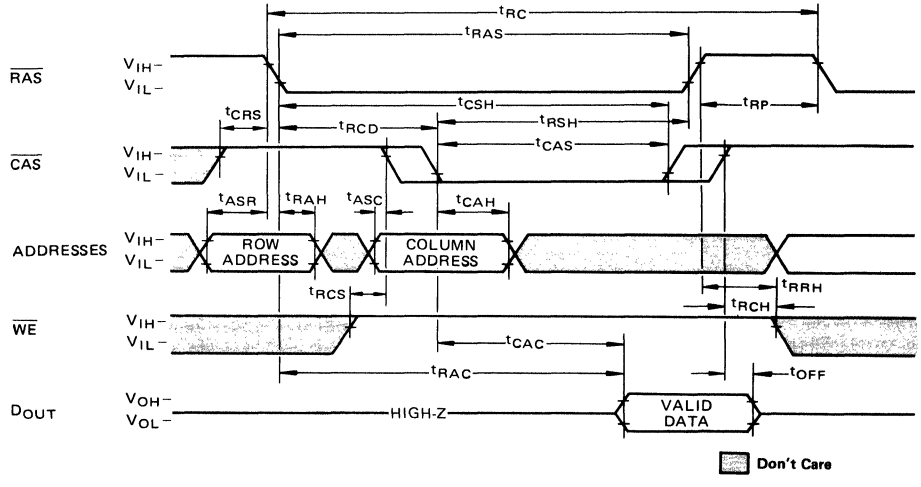
Parameter	NOTES	Symbol	MB 81257-10		MB 81257-12		MB 81257-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	45		50		60		ns
Nibble Mode Read-Write Cycle Time		t_{NRWC}	45		50		60		ns
Nibble Mode Access Time		t_{NCAC}		20		25		30	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	20		25		30		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		15		20		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	20		25		30		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	35		40		45		
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	20		20		20		ns
Refresh Counter Test Cycle Time	11	t_{RTC}	330		375		430		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	11	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	11	t_{CPT}	50		60		70		ns

Notes:

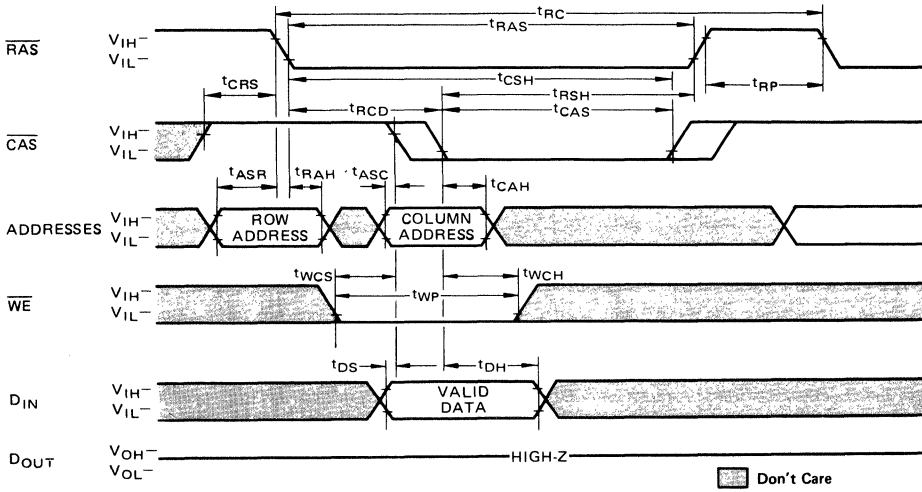
1. An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
11. Test mode cycle only.

1

Read Cycle

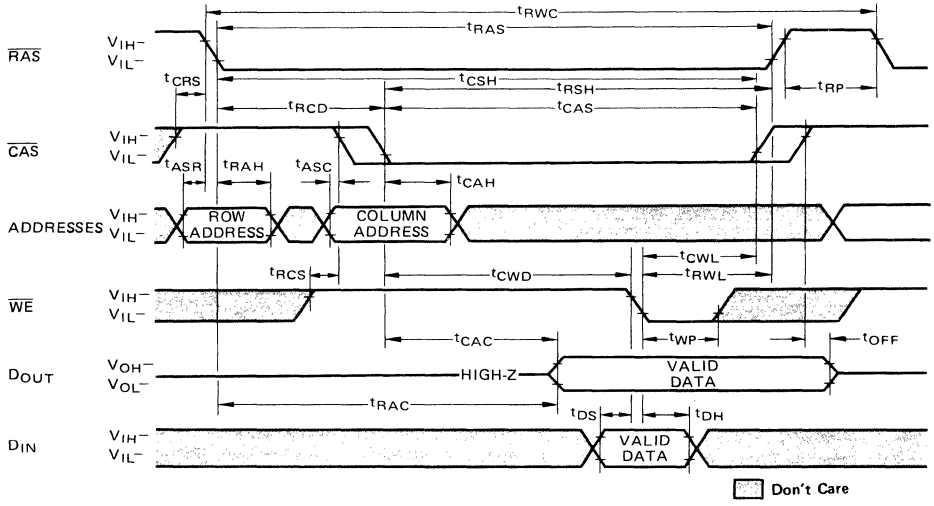


Write Cycle (Early Write)

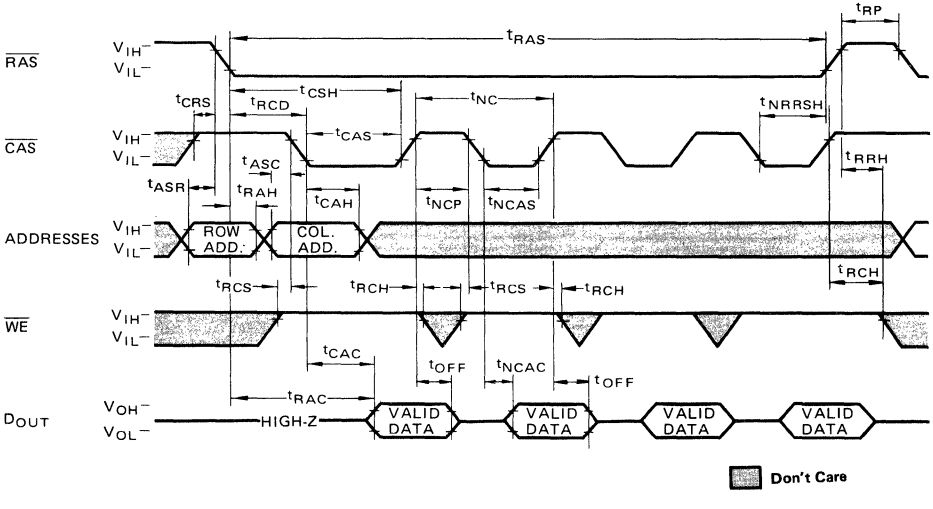


1

Read–Write/Read–Modify–Write Cycle

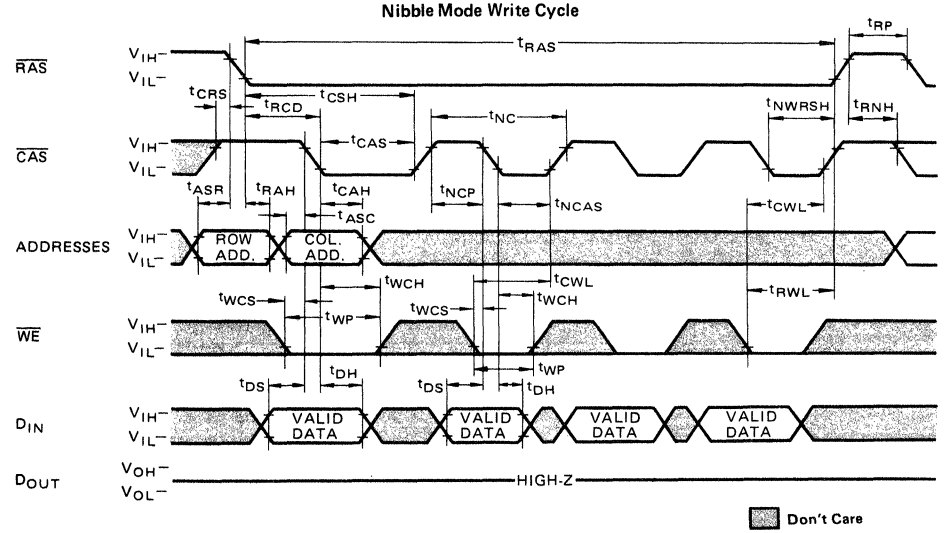


Nibble Mode Read Cycle

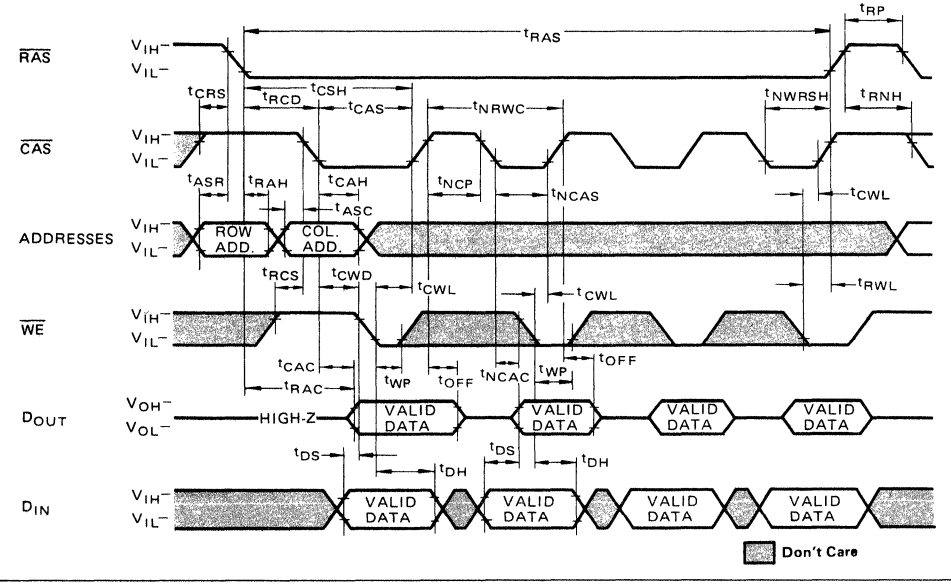


1

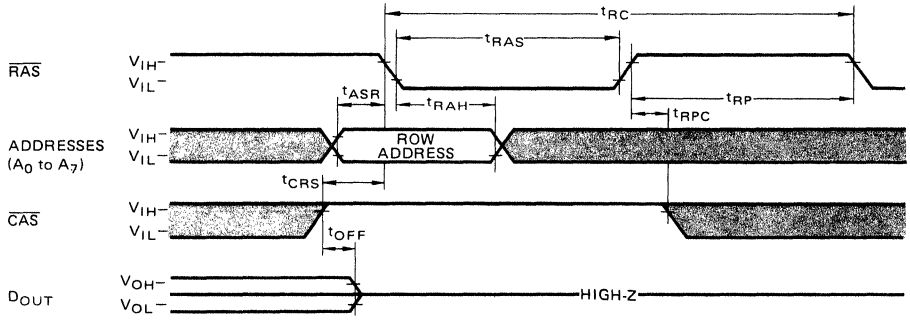
Nibble Mode Write Cycle



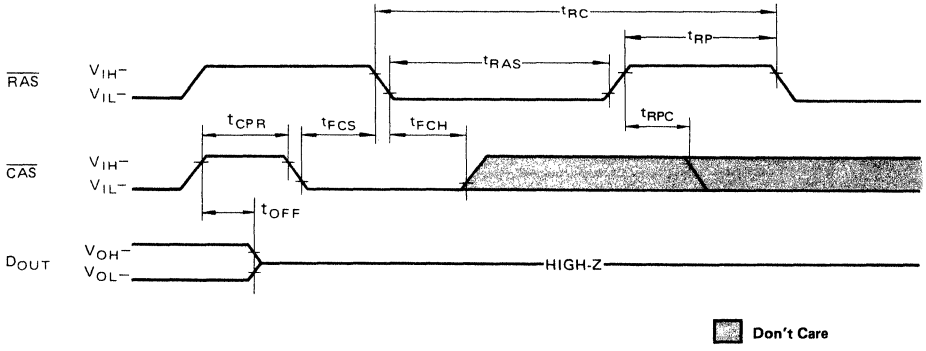
Nibble Mode Read-Write Cycle



$\overline{RAS}$-only Refresh Cycle
NOTE: $\overline{WE}$, D_{IN} = Don't care, $A_8 = V_{IH}$ or V_{IL}

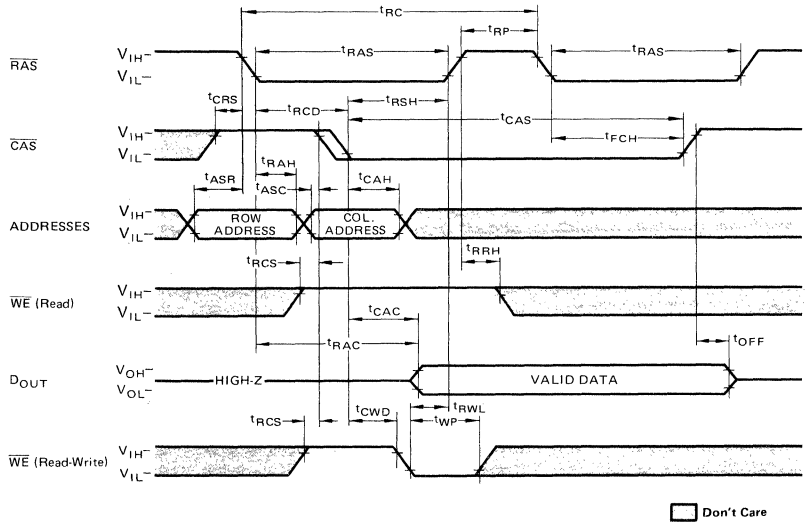


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
NOTE: Address, $\overline{WE}$, D_{IN} = Don't care

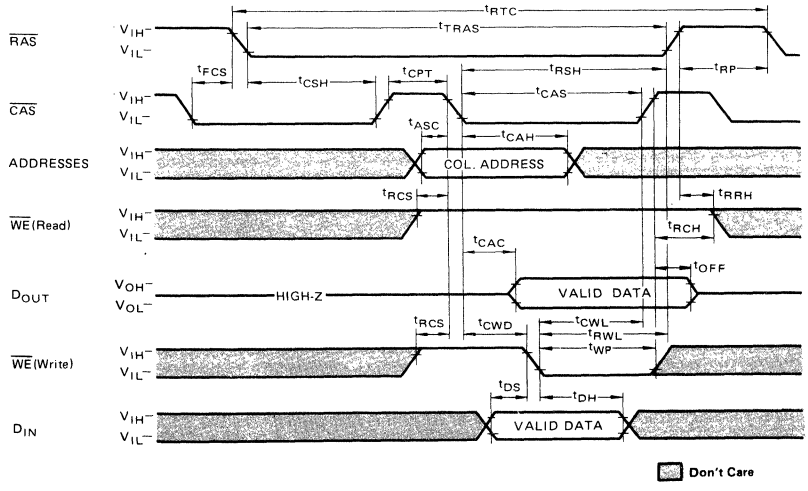


1

Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Simple Timing Requirement

The MB 81257 has improved circuitry that eases timing requirements for high speed access operations. The MB 81257 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 81257 has the minimal hold times of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 81257 provides higher throughput in inter-leaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB 81257. Nine row-address bits are established on the input pins (A_0 to A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column-address bits are established on the input pins and are latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode, low selects write mode. The data input is disabled when read mode is selected.

Data Input:

Data is written into the MB 81257 during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be delayed after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.) Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs, but data is not valid.

Fast Read-While-Write cycle

The MB 81257 has a fast read while write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings, described in the previous section. The output buffer is controlled by the sate of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MB 81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB 81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, a very fast read write cycle (t_{RWC} = t_{RC}) is possible with the MB 81257.

Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled only by the $\overline{WE}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{WE}$ state. The write operation is done during the period in which the $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit).

See Fig. 2.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 ms.

The MB 81257 offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh;

The $\overline{RAS}$ only refresh aboids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each

1

of 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81257 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh;
A hidden refresh cycle may takes place while maintaining latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB 81257, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counters provide the refresh addresses, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

CAS-before-RAS Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

- *A ROW ADDRESS – Bits A_0 to A_7 are defined by the refresh counter. The bit A_8 is set high internally.
- *A COLUMN ADDRESS – All the bits A_0 to A_8 are defined by latching levels on A_0 to A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for the following operations:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

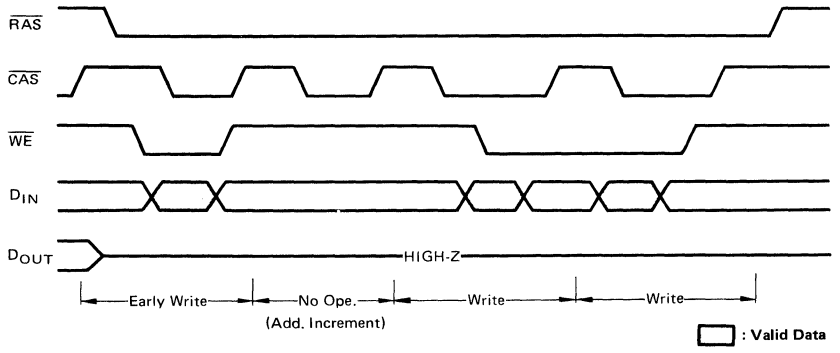
Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

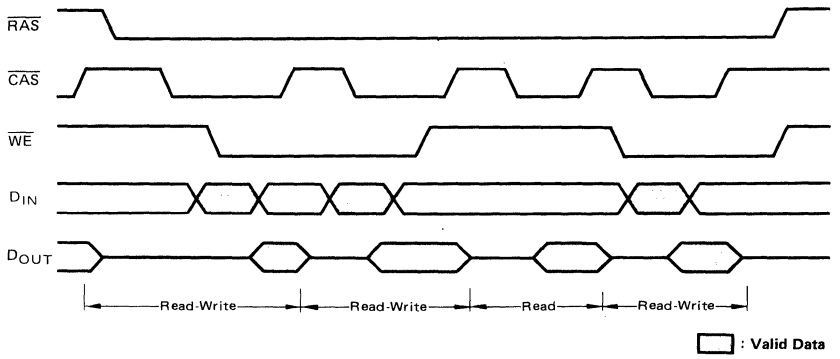
1

Fig. 2 – Nibble Mode

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)

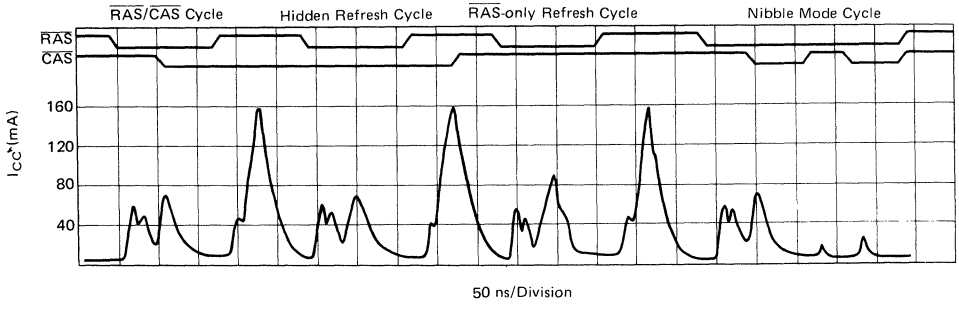


1

Table-2 FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geqq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write ($t_{WCS} \leqq t_{WCS}$ (min) or $t_{CWD} \geqq t_{CWD}$ (min))
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Fig. 3 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

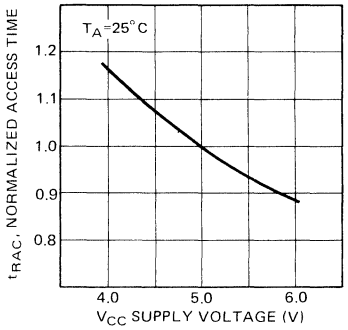


Fig. 5 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERAUTRE

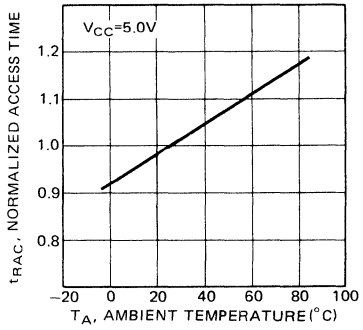


Fig. 6 – OPERATING CURRENT vs CYCLE RATE

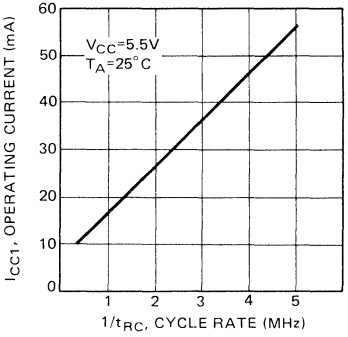


Fig. 7 – OPERATING CURRENT vs SUPPLY VOLTAGE

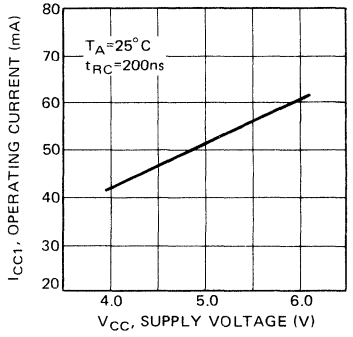


Fig. 8 – OPERATING CURRENT vs AMBIENT TEMPERATURE

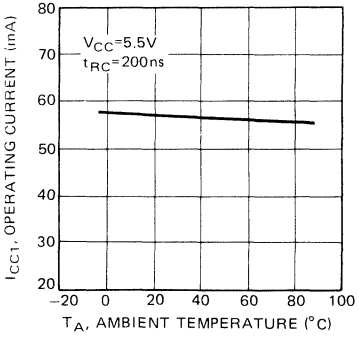
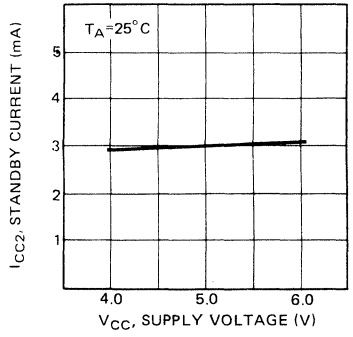


Fig. 9 – STANDBY CURRENT vs SUPPLY VOLTAGE



1

Fig. 10 – STANDBY CURRENT vs AMBIENT TEMPERATURE

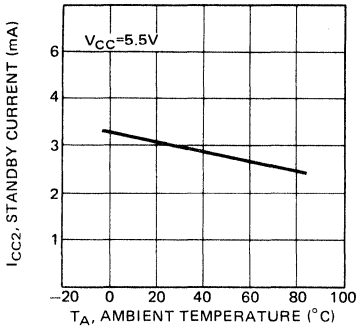


Fig. 11 – REFRESH CURRENT 1 vs CYCLE RATE

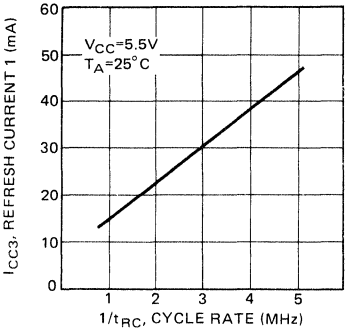


Fig. 12 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

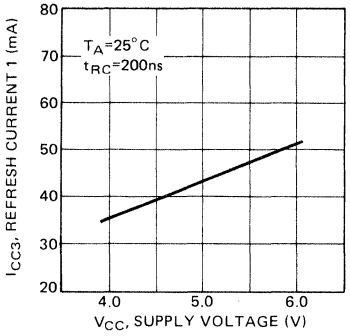


Fig. 13 – NIBBLE MODE CURRENT vs CYCLE RATE

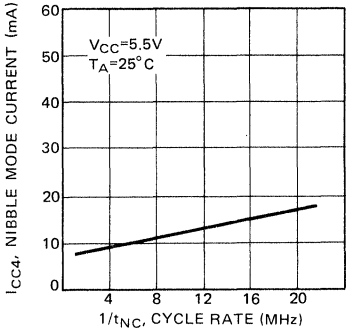


Fig. 14 – NIBBLE MODE CURRENT vs SUPPLY VOLTAGE

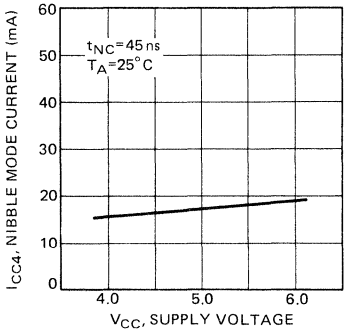


Fig. 15 – REFRESH CURRENT 2 vs CYCLE RATE

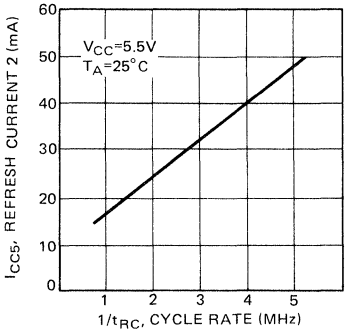


Fig. 16 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

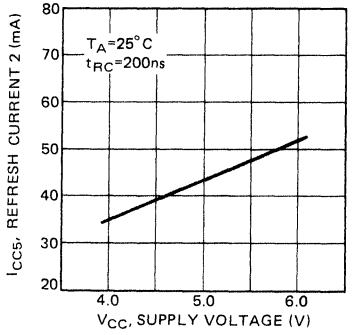


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

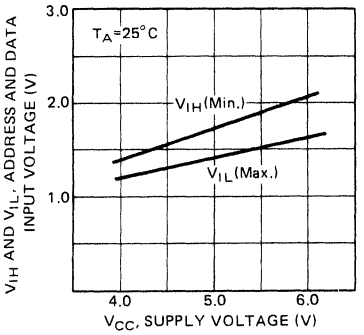


Fig. 18 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

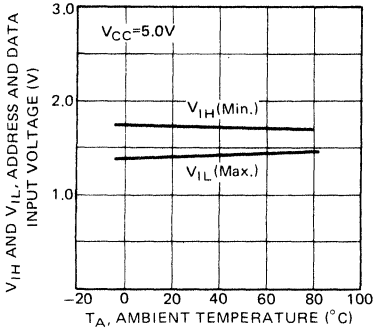


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

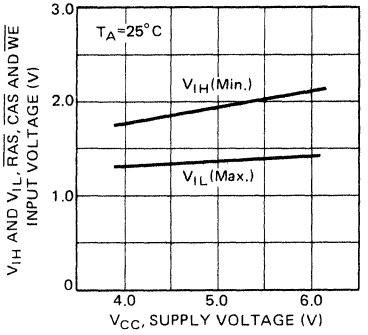


Fig. 20 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

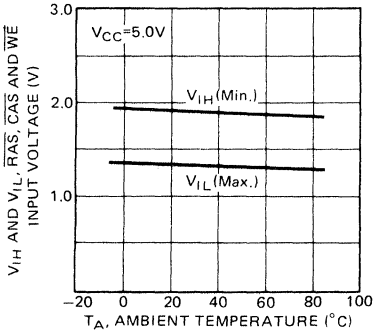
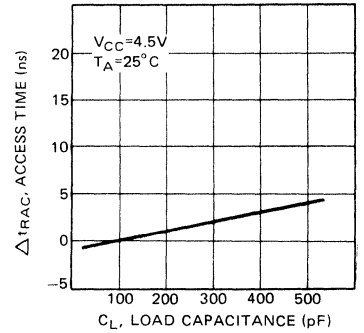


Fig. 21 – ACCESS TIME vs LOAD CAPACITANCE



1

Fig. 22 – OUTPUT CURRENT vs OUTPUT VOLTAGE

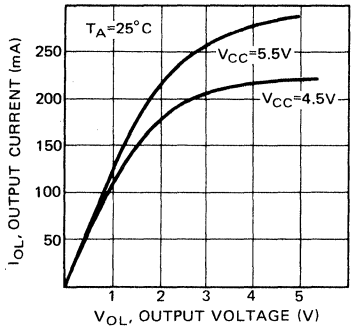


Fig. 23 – OUTPUT CURRENT vs OUTPUT VOLTAGE

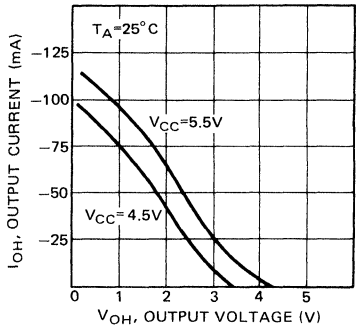


Fig. 24 – CURRENT WAVEFORM DURING POWER UP

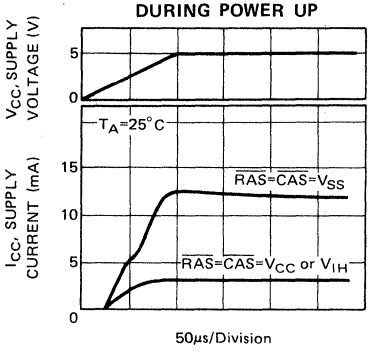
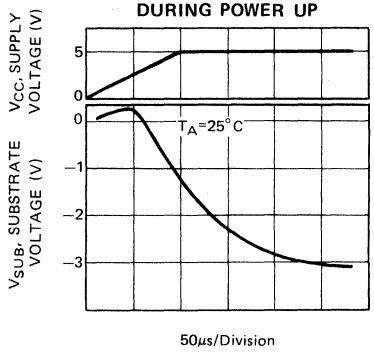
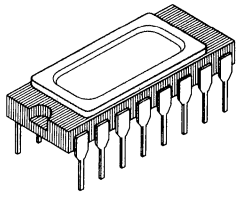


Fig. 25 – SUBSTRATE VOLTAGE DURING POWER UP



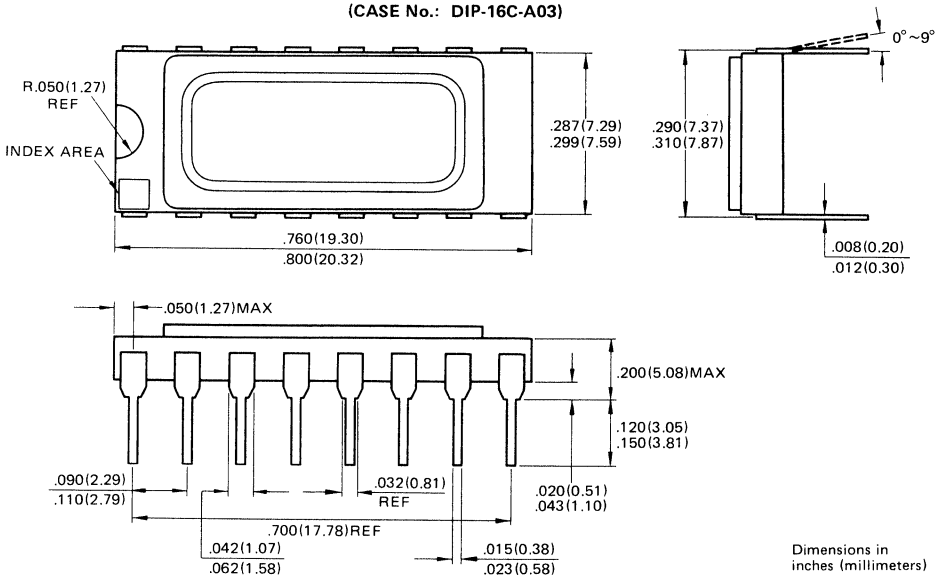
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A03

16-DEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-A03)

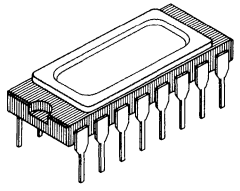


Dimensions in inches (millimeters)

1

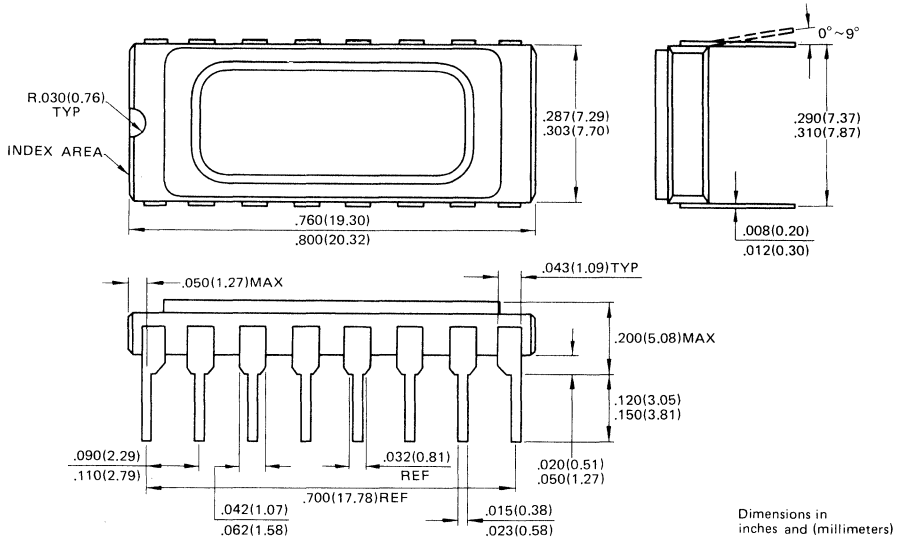
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -C)



DIP-16C-A04

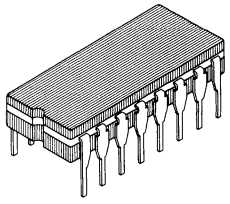
16-LEAD SEAM WELD DIP PACKAGE
(CASE No.: DIP-16C-A04)



Dimensions in inches and (millimeters)

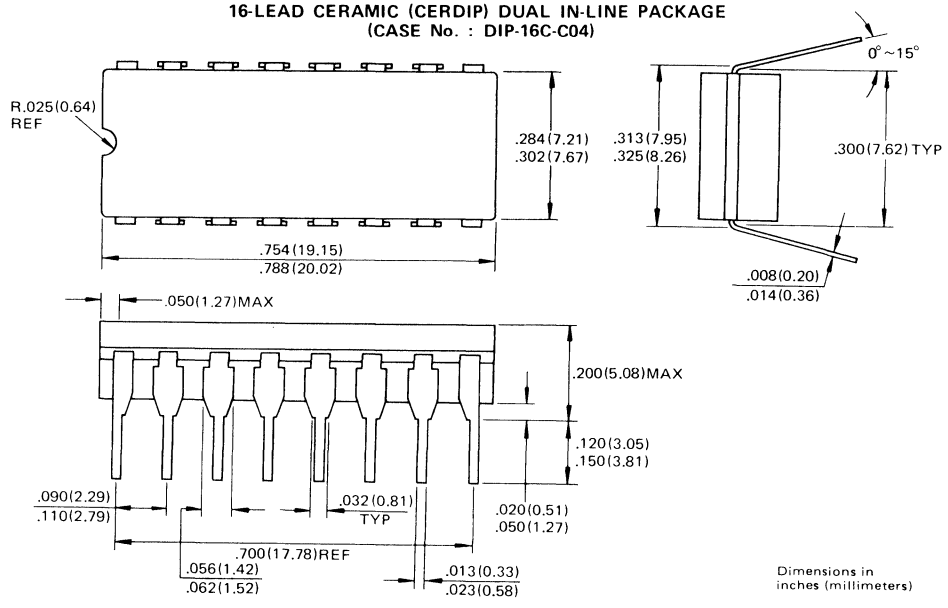
PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Suffix: -Z)



DIP-16C-C04

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C04)

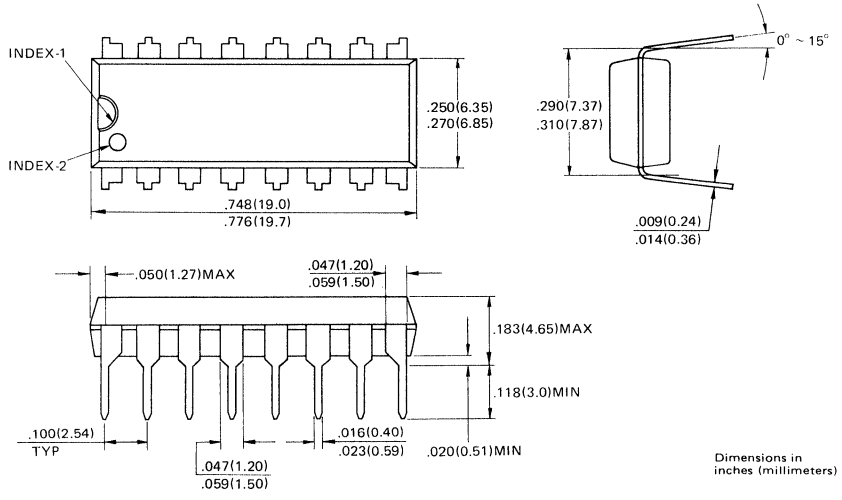


1

PACKAGE DIMENSIONS

Standard 16-pin Plastic DIP (Suffix: -P)

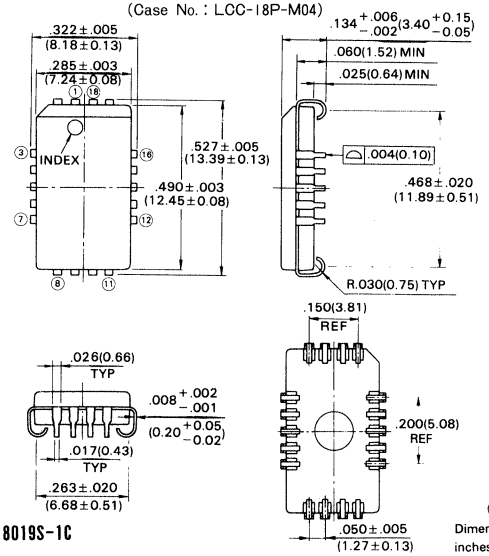
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Dimensions in inches (millimeters)

Standard 18-pin Plastic LCC (Suffix: -PV)

18-LEAD PLASTIC LEADED CHIP CARRIER
(Case No. : LCC-18P-M04)



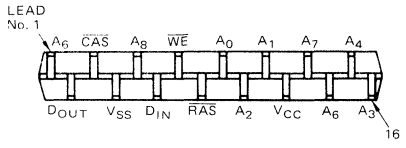
(No.): LEAD No.
Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS

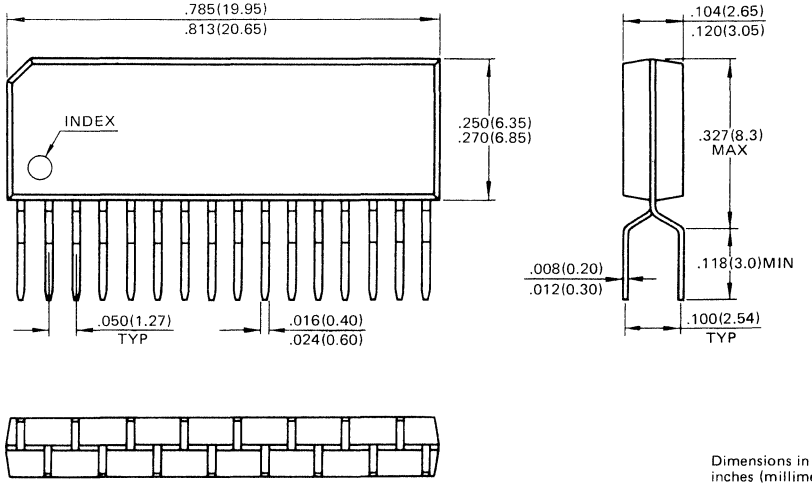
Standard 16-Pin Plastic ZIP(Suffix: -PSZ)

PIN ASSIGNMENT



ZIP-16P-M01

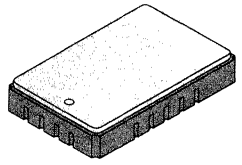
16 LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-16P-M01)



Dimensions in
inches (millimetres)

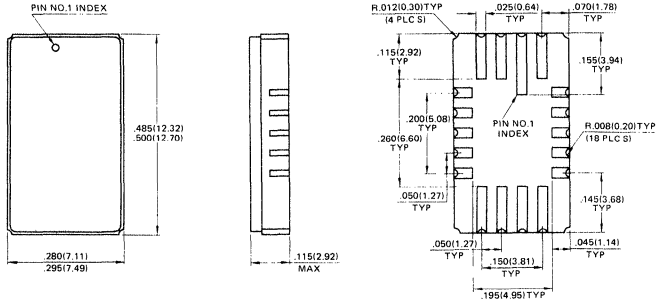
PACKAGE DIMENSIONS

Standard 18-pin Ceramic LCC (Suffix: -TV)



LCC-18C-F04

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F04)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches (millimeters).

FUJITSU

MOS 262144-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 81464-10
MB 81464-12
MB 81464-15

June 1987
Edition 4.0

65,536 x 4 DYNAMIC RANDOM ACCESS MEMORY

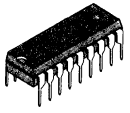
The Fujitsu MB 81464 is fully decoded, dynamic random access memory organized as 65,536 words by 4-bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and system memory for microprocessor unit where low power dissipation and compact layout is required.

The multiplex row and column address inputs permit the MB 81464 to be housed in a standard 18 pin DIP, 18 pin PLCC, and 20 pin ZIP. Additionally the MB 81464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. The "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh cycle is provided an on chip refresh capability. MB 81464 also features "page mode" which allows high speed random access to up 256 bits within a same row.

The MB 81464 is fabricated using silicon gate NMOS and Fujitsu's advanced "Triple Layer Polysilicon" process technology. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

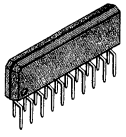
The clock timing requirements are non critical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 65,536 x 4 DRAM, 18 pin DIP, 18 pin PLCC, and 20 pin ZIP.
- Silicon gate, Triple Poly NMOS, single transistor cell.
- Row access time (t_{RAC}),
  100 ns max. (MB 81464-10)
  120 ns max. (MB 81464-12)
  150 ns max. (MB 81464-15)
- Cycle time (t_{RC}),
  200 ns min. (MB 81464-10)
  220 ns min. (MB 81464-12)
  260 ns min. (MB 81464-15)
- Page cycle time (t_{PC}),
  100 ns min. (MB 81464-10)
  120 ns min. (MB 81464-12)
  145 ns min. (MB 81464-15)
- Single +5V supply, 10% tolerance
  Low power,
  385 mW max. (MB 81464-10)
  358 mW max. (MB 81464-12)
  314 mW max. (MB 81464-15)
  27.5 mW max. (Standby)
- On chip substrate bias generator for high performance
- All inputs/outputs are TTL compatible
- 4 ms/256 refresh cycles
- Early write or $\overline{\text{OE}}$ controlled write capacity
- "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$", $\overline{\text{RAS}}$-only and hidden refresh capability
- Read write capability
- On chip latches for addresses and DQs.
- Compatible with μPD41254, HM50464, and TM4464
- Stanadard 18-pin Ceramic (Metal Seal) DIP (Suffix: -C)
- Standard 18-pin Plastic DIP: (Suffix: -P)
- Standard 18 pin PLCC (Suffix: -PD)
- Standard 20 pin ZIP (Suffix: -PSZ)



PLASTIC PACKAGE
DIP-18P-M03

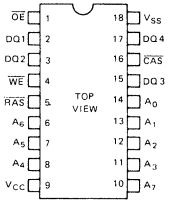
PLASTIC PACKAGE
LCC-18P-M02

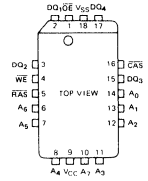


PLASTIC PACKAGE
ZIP-20P-M01

DIP-18C-A01: See Page 22

PIN ASSIGNMENT





Pin assignment for ZIP: See page 21

ABSOLUTE MAXIMUM RATING (See NOTE)

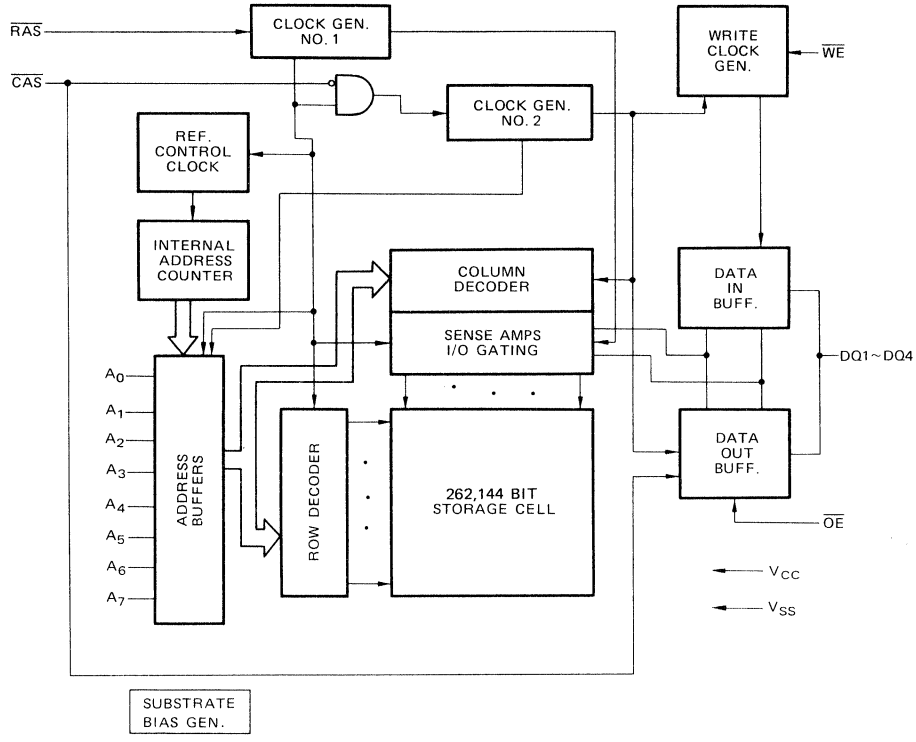
Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB 81464 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance A_0 to A_7	C_{IN1}	–	7	pF
Input Capacitanct $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	–	10	pF
Data I/O Capacitance (DQ1 to DQ4)	C_{DQ}	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	-2.0	–	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	-1.0	–	0.8	V	

* The device will withstand undershoots to the -2.0 V level with a maximum pulse width of 20 ns at the -1.5 V level.

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81464-10	I_{CC1}			70	mA
	MB 81464-12				65	
	MB 81464-15				57	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}			5.0	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81464-10	I_{CC3}			60	mA
	MB 81464-12				55	
	MB 81464-15				50	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling; t_{PC} = min)	MB 81464-10	I_{CC4}			40	mA
	MB 81464-12				35	
	MB 81464-15				30	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81464-10	I_{CC5}			65	mA
	MB 81464-12				60	
	MB 81464-15				55	
INPUT LEAKAGE CURRENT any input (0V ≦ V_{IN} ≦ 5.5V, 4.5V ≦ V_{CC} ≦ 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	-10		10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0 V ≦ V_{OUT} ≦ 5.5 V)		$I_{DQ(L)}$	-10		10	μA
OUTPUT LEVEL Output High Voltage (I_{OH} = -5 mA)		V_{OH}	2.4			V
OUTPUT LEVEL Output Low Voltage (L_{OL} = 4.2 mA)		V_{OL}			0.4	V

* : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
I_{CC} is dependent on input low voltage level V_{ILD}, V_{ILD} > -0.5 V.

1

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 81464-10		MB 81464-12		MB 81464-15		Unit
		Min	Max	Min	Max	Min	Max	
Time between Refresh	t_{REF}		4		4		4	ms
Random Read/Write Cycle Time	t_{RC}	200		220		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	270		305		345		ns
Page Mode Cycle Time	t_{PC}	100		120		145		ns
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	170		195		225		ns
Access Time from $\overline{RAS}$ 4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$ 5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay	t_{OFF}	0	25	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time	t_{RP}	80		90		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	100	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	50		60		75		ns
$\overline{CAS}$ Precharge Time (Page mode only)	t_{CP}	40		50		60		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)	t_{CPN}	30		32		35		ns
$\overline{CAS}$ Pulse Width	t_{CAS}	50	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time	t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time 7 8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	10		10		10		ns
Row Address Set Up Time	t_{ASR}	0		0		0		ns
Row Address Hold Time	t_{RAH}	10		12		15		ns
Column Address Set Up Time	t_{ASC}	0		0		0		ns
Column Address Hold Time	t_{CAH}	15		20		25		ns
Read Command Set Up Time	t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ 9	t_{RRH}	10		15		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$ 9	t_{RCH}	0		0		0		ns
Write Command Set Up Time 10	t_{WCS}	–5		–5		–5		ns
Write Command Hold Time	t_{WCH}	25		30		35		ns
Write Command Pulse Width	t_{WP}	25		30		35		ns
Write Command to $\overline{RAS}$ Lead Time 10	t_{RWL}	35		40		45		ns

AC CHARACTERISTICS (cont'd)

(At recommended operating conditions unless otherwise noted.)

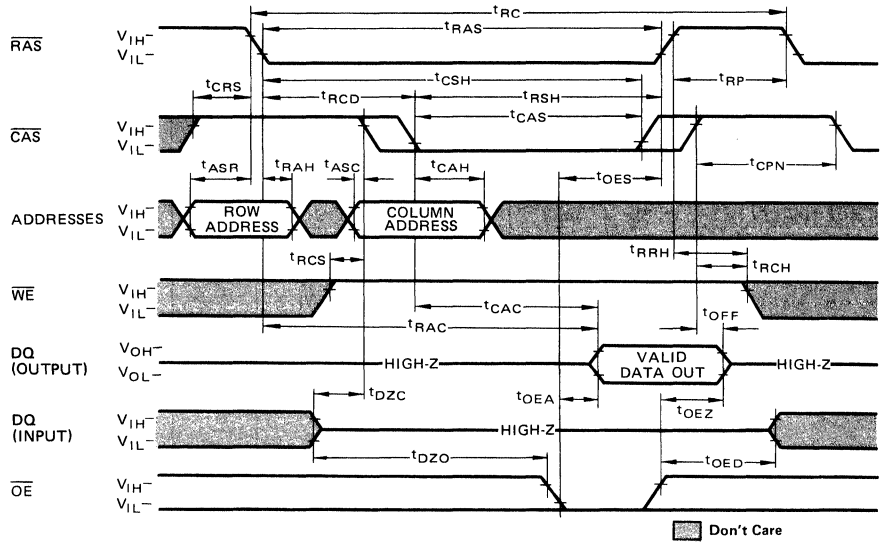
Parameter	NOTES	Symbol	MB 81464-10		MB 81464-12		MB 81464-15		Unit
			Min	Max	Min	Max	Min	Max	
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	25		30		35		ns
Access Time from $\overline{OE}$		t_{OEA}		27		30		40	ns
$\overline{OE}$ to Data In Delay Time		t_{OED}	25		25		30		ns
Output Buffer Turn Off Delay from $\overline{OE}$		t_{OEZ}	0	25	0	25	0	30	ns
$\overline{OE}$ Hold Time Referenced to $\overline{WE}$		t_{OEH}	0		0		0		ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCS}	20		20		20		ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)		t_{FCH}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time (Refresh cycles)		t_{RPC}	10		10		10		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycles)		t_{CPR}	30		30		30		ns
$\overline{OE}$ to $\overline{RAS}$ in active Set Up Time		t_{OES}	0		0		0		ns
D_{IN} to $\overline{CAS}$ Delay Time	11	t_{DZC}	0		0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	11	t_{DZO}	0		0		0		ns
Refresh Counter Test Cycle Time	12	t_{RTC}	375		430		505		ns
Refresh Counter Test Cycle $\overline{RAS}$ Pulse Width	12	t_{TRAS}	285	10000	330	10000	395	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	12	t_{CPT}	50		60		70		ns

Notes:

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5 ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. Even if $t_{WCS} \leqq t_{WCS}$(min), the write cycle can be excuted by satisfying t_{RWL} or t_{CWL} specification.
11. Either t_{DZC} or t_{DRO} must be satisfied for all cycles.
12. Refresh Counter Test Cycle only.

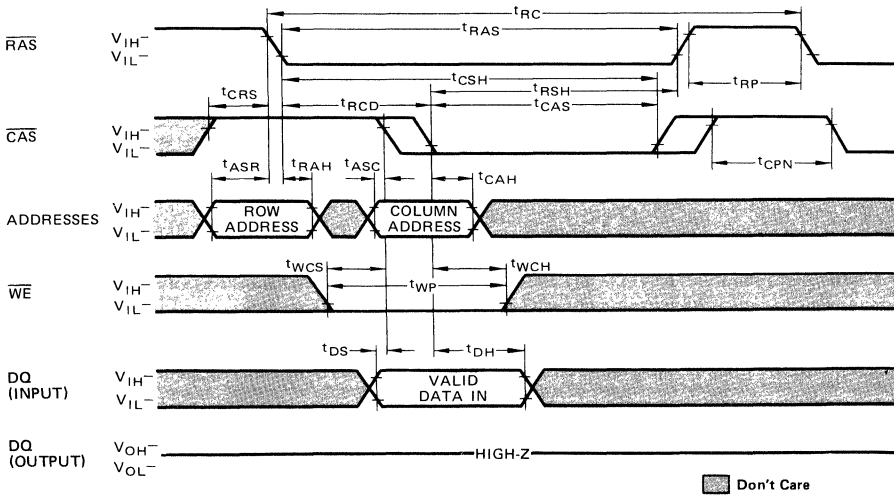
1

Read Cycle

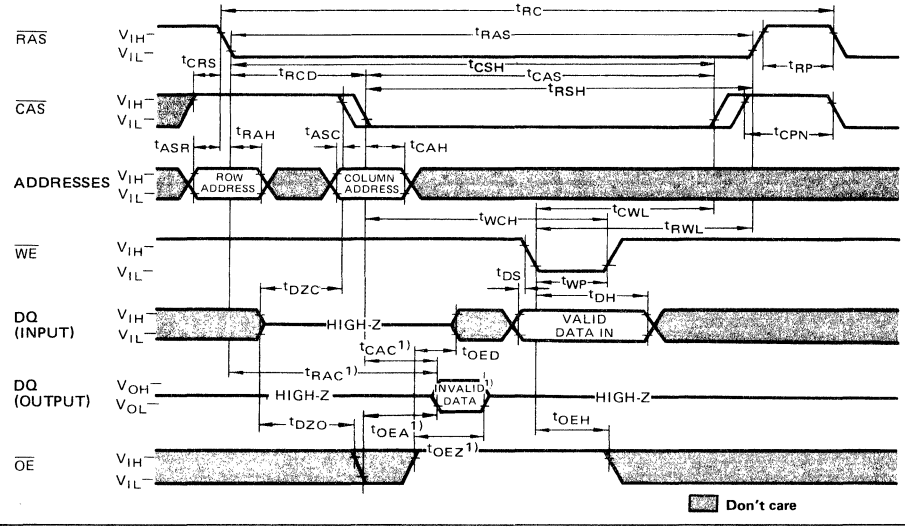


Write Cycle (Early Write)

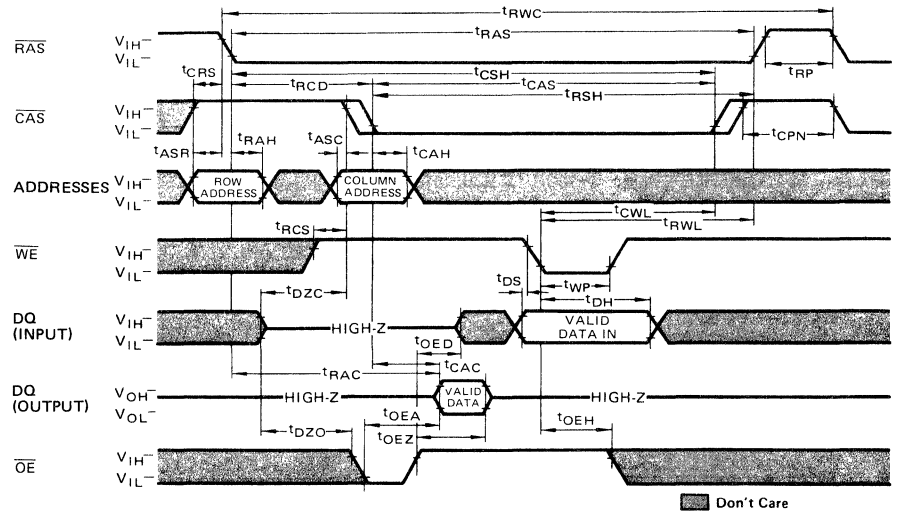
$\overline{OE}$: Don't care



$\overline{OE}$ Write Cycle



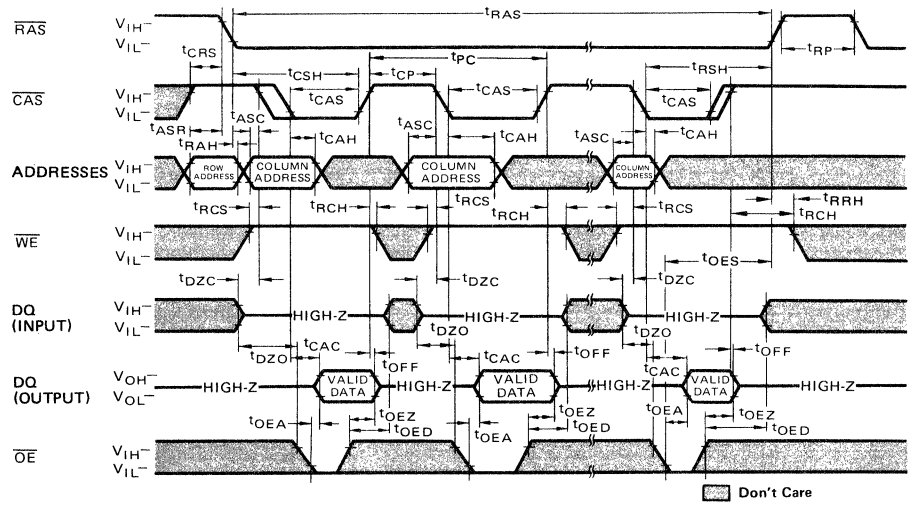
Read-Modify-Write Cycle



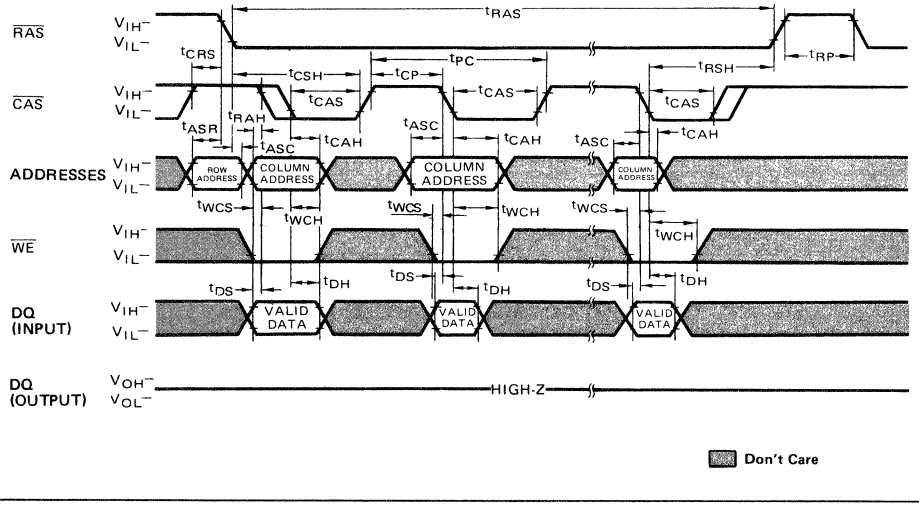
Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

1

Page Mode Read Cycle

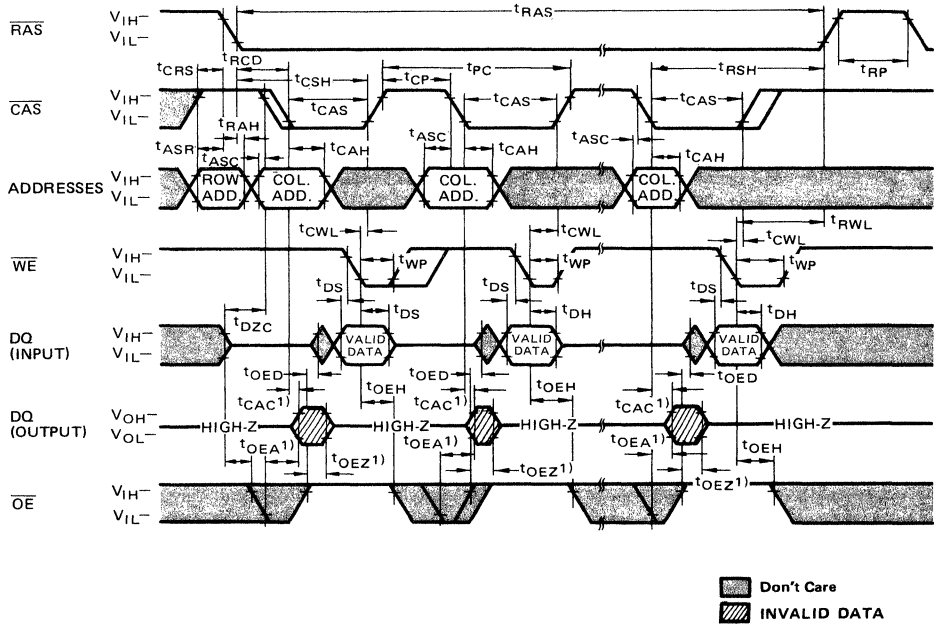


Page Mode Write Cycle
(OE=Don't Care)



1

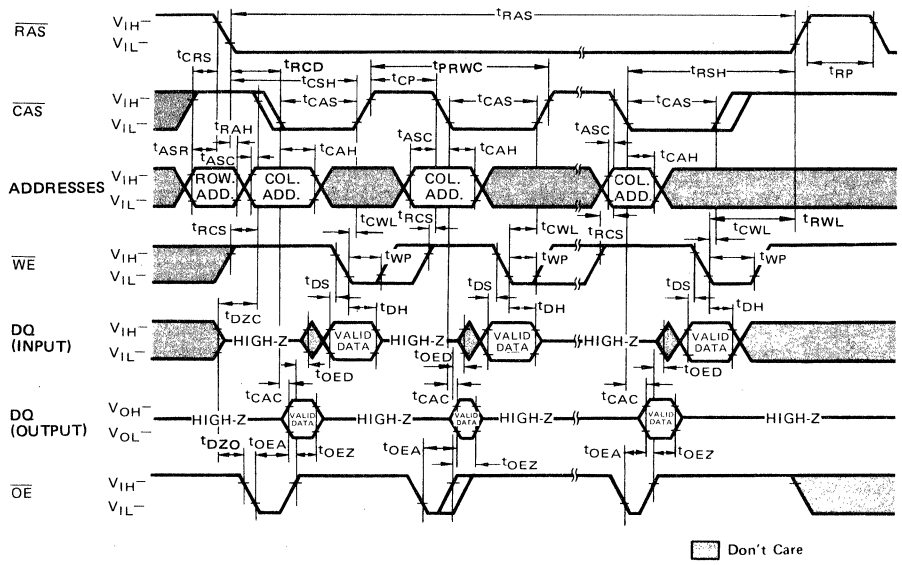
Page Mode $\overline{OE}$ Write Cycle



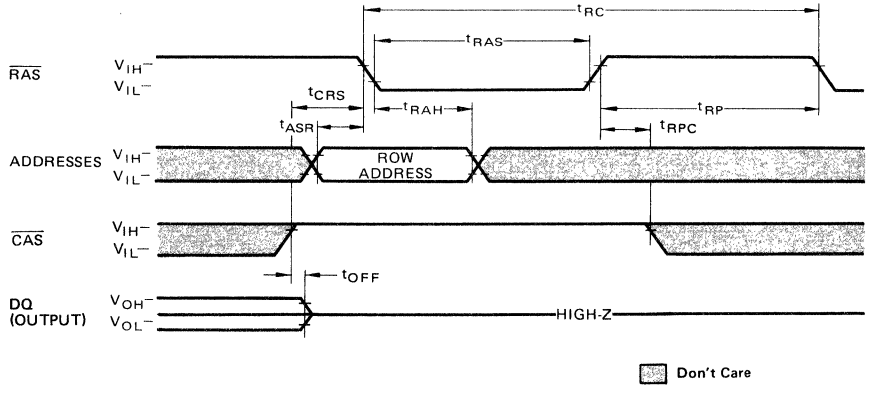
Note: 1) When $\overline{OE}$ is kept high through a cycle, the DQ pins are kept high-Z state.

1

Page Mode Read Modify-Write Cycle



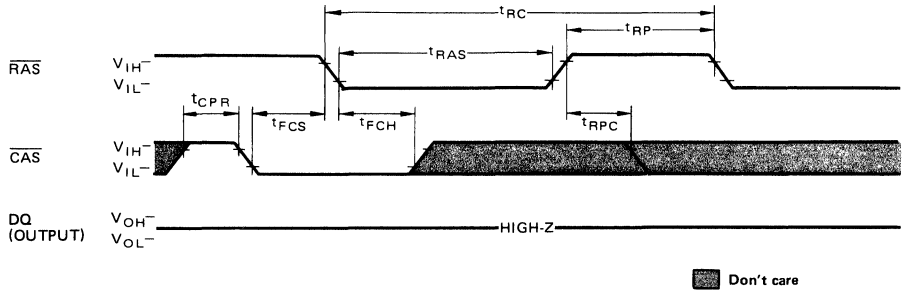
RAS-Only Refresh Cycle
(WE, OE=Don't Care)



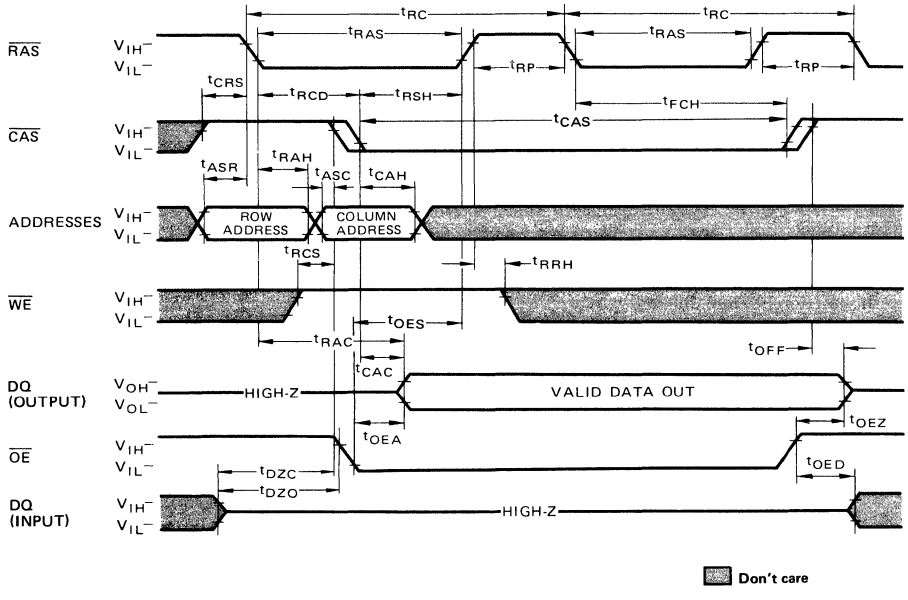
1

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE: Addresses, $\overline{WE}$, $\overline{OE}$ = Don't care

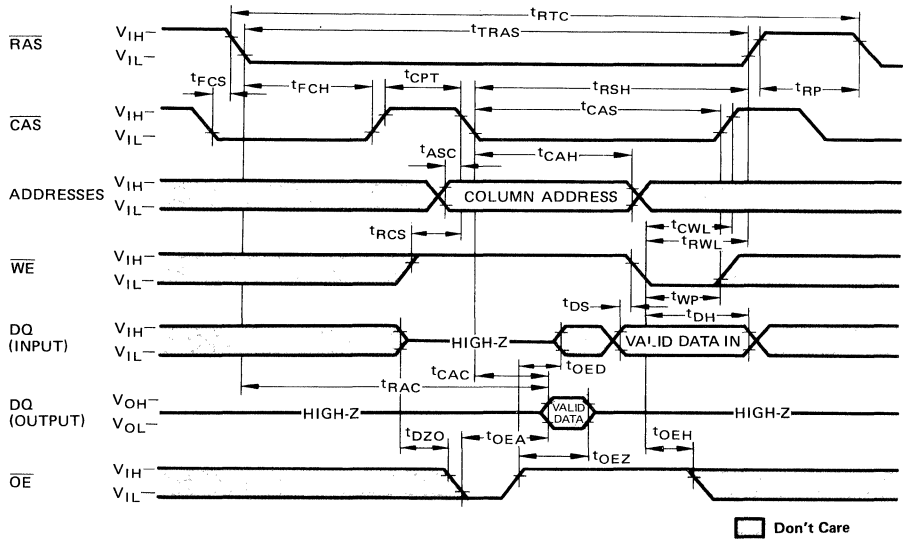


Hidden Refresh Cycle



1

Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode parallel 4 bits of 262,144 storage cell locations within the MB 81464.

Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins (A_0 through A_7) and latched with the Column Address Strobe ($\overline{CAS}$).

The row and column address inputs must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the Write Enable ($\overline{WE}$) input. A high on $\overline{WE}$ selects read mode and low selects write mode. The data inputs are disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data-outs will remain in the high-impedance state allowing a write cycle.

Data Pins:

Data Inputs;

Data are written during a write or read-modify-write cycle. The later falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed by $\overline{CAS}$ with setup and hold times referenced to $\overline{CAS}$. In a read-modify-write cycle, thus the data will be strobed by $\overline{WE}$ with set-up and hold times referenced to $\overline{WE}$.

In a read-modify-write cycle, $\overline{OE}$ must be low after t_{DZO} to change the data pins from input mode to output mode and then $\overline{OE}$ must be changed to low before t_{OED} to return the data pins to input mode. In an early write cycle, data pins are in input mode regardless of the status of $\overline{OE}$.

Data Outputs;

The three-state output buffers provide direct TTL compatibility with a fan out of two standard TTL loads. Data-out are the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{OE}$ are low. In a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high brings the outputs into the high impedance state.

Output Enable:
The $\overline{OE}$ controls the impedance of the output buffers. In the high state on $\overline{OE}$, the output buffers are high impedance state. In the low state on $\overline{OE}$, the output buffers are low impedance state. But in early write cycle, the output buffers are in high impedance state even if $\overline{OE}$ is low. In the page mode read cycle, $\overline{OE}$ can be allowed low through the cycle. In the page mode early write cycle, $\overline{OE}$ can be allowed high throughout the cycle. In the page mode read-modify-write or delayed write cycle, $\overline{OE}$ must be changed from low to high with t_{OED}.

Page Mode:
Page Mode operation permits strobing the row-address into the MB 81464 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh;
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 through A_7) at least every four milliseconds.
The MB 81464 offeres the following three types of refresh.

$\overline{RAS}$-Only Refresh:
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffuers are in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81464 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and a internal refresh operation takes place.
After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh:
Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time.
In MB 81464, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses i.e., it doesn't need to apply refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in the cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed can be defined as follows:

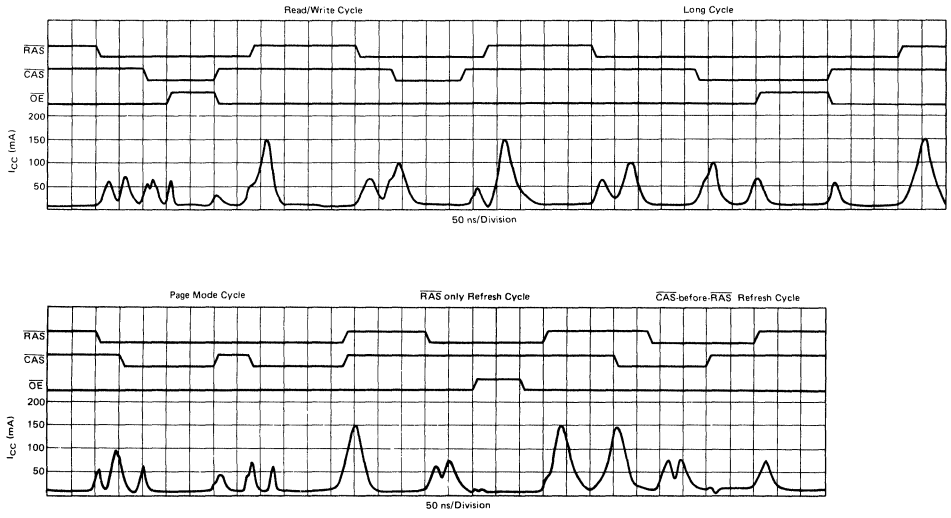
*A ROW ADDRESS – All bits are defined by the refresh counter.
*A COLUMN ADDRESS – All the bits A_0 to A_7 are defined by latching levels on A_0 to A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for the following operations:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3) and check, and simultaneously write "high" to the same address by using internal refresh counter test cycles. This step is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

1

Fig. 2 – CURRENT WAVEFORM (V_{CC} = 5.5 V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

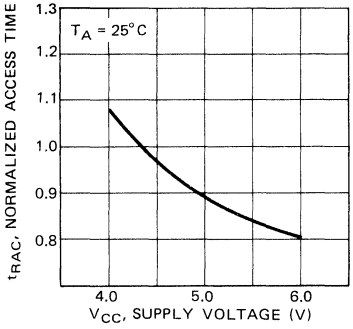


Fig. 4 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

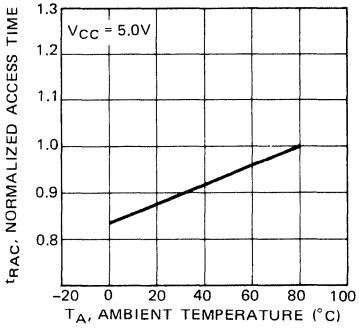


Fig. 5 – OPERATING CURRENT vs. CYCLE RATE

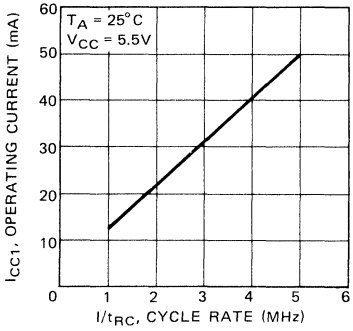


Fig. 6 – OPERATING CURRENT vs. SUPPLY VOLTAGE

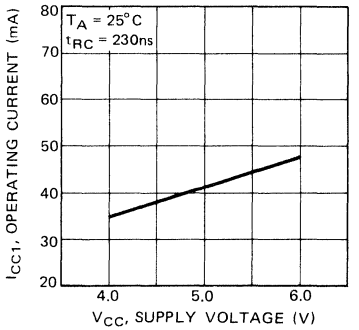


Fig. 7 – OPERATING CURRENT vs. AMBIENT TEMPERATURE

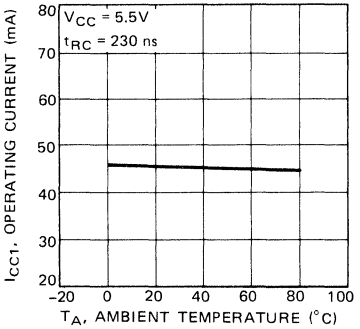
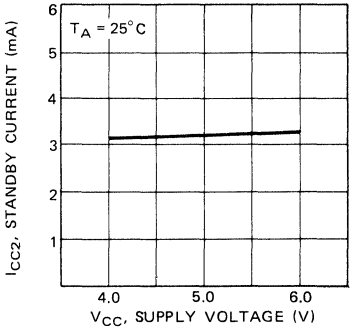


Fig. 8 – STANDBY CURRENT vs. SUPPLY VOLTAGE



1

Fig. 9 – STANDBY CURRENT vs. AMBIENT TEMPERATURE

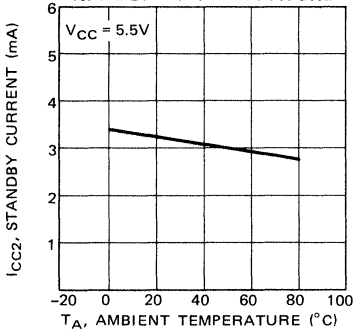


Fig. 10 – REFRESH CURRENT 1 vs. CYCLE RATE

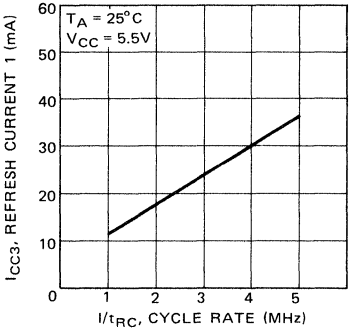


Fig. 11 – REFRESH CURRENT 1 vs. SUPPLY VOLTAGE

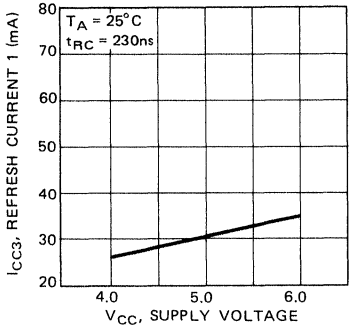


Fig. 12 – PAGE MODE CURRENT vs. CYCLE RATE

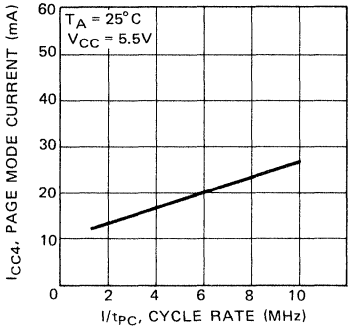


Fig. 13 – PAGE MODE CURRENT vs. CYCLE RATE

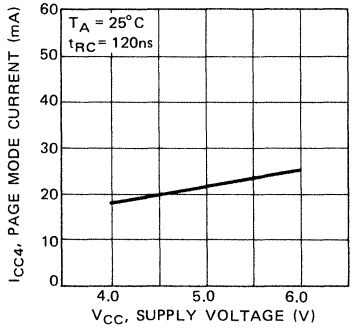


Fig. 14 – REFRESH CURRENT 2 vs. CYCLE RATE

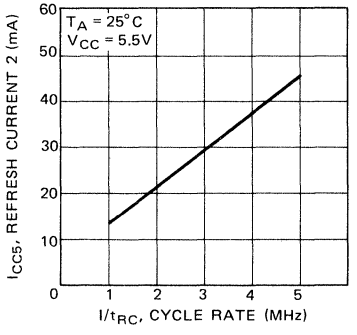


Fig. 15 – REFRESH CURRENT 2 vs. SUPPLY VOLTAGE

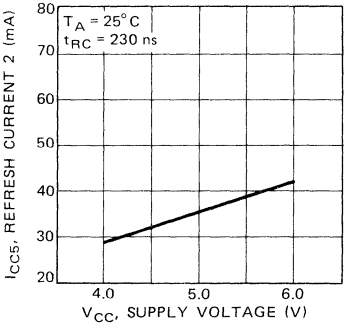


Fig. 16 – ADDRESS AND DATA INPUT VOLTAGE vs. SUPPLY VOLTAGE

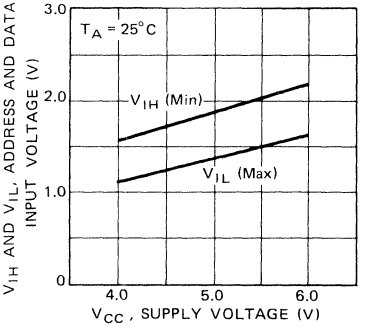


Fig. 17 – ADDRESS AND DATA INPUT VOLTAGE vs. AMBIENT TEMPERATURE

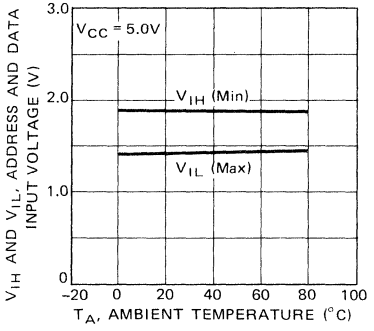


Fig. 18 – $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. SUPPLY VOLTAGE

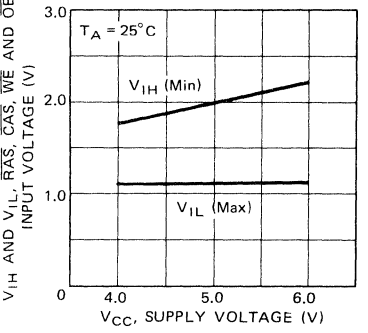


Fig. 19 – $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. AMBIENT TEMPERATURE

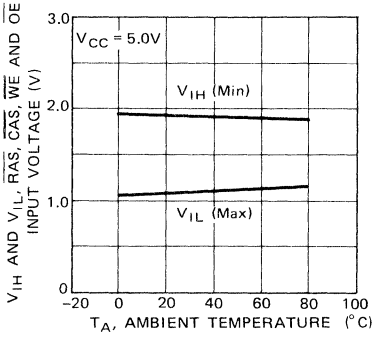
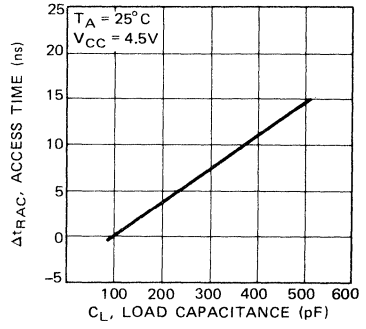


Fig. 20 – ACCESS TIME vs. LOAD CAPACITANCE



1

Fig. 21 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

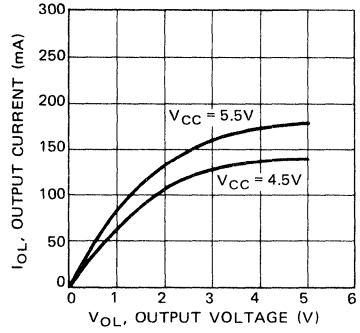


Fig. 22 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

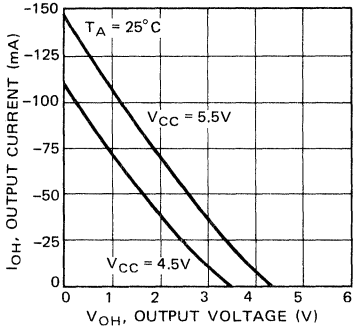


Fig. 23 – SUBSTRATE VOLTAGE DURING POWER UP

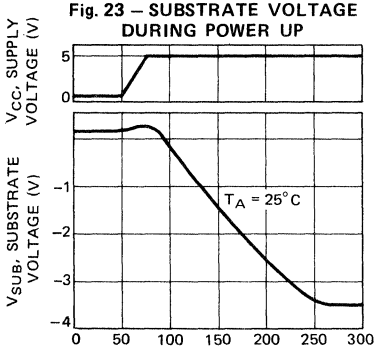
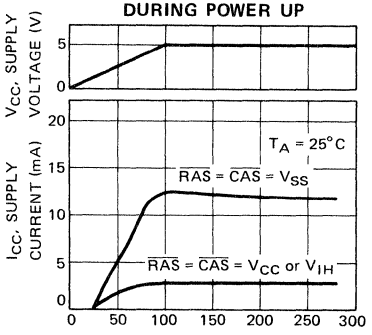


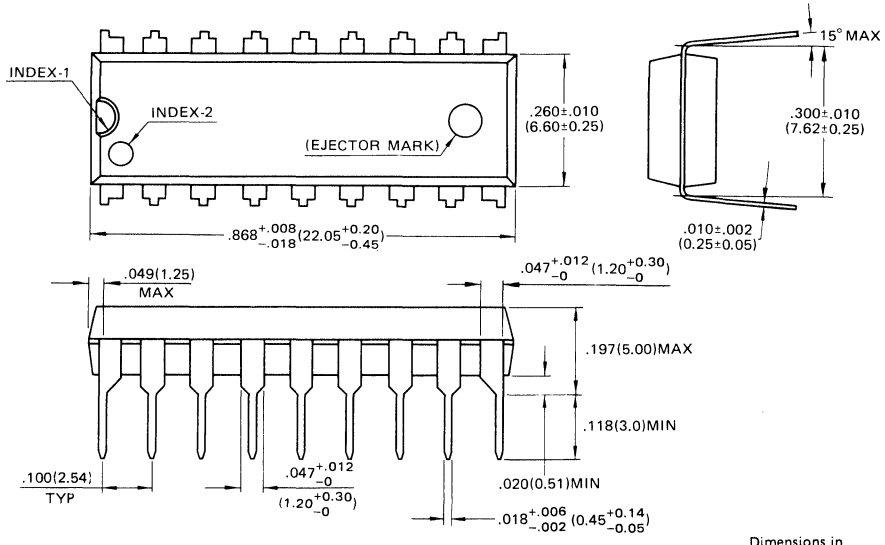
Fig. 24 – CURRENT WAVEFORM DURING POWER UP



PACKAGE DIMENSIONS

(Suffix: -P)

18 LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M03)



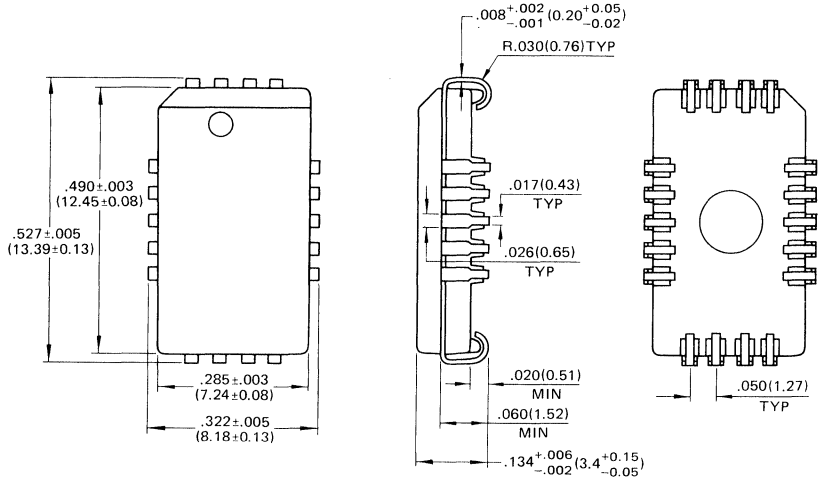
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PD)

1

18-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-18P-M02)

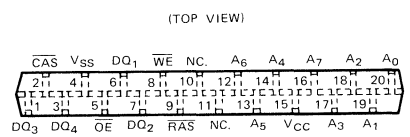


Dimensions in
inches (millimeters)

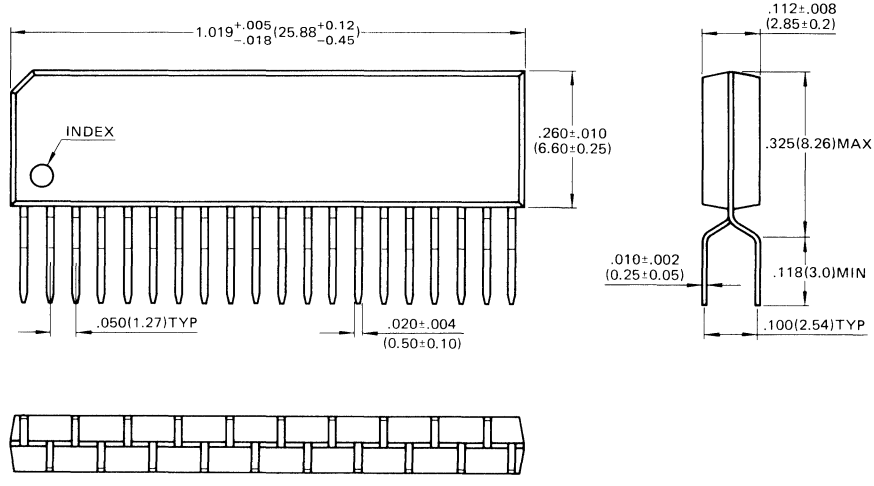
1

PACKAGE DIMENSIONS

(Suffix: -PSZ)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE NO.: ZIP-20P-M01)

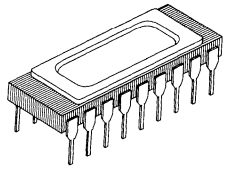


Dimensions in
inches (millimeters)

1

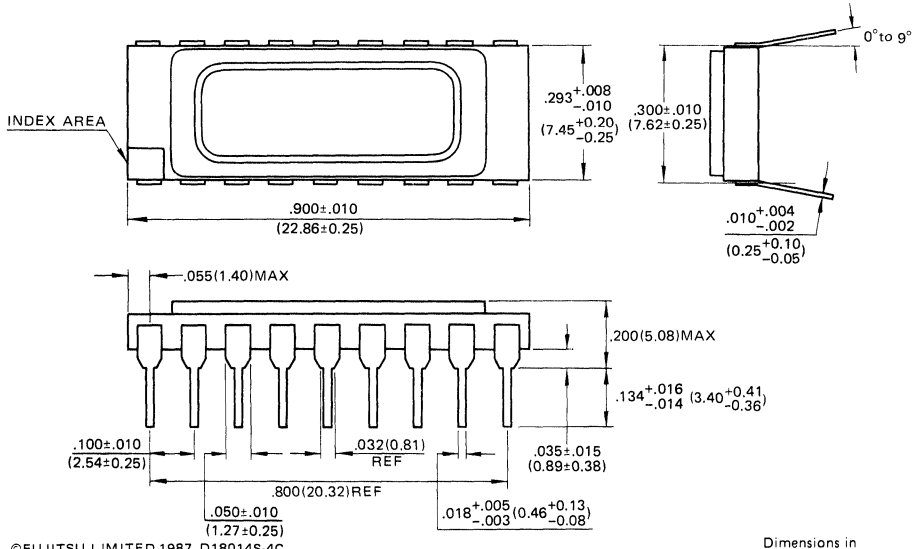
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Dimensions in inches (millimeters)

CMOS DRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
2–3	MB81C258–10	100	262144 bits	16-pin Plastic DIP
	–12	120	(262144w x 1b)	18-pin Plastic LCC
	–15	150		
2-25	MB81C466–10	100	262144 bits	18-pin Plastic DIP
	–12	120	(65536w x 4b)	18-pin Ceramic DIP
	–15	150		20-pin Plastic ZIP
2-41	MB81C1000–70	70	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576w x 1b)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
	–12	120		26-pin Plastic LCC
2-61	MB81C1000A–60	60	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576w x 1b)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
				26-pin Plastic LCC
2-63	MB81C1001–70	70	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576w x 1b)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
	–12	120		26-pin Plastic LCC
2-83	MB81C1001A–60	60	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576w x 1b)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
				26-pin Plastic LCC
2-85	MB81C1002–70	70	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576w x 1b)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
	–12	120		26-pin Plastic LCC
2-109	MB81C1002A–60	60	1048576 bits	18-pin Plastic DIP
	–80	80	(1048576w x 1b)	18-pin Ceramic DIP
	–10	100		20-pin Plastic ZIP
				26-pin Plastic LCC
2-111	MB81C4256–70	60	1048576 bits	20-pin Plastic DIP
	–80	80	(262144w x 4b)	20-pin Ceramic DIP, ZIP
	–10	100		26-pin Plastic LCC
	–12	120		
2-135	MB81C4256A–60	60	1048576 bits	20-pin Plastic DIP, ZIP
	–80	80	(262144w x 4b)	20-pin Ceramic DIP
	–10	100		26-pin Plastic LCC
2–137	MB81C4257–85	85	1048576 bits	20-pin Plastic DIP,ZIP
	–10	100	(262144w x 4b)	20-pin Ceramic DIP
	–12	120		26-pin Plastic LCC
2-161	MB81C4258–70	70	1048576 bits	20-pin Plastic DIP, ZIP
	–80	80	(262144w x 4b)	20-pin Ceramic DIP
	–10	100		26-pin Plastic LCC
	–12	120		
2-185	MB81C4258A–60	60	1048576 bits	20-pin Plastic DIP, ZIP
	–80	80	(262144w x 4b)	20-pin Ceramic DIP
	–10	100		26-pin Plastic LCC
2-187	MB814100 –80	80	4194304 bits	18-pin Plastic DIP
	–10	100	(4194304w x 1b)	20-pin Plastic ZIP
	–12	120		26-pin Plastic LCC
2-207	MB814400–80	80	4194304 bits	20-pin Plastic DIP, ZIP
	–10	100	(1048576 x 4b)	26-pin Plastic LCC
	–12	120		

2

FUJITSU

262144 BIT CMOS STATIC COLUMN DYNAMIC RAM

MB81C258-10
MB81C258-12
MB81C258-15

October 1988
Edition 3.0

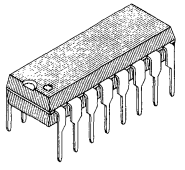
262,144 x 1 BIT CMOS STATIC COLUMN DYNAMIC RAM

The Fujitsu MB 81C258 is CMOS static column dynamic random access memory, SC-DRAM, which is organized as 262144 word by 1 bit. This SC-DRAM is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required.

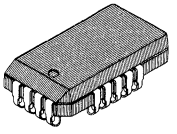
The advantage of SC-DRAM is achieving the static mode operation such as read, write and read-modify-write cycles in spite of dynamic RAM and the fast read and write operation can be performed by this mode.

The MB 81C258 is fabricated using silicon gate CMOS process. Since the CMOS circuit dissipates very small power, it can be easily used in battery backed-up application system such as hand held computer.
The MB 81C258 is pin compatible with HM 51258.
All inputs and outputs are TTL compatible.

- 262144 x 1 SC-DRAM, 16-pin DIP/18-pin PLCC
- Silicon-gate, CMOS, single transistor cell
- Row Access Time (t_{RAC}),
  100 ns max. (MB 81C258-10)
  120 ns max. (MB 81C258-12)
  150 ns max. (MB 81C258-15)
- Random Cycle Time (t_{RC}),
  200 ns min. (MB 81C258-10)
  230 ns min. (MB 81C258-12)
  260 ns min. (MB 81C258-15)
- Address Access Time (t_{AA}),
  45 ns max. (MB 81C258-10)
  55 ns max. (MB 81C258-12)
  70 ns max. (MB 81C258-15)
- Static Mode Cycle Time (t_{SC}),
  50 ns min. (MB 81C258-10)
  60 ns min. (MB 81C258-12)
  75 ns min. (MB 81C258-15)
- Low Power Dissipation
  330 mW max. (MB 81C258-10)
  275 mW max. (MB 81C258-12)
  248 mW max. (MB 81C258-15)
  11 mW max. (TTL level input)
  1.65 mW max. (CMOS level input)
- Single 5V supply, ±10% tolerance
- 32 ms/256 refresh cycles
- $\overline{RAS}$-Only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh capability
- Standard 16-pin Plastic DIP (Suffix: -P)
- Standard 18-pin Plastic LCC (Suffix: -PD)

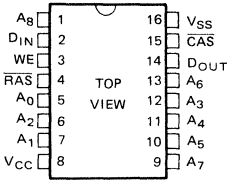


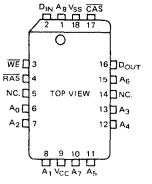
PLASTIC PACKAGE
DIP-16P-M03



PLASTIC PACKAGE
LCC-18P-M04

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

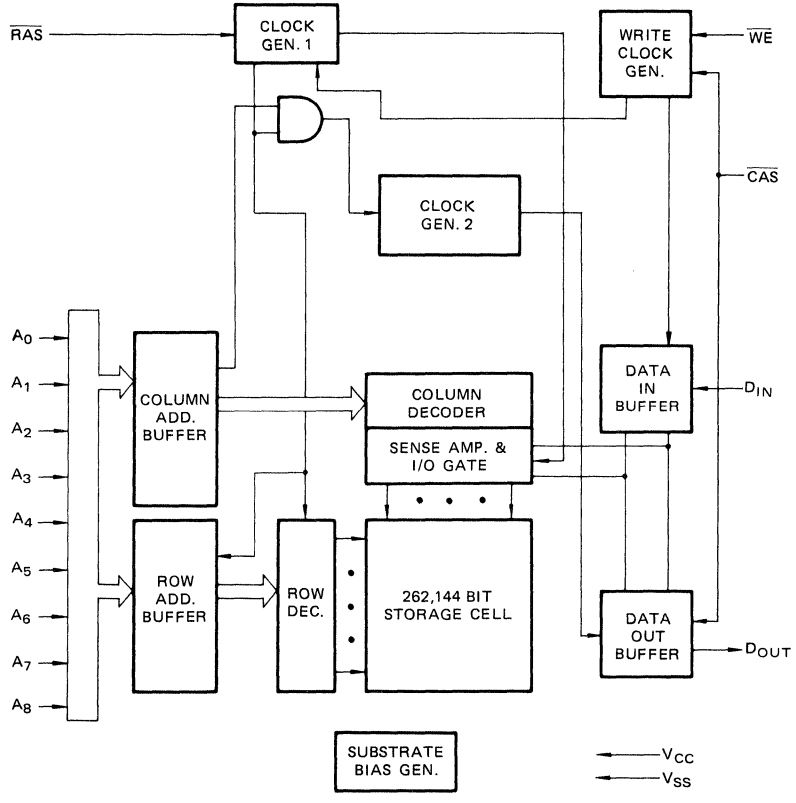
Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	−1 to +7	V
Storage Temperature	T_{STG}	−55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current		50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8 and D_{IN}	C_{IN1}	–	7	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	–	10	pF
Output Capacitance, D_{OUT}	C_{OUT}	–	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	–	0.8	V	

2

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

Parameter		Conditions	Symbol	Values		Unit
				Min	Max	
Operating Current* (Average power supply current)	MB81C258-10	$\overline{CAS}$ = V_{IL} or V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC1}	–	60	mA
	MB81C258-12			–	50	
	MB81C258-15			–	45	
Standby Current (Power supply current)	TTL level	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}	–	2.0	mA
	CMOS level	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC}-0.2V		–	0.3	
Static Mode Current*	MB81C258-10	$\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{RAS}$ cycling; t_{SC} = min.	I_{CC3}	–	40	mA
	MB81C258-12			–	35	
	MB81C258-15			–	30	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current* (Average power current)	MB81C258-10	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC4}	–	55	mA
	MB81C258-12			–	45	
	MB81C258-15			–	40	
Input Leakage Current		0V ≦ V_{IN} ≦ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V; pins not under test = 0V	$I_{I(L)}$	-10	10	μA
Output Leakage Current		0V ≦ V_{OUT} ≦ 5.5V; Data out disabled	$I_{O(L)}$	-10	10	
Output High Voltage		I_{OH} = -5mA	V_{OH}	2.4	–	V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}	–	0.4	

NOTE: *; I_{CC} depends on the output load operating speed. The specified values are with the output pin open.

AC CHARACTERISTICS

(At Recommended operating conditions unless otherwise noted) Notes 1, 2

Parameter NOTES	Symbol	MB 81C258-10		MB 81C258-12		MB 81C258-15		Unit
		Min	Max	Min	Max	Min	Max	
Time Between Refresh	t_{REF}	–	32	–	32	–	32	ms
Random Read/Write Cycle Time	t_{RC}	200	–	230	–	260	–	ns
Read-Modify-Write Cycle Time	t_{RWC}	245	–	285	–	325	–	ns
Access Time from $\overline{RAS}$ 3 5	t_{RAC}	–	100	–	120	–	150	ns
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	30	–	35	ns
Output Buffer Turn off Delay Time	t_{OFF}	0	25	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	3	50	ns
Column Address Access Time 4 5	t_{AA}	–	45	–	55	–	70	ns
Output Hold Time from Column Address Change	t_{AOH}	5	–	5	–	5	–	ns
Access Time from $\overline{WE}$ Precharge	t_{WPA}	–	25	–	30	–	35	ns
Access Time Relative to last Write 6	t_{ALW}	–	90	–	110	–	140	ns
Write Latched Data Hold Time	t_{WOH}	0	–	0	–	0	–	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	100	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	25	–	30	–	35		ns
$\overline{CAS}$ Pulse Width (Read)	t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ Pulse Width (Write)	t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ Hold Time (Read)	t_{CSH}	100	–	120	–	150	–	ns
$\overline{CAS}$ Hold Time (Write)	t_{CSH}	80	–	95	–	115	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	20	–	25	–	30	–	ns
Row Address Set Up Time	t_{ASR}	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns
Column Address Set Up Time 7	t_{ASC}	0	–	0	–	0	–	ns
Column Address Hold Time 7	t_{CAH}	20	–	25	–	30	–	ns
$\overline{RAS}$ to Column Address Delay Time 8 9	t_{RAD}	20	55	20	65	25	80	ns
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	100	–	120	–	150	–	ns
Write Address Hold Time Referenced to $\overline{RAS}$	t_{AWR}	80	–	90	–	110	–	ns
Read Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	–	55	–	70	–	ns
Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time 10	t_{AHR}	15	–	15	–	20	–	ns

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) **Notes 1, 2**

Parameter	NOTES	Symbol	MB 81C258-10		MB 81C258-12		MB 81C258-15		Unit
			Min	Max	Min	Max	Min	Max	
Last Write to Column Address Delay Time	11 12	t_{LWAD}	20	45	20	55	25	70	ns
Column Address Hold Time Referenced to Last Write		t_{AHLW}	90	–	110	–	140	–	ns
Read Command Set Up Time Referenced to $\overline{CAS}$		t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	10	–	10	–	10	–	ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0	–	0	–	0	–	ns
$\overline{WE}$ Pulse Width		t_{WP}	15	–	20	–	25	–	ns
$\overline{WE}$ Inactive Time		t_{WI}	15	–	20	–	25	–	ns
Write Command Hold Time		t_{WCH}	15	–	20	–	25	–	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	–	30	–	35	–	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	25	–	30	–	35	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	14	t_{RWD}	100	–	120	–	150	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	25	–	30	–	35	–	ns
Column Address to $\overline{WE}$ Delay Time		t_{AWD}	45	–	55	–	70	–	ns
$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	105	–	125	–	155	–	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	80	–	95	–	115	–	ns
$\overline{RAS}$ Precharge Time from Last Write		t_{RPLW}	135	–	155	–	165	–	ns
Write Set Up Time for Output Disable	14	t_{WS}	0	–	0	–	0	–	ns
Write Hold Time for Output Disable	14	t_{WH}	0	–	0	–	0	–	ns
D_{IN} Set Up Time		t_{DS}	0	–	0	–	0	–	ns
D_{IN} Hold Time		t_{DH}	20	–	25	–	30	–	ns
D_{IN} Hold Time Reference to $\overline{RAS}$		t_{DHR}	80	–	90	–	110	–	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20	–	25	–	30	–	ns

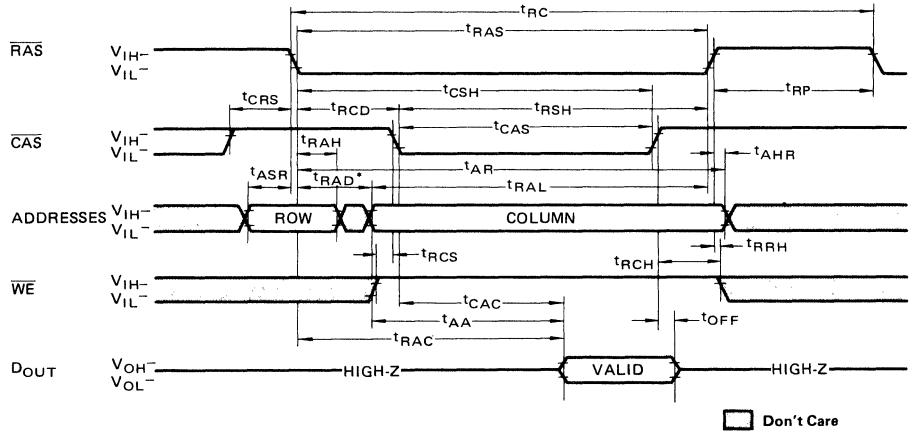
AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) Notes 1, 2

Parameter	NOTES	Symbol	MB 81C258-10		MB 81C258-12		MB 81C258-15		Unit
			Min	Max	Min	Max	Min	Max	
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20	–	25	–	30	–	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20	–	25	–	30	–	ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20	–	20	–	20	–	ns
Static Mode Read/Write Cycle Time		t_{SC}	50	–	60	–	75	–	ns
Static Mode Read-Modify-Write Cycle Time		t_{SRWC}	95	–	115	–	145	–	ns
Static Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	–	20	–	25	–	ns
Refresh Counter Test Cycle Time	15	t_{RTC}	440	–	520	–	610	–	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	15	t_{TRAS}	340	10000	410	10000	500	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	15	t_{CPT}	50	–	60	–	70	–	ns
Refresh Counter Test $\overline{CAS}$ to Col. Address Delay Time	15	t_{CADT}	–	100	–	120	–	150	ns
Refresh Counter Test Access Time from $\overline{CAS}$	15	t_{CACT}	–	135	–	165	–	205	ns
Refresh Counter Test $\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWDT}	135	–	165	–	205	–	ns

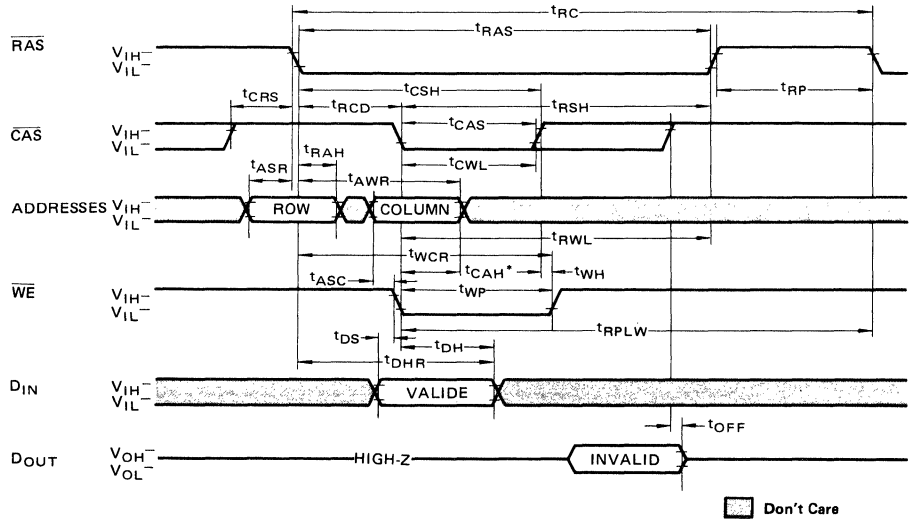
NOTES:
1. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
4. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
7. Write Cycle Only.
8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
9. t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5ns)
10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
12. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5ns).
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geq t_{RWD}$ (min), The data output will contain data read from the selected cell.
15. $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Read Cycle



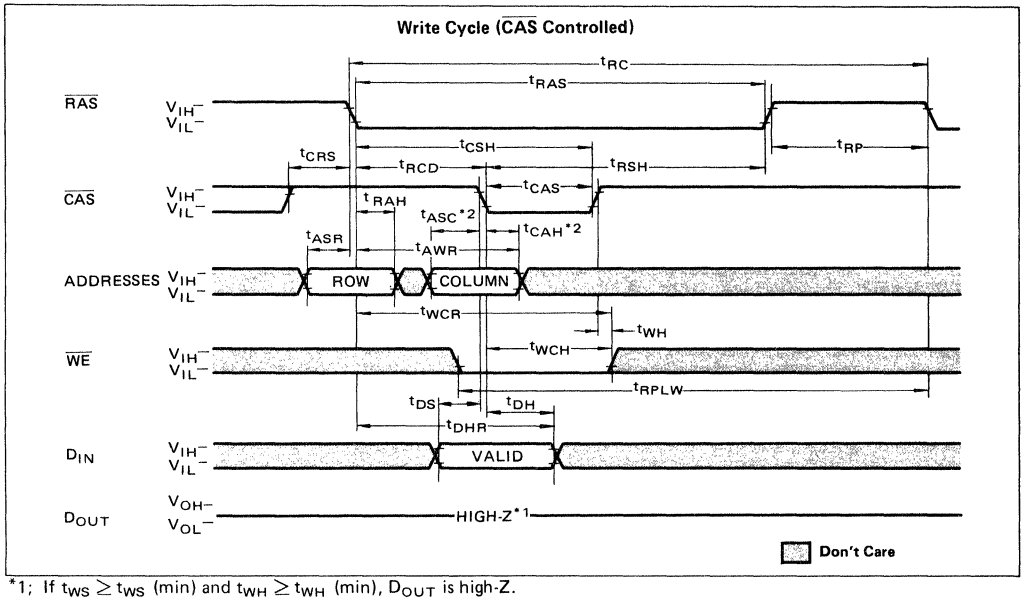
*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}.

Write Cycle ($\overline{WE}$ Controlled)

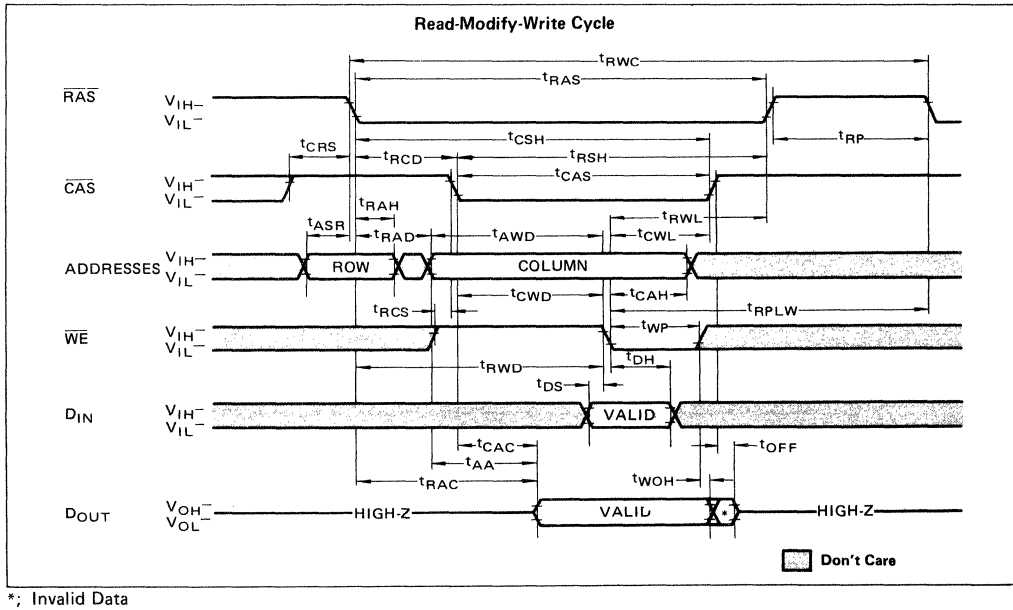


*; Write Cycle only.

2



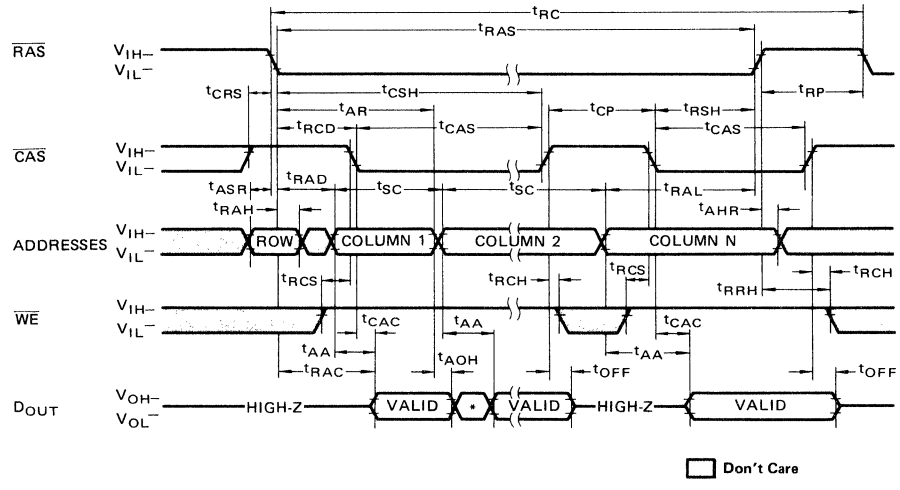
*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.
*2; Write Cycle only.



*; Invalid Data

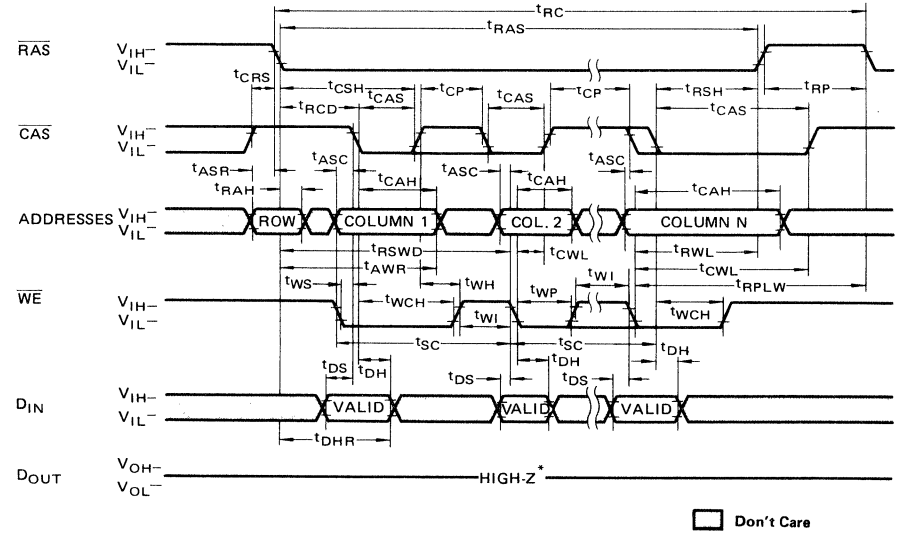
2

Static Mode Read Cycle



*; Invalid Data.

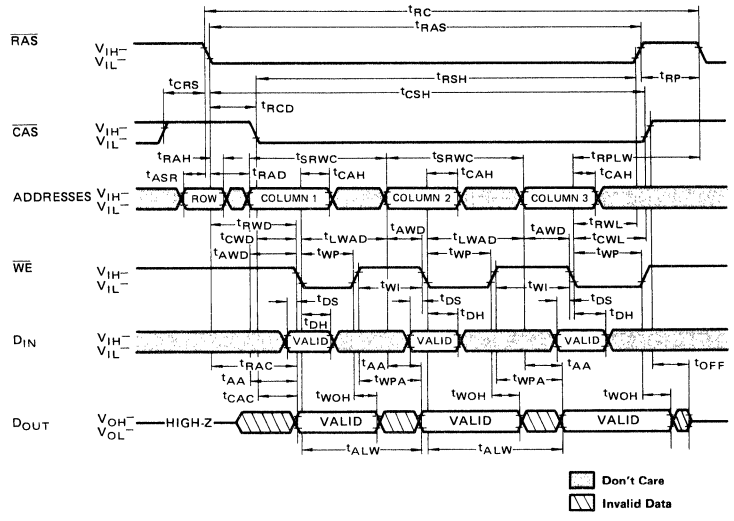
Static Mode Write Cycle



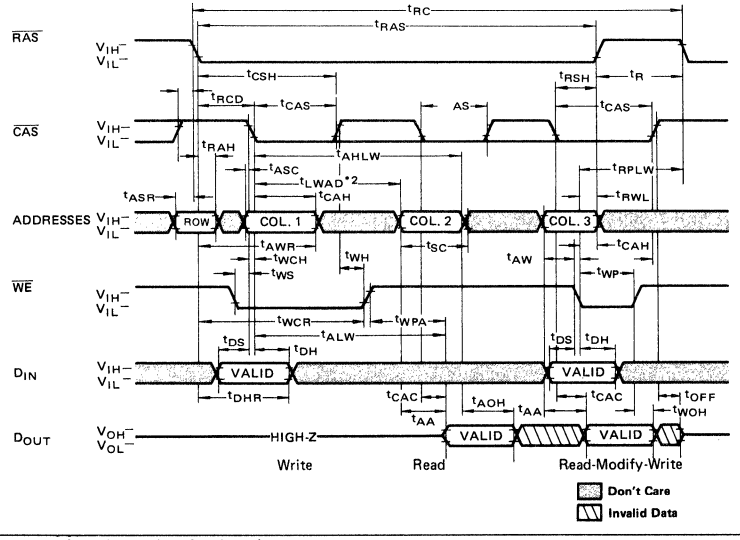
*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

2

Static Mode Read-Modify-Write



Static Mode Mixed Cycle*1



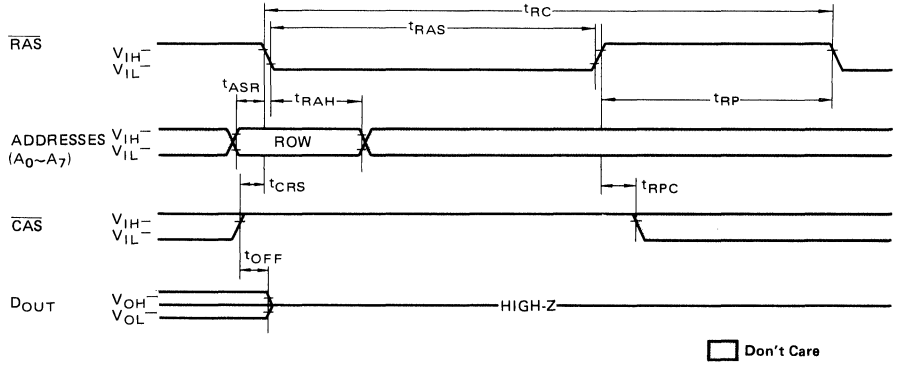
*1; This is an example of static mode mixed cycle.

*2; If t_{LWAD} is satisfied its min/max value, $t_{ALW} = t_{SC}$ (min) + t_{AA} (max)

2

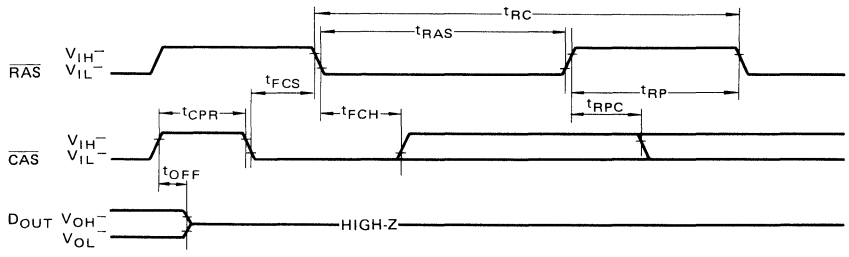
$\overline{RAS}$-Only Refresh Cycle

(Note; $\overline{WE}$, D_{IN} = Don't Care, $A_8 = V_{IH}$ or V_{IL})



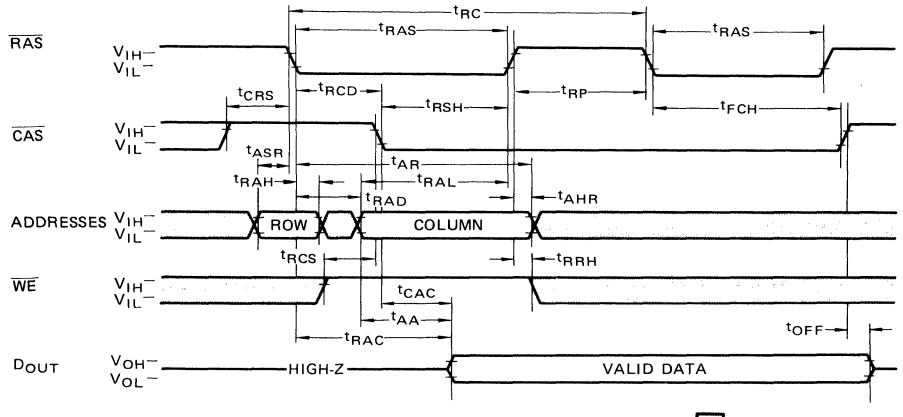
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

(Note; Address, $\overline{WE}$, D_{IN} = Don't Care)

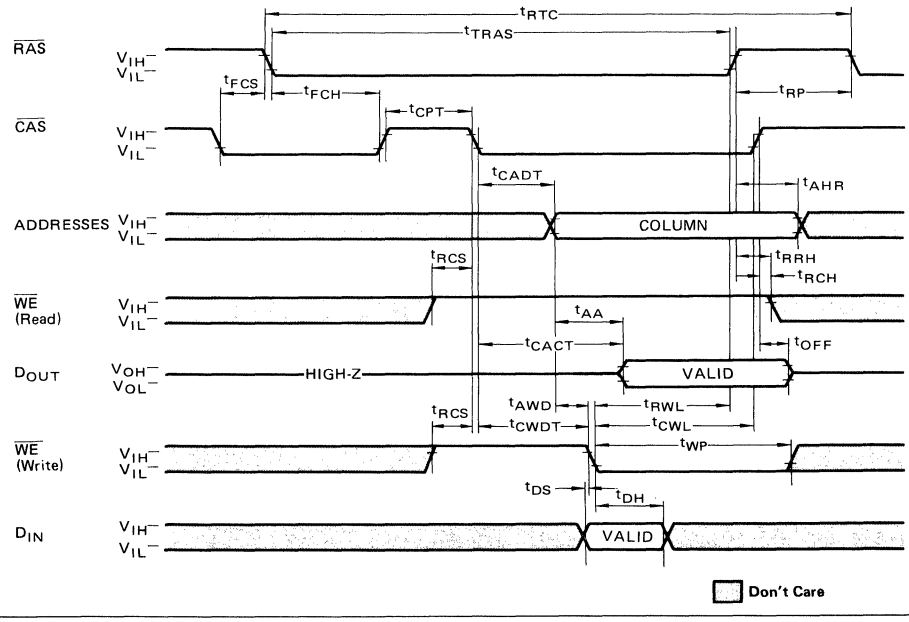


2

Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within the MB 81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe ($\overline{RAS}$). The nine column address bits are established on the address input pins (A_0 to A_8) after the Row Address Hold Time has been satisfied. In read cycle, the column address are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of $\overline{CAS}$ or $\overline{WE}$ (Both $\overline{CAS}$ and $\overline{WE}$ are low). The time period of the write operation is determined by internal circuit, thus next write operation will be inhibited during the write operation.

Data Input:
Data is written into the MB 81C258 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC}=t_{RCD}+t_{CAC}$ or $t_{RAC}=t_{RAD}+t_{AA}$.
Data output remains valid while the column address inputs are kept constant. However, when $\overline{CAS}$ goes high, the output returns to high impedance state. In the static mode, the output data is internally latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and remains valid internally until either returns to high.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle,
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge a of $\overline{WE}$.
4. Static mode mixed cycle,
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the falling edge of $\overline{WE}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 4ms.

The MB 81C258 offers the following three types of refresh.
1. $\overline{RAS}$ only refresh;
   The $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is high impedance state due to $\overline{CAS}$ high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. During $\overline{RAS}$-only refresh cycle, (either V_{IH} or V_{IL}) is permitted to A_8.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh;
   CAS-before-RAS refreshing available on the MB 81C258 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid data at the output pin by extending the $\overline{CAS}$ low time. For the MB 81C258, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh counter Test:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the function of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before -$\overline{RAS}$ refresh cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and read-modify-write cycles are enabled according to the state of $\overline{WE}$. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be accessed is shown below.
ROW ADDRESS – Bits A_0 to A_7 are provided by the refresh counter. The

bits A_8 is set high internally.

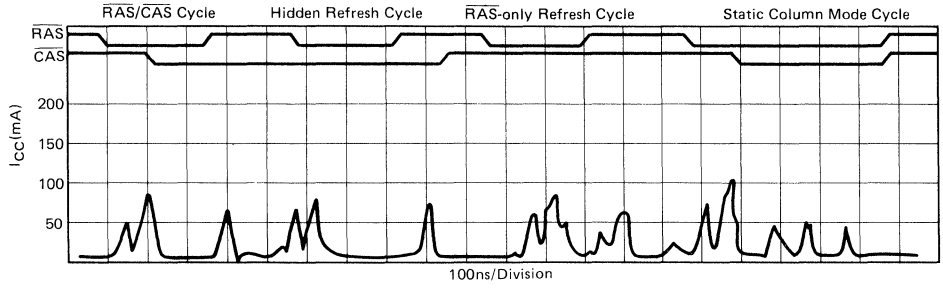
COLUMN ADDRESS – All the bits A_0 to A_8 are provided by externally after t_{CADT}.

The recommended procedure of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle is shown below. The timing of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle should be used.

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Using a write cycle, write 0s to all 256 row addresses.
4) Using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write a 1 to the same cell. This step is repeated 256 row address generated by internal refresh address counter.
5) Using a normal read cycle, read back the 1s written in step 4), from all 256 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

2

Fig. 2 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – NORMALIZED ACCESS TIME (t_{RAC}) vs SUPPLY VOLTAGE

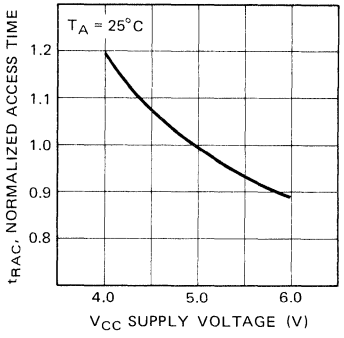


Fig. 4 – NORMALIZED ACCESS TIME (t_{RAC}) vs AMBIENT TEMPERATURE

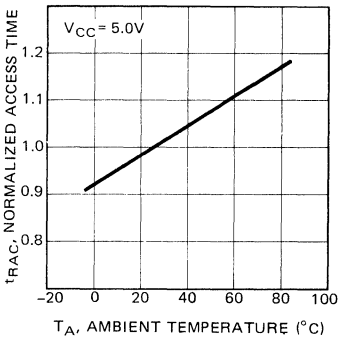


Fig. 5 – NORMALIZED ACCESS TIME (t_{AA}) vs SUPPLY VOLTAGE

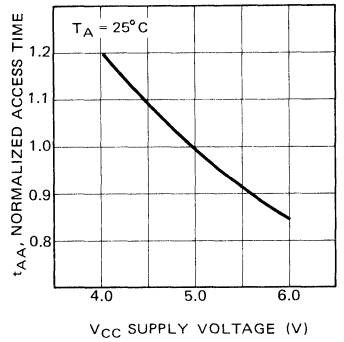


Fig. 6 – NORMALIZED ACCESS TIME (t_{AA}) vs AMBIENT TEMPERATURE

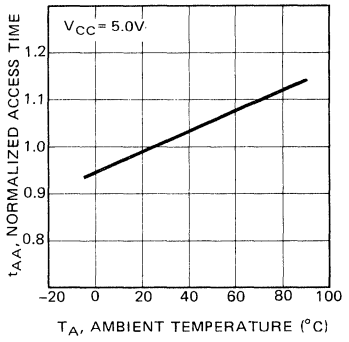


Fig. 7 – OPERATING CURRENT vs CYCLE RATE

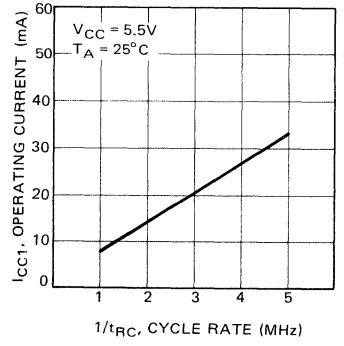
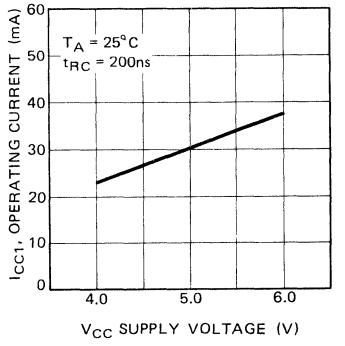


Fig. 8 – OPERATING CURRENT vs SUPPLY VOLTAGE



2

Fig. 9 – OPERATING CURRENT vs AMBIENT TEMPERATURE

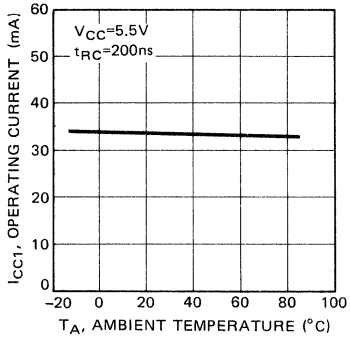


Fig. 10 – TTL STANDBY CURRENT vs SUPPLY VOLTAGE

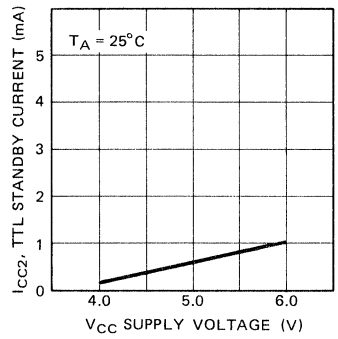


Fig. 11 – CMOS STANDBY CURRENT vs SUPPLY VOLTAGE

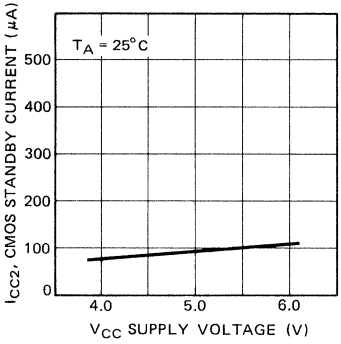


Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

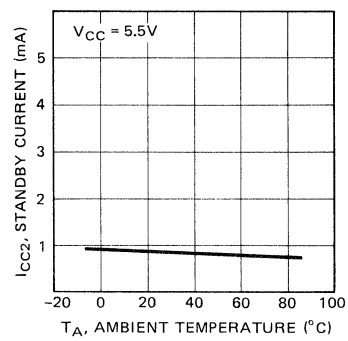


Fig. 13 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

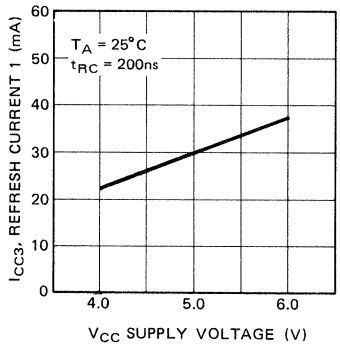


Fig. 14 – REFRESH CURRENT 1 vs CYCLE RATE

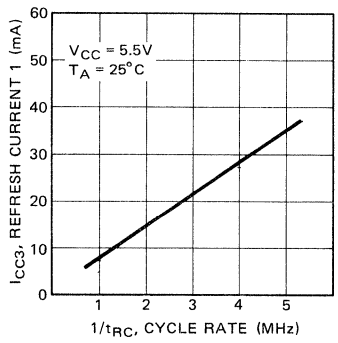


Fig. 15 – STATIC COLUMN MODE CURRENT vs CYCLE RATE

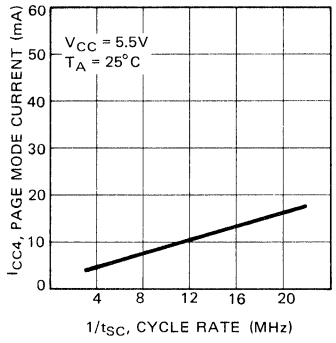


Fig. 16 – STATIC COLUMN MODE CURRENT vs SUPPLY VOLTAGE

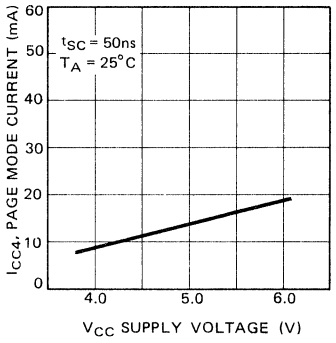


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

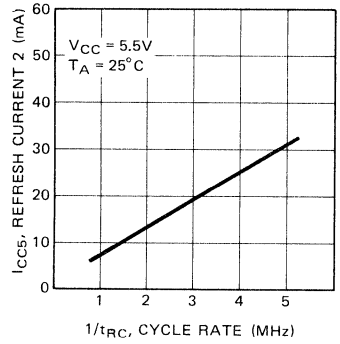


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

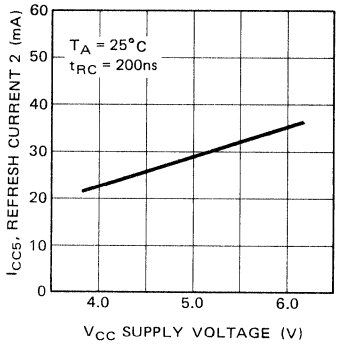


Fig. 19 – ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

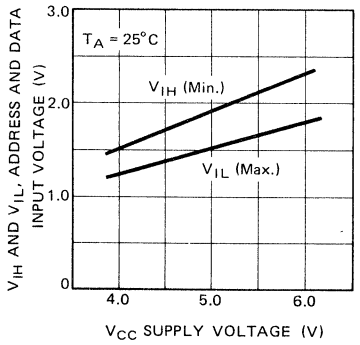
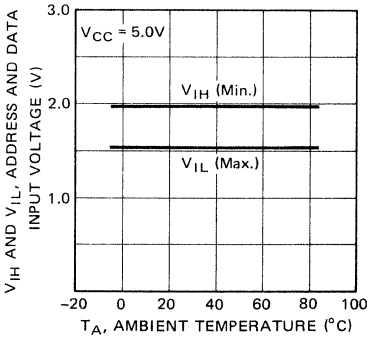


Fig. 20 – ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE



2

Fig. 21 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

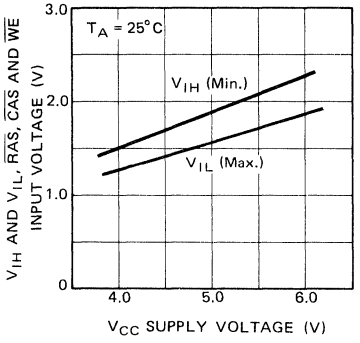


Fig. 22 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE

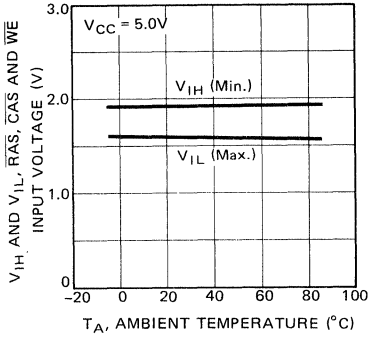


Fig. 23 – ACCESS TIME (t_{RAC}) vs LOAD CAPACITANCE

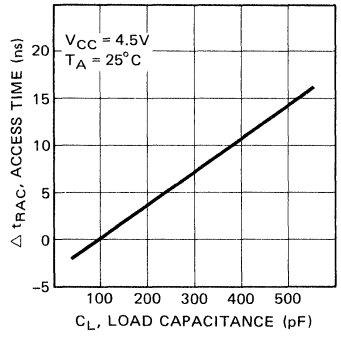


Fig. 24 – ACCESS TIME (t_{AA}) vs LOAD CAPACITANCE

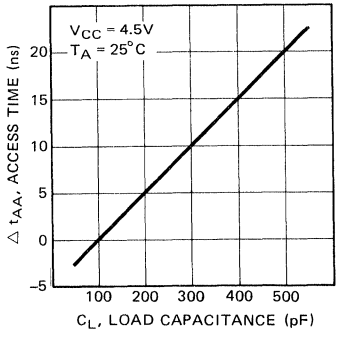


Fig. 25 – OUTPUT CURRENT vs OUTPUT VOLTAGE

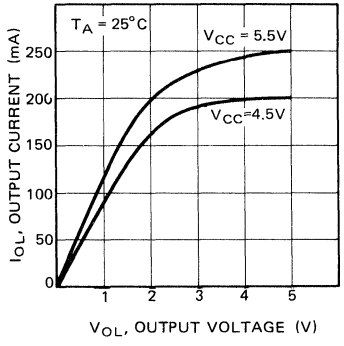


Fig. 26 – OUTPUT CURRENT vs OUTPUT VOLTAGE

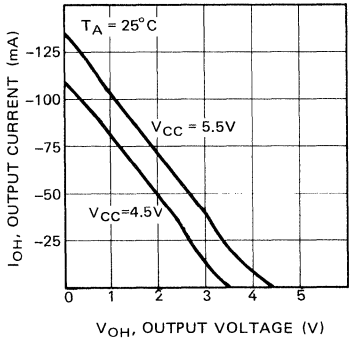


Fig. 27 – CURRENT WAVEFORM DURING POWER UP (1)

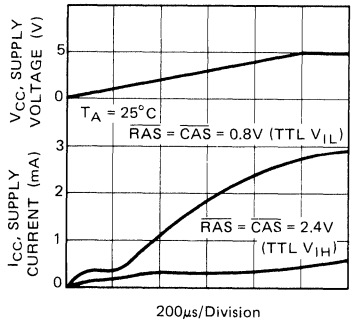
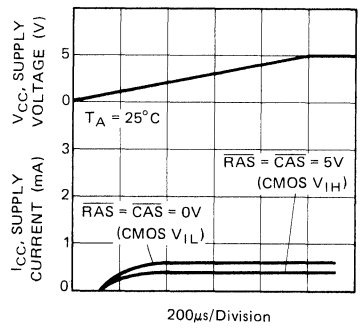


Fig. 28 – CURRENT WAVEFORM DURING POWER UP (2)



2

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output
Standby	H	H	X	X	X	X	High-Z
Read Cycle	L	L	H	Valid	Valid	X	Valid
Write Cycle	L	L	L	Valid	Valid	Valid	High-Z*1
Static Mode Read Cycle	L	L	H	Valid*2	Valid	X	Valid
Static Mode Write Cycle	L	L	L	Valid*2	Valid	Valid	High-Z*1
Static Mode Mixed Cycle	L	L	L/H	Valid*2	Valid	Valid	High-Z or Valid
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	X	X	High-Z

X: Don't Care H: High level L: Low level

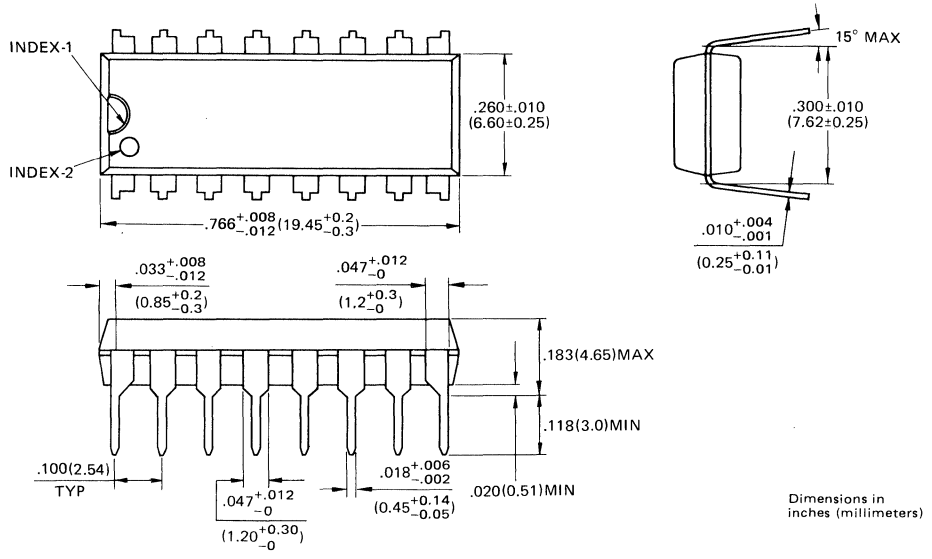
Note: *1: If $t_{WS} < t_{WS(min)}$ and $t_{WH} < t_{WH(min)}$, the data output become invalid.
*2: After first cycle, row address is not necessary.

2

PACKAGE DIMENSIONS

(Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



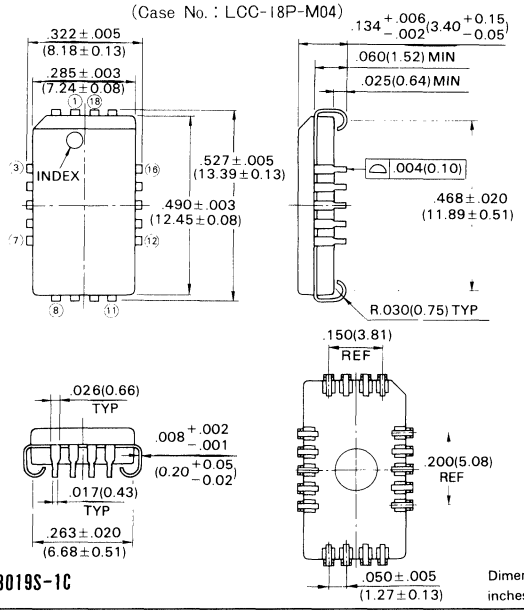
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PD)

18-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-18P-M04)



(No.): LEAD No.

Dimensions in inches (millimeters)

FUJITSU

262144 BIT CMOS STATIC COLUMN DYNAMIC RAM

MB 81C466-10
MB 81C466-12
MB 81C466-15

March 1987
Edition 2.0

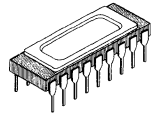
65,536 x 4 BIT CMOS STATIC COLUMN DYNAMIC RANDOM ACCESS MEMORY

The Fujitsu MB 81C466 is static column dynamic random access memory, SC-DRAM, which is organized as 65536 word by 4 bits. This SC-DRAM is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required.

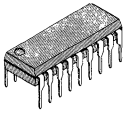
The advantage of SC-DRAM is achieving the static mode operation such as read, write and read-modify-write cycles in spite of dynamic RAM and the fast read and write operation can be performed by this mode.

The MB 81C466 is fabricated using silicon gate CMOS process. Since the CMOS circuit dissipates very small power, it can be easily used in battery backed-up application system such as hand held computer.
The MB 81C466 is pin compatible with Intel's 51C259.
All inputs and outputs are TTL compatible.

- 65536 x 4 SC-DRAM, 18-pin DIP/ 20-pin ZIP
- Silicon-gate, CMOS, single transistor cell
- Row Access Time (t_{RAC}),
  100 ns max. (MB 81C466-10)
  120 ns max. (MB 81C466-12)
  150 ns max. (MB 81C466-15)
- Random Cycle Time (t_{RC}),
  200 ns min. (MB 81C466-10)
  230 ns min. (MB 81C466-12)
  260 ns min. (MB 81C466-15)
- Address Access Time (t_{AA}),
  45 ns max. (MB 81C466-10)
  55 ns max. (MB 81C466-12)
  70 ns max. (MB 81C466-15)
- Static Mode Cycle Time (t_{SC}),
  50 ns min. (MB 81C466-10)
  60 ns min. (MB 81C466-12)
  75 ns min. (MB 81C466-15)
- Low Power Dissipation
  385 mW max. (MB 81C466-10)
  330 mW max. (MB 81C466-12)
  275 mW max. (MB 81C466-15)
  11 mW max. at standby with TTL level input
  1.65 mW max. at standby with CMOS level input
- Single 5V supply ±10% tolerance
- Internal write period control
- On chip latches for address and data inputs
- 32ms/256 refresh cycle
- $\overline{RAS}$-Only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh capability
- Standard 18-pin ceramic (Metal seal) DIP (Suffix: -C)
- Standard 18-pin Plastic DIP (Suffix: -P)
- Standard 20-Pin Plastic ZIP (Suffix: -PSZ)



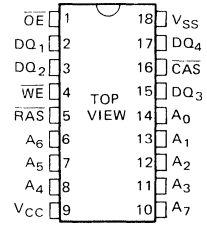
CERAMIC PACKAGE
DIP-18C-A01

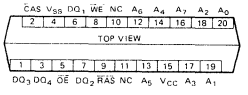


PLASTIC PACKAGE
DIP-18P-M01

PLASTIC PACKAGE
ZIP-20P-M01

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

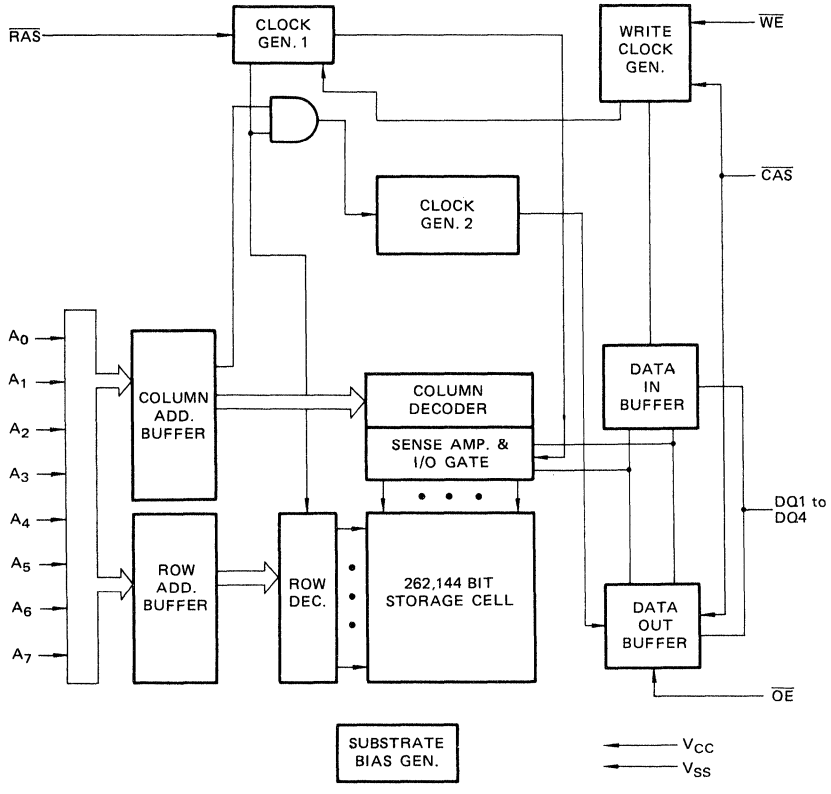
Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

BLOCK DIAGRAM



CAPACITANCE (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_7	C_{IN1}		7	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}		10	pF
Input/Output Capacitance, DQ_1 to DQ_4	C_{IO}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IN}	-1.0		0.8	V	

2

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING/REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81C466-10	I_{CC1}			70	mA
	MB 81C466-12				60	
	MB 81C466-15				50	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	TTL Level	I_{CC2}			2	mA
	CMOS Level				0.3	
STATIC MODE OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{WE}$ or Address = cycling; t_{SC} = min)	MB 81C466-10	I_{CC3}			50	mA
	MB 81C466-12				40	
	MB 81C466-15				35	
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81C466-10	I_{CC4}			65	mA
	MB 81C466-12				55	
	MB 81C466-15				45	
INPUT LEAKAGE CURRENT, ALL INPUTS (V_{IN} = 0V to 5.5V, V_{CC} = 5V, V_{SS} = 0V, all other inputs not under test = 0V)		$I_{I(L)}$	-10		10	μA
INPUT/OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)		$I_{DQ(L)}$	-10		10	μA
OUTPUT LEVEL, OUTPUT LOW VOLTAGE (I_{OL} = 4.2mA)		V_{OL}			0.4	V
OUTPUT LEVEL, OUTPUT HIGH VOLTAGE (I_{OH} = -5.0 mA)		V_{OH}	2.4			V

NOTE *; I_{CC} is depended on the output loading and cycle rate. The specified values are obtained with the output open.

AC CHARACTERISTICS

(At Recommended operating conditions unless otherwise noted) NOTE 1, 2

Parameter NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
		Min	Max	Min	Max	Min	Max	
Time Between Refresh	t_{REF}		32		32		32	ms
Random Read/Write Cycle Time	t_{RC}	200		230		260		ns
Read-Modify-Write Cycle Time	t_{RWC}	270		315		360		ns
Access Time from $\overline{RAS}$ 3 5	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$ 5	t_{CAC}		25		30		35	ns
Output Buffer Turn off Delay Time	t_{OFF}	0	25	0	25	0	30	ns
Transition Time	t_T	3	50	3	50	3	50	ns
Column Address Access Time 5	t_{AA}		45		55		70	ns
Output Hold Time from Column Address Change	t_{AOH}	5		5		5		ns
Access Time from $\overline{WE}$ Precharge	t_{WPA}		25		30		35	ns
Access Time Relative to Last Write 6	t_{ALW}		90		110		140	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		100		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	25		30		35		ns
$\overline{CAS}$ Pulse Width (Read)	t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ Pulse Width (Write)	t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ Hold Time (Read)	t_{CSH}	100		120		150		ns
$\overline{CAS}$ Hold Time (Write)	t_{CSH}	80		95		115		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	20		25		30		ns
Row Address Set Up Time	t_{ASR}	0		0		0		ns
Row Address Hold Time	t_{RAH}	15		15		20		ns
Column Address Set Up Time 7	t_{ASC}	0		0		0		ns
Column Address Hold Time 7	t_{CAH}	20		25		30		ns
$\overline{RAS}$ to Column Address Delay Time 8 9	t_{RAD}	20	55	20	65	25	80	ns
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	100		120		150		ns
Write Address Hold Time Referenced to $\overline{RAS}$	t_{AWR}	80		90		110		ns
Read Address to $\overline{RAS}$ Lead Time	t_{RAL}	45		55		70		ns
Column Address Hold Time Reference to $\overline{RAS}$ Rising Time 10	t_{AHR}	15		15		20		ns
Last Write to Column Address Delay Time 11 12	t_{LWAD}	20	45	20	55	25	70	ns
Column Address Hold Time Reference to Last Write	t_{AHLW}	90		110		140		ns

AC CHARACTERISTICS (Cont'd)

(At Recommended operating conditions unless otherwise noted) NOTE 1,2

Parameter NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Command Set Up Time Referenced to $\overline{CAS}$	t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ 13	t_{RRH}	10		10		10		ns
Read Command Hold Time Referenced to $\overline{CAS}$ 13	t_{RCH}	0		0		0		ns
$\overline{WE}$ Pulse Width	t_{WP}	15		20		25		ns
$\overline{WE}$ Inactive Time	t_{WI}	15		20		25		ns
Write Command Hold Time	t_{WCH}	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25		30		35		ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	25		30		35		ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time 14	t_{RWD}	125		150		185		ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	50		60		70		ns
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	70		85		100		ns
$\overline{RAS}$ to Second Write Delay Time	t_{RSWD}	105		125		155		ns
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	80		95		115		ns
$\overline{RAS}$ Precharge Time from Last Write	t_{RPLW}	135		155		165		ns
Write Set Up Time for Output Disable 14	t_{WS}	0		0		0		ns
Write Hold Time for Output Disable 14	t_{WH}	0		0		0		ns
D_{IN} Set Up Time	t_{DS}	0		0		0		ns
D_{IN} Hold Time	t_{DH}	20		25		30		ns
D_{IN} Hold Time Referenced to $\overline{RAS}$	t_{DHR}	80		90		110		ns
Access Time from $\overline{OE}$	t_{OEA}		25		30		35	ns
OE to Data In Delay Time	t_{OED}	20		25		30		ns
Output Buffer Turn off Delay Time from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns
$\overline{OE}$ Hold Time Referenced to $\overline{RAS}$ 15	t_{OEHR}	20		20		20		ns
$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$ 15	t_{OEHC}	20		20		20		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCS}	20		25		30		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCH}	20		25		30		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20		25		30		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	20		20		20		ns

2

AC CHARACTERISTICS (Cont'd)

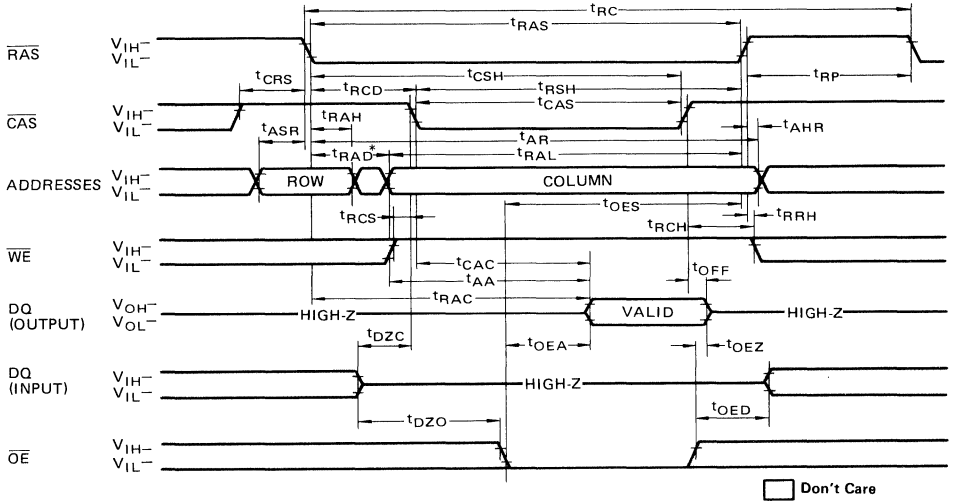
(At Recommended operating conditions unless otherwise noted) NOTE 1, 2

Parameter	NOTE	Symbol	MB 81C466-10		MB 81C466-12		MB 81C466-15		Unit
			Min	Max	Min	Max	Min	Max	
Static Mode Read/Write Cycle Time		t_{SC}	50		60		75		ns
Static Mode Read-Modify-Write Cycle Time		t_{SRWC}	120		145		180		ns
Static Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		20		25		ns
$\overline{OE}$ to $\overline{RAS}$ Inactive Set Up Time		t_{OES}	25		30		35		ns
D_{IN} to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		0		ns
D_{IN} to $\overline{OE}$ Delay Time	16	t_{DZO}	0		0		0		ns
Refresh Counter Test Cycle Time	17	t_{RTC}	465		550		645		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	17	t_{TRAS}	365	10000	440	10000	535	10000	ns
Refresh Counter Test $\overline{CAS}$ Precharge Time	17	t_{CPT}	50		60		70		ns
Refresh Counter Test $\overline{CAS}$ to Column Address Delay Time	17	t_{CADT}		100		120		150	ns
Refresh Counter Test Access Time from $\overline{CAS}$	17	t_{CACT}		135		165		205	ns
Refresh Counter Test $\overline{CAS}$ to $\overline{WE}$ Delay Time	17	t_{CWDT}	135		165		205		ns

NOTES:

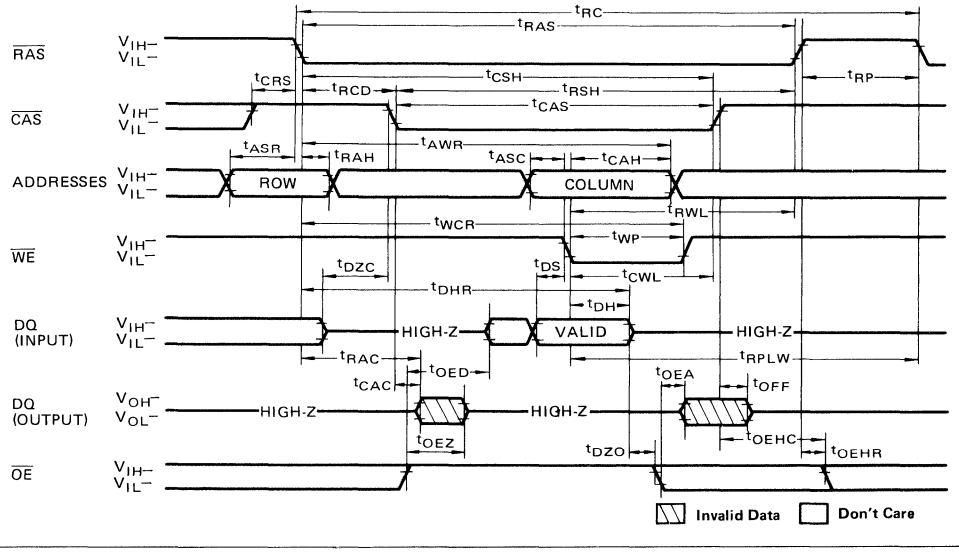
1. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8, V_{OH} = 2.4V, and V_{OL} = 0.4V.
3. Assumes that $t_{RAD} \leqq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
4. Assumes that $t_{RAD} \geqq t_{RAD}$ (max).
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
7. Write Cycle only.
8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
9. t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5ns)
10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
12. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5ns).
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geqq t_{RWD}$ (min). The data output will contain data read from the selected cell.
15. Either t_{OEHR} or t_{OEHC} is satisfied, output is disabled.
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Read Cycle



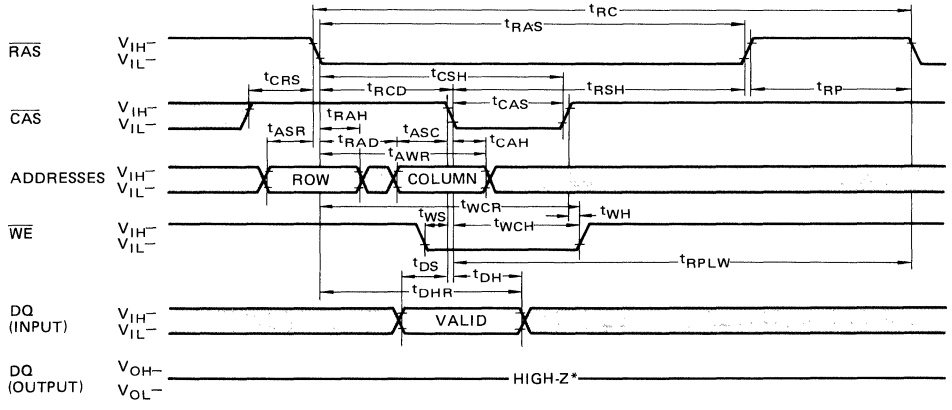
*; If $t_{RAD} \geqq t_{RAD}$ (max), access time is t_{AA}.

Write Cycle ($\overline{WE}$ Controlled)



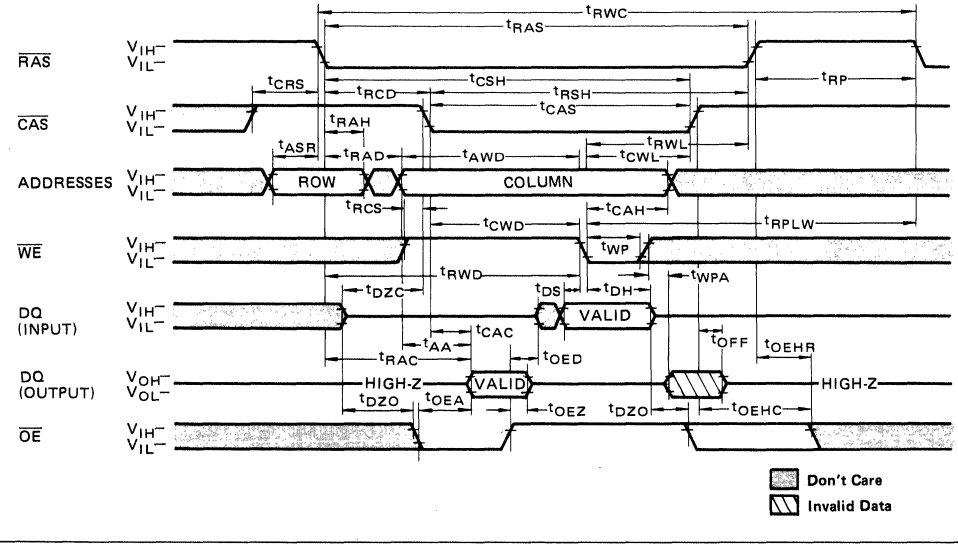
2

Write Cycle ($\overline{CAS}$ Controlled)
$\overline{OE}$; Don't Care



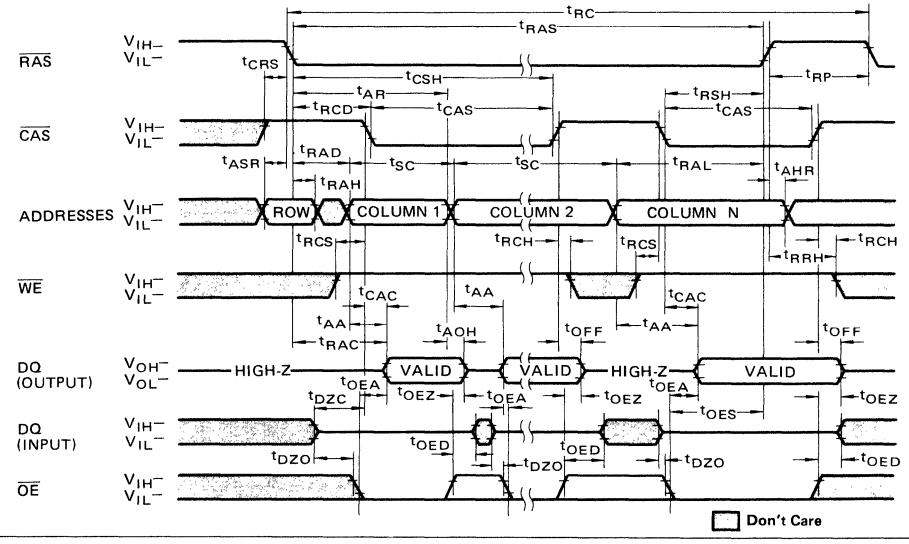
*; If $\overline{OE}$ is kept high through a cycle or $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min) are met, DQ pins are kept high impedance state.

Read-Modify-Write Cycle

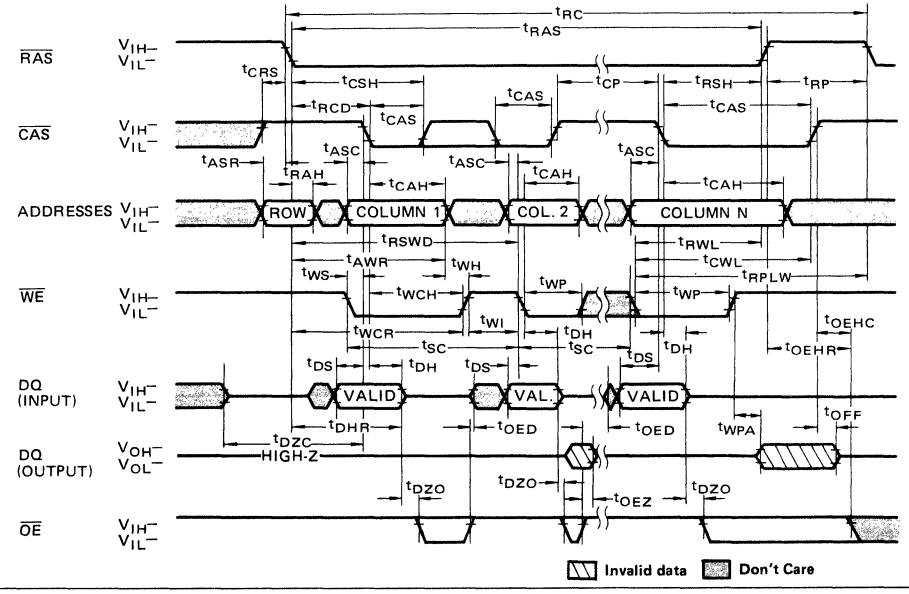


2

Static Mode Read Cycle

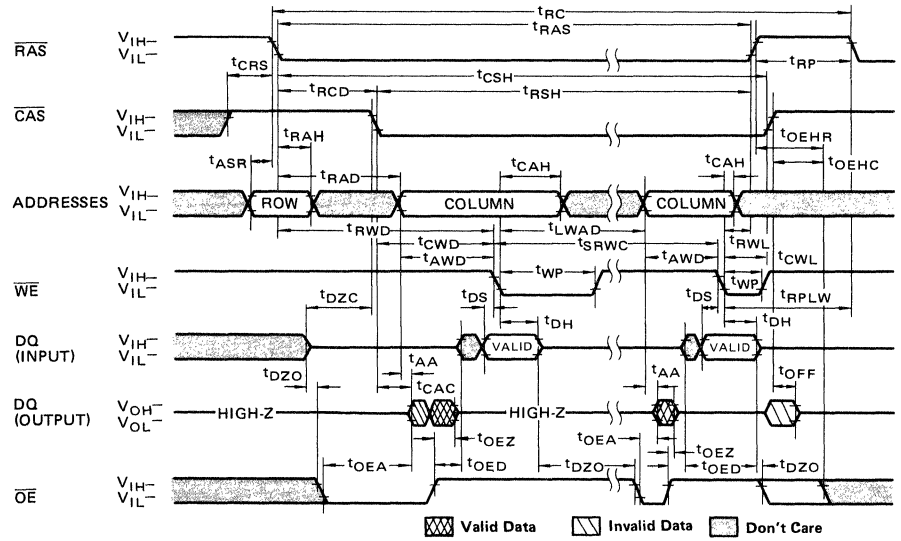


Static Mode Write Cycle

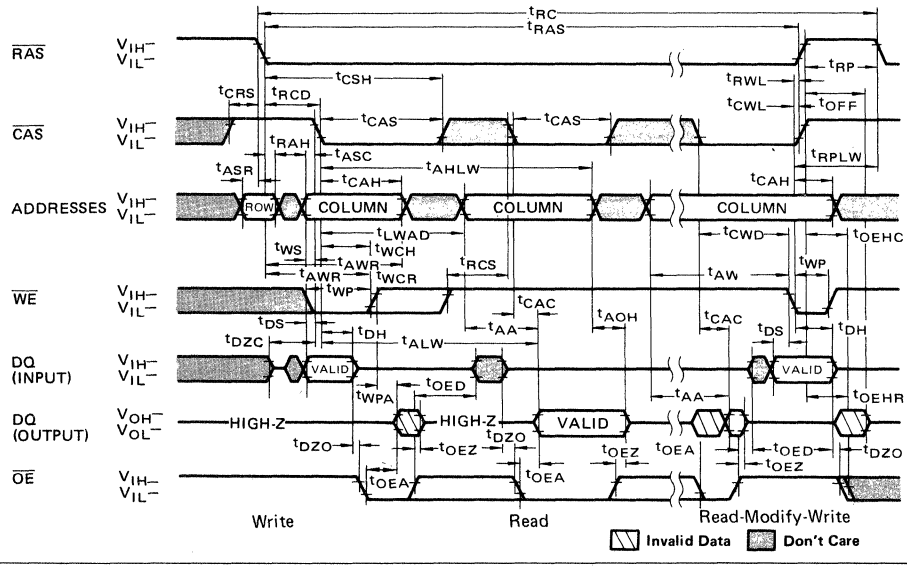


2

Static Mode Read-Modify-Write Cycle

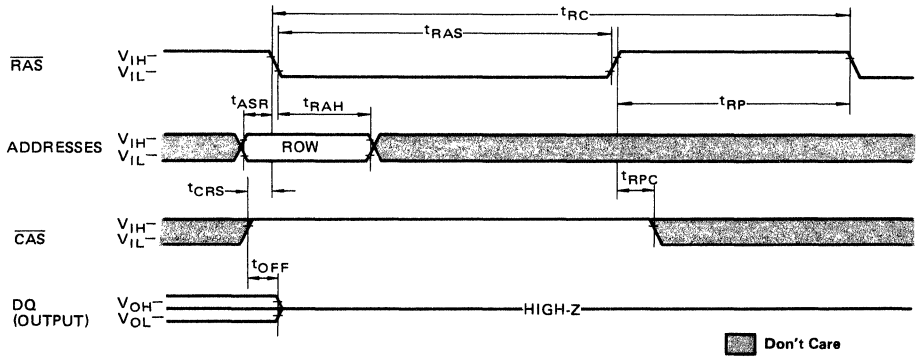


Static Mode Mixed Cycle

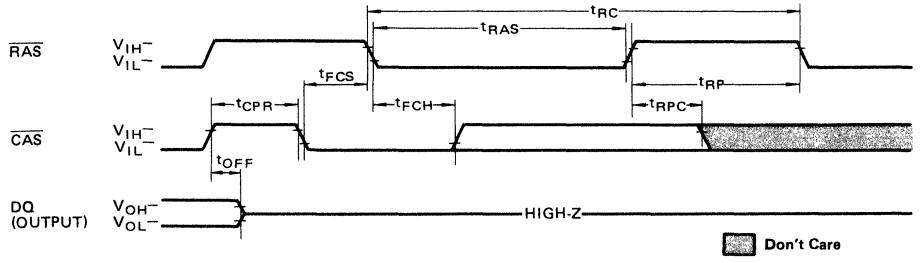


2

$\overline{RAS}$-Only Refresh Cycle
(Note; $\overline{WE}$, $\overline{OE}$, D_{IN} = Don't Care)

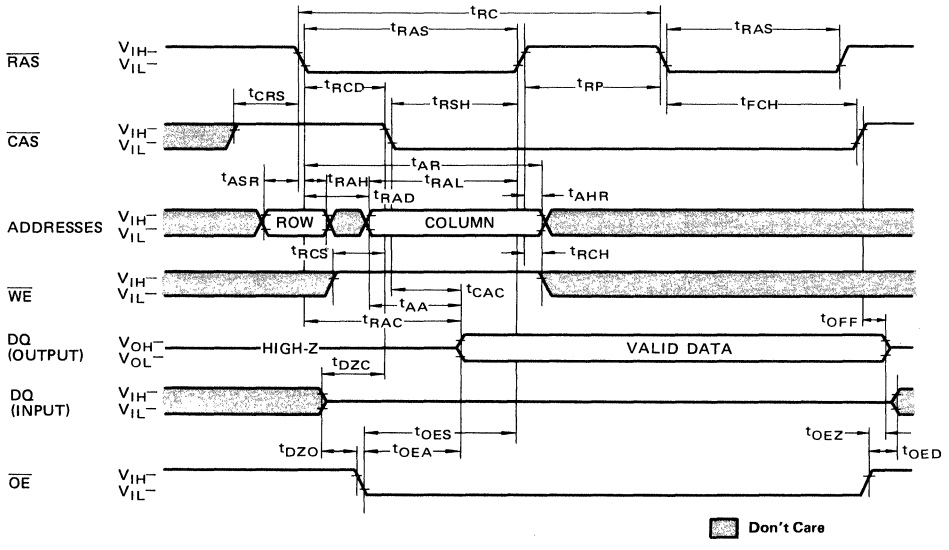


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)
(Note; Address, $\overline{WE}$, $\overline{OE}$, D_{IN} = Don't Care)



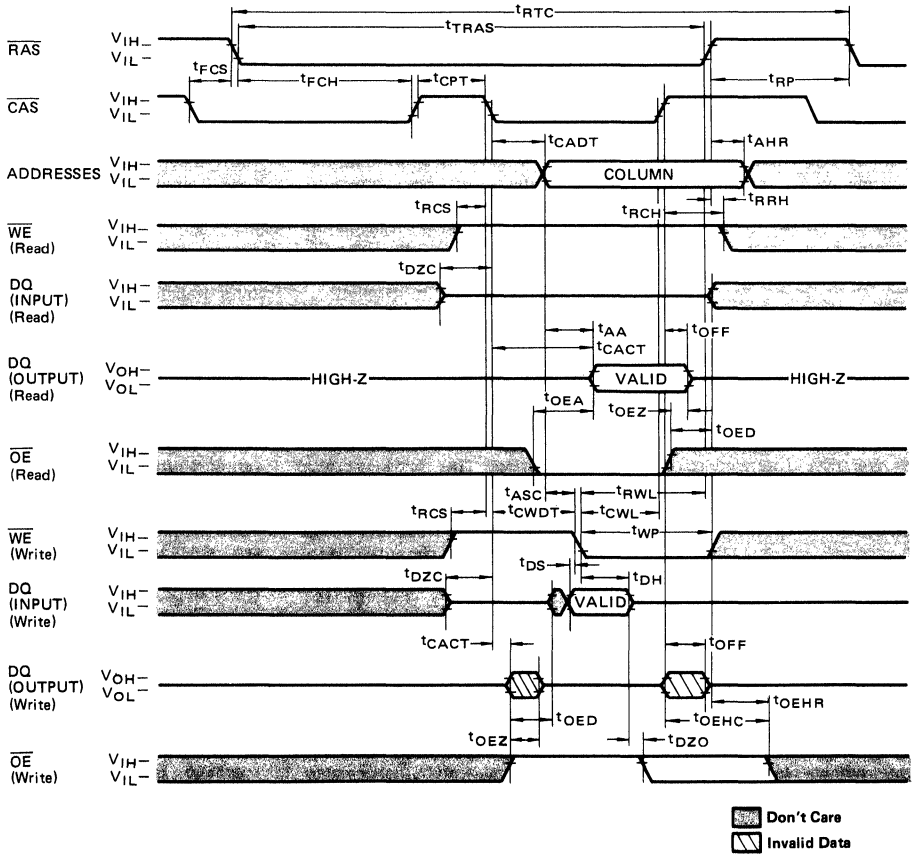
2

Hidden Refresh Cycle



2

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode parallel 4 bits of the 262,144 storage cells within the MB 81C466. Eight row address bits are established on the address input pins (A_0 to A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column address bits are established on the address input pins (A_0 to A_7) after the Row Address Hold Time has been satisfied. In read cycle, the column addresses are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of $\overline{CAS}$ or $\overline{WE}$ (Both $\overline{CAS}$ and $\overline{WE}$ are low). The time period of the write operation is determined by internal circuit, thus the next write operation will be inhibited during the write operation.

Data Pins:
Data Inputs;
Data are written into the MB 81C466 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.
4. t_{OEA} from the falling edge of $\overline{OE}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC}=t_{RCD}+t_{CAC}$ or $t_{RAC}=t_{RAD}+t_{AA}$.
Data output remains valid while the column address inputs are kept constant. However, when either $\overline{CAS}$ or $\overline{OE}$ goes high, the output returns to a high impedance state. In the static write cycle ($\overline{CAS}$ controlled), if both $t_{WS} \geqq t_{WS}$(min) and $t_{WH} \geqq t_{WH}$(min) are met, data pins are input mode regardless of the state of $\overline{OE}$.

Output Enable:
The $\overline{OE}$ controls the impedance of the output buffers. In the high state on $\overline{OE}$, the output buffers are high impedance state. In the low state on $\overline{OE}$, the output buffers are low impedance state. In the write cycle ($\overline{WE}$ controlled), the $\overline{OE}$ must be high before the data applied to DQ pins. When $\overline{WE}$ controlled write cycles is not used, $\overline{OE}$ can be low throughout the operation.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle,
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input or t_{OEA} from the falling edge of $\overline{OE}$. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle. The $\overline{OE}$ must be high before the data are applied to DQ pins.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{WE}$. The $\overline{OE}$ must be high before the data are applied to DQ pins.
4. Static mode mixed cycle;
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the falling edge of $\overline{WE}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.
5. t_{OEA} from the falling edge of $\overline{OE}$.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 4ms.
The MB 81C466 offers the following three types of refresh.
1. $\overline{RAS}$ only refresh;
   The $\overline{RAS}$-only refresh avoids any outputs during refresh because the outputs buffers are high impedance state due to $\overline{CAS}$-high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 81C466 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid data at the output pin by extending the $\overline{CAS}$ low time. For the MB 81C466, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter Test:
A special timing sequence using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the function of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh activated circuitry. After the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, if $\overline{\text{CAS}}$ goes to high and goes to low again while $\overline{\text{RAS}}$ is held low, the read and read-modify-write cycles are enabled according to the state of $\overline{\text{WE}}$. This is shown in the $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be accessed is shown below.

ROW ADDRESS – All bits A_0 to A_7 are provided by the refresh counter.

COLUMN ADDRESS – All the bits A_0 to A_7 are provided by externally after t_{CADT}.

The recommended procedure of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test is shown below. The timing of $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle should be used.

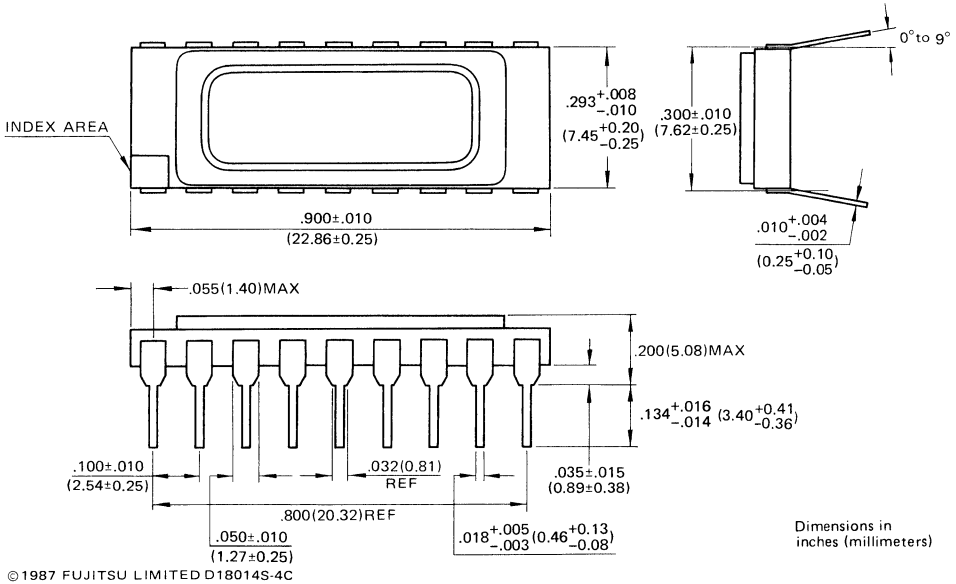
1) Initialize the internal refresh address counter by using eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Using a write cycle, write 0s to all 256 row addresses.
4) Using $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write a 1 to the same cell. This step is repeated 256 row address generated by internal refresh address counter.
5) Using a normal read cycle, read back the 1s written in step 4), from all 256 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

2

PACKAGE DIMENSIONS

(Suffix: -C)

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)

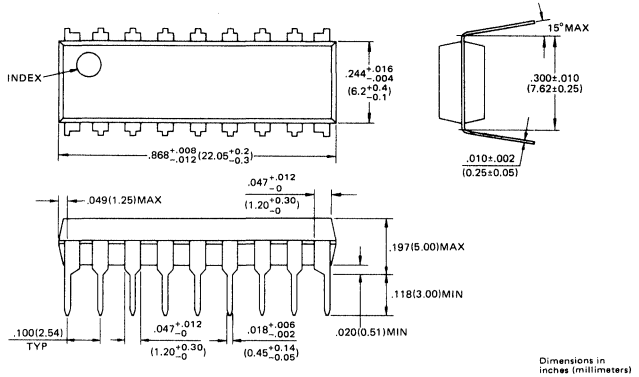


2

PACKAGE DIMENSIONS

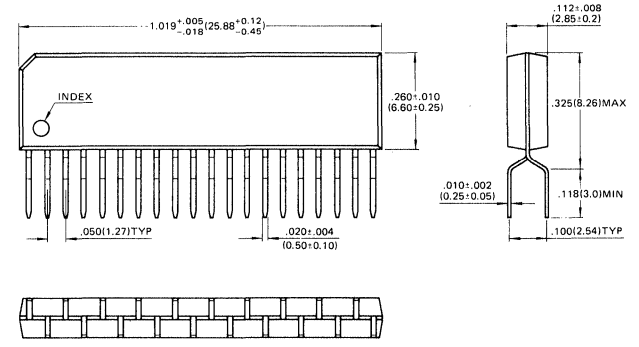
(Suffix: -P) (Suffix: -PSZ)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-18P-M01)



Dimensions in inches (millimeters)

20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE NO.: ZIP-20P-M01)



Dimensions in inches (millimeters)

October 1989
Edition 3.0

FUJITSU

DATA SHEET

MB81C1000-70/-80/-10/-12
CMOS 1048576 BIT FAST PAGE DYNAMIC RAM

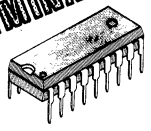
CMOS 1,048,576 x 1 BIT FAST PAGE MODE DYNAMIC RAM

The Fujitsu MB81C1000 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

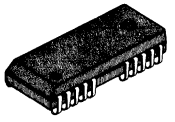
Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1000 high α-ray soft error immunity and long refresh time.
Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

This specification is applied to "BC" version revised with intent to realize faster access time. So faster speed version (70ns and 80ns) are available on this chip.

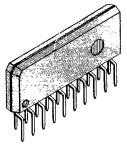
PRELIMINARY



PLASTIC PACKAGE
DIP-18P-M04



PLASTIC PACKAGE
LCC-26P-M04



PLASTIC PACKAGE
ZIP-20P-M02
DIP-18C-A01: See Page 19

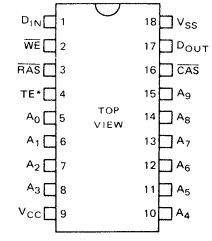
PRODUCT LINE

Parameter	MB81C1000 -70	MB81C1000 -80	MB81C1000 -10	MB81C1000 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Fast Page Mode Cycle Time	53ns min.	55ns min.	60ns min.	70ns min.
Low Power Dissipation				
• Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level)/5.5mW max. (CMOS level)			

FEATURES

- 1,048,576 word x 1bit organization
- Silicon Gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2ms
- Common I/O capability by using early write
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

PIN ASSIGNMENT



*: Test Enable (will be available)

Pin Assignment
For SOJ: See Page 17

Pin Assignment
For ZIP: See Page 18

ABSOLUTE MAXIMUM RATINGS (See NOTE)

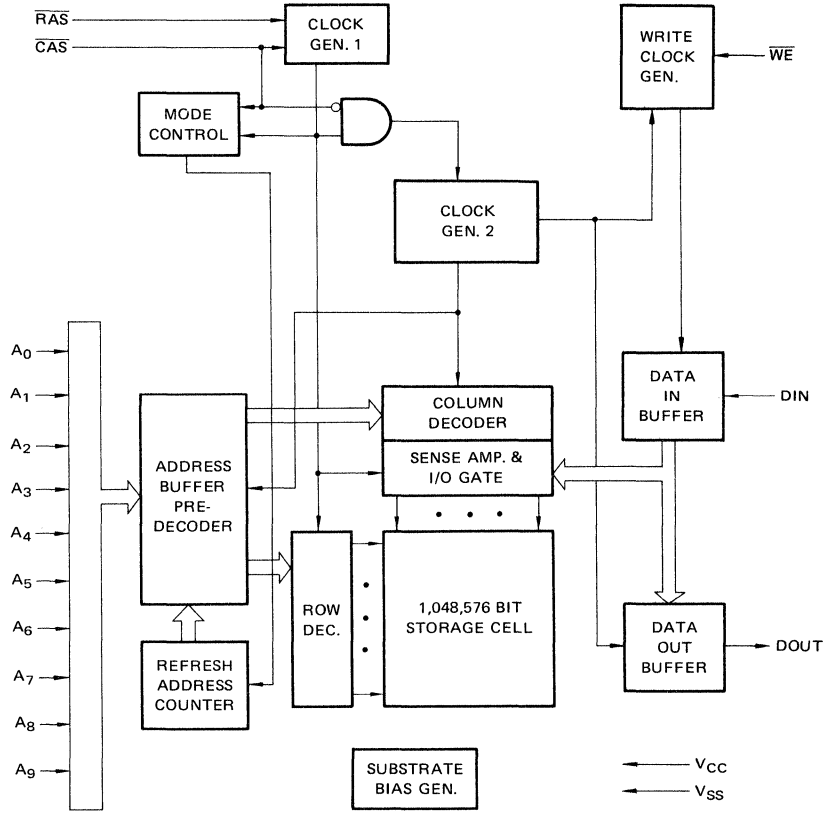
Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – BLOCK DIAGRAM



CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance, A_0 to A_9, D_{IN}	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$ $\overline{CAS}$, $\overline{WE}$	C_{IN2}		5	pF
Output Capacitance, D_{OUT}	C_{OUT}		5	pF

2

RECOMMENDED OPERATING CONDITIONS

Parameter	NOTES	Symbol	Value			Unit	Ambient Operating Temperature
			Min	Typ	Max		
Supply Voltage	1	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, All inputs	1	V_{IH}	2.4		6.5	V	
Input Low Voltage, All inputs	1	V_{IL}	−2.0		0.8	V	

2

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) Notes 3

Parameter	NOTES	Conditions	Symbol	Values Min	Values Max	Unit
Operating Current (Average power Supply current) 2	MB81C1000-70	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	I_{CC1}		75	mA
	MB81C1000-80				70	
	MB81C1000-10				60	
	MB81C1000-12				50	
Standby Current (Power supply current)	TTL level	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}		2.0	mA
	CMOS level	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC}−0.2V			1.0	
Refresh Current 1 (Average power supply current 2	MB81C1000-70	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC3}		70	mA
	MB81C1000-80				65	
	MB81C1000-10				55	
	MB81C1000-12				45	
Fast Page Mode Current 2	MB81C1000-70	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min	I_{CC4}		47	mA
	MB81C1000-80				45	
	MB81C1000-10				40	
	MB81C1000-12				33	
Refresh Current 2 (Average power current) 2	MB81C1000-70	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC5}		70	mA
	MB81C1000-80				65	
	MB81C1000-10				55	
	MB81C1000-12				45	
Input Leakage Current		0V ≦ V_{IN} ≦ 5.5V, 4.5V ≦ V_{CC} ≦ 5.5V, V_{SS} = 0V; pins not under test = 0V	$I_{I(L)}$	−10	10	μA
Output Leakage Current		0V ≦ V_{OUT} ≦ 5.5V; Data out disabled	$I_{O(L)}$	−10	10	
Output High Voltage		I_{OH} = −5mA	V_{OH}	2.4		V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}		0.4	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter NOTES	Symbol	MB81C1000-70		MB81C1000-80		MB81C1000-10		MB81C1000-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh	t_{REF}		8.2		8.2		8.2		8.2	ms
2	Random Read/Write Cycle Time	t_{RC}	140		155		180		210		ns
3	Read-Modify-Write Cycle Time	t_{RWC}	167		182		210		245		ns
4	Access Time from $\overline{RAS}$ 6 9	t_{RAC}		70		80		100		120	ns
5	Access Time from $\overline{CAS}$ 7 9	t_{CAC}		25		25		25		35	ns
6	Access Time from Column Address 8 9	t_{AA}		43		45		50		60	ns
7	Output Data Hold Time	t_{OH}	7		7		7		7		ns
8	Output Buffer Turn on Delay Time	t_{ON}	5		5		5		5		ns
9	Output Buffer Turn Off Delay Time 10	t_{OFF}		25		25		25		25	ns
10	Transition Time	t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time	t_{RP}	60		65		70		80		ns
12	$\overline{RAS}$ Pulse Width	t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time	t_{RSH}	25		25		30		35		ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		0		ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time 11 12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25		25		30		35		ns
17	$\overline{CAS}$ Hold Time	t_{CSH}	70		80		100		120		ns
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ Cycle) 17	t_{CPN}	15		15		15		15		ns
19	Row Address Set Up Time	t_{ASR}	0		0		0		0		ns
20	Row Address Hold Time	t_{RAH}	10		12		15		15		ns
21	Column Address Set Up Time	t_{ASC}	0		0		0		0		ns
22	Column Address Hold Time	t_{CAH}	15		15		15		20		ns
23	$\overline{RAS}$ to Column Address Delay Time 13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	43		45		50		60		ns
25	Read Command Set Up Time	t_{RCS}	0		0		0		0		ns

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter NOTES	Symbol	MB81C1000-70		MB81C1000-80		MB81C1000-10		MB81C1000-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
26	Read Command Hold Time Referenced to $\overline{RAS}$ [14]	t_{RRH}	0		0		0		0		ns
27	Read Command Hold Time Referenced to $\overline{CAS}$ [14]	t_{RCH}	0		0		0		0		ns
28	Write Command Set Up Time [15]	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time	t_{WCH}	15		15		15		20		ns
30	$\overline{WE}$ Pulse Width	t_{WP}	15		15		15		20		ns
31	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	22		22		25		30		ns
32	Write Commnd to $\overline{CAS}$ Lead Time	t_{CWL}	17		17		20		25		ns
33	D_{IN} Set Up Time	t_{DS}	0		0		0		0		ns
34	D_{IN} Hold time	t_{DH}	15		15		15		20		ns
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time [15]	t_{RWD}	70		80		100		120		ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time [15]	t_{CWD}	25		25		30		35		ns
37	Column Address to $\overline{WE}$ Delay Time [15]	t_{AWD}	43		45		50		60		ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		0		0		ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		0		0		ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		15		15		20		ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)	t_{CAT}		43		45		50		60	ns
50	Fast Page Mode Read/Write Cycle Time	t_{PC}	53		55		60		70		ns
51	Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	75		77		85		100		ns
52	Access Time from $\overline{CAS}$ Precharge [9] [16]	t_{CPA}		53		55		60		70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	15		15		15		15		ns

NOTES:

[1] Referenced to V_{SS}.

[2] I_{CC} depends on the output load conditions and cycle rate. The specified values are obtained with the output open.
I_{CC} depends on the number of address changes as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
I_{CC4} is specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

[3] An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

[4] AC characteristics assume $t_T = 5$ ns.

[5] V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

[6] Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.

[7] If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

[8] If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

[9] Measured with a load equivalent to two TTL loads and 100 pF.

[10] t_{OFF} is specified that output buffer changes to high impedance state.

[11] Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

[12] t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).

[13] Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

[14] Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

[15] t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restructive operating parameter. They are included in the data sheet as the electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin.
If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the D_{OUT} pin, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, and t_{RAL} specifications.

[16] t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).

[17] Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only

2

Fig. 2 – t_{RAC} vs t_{RCD}

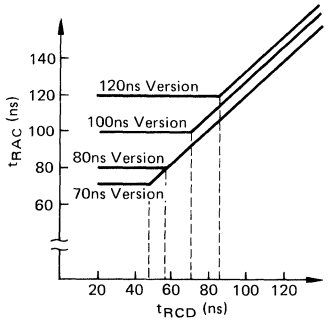
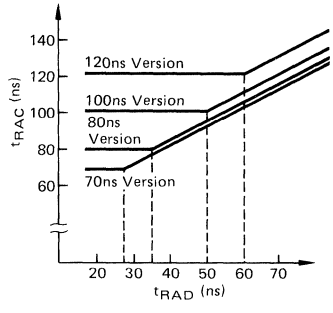


Fig. 3 – t_{RAC} vs t_{RAD}



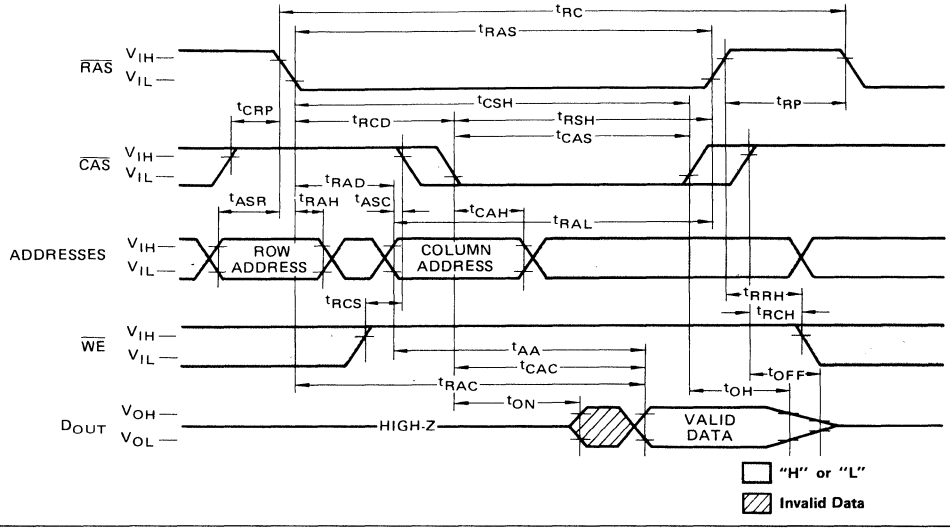
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	Valid	Valid	–	Valid	O *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	O *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	O *	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	–	–	High-Z	O	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	L	L	X	–	–	–	High-Z	O	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	X	–	–	–	Valid	O	Previous data is kept.

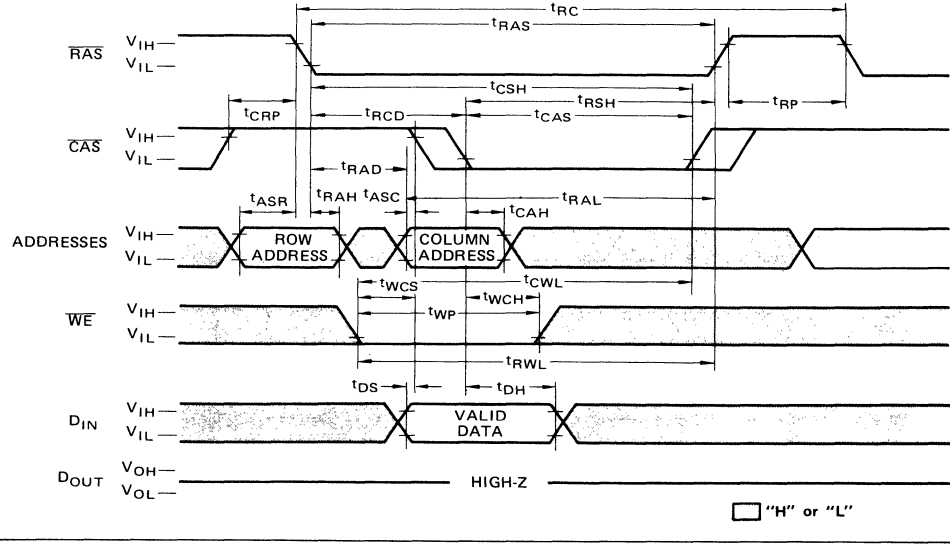
X; "H" or "L"
*; It is impossible in fast page mode.

2

Read Cycle

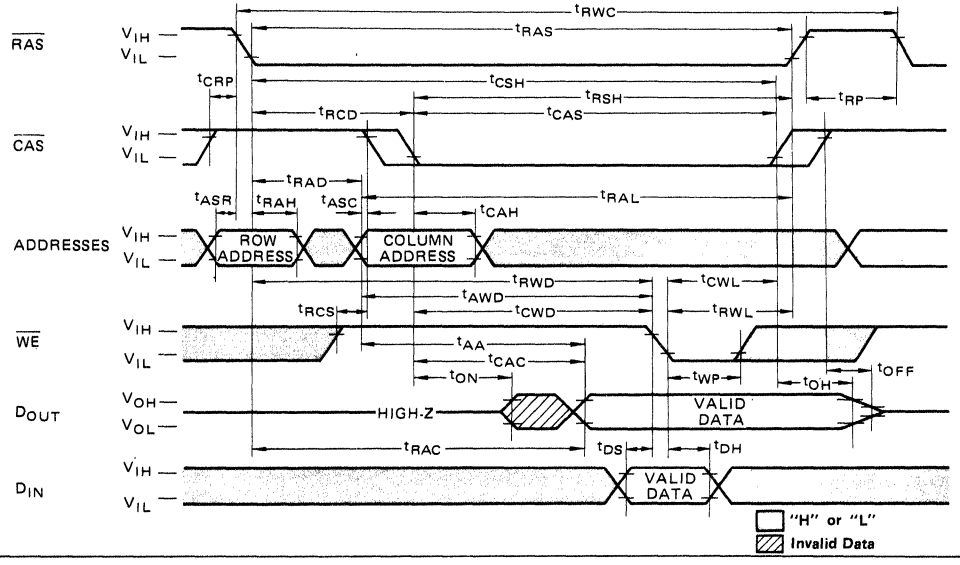


Write Cycle (Early Write)

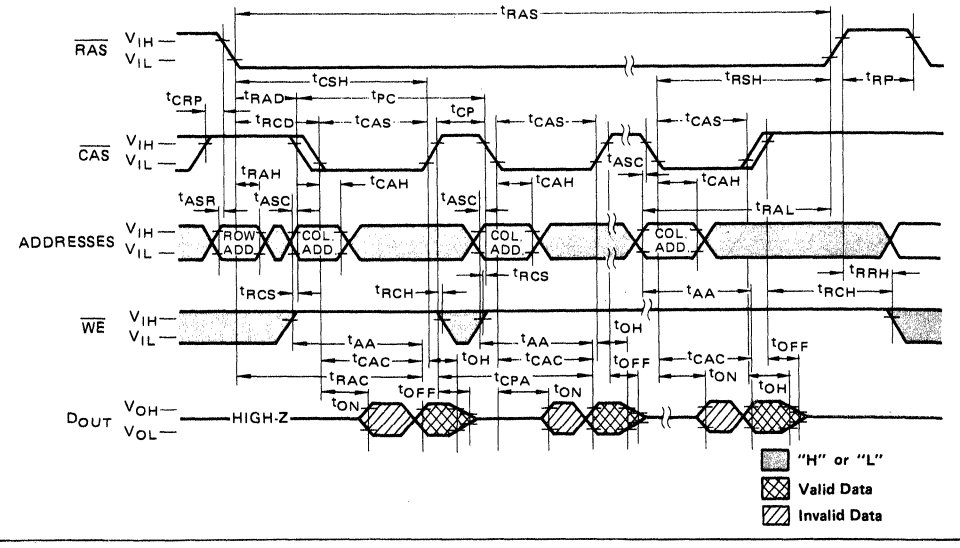


2

Read-Write/Read-Modify-Write Cycle

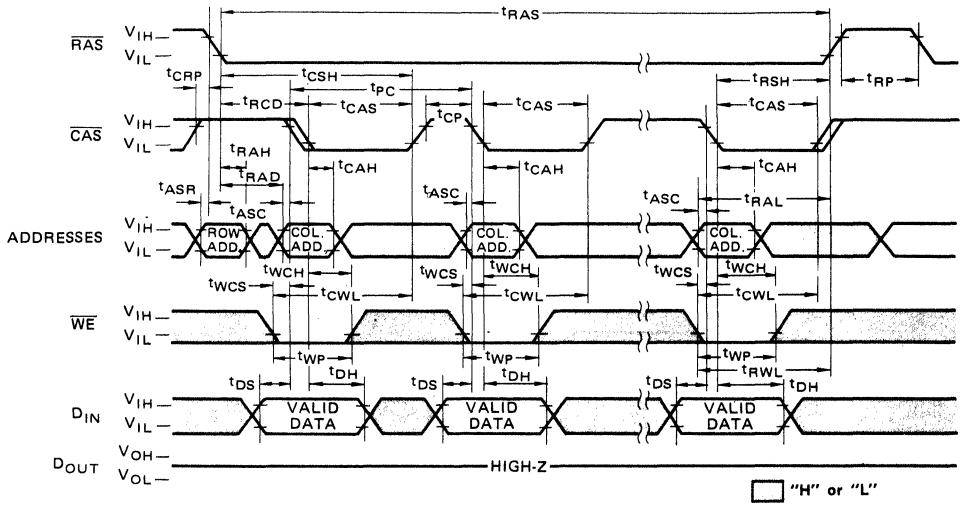


Fast Page Mode Read Cycle

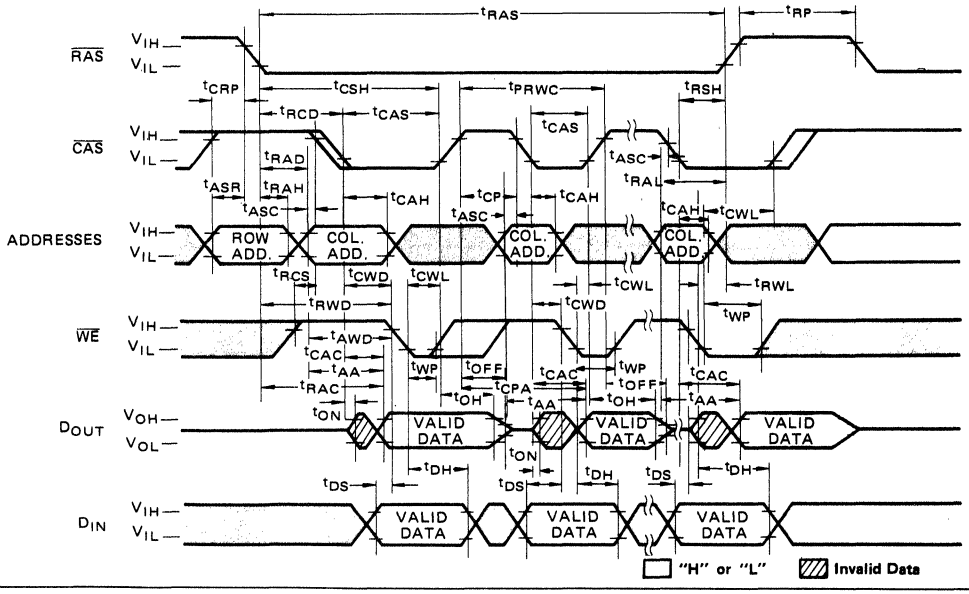


2

Fast Page Mode Write Cycle (Early Write)



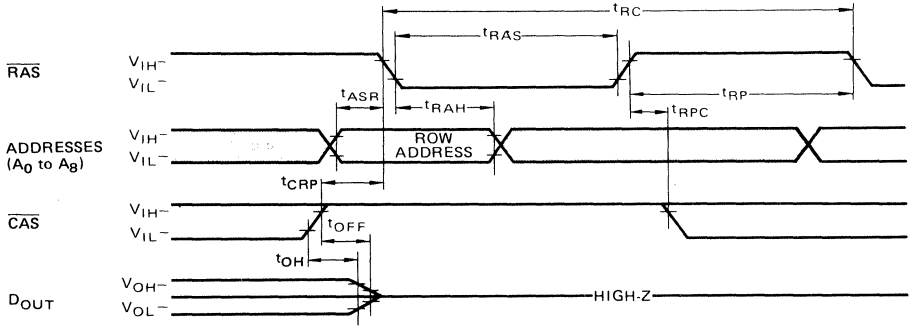
Fast Page Mode Read-Modify-Write Cycle



2

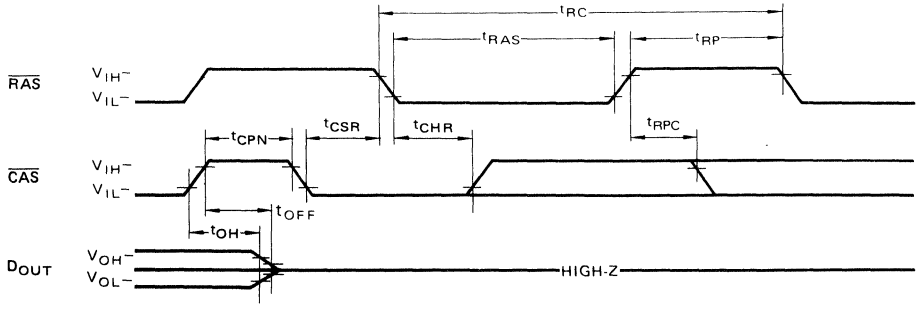
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, D_{IN} = "H"or"L", $A_9 = V_{IH}$ or V_{IL}

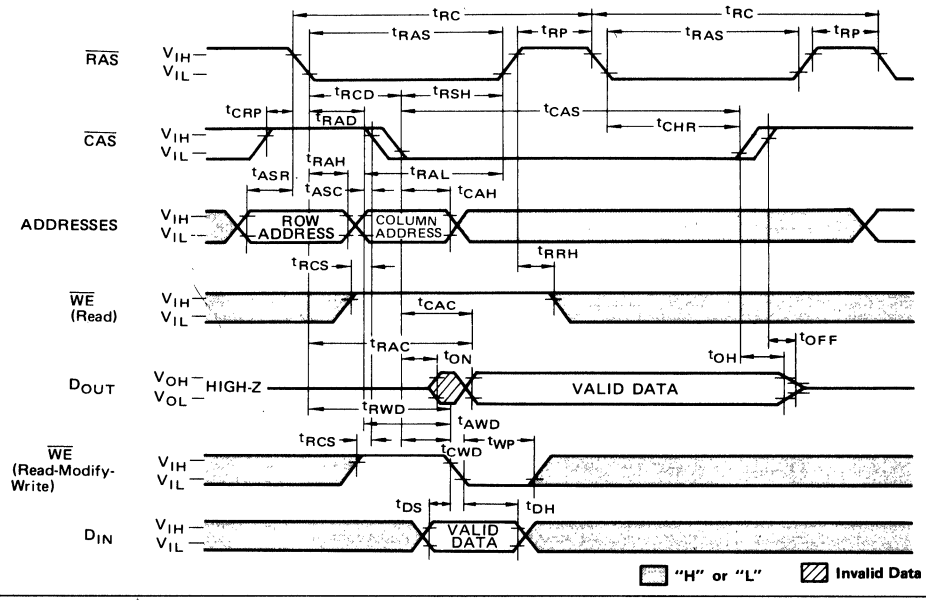


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

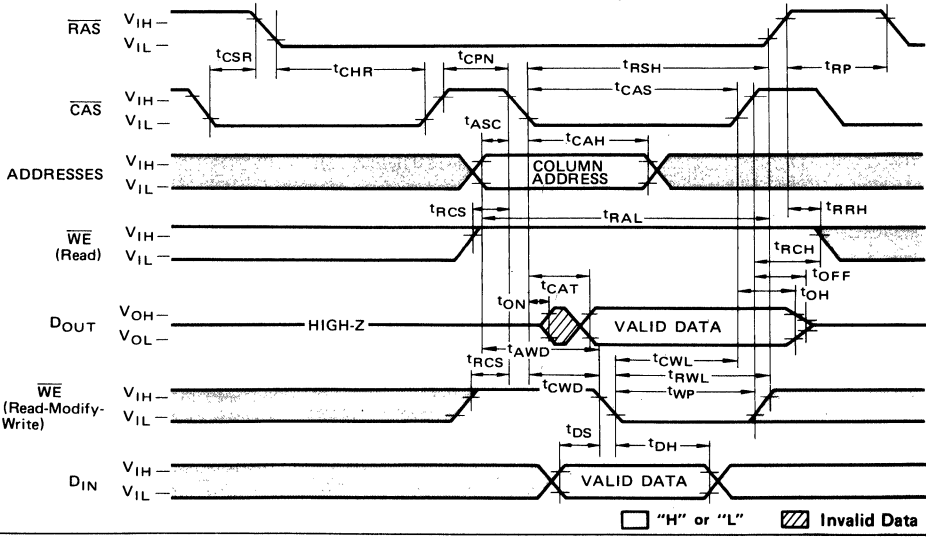
NOTE: Address, $\overline{WE}$, D_{IN} = "H"or"L"



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



2

DESCRIPTION

Address Inputs:
A total of twenty binary input address bits are required to decode any one of the 1,048,576 storage cells whthin the MB 81C1000. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe ($\overline{RAS}$). The ten column address bits are established on the address input pins (A_0 to A_9) and latched with the Column Address Strobe ($\overline{CAS}$). All row and column address must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min) + t_T.
Therefore, to get valid data within t_{RAC}, it is necessary to apply column address within t_{RAD} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occur later.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. Data input is ignored during read cycle. Data output is high impedance state during write cycle.

Data Input:
Data is written into the MB 81C1000 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is high impedance state until $\overline{CAS}$ is brought low. In a read or read-modify-write cycle, the output becomes valid after t_{RAC} from the falling edge of $\overline{CAS}$ when t_{RCD} (max) is satisfied or after t_{CAC} when t_{RCD} is longer than t_{RCD} (max). The data output remains valid until $\overline{CAS}$ returns to high with t_{OH} and becomes high impedance state after t_{OFF}. In an early write cycle, the output buffer is high impedance state during the entire cycle. In a delayed write cycle, if t_{RWD} or t_{CWD} is less than t_{RWD} (min) or t_{CWD} (min), the output is invalid.

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output is remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with t_{OH}. During read cycle, the D_{IN} pin is "H" or "L". The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), or Column address input (t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and D_{IN} pin. The data on D_{IN} pin is latched with the latter falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL} and t_{RAL} must be satisfied the specifications.

Read-Modify-Write Cycle:
The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the D_{OUT} pin. After the current data is read out, modified data can be re-written into the same address quickly.

Fast Page Mode Read Cycle:
The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. So power consumption and cycle time are reduced. During fast page mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occurs later. Any of the 1024 bits belonging to each row can be accessed.

Fast Page Mode Write Cycle:
The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$. The data on D_{IN} pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, t_{CWL} must be satisfied. Any of the 1024 bits belonging to each row can be accessed.

Fast Page Mode Read-Modify-Write Cycle:
During fast page mode, the read-modify-write cycle can be executed by changing $\overline{WE}$ high to low after the data appears at the D_{OUT} pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Refresh:
The refresh of DRAM is executed by normal read, write or read-modiqy-write cycle, i.e., the cells on the one row line are refreshed by executing one of three cycles. 512 row address must be refreshed every 8.2 ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-written to the cell. The MB81C1000 also has thdee types of refresh modes, $\overline{RAS}$-Only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

1. $\overline{RAS}$-Only Refresh;

The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$ "L" and keeping $\overline{CAS}$ "H" through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, the D_{OUT} pin is kept high impedance state.

2. $\overline{CAS}$-before-$\overline{RAS}$ Refresh;

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB 81C1000 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. Hidden Refresh;

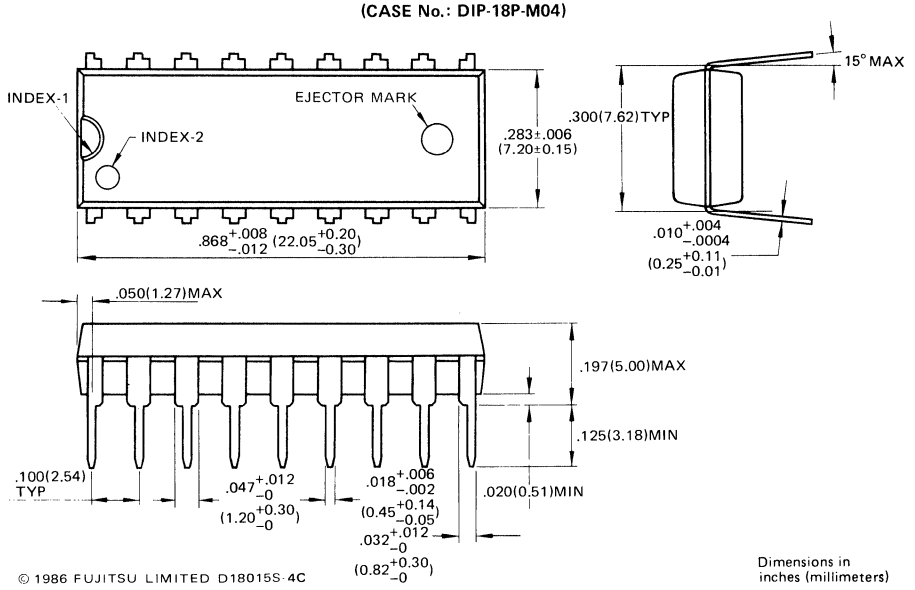
The Hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuosly from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

2

PACKAGE DIMENSIONS

(Suffix: -P)

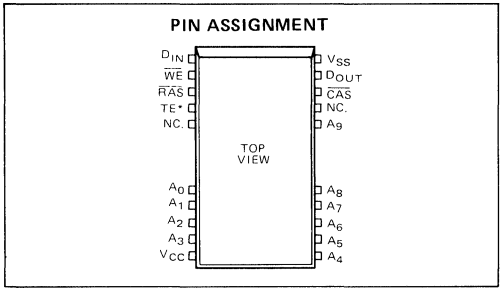
18 LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M04)



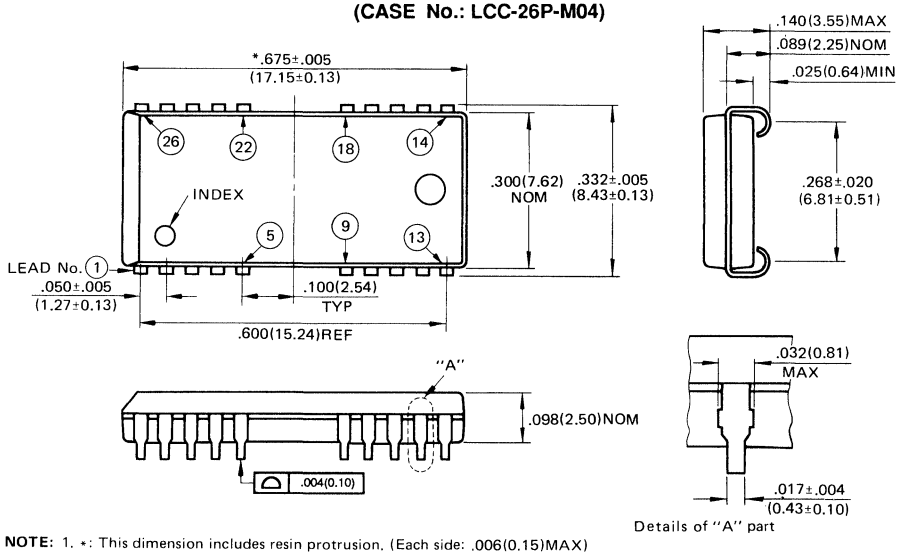
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PJ)



26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

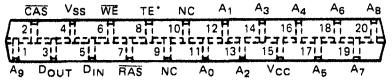
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

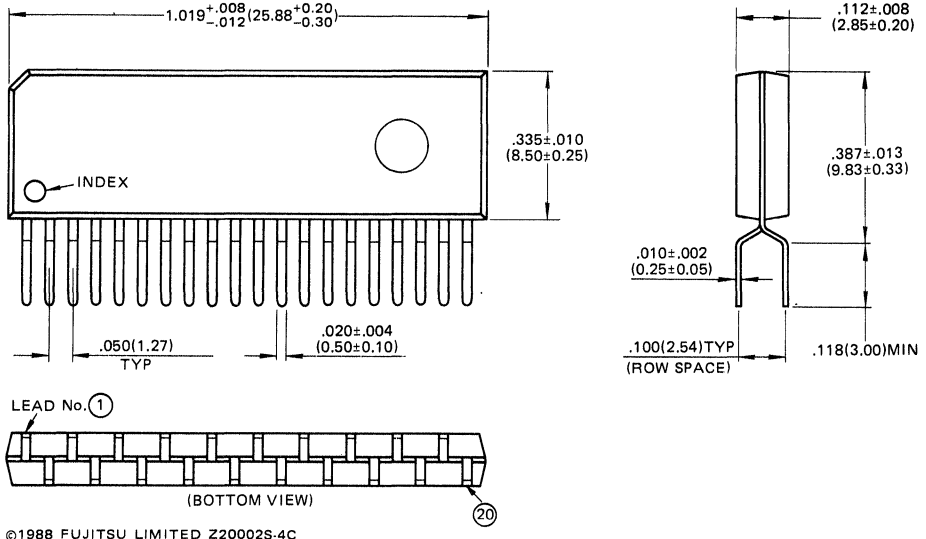
(Suffix: -PSZ)

PIN ASSIGNMENT

(TOP VIEW)



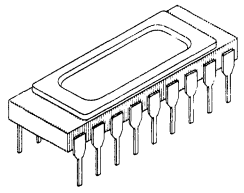
20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in
inches (millimeters)

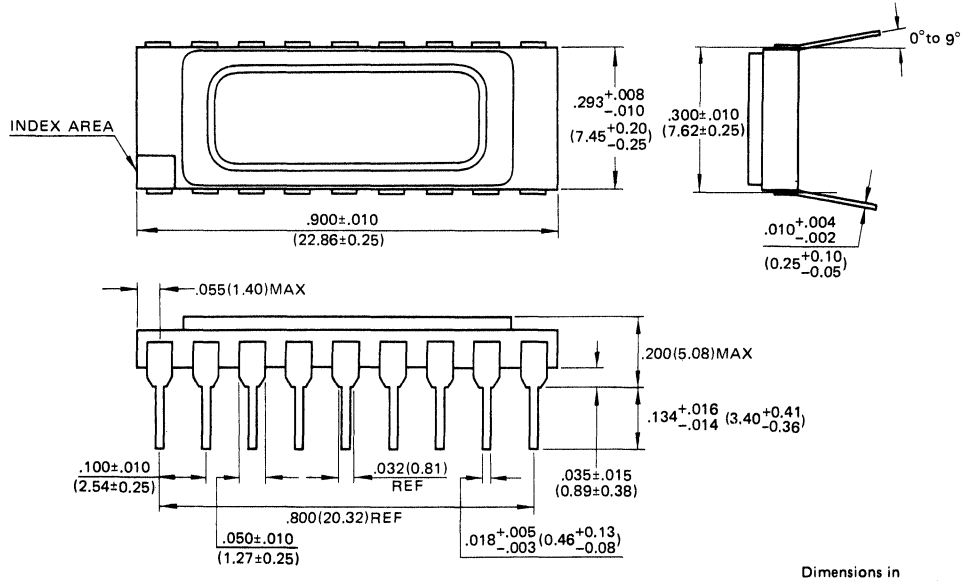
PACKAGE DIMENSIONS

(Suffix :-C)



DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Dimensions in inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C1000A-60/-80/-10

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

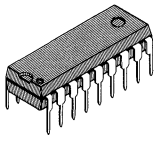
CMOS 1,048,576 X 1 BIT Fast Page Mode Dynamic RAM

ADVANCE INFO.

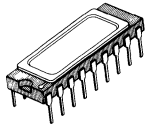
The Fujitsu MB81C1000A is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1000A High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

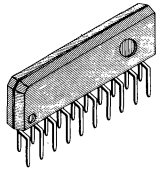


DIP-18P-M04



DIP-18C-A02

LCC-26P-M04



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C1000A-60	MB81C1000A-80	MB81C1000A-10
$\overline{RAS}$ Access Time	60ns max.	80ns max.	100ns max.
Randam Cycle Time	130ns min.	155ns min.	180ns min.
Address Access Time	30ns max.	40ns max.	50ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	25ns max.
Fast Page Mode CycleTime	45ns min.	55ns min.	65ns min.
Low Power Dissipation • Operating current	330mW max.	275mW max.	248mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

October 1989
Edition 3.0

FUJITSU

DATA SHEET

MB81C1001-70/-80/-10/-12
CMOS 1048576 BIT NIBBLE DYNAMIC RAM

CMOS 1,048,576 x 1 BIT NIBBLE MODE DYNAMIC RAM

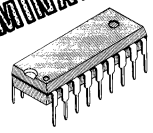
The Fujitsu MB81C1001 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001 has been designed for mainframe memories, buffer memories, and video image memories requiring highspeed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very lower power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1001 high α-ray soft error immunity and long refresh time.

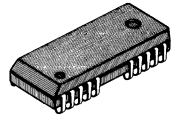
Since the CMOS circuits are used for peripheral circuits, low power dissipation and high speed operation are realized.

This specification is applied to "BC" version revised with intent to realize faster access time. So faster speed version (70ns and 80ns) are available on this chip.

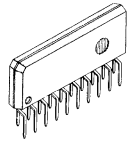
PRELIMINARY



PLASTIC PACKAGE
DIP-18P-M04



PLASTIC PACKAGE
LCC-26P-M04



PLASTIC PACKAGE
ZIP-20P-M02

DIP-18C-A01: See Page 19

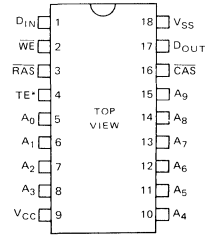
PRODUCT LINE

Parameter	MB81C1001 -70	MB81C1001 -80	MB81C1001 -10	MB81C1001 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Nibble Mode Cycle Time	50ns min.	50ns min.	55ns min.	60ns min.
Low Power Dissipation • Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level)/5.5mW max. (CMOS level)			

FEATURES

- 1,048,576 word x 1bit organization
- Silicon Gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2ms
- Common I/O capability by using early write
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance.

PIN ASSIGNMENT



*: Test Enable (will be available)

Pin Assignment
For SOJ: See Page 17
Pin Assignment
For ZIP: See Page 18

ABSOLUTE MAXIMUM RATINGS (See NOTE)

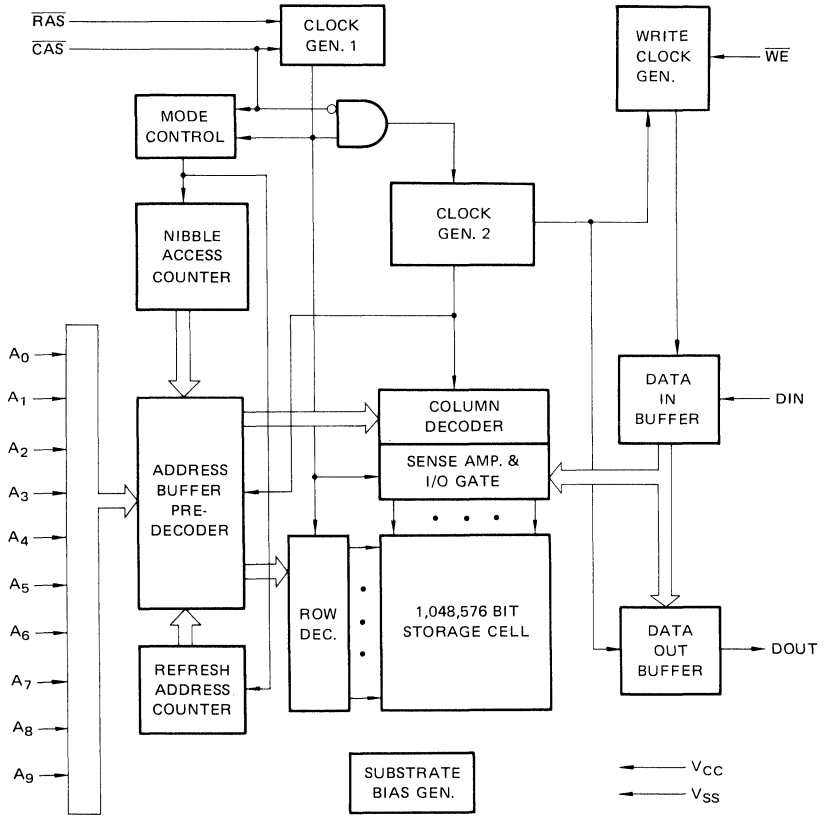
Rating		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} Relative to V_{SS}		V_{CC}	-1 to +7	V
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – BLOCK DIAGRAM



CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Value		Unit
		Typ	Max	
Input Capacitance, A_0 to A_9, D_{IN}	C_{IN1}		5	pF
Input Capacitance, $\overline{RAS}$ $\overline{CAS}$, $\overline{WE}$	C_{IN2}		5	pF
Output Capacitance, D_{OUT}	C_{OUT}		5	pF

2

RECOMMENDED OPERATING CONDITIONS

Parameter NOTES	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage [1]	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input High Voltage, All inputs [1]	V_{IH}	2.4	–	6.5	V	
Input Low Voltage, All inputs [1]	V_{IL}	-2.0	–	0.8	V	

2

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted) Notes 3

Parameter	NOTES	Conditions	Symbol	Values		Unit
				Min	Max	
Operating Current (Average power supply current) 2	MB81C1001-70	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	I_{CC1}		75	mA
	MB81C1001-80				70	
	MB81C1001-10				60	
	MB81C1001-12				50	
Standby Current (Power supply current)	TTL level	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}		2.0	mA
	CMOS level	$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC}−0.2V			1.0	
Refresh Current 1 (Average power supply current) 2	MB81C1001-70	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	I_{CC3}		70	mA
	MB81C1001-80				65	
	MB81C1001-10				55	
	MB81C1001-12				45	
Nibble Mode Current 2	MB81C1001-70	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min	I_{CC4}		45	mA
	MB81C1001-80				45	
	MB81C1001-10				35	
	MB81C1001-12				25	
Refresh Current 2 (Average power current) 2	MB81C1001-70	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	I_{CC5}		70	mA
	MB81C1001-80				65	
	MB81C1001-10				55	
	MB81C1001-12				45	
Input Leakage Current		0V ≦ V_{IN} ≦ 5.5V, 4.5V ≦ V_{CC} ≦ 5.5V, V_{SS} = 0V; pins not under test = 0V	$I_{I(L)}$	−10	10	μA
Output Leakage Current		0V ≦ V_{OUT} ≦ 5.5V; Data out disabled	$I_{O(L)}$	−10	10	
Output High Voltage		I_{OH} = −5mA	V_{OH}	2.4		V
Output Low Voltage		I_{OL} = 4.2mA	V_{OL}		0.4	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter NOTES	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh	t_{REF}		8.2		8.2		8.2		8.2	ms
2	Random Read/Write Cycle Time	t_{RC}	140		155		180		210		ns
3	Read-Modify-Write Cycle Time	t_{RWC}	167		182		210		245		ns
4	Access Time from $\overline{RAS}$ 6 9	t_{RAC}		70		80		100		120	ns
5	Access Time from $\overline{CAS}$ 7 9	t_{CAC}		25		25		25		35	ns
6	Access Time from Column Address 8 9	t_{AA}		43		45		50		60	ns
7	Output Data Hold Time	t_{OH}	7		7		7		7		ns
8	Output Buffer Turn on Delay Time	t_{ON}	5		5		5		5		ns
9	Output Buffer Turn Off Delay Time 10	t_{OFF}		25		25		25		25	ns
10	Transition Time	t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time	t_{RP}	60		65		70		80		ns
12	$\overline{RAS}$ Pulse Width	t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time	t_{RSH}	25		25		30		35		ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		0		ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time 11 12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25		25		30		35		ns
17	$\overline{CAS}$ Hold Time	t_{CSH}	70		80		100		120		ns
18	$\overline{CAS}$ Precharge Time ($\overline{C}$-B-$\overline{R}$ Cycle) 17	t_{CPN}	15		15		15		15		ns
19	Row Address Set Up Time	t_{ASR}	0		0		0		0		ns
20	Row Address Hold Time	t_{RAH}	10		12		15		15		ns
21	Column Address Set Up Time	t_{ASC}	0		0		0		0		ns
22	Column Address Hold Time	t_{CAH}	15		15		15		20		ns
23	$\overline{RAS}$ to Column Address Delay Time 13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	43		45		50		60		ns
25	Read Command Set Up Time	t_{RCS}	0		0		0		0		ns

2

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter NOTES	Symbol	MB81C1001-70		MB81C1001-80		MB81C1001-10		MB81C1001-12		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
26	Read Command Hold Time Referenced to $\overline{RAS}$ 14	t_{RRH}	0		0		0		0		ns
27	Read Command Hold Time Referenced to $\overline{CAS}$ 14	t_{RCH}	0		0		0		0		ns
28	Write Command Set Up Time 15	t_{WCS}	0		0		0		0		ns
29	Write Command Hold Time	t_{WCH}	15		15		15		20		ns
30	$\overline{WE}$ Pulse Width	t_{WP}	15		15		15		20		ns
31	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	22		22		25		30		ns
32	Write Commnd to $\overline{CAS}$ Lead Time	t_{CWL}	17		17		20		25		ns
33	D_{IN} Set Up Time	t_{DS}	0		0		0		0		ns
34	D_{IN} Hold time	t_{DH}	15		15		15		20		ns
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time 15	t_{RWD}	70		80		100		120		ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time 15	t_{CWD}	25		25		30		35		ns
37	Column Address to $\overline{WE}$ Delay Time 15	t_{AWD}	43		45		50		60		ns
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		0		0		ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		0		0		ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		15		15		20		ns
41	Access Time from $\overline{CAS}$ (Counter Test Cycle)	t_{CAT}		43		45		50		60	ns
50	Nibble Mode Read/Write Cycle Time	t_{NC}	50		50		55		60		ns
51	Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	67		67		75		85		ns
52	Access Time from $\overline{CAS}$ Precharge 9 16	t_{NPA}		45		45		50		55	ns
53	Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	15		15		15		15		ns

NOTES:

[1] Referenced to V_{SS}.

[2] I_{CC} depends on the output load conditions and cycle rate. The specified values are obtained with the output open.
I_{CC} depends on the number of address changes as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
I_{CC4} is specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.

[3] An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

[4] AC characteristics assume t_T = 5 ns.

[5] V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

[6] Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.

[7] If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

[8] If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

[9] Measured with a load equivalent to two TTL loads and 100 pF.

[10] t_{OFF} is specified that output buffer changes to high impedance state.

[11] Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

[12] t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).

[13] Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

[14] Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

[15] t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restructive operating parameter. They are included in the data sheet as the electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin.
If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the D_{OUT} pin, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, and t_{RAL} specifications.

[16] t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).

[17] Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only

2

Fig. 2 – t_{RAC} vs t_{RCD}

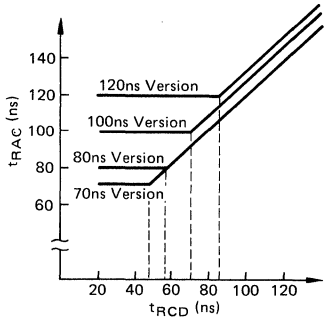
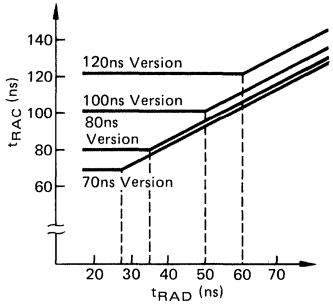


Fig. 3 – t_{RAC} vs t_{RAD}



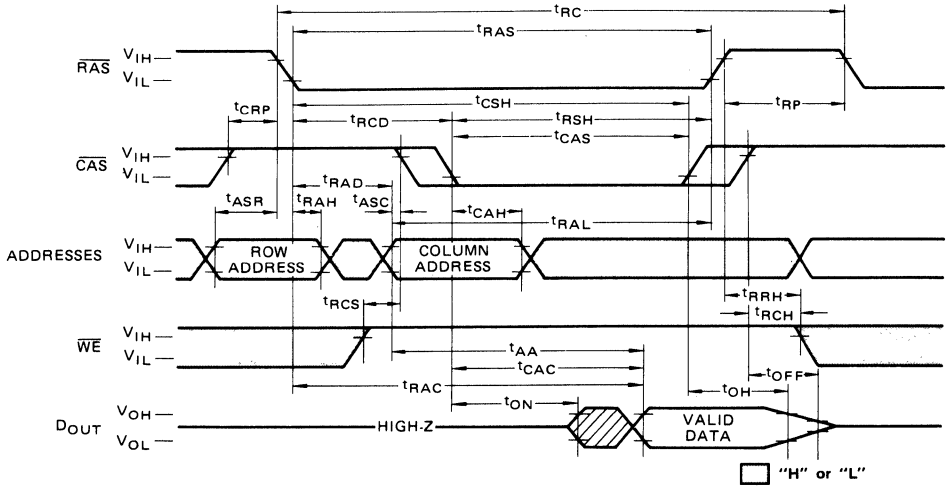
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	Valid	Valid	–	Valid	O*	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	O*	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	Valid	Valid	X→ Valid	Valid	O*	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$-only Refresh Cycle	L	H	X	Valid	–	–	High-Z	O	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	L	L	X	–	–	–	High-Z	O	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L	X	–	–	–	Valid	O	Previous data is kept.

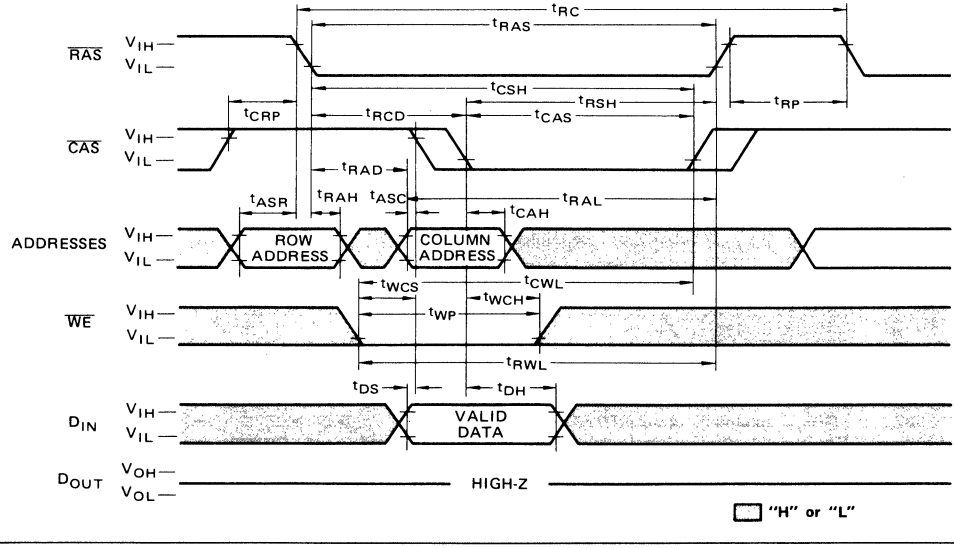
X; "H" or "L"
* ; It is impossible in nibble mode.

2

Read Cycle

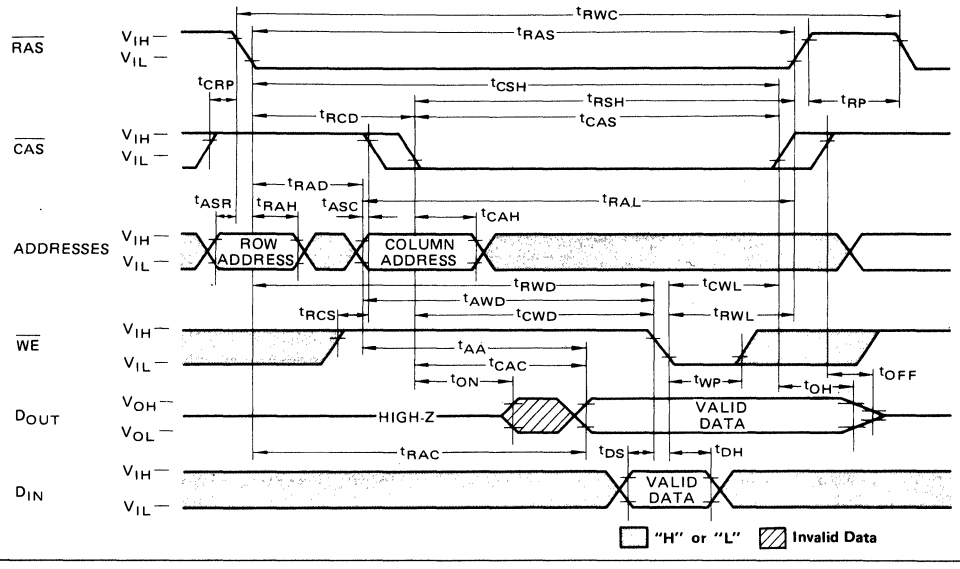


Write Cycle (Early Write)

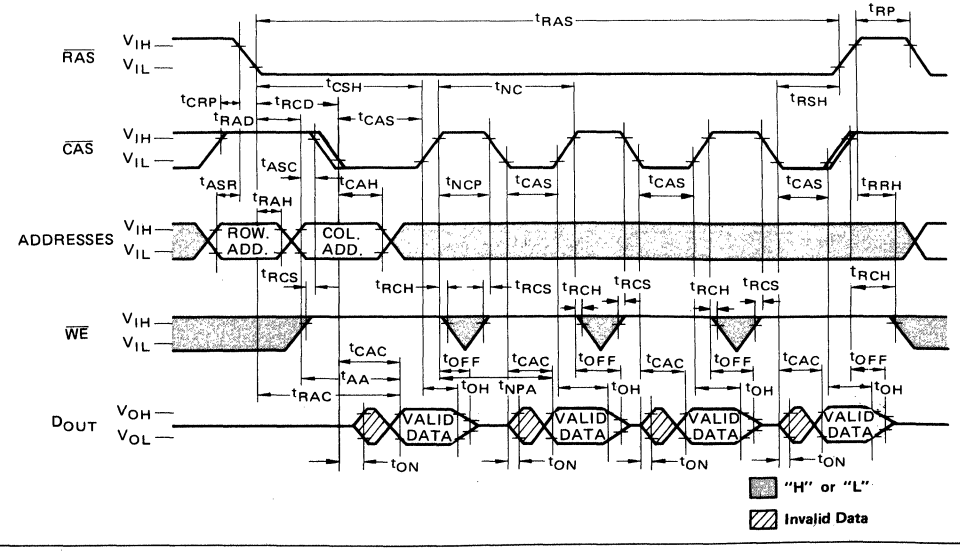


2

Read-Write/Read-Modify-Write Cycle

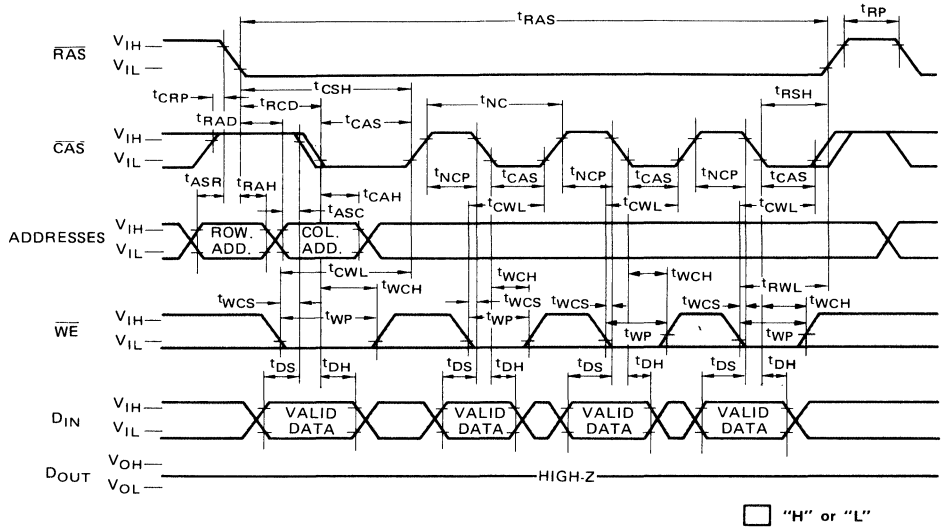


Nibble Mode Read Cycle

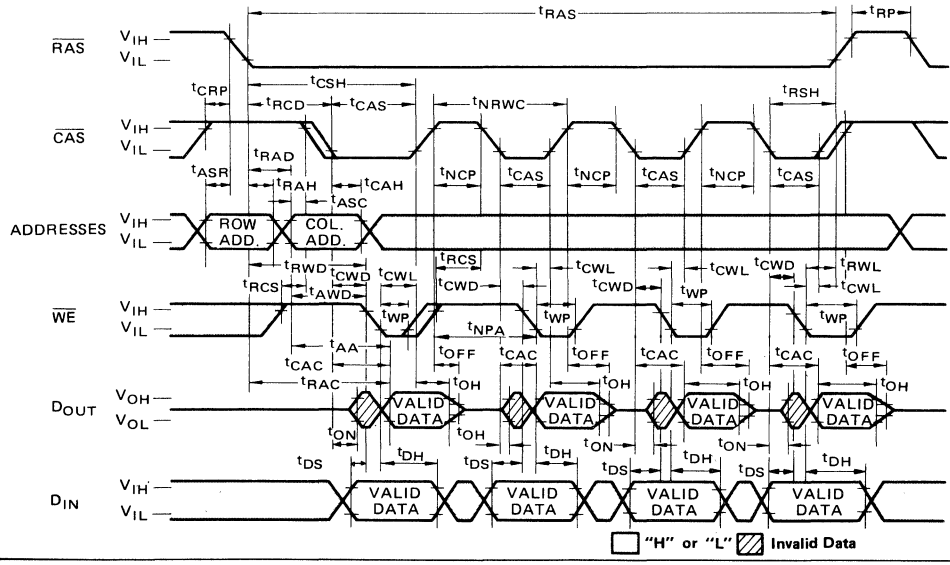


2

Nibble Mode Write Cycle (Early Write)



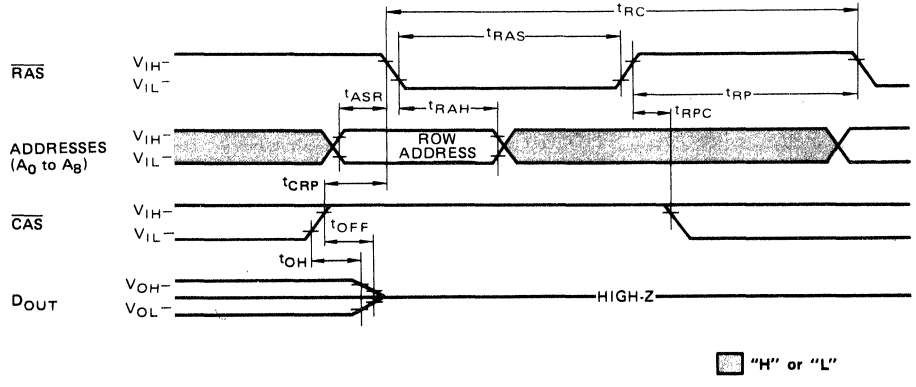
Nibble Mode Read-Modify-Write Cycle



2

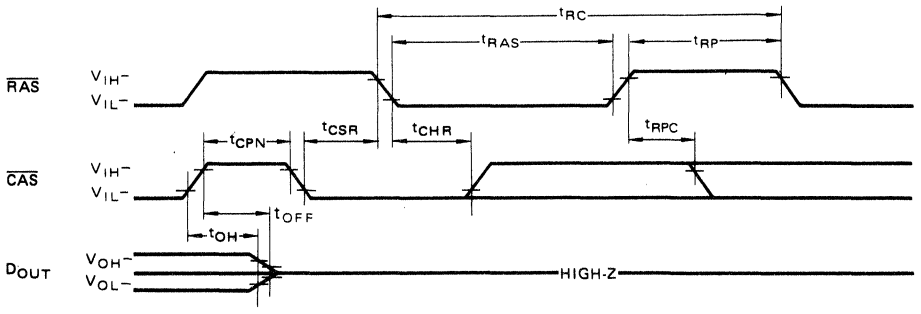
$\overline{RAS}$-Only Refresh Cycle

NOTE: $\overline{WE}$, D_{IN} = "H"or"L", A_9 = V_{IH} or V_{IL}

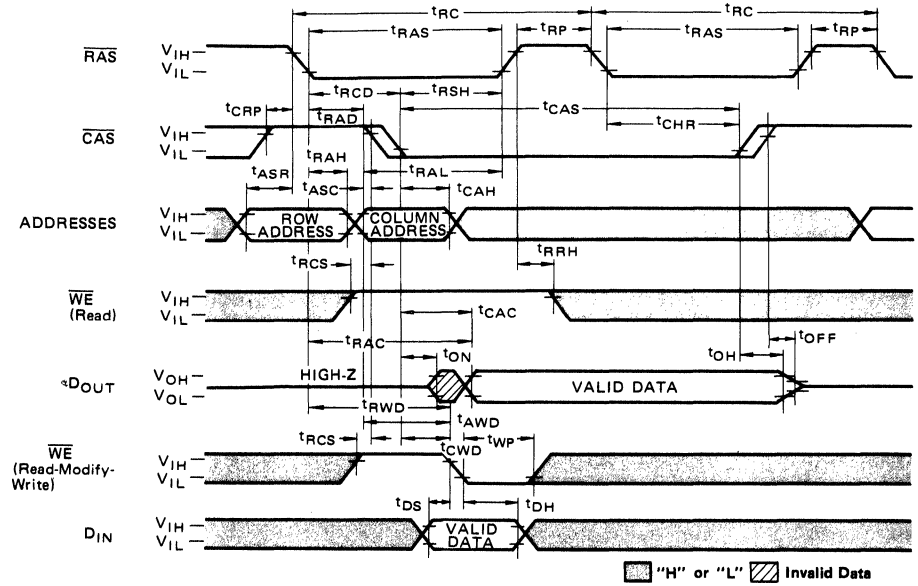


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

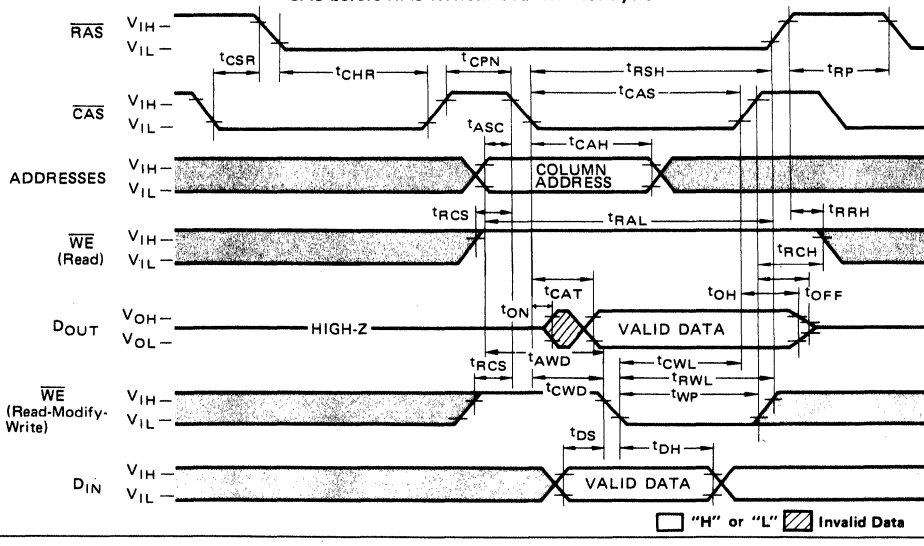
NOTE: Address, $\overline{WE}$, D_{IN} = "H"or"L"



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of twenty binary input address bits are required to decode any one of the 1,048,576 storage cells within the MB 81C1001. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe ($\overline{RAS}$). The ten column address bits are established on the address input pin (A_0 to A_9) and latched with the Column Address Strobe ($\overline{CAS}$). All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min) + t_T.
Therefore, to get valid data within t_{RAC}, it is necessary to apply column address within t_{RAD} (max).
If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occure later.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. Data input is ignored during read cycle. Data output is high impedance state during write cycle.

Data Input:
Data is written into the MB 81C1001 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-modify-write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is high impedance state until $\overline{CAS}$ is brought low. In a read or read-modify-write cycle, the output becomes valid after t_{RAC} from the falling edge of $\overline{CAS}$ when t_{RCD} (max) is satisfied or after t_{CAC} when t_{RCD} is longer than t_{RCD} (max). The data output remains valid until $\overline{CAS}$ returns to high with t_{OH} and becomes high impedance state after t_{OFF}. In an early write cycle, the output buffer is high impedance state during the entire cycle. In a delayed write cycle, if t_{RWD} or t_{CWD} is less than t_{RWD} (min) or t_{CWD} (min), the output is invalid.

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" through-out the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output is remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with t_{OH}. During read cycle, the D_{IN} pin is "Don't Care". The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), or Column address input (t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and D_{IN} pin. The data on D_{IN} pin is latched with the latter falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL} and t_{RAL} must be satisfied the specifications.

Read-Modify-Write Cycle:
The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears at the D_{OUT} pin. After the current data is read out, modified data can be re-written into the same address quickly.

Nibble Mode Read/Write/Read-Modify-Write Cycle:
Nibble mode allows high speed serial read, write, or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row and 9 column address bits (RA0 to RA8 and CA0 to CA8). The 2 bits of addresses (RA9 and CA9) are used to select 1 of 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "H" then "L" while $\overline{RAS}$ remains "L". Toggling $\overline{CAS}$ causes RA9 and CA9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. Refer to the table 1 for nibble mode address sequence.
If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat.

Refresh:
The refresh of DRAM is executed by normal read, write or read-modify-write cycle, i.e., the cells on the one row line are refreshed by executing one of three cycles. 512 row address must be refreshed every 8.2 ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-written to the cell. The MB81C1001 also has three types of refresh modes, $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and Hidden refresh.

1. **$\overline{RAS}$-Only Refresh;**
   The $\overline{RAS}$-Only refresh is executed by keeping $\overline{RAS}$ "L" and keeping $\overline{CAS}$ "H" through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During $\overline{RAS}$-Only refresh, the D_{OUT} pin is kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB 81C1001 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The Hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuosly from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Table 1 – NIBBLE MODE ADDRESS SEQUENCE

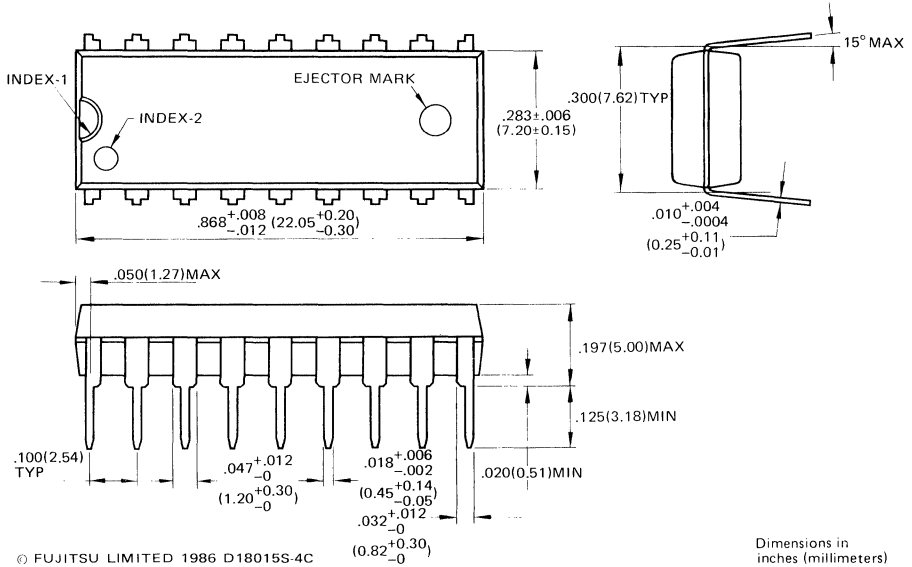
Sequence	Mode	Nibble bit	RA_9	Row address ($A_8 \sim A_0$)	CA_9	Column address ($A_8 \sim A_0$)	
$\overline{RAS}/\overline{CAS}$	Normal	1	0	1 0 1 0 1 0 1 0 0	0	1 0 1 0 1 0 1 0 0	Input address
Toggle $\overline{CAS}$	Nibble	2	1	1 0 1 0 1 0 1 0 0	0	1 0 1 0 1 0 1 0 0	Generated Internally
Toggle $\overline{CAS}$	Nibble	3	0	1 0 1 0 1 0 1 0 0	1	1 0 1 0 1 0 1 0 0	
Toggle $\overline{CAS}$	Nibble	4	1	1 0 1 0 1 0 1 0 0	1	1 0 1 0 1 0 1 0 0	
Toggle $\overline{CAS}$	Nibble	1	0	1 0 1 0 1 0 1 0 0	0	1 0 1 0 1 0 1 0 0	Sequence repeats

2

PACKAGE DIMENSIONS

(Suffix: -P)

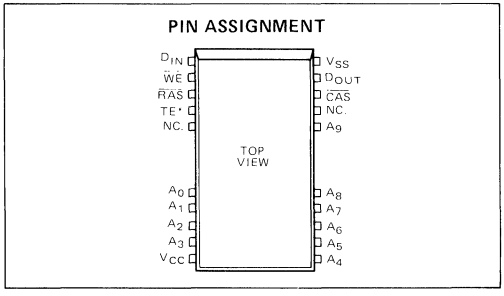
18 LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M04)

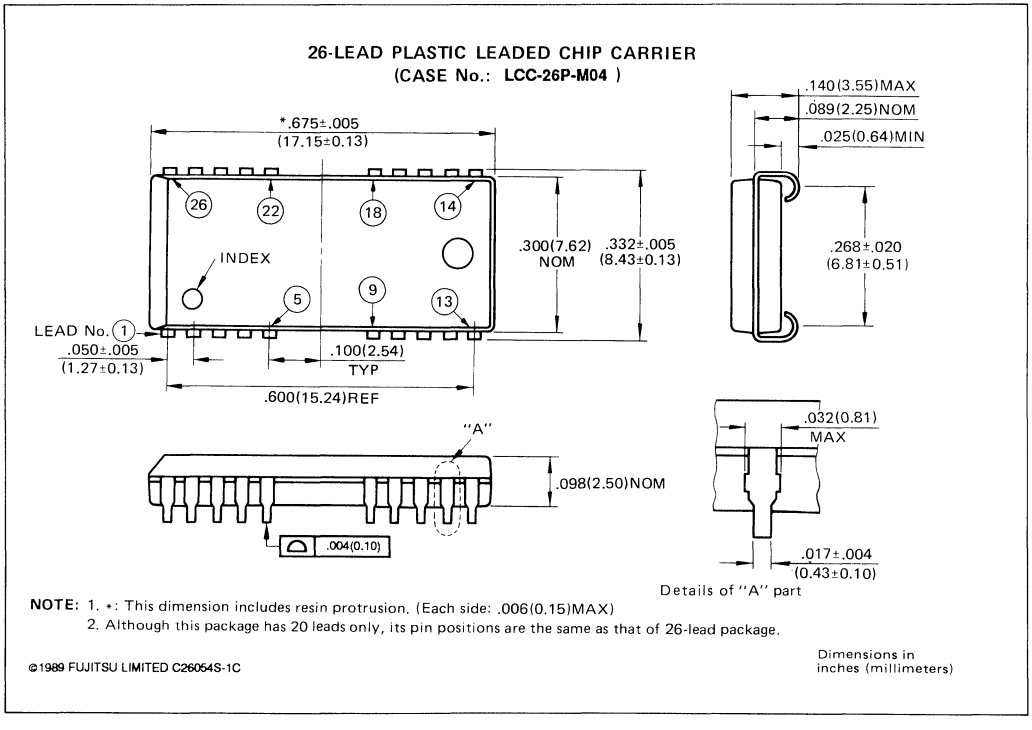


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -PJ)





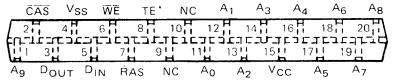
PACKAGE DIMENSIONS

(Suffix:-PSZ)

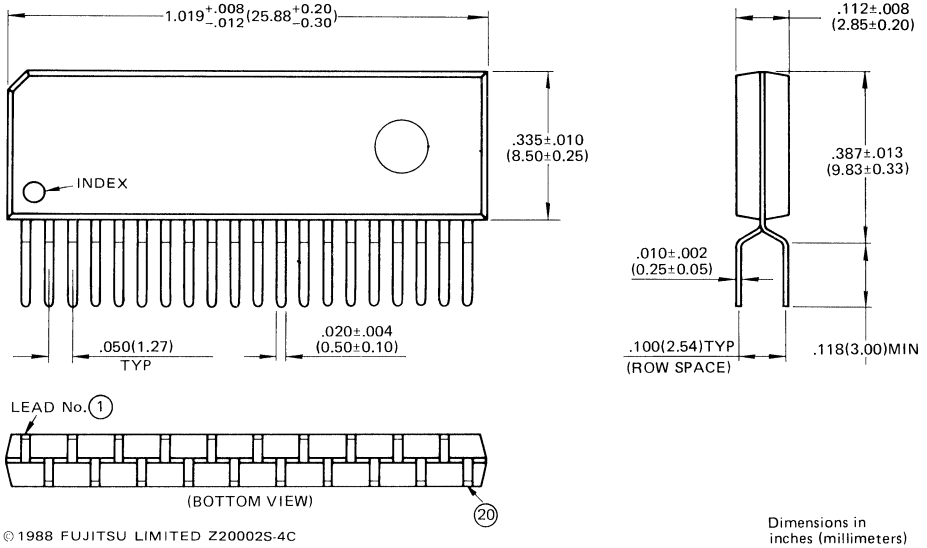
2

PIN ASSIGNMENT

(TOP VIEW)



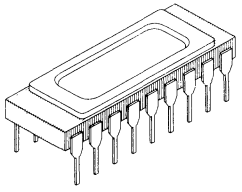
20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in
inches (millimeters)

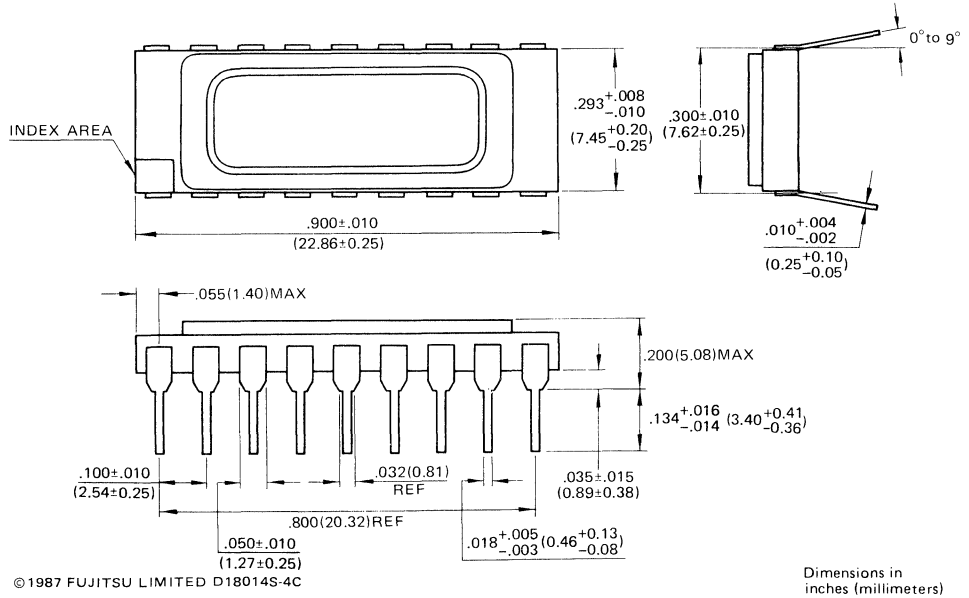
PACKAGE DIMENSIONS

(Suffix: -C)



DIP-18C-A01

18-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-18C-A01)



Dimensions in inches (millimeters)

2

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C1001A-60/-80/-10

CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

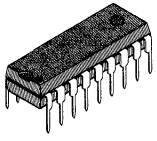
CMOS 1,048,576 X 1 Bit Nibble Mode Dynamic RAM

ADVANCE INFO.

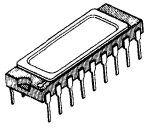
The Fujitsu MB81C1001A is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1001A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1001A High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

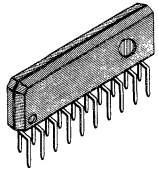


DIP-18P-M04



DIP-18C-A02

LCC-26P-M04



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C1001A-60	MB81C1001A-80	MB81C1001A-10
$\overline{RAS}$ Access Time	60ns max.	80ns max.	100ns max.
Randam Cycle Time	130ns min.	155ns min.	180ns min.
Address Access Time	30ns max.	40ns max.	50ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	25ns max.
Nibble Mode Cycle Time	35ns min.	42 ns min.	50ns min.
Low Power Dissipation • Operating current	330mW max.	275mW max.	248mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

November 1989
Edition 1.1

FUJITSU

DATA SHEET

MB81C1002-70/-80/-10/-12

CMOS 1,048,576 BIT STATIC COLUMN MODE DYNAMIC RAM

CMOS 1,048,576 X 1 BIT Static Column Mode Dynamic RAM

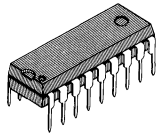
PRELIMINARY

The Fujitsu MB81C1002 is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1002 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high–band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

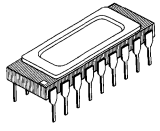
Fujitsu's advanced three–dimensional stacked capacitor cell technology makes the MB81C1002 High α–ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

The specification is applied to "BC" version revised with intent to realized faster access time. So faster speed version (70ns and 80ns) are available on this chip.

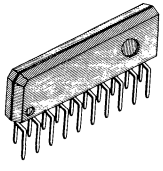


DIP–18P–M04



DIP–18C–A01

LCC–26P–M04



ZIP–20P–M02

PRODUCT LINE & FEATURES

Parameter	MB81C1002 -70	MB81C1002 -80	MB81C1002 -10	MB81C1002 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Static Column Mode Cycle Time	48ns min.	50ns min.	55ns min.	65ns min.
Low Power Dissipation • Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D–Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$–before–$\overline{RAS}$, or Hidden Refresh
- Static column Mode, Read–Modify–Write capacity
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

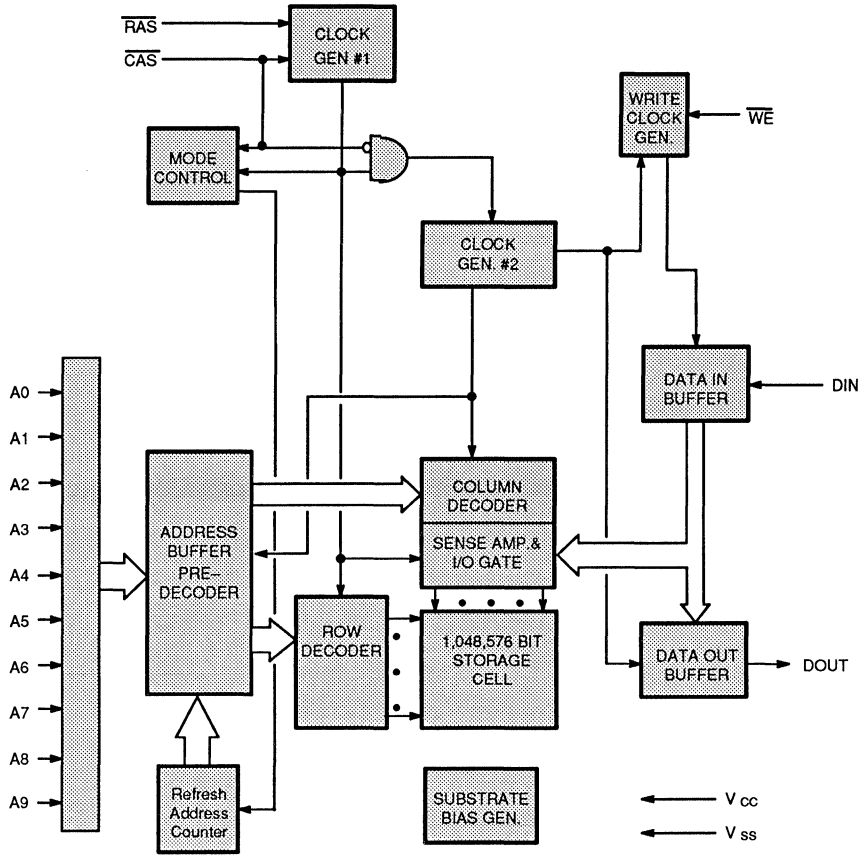
Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	–1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	–1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	–55 to +150	°C
	Plastic		–55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 — MB81C1002 DYNAMIC RAM—BLOCK DIAGRAM

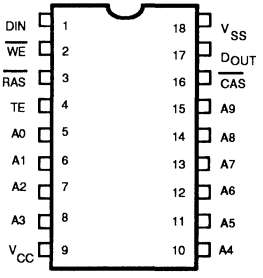


CAPACITANCE (T_A = 25°C, f = 1MHz)

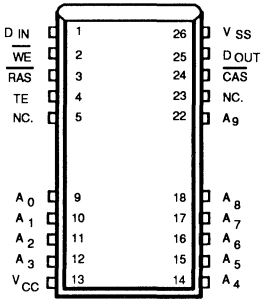
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D_{IN}	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, D_{OUT}	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

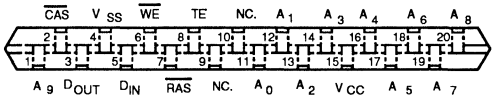
18–Pin DIP:
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
TE	Test Enable (will be available).
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

2

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Data is written into the MB81C1002 during write or read–modify–write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. In an early write cycle, data input is strobed by $\overline{CAS}$, and set up and hold times are referenced to $\overline{CAS}$. In a delayed write or read–modify–write cycle, $\overline{WE}$ is set low after $\overline{CAS}$. Thus, data input is strobed by $\overline{WE}$, and set up and hold times are referenced to $\overline{WE}$.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater then t_{RAD} (max).

STATIC COLUMN MODE OF OPERATION

The static column mode operation allows continuous read, write, or read–modify–write cycle within a rowby applying new column address. In the static column mode, $\overline{RAS}$ can be kept low throughout static column mode operation.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		V_{OH}	IOH = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	IOL = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V ≤ VIN ≤ 5.5V; 4.5V ≤ VCC ≤ 5.5V; VSS=0V;All other pins not under test =0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V ≤ VOUT ≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average power supply current)	MB81C1002–70	ICC_1	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C1002–80					70	
	MB81C1002–10					60	
	MB81C1002–12					50	
Standby current (Power supply current)	TTL level	ICC_2	$\overline{RAS}$=$\overline{CAS}$=VIH	—	—	2.0	mA
	CMOS level		$\overline{RAS}$=$\overline{CAS}$ ≥ VCC–0.2V			1.0	
Refresh current #1 (Average power supply current)	MB81C1002–70	ICC_3	$\overline{CAS}$=VIH, $\overline{RAS}$ cycling; t_{RC}= min	—	—	70	mA
	MB81C1002–80					65	
	MB81C1002–10					55	
	MB81C1002–12					45	
Static column mode current	MB81C1002–70	ICC_4	$\overline{RAS}$ = $\overline{CAS}$ =VIL cycling; t_{SC} = min	—	—	37	mA
	MB81C1002–80					35	
	MB81C1002–10					30	
	MB81C1002–12					23	
Refresh current #2 (Average power supply current)	MB81C1002–70	ICC_5	$\overline{RAS}$ cycling ; $\overline{CAS}$–before–$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C1002–80					65	
	MB81C1002–10					55	
	MB81C1002–12					45	

2

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1002-70		MB81C1002-80		MB81C1002-10		MB81C1002-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	167	—	182	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn on Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	21	t_{CPN}	15	—	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time	7	t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	20	—	20	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Hold Time		t_{WCH}	20	—	20	—	20	—	25	—	ns
29	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
30	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
31	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
32	DIN Set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
33	DIN Hold Time		t_{DH}	20	—	20	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1002-70		MB81C1002-80		MB81C1002-10		MB81C1002-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
34	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15,20	t_{RWD}	70	—	80	—	100	—	120	—	ns
35	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	25	—	30	—	35	—	ns
36	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	43	—	45	—	50	—	60	—	ns
37	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
38	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Hold Time for $\overline{CAS}$–before –$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
40	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Static Column Mode Read/Write Cycle Time		t_{SC}	48	—	50	—	55	—	65	—	ns
51	Static Column Mode Read–Modify–Write Cycle Time		t_{SRWC}	96	—	100	—	110	—	130	—	ns
52	Access Time Relative to Last Write	16	t_{ALW}	—	91	—	95	—	105	—	125	ns
53	Access Time from $\overline{WE}$ Precharge		t_{WPA}	—	25	—	25	—	30	—	35	ns
54	Output Hold Time for Column Address Change		t_{AOH}	10	—	10	—	10	—	10	—	ns
55	Write Latched Data Hold Time		t_{WOH}	0	—	0	—	0	—	0	—	ns
56	Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	17	t_{AHR}	15	—	15	—	15	—	15	—	ns
57	Last Write to Column Address Delay Time	18,19	t_{LWAD}	25	48	25	50	25	55	30	65	ns
58	Column Address Hold Time Referenced to Last Write		t_{AHLW}	91	—	95	—	105	—	125	—	ns
59	$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	70	—	80	—	100	—	120	—	ns
60	$\overline{WE}$ Inactive Time		t_{WI}	13	—	15	—	15	—	20	—	ns
61	Write Set Up Time for Output Disable	20	t_{WS}	0	—	0	—	0	—	0	—	ns
62	Write Hold Time for Output Disable	20	t_{WH}	0	—	0	—	0	—	0	—	ns
63	Static Column Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	15	—	ns
64	Write Command Hold Time Referenced to $\overline{RAS}$		t_{WHR}	5	—	5	—	5	—	5	—	ns

2

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200µs is required after power–up followed by any 8 $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leqq t_{RCD}$ (max), and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that write cycle only.
8. If $t_{RAD} \geqq t_{RAD}$ (max), access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
16. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{AWL} will be increased by the amount that t_{LWAD} exceeds the value shown.
17. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
18. Operation within the t_{LWAD} (max) limit insures that t_{AWL} (max) can be met. t_{LWAD}(max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
19. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T=5ns).
20. t_{WS}, t_{WH} and t_{RWD} are specified as a reference point only. If $t_{WS} \geqq t_{WS}$(min) and $t_{WH} \geqq t_{WH}$(min), the data output pin will remain High–Z state through entire cycle. If It $t_{RWD} \geqq t_{RWD}$(min), the data output will contain data read from the selected cell.
21. Assumes that $\overline{CAS}$ –before–$\overline{RAS}$ refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh counter test cycle only

Fig. 2 – t_{RAC} vs. t_{RCD}

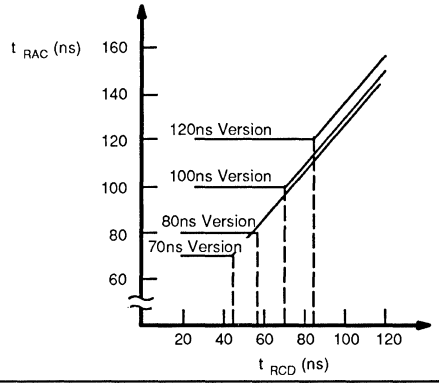
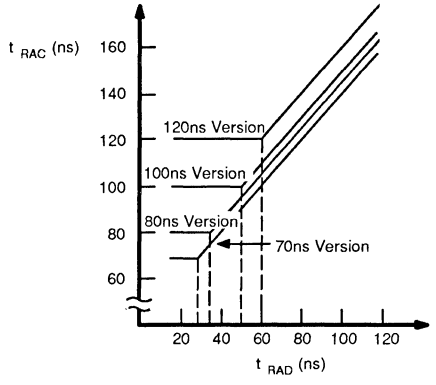


Fig. 3 – t_{RAC} vs. t_{RAD}



FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	O	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	*1 High-Z	O	$t_{WS} \geq t_{WS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	O	$t_{CWD} \geq t_{CWD}$ (min)
Static Column Mode Read Cycle	L	L	H	*2 Valid	Valid	—	Valid	X	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Static Column Mode Write Cycle	L	L	L	*2 Valid	Valid	Valid	*1 High-Z	X	
Static Column Mode Read–Modify–Write Cycle	L	L	H → L	*2 Valid	Valid	X → Valid	Valid	X	$t_{CWD} \geq t_{CWD}$ (min)
Static Column Mode Mixed Cycle	L	L	L/H	*2 Valid	Valid	Valid	High-Z or Valid	X	
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	O	
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	O	Previous data is kept

Notes:

X : "H" or "L"

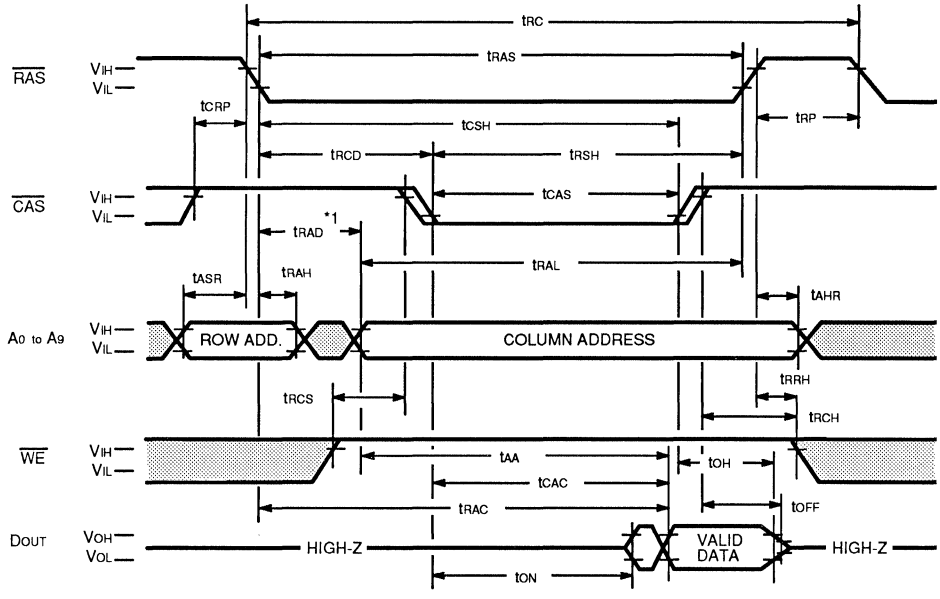
*1: If $t_{WS} < t_{WS}$ (min) and $t_{WH} < t_{WH}$ (min), the data output become invalid.

*2: After first cycle, row address is not necessary.

2

TIMING DIAGRAMS

Fig. 4 – READ CYCLE



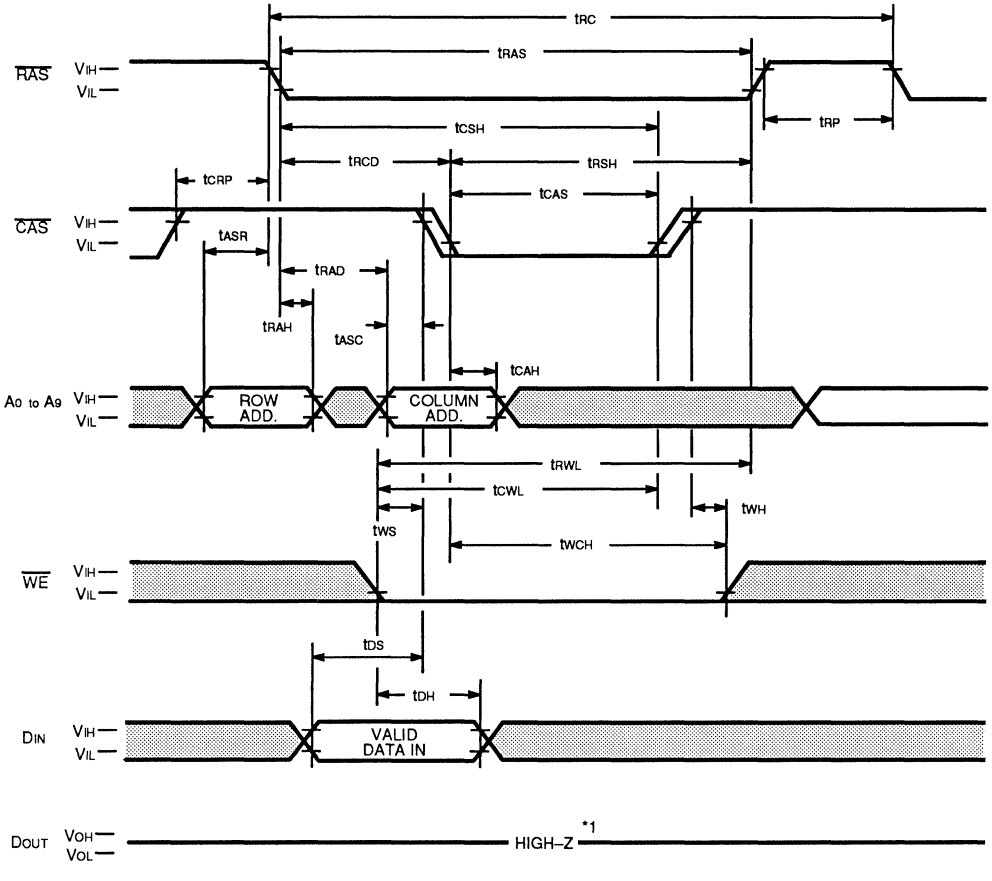
*1; If tRAD ≥ tRAD (max), access time is tCAC or tAA whichever occur later.

"H" or "L"

DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" through out the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remain valid with $\overline{CAS}$ "L", i.e., if $\overline{CAS}$ goes "H", the data becomes invalid with tDH. During read cycle, the DIN pin is "H" or "L". The acces time is determined by $\overline{RAS}$(tRAC), $\overline{CAS}$(tCAC), or Column address input(tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is tCAC or tAA whichever occur later.

Fig. 5 – WRITE CYCLE (Early Write)



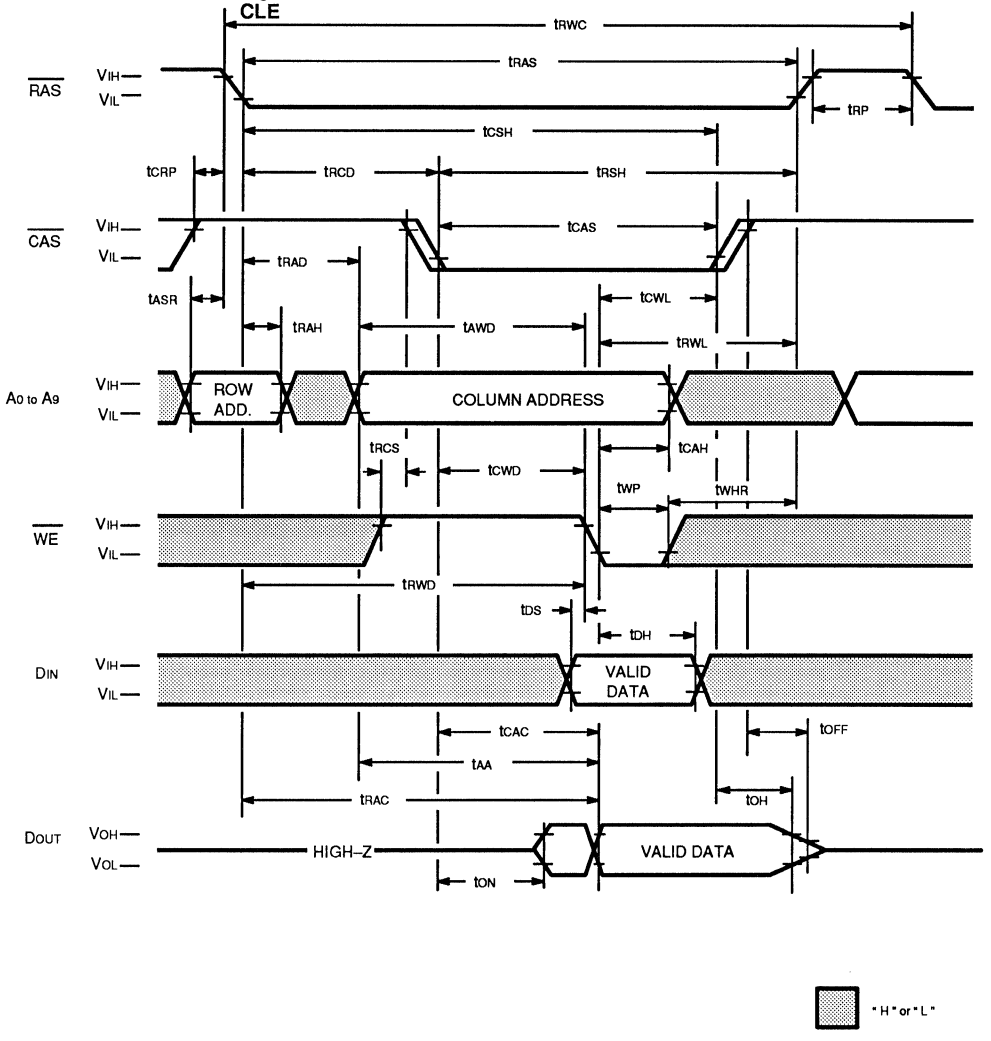
*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high–Z.

DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pin. The data on DIN pin is latched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, duringwrite cycle, t_{RWL}, t_{CWL} and t_{RAL} must be satisfied the specifications.

2

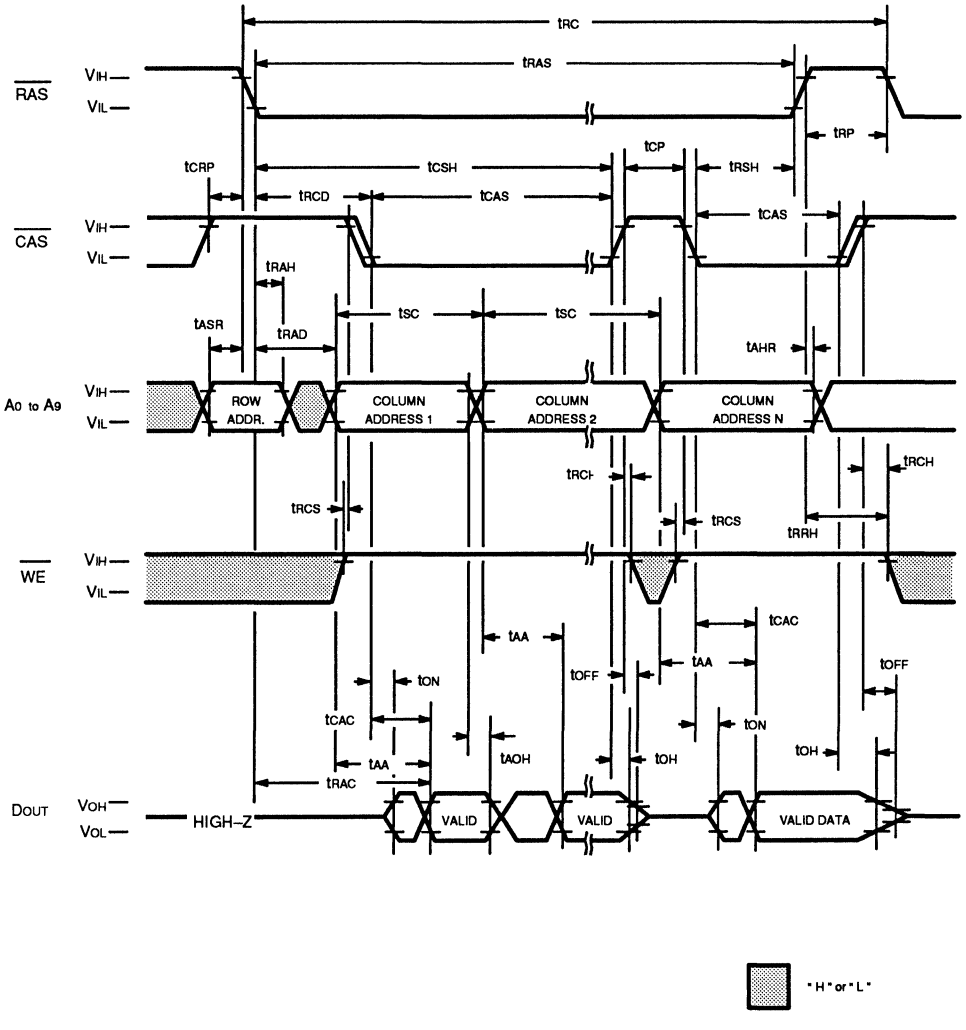
Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE



DESCRIPTION

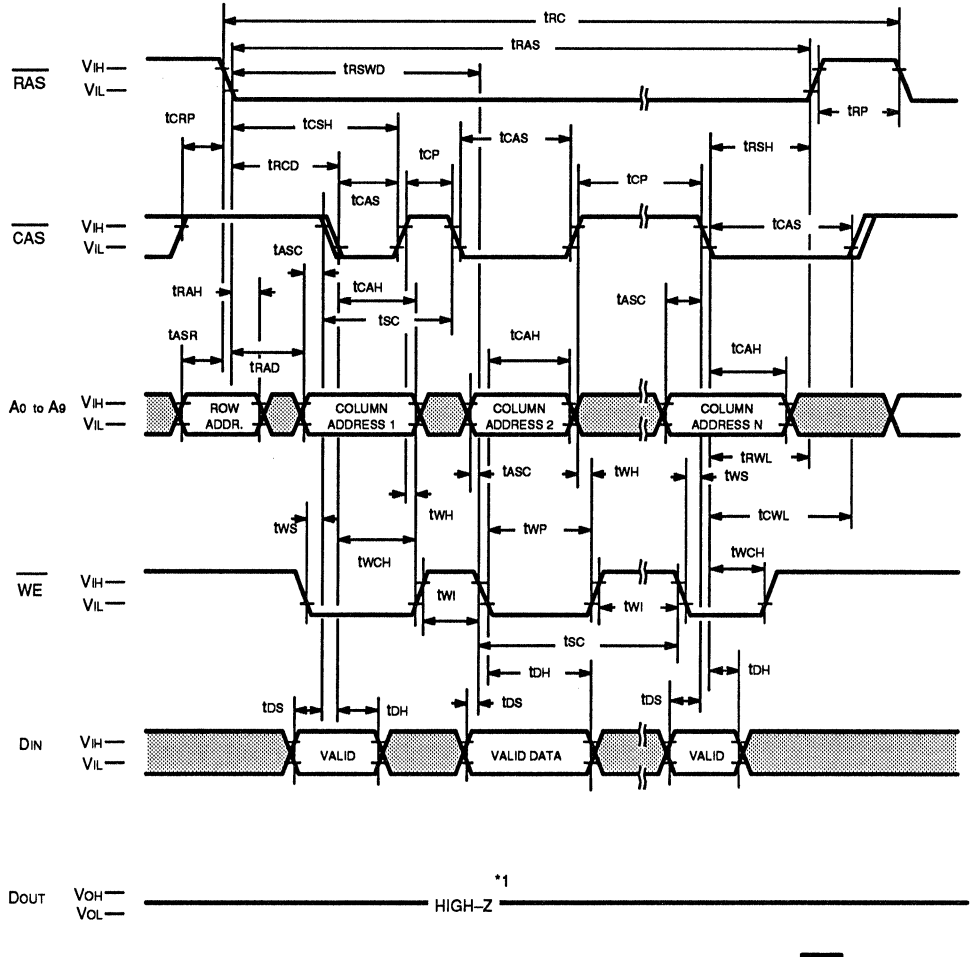
The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DOUT pin. This new data is written into the same address as read out.

Fig. 7 – STATIC COLUMN MODE READ CYCLE



2

Fig. 8 – STATIC COLUMN MODE WRITE CYCLE

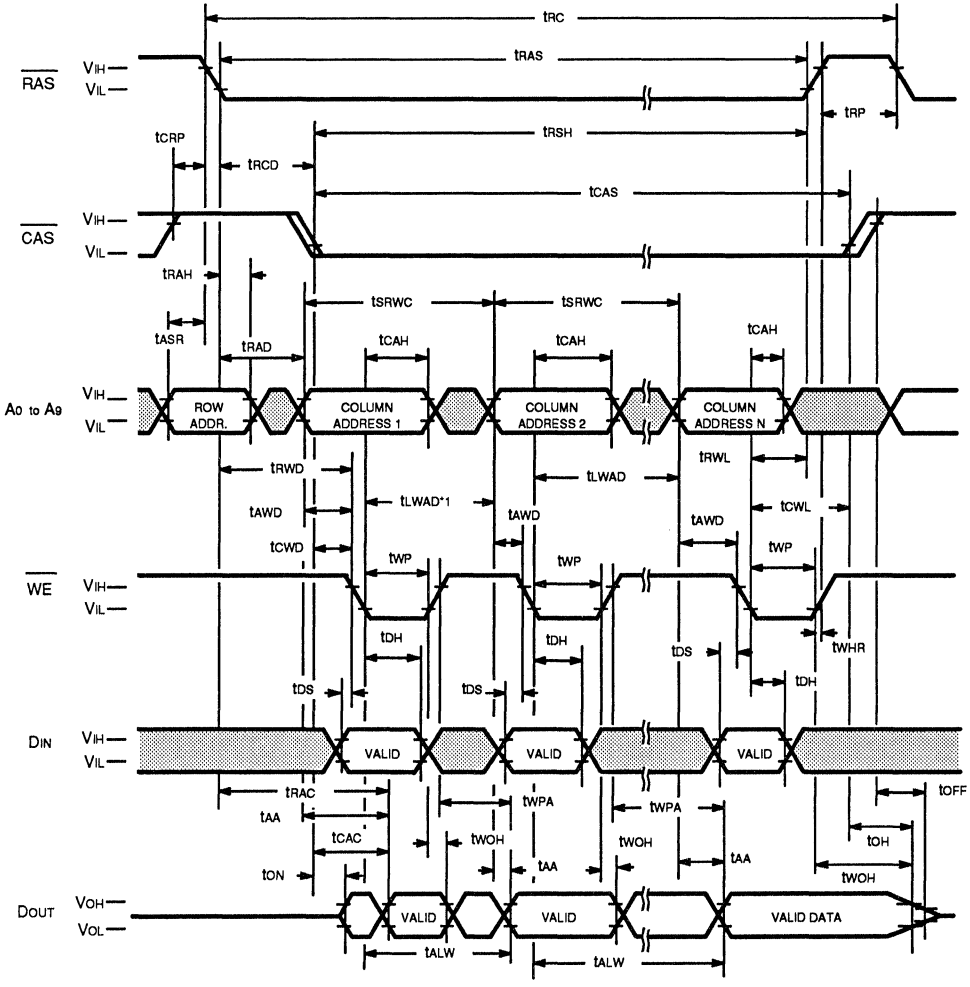


*1; If $t_{WS} \geqq t_{WS}$ (min) and $t_{WH} \geqq t_{WH}$ (min), D_{OUT} is high-Z.

DESCRIPTION

In a static column mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. It is not necessary to bring both $\overline{WE}$ and $\overline{CAS}$ "L", only one signal should be brought "L" while the other signal is toggled. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static column mode write cycle.

Fig. 9 – STATIC COLUMN MODE READ–MODIFY–WRITE CYCLE



*1; If tLWAD (min) ≤ tLWAD ≤ tLWAD (max), tALW = tSC (min) + tAA (max).

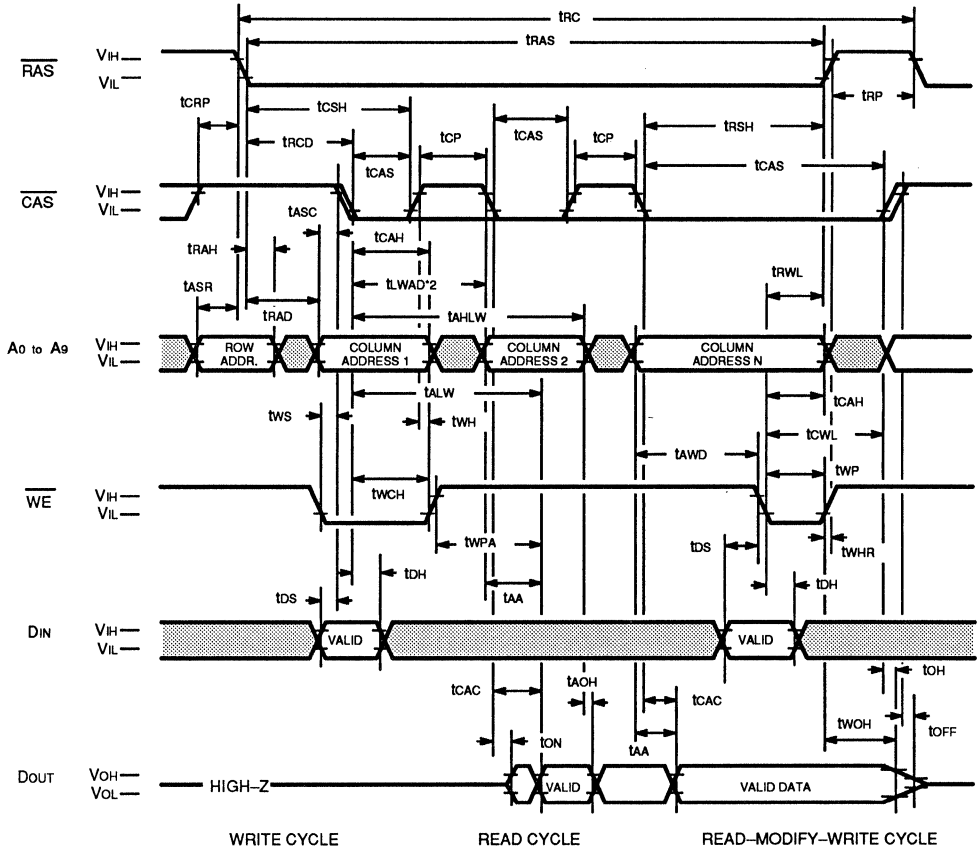
"H" or "L"

DESCRIPTION

In the static column mode read-modify-write cycle, $\overline{WE}$ goes low after tAWD from the column address inputs and tCWD from the faling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{WE}$.

2

Fig. 10 – STATIC COLUMN MODE MIXED CYCLE *1



*1; This is an example of static column mode mixed cycle.
*2; If tLWAD is satisfied its min/max value, tALW = tSC (min) + tAA (max)

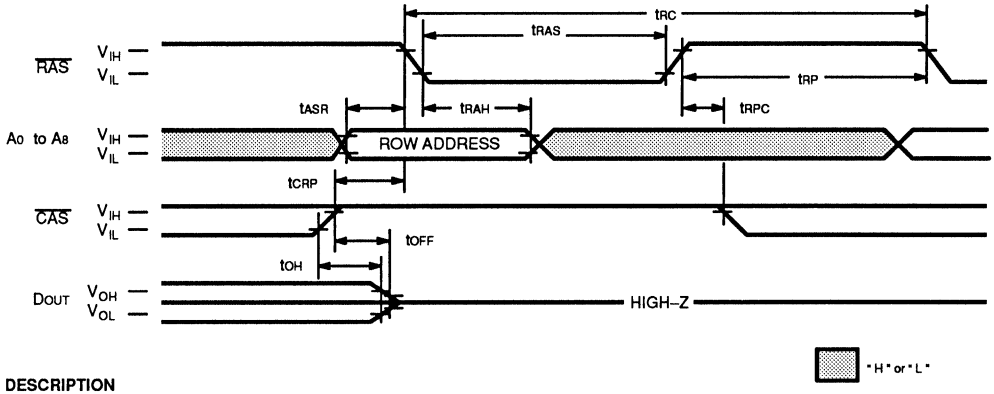
"H" or "L"

DESCRIPTION

In the static column mode, read, write, and read-modify-write cycles can be mixed in any order.
In the next read cycle of static column mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. tALW from the falling edge of $\overline{WE}$ or $\overline{CAS}$ at previous write cycle.
2. tAA from the column address inputs.
3. tWPA from the rising edge of $\overline{WE}$ at the read cycle.
4. tCAC from the falling edge of $\overline{CAS}$.

Fig. 11 – $\overline{RAS}$–ONLY REFRESH CYCLE
NOTE: A9, $\overline{WE}$, DIN = " H " or " L "

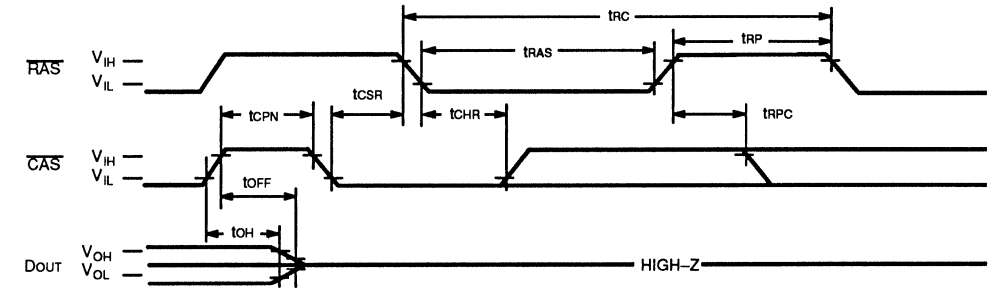


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DOUT pin is kept in a high-impedance state.

Fig. 12 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH CYCLE
NOTE: A0 to A9, $\overline{WE}$, DIN = " H " or " L "

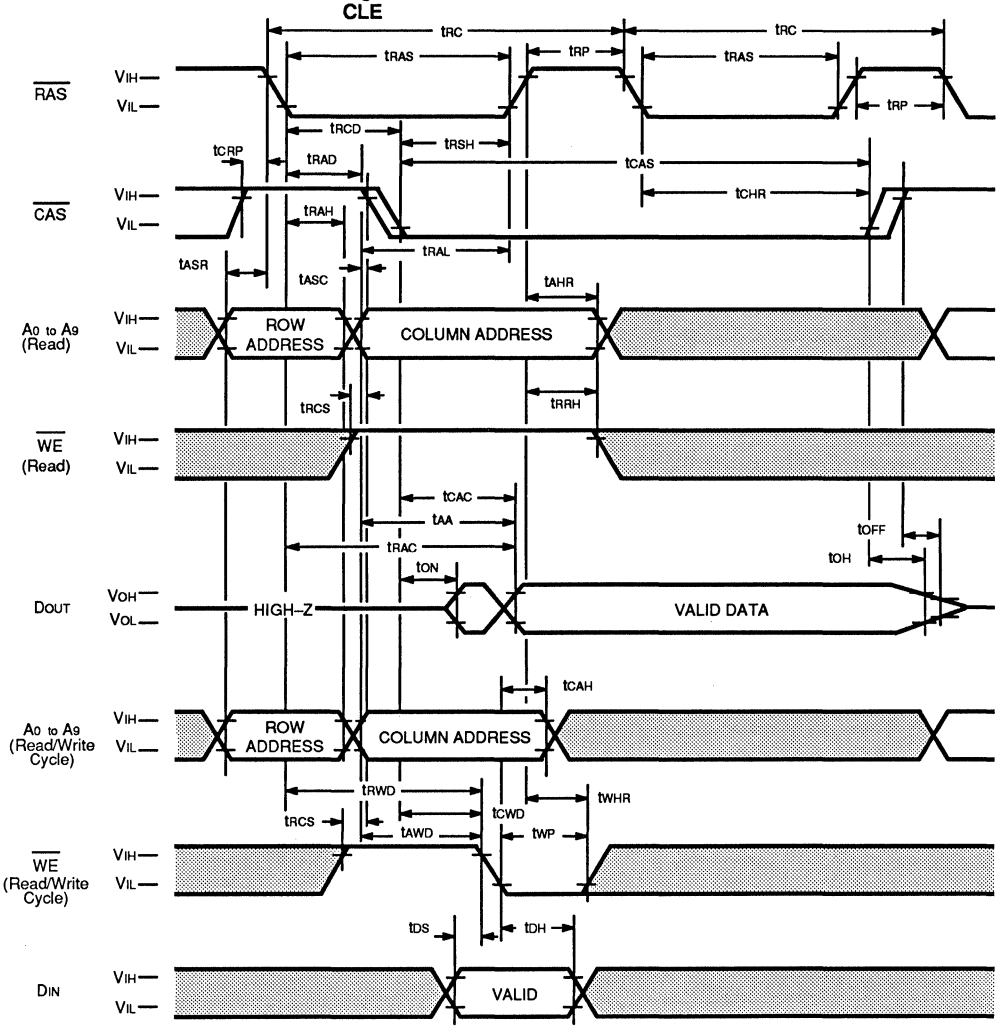


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

Fig. 13 – HIDDEN REFRESH CYCLE

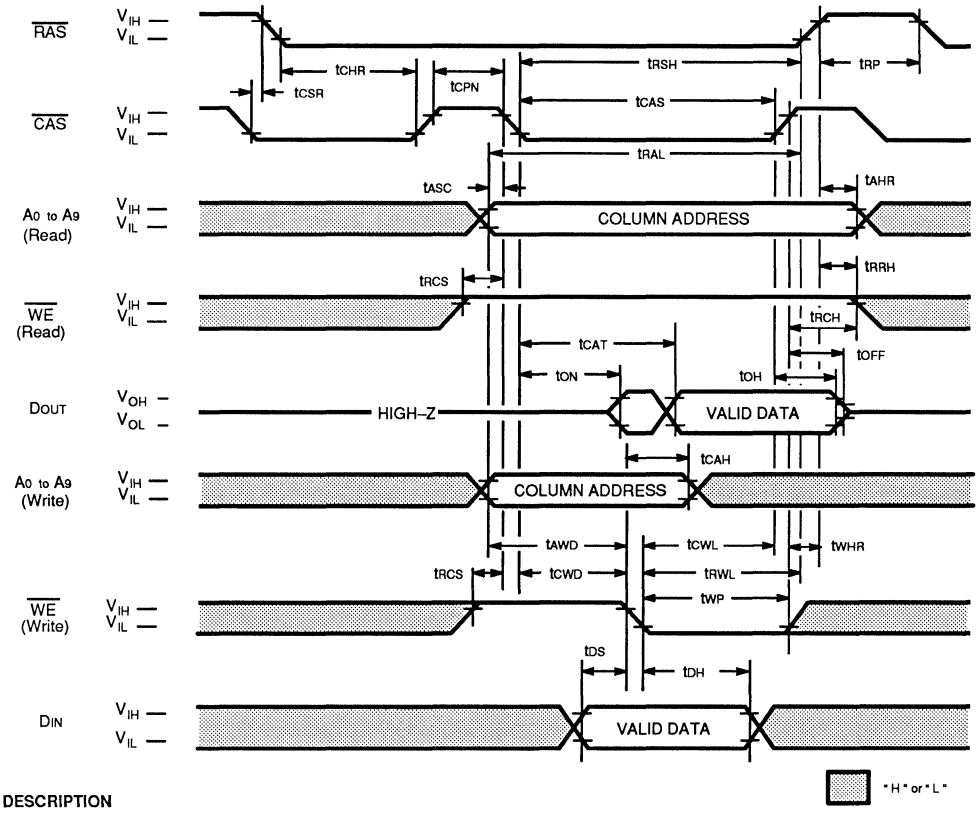


DESCRIPTION

"H" or "L"

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A9 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of $\overline{CAS}$.

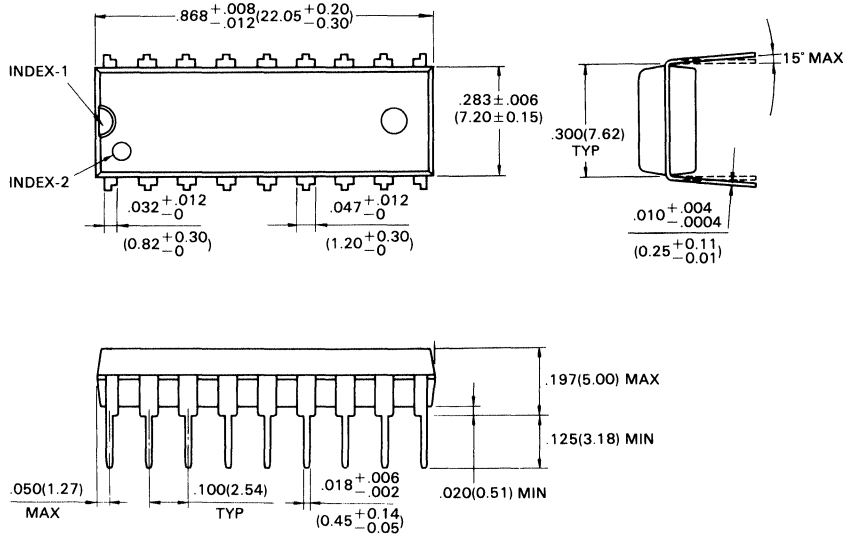
The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
4) Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix: –P)

18–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–18P–M04)

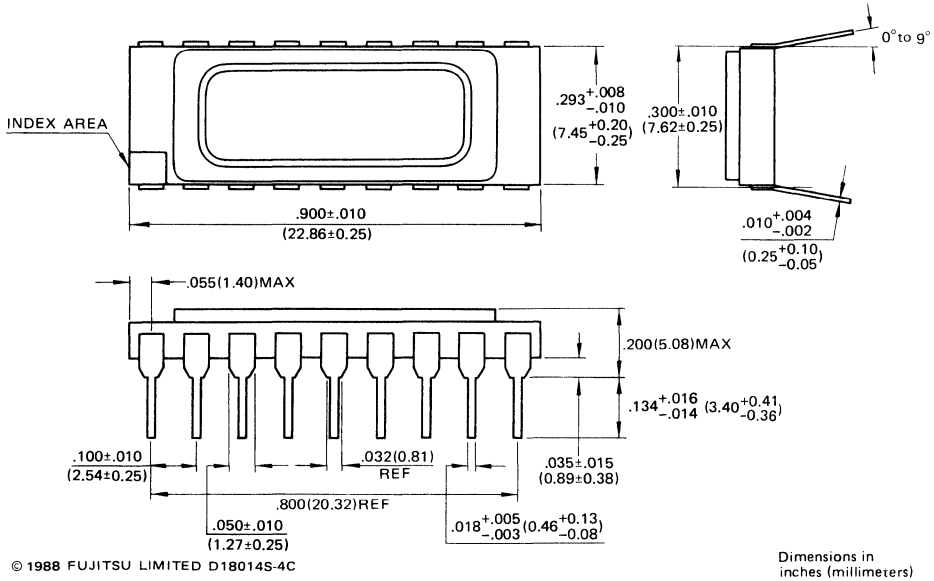


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –C)

18–LEAD CERAMIC (METAL SEAL) DUAL IN–LINE PACKAGE
(CASE No.: DIP–18C–A01)

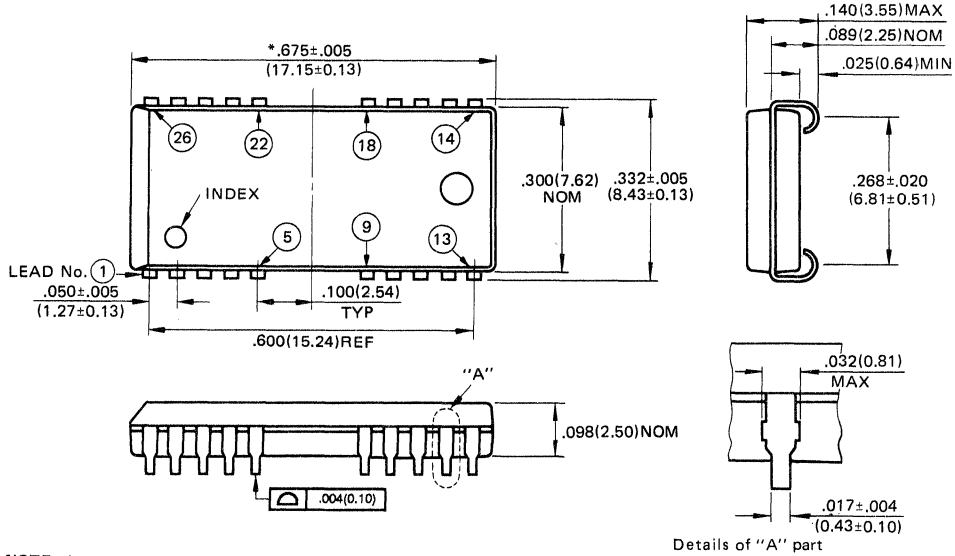


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER (SOJ-26)
(CASE No.: LCC-26P-M04)



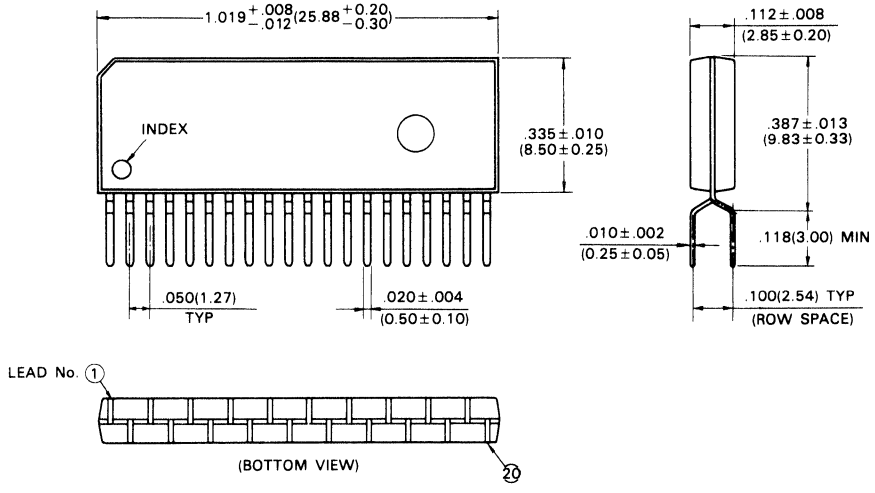
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: –PSZ)

20–LEAD PLASTIC ZIGZAG–IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



Dimensions in
inches (millimeters)

2

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C1002A-60/-80/-10

CMOS 1,048,576 BIT STATIC COLUMN MODE DYNAMIC RAM

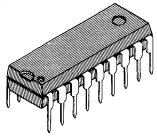
CMOS 1,048,576 X 1 BIT Static Column Mode Dynamic RAM

The Fujitsu MB81C1002A is CMOS fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1002A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C1002A High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

ADVANCE INFO.

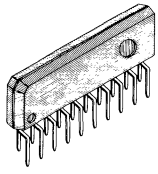


DIP-18P-M04

T.B.D

DIP-18C-XXX

LCC-26P-M04



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C1002A-60	MB81C1002A-80	MB81C1002A-10
$\overline{RAS}$ Access Time	60ns max.	80ns max.	100ns max.
Randam Cycle Time	130ns min.	155ns min.	180ns min.
Address Access Time	30ns max.	40ns max.	50ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	25ns max.
Static Column Mode Cycle	35ns min.	45ns min.	55ns max.
Low Power Dissipation • Operating current	330mW max.	275mW max.	248mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static column Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

December 1989
Edition 1.2

FUJITSU

DATA SHEET

MB81C4256-70/-80/-10/-12

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 262,144 x 4 BIT Fast Page Mode DYNAMIC RAM

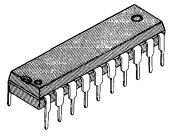
The Fujitsu MB81C4256 is CMOS fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C4256 High α-ray soft error immunity and long refresh time.

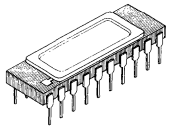
The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

The specification is applied to "BC" version revised with intent to realized faster access time. So faster speed version (70ns and 80ns) are available on this chip.

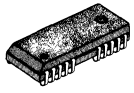
PRELIMINARY



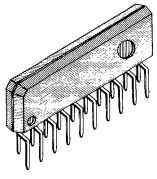
DIP-20P-M03



DIP-20C-A03



LCC-26P-M04



ZIP-20P-M02

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PRODUCT LINE & FEATURES

Parameter	MB81C4256 -70	MB81C4256 -80	MB81C4256 -10	MB81C4256 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Randam Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Fast Page Mode Cycle Time	53ns min.	55ns min.	60ns min.	70ns min.
Low Power Dissipation • Operating current	413mW max.	385mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capacity
- On chip substrate bias generator for high performance

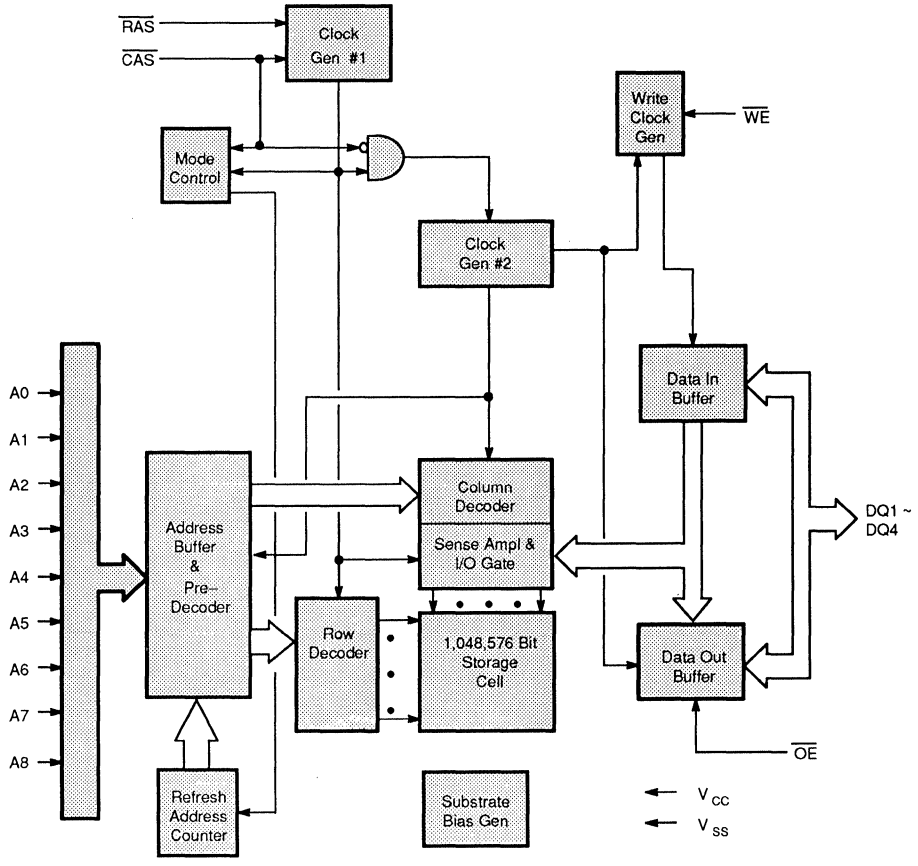
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 – MB81C4256 DYNAMIC RAM – BLOCK DIAGRAM

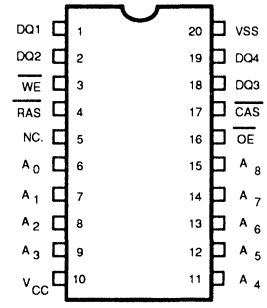


CAPACITANCE (T_A = 25°C, f = 1MHz)

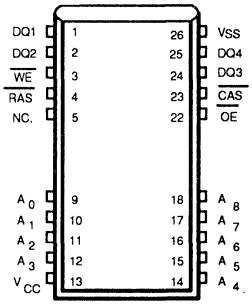
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

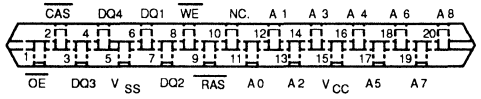
20–Pin DIP :
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

2

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD}, t_{RAD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512–bits can be accessed and, when multiple MB 81C4256s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤ V_{IN} ≤ 5.5V; 4.5V≤ V_{CC} ≤ 5.5V; V_{SS} = 0V; All other pins under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤ V_{OUT} ≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply Current) [2]	MB81C4256–70	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C4256–80					70	
	MB81C4256–10					60	
	MB81C4256–12					50	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB81C4256–70	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	70	mA
	MB81C4256–80					65	
	MB81C4256–10					55	
	MB81C4256–12					45	
Fast Page Mode current [2]	MB81C4256–70	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	47	mA
	MB81C4256–80					45	
	MB81C4256–10					40	
	MB81C4256–12					33	
Refresh current #2 (Average power supply current) [2]	MB81C4256–70	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C4256–80					65	
	MB81C4256–10					55	
	MB81C4256–12					45	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70		MB81C4256-80		MB81C4256-10		MB81C4256-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	197	—	212	—	240	—	275	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)	19	t_{CPN}	15	—	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4256-70		MB81C4256-80		MB81C4256-10		MB81C4256-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$–before–$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before–$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
38	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	22	—	25	—	30	ns
39	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	—	25	ns
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	0	—	ns
42	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	25	—	ns
43	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	0	—	ns
44	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	0	—	ns
45	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	53	—	55	—	60	—	70	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	105	—	107	—	115	—	130	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	53	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	15	—	ns

Notes:

1. Referenced to V_{SS}
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200μs is required after power–up followed by any eight $\overline{RAS}$–only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$–before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min)
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is shortened, t_{CPA} is longer than t_{CPA} (max).
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

2

Fig. 2 – t_{RAC} vs. t_{RCD}

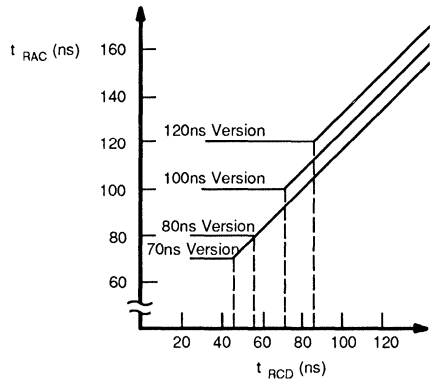
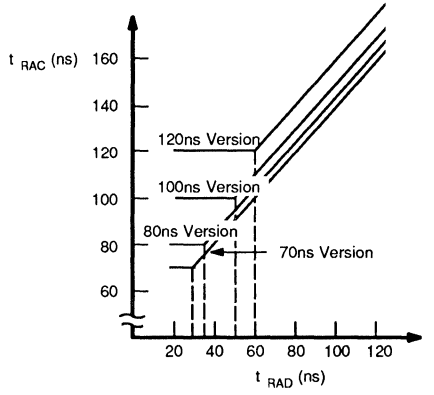


Fig. 3 – t_{RAC} vs. t_{RAD}



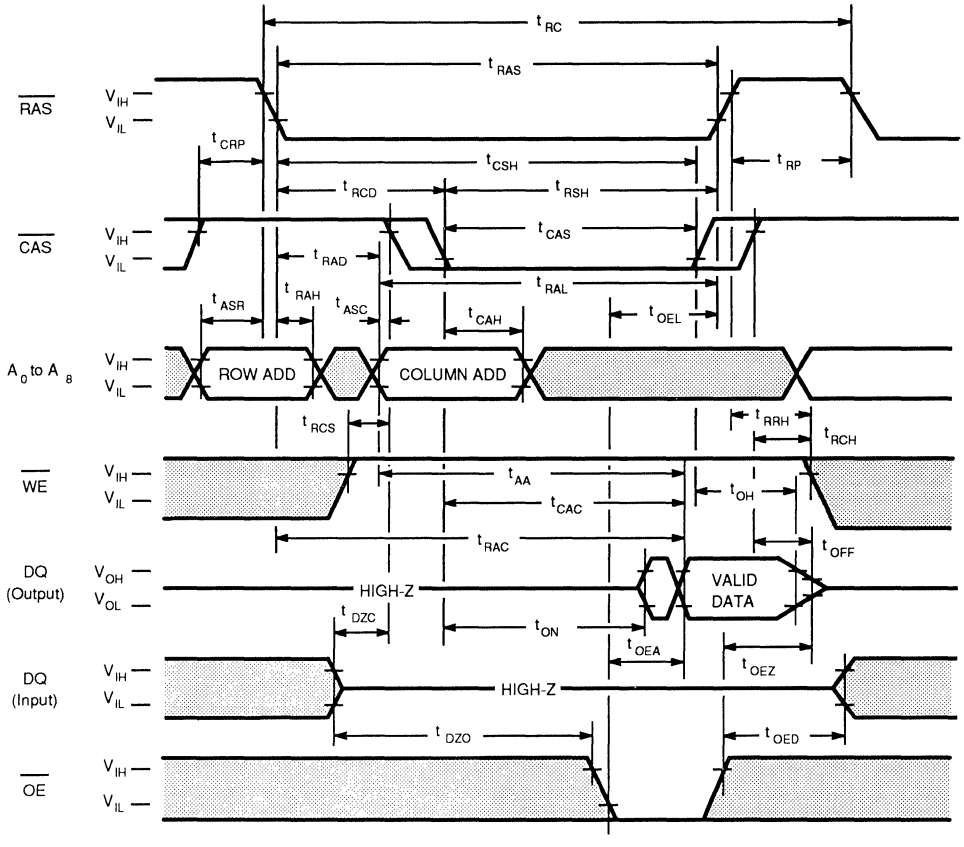
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	O *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	O *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	O *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High–Z	O	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh	H→L	L	X	L	—	—	—	Valid	O	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

TIMING DIAGRAMS

Fig. 4 – READ CYCLE



DESCRIPTION

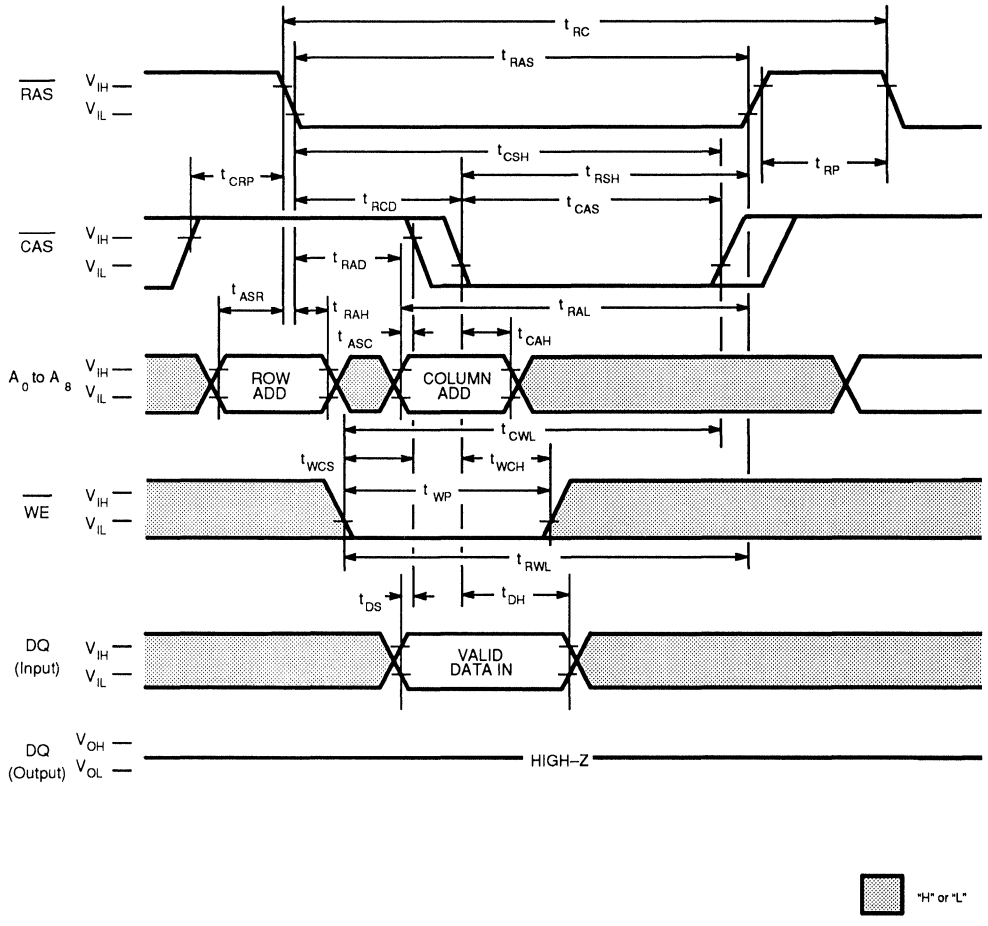
To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

2

Fig. 5 — EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")

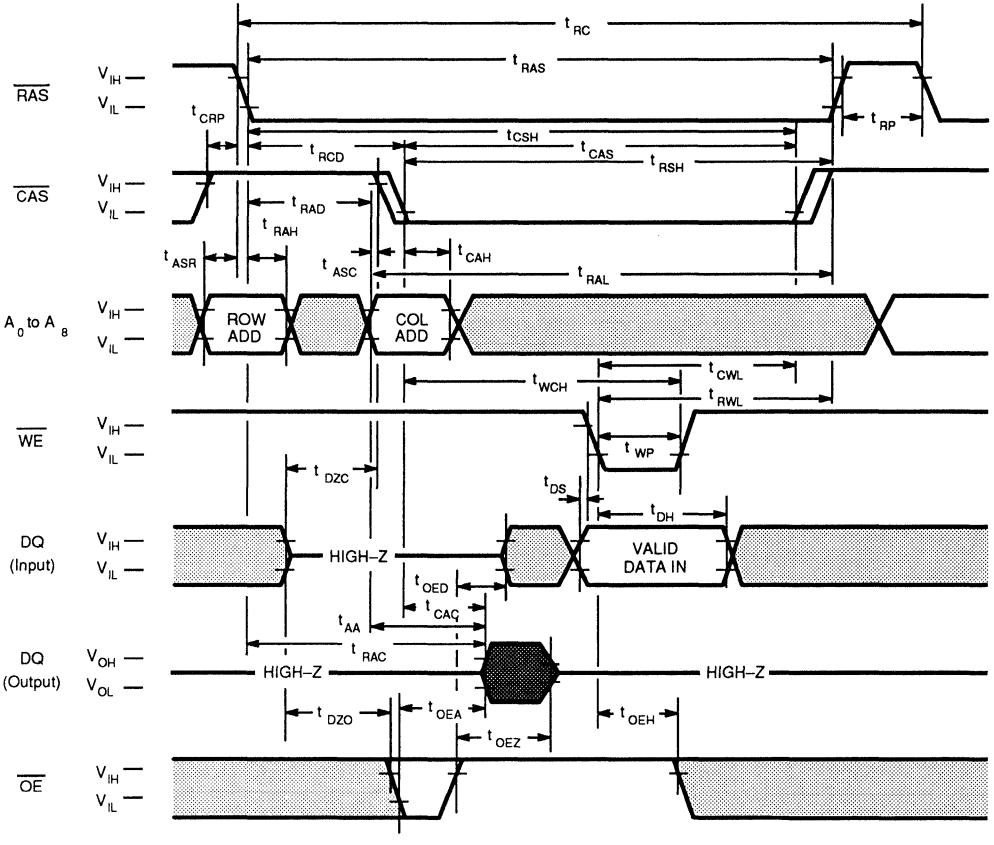


DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways — early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

2

Fig. 6 — $\overline{OE}$ (DELAYED WRITE CYCLE)

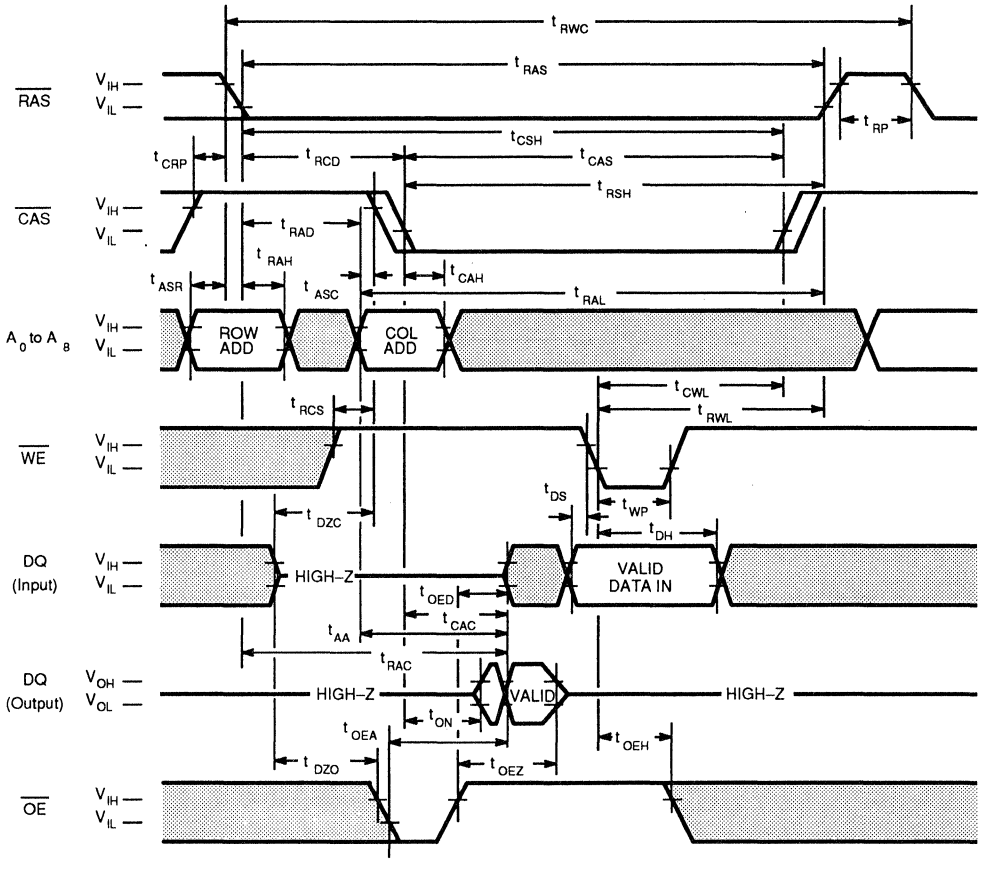


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_{DS}$).

2

Fig. 7 — READ–MODIFY–WRITE–CYCLE

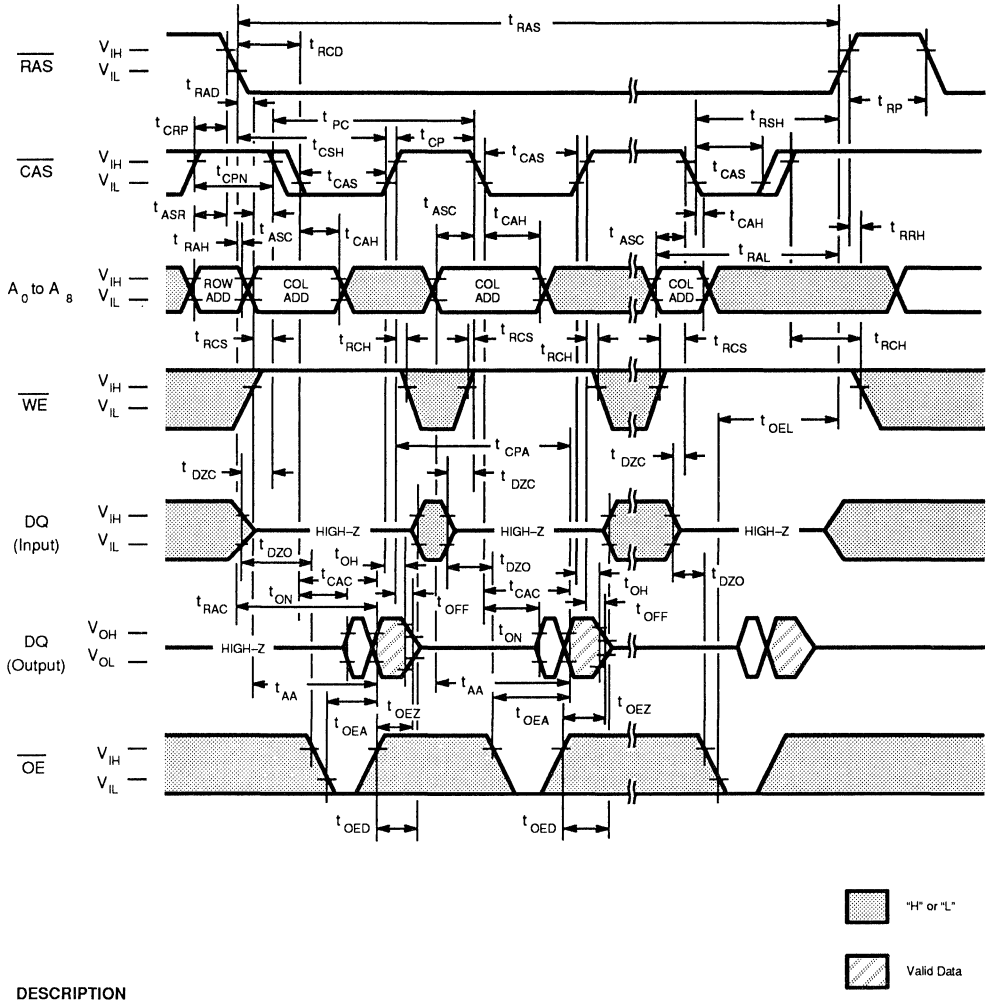


DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

2

Fig. 8 – FAST PAGE MODE READ CYCLE

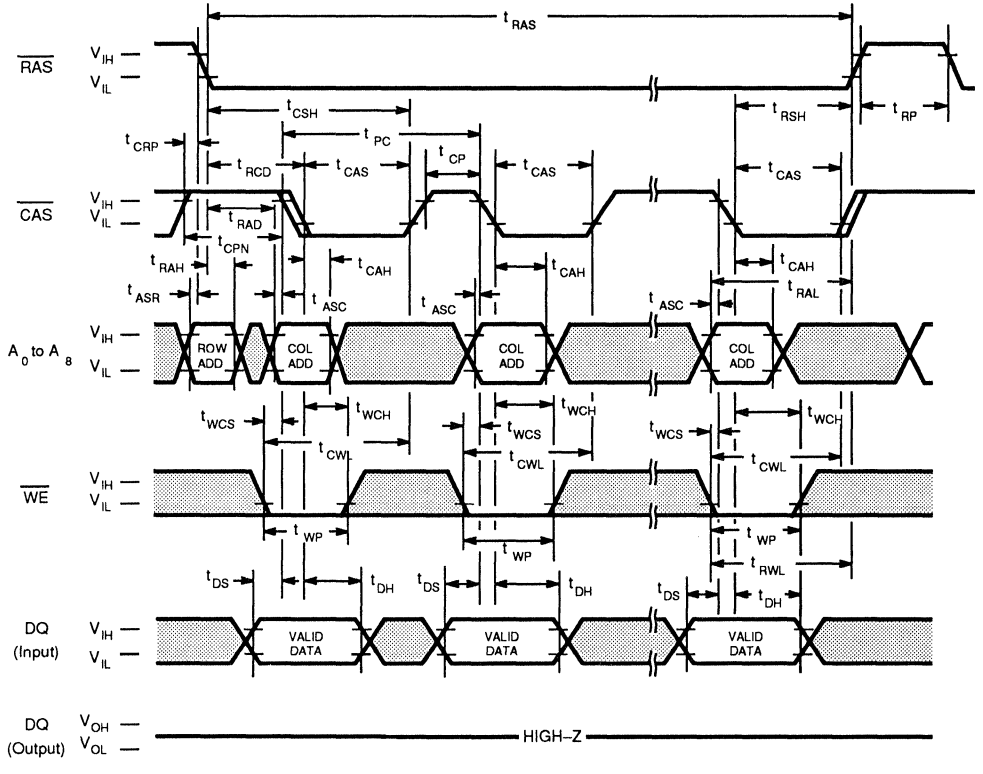


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occuring.

2

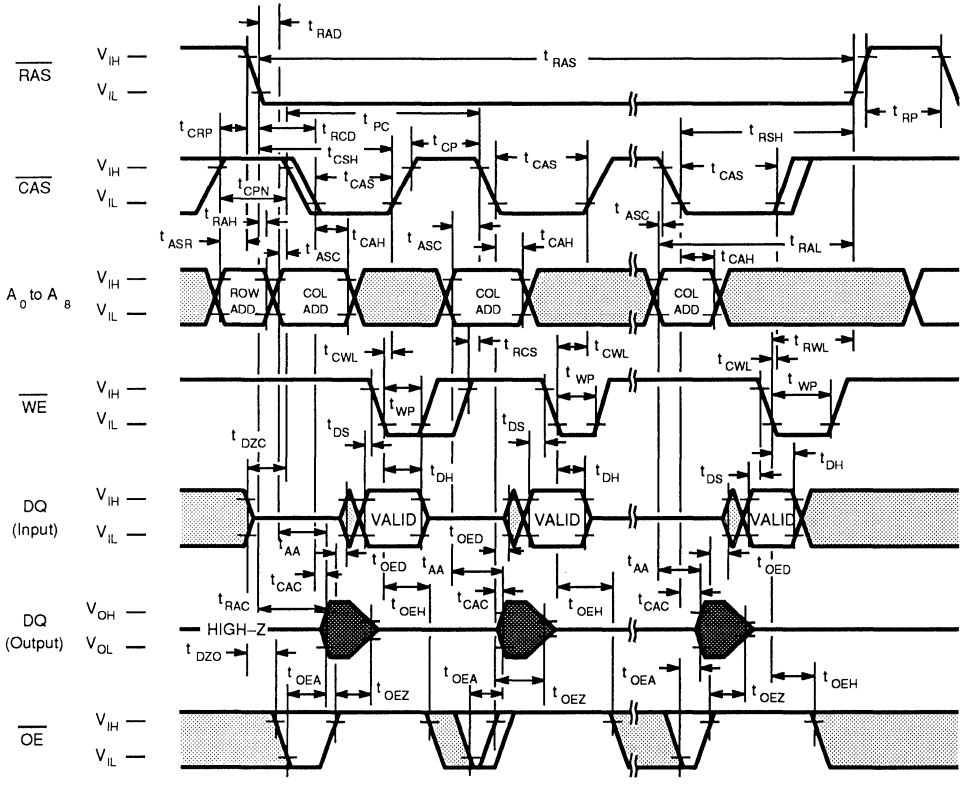
Fig. 9 — FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, t_{CWL} must be satisfied.

Fig. 10 — FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

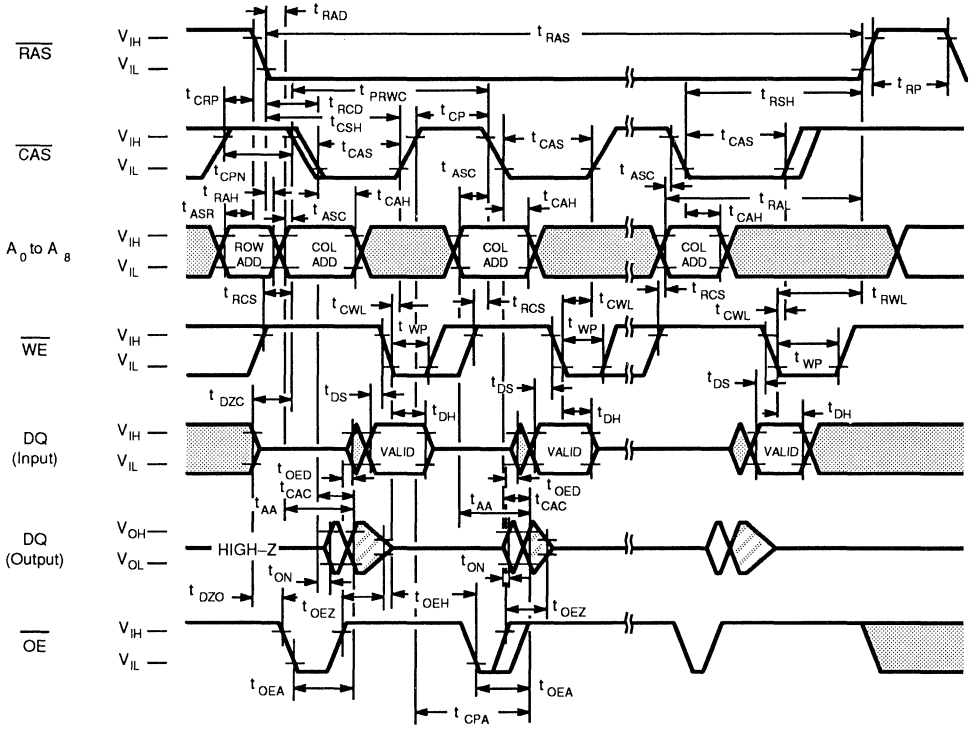


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_{DS}$).

2

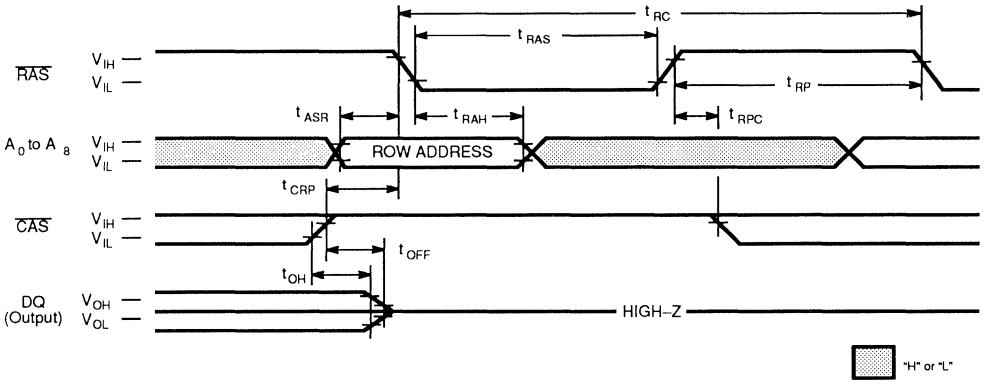
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 — $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

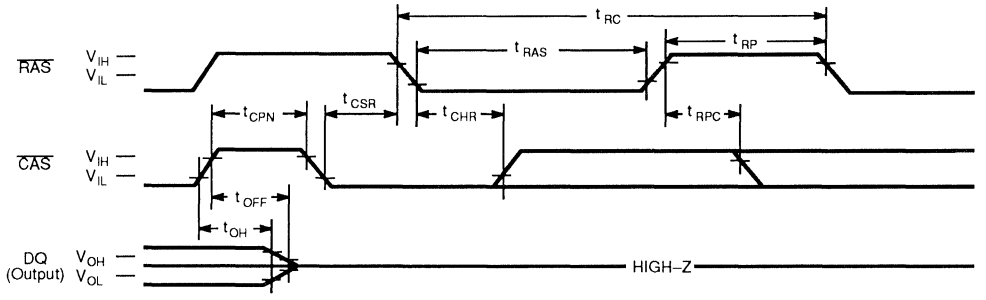


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read–modify–write cycle at each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available: $\overline{RAS}$–only refresh, $\overline{CAS}$–before–$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DQ pins are kept in a high–impedance state.

Fig. 13 — $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

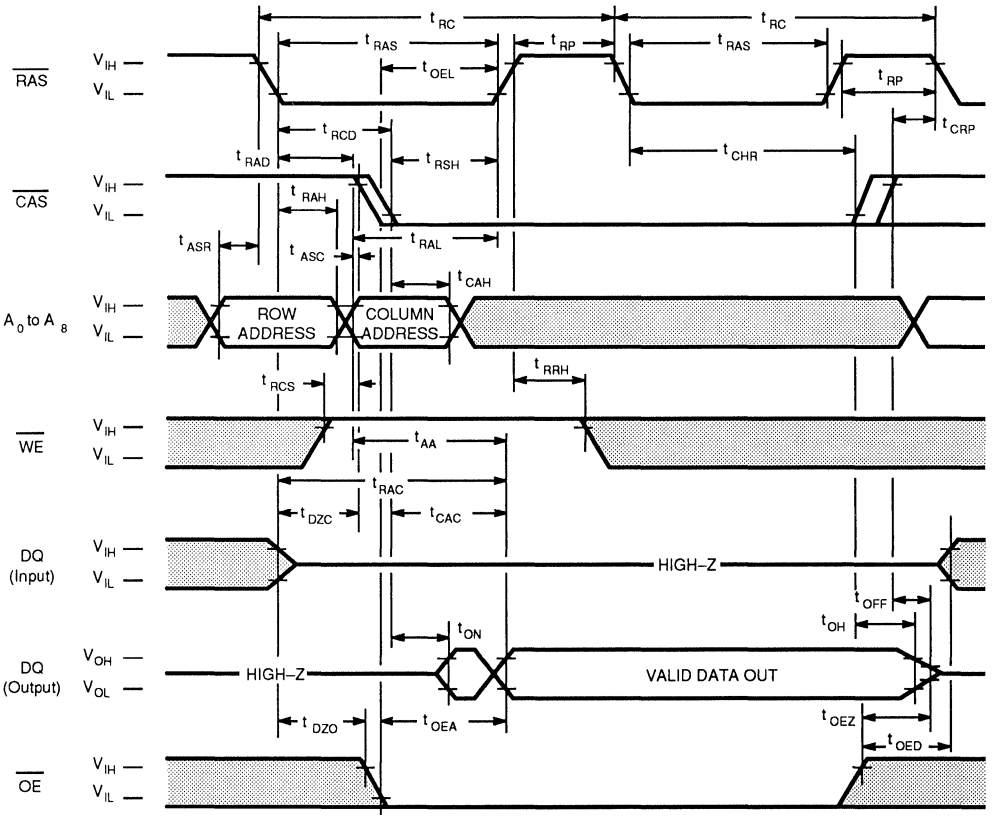


DESCRIPTION

$\overline{CAS}$–before–$\overline{RAS}$ refresh is an on–chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on–chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$ –before–$\overline{RAS}$ refresh operation.

2

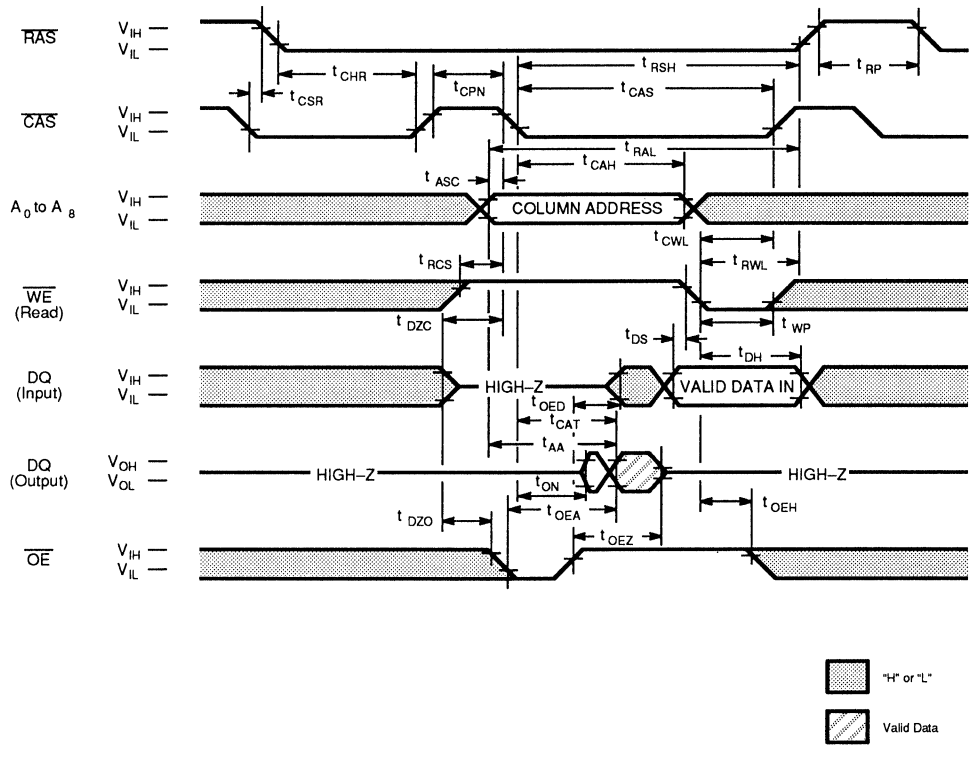
Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on–chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$–before–$\overline{RAS}$ refresh capability.

Fig. 15 — $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$–before–$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$–before–$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$–before–$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above, Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on–chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{CAS}$.

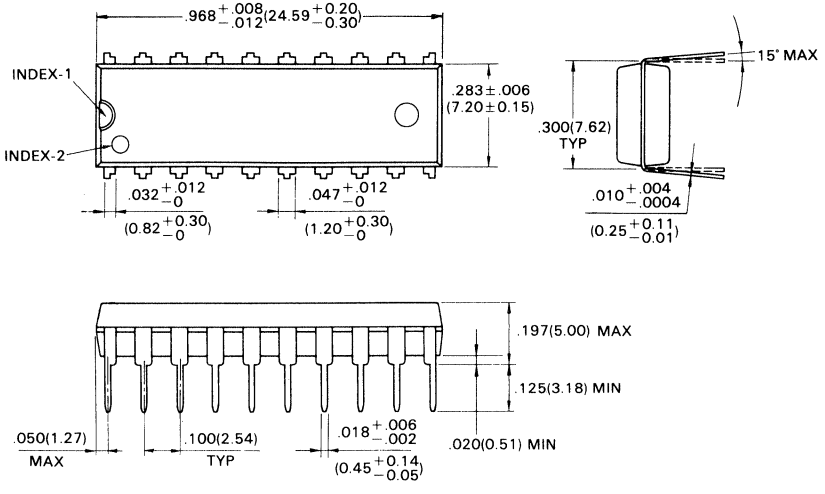
The $\overline{CAS}$–before–$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

- Initialize the internal refresh address counter by using eight $\overline{CAS}$–before–$\overline{RAS}$ refresh cycles.
- Use the same column address throughout the test.
- Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
- Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read–write cycles. Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
- Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
- Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix : –P)

20–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20P–M03)

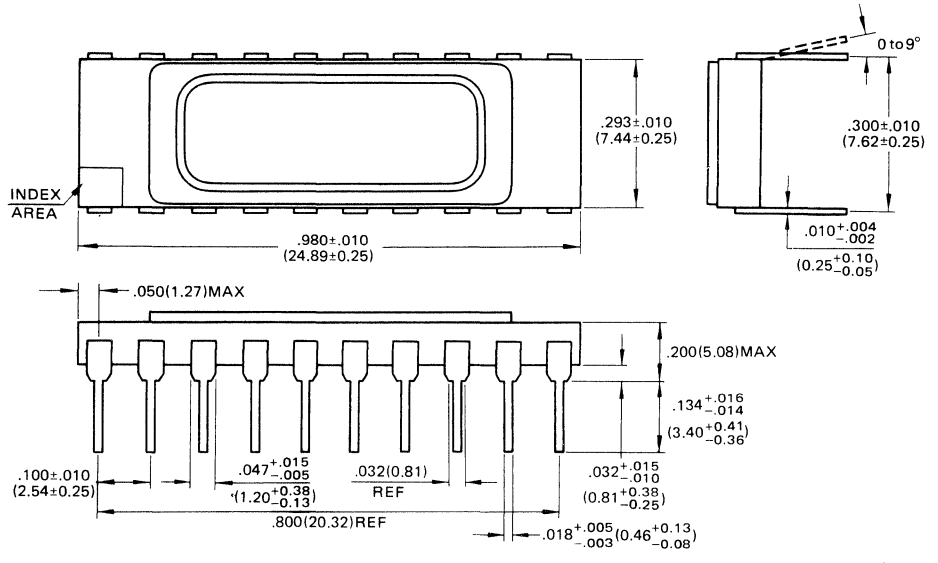


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)

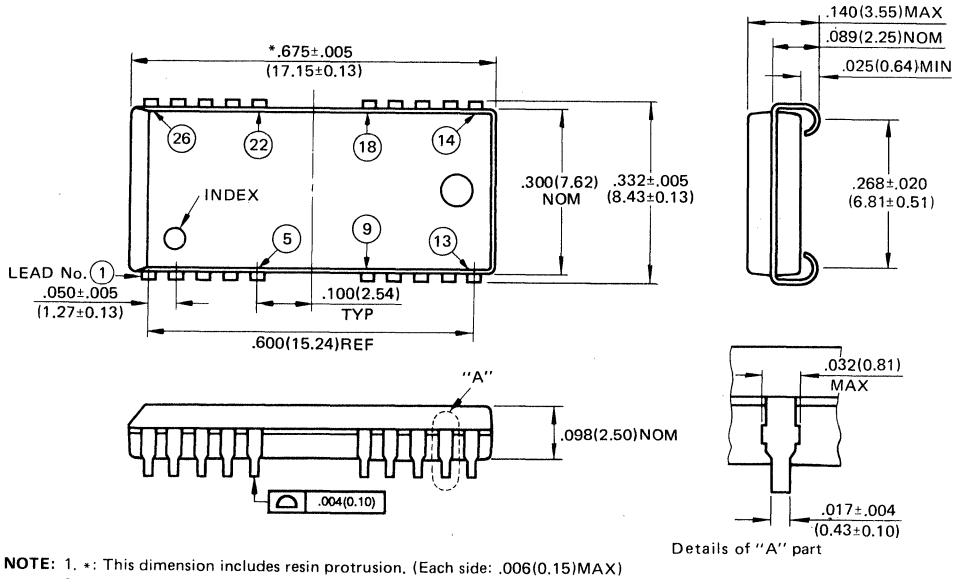


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)



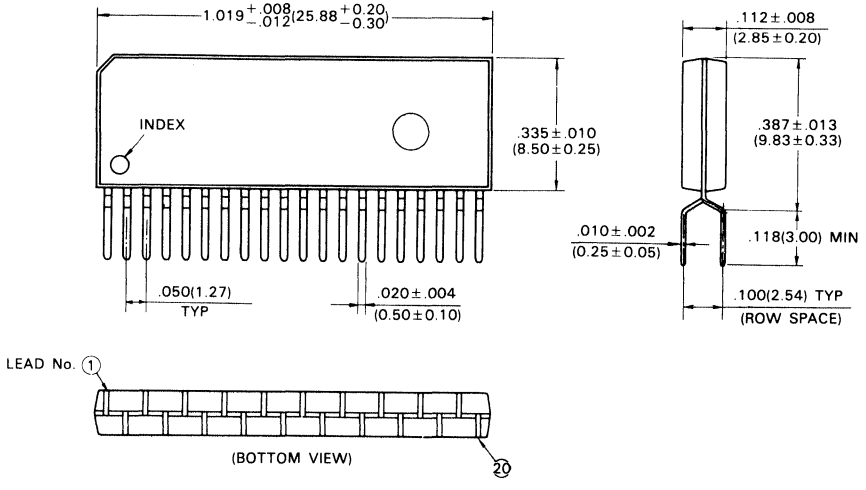
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



Dimensions in
inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C4256A-60/-80/-10

CMOS 1,048,576 BIT FAST PAGE MODE DYNAMIC RAM

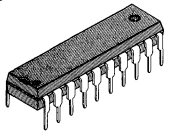
CMOS 262,144 x 4 BIT Fast Page Mode Dynamic RAM

The Fujitsu MB81C4256A is CMOS fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4256A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C4256A High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

ADVANCE INFO.

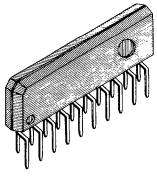


DIP-20P-M03

T.B.D

DIP-20C-XXX

LCC-26P-M04



ZIP-20P-M02

2

PRODUCT LINE & FEATURES

Parameter	MB81C4256A-60	MB81C4256A-80	MB81C4256A-10
$\overline{RAS}$ Access Time	60ns max.	80ns max.	100ns max.
Randam Cycle Time	130ns min.	155ns min.	180ns min.
Address Access Time	30ns max.	40ns max.	50ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	25ns max.
Fast Page Mode Cycle Time	45ns min.	55ns min.	65ns min.
Low Power Dissipation • Operating current • Standby current	330mW max.	275mW max.	248mW max.
	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

FUJITSU

CMOS 1,048,576 BIT NIBBLE MODE DYNAMIC RAM

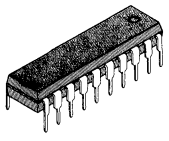
MB81C4257-85
MB81C4257-10
MB81C4257-12

February 1989
Edition 1.0

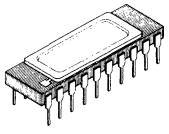
CMOS 262,144 x 4 BIT Nibble Mode Dynamic RAM

The Fujitsu MB81C4257 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 1,048,576 memory cells accessible in 4-bit increments. The MB81C4257 features a "Nibble" mode of operation whereby high-speed random access of up to 512-bits of data within the same row can be selected. The MB81C4257 DRAM is ideally suited for mainframes, buffers, hand-held computers, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81C4257 is only about one-fifth that of a conventional NMOS DRAM, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81C4257 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81C4257 are not critical and all inputs are TTL compatible.

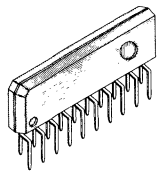


DIP-20P-M03



DIP-20C-A03

LCC-26P-M04



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C4257-85	MB81C4257-10	MB81C4257-12
Row Access Time	85ns max.	100ns max.	120ns max.
Random Cycle Time	160ns min.	180ns min.	210ns min.
Column Address Time	50ns max.	50ns max.	60ns max.
Column Access Time	25ns max.	30ns max.	35ns max.
Nibble Mode Cycle Time	60ns min.	60ns min.	70ns min.
Low Power Dissipation			
• Operating current	358mW max.	330mW max.	275mW max.
• Standby current	11mW max. (TTL level) /5.5mW max. (CMOS level)		

- 262,144 words x 4 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write or $\overline{OE}$ controlled write capacity
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Nibble Mode, Read-Modify-Write capacity
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

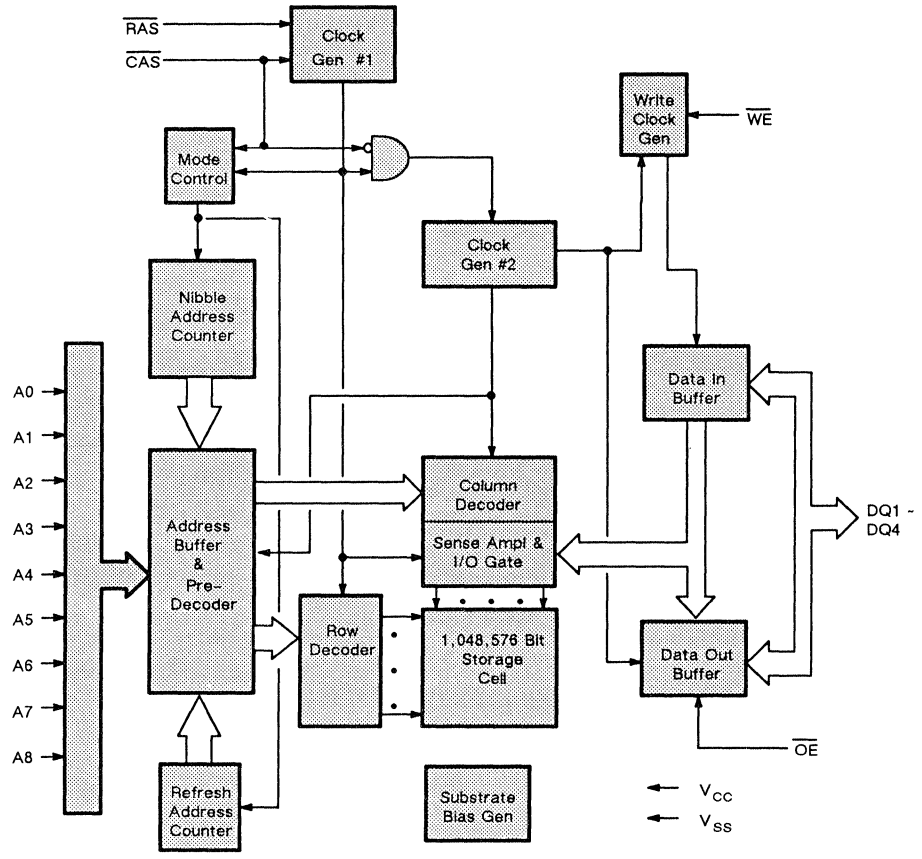
Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	-1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		--	50	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

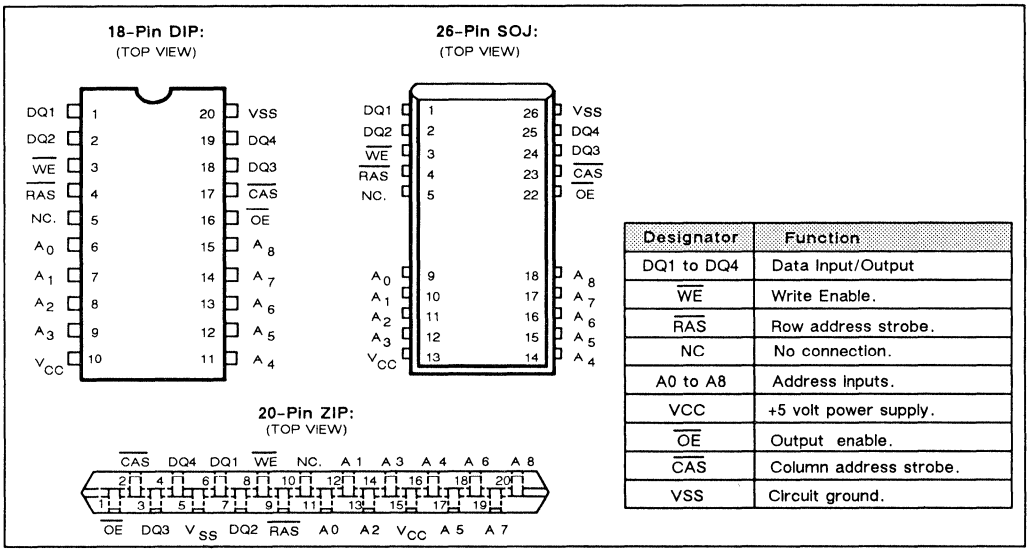
Fig. 1 – MB81C4257 DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A= 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ1 to DQ4	Data Input/Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

RECOMMENDED OPERATING CONDITIONS

(All voltages referenced to ground; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	VSS	0	0	0	
Input High Voltage, all inputs	VIH	2.4	—	6.5	V
Input Low Voltage, all inputs	VIL	-2.0	—	0.8	V
Input Low Voltage, DQ(Note)	VILD	-1.0	—	0.8	V

Note: Undershoots of up to -2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 4. First, nine row address bits are input on pins A0-through-A8 and latched with the row address strobe ($\overline{RAS}$); then nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways--an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ1-DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- **tRAC:** from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.
- **tCAC:** from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RAD} (max).
- **tAA:** from column address input when t_{RAD} is greater than t_{RAD} (max).
- **tOEA:** from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{CAA}.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

NIBBLE MODE OF OPERATION

In the nibble mode of operation, the user can serially access from one to four bits of data and perform high-speed read, write, or read-modify-write operations. During the nibble mode, the accessed bits of data are determined by row address zero (0) and column address one (1). For initial access, address bits CA0 and CA1 are used to select one of four nibble bits. After the first bit is accessed by this method, all remaining bits are accessed by simply toggling the column address strobe ($\overline{CAS}$) from High to Low. Each High-to-Low transition of $\overline{CAS}$ internally increments CA0 and CA1 and provides access to the next nibble bit.

If more than four bits are accessed during the nibble mode, the address sequence shown in Table 1 will repeat. AC parameters for each nibble mode of operation are shown in subsequent timing diagrams (Figures 9 through 12).

Table 1 - NIBBLE MODE ADDRESS SEQUENCE

Sequence	Nibble Bit	(A8 to A0) Row Address	CA0	(A8 to A2) Column Address	CA1	Remarks
$\overline{RAS}$/$\overline{CAS}$ (Normal mode)	1	101010101	0	1010101	0	Input address
Toggle $\overline{CAS}$ (Nibble mode)	2	101010101	1	1010101	0	Internally generated address
Toggle $\overline{CAS}$ (Nibble mode)	3	101010101	0	1010101	1	
Toggle $\overline{CAS}$ (Nibble mode)	4	101010101	1	1010101	1	
Toggle $\overline{CAS}$ (Nibble mode)	1	101010101	0	1010101	0	Sequence repeats

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Output High Voltage		V_{OH}	I_{OH} = -5 mA	2.4	—	—	V
Output Low Voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input Leakage Current (Any Input)		$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V; 4.5 V ≤ V_{CC} ≤ 5.5 V; V_{SS} = 0 V; All other pins not under test = 0V	-10	—	10	µA
Output Leakage Current		$I_{DQ(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V; Data out disabled	-10	—	10	µA
Operating Current (Average Power Supply Current)	MB81C4257-85	I_{CC1} (Note)	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	65	mA
	MB81C4257-10					60	
	MB81C4257-12					50	
Standby Current (Power Supply Current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} -0.2 V			1.0	
Refresh Current #1 (Average Power Supply Current)	MB81C4257-85	I_{CC3} (Note)	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	60	mA
	MB81C4257-10					55	
	MB81C4257-12					45	
Nibble Mode Current	MB81C4257-85	I_{CC4} (Note)	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling t_{NC} = min	—	—	40	mA
	MB81C4257-10					40	
	MB81C4257-12					33	
Refresh Current #2 (Average Power Supply Current)	MB81C4257-85	I_{CC5} (Note)	$\overline{RAS}$ cycling $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	60	mA
	MB81C4257-10					55	
	MB81C4257-12					45	

Note: I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open. I_{CC} depends on the input low voltage level VIL, VIL>-0.5V.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4257-85		MB81C4257-10		MB81C4257-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
1	Time Between Refresh	t_{REF}	—	8.2	—	8.2	—	8.2	ms	—
2	Random Read/Write Cycle Time	t_{RC}	160	—	180	—	210	—	ns	—
3	Read-Modify-Write Cycle Time	t_{RWC}	220	—	240	—	275	—	ns	—
4	Access Time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	4,7
5	Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	35	ns	5,7
6	Access Time from Column Address	t_{AA}	—	50	—	50	—	60	ns	6,7
7	Output Hold Time	t_{OH}	7	—	7	—	7	—	ns	—
8	Output Buffer Turn On Delay Time	t_{ON}	5	—	5	—	5	—	ns	—
9	Output Buffer Turn off Delay Time	t_{OFF}	—	25	—	25	—	25	ns	8
10	Transition Time	t_T	3	50	3	50	3	50	ns	—
11	$\overline{RAS}$ Precharge Time	t_{RP}	65	—	70	—	80	—	ns	—
12	$\overline{RAS}$ Pulse Width	t_{RAS}	85	100000	100	100000	120	100000	ns	—
13	$\overline{RAS}$ Hold Time	t_{RSH}	25	—	30	—	35	—	ns	—
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0	—	0	—	0	—	ns	—
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	60	25	70	25	85	ns	9,10
16	$\overline{CAS}$ Pulse Width	t_{CAS}	25	—	30	—	35	—	ns	—
17	$\overline{CAS}$ Hold Time	t_{CSH}	85	—	100	—	120	—	ns	—
18	$\overline{CAS}$ Precharge Time (Normal)	t_{CPN}	15	—	15	—	15	—	ns	17
19	Row Address Set Up Time	t_{ASR}	0	—	0	—	0	—	ns	—
20	Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	—
21	Column Address Set Up Time	t_{ASC}	0	—	0	—	0	—	ns	—
22	Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	ns	—
23	$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	35	20	50	20	60	ns	11
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	45	—	50	—	60	—	ns	—
25	Read Command Set Up Time	t_{RCS}	0	—	0	—	0	—	ns	—
26	Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	12
27	Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	12
28	Write Command Set Up Time	t_{WCS}	0	—	0	—	0	—	ns	15
29	Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	ns	—
30	$\overline{WE}$ Pulse Width	t_{WP}	15	—	15	—	20	—	ns	—
31	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	25	—	25	—	30	—	ns	—
32	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	ns	—
33	DIN set Up Time	t_{DS}	0	—	0	—	0	—	ns	—
34	DIN Hold Time	t_{DH}	15	—	15	—	20	—	ns	—

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB81C4257-85		MB81C4257-10		MB81C4257-12		Unit	Note
			Min	Max	Min	Max	Min	Max		
35	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	t_{RPC}	0	—	0	—	0	—	ns	—
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before $\overline{RAS}$ Refresh	t_{CSR}	0	—	0	—	0	—	ns	—
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before $\overline{RAS}$ Refresh	t_{CHR}	15	—	15	—	20	—	ns	—
38	Access Time from $\overline{OE}$	t_{OEA}	—	22	—	25		30	ns	7
39	Output Buffer Turn Off Delay from $\overline{OE}$	t_{OEZ}	—	25	—	25	—	25	ns	8
40	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data	t_{OEL}	10	—	10	—	10	—	ns	—
41	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	t_{OEH}	0	—	0	—	0	—	ns	13
42	$\overline{OE}$ to Data In Delay Time	t_{OED}	25	—	25	—	25	—	ns	
43	DIN to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	14
44	DIN to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	14
45	Access Time from $\overline{CAS}$ (Counter Test Cycle)	t_{CAT}	—	50	—	50	—	60	ns	—
50	Nibble Mode Read/Write Cycle Time	t_{NC}	60	—	60	—	70	—	ns	—
51	Nibble Mode Read-Modify-Write Cycle Time	t_{NRWC}	115	—	115	—	130	—	ns	—
52	Access Time from Nibble Mode $\overline{CAS}$ Precharge	t_{NPA}	—	60	—	60	—	70	ns	7.16
53	Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	15	—	15	—	15	—	ns	—

Notes:

1. An Initial pause ($\overline{RAS}$=$\overline{CAS}$=VIH) of 200μs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max). If $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min)
11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. Assumes that $t_{WCS} < t_{WCS}$ (min)
14. Either t_{DZC} or t_{DZO} must be satisfied.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. t_{NPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{NCP} is shortened, t_{CAC} is longer than t_{CAC} (max).
17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

2

Fig. 2 - t_{RAC} vs. t_{RCD}

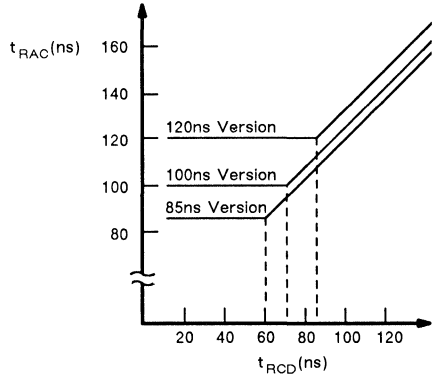
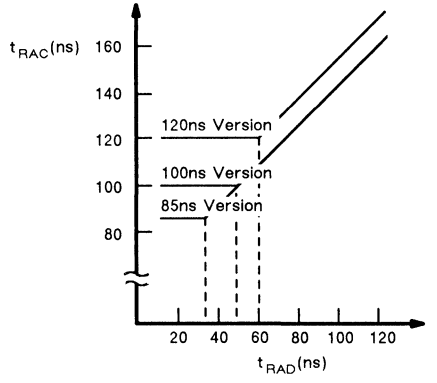


Fig. 3 - t_{RAC} vs. t_{RAD}



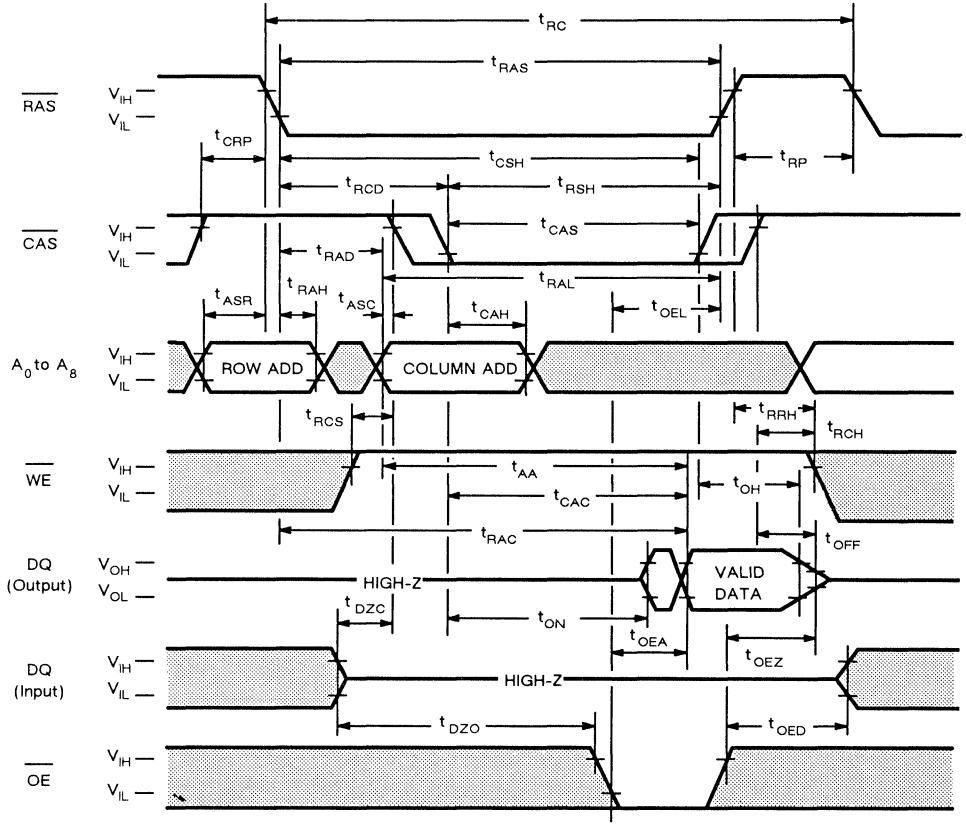
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	○ *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	○ *	$t_{WCS} \geq t_{WCS}$ (min)
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	○ *	
$\overline{RAS}$-only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	○	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High-Z	○	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H→L	L	X	L	—	—	—	Valid	○	Previous data is kept.

X; "H" or "L"
*; It is impossible in Nibble Mode

TIMING DIAGRAMS

Fig. 4 – READ CYCLE



"H" or "L"

DESCRIPTION

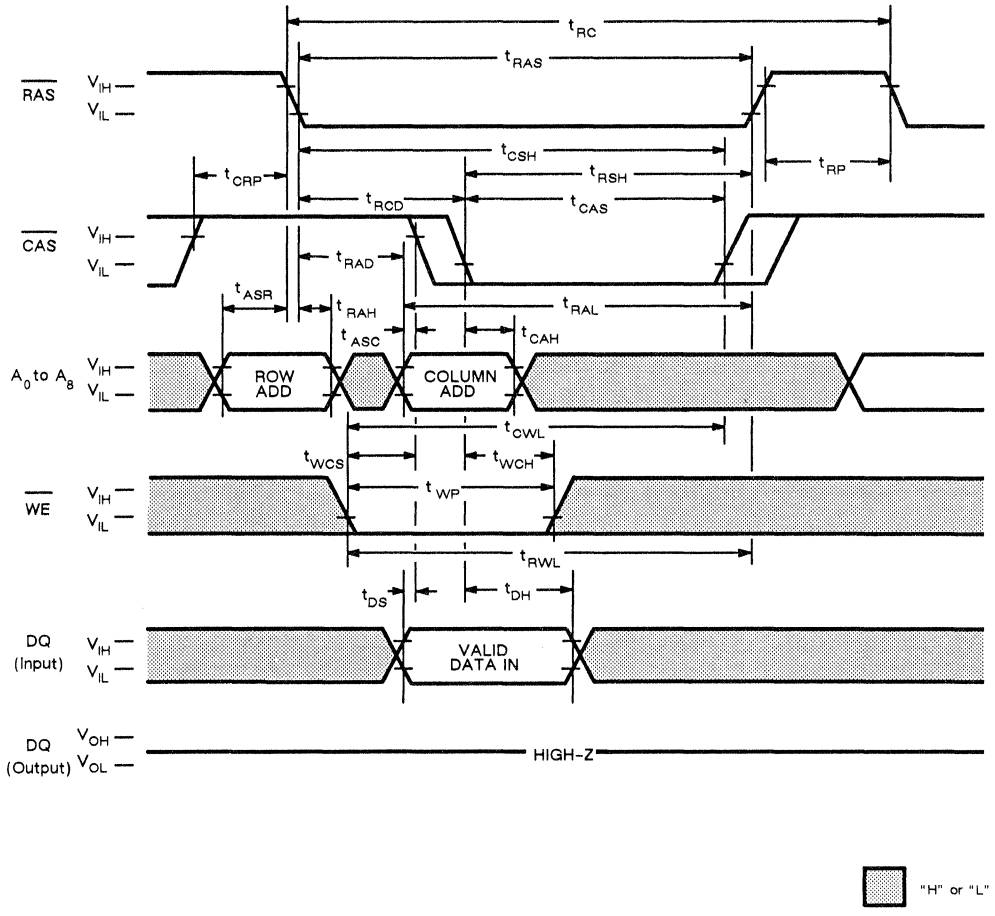
To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC} t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

2

Fig. 5 — EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")

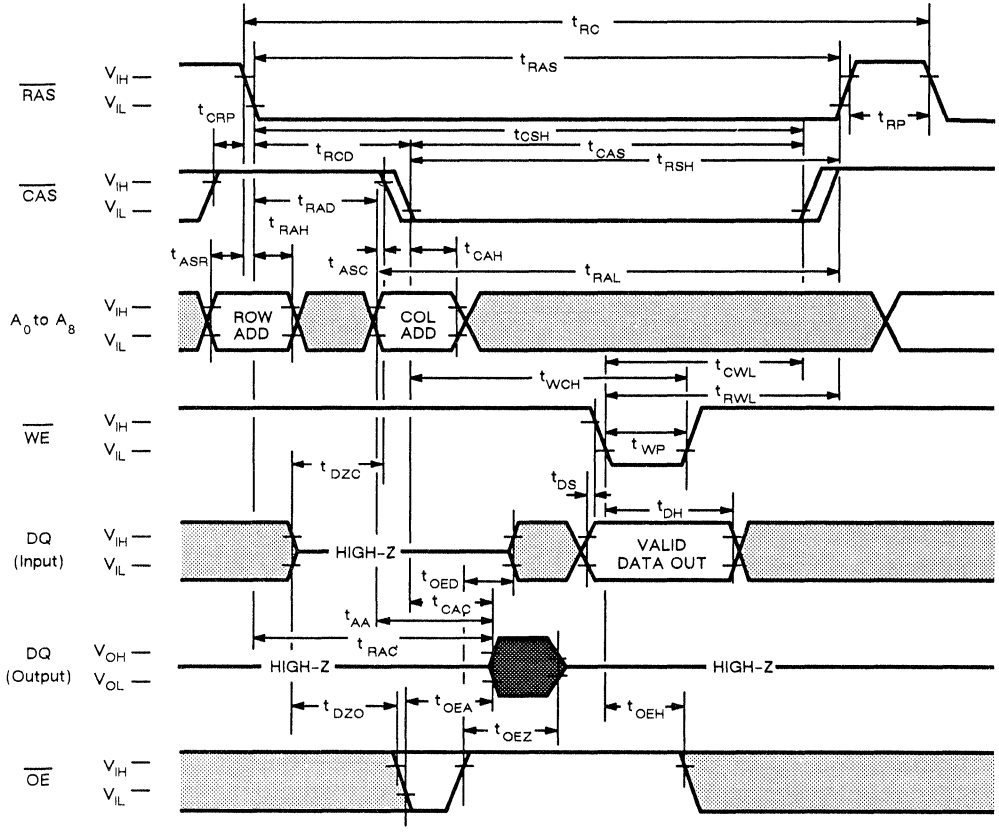


DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways — early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

2

Fig. 6 — $\overline{OE}$ (DELAYED WRITE CYCLE)

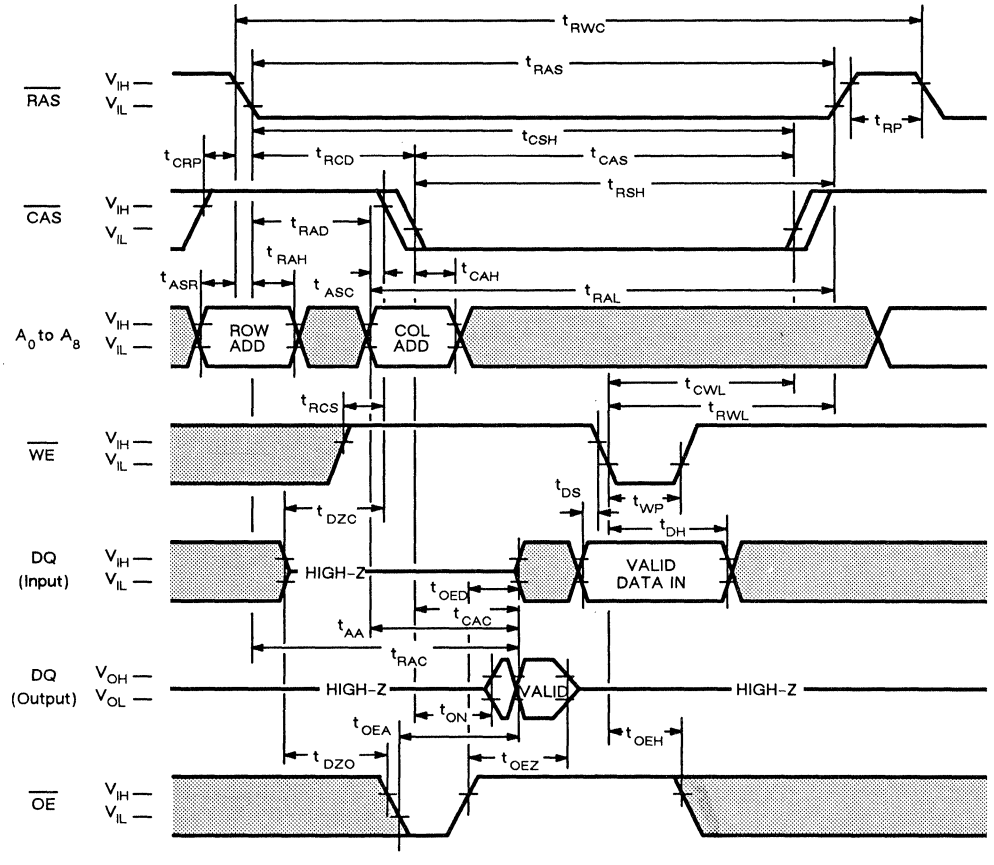


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_{DS}$).

2

Fig. 7 — READ-MODIFY-WRITE-CYCLE



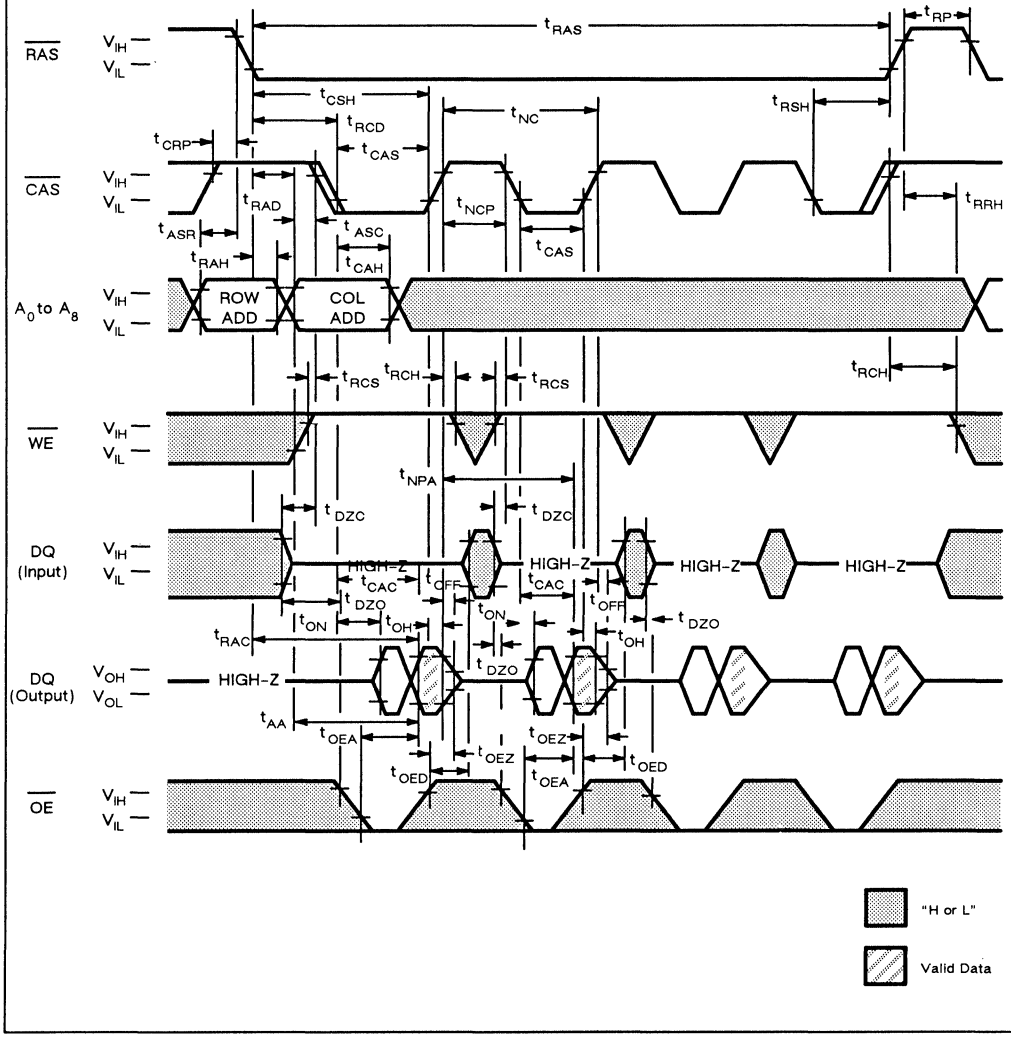
"H" or "L"

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

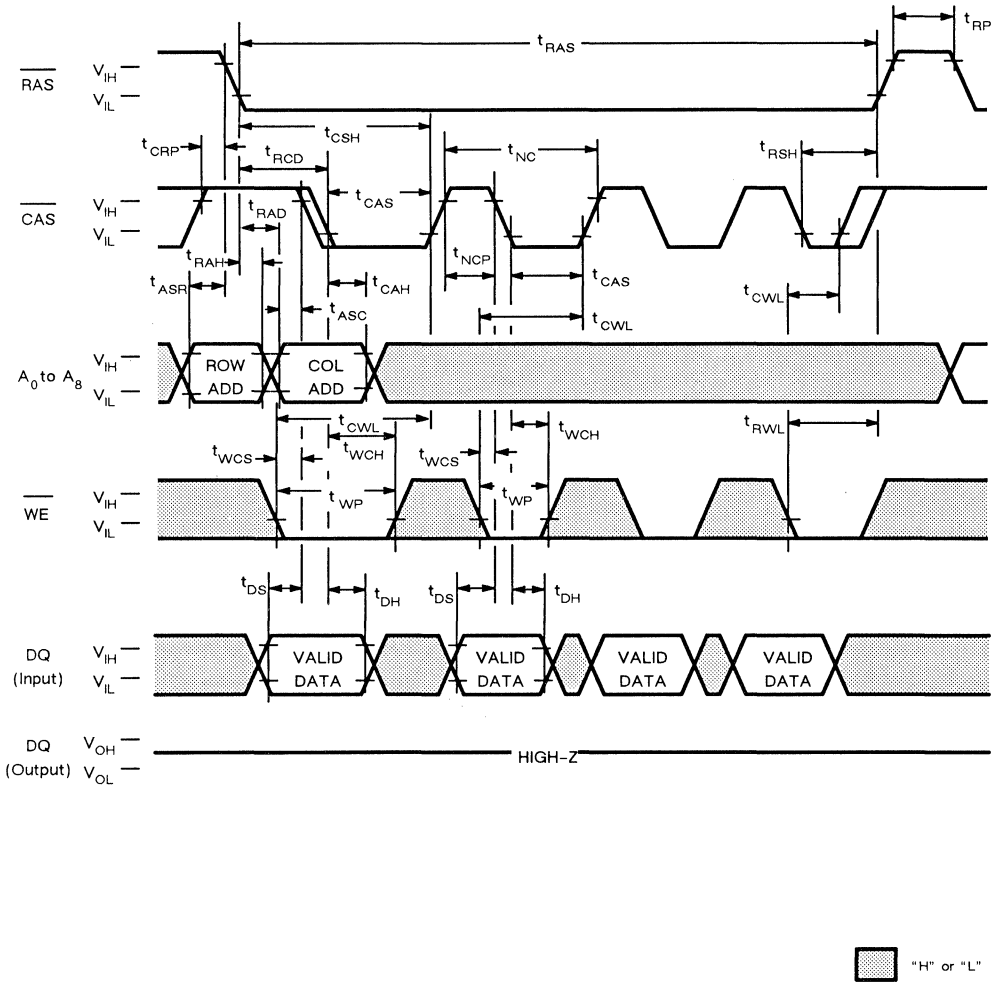
2

Fig. 9 - NIBBLE MODE READ CYCLE



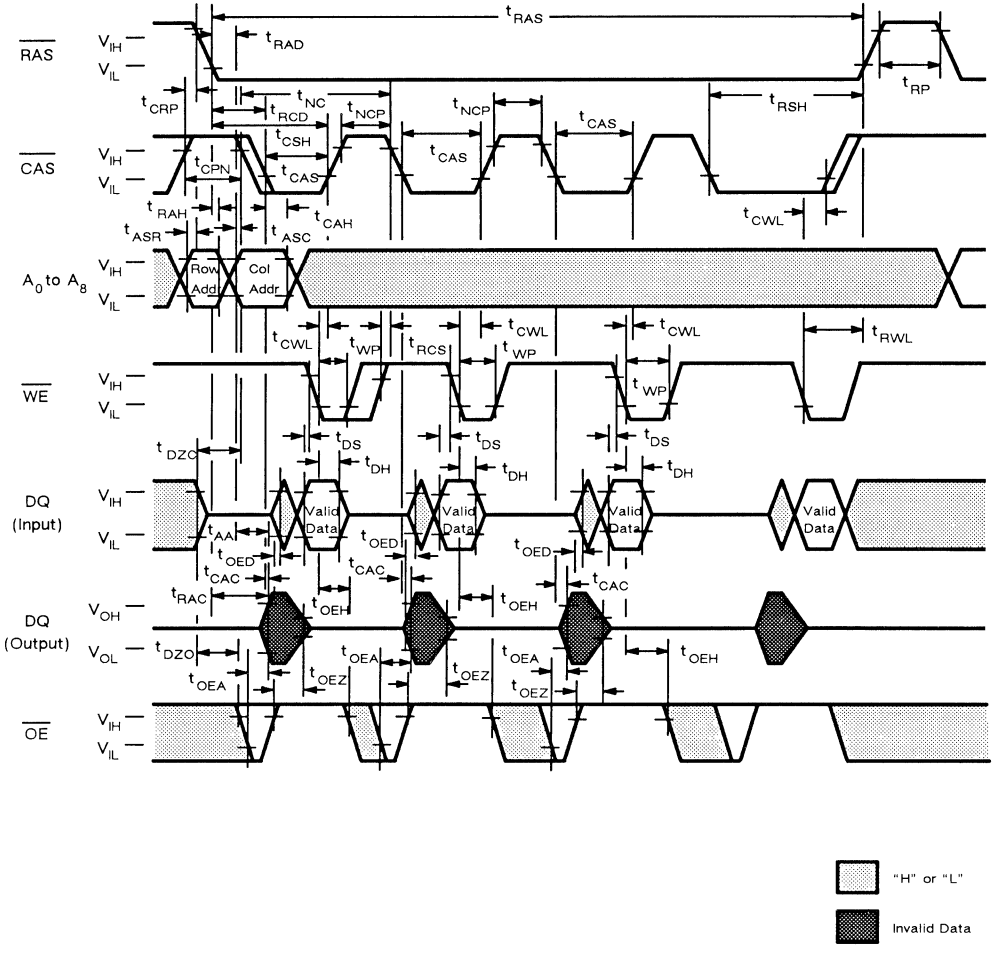
2

Fig. 10 - NIBBLE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



2

Fig. 11 – NIBBLE MODE $\overline{OE}$ (DELAYED) WRITE CYCLE



2

Fig. 12 - NIBBLE MODE READ-MODIFY-WRITE CYCLE

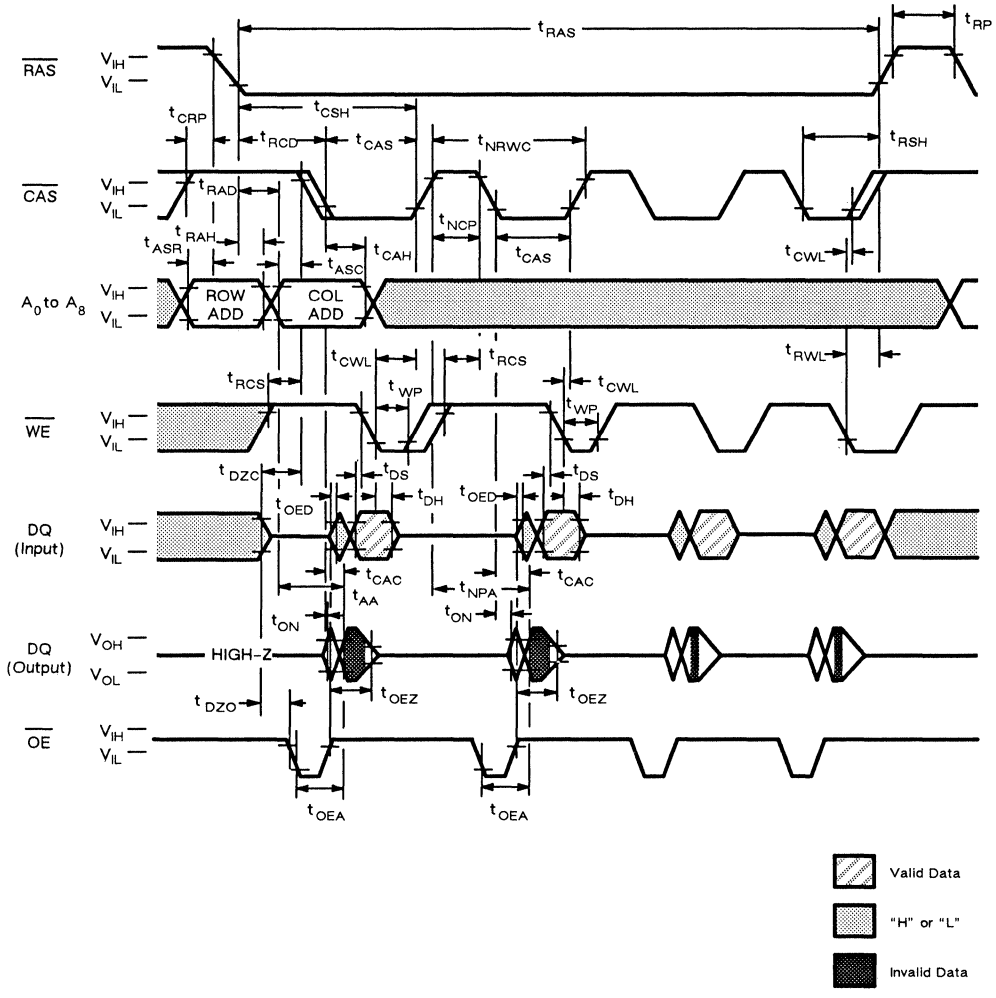
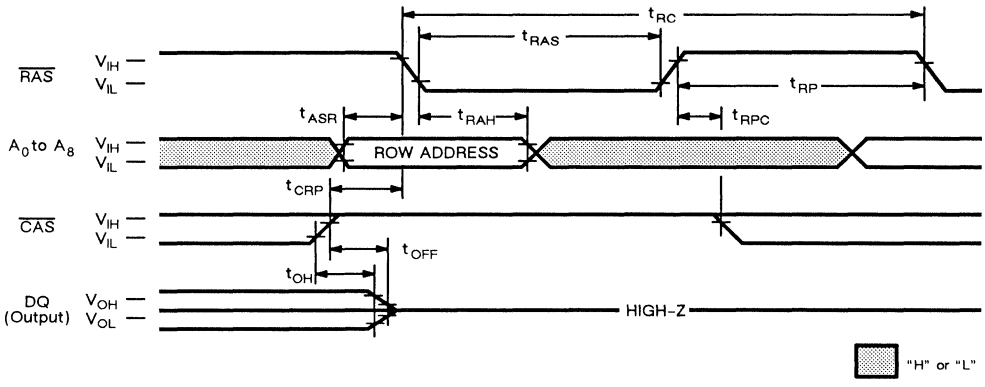


Fig. 12 — $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

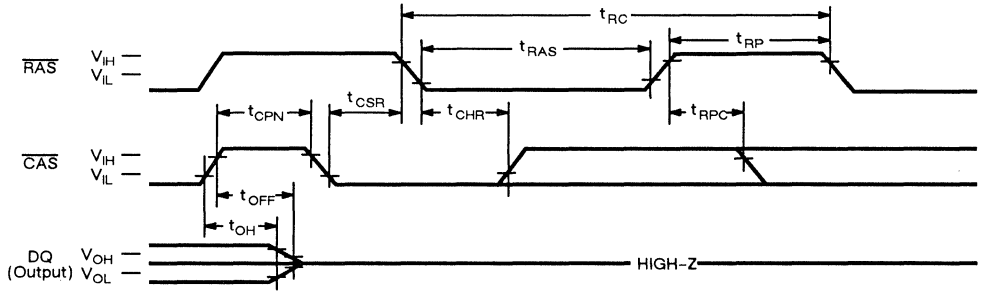


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

Fig. 13 — $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

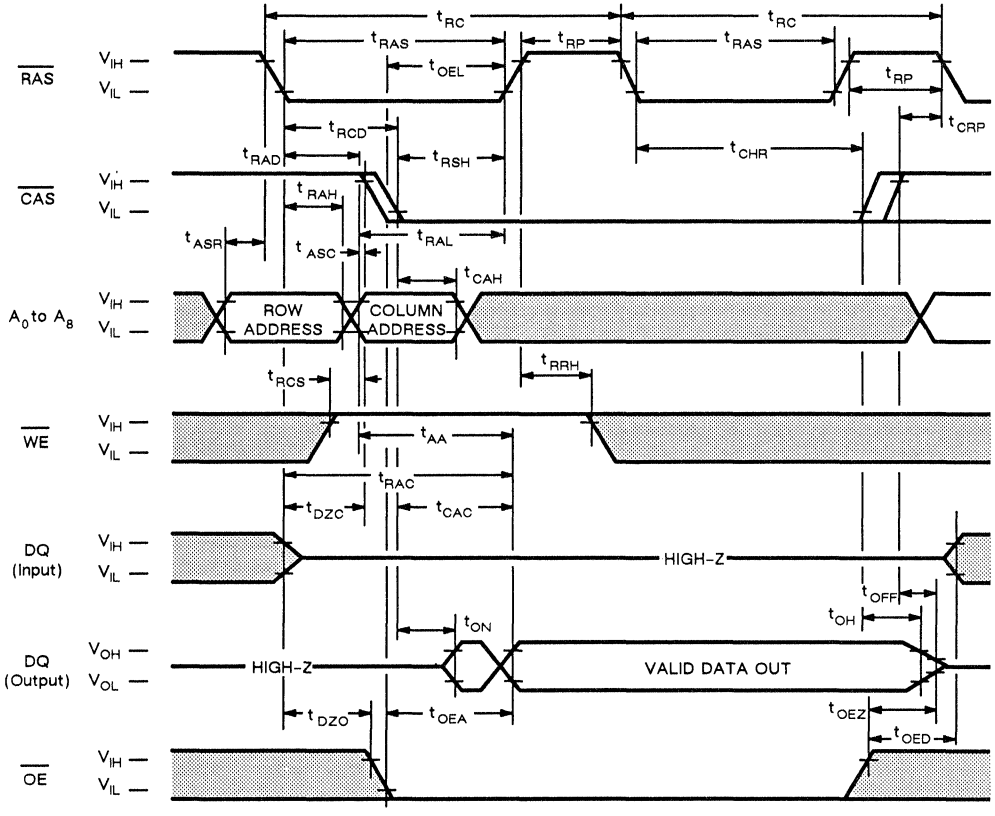


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

Fig. 14 - HIDDEN REFRESH CYCLE

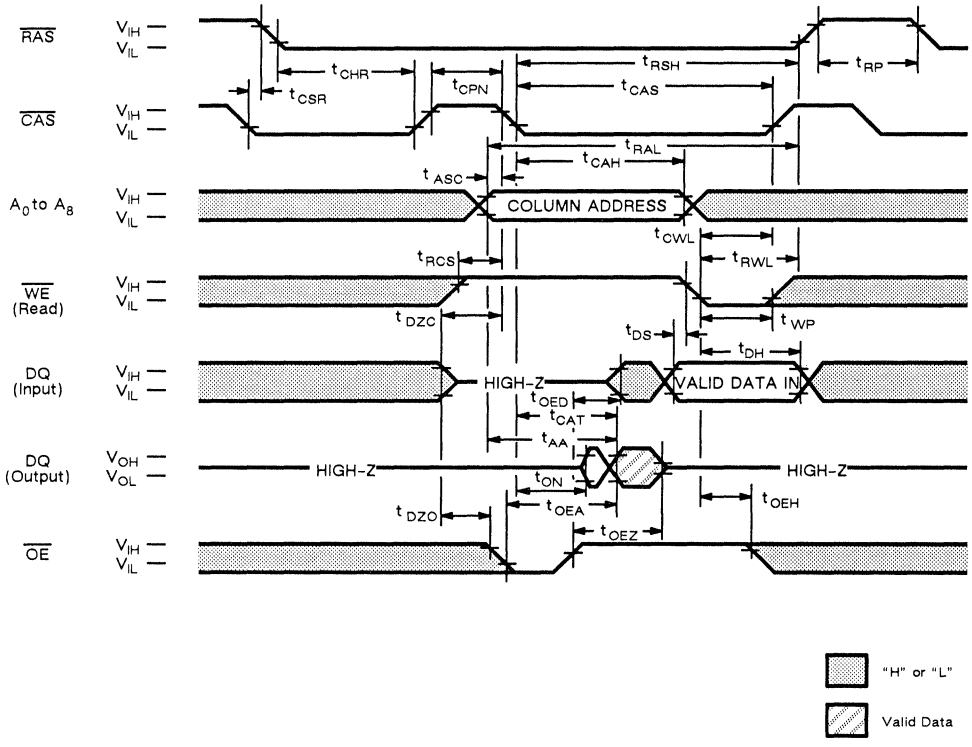


DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$ -before- $\overline{RAS}$ refresh capability.

2

Fig. 15 — $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above, Row and column addresses are defined as follows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0-A8 at the second falling edge of $\overline{CAS}$.

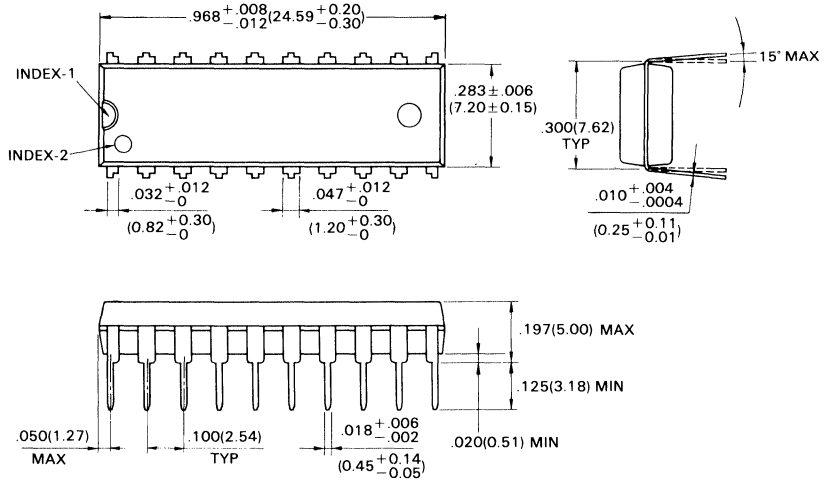
The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

- Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
- Use the same column address throughout the test.
- Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
- Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
- Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
- Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix : -P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M03)

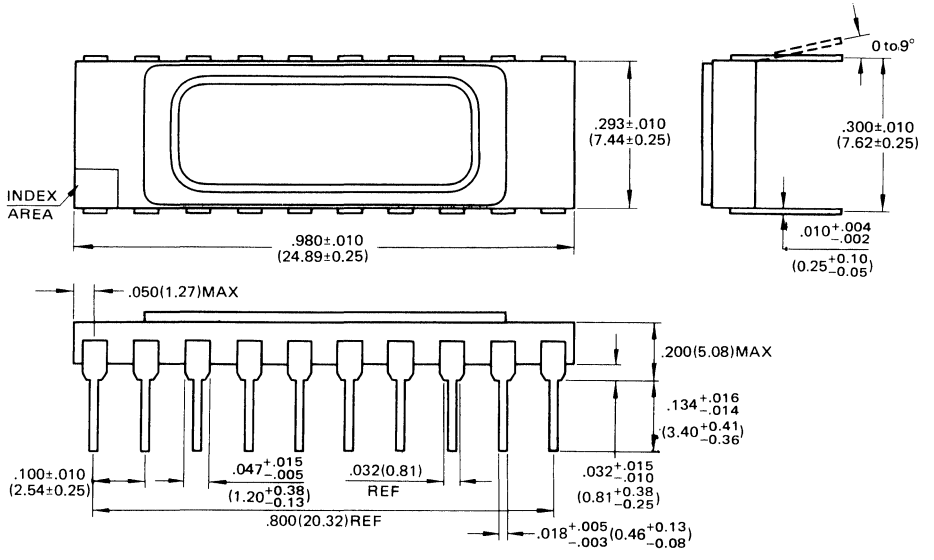


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : -C)

20-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-A03)

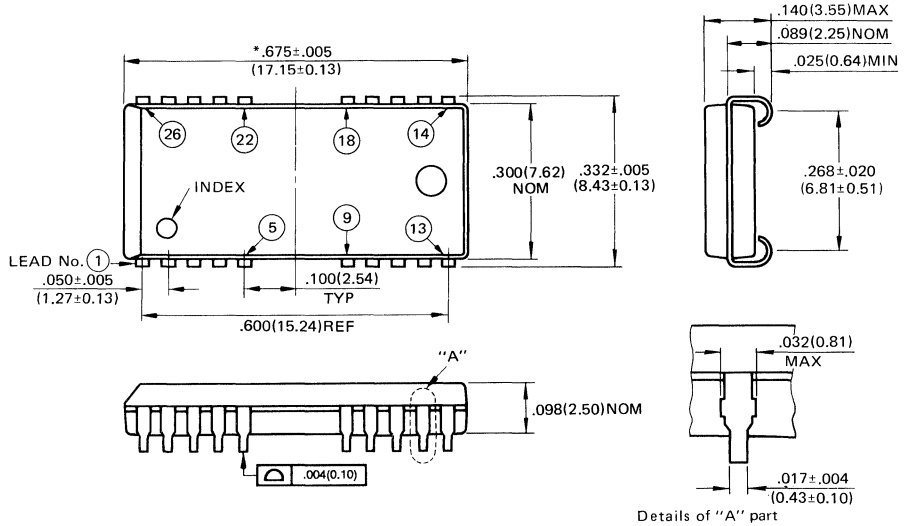


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : -PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER
(CASE No.: LCC-26P-M04)



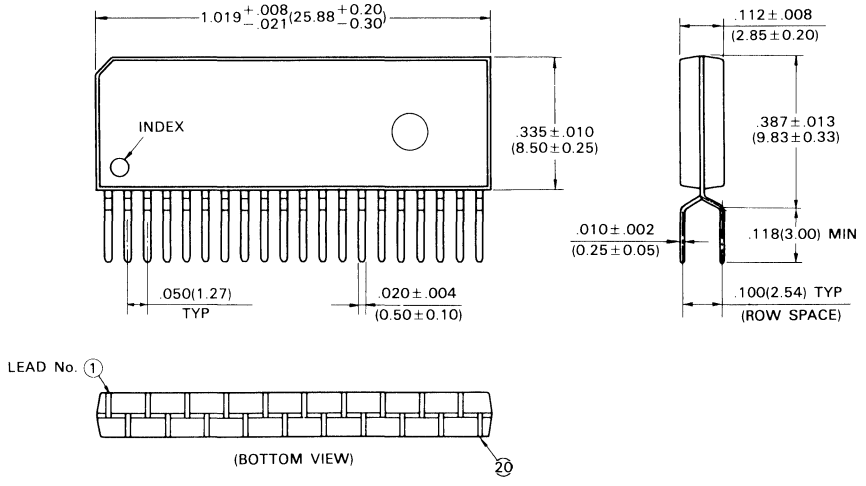
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : -PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(CASE No.: ZIP-20P-M02)



Dimensions in
inches (millimeters)

2

November 1989
Edition 1.1

FUJITSU

DATA SHEET

MB81C4258-70/-80/-10/-12

CMOS 1,048,576 BIT STATIC COLUMN MODE DYNAMIC RAM

CMOS 262,144 x 4 BIT Static Column Mode Dynamic RAM

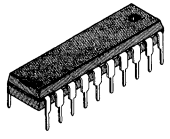
PRELIMINARY

The Fujitsu MB81C4258 is CMOS fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4258 has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

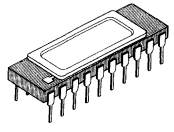
Fujitsu's advanced three-dimensional stacked capacitor cell technologymakes the MB81C4258 High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

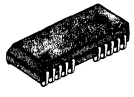
The specification is applied to "BC" version revised with intent to realized faster access time.So faster speed version (70ns and 80ns) are available on this chip.



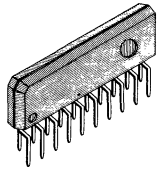
DIP-20P-M03



DIP-20C-A03



LCC-26P-M04



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB81C4258 -70	MB81C4258 -80	MB81C4258 -10	MB81C4258 -12
$\overline{RAS}$ Access Time	70ns max.	80ns max.	100ns max.	120ns max.
Random Cycle Time	140ns min.	155ns min.	180ns min.	210ns min.
Address Access Time	43ns max.	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	25ns max.	25ns max.	35ns max.
Static Column Mode Cycle Time	48ns min.	50ns min.	55ns min.	65ns min.
Low Power Dissipation	413mW max.	385mW max.	330mW max.	275mW max.
• Operating current • Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)			

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static Column Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

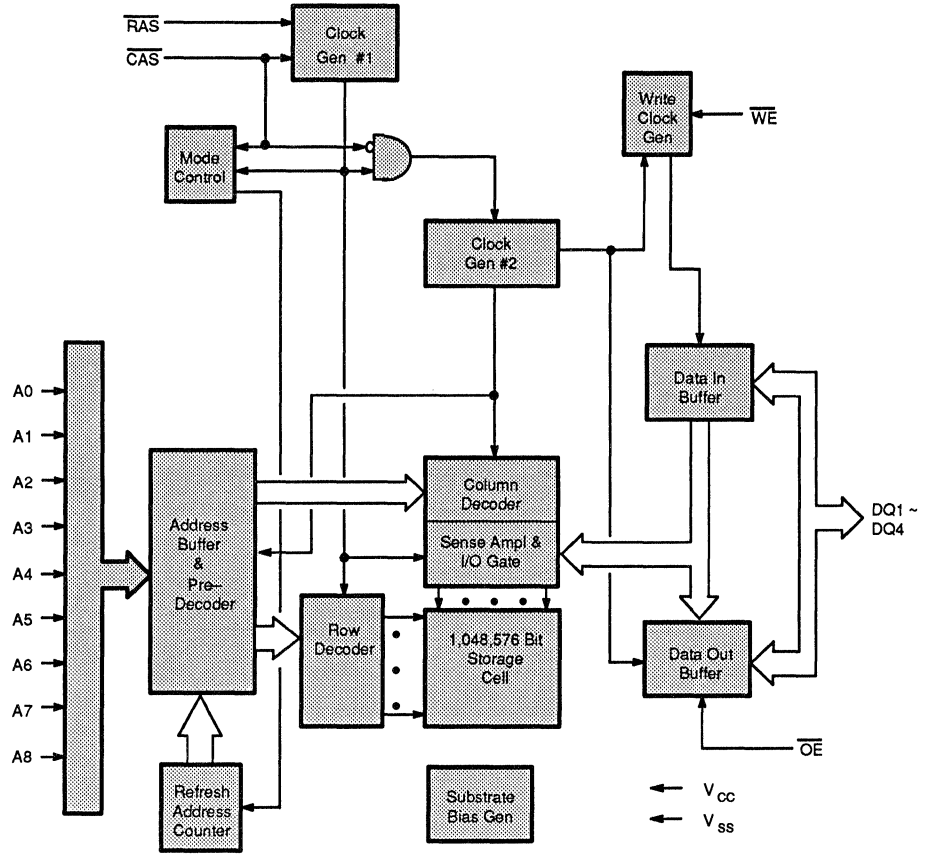
Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

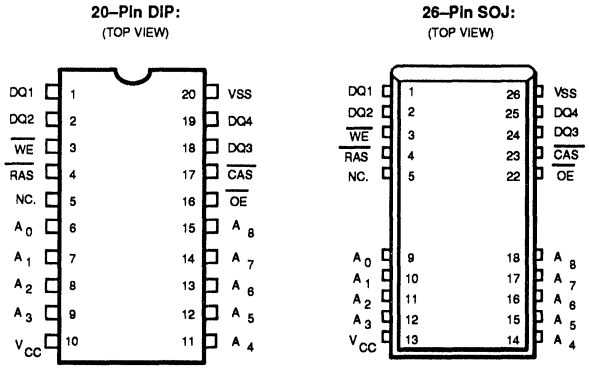
Fig. 1 – MB81C4258 DYNAMIC RAM – BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A8	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	−2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	−1.0	—	0.8	V	

* : Undershoots of up to −2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any four of 1,048,576 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, nine row address bits are input on pins A0–through–A8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

2

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

tOEA : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

STATIC COLUMN MODE OF OPERATION

The static column mode operation allows continuous read, write, or read–modify–write cycle within a row byapplying new column address. In the static column mode, $\overline{RAS}$ can be kept low throughout static column mode operation. The following four cycles are allowed in the static column mode.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Parameter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = −5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	−10	—	10	µA
Output leakage current		$I_{DQ(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	−10	—	10	µA
Operating current (Average Power supply Current) [2]	MB81C4258-70	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB81C4258-80					70	
	MB81C4258-10					60	
	MB81C4258-12					50	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} −0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB81C4258-70	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	70	mA
	MB81C4258-80					65	
	MB81C4258-10					55	
	MB81C4258-12					45	
Static Column Mode current [2]	MB81C4258-70	I_{CC4}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IL} t_{SC} = min	—	—	37	mA
	MB81C4258-80					35	
	MB81C4258-10					30	
	MB81C4258-12					23	
Refresh current #2 (Average power supply current) [2]	MB81C4258-70	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	70	mA
	MB81C4258-80					65	
	MB81C4258-10					55	
	MB81C4258-12					45	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4258-70		MB81C4258-80		MB81C4258-10		MB81C4258-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	140	—	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	197	—	212	—	240	—	275	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	70	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	9	t_{CAC}	—	25	—	25	—	25	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	43	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	7	—	7	—	7	—	7	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	60	—	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	70	100000	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	20	45	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time	23	t_{CSH}	70	—	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (C–B–R cycle)		t_{CPN}	15	—	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	12	—	15	—	15	—	ns
21	Column Address Set Up Time	7	t_{ASC}	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time	7	t_{CAH}	20	—	20	—	20	—	25	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	15	27	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	43	—	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	0	—	ns
28	Write Command Hold Time		t_{WCH}	20	—	20	—	20	—	25	—	ns
29	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	15	—	20	—	ns
30	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	22	—	22	—	25	—	30	—	ns
31	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	17	—	17	—	20	—	25	—	ns
32	DIN set Up Time		t_{DS}	0	—	0	—	0	—	0	—	ns
33	DIN Hold Time		t_{DH}	20	—	20	—	20	—	25	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C4258-70		MB81C4258-80		MB81C4258-10		MB81C4258-12		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
34	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	0	—	ns
35	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	15	—	20	—	ns
37	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	22	—	25	—	30	ns
38	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	—	25	ns
39	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	10	—	ns
40	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	15	t_{OEH}	0	—	0	—	0	—	0	—	ns
41	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	25	—	ns
42	DIN to $\overline{CAS}$ Delay Time	16	t_{DZC}	0	—	0	—	0	—	0	—	ns
43	DIN to $\overline{OE}$ Delay Time	16	t_{DZO}	0	—	0	—	0	—	0	—	ns
44	Access Time from $\overline{CAS}$ (Counter Test Cycle)		t_{CAT}	—	43	—	45	—	50	—	60	ns
50	Static Column Mode Read/Write Cycle Time		t_{SC}	48	—	50	—	55	—	65	—	ns
51	Static Column Mode Read-Modify-Write Cycle Time		t_{SRWC}	121	—	125	—	135	—	155	—	ns
52	Access Time Relative to Last Write	17	t_{ALW}	—	91	—	95	—	105	—	125	ns
53	Access Time from $\overline{WE}$ Precharge		t_{WPA}	—	25	—	25	—	30	—	35	ns
54	Output Hold Time for Column Address Change		t_{AOH}	10	—	10	—	10	—	10	—	ns
55	Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	18	t_{AHR}	15	—	15	—	15	—	15	—	ns
56	Last Write to Column Address Delay Time	19,20	t_{LWAD}	25	48	25	50	25	55	30	65	ns
57	Column Address Hold Time Referenced to Last Write		t_{AHLW}	91	—	95	—	105	—	125	—	ns
58	$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	70	—	80	—	100	—	120	—	ns
59	$\overline{WE}$ Inactive Time		t_{WI}	13	—	15	—	15	—	20	—	ns
60	Write Set Up Time for Output Disable	21	t_{WS}	0	—	0	—	0	—	0	—	ns
61	Write Hold Time for Output Disable	21	t_{WH}	0	—	0	—	0	—	0	—	ns
62	$\overline{OE}$ Hold Time Referenced to $\overline{RAS}$	22	t_{OEHR}	20	—	20	—	20	—	20	—	ns
63	$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$	22	t_{OEHC}	20	—	20	—	20	—	20	—	ns
64	Static Column Mode CAS Precharge Time		t_{CP}	15	—	15	—	15	—	15	—	ns
65	Write Command Hold Time Referenced to $\overline{RAS}$		t_{WHR}	5	—	5	—	5	—	5	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ –only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ –before–$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. Assumes that write cycle only.
8. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA} .
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
12. t_{RCD} (min) = t_{RAH} (min)+ 2t_T + t_{ASC} (min)
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Assumes that t_{WCS} < t_{WCS} (min)
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
18. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
19. Operation within the t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, access time is controlled by t_{AA} .
20. t_{LWAD} (min) = t_{CAH} (min)+ t_T (t_T – 5ns).
21. t_{WS} and t_{WH} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High–Z state through entire cycle.
22. Either t_{OEHR} or t_{OEHC} is satisfied.
23. Assumes that $\overline{CAS}$ -before-$\overline{RAS}$ refresh, $\overline{CAS}$ -before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 2 – t_{RAC} vs. t_{RCD}

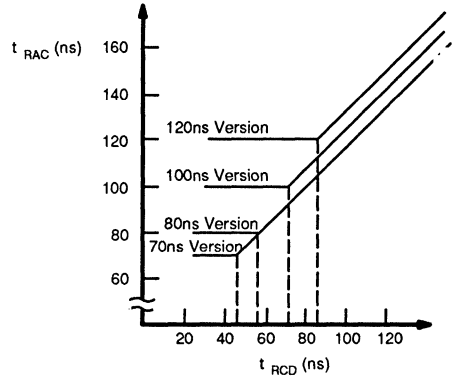
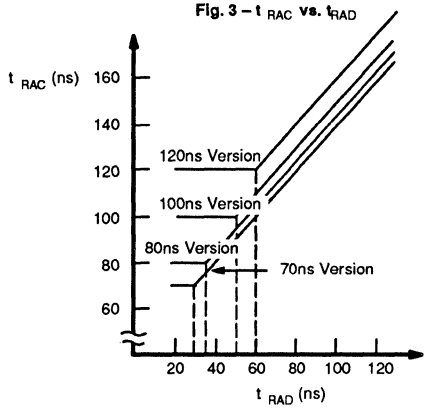


Fig. 3 – t_{RAC} vs. t_{RAD}



2

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	O	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	*1 High-Z	O	$t_{WS} \geq t_{WS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	L → H	Valid	Valid	Valid	Valid	O	
Static Column Mode Read Cycle	L	L	H	L	*2 Valid	Valid	—	Valid	X	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Static Column Mode Write Cycle	L	L	L	H	*2 Valid	Valid	Valid	*1 High-Z	X	
Static Column Mode Read–Modify–Write Cycle	L	L	H → L	L → H	*2 Valid	Valid	Valid	Valid	X	
Static Column Mode Mixed Cycle	L	L	L/H	L/H	*2 Valid	Valid	Valid	High-Z or Valid	X	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	X	X	—	—	—	High-Z	O	
Hidden Refresh Cycle	H → L	L	X	L	—	—	—	Valid	O	Previous data is kept

Notes:

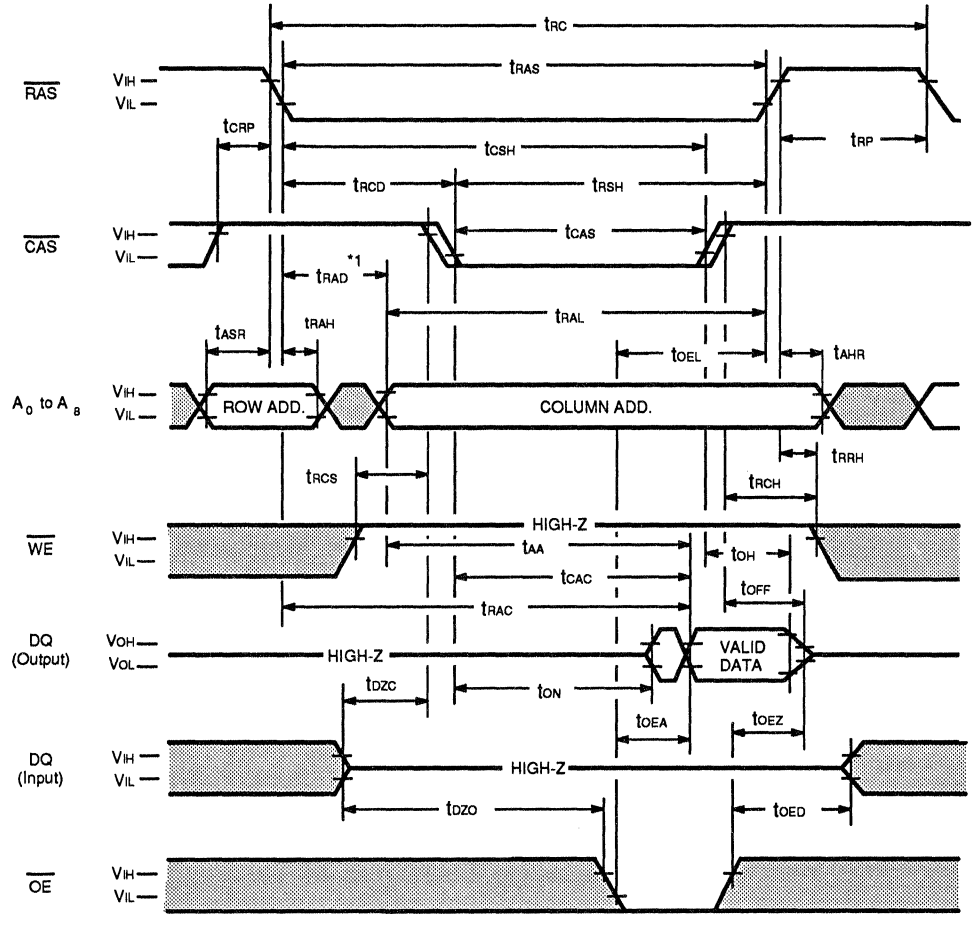
X : "H" or "L"

*1: If tWS < tWS (min) and tWH < tWH (min), the data output become invalid.

*2: After first cycle, row address is not necessary.

2

Fig. 4 – READ CYCLE



*1; If tRAD ≧ tRAD (max), access time is tCAC or tAA whichever occur later.

"H" or "L"

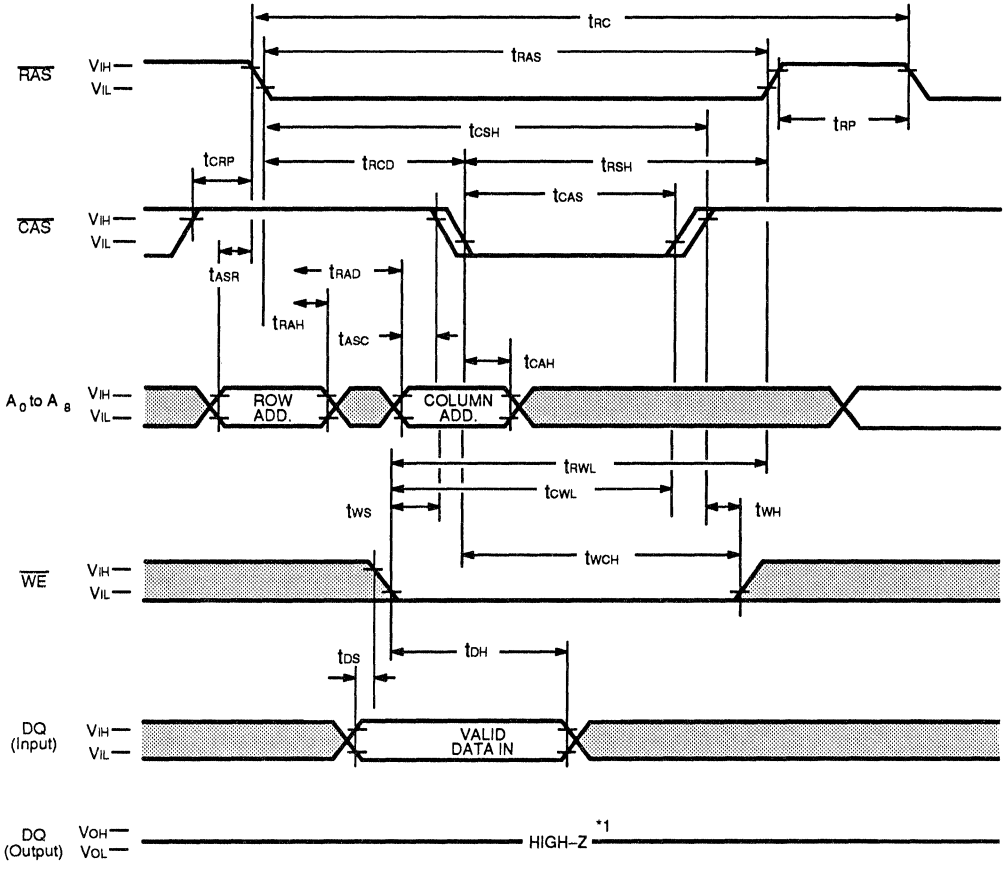
DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by RAS ($\overline{RAC}$), CAS ($\overline{CAC}$), OE, ($\overline{OEA}$) or column addresses (tAA) under the following conditions:

- If tRCD > tRCD (max), access time = tCAC.
- If tRAD > tRAD (max), access time = tAA.
- If $\overline{OE}$ is brought Low after tRAC, tCAC, or tAA (which ever occurs later), access time = tOEA.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after tOH is satisfied.

Fig. 5 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



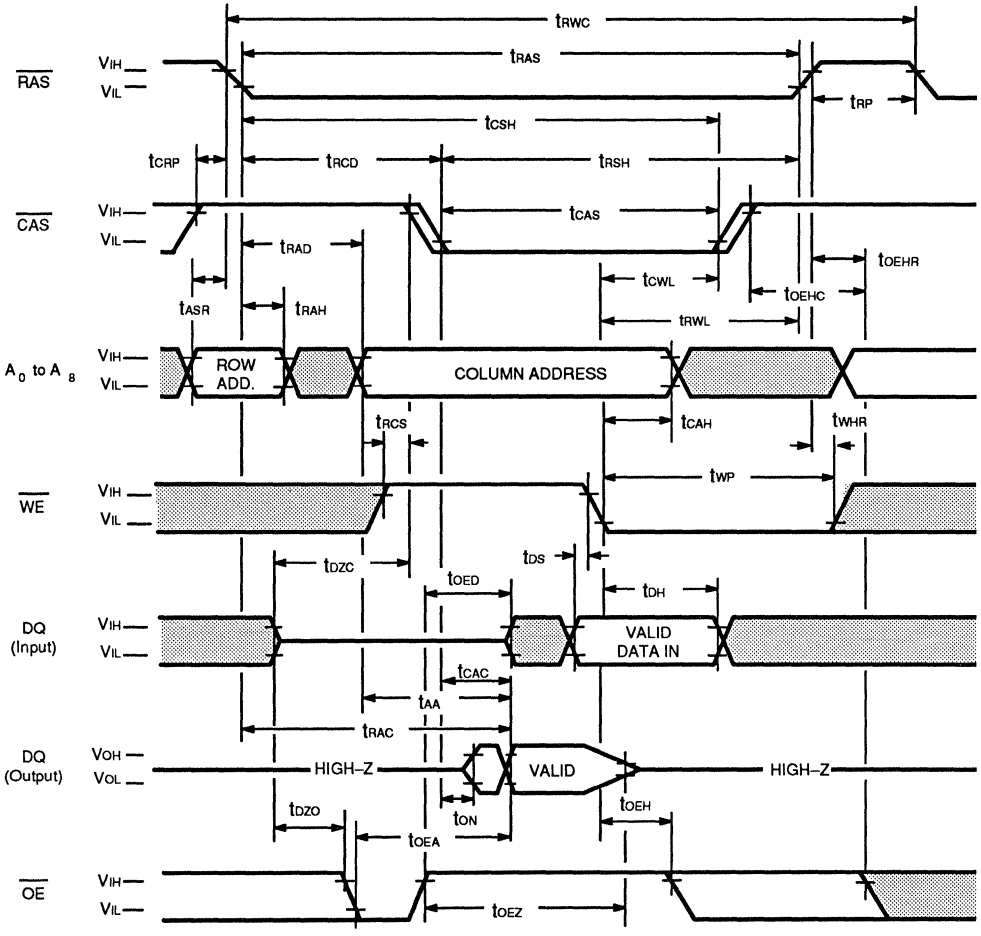
*1; If tWS ≥ tWS (min) and tWH ≥ tWH (min), DQ (Output) pin is high-Z.

DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways—early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters tRWL, tCWL and tRAL must be satisfied. In the early write cycle shown above twcs satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

2

Fig. 6 – READ–MODIFY–WRITE–CYCLE

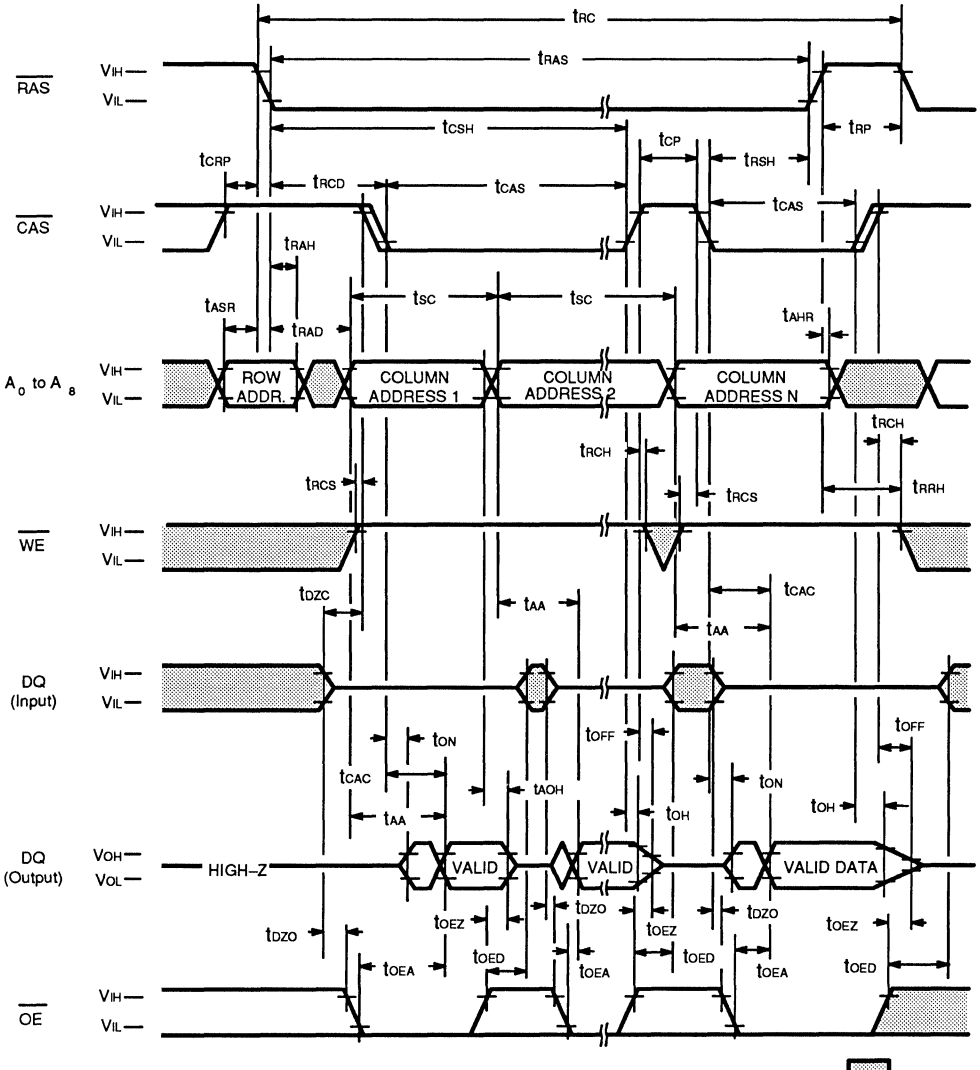


"H" or "L"

DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 7 – STATIC COLUMN MODE READ CYCLE

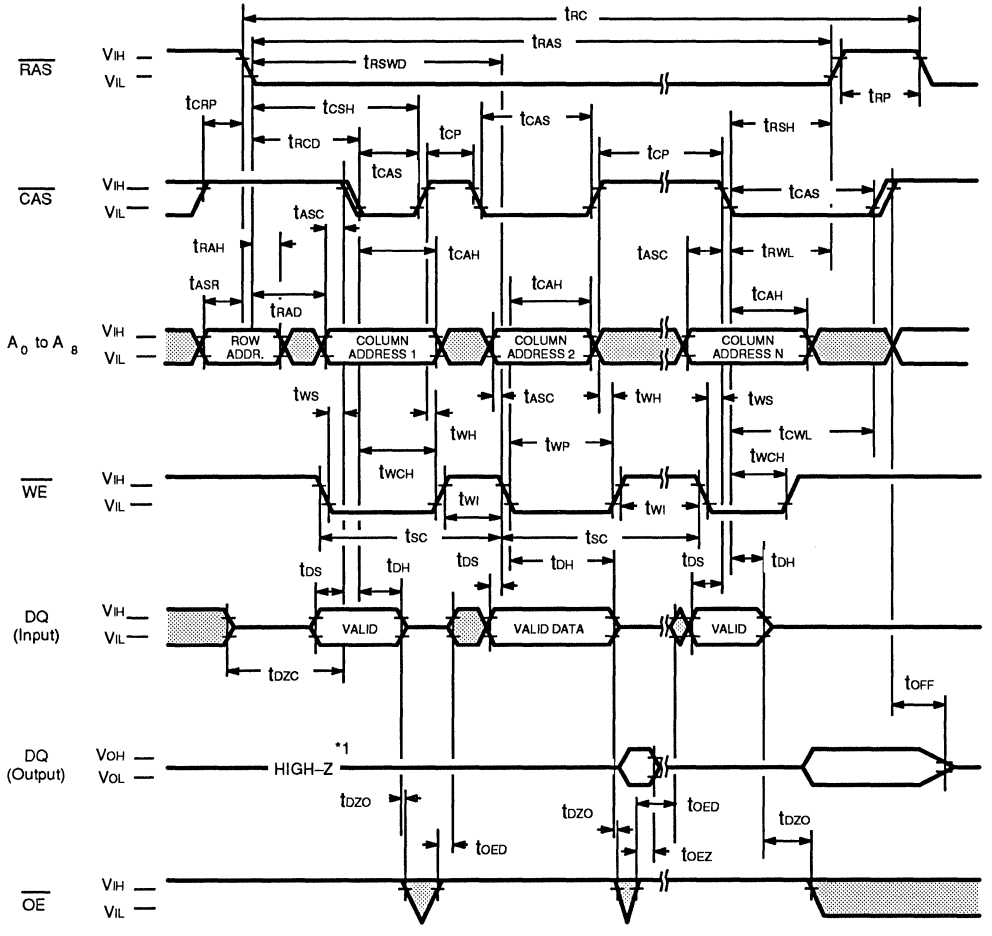


DESCRIPTION

In a static column mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input or t_{OEA} from the falling edge of $\overline{OE}$. The data remains valid for a time t_{AOH} after the column address is changed.

2

Fig. 8 – STATIC COLUMN MODE WRITE CYCLE ($\overline{OE}$ = "H " or "L")



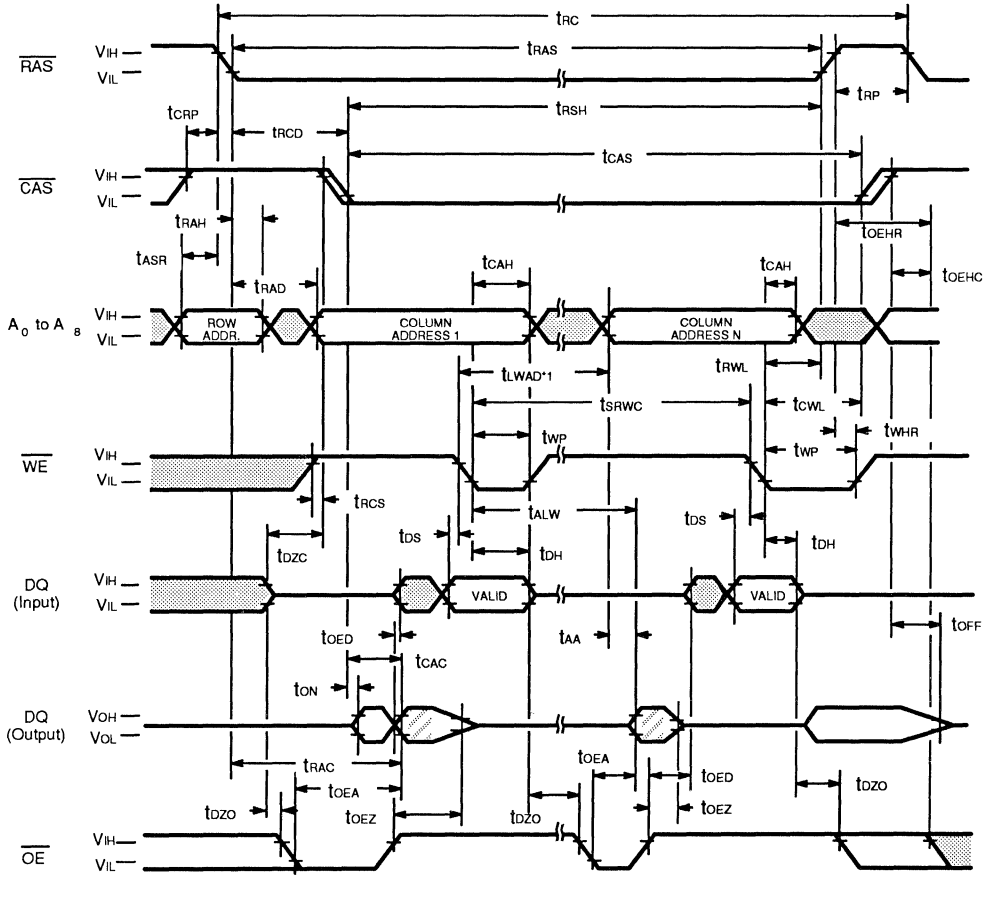
*1; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), DQ (Output) pin is high–Z.

"H" or "L"

DESCRIPTION

In a static column mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static column mode write cycle. The $\overline{OE}$ must be high before the data are applied to DQ pins.

Fig. 9 – STATIC COLUMN MODE READ–MODIFY–WRITE CYCLE



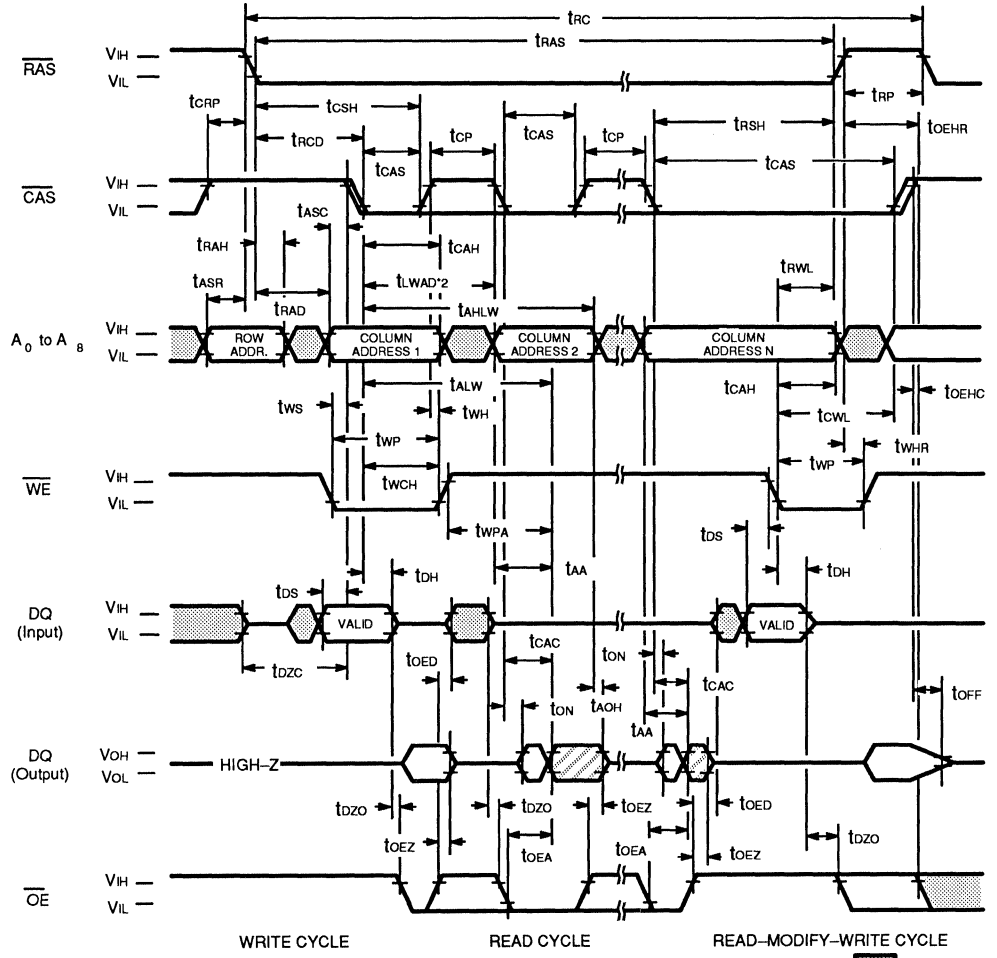
*1; If t_{LWAD} (min) ≤ t_{LWAD} ≤ t_{LWAD} (max), t_{ALW} = t_{SC} (min) + t_{AA} (max).

DESCRIPTION

In the static column mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the faling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of WE. The OE must be high before the data are applied to DQ pins.

2

Fig. 10 – STATIC COLUMN MODE MIXED CYCLE *1



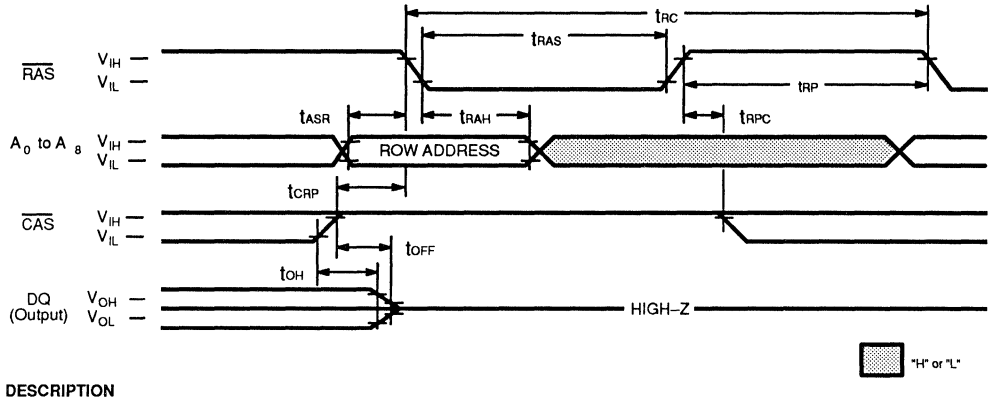
*1; This is an example of static column mode mixed cycle.
*2; If t_{LWAD} is satisfied its min/max value, $t_{ALW} = t_{SC}$ (min) + t_{AA} (max)

DESCRIPTION

In the static column mode, read, write, and read-modify-write cycles can be mixed in any order.
In the next read cycle of static column mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. t_{ALW} from the falling edge of $\overline{WE}$ or $\overline{CAS}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$
5. t_{OEA} from the falling edge of $\overline{OE}$

Fig. 11 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

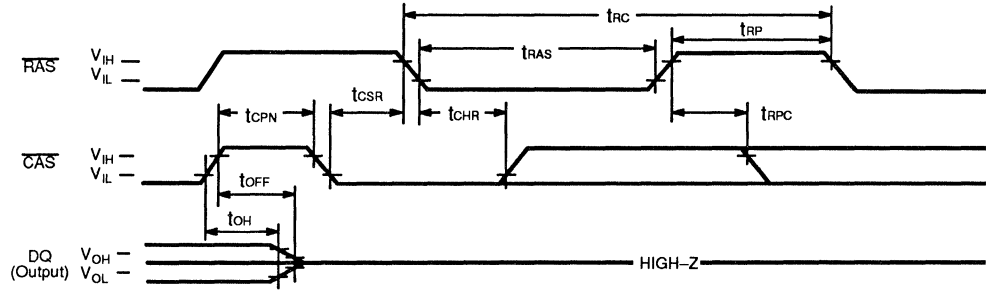


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycleat each of 512 row addresses every 8.2–milliseconds. Three refresh modes are available; $\overline{RAS}$–only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DQ pins are kept in a high-impedance state.

Fig. 12 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (A0 to A8 = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

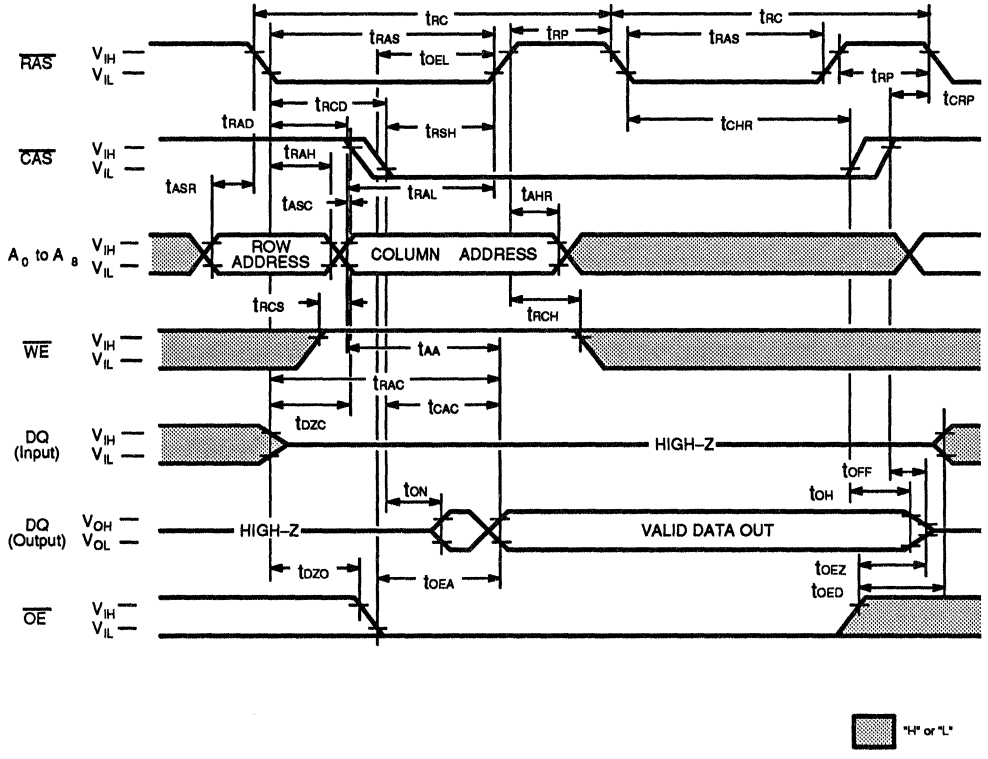


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (tCSR) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

2

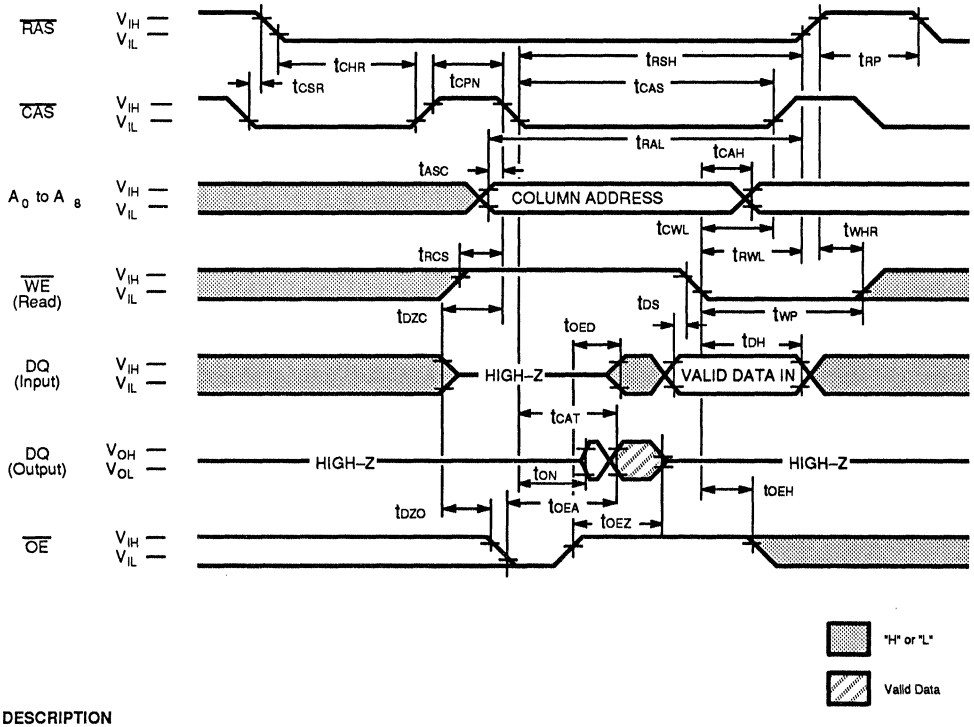
Fig. 13 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminatesthe need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Fig. 14 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above, Row and column addresses are defined asfollows:

Row Address: Bits A0 through A8 are defined by the on-chip refresh counter.
Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of $\overline{CAS}$.

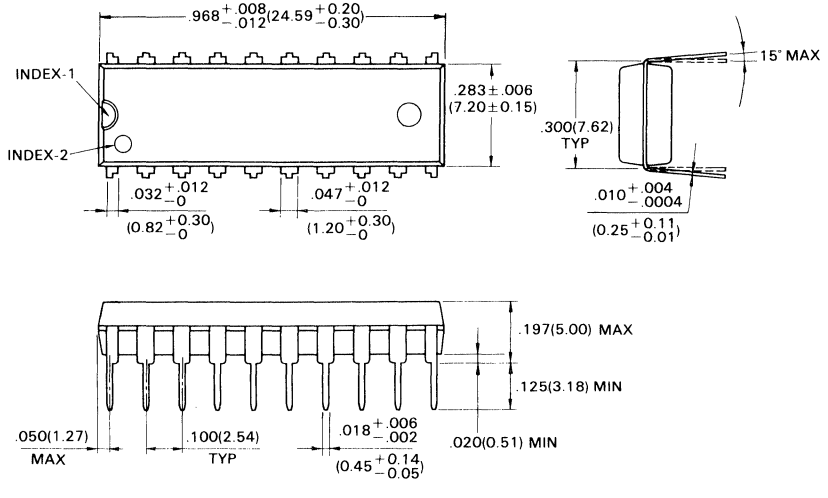
The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle is designed for use with the following procedures:

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Use the same column address throughout the test.
3) Write zeroes (0s) to all 512 row addresses at the same column address by using normal early write cycles.
4) Read zeroes written in procedure 3 and check; simultaneously write ones (1s) to the same addresses by using internal refresh counter test read-write cycles. Repeat this procedure 5.2 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4 by using normal read cycle for all 512 memory locations.
6) Complement test pattern and repeat procedures 3, 4, and 5.

PACKAGE DIMENSIONS

(Suffix : –P)

20–LEAD PLASTIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20P–M03)

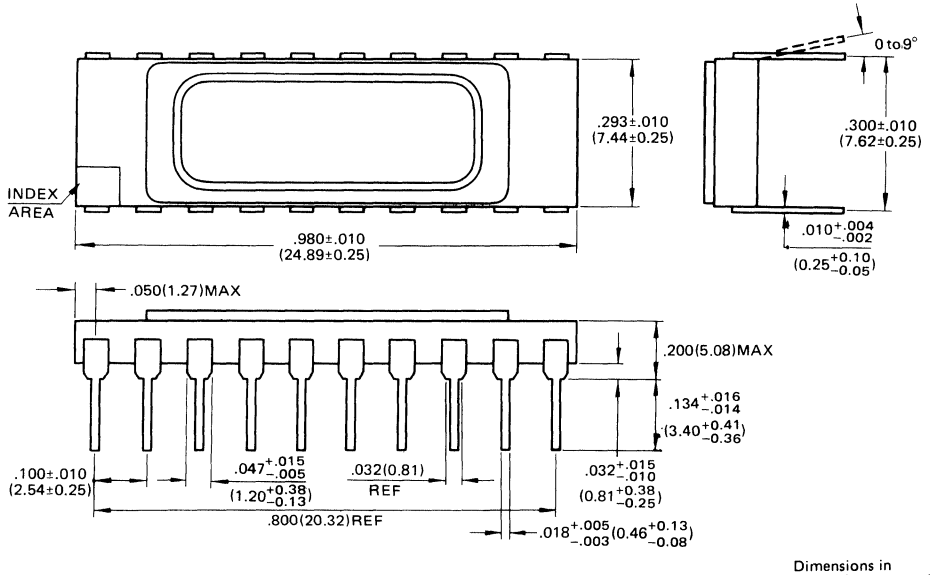


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –C)

20–LEAD CERAMIC DUAL IN–LINE PACKAGE
(CASE No.: DIP–20C–A03)

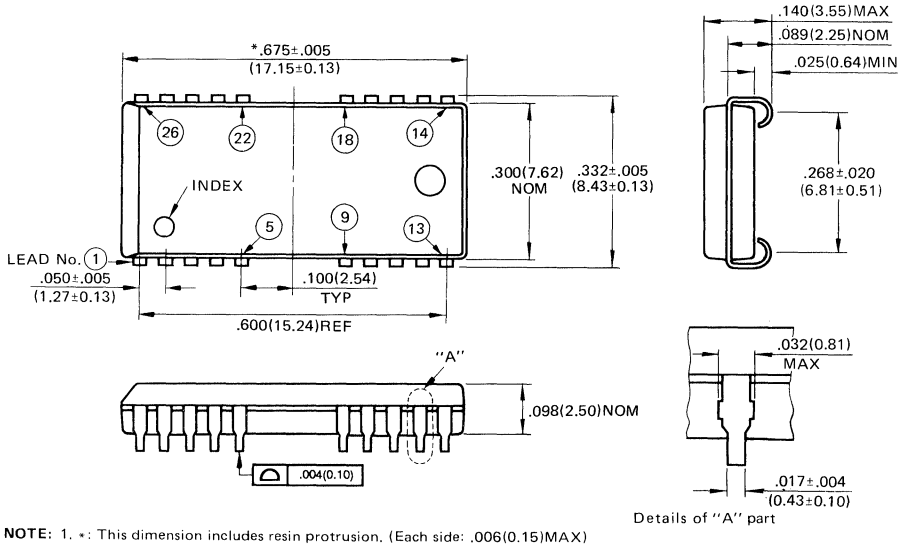


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26–LEAD PLASTIC LEADED CHIP CARRIER (SOJ–26)
(CASE No.: LCC–26P–M04)



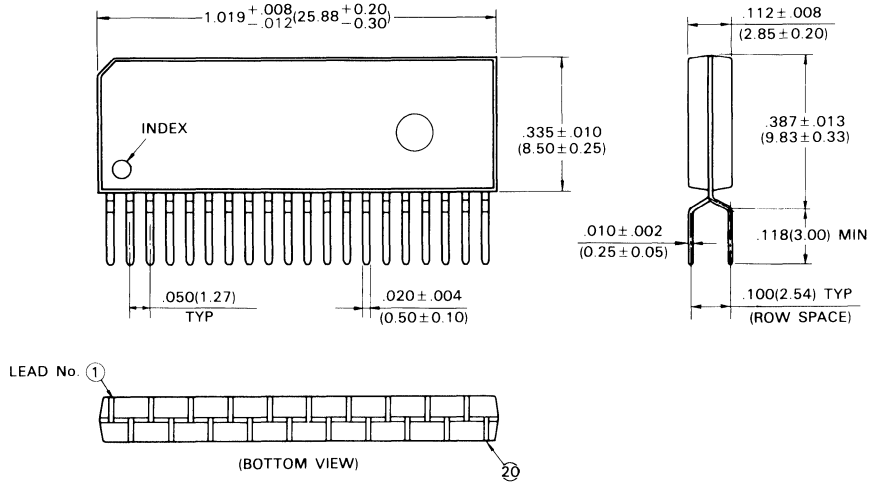
NOTE: 1. *: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.

Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(CASE No.: ZIP–20P–M02)



Dimensions in
inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C4258A-60/-80/-10

CMOS 1,048,576 BIT STATIC COLUMN MODE DYNAMIC RAM

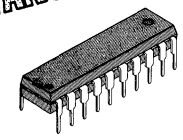
CMOS 262,144 x 4 BIT Static Column Mode Dynamic RAM

The Fujitsu MB81C4258A is CMOS fully decoded dynamic RAM organized as 262,144 words x 4 bits. The MB81C4258A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed, high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology makes the MB81C4258A High α-ray soft error immunity and long refresh time.

The CMOS circuits can be used as peripheral circuits. In addition, low power dissipation and high speed operation are realized.

ADVANCE INFO.

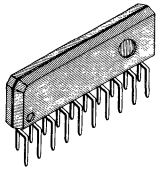


DIP-20P-M03

T.B.D

DIP-20C-XXX

LCC-26P-M04



ZIP-20P-M02

2

PRODUCT LINE & FEATURES

Parameter	MB81C4258A-60	MB81C4258A-80	MB81C4258A-10
$\overline{RAS}$ Access Time	60ns max.	80ns max.	100ns max.
Randam Cycle Time	130ns min.	155ns min.	180ns min.
Address Access Time	30ns max.	40ns max.	50ns max.
$\overline{CAS}$ Access Time	15ns max.	20ns max.	25ns max.
Static Column Mode Cycle	35ns min.	45ns min.	55ns max.
Low Power Dissipation • Operating current	330mW max.	275mW max.	248mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 262,144 words x 4 bits organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Early write $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Static Column Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Voltage at any pin relative to VSS		V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS		V_{CC}	−1 to +7	V
Power Dissipation		PD	1.0	W
Short Circuit Output Current		—	50	mA
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB814100-80/-10/-12

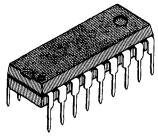
CMOS 4,194,304 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 4,194,304 x 1 BIT Fast Page Mode Dynamic RAM

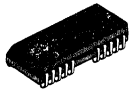
PRELIMINARY

The Fujitsu MB814100 is a fully decoded CMOS Dynamic RAM (DRAM) that contains a total of 4,194,304 memory cells in a x1 configuration. The MB814100 features a "fast page" mode of operation whereby high-speed random access of up to 2,048-bits of data within the same row can be selected. The MB814100 DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814100 is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB814100 is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814100 are not critical and all inputs are TTL compatible.

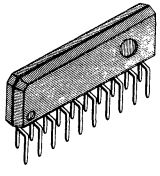


DIP-18P-M04



LCC-26P-M04

LCC-26P-M03



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB814100-80	MB814100-10	MB814100-12
$\overline{RAS}$ Access Time	80ns max.	100ns max.	120ns max.
Randam Cycle Time	155ns min.	180ns min.	210ns min.
Address Access Time	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	30ns max.	35ns max.
Fast Page Mode Cycle Time	55ns min.	60ns min.	70ns min.
Low Power Dissipation • Operating current	413mW max.	358mW max.	303mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 4,194,304 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4ms
- Common I/O capability by using early write
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

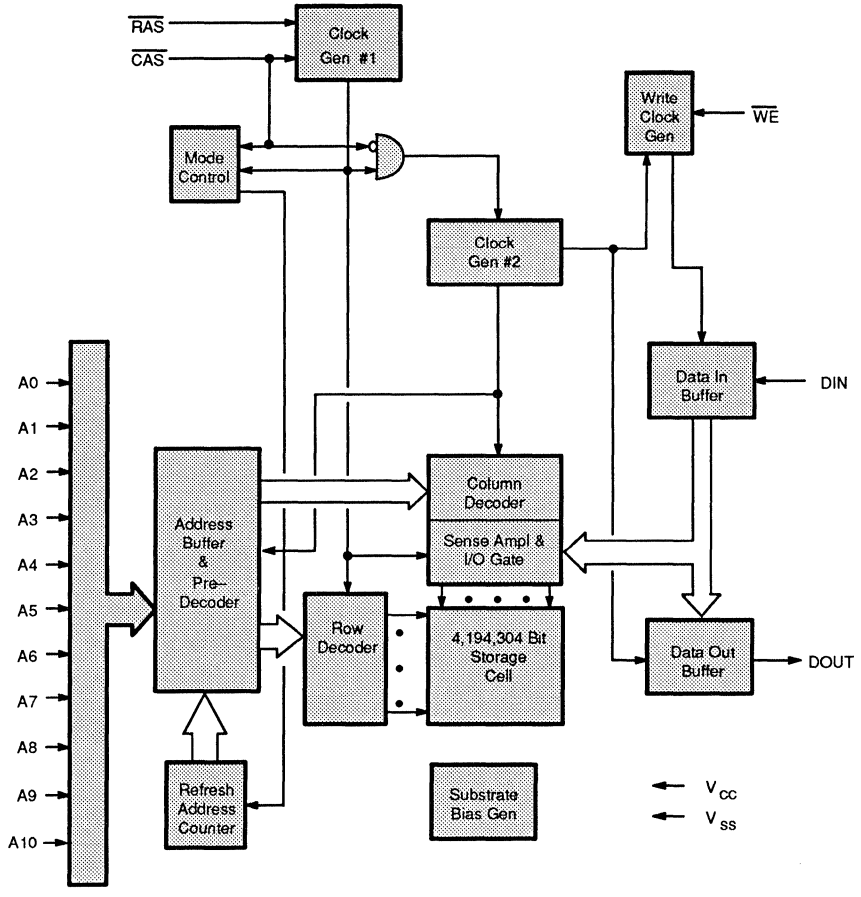
Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB814100 DYNAMIC RAM – BLOCK DIAGRAM

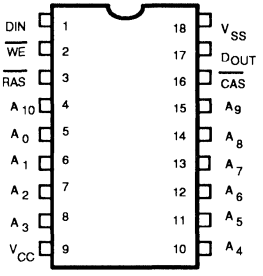


CAPACITANCE (T_A = 25°C, f = 1MHz)

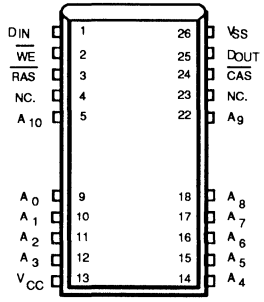
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A10, DIN	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	5	pF
Output Capacitance, DOUT	C_{OUT}	—	5	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

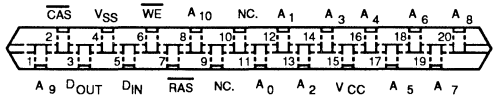
18–Pin DIP:
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
D_{IN}	Data Input.
D_{OUT}	Data Output.
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
NC	No connection.
A0 to A10	Address inputs.
VCC	+5 volt power supply.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty–two input bits are required to decode any one of 4,194,304 cell addresses in the memory matrix. Since only eleven address bits (A0–A10) are available, the column and row inputs are separately strobed by $\overline{RAS}$ and $\overline{CAS}$ as shown in Figure 4. First, eleven row address bits are applied on pins A0–through–A10 and latched with the row address strobe ($\overline{RAS}$) then, eleven column address bits are applied and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or beforethe falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

2

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of two basic ways—an early write cycle and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

tRAC : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

tCAC : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

tAA : from column address input when t_{RAD} is greater than t_{RAD} (max).

The data remains valid until either $\overline{CAS}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 2,048–bits can be accessed and, when multiple MB 814100s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) **Notes 3**

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	V
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	–10	—	10	µA
Output leakage current		$I_{O(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10	—	10	µA
Operating current (Average Power supply current)	MB814100–80	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814100–10					65	
	MB814100–12					55	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current)	MB814100–80	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814100–10					65	
	MB814100–12					55	
Fast Page Mode current	MB814100–80	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	75	mA
	MB814100–10					65	
	MB814100–12					55	
Refresh current #2 (Average power supply current)	MB814100–80	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	75	mA
	MB814100–10					65	
	MB814100–12					55	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100-80		MB814100-10		MB814100-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	185	—	210	—	245	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	30	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	17	t_{CPN}	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814100-80		MB814100-10		MB814100-12		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ to $\overline{WE}$ Delay Time	15	t_{RWD}	80	—	100	—	120	—	ns
36	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	—	30	—	35	—	ns
37	Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	—	50	—	60	—	ns
38	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	ns
39	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
40	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	20	—	ns
41	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
42	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	15	—	15	—	20	—	ns
51	Fast Page Mode Read/Write Cycle Time		t_{PC}	55	—	60	—	70	—	ns
52	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	85	—	90	—	105	—	ns
53	Access Time from $\overline{CAS}$ Precharge	9,16	t_{CPA}	—	55	—	60	—	70	ns
54	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	ns

Notes:

1. Referenced to VSS
2. Icc depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   Icc depends on the number of address change as $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc1, Icc3 and Icc5 are specified at three time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
   Icc4 is specified at one time of address change during $\overline{RAS}$ = VIL and $\overline{CAS}$ = VIH.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ =VIH) of 200µs is required after power-up followed by any eight $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ -before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIH (min) and VIL (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min)+ $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and Dout pin will maintain high impedance state thoughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min), $t_{RWD} > t_{RWD}$ (min), and $t_{AWD} > t_{AWD}$ (min), the cycle is a read modify-write cycle and data from the selected cell will apper at the Dout pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the Dout pin, and write operation can be exected by satisfying t_{RWL}, t_{CWL}, and t_{RAL} specifications.
16. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$ -before- $\overline{RAS}$ refresh.

2

Fig. 2 – t_{RAC} vs. t_{RCD}

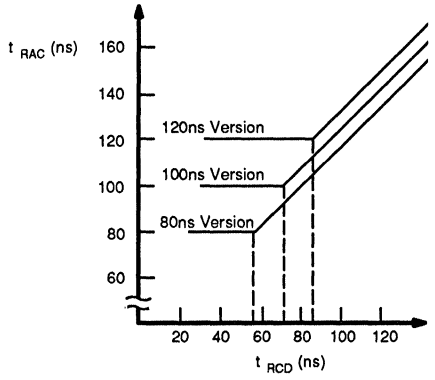
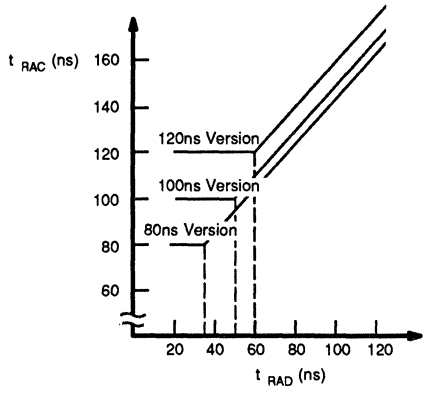


Fig. 3 – t_{RAC} vs. t_{RAD}

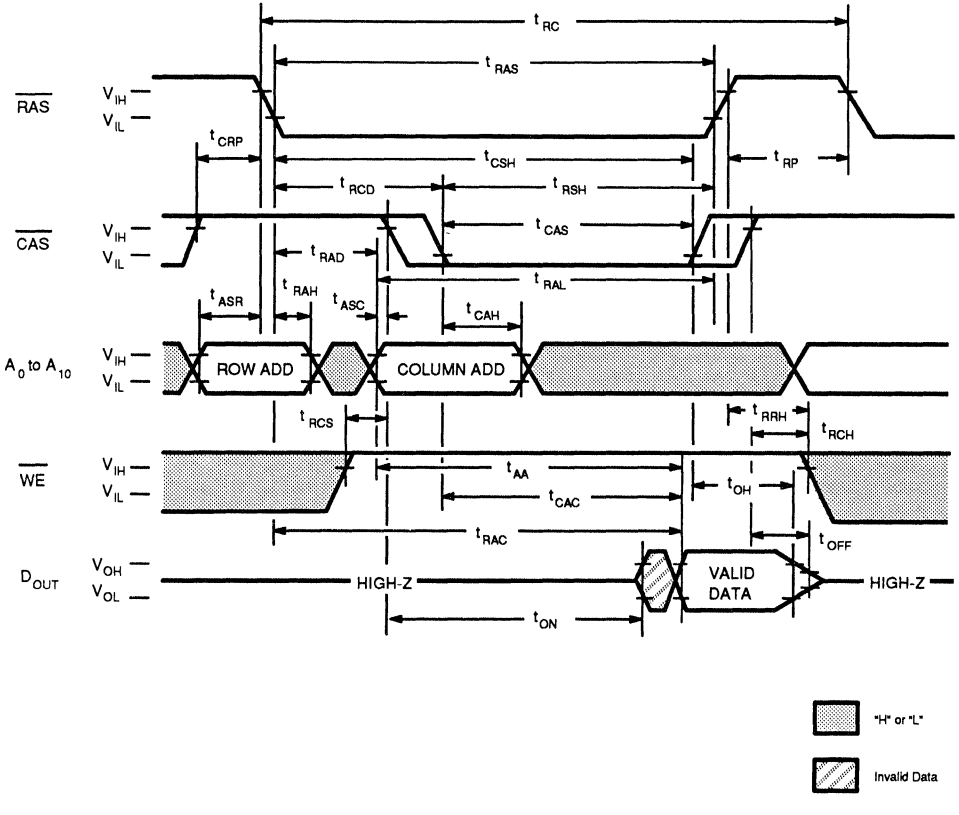


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	O *1	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	O *1	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	O *1	$t_{CWD} \geq t_{CWD}$ (min)
$\overline{RAS}$–only Refresh Cycle	L	H	X	Valid	—	—	High-Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	—	—	—	High-Z	O	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh Cycle	H → L	L	H	—	—	—	Valid	O	Previous data is kept

Notes:
X : "H" or "L"
*1: It is impossible in Fast Page Mode.

Fig. 4 – READ CYCLE

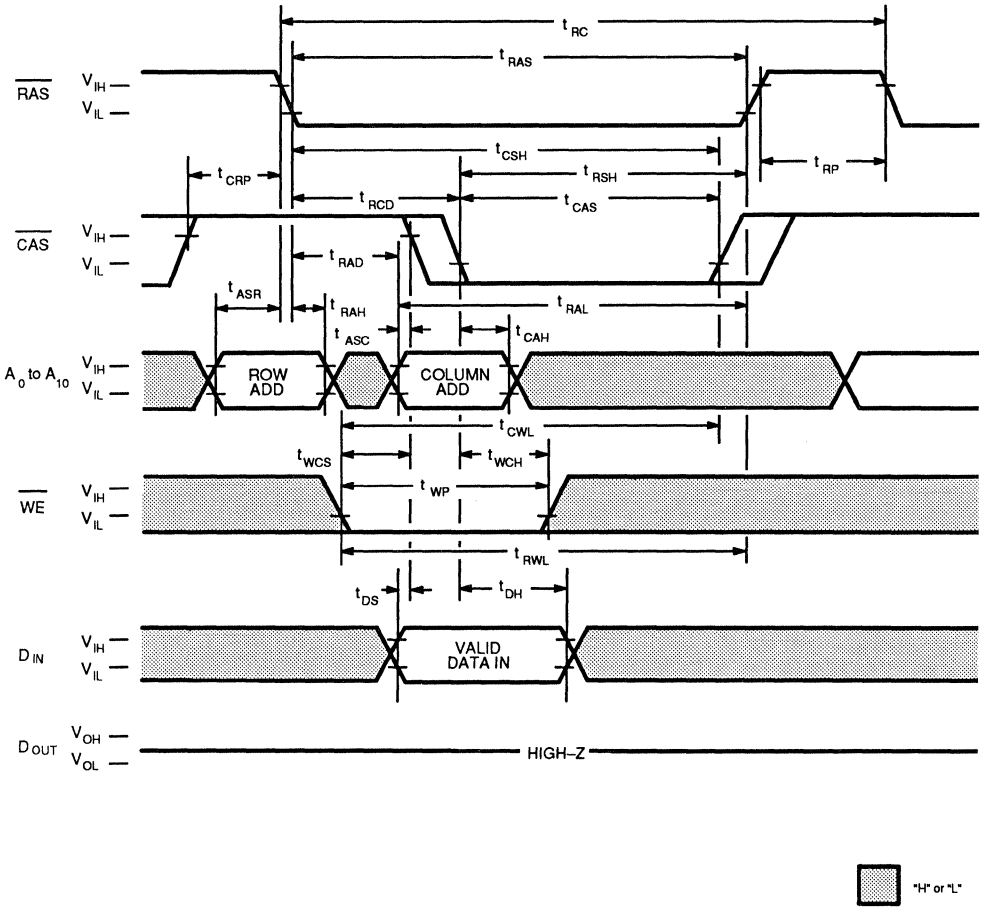


DESCRIPTION

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ "L" and keeping $\overline{WE}$ "H" throughout the cycle. Therow and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The data output remains valid with $\overline{CAS}$ "L", ie., if $\overline{CAS}$ goes "H", the data becomes invalid after tOH is satisfied. The access time is determined by $\overline{RAS}$ (tRAC), $\overline{CAS}$ (tCAC), or Column address input (tAA). If tRCD ($\overline{RAS}$ to $\overline{CAS}$ delay time)is greater than the specification, the access time is tAA.

2

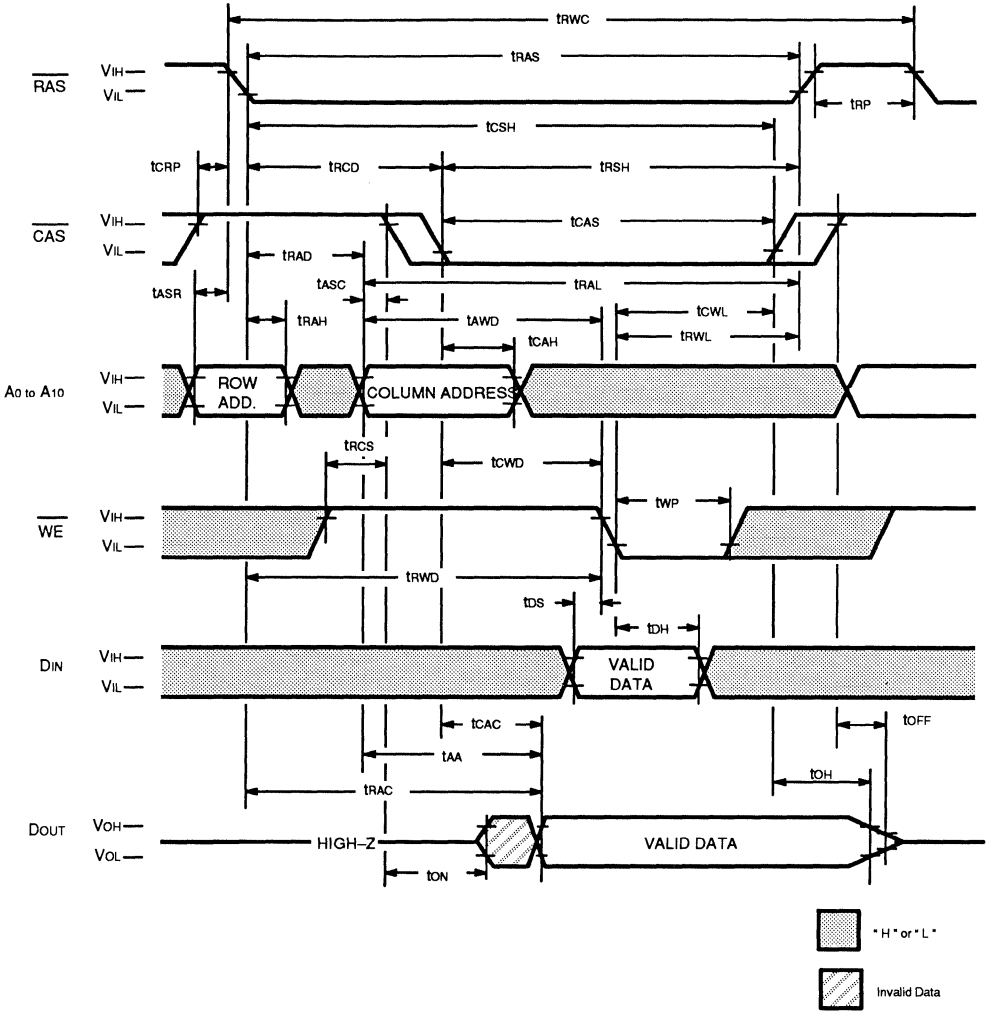
Fig. 5 — WRITE CYCLE (Early Write)



DESCRIPTION

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$ and DIN pins. The data on DIN pin islatched with the later falling edge of $\overline{CAS}$ or $\overline{WE}$ and written into memory. In addition, during write cycle, tRWL and tRAL must be satisfied with the specifications.

Fig. 6 – READ WRITE/READ–MODIFY–WRITE CYCLE

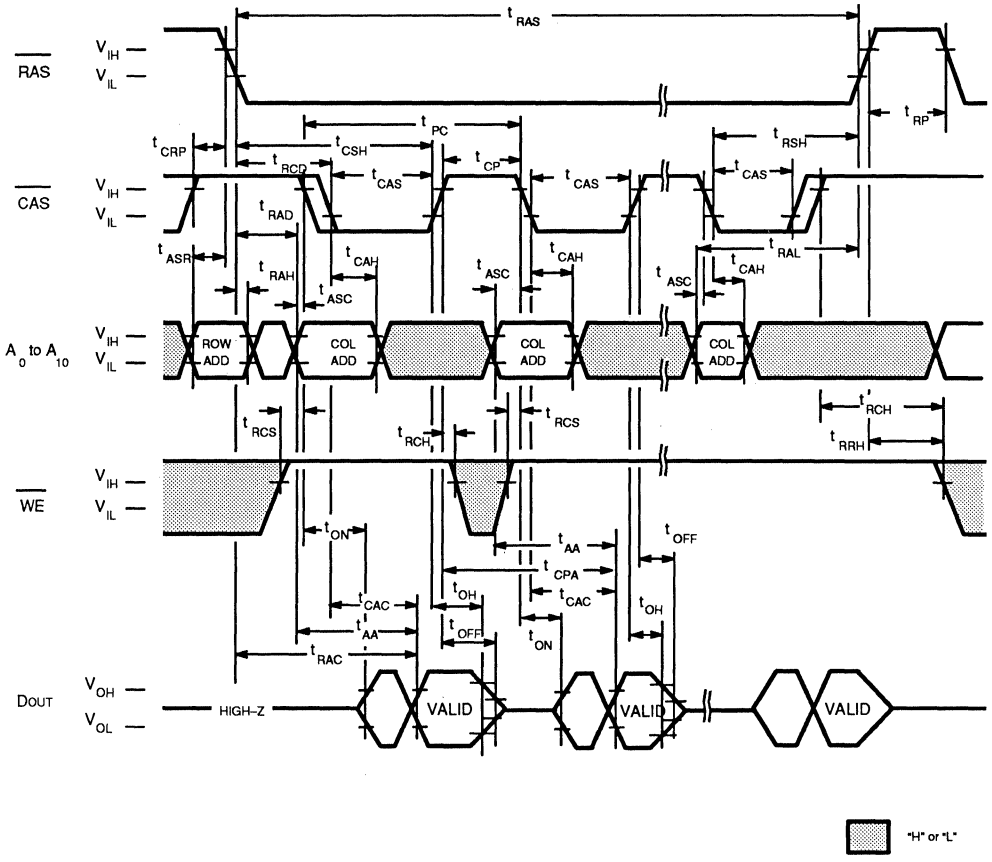


DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from "H" to "L" after the data appears on the DOUT pin. After the current data is read out, modified data can be rewritten into the same address quickly.

2

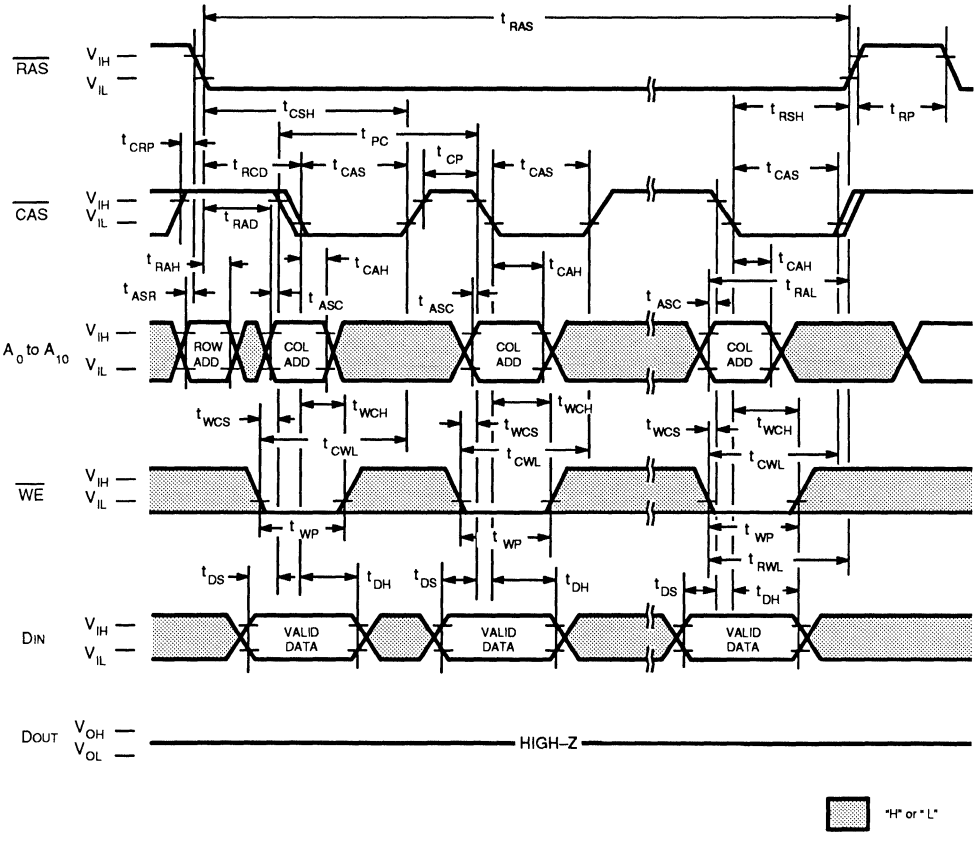
Fig. 7 – FAST PAGE MODE READ CYCLE



DESCRIPTION

The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ "L", applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ "H". Once an address is selected normally using the $\overline{RAS}$ and $\overline{CAS}$, other addresses in the same row can be selected by only changing the column address and applying the $\overline{CAS}$. During fast page mode, the access time is tCAC, tAA, or tCPA, whichever occurs later.
Any of the 2048 bits belonging to each row can be accessed.

Fig. 8 – FAST PAGE MODE WRITE CYCLE (Early Write)

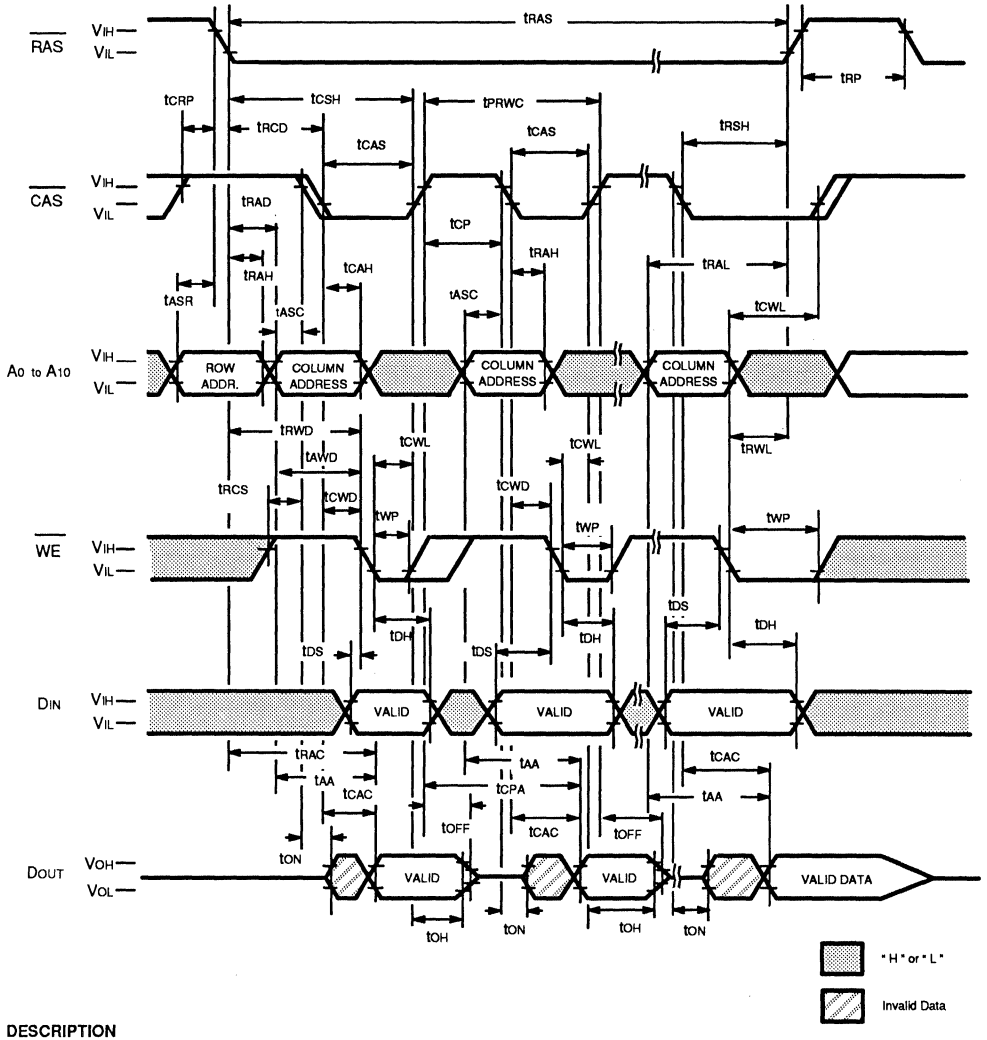


DESCRIPTION

The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$.
The data on DIN pin is latched with the falling edge of $\overline{CAS}$ and written into the memory. During fast page mode write cycle, tCWL must be satisfied. Any of the 2048 bits belonging to each row can be accessed.

2

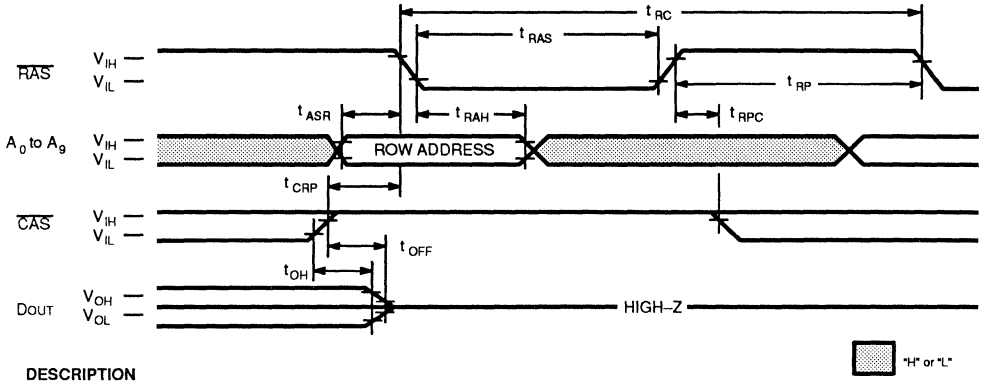
Fig. 9 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode, the read–modify–write cycle can be executed by changing $\overline{WE}$ high to low after the data appearsat DOUT pin as well as normal cycle. Any of the 2048 bits belonging to each row can be accessed.

Fig. 10 – $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$, DIN, A10 = "H" or "L")

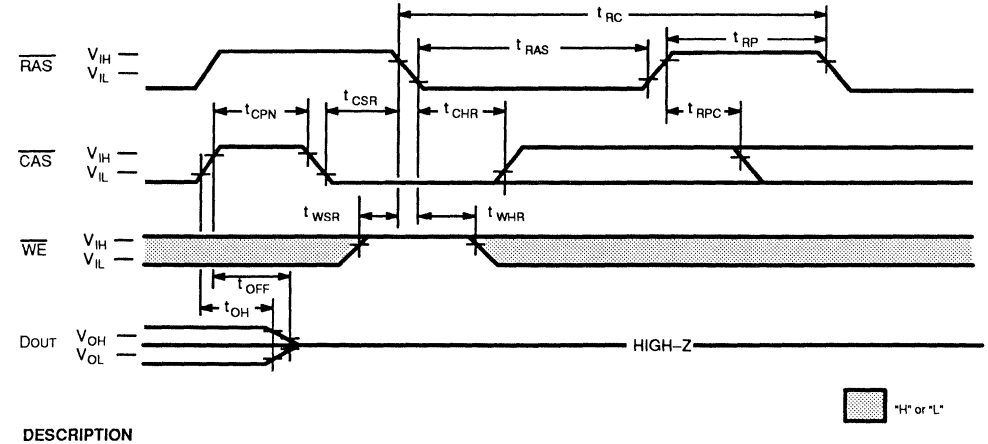


DESCRIPTION

The refresh of DRAM is executed by normal read, write or read–modify–write cycle, i.e., the cells on the one row line are also refreshed by executing one of three cycles. 1024 row address must be refreshed every 16.4ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re–written to the cell. The MB814100 has three types of refresh modes, $\overline{RAS}$–only refresh, $\overline{CAS}$–before–$\overline{RAS}$ refresh, and Hidden refresh.

The $\overline{RAS}$ only refresh is executed by keeping $\overline{RAS}$ "L" and $\overline{CAS}$ "H" throughout the cycle. The row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, the DOUT pin is kept in a high impedance state.

Fig. 11 – $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (A0 to A10, DIN="H" or "L")



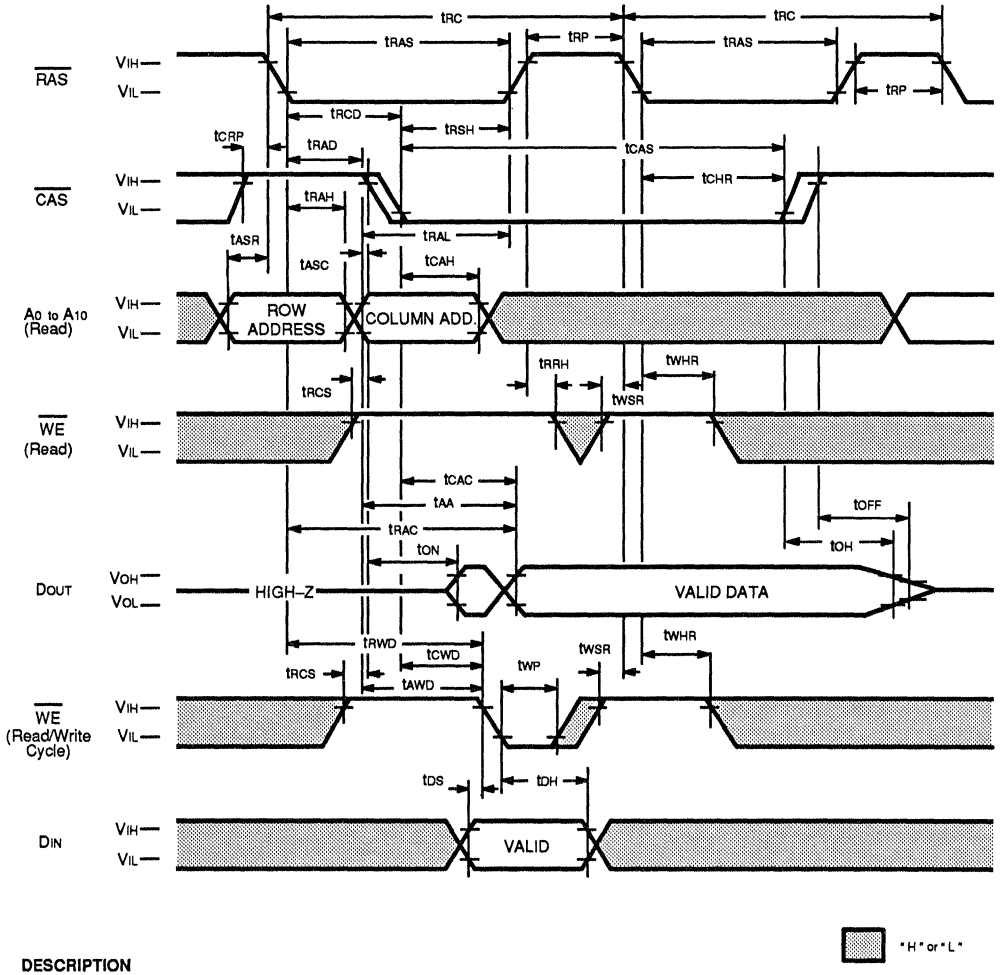
DESCRIPTION

The $\overline{CAS}$–before–$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ "L" before $\overline{RAS}$. By this timing combination, the MB814100 executes $\overline{CAS}$–before–$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" in order not to enter "test mode" to be specified later.

2

Fig. 12 – HIDDEN REFRESH CYCLE



DESCRIPTION

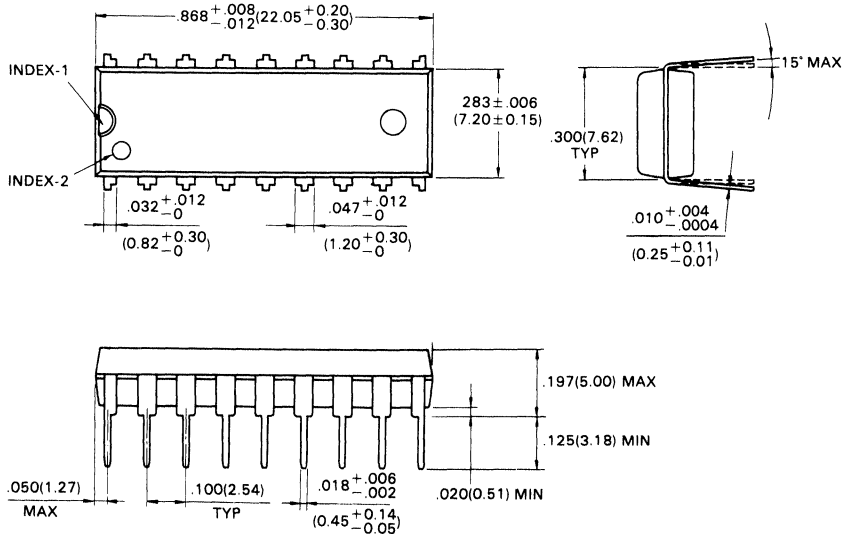
The hidden refresh is executed by keeping $\overline{CAS}$ "L" to next cycle, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$–before–$\overline{RAS}$ refresh.
$\overline{WE}$ must be held "H" for the specified set up time (tWSR) before $\overline{RAS}$ goes "L" for the second time in order not to enter "test mode" to be specified later.

PACKAGE DIMENSIONS

(Suffix : –P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-18P-M04)



Dimensions in
inches (millimeters)

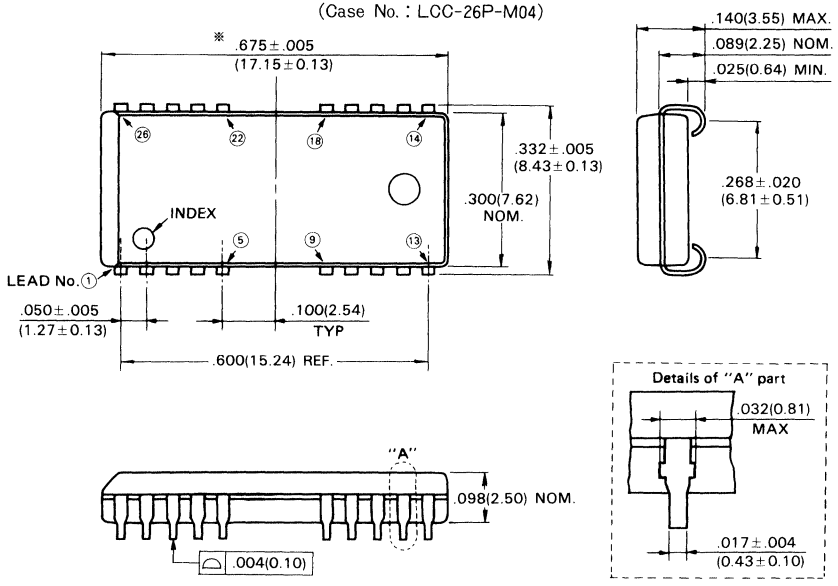
2

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-26P-M04)



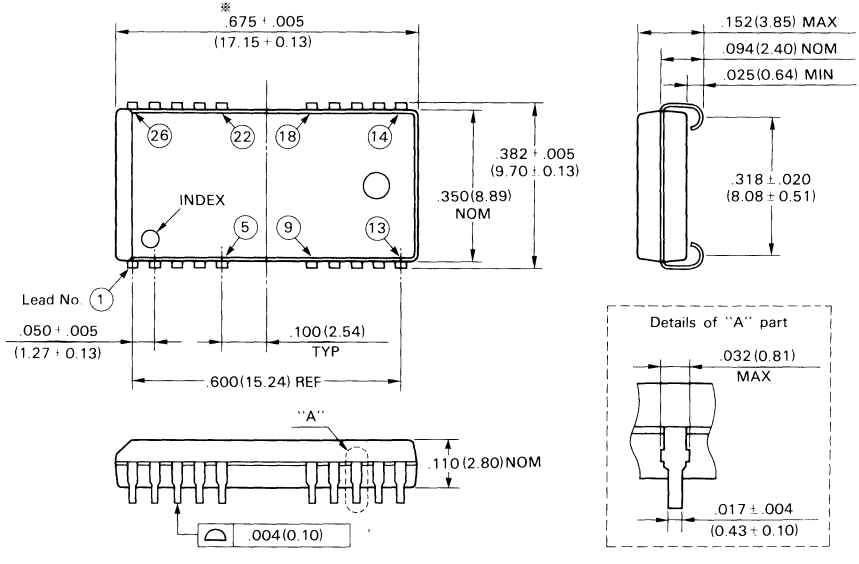
NOTE: 1. ※: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", (LCC-26C-A01)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-26P-M03)



※ Remaining Resin .006(0.15) MAX

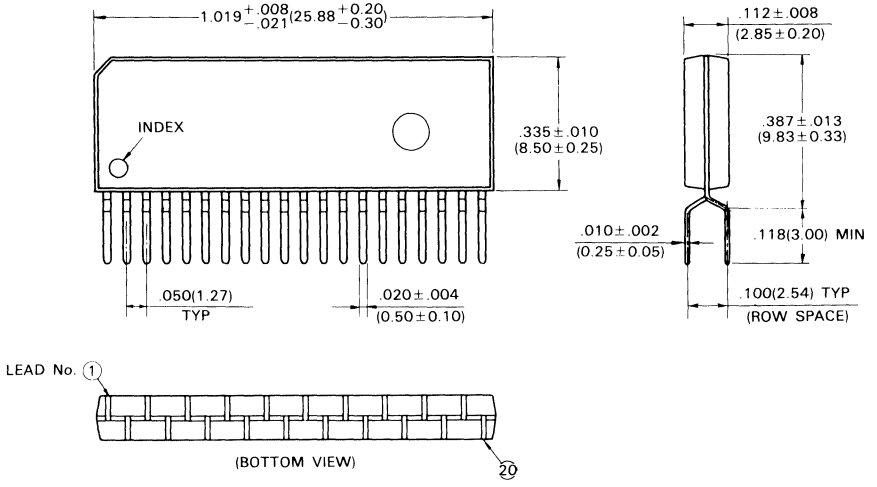
Dimensions in inches (millimeters).

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB814400-80/-10/-12

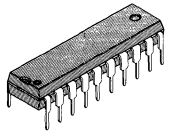
CMOS 4,194,304 BIT FAST PAGE MODE DYNAMIC RAM

CMOS 1,048,576 x 4 BIT Fast Page Mode Dynamic RAM

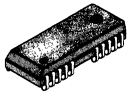
PRELIMINARY

The Fujitsu MB814400 is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 4-bit increments. The MB814400 features a "fast page" mode of operation whereby high-speed random access of up to 1,024-bits of data within the same row can be selected. The MB814400 DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB814400 is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

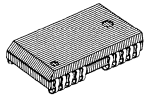
The MB814400 is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB814400 are not critical and all inputs are TTL compatible.



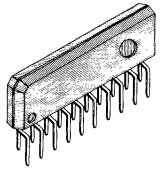
DIP-20P-M03



LCC-26P-M04



LCC-26P-M03



ZIP-20P-M02

PRODUCT LINE & FEATURES

Parameter	MB814400-80	MB814400-10	MB814400-12
$\overline{RAS}$ Access Time	80ns max.	100ns max.	120ns max.
Randam Cycle Time	155ns min.	180ns min.	210ns min.
Address Access Time	45ns max.	50ns max.	60ns max.
$\overline{CAS}$ Access Time	25ns max.	30ns max.	35ns max.
Fast Page Mode Cycle Time	55ns min.	60ns min.	70ns min.
Low Power Dissipation • Operating current	413mW max.	358mW max.	303mW max.
• Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)		

- 1,048,576 words x 4 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 1024 refresh cycles every 16.4ms
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

ABSOLUTE MAXIMUM RATINGS (see NOTE)

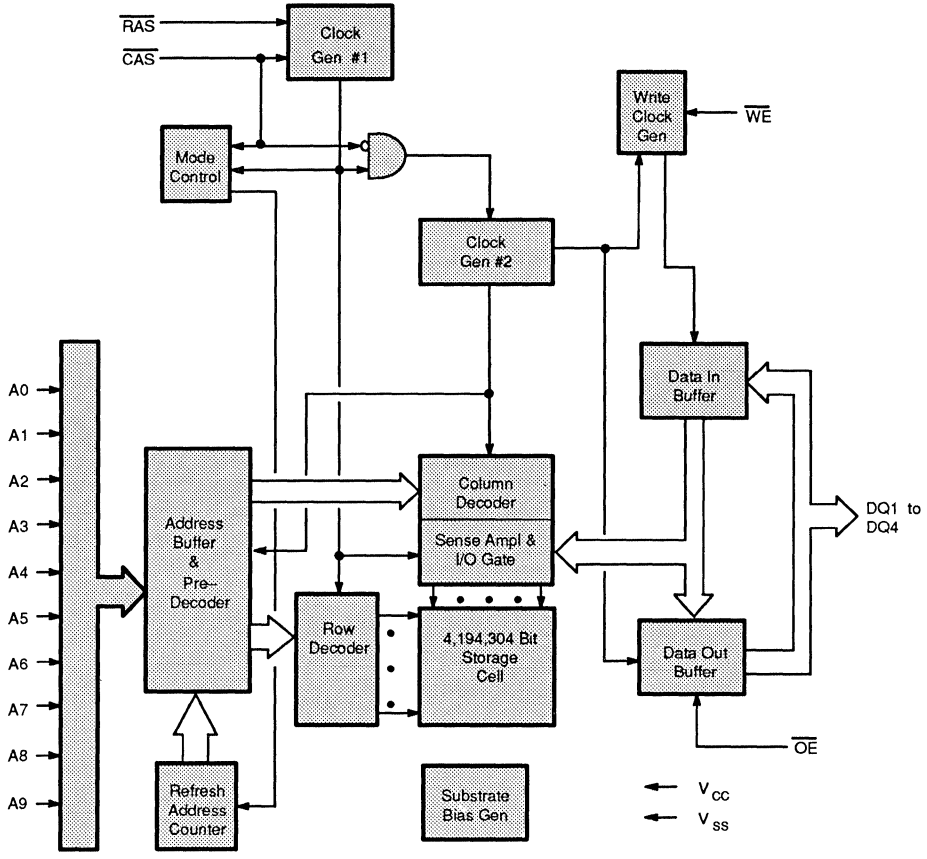
Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	-1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB814400 DYNAMIC RAM – BLOCK DIAGRAM

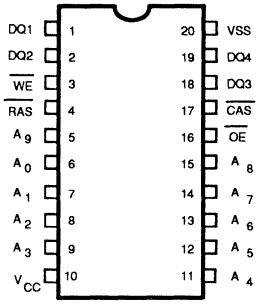


CAPACITANCE (T_A = 25°C, f = 1MHz)

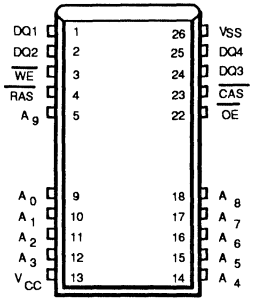
Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	5	pF
Input/Output Capacitance, DQ1 to DQ4	C_{DQ}	—	6	pF

PIN ASSIGNMENTS AND DESCRIPTIONS

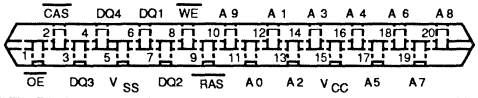
20–Pin DIP:
(TOP VIEW)



26–Pin SOJ:
(TOP VIEW)



20–Pin ZIP:
(TOP VIEW)



Designator	Function
DQ1 to DQ4	Data Input/ Output
$\overline{WE}$	Write Enable.
$\overline{RAS}$	Row address strobe.
A0 to A9	Address inputs.
VCC	+5 volt power supply.
$\overline{OE}$	Output enable.
$\overline{CAS}$	Column address strobe.
VSS	Circuit ground.

2

RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0 °C to +70 °C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	1	VIH	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	VIL	–2.0	—	0.8	V	
Input Low Voltage, DQ(*)	1	VILD	–1.0	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any four of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 1. First, ten row address bits are input on pins A0–through–A9 and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow–through type; thus, address information appearing after t_{RAH} (min)+ t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read–modify–write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data–latch strobe. In an early write cycle, the input data (DQ1–DQ4) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read–modify–write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write–enable signal.

DATA OUTPUT

The three–state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high–impedance state until the column address strobe goes Low. When a read or read–modify–write cycle is executed, valid outputs are obtained under the following conditions:

t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied.

t_{CAC} : from the falling edge of $\overline{CAS}$ when t_{RCD} is greater than t_{RCD} (max).

t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max).

t_{OEA} : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}

The data remains valid until either $\overline{CAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high–impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024–bits can be accessed and, when multiple MB 814400s are used, $\overline{CAS}$ is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready–modify–write cycles are permitted.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted) Notes 3

Paramter	Notes	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit
Output high voltage		V_{OH}	I_{OH} = –5 mA	2.4	—	—	V
Output low voltage		V_{OL}	I_{OL} = 4.2 mA	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	0V≤V_{IN}≤ 5.5V; 4.5V≤V_{CC}≤ 5.5V; V_{SS} = 0V; All other pins not under test = 0V	–10	—	10	µA
Output leakage current		$I_{DQ(L)}$	0V≤V_{OUT}≤ 5.5V; Data out disabled	–10	—	10	
Operating current (Average Power supply current)	MB814400–80	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814400–10					65	
[2]	MB814400–12					55	
Standby current (Power supply current)	TTL level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ =V_{IH}	—	—	2.0	mA
	CMOS level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2V			1.0	
Refresh current #1 (Average power supply current) [2]	MB814400–80	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min	—	—	75	mA
	MB814400–10					65	
	MB814400–12					55	
Fast Page Mode current [2]	MB814400–80	I_{CC4}	$\overline{RAS}$ =VIL, $\overline{CAS}$ cycling; t_{PC} = min	—	—	75	mA
	MB814400–10					65	
	MB814400–12					55	
Refresh current #2 (Average power supply current) [2]	MB814400–80	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min	—	—	75	mA
	MB814400–10					65	
	MB814400–12					55	

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814400-80		MB814400-10		MB814400-12		Unit
				Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		t_{REF}	—	16.4	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t_{RC}	155	—	180	—	210	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	220	—	245	—	280	—	ns
4	Access Time from $\overline{RAS}$	6,9	t_{RAC}	—	80	—	100	—	120	ns
5	Access Time from $\overline{CAS}$	7,9	t_{CAC}	—	25	—	30	—	35	ns
6	Column Address Access Time	8,9	t_{AA}	—	45	—	50	—	60	ns
7	Output Hold Time		t_{OH}	5	—	5	—	5	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	5	—	5	—	5	—	ns
9	Output Buffer Turn off Delay Time	10	t_{OFF}	—	25	—	25	—	25	ns
10	Transition Time		t_T	3	50	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	65	—	70	—	80	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	80	100000	100	100000	120	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	25	—	30	—	35	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	t_{RCD}	22	55	25	70	25	85	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	25	—	30	—	35	—	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	80	—	100	—	120	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	t_{CPN}	15	—	15	—	15	—	ns
19	Row Address Set Up Time		t_{ASR}	0	—	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	12	—	15	—	15	—	ns
21	Column Address Set Up Time		t_{ASC}	0	—	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	15	—	15	—	20	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	t_{RAD}	17	35	20	50	20	60	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	—	50	—	60	—	ns
25	Read Command Set Up Time		t_{RCS}	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	t_{RRH}	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	t_{RCH}	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	t_{WCS}	0	—	0	—	0	—	ns
29	Write Command Hold Time		t_{WCH}	15	—	15	—	20	—	ns
30	$\overline{WE}$ Pulse Width		t_{WP}	15	—	15	—	20	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25	—	25	—	30	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20	—	20	—	25	—	ns
33	DIN set Up Time		t_{DS}	0	—	0	—	0	—	ns
34	DIN Hold Time		t_{DH}	15	—	15	—	20	—	ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB814400-80		MB814400-10		MB814400-12		Unit
				Min	Max	Min	Max	Min	Max	
35	$\overline{RAS}$ Precharge time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	0	—	0	—	0	—	ns
36	$\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	0	—	ns
37	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15	—	15	—	20	—	ns
38	$\overline{WE}$ Set Up Time from $\overline{RAS}$		t_{WSR}	0	—	0	—	0	—	ns
39	$\overline{WE}$ Hold Time from $\overline{RAS}$		t_{WHR}	15	—	15	—	20	—	ns
40	Access Time from $\overline{OE}$	9	t_{OEA}	—	22	—	25	—	30	ns
41	Output Buffer Turn Off Delay from $\overline{OE}$	10	t_{OEZ}	—	25	—	25	—	25	ns
42	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	10	—	ns
43	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	16	t_{OEH}	0	—	0	—	0	—	ns
44	$\overline{OE}$ to Data In Delay Time		t_{OED}	25	—	25	—	25	—	ns
45	DIN to $\overline{CAS}$ Delay Time	17	t_{DZC}	0	—	0	—	0	—	ns
46	DIN to $\overline{OE}$ Delay Time	17	t_{DZO}	0	—	0	—	0	—	ns
50	Fast Page Mode Read/Write Cycle Time		t_{PC}	55	—	60	—	70	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	120	—	125	—	140	—	ns
52	Access Time from $\overline{CAS}$ Precharge	9,18	t_{CPA}	—	55	—	60	—	70	ns
53	Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15	—	15	—	15	—	ns

Notes:

1. Referenced to VSS.
2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, V_{IL} > -0.5V.
   I_{CC1}, I_{CC3} and I_{CC5} are specified at three time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
   I_{CC4} is specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200μs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume t_T = 5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min) and V_{IL} (max).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
8. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
9. Measured with a load equivalent to two TTL loads and 100 pF.
10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min).
17. Either t_{DZC} or t_{DZO} must be satisfied.
18. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max).
19. Assuemes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Fig. 2 – t_{RAC} vs. t_{RCD}

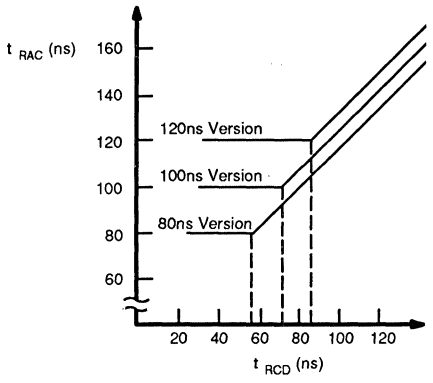
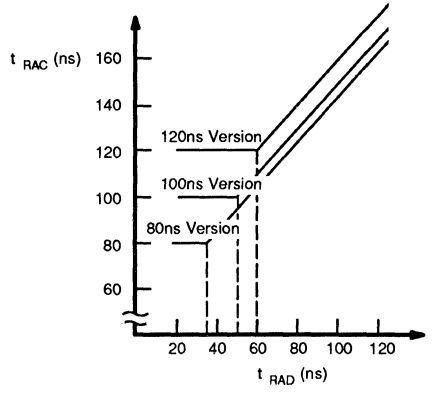


Fig. 3 – t_{RAC} vs. t_{RAD}

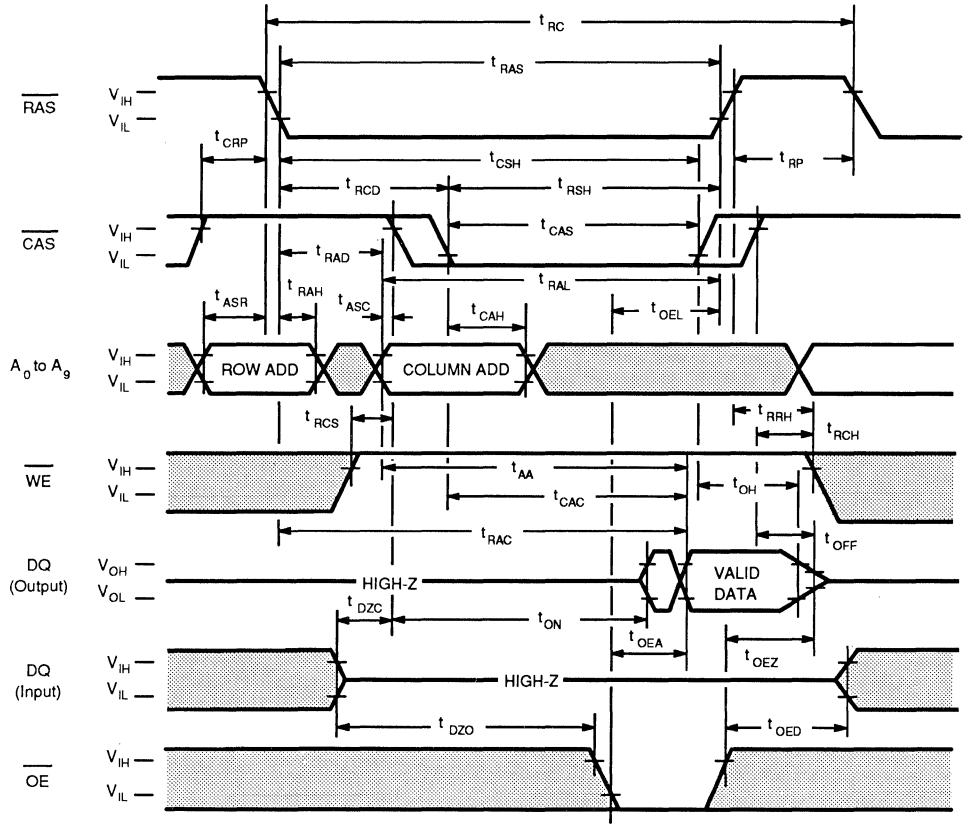


FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High–Z	—	
Read Cycle	L	L	H	L	Valid	Valid	—	Valid	O *	$t_{RCS} \geq t_{RCS}$ (min)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High–Z	O *	$t_{WCS} \geq t_{WCS}$ (min)
Read–Modify–Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	O *	
$\overline{RAS}$–only Refresh Cycle	L	H	X	X	Valid	—	—	High–Z	O	
$\overline{CAS}$–before–$\overline{RAS}$ Refresh Cycle	L	L	H	X	—	—	—	High–Z	O	$t_{CSR} \geq t_{WCSR}$ (min)
Hidden Refresh Cycle	H→L	L	H	L	—	—	—	Valid	O	Previous data is kept.

X; "H" or "L"
*; It is impossible in Fast Page Mode

Fig. 4 – READ CYCLE



DESCRIPTION

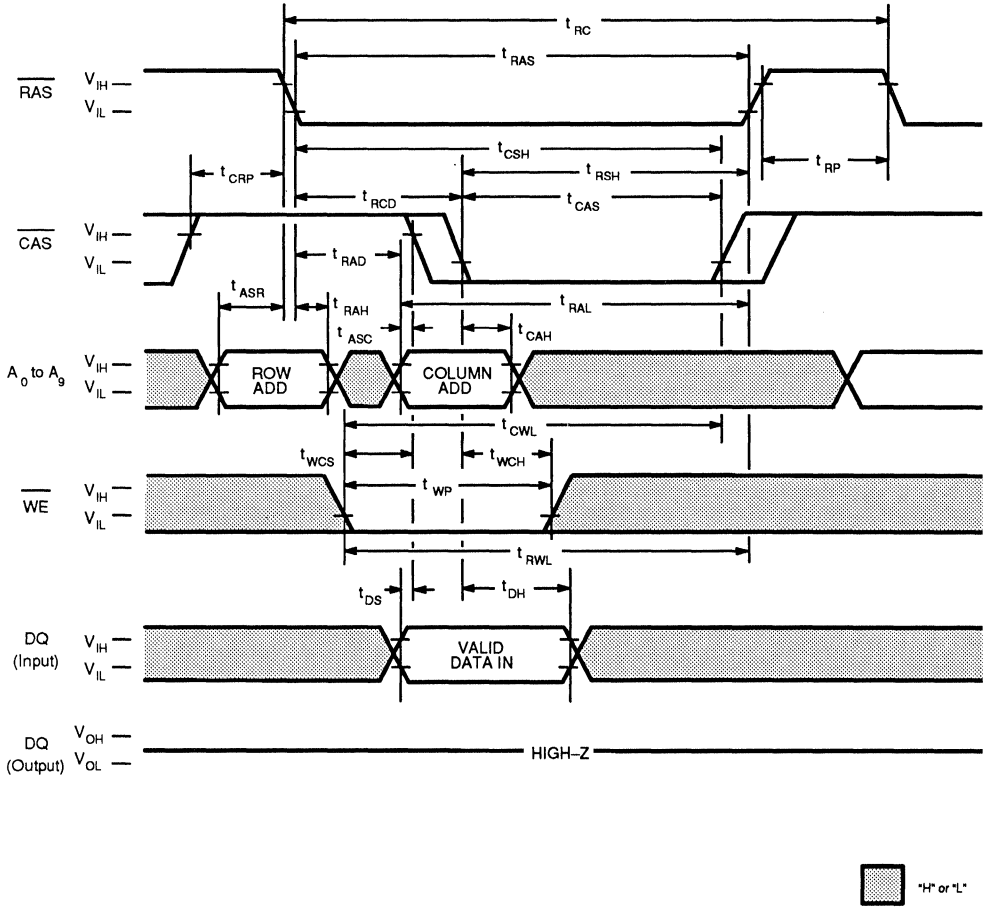
To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and, with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), $\overline{OE}$, (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

- If $t_{RCD} > t_{RCD}$ (max), access time = t_{CAC}.
- If $t_{RAD} > t_{RAD}$ (max), access time = t_{AA}.
- If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (which ever occurs later), access time = t_{OEA}.

However, if either $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

2

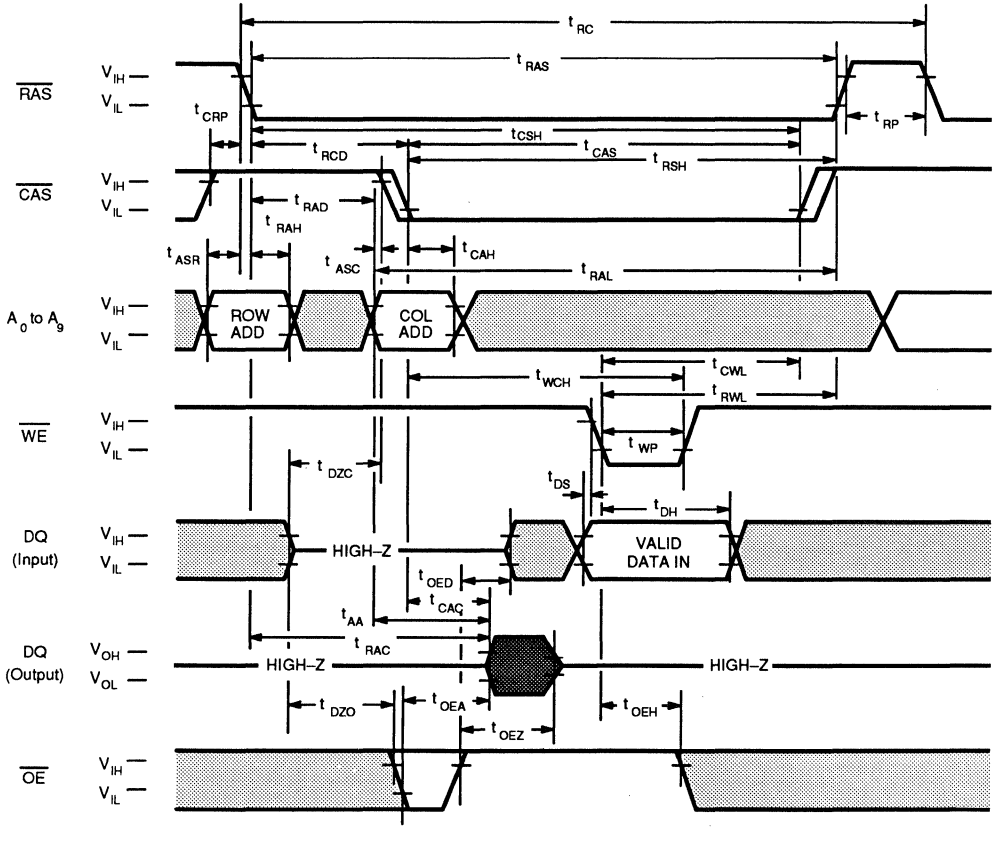
Fig. 5 — EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is a "H" or "L" signal. A write cycle can be implemented in either of three ways — early write, $\overline{OE}$ write (delayed write), or read–modify–write. During all write cycles, timing parameters t_{RWL}, t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins is latched with the falling edge of $\overline{CAS}$ and written into memory.

Fig. 6 — $\overline{OE}$ (DELAYED WRITE CYCLE)

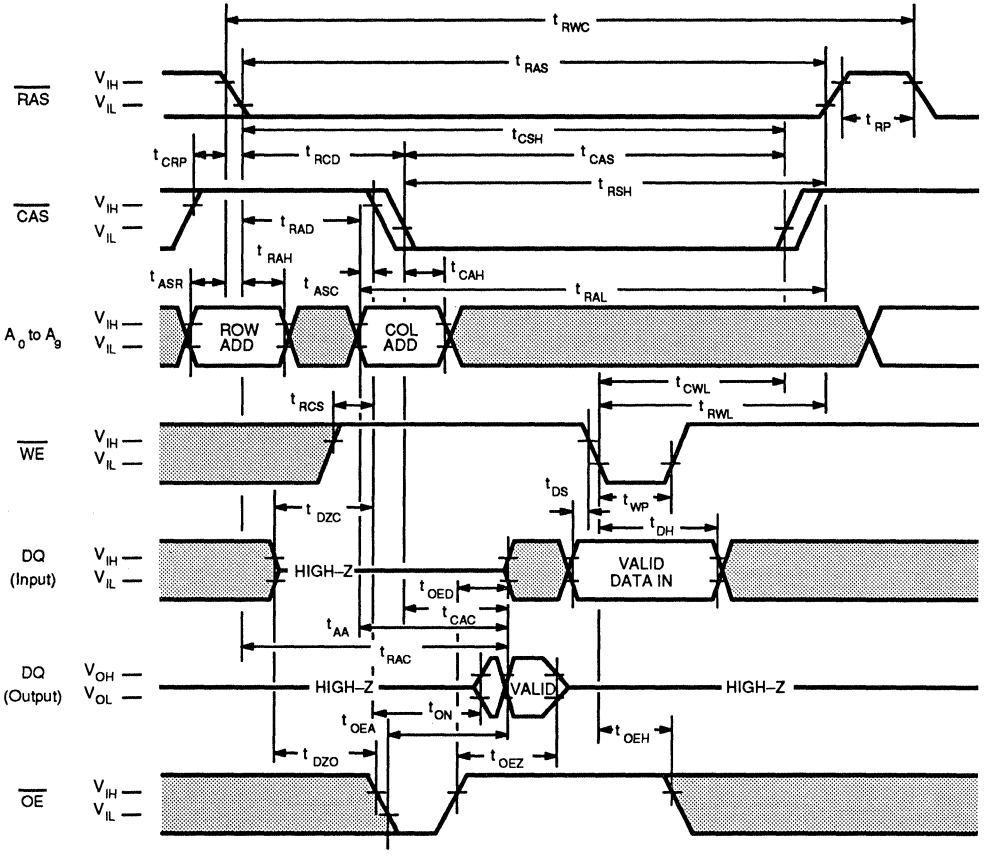


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

2

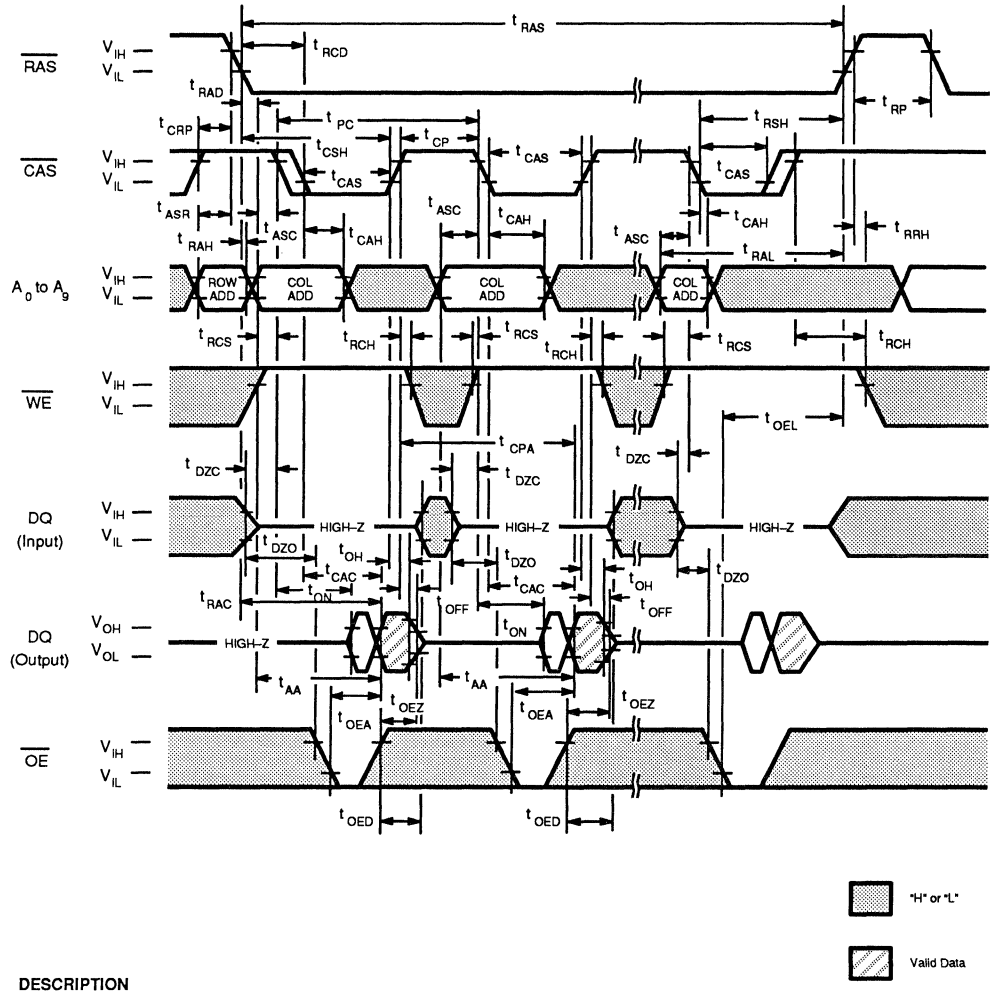
Fig. 7 — READ–MODIFY–WRITE–CYCLE



DESCRIPTION

The read–modify–write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read–modify–write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 8 – FAST PAGE MODE READ CYCLE

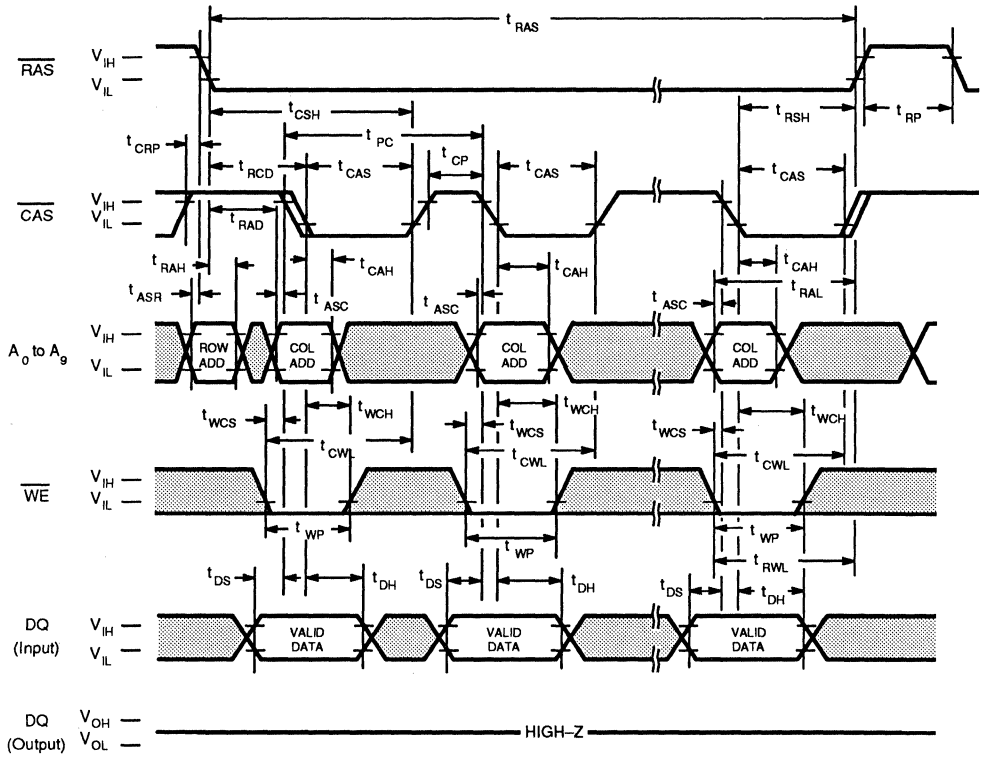


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occuring.

2

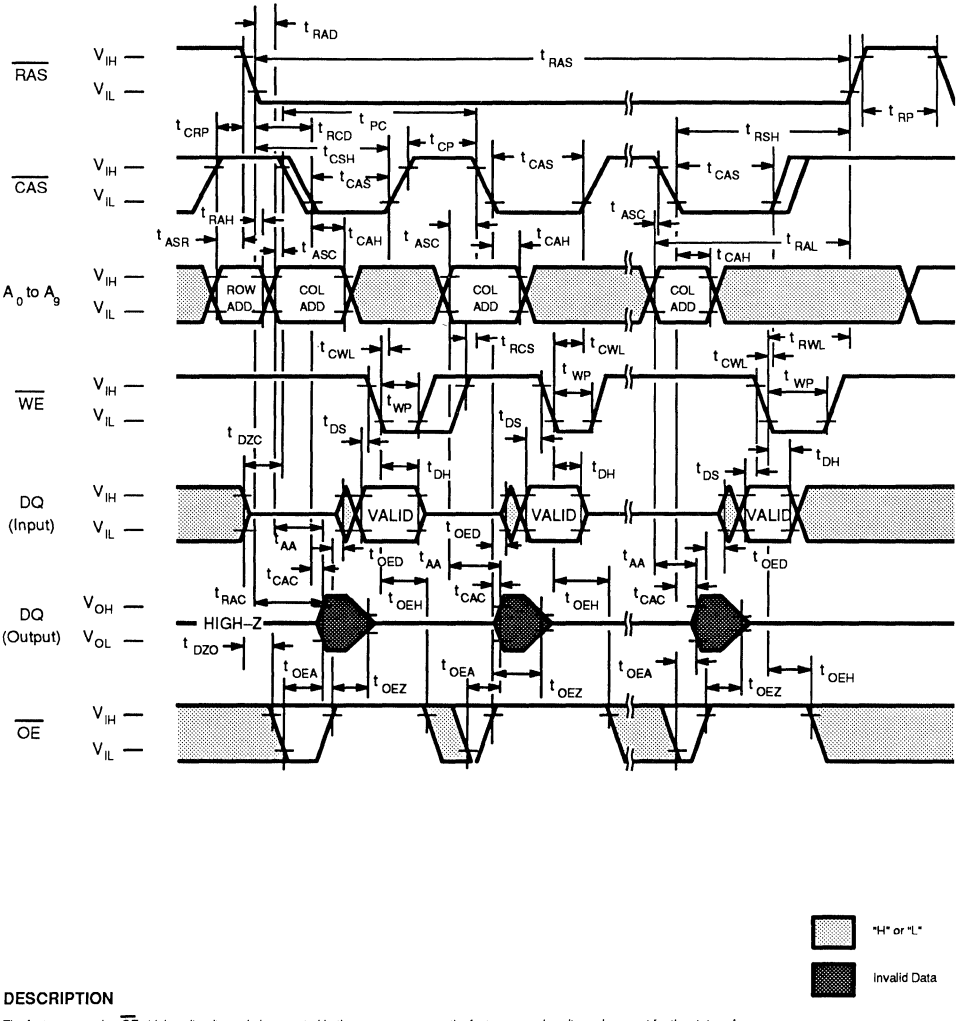
Fig. 9 — FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and written into memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read–modify–write cycles, t_{CWL} must be satisfied.

Fig. 10 — FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

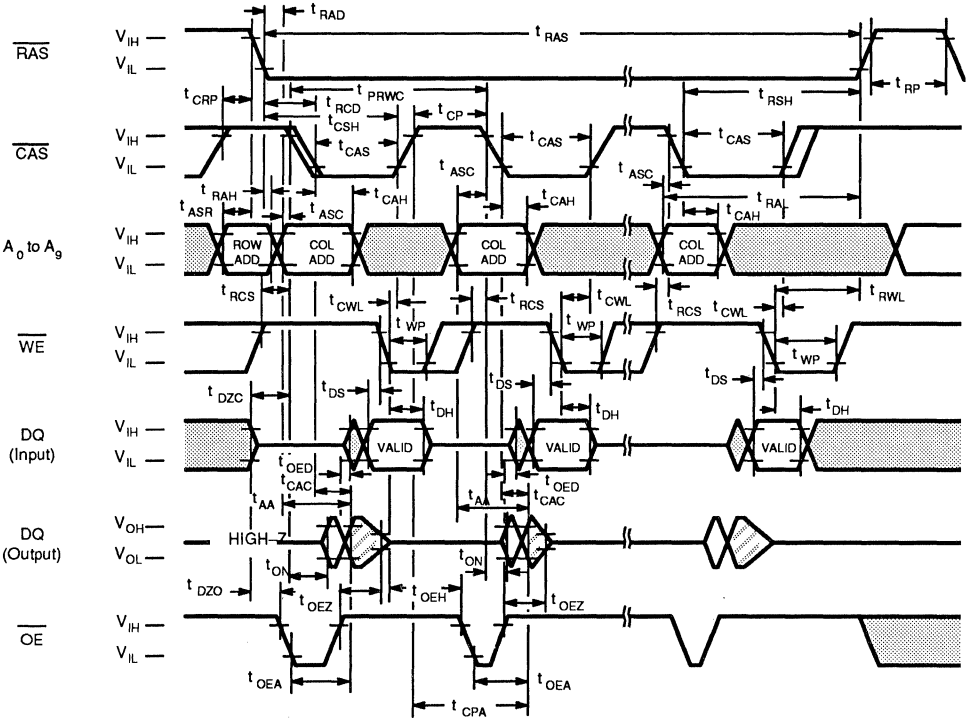


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

2

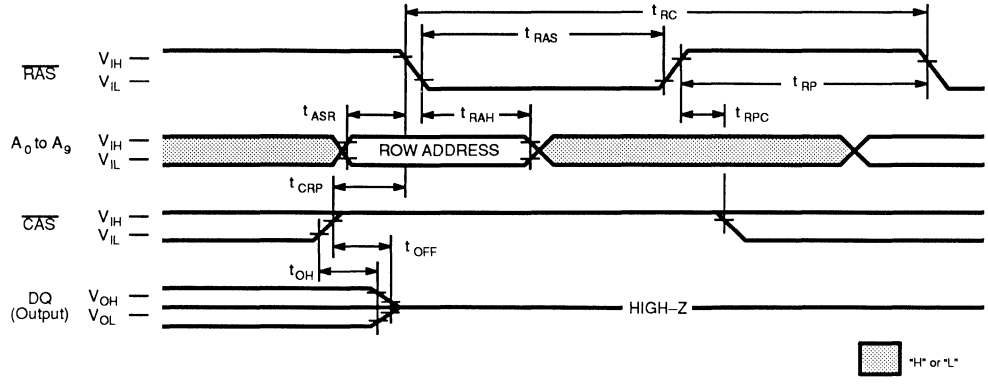
Fig. 11 – FAST PAGE MODE READ–MODIFY–WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read–modify–write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 12 — $\overline{RAS}$–ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

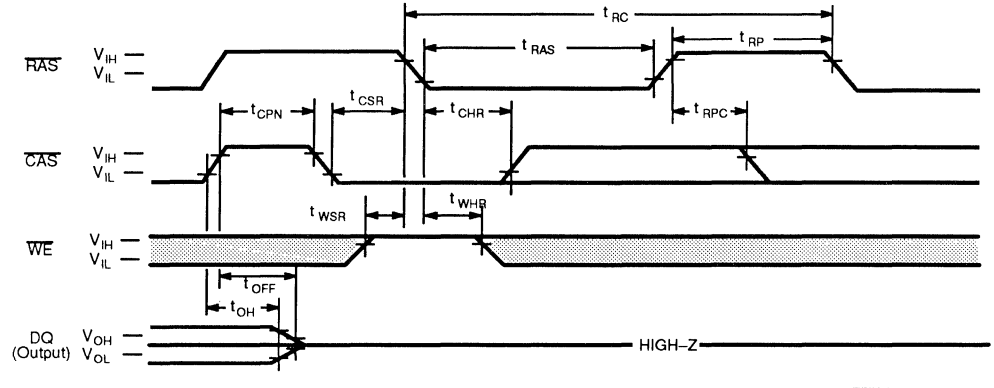


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read–modify–write cycle at each of 1024 row addresses every 16.4–milliseconds. Three refresh modes are available: $\overline{RAS}$ –only refresh, $\overline{CAS}$ –before–$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$–only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$–only refresh, DQ pins are kept in a high–impedance state.

Fig. 13 — $\overline{CAS}$–BEFORE–$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{OE}$ = "H " or "L")



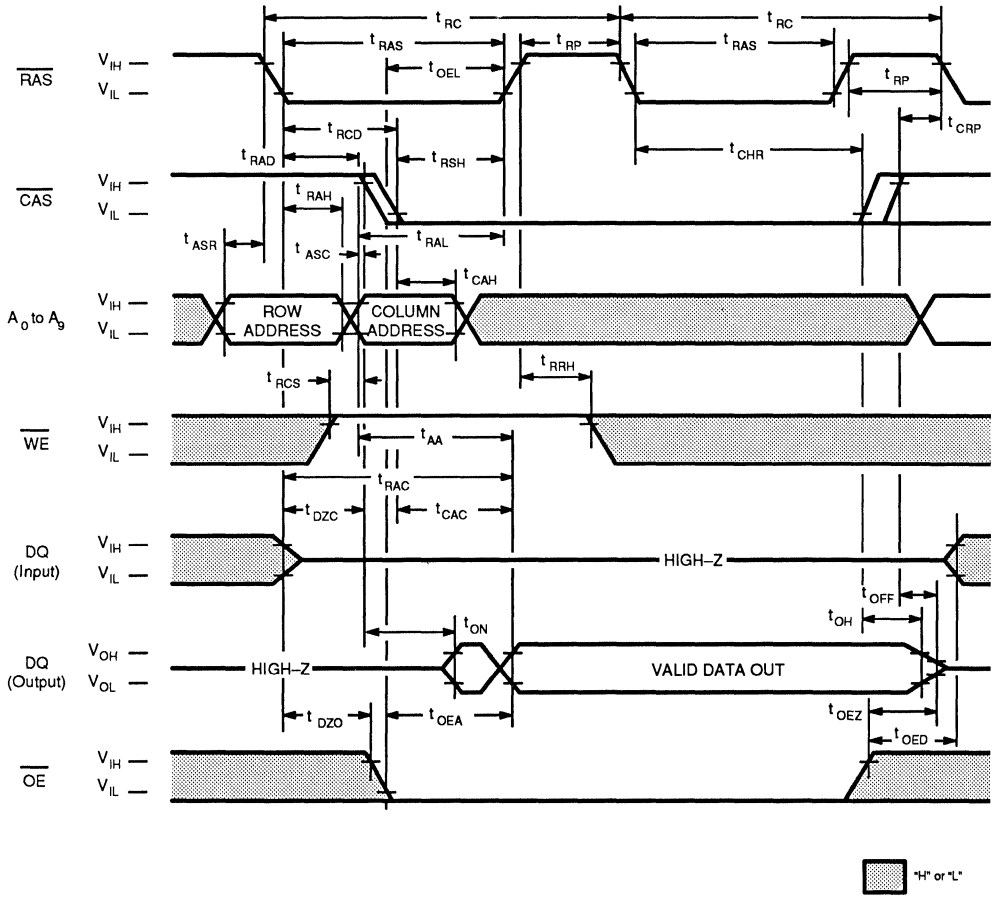
DESCRIPTION

$\overline{CAS}$–before–$\overline{RAS}$ refresh is an on–chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on–chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$ –before–$\overline{RAS}$ refresh operation .

$\overline{WE}$ must be held High for the specified set up time (tWSR) before RAS goes Low in order not to enter "test mode" to be specified later.

2

Fig. 14 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

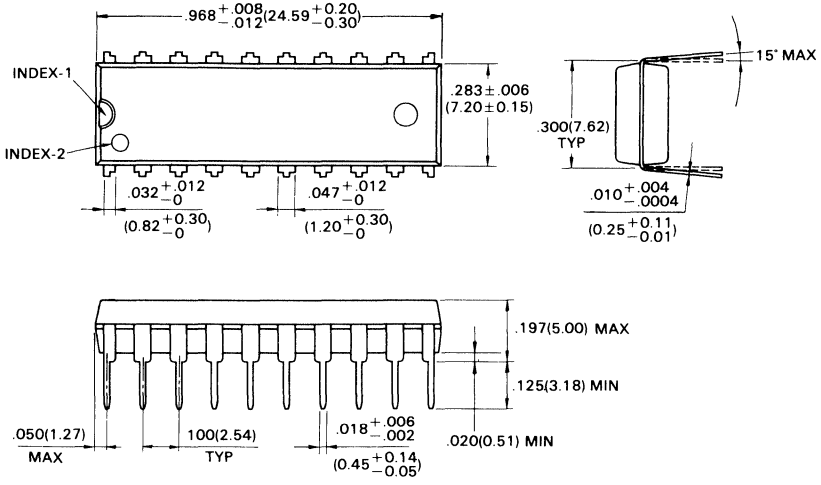
$\overline{WE}$ must be held High for the specified set up time (tWSR) before RAS goes Low in order not to enter "test mode" to be specified later.

PACKAGE DIMENSIONS

(Suffix : –P)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M03)



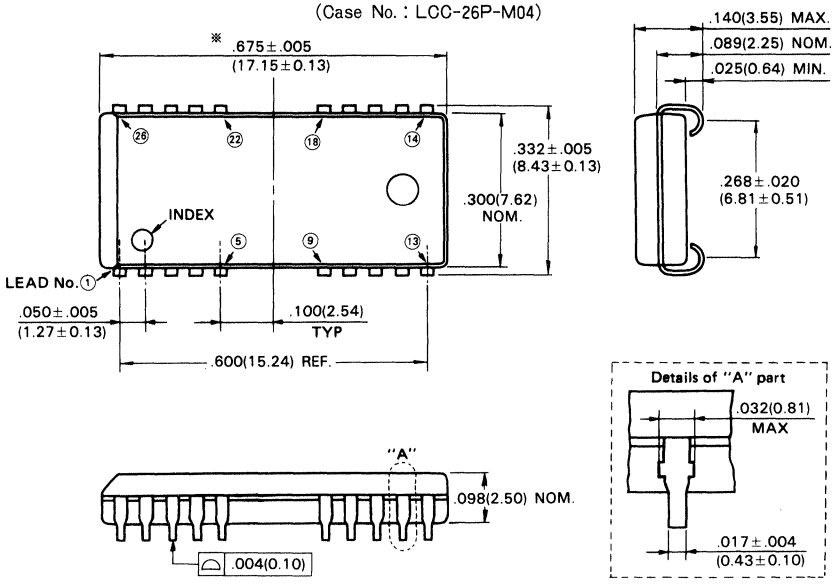
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJN)

26-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-26P-M04)



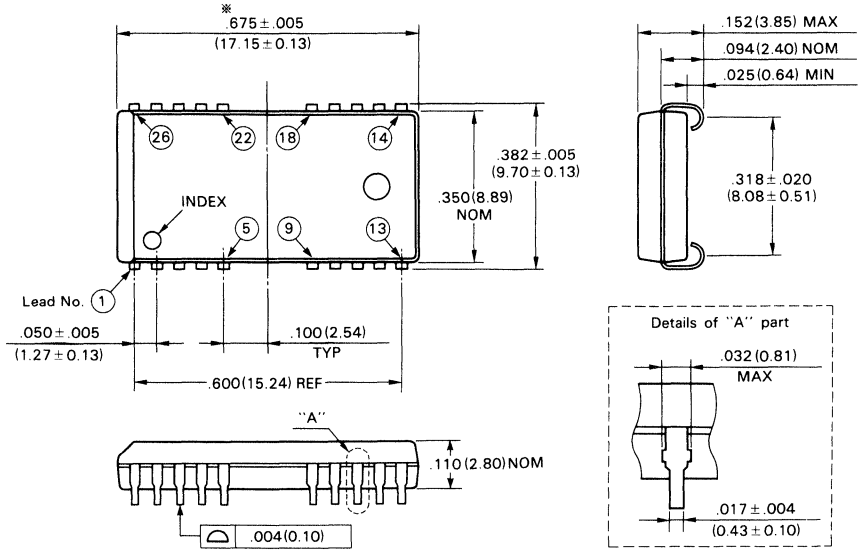
NOTE: 1. ※: This dimension includes resin protrusion. (Each side: .006(0.15)MAX)
2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package. Foot-print compatible with "SOJ-26", (LCC-26C-A01)

PACKAGE DIMENSIONS (Continued)

(Suffix : –PJ)

26-LEAD PLASTIC LEADED CHIP CARRIER

(Case No. : LCC-26P-M03)



※ Remaining Resin .006(0.15) MAX

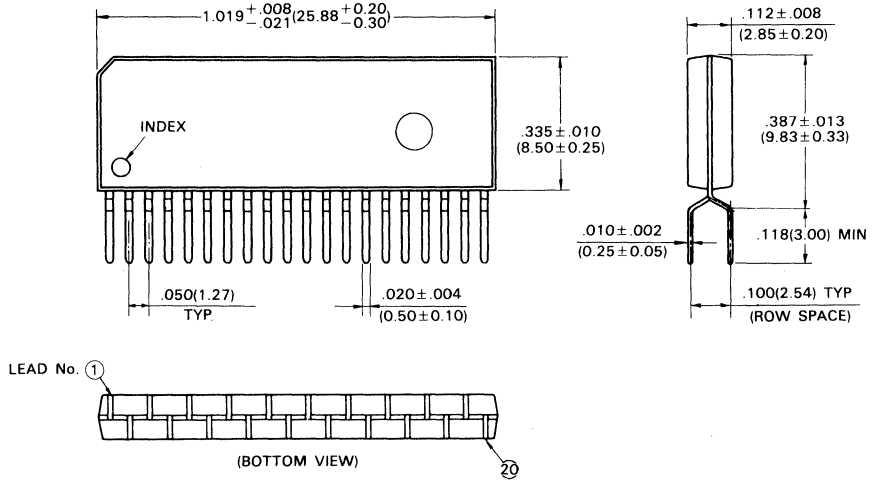
Dimensions in inches (millimeters).

PACKAGE DIMENSIONS (Continued)

(Suffix : –PSZ)

20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-20P-M02)



Dimensions in
inches (millimeters)

Section 3

Application Specific DRAMs — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
3–3	MB81461–12 –15	120 150	DRAM: 262144 bits (65536w x 4b) SAM: 1016 bits (256w x 4b)	24-pin Plastic DIP, ZIP
3–35	MB81461B–12 –15	120 150	DRAM: 262144 bits (65536w x 4b) SAM: 1016 bits (256w x 4b)	24-pin Plastic DIP, ZIP
3–67	MB81C4251–10 –12 –15	100 120 150	DRAM: 1048576 bits (262144w x 4b) SAM: 2048 bits (512w x 4b)	28-pin Plastic DIP, ZIP 28-pin Plastic LCC
3–69	MB81C4253–10 –12 –15	100 120 150	DRAM: 1048576 bits (262144w x 4b) SAM: 2048 bits (512w x 4b)	28-pin Plastic DIP, ZIP 28-pin Plastic LCC
3–71	MB81C1501	25	Read: 2350080 bits (293760w x 4b x 2) Write: 1175040 bits (293760w x 4b x 1)	38-pin Plastic FPT

3

FUJITSU

262144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

MB81461-12
MB81461-15

July 1987
Edition 3.0

262,144 BIT DUAL PORT DRAM

The Fujitsu MB 81461 is a fully decoded dual port NMOS dynamic random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

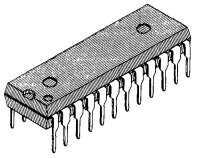
The DRAM port is identical to the Fujitsu MB 81464 with four bits parallel random access I/O while the SAM port is designed as four 256 bit registers each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

The MB 81461 offers complementely asynchronous access of both the DRAM and SAM ports except when data is transfered between them internally.

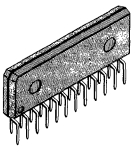
The design is optimized for high speed and performance which makes the MB 81461 the most efficient solution for implementing the frame buffer of a bit mapped video display system. Multiplexed row and column address inputs permit the MB 81461 to be housed in a 400 mil wide 24 pin DIP and ZIP. Pin outs conformed to the JEDEC approved pin out.

The MB 81461 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple Layer Polysilicon process technology. This process coupled with single transistor memory storage cells permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible.

- Dual port organization
  64K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24 pin DIP and ZIP package
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  - Access Time (t_{RAC}),
    120ns max. (MB 81461-12)
    150ns max. (MB 81461-15)
  - Cycle Time (t_{RC}),
    230ns min. (MB 81461-12)
    260ns min. (MB 81461-15)
- SAM Port
  - Access Time (t_{SAC}),
    40 ns max. (MB 81461-12)
    60 ns max. (MB 81461-15)
  - Cycle Time (t_{SC}),
    40ns min. (MB 81461-12)
    60ns min. (MB 81461-15)
- Single +5V power supply, ±10% tolerance
- Power Dissipation
  - DRAM; Act/SAM; Stby
    523mW max. (MB 81461-12)
    468mW max. (MB 81461-15)
  - DRAM; Stby/SAM; Act
    275mW max. (MB 81461-12)
    220mW max. (MB 81461-15)
  - DRAM; Stby/SAM; Stby
    110mW max.
- Bi-directional Data Transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Real Time Read Transfer Capability
- Page Mode capability
- Bit Masked Write Mode capability
- 256 refresh cycles every 4ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24 pin plastic DIP (Suffix; -P)
- Standard 24 pin plastic ZIP (Suffix; -PSZ)

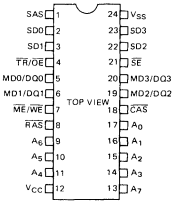


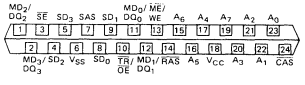
PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT





BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

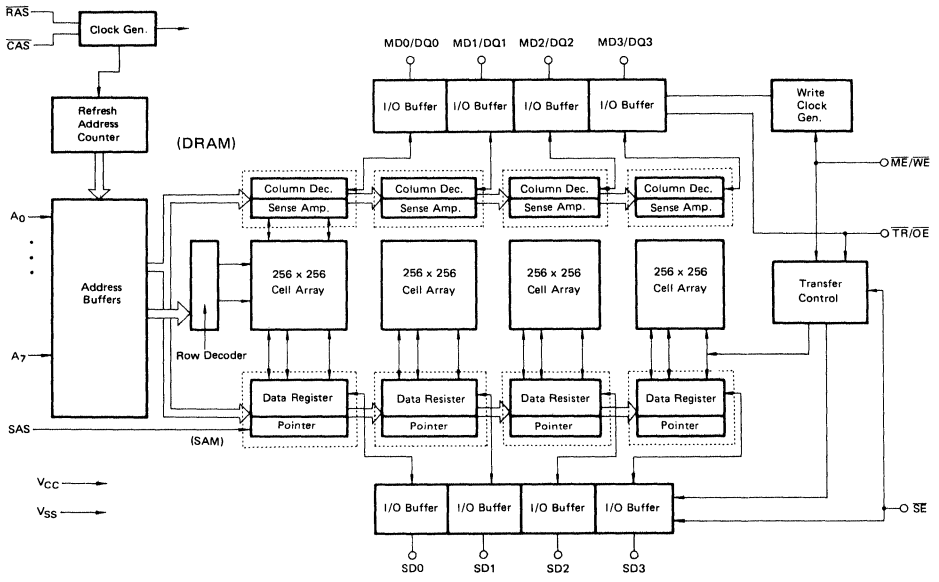
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

3

Fig. 1 – BLOCK DIAGRAM OF MB 81461 and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

$\overline{RAS}$;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$ and bit mask write cycle or not (by $\overline{ME}/\overline{WE}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, to maintain $\overline{RAS}$ = "H" (standby condition) is effective to save power dissipation.

$\overline{CAS}$;

This pin is used to strobe eight column address inputs at the falling edge. $\overline{CAS}$ pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.

Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{WE}$ = "L".

$\overline{ME}/\overline{WE}$;

This pin is used to select read or write cycle. $\overline{ME}/\overline{WE}$ = "L" select write mode and $\overline{ME}/\overline{WE}$ = "H" select read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;

This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.

The $\overline{TR}/\overline{OE}$ controls the impedance of the output buffers. $\overline{TR}/\overline{OE}$ = "H" forces the output buffers at high impedance state. $\overline{TR}/\overline{OE}$ = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if $\overline{TR}/\overline{OE}$ is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB 81461. The eight row address inputs are strobed by $\overline{RAS}$ and followed eight column address inputs are strobed by $\overline{CAS}$. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.

In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by $\overline{CAS}$ while $\overline{RAS}$ is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of $\overline{RAS}$ falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.

The MB 81461 offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$="H" condition. Strobing every 256 row addresses with $\overline{RAS}$ will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further $\overline{RAS}$-only refresh saves the power dissipation substantially.
2) $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of $\overline{RAS}$, for example, if MD0/DQ0 and $\overline{ME}/\overline{WE}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of $\overline{RAS}$						Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$	$\overline{TR}/\overline{OE}$	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H → X → H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	$\overline{RAS}$-Only Refresh
H→L	L	X	H→X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

*: If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write mode is enabled.

TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of $\overline{ME}/\overline{WE}$ at the falling edge of $\overline{RAS}$. $\overline{ME}/\overline{WE}$="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and $\overline{ME}/\overline{WE}$="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set ($\overline{TR}/\overline{OE}$="L") conjunctioned with $\overline{ME}/\overline{WE}$ state.

After Read Transfer Cycle, please apply two or more SAS Clock.

$\overline{TR}/\overline{OE}$;

This pin is used to enable transfer operation at the falling edge of $\overline{RAS}$.

$\overline{ME}/\overline{WE}$;

This pin is used to select the direction of transfer at the falling edge of $\overline{RAS}$.

A0 to A7;

These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by $\overline{RAS}$ and the start address is strobed by $\overline{CAS}$.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461 has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under $\overline{SE}$="L" condition, and $\overline{SE}$="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, out-

put data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation by bit to bit. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" leads SD pins to "High-Z" state. $\overline{SE}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{TR}/\overline{OE}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{TR}/\overline{OE}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{TR}/\overline{OE}$.

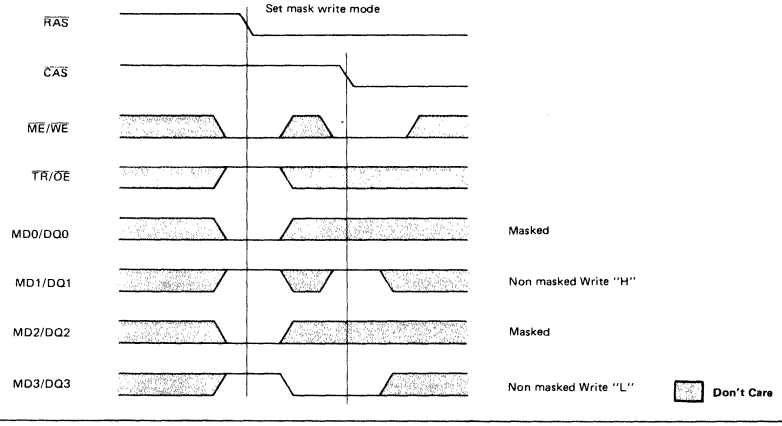
FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$		SAS	$\overline{SE}$	SD0 to SD3	Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

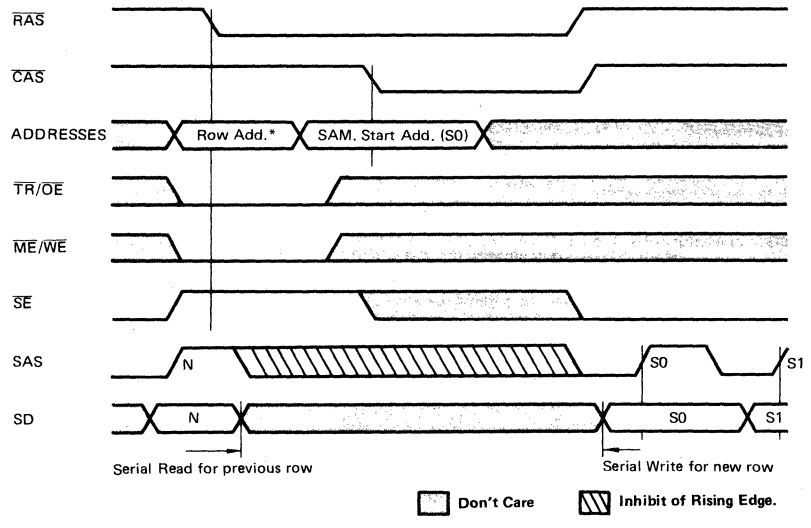
X; Don't Care

Fig. 2 – EXAMPLE OF BIT MASK WRITE OPERATION



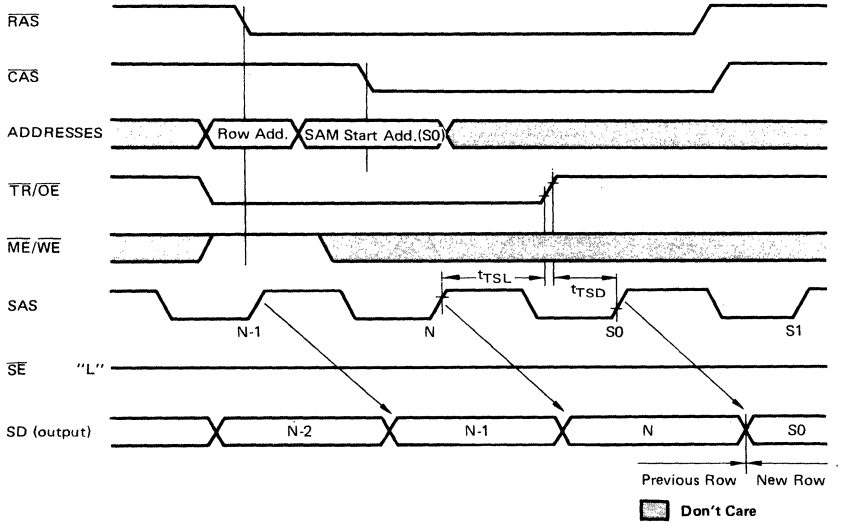
3

Fig. 3 – EXAMPLE OF PSEUDO WRITE TRANSFER CYCLE



*The DRAM data of this row address are refreshed during pseudo write transfer cycle.

Fig. 4 – EXAMPLE OF REAL TIME READ TRNASFER OPERATION



RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

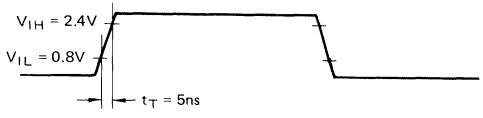
Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

CAPACITANCE (T_A=25°C)

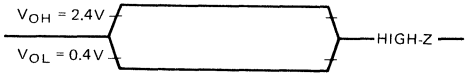
Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{SE}$, $\overline{TR}$/$\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

AC TEST CONDITIONS

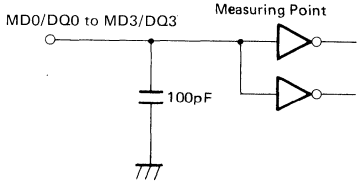
1) Input

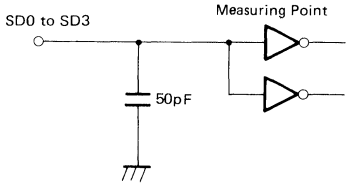


2) Output



3) Output Load





DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE}$ = V_{IH}, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC1}		95	mA
	MB 81461-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC3}		77	mA
	MB 81461-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461-12	I_{CC4}		50	mA
	MB 81461-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC5}		77	mA
	MB 81461-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC6}		110	mA
	MB 81461-15			100	
SAM ACTIVE $\overline{SE}$ = V_{IL}, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC7}		130	mA
	MB 81461-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MB 81461-12	I_{CC8}		50	mA
	MB 81461-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC9}		112	mA
	MB 81461-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461-12	I_{CC10}		85	mA
	MB 81461-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461-12	I_{CC11}		112	mA
	MB 81461-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461-12	I_{CC12}		145	mA
	MB 81461-15			125	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1 2 3

Parameter	NOTES	Symbol	MB 81461-12		BM 81461-15		Unit
			Min	Max	Min	Max	
Time between Refresh (RAM/SAM)		t_{REF}		4		4	ms
Random Read/Write Cycle Time		t_{RC}	230		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	305		345		ns
Page Mode Cycle Time		t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	25	0	35	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60		75		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)		t_{CPR}	25		30		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	60000	75	60000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{TR}/\overline{OE}$	6	t_{OEA}		35		40	ns
$\overline{TR}/\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$		t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time		t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time	16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	20		20		ns
Serial Clock Cycle Time		t_{SC}	40	50000	60	50000	ns
Access Time from SAS	10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$	10	t_{SEA}		40		50	ns
SAS Precharge Time		t_{SP}	10		20		ns
SAS Pulse Width		t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time		t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width		t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High		t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$		t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time	11	t_{SDS}	0		0		ns
Serial Data In Hold Time	11	t_{SDH}	20		25		ns

3

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time		t_{TRL}	130		140		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Delay Time		t_{TRD}	-65		-50		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}/\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	13	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

AC CHARACTERISTICS

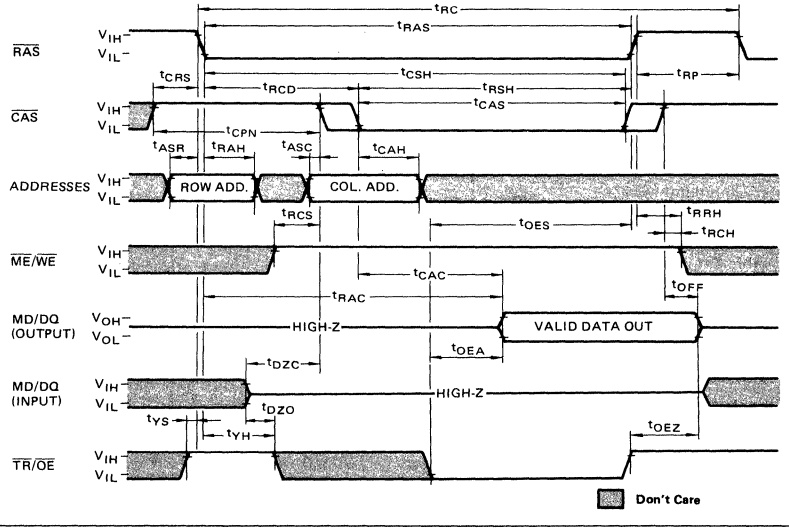
Parameter	NOTES	Symbol	MB 81461-12		MB 81461-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

NOTES;

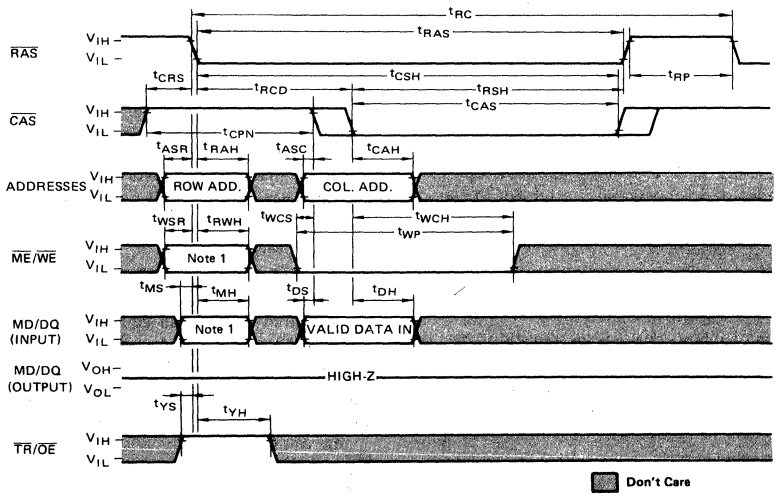
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycle are required
2. AC characteristics assume
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.

3

READ CYCLE

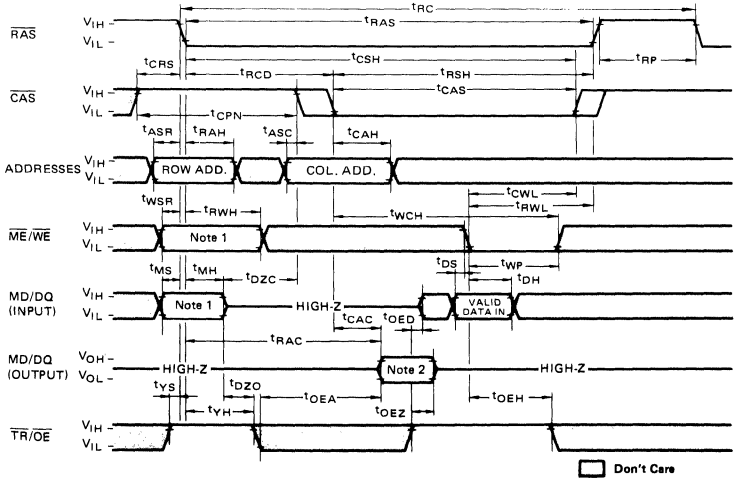


WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

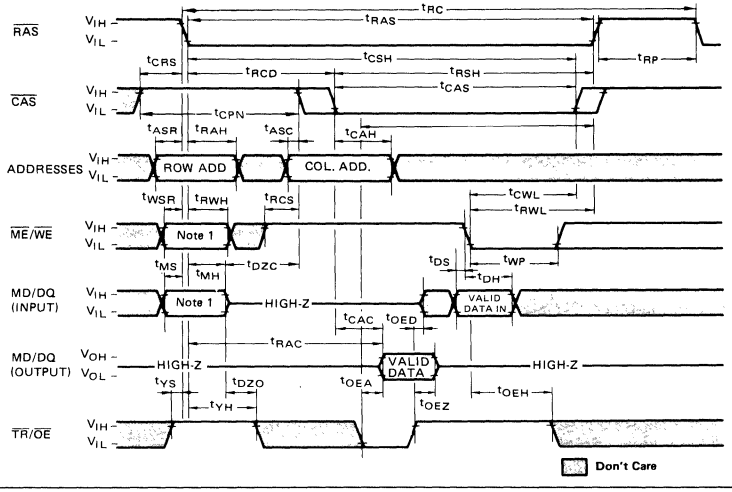
DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

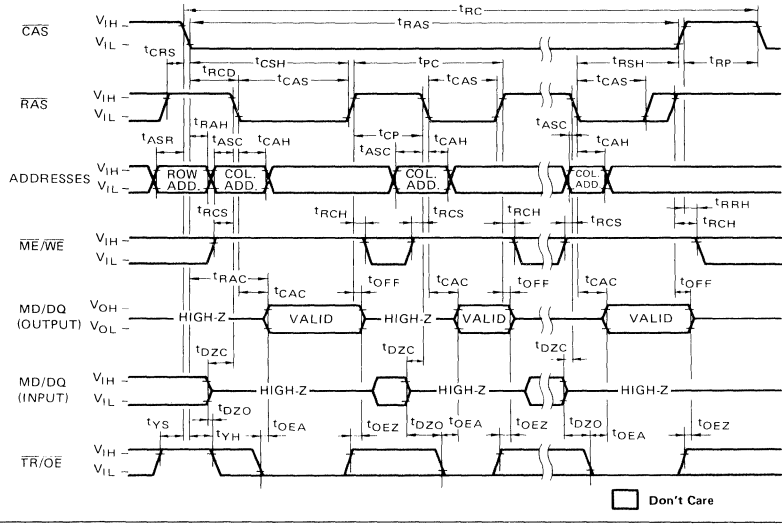
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

READ-MODIFY-WRITE CYCLE

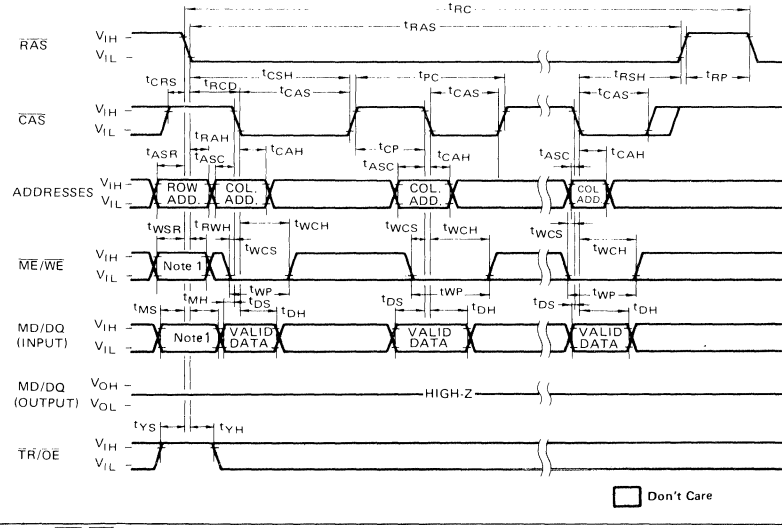


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

PAGE MODE READ CYCLE

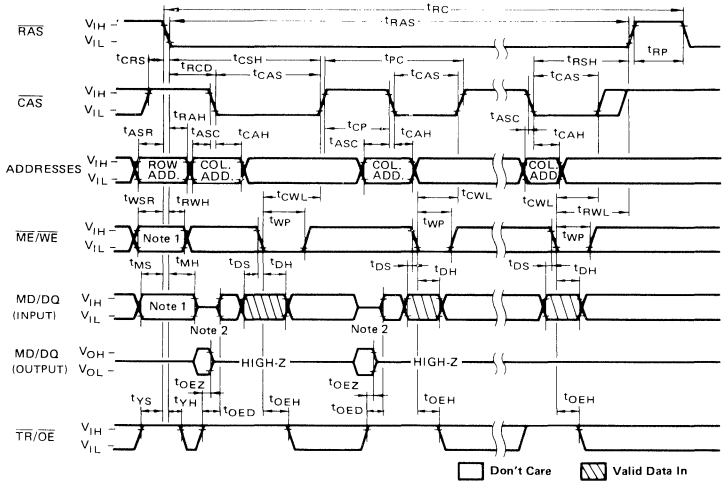


PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

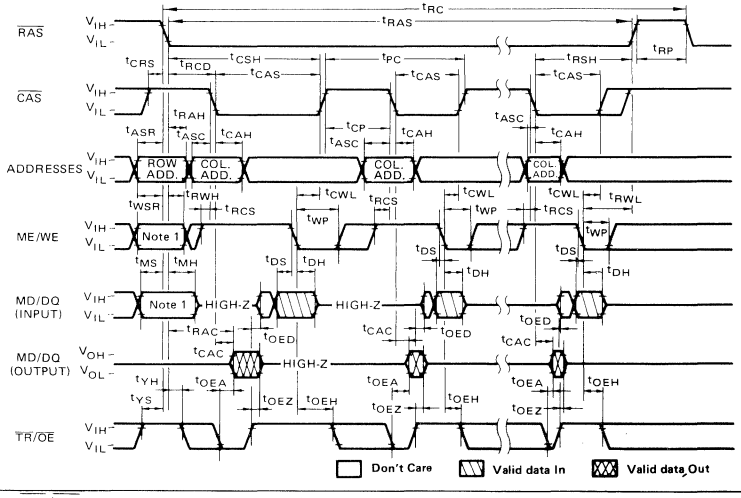
PAGE MODE DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

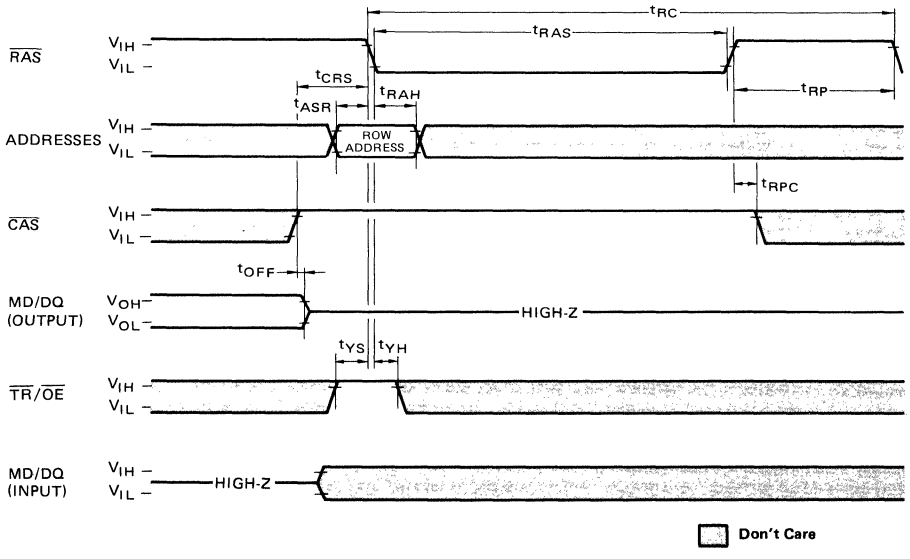
PAGE MODE READ-MODIFY-WRITE CYCLE



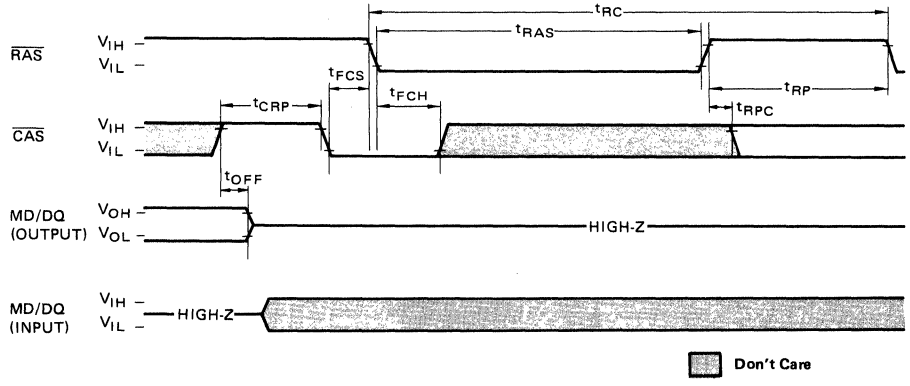
Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

3

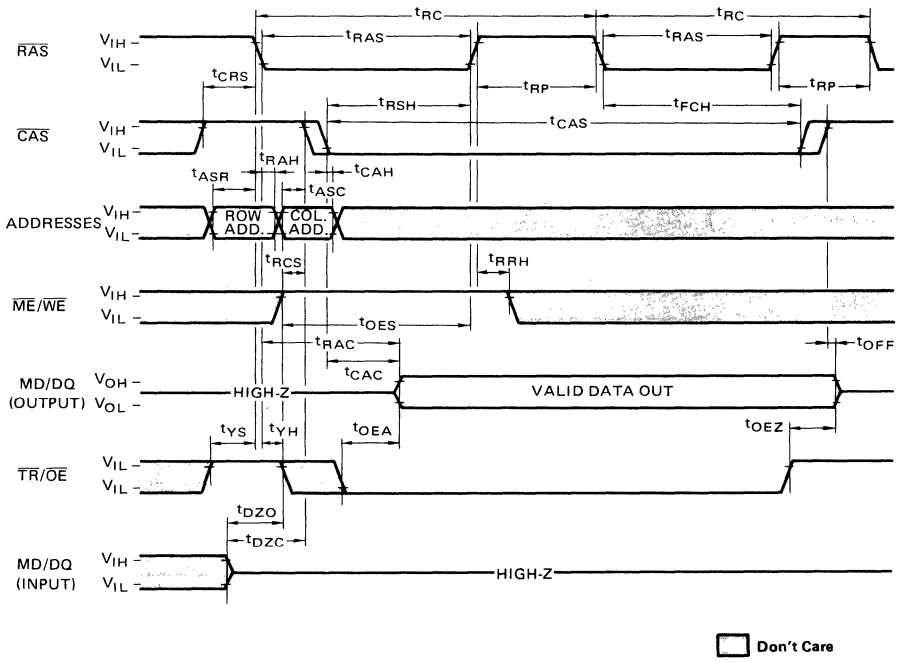
$\overline{RAS}$-ONLY REFRESH CYCLE ($\overline{ME}$/$\overline{WE}$=Don't Care)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (ADDRESS, $\overline{ME}$/$\overline{WE}$, $\overline{TR}$/$\overline{OE}$=Don't Care)

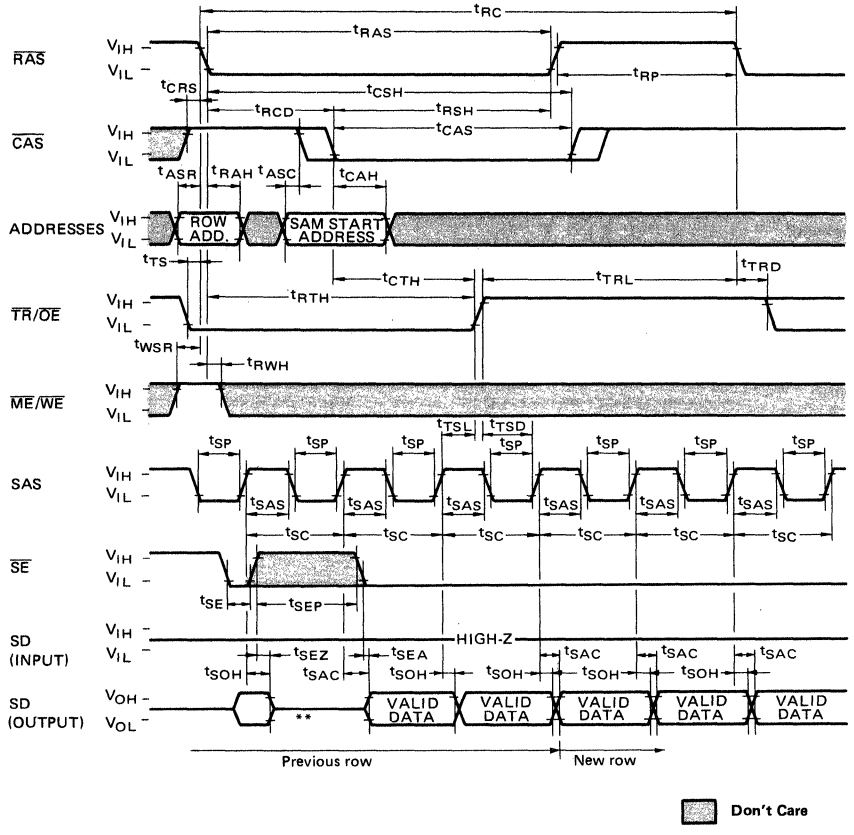


HIDDEN REFRESH CYCLE



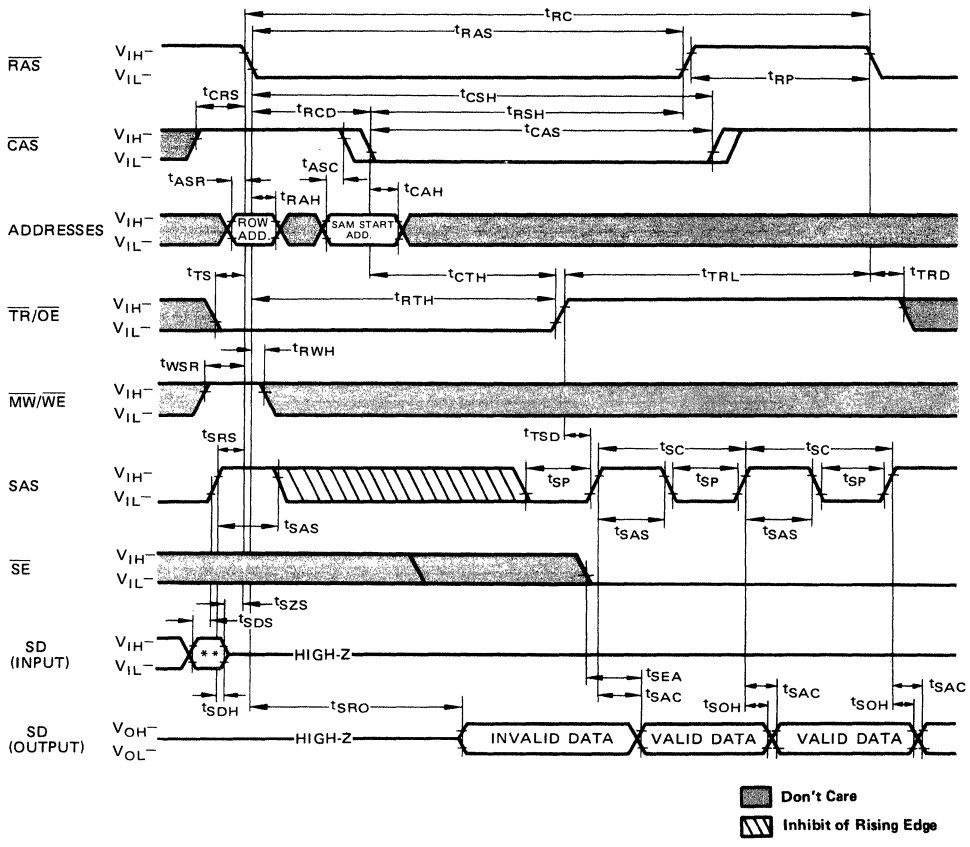
3

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.

READ TRANSFER CYCLE* (MD/DQ = Don't Care)

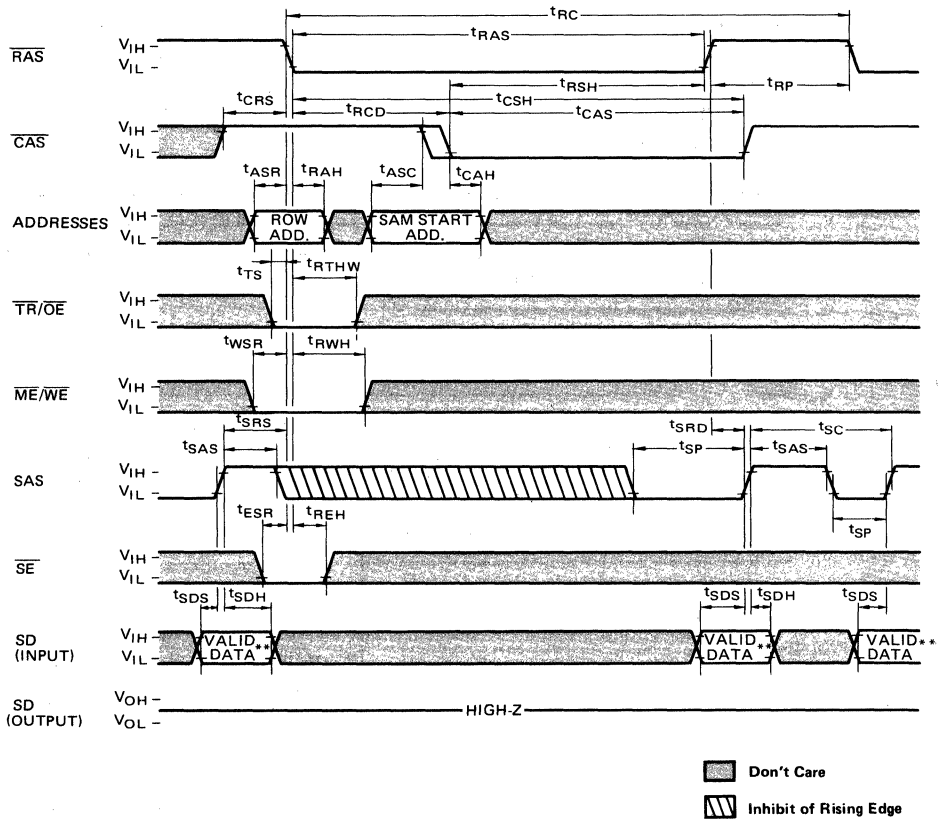


*; In the case that the previous transfer is write transfer.

**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.

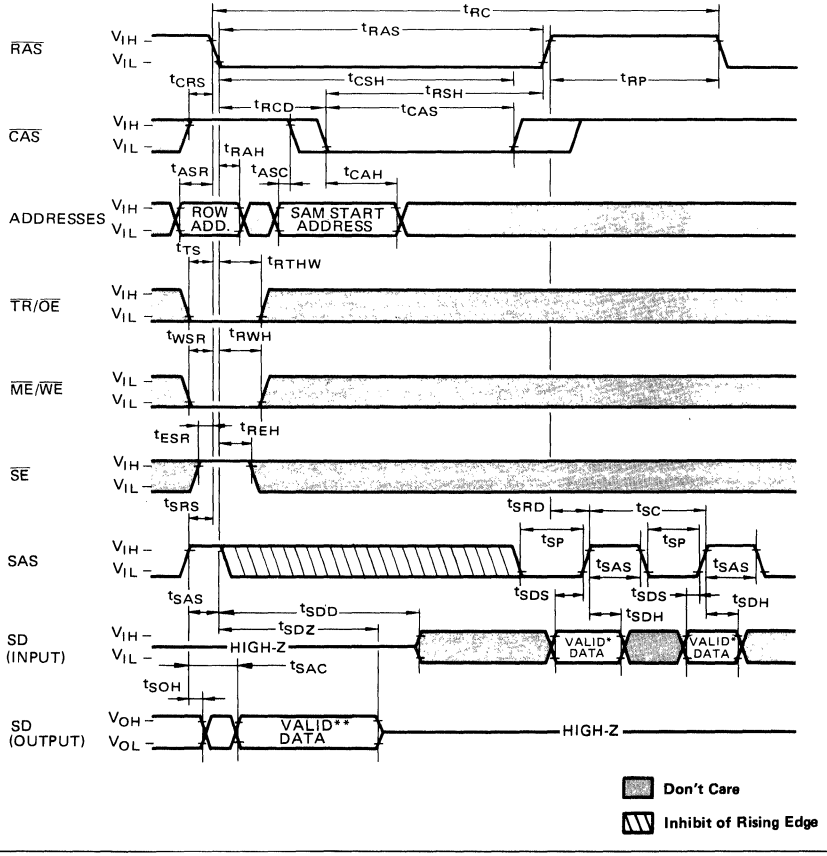
3

WRITE TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)

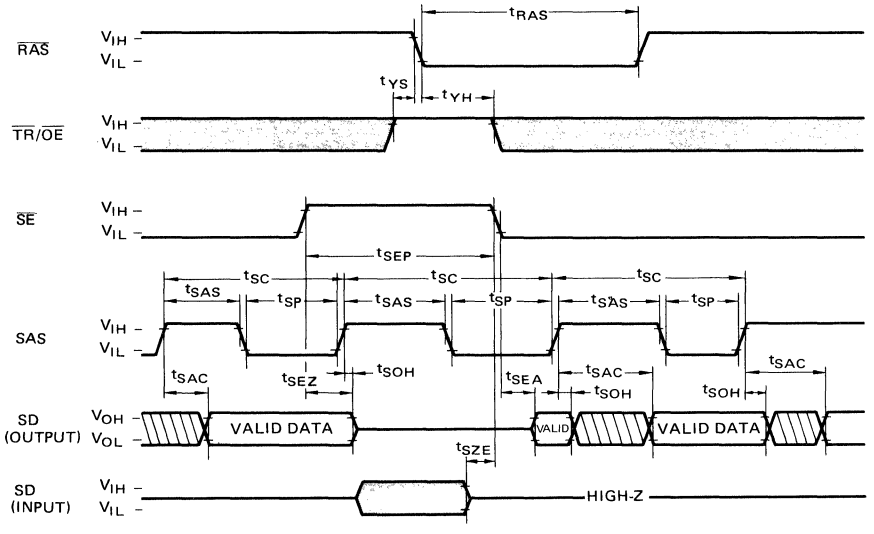


*: If $\overline{SE}$ is high, these data are not written into SAM.

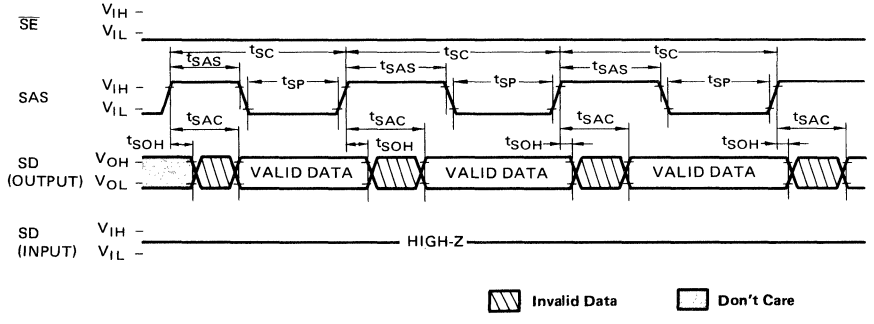
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

3

SERIAL READ CYCLE



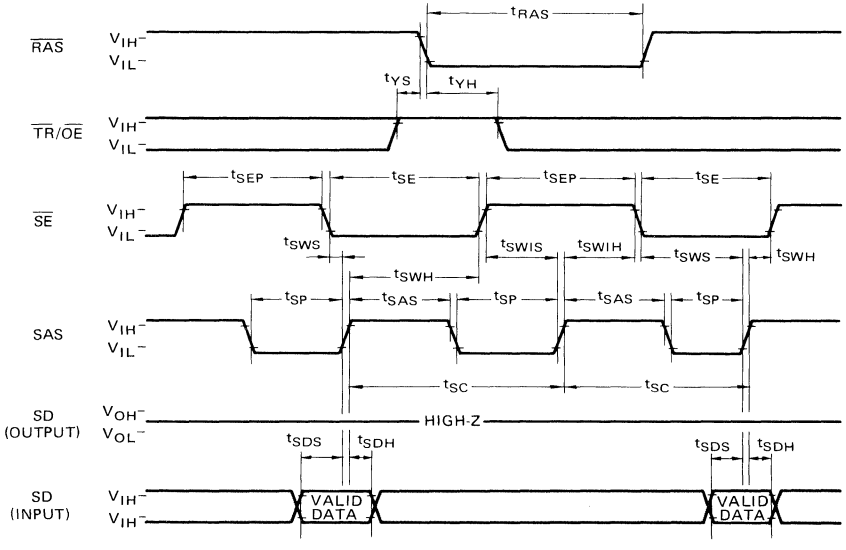
In the case of $\overline{SE}$="L" while the operation;



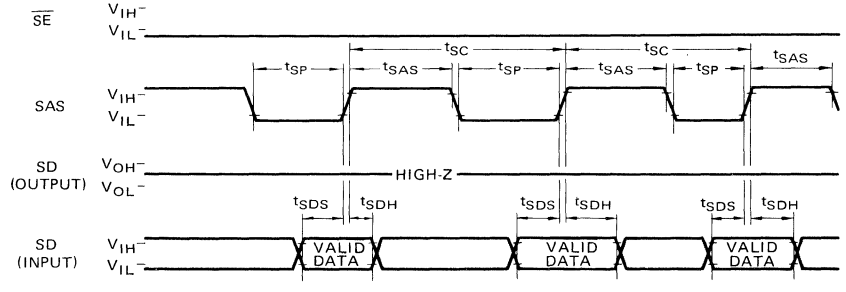
Invalid Data Don't Care

3

SERIAL WRITE CYCLE



In the case of $\overline{SE}$="L" while the operation;



Don't Care

Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

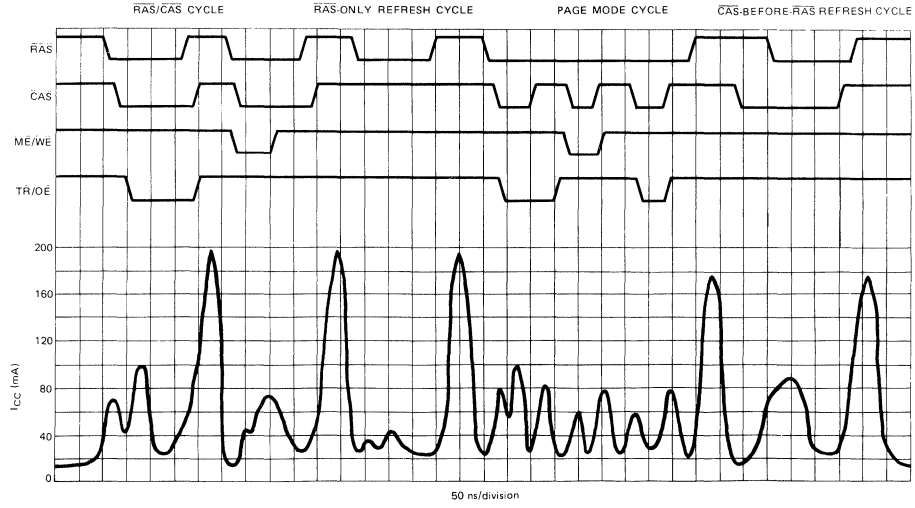
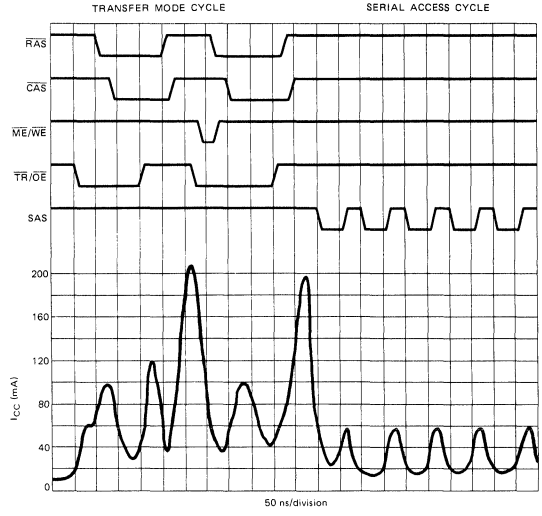


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

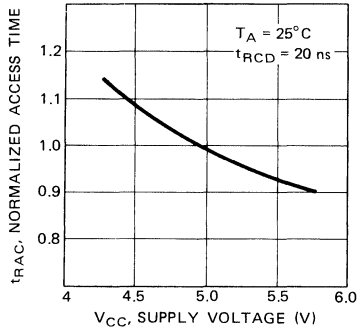


Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

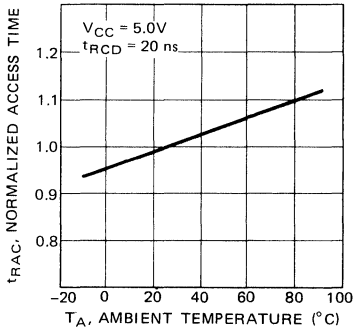


Fig. 8 – OPERATING CURRENT vs CYCLE RATE

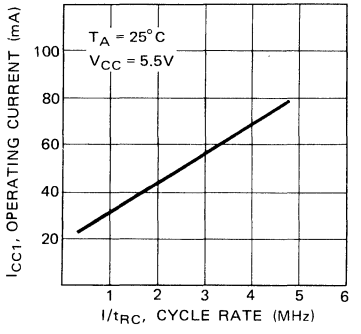


Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

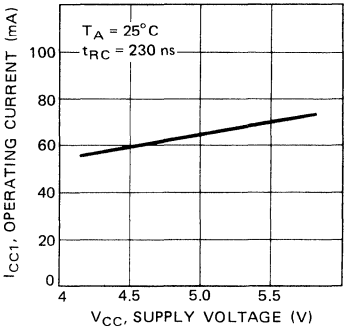


Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

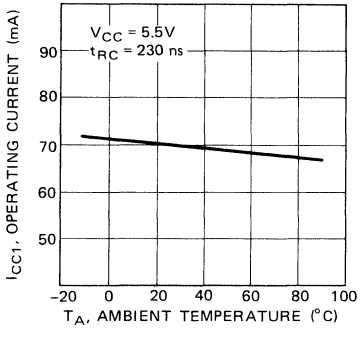
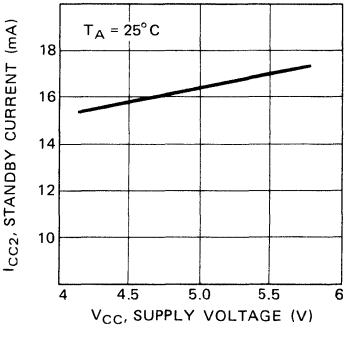


Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE



3

3

Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

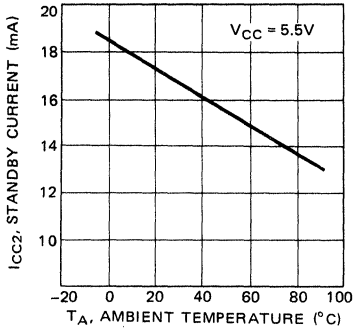


Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE

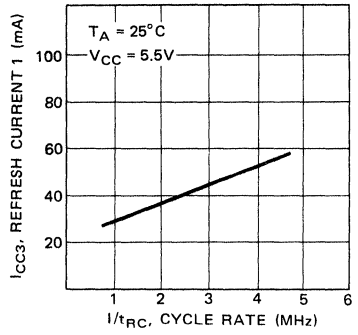


Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

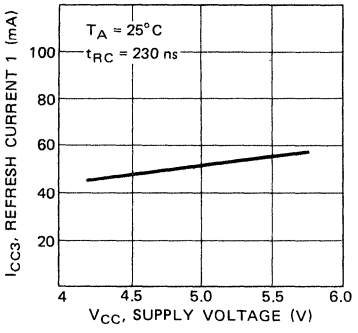


Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

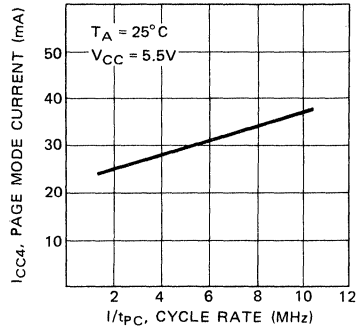


Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

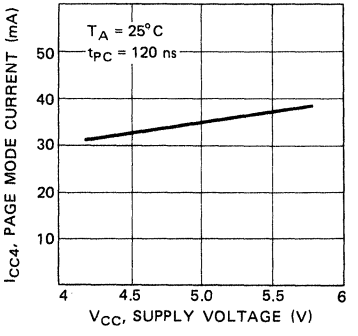


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

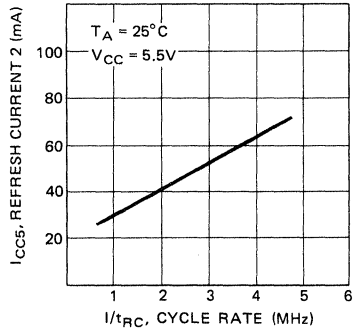


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

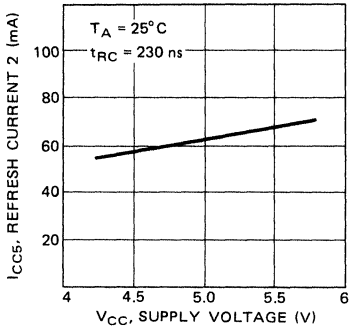


Fig. 19 – TRANSFER MODE CURRENT vs CYCLE RATE

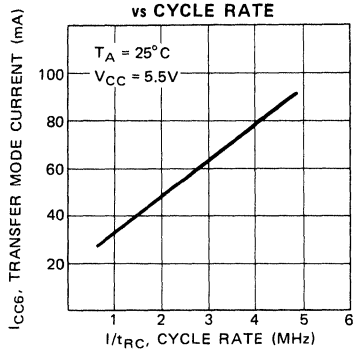


Fig. 20 – TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

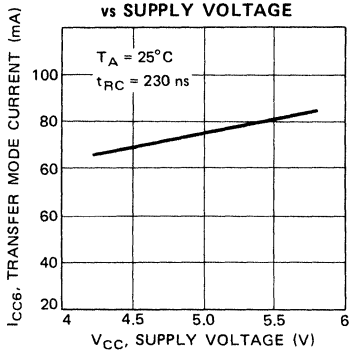


Fig. 21 – RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

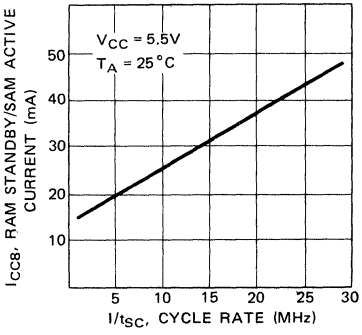


Fig. 22 – RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

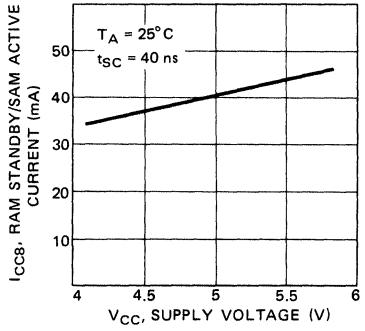
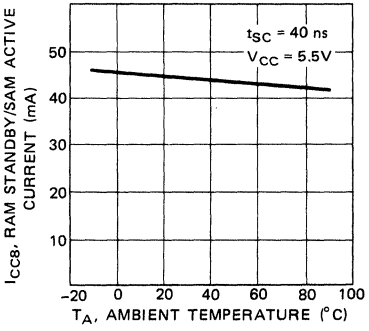


Fig. 23 – RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE



3

Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

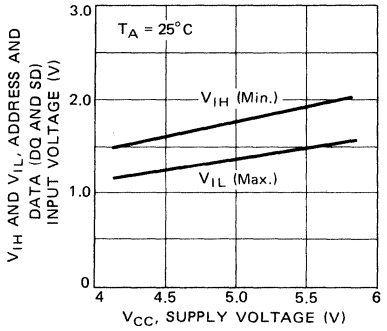


Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

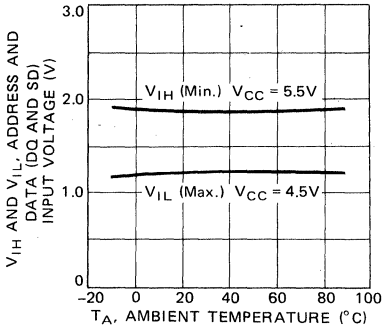


Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

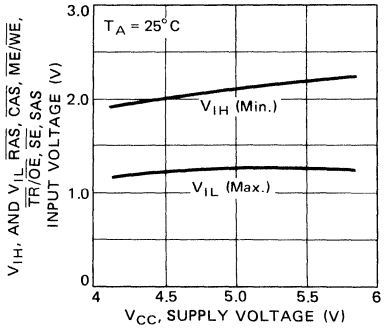


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs AMBIENT TEMPERATURE

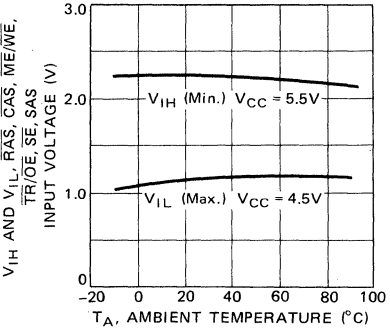


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

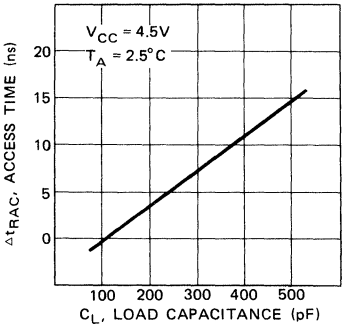


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

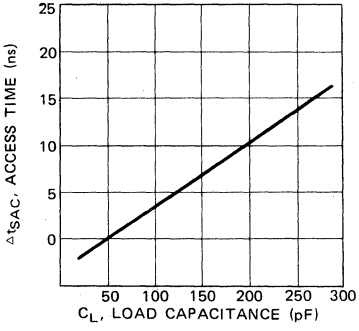


Fig. 30 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

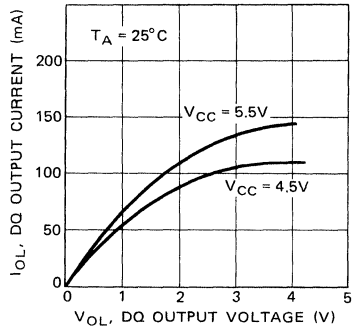


Fig. 31 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

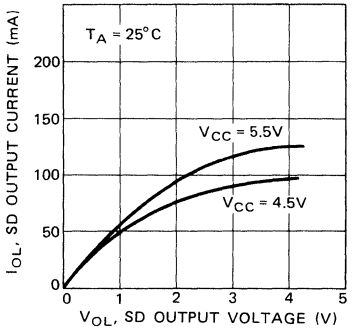


Fig. 32 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

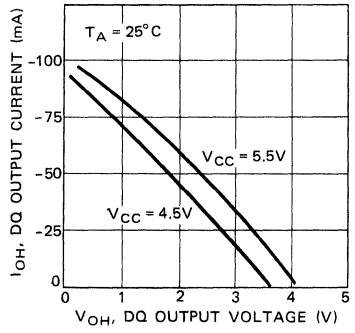


Fig. 33 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

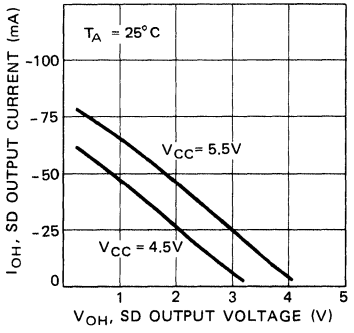
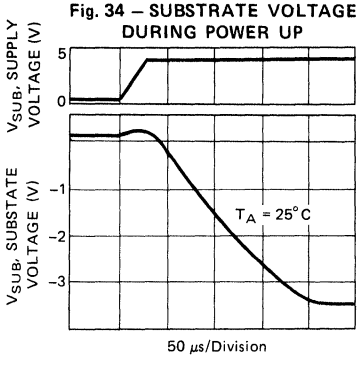


Fig. 34 – SUBSTRATE VOLTAGE DURING POWER UP

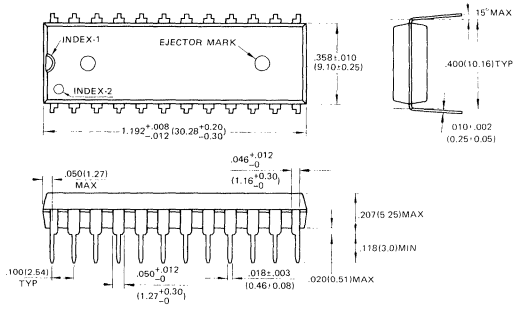


3

PACKAGE DIMENSIONS

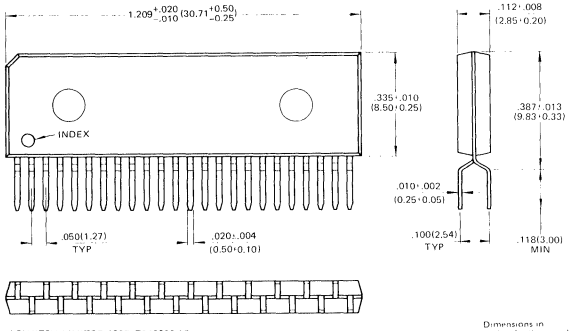
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M04)



Dimensions in inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-24P-M02)



Dimensions in inches (millimeters)

FUJITSU

262144-BIT DUAL PORT DYNAMIC RANDOM ACCESS MEMORY

MB81461B-12
MB81461B-15

July 1987
Edition 1.0

262, 144 BIT DUAL PORT DRAM

The Fujitsu MB 81461B is a fully decoded dual port NMOS dynamic random access memory organized as 65,536 words by 4 bits dynamic RAM port and 256 words by 4 bits serial access memory (SAM) port.

The DRAM port is identical to the Fujitsu MB 81464 with four bits parallel random access I/O while the SAM port is designed as four 256 bit registers each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

The MB 81461B offers complementely asynchronous access of both the DRAM and SAM ports except when data is transfered between them internally. The design is optimized for high speed and performance which makes the MB 81461B the most efficient solution for implementing the frame buffer of a bit mapped video display system. Multiplexed row and column address inputs permit the MB 81461B to be housed in a 400 mil wide 24 pin DIP and ZIP. Pin outs conformed to the JEDEC approved pin out.

The MB 81461B is fabricated using silicon gate NMOS and Fujitsu's advanced Triple Layer Polysilicon process technology. This process coupled with single transistor memory storage cells permits maximum circuit density and minimum chip size. All inputs and outputs are TTL compatible.

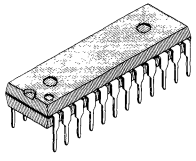
Some of the transfer cycle timing specification are different from MB 81461.

- Dual port organization
  64K x 4 Dynamic RAM port (DRAM)
  256 x 4 Serial Access Memory port (SAM)
- 24 pin DIP and ZIP package
- Silicon-gate, Triple Poly NMOS, single transistor cell
- DRAM Port
  Access Time (t_{RAC}),
  120ns max. (MB 81461B-12)
  150ns max. (MB 81461B-15)
  Cycle Time (t_{RC}),
  230ns min. (MB 81461B-12)
  260ns min. (MB 81461B-15)
- SAM Port
  Access Time (t_{SAC}),
  40 ns max. (MB 81461B-12)
  60 ns max. (MB 81461B-15)
  Cycle Time (t_{SC}),
  40ns min. (MB 81461B-12)
  60ns min. (MB 81461B-15)
- Single +5V power supply, ±10% tolerance
- Power Dissipation
  DRAM; Act/SAM; Stby
  523mW max. (MB 81461B-12)
  468mW max. (MB 81461B-15)
  DRAM; Stby/SAM; Act
  275mW max. (MB 81461B-12)
  220mW max. (MB 81461B-15)
  DRAM; Stby/SAM; Stby
  110mW max.
- Bi-directional Data Transfer between DRAM and SAM
- Fast serial access asynchronous to DRAM except transfer operation
- Real Time Read Transfer Capability
- Page Mode capability
- Bit Masked Write Mode capability
- 256 refresh cycles every 4ms
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Delayed write and Read-Modify-Write capability
- Standard 24 pin plastic DIP (Suffix; -P)
- Standard 24 pin plastic ZIP (Suffix; -PSZ)

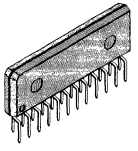
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	-1 to +7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

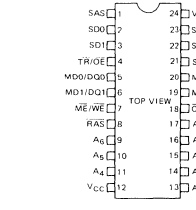


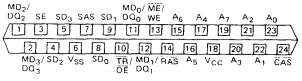
PLASTIC PACKAGE
DIP-24P-M04



PLASTIC PACKAGE
ZIP-24P-M02

PIN ASSIGNMENT





BOTTOM VIEW

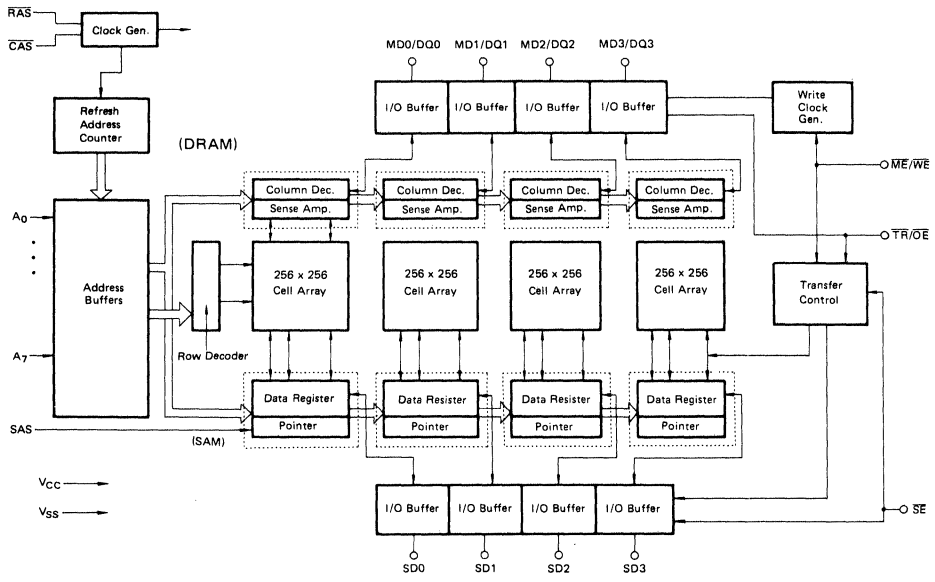
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

3

Fig. 1 – BLOCK DIAGRAM OF MB 81461B and PIN DESCRIPTION

Block Diagram



Pin Description

Pin Number		Symbol	Parameter	Mode
DIP	ZIP			
1	7	SAS	Serial Access Memory Strobe	Input
2,3,22,23	8,9,4,5	SD0 to SD3	Serial Data I/O	I/O
4	10	$\overline{TR}/\overline{OE}$	Transfer Enable/ Output Enable	Input
5,6,19,20	11,12,1,2	MD0/DQ0 to MD3/DQ3	Mask Data/Data I/O	I/O
7	13	$\overline{ME}/\overline{WE}$	Mask Mode Enable/Write Enable	Input
8	14	$\overline{RAS}$	Row Address Strobe	Input
17, 16, 15 14, 11, 10 9, 13	23,22,21, 20,17,16, 15,19	A_0 to A_7	Address Input	Input
12	18	V_{CC}	Supply Voltage +5 V	Power Supply
18	24	$\overline{CAS}$	Column Address Strobe	Input
21	3	$\overline{SE}$	Serial port Enable	Input
24	6	V_{SS}	Ground	Power Supply

DESCRIPTION

DRAM OPERATION

$\overline{RAS}$;

This pin is used to strobe eight row-address inputs from A0 to A7 pins and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$ and bit mask write cycle or not (by $\overline{ME}/\overline{WE}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, to maintain $\overline{RAS}$ = "H" (standby condition) is effective to save power dissipation.

$\overline{CAS}$;

This pin is used to strobe eight column address inputs at the falling edge. $\overline{CAS}$ pin has the function to enable and disable the output at "L" and "H" respectively during the read operation.

Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{WE}$ = "L".

$\overline{ME}/\overline{WE}$;

This pin is used to select read or write cycle. $\overline{ME}/\overline{WE}$ = "L" select write mode and $\overline{ME}/\overline{WE}$ = "H" select read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;

This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$, $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.

The $\overline{TR}/\overline{OE}$ controls the impedance of the output buffers. $\overline{TR}/\overline{OE}$ = "H" forces the output buffers at high impedance state. $\overline{TR}/\overline{OE}$ = "L" leads the output buffers at low impedance state. But in early write cycle, the output buffers are high impedance state even if $\overline{TR}/\overline{OE}$ is low.

A0 to A7;

These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB81461B The eight row address inputs are strobed by $\overline{RAS}$ and followed eight column address inputs are strobed by $\overline{CAS}$. These are used to select the start address of serial access memory also.

MD0/DQ0 to MD3/DQ3

These are common I/O pins of DRAM port. I/O mode is as specified for each function mode in the truth table.

Data Outputs:

The output buffers have three-state capability "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read" or "read-modify-write" mode. During a refresh cycle, either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data inputs:

These are used as data input pins when a data write mode such as "Early-Write", "Delayed Write" or "Read-modify-Write" is selected. In any of the above cases, these pins are set at "High-Z" state to enable data-in without any bus conflict.

In any operation mode, read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for write inhibit with MDi/DQi = "L" on the selected bit i.

Page Mode;

The page mode operation is to strobe the column address by $\overline{CAS}$ while $\overline{RAS}$ is maintained at "L" through all the successive memory operations if the row address doesn't change. This mode can save power dissipation and get the faster access time due to the elimination of $\overline{RAS}$ falling edge function.

Refresh;

Refresh of the DRAM cells is performed for every 256 rows per every 4 milliseconds.

The MB81461B offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$="H" condition. Strobing every 256 row addresses with $\overline{RAS}$ will complete all bits of memory cell to be refreshed while all outputs are invalid due to "High-Z" state. Further $\overline{RAS}$-only refresh saves the power dissipation substantially.
2) $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and an refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3) Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes to low in the next cycle.

Bit Mask Write;

This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, delayed write or read-modify-write cycle). The bits to be masked (or inhibited to write) is determined by MD/DQ state at the falling edge of $\overline{RAS}$, for example, if MD0/DQ0 and $\overline{ME}/\overline{WE}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle. Refer to the Fig. 2.

3

EXAMPLE OF BIT MASK WRITE OPERATION

Falling edge of $\overline{RAS}$						Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	Write enable
	L	H	L	H	L	Write enable for DQ0 and DQ2 Write disable for DQ1 and DQ3

X: Don't Care

FUNCTIONAL TRUTH TABLE FOR DRAM OPERATION

$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{WE}$	$\overline{TR}/\overline{OE}$	ADDRESSES	MD0/DQ0 to MD3/DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L*	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H → X → H	Valid	Valid Data In	Delayed Write
L	L	H→L	H→L→H	Valid	Valid Data Out → Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	$\overline{RAS}$-Only Refresh
H→L	L	X	H→X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

*: If $\overline{ME}/\overline{WE}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write mode is enabled.

TRANSFER OPERATION:

The transfer operation is featured in the MB 81461B. This mode is used to transfer simultaneously 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of $\overline{ME}/\overline{WE}$ at the falling edge of $\overline{RAS}$. $\overline{ME}/\overline{WE}$="H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and $\overline{ME}/\overline{WE}$="L" defines the transfer from SAM to DRAM (Write Transfer Cycle).

I/O mode of SD0 to SD3 determined while the transfer operation is set ($\overline{TR}/\overline{OE}$="L") conjunctioned with $\overline{ME}/\overline{WE}$ state.

After Read Transfer Cycle, please apply two or more SAS Clock.

$\overline{TR}/\overline{OE}$;

This pin is used to enable transfer operation at the falling edge of $\overline{RAS}$.

$\overline{ME}/\overline{WE}$;

This pin is used to select the direction of transfer at the falling edge of $\overline{RAS}$.

A0 to A7;

These pins are used to seiect the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by $\overline{RAS}$ and the start address is strobed by $\overline{CAS}$.

Pseudo Write Transfer:

To start serial write cycle, the SD pins must be set in input mode. To do this, write transfer cycle should be executed. The pseudo write transfer cycle is to change the SD pins into input mode without data transfer from SAM to DRAM. Refer to Fig. 3.

Refresh during transfer cycle;

DRAM and SAM are refreshed during transfer cycle as shown below.

1) Read transfer cycle:
   During read transfer cycle, the selected row address of DRAM to be transfered to SAM is refreshed. SAM data are kept by applying 256 SAS clocks within 4 ms after the read transfer cycle.
2) Write transfer cycle:
   During write transfer cycle, the new data are written from SAM to DRAM and this row address should be refreshed within 4 ms.
   But SAM data are not refreshed during write transfer cycle. Therefore, the SAM refresh (applying 256 SAS clocks within 4 ms) must be executed. Especially, when the write transfer cycle is executed continuously, 256 SAS clock should be applied within 4 ms.

SERIAL ACCESS OPERATION:

The MB 81461B has 256 words by 4 bits Serial Acess Memory (SAM) corresponding to 64K words by 4 bits DRAM and the fast serial read/write access is achieved by SAM architecture. Read or write cycle is determined when the last read or write transfer operation is executed. If the last transfer operation was read transfer, the serial read cycle is performed until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write or pseudo write transfer, the serial write cycle is performed. In the serial write operation, 256 words by 4 bits data stored in the SAM can be transfered to DRAM under $\overline{SE}$="L" condition, and $\overline{SE}$="H" condition disables data transfer from SAM to DRAM. The serial access operation can be done asynchronously from DRAM port.

SAS;

This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data of the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, out-

put data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returnes to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation by bit to bit. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" leads SD pins to "High-Z" state. $\overline{SE}$ = "L" leads SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by last occured transfer operation, if last transfer operation was read transfer mode, they are output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is constructed by dynamic circuitry, the refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is applicable to obtain valid data continuously when row address is changed without any timing loss from the last bit of previous row to the first bit of new row. Data transfer from DRAM to SAM is triggered by rising edge of $\overline{TR}/\overline{OE}$ after the preparation of internal circuit for this operation, while SAM port can continue read operation asynchronously from the above mentioned internal move. Once $\overline{TR}/\overline{OE}$ returns to "H" with the restricted timing specification t_{TSL} and t_{TSD} refered to SAS clock, SD pins can get the valid output data continuously as shown in Fig. 4. The key issue to achieve this feature is to apply SAS clock continuously with the timing consideration to the rising edge of $\overline{TR}/\overline{OE}$.

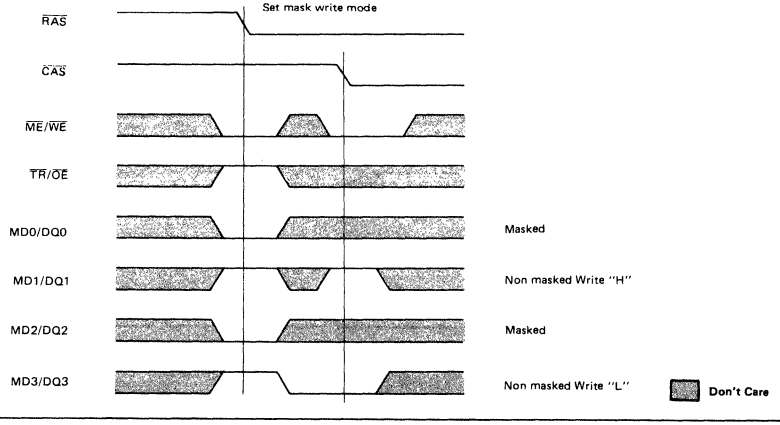
FUNCTIONAL TRUTH TABLE FOR SERIAL ACCESS (Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$		SAS	$\overline{SE}$	SD0 to SD3	Function
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{WE}$				
H	X	Clock	L	Input/Output*	Sequential access enable
		Clock	H	Input/Output*	Sequential access disable

*: The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.

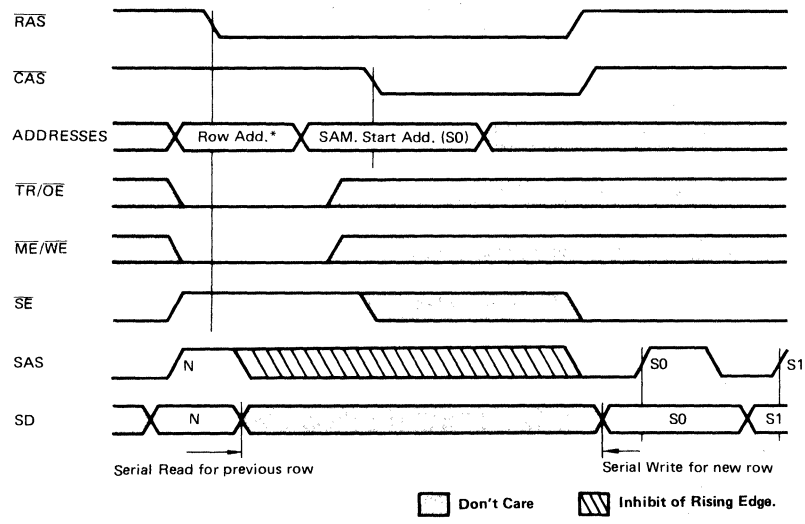
X; Don't Care

Fig. 2 – EXAMPLE OF BIT MASK WRITE OPERATION



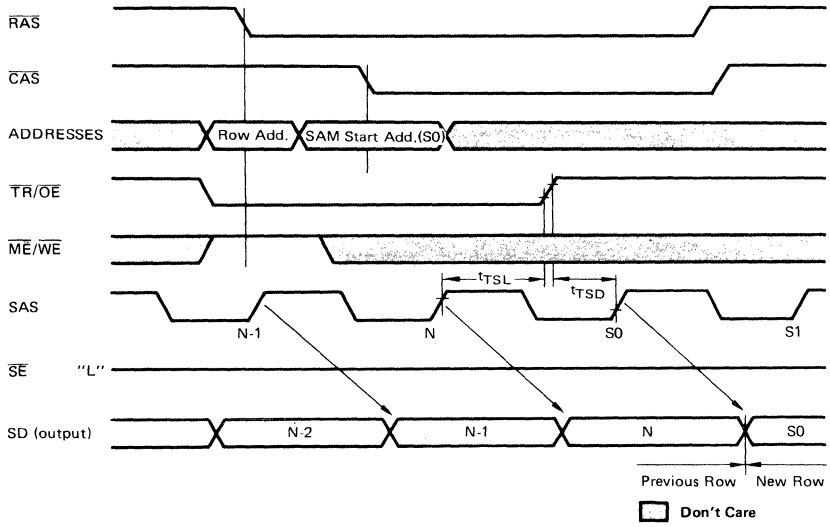
3

Fig. 3 – EXAMPLE OF PSEUDO WRITE TRANSFER CYCLE



*The DRAM data of this row address are refreshed during pseudo write transfer cycle.

Fig. 4 – EXAMPLE OF REAL TIME READ TRNASFER OPERATION



RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

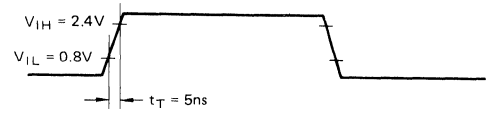
Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}	-2.0		0.8	V	

CAPACITANCE (T_A=25°C)

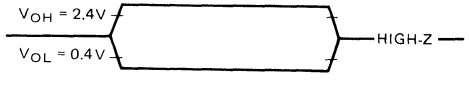
Paramter	Symbol	Typ	Max		Unit
			DIP	ZIP	
Input Capacitance (A0 to A7)	C_{IN1}		7	8	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{ME}$/$\overline{WE}$, $\overline{SE}$, $\overline{TR}$/$\overline{OE}$)	C_{IN2}		10	12	pF
Input Capacitance (SAS)	C_{IN3}		7	7	pF
Input/Output Capacitance (MD0/DQ0 to MD3/DQ3)	C_{IO1}		7	8	pF
Input/Output Capacitance (SD0 to SD3)	C_{IO2}		7	8	pF

AC TEST CONDITIONS

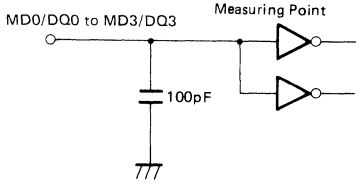
1) Input

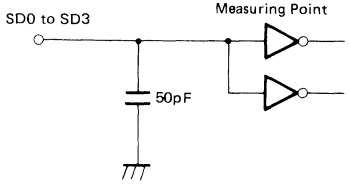


2) Output



3) Output Load





DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
SAM STANDBY $\overline{SE}$ = V_{IH}, SAS = V_{IL}					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC1}		95	mA
	MB 81461B-15			85	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		20	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC3}		77	mA
	MB 81461B-15			70	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min)	MB 81461B-12	I_{CC4}		50	mA
	MB 81461B-15			45	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461B-12	I_{CC5}		77	mA
	MB 81461B-15			70	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC6}		110	mA
	MB 81461B-15			100	
SAM ACTIVE $\overline{SE}$ = V_{IL}, t_{SC} = min					
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC7}		130	mA
	MB 81461B-15			110	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MB 81461B-12	I_{CC8}		50	mA
	MB 81461B-15			40	
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC9}		112	mA
	MB 81461B-15			95	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	MB 81461B-12	I_{CC10}		85	mA
	MB 81461B-15			70	
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB 81461B-12	I_{CC11}		112	mA
	MB 81461B-15			95	
TRANSFER MODE CURRENT Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 81461B-12	I_{CC12}		145	mA
	MB 81461B-15			125	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC}=5.5V, V_{SS}=0V, all other pins not under test=0V)	$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH}=-5mA/-2mA for DQi/SDi) Output low voltage (I_{OL}=4.2mA)	V_{OH} V_{OL}	2.4	 0.4	V

Note: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

3

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1 2 3

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Time between Refresh (RAM/SAM)		t_{REF}		4		4	ms
Random Read/Write Cycle Time		t_{RC}	230		260		ns
Read-Modify-Write Cycle Time		t_{RWC}	305		345		ns
Page Mode Cycle Time		t_{PC}	120		145		ns
Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	195		225		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	25	0	35	ns
Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	60000	150	60000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60		75		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
$\overline{CAS}$ Precharge Time (Normal cycle)		t_{CPN}	40		50		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50		60		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$)		t_{CPR}	25		30		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	60000	75	60000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	9	t_{RRH}	20		20		ns
Read Command Hold Time Referenced to $\overline{CAS}$	9	t_{RCH}	0		0		ns
Write Command Set Up Time		t_{WCS}	-5		-5		ns
Write Command Hold Time		t_{WCH}	30		35		ns
Write Command Pulse Width		t_{WP}	30		35		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40		45		ns
Data In Set Up Time		t_{DS}	0		0		ns
Data In Hold Time		t_{DH}	30		35		ns
Access Time from $\overline{TR}$/$\overline{OE}$	6	t_{OEA}		35		40	ns
$\overline{TR}$/$\overline{OE}$ to Data In Delay Time		t_{OED}	25		30		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Output Buffer Turn Off Delay from $\overline{TR}/\overline{OE}$		t_{OEZ}	0	25	0	30	ns
$\overline{TR}/\overline{OE}$ Hold Time Referenced to $\overline{ME}/\overline{WE}$		t_{OEH}	0		0		ns
$\overline{TR}/\overline{OE}$ to $\overline{RAS}$ inactive Set Up Time		t_{OES}	0		0		ns
Data In to $\overline{CAS}$ Delay Time	16	t_{DZC}	0		0		ns
Data In to $\overline{TR}/\overline{OE}$ Delay Time	16	t_{DZO}	0		0		ns
Refresh Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCS}	25		30		ns
Refresh Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)		t_{FCH}	25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	20		20		ns
Serial Clock Cycle Time		t_{SC}	40	50000	60	50000	ns
Access Time from SAS	10	t_{SAC}		40		60	ns
Access Time from $\overline{SE}$	10	t_{SEA}		40		50	ns
SAS Precharge Time		t_{SP}	10		20		ns
SAS Pulse Width		t_{SAS}	10		20		ns
$\overline{SE}$ Precharge Time		t_{SEP}	25		45		ns
$\overline{SE}$ Pulse Width		t_{SE}	25		45		ns
Serial Data Out Hold Time after SAS High		t_{SOH}	10		10		ns
Serial Output Buffer Turn Off Delay from $\overline{SE}$		t_{SEZ}	0	25	0	30	ns
Serial Data In Set Up Time	11	t_{SDS}	0		0		ns
Serial Data In Hold Time	11	t_{SDH}	20		25		ns

AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{TS}	0		0		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{RTH}	90		110		ns
Write Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time	12	t_{RTHW}	12		15		ns
Transfer Command ($\overline{TR}$) to $\overline{CAS}$ Hold Time		t_{CTH}	30		35		ns
Transfer Command ($\overline{TR}$) to SAS Lead Time		t_{TSL}	5		10		ns
Transfer Command ($\overline{TR}$) to $\overline{RAS}$ Lead Time	17	t_{TRRL}	25		35		ns
Transfer Command ($\overline{TR}$) Hold Time from $\overline{RAS}$	17	t_{TRRH}	25		35		ns
First SAS Edge to Transfer Command Delay Time		t_{TSD}	25		35		ns
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ Set Up Time		t_{WSR}	0		0		ns
$\overline{ME}$/$\overline{WE}$ to $\overline{RAS}$ Hold Time		t_{RWH}	12		15		ns
Mask Data (MD) to $\overline{RAS}$ Set Up Time		t_{MS}	0		0		ns
Mask Data (MD) to $\overline{RAS}$ Hold Time		t_{MH}	35		45		ns
Serial Output Buffer Turn Off Delay from $\overline{RAS}$	12	t_{SDZ}	10	60	10	75	ns
Serial Output Buffer Turn On Delay from $\overline{RAS}$	13	t_{SRO}	0		0		ns
SAS to $\overline{RAS}$ Set Up Time	11	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS Delay Time	12	t_{SRD}	30		45		ns
Serial Data Input to $\overline{SE}$ Delay Time		t_{SZE}	0		0		ns
Serial Data Input Delay from $\overline{RAS}$	12	t_{SDD}	60		75		ns

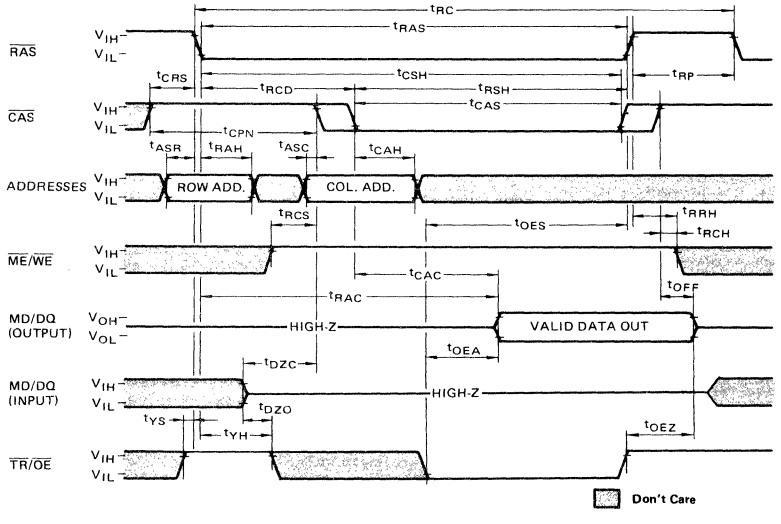
AC CHARACTERISTICS

Parameter	NOTES	Symbol	MB 81461B-12		MB 81461B-15		Unit
			Min	Max	Min	Max	
Serial Data Input to $\overline{RAS}$ Delay Time	13	t_{SZS}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Set up Time	14	t_{ESR}	0		0		ns
Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	14	t_{REH}	12		15		ns
Serial Write Enable Set up Time	11	t_{SWS}	20		30		ns
Serial Write Enable Hold Time	11	t_{SWH}	80		120		ns
Serial Write Disable Set Up Time	11	t_{SWIS}	20		30		ns
Serial Write Disable Hold Time	11	t_{SWIH}	40		60		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Set Up Time		t_{YS}	0		0		ns
Asynchronous Command ($\overline{TR}$) to $\overline{RAS}$ Hold Time		t_{YH}	12		15		ns
Time between Transfer	15	t_{REFT}		4		4	ms

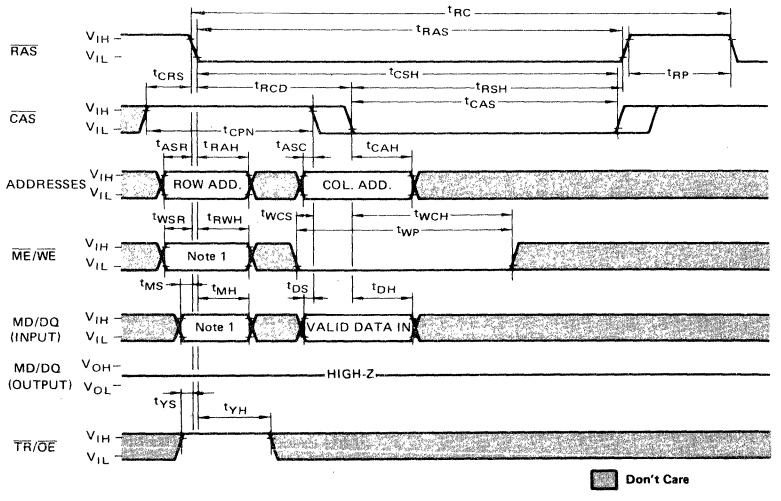
NOTES:

1. An initial pause of 200μs is required after power-up followed by any 8 RAS, 8 transfer, and 8 SAS cycle before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycle are required.
2. AC characteristics assume.
3. V_{IH} (min) and L_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T=5ns) + t_{ASC} (min)
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Measured with a load equivalent to 2 TTL loads and 50pF.
11. Input mode only
12. Write transfer and pseuso write transfer only.
13. Read transfer only in the case that the previous transfer was write transfer.
14. Pseudo write transfer only.
15. If t_{REFT} is not satisfied, 8 transfer and 8 SAS cycles before proper device operation is needed.
16. Either t_{DZC} or t_{DZO} must be satisfied.
17. This timing specification is different from that of MB 81461.

READ CYCLE

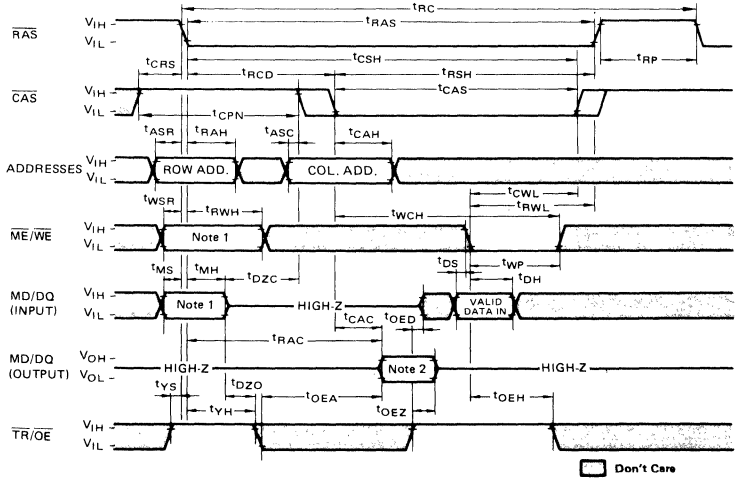


WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

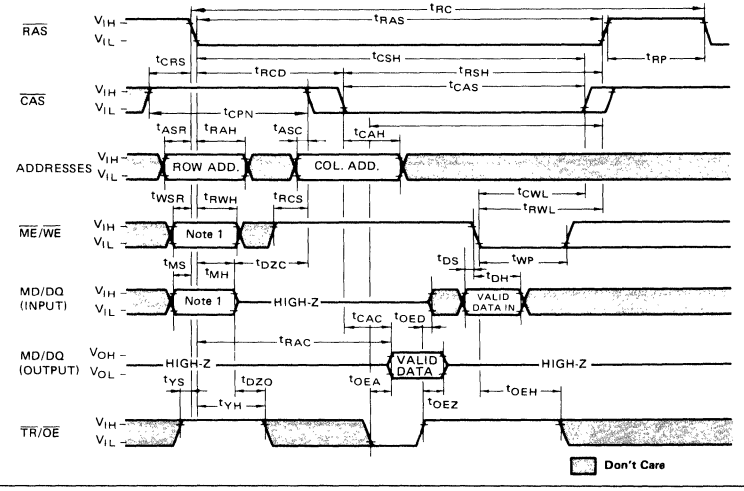
DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

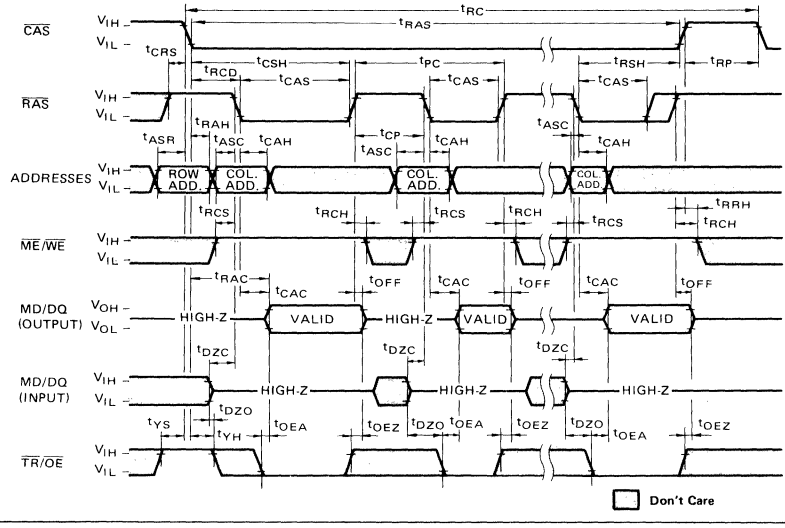
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

READ-MODIFY-WRITE CYCLE

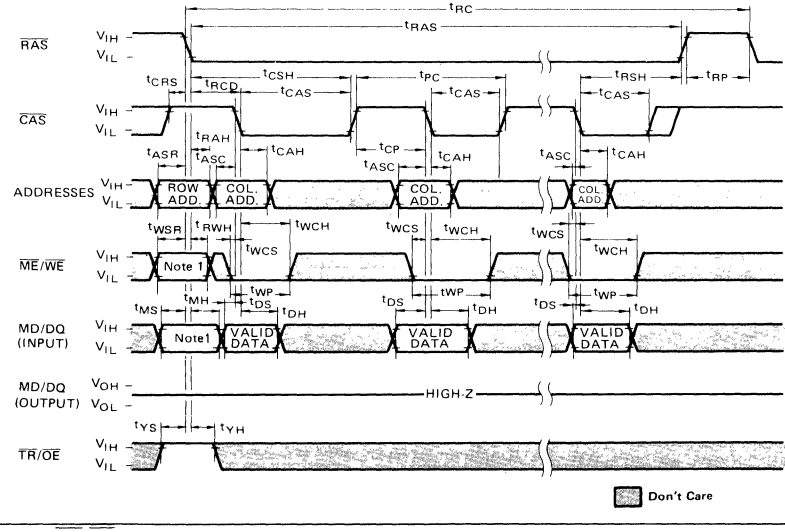


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

PAGE MODE READ CYCLE

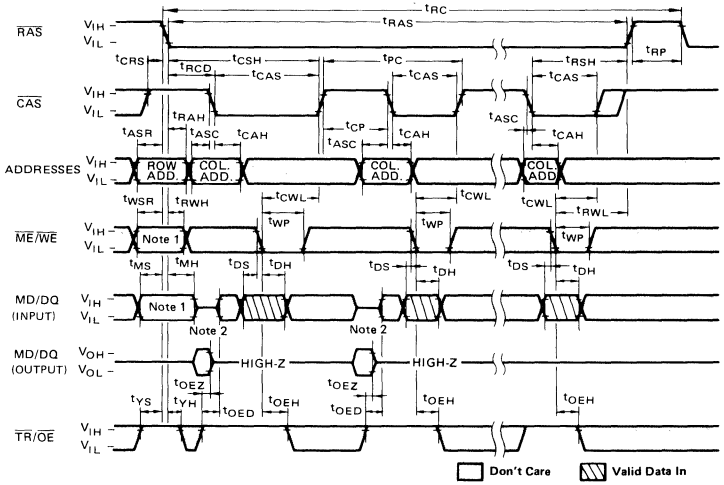


PAGE MODE WRITE CYCLE (EARLY WRITE)



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

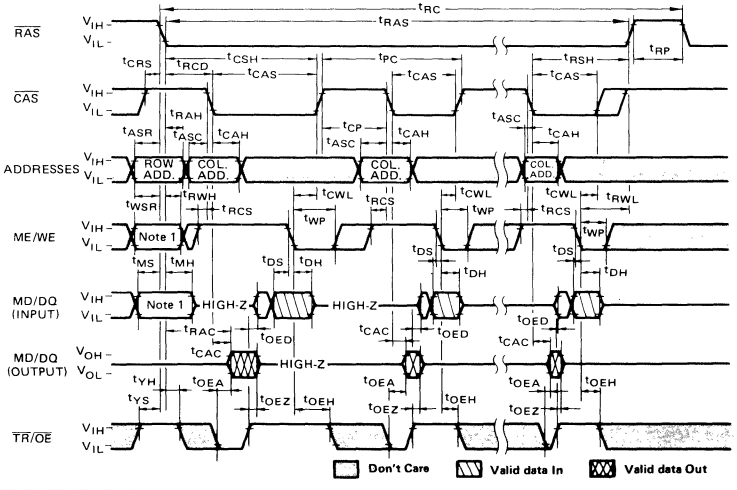
PAGE MODE DELAYED WRITE CYCLE



Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

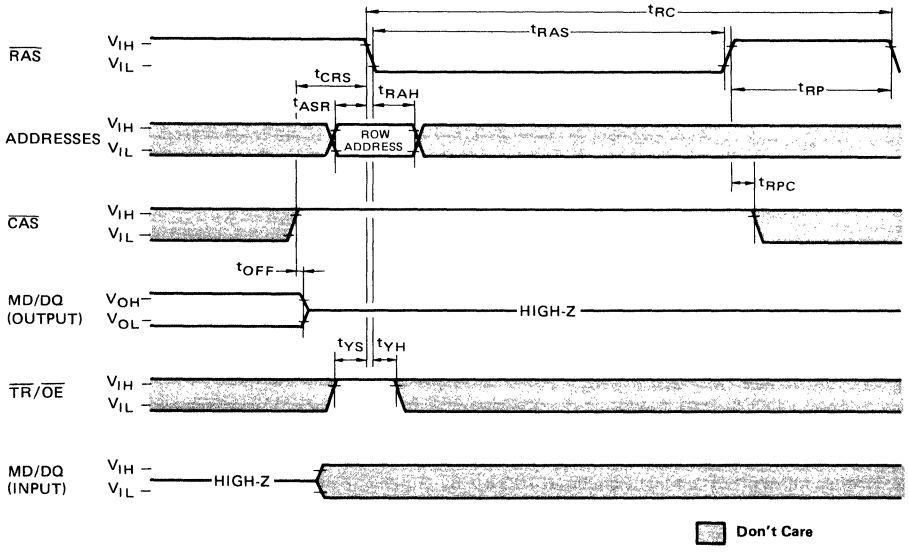
Note 2) When $\overline{TR}/\overline{OE}$ is kept "H" through a cycle, the MD/DQ are kept High-Z state.

PAGE MODE READ-MODIFY-WRITE CYCLE

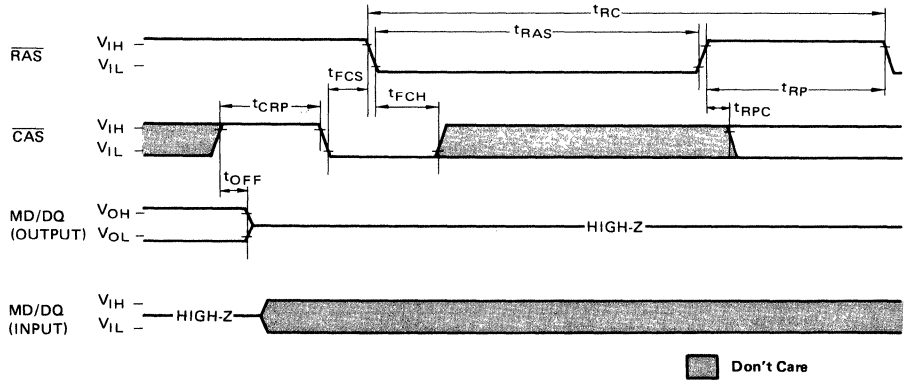


Note 1) When $\overline{ME}/\overline{WE}$ = "H", all data on the MD/DQ can be written into the cell.
When $\overline{ME}/\overline{WE}$ = "L", the data on the MD/DQ are not written (masked) except for when MD/DQ = "H" at the falling edge of $\overline{RAS}$.

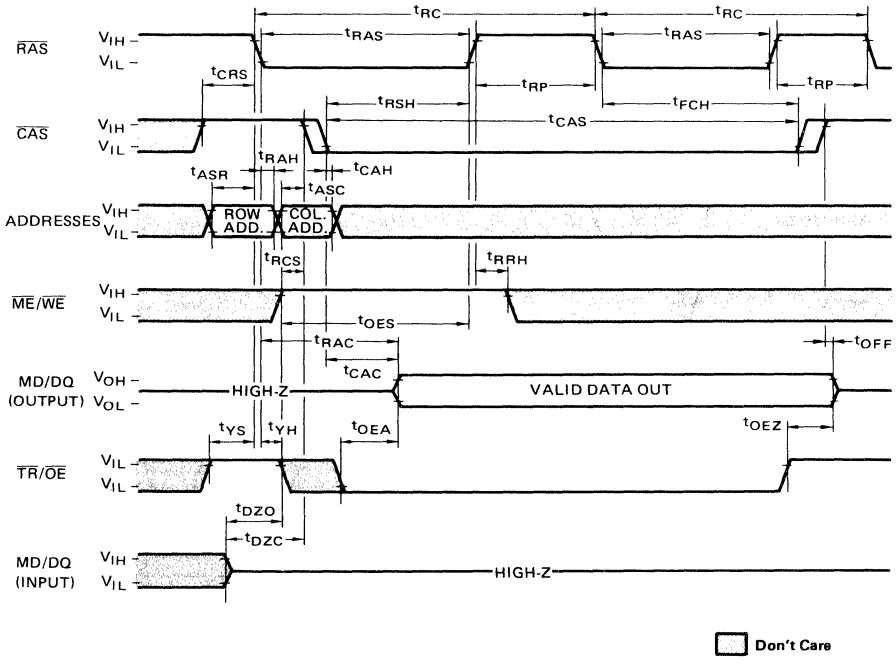
$\overline{RAS}$-ONLY REFRESH CYCLE ($\overline{ME}/\overline{WE}$=Don't Care)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE (ADDRESS, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$=Don't Care)



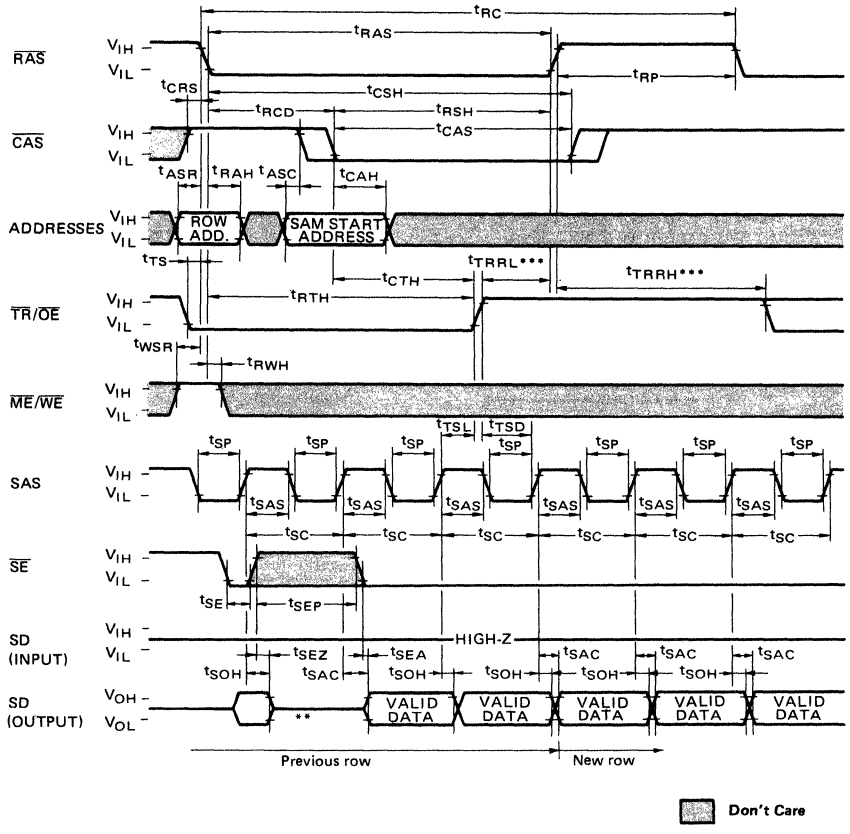
HIDDEN REFRESH CYCLE



3

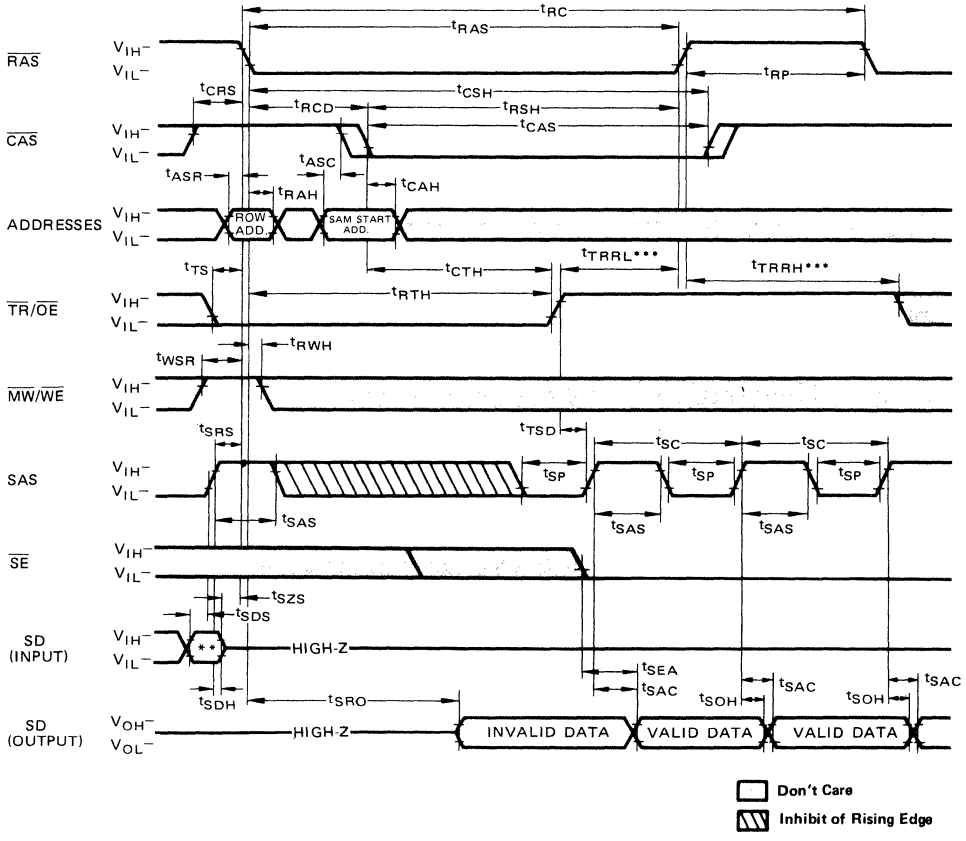
3

READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*: In the case that the previous transfer is read transfer.
**: If $\overline{SE}$ is low, the valid data will appear within t_{SAC} or t_{SEA}.
***: These parameters are different from that of MB 81461.

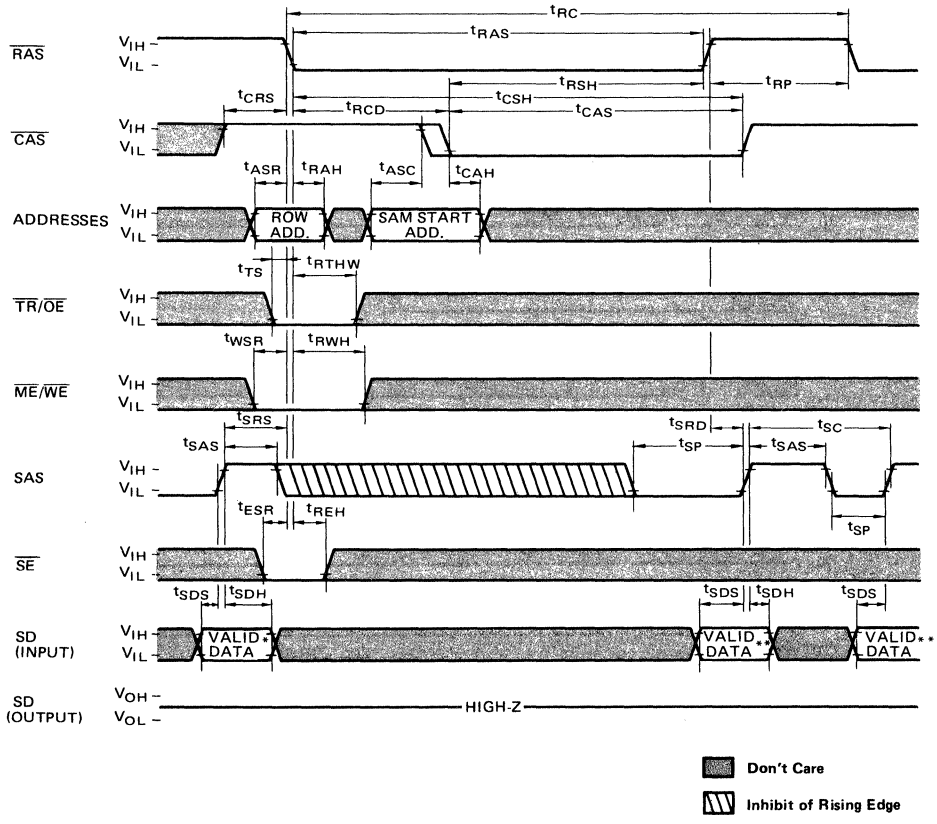
READ TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is low and the previous cycle is serial write cycle, this should be valid data input.
***; These parameters are different from that of MB 81461.

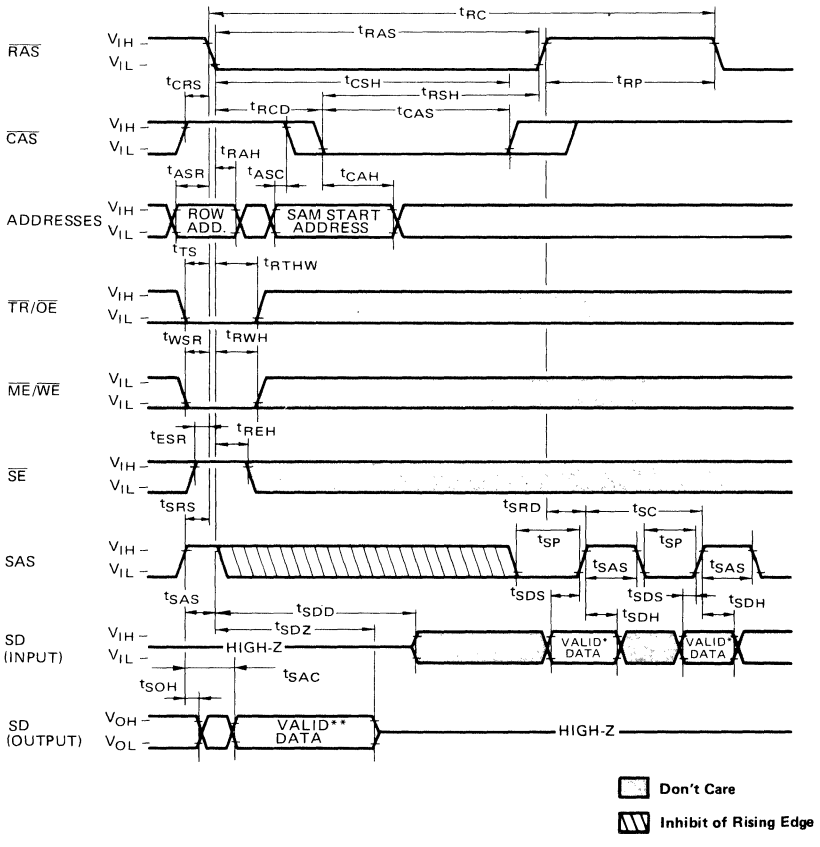
3

WRITE TRANSFER CYCLE* (MD/DQ = Don't Care)



*; In the case that the previous transfer is write transfer.
**; If $\overline{SE}$ is high these data are not written into the SAM.

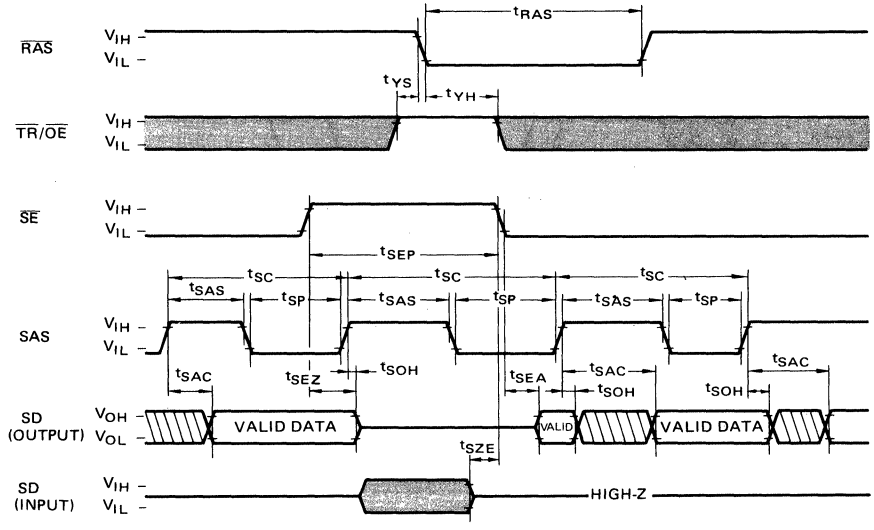
PSEUDO WRITE TRANSFER CYCLE (MD/ DQ = Don't Care)



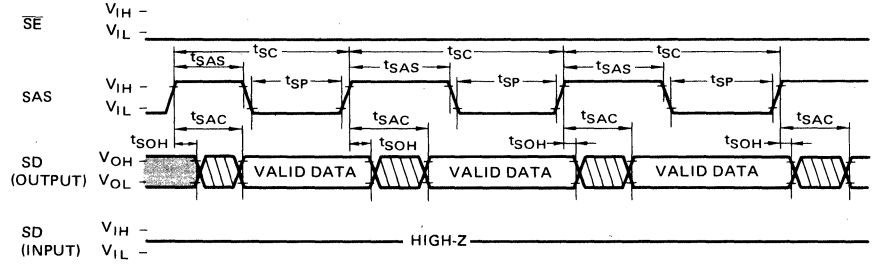
*: If $\overline{SE}$ is high, these data are not written into SAM.
**: If $\overline{SE}$ is high, SD (SD0 to SD3) are in High-Z state after t_{SEZ}.
If $\overline{SE}$ becomes low, the valid data will appear meeting t_{SAC} and t_{SEA}.

3

SERIAL READ CYCLE



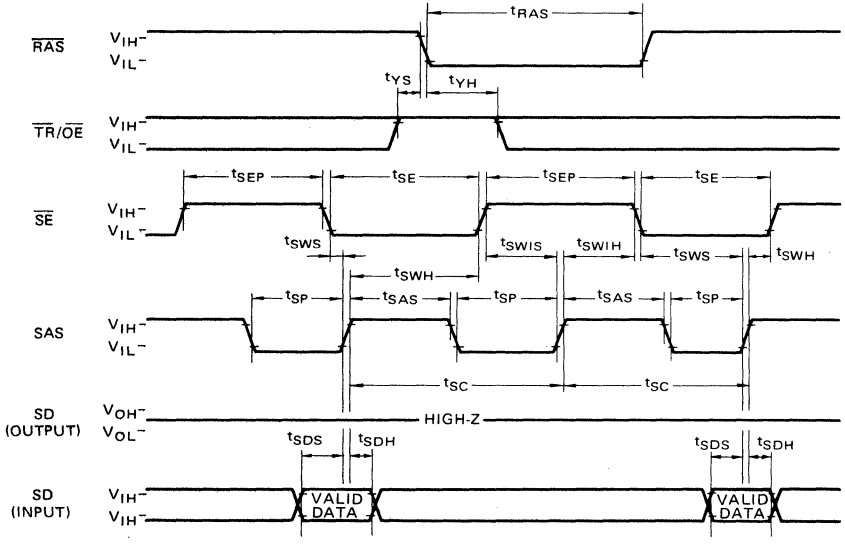
In the case of $\overline{SE}$="L" while the operation;



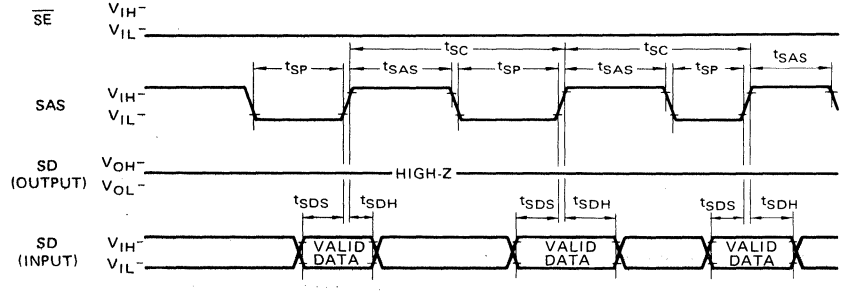
Invalid Data Don't Care

3

SERIAL WRITE CYCLE



In the case of $\overline{SE}$="L" while the operation;



Don't Care

3

Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

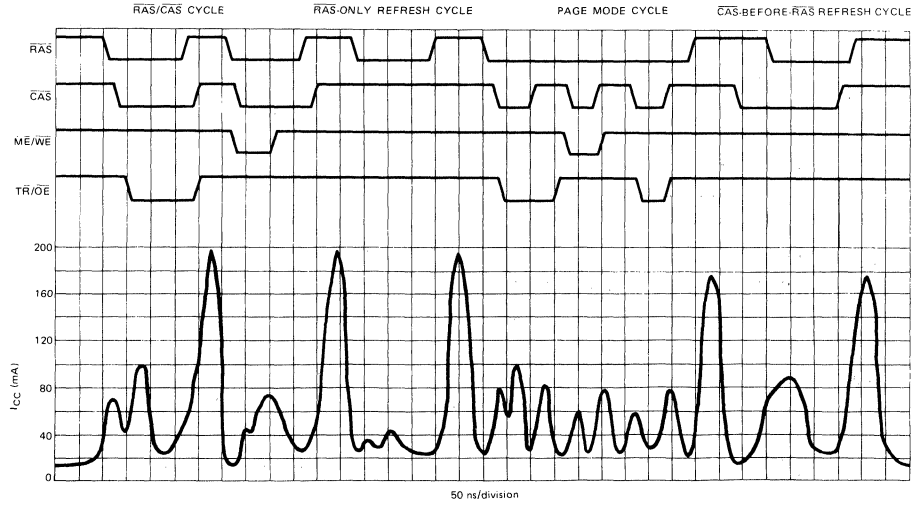
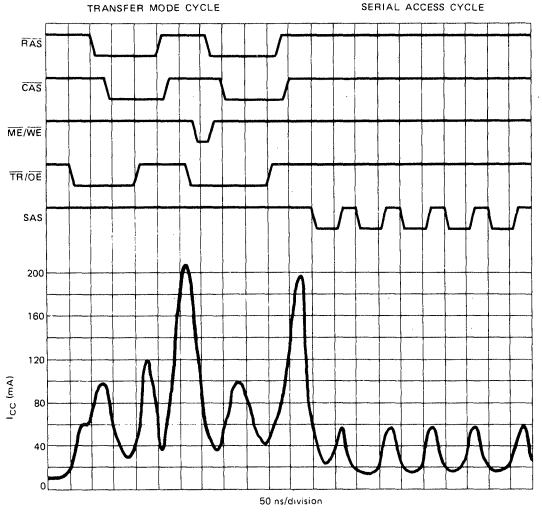


Fig. 5 – CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C) (cont'd)



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

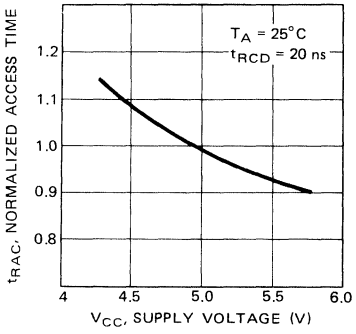


Fig. 7 – NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

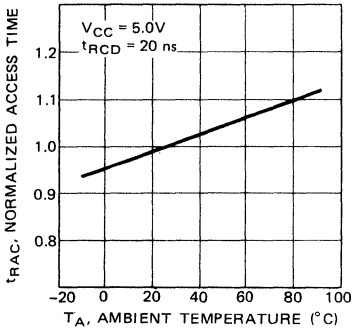


Fig. 8 – OPERATING CURRENT vs CYCLE RATE

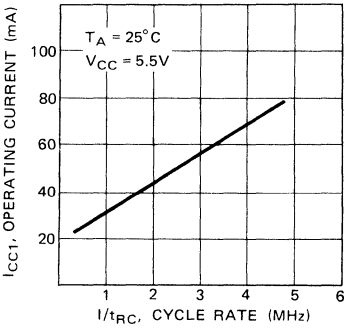


Fig. 9 – OPERATING CURRENT vs SUPPLY VOLTAGE

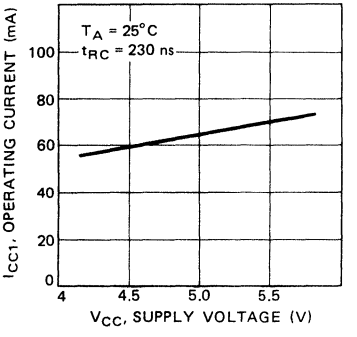


Fig. 10 – OPERATING CURRENT vs AMBIENT TEMPERATURE

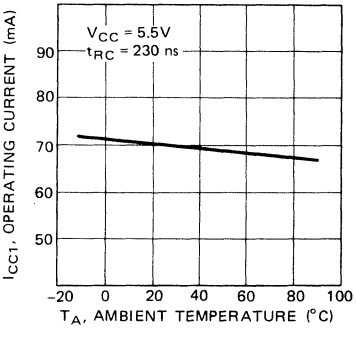
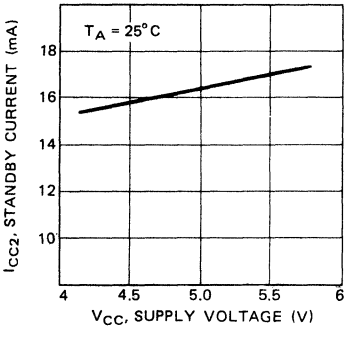


Fig. 11 – STANDBY SURRENT vs SUPPLY VOLTAGE



3

3

Fig. 12 – STANDBY CURRENT vs AMBIENT TEMPERATURE

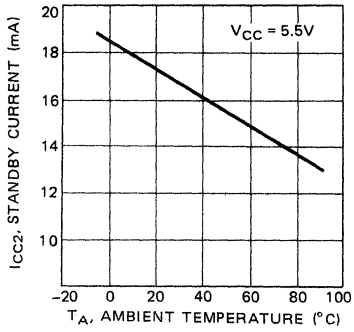


Fig. 13 – REFRESH CURRENT 1 vs CYCLE RATE

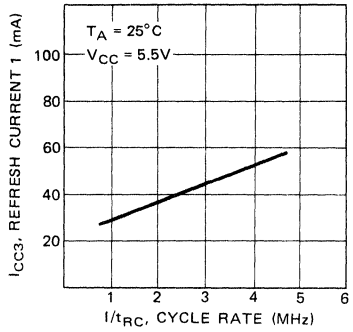


Fig. 14 – REFRESH CURRENT 1 vs SUPPLY VOLTAGE

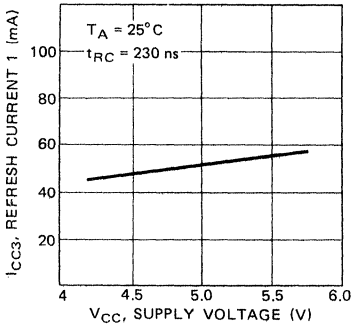


Fig. 15 – PAGE MODE CURRENT vs CYCLE RATE

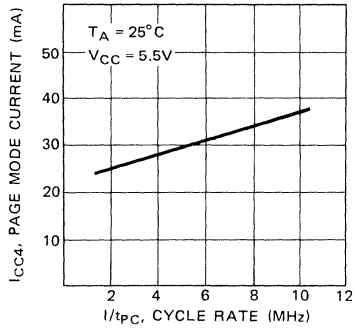


Fig. 16 – PAGE MODE CURRENT vs SUPPLY VOLTAGE

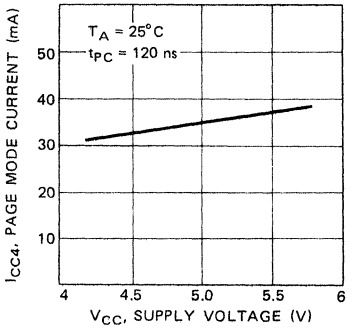


Fig. 17 – REFRESH CURRENT 2 vs CYCLE RATE

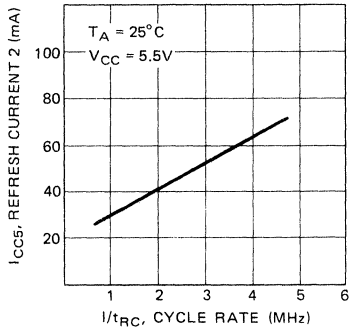


Fig. 18 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

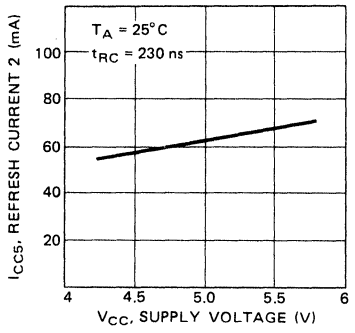


Fig. 19 – TRANSFER MODE CURRENT vs CYCLE RATE

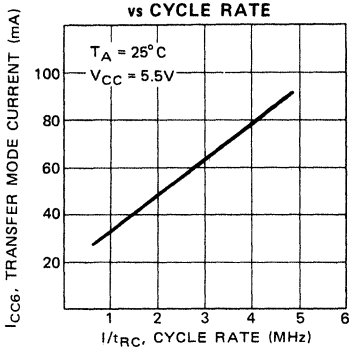


Fig. 20 – TRANSFER MODE CURRENT vs SUPPLY VOLTAGE

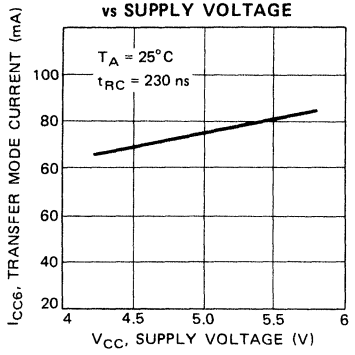


Fig. 21 – RAM STANDBY/SAM ACTIVE CURRENT vs CYCLE RATE

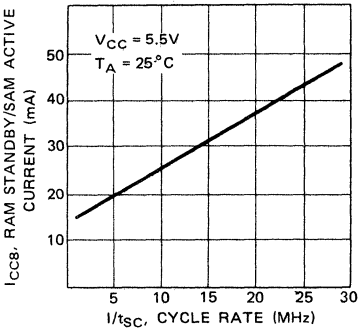


Fig. 22 – RAM STANDBY/SAM ACTIVE CURRENT vs SUPPLY VOLTAGE

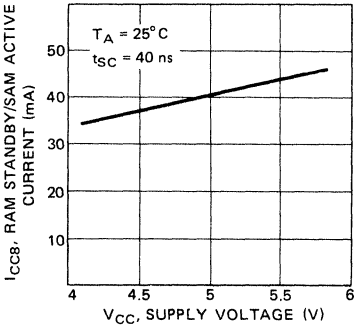


Fig. 23 – RAM STANDBY/SAM ACTIVE CURRENT vs AMBIENT TEMPERATURE

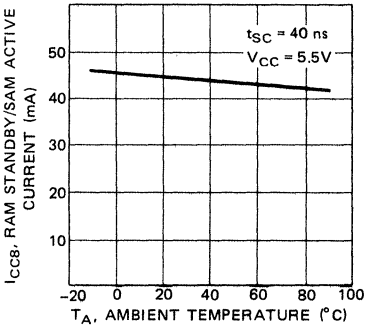


Fig. 24 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

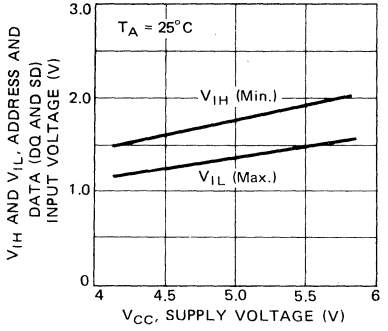


Fig. 25 – ADDRESS AND DATA (DQ AND SD) INPUT VOLTAGE vs SUPPLY VOLTAGE

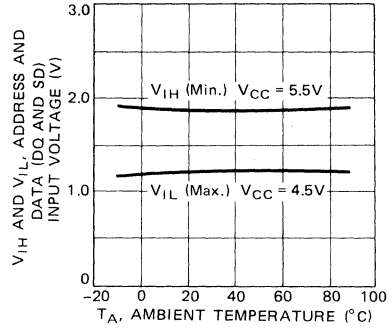


Fig. 26 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs SUPPLY VOLTAGE

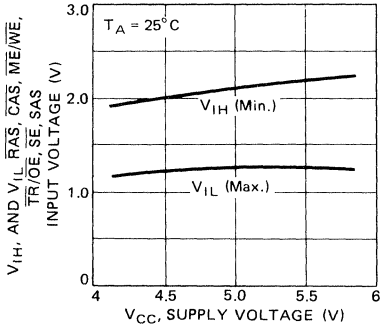


Fig. 27 – $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{WE}$, $\overline{TR}/\overline{OE}$, $\overline{SE}$, SAS INPUT VOLTAGE vs AMBIENT TEMPERATURE

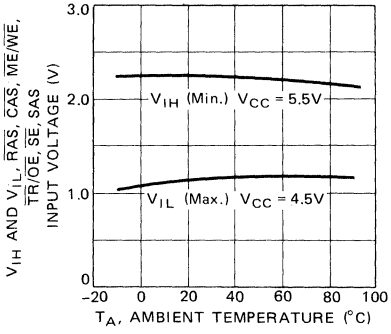


Fig. 28 – ACCESS TIME (RAM) vs LOAD CAPACITANCE

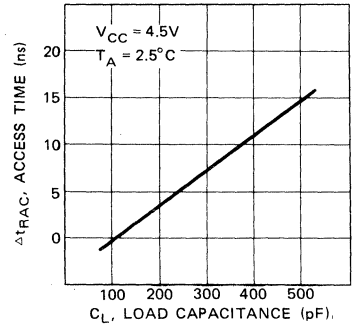


Fig. 29 – ACCESS TIME (SAM) vs LOAD CAPACITANCE

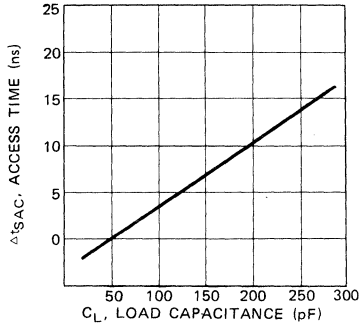


Fig. 30 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

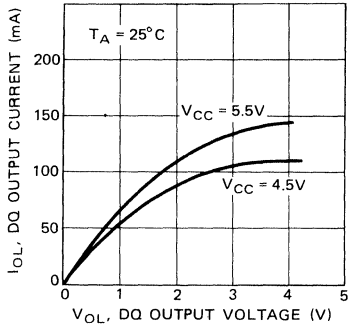


Fig. 31 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

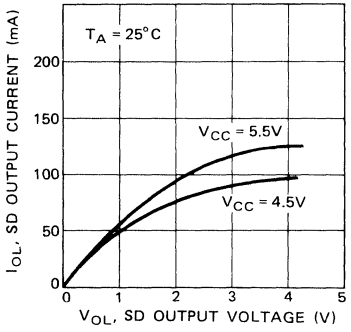


Fig. 32 – DQ OUTPUT CURRENT vs DQ OUTPUT VOLTAGE

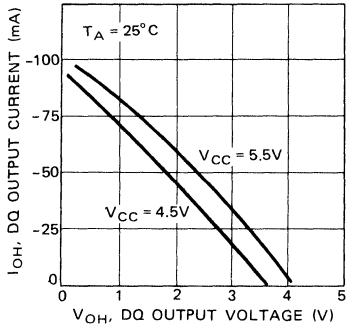


Fig. 33 – SD OUTPUT CURRENT vs SD OUTPUT VOLTAGE

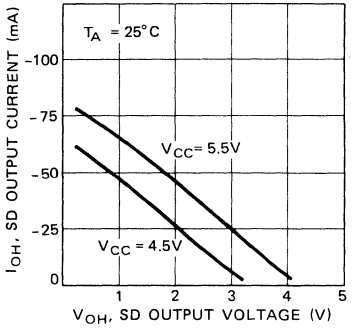
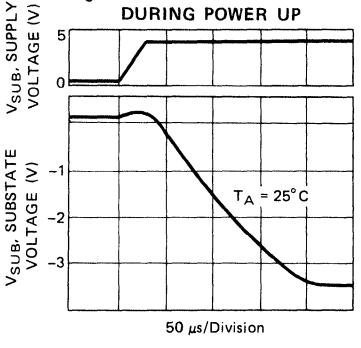


Fig. 34 – SUBSTRATE VOLTAGE DURING POWER UP

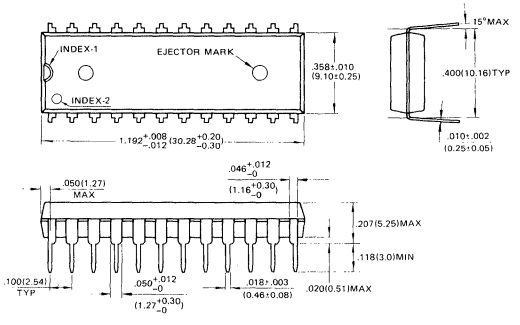


3

PACKAGE DIMENSIONS

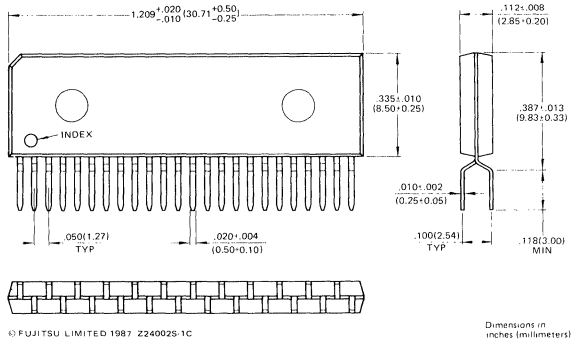
PLASTIC DIP (Suffix: -P) PLASTIC ZIP (Suffix: -PSZ)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-24P-M04)



Dimensions in
inches (millimeters)

24-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-24P-M02)



Dimensions in
inches (millimeters)

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C4251-10/-12/-15

1,048,576 BIT DUAL PORT CMOS DYNAMIC RAM

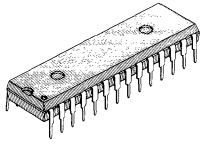
262,144 X 4 Bit Dual Port CMOS Dynamic RAM

ADVANCE INFO.

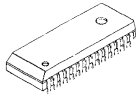
The Fujitsu MB81C4251 is a fully decoded dual port CMOS Dynamic RAM (DRAM) organized as 262,144 words by 4 bits dynamic RAM port and 512 words by 4 bits serial access memory (SAM) port.

The MB81C4251 is ideally suited for mainframes, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Multiplexed row and column address inputs permit the MB81C4251 to behoused in 400mil wide 28 pin DIP, SOJ and ZIP. Pin outs conformed to the JEDEC approved pinout. The MB81C4251 features a Bit Masked Write operation whereby the user can inhibit writing to particular bits.

The MB81C4251 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.



DIP-28P-M06



LCC-28P-M05

T.B.D

ZIP-28P-M01

3

PRODUCT LINE & FEATURES

Parameter		MB81C4251-10	MB81C4251-12	MB81C4251-15
Access Time	DRAM	100ns max.	120ns max.	150ns max.
	SAM	30ns max.	40ns max.	60ns max.
Cycle Time	DRAM	180ns min.	210ns min.	260ns min.
	SAM	30ns min.	40ns min.	60ns min.
Power Dissipation	DRAM ; Active SAM ; Standby	450mW max.	400mW max.	350mW max.
	DRAM ; Standby SAM ; Active	330mW max.	280mW max.	250mW max.
	DRAM ; Standby SAM ; Standby	22mW max.		

- Dual port organization
  262,144 words x 4 bits (DRAM port)
  512 words x 4 bits (SAM port)
- Silicon gate, CMOS, 1 transistor cell
- Single +5V power supply, +/−0.5 V tolerance
- All inputs and outputs are TTL compatible
- 512 refresh cycles every 8.2 ms
- Bi-directional data transfer capability
- Fast serial access asynchronous to DRAM expect transfer operation
- Addressable start location (TAP) on serial shift register
- Realtime Read Transfer capability
- Bit Masked Write Mode capability
- I/O switch by transfer cycle
- Fast page Mode, Read-Modify-Write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	−1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB81C4253-10/-12/-15

1,048,576 BIT DUAL PORT CMOS DYNAMIC RAM

262,144 X 4 Bit Dual Port CMOS Dynamic RAM

The Fujitsu MB81C4253 is a fully decoded dual port CMOS Dynamic RAM (DRAM) organized as 262,144 words by 4 bits dynamic RAM port and 512 words by 4 bits serial access memory (SAM) port.

The MB81C4253 is ideally suited for mainframes, video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Multiplexed row and column address inputs permit the MB81C4253 to behoused in 400mil wide 28 pin DIP, SOJ and ZIP. Pin outs conformed to the JEDEC approved pinout. The MB81C4253 features a Bit Masked Write operation whereby the user can inhibit writing to particular bits, Flash Write operation which is suitable for fast clear, and Mask Write Transfer operation whrereby the user can inhibit write transfer from SAM to RAM per plane.

The MB81C4253 is fabricated using silicon gate CMOS and Fujitsu's advanced triple-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

PRODUCT LINE & FEATURES

Parameter		MB81C4253-10	MB81C4253-12	MB81C4253-15
Access Time	DRAM	100ns max.	120ns max.	150ns max.
	SAM	30ns max.	40ns max.	60ns max.
Cycle Time	DRAM	180ns min.	210ns min.	260ns min.
	SAM	30ns min.	40ns min.	60ns min.
Power Dissipation	DRAM ; Active SAM ; Standby	450mW max.	400mW max.	350mW max.
	DRAM ; Standby SAM ; Active	330mW max.	280mW max.	250mW max.
	DRAM ; Standby SAM ; Standby	22mW max.		

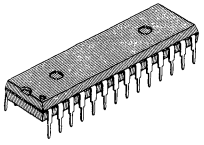
- Dual port organization
  262,144 words x 4 bits (DRAM port)
  512 words x 4 bits (SAM port)
- Silicon gate, CMOS, 1 transistor cell
- Single +5V power supply, +/−0.5V tolerance
- All inputs and outputs are TTL compatible
- 512 refresh cycles every 8.2 ms
- Bi-directional data transfer capability
- Fast serial access asynchronous to DRAM expect transfer operation
- Addressable start location(TAP) on serial shift register
- Realtime Read Transfer capability
- Mask Write Transfer capability
- Bit Masked Write Mode capability
- I/O switch by transfer cycle
- Fast page Mode, Read-Modify-Write Flash Write capability
- $\overline{RAS}$ only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh

ABSOLUTE MAXIMUM RATINGS (see NOTE)

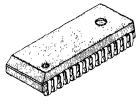
Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	−1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	−1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFO.



DIP-28P-M06



LCC-28P-M05

T.B.D

ZIP-28P-M01

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

October 1989
Edition 1.0

FUJITSU

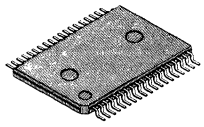
DATA SHEET

MB81C1501

1,175,040 BIT 3 PORT CMOS DYNAMIC FIELD MEMORY

1M Bit 3 Port CMOS Dynamic Field Memory

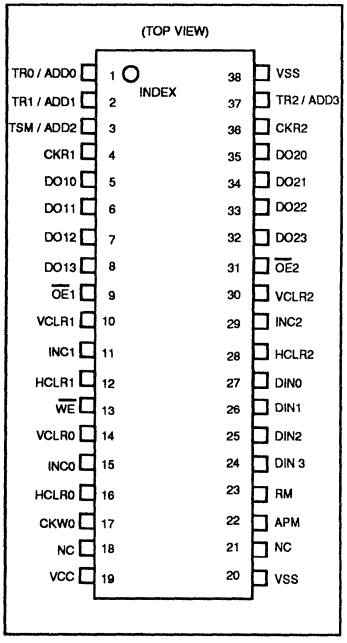
ADVANCE INFO.



FPT-38P-M01

FEATURES

- 3 port organization
  293,760 words x 4bit x 1 (Serial Write Port)
  293,760 words x 4bit x 2 (Serial Read Port)
- Silicon gate, CMOS, 1 transistor cell
- Single +5V +/– 10% supply
- All inputs and outputs are TTL compatible
- 293,760 bit refresh cycle / 21 ms
- Asynchronous operation between 3 ports
- Recursive mode : Automatic increment of vertical and horizontal addresses
- Non recursive mode : Controlled by HCLR, INC and VCLR
- Synchronous signal transfer capability between chip and chip
- Address preset mode per 1 block (60 bits) in a horizontal line (APM = "H")
- Data compression capability by controlling input clock (CKW0) by $\overline{WE}$



PRODUCT LINE

Item		Access Time	Cycle Time		
		(MAX.)	Parameter	(MIN.)	(MAX.)
Read Port		25ns	tSCR	30ns	70ns
Write Port		—	tSCW	50ns	2tSCR
Power Dissipation	Active	250MW (tSCW = tSCR1 = tSCR2 = 70ns) 330MW (tSCW = 70ns, tSCR1 = tSCR2 = 35ns)			
	Refresh	110MW (tSCW =420ns, tSCR = 70ns)			

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	V_{IN}, V_{OUT}	–1 to +7	V
Voltage of V_{CC} supply relative to VSS	V_{CC}	–1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	–55 to +125	° C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Section 4

NMOS DRAM Modules — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
4–3	MB85227–10 –12 –15	100 120 150	2359296 bits (262144w x 9b)	30-pin Plastic SIP

FUJITSU

262144×9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

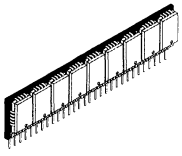
MB85227-10
MB85227-12
MB85227-15

December 1987
Edition 2.0

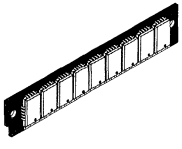
262,144 x 9-BIT DYNAMIC RANDOM ACCESS MEMORY SIP MODULE

This Fujitsu MB85227 is a fully decoded, 262,144 words x 9 bits NMOS dynamic random access memory composed of nine 256K DRAM chips (MB81256 x 9). Assembling nine PLCC chips on a 30 pin PCB, this RAM module is optimized for the applications where high-density and large capacity of storage memory with parity bit is needed.
The electrical characteristics of the MB85227 are the same as the original MB81256; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 262,144 x 9 DRAM, 30-pin SIP (MB81256 x 9)
- Row access time (t_{RAC}),
  100 ns max. (MB85227-10)
  120 ns max. (MB85227-12)
  150 ns max. (MB85227-15)
- Cycle time (t_{RC}),
  200 ns min. (MB85227-10)
  220 ns min. (MB85227-12)
  260 ns min. (MB85227-15)
- Page Cycle Time (t_{PC}),
  100 ns min (MB85227-10)
  120 ns min (MB85227-12)
  150 ns min. (MB85227-15)
- Single +5V supply, ±10% tolerance
- Low power (active)
  3465 mW max. (MB85227-10)
  3213 mW max. (MB85227-12)
  2822 mW max. (MB85227-15)
  226 mW max. (Standby)
- 4 ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability
- Page Mode Capability
- On-chip latches for Addresses and Data-in
- Leaded and Leadless types are available
- Compatible with TM4256EL9/TM4256EU9 and MH25609J
- Standard Leaded Epoxy SIP (Suffix: PDPS)
- Standard Leadless Epoxy SIM (Suffix: PDPB)

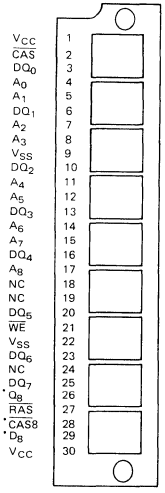


PLASTIC PACKAGE
MSP-30P-P02



PLASTIC PACKAGE
MSS-30P-P01

PIN ASSIGNMENT



* ; For parity bit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to 125	°C
Power dissipation	P_D	4.5	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – FUNCTIONAL BLOCK DIAGRAM

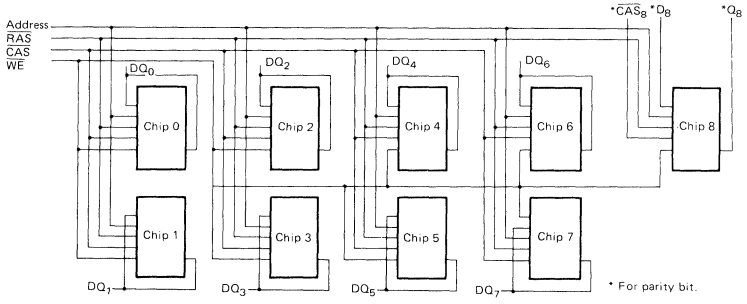
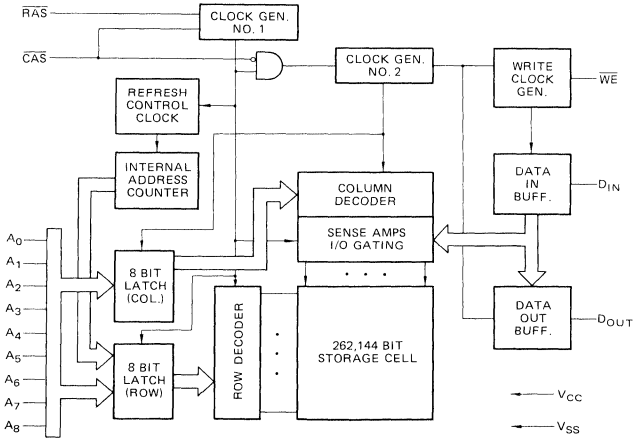


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8	C_{IN1}		75	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}		80	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		55	pF
Input Capacitance, $\overline{CAS8}$	C_{IN5}		10	pF
Input Capacitance, D_8	C_{IN6}		7	pF
I/O Capacitance, DQ_0 to DQ_7	C_D		17	pF
Output Capacitance, Q_8	C_O		12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C*
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	-2.0	–	0.8	V	

Note * : Maximum ambient temperature is permissible under certain conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for page mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling; t_{RC} = Min.)	MB85227-10	I_{CC1}		630	mA
	MB85227-12			585	
	MB85227-15			513	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{CAS8}$ = V_{IH})		I_{CC2}		41	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ = V_{IH}; t_{RC} = Min.)	MB85227-10	I_{CC3}		540	mA
	MB85227-12			495	
	MB85227-15			450	
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling; t_{PC} = Min.)	MB85227-10	I_{CC4}		315	mA
	MB85227-12			270	
	MB85227-15			225	
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = Min.)	MB85227-10	I_{CC5}		585	mA
	MB85227-12			540	
	MB85227-15			495	
INPUT LEAKAGE CURRENT (Except for DQ_0 to DQ_7) Input Leakage Current, Any Input ($0 \leqq V_{IN} \leqq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)1}$ ($\overline{CAS8}$, D8)	-10	10	μA
		$I_{I(L)2}$ (Others)	-90	90	
DQ and Q8 LEAKAGE CURRENT (Data out is disabled, $0V \leqq V_{OUT} \leqq 5.5V$) Each DQ is high impedance		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = -5 mA) Output Low Voltage (I_{OL} = -4.2 mA)		V_{OH} V_{OL}	2.4	0.4	V

Note 1): I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

4

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB85227-10		MB85227-12		MB85227-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		4		4		4	ms
Random Read/Write Cycle Time	4	t_{RC}	200		220		260		ns
Access Time from $\overline{RAS}$	5 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	6 7	t_{CAC}		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	0	25	0	25	0	30	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delat Time	8 9	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	10		10		10		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		12		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		20		25		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time		t_{WCS}	0		0		0		ns
Write Command Pulse Width		t_{WP}	15		20		25		ns
Write Command Hold Time		t_{WCH}	15		20		25		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCH}	20		25		30		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

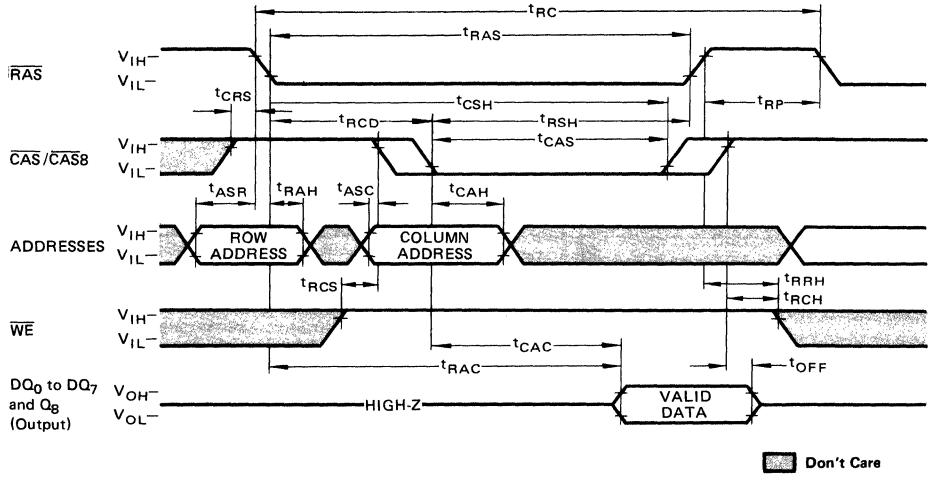
Parameter	NOTES	Symbol	MB85227-10		MB85227-12		MB85227-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	20		20		20		ns
Page Mode Read/Write Cycle Time	11	t_{PC}	100		120		150		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	40		50		65		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{CPR}	20		25		30		ns
Write Command to $\overline{RAS}$ Lead Time	12	t_{RWL}	40		50		60		ns
Write Command to $\overline{CAS}$ Lead Time	12	t_{CWL}	40		50		60		ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	12	t_{CWD}	15		20		25		ns
Read-Write Cycle Time	12	t_{RWC}	200		220		260		ns

4

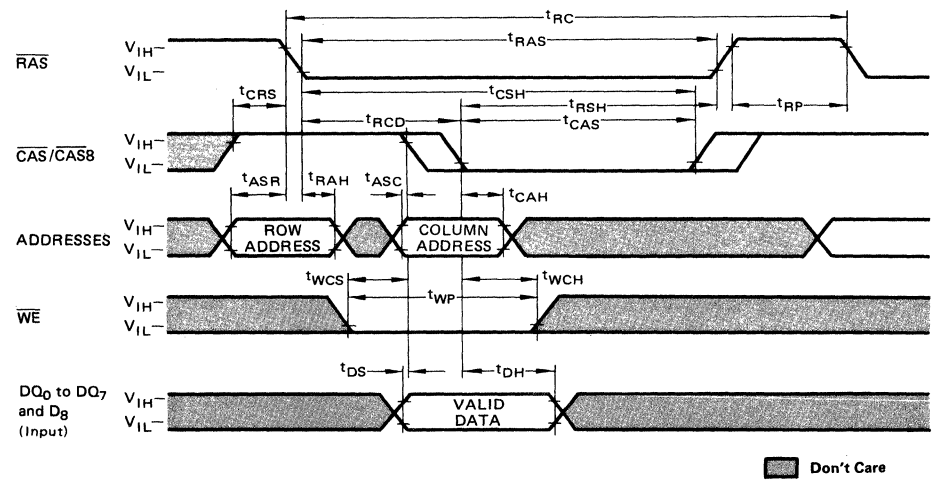
Notes:

1. An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
   If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are refrence levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
   See Fig. 3 for durating curve.
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
8. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5 ns) + t_{ASC} (min).
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. The minimum cycle time is dependent on the ambient temperature and cooling conditions.
    See Fig. 4 for derating curve.
12. Only for parity bit.

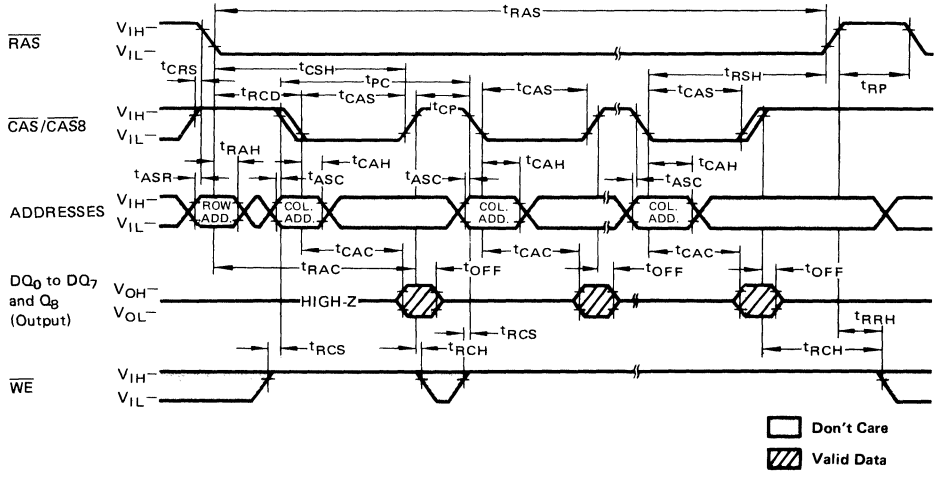
Read Cycle



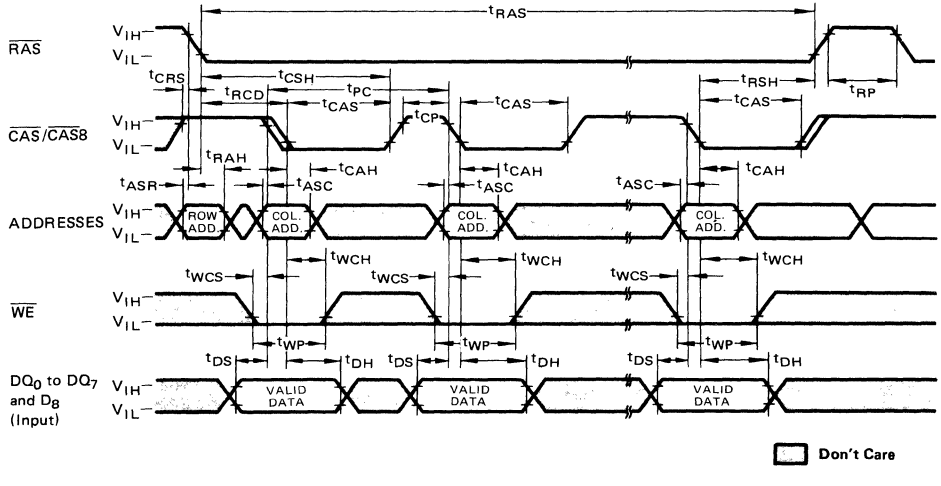
Write Cycle



Page Mode Read Cycle

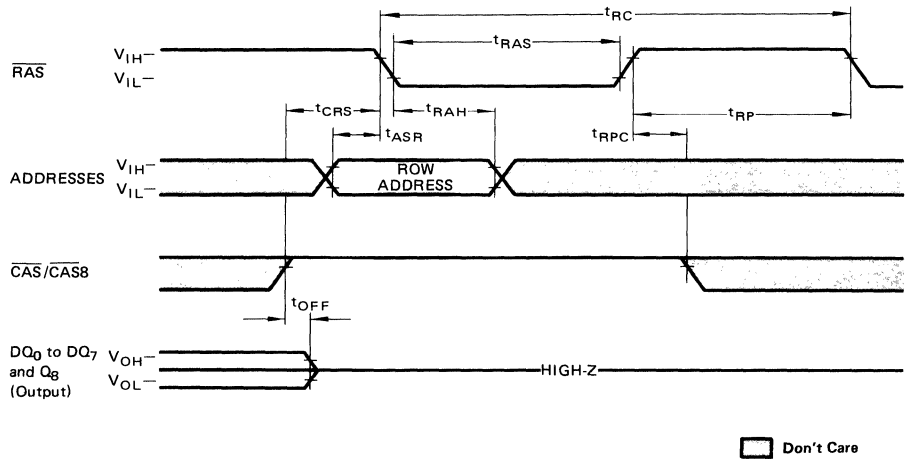


Page Mode Write Cycle



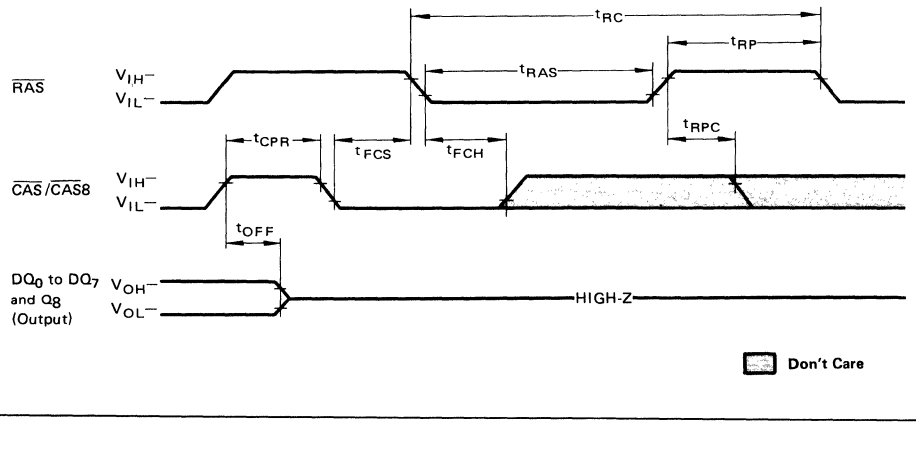
$\overline{RAS}$-only Refresh Cycle

NOTE: $\overline{WE}$, and D_8 = Don't Care

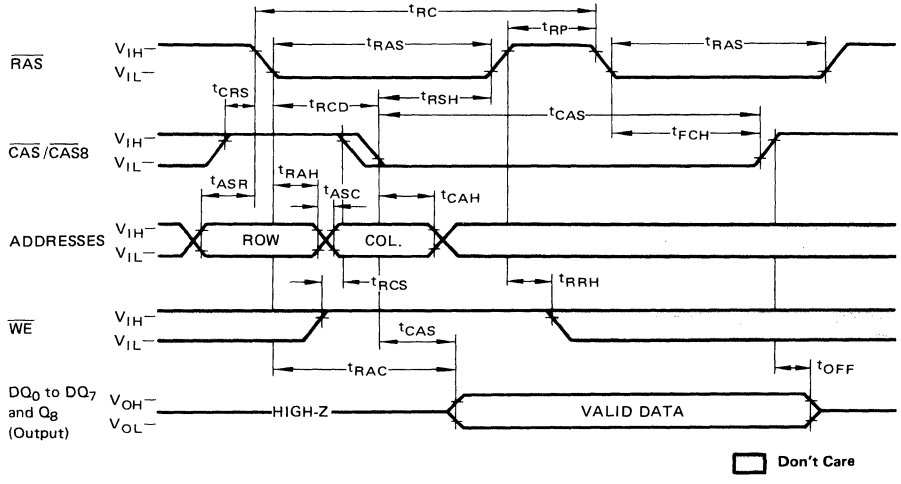


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

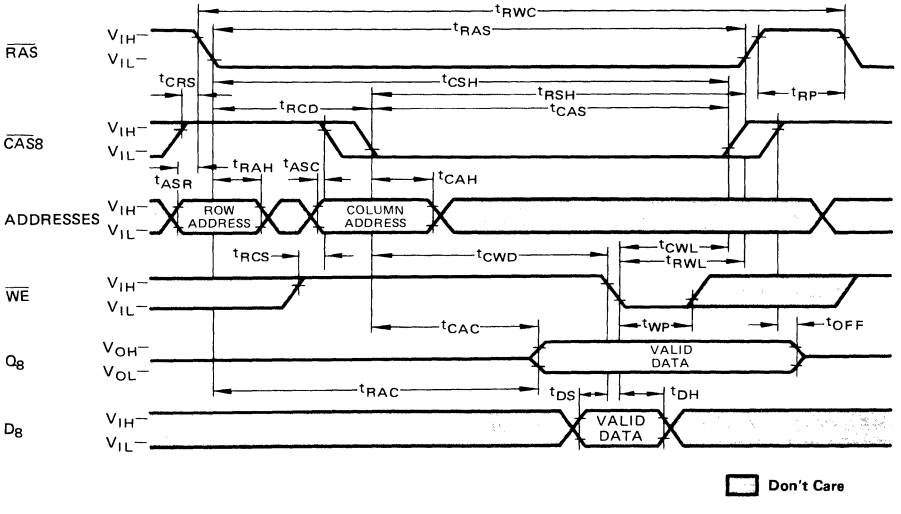
NOTE: Address, $\overline{WE}$, and D_8 = Don't Care



Hidden Refresh Cycle



Read–Write/Read–Modify–Write Cycle*



* ; Only for parity bit.

FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1)]	Ready cycle
L	L	L	Valid Data In[2)]	Write cycle
L	L[3)]	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L[4)]	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Pairyt bit) Read-Write/Read-Modify-Write (Parity bit)

Notes: 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geqq t_{FCS}$ (min)
4): $t_{CWD} \geqq t_{CWD}$ (min)

DESCRIPTION

Simple Timing Requirement:
The MB 85227 has improved circuitry that eases timing requirements for high speed access operations. The MB 85227 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB 85227 has the minimal hold times of address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). The MB 85227 provides higher throughput in interleaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, and t_{DHR}. As a result, the hold times of the column address, D_{IN} and $\overline{WE}$ are not restricted by t_{RCD}.

Address Inputs:
A total of eighteen binary input address bits are required to decode any 9 bits data of 2359296 storage cells within the MB 85227.
Nine row address bits are established on the input pin (A_0 through A_8) and latched with $\overline{RAS}$.
Nine columns address bits are established on the input pins and latched with $\overline{CAS}$ and $\overline{CAS}8$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ and $\overline{CAS}8$ are internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ and $\overline{CAS}8$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on the $\overline{WE}$ selects read mode, low selects write mode. Data inputs are disabled when read mode is selected.

Data Pins:
The input and output pins of each PLCC except for parity bit are directly connected on the mother board to minimized the number of I/O pins. The write cycle should be early write cycle in order to avoid data conflict between output data and input data. However, it is possible to execute read-modify-write cycle on the parity bit because the input & output of parity bit are separated.

Data Input:
The 9 bits data are written through the DQ pins (DQ_0 to DQ_7 and D_8) during write (early write) cycle.
The falling edge of $\overline{CAS}$ and $\overline{CAS}8$ are triggered for the data input register. The set up and hold times are referenced to $\overline{CAS}$ and $\overline{CAS}8$.

Data Output:
The output buffer of each chips are three state TTL compatible with a fan out of two standard TTL loads.
The outputs are in high impedance state until $\overline{CAS}$ and $\overline{CAS}8$ are brought low. In a read cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ and $\overline{CAS}8$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ and $\overline{CAS}8$ are returned to a high level.

Page-Mode:
Page-mode operation permits strobing the row-address into the MB 85227 while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each 256 row address (A_0 through A_7 of the at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.
The MB 85227 offers the following three types of refresh.

1) $\overline{RAS}$-only Refresh;
   $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ and $\overline{CAS}8$ are brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB 85227 offers an alternate refresh method. If $\overline{CAS}$ and $\overline{CAS}8$ are held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter on each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. So, by performing 256 cycles for $\overline{CAS}$-before-$\overline{RAS}$ refresh, all bits in a module are refreshed.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ and $\overline{CAS}8$ active time. In MB 85227, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address and used, that is no external refresh address is needed.

Notice for using MB 85227
The MB 85227 is a SIP (Single-In-Line-Package) module which is composed of nine MB 81256 DRAMs housed in plastic LCC, and assembled on the epoxy printed circuit board. Generally the multilayer PCB board has large wiring capacitance. This disadvantage causes relatively noise induction between signal lines and power supply lines (V_{SS} or V_{CC}).
Furthermore, as the MB 85227 is a very high-speed memory, the timing windows to strobe address $\overline{WE}$ and D_{IN} signals are very short (Approx. 5 ns). Therefore, it is very sensitive even to very sharp noise.
From the above reasons, special care should be taken for use the MB 85227. The following notices are recommended;

4

DESCRIPTION

1. Provide a externally capacitor of approx. a few μF each module, the MB 85227 has the nine decoupling capacitors (0.22 μF on each module 0.22 μF x 9).
2. Remove noise, riging, overshoot and undershoot from the address, clocks and DQ lines, so that the MB 85227 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 – MB 85227 DERATING CURVE (Normal Cycle)

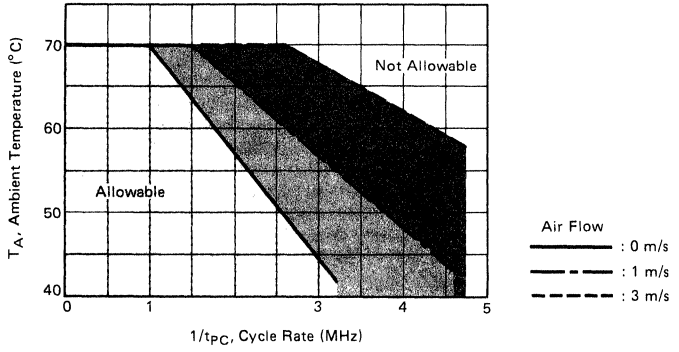
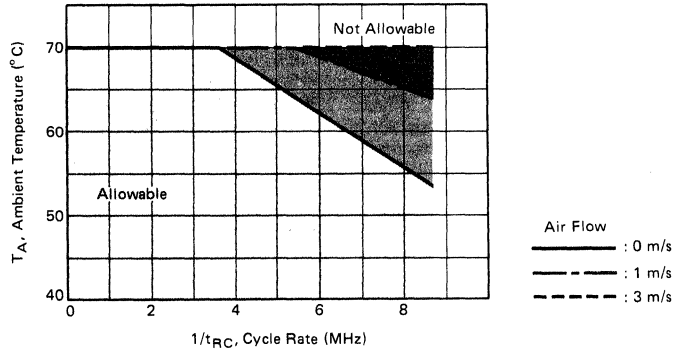
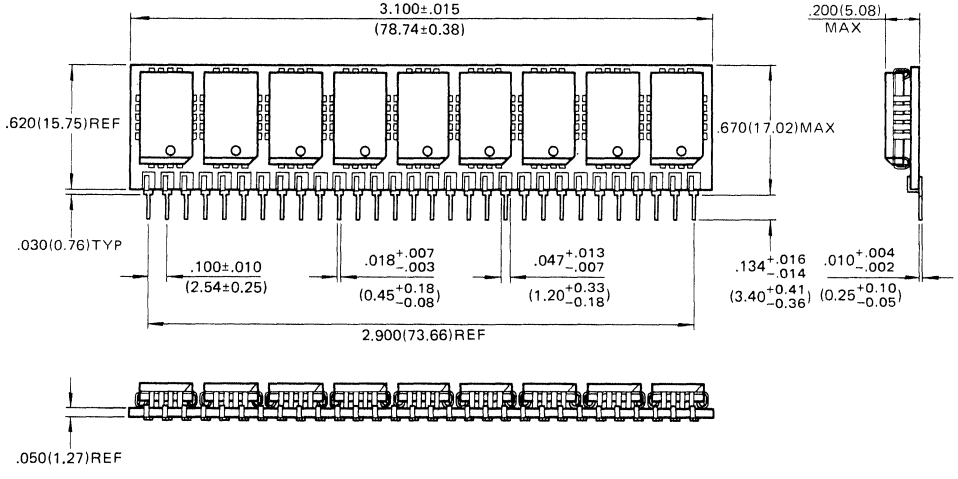


Fig. 4 – MB 85227 DERATING CURVE (Page Mode Cycle)



PACKAGE DIMENSIONS

30-LEAD SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P02)

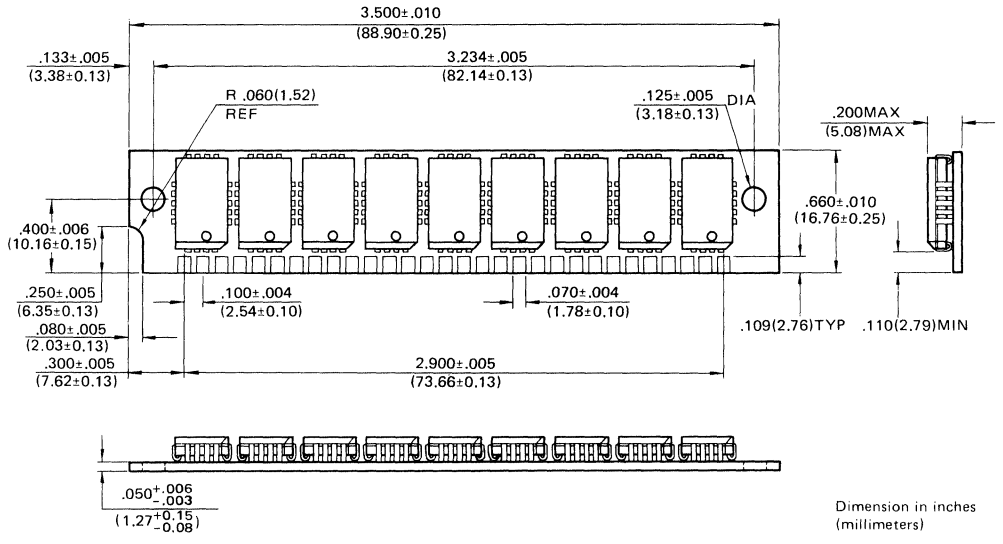


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

30-PAD PLASTIC SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSS-30P-P01)



4

Section 5

CMOS DRAM Modules — *At a Glance*

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
5–3	MB85230–10	100	8388608 bits	30-pin Plastic SIP
	–12	120	(1048576w x 8b)	30-pad Plastic SIMM
5–21	MB85231–10	100	8388608 bits	30-pin Plastic SIP
	–12	120	(1048576w x 8b)	30-pad Plastic SIMM
5–38	MB85235–10	100	9437184 bits	30-pin Plastic SIP
	–12	120	(1048576w x 9b)	30-pad Plastic SIMM
5–55	MB85237–10	100	9437184 bits	30-pin Plastic SIP
	–12	120	(1048576w x 9b)	30-pad Plastic SIMM
5–73	MB85240–10	100	2359296 bits	30-pin Plastic SIP
	–12	120	(262144w x 9b)	30-pad Plastic SIMM
5–89	MB85254–80	80	20971520 bits	72-pin Plastic SIMM
	–10	100	(524288w x 40b)	
	–12	120		
5–93	MB85260–10	100	8388608 bits	30-pin Plastic SIP
	–12	120	(1048576w x 8b)	
5–107	MB85265–10	100	9437184 bits	30-pin Plastic SIP
	–12	120	(1048576w x 9b)	

FUJITSU

1,048,576 × 8 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

MB85230-10
MB85230-12

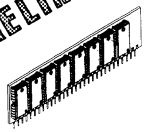
May 1988
Edition 1.0

1M x 8 BIT DYNAMIC RANDOM ACCESS MEMORY SIP MODULE

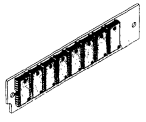
The Fujitsu MB85230 is a fully decoded, dynamic CMOS random access memory modulew with eight MB81C1000, in 26-pin SOJ packages, and eight .22µF decoupling capacitor under the each memory, mounted on a 30-pin SIP or a 30-pad SIMM module. Organized as 1,048,576 x 8-bit words, the MB85230 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85230 are the same as the MB81C1000 devices which feature a Fast Page mode operation.

- 1,048,576 x 8 DRAM, 30-pin SIP and SIMM
- Row access time (t_{RAC}):
  100 ns max. (MB85230-10)
  120 ns max. (MB85230-12)
- Cycle time (t_{RC}):
  180 ns min. (MB85230-10)
  210 ns max. (MB85230-12)
- Column access time (t_{CAC}):
  30 ns max. (MB85230-10)
  35 ns max. (MB85230-12)
- Fast Page mode cycle time (t_{PC}):
  60 ns max. (MB85230-10)
  70 ns max. (MB85230-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  Active = 2640 mW max. (MB85230-10)
  2200 mW max. (MB85230-12)
  Standby = 44 mW max. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capabilities
- TTL compatible inputs and outputs
- Leaded and Leadless type are available.
- JEDEC standard (30-pin SIP) pin assignment

PRELIMINARY

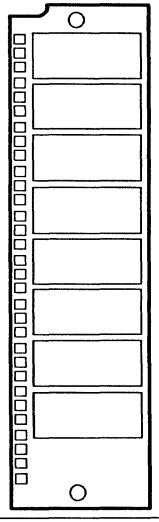


MSP-30P-P05



MSS-30P-P04

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	8.0	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 – BLOCK DIAGRAM

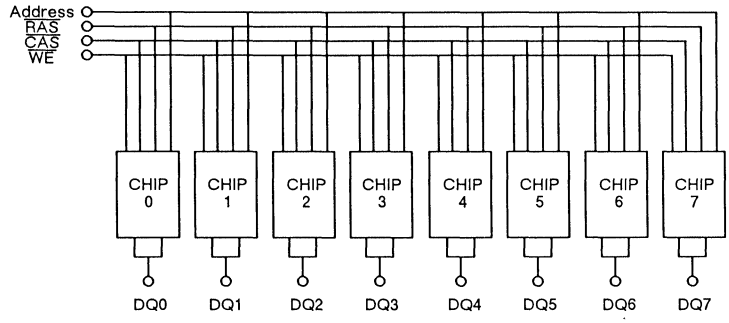
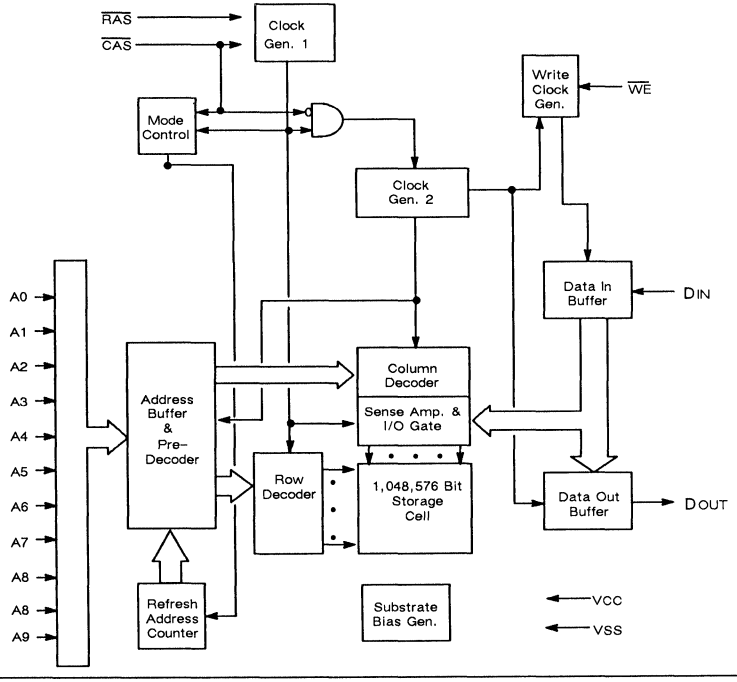


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



5

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Value		Unit
		Typ	Max	
Address Input Capacitance	C_{IN1}		56	pF
$\overline{RAS}$ pin Capacitance	C_{IN2}		47	pF
$\overline{CAS}$ pin Capacitance	C_{IN3}		49	pF
$\overline{WE}$ pin Capacitance	C_{IN4}		46	pF
DQ pin Capacitance	C_{DQ}		14	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Level	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0 *1		0.8 0.8	V V
Operating Temperature	T_A	0	25	70 *2	V

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

5

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	-10	I_{CC1}			480	mA
	-12				400	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL	I_{CC2}			16	mA
	CMOS				8	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}; $\overline{RAS}$=min cycling)	-10	I_{CC3}			440	mA
	-12				360	
FAST PAGE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=min cycling)	-10	I_{CC4}			320	mA
	-12				264	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	-10	I_{CC5}			440	mA
	-12				360	
INPUT LEAKAGE CURRENT		I_{IL}	-30		30	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5MA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

5

AC CHARACTERISTICS

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85230-10		MB85230-12		Unit
			Min.	Max.	Min.	Max.	
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from $\overline{RAS}$	5,8	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	7		7		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to RAS Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to CAS Delay Time	10,11	t_{RCD}	25	70	25	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
$\overline{RAS}$ to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
Fast Page Mode Read/Write Cycle Time		t_{PC}	60		70		ns
Access Time from $\overline{CAS}$ Precharge	8,15	t_{CPA}		60		70	ns
Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		15		ns

5

AC CHARACTERISTICS (Continued)

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter / NOTES	Symbol	MB85230-10		MB85230-12		Unit
		Min.	Max.	Min.	Max.	
$\overline{CAS}$ Precharge Time	t_{CPN}	15		15		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		20		ns

NOTES:

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig. 3 and 4.
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 5 and 6.
6. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{CAC}.
7. If $t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{AA}.
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. t_{OFF} is specified that output buffer changes to high impedance state.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RAC} (max) is specifies as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAS} or t_{AA}.
11. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WCS} is specified as a reference point only and must be satisfied for a write cycle.
15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from V_{IL} to V_{IH}.). Therefore, if t_{CP} is short, t_{CAC} is longer than t_{CAC} (max).

Fig. 3 – MB85230 DERATING CURVE (Normal Cycle)

T.B.D.

Fig. 4 – MB85230 DERATING CURVE (Fast Page Mode Cycle)

T.B.D.

5

Fig. 5 – tRAC vs tRCD

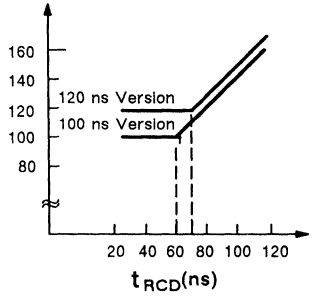
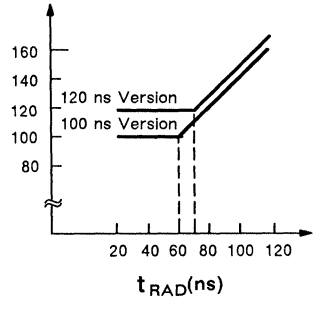
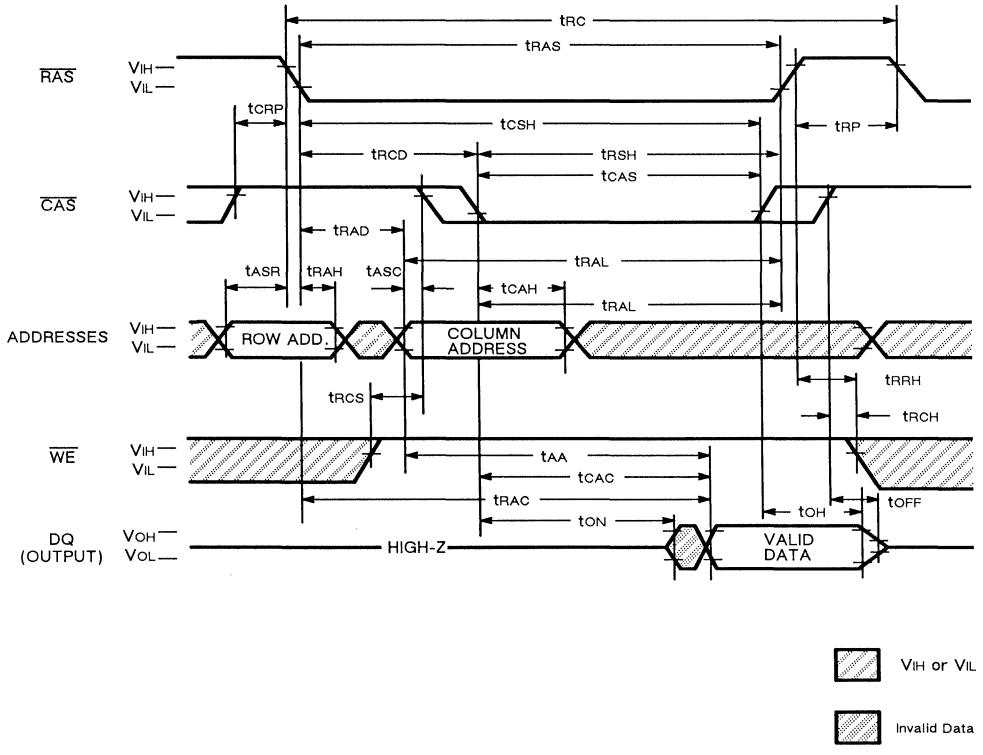


Fig. 6 – tRAC vs tRAD

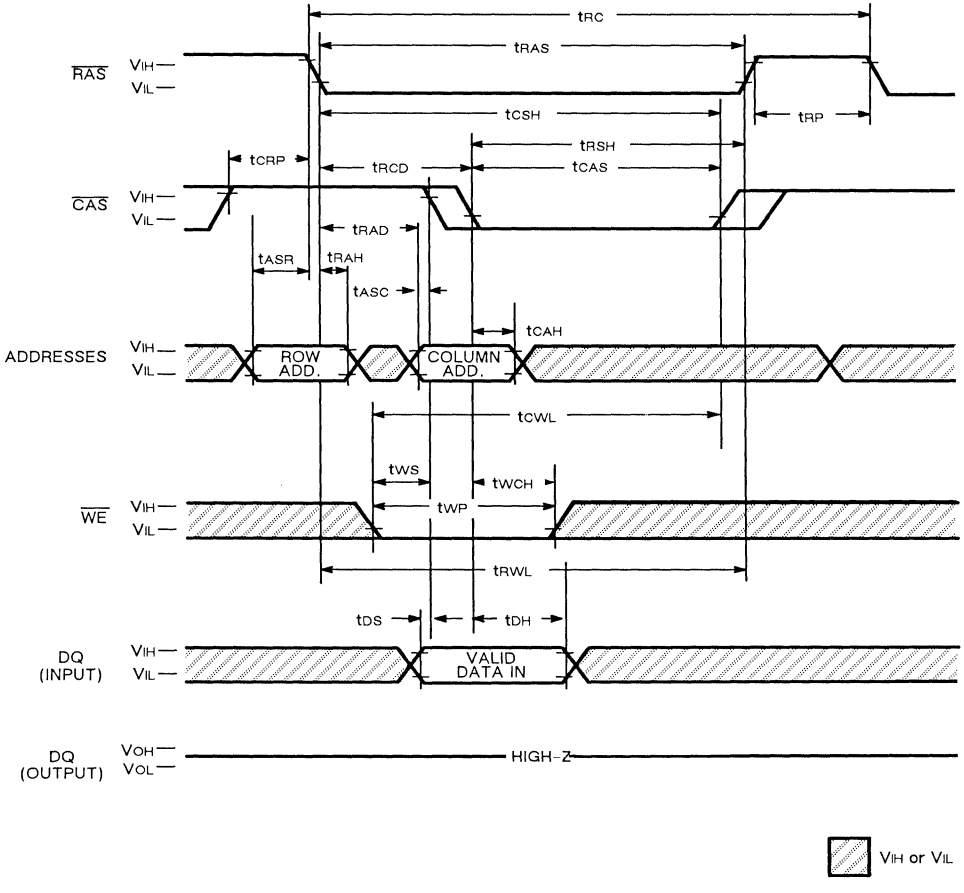


READ CYCLE

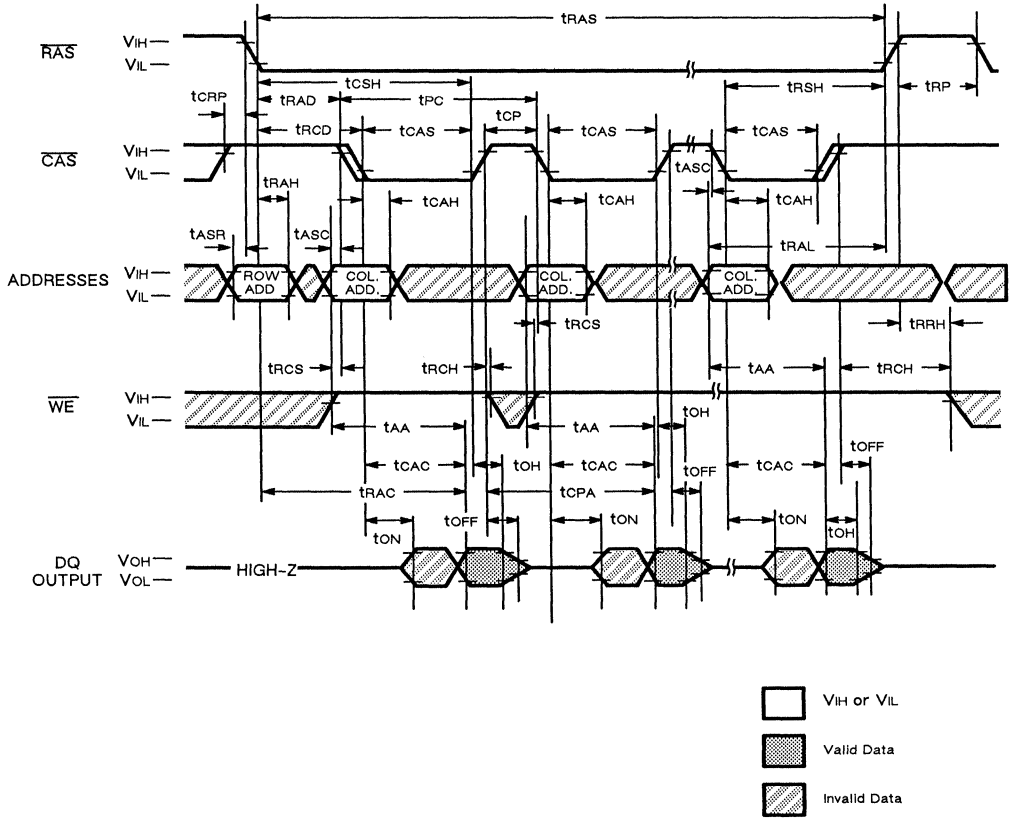

tRC
tRAS
RAS
VIH
VIL
tCRP
tCSH
tRP
tRCD
tRSH
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
tRAL
ADDRESSES
ROW ADD.
COLUMN ADDRESS
tRRH
tRCS
tRCH
WE
tAA
tCAC
tRAC
tOH
tOFF
tON
DQ (OUTPUT)
VOH
VOL
HIGH-Z
VALID DATA
VIH or VIL
Invalid Data

5

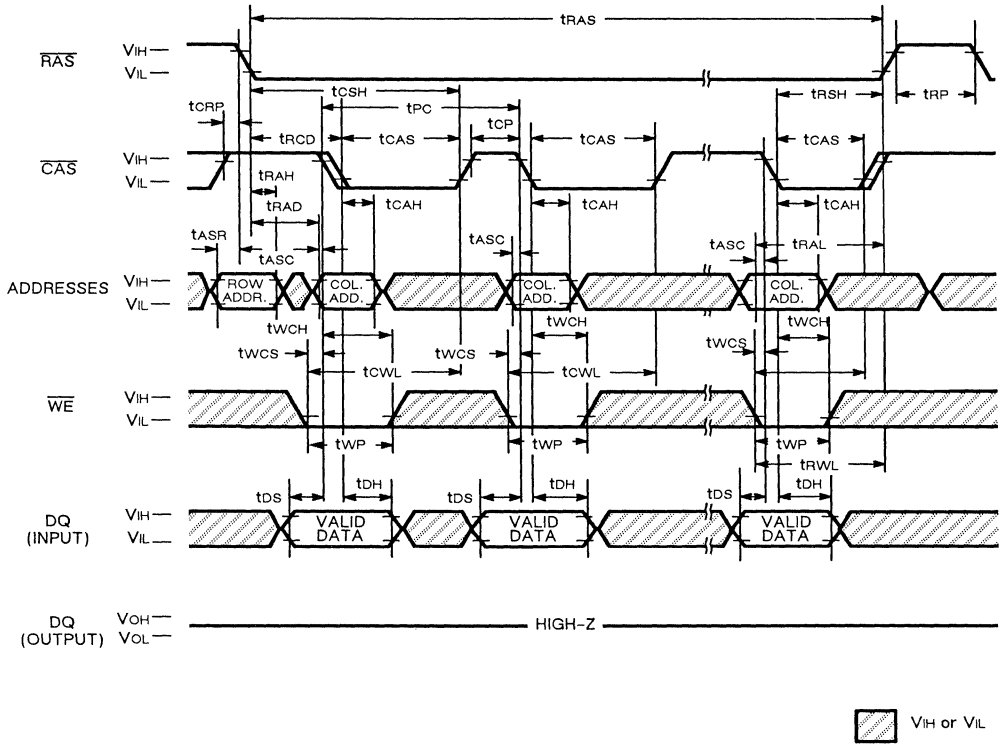
WRITE CYCLE (Early Write)



FAST PAGE MODE READ CYCLE



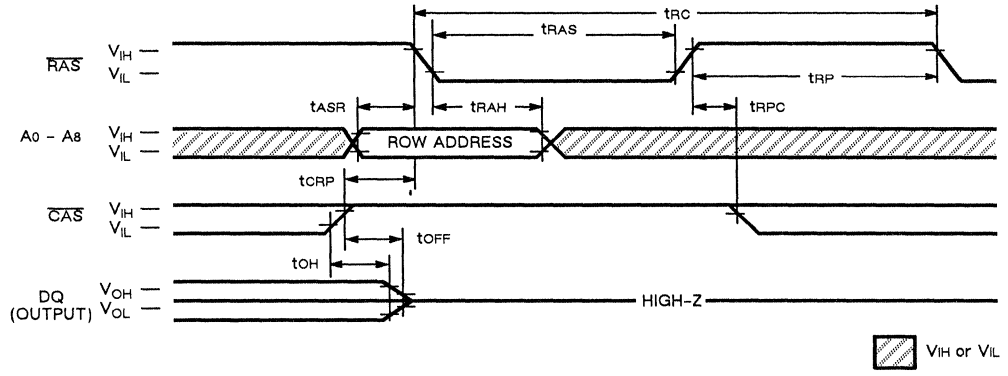
FAST PAGE MODE WRITE CYCLE



5

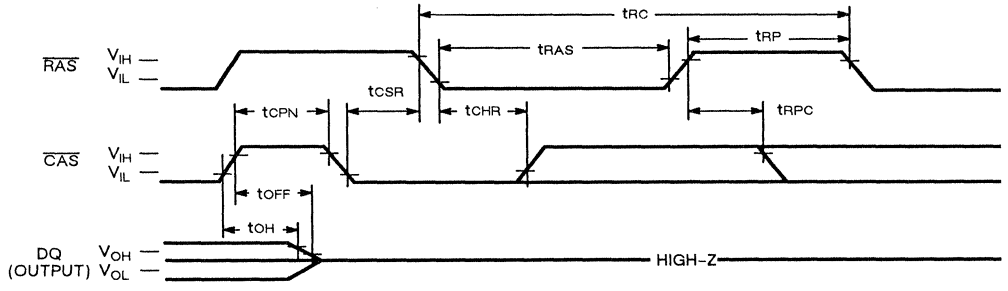
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{WE}$, DQ(Input)=Don't care, A9 = VIH or VIL



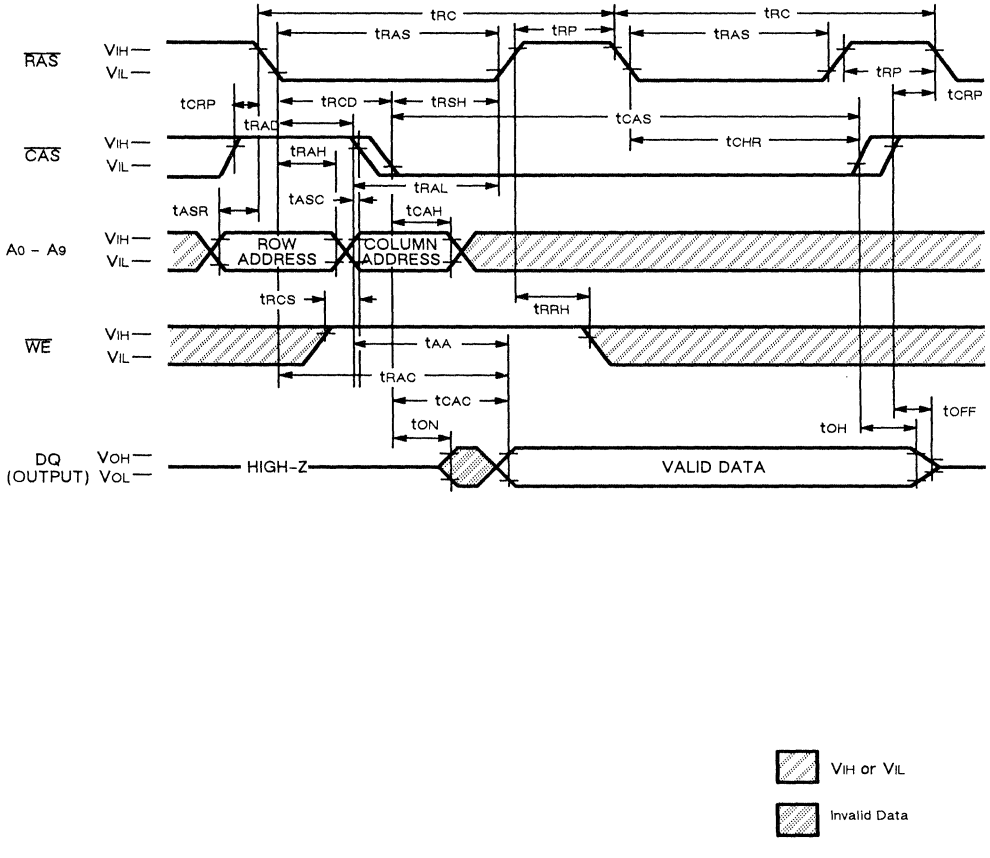
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{WE}$, DIN = Don't Care



5

HIDDEN REFRESH CYCLE



5

DESCRIPTION

Block Analysis:
As shown in Fig. 1 and Fig. 2, the MB85230 is composed of eight MB81C1000, and the memory selection of the each MB81C1000 consists of a 1024-by-1024 cell matrix.
Operational modes of the device are shown in the FUNCTIONAL TRUTH TABLE below.

Address Inputs:
A total of twenty binary input address bits are required to decde any 8-bit of the 8,388,608 storage cells within the MB85230. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins(A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min)+ t_T. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:
Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:

1. **Data Input;**
   In write cycle, the 8-bit data is written into the MB85230 during write cycle through each DQ pins. Each input data is strobed and latched by falling edge of $\overline{CAS}$, and $\overline{WE}$ must be brought to V_{IL} before falling edge of $\overline{CAS}$, data input strobed by $\overline{CAS}$, and setup and hold times are referenced to $\overline{CAS}$.

2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}$.
   The data output remans valid until $\overline{CAS}$ returns to high.

5

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$=V_{IL} and keeping $\overline{WE}$=V_{IH} throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The output data is remain valid with $\overline{CAS}$=V_{IL}, i.e., if $\overline{CAS}$ goes V_{IH}, the data becomes invalid with t_{OH}. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input (t_{AA}). If t_{RCD}($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:
The write cycle is executed is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 8-bit data on DQ pins are latched with the falling edge of $\overline{CAS}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

Fast Page Mode Read Cycle:
The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$=V_{IL}, applying column address and $\overline{CAS}$, and keeping $\overline{WE}$=V_{IH}. Since the row address during fast page mode cycle is latched by normal cycle, the cycle time is reduced. During this mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occur later. Any of the 1024 bits belonging to each internal row address can be accessed.

Fast Page Mode Write Cycle:
The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of WE. The data on each DQ is latched with the falling edge of $\overline{CAS}$ and written into the memory. During this write cycle, t_{CWL} must be satisfied. Any of 1024 bits belonging to each internal row address can be accessed.

DESCRIPTION (Continued)

Refresh:
The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85230 also has three types of refresh modes, $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$=V_{IL} and keeping $\overline{CAS}$=V_{IH} through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the DQ pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$=V_{IL} before $\overline{RAS}$. By this combination, the MB85230 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is execute dby keeping $\overline{CAS}$=V_{IL} to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept V_{IL} continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

5

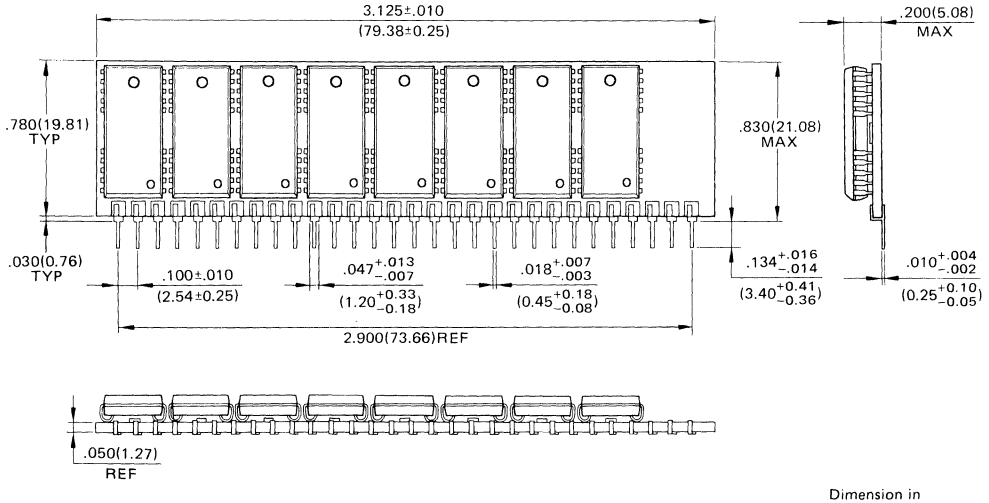
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CRS} \geq t_{CRS}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X: Don't Care
*; $\overline{RAS}$ puts V_{IH} at once.

PACKAGE DIMENSIONS

30-LEAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P05)

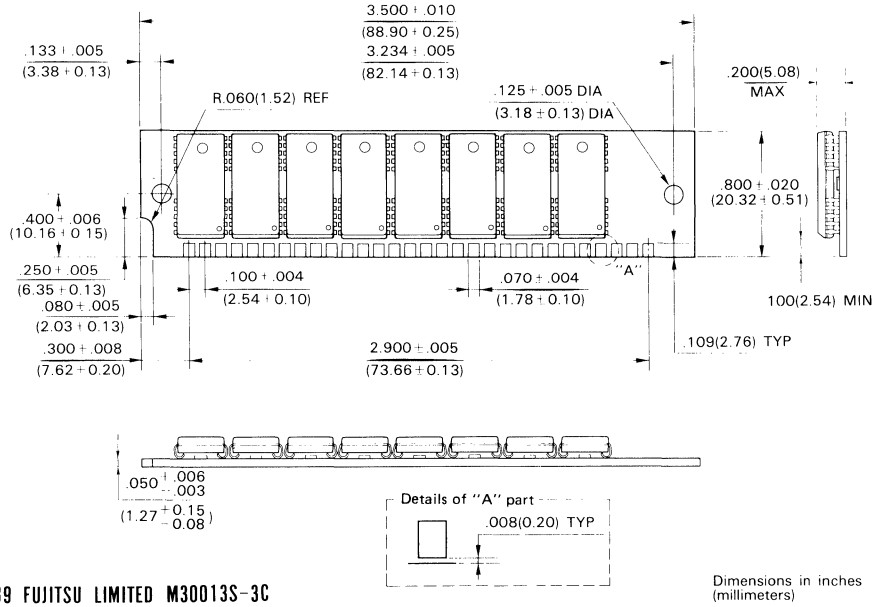


Dimension in
inches (millimeters)

5

PACKAGE DIMENSIONS (Continued)

30-LEAD PLASTIC MODULE (SOCKET TYPE)
(Case No. : MSS-30P-P04)



Dimensions in inches
(millimeters)

5

5

1M x 8 DRAM MODULE

MB85231-10
MB85231-12

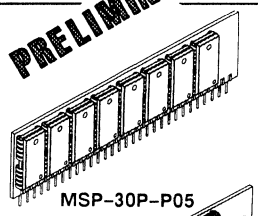
July 1988
Edition 1.0

1,048,576 x 8 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

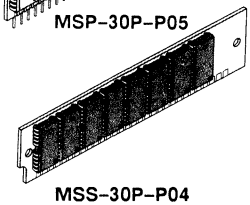
The Fujitsu MB85231 is a fully decoded, dynamic CMOS random access memory module with eight MB81C1001, in 26-pin SOJ packages, and eight .22µF decoupling capacitor under the each memory, mounted on a 30-pin SIP or a 30-pad SIMM module. Organized as 1,048,576 x 8-bit words, the MB85231 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85231 are the same as the MB81C1001 devices which feature a Nibble mode operation.

- 1,048,576 x 8 DRAM, 30-pin SIP and SIMM
- RAS access time (t_{RAC}):
  100 ns max. (MB85231-10)
  120 ns max. (MB85231-12)
- Cycle time (t_{RC}):
  180 ns min. (MB85231-10)
  210 ns max. (MB85231-12)
- Column access time (t_{CAC}):
  30 ns max. (MB85231-10)
  35 ns max. (MB85231-12)
- Nibble mode cycle time (t_{NC}):
  50 ns max. (MB85231-10)
  55 ns max. (MB85231-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  Active = 2640 mWmax. (MB85231-10)
  2200mW max. (MB85231-12)
  Standby = 44 mWmax. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capability
- Nibble Mode Read and Write capability
- Leaded and Leadless type are available.
- JEDEC standard (30 pin SIP) pin assignment

PRELIMINARY

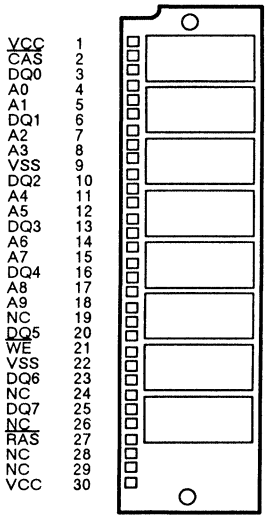


MSP-30P-P05



MSS-30P-P04

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	8.0	W
Short circuit output current	—	50	mA

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - BLOCK DIAGRAM

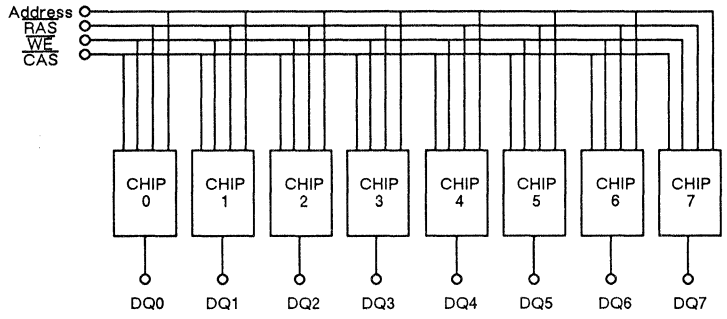
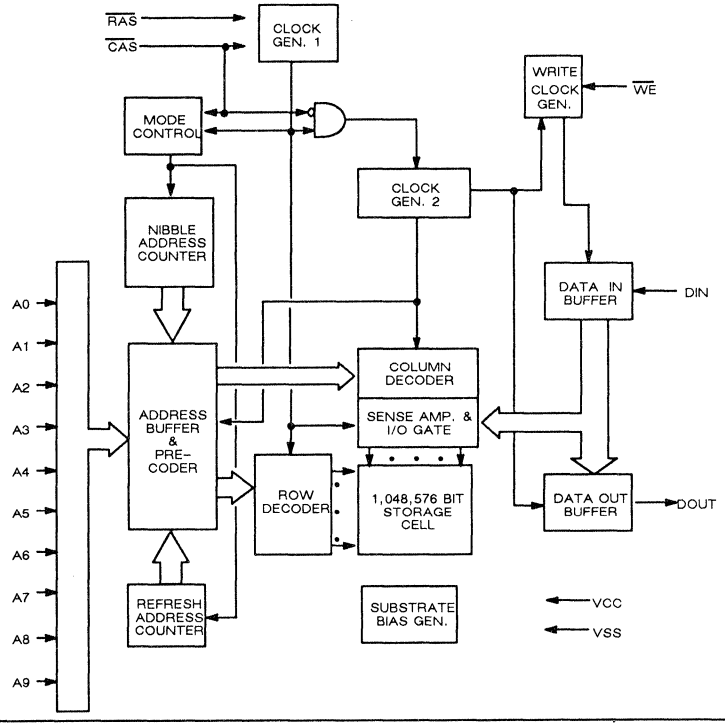


Fig. 2 - BLOCK DIAGRAM FOR EACH CHIP



5

CAPACITANCE (TA=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	—	56	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}	—	47	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}	—	49	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	46	pF
I/O Capacitance, DQ0 to DQ7	C_{DQ}		14	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Leve, all inputs	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0*1		0.8 0.8	V V
Operating Temperature Range	T_A	0	25	70*2	°C

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

5

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	MB85231-10	I_{CC1}			480	mA
	MB85231-12				400	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL level	I_{CC2}			16	mA
	CMOS level				8	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}; $\overline{RAS}$=min cycling)	MB85231-10	I_{CC3}			440	mA
	MB85231-12				360	
NIBBLE MODE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=min cycling)	MB85231-10	I_{CC4}			320	mA
	MB85231-12				264	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	MB85231-10	I_{CC5}			440	mA
	MB85231-12				360	
INPUT LEAKAGE CURRENT		I_{IL}	-30		30	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

5

AC CHARACTERISTICS

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85231-10		MB85231-12		Unit
			Min.	Max.	Min.	Max.	
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from $\overline{RAS}$	5,8	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	10		10		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to RAS Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to CAS Delay Time	10,11	t_{RCD}	20	70	20	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
$\overline{RAS}$ to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	50		55		ns
Access Time from $\overline{CAS}$ Precharge	8,15	t_{CPA}		60		55	ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	15		15		ns

AC CHARACTERISTICS (Continued)

(At recommended operating conditions otherwise noted.) Notes 1, 2, 3

Parameter / NOTES	Symbol	MB85230-10		MB85230-12		Unit
		Min.	Max.	Min.	Max.	
$\overline{CAS}$ Precharge Time($\overline{CAS}$-before $\overline{RAS}$ refresh)	t_{CPN}	15		15		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{CHR}	15		20		ns

NOTES;

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig. 3.
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 4 and 5.
6. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{CAC}.
7. If $t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{AA}-t_{CAS}-t_T$, access time is t_{AA}.
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. t_{OFF} is specified that output buffer changes to high impedance state.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RAC} (max) is specifies as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAS} or t_{AA}.
11. t_{RCD} (min) = t_{RAH} (min) +2t_T + t_{ASC} (min).
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WCS} is specified as a reference point only. If tWCS(min),the DQn pins will maintain impedance(High-Z) state throughout the entire cycle.
15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from V_{IL} to V_{IH}.). Therefore, if t_{CP} is short, t_{CAC} is longer than t_{CAC} (max).

Fig. 3 - MB85230 DERATING CURVE (Normal Cycle)

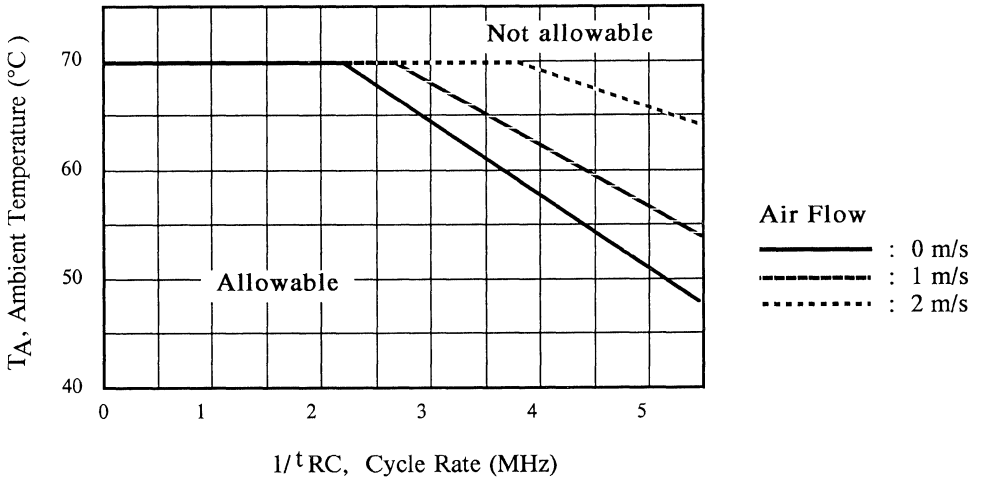


Fig. 4 - tRAC vs tRCD

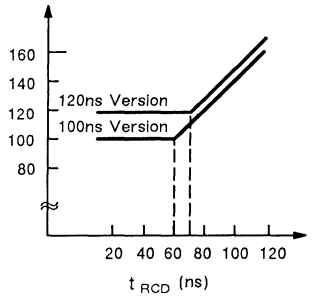
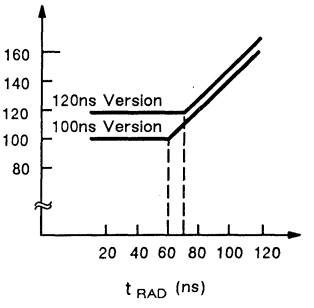
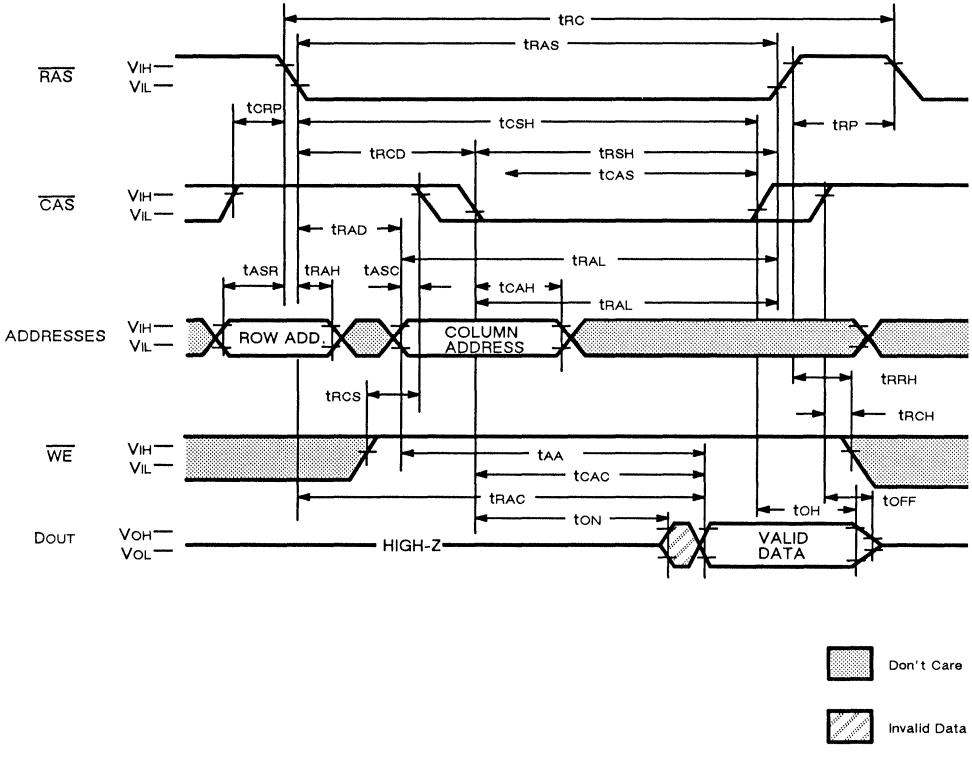


Fig. 5 - tRAC vs tRAD

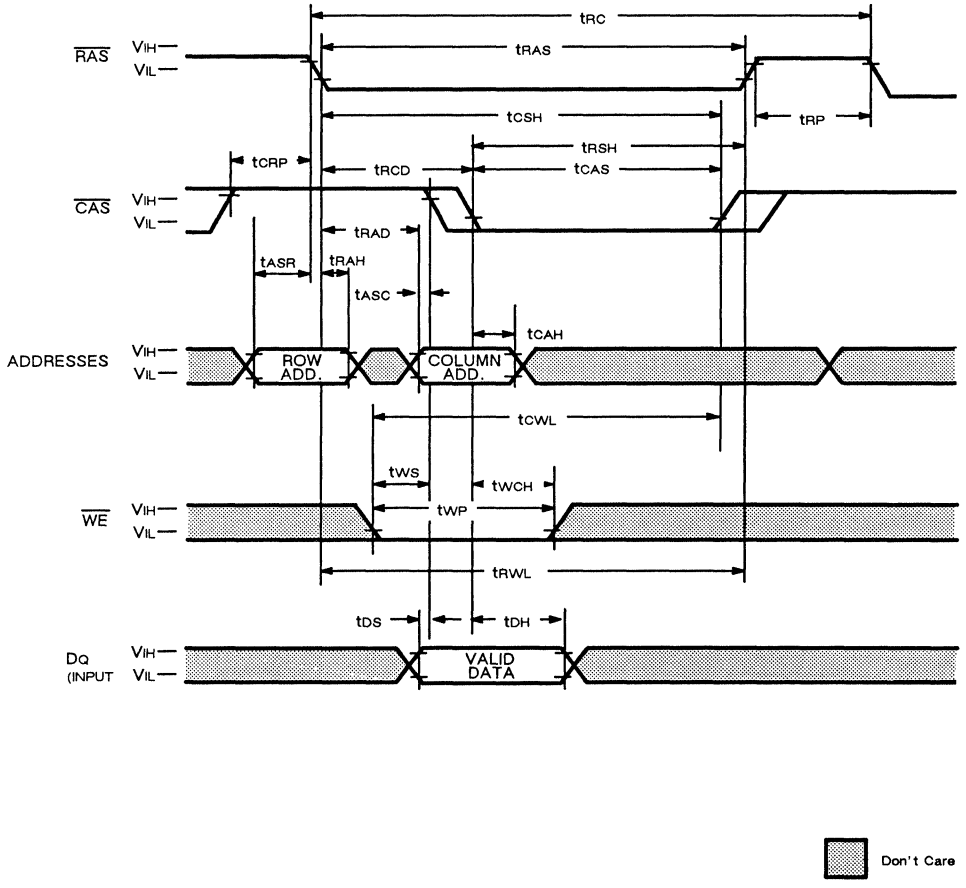


5

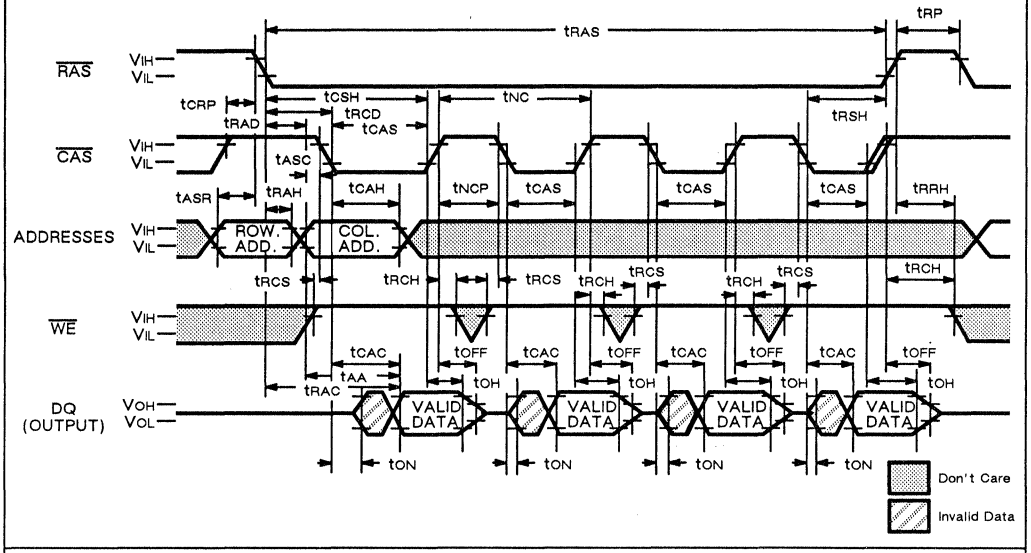
READ CYCLE


tRC
tRAS
RAS
VIH
VIL
tCRP
tCSH
tRP
tRCD
tRSH
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
ADDRESSES
ROW ADD.
COLUMN ADDRESS
tRRH
tRCS
tRCH
WE
tAA
tCAC
tRAC
tON
tOH
tOFF
DOUT
VOH
VOL
HIGH-Z
VALID DATA
Don't Care
Invalid Data

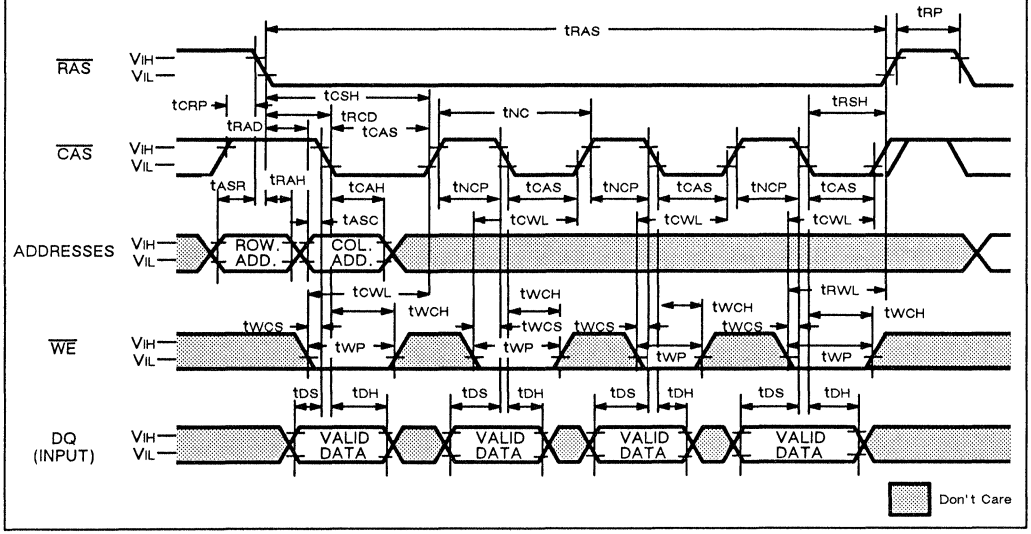
WRITE CYCLE (Early Write)



NIBBLE MODE READ CYCLE



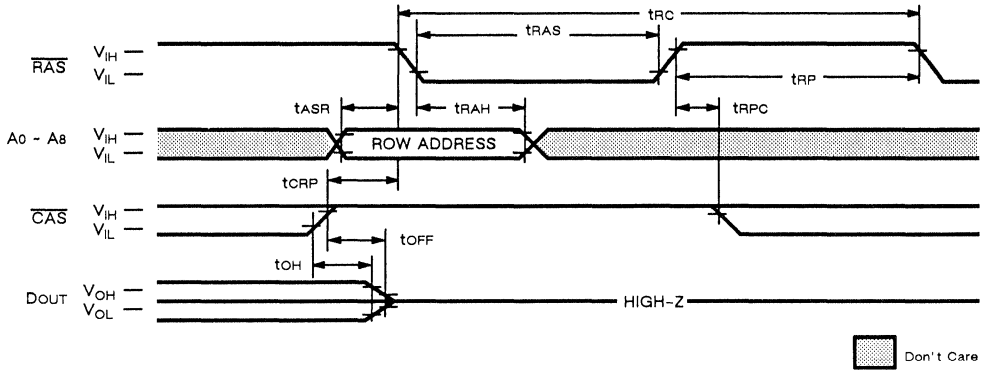
NIBBLE MODE WRITE CYCLE



5

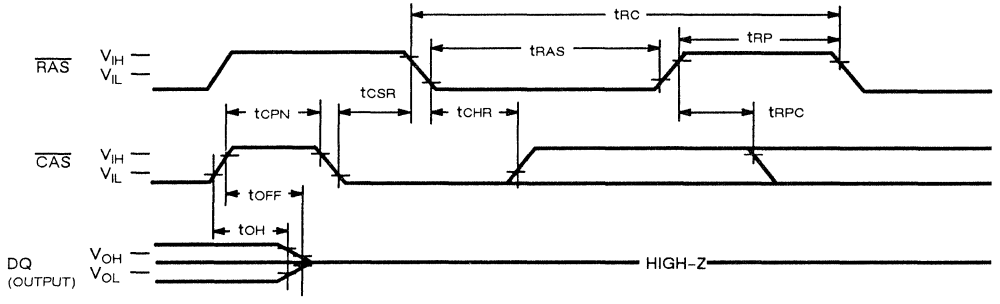
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE: $\overline{WE}$, DQ (Input) = Don't Care, A9=VIH or VIL



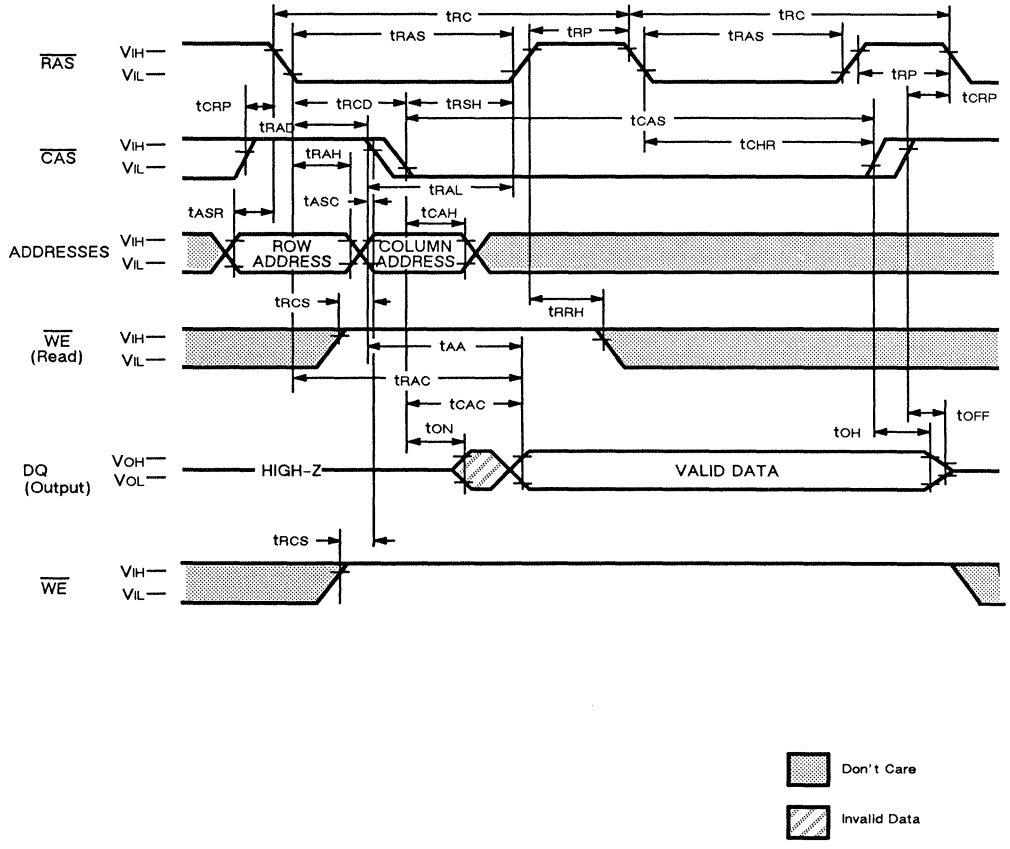
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE: ADDRESS, $\overline{WE}$, DQ (Input) = Don't Care



5

HIDDEN REFRESH CYCLE



DESCRIPTION

Block Analysis:

As shown in Fig. 1 and Fig. 2, the MB85231 is composed of eight MB81C1001, and the memory selection of the each MB81C1001 consists of a 1024-by-1024 cell matrix.
Operational modes of this module are specified below.

Address Inputs:

A total of twenty binary input address bits are required to decde any 8-bit of the 8,388,608 storage cells within the MB85231. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins(A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min)+ t_T. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:

Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:

1. **Data Input;**
   In write cycle, the 8-bit data is written into the MB85231 during write cycle through each DQ pins. Each input data is strobed and latched by falling edge of $\overline{CAS}$, and $\overline{WE}$ must be brought to V_{IL} before falling edge of $\overline{CAS}$, data input strobed by $\overline{CAS}$, and setup and hold times are referenced to $\overline{CAS}$.

2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}$. The data output remans valid until $\overline{CAS}$ returns to high.

Read Cycle:

The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$=V_{IL} and keeping $\overline{WE}$=V_{IH} throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The output data is remain valid with $\overline{CAS}$=V_{IL}, i.e., if $\overline{CAS}$ goes V_{IH}, the data becomes invalid with t_{OH}. The access time is determined by $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input (t_{AA}). If t_{RCD}($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}.

Write Cycle:

The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 8-bit data on DQ pins are latched with the falling edge of $\overline{CAS}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

Nibble Mode:

The nibble mode is a 4-bit serial access mode allows high speed addressing with $\overline{CAS}$ during read or write cycle. The each cell accessed dring nibble mode are determined by the combination of row and column address on A9(RA9 and CA9). The two address are used to select one of four bits for initial access. After the first bits is accessed by normal read or write mode, the remaining nibble bits can be accessed by toggling $\overline{CAS}$, high to row level. Toggling $\overline{CAS}$ causes RA9 and CA9 to be increased internally while all other address bits are held constant and makes the next nibble bit available for access.
Refer to Table 1 for nibble mode address sequence.
If more than four bits are accessed during nibble mode, the address sequence will begin to repeat.

1. **Nibble Mode Read Cycle:**
   The nibble mode write cycle is also executed after normal cycle with holding $\overline{RAS}$=V_{IL}, applying column address and $\overline{CAS}$, and keeping $\overline{WE}$=V_{IH}. Since all address during nibble mode cycle is latched by normal cycle, the read operation is simplified.

2. **Nibble Mode Read Cycle:**
   The nibble mode write cycle is also executed by the same manner as nibble mode read cycle except for the state of $\overline{WE}$. The data on each DQ is latched with the falling edge of $\overline{CAS}$ and written into the memory.

5

DESCRIPTION (Continued)

Refresh:

The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85230 also has three types of refresh modes, $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden refresh.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$=V_{IL} and keeping $\overline{CAS}$=V_{IH} through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the DQ pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$=V_{IL} before $\overline{RAS}$. By this combination, the MB85231 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is execute dby keeping $\overline{CAS}$=V_{IL} to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept V_{IL} continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Table 1 — NIBBLE MODE ADDRESS SEQUENCE

Sequence	Nibble bit	Row address	RA9	Column address	CA9	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	101010101	0	101010101	0	Input address
Toggling $\overline{CAS}$ (nibble mode)	2	101010101	1	101010101	0	Generated
Toggling $\overline{CAS}$ (nibble mode)	3	101010101	0	101010101	1	internally
Toggling $\overline{CAS}$ (nibble mode)	4	101010101	1	101010101	1	
Toggling $\overline{CAS}$ (nibble mode)	1	101010101	0	101010101	0	Sequence repeats

FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CRS} \geq t_{CRS}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X: Don't Care
*: $\overline{RAS}$ puts V_{IH} at once.

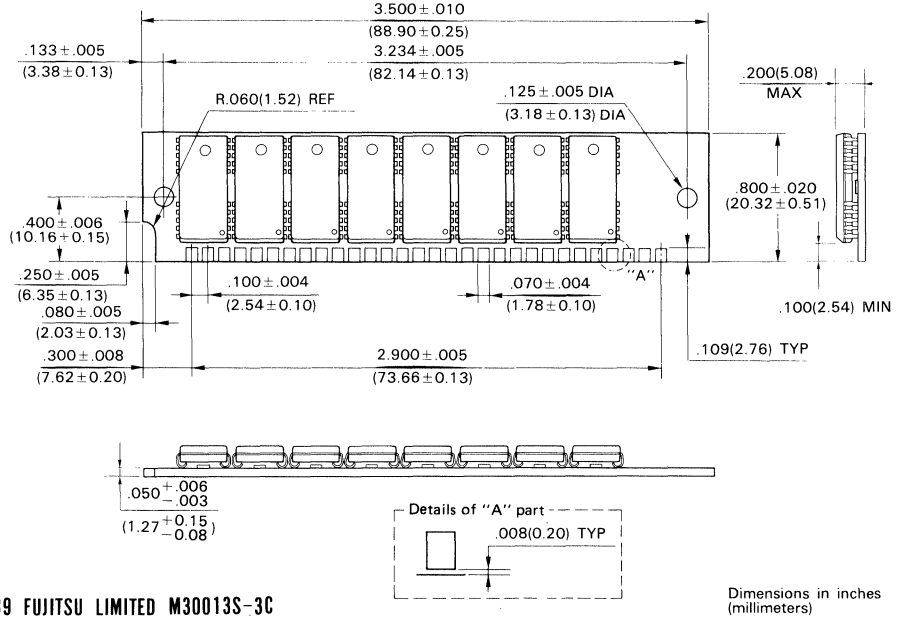
5

PACKAGE DIMENSIONS

(Suffix: PJPB)

30-LEAD PLASTIC MODULE (SOCKET TYPE)

(Case No. : MSS-30P-P04)



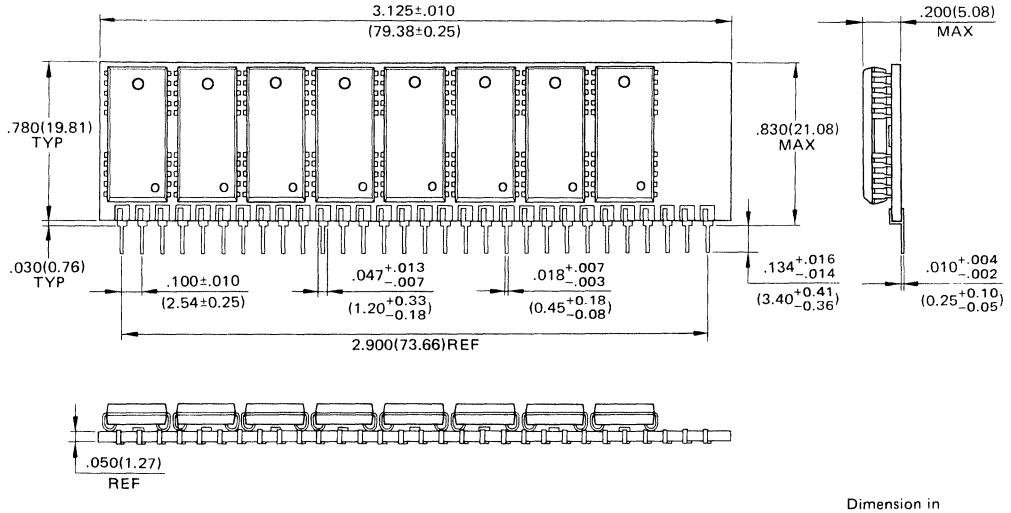
Dimensions in inches
(millimeters)

5

PACKAGE DIMENSIONS (Continued)

(Suffix: PJPS)

30-LEAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P05)



Dimension in inches (millimeters)

5

5

FUJITSU

1M x 9 DRAM MODULE

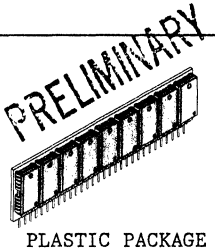
MB85235-10
MB85235-12

1,048,576 x 9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

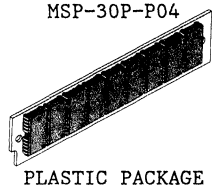
TS028-B87Z
Dec. 1987

The Fujitsu MB85235 is a fully decoded, dynamic CMOS random access memory module with eight MB81C1000, in 26-pin SOJ packages, and nine .22µF decoupling capacitors under the each memory, mounted on a 30-pin SIP or a 30-pad SIMM module. Organized as 1,048,576 x 9-bit words, the MB85235 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85235 are the same as the MB81C1000 devices which feature a Fast Page mode operation.

- 1,048,576 x 9 DRAM, 30-pin SIP and SIMM
- RAS access time (t_{RAC}):
  - 100 ns max. (MB85235-10)
  - 120 ns max. (MB85235-12)
- Cycle time (t_{RC}):
  - 180 ns min. (MB85235-10)
  - 210 ns max. (MB85235-12)
- Column access time (t_{CAC}):
  - 30 ns max. (MB85235-10)
  - 35 ns max. (MB85235-12)
- Fast Page mode cycle time (t_{PC}):
  - 60 ns max. (MB85235-10)
  - 70 ns max. (MB85235-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  - Active = 2970 mW max. (MB85235-10)
  - 2475 mW max. (MB85235-12)
  - Standby = 49.5 mW max. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capability
- Fast Page Mode Read and Write capability
- Leaded and Leadless type are available.
- JEDEC standard (30 pin SIP) pin assignment

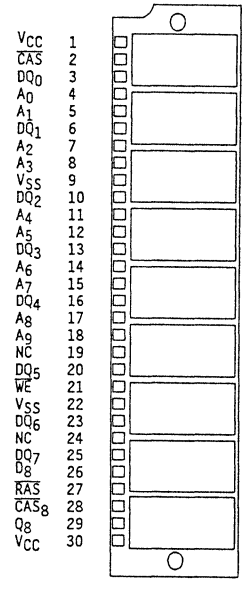


PLASTIC PACKAGE
MSP-30P-P04



PLASTIC PACKAGE
MSS-30P-P03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 - BLOCK DIAGRAM

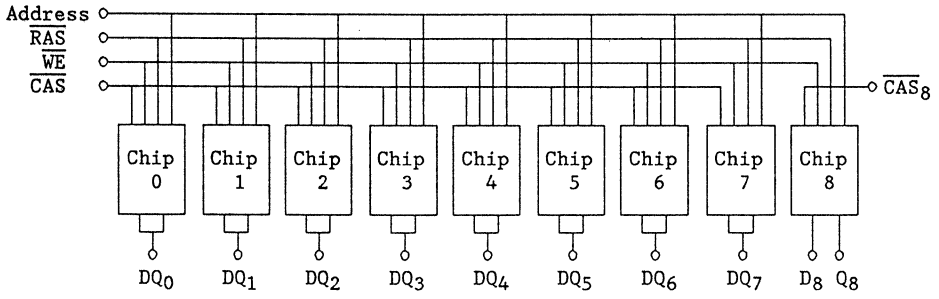
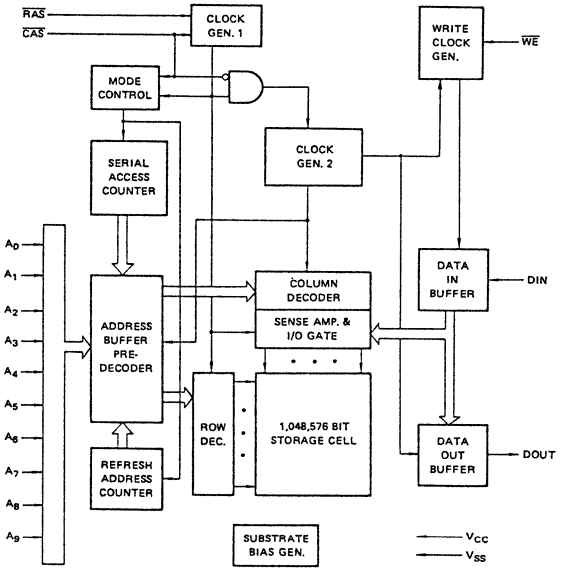


Fig. 2 - BLOCK DIAGRAM FOR EACH CHIP



5

CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	-	60	pF
Input Capacitance, RAS	C_{IN2}	-	49	pF
Input Capacitance, CAS	C_{IN3}	-	49	pF
Input Capacitance, WE	C_{IN4}	-	48	pF
Input Capacitance, CAS_8	C_{IN5}	-	9	pF
Input Capacitance, D_8	C_D	-	7	pF
I/O Capacitance, DQ_0 to DQ_7	C_{DQ}	-	14	pF
Output Capacitance, Q_8	C_O	-	10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Level, all inputs	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0*1		0.8 0.8	V V
Operating Temperature Range	T_A	0	25	70*2	°C

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	MB85235-10	I_{CC1}			540	mA
	MB85235-12				450	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL level	I_{CC2}			18	mA
	CMOS level				9	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$=min cycling)	MB85235-10	I_{CC3}			495	mA
	MB85235-12				405	
FAST PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=min cycling)	MB85235-10	I_{CC4}			360	mA
	MB85235-12				297	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	MB85235-10	I_{CC5}			495	mA
	MB85235-12				405	
INPUT LEAKAGE CURRENT, all inputs		I_{IL1}	-30		30	µA
INPUT LEAKAGE CURRENT, $\overline{CAS}_8$ and D_8		I_{IL2}	-10		10	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85235-10		MB85235-12		Unit
			Min	Max	Min	Max	
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from $\overline{RAS}$	5,8	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	10		10		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10,11	t_{RCD}	20	70	20	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
RAS to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
Fast Page Mode Read/Write Cycle Time		t_{PC}	60		70		ns
Access Time from $\overline{CAS}$ Precharge	8,15	t_{CPA}		60		70	ns
Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		15		ns
$\overline{CAS}$ Precharge Time		t_{CPN}	15		15		ns
RAS Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	15		20		ns

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85235-10		MB85235-12		Unit
			Min	Max	Min	Max	
Read-Modify-Write Cycle Time	16	t_{RWC}	210		245		ns
Fast Page Mode Read-Modify-Write Cycle Time	16	t_{PRWC}	85		100		ns
RAS to WE Delay Time	14,16	t_{RWD}	100		120		ns
CAS to WE Delay Time	14,16	t_{CWD}	30		35		ns
Column Address to WE delay Time	14,16	t_{AWD}	50		60		ns

NOTES;

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$/CAS_8=V_{IH}) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig.4.
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
6. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA}-t_{CAC}-t_T$, access time is t_{CAC}.
7. If $t_{RAD} \geq t_{RAD}$ (max), $t_{ASC} \geq t_{AA}-t_{CAC}-t_T$, access time is t_{AA}.
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. t_{OFF} is specified that output buffer changes to high impedance state.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
11. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is early write cycle and the output pins will maintain high impedance(High-Z) state throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the output pins.
    If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the output pins, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, and t_{RAL} specifications.
15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$/$\overline{CAS_8}$ from V_{IL} to V_{IH}.). Therefore, if t_{CP} is short, t_{CAC} is longer than t_{CAC} (max).
16. For parify bit only.

Fig.3 - DERATING CURVE (Normal Cycle)

T.B.D.

Fig.4 - DERATING CURVE (Fast Page Mode Cycle)

T.B.D.

5

Fig.5 - t_{RAC} vs t_{RCD}

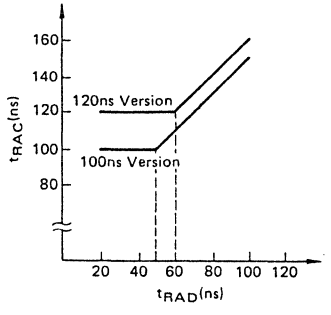
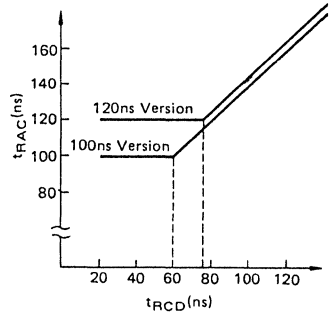
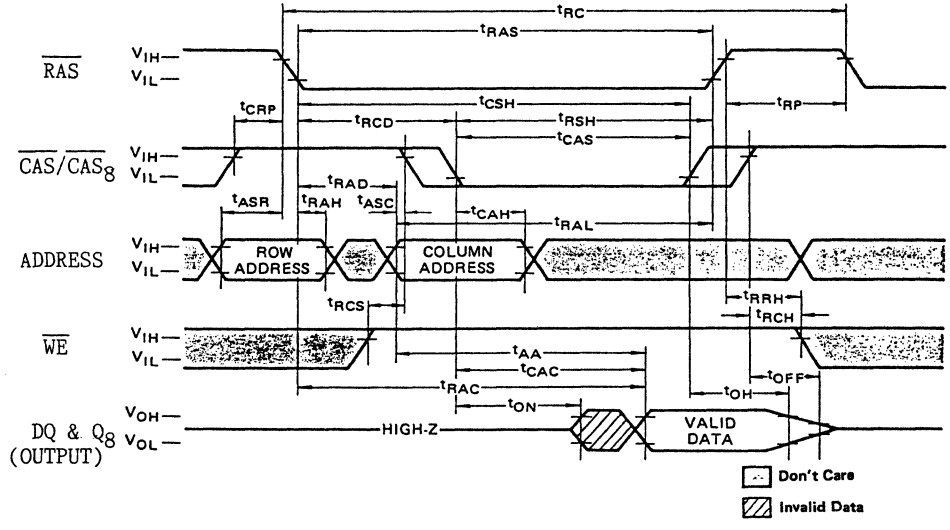


Fig.6 - t_{RAC} vs t_{RAD}

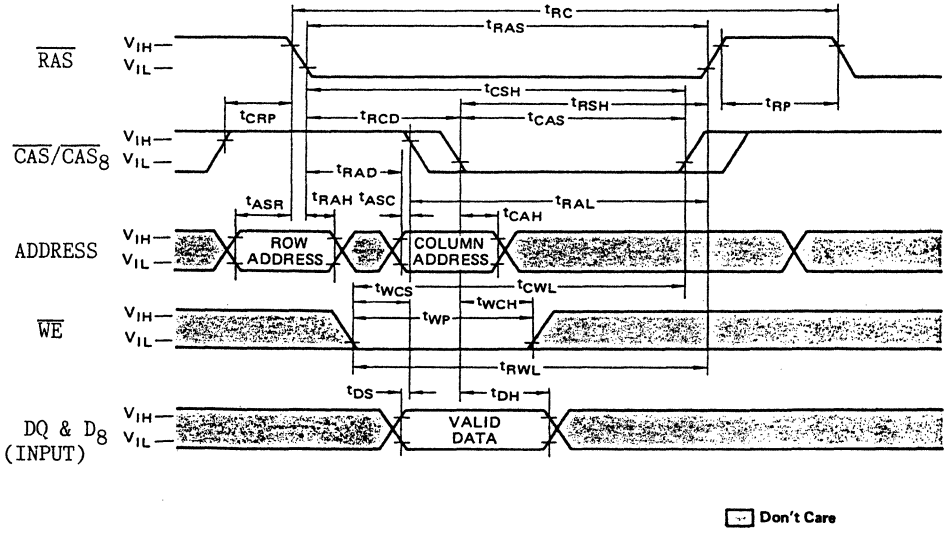


Read Cycle

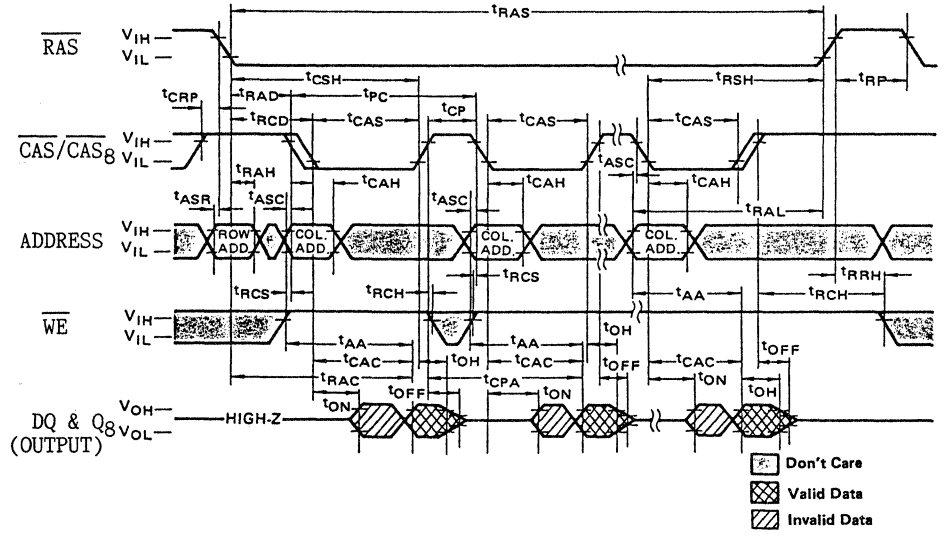


5

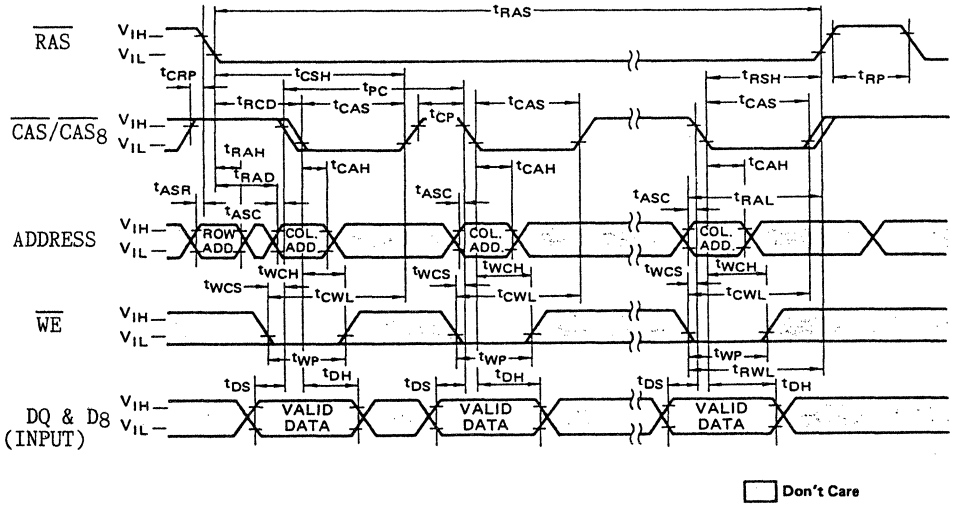
Write Cycle (Early Write)



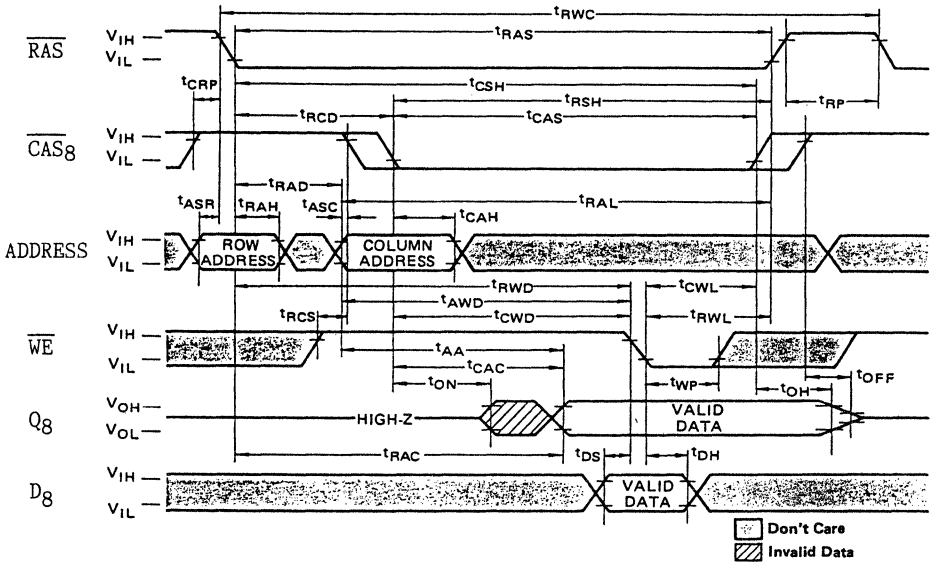
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

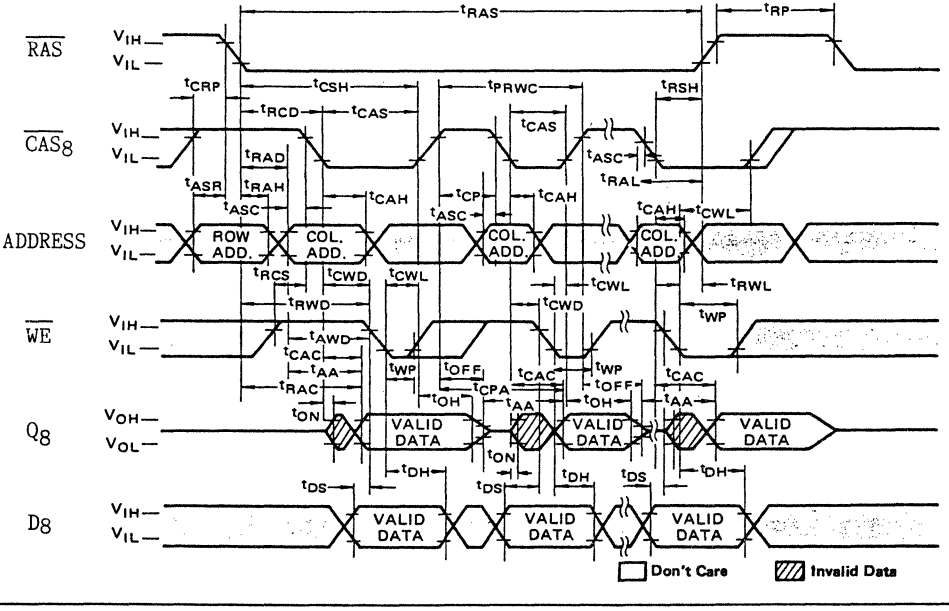


Read-Modify-Write Cycle



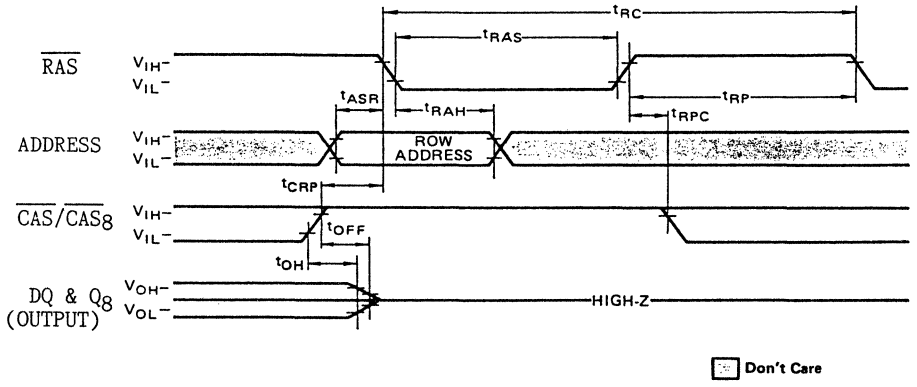
5

Fast Page Mode Read-Modify-Write Cycle



$\overline{RAS}$-only Refresh Cycle

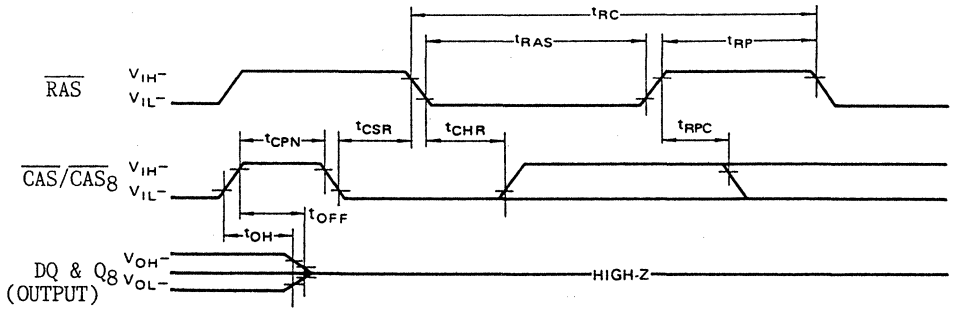
NOTE : $\overline{WE}$, D, DQ(Input)=Don't care, $A_9=V_{IH}$ or V_{IL}



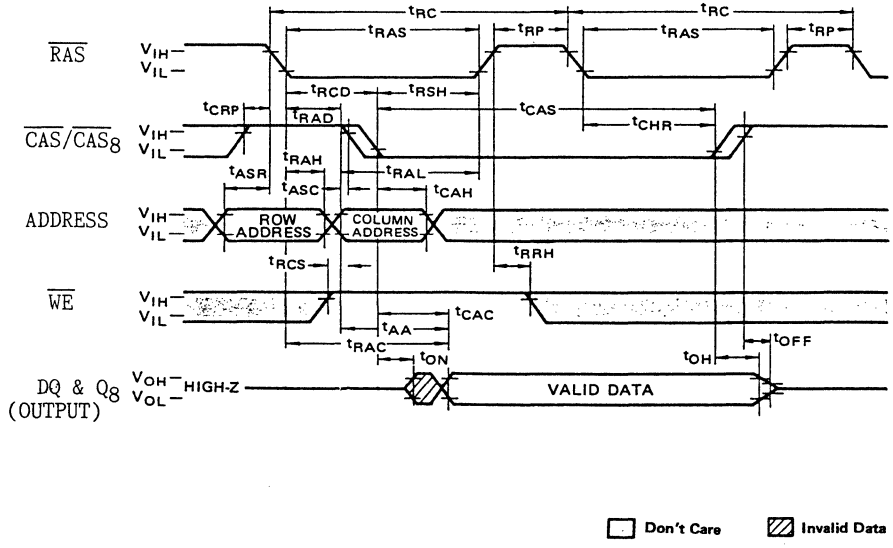
5

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE : Address, $\overline{WE}$, D, DQ(Input)=Don't care



Hidden Refresh Cycle



5

DESCRIPTION

Block Analysis:
As shown in Fig. 1 and Fig. 2, the MB85235 is composed of nine MB81C1000, and the memory selection of the each MB81C1000 consists of a 1024-by-1024 cell matrix. Operational modes of the device are shown in the FUNCTIONAL TRUTH TABLE below.

Address Inputs:
A total of twenty binary input address bits are required to decode any 9-bit of the 9,437,184 storage cells within the MB85235. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins(A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}/\overline{CAS}_8$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}/\overline{CAS}_8$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after t_{RAH} (min)+ t_T. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:
Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:
1. **Data Input;**
   In write cycle, the 9-bit data is written into the MB85235 during write cycle through each DQ and D pin. Each input data is strobed and latched by falling edge of $\overline{CAS}/\overline{CAS}_8$ and $\overline{WE}$ must be brought to V_{IL} before falling edge of $\overline{CAS}/\overline{CAS}_8$, data input is strobed by $\overline{CAS}/\overline{CAS}_8$, and setup and hold times are referenced to $\overline{CAS}/\overline{CAS}_8$.
2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ and $\overline{CAS}_8$ are brought low. In a read cycle, the output becomes valid within t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD}(max) is satisfied. In the meanwhile when either t_{RCD} or t_{RAD}, or both, are equal or greater than their maximum value, the output data becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}/\overline{CAS}_8$. The data output remains valid until $\overline{CAS}$ and $\overline{CAS}_8$ return to high.

Read Cycle:
The read cycle is executed by the falling edge of both $\overline{RAS}$ and $\overline{CAS}/\overline{CAS}_8$, and keeping $\overline{WE}$ to high throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}/\overline{CAS}_8$ respectively. The valid data will appear at the DQ and Q pins after determined by $\overline{RAS}$(t_{RAC}), $\overline{CAS}$(t_{CAC}), or Column address input(t_{AA}). If t_{RCD}($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}. The output data becomes invalid after $\overline{CAS}/\overline{CAS}_8$ is brought high, with a delay time of t_{OH}, and the DQ and Q pins return to the high impedance with t_{OH}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 9-bit data on DQ and D pins are latched with the falling edge of $\overline{CAS}/\overline{CAS}_8$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

DESCRIPTION (Continued)

Fast Page Mode Read Cycle:
The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ low, applying column address and $\overline{CAS}/\overline{CAS_8}$, and keeping $\overline{WE}$ high. Since the row address during fast page mode cycle is latched by normal cycle, the cycle time is reduced. During this mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occur later. Any of the 1024 bits belonging to each internal row address can be accessed.

Fast Page Mode Write Cycle:
The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$. The data on each DQ and D are latched with the falling edge of $\overline{CAS}/\overline{CAS_8}$ and written into the memory. During this write cycle, t_{CWL} must be satisfied. Any of 1024 bits belonging to each internal row address can be accessed.

Refresh:
The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85231 also has three types of refresh modes below.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$ low, and $\overline{CAS}/\overline{CAS_8}$ remains high through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the data pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}/\overline{CAS_8}$ low before $\overline{RAS}$ brought low. By this combination, the MB85235 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is executed by keeping $\overline{CAS}/\overline{CAS_8}$ low to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ and $\overline{CAS_8}$ are kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

5

FUNCTIONAL TRUTH TABLE

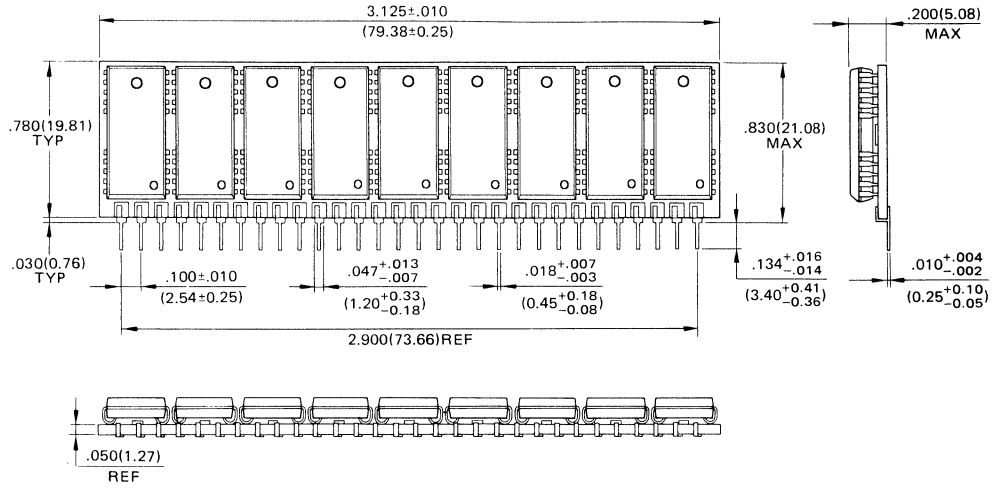
Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$(8)	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X; Either V_{IH} or V_{IL}.
*; $\overline{RAS}$ puts V_{IH} at once.

5

PACKAGE DIMENSIONS
(Suffix: PJPS)

30-LEAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P04)

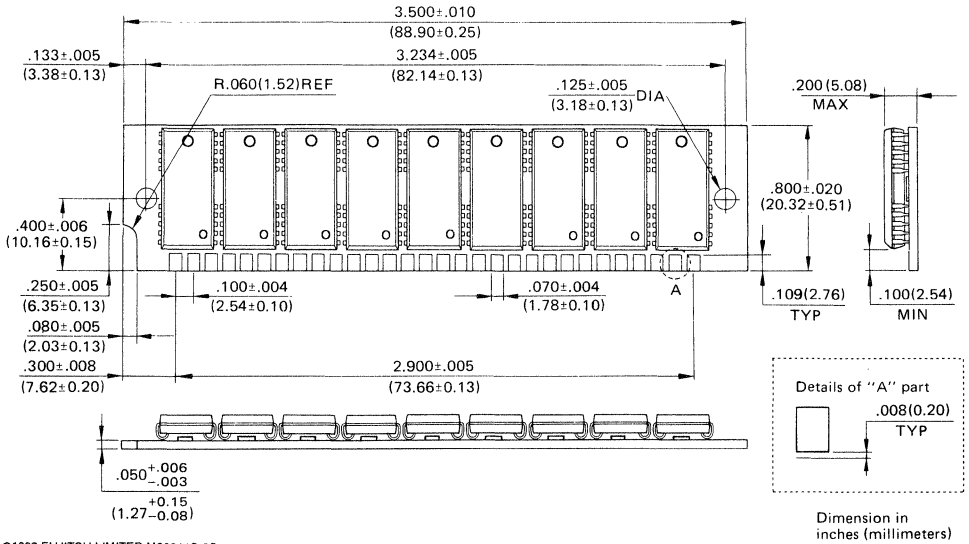


Dimension in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PJPB)

30-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-30P-P03)



5

FUJITSU

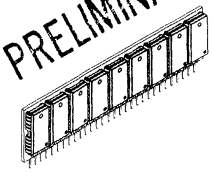
1M x 9 SCRAM MODULE

MB85237-10
MB85237-12

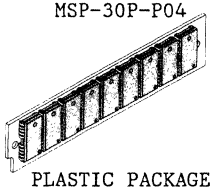
1,048,576 x 9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

TS029-A881
Jan. 1988

PRELIMINARY



PLASTIC PACKAGE
MSP-30P-P04

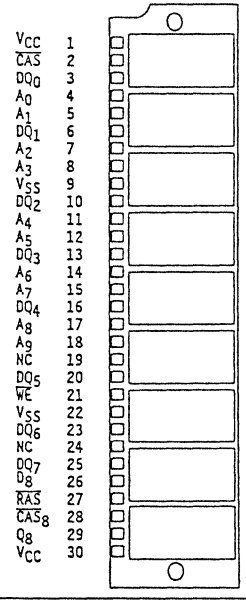


PLASTIC PACKAGE
MSS-30P-P03

The Fujitsu MB85237 is a fully decoded, dynamic CMOS random access memory module with nine MB81C1002, in 26-pin SOJ packages, and nine .22µF decoupling capacitors under the each memory, mounted on a 30-pin SIP or a 30-pad SIM module. Organized as 1,048,576 x 9-bit words, the MB85237 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85237 are the same as the MB81C1002 devices which feature a Static Column mode operation.

- 1,048,576 x 9 DRAM, 30-pin SIP and SIMM
- RAS access time (t_{RAC}):
  100 ns max. (MB85237-10)
  120 ns max. (MB85237-12)
- Cycle time (t_{RC}):
  180 ns min. (MB85237-10)
  210 ns max. (MB85237-12)
- Address access time (t_{AA}):
  50 ns max. (MB85237-10)
  60 ns max. (MB85237-12)
- Static Column mode cycle time (t_{SC}):
  55 ns max. (MB85237-10)
  65 ns max. (MB85237-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  Active = 2970 mW max. (MB85237-10)
  2475 mW max. (MB85237-12)
  Standby = 49.5 mW max. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capability
- Static Column Mode Read and Write capability
- Leaded and Leadless type are available.
- JEDEC standard (30 pin SIP) pin assignment

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 - BLOCK DIAGRAM

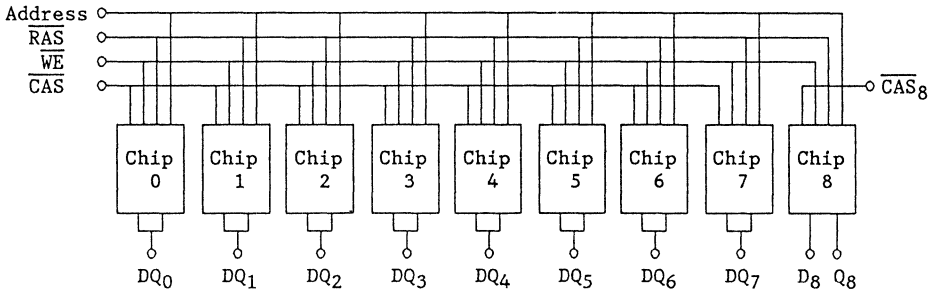
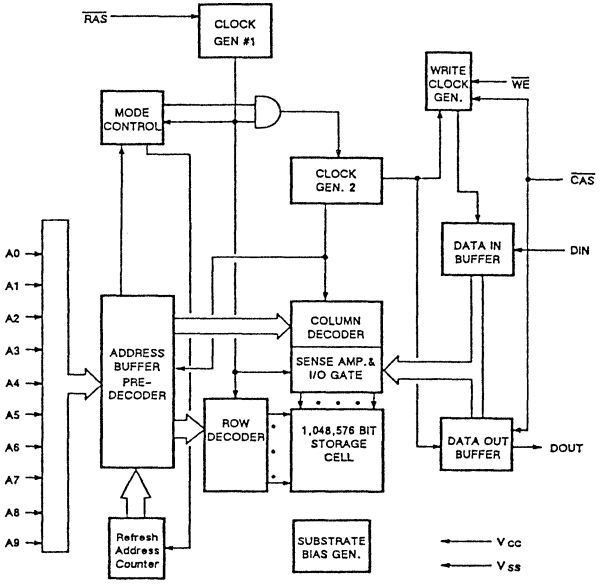


Fig. 2 - BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_9	C_{IN1}	-	60	pF
Input Capacitance, RAS	C_{IN2}	-	49	pF
Input Capacitance, CAS	C_{IN3}	-	49	pF
Input Capacitance, WE	C_{IN4}	-	48	pF
Input Capacitance, CAS_8	C_{IN5}	-	9	pF
Input Capacitance, D_8	C_D	-	7	pF
I/O Capacitance, DQ_0 to DQ_7	C_{DQ}	-	14	pF
Output Capacitance, Q_8	C_O	-	10	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Level, all inputs	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0*1		0.8 0.8	V V
Operating Temperature Range	T_A	0	25	70*2	°C

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	MB85237-10	I_{CC1}			540	mA
	MB85237-12				450	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL level	I_{CC2}			18	mA
	CMOS level				9	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$=min cycling)	MB85237-10	I_{CC3}			495	mA
	MB85237-12				405	
STATIC COLUMN MODE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycling, t_{SC}=min)	MB85237-10	I_{CC4}			270	mA
	MB85237-12				207	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	MB85237-10	I_{CC5}			495	mA
	MB85237-12				405	
INPUT LEAKAGE CURRENT, all inputs		I_{IL1}	-30		30	µA
INPUT LEAKAGE CURRENT, $\overline{CAS}_8$ and D_8		I_{IL2}	-10		10	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85237-10		MB85237-12		Unit
			Min	Max	Min	Max	
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Read-Modify-Write Cycle Time	21	t_{RWC}	210		245		ns
Access Time from $\overline{RAS}$	5,6	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	5	t_{CAC}		30		35	ns
Access Time from Column Address	5,7	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	7		7		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	8	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	9,10	t_{RCD}	25	70	25	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)		t_{CPN}	15		15		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time	11	t_{ASC}	0		0		ns
Column Address Hold Time		t_{CAH}	15		20		ns
$\overline{RAS}$ to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	20		25		ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	14,21	t_{RWD}	100		120		ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	14,21	t_{CWD}	30		35		ns
Column Address to $\overline{WE}$ delay Time	14,21	t_{AWD}	50		60		ns

5

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85237-10		MB85237-12		Unit
			Min	Max	Min	Max	
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for CAS-before-$\overline{RAS}$ Refresh		t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for CAS-before-$\overline{RAS}$ Refresh		t_{CHR}	15		20		ns
Static Column Mode Read/Write Cycle Time	4	t_{SC}	55		65		ns
Static Column Mode CAS Precharge Time		t_{CP}	15		15		ns
Static Column Mode Read-Modify-Write Cycle Time	21	t_{SRWC}	95		115		ns
Access Time from Last Write	5,15	t_{ALW}		90		110	ns
Access Time from $\overline{WE}$ Precharge	5	t_{WPA}		30		35	ns
Output Hold Time from Column Address Change		t_{AOH}	10		10		ns
Write Latched Data Hold Time		t_{WOH}	0		0		ns
Column Address Hold Time Referenced to $\overline{RAS}$	16	t_{AHR}	15		15		ns
Last Write to Column Address Delay Time	17,18	t_{LWAD}	25	40	30	50	ns
Column Address Hold Time Referenced to Last Write		t_{AHLW}	95		120		ns
$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	100		100		ns
$\overline{WE}$ Inactive time		t_{WI}	15		20		ns
$\overline{WE}$ Setup Time for Output Disable	19	t_{WS}	0		0		ns
$\overline{WE}$ Hold Time for Output Disable	19	t_{WH}	0		0		ns
$\overline{WE}$ Setup Time for Output Disable	20,21	t_{WS}	0		0		ns
$\overline{WE}$ Hold Time for Output Disable	20,21	t_{WH}	0		0		ns

AC CHARACTERISTICS (Cont'd)

NOTES;

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$/$\overline{CAS}_8$=V_{IH}) of 200 µs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T=5ns
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig. 2 and 3.
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} and/or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 3 and 4.
7. If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}.
8. t_{OFF} is specified that output buffer changes to high impedance state.
9. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}. Refer to Fig. 5.
10. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).
11. Assumes that write cycle only.
12. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{AA}. Refer to Fig. 6.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{RWD}, t_{CWD}, t_{AWD}, and t_{WS} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min), the cycle entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the output pins.
    If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear at the output pins, and write operation can be executed by satisfing t_{RWL}, t_{CWL}, and t_{RAL} specifications.
15. Assumes tha $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value, t_{ALW} will be increased by the amount of the t_{LWAD} exceeds the value shown. Refer to Fig. 7.
16. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
17. Operation within t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a refrence point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
18. t_{LWAD} (min) = t_{CAH} (min) + t_T.
19. Both t_{WS} (min) and t_{WH} (min) must be satisfied for a write cycle to avoid output confliction.
20. t_{WS}, t_{WH} and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and tWH $\geq$ tWH(min), the data output pin will remain High-Z state through entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), the data output will contain data read from the selected cell.
21. For parify bit only.

Fig.3 - DERATING CURVE (Normal Cycle)

T.B.D.

Fig.4 - DERATING CURVE (Static Column Mode Cycle)

T.B.D.

Fig.5 - t_{RAC} vs t_{RCD}

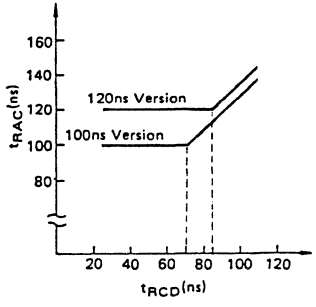


Fig.6 - t_{RAC} vs t_{RAD}

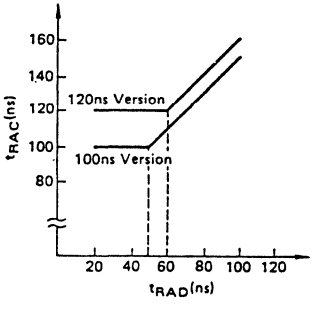
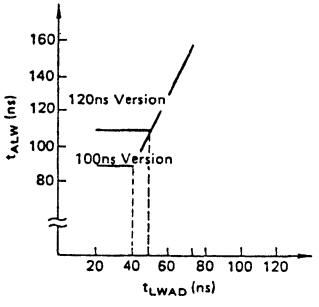
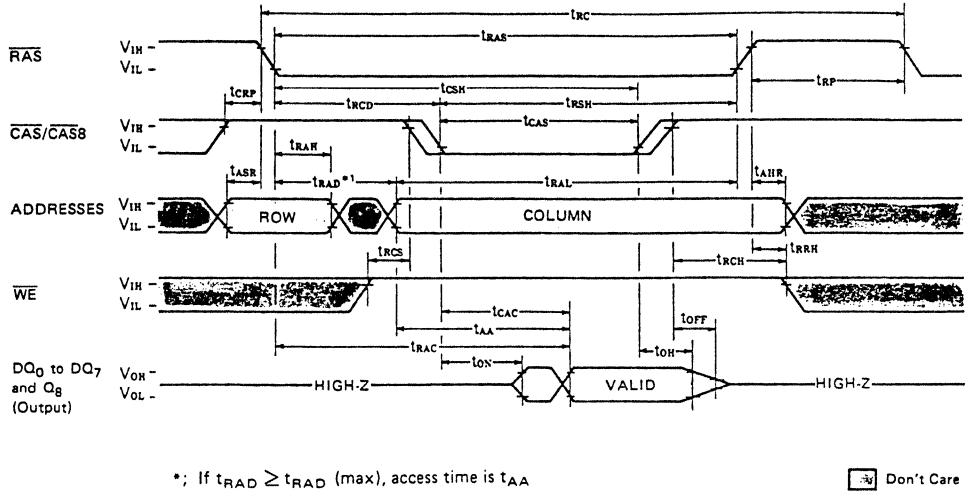


Fig.7 - t_{ALW} vs t_{LWAD}



Read Cycle

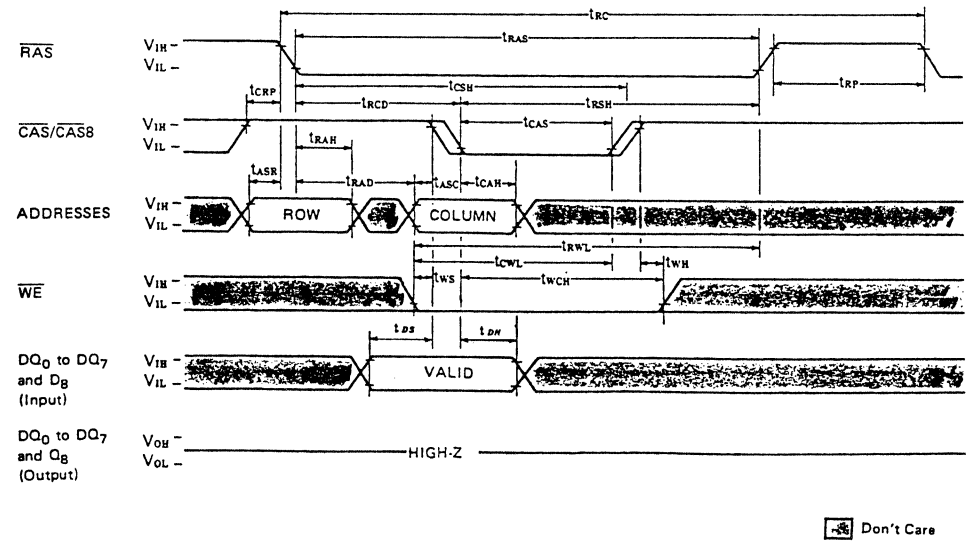


*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}

Don't Care

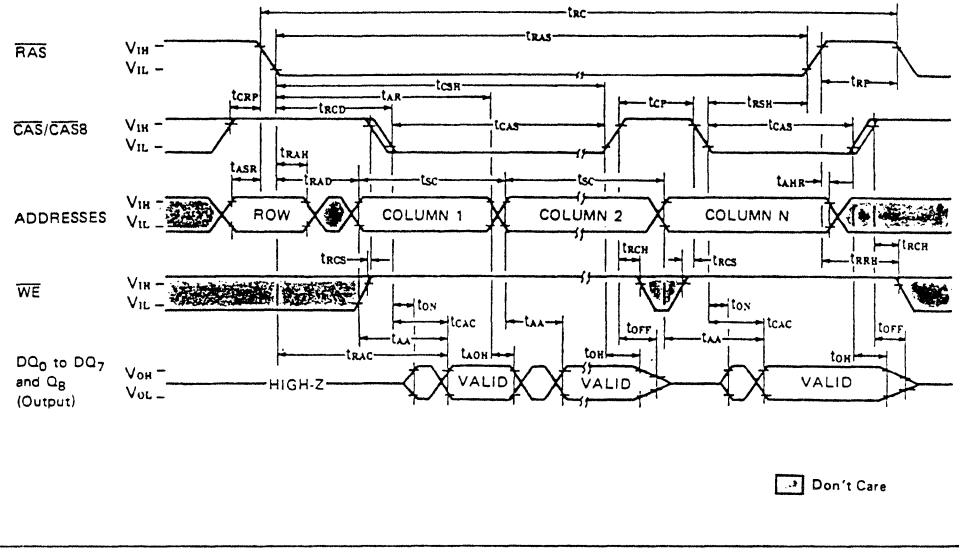
5

Write Cycle (Early Write)

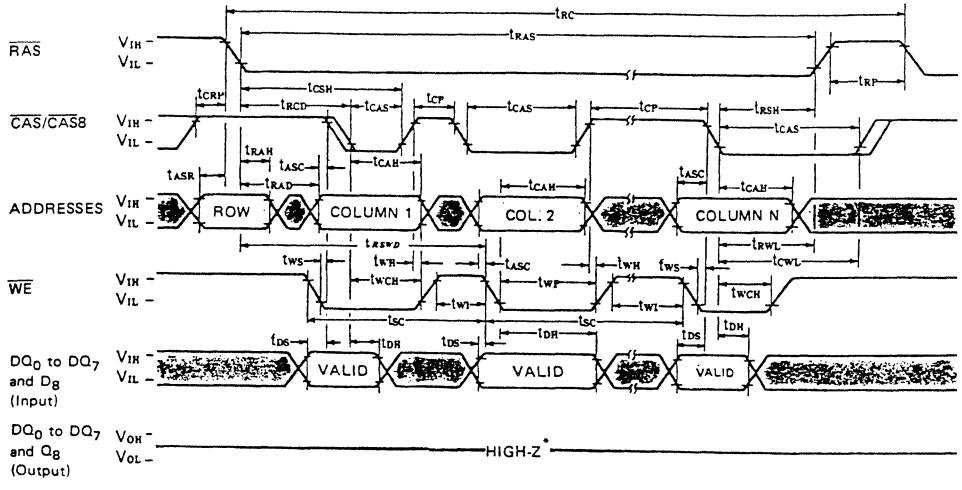


Don't Care

Static Column Mode Read Cycle



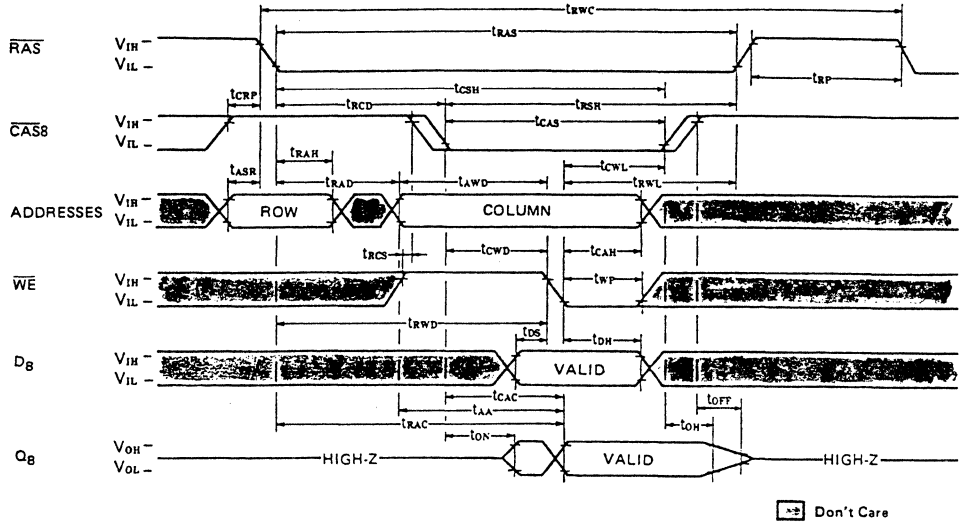
Static Column Mode Write Cycle



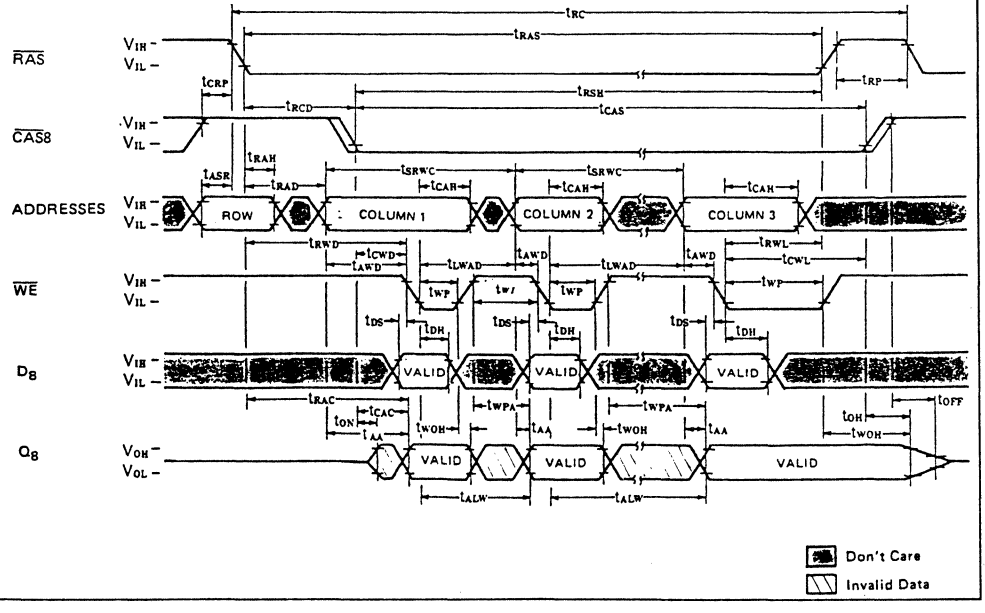
*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

5

Read-Modify-Write Cycle

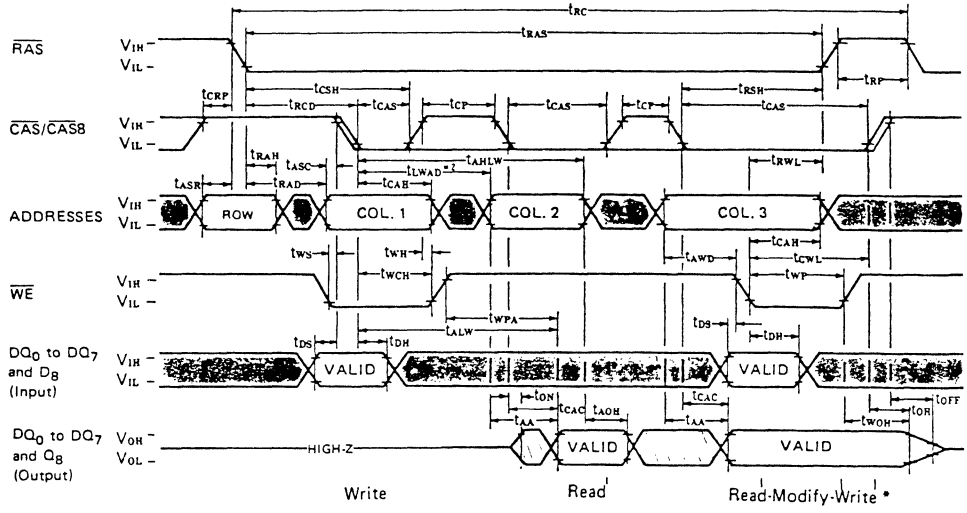


Static Column Mode Read-Modify-Write Cycle



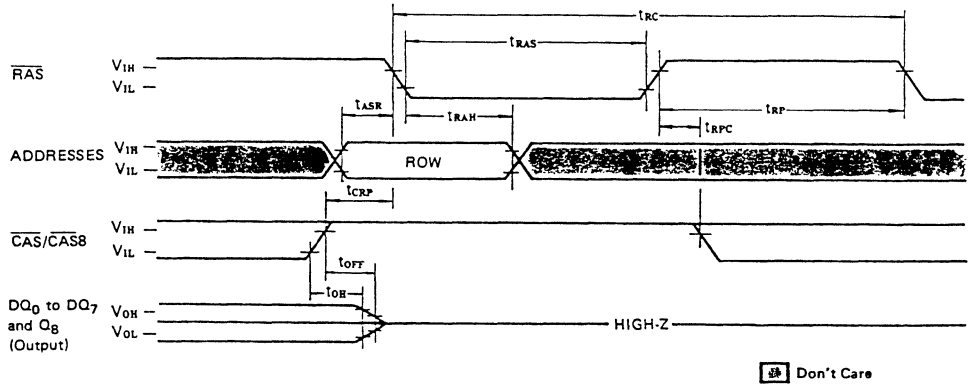
5

Static Column Mode Mixed Cycle



RAS-only Refresh Cycle

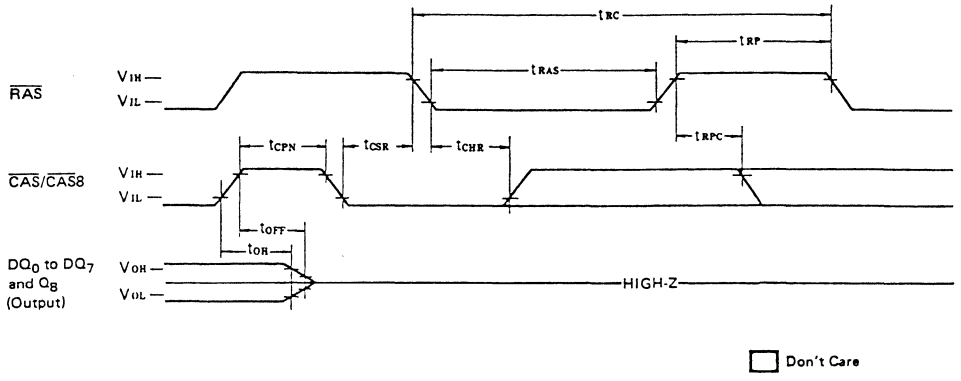
NOTE : WE, D, DQ(Input)=Don't care, Ag=V_{IH} or V_{IL}



5

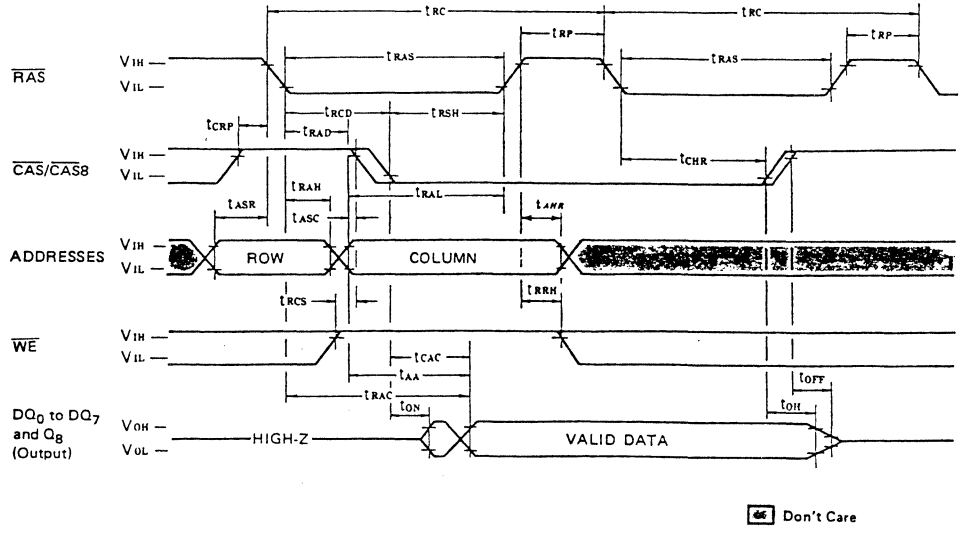
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE : Address, $\overline{WE}$, D, DQ(Input)=Don't care



5

Hidden Refresh Cycle



DESCRIPTION

Block Analysis:
As shown in Fig. 1 and Fig. 2, the MB85237 is composed of nine MB81C1002, and the memory selection of the each MB81C1002 consists of a 1024-by-1024 cell matrix. Operational modes of the device are shown in the FUNCTIONAL TRUTH TABLE below.

Address Inputs:
A total of twenty binary input address bits are required to decode any 9-bit of the 9,437,184 storage cells within the MB85237. Ten row address bits are established on the address input pins(A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. All row addresses must be stable on or before the falling edge of $\overline{RAS}$. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after $t_{RAH}(min) + t_T$. If $t_{RAD} \geq t_{RAD}(max)$, access time is t_{CAC} or t_{AA}, whichever occurs later. In case of write mode, all column addresses are latched with the Column Address Strobe, $\overline{CAS}/\overline{CAS_8}$, and must be stable on or before the falling edge of $\overline{CAS}/\overline{CAS_8}$.

Write Enable:
Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:
1. **Data Input;**
   In write cycle, the 9-bit data is written into the MB85237 during write cycle through each DQ and D pin. Each input data is strobed and latched by later falling edge of $\overline{CAS}/\overline{CAS_8}$ or $\overline{WE}$. In case of early write($\overline{CAS}$ controll write) cycle, data input is strobed by $\overline{CAS}/\overline{CAS_8}$, and setup and hold times are referenced to $\overline{CAS}/\overline{CAS_8}$.

2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ and $\overline{CAS_8}$ are brought low. In a read cycle, the output becomes valid within t_{RAC} from the falling edge of $\overline{RAS}$ when $t_{RCD}(max)$ is satisfied. In the meanwhile when either t_{RCD} or t_{RAD}, or both, are equal or greater than their maximum value, the output data becomes valid within t_{CAC} or t_{AA} whichever occurs later after falling edge of $\overline{CAS}/\overline{CAS_8}$. The data output remains valid until $\overline{CAS}$ and $\overline{CAS_8}$ return to high.

Read Cycle:
The read cycle is executed by the falling edge of both $\overline{RAS}$ and $\overline{CAS}/\overline{CAS_8}$, applying column addresses, and keeping $\overline{WE}$ to high throughout the cycle. The row address are latched with $\overline{RAS}$. The valid data will appear at the DQ and Q pins after determined by $\overline{RAS}(t_{RAC})$, $\overline{CAS}(t_{CAC})$, or Column address input(t_{AA}). If t_{RCD} ($\overline{RAS}$ to $\overline{CAS}$ delay time) is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}. The output data becomes invalid after $\overline{CAS}/\overline{CAS_8}$ is brought high, with a delay time of t_{OH}, and the DQ and Q pins return to the high impedance with t_{OH}. During this cycle, all column addresses must be held before $\overline{RAS}$ is brought high with t_{AHR}.

Write Cycle:
The write cycle is executed by almost same manner as read cycle. The column addresses are latched with falling edge of $\overline{CAS}/\overline{CAS_8}$. The 9-bit data on DQ and D pins are also latched with the falling edge of $\overline{CAS}/\overline{CAS_8}$ and are written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

DESCRIPTION (Continued)

Static Column Mode Read Cycle:
The static column mode read cycle is executed after normal cycle with holding $\overline{RAS}$ low, applying column address and $\overline{CAS}/\overline{CAS_8}$, and keeping $\overline{WE}$ high. Since the row address during static column mode cycle is latched by normal cycle, the cycle time is reduced. During this mode, the access time is determined by t_{CAC}, or t_{AA}, whichever occur later. Any of the 1024 bits belonging to each internal row address can be accessed.

Static Column Mode Write Cycle:
The static column mode write cycle is executed by the same manner as static column mode read cycle except for the state of $\overline{WE}$. The data on each DQ and D are latched with the falling edge of $\overline{CAS}/\overline{CAS_8}$ and written into the memory. During this write cycle, t_{WS} and t_{WI} must be satisfied. Any of 1024 bits belonging to each internal row address can be accessed.

Read-Modify-Write Cycle:
The read-modify-write cycle is permitted on parity chip, and is executed by changing WE high to low after the output data appears the Q pin. The input data on D pin is written into the same address as read out.

Static Column Mode Read-Modify-Write Cycle:
The static column mode read-modify-write cycle is also permitted on parity chip, and is executed by $\overline{WE}$ low pulse. The $\overline{WE}$ must be brought low after t_{RWD}, t_{CWD}, and t_{AWD} to strobe output data.

5

Refresh:
The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85237 also has three types of refresh modes below.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$ low, and $\overline{CAS}/\overline{CAS_8}$ remains high through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the data pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}/\overline{CAS_8}$ low before $\overline{RAS}$ brought low. By this combination, the MB85237 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally.

3. **Hidden Refresh;**
   The hidden refresh is executed by keeping $\overline{CAS}/\overline{CAS_8}$ low to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ and $\overline{CAS_8}$ are kept low continuously from previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

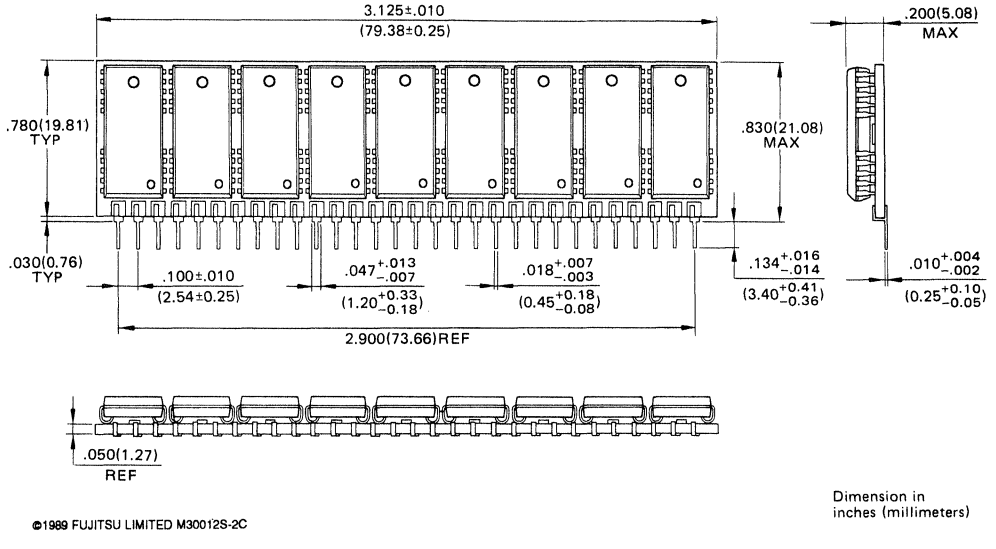
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$(8)	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) $t_{RCH} \geq t_{RCH}$ (min)
Read (Static Column)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WS} \geq t_{WS}$ (min) $t_{WH} \geq t_{WH}$ (min)
Write (Static Coulmn)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WS} \geq t_{WS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X Either V_{IH} or V_{IL}.
* $\overline{RAS}$ puts V_{IH} at once.

PACKAGE DIMENSIONS
(Suffix: PJPS)

30-LEAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P04)



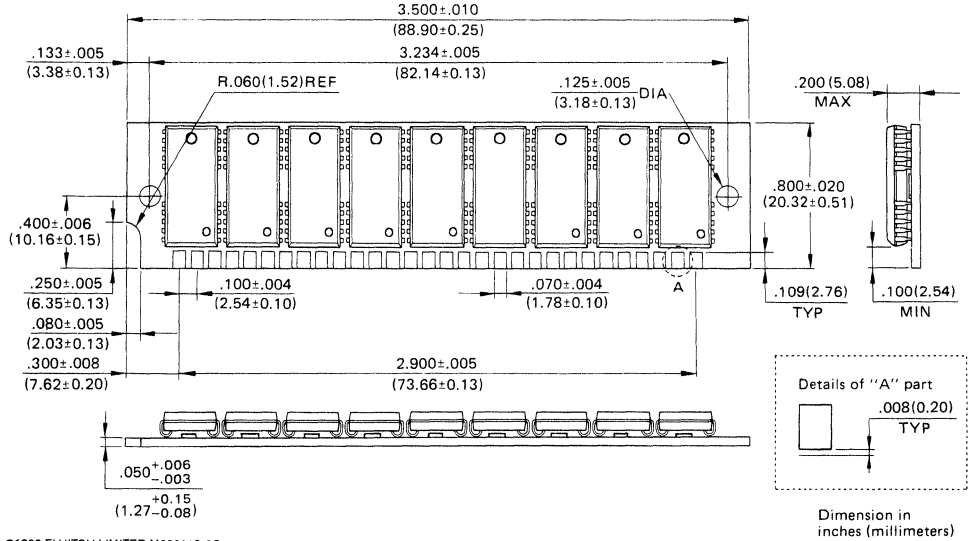
Dimension in
inches (millimeters)

5

PACKAGE DIMENSIONS

(Suffix: PJPB)

30-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-30P-P03)



5

5

FUJITSU

262144×9 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

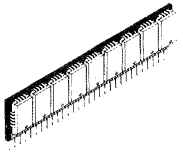
MB85240-10
MB85240-12

December 1987
Edition 1.0

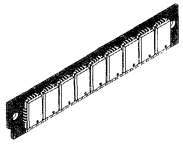
262,144 x 9 BIT CMOS STATIC COLUMN RANDOM ACCESS MEMORY

This Fujitsu MB85240 is a fully decoded, 262,144 words x 9 bits CMOS static column random access memory composed of nine 256k SCRAM chips (MB81C258x9). This module is designed for high speed, high performance applications such as main frame memory, buffer memory, and video memory, and for applications to battery backed-up systems where very low power dissipation and compact layout is required. The electrical characteristics of the MB85240 are quite same as the original MB81C258; each timing requirements are noncritical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

- 262,144 x 9 SCRAM MODULE, 30-pin SIP and socket type
- Row Access Time (t_{RAC})
  - 100 ns max. (MB85240-10)
  - 120 ns max. (MB85240-12)
- Random Cycle Time (t_{RC})
  - 200 ns min. (MB85240-10)
  - 230 ns min. (MB85240-12)
- Address Access Time (t_{AA})
  - 45 ns max. (MB85240-10)
  - 55 ns max. (MB85240-12)
- Static Mode Cycle Time (t_{SC})
  - 50 ns min. (MB85240-10)
  - 60 ns min. (MB85240-12)
- Low Power Dissipation
  - 2970 mW max. (MB85240-10)
  - 2475 mW max. (MB85240-12)
  - 99 mW max. standby with TTL level input
  - 15 mW max. standby with CMOS level input
- +5V supply, ±10% tolerance
- 32ms/256 refresh cycles capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability

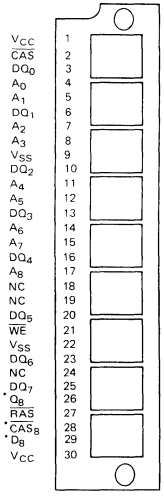


PLASTIC PACKAGE
MSP-30P-P02



PLASTIC PACKAGE
MSS-30P-P01

PIN ASSIGNMENT



* ; For parity bit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 – FUNCTIONAL BLOCK DIAGRAM

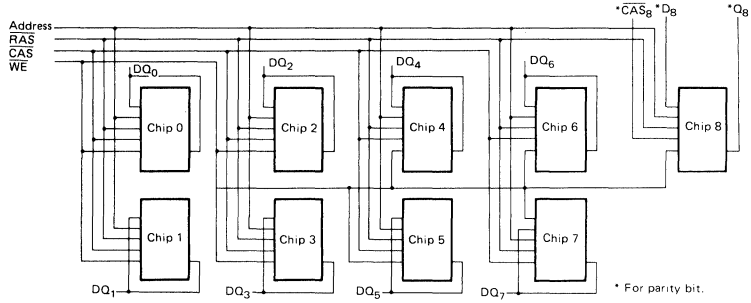
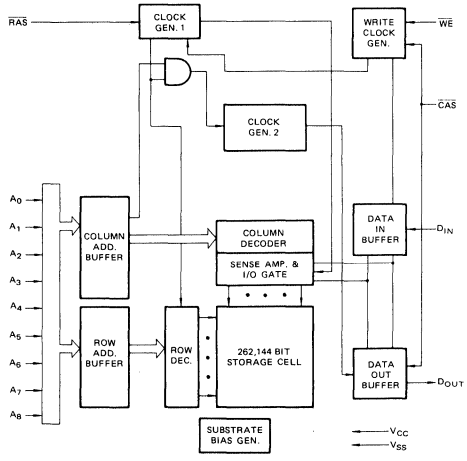


Fig. 2 – BLOCK DIAGRAM FOR EACH CHIP



5

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A_0 to A_8	C_{IN1}		80	pF
Input Capacitance, $\overline{RAS}$	C_{IN2}		88	pF
Input Capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input Capacitance, $\overline{WE}$	C_{IN4}		49	pF
Input Capacitance, $\overline{CAS}_8$	C_{IN5}		11	pF
Input Capacitance, D_8	C_{IN6}		7	pF
I/O Capacitance, DQ_0 to DQ_7	C_{DQ}		15	pF
Output Capacitance, Q_8	C_O		11	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	–	6.5	V	
Input Low Voltage	V_{IL}	-1.0	–	0.8	V	

Note *: Ambient temperature is dependent on cycle time and cooling conditions.
See the derating curve Fig. 3 for normal cycle, and Fig. 4 for static mode cycle.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING/REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB85240-10	I_{CC1}		540	mA
	MB85240-12			450	
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	TTL Level	I_{CC2}		18	mA
	CMOS Level			2.7	
STATIC MODE OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{WE}$ or Address = cycling; t_{SC} = min)	MB85240-10	I_{CC3}		360	mA
	MB85240-12			315	
$\overline{CAS}$-BEFORE-RAS REFRESH CURRENT* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$ refresh; t_{RC} = min)	MB85240-10	I_{CC4}		495	mA
	MB85240-12			405	
INPUT LEAKAGE CURRENT, ALL INPUTS (V_{IN} = 0V to 5.5V, V_{CC} = 5V, V_{SS} = 0V, all other inputs not under test = 0V)		$I_{I(L)1}$ ($\overline{CAS}_8$, D_8)	-10	10	μA
		$I_{I(L)2}$ (Others)	-30	30	
OUTPUT LEAKAGE CURRENT Each output is high impedance (Data is disable, V_{OUT} = 0V to 5.5V)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output High Voltage (I_{OH} = -5 mA)		V_{OH}	2.4		V
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	

Note 1): I_{CC} is dependent on the output loading and cycle time. Output pins are open.

5

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter NOTE	Symbol	MB85240-10		MB85240-12		Unit
		Min	Max	Min	Max	
Time between Refresh	t_{REF}	–	32	–	32	ms
Random Read/Write Cycle Time	t_{RC}	200	–	230	–	ns
Read-Modify-Write Cycle Time 15	t_{RWC}	245	–	285	–	ns
Access Time from $\overline{RAS}$ 3 5	t_{RAC}	–	100	–	120	ns
Access Time from $\overline{CAS}$	t_{CAC}	–	25	–	30	ns
Output Buffer Turn Off Delay Time	t_{OFF}	0	25	0	25	ns
Transition Time	t_T	3	50	3	50	ns
Column Address Access Time 4 5	t_{AA}	–	45	–	55	ns
Output Hold Time from Column Address Change	t_{AOH}	5	–	5	–	ns
Access Time from $\overline{WE}$ Precharge 15	t_{WPA}	–	25	–	30	ns
Access Time Relative to Last Write 6 15	t_{ALW}	–	90	–	110	ns
Write latched Output Hold Time 15	t_{WOH}	0	–	0	–	ns
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	ns
$\overline{RAS}$ Pulse Width	t_{RAS}	65	100000	75	100000	ns
$\overline{RAS}$ Hold Time	t_{RSH}	25	–	30	–	ns
$\overline{CAS}$ Pulse Width (Read)	t_{CAS}	25	100000	30	100000	ns
$\overline{CAS}$ Pulse Width (Write)	t_{CAS}	15	100000	20	100000	ns
$\overline{CAS}$ Hold Time (Read)	t_{CSH}	100	–	120	–	ns
$\overline{CAS}$ Hold Time (Write)	t_{CSH}	80	–	95	–	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	25	90	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time	t_{CRS}	20	–	25	–	ns
Row Address Set Up Time	t_{ASR}	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	15	–	15	–	ns
Column Address Set Up Time 7	t_{ASC}	0	–	0	–	ns
Column Address Hold Time 7	t_{CAH}	20	–	25	–	ns
$\overline{RAS}$ to Column Address Delay Time 8 9	t_{RAD}	20	55	20	65	ns
Column Address Hold Time Reference to $\overline{RAS}$	t_{AR}	100	–	120	–	ns
Write Address Hold Time Referenced to $\overline{RAS}$	t_{AWR}	80	–	90	–	ns

5

AC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.) Note 1, 2

Parameter	NOTE	Symbol	MB85240-10		MB85240-12		Unit
			Min	Max	Min	Max	
Read Address to $\overline{RAS}$ Lead Time		t_{RAL}	45	–	55	–	ns
Column Address Hold Time Referenced to $\overline{RAS}$ Rising Time	10	t_{AHR}	15	–	15	–	ns
Last Write to Column Address Delay Time	11 12 15	t_{LWAD}	25	45	30	55	ns
Column Address Hold Time Referenced to Last Write		t_{AHLW}	90	–	110	–	ns
Read Command Set Up Time Referenced to $\overline{CAS}$		t_{RCS}	0	–	0	–	ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	10	–	10	–	ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0	–	0	–	ns
$\overline{WE}$ Pulse Width		t_{WP}	15	–	20	–	ns
$\overline{WE}$ Inactive Time		t_{WI}	15	–	20	–	ns
Write Command Hold Time		t_{WCH}	15	–	20	–	ns
Write Command to $\overline{RAS}$ Lead Time	15	t_{RWL}	25	–	30	–	ns
Write Command to $\overline{CAS}$ Lead Time	15	t_{CWL}	25	–	30	–	ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time	14 15	t_{RWD}	100	–	120	–	ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	t_{CWD}	25	–	30	–	ns
Column Address to $\overline{WE}$ Delay Time	15	t_{AWD}	45	–	55	–	ns
$\overline{RAS}$ to Second Write Delay Time		t_{RSWD}	105	–	125	–	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	80	–	95	–	ns
Write Set Up Time for Output Disable	14	t_{WS}	0	–	0	–	ns
Write Hold Time for Output Disable	14	t_{WH}	0	–	0	–	ns
D_{IN} Set Up Time		t_{DS}	0	–	0	–	ns
D_{IN} Hold Time		t_{DH}	20	–	25	–	ns
D_{IN} Hold Time Reference to $\overline{RAS}$		t_{DHR}	80	–	90	–	ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)		t_{FCS}	20	–	25	–	ns

5

AC CHARACTERISTICS (Cont'd)

(Recommended operating conditions unless otherwise noted.) Note 1, 2

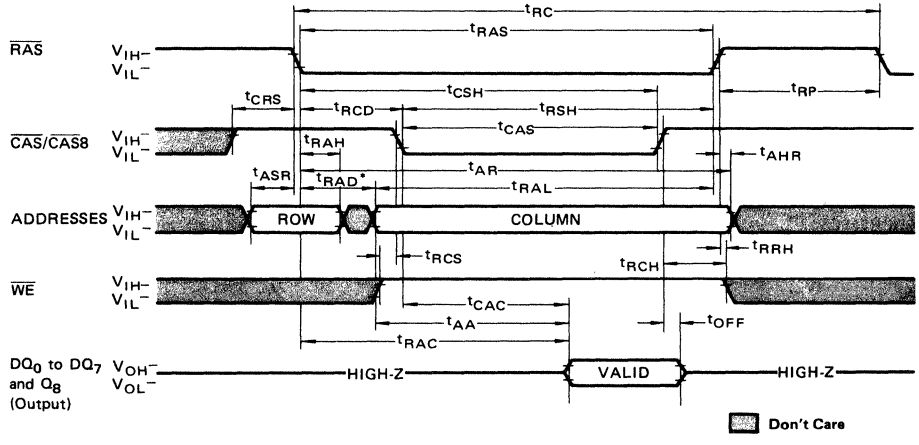
Parameter NOTES	Symbol	MB85240-10		MB85240-12		Unit
		Min	Max	Min	Max	
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{FCH}	20	–	25	–	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20	–	25	–	ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)	t_{RPC}	20	–	20	–	ns
Static Mode Read/Write Cycle Time	t_{SC}	50	–	60	–	ns
Static Mode Read-Modify-Write Cycle Time 15	t_{SRWC}	95	–	115	–	ns
Static Mode $\overline{CAS}$ Precharge Time	t_{CP}	15	–	20	–	ns

5

NOTES:

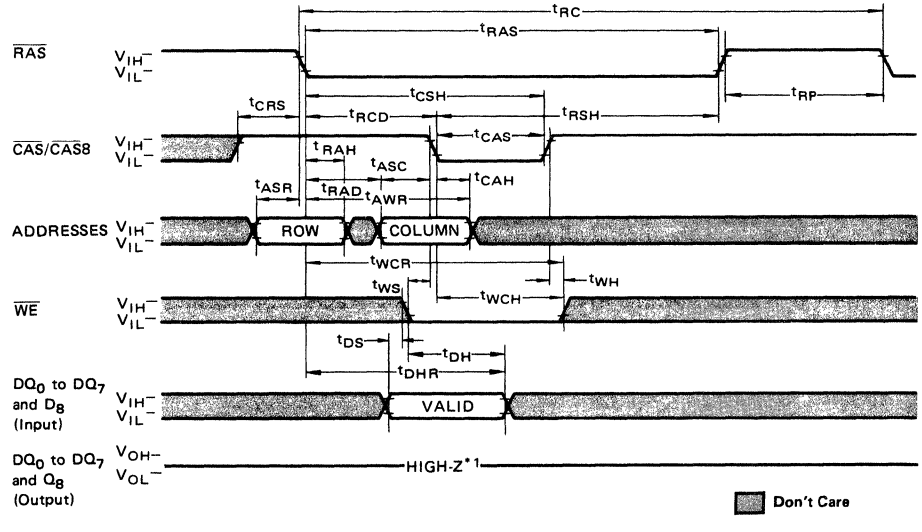
1. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC characteristics assume t_T = 5ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
4. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} will be increased by the amount that t_{LWAD} exceeds the value shown.
7. Write Cycle Only.
8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
9. t_{RAS} (min) = t_{RAH} (min) + t_T (t_T = 5ns)
10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.
11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.
12. t_{LWAD} (min) = t_{AHW} (min) + t_T (t_T = 5ns)
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geq t_{RWD}$ (min). The data output will contain data read from the selected cell.
15. Parity bit only.

Read Cycle



*; If $t_{RAD} \geq t_{RAD}$ (max), access time is t_{AA}

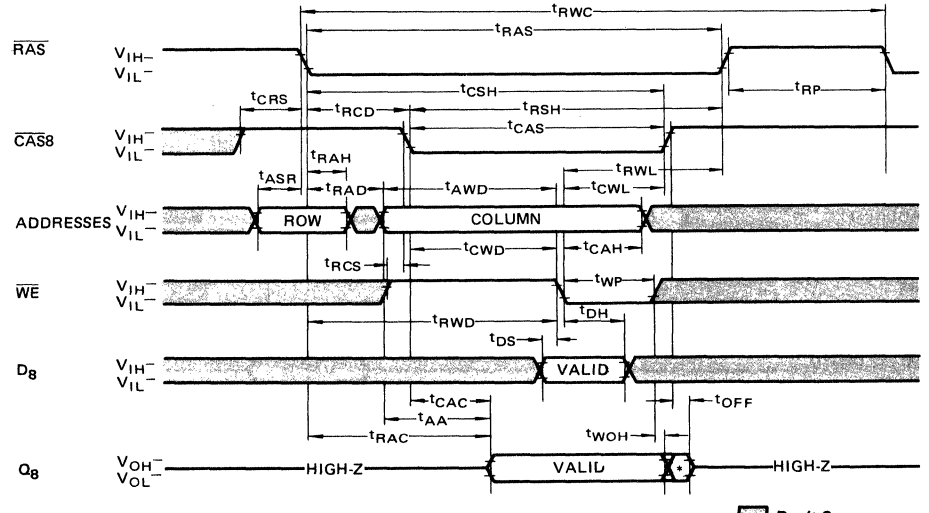
Write Cycle ($\overline{CAS}$ Controlled)



*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

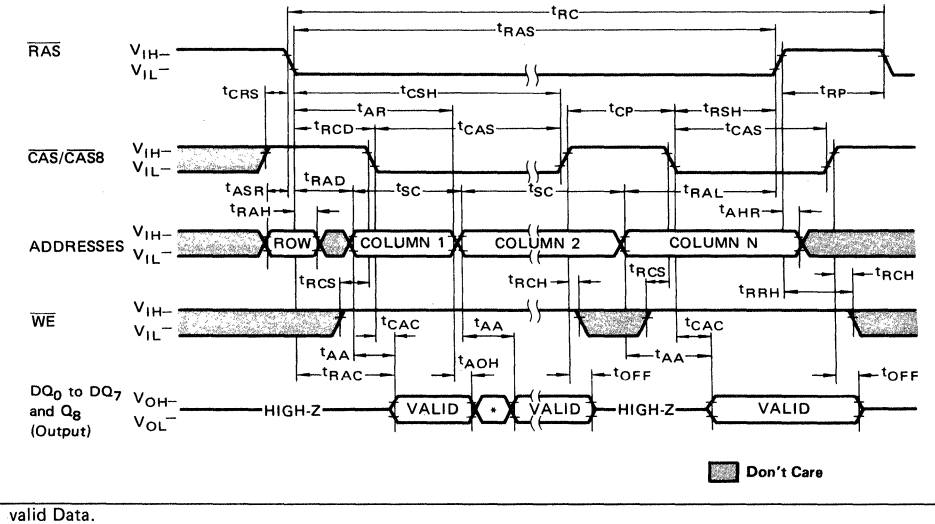
5

Read-Modify-Write Cycle
(Note; Only for parity bit.)



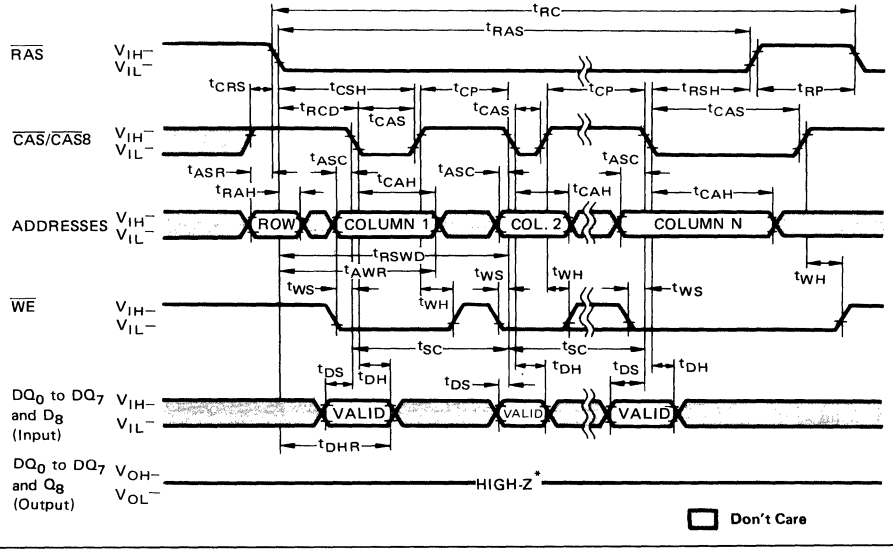
*; Invalid Data

Static Mode Read Cycle



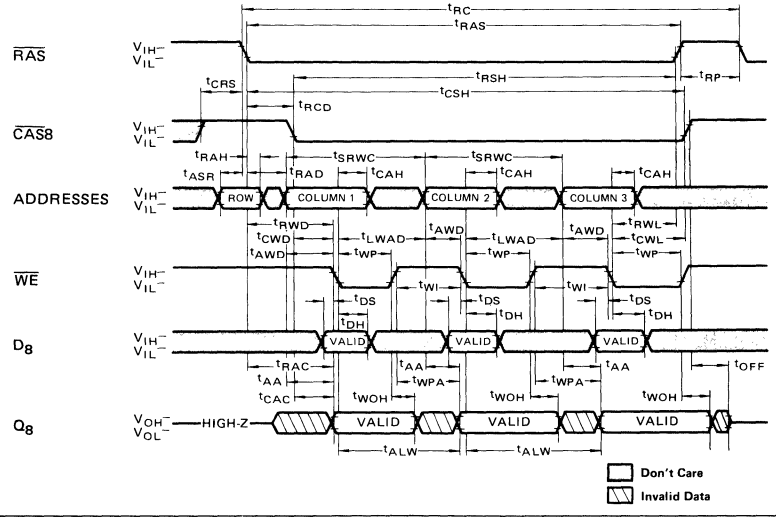
valid Data.

Static Mode Write Cycle



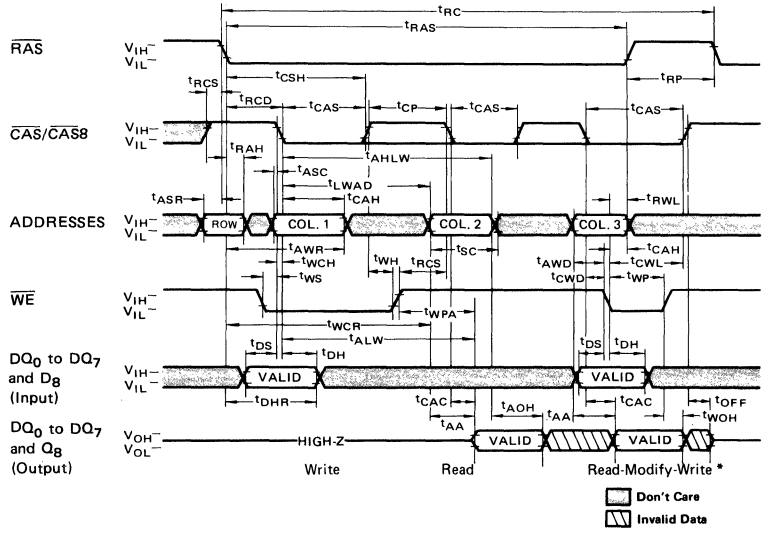
*; If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), D_{OUT} is high-Z.

Static Mode Read-Modify-Write
(Note; Only for parity bit.)



5

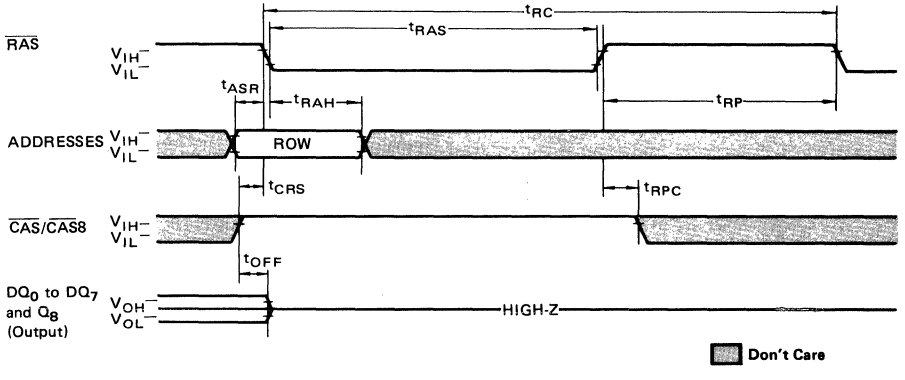
Static Mode Mixed Cycle



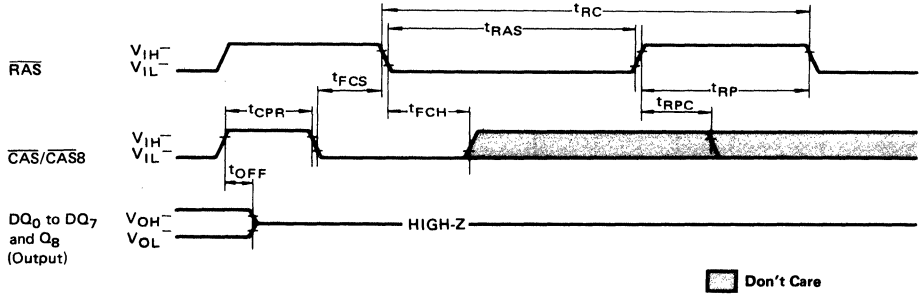
*; Only for parity bit.

RAS-Only Refresh Cycle

(Note; $\overline{WE}$, D_{IN} = Don't Care, $A_8 = V_{IH}$ or V_{IL})

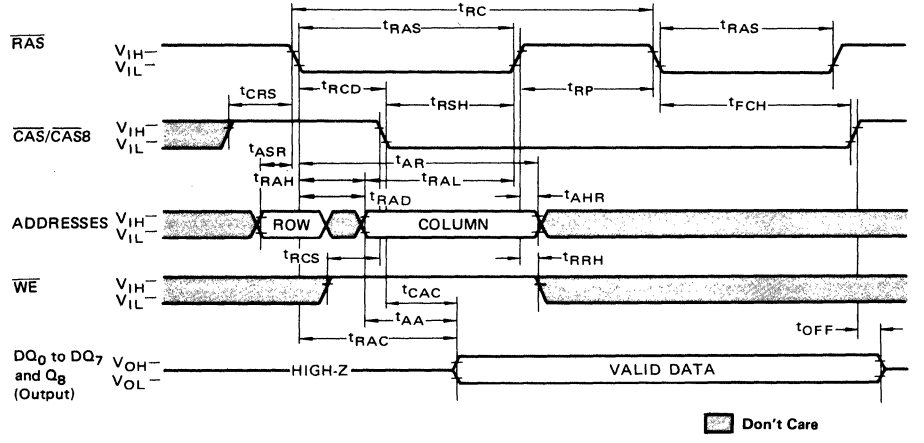


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
(Note; Address, $\overline{WE}$, D_{IN} = Don't Care)



5

Hidden Refresh Cycle



FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out[1)]	Ready cycle
L	L	L	Valid Data In[2)]	Write cycle
L	L[3)]	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L[4)]	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Pairyt bit) Read-Write/Read-Modify-Write (Parity bit)

Notes: 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geqq t_{FCS}$ (min)
4): $t_{CWD} \geqq t_{CWD}$ (min)

5

DESCRIPTION

Address Inputs:
A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within each MB81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe ($\overline{RAS}$). The nine column address bits are established on the address input pins (A_0 to A_8) after the Row Address Hold Time (t_{RAH}) has been satisfied. In read cycle, the column address are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column address are latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Write Enable:
Read or Write cycle is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write cycle. The write operation is asserted on the later falling edge of $\overline{CAS}$ or $\overline{WE}$ (Both $\overline{CAS}$ and $\overline{WE}$ are low). The time period of the write operation is determined by internal circuit, thus next write operation will be inhibited during the write operation.

Data Input:
Data is written into the MB85240 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{WE}$.

Data Output:
Each output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. Each output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:
1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC} = t_{RCD} + t_{CAC}$ or $t_{RAC} = t_{RAD} + t_{AA}$.
Data outputs remain valid while the column address inputs are kept constant. However, when $\overline{CAS}$ goes high, the output returns to high impedance state.

Static Mode:
The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.
1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{WE}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle.
3. Static mode read-modify-write cycle;
   In the static mode read-modify-write cycle, $\overline{WE}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge a of $\overline{WE}$.
4. Static mode mixed cycle;
   In the static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.
1. t_{ALW} from the later falling edge of $\overline{CAS}$ or $\overline{WE}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{WE}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.

Refresh:
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7) at least every 32ms.
The MB85240 offers the following three types of refresh.
1. $\overline{RAS}$-only refresh;
   The $\overline{RAS}$-only refresh avoids any output during refresh because each output buffer is high impedance state due to $\overline{CAS}$ high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. During $\overline{RAS}$-only refresh cycle, either V_{IH} or V_{IL} is permitted to A_8.
2. CAS-before-RAS refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB85240 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the internal refresh address counter are enabled, and an internal refresh operation is executed. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.
3. Hidden refresh;
   A hidden refresh cycle will be executed while maintaining latest valid output datas at the DQ pins by extending the $\overline{CAS}$ low time. For the MB85240, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Notice for using MB8520
The MB85240 is a SIP (Single-In-Line-Package) module which is composed of nine MB81C258 DRAMs housed in plastic LCC, and assembled on the epoxy printed circuit board. Generally the multilayer PCB board has large wiring capacitance. This disadvantage causes relatively noise induction between signal lines and power supply lines (V_{SS} or V_{CC}).
Furthermore, as the MB85240 is a very high-speed memory, the timing windows to strobe address $\overline{WE}$ and D_{IN} signals are very short (Approx. 10ns). Therefore, it is very sensitive even to very sharp noise.
From the above reasons, special care should be taken for use the MB85240. The following notices are recommended;

5

DESCRIPTION

1. Provide a externally capacitor of approx. a few μF each module, the MB85240 has the nine decoupling capacitors (0.22 μF on each SCRAM 0.22 μF x 9).
2. Remove noise, riging, overshoot and undershoot from the address, clocks and DQ lines, so that the MB85240 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate dumping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

Fig. 3 – MB85240 DERATING CURVE

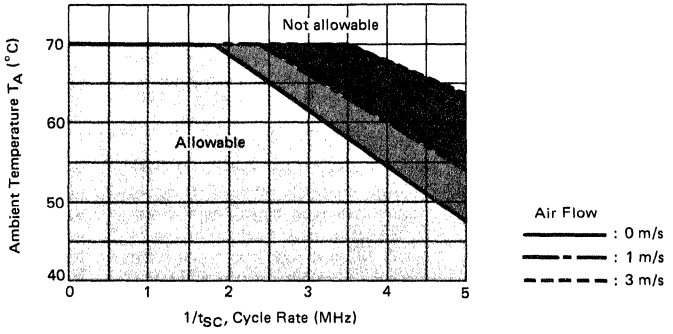
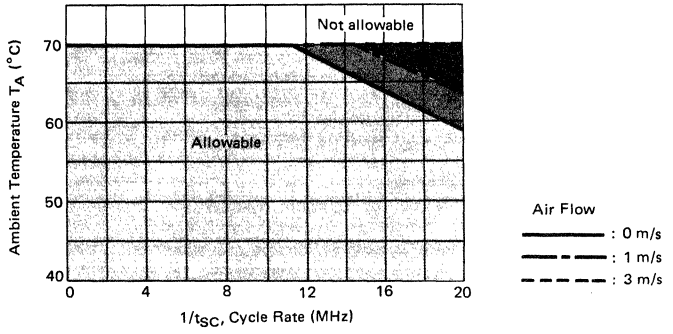
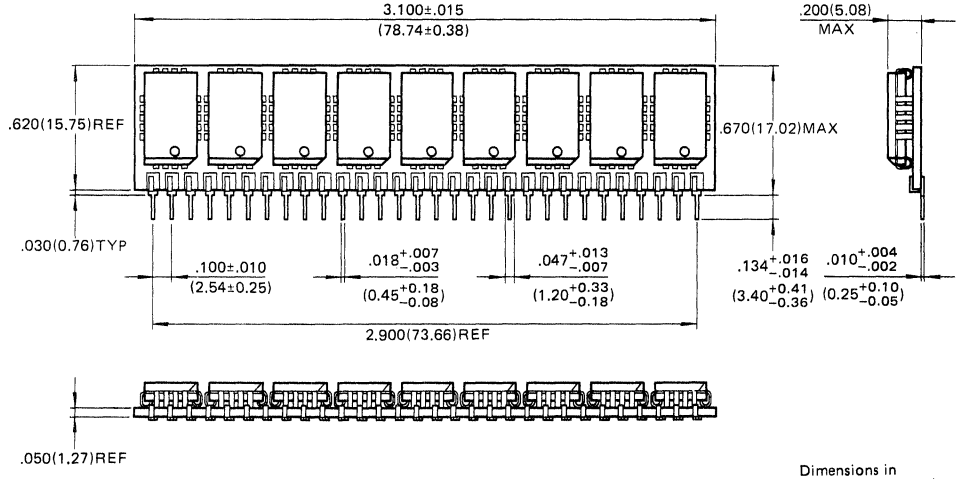


Fig. 4 – MB85240 DERATING CURVE



PACKAGE DIMENSIONS

30-LEAD SINGLE IN-LINE TYPE MODULE
(CASE No.: MSP-30P-P02)

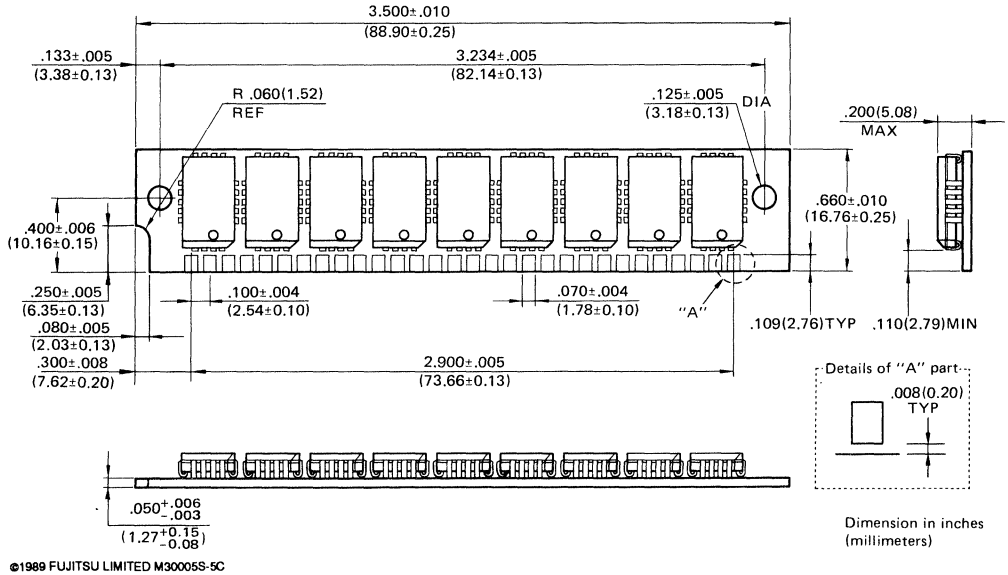


Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS

30-PAD PLASTIC SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSS-30P-P01)



5

September 1989
TS042-A899

FUJITSU

DATA SHEET

MB85254-80 / -10 / -12

CMOS 512K x 40 DYNAMIC RANDOM ACCESS MEMORY MODULE

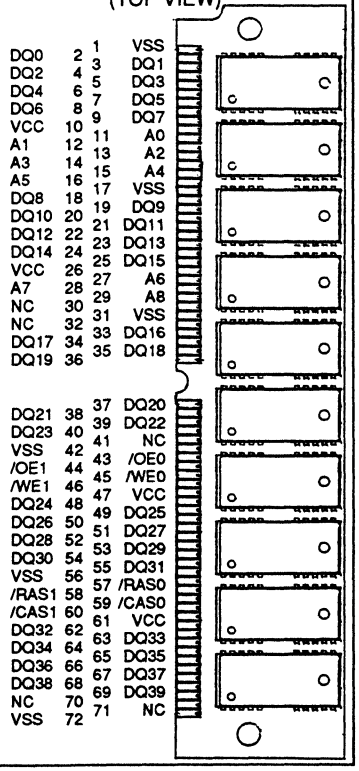
PRELIMINARY

The Fujitsu MB85254 is a fully decoded, CMOS dynamic random access memory module consists of twenty MB81C1000 devices, the MB85254 is optimized for those applications requiring high speed, high performance, large momory storage, and high density in ECC (Error Checking and Correction) memory organizations.

- Organization :
  524,288 words x 40 bit
- Memory :
  MB81C1000, 20 pcs
- $\overline{RAS}$ Access time :
  80ns max. (MB85254-80)
  100ns max. (MB85254-10)
  120ns max. (MB85254-12)
- $\overline{CAS}$ Access time :
  25ns max. (MB85254-80)
  30ns max. (MB85254-10)
  35ns max. (MB85254-12)
- Column Address Access time :
  45ns max. (MB85254-80)
  50ns max. (MB85254-10)
  60ns max. (MB85254-12)
- Active Power :
  3.960mW max. (MB85254-80)
  3.410mW max. (MB85254-10)
  2.860mW max. (MB85254-12)
- Standby :
  220mW max. (CMOS Level)
  110mW max. (TTL Level)
- Single +5V supply ±10% torelance
- TTL compatible I/O
- Decoupling Capacitor :
  0.22µF, 20 pcs
- JEDEC Standard 72-pin SIMM Package Outline

PLASTIC PACKAGE
MSS-72P-Pxx

PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

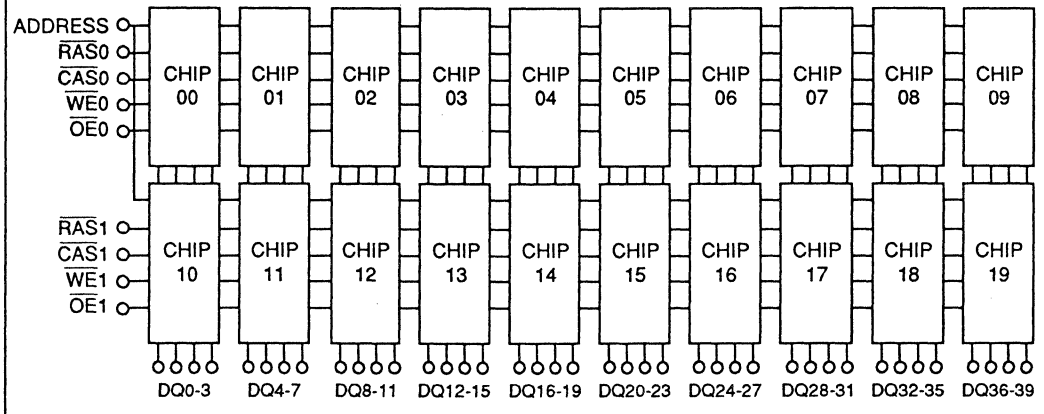
ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-1.0 to +7.0	V
Input Voltage	VIN	-1.0 to +7.0	V
Output Voltage	VOUT	-0.5 to + 7.0	V
Short Circuit Output Current	IOUT	±50	mA
Power Dissipation	PD	20.0	W
Storage Temperature	TSTG	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGES are exceeded. Functioncal operation should be restricted to the conditions as detailed in the operationcal sections of this data sheet. Exposure to absolute maximu rating conditions for exteded period may affect devise reliability.

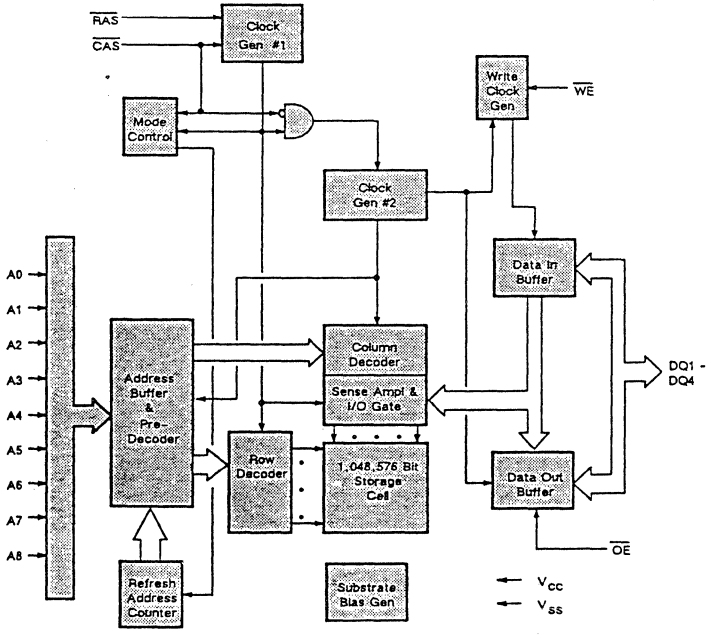
5

Fig. 1 - BLOCK DIAGRAM



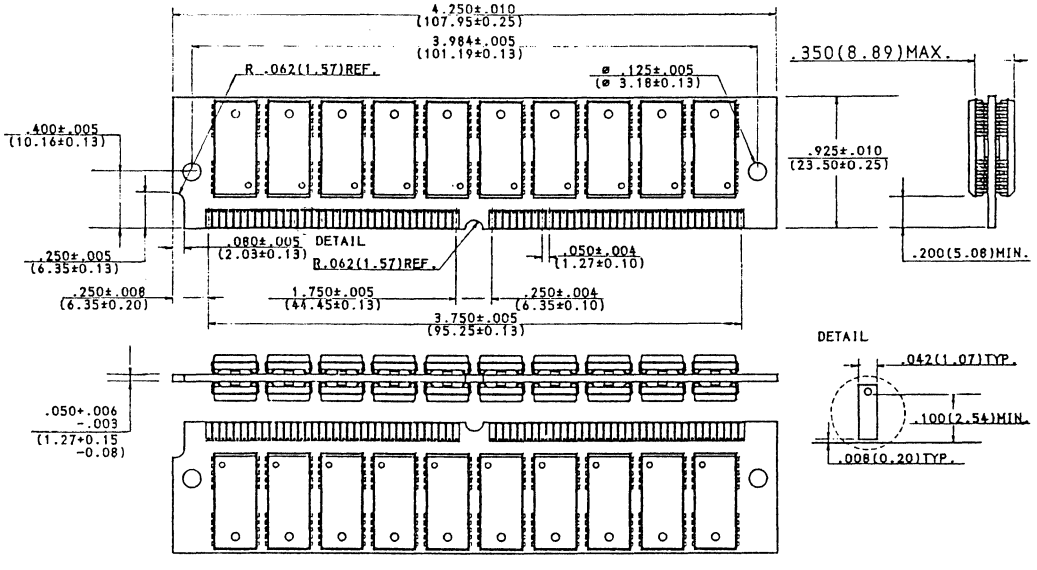
5

Fig. 2 - BLOCK DIAGRAM for EACH CHIP



PACKAGE DIMENSIONS

(Suffix : PJPBK)



Note : Dimensions in inches and (milimeters)

5

5

FUJITSU

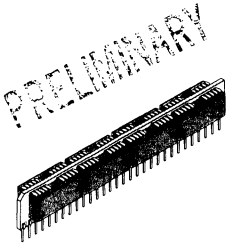
1M x 8 DRAM MODULE

MB85260-10
MB85260-12

1,048,576 x 8 BIT DYNAMIC RANDOM ACCESS MEMORY MODULE

TS033-A882
Feb. 1988

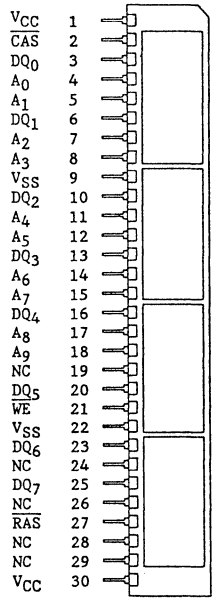
The Fujitsu MB85260 is a fully decoded, dynamic CMOS random access memory module with eight MB81C1000, in 26-pin SOJ packages, and eight .22µF decoupling capacitor under the each memory, mounted on a low profile 30-pin SIP module. Organized as 1,048,576 x 8-bit words, the MB85260 PCB module is optimized for those applications requiring high density and large memory storage capability. The operation and electrical characteristics of the MB85260 are the same as the MB81C1000 devices which feature a Fast Page mode operation.



PLASTIC PACKAGE
MSP-30P-P06

- 1,048,576 x 8 DRAM, 30-pin SIP
- Row access time (t_{RAC}):
  100 ns max. (MB85260-10)
  120 ns max. (MB85260-12)
- Cycle time (t_{RC}):
  180 ns min. (MB85260-10)
  210 ns max. (MB85260-12)
- Column access time (t_{CAC}):
  30 ns max. (MB85260-10)
  35 ns max. (MB85260-12)
- Fast Page mode cycle time (t_{PC}):
  60 ns max. (MB85260-10)
  70 ns max. (MB85260-12)
- Dual +5V supply, ±10% tolerance
- Low power:
  Active = 2640 mW max. (MB85260-10)
  2200 mW max. (MB85260-12)
  Standby = 44 mW max. (CMOS level)
- Refresh:
  - 8.2 ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$" and "Hidden" refresh capabilities
- TTL compatible inputs and outputs
- Leaded and Leadless type are available.
- JEDEC standard (30-pin SIP) pin assignment

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-1 to +7	V
Storage temperature	T_{STG}	-55 to 125	°C
Power dissipation	P_D	9.0	W
Short circuit output current	–	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 - BLOCK DIAGRAM

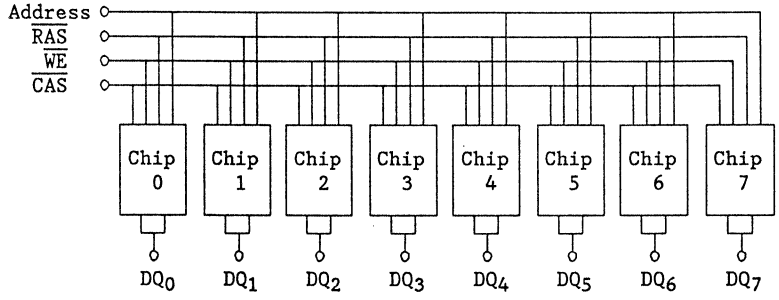
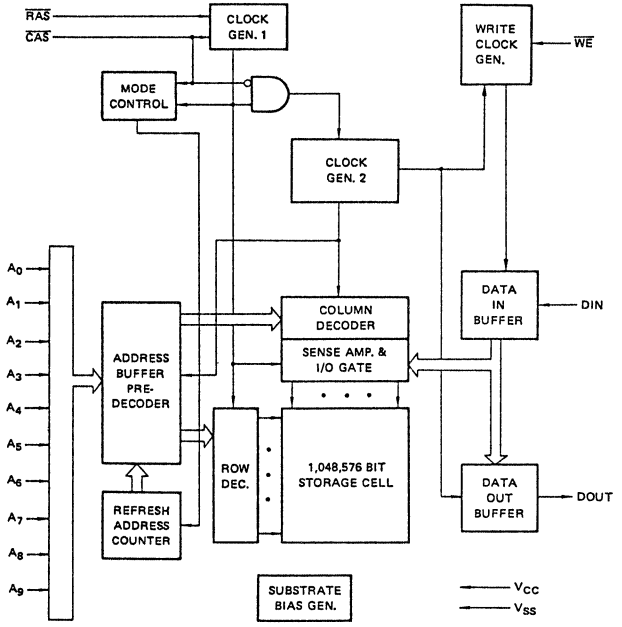


Fig. 2 - BLOCK DIAGRAM FOR EACH CHIP



CAPACITANCE (T_A=25°C, f=1MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9	C_{IN1}	-	TBD	pF
Input Capacitance, RAS	C_{IN2}	-	TBD	pF
Input Capacitance, CAS	C_{IN3}	-	TBD	pF
Input Capacitance, WE	C_{IN4}	-	TBD	pF
I/O Capacitance, DQ0 to DQ7	C_{DQ}	-	TBD	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V
Input High Level, all inputs	V_{IH}	2.4		6.5	V
Input Low Level, all inputs all DQs	V_{IL1} V_{IL2}	-2.0 -1.0*1		0.8 0.8	V V
Operating Temperature Range	T_A	0	25	70*2	°C

Note: *1 The device will withstand undershoots to the -2.0V level with a maximum pulse width of 20ns at the -1.5V level.
*2 Maximum ambient temperature is permissible under certain conditions.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (conditions)		Symbol	Value			Unit
			Min	Typ	Max	
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC}=min.)	MB85260-10	I_{CC1}			480	mA
	MB85260-12				400	
STANDBY CURRENT Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	TTL level	I_{CC2}			16	mA
	CMOS level				8	
REFRESH CURRENT 1 Average Power Supply Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$=min cycling)	MB85260-10	I_{CC3}			440	mA
	MB85260-12				360	
FAST PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycling, t_{SC}=min)	MB85260-10	I_{CC4}			320	mA
	MB85260-12				264	
REFRESH CURRENT 2 Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC}=min)	MB85260-10	I_{CC5}			440	mA
	MB85260-12				360	
INPUT LEAKAGE CURRENT		I_{IL1}	-30		30	µA
OUTPUT LEAKAGE CURRENT		I_{OL}	-10		10	µA
OUTPUT HIGH LEVEL (I_{OH}=-5mA)		V_{OH}	2.4			V
OUTPUT LOW LEVEL (I_{OL}=4.2mA)		V_{OL}			0.4	V

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85260-10		MB85260-12		Unit
			Min	Max	Min	Max	
Time Between Refresh		t_{REF}		8.2		8.2	ms
Random Read/Write Cycle Time	4	t_{RC}	180		210		ns
Access Time from $\overline{RAS}$	5,8	t_{RAC}		100		120	ns
Access Time from $\overline{CAS}$	6,8	t_{CAC}		30		35	ns
Access Time from Column Address	7,8	t_{AA}		50		60	ns
Output Data Hold Time		t_{OH}	7		7		ns
Output Buffer Turn On Delay Time		t_{ON}	5		5		ns
Output Buffer Turn Off Delay Time	9	t_{OFF}		25		25	ns
Input Transition Time		t_T	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	70		80		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	100000	120	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	30		35		ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	10,11	t_{RCD}	25	70	25	85	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	30		35		ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)		t_{CPN}	15		15		ns
Row Address Setup Time		t_{ASR}	0		0		ns
Row Address Hold Time		t_{RAH}	15		15		ns
Column Address Setup Time		t_{ASC}	0		0		ns
Column Address Setup Time		t_{CAH}	15		20		ns
$\overline{RAS}$ to Column Address Delay Time	12	t_{RAD}	20	50	20	60	ns
Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	50		60		ns
Read Command Setup Time		t_{RCS}	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	13	t_{RRH}	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	13	t_{RCH}	0		0		ns
Write Command Setup Time	14	t_{WCS}	0		0		ns
Write Command Hold Time		t_{WCH}	15		20		ns
$\overline{WE}$ Pulse Width		t_{WP}	15		20		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	25		30		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	20		25		ns
DIN Setup Time		t_{DS}	0		0		ns
DIN Hold Time		t_{DH}	15		20		ns
$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	0		0		ns
$\overline{CAS}$ Setup Time for CAS-before-$\overline{RAS}$ Refresh		t_{CSR}	0		0		ns
$\overline{CAS}$ Hold Time for CAS-before-$\overline{RAS}$ Refresh		t_{CHR}	15		20		ns

5

AC CHARACTERISTICS (Cont'd)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

Parameter	NOTES	Symbol	MB85260-10		MB85260-12		Unit
			Min	Max	Min	Max	
Fast Page Mode Read/Write Cycle Time	4	t_{PC}	60		70		ns
Access Time from $\overline{CAS}$ Precharge	8,15	t_{CPA}		60		70	ns
Fast Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	15		15		ns

NOTES;

1. An initial pause ($\overline{RAS}$=$\overline{CAS}$=V_{IH}) of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

2. AC characteristics assume t_T=5ns

3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH}(min) and V_{IL}(max).

4. The minimum cycle time depends upon the ambient temperature and cooling condition. See Fig. 3 and 4.

5. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} (or t_{RAD}) is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} (or t_{RAD}) exceeds the value shown. Refer to Fig. 5 and 6.

6. If $t_{RCD} \geq t_{RCD}$(max) and $t_{ASC} \geq t_{RCD}$(max) - t_{RAD}(max), access time is t_{CAC}.

7. If $t_{RAD} \geq t_{RAD}$(max), access time is t_{AA}.

8. Measured with a load equivalent to two TTL loads and 100 pF.

9. t_{OFF} is specified that output buffer changes to high impedance state.

10. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specfied as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

11. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ + t_{ASC} (min).

12. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

14. t_{WCS} is specified as a reference point only and must be satisfied for a write cycle.

15. t_{CPA} is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from Low to High.). Therefore, if t_{CP} is short, t_{CAC} is longer than t_{CAC}(max).

Fig.3 - MB85260 DERATING CURVE (Normal Cycle)

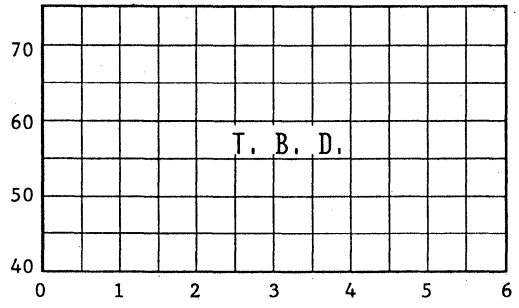
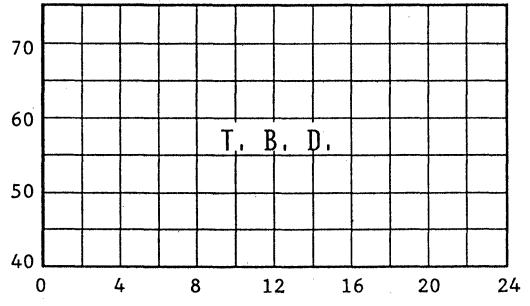


Fig.4 - MB85260 DERATING CURVE (Fast Page Mode Cycle)



5

Fig.5 - t_{RAC} vs t_{RCD}

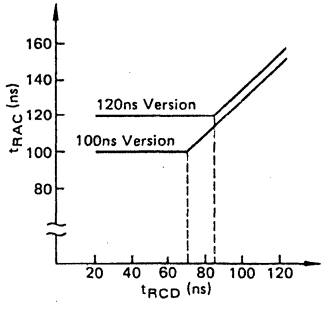
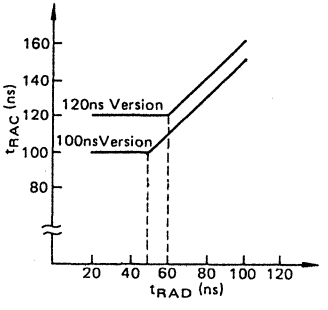
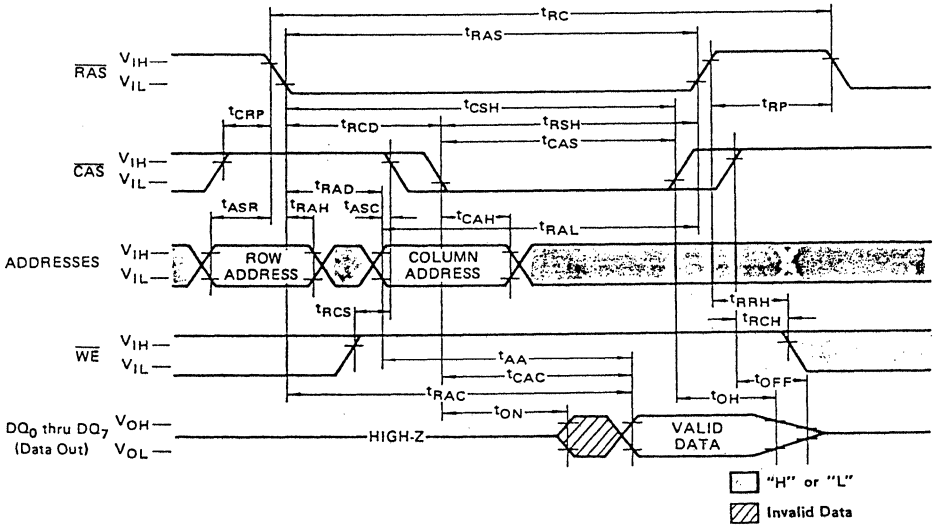


Fig.6 - t_{RAC} vs t_{RAD}

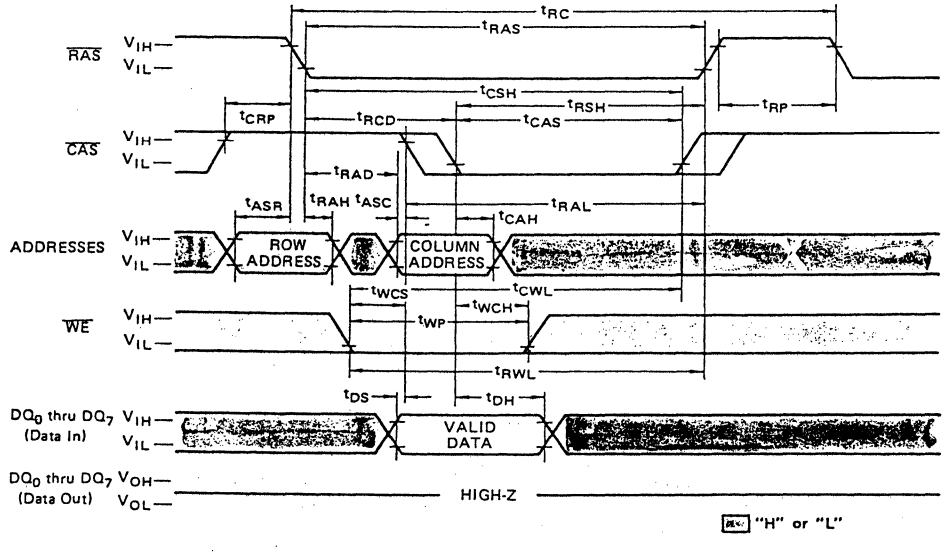


Read Cycle

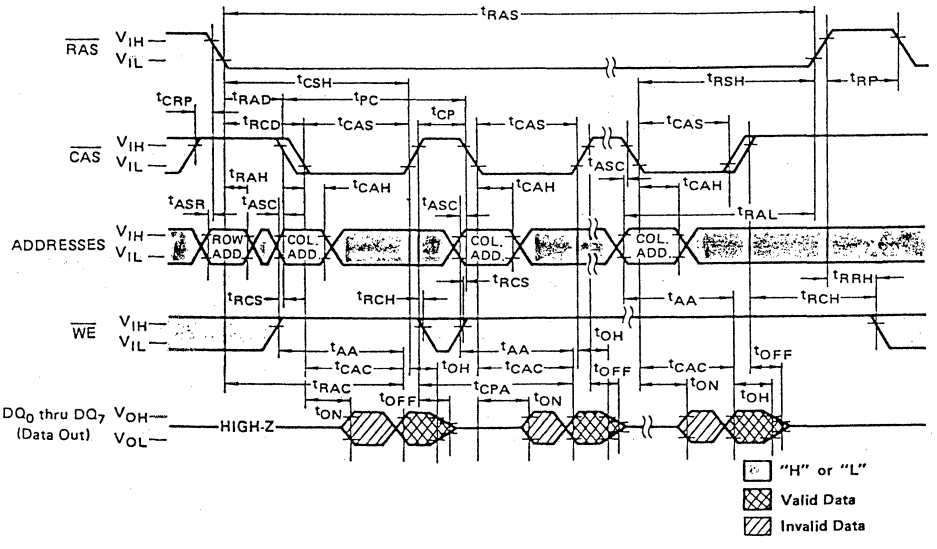


5

Write Cycle (Early Write)

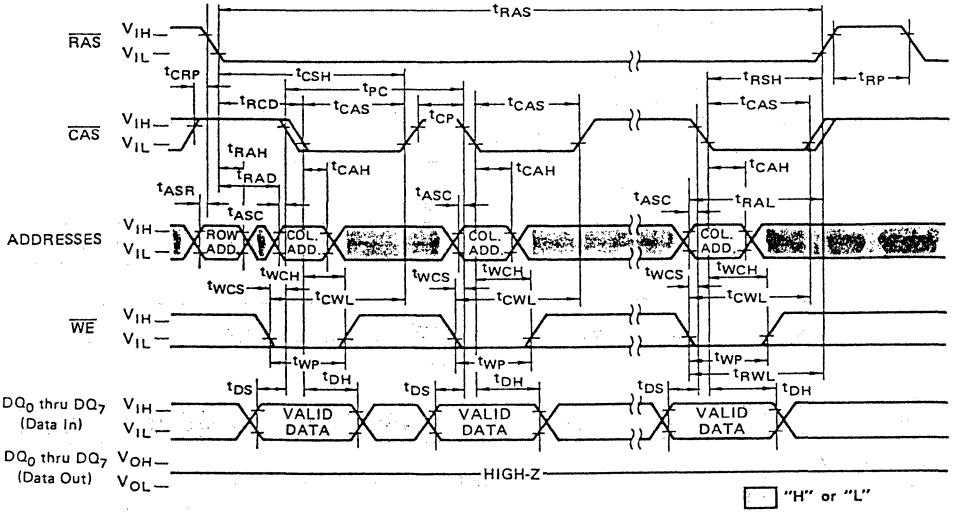


Fast Page Mode Read Cycle



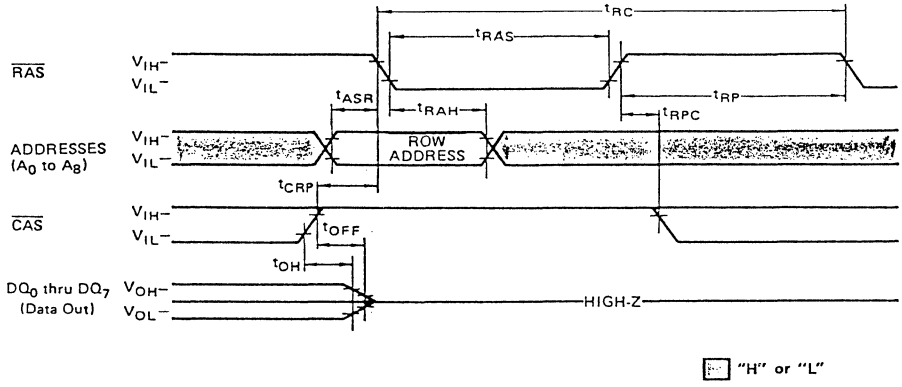
5

Fast Page Mode Write Cycle



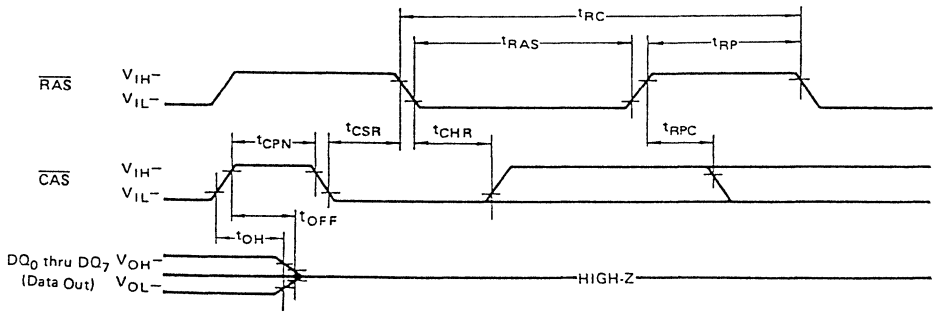
$\overline{RAS}$-only Refresh Cycle

NOTE : $\overline{WE}$, D, DQ(Input)=Don't care, Ag=V_{IH} or V_{IL}



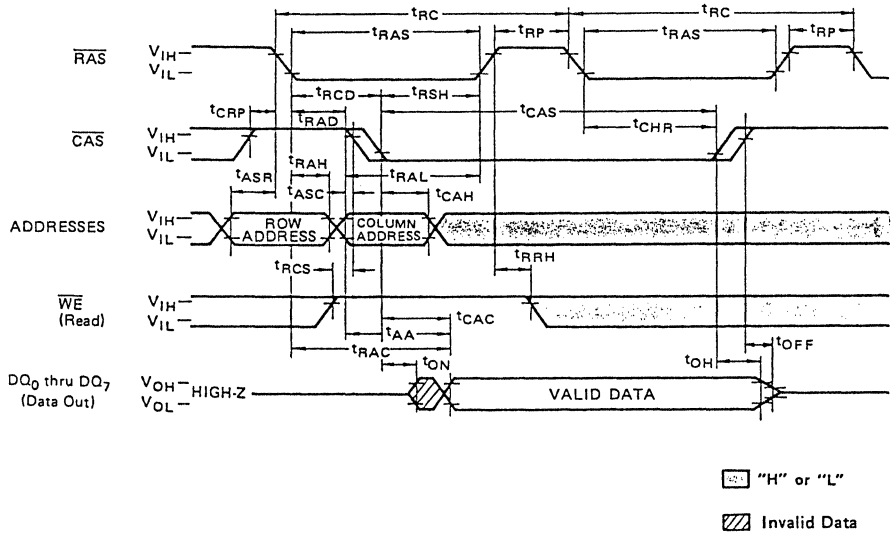
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

NOTE : Address, $\overline{WE}$, D, DQ(Input)=Don't care



5

Hidden Refresh Cycle



5

DESCRIPTION

Block Analysis:
As shown in Fig. 1 and Fig. 2, the MB85260 is composed of eight MB81C1000, and the memory selection of the each MB81C1000 consists of a 1024-by-1024 cell matrix. Operational modes of the device are shown in the FUNCTIONAL TRUTH TABLE below.

Address Inputs:
A total of twenty binary input address bits are required to decode any 8-bit of the 8,388,608 storage cells within the MB85260. Ten row address bits are established on the address input pins (A_0 to A_9) and latched with the Row Address Strobe, $\overline{RAS}$. The ten column address bits are established on the address input pins (A_0 to A_9) and latched with the Column Address Strobe, $\overline{CAS}$. All row and column addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. Since the flow through type address latches are used, address information at address pins are automatically latched as column address after $t_{RAH}(min)+ t_T$. Therefore, to get valid data within t_{RAC}, it is necessary to apply column address within $t_{RAD}(max)$. If $t_{RAD} \geq t_{RAD}(max)$, access time is t_{CAC} or t_{AA} whichever occurs later.

Write Enable:
Read or Write mode is selected with the $\overline{WE}$ inputs. A high on $\overline{WE}$ selects read cycle and low selects write mode.

Data Input/Output:
1. **Data Input;**
   The 8-bit data is written into the MB85260 during write cycle through each DQ pin. In write cycle, $\overline{WE}$ must be brought to low before falling edge of $\overline{CAS}$. Each input data is strobed and latched by falling edge of $\overline{CAS}$, and setup and hold times are referenced to $\overline{CAS}$.

2. **Data Output;**
   The output buffers on each chip are three state TTL compatible with a fan out of 2 TTL loads. Output data has the same porality as input data. The outputs are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output becomes valid within t_{RAC} from the falling edge of $\overline{RAS}$ when $t_{RCD}(max)$ and $t_{RAD}(max)$ are satisfied. In the meanwhile when either t_{RCD} or t_{RAD}, or both, are greater than their maximum value, the output data becomes valid within t_{CAC} or t_{AA} whichever occur later after falling edge of $\overline{CAS}$. The data output remains valid until CAS returns to high.

Read Cycle:
The read cycle is executed by keeping both $\overline{RAS}$ and $\overline{CAS}$ high, and keeping $\overline{WE}$ to high throughout the cycle. The row and column addresses are latched with $\overline{RAS}$ and $\overline{CAS}$, respectively. The valid data will appear at the DQ pins after determined by t_{RAC}, t_{CAC}, or t_{AA}. If t_{RCD} is greater than the specification, the access time is t_{CAC}. If t_{RAD} is greater than the specification, the access time is t_{AA}. The output data becomes invalid after $\overline{CAS}$ is brought high, with a delay time of t_{OH}, and the DQ pins return to the high impedance with t_{OFF}.

Write Cycle:
The write cycle is executed by the same manner as read cycle except for the state of $\overline{WE}$. The 8-bit data on DQ pins are latched with the falling edge of $\overline{CAS}$ and written into memory. In addition, during write cycle, t_{RWL}, t_{CWL}, and t_{RAL} must be satisfied the specifications.

DESCRIPTION (Continued)

Fast Page Mode Read Cycle:
The fast page mode read cycle is executed after normal cycle with holding $\overline{RAS}$ low, applying column address and $\overline{CAS}$, and keeping $\overline{WE}$ high. Since the row address during fast page mode cycle is latched by normal cycle, the cycle time is reduced. During this mode, the access time is t_{CAC}, t_{AA}, or t_{CPA}, whichever occur later. Any of each 1024 bits belonging to the internal row addresses can be accessed.

Fast Page Mode Write Cycle:
The fast page mode write cycle is executed by the same manner as fast page mode read cycle except for the state of $\overline{WE}$. The data on each DQ pins are latched with the falling edge of $\overline{CAS}$ and written into the memory. During this write cycle, t_{CWL} must be satisfied. Any of each 1024 bits belonging to the internal row addresses can be written into data within one $\overline{RAS}$ cycle.

Refresh:
The refresh of DRAM is executed by normal read and write cycle, i.e., the cells on each one row line, A_0 through A_8 except for A_9, are refreshed by one of two cycles. Each 512 row address must be refreshed every 8.2ms period. During the refresh cycle, the cell data connected to the selected row are sent to sense amplifier and re-write to the cell. The MB85260 also has three types of refresh modes below.

1. **$\overline{RAS}$-only Refresh;**
   The $\overline{RAS}$-only refresh is executed by keeping $\overline{RAS}$ low, and $\overline{CAS}$ remains high through the cycle. The row address to be refreshed is latched with the falling edge of $\overline{RAS}$. During this refresh, the data pins are kept high impedance state.

2. **$\overline{CAS}$-before-$\overline{RAS}$ Refresh;**
   The $\overline{CAS}$-before-$\overline{RAS}$ refresh is executed by bringing $\overline{CAS}$ low before $\overline{RAS}$ brought low. By this combination, the MB85260 executes $\overline{CAS}$-before-$\overline{RAS}$ refresh. The row address input is not necessary because it is generated internally. This internal row address counter is incremented automatically after every $\overline{CAS}$-before-$\overline{RAS}$ refresh is done.

3. **Hidden Refresh;**
   The hidden refresh is executed by keeping $\overline{CAS}$ low to next cycle during read mode, i.e., the output data at previous cycle is kept during next refresh cycle. Since the $\overline{CAS}$ is kept low continuously from the previous cycle, followed refresh cycle should be $\overline{CAS}$-before-$\overline{RAS}$ refresh.

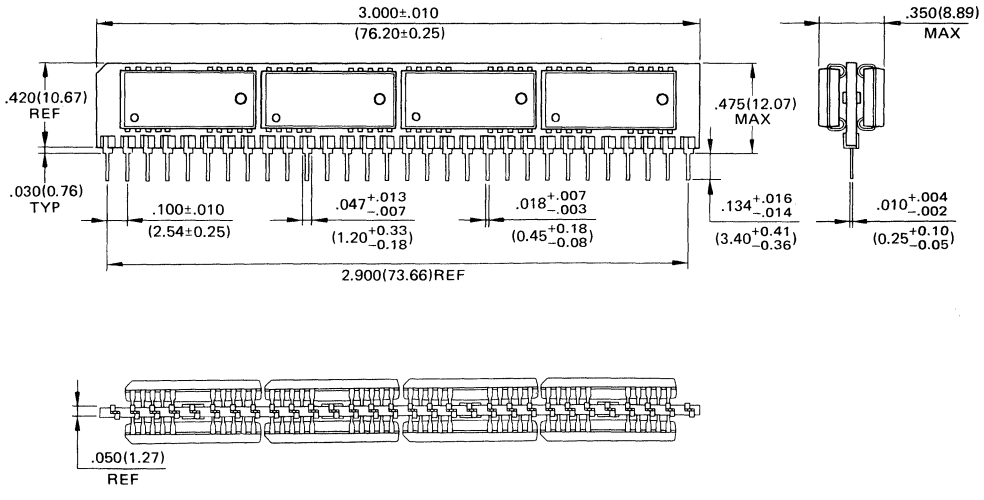
FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data I/O	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column		
Standby	V_{IH}	V_{IH}	X	X	X	High-Z	Cells are not refreshed.
Read (Normal)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min)
Read (Fast Page)	V_{IL}	V_{IL}	V_{IH}	Valid	Valid	Output Valid	$t_{RCS} \geq t_{RCS}$ (min) Cells are not refreshed.
Write (Normal)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min)
Write (Fast Page)	V_{IL}	V_{IL}	V_{IL}	Valid	Valid	Input Valid	$t_{WCS} \geq t_{WCS}$ (min) Cells are not refreshed.
$\overline{RAS}$-only Refresh	V_{IL}	V_{IH}	X	Valid	X	High-Z	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	V_{IL}	V_{IL}	X	X	X	High-Z	$t_{CSR} \geq t_{CSR}$ (min)
Hidden Refresh	V_{IL} *	V_{IL}	V_{IH}	X	X	Output Valid	Previous data is kept.

Note: X; Either V_{IH} or V_{IL}.
*; $\overline{RAS}$ puts V_{IH} at once.

PACKAGE DIMENSIONS
(Suffix: PJPS)

30-LEAD PLASTIC SINGLE-IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P06)



Dimension in
inches (millimeters)

5

FUJITSU

CMOS 1M x 9 DRAM MODULE

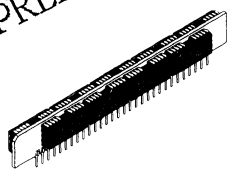
MB85265-10
MB85265-12

TS040-A892
February 1989

1M WORDS x 9-BIT HIGH SPEED CMOS DYNAMIC RANDOM ACCESS MEMORY MODULE

PRELIMINARY

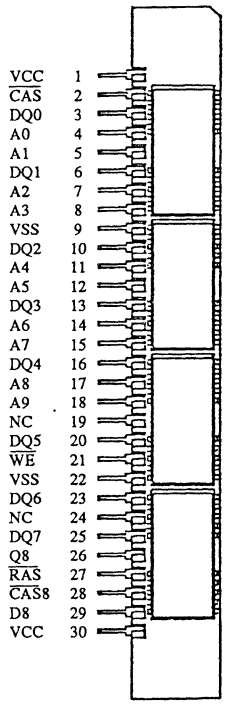
The Fujitsu MB85265 is a fully decoded, CMOS dynamic random access memory module consists of nine MB81C1000 devices, the MB85265 is optimized for those applications requiring high speed, high performance, large momory storage, and high density.



PLASTIC PACKAGE
MSP-30P-P07

- Organization : 1,048,576 words x 9 bit
- Memory : MB81C1000, 9 pcs
- $\overline{RAS}$ Access time (t RAC) :
  100ns max. (MB85265-10)
  120ns max. (MB85265-12)
- $\overline{CAS}$ Access time (t CAC) :
  30ns max. (MB85265-10)
  35ns max. (MB85265-12)
- Column Address Access time (t AA) :
  100ns max. (MB85265-10)
  120ns max. (MB85265-12)
- Fast Page Mode Cycle time (t PC) :
  60ns max. (MB85265-10)
  70ns max. (MB85265-12)
- Low power :
  Active 2970mW max. (MB85265-10)
  2475mW max. (MB85265-12)
  Standby 49.5mW max. (CMOS level)
  247.5mW max. (TTL level)
- Refresh :
  - 8.2ms / 512 refresh cycle
  - "$\overline{RAS}$-only", "$\overline{CAS}$-before-$\overline{RAS}$", and "Hidden" refresh capability
- Fast Page Mode Read and Write capability
- Decoupling Capacitor : 0.22µF, 9 pcs
- JEDEC Standard 30-pin SIP Package

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +7.0	V
Input Voltage	VIN	-3.5 to +7.0	V
Output Voltage	VOUT	-0.5 to + 7.0	V
Short Circuit Output Voltage	IOUT	±20	mA
Power Dissipation	PD	9.0	W
Temperature under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-45 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGES are exceeded. Functioncal operation should be restricted to the conditions as detailed in the operationcal sections of this data sheet. Exposure to absolute maximu rating conditions for exteded period may affect devise reliability.

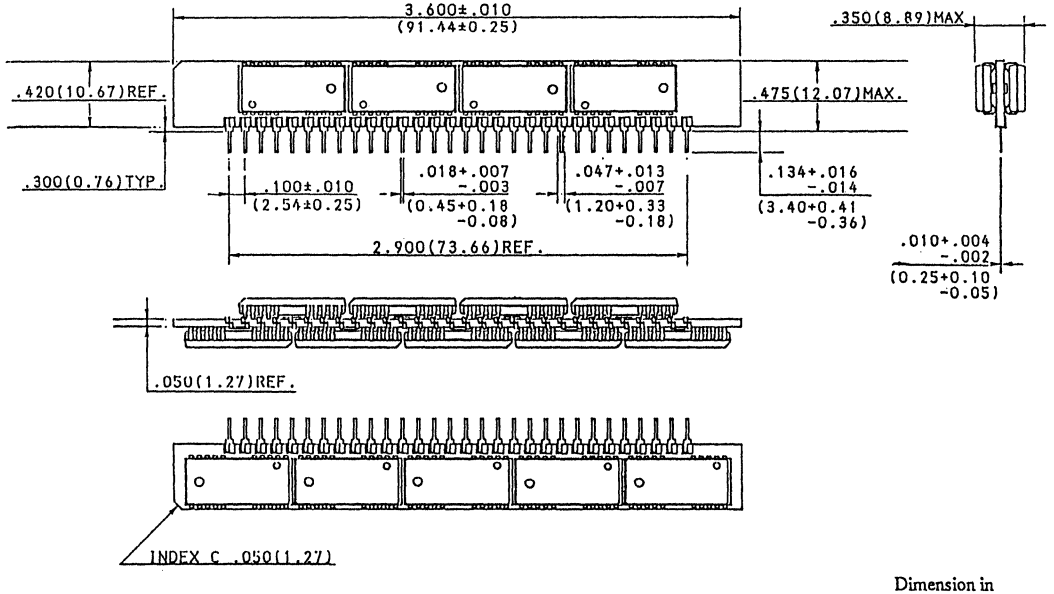
This device contains circuitry to protect the inputs against damage due to static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum reted voltages to this high impedance circuit.

5

PACKAGE DIMENSIONS

(Suffix : PJPS)

30-LEAD PLASTIC SINGLE IN-LINE PACKAGE MODULE
(CASE No.: MSP-30P-P07)



Dimension in
inches (millimeters)

5

Section 6

Quality and Reliability — *At a Glance*

Quality Control at Fujitsu

Built-in Quality and Reliability

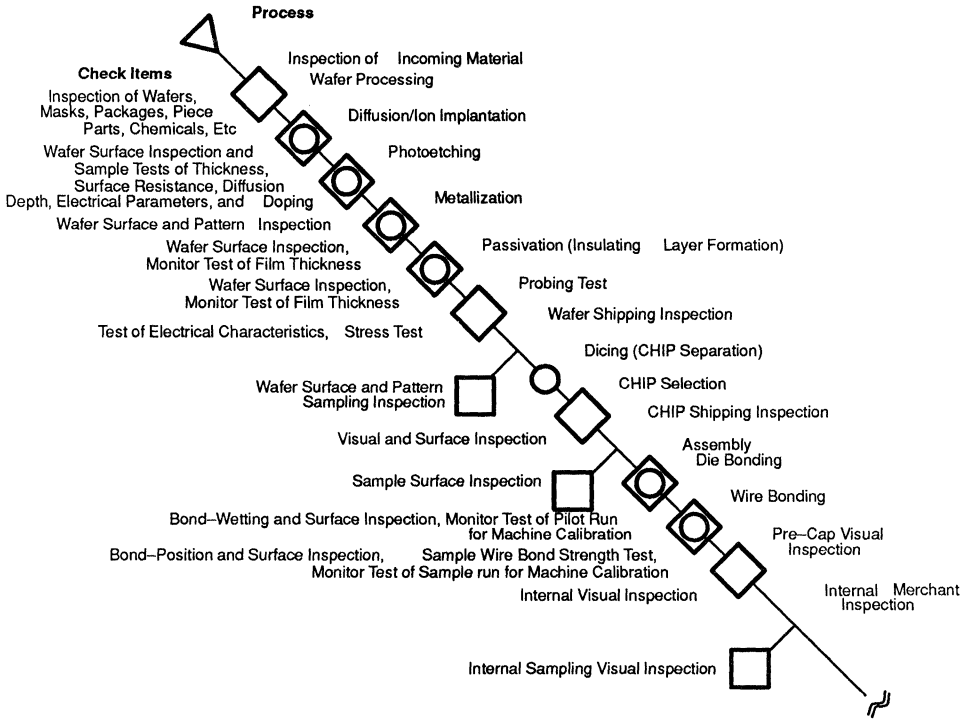
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

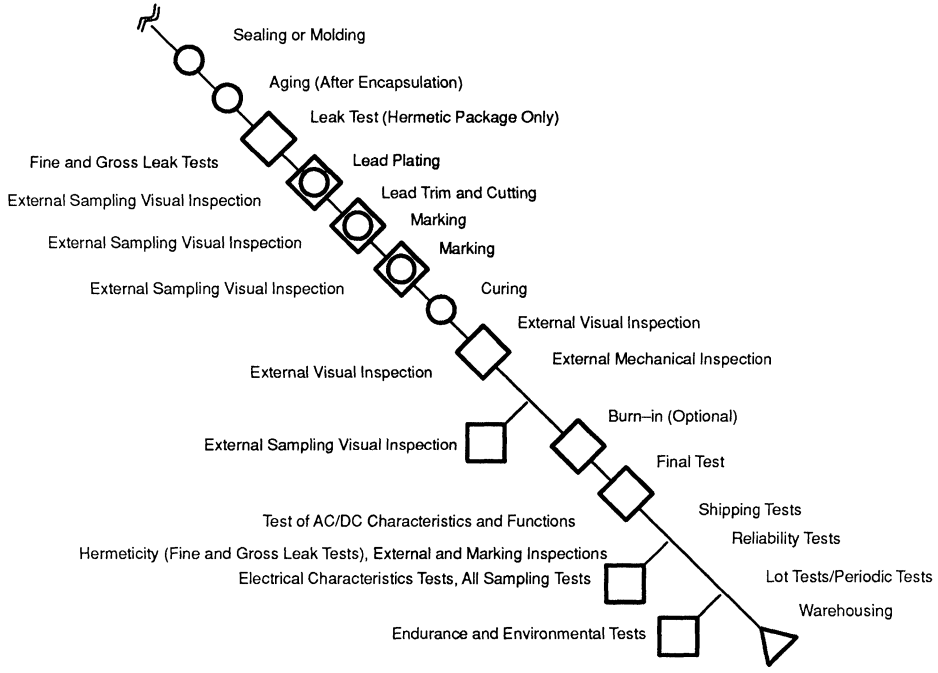
Quality Control Processes at Fujitsu



Continued on next page

6

Quality Control Processes at Fujitsu (Continued)



Legend:

- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

Note:
The flow sequence may vary slightly with individual product type.

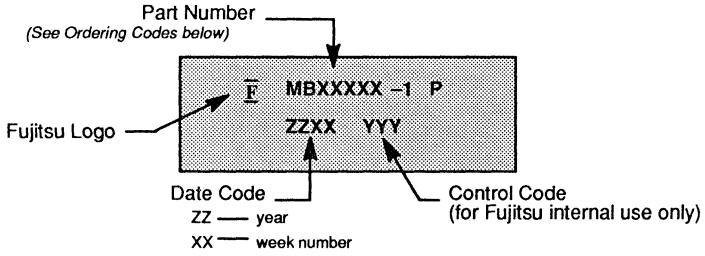
6

Section 7

Ordering Information — *At a Glance*

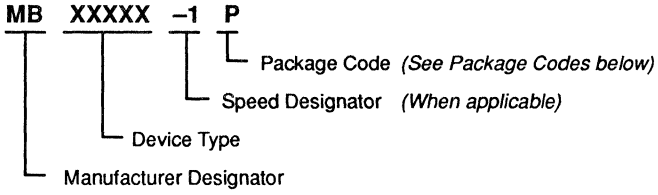
7

IC Product Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

IC Ordering Code (Part Number)



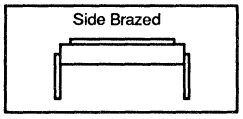
MB Identifies an IC designed and manufactured by Fujitsu that uses a Fujitsu-designated device number.
MBM Identifies an IC designed and manufactured by Fujitsu that uses a device number designated by the industry to be the industry standard number.
Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

IC Package Codes

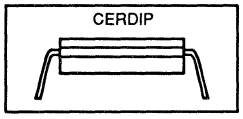
Ceramic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	TV,CV
PGA (Pin Grid Array)	CR
DIP (Side Brazed)[1]	C
DIP (CERDIP)[2]	Z
Shrink DIP	CSH
Flatpack, Metal Seal	CF
Flatpack, Glass Seal	ZF
SOJ (Single Outline Junction)	CJ

Plastic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	PV
PLCC (Leaded Chip Carrier)	PD
PGA (Pin Grid Array)	PR
DIP (Dual In-line Package)	P,M
Shrink DIP	PSH
Flatpack	PF
Single In-line, straight leads	PS
Single in-line, zig-zag leads	PSZ,PZ
SOJ (Single Outline Junction)	PJ

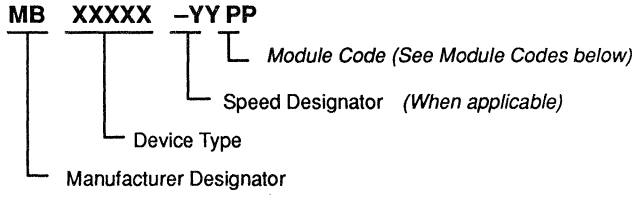
1 Side Brazed



2 CERDIP



IC Module Ordering Codes



MB Identifies an IC designed and manufactured by Fujitsu that uses a Fujitsu-designated device number.
MBM Identifies an IC designed and manufactured by Fujitsu that uses a device number designated by the industry to be the industry standard number.
Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

IC Module Package Codes

Ceramic	
Package Type	*Module Code*
Ceramic dual leads	CDL

Plastic	
Package Type	*Module Code*
Single in-line, leads	PL
Single in-line, zig-zag leads	PZ
Single in-line, pads	PS

7

Section 8

Sales Information — *At a Glance*

8

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to include one research and development division, two marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

- DRAMs and DRAM Modules
- EPROMs
- EEPROMs
- NOVRAMs
- CMOS masked ROMs
- CMOS SRAMs and CMOS SRAM Modules
- BiCMOS SRAMs
- Bipolar PROMs
- ECL RAMs
- STRAMs (self-timed RAM)
- Hi-Rel PROMs and SRAMs
- Ultra High-speed ECL/ECL—TTL Translator Circuits
- Linear ICs and Transistors

Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays
CMOS standard cells
Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

8

Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

8

SPARC™ is a trademark of Sun Microsystems, Inc.
Ethernet® is a registered trademark of Xerox Corporation.
EtherStar™ is a trademark of Fujitsu Microelectronics, Inc.
StarLAN™ is a trademark of AT&T.

Integrated Circuits Corporate Headquarters — Worldwide

International Corporate Headquarters

FUJITSU LIMITED
Marunouchi Headquarters
6–1, Marunouchi 1–chome
Chiyoda–ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781–22833
FAX: (03) 213-7174

For integrated circuits marketing information please contact the following:

Headquarters for Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6–1, Marunouchi 2–chome
Chiyoda–ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781–2224361
FAX: (03) 211-3987

Headquarters for North and South America

FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134–1804
USA
Tel: (408) 922–9000
Telex: 910–338–0190
FAX: (408) 432–9044

Headquarters for Europe

FUJITSU MIKROELEKTRONIK GmbH
Lyoner Strasse 44–48
Arabella Centre 9. OG
D–6000 Frankfurt 71
Federal Republic of Germany
Tel: (069) 66320
Telex: 441963
FAX: (069) 6632122

Headquarters for Asia and Australia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
06-04/06-07 Plaza by the Park
No. 51 Bras Basah Road
Singapore 0719
Tel: (65) 336–1600
Telex: 55573
FAX: (65) 336–1609

Fujitsu Microelectronics, Inc. (FMI) Sales Offices for *North and South America*

NORTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
10600 N. De Anza Blvd.
Suite 225
Cupertino, CA 95014
Tel: (408) 996–1600
FAX: (408) 725–8746

SOUTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
Century Centre
2603 Main Street
Suite 510
Irvine, CA 92714
Tel: (714) 724–8777
FAX: (714) 724–8778

GEORGIA (Atlanta)

Fujitsu Microelectronics, Inc.
3500 Parkway Lane
Suite 210
Norcross, GA 30092
Tel: (404) 449–8539
FAX: (404) 441–2016

ILLINOIS (Chicago)

Fujitsu Microelectronics, Inc.
One Pierce Place
Suite 910
Itasca, IL 60143–2681
Tel: (708) 250–8580
FAX: (708) 250–8591

MASSACHUSETTS (Boston)

Fujitsu Microelectronics, Inc.
75 Wells Avenue
Suite 5
Newton Center, MA 02159–3251
Tel: (617) 964–7080
FAX: (617) 964–3301

MINNESOTA (Minneapolis)

Fujitsu Microelectronics, Inc.
3460 Washington Drive
Suite 209
Eagan, MN 55122–1303
Tel: (612) 454–0323
FAX: (612) 454–0601

NEW JERSEY (Mt. Laurel)

Fujitsu Microelectronics, Inc.
Horizon Corporate Center
3000 Atrium Way
Suite 100
Mt. Laurel, NJ 08054
Tel: (609) 727–9700
FAX: (609) 727–9797

NEW YORK (Hauppauge)

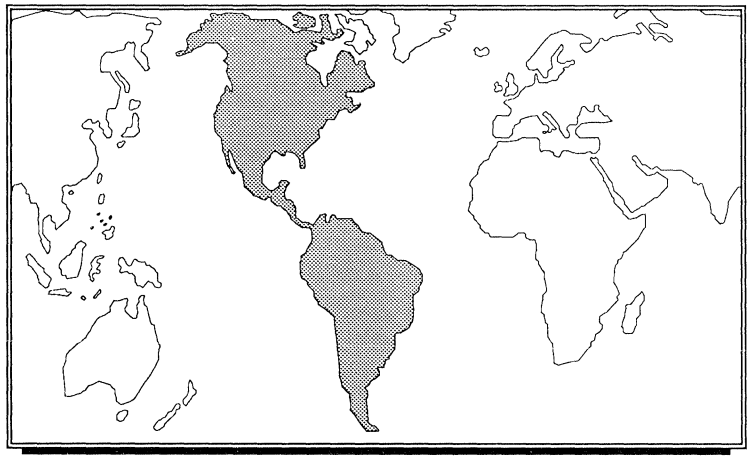
Fujitsu Microelectronics, Inc.
601 Veterans Memorial Highway
Suite P
Hauppauge, NY 11788–1054
Tel: (516) 361–6565
FAX: (516) 361–6480

OREGON (Portland)

Fujitsu Microelectronics, Inc.
5285 SW Meadows Road
Suite 222
Lake Oswego, OR 97035–9998
Tel: (503) 684–4545
FAX: (503) 684–4547

TEXAS (Dallas)

Fujitsu Microelectronics, Inc.
14785 Preston Road
Suite 670
Dallas, TX 75240
Tel: (214) 233–9394
FAX: (214) 386–7917



8

FMI Representatives — USA

For product information, contact your nearest Representative.

Alabama

The Novus Group, Inc.
2905 Westcorp Blvd.
Suite 120
Huntsville, AL 35805
Tel: (205) 534–0044
FAX: (205) 534–0186

Arizona

Aztech Component Sales Inc.
15230 N 75th Street
Suite 1031
Scottsdale, AZ 85260
Tel: (602) 991–6300
FAX: (602) 991–0563

California

Harvey King, Inc.
6393 Nancy Ridge Drive
San Diego, CA 92121
Tel: (619) 587–9300
FAX: (619) 587–0507

Infinity Sales, Inc.
4500 Campus Drive
Suite 300
Newport Beach, CA 92660
Tel: (714) 833–0300
FAX: (714) 833–0303

Norcomp
3350 Scott Blvd.,
Suite 24
Santa Clara, CA 95054
Tel: (408) 727–7707
FAX: (408) 986–1947

Norcomp
2140 Professional Drive
Suite 200
Roseville, CA 95661
Tel: (916) 782–8070
FAX: (916) 782–8073

Colorado

Front Range Marketing
3100 Arapahoe Road
Suite 404
Boulder, CO 80303
Tel: (303) 443–4780
FAX: (303) 447–0371

Connecticut

Conntech Sales, Inc.
182 Grand Street
Suite 318
Waterbury, CT 06702
Tel: (203) 754–2823
FAX: (203) 573–0538

Florida

Semtronic Associates, Inc.
657 Maitland Avenue
Altamonte Springs, FL 32701
Tel: (407) 831–8233
FAX: (407) 831–2844

Semtronic Associates, Inc.
1467 S. Missouri Avenue
Clearwater, FL 33516
Tel: (813) 461–4675
FAX: (813) 442–2234

Semtronic Associates, Inc.
3471 NW 55th Street
Ft. Lauderdale, FL 33309
Tel: (305) 731–2484
FAX: (305) 731–1019

Georgia

The Novus Group, Inc.
6115-A Oakbrook Pkwy
Norcross, GA 30093
Tel: (404) 263–0320
FAX: (404) 263–8946

Idaho

Cascade Components
2710 Sunrise Rim Road
Suite 130
Boise, ID 83705
Tel: (208) 343–9886
FAX: (208) 343–9887

Illinois

Beta Technology
1009 Hawthorn Drive
Itasca, IL 60143
Tel: (708) 256–9586
FAX: (708) 256–9592

Indiana

Fred Dorsey & Associates
3518 Eden Place
Carmel, IN 46032
Tel: (317) 844–4842
FAX: (317) 844–4843

Iowa

Electromec Sales
1500 2nd Avenue
Suite 205
Cedar Rapids, IA 52403
Tel: (319) 362–6413
FAX: (319) 362–6535

Maryland

Arbotek Associates
102 W. Joppa Road
Towson, MD 21204
Tel: (301) 825–0775
FAX: (301) 337–2781

Massachusetts

Mill–Bern Associates
2 Mack Road
Woburn, MA 01801
Tel: (617) 932–3311
FAX: (617) 932–0511

Michigan

Greiner Associates, Inc.
15324 E. Jefferson Avenue
Suite 12
Grosse Point Park, MI 48230
Tel: (313) 499–0188
FAX: (313) 499–0665

Minnesota

Electromec Sales
1601 E Highway 13
Suite 200
Burnsville, MN 55337
Tel: (612) 894–8200
FAX: (612) 894–9352

FMI Representatives — USA (Continued)

New Jersey

BGR Associates
Evesham Commons
525 Route 73
Suite 100
Marlton, NJ 08053
Tel: (609) 983–1020
FAX: (609) 983–1879

Technical Applications & Marketing
91 Clinton Road
Suite 1D
Fairfield, NJ 07006
Tel: (201) 575–4130
FAX: (201) 575–4563

New York

Quality Components
3343 Harlem Road
Buffalo, NY 14225
Tel: (716) 837–5430
FAX: (716) 837–0662

Quality Components
116 Fayette Street
Manlius, NY 13104
Tel: (315) 682–8885
FAX: (315) 682–2277

Quality Components
2318 Titus Ave.
Rochester, NY 14622
Tel: (716) 342–7229
FAX: (716) 342–7227

North Carolina

The Novus Group, Inc.
1026 Commonwealth Court
Cary, NC 27511
Tel: (919) 460–7771
FAX: (919) 460–5703

Ohio

Spectrum ESD
3947 Ray Court Road
Morrow, OH 45152
Tel: (513) 899–3260
FAX: (513) 899–3260

Spectrum ESD
8925 Galloway Trail
Novelty, OH 44072
Tel: (216) 338–5226
FAX: (216) 338–3214

Oregon

L–Squared Limited
15234 NW Greenbrier Pkwy
Beaverton, OR 97006
Tel: (503) 629–8555
FAX: (503) 645–6196

Texas

Technical Marketing, Inc.
3320 Wiley Post Road
Carrollton, TX 75006
Tel: (214) 387–3601
FAX: (214) 387–3605

Technical Marketing, Inc.
2901 Wilcrest Drive
Suite 139
Houston, TX 77042
Tel: (713) 783–4497
FAX: (713) 783–5307

Technical Marketing, Inc.
1315 Sam Bass Circle
Suite B–3
Round Rock, TX 78681
Tel: (512) 244–2291
FAX: (512) 338–1596

Washington

L–Squared Limited
105 Central Way
Suite 203
Kirkland, WA 98033
Tel: (206) 827–8555
FAX: (206) 828–6102

Wisconsin

Beta Technology
9401 W Beloit Street
Suite 304C
Milwaukee, WI 53227
Tel: (414) 543–6609
FAX: (414) 543–9288

FMI Representatives — Canada, Mexico and Puerto Rico

Canada

Pipe-Thompson Limited
5468 Dundas Street W.
Suite 206
Islington, Ontario M9B 6E3
Tel: (416) 236–2355
FAX: (416) 236–3387

Pipe-Thompson Limited
RR2 North Gower
Ottawa, Ontario K0Z 2T0
Tel: (613) 258–4067
FAX: (613) 258–7649

Mexico

Solano Electronica
Ermita 1039-10
Colonia Chapalita
Guadalajara, JAL. 45042
Tel: (36) 47–4250
FAX: (36) 473433

Solano Electronicas
Thiers 100
Colonia Anzures
Mexico City, D.F. 11590
Tel: (55) 31–5915
FAX: (55) 31–5915

Puerto Rico

Semtronic Associates
Mercantil Plaza Building
Suite 816
Hato Rey, Puerto Rico 00918
Tel: (809) 766–0700

FMI Distributors — USA

Alabama

Marshall Industries
3313 S. Memorial Highway
Suite 121
Huntsville, AL 35801
(205) 881–9235

Repton Electronics
4950 Corporate Drive
Suite 105C
Huntsville, AL 35805
(205) 722–9565

Arizona

Insight Electronics
1515 W. University Drive
Suite 103
Tempe, AZ 85281
(602) 829–1800

Sterling Electronics
3501 E. Broadway Road
Phoeniz, AZ 85040
(602) 268–2121

Marshall Industries
9830 S. 51st Street
Suite B121
Phoenix, AZ 85044
(602) 496–0290

California

Insight Electronics
28035 Dorothy Drive
Suite 220
Agoura, CA 91301
(818) 707–2100

Insight Electronics
15635 Alton Parkway
Suite 120
Irvine, CA 92718
(714) 727–2111

Insight Electronics
6885 Flanders Drive
Suite G
San Diego, CA 92126
(619) 587–9757

Marshall Industries
9710 Desoto Ave.
Chatsworth, CA 91311
(818) 407–4100

Marshall Industries
9674 Telstar Ave.
El Monte, CA 91731
(818) 459–5500

Marshall Industries
One Morgan
Irvine, CA 92718
(714) 458–5308

Marshall Industries
336 Los Coches Street
Milpitas, CA 95035
(408) 942–4600

Marshall Industries
3039 Kilgore Ave.
Rancho Cordova, CA 95670
(916) 635–9700

Marshall Industries
10105 Carroll Canyon Road
San Diego, CA 92131
(619) 578–9600

Merit Electronics
2070 Ringwood Avenue
San Jose, CA 95131
(408) 434–0800

Sterling Electronics
55310 Derry
Unit X
Agoura, CA 91301
(818) 707–0911

Sterling Electronics
9410 Topanga Canyon Rd.
Chatsworth, CA 91311
(818) 407–8850

Sterling Electronics
1342 Bell Avenue
Tustin, CA 92680
(714) 259–0900

Western Microtechnology
28720 Roadside Dr.
Suite 175
Agoura Hills, CA 91301
(818) 356–0180

Western Microtechnology
1637 North Brian
Orange, CA 92667
(714) 637–0200

Western Microtechnology
6837 Nancy Ridge Drive
San Diego, CA 92121
(619) 453–8430

Western Microtechnology
12900 Saratoga Ave.
Saratoga, CA 95070
(408) 725–1660

Colorado

Marshall Industries
12351 N. Grant Road
Suite A
Thornton, CO 80241
(303) 451–8383

Sterling Electronics
8200 South Akron Street
Suite 111
Englewood, CO 80112
(303) 792-3939

Connecticut

Marshall Industries
20 Sterling Drive
Wallingford, CT 06492
(203) 265–3822

Milgray Electronics
326 W. Main Street
Milford, CT 06460
(203) 795–0711

Western Microtechnology, Inc.
731 Main Street
Suite B2
Lantern Ridge Monroe, CT 06468
(203) 452-0533

Florida

Marshall Industries
380 S. Northlake Blvd
Suite 1024
Altamonte Springs, FL 32701
(407) 767–8585

Marshall Industries
2700 W. Cypress Creek Rd.
Suite C 106
Ft. Lauderdale, FL 33309
(305) 977–4880

Marshall Industries
2840 Sherer Drive
St. Petersburg, FL 33716
(813) 573–1399

Milgray Electronics
1850 Lee Road
Suite 104
Winter Park, FL 32789
(407) 647–5747

FMI Distributors — USA (Continued)

Florida (Continued)

Reptron Electronics
33320 N.W. 53rd Street
Suite 206
Ft. Lauderdale, FL 33309
(305) 735–1112

Reptron Electronics
14501 McCormick Drive
Tampa, FL 33626
(813) 855–2351

Georgia

Marshall Industries
5300 Oakbrook Pkwy
Suite 146
Norcross, GA 30093
(404) 923–5750

Georgia

Milgray Electronics
3000 Northwoods Parkway
Suite 270
Norcross, GA 30071
(404) 446–9777

Reptron Electronics
3040 H Business Park Drive
Norcross, GA 30071
(404) 446–1300

Illinois

Classic Components
3336 Commercial Ave.
Northbrook, IL 60062
(312) 272–9650

Marshall Industries
50 E. Commerce Dr.
Suite I
Schaumburg, IL 60173
(312) 490–0155

Milgray Electronics
3223 N. Wilkey Road
Arlington Heights, IL 60004
(312) 253–1573

Reptron Electronics
1000 E. State Hwy
Suite K
Schaumburg, IL 60173
(312) 882–1700

Indiana

Marshall Industries
6990 Corporate Drive
Indianapolis, IN 46278
(317) 297–0483

Kansas

Marshall Industries
10413 W. 84th Terrace
Lenexa, KS 66214
(913) 492–3121

Milgray Electronics
6901 W. 63rd Street
Overland Park, KS 66202
(913) 236–8800

Maryland

Marshall Industries
2221 Broadbirch
Suite G
Silver Springs, MD 20910
(301) 622–1118

Milgray Electronics
9801 Broken Land Parkway
Columbia, MD 21045
(301) 995–6169

Vantage Components, Inc.
6925-R Oakland Mills Road
Columbia, MD 21045
(301) 720–5100

Massachusetts

Interface Electronic Corp.
228 South Street
Hopkinton, MA 01748
(617) 435–6858

Marshall Industries
33 Upton Drive
Wilmington, MA 01887
(508) 658–0810

Milgray Electronics
187 Ballardvale Street
Wilmington, MA 01887
(508) 657–5900

Vantage Components, Inc.
200 Bulfinch Drive
Andover, MA 01810
(508) 687-3900

Western Microtechnology
20 Blanchard Road
9 Corporate Place
Burlington, MA 01803
(617) 273–2800

Michigan

Marshall Industries
31067 Schoolcraft Rd.
Livonia, MI 48150
(313) 525–5850

Michigan

Reptron Electronics
34403 Glendale
Livonia, MI 48150
(313) 525–2700

Minnesota

Marshall Industries
3955 Annapolis Lane
Plymouth, MN 55447
(612) 559–2211

Reptron Electronics
5929 Baker Road
Minnetonka, MN 55345
(612) 938–0000

Missouri

Marshall Industries
3377 Hollenberg Drive
Bridgeton, MO 63044
(314) 291–4650

New Jersey

Marshall Industries
101 Fairfield Road
Fairfield, NJ 07006
(201) 882–0320

Marshall Industries
158 Gaither Drive
Mt. Laurel, NJ 08054
(609) 234–9100

Milgray Electronics
3002 Greentree Exec. Campus
Suite B
Marlton, NJ 08053
(609) 983–5010

Vantage Components, Inc.
23 Sebago Street
P.O. Box 2939
Clifton, NJ 07013
(201) 777–4100

Western Microtechnology, Inc.
387 Passaic Avenue
Fairfield, NJ 07006
(201) 882-4999

New Mexico

Sterling Electronics
3450-D Pan American Freeway
Albuquerque, NM 87107
(505) 884-1900

FMI Distributors — USA (Continued)

New York

Marshall Industries
275 Oser Avenue
Hauppauge, NY 11788
(516) 273–2424

Marshall Industries
129 Brown Street
Johnson City, NY 13790
(607) 798–1611

New York

Marshall Industries
1280 Scottsville Road
Rochester, NY 14624
(716) 235–7620

Mast Distributors
95 Oser Avenue
P.O. Box 12248
Hauppauge, NY 11788
(516) 273–4422

Micro Genesis
90–10 Colin Drive
Holbrook, NY 11741
(516) 472–6000

Milgray Electronics
77 Schmitt Blvd.
Farmingdale, NY 11735
(516) 420–9800

Milgray Electronics
1200 A Scottsville Rd.
Rochester, NY 14624
(716) 235–0830

Vantage Components, Inc.
1041-G West Jericho Turnpike
Smithtown, NY 11787
(516) 543–2000

North Carolina

Marshall Industries
5224 Greens Dairy Road
Raleigh, NC 27604
(919) 878–9882

Reptron Electronics
5954-A Six Fork Road
Raleigh, NC 27609
(214) 783-0800

Ohio

Marshall Industries
3520 Park Center Drive
Dayton, OH 45414
(513) 898–4480

Marshall Industries
30700 Bain Bridge Road
Unit A
Solon, OH 44139
(216) 248–1788

Milgray Electronics
6155 Rockside Road
Cleveland, OH 44131
(216) 447–1520

Reptron Electronics
404 E. Wilson Bridge Road
Suite A
Worthington, OH 43085
(614) 436–6675

Oklahoma

Radio Inc.
1000 South Main
Tulsa, OK 74119
(918) 587–9123

Oregon

Marshall Industries
9705 S.W. Gemin Drive
Beaverton, OR 97005
(503) 644–5050

Western Microtechnology
1800 N.W. 169th Place
Suite B300
Beaverton, OR 97006
(503) 629–2082

Pennsylvania

Interface Electronic Corp.
7 Great Valley Parkway
Malvern, PA 19355
(215) 889-2060

Marshall Industries
701 Alpha Drive
Pittsburg, PA 15237
(412) 788–0441

Texas

Insight Electronics, Inc.
1778 Plano Road
Suite 320
Richardson, TX 75081
(214) 783–0800

Marshall Industries
8504 Cross Park Drive
Austin, TX 78754
(512) 837–1991

Marshall Industries
2045 Chenault
Carrollton, TX 75006
(214) 233–5200

Marshall Industries
2635 South Highway 77
Harlingen, TX 78550
(512) 421-4621

Marshall Industries
7250 Langtry
Houston, TX 77040
(713) 895–9200

Milgray Electronics
16610 N. Dallas Pkwy
Suite 1300
Dallas, TX 75248
(214) 248–1603

Reptron Electronics
3410 Midcourt
Carrollton, TX 75006
(214) 702-9373

Western Microtechnology, Inc.
18333 Preston Road
Suite 460
Dallas, TX 75252
(214) 248-3775

Western Microtechnology, Inc.
2500 Wilcrest, 3rd Floor
Houston, TX 77042
(713) 954-4850

FMI Distributors — USA (Continued)

Utah

Marshall Industries
466 Lawndale Drive
Suite C
Salt Lake City, UT 84115
(801) 485–1551

Milgray Electronics
4190 S. Highland Drive
Suite 102
Salt Lake City, UT 84124
(801) 272–4999

Washington

Insight Electronics, Inc.
12002 115th Avenue, NE
Kirkland, WA 98034
(206) 820-8100

Marshall Industries
11715 N. Creek Parkway
Suite 112
Bothell, WA 98011
(206) 486–5747

Western Microtechnology
14636 N.E. 95th Street
Redmond, WA 98052
(206) 881–6737

Wisconsin

Classic Components
2925 S. 160th Street
New Berlin, WI 53151
(414) 786–5300

Marsh Electronics
1563 S. 101st Street
Milwaukee, WI 53214
(414) 475–6000

Marshall Industries
20900 Swenson Drive
Suite 150
Waukesha, WI 53186
(414) 797–84004

FMI Distributors — Canada

British Columbia

ITT Industries
3455 Gardner Court
Burnaby, B.C. V5G 4J7
(604) 291–1227

Space Electronics
1695 Boundry Road
Vancouver, B.C. V5K 4X7
(604) 294–1166

Ontario

ITT Industries
300 North Rivermede Road
Concord, ON L4K 2Z4
(416) 736–1114

Marshall Industries
4 Paget Road
Unit 10 & 11
Framton, ON L6T 5G3
(416) 458–8046

Milgray Electronics
150 Consumers Road
Suite 502
Willowdale, ON M2J 4R4
(416) 756–4481

Quebec

Marshall Industries
3869 Sources Blvd
Suite 207
D.D.O., QUE H9B 2A2
(514) 683–9440

Space Electronics
5651 Rue Ferrier Street
Montreal, QUE H4P 2K5
(514) 697–8676

Fujitsu Mikroelektronik GmbH (FMG) Sales Offices for *Europe*

France

Fujitsu
Immeuble le Trident
3–5, Voie Felix Eboue
F–94024 Creteil Cedex
Tel: (1)4–207–8200
Telex: 262861
FAX: (1)4–207–7933

F.R. Germany

Fujitsu Mikroelektronik GmbH
Lyoner Strasse 44–48
Arabella Center 9. OG
D–6000 Frankfurt am Main 71
Tel: (69)66320
Telex: 411963
FAX: (69)66321

Fujitsu Mikroelektronik GmbH
Am Joachimsberg 10–12
D–7033 Herrenberg
Tel: (07032) 4085
FAX: (07032) 4088

Fujitsu Mikroelektronik GmbH
Carl-Zeiss-Ring 11
D-8045 Ismaning
bei Munchen
Tel: (89)960–9440
Telex: 8974464
FAX: (89)960–9442

Italy

Fujitsu Microelectronics
Italia S.R.L.
Centro Direzionale Milanofiori
Strada 4 – Palazzo A/2
I–20094 Milano
Tel: (39)(2)824–6170/176
Telex: 318546
FAX: (39)(2)824–6189

Netherlands

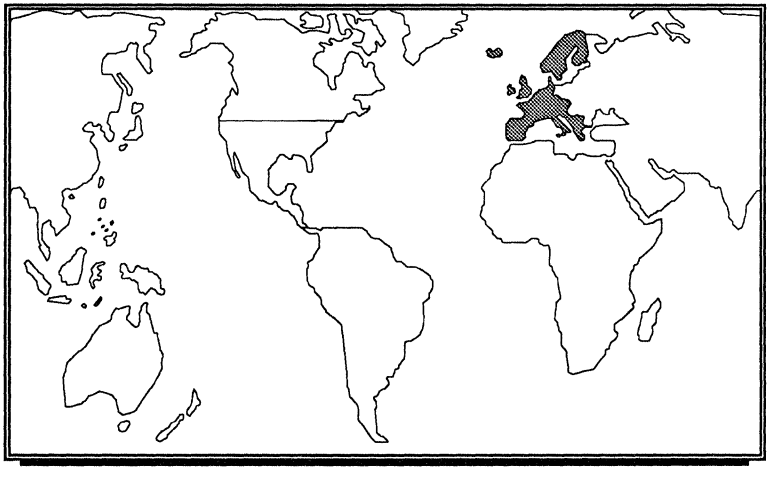
Fujitsu Benelux
Europalaan 6/B
5623 LJ Eindhoven
Tel: (31)44–7440
Telex: 59265
FAX: (31)44–4158

Sweden

Fujitsu Microelectronics Ltd.
Torggatan 8
17154 Solna
Tel: (8)764–6365
Telex: 13411
FAX: (8)28–0345

United Kingdom

Fujitsu Microelectronics Ltd.
Hargrave House
Belmont Road
Maidenhead
Berkshire SL6 6NE
Tel: (0628)76100
Telex: 848955
FAX: (0628)781484



FMG Distributors — Europe

Austria

Eljapex Handelsges. MBH
Eitnergasse 6
1232 Wien
Tel: (222)861531
Telex: 112344
FAX: (222)863211200

MHV/EBV Elektronik
Diefenbachgasse 35/6
1150 Wien
Tel: (222)838519
Telex: 134946
FAX: (222) 838530

Belgium

Eriat SA
83, Rue des Fraisiers
4410 Herstal Vottem
Tel: (41)271993
Telex: 41782
FAX: (41)278085

MHV/EBV Elektronik
Excelsiorlaan 35
Avenue Excelsion 35
1930 Zaventem
Tel: (2)7209936
Telex: 62590
FAX: (2)7208152

Denmark

Nordisk Elektronik AS
Transformervej 17
2730 Herlev
Tel: (2)842000
Telex: 35200
FAX: (2)921552

Finland

Gadelius OY
Kaupintie 18
00440 Helsinki
Tel: (90)5626644
Telex: 121274
FAX: (90)5626196

Aspecs OY
Myyrmaentie 2 A
01600 Vantaa
Helsinki
Tel: (90)5668686

France

D P A
12, Avenue des Pres
78180 Montigny le Bretonneux
Tel: (1)30575040
Telex: 689423
FAX: (1)30571863

Microram
6, Rue le Corbusier
Silic 424
94583 Rungis Cedex
Tel: (1)46868170
Telex: 2265909
FAX: (1)45605549

Germany

Eljapex GmbH
Felsenauerstr. 18
7890 Waldshut–Tiengen
Tel: (07751)2035
Telex: (07751)6603

Micro Halbleiter GmbH
Jagerweg 10
8012 Ottobrunn
Tel: (089)6096068
Telex: 5213807
FAX: (089)6093758

Italy

Unidis Group Bologna
Malpassi SRL
Via Baravelli, 1
40012 Calderara di Reno
Tel: (051)727252
Telex: 583118
FAX: (051)727515

Unidis Group Torino
PCM SnC
Via Piave 54/B
10099 Rivoli
Tel: (011)9532256
FAX: (011)9534238

Netherlands

MHV/EBV Elektronik
Planetenbaan 2
3606 AK–Maarssenbroek
Tel: (3465)62353
Telex: 76089
FAX: (3465)64277

P & T Electronics B.V.
Esse Baan 77
P.O. Box 329
2908 LJ Capelle A/D Ijssel
Tel: 104501444
Telex: 26096
FAX: 104507092

Norway

Odin Electronics AS
Postboks 72
Edv. Griegsvei 2
1472 Fjellhamar
Tel: (02)703730
Telex: 19732
FAX: (02)700310

Republic of Ireland

Allied Semiconductors International Ltd.
Unit 1
Distribution Park
Shannon Industrial Estate
Shannon
Co. Clare
Tel: (61)61777
Telex: 70358
FAX: (61)363141

FMG Distributors — Europe (Continued)

Spain

Comelta S.A.
Pedro IV–84, 5 Pl
08005 Barcelona
Tel: (93)3007712
Telex: 51934
FAX: (93)3005156

Comelta S.A.
Emilio Munoz 41
Nave 1–1–2
28037 Madrid
Tel: (1)7543001
Telex: 42007
FAX: (1)7542151

Sweden

Martinsson Elektronik AB
Box 9060
Instrumentvagen 16
12609 Hagersten
Tel: (8)7440300
Telex: 13077
FAX: (8)7443403

Switzerland

Eljapex AG
Hardstrasse 72
5430 Wettingen
Tel: (56)275777
Telex: 826300
FAX: (56)261486

United Kingdom

Hawke Components
Amotex House
45 Hanworth Road
Sunbury on Thames
Middlesex
TW16 5DA
Tel: (0197)97799
Telex: 923592
FAX: (9327)87333

Pronto Electronic Systems Ltd.
City Gate House
399/425 Eastern Avenue
Gants Hills
Ilford
Essex IG2 6LR
Tel: (15)546222
Telex: 8954213
FAX: (15)183222

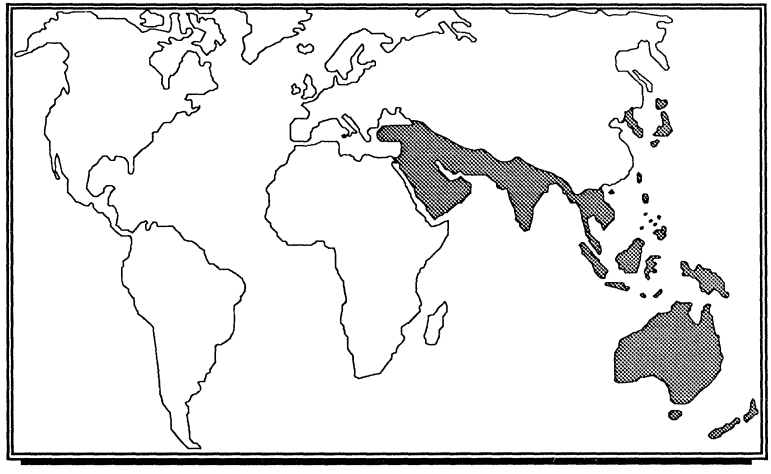
Fujitsu Microelectronics Asia PTE Limited (FMA) Sales Offices for *Asia and Australia*

Taiwan

Fujitsu Microelectronics Asia PTE Ltd.
1906 No. 333 Keelung Road Sec.1
Taipei, Taiwan 10548
Republic of China
Tel: (02) 757–6548
Telex: 17312 FMPTPI
FAX: (02) 757–6571

Singapore

Fujitsu Electronics PTE Ltd.
7500A Beach Road
05–301/2, The Plaza
Singapore 0719
Tel: (65) 296–1818
Telex: RS55573 FESPL
FAX: (65) 298–1571



FMA Representatives — Asia and Australia

Australia

Pacific Microelectronics
Unit A20, 4 Central Ave.
Thornleigh. NSW 2120
Australia
Tel: (2)481–0065
Telex: 24844460

Korea

KML Corporation
3RD/F, Bangbae Station Bldg.
981–15 Bangbae 3–Dong
Shucho–gu, Seoul
C.P.O. Box 7981
Korea
Tel: (2)588–2011/6
Telex: K25981 KMLCORP
FAX: (2)588–2017

FMA Distributors — Asia

Hong Kong

Famint Ltd.
Room 1502, No. 111 Leighton Road
Causeway Bay, Hong Kong
Tel: 5–760130 / 5–760146
FAX: 5–765619

Tektron Electronics Ltd.
1702, Bank Centre, 636 Nathan Road
Kowloon, Hong Kong
Tel: 3–880629
Telex: 38513 TEKHL
FAX: 123–40746 / 3–7234029

Singapore

Cony Electronics PTE Ltd.
10 Jalan Besar 03–25
Sim Lim Tower
Singapore 0820
Tel: 2962111
Telex: CONY RS34808
FAX: 2960339

Famint Electronics Ltd.
7500A Beach Road, 01/302
The Plaza
Singapore 0719
Tel: 2984566
Telex: RS37295 FAMINT
FAX: 2972597

Taiwan

Advance Microelectronics Co., Ltd.
5/F., No. 52 Tien Tsin Street
Taipei, Taiwan
Republic of China
Tel: (02) 5613361
Telex: 12284 ADVMICRO
FAX: (02) 5635958

Fametech Inc.
2/F, No. 298, Sec. 5
Nanking E. Road
Taipei, Taiwan,
Republic of China
Tel: (02) 7670101
Telex: 27271 COMMOTEK
FAX: (02) 7617743

Famint Co., Ltd.
Room 9–3, 9/F. No. 106 Sec. 2
Chang An East Road
Taipei, Taiwan
Republic of China
Tel: (02) 5051963
FAX: (02) 5080385

Section 9

Design Information — *At a Glance*

Appendix

Application Note

November 1989
Edition 1.1

FUJITSU

APPLICATION NOTE

Dynamic RAMs

Various Features of Fujitsu DRAMs

Applications Engineering Department
Fujitsu Microelectronics, Inc.
Integrated Circuits Division

Abstract

DRAMs are not only becoming denser, but also increasingly varied in scope. This note comprehensively describes the assorted features and various refresh modes available in Fujitsu DRAMs. Also discussed are standard memory board design tips and a 32-bit microprocessor application.

Circuit diagrams using Fujitsu products are included to illustrate typical semiconductor applications. Information sufficient for construction purposes may not be shown.

The information contained in this document has been carefully checked and is believed to be reliable. However, Fujitsu Microelectronics, Inc. assumes no responsibility for inaccuracies.

The information conveyed in this document does not convey any license under the copyrights, patent rights or trademarks claimed and owned by Fujitsu Limited, its subsidiaries, or Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. reserves the right to change products or specifications without notice.

This document is published by the Publications Department, Fujitsu Microelectronics, Inc.,
3545 North First Street, San Jose, California, U.S.A. 95134–1804; U.S.A.

Printed in the U.S.A.

Edition 1.1

Contents

Illustrations

Figures **Page**

Tables **Page**

Introduction

DRAMs are almost as old as the first microprocessor-based computers, yet new features are continually being introduced to DRAM technology. This publication consolidates and explains many of the various features found on present day DRAMs. Although all these features are not found on a single DRAM, they are available in Fujitsu's extensive DRAM family.

DRAM Features

Fast Page Mode

Fast page mode (also known as ripple mode) is a unique mode designed to decrease power consumption and access times between memory read or write cycles. Quick access to different columns in the same row is accomplished by keeping the Row Address Strobe ($\overline{RAS}$) low throughout the operation. Then a new column address is applied and the Column Address Strobe ($\overline{CAS}$) is brought low and valid data is either read from or written to the memory cell depending upon the value of the Write Enable ($\overline{WE}$). $\overline{CAS}$ is then brought high and a new address is applied. $\overline{CAS}$ is again brought low to latch the address. A timing diagram for the CMOS 1-megabit DRAM (MB81C1000) is shown in Figure 1.

Nibble Mode

Nibble mode allows high-speed reading and writing of data. An example of 1-megabit DRAM address generation using nibble mode is shown in Table 1 where the starting address is 0. The procedure represented by this table is to access a memory cell, either in the normal read or write manner, then to toggle $\overline{CAS}$ which enables an internal address generator that automatically sets row address (RA)9 to high (1) yet leaves all other bits unchanged. By toggling $\overline{CAS}$ once more the internal address generator causes RA9 to go to low (0) and column address (CA)9 to go to high (1). Another toggle of $\overline{CAS}$ causes RA9 to go to high (1) and CA9 to remain high (1). One last toggle of $\overline{CAS}$ causes RA9 and CA9 to return to their original state and the entire process repeats.

There are two advantages to using this method of internal address generation. The first advantage is that read/write cycle times are reduced to 50 ns (for Fujitsu's MB81C1001-80, a 1,048,576 x 1 bit Nibble Mode DRAM), which is faster than comparable DRAM cycle times by at least a factor of three. The second advantage is that the system chip count is reduced since there is no longer a need for external glue logic. One practical implementation of nibble mode is accomplished by grounding A9, thereby making RA9 and CA9 the least significant bits (LSBs) in an address. Once A9 is grounded, sequential memory accesses can be made simply by toggling $\overline{CAS}$.

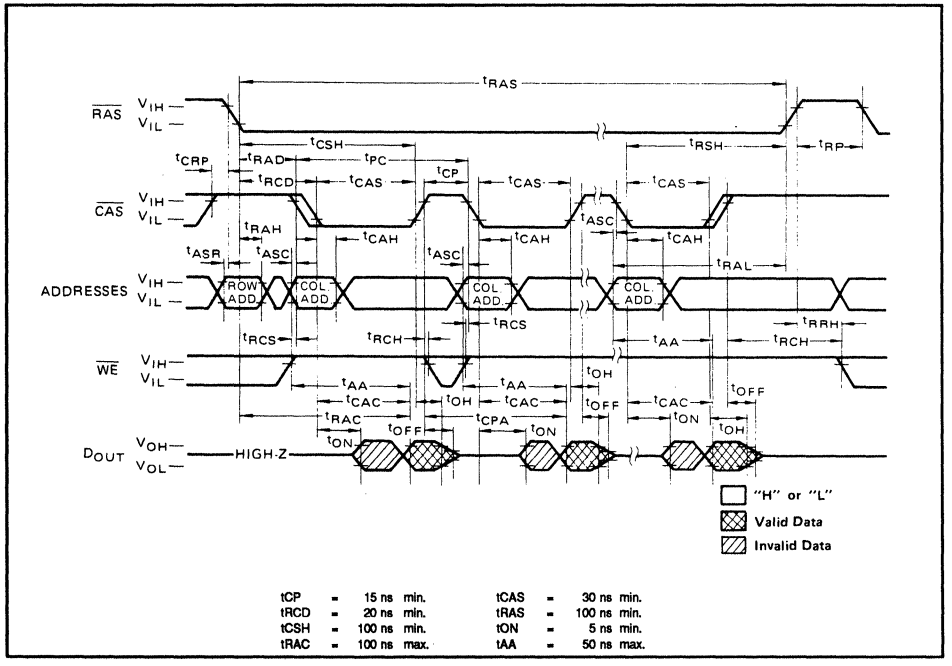


Figure 1. Fast Page Mode Read Cycle

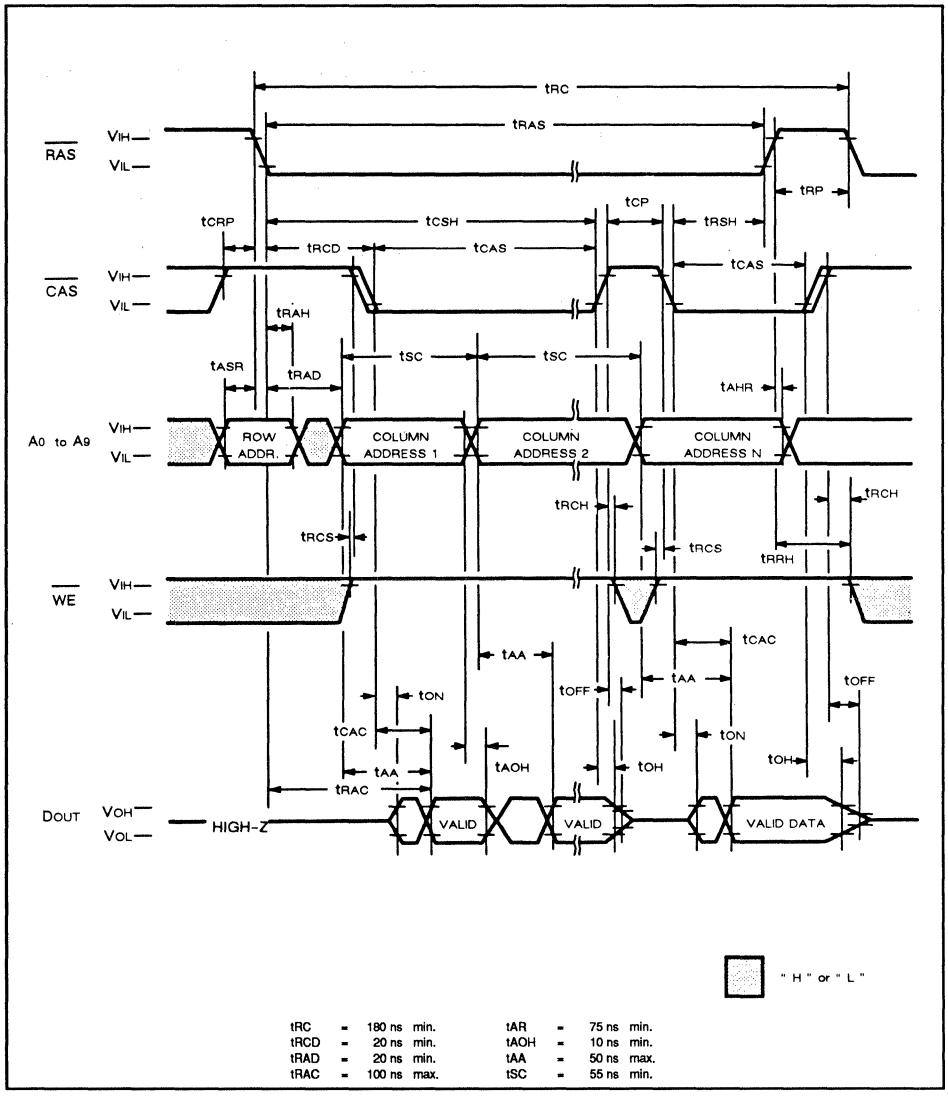
9

Table 1. Address Generation Using Nibble Mode

Sequence	Bit Accessed	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Normal $\overline{CAS}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{CAS}$	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$\overline{CAS}$	3	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
$\overline{CAS}$	4	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Normal $\overline{CAS}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Static Column Mode

A Static Column DRAM (SCRAM) offers a significant speed advantage. Sequential accesses are made in nearly 50 percent of the time it takes to make random accesses. A typical read/write cycle can be done in 55 ns (Fujtsu's MB81C1002-10, a 1,048,576 x 1 bit Static Column DRAM). This is the closest a DRAM comes to being operated as a less complex, fast SRAM. The procedure followed by a SCRAM is to apply a row address, latch it by dropping the $\overline{RAS}$ then apply a column address and latch it by dropping the $\overline{CAS}$. To access more column addresses there is no need to strobe a column address anymore. Instead, the new column address is applied at any time and new data becomes available after a short delay time (t_{AA}). To access any random column, apply the column address and the data appears after a short delay time. A comparison of static column mode versus fast page mode reveals that random column addresses for fast page mode are latched by dropping the $\overline{CAS}$, while column addresses for the static column mode are randomly applied while the $\overline{CAS}$ is low. See Figure 2 for a timing diagram.



tRC	= 180 ns min.		tAR	= 75 ns min.	
tRCD	= 20 ns min.		tAOH	= 10 ns min.	
tRAD	= 20 ns min.		tAA	= 50 ns max.	
tRAC	= 100 ns max.		tSC	= 55 ns min.	

Figure 2. Typical Static Mode Read Cycle

9

Comparison of DRAMs

Table 2 lists the specifications of the various DRAM features.

Table 2. Comparison of DRAMs

Type of DRAM	Mode Access Time (ns)	Cycle Time (ns)	Type of Access	Total Accessible Bits
Fast page mode (–80)	t_{cac} = 25 ns	t_{pc} = 55 ns	Random columns	1024
Nibble mode (–80)	t_{cac} = 25 ns	t_{nc} = 50 ns	Sequential columns	4
Static column mode (–80)	t_{AA} = 50 ns	t_{sc} = 55 ns	Random columns	1024

Internal DRAM Operation

To the average user, DRAMs are thought of as a simple storage device. However, DRAMs consist not only of storage capacitors but also internal decoders, sense amplifiers, buffers and address transition detectors (ATD). The following paragraphs will discuss DRAM inner circuitry in more detail.

Multiplexed Addressing

Present day DRAMs have exactly half the number of actual address pins needed to address all the words in the DRAM. Clever use of multiplexed address pins makes it possible to address 1 megabit of words with only 10 actual addresses in the pin assignment. This is accomplished by latching RA0 through RA9 (the row address) on the fall of the $\overline{RAS}$ and then applying new addresses to CA0 through CA9 (the column address) and latching them on the fall of the $\overline{CAS}$, thereby accessing 1 megabit of words by applying only 10 address lines at one time. This approach allows for more compact packages.

Word Line versus Bit Line

Even though a 1-megabit DRAM is physically arranged as 1024 rows and 1024 columns, for refresh purposes the operation is that of 512 rows and 2048 columns. This effectively halves the number of refresh cycles needed from 1024 to 512 thereby decreasing the amount of time the system wastes in refreshing.

A schematic of a single cell is given in Figure 3. Access to each cell in the DRAM is accomplished by connecting to one of 512 row lines (referred to as word lines), and to one of 2048 column lines (referred to as bit lines). The input row address is applied to a row decoder which selects one of the 512 rows. The input column address is applied to a column decoder which selects one of the 2048 columns. By this method one of the 1,048,576 storage cells is singled out.

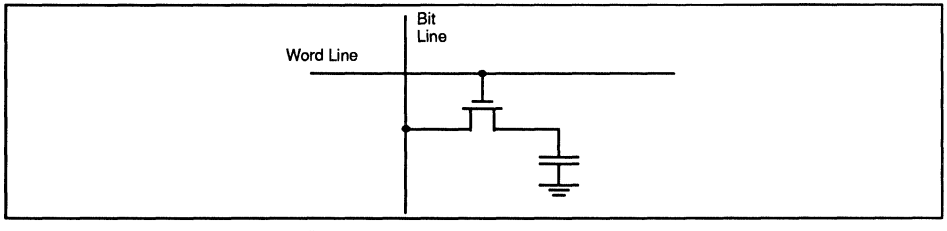


Figure 3. One Transistor (and One Capacitor) RAM Cell

Sense Amplifiers

Sense amplifiers are necessary to correctly read the stored value in each cell storage capacitor. Since each cell capacitance has a value in the femtofarad (10^{-15} farads) range, while the interconnecting lines have capacitance values in the picofarad (10^{-12} farads) range, it is not difficult to understand why the stored voltage can be corrupted by noise during transfer to the output buffers. This obstacle is overcome by comparing the stored or unstored charge to a known charge in a "dummy cell." Once the comparison is completed the output is amplified by the sense amplifiers resulting in better noise immunity.

Memory Board Design Rules of Thumb

Decoupling and Isolation Capacitors

An inherent system-level problem in DRAM designs is transient noise resulting from switching internal currents during refresh cycles. During refresh, DRAMs can require peak currents in the 50- to 100-mA range. Most of the instantaneous current demand is supplied by the decoupling capacitor. In addition to supplying instantaneous current, the capacitor must also meet the following requirements:

- Low inductance and low effective series resistance to minimize the voltage drop across the device. (These parameters are a function of the capacitor type.)
- A capacity to absorb the voltage bumps that occur due to fast edge rates during DRAM access.

Ceramic capacitors have been found to best meet the above requirements. Using a 0.22 µF decoupling capacitor for each DRAM in a 1-megabit application yields the following acceptable voltage undershoot for a 250 ns cycle:

$$V_{under} = (I * t)/C = (100\ mA * 250\ ns)/0.22\ \mu F = 114\ mV$$

Another necessary capacitor needed on a DRAM memory board is the isolation capacitor for the incoming main power bus. Since wiring from the power supply to the memory card can have significant resistance and inductance, which results in power supply ripple and noise, it is recommended that a 50- to 100-mF electrolytic capacitor be inserted.

Power Up Recommendations

DRAMs have historically needed multiple input voltages for substrate bias generation. Currently, all that is needed is 5 V because the substrate bias generator is internal to the chip. The bias generator takes approximately 200 ms to stabilize the substrate voltage hence it is recommended that the $\overline{CAS}$ and $\overline{RAS}$ be on high during this time period. There are two reasons for keeping the $\overline{RAS}$ and $\overline{CAS}$ high in a dense memory board. The first is that if the $\overline{RAS}$ and $\overline{CAS}$ were both low, the DRAMs would draw much larger currents, which could result in a system failure. The second reason is that all the DRAM output levels during power up are unknown, so if the $\overline{RAS}$ and $\overline{CAS}$ were low, there could be data contention in the case of wired AND outputs. However, if the $\overline{RAS}$ and $\overline{CAS}$ were high then the outputs would not conflict since they are guaranteed to be in the high-impedance state.

Once power up has been established, it is necessary to perform eight dummy cycles to stabilize the internal circuitry. The type of cycle (read, write, $\overline{CAS}$-before-$\overline{RAS}$, hidden refresh) required depends on

whether the internal refresh counter will be implemented or not. (Check the data sheet of the specific device.)

Undershoot and Ringing

Undershoot and ringing occur only when line voltages go from high to low or from low to high respectively and not during static state operation. Undershoot and ringing are caused by noise, inherent transistor switching characteristics, and mismatched impedances between the driver output, the signal line, and the load.

Undershoot and ringing due to mismatched impedances can be effectively eliminated by understanding their cause and implementing good design techniques. In present high-frequency applications, line impedance is a function of line capacitance and line inductance is as given by the following equation:

$$Z = (L/C)^{1/2}$$

There is approximately 10 nH of inductance per inch in a 13-mil wide trace. Similarly, there is approximately 4 pF of capacitance per inch in a 13-mil wide trace. So it is easy to see how the impedance of traces can be 50 ohms.

From physics we know that if an initial voltage (Vo) meets a mismatch between the line impedance (Zo) and the load impedance (Zl), Vo will break into two separate components: transmitted voltage (Vt) and reflected voltage (Vr). The reflected voltage equation is as follows:

$$Vr = [Vo\ (Zl - Zo)]/(Zl + Zo)$$

When load impedance is equal to line impedance there is no reflected voltage wave. When there is mismatch between load and line impedance, the reflected wave causes oscillations in Vo resulting in ringing and undershoot.

The best way to prevent ringing and undershoot is to put a 20- to 30-ohm series damping resistor in all trace circuits to the DRAM. This generally decreases load and line impedance mismatch enough to significantly decrease undershoot and ringing.

The Difference Between Soft and Hard Errors

A soft error is a bit error that disappears when a system is rebooted. A hard error causes permanent damage to a particular cell, or group of cells, in a memory device. Consequently, random soft errors are much more difficult to trace and fix, whereas hard errors are only remedied by replacing the entire chip.

Soft Error Causes

There are two major causes of soft errors. The first cause is alpha particles emitted by radioactive impurities in memory component packages. The stray alpha particles cause ionization along their paths, thus changing the charge stored in the memory cell. The second cause of soft errors is internal noise in the die. Internal noise problems can only be eliminated by prudent and proven transistor design techniques such as those used by Fujitsu's Design Engineering Group in Kawasaki, Japan. Fujitsu has taken extensive steps to decrease soft errors due to alpha particles by implementing the following design techniques:

- Using metal bit lines which physically reduce the size of alpha particle-sensitive portions on the die.
- Applying a thin layer of polyamide (which is known to absorb alpha particles) to the die. For example, a 3.5-mil thick polyamide coating can stop most alpha particles from entering and corrupting cells.

Fujitsu has also designed and manufactured a full line of CMOS DRAMs since CMOS has better noise immunity and it is also inherently less prone to soft errors than NMOS.

The number of failures that can be expected due to soft and hard errors is minute. Table 3 displays the number of expected soft errors per device for a time period of one billion device hours. The industry nomenclature for device failures is failures in time (FITs).

Table 3. Failures Per Billion Device Hours

Fujitsu Device	Soft Errors
256 k DRAM	<500 FITs
1 Mbit DRAM	<1000 FITs
4 Mbit DRAM	<1000 (target) FITs

Hard Error Causes

Latchup

One of the disadvantages of CMOS is the inherent problem of latchup. Latchup occurs from parasitic bipolar actions and results in excessive current-sinking logic which destroys the device. Fujitsu reduces the possibility of latchup by using the following preventative measures:

- Incorporating substrate bias generators on the die so that uniform substrate potential of the transistors is maintained. This prevents the parasitic diodes from forward biasing (which would permit excess current to flow) when undershoot occurs.
- Clamping diodes on the inputs which prevents excessive undershoot voltages from occurring.

Electrostatic Discharge

Since MOS has high input impedance and low breakdown voltage, another inherent CMOS disadvantage is device sensitivity to electrostatic discharge (ESD). Fujitsu offers ESD protection in the thousands of volts range, in addition to undershoot and overshoot protection. The input protection circuitry for 1-megabit DRAMs is shown in Figure 4. Grounding any people or machinery that touch the device will nearly eliminate ESD failures.

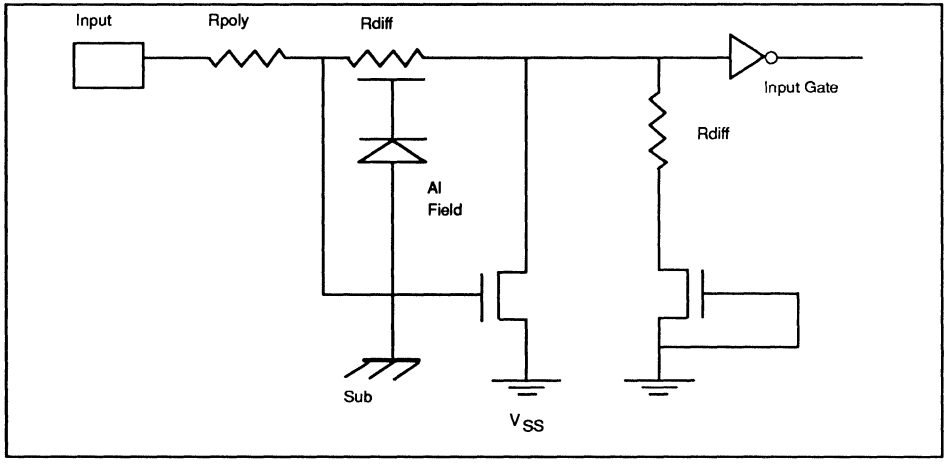


Figure 4. 1-megabit CMOS DRAM Input Protection Circuit

Dual-Port DRAMs

Since memory is inherently parallel and video data is inherently serial, graphics systems have always needed parallel-to-serial shift registers. The extra logic needed to perform graphics tasks increased delay times, used board space, and was not very efficient in high-end graphics applications. These drawbacks have completely vanished with the introduction of Dual-Port DRAMs.

Dual-Port DRAMs are designed to bridge the parallel-to-serial gap by having separate parallel and serial ports. This feature permits image memory to be updated while previous data is being shifted out to the display. The transfer of parallel data to serial data is accomplished by an on-board parallel-to-serial shift register. Conversely, because the serial port has its own clock, it is possible to load the serial port, then shift the data to the parallel access RAM. This type of data manipulation reduces the problem of bus contention especially apparent in display applications. In fact, the Dual-Port DRAM is almost exclusively used for video applications; it is also called a Video RAM.

Bit Masking

Bit masking is used to inhibit (mask) writing to certain bits of nibbles. It is found only in Dual-Port DRAMs where it is most useful in quickly manipulating and operating on individual pixel data.
The advantage of bit masking is that instead of doing a read-compare-modify-write cycle, only a masked write is necessary. The pins used in masking are $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ mask enable ($\overline{ME}$), masked data (MD) <0...3>/data out (DQ) <0...3>, and output enable ($\overline{OE}$). Figure 5 shows the timing for bit masking.

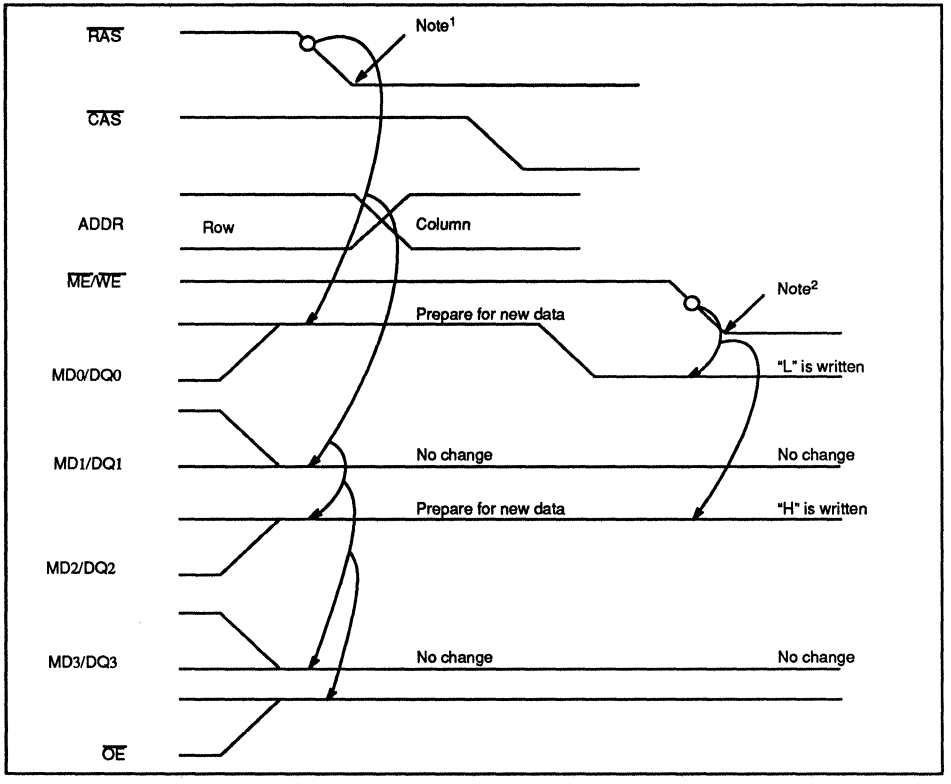


Figure 5. Bit Masking

Notes: [1]At the fall of $\overline{RAS}$ (and if $\overline{OE}$ = H and $\overline{ME}$ = H), all MD inputs that are high will be prepared to receive new data. MD inputs that are low at the fall of $\overline{RAS}$ will not be prepared to be rewritten.

[2]At the fall of $\overline{ME}$ the new data present on all MD pins that were high at the fall of $\overline{RAS}$ will be written to the appropriate bit of the memory.

9

DRAM Refresh Methods

DRAMs are basically made up of decoders, latches and capacitors. Capacitors store charges applied to them. Due to leakage, capacitors also dissipate that charge. Consequently, in order to retain their data, all DRAMs need to be periodically refreshed with a pulse to each cell. Methods of refreshing vary from device to device. Some of these methods are discussed in the following paragraphs.

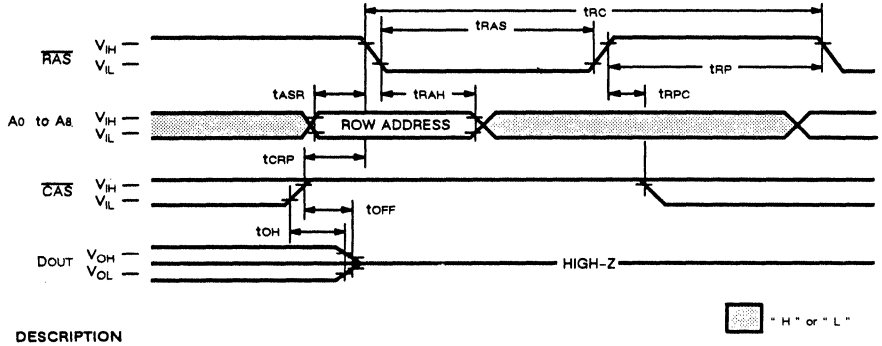
$\overline{RAS}$-Only Refresh

$\overline{RAS}$-only refresh causes the output buffer to remain in a high-impedance state until certain $\overline{RAS}$ and $\overline{CAS}$ timing parameters are met. This type of refresh cycle is ideal for wired-OR outputs. External glue logic

generates row addresses and timing parameters so that all rows are refreshed within the allotted refresh cycle time. Also, whenever a row is accessed for a read or write operation it is refreshed. A two-step process is required to refresh all the cells.

1. Initially the $\overline{RAS}$ and $\overline{CAS}$ are high. Then a row address is applied and the $\overline{RAS}$ is brought low, thereby refreshing all cells in that row.
2. After the $\overline{RAS}$ is brought high, a new row address is applied and the procedure repeats.

A timing diagram is shown in Figure 6.



DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DOUT pin is kept in a high-impedance state.

Figure 6. Typical $\overline{RAS}$-Only Refresh Cycle

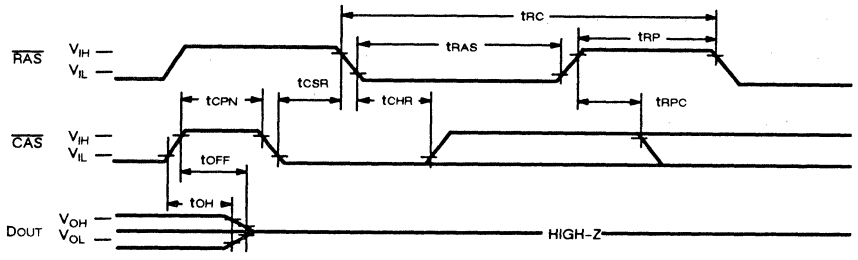
$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh eliminates the need for external logic to generate refresh addresses. When using the $\overline{CAS}$ before $\overline{RAS}$ refresh, a one-time start-up procedure must be undertaken enabling this feature and ensuring proper device operation. This procedure initializes the internal address generator.
One requirement of the procedure is that when power is applied, the $\overline{CAS}$ and $\overline{RAS}$ should be high. After power stabilization, the $\overline{CAS}$ should go low before the $\overline{RAS}$ goes low. This cycle has certain setup and hold time constraints, depending on the particular chip being used, but generally speaking at least eight $\overline{CAS}$ before $\overline{RAS}$ cycles must occur to initialize the internal counter.

Once this procedure is completed the normal $\overline{CAS}$ before $\overline{RAS}$ refresh operation is as follows:

1. The $\overline{CAS}$ is brought low then the $\overline{RAS}$ is brought low.
2. The refresh address is supplied by an internal address generator.

A timing diagram is shown in Figure 7.



DESCRIPTION

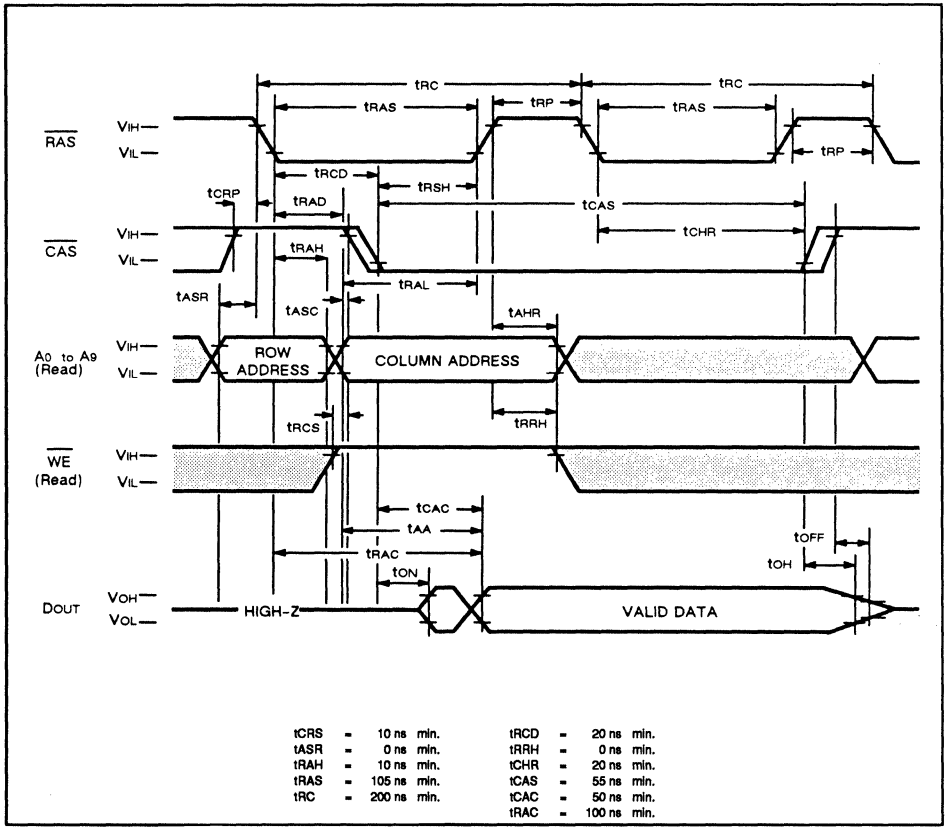
CAS-before-RAS refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If CAS is held Low for the specified setup time (tCSR) before RAS goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next CAS-before-RAS refresh operation.

tCHR	=	15 ns min.	tRAS	=	105 ns min.
tCSR	=	0 ns min.	tRC	=	200 ns min.
tOFF	=	25 ns max.	tRPC	=	20 ns min.

Figure 7. CAS Before RAS Refresh Cycle

Hidden CAS Before RAS On-Chip Refresh

Hidden CAS before RAS on-chip refresh is similar to a CAS before RAS refresh except that data remains valid on the data pins as long as the CAS is low. Because the internal address counter is used in this cycle, at least eight dummy CAS-before-RAS refresh cycles should occur immediately after power-up. For this type of refresh, keep the CAS low at the end of a normal read or read-write cycle, and then bring the RAS high, then back to low. Since data remains valid on the output until the CAS goes high, this cycle is an extended read or write cycle in the foreground and a "hidden" refresh cycle in the background. A timing diagram is shown in Figure 8.



tCRS	=	10 ns min.	tRCD	=	20 ns min.
tASR	=	0 ns min.	tRRH	=	0 ns min.
tRAH	=	10 ns min.	tCHR	=	20 ns min.
tRAS	=	105 ns min.	tCAS	=	55 ns min.
tRC	=	200 ns min.	tCAC	=	50 ns min.
			tRAC	=	100 ns min.

Figure 8. Typical Hidden $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

DRAM Implementation in an MBL80286 Environment

Figure 9 shows a typical implementation of an MBL80286 microprocessor, an MB1430A DRAM controller, an MBL82288 bus controller and several 1-megabit DRAMs. The memory is organized in two banks; one bank contains the data of odd addresses and the other bank contains the data of even addresses. This type of configuration is known as interleaving memory. The main advantage to such an organization is that while one bank of memory is in tRP (RAS precharge time) the second bank is accessed by the bus. Then, while the second bank is in tRP the first bank is accessed by the bus. This decreases the perceived DRAM cycle time. Interleaving memory is an optimum configuration as long as the same bank of memory cells doesn't need to be accessed sequentially.

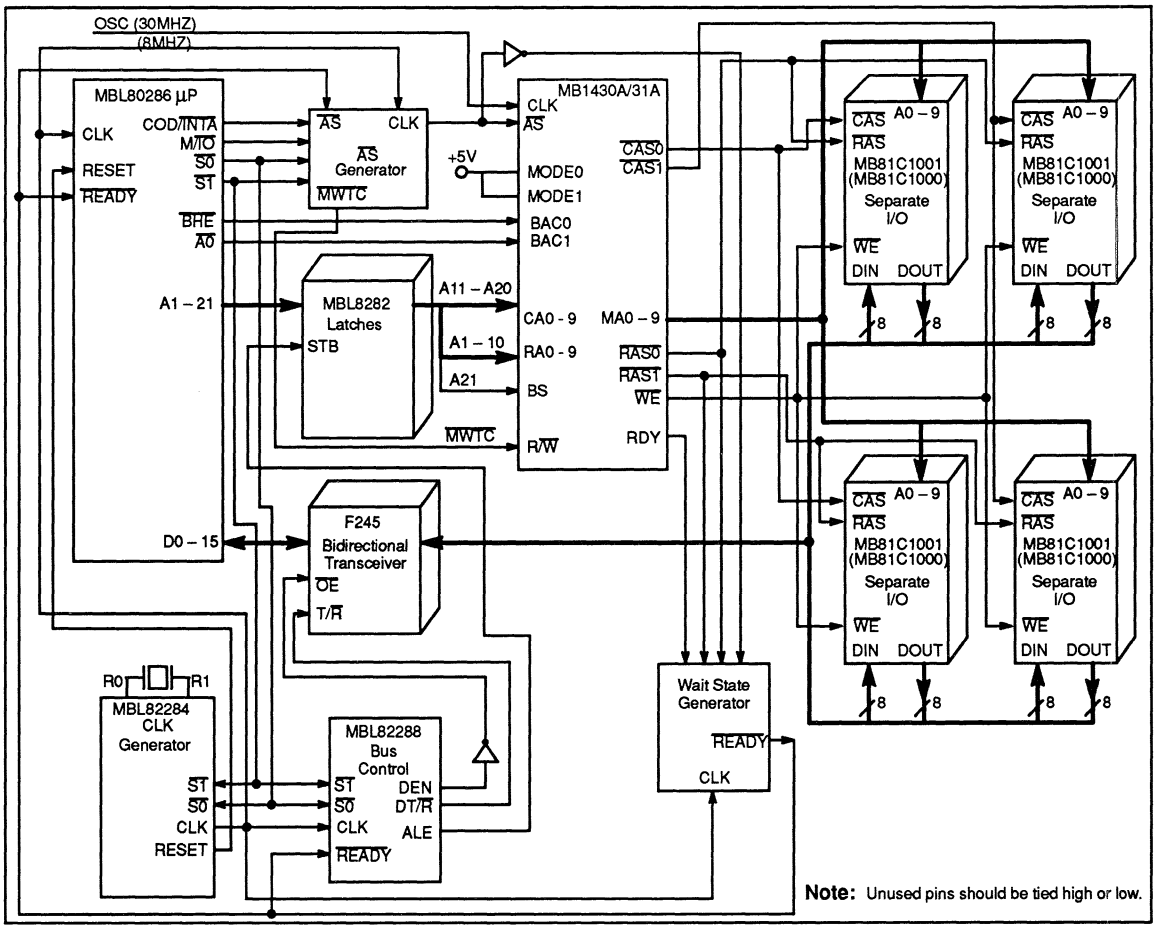


Figure 9. Schematic of 1 megabit x 32 DRAM with Zero Wait States

Figure 10 shows the RAS0 and RAS1 timing that allows interleaving. If the same bank is accessed sequentially then the microprocessor must generate wait states and endure the tRP. The odd or even bank is selected depending on the value of bus high enable ($\overline{BHE}$) and A0. The size of the operation taking place (word or byte) can also be determined by polling $\overline{BHE}$ and A0. This relationship is shown in Table 4.

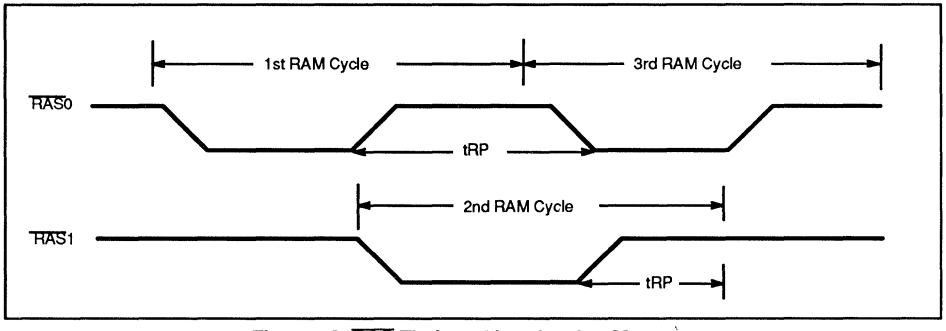


Figure 10. $\overline{RAS}$ Timing of Interleaving Memory

Table 4. Relationship Between $\overline{BHE}$, A0, and Size of Operation

$\overline{BHE}$	A0	Operation
0	0	Word Transfer
0	1	Byte Transfer on Upper Half of Data Bus (D15–D8)
1	0	Byte Transfer on Lower Half of Data Bus (D7–D0)
1	1	Reserved

The purpose of the octal latches in the Figure 9 schematic (MBL8282) is two-fold: first to demultiplex the address lines and secondly to increase the total drive capability to 32 mA. Once the address lines have been demultiplexed they become inputs to a DRAM controller. The DRAM controller generates the necessary $\overline{RAS}$ and $\overline{CAS}$ timing on the $\overline{RAS0}$, $\overline{CAS0}$, $\overline{RAS1}$, and $\overline{CAS1}$ lines. The MB1430A DRAM controller can accommodate various microprocessors including the Motorola 68000. In addition, the MB1430A can drive up to 44 DRAMs without the use of drivers.

The purpose of the bus transceivers in the Figure 9 schematic is two-fold: first to demultiplex the data lines from the multiplexed address-data lines, and secondly to allow microprocessor read-writes. In the case of a write operation, once the data has been demultiplexed it is put through a bidirectional bus driver which allows data to be read and increases the drive capability. The direction of data flow is determined by the data transmit/receive (DT/$\overline{R}$) pin. The bus controller in the Figure 9 schematic orchestrates the entire system under the control of the microprocessor, MBL80286. The signals output by the microprocessor determine the operation taking place (see Table 5).

Table 5. MBL80286 Bus Cycle Status Definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0 (low)	0	0	0	Interrupt Acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None: Not a Status Cycle
0	1	0	0	If A1 = 1 Then Halt; Else Shutdown
0	1	0	1	Memory Data Read
0	1	1	0	Memory Data Write
0	1	1	1	None: Not a Status Cycle
1 (high)	0	0	0	Reserved
1	0	0	1	I/O Read
1	0	1	0	I/O Write
1	0	1	1	None: Not a Status Cycle
1	1	0	0	Reserved
1	1	0	1	Memory Instruction Read
1	1	1	0	Reserved
1	1	1	1	None: Not a Status Cycle

DRAM Modules

DRAM modules are dense memory packages that are a fraction of the size of the same memory structure in a board design. Some of the common module sizes are 1M x 9, 256 k x 9, and 16 k x 32.

Summary

Fujitsu DRAMs offer a selection of features that include: fast page mode, nibble mode, and static column mode. Fujitsu also manufactures dual-port DRAMs and DRAM modules.

References

Fujitsu Microelectronics, Inc. *8/16-Bit Microprocessors Microcomputers Peripherals*, 1987 Data Book. Tokyo, Japan: Fujitsu Limited; San Jose, CA: Fujitsu Microelectronics, Inc., 1986.

___. *Memories*, 1986-87 Data Book. Tokyo, Japan: Fujitsu Limited; San Jose, CA: Fujitsu Microelectronics, Inc., 1986.

Iqbal, Mohammad S. *Effects of Soft Errors on Bipolar and MOS Memories.* Application Note. San Jose, CA: Fujitsu Microelectronics, Inc., 1989.

Sedra, Adel S. and Kenneth C. Smith. *Microelectronic Circuits.* New York: CBS College Publishing, 1982.

Stone, Harold S. *Microcomputer Interfacing.* Reading, Massachusetts: Addison-Wesley Publishing Company, 1982.

Notes

Notes

Notes

FUJITSU LIMITED

Marunouchi Headquarters
6-1, Marunouchi 1-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: (03) 216-3211
Telex: 781-22833
FAX: (03) 213-7174

For further information, please contact:

Japan

FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6-1, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: (03) 216-3211
Telex: 781-2224361
FAX: (03) 211-3987

Europe

FUJITSU MIKROELEKTRONIK GmbH
Lyoner Strasse 44-48
Arabella Centre 9. 0G
D-6000 Frankfurt 71
Federal Republic of Germany
Tel: (49) (069) 66320
Telex: 441-963
FAX: (069) 663-2122

Asia

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
06-04/06-07 Plaza By the Park
No. 51 Bras Basah Road
Singapore
Tel: (65) 336-1600
Telex: 55573
FAX: (65) 336-1609

North and South America

FUJITSU MICROELECTRONICS, INC.
Integrated Circuits Division
3545 North First Street
San Jose, CA 95134-1804 USA
Tel: (408) 922-9000
Telex: 910-338-0190
FAX: (408) 432-9044

Printed in USA OV0212-901F1